"Analysis and Design of CMOS Comparator based on g_m/I_d approach for CBSC circuits"

Thesis submitted in the partial fulfillment of requirement

for the award of degree of

Master of Technology

in

VLSI Design

Submitted by:

Abhishek Patyal

Roll No: 601061002

Under the guidance of:

Mr. Rishikesh Pandey

Assistant Professor

ELECTRONICS AND COMMUNICATION ENGINEERING DEPARTMENT

THAPAR UNIVERSITY

(Established under the section 3 of UGC Act, 1956)

PATIALA – 147004 (PUNJAB)

DECLARATION

I hereby declare that the thesis report entitled **"Analysis and Design of CMOS Comparator based on g_m/I_d approach for CBSC circuits"** is an authentic record of my own work carried out as requirement for the award of **Master of Technology in VLSI Design & CAD at Thapar University, Patiala** under the guidance of Mr. Rishikesh Pandey, Assistant Professor, ECED.

The matter embedded in this thesis has not been submitted in any other University/Institute for the award of any degree.

Abhishek Patyal

Date: 11-07-2012

Abhishek Patyal

601061002

It is certified that the above statement made by candidate is correct to the best of my knowledge and belief.

Mr. Rishikesh Pandey
Assistant Professor
Thapar University, Patiala

Countersigned by:

Head
Electronics & Communication
Engineering Department
Thapar University, Patiala

Dean of Academic Affairs
Thapar University, Patiala

ACKNOWLEDGEMENT

First of all, I would like to express my gratitude to Mr. Rishikesh Pandey, Assistant Professor, Electronics & Communication Engineering Department, Thapar University, Patiala for his guidance and support throughout this thesis work. I am really very fortunate to have the opportunity to work with him.

I am also thankful to the Head of Department, Professor (Dr.) Rajesh Khanna and PG Coordinator, Dr. Kulbir Singh (Associate Professor) of Electronics & Communication Engineering Department for their encouragement and inspiration for the execution of this thesis work.

I am also thankful to the entire faculty and staff of Electronics & Communication Engineering Department for the help and moral support which went along the way for the successful completion of this thesis work.

Next I would like to thank Mr. Anil Singh, Ms. Nidhi Agrarwal, Ms. Megha Agarwal and friends for all the good times at the lab and for their help, criticisms, suggestions which makes everyday a pleasant one. Thanks so much to all of you for the fun, and great memories here at Thapar University.

Finally and above everyone else, my heartfelt thanks and life-long gratitude goes to my parents for their love, affection, constant support and encouragement.

I am also thankful to God who bestowed upon his grace and always with me.

ABSTRACT

The design of high gain op-amps for switched-capacitor circuits has become increasingly challenging with the migration of designs to scaled CMOS technologies. In order to eliminate the use of op-amps in sampled data systems and thus avoid several delicate trade-off between the designs, a new class of Comparator-Based Switched Capacitor (CBSC) has been introduced, that replaces op-amp in sampled data systems with the comparator and a set of current mirrors. CBSC circuits have lower power consumption, compared to op-amp based system and avoid several delicate trade-off of the op-amp circuits. CBSC can be used in switched capacitor filters, pipelined ADC & integrator in sigma-delta ADC etc.

A critical circuit in the CBSC method is the virtual ground detection comparator. The comparator used must have high speed and low offset, so as to avoid the delay in virtual ground detection. The role of the virtual ground detection by the comparator is of critical importance to the accuracy of the CBSC circuits.The major objective of this work is to understand the concepts behind the Comparator-Based Switched Capacitor (CBSC) technique for scaled technologies and designing a high speed and low offset comparator for the CBSC circuits.The g_m/I_d technique is also adopted in this work, to help us designing analog circuits in submicron technologies. This work also compares the designing of high speed and low offset comparator using g_m/I_d technique with that of conventional design technique.

The design was simulated in UMC 0.18μm CMOS process with power supply of 1.8V in Cadence Analog Design environment.

TABLE OF CONTENTS

LIST OF FIGURES

LIST OF TABLES

CHAPTER 1

INTRODUCTION

The needs of large digital systems have driven the development of modern scaled CMOS processes. Process advances such as lower power supplies and shorter gate lengths which lead to lower power consuming, faster digital circuits can also lead to higher power consuming, lower performance analog circuits. Although the higher f_T of scaled devices can be used to increase analog performance, other process characteristics such as reduced transistor output resistance and lower supply voltage make the design of op-amps, a fundamental analog building block, more challenging. Traditional analog design techniques require op-amps with very high gain to achieve accurate results. The objective of this work is to study different comparator-based switched-capacitor techniques that remove the need for op-amps in switched-capacitor circuits. The high speed, low offset continuous time voltage comparator required for the comparator-based switched-capacitor technique is then designed using g_m/I_d technique.

1.1 MOTIVATION

The persistent advance of CMOS process technology which has enabled unprecedented performance advancement of digital integrated circuits has also created many new challenges in the design of analog integrated circuits. Analog designers have been able to overcome the challenges of modern CMOS technology in order to take advantage of its inherent advancement. As CMOS continues to scale, this designing will become more and more difficult. One of the most important design challenges posed by CMOS scaling is the design of high gain operation amplifiers (op-amps). Op-amps are essential analog building blocks. They often limit the performance integrated systems. Often the gain of the op-amp will limit the accuracy of the analog system and the bandwidth of the op-amp will limit the speed of the system. The gain of op-amps contained in the input sample and-hold as well as the pipeline stages will directly limit its accuracy.

Two aspects of CMOS scaling are increasing the difficulty of designing high gain op-amps: smaller gate length and reduced supply voltage. The ever shrinking gate length of modern CMOS devices is the heart of CMOS scaling. Smaller transistors enable faster smaller digital circuits, but also provide lower output resistance (r_o). Since the $g_m \times r_o$ product of a transistor fundamentally limits the gain of any amplifier, scaled devices produce lower gain op-amps. This effect could traditionally be negated by using longer than minimum length devices in a

design. Intrinsic speed (f_T) would be sacrificed for higher intrinsic gain. The output resistance of modern digital devices does not increase significantly with increasing length.

Reduced supply voltages are both a feature and requirement of scaling. Using a lower supply voltage enables lower power consumption in digital circuits, but it is also a requirement of using scaled devices. In order to maintain gate control over very small devices it is required that one uses a very thin gate oxide. A low supply voltage must be used in order not to damage this oxide or cause break down in the very short channel. Unfortunately in analog circuits a lower supply voltage usually leads to higher power dissipation for a similarly performing circuit. A lower supply voltage limits the output swing and consequently causes the signal to noise ratio to decrease. In order to maintain the same signal to noise ratio capacitor sizes must be increased to reduce noise. The power consumption of the circuit must be increased to drive the larger capacitors at the same speed as the original circuit.

In order to achieve reasonable gain in an amplifier designed, it is often necessary to cascode transistors. The cascoded topology further reduces the already limited output swing. Another novel approach is suggested to address the challenges of scaled CMOS analog circuit design in [1] which is the basis for this thesis. In this paper they suggest the use of comparators instead of the op-amp, a new class of comparator-based switched-capacitor circuit topologies is proposed [1] that does not require op-amps in the signal path. The design of a comparator is more relaxed and simpler than the op-amp in scaled CMOS technologies.

1.2 COMPARATOR-BASED SWITCHED-CAPACITOR CIRCUITS

An alternative to op-amp based implementation as shown in Figure 1.1 is architecture called Comparator-Based Switched-Capacitor (CBSC) circuits. This architecture replaces the op-amp with a continuous time comparator and a current source as shown in Figure 1.2.

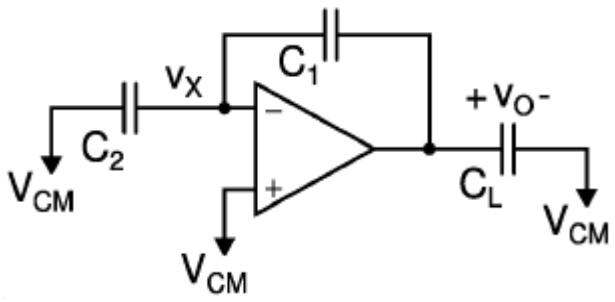


Figure 1.1: Op-amp based switched-capacitor gain stage. [2]

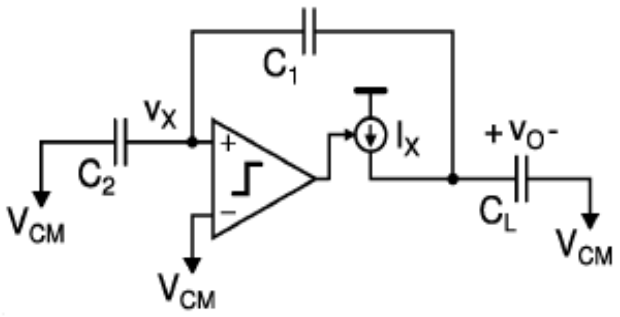


Figure 1.2: Comparator-based switched-capacitor gain stage. [2]

The op-amp based implementation forces the virtual ground condition, the CBSC implementation sweeps the output voltage and searches for the virtual ground condition. It is the accuracy of the virtual ground condition that matters. A critical circuit in the CBSC method is the virtual ground detection comparator. Unlike the traditional clocked comparator that compares voltage at a specific point in time the virtual ground detection comparator must detect the time the voltage ramp crosses the virtual ground condition and must then open the output sampling switch. Comparators can achieve high gain by cascading several gain stages. Because the comparator is only used in open-loop configuration, there are no associated stability issues with this approach.

The comparator used in threshold detection must have high speed and low offset, so as to avoid the delay in virtual ground detection. So, high-performance comparator architecture is chosen for the CBSC technique, which consists of 3 stages i.e. a Preamplification stage, a decision circuit, and an output buffer. The pre-amplification stage is a differential amplifier (diff-amp) with active loads suitable for high speed since there aren't any high-impedance nodes other than the input and output nodes. The decision circuit uses positive feedback from the cross-gate connection between the transistors to increase the gain of the decision element and also includes a bottom transistor, which acts to shift the output level of the decision circuit upward and thereby moves it into the common-mode range of the output buffer. Finally, the output buffer or post-amplification stage. The role of the virtual ground detection by the comparator is of critical importance to the accuracy of the CBSC charge transfer accuracy.

The g_m/I_d technique is adopted in this thesis, to help us designing analog circuits in submicron technologies. The work is motivated by basic circuit design challenges: sizing up the transistors in modern processing technologies. By understanding basic characteristics of

modern MOSFET, a simple and new design equation based on trans-conductance efficiency has been utilized in the design process.

1.3 THESIS ORGANIZATION

The thesis is organized into eight chapters. The outline of each chapter is as follows:

CHAPTER 1 – INTRODUCTION

This chapter introduces the motivation and the organization of the Thesis.

CHAPTER 2 - COMPARATOR BASED SWITCH CAPACITOR CIRCUITS

This chapter provides an introduction to the comparator-based switch-capacitor technique. This chapter covers the basic principle of operation and compares the technique to standard op-amp based switched capacitor technique.

CHAPTER 3 - HIGH-SPEED, LOW-OFFSET COMPARATOR

This chapter focuses on background and characterization of comparator & high performance comparator. The high performance comparator has the characteristics of high-speed and low-offset voltage.

CHAPTER 4 - CASCODE CURRENT MIRROR

This chapter discusses the background of current mirror and high-swing cascode current mirror.

CHAPTER 5 - Gm/Id BASED DESIGN

This chapter provides an introduction to g_m/I_d technique and its design flow with a design example of common source amplifier with resistive load.

CHAPTER 6 - DESIGNING OF HIGH-SPEED, LOW-OFFSET COMPARATOR

This chapter describes the designing of comparator using g_m/I_d technique and comparison of g_m/I_d design technique with conventional design technique. The design and simulations are performed in Cadence environment.

CHAPTER 7 - LAYOUT DESIGN

This chapter describes the layout design of various blocks in Comparator.

CHAPTER 8 – CONCLUSION AND FUTURE SCOPE

This chapter summarizes the contributions of this thesis and suggests areas for future work.

CHAPTER 2

COMPARATOR BASED SWITCH CAPACITOR CIRCUITS (CBSC)

2.1 OVERVIEW

The CBSC stands for Comparator Based Switch Capacitor Circuits. The basic operation of comparator-based switched-capacitor circuits (CBSC) is introduced. After establishing the basics, a more practical comparator-based charge transfer phase is described. Finally, a summary of the known limitations and potential advantages of the CBSC technique is given.

2.2 CBSC BASIC PRINCIPLE OF OPERATION

Although the CBSC technique is applicable to a wide range of switched-capacitor circuits, a simple switched-capacitor gain stage is used to illustrate the basic principle of operation. A traditional op-amp based switched-capacitor gain stage is compared to the proposed comparator-based implementation. Both circuits use the same input sampling circuit. The difference is in the method of achieving the virtual ground condition during the charge transfer or amplification phase.

2.2.1 Sampling Circuit

Assume that both circuits use the same open-loop input sampling circuit shown in Figure 2.1. During the sampling phase φ_1, the input voltage sampled onto both C_1 and C_2.

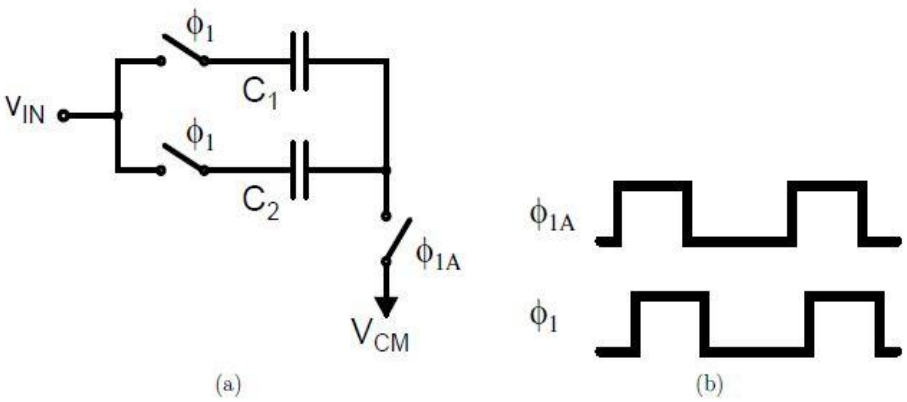


Figure 2.1: Bottom plate open-loop sampling (a) Sampling circuit. (b) Sampling clocks. $Ø_{1A}$ defines sampling instant to minimize input dependent charge injection. [2]

The opening the bottom plate switch to V_{CM} at the falling edge of $Ø_{1A}$ defines the sampling instant. The clock $Ø_{1A}$ is an advanced version of the sampling phase clock $Ø_1$. This sampling method minimizes signal dependent charge injection from the sampling switch.

2.2.2 Op-amp Based Charge Transfer Phase

In the traditional op-amp based charge transfer phase, the capacitors C_1 and C_2 are reconfigured as shown in Figure 2.2. The op-amp then forces a virtual ground condition at node V_X. This force all the charge sampled onto C_2 to transfer to C_1. During the charge transfer, both the output voltage V_O and the virtual ground node V_X exponentially settle to their steady-state values. In Figure 2.2, the exponential settling neglects slew rate limitations and the effects of higher order poles in the op-amp that would increase the required settling time. After a number of time-constants have passed to achieve the desired output voltage accuracy, the output of the stage can be sampled. The relationship between the input and output samples is given by equation (2.1) and the capacitor ratio (C_2/C_1) determines the gain of the amplifier.

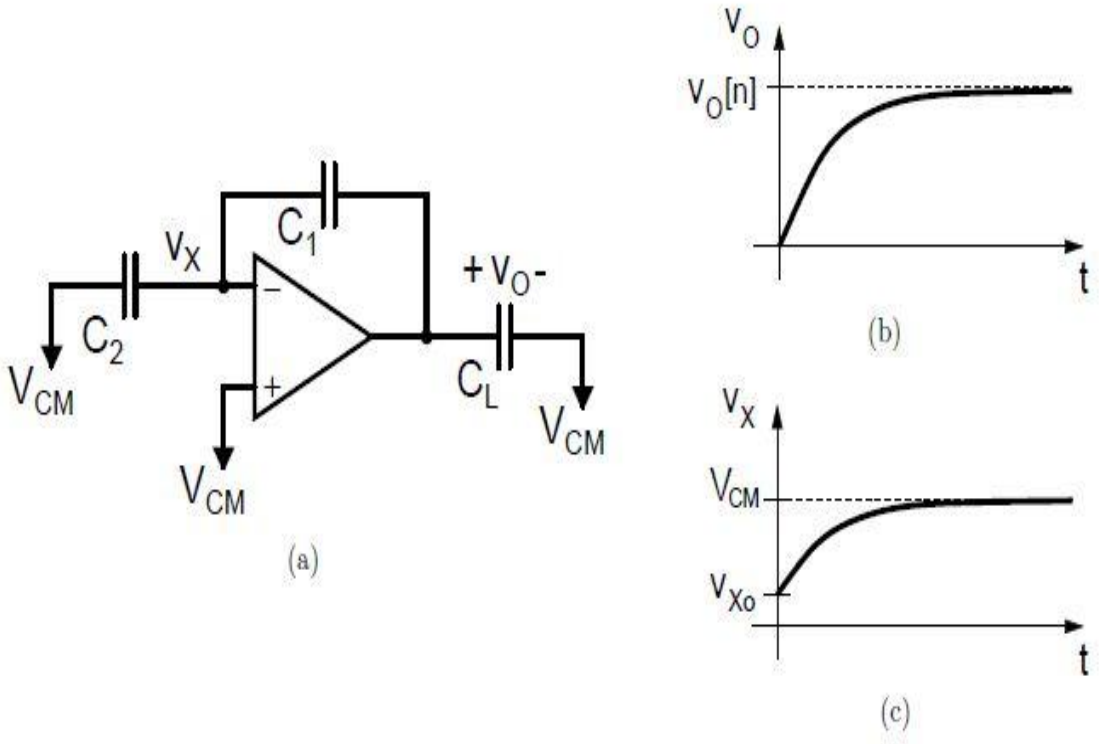


Figure 2.2: Op-amp based switched-capacitor gain stage charge transfer phase. (a) Switched-capacitor circuit (b) The output voltage exponentially settles to the final value. (c) The summing node voltage exponentially settles to the virtual ground condition. [2]

$$Vo[n] = \frac{C1+C2}{C1} Vin\left[n - \frac{1}{2}\right] \quad (2.1)$$

Note that during the charge transfer phase, the accuracy of the output voltage directly depends on the accuracy of the virtual ground condition. In conventional designs, the op-amp forces the virtual ground in a continuous-time manner, but in switched capacitor circuits, an accurate virtual ground condition is only required at the sampling instant. Therefore, it should be possible to detect the virtual ground condition at a single time point using a threshold-detection comparator rather than force it with an op-amp. Also, detecting the virtual ground condition should be more energy efficient than forcing it.

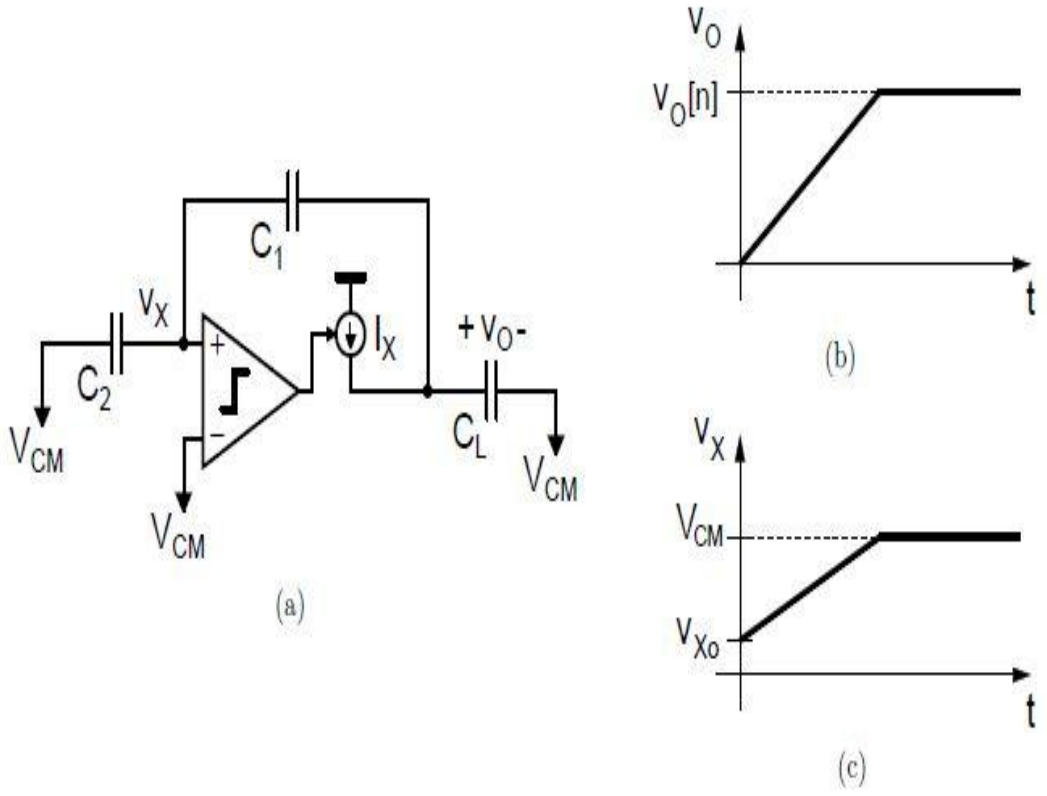


Figure 2.3: Op-amp based switched-capacitor gain stage charge transfer phase. (a) Switched-capacitor circuit (b) The output voltage exponentially settles to the final value. (c) The summing node voltage exponentially settles to the virtual ground condition. [2]

2.2.3 Comparator-Based Charge Transfer Phase

Detecting the virtual ground condition is the approach taken in the Comparator-based charge transfer phase. The procedure for implementing a comparator based charge transfer phase is now presented. Again, assuming the input was sampled just like in the op-amp case, and the

capacitors C_1 and C_2 are reconfigured in a similar manner; the result is the circuit in Figure 2.3. The op-amp has been replaced with a virtual-ground threshold-detection comparator and a current source I_X. Assuming for the moment that something has been done to ensure that V_X always starts below the virtual ground condition ($V_{XO} < V_{CM}$), the current source I_X turns on at the beginning of the charge transfer phase and charges up the capacitor network consisting of C_1, C_2 and C_L.

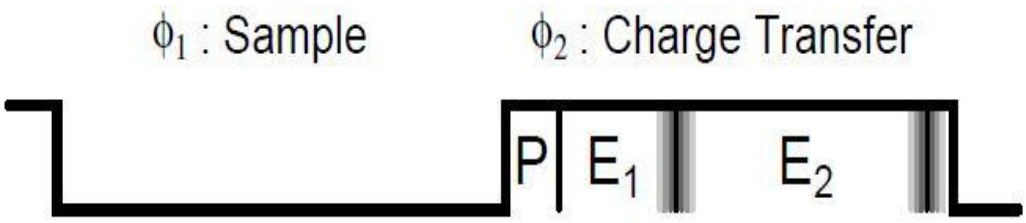


Figure 2.4: CBSC charge transfer phase timing. [2]

The ramp voltage waveforms are shown in Figure 2.3. The voltage V_X continues to increase until it equals V_{CM}. At this point, the comparator detects the virtual ground condition and turns off the current source I_X. Therefore, the comparator defines the sampling instant. The state of the circuit is identical to that of the op-amp based implementation, and the relationship between the input and output samples are identical to equation (2.1).

2.3 PRACTICAL CBSC GAIN STAGE CHARGE TRANSFER

Now that the basic principle of operation has been established, a more practical version like that used in the prototype system is described. The first issue that must be addressed is to ensure the initial condition in the charge transfer phase. The second issue is maximizing the accuracy of the charge transfer phase. To minimize the noise in the comparator decision, it is desirable to maximize the time available to the comparator to do noise averaging when making its decision. It is also desirable to minimize the final overshoot to minimize the sensitivity to nonlinearity in the ramp rate.

To address these requirements, the charge transfer phase for the prototype was divided into three sub-phases: preset phase (P), coarse charge transfer phase (E_1), and fine charge transfer phase (E_2).The time available for each sub-phase is as illustrated in Figure 2.4. The time spent on

coarse and fine charge transfer is signal dependent because of the self-timed nature of the comparator-based circuit.

2.3.1 Preset Phase

To ensure the voltage V_X starts out below the virtual ground condition V_{CM}, a brief preset phase is used in Figure 2.5. Assuming the input has just been sampled onto C_1 and C_2, the summing node voltage V_X starts at V_{CM}.

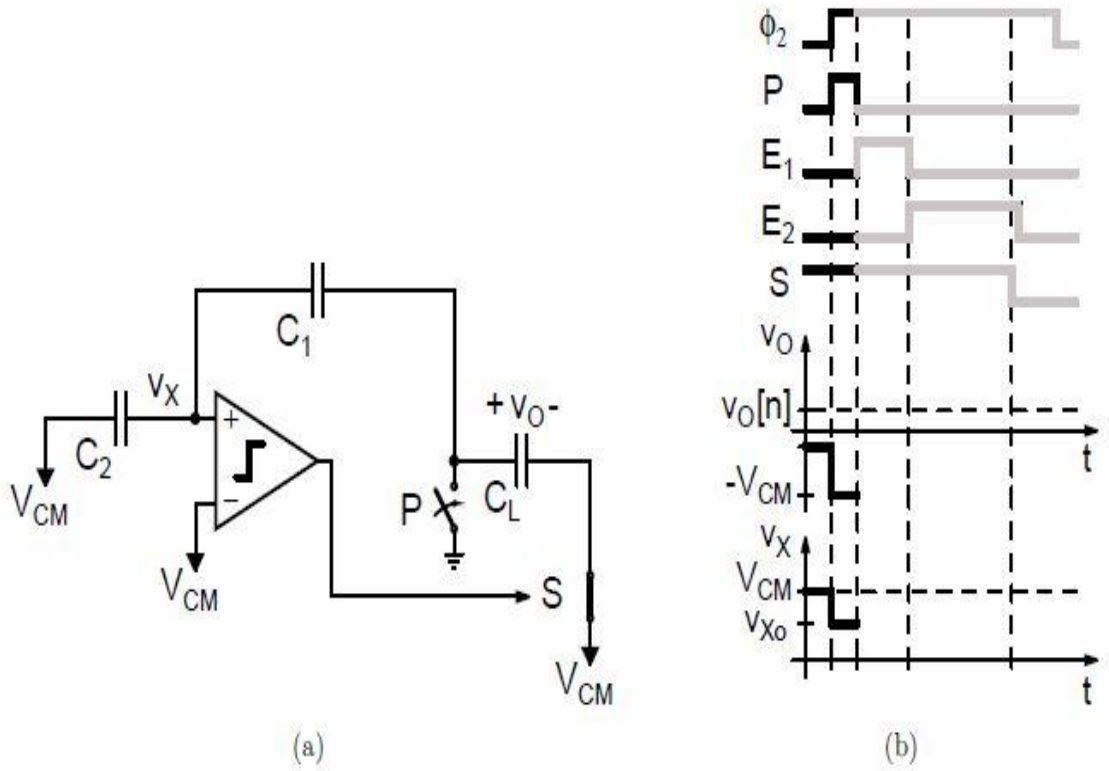


Figure 2.5: Preset phase (P). (a) Switch P closes. (b) V_O grounded and V_X set below $V_{CM.}$ [2]

If at the same time C_2 is connected to V_{CM}, the output node is also switched to the lowest voltage in the system (ground), then a negative step results at the summing node V_X through the capacitive divider C_1 and C_2. This negative step can be used to ensure the preset voltage for V_X is less than the common-mode voltage over a range of input voltages. During the preset phase, the output sampling switch S is also closed after the preset switch to ground has been closed. Therefore, the preset state also resets the load capacitance before charge transfer begins.

2.3.2 Coarse Charge Transfer Phase

To obtain a quick, rough estimate of the output and virtual ground condition, a relatively

fast ramp-rate is used in the coarse charge transfer phase. The coarse phase ramp is generated with current source I_1 in Figure 2.6. Because of finite delay of the comparator, the output of the gain stage overshoots the correct value.

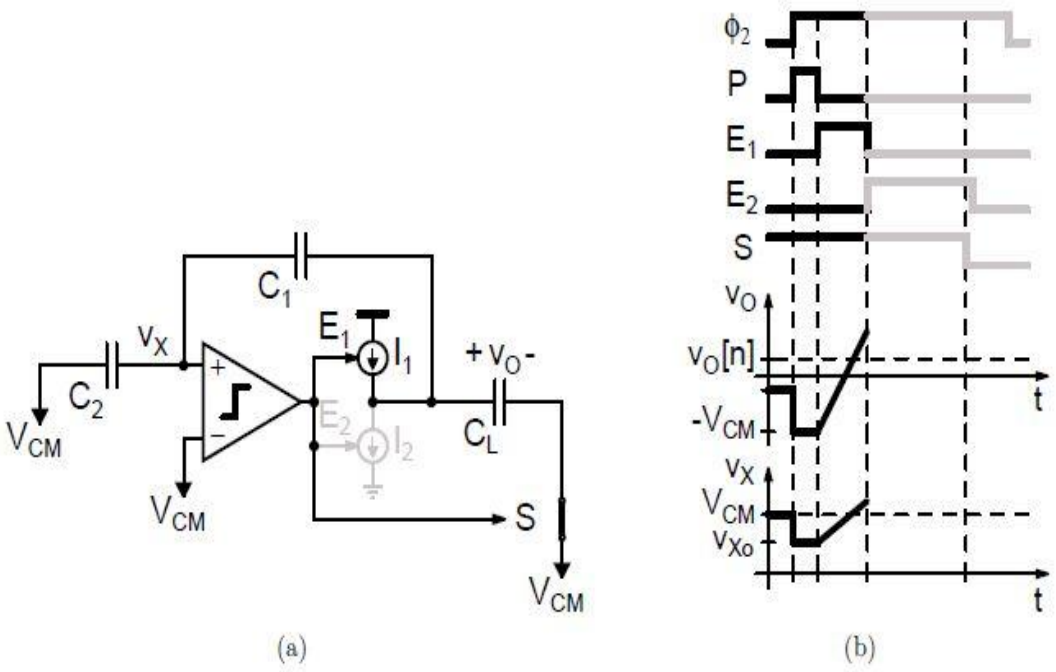


Figure 2.6: Coarse charge transfer phase (E_1). (a) Current source I_1 charges output. (b) V_O and V_X ramp and overshoot their ideal values. [2]

2.3.3 Fine Charge Transfer Phase

To obtain a more accurate virtual ground condition, a fine charge transfer phase with a significantly more gradual ramp rate is used. The fine charge transfer ramp is generated with current source I_2 in Figure 2.7. The use of the fine charge transfer phase also erases any noise and nonlinearity from the first comparator decision and overshoot. It is the final overshoot that determines the offset and nonlinearity of the stage. If the ramp rate is perfectly constant over the full-scale output range of the stage, then the final overshoot would only be an offset, and in many systems, it could be easily be corrected. Unfortunately, the overshoot is not constant in a real system. Therefore, the second overshoot must be kept small enough to meet the linearity requirements of the stage.

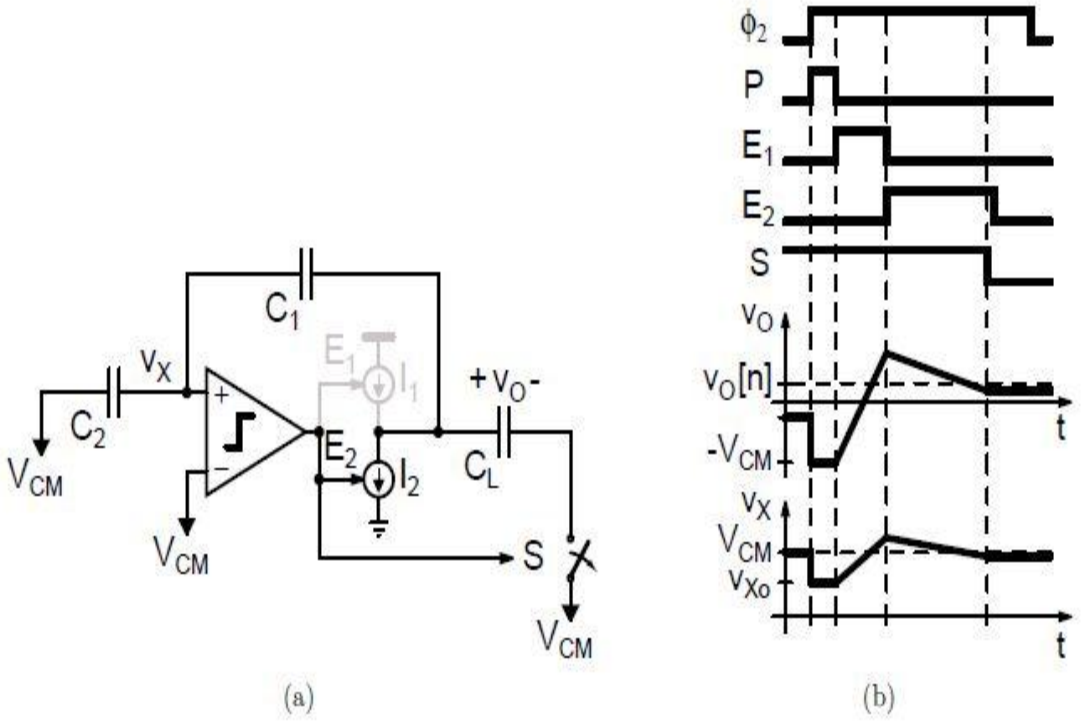


Figure 2.7: Fine charge transfer phase (E_2). (a) Current source I_2 discharges output. (b) V_O and V_X ramp to their final values. [2]

2.4 DIFFERENT CBSC TOPOLOGIES

In scaled CMOS technologies, analog circuit design becomes more challenging. The reduced output resistance of the devices has brought down the gain of the operational amplifiers. It is a known fact that the finite gain of the op-amp results in errors in switched capacitor circuits. As the power supply is scaled down, many topologies used previously to improve the performance fail to work. An effort to boost the gain and GBW of the amplifier meant a burning a lot of power for the same performance.

Different approaches have been suggested to overcome this problem. One of them is to use an adaptive algorithm and do digital calibration in the background. The performance of the analog circuit is enhanced by some digital post processing. Another novel approach is suggested in [2] which is the basis for this project. The paper describes a single-ended switched capacitor gain stage using a comparator and a current source to replace the op-amp. The basic principle of CBSC operation is based on the detection of a virtual ground condition in the CBSC case rather than forcing it via feedback in the op-amp case.

To achieve high accuracy and linearity, the charge transfer phase is divided into two sub-phases: a coarse charge-transfer phase and a fine charge-transfer phase. The coarse charge-transfer phase (E_1) is used to get a fast, rough estimate of the output voltage and virtual ground condition. The finite delay of the comparator and the high output ramp rate results in an overshoot of the correct value. When the comparator makes its decision, the current source I_1 is turned off. The fine transfer phase (E_2) is used to get a more accurate detection of the virtual ground condition and consequently a more accurate value for the output voltage. The fine phase current I_2 is much less than the coarse phase current I_1 and of opposite sign. This allows the comparator to have a longer delay without causing a large final overshoot. When the comparator detects the second threshold crossing, the sampling switch S is opened. This defines the sampling instant and locks the sampled charge on the load capacitance C_L. The current source I_2 is turned off slightly after the sampling switch opens, but the extra current it sinks does not disturb the sampled charge because it only discharges the parasitic capacitance at the output node.

The time required to complete the charge transfer is signal dependent. The duration of the coarse charge transfer phase E_1 depends on the preset value V_{X0}, which depends on the input signal. The charge transfer is self timed, but for correct operation, the total charge transfer must be complete before the end of the time allocated for charge transfer. As shown in Figure 2.7, the falling edge of Φ2 represents the end of the allocated charge-transfer time. During the coarse charge-transfer phase, a large current is used to charge the output capacitance, thereby creating a potentially large offset and nonlinearity. The large overshoot slows the operation of the circuit because the fine phase current needs a long time to discharge the output and recover from the coarse phase overshoot. In order to minimize this recovery time, the coarse phase comparator delay must be made as short as possible. Also, the constant portion of the overshoot can be canceled. One way to do this is to change the reference voltage of the level detection comparator from V_{CM} to a lower voltage V_{OC}, or subtracting a predetermined amount of charge after the coarse transfer [2].This technique is called Overshoot Correction.

The Overshoot Correction technique, maximize the time available for the comparator decision in the charge transfer phase without placing excessive speed requirements on the comparator during the coarse charge transfer phase.

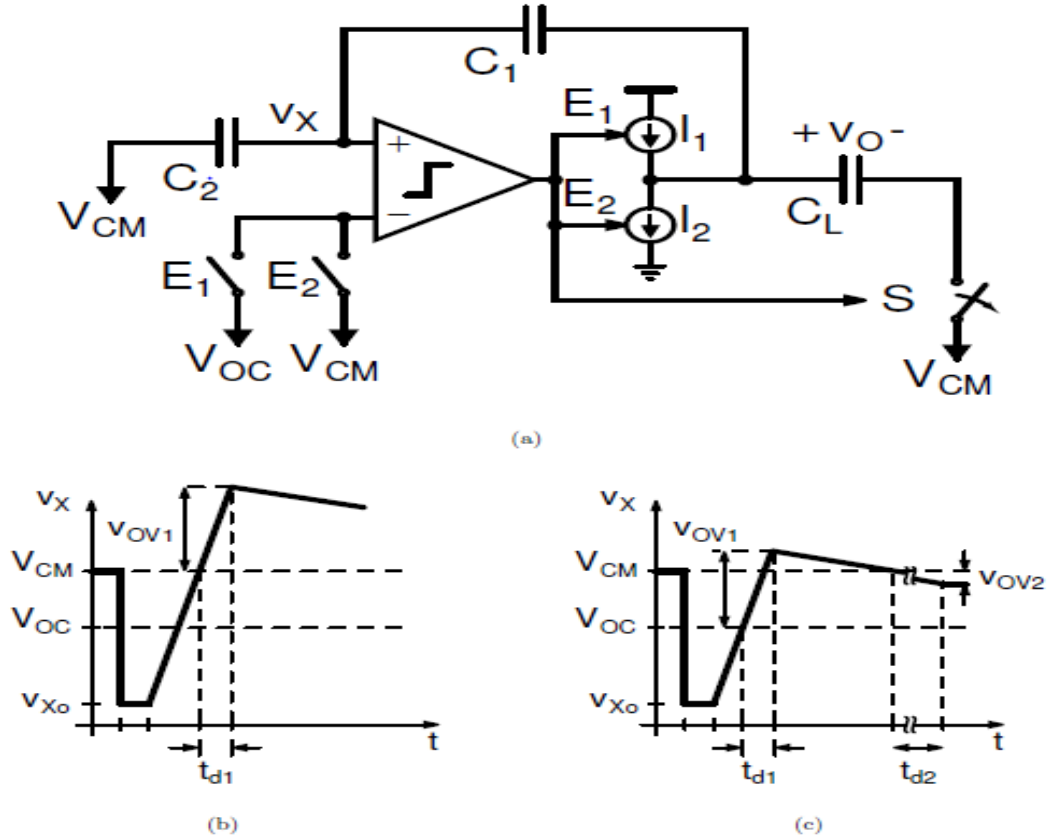


Figure 2.8: Overshoot cancellation. (a) CBSC stage with overshoot cancellation. (b) V_X node voltage during the charge transfer phase without overshoot correction. The large overshoot during the coarse phase prevents the charge transfer operation from finishing in allowed time. (c) CBSC stage with overshoot cancellation. [2]

Consider the coarse phase decision shown in Figure 2.8(b). If the comparator has a total delay time of t_{d1} for the coarse charge transfer phase, and the reference voltage on the comparator is the common-mode voltage V_{CM}, then the overshoot v_{OV1} of the true virtual condition is relatively large. The fine phase charge current must discharge the summing node voltage back to V_{CM} before the comparator can make its second decision in the fine charge transfer phase. Therefore, the overshoot of V_{CM} limits how much the ramp rate can be reduced for the fine charge transfer phase while maintaining the same speed of operation. However, if the coarse phase ramp rate is constant, then the overshoot V_{OV1} is the same every time, and it is possible to use a comparator reference voltage V_{OC} that is slightly below V_{CM} to anticipate the threshold crossing as shown in Figure 2.8(c). The circuit implementation for the overshoot correction is shown in Figure 2.8(a), where two different references are switched to the comparator for the coarse and fine charge transfer phases. For a perfectly constant ramp

rate, the coarse phase overshoot could be completely canceled, but ramp rate variation and noise in the coarse phase comparator decision place a limit on the amount of overshoot correction. The supply voltages also place a constraint on the possible amount of overshoot correction.

There is stringent trade-off between speed and accuracy in the conventional CBSC circuits. Figure 2.9 illustrates the stringent trade-off between speed and accuracy presents in the conventional CBSC circuits. When its operation speed is increasing the coarse transfer phase

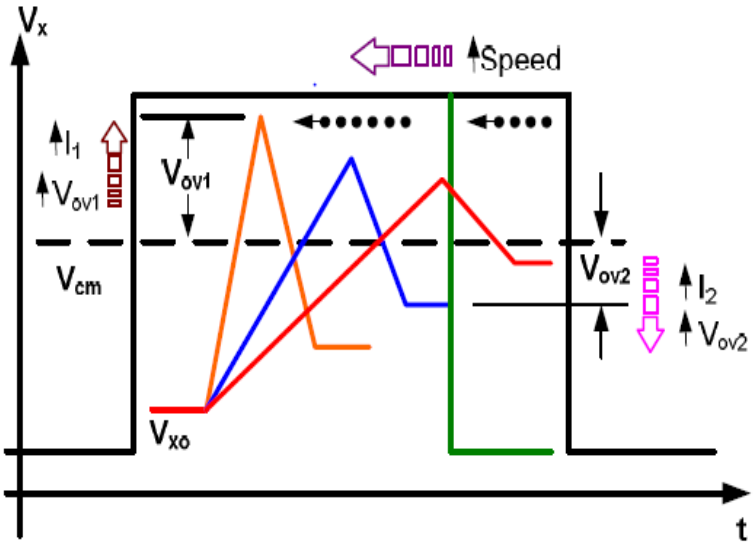


Figure 2.9: Relationship between speed and accuracy in conventional CBSC circuits. [3]

Current I1 and the overshoot Vov_1 will also increase. In order to recover from the large overshoot Vov_1 and, to guarantee that the fine transfer phase finishes before the end of the operation period, the fine phase current I_2 should increase leading, consequently, to a reduction in accuracy. Therefore, the large overshoot Vov_1 is the main barrier to increase speed while maintaining accuracy in the conventional CBSC circuits.

In order to increase the speed, i.e. to make the charge transfer phase faster, a new charge control scheme was presented by [3]. In this approach, new charge transfer scheme over conventional CBSC [2] , does not need any preset of the output node at the beginning of the charge transfer phase, because here it is not necessary for V_X to start below the comparator input common mode voltage (V_{CM}). This approach [3] and its timing diagram are depicted in Figure 2.10.

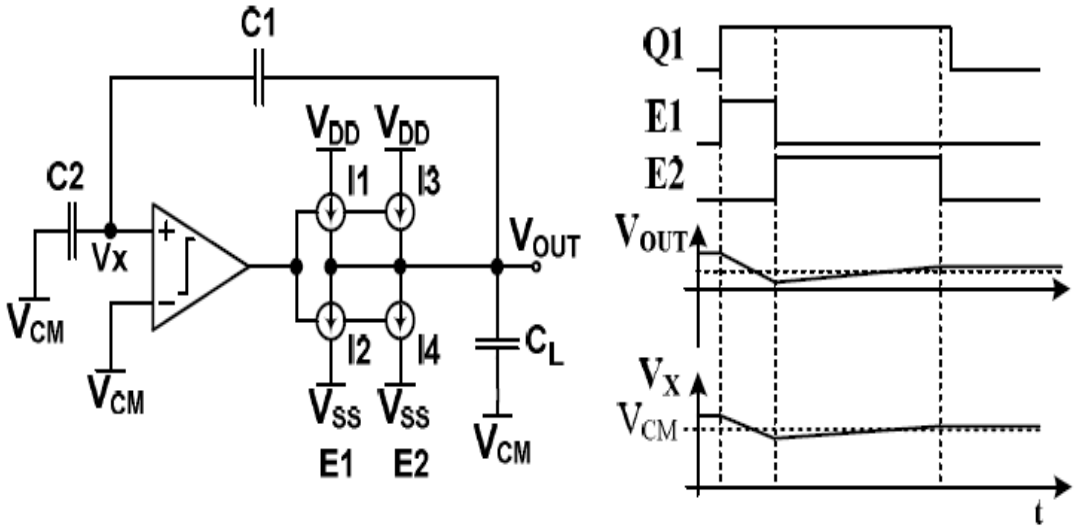


Figure 2.10: New approach to control the charge transfer phase. [3]

In this, at the beginning of the charge transfer phase, based on the voltage V_X, the current source I_1 or the current sink I_2 will turn on to begin the coarse charge transfer phase (E1). As soon as V_X crosses V_{CM}, the active current source (I_1 or I_2) will turn off and the fine charge transfer phase will start by turning either I_3 or I_4 on. The current I_3 and I_4 are less than I_1 and I_2 and result in a slower ramp back toward V_{CM}. The fine charge transfer phase will finish as soon as V_X crosses V_{CM} again and the active current source (I_3 or I_4) will then turn off. When all the current sources and the current sinks are inactive, the output node will be floating; therefore, the charge on C_L will not change. Eliminating the need to preset the output node at the beginning of the charge transfer phase will result in faster output settling. That is because the output node is not forced to start being charged from V_{SS} in each clock cycle so less charge and consequently less time is needed to make output.

To address the issue of increasing accuracy of conventional CBSC circuits, 3-phase mode conventional CBSC gain stage is converted to 4 phase mode, modified CBSC gain stage [4]. This modified CBSC structure is shown in Figure 2.11, which interposes middle-phase E_{mid} between E_1 and E_2. For this, a "soft" current source (I_{mid}) is used which turns on when V_X is in the range of V_{COMP1} to V_{CM}. Since I_{mid} is much smaller than I_1, lower settling-time can be achieved without decreasing input-swing or accuracy. Depending on input level, charge-transfer mode is divided to 3 or 4 phases of operation. The first phase is Preset phase, E_{PRST}. If at the end of E_{PRST}, V_X is smaller than V_{COMP1}, Preset will be followed by 3 other phases: E_1, E_{mid} and E_2. Otherwise, charge-transfer mode will be completed in 2 phases E_{mid} and

E_2, following E_{PRST}. Thus this novel structure [4] uses interposing middle-phase in charge transfer mode to reduce V_{ERR} without speed degradation.

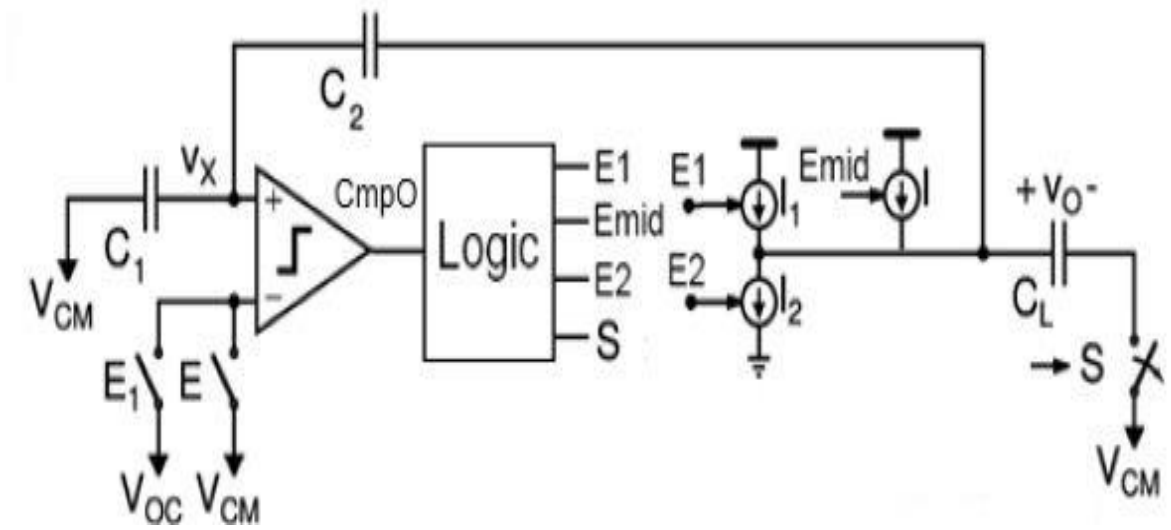


Figure 2.11: Modified CBSC structure. [4]

In the comparator based switch capacitor circuit, the charge transfer error is a function of comparator delay and output current, where a portion of this error term is nonlinearity and gain error caused by finite resistance of current source. The rest of the error term is offset. The speed of operation is proportional to the current charging the capacitors; hence there is a trade-off between speed and accuracy. In the conventional CBSC technique [2], accuracy issue is partially solved by utilizing an extra fine correction phase [2-3], which in turn imposes longer settling time and lower sampling speed. One interesting feature of CBSC technique is that the linearity of current is only important at virtual ground detection instant In order to achieve faster settling, variable current source can be used. The idea is to charge the capacitor with current proportional to the difference between V_X and V_{REF} [5]. This can be done by using a voltage controlled current source instead of the constant current source used in the conventional CBSC circuit. The variable current source changes proportionally to the difference between the virtual ground V_X of capacitors network and the comparator's reference voltage.

One of the issues which these architectures [2-5] suffer from it is overshoot at the end of the coarse phase. It decreases the speed and accuracy. By attenuating the primary overshoot, we can increase the speed (fastest settling) and decrease power consumption. A new novel architecture was proposed by [6], which utilizes an extra comparator to make a variable comparator threshold, in order to attenuating the overshoot at the end of the coarse phase.

The Gain stage of this new structure is shown in Figure 2.12 and its timing diagram with variable comparator threshold.

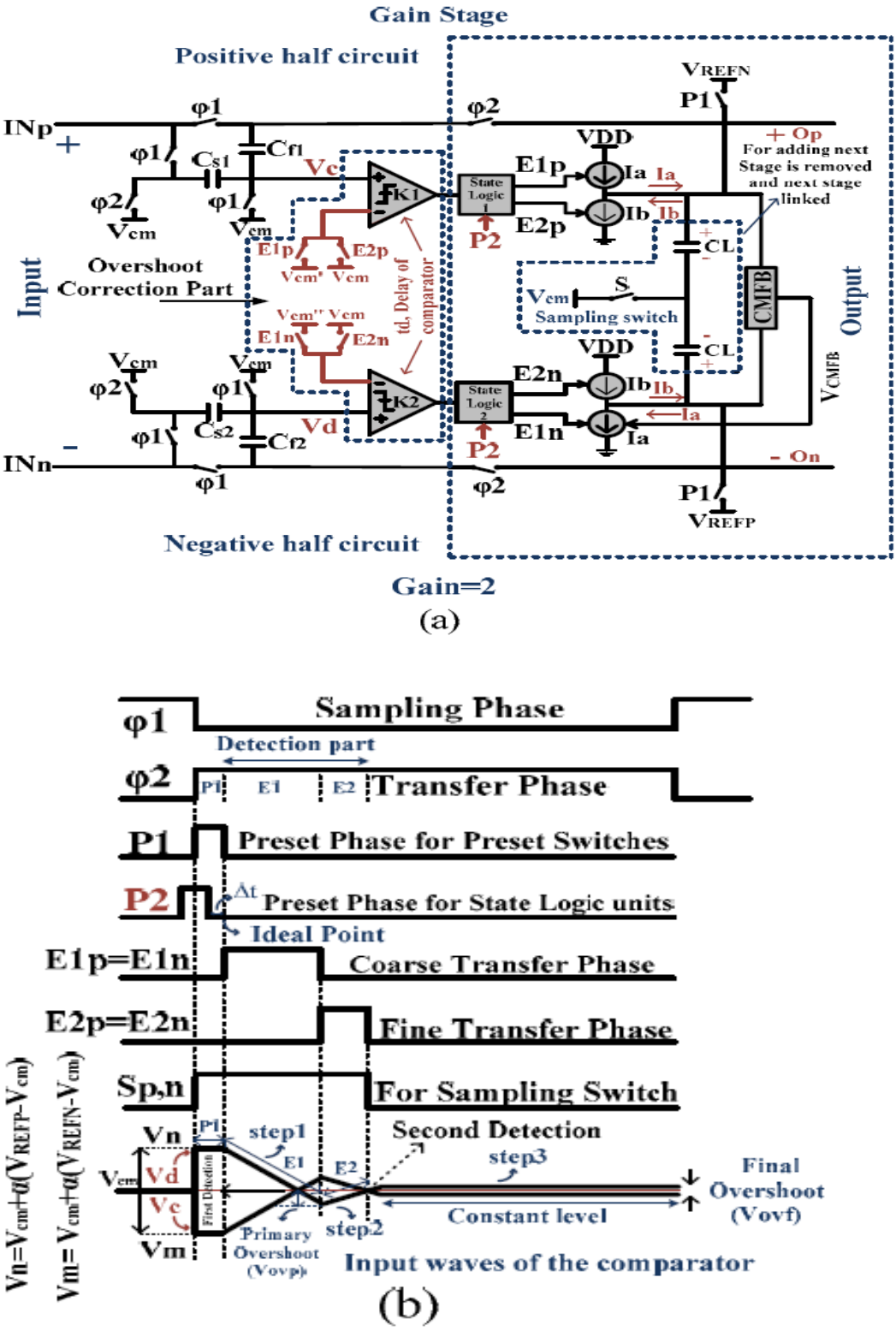


Figure 2.12: (a) Gain stage with variable comparator threshold (b) Timing diagram [6]

As it is seen from timing diagram, Φ1 is sampling phase and Φ2 is charge transfer phase. In Φ1 phase, the input signal is sampled by input capacitors ($C_{S1,2}$ and $C_{f1,2}$).

The charge Transfer phase is divided into four following sub-phases: 1) preset phase for preset switches (P1), 2) preset phase for driving the state logic units (P2), 3) coarse transfer phase (E1) and 4) fine transfer phase (E2). After sampling, the outputs (O_p, O_n) are preset to V_{REFP} and V_{REFN}. Preset phase sets the outputs nodes to preset levels away from common voltage level (V_{CM}). P2 is used to compensate for the delay in the state logic units and driver switches of the current sources. After preset phase, state logic units produce ($E_{1p,n}$) and trigger coarse current sources to charge the capacitor network. I_a charges the positive half circuit and discharges the negative half circuit. As a result input nodes of the comparator (V_C and V_D) are charged in opposite directions to cross each other for making first decision as seen in Figure 1(b). However, there is overshoot in the output due to the finite delay in the comparators and ramp rate (V_{OVP}). For this reason, two comparators have been used in this design (K1, K2), so we can already adjust the comparison levels for delay compensation and attenuating the primary overshoot.

To achieve more accurate output, the fine transfer phase is used. During this phase, fine current sources are turned on to reduce the final overshoot and also achieve to second detection as seen in Figure 2.12(b). Accuracy of the fine current sources determines the final error which determines the offset and nonlinearity .To produce a very highly accurate CBSC gain stage, a three-step pattern was used as it is seen from input waves of the comparators in Figure 2.12(b). By using this technique more constant output voltage would be achieved which can be used in high precision and high frequency applications. Thus this architecture [6] utilizes an extra comparator to attenuate the primary overshoot at the end of the coarse phase for increasing the speed and accuracy.

Comparator based switch capacitor technique provides a simple solution for amplifier gain problem, but accuracy of these techniques is limited by the comparator and the current source. Delay of comparator and finite output resistance of current sources will directly affect the accuracy of comparator based circuits. Table 2.1 summarizes the comparison between various CBSC architectures in the literature.

Table 2.1 Comparison between various CBSC architectures in the literature.

Architecture	[6]	[2]
Sampling frequency	20 MHz	20 MHz
Coarse charge current (I_1)	230 µA	250 µA
Fine charge current (I_2)	58 µA	90 µA
Supply Voltage	1.8 V	1.8 V
Technology	0.18 µm	0.18 µm
Primary overshoot at the input nodes of the comparators ($V_c - V_d$)	54.7 mV	83.3 mV
Final overshoot at the input nodes of the comparators ($V_c - V_d$)	31.2 mV	34.1 mV

2.4 SUMMARY

The basic principle of a comparator-based charge transfer phase has been explained. Its operation parallels that of an op-amp based system, but it takes advantage of the fact that an accurate virtual ground is only needed at the sampling instant. A brief overview of accuracy limitations is given.

2.4.1 Limitations

Because CBSC systems lack an output amplifier, they can only drive switched capacitor loads. This is expected since it was one of the drawbacks stated above for op-amp systems that continuously force the virtual ground and output voltages. Only being able to drive switched-capacitor loads does not severely limit the applicability of the CBSC approach. If a continuous load needs to be driven, then an output buffer could be used. A related limitation is that CBSC designs cannot drive both sides of the sampling capacitor simultaneously. This makes the technique incompatible with conventional closed-loop offset cancellation where the input sampling capacitors sample with reference to a driven virtual ground node. The comparator is still free during the sampling phase, and other techniques should be possible to perform offset cancellation

if necessary. As discussed above, finite output resistance of the ramp current sources have an effect similar to finite op-amp gain. However, designing a constant current source in scaled technologies should be easier than designing a high-gain op-amp because the current source is not directly in the signal path, and therefore it has fewer design constraints.

2.4.2 Advantages

Comparator-based systems have the potential for significant power reduction compared to op-amp based designs because of the differences in the noise-bandwidth and speed requirements of op-amp and comparator-based designs. In addition, comparator-based systems are more amenable to design in scaled technologies than op-amp based systems because of differences in the requirements for the comparator and current sources compared to the op-amp. The big difference is that feedback and stability concerns have been removed for comparator-based systems, and the high output resistance current sources are not directly in the signal path. Finally, the CBSC design method should be applicable to a wide range of switched-capacitor circuits and compatible with most known architectures. In sampled data systems, circuit designs that traditionally use feedback to force a virtual ground should be compatible with the proposed virtual ground detection scheme. Switched-capacitor filter, integrators, DACs and ADCs should all be compatible with the CBSC technique. Because the CBSC approach utilizes architectures similar to traditional op-amp based designs, with some notable exceptions made above, the wealth of the design techniques and architectures from op-amp designs should transfer to CBSC designs.

CHAPTER 3

CASCODE CURRENT MIRROR

The current mirror is one of the most useful building blocks for analog integrated circuits. It is largely employed as a biasing element and as a load device for amplifier stages. The use of current mirror in biasing can result in superior insensitivity of circuit performance to variations in power supply and temperature. When used as a load element in transistor amplifiers, the high incremental resistances of the current mirror results in high voltage gain at low-power supply voltages. Current mirrors are frequently more economical than resistors in terms of the die area required to provide bias current of a certain value, particularly when the required value of bias current is small. In this chapter, the background of current mirror and high-swing cascode current mirror are discussed.

3.1 INTRODUCTION

Basically, a current mirror is a circuit that copies a current flowing through one active device (input) to another active device (output) of a circuit, keeping the output current independent of loading. Ideally, the output current is equal to the input current multiplied by a desired current gain. If the gain is unity, the input current is reflected to the output, leading to the name current mirror**.** Under ideal conditions, i.e. an ideal current mirror as shown in figure 3.1 provides the current-mirror gain which is independent of input frequency, and the output current is independent of the voltage between the output and common terminals.

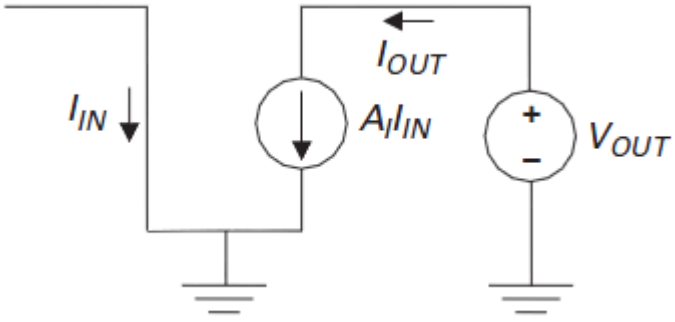


Figure 3.1: The Ideal Current Mirror. [12]

3.2 TWO-TRANSISTOR CURRENT MIRROR

The basic current mirror is shown in Figure 3.2. It consists of a diode-connected input transistor and an output transistor that share the same gate, source, and substrate voltages. The current mirror uses the principle that if the gate-source potential of two identical MOS transistors are equal, the channel currents should be equal.

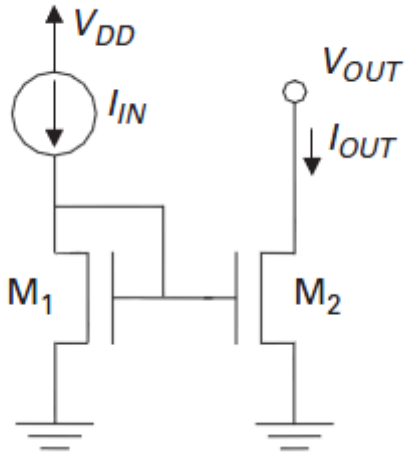


Figure 3.2: A basic MOS current mirror. [12]

A current I_{IN} flows through M1 corresponding to V_{GS1}. Since $V_{GS1} = V_{GS2}$, ideally the same current flows through M2. If the MOSFET's are of the same size, the same drain current flows in each MOSFET provided M2 stays in the saturation region. The current I_{IN} is given by

$$I_{IN} = \frac{1}{2}\mu_n C_{OX}\left(\frac{W}{L}\right)_1 * [(V_{GS1} - V_{TH})^2] \quad (3.1)$$

While the output current, assuming M2 in saturation flowing in M2 is given by

$$I_{OUT} = \frac{1}{2}\mu_n C_{OX}\left(\frac{W}{L}\right)_2 * [(V_{GS2} - V_{TH})^2] \quad (3.2)$$

Since $V_{GS1} = V_{GS2}$, & assuming the transistors is properly matched the ratio of the drain currents is given by

$$\frac{I_{IN}}{I_{OUT}} = \frac{(W/L)_1}{(W/L)_2} \quad (3.3)$$

By adjusting the W/L ratio of the two devices, a desired output current can be achieved.

$$I_{OUT} = \frac{(W/L)_2}{(W/L)_1} * I_{IN} \tag{3.4}$$

So far the effect of channel length modulation has been neglected. However, when also taking into account channel length modulation, the simple current mirror equation 3.4 Becomes

$$I_{OUT} = \frac{(W/L)_2}{(W/L)_1} * \frac{1 + \lambda V_{ds2}}{1 + \lambda V_{ds1}} * I_{IN} \tag{3.5}$$

Equation 3.5 shows that the drain-source voltages of M1 and M2 should be made equal for I_{OUT} to be a precise copy of $I_{IN.}$

The main drawback of this current mirror is its low output impedance, which results in inaccurate matching due to the variation of the drain voltage of M2 with the output voltage.

3.3 CASCODE CURRENT MIRRORS

One of the main problems with a simple current mirror is its relatively low output impedance, which can be insufficient for some applications. A simple way to increase the output impedance of a transistor is to increase the channel length. The output impedance increases (approximately) proportionally to the channel length, whereas the transition frequency will decrease proportionally to the reciprocal of the square of the channel length, which, in some cases, leads to a transition frequency that is not high enough for the application.

3.3.1 Self-Biased Cascode Current Mirror

One way to increase the output impedance of a current mirror is through a change in the circuit topology. The idea is now to use a cascode in the output branch, i.e. to stack another transistor on top of M2 in order to shield the drain of M2 from variations of the output voltage. The resulting structure is known as a cascode current mirror, which is shown in Figure 3.3. The concept of the self-biased cascode current mirror is to use feedback to ensure that the drain voltage of the mirror transistor follows the drain voltage of the input transistor. If transistors M1–M4 are identical and all of them operate in saturation, then $I_O \cong I_I$ and,

consequently, $V_{S3} \cong V_{S4}$ which means that M1 and M2 operate with approximately the same set of voltages.

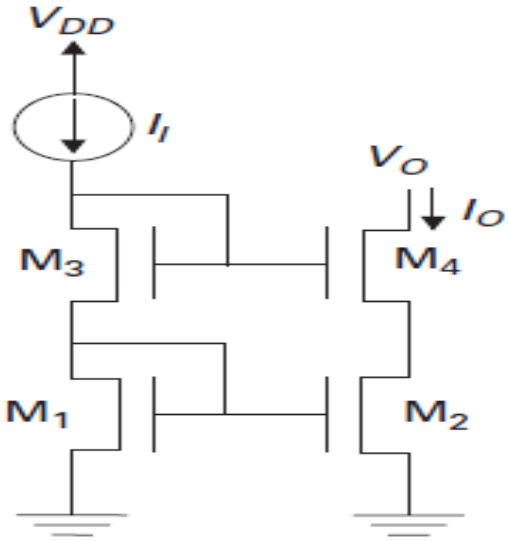


Figure 3.3: A self-biased cascode current mirror. [12]

This means that the sensitivity of the output current, which is equal to the current flowing through M2, to the output voltage is very low, since the drain voltage of M2 is almost unaffected by the output voltage as long as M4 operates in saturation. Since the currents flowing through M4 and M3 are approximately the same, we have $V_{S4} \cong V_{G1}$.Once $V_{G1}$is known, one can immediately find the minimum output voltage required to keep M4 in saturation.

The main advantage to this design is that it provides stable current and it has relatively small transistor sizes. In addition to this we have a higher output resistance compared to the basic current mirror. The main disadvantage to this type of current mirror is a reduced dynamic range. This cascode current mirror loses one threshold voltage in voltage headroom for $V_{O.}$

3.3.2 High-Swing Cascode Current Mirror

The main drawback of self-biased cascode current mirrors is a very serious loss of signal swing, which is especially critical for low supply voltages. As previously discussed, the minimum output voltage required to keep M4 in saturation, where $V_{G1} \cong V_{DS2}$ is usually relatively larger thanV_{DSsat2}. Thus, the minimum output voltage necessary to keep M4 in

saturation can be reduced if a scheme for decreasing V_{DS2} is devised, such a scheme is shown in figure 3.4. The basic idea behind the circuit shown in Figure 3.4 is to generate a voltage V_{DS2} that is just enough to bias the drain-to-source voltage of M2 close to V_{DSsat2}.

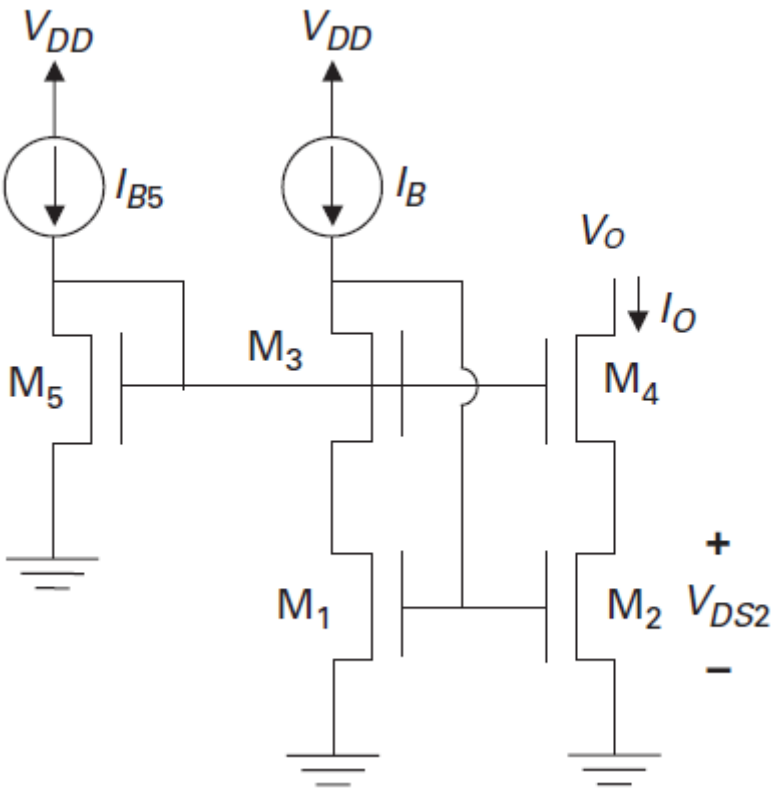


Figure 3.4: A high-swing cascode current mirror. [12]

The minimum output voltage required to keep the M2 and M4 in saturation region is $2V_{DSsat2}$. Also this current source has high output impedance. It has good current matching capability since M1 and M2 have equal V_{GS} and equal V_{DS} values. Therefore, in practical circuits the high swing cascode current mirror of Figure 3.4 is used, since this structure does not exhibit the mentioned disadvantage of the normal cascode current mirror. We use the high-swing cascoded current mirror to maximize robustness over process and supply voltage variation while also providing excellent current mirroring.

CHAPTER 4

HIGH-SPEED, LOW-OFFSET COMPARATOR

The comparator is a circuit that compares an analog signal with another analog signal or reference and outputs a binary signal based on comparison. A simple comparator is an op-amp without compensation. In effect, the comparator can be viewed as a one-bit analog-to-digital converter and it serves as the front-end circuit of most analog-to-digital converters. Besides being key components of A/D converters, comparators are also widely used in level detection, on-off controls, clock-recovery circuits, window detectors, and Schmitt triggers. Comparators are generally used in open-loop mode and so it is not necessary to compensate the comparator. Comparators can be classified into two types depending on architecture. Static comparators are those which perform threshold detection based on the input and a reference without a clocking mechanism. Dynamic comparators on the other hand, make use of the phase/time based clocking mechanism to perform the switching action. The speed of the clocking mechanism defines the speed of the comparator. Since no compensation is needed, it has the largest bandwidth possible which gives a faster response. In this chapter, the background of comparators and high performance comparators are discussed.

4.1 COMPARATOR

The comparator can be thought of as a decision-making circuit. In a comparator circuit, if the input voltage is higher than the reference voltage, the output swings to a voltage representing logic **1,** whereas if the input voltage is less than the reference voltage, the output swings to a voltage representing logic **0**. The circuit symbol of the comparator is shown below in Figure 4.1.The output of the device in the digital that is in binary format.

If $V_{in+} \geq V_{in-}$ then $V_{OUT} = VDD \text{ or } V_{OH}$ (4.1)

Else if $V_{in+} < V_{in-}$ then $V_{OUT} = GND \text{ or } V_{OL}$ (4.2)

Where V_{OH} & V_{OL} are the output voltage levels for high and low output signal and V_{in+} & V_{in-} are the input voltage signals to be compared.

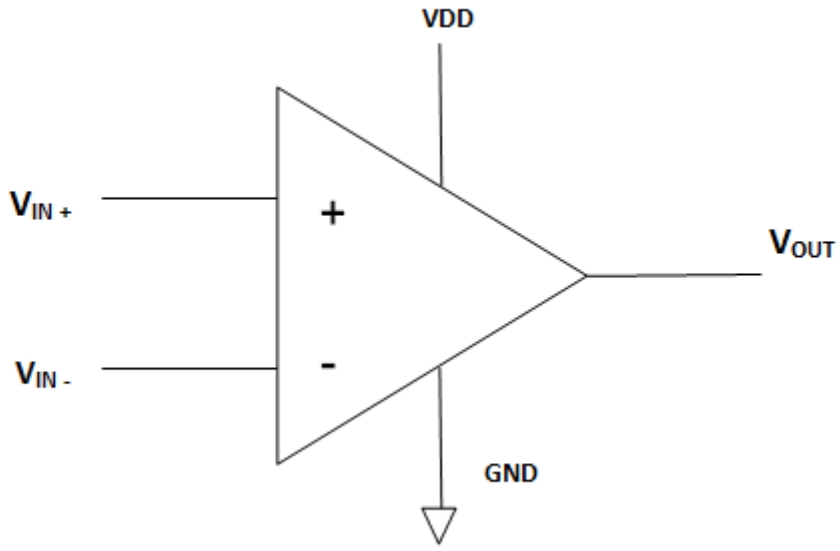


Figure 4.1: Circuit symbol of the Comparator. [11]

4.2 COMPARATOR PERFORMANCE METRICS

Comparators are characterized by Static and Dynamic characteristics.

4.2.1 STATIC CHARACTERISTICS

Static characteristics comprises of gain, resolution, input offset voltage & noise.

Gain: The DC-gain of a comparator is defined as the ratio between, the difference of high and low output signal voltage and the difference of high and low input signal voltage. The transfer curve of an ideal comparator with infinite gain is shown in Figure 4.2.

$$V_O = \begin{cases} V_{OH} & \text{if } V_{in+} - V_{in-} > 0 \\ V_{OL} & \text{if } V_{in+} - V_{in-} < 0 \end{cases} \quad (4.3)$$

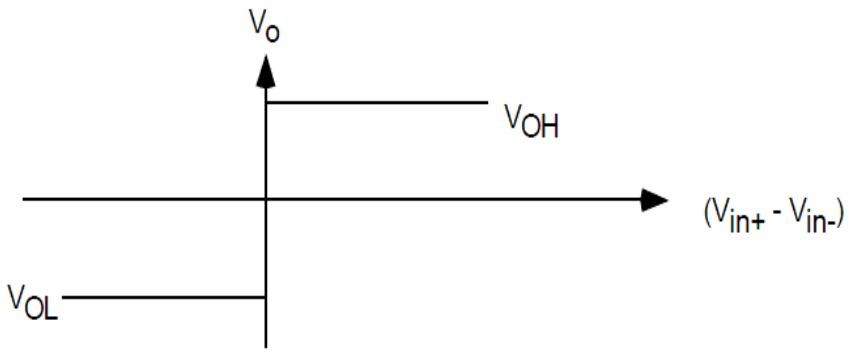


Figure 4.2: Transfer curve of an ideal comparator with infinite gain. [11]

A comparator with infinite gain is not realizable. Figure 4.3 shows a more realistic piecewise linear transfer curve of a comparator. The Gain can be expressed as $A_V = \frac{V_{OH}-V_{OL}}{V_{IH}-V_{IL}}$

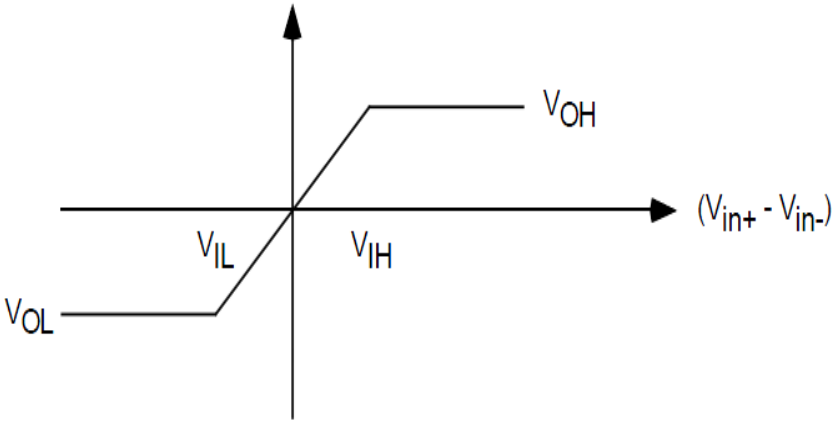


Figure 4.3: Transfer curve of the comparator with finite gain. [11]

Where, V_{IH} and V_{IL} are the input voltage difference needed to just saturate the output at its upper and lower limit, respectively. Gain is very important characteristic describing comparator operation. It defines the minimum amount of input change (resolution) necessary to make the output swing between two binary states.

The output equations can be defined as follows

$$V_O = \begin{cases} V_{OH} & \text{if } (V_{in+} - V_{in-}) > V_{IH} \\ A_V * (V_{in+} - V_{in-}) & \text{if } V_{IL} < (V_{in+} - V_{in-}) < V_{IH} \\ V_{OL} & \text{if } (V_{in+} - V_{in-}) < V_{IL} \end{cases} \quad (4.4)$$

Input Offset Voltage:

Input offset voltage can be classified as two types.(i) Systematic offset and (ii) Random offset. Offset in the Comparators generates due to input transistor mismatches (i.e. mismatches in the threshold voltages and mismatches in the trans-conductance parameter $\beta = \mu Cox \frac{W}{L}$).The output changes as the input differences crosses zero as shown in Figure 4.3.If the output did not change until the input difference reached a value Vos then this difference would be defined as the offset voltage shown in Figure 4.4.

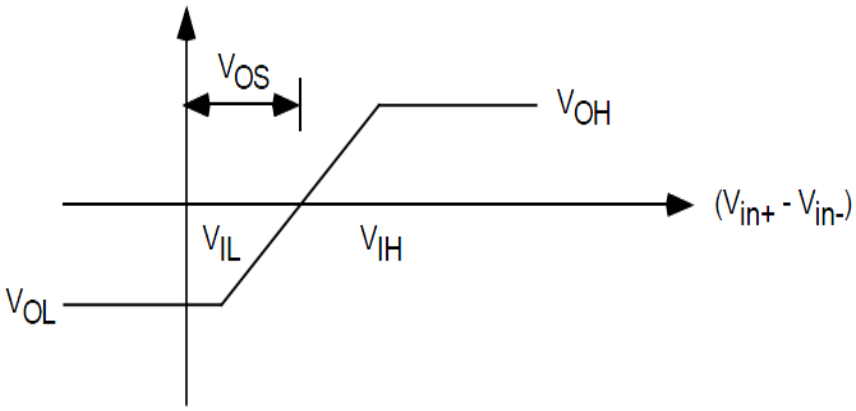


Figure 4.4: Transfer curve of the comparator including input-offset voltage. [11]

This would not be a problem if the offset could be predicted, but it varies randomly from the circuit to circuit for a given design. The sign of Vos is unknown in polarity. The offset voltage can be formally defined as the input level which forces the output voltage to go to zero. It can limit the resolution of the comparator, thus adversely affecting the accuracy of the comparator and the ADC it is used in.

4.2.2 DYNAMIC CHARACTERISTICS

Dynamic characteristics of comparator comprises of speed or propagation time delay. The dynamic characteristics of the comparator include both small-signal and large-signal behavior. We do not know, at this point, how long it takes for the comparator to respond to the given differential input. The characteristic delay between input excitation and output transition is the time response of the comparator.

Propagation Delay:

The propagation delay of a comparator is the total time elapsed between input excitation and output response of the comparator. It is measured as the difference between the time input signal crosses half the minimum input signal and the time the output reaches its mean value. It is a very important dynamic characteristic, as it limits the conversion rate of the comparator, in turn limiting the speed of the ADC it is used in. The propagation delay can be calculated as

$$\text{Propagation delay or } t_P = \frac{t_{LH} + t_{HL}}{2} \qquad (4.5)$$

t_{LH} = The delay time between the input and output, when the output switching the levels from low to high.

t_{HL} = The delay time between the input and output, when the output switching the levels from high to low.

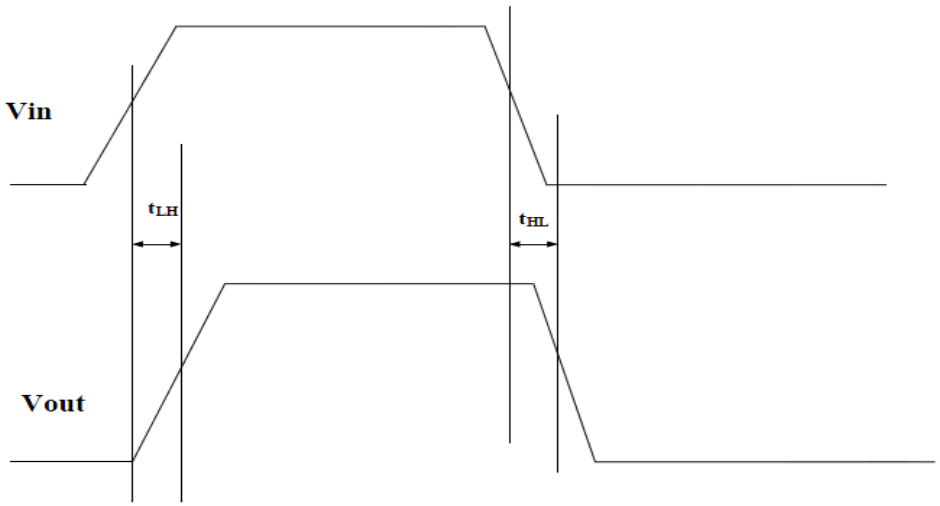


Figure 4.5: Propagation delay definition for a comparator. [11]

The propagation delay time of the comparators generally varies as a function of the amplitude of the input. A larger input will result in a smaller delay time. There is an upper limit at which further increases in the input voltage will no longer affect the delay .This mode of operation is called slewing or slew rate. Slew rate can be defined as the rate of change of output voltage with respect to time.

$$SR = \frac{dV_O}{dt} \tag{4.6}$$

If the rate of rise or fall of a comparator becomes large, the dynamics may be limited by the slew rate. Slew-rate comes from the relationship,

$$I = C\frac{dV}{dt} \tag{4.7}$$

Where I is the current through a capacitor and V is the voltage across it. If the current becomes limited, then the voltage rate becomes limited. Therefore for a comparator that is slew rate limited we have,

$$t_P = \frac{\Delta V}{SR} = \frac{(V_{OH} - V_{OL})}{2 * SR} \tag{4.8}$$

where SR=slew rate of Comparator.

4.3 HIGH PERFORMANCE COMPARATOR

A block diagram of a high-performance comparator is shown in the figure 4.6 below. The comparator consists of three stages.

1. Input preamplifier stage
2. Positive feedback or decision stage
3. An output buffer stage

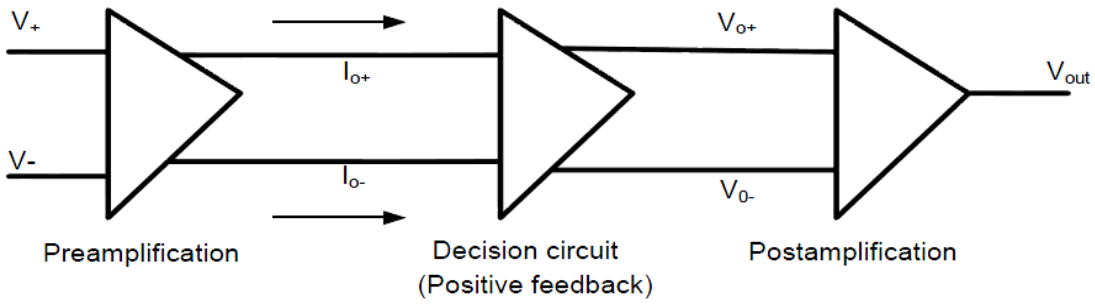


Figure 4.6: Block diagram of high-performance voltage comparator. [11]

The pre-amp stage amplifies the input signal to improve the comparator sensitivity (i.e. increases the minimum input signal with which the comparator can make a decision) and isolates the input of the comparator from switching noise coming from the positive feedback stage. The positive feedback stage is used to determine which of the input signal is larger. The output buffer amplifies this information and outputs a digital signal. Designing a comparator can begin with considering input common mode range, power dissipation, propagation delay and comparator gain.

PRE-AMPLIFICATION STAGE:

The preamp stage amplifies the input signal to improve the comparator sensitivity. i.e., increases the minimum input signal with which the comparator can make a decision and isolates the input of the comparator from switching noise coming from the positive feedback stage. The schematic of the pre-amplification stage of the comparator is shown in the figure 4.7 below. The Pre-amplifier consists of the differential amplifier with active loads or resistive load. In many CMOS technologies, it is difficult to fabricate resistors with tight controlled values or a reasonable physical size. Consequently, it is desirable to replace

resistor with a MOS transistor. A MOS can be operated as a resistor if its gate and drain are shorted. The design of the preamplifier must be done in such a manner that the desired latch input voltage is achieved in minimum time. This means that the bandwidth must be as large

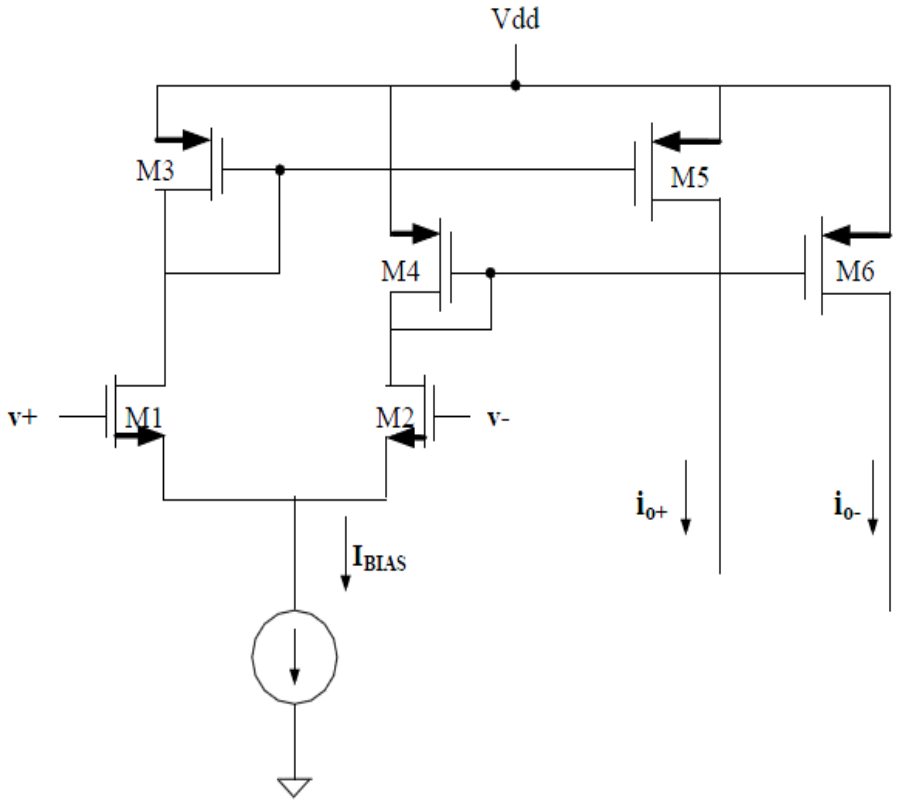


Figure 4.7: Pre-amplification stage of the comparator. [11]

as possible. We know that the gain-bandwidth product is normally constant. The low gain preamplifiers must compromise between a high bandwidth and sufficient gain. The sources of offsets in the preamplifier are the mismatch between the input transistors of differential pair.

DECISION STAGE:

The decision stage is the heart of this comparator and is used to determine which of the input signals is larger (i.e. should be capable of discriminating mV level signals). The schematic of the decision stage of the comparator is shown in the figure 4.8 below. This circuit uses positive feedback from the cross-gate connection of M6 and M7 to increase the gain of the decision element. Hysteresis can be part of the design in the decision circuit.

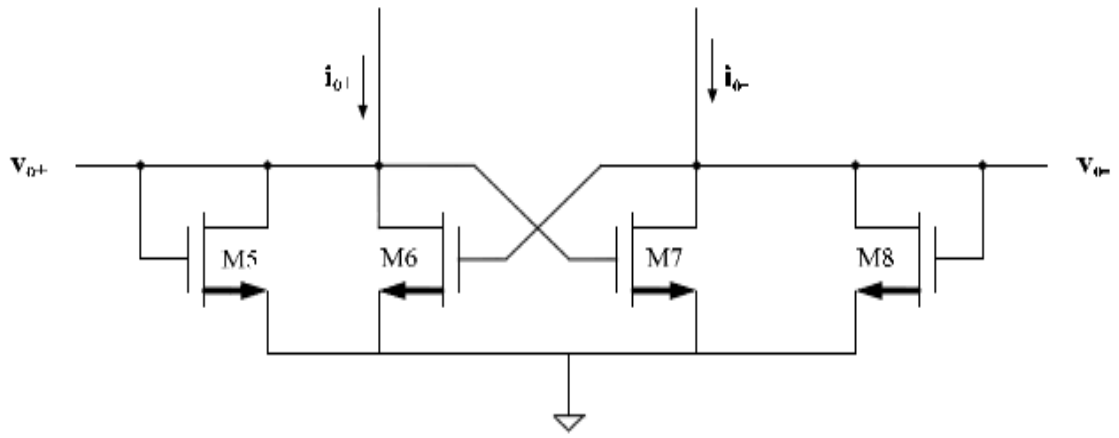


Figure 4.8: Positive feedback decision circuit. [11]

Assuming that $i_{o+} > i_{o-}$, M5 and M7 are on and M6 and M8 are off. Also assume that $\beta_5 = \beta_8 = \beta_A$ and $\beta_6 = \beta_7 = \beta_B$ where β_5, β_6, β_7, β_8 are the trans-conductance parameters of the transistors M5, M6, M7 and M8 respectively. Under these assumptions $V_O(-)$ is approximately 0 V and $V_O(+)$ is

$$V_O(+) = \sqrt{\frac{2 * i_O(+)}{\beta_A}} + V_{TH} \tag{4.9}$$

If i_{o-} is increased and i_{o+} is decreased, switching takes place when the drain-source voltage of M7 is equal to V_{TH} of M6. So M6 turns on and M7 shuts off. At this point, i_{o-} is given by

$$i_O(-) = \frac{\beta_B}{\beta_A} * i_O(+) \tag{4.10}$$

A similar analysis for increasing i_{o+} and decreasing i_{o-} yields a switching point of

$$i_O(+) = \frac{\beta_B}{\beta_A} * i_O(-) \tag{4.11}$$

The circuit can be designed to add hysteresis to it.

OUTPUT BUFFER STAGE:

This stage is also called post-amplifier stage. The main purpose of the output buffer is to convert the output of the decision circuit into a logic signal. The output buffer should accept a differential input signal and not have slew-rate limitations. This circuit is a self-biased differential amplifier.

This self-biased differential amplifier is also called a Fully Complementary Self-Biased CMOS Differential Amplifier (CSDA). In the CSDA, devices top and bottom transistors operate in the linear region. Consequently, the voltages on their drain may be set very close to the supply voltages. Since these two voltages determine the output swing of the amplifier, the output swing can be very close to the difference between the two supply rails. This large output swing makes interfacing the CSDA to ordinary CMOS logic gates straightforward, since it provides a large margin for variations in the logic threshold of the gates. Another consequence of the linear-region operation of devices is that the CSDA can provide output switching currents that are significantly greater than its quiescent current. This capability of supplying momentarily large current pulses makes the CSDA especially suitable for high-speed comparator applications, where it is necessary to rapidly charge and discharge output capacitive loads without at the same time consuming inordinate amounts of power.

The circuit configuration of this amplifier differs from those of conventional CMOS differential amplifier configurations in two important ways:

1) The amplifiers are completely complementary, i.e., each n-type device operates in push-pull fashion with a corresponding p-type device.

2) The amplifiers are self-biased through negative feedback.

These two differences in the amplifier configurations result in several performance enhancements: Less sensitivity of active-region biasing to variations in processing, temperature and supply & capability of supplying switching currents that are significant greater than the quiescent bias current.

These performance enhancements are particularly desirable in comparator applications in commercial digital CMOS VLSI integrated circuits, where precision, high speed, ease of interfacing to ordinary logic gates, consistently high producing yields are required. This amplifier consists of two differential amplifiers each serving as the load for other. An inverter pair will add on the output of the amplifier to isolate any load capacitance from the self-based differential amplifier.

CHAPTER 5

Gm/Id BASED DESIGN

5.1 INTRODUCTION

The long channel MOS devices with length greater than 2µm, generally follows the "square-law" models, where hand calculation and simulation results are comparable. The long-channel MOS followed analytical and matched SPICE (Simulation Program with Integrated Circuit Emphasis) level 1 and 2 models. These models yield simulation result that match hand-calculations and gives us feedback. Given a set of design specifications, we may start our design by using simple hand analysis equations.

As the dimensions of MOSFET continue to scale down, square-law model becomes less accurate. Modern MOS transistors have become nonlinear, non-ideal behavior so paper-pencil analysis is almost impossible and we need simulation to accurately predict the detailed circuit behavior. In today's small dimension MOS transistor, BSIM (Berkeley Short Channel IGFET Model) is more accurate, silicon proven and widely accepted in the industry. However, when we open the modern device models such as BSIM model, usually we can't find µ.Cox, lambda or any parameters that we are familiar with. The equations used in BSIM models or any other models are too complicated for hand analysis. There is a huge discrepancy between modern CMOS models and traditional square law equations. All these discrepancies posing a challenge for modern circuit designer, as shown in Figure 5.1

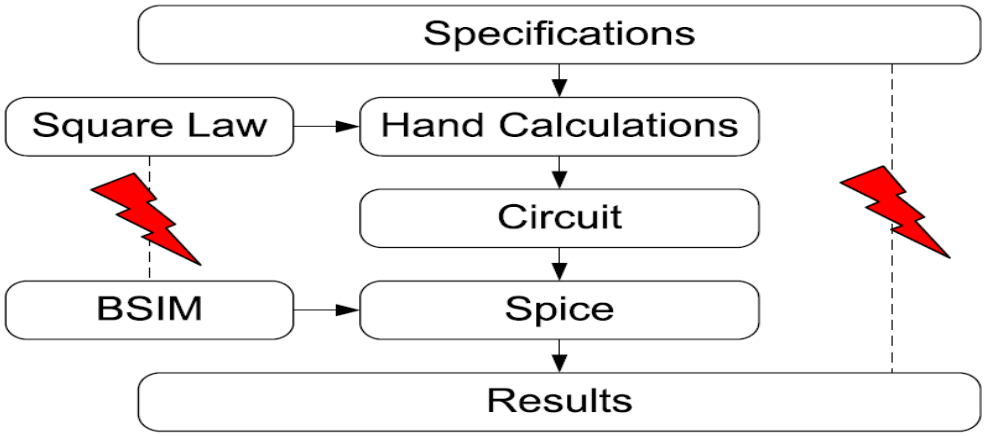
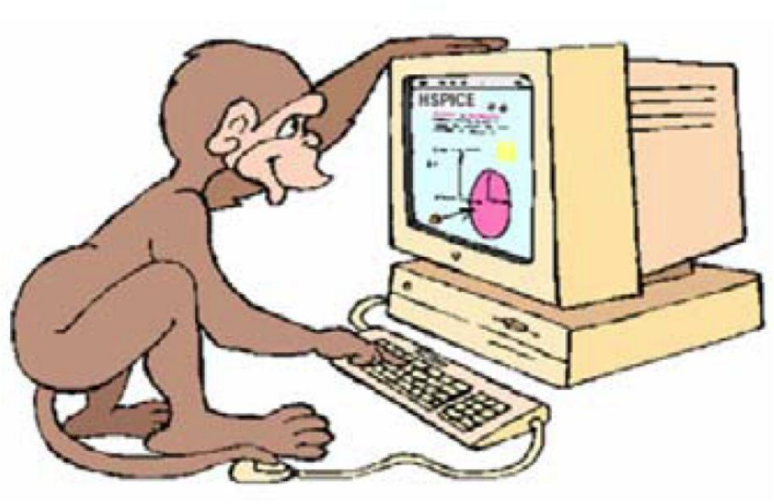


Figure 5.1: The Problem. [14]

The lack of good hand analysis models to design circuits forcing many designers to give up hand calculations; they iterate their design problem in the simulators until they somehow meet the design specs. Even the circuit meet the design targets; usually the design is not guarantee to be optimal. In other words, this issue or challenge turns many designers into "SPICE Monkey", Figure 5.2. Normally, any design should be based on a systematic analysis and reasonable considerations, the simulator is just a calculator to check the design meet the specs or not.



[Courtesy Isaac Martinez]

Figure 5.2: SPICE Monkey [14]

There are many versions of BSIM models that grew with time. BSIM versions 1, 2, 3v3 and 4 are implemented as SPICE level 13, 39, 49 and 54 respectively. In the present work BSIM3v3 (Level 49) model has been used. It is good for circuit simulation except it does not model gate leakage, which is supported in BSIM4 along with other very thin gate effects.

5.2 DESIGN PARAMETERS

The long-channel design has different set of equations which govern each region of operation. The overdrive voltage Vov is a key parameter which defines the region the device is operating in. The g_m/I_d method characterizes the performance of a transistor in all regions of operation. The following section develops the long-channel equations of the transistor. From these equations we derive the figure of merits for the g_m/I_d method.

Triode Region

The current equation of MOSFET using square law model operating in the triode region is:

$$I_D = \mu C_{OX} \frac{W}{L} \left[(V_{GS} - V_{TH}) - \frac{V_{DS}}{2} \right] . V_{DS} \quad (5.1)$$

Saturation Region

The current equation of MOSFET operating in the triode region is:

$$I_D = \frac{1}{2} \mu C_{OX} \frac{W}{L} [(V_{GS} - V_{TH})^2] \quad (5.2)$$

Trans-conductance

The trans-conductance g_m of MOSFET operating in the saturation region is:

$$g_m = \frac{dI_D}{dV_{GS}} = \mu Cox \frac{W}{L} (V_{GS} - V_{TH}) = \mu Cox \frac{W}{L} Vov \quad (5.3)$$

$$g_m = \sqrt{2I_D \, \mu Cox \frac{W}{L}} = \frac{2I_D}{V_{OV}} \quad (5.4)$$

The overdrive voltage V_{OV} or so called V_{DSAT} or $V_{GS} - V_{TH}$ tells us two things, swing and trans-conductance efficiency. The lower the V_{OD}, the higher the swing and more g_m you get per unit current you spent.

Output Conductance with Channel Length Modulation

The output conductance of MOSFET has the following equations:

$$g_{ds} = \frac{dI_D}{dV_{DS}} = \frac{d}{dV_{DS}} \left[\frac{1}{2} \mu Cox \frac{W}{L} (V_{GS} - V_{TH})^2 (1 + \lambda V_{DS}) \right] \quad (5.5)$$

$$g_{ds} = \frac{1}{2} \mu Cox \frac{W}{L} (V_{GS} - V_{TH})^2 \lambda = \frac{\lambda I_D}{1 + \lambda V_{DS}} \simeq \lambda I_D \quad (5.6)$$

Intrinsic Gate Capacitances

The intrinsic gate capacitance of MOSFET can be expressed as:

$$Cgg \cong Cgs + Cgb + Cgd \quad (5.7)$$

The performance of any analog circuit can be broadly divided into its large signal and small signal characteristics. The current I_D determines the power dissipation, voltage V_{DS} the

available signal swing (both the ICMR and ODR), trans-conductance gm signifies speed and voltage gain, the intrinsic capacitances Cgs, Cgd, Cgb determine the speed and the output impedance, r_O determines the voltage gain of the circuit. Summarizing the above we have

DC Voltage Gain

$$A_{dc} = g_m * r_O \tag{5.8}$$

Bandwidth

$$F_{transit} = \frac{1}{2 * 3.14 * R_{IN} * Cgg} \tag{5.9}$$

Power Dissipation

$$P = V_{DD} * I_D \tag{5.10}$$

5.3 FIGURE OF MERIT PARAMETERS

We can now define certain figure of merits for the technology characterization in the g_m/I_d based method.

Trans-conductor Efficiency

$$\frac{g_m}{I_d} = \frac{2}{V_{OV}} \tag{5.11}$$

Transit Frequency

$$\frac{g_m}{Cgg} \cong \frac{3}{2}\frac{\mu V_{OV}}{L^2} \tag{5.12}$$

Intrinsic Gain

$$\frac{g_m}{g_{ds}} \cong \frac{2}{\lambda V_{OV}} \tag{5.13}$$

The equations on the right hand side are derived from the square law equations.

5.3.1 Trans-conductance Efficiency as Design Parameter

We can always determine the g_m/I_d ratio of any MOSFET. All we have to do is take the device and measure its current. To get g_m, we take the derivative of that drain current with

respect to gate voltage. By using simulator, we can always determine the g_m/I_d regardless of any short channel effect or complex modeling equations. We can always plot g_m vs. ID of MOSFET for any process technology because it is a pure DC metric. From Fig. 5.3 we know that before the moderate inversion or sub-threshold regions, the curve can be approximated by $\frac{\text{Gm}}{\text{Id}} = \frac{2}{\text{Vov}}$ .The equation used in the sub-threshold region is $\frac{\text{Gm}}{\text{Id}} = \frac{1}{\text{nKT/q}}$. Fig. 5.4, we can see that the trans-conductance efficiency metric is mostly independent of device types.

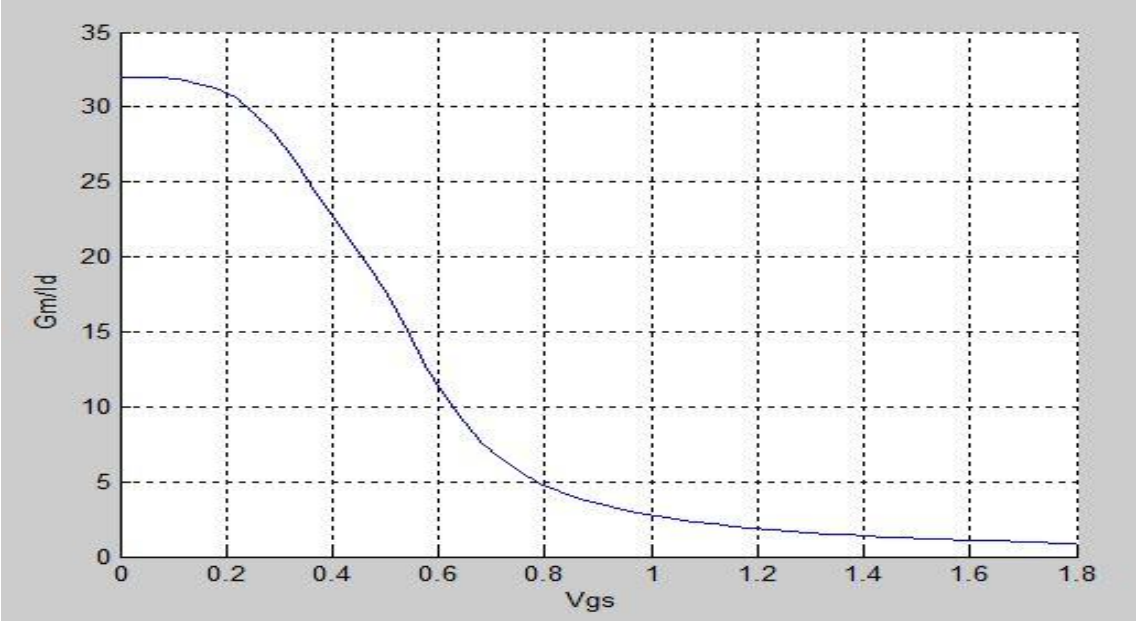


Figure 5.3: Figure of Merit.

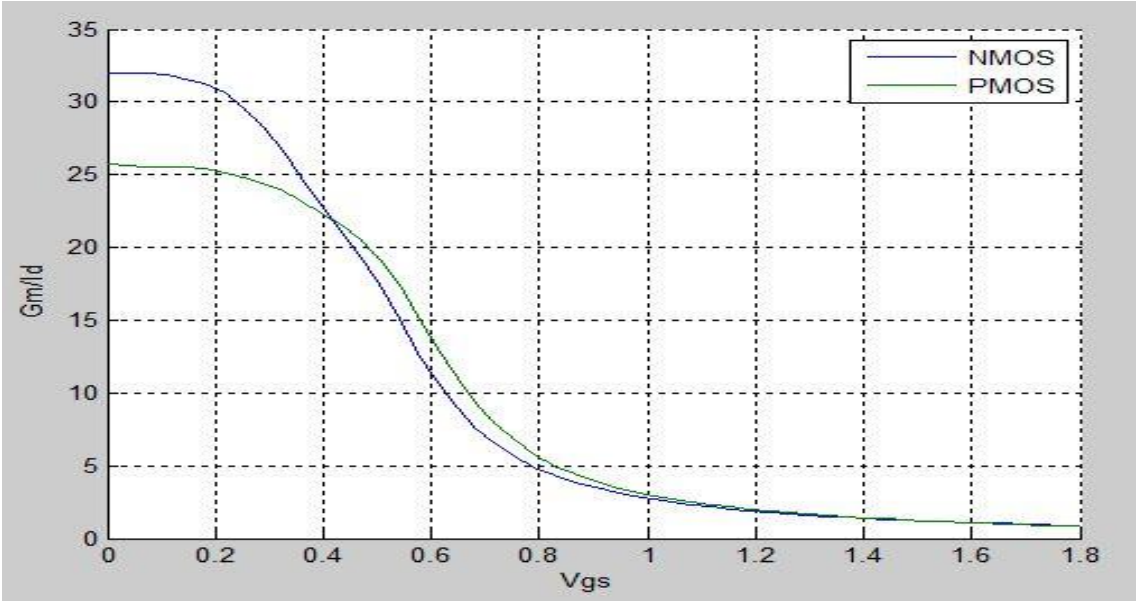


Figure 5.4: Figure of Merit for NMOS and PMOS.

5.3.2 Overdrive Voltage (V*)

After we see that the trans-conductance efficiency is a good design parameter, we can take equation 5.14 and define a new parameter called V* [16].

$$\frac{g_m}{I_d} = \frac{2}{(V_{GS} - V_{TH})} = \frac{2}{V_{OV}} \tag{5.14}$$

$$V^* = \frac{2 * I_d}{g_m} \Leftrightarrow \frac{g_m}{I_d} = \frac{2}{V^*} \tag{5.15}$$

In square law model, $V^* = V_{DSAT} = V_{OV} = V_{OD} = V_{GS}-V_{TH}$ as we can see in equation (2.8a).We define V* for modern MOSFET not because real device behave like square law device. Because it is simple and useful, it allows us to by analogy, think about how to pick V* in the same way as to pick V_{OD} for the square law device. We already know that the real MOSFET do not obey square law equations. So how does V* work? For example, if we have a V* = 200mV, that means we have $\frac{g_m}{I_d} = 10V^{-1}$. If we lower the V*, for the same current, we will have better trans-conductance efficiency and potentially higher swing, we will have larger device, therefore, more parasitic capacitance.

By taking a MOSFET and connect its gate and drain and doing a voltage sweep in the simulator, we can plot Vgs vs. ft and g_m/I_d. Based on the plot we found that if we make Vgs larger, generally we will get more gm and the ft will go up. Therefore, if we want fast device, we want large Vgs and device with smaller channel length, but if we want a good current efficiency, we want low V_{GS} (low current density region) to operate the device in moderate or weak inversion region. To have higher trans-conductance efficiency, the Vgs is lower and the device is larger, which means we have lower g_m per unit capacitance, therefore, it is slower.

5.4 g_m/I_d GRAPHS

The next step in the g_m/I_d approach is the generation of plots which are useful for hand analysis. Figure 3.5 shows an N-Channel Metal Oxide Semiconductor (NMOS) transistor setup in cadence which is used for generating the plots. In a similar manner Figure 5.6 shows a P-Channel Metal Oxide Semiconductor (PMOS) transistor setup to obtain the g_m/I_d graphs. A family of curves for NMOS and PMOS transistors are obtained for various transistor lengths 0.18um, 0.2um, 0.22um, 0.24um, 0.26um, 0.35um, 0.36um are the lengths of

transistors chosen for simulation in the TSMC 0.18µm process. The obtain plots have been obtained as following:

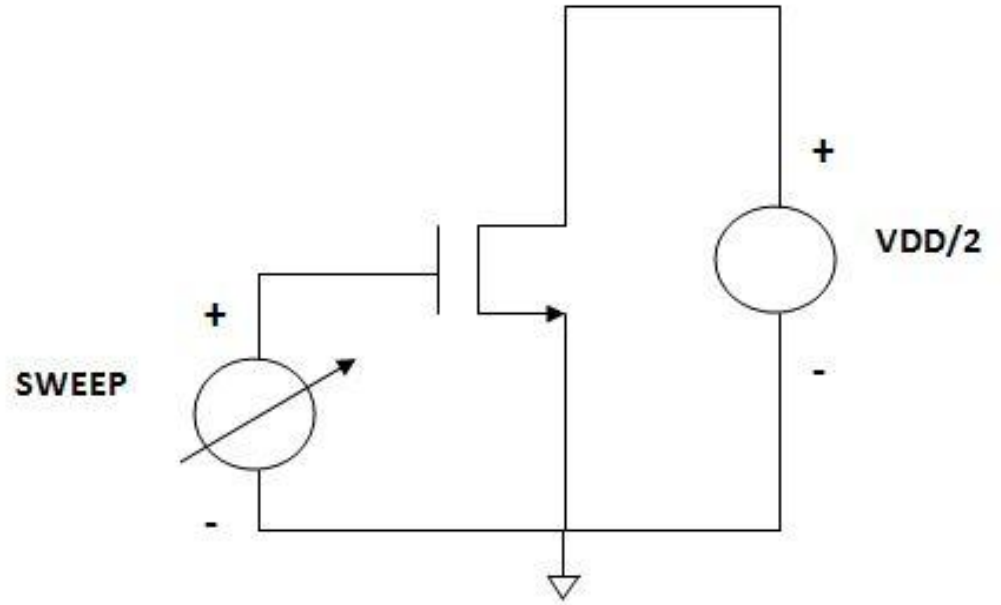


Figure 5.5: Schematic of the NMOS transistor.

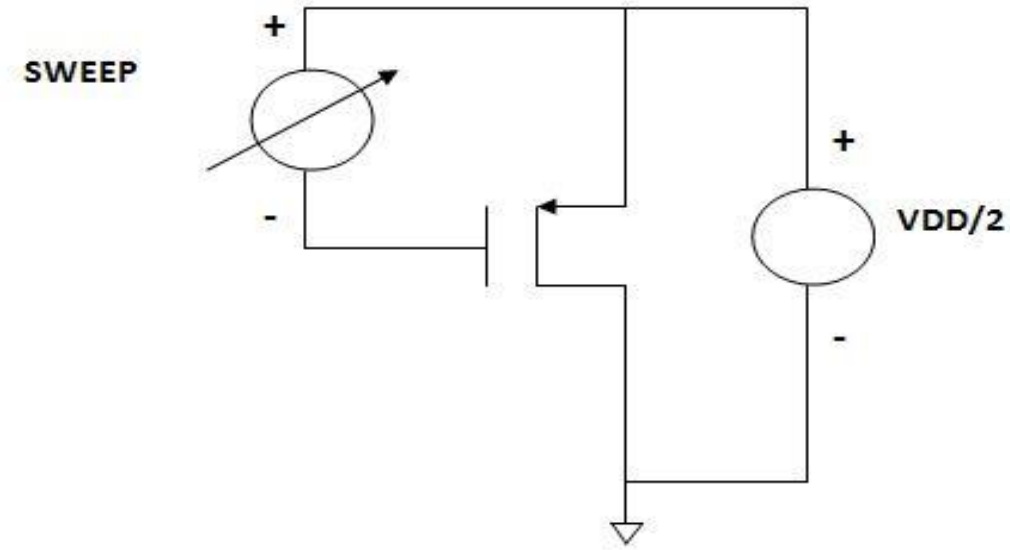


Figure 5.6: Schematic of the PMOS transistor.

The following plots have been obtained:

Ft vs g_m/I_d Plot or Transit Frequency Plot

- Figure 5.7(a) shows the plot of NMOS device.
- Figure 5.7(b) shows the plot of PMOS device.
- Figure 5.7(c) shows the plot of NMOS device with different transistor lengths.
- Figure 5.7(d) shows the plot of PMOS device with different transistor lengths.

Gm*r0 vs g_m/I_d Plot or Intrinsic Gain Plot

- Figure 5.8(a) shows the plot of NMOS device.
- Figure 5.8(b) shows the plot of PMOS device.
- Figure 5.8(c) shows the plot of NMOS device with different transistor lengths.
- Figure 5.8(d) shows the plot of PMOS device with different transistor lengths.

Id/W vs g_m/I_d Plot or Current Density Plot

- Figure 5.9(a) shows the plot of NMOS device.
- Figure 5.9(b) shows the plot of PMOS device.
- Figure 5.9(c) shows the plot of NMOS device with different transistor lengths.
- Figure 5.9(d) shows the plot of PMOS device with different transistor lengths.

g_m/I_d vs V_{OD} Plot or Trans-Conductance Plot

- Figure 5.10(a) shows the plot of NMOS device.
- Figure 5.10(b) shows the plot of PMOS device.
- Figure 5.10(c) shows the plot of NMOS device with different transistor lengths.
- Figure 5.10(d) shows the plot of PMOS device with different transistor lengths.

Ft * (g_m/I_d) vs V_{OD} Plot or FOM (Figure of Merit) Plot

- Figure 5.11(a) shows the plot of NMOS device.
- Figure 5.11(b) shows the plot of PMOS device.
- Figure 5.11(c) shows the plot of NMOS device with different transistor lengths.
- Figure 5.11(d) shows the plot of PMOS device with different transistor lengths.

Vgs vs V_{OD} Plot

- Figure 5.12(a) shows the plot of NMOS device.

- Figure 5.12(b) shows the plot of PMOS device.
- Figure 5.12(c) shows the plot of NMOS device with different transistor lengths.
- Figure 5.12(d) shows the plot of PMOS device with different transistor lengths.

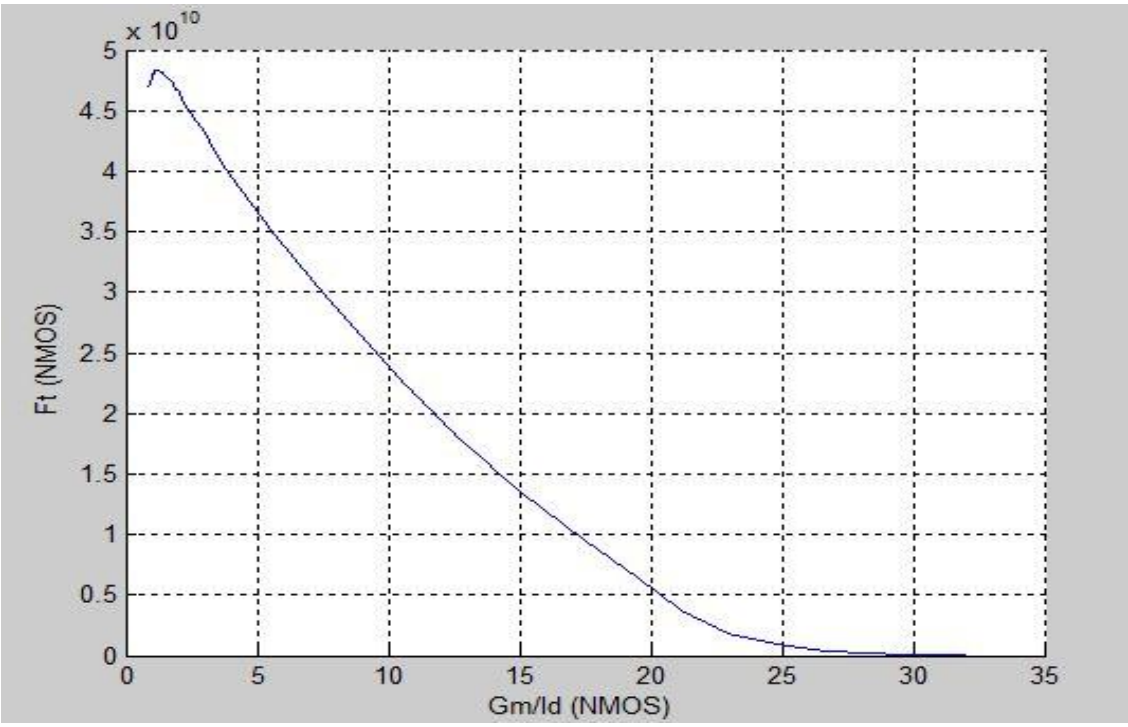


Figure 5.7(a) Ft vs g_m/I_d plot of NMOS device.

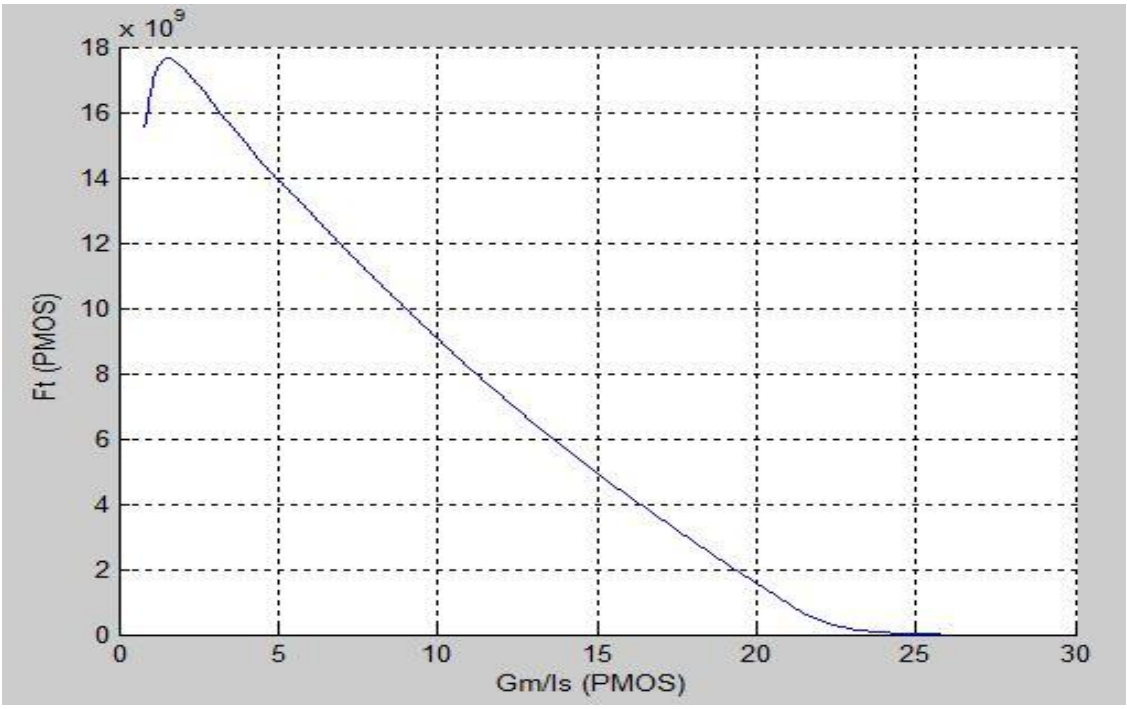


Figure 5.7(b) Ft vs g_m/I_d plot of PMOS device.

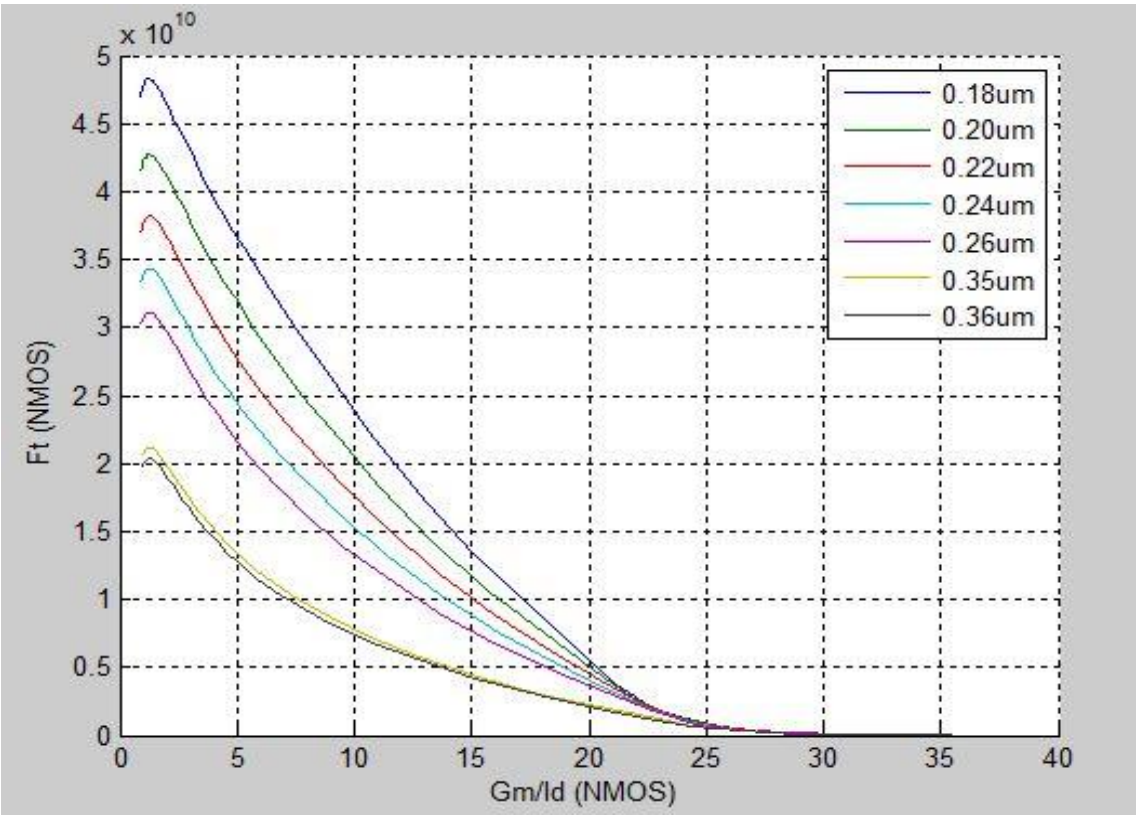


Figure 5.7(c) Ft vs g_m/I_d plot of NMOS device with different transistor lengths.

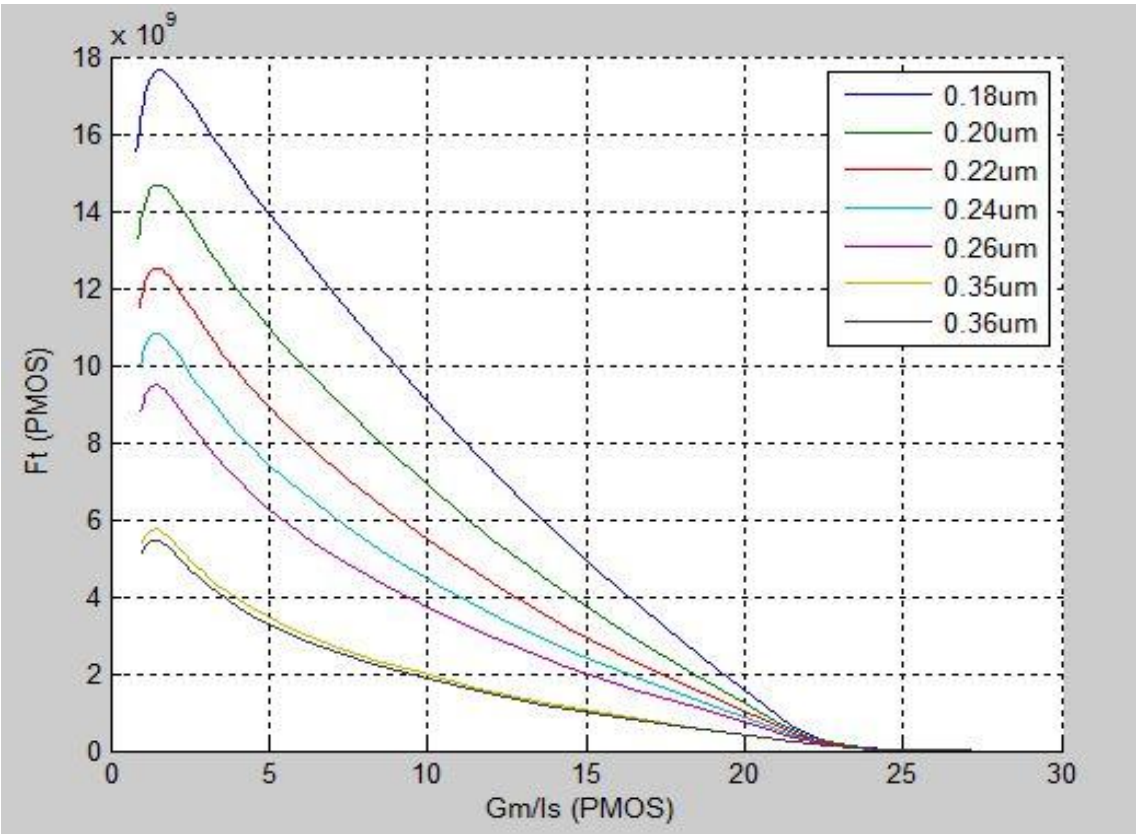


Figure 5.7(d) Ft vs g_m/I_d plot of PMOS device with different transistor lengths.

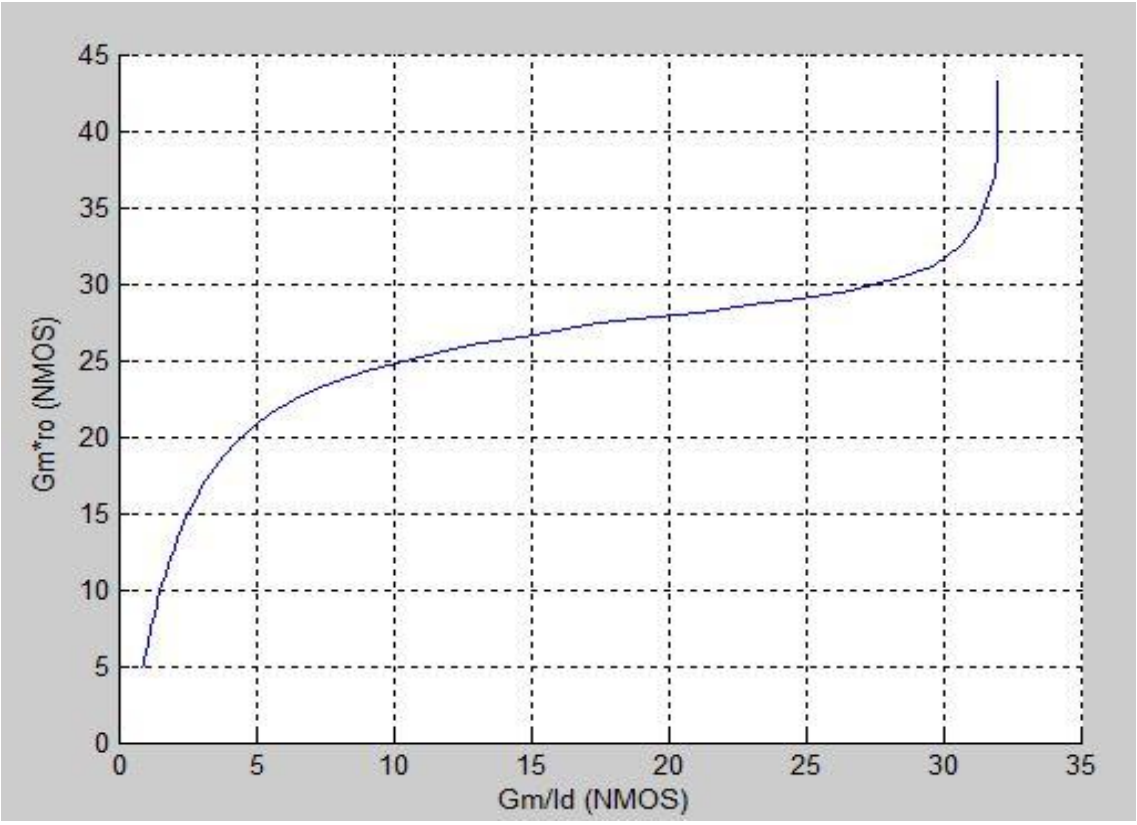


Figure 5.8(a) Gm*r0 vs g_m/I_d plot of NMOS device.

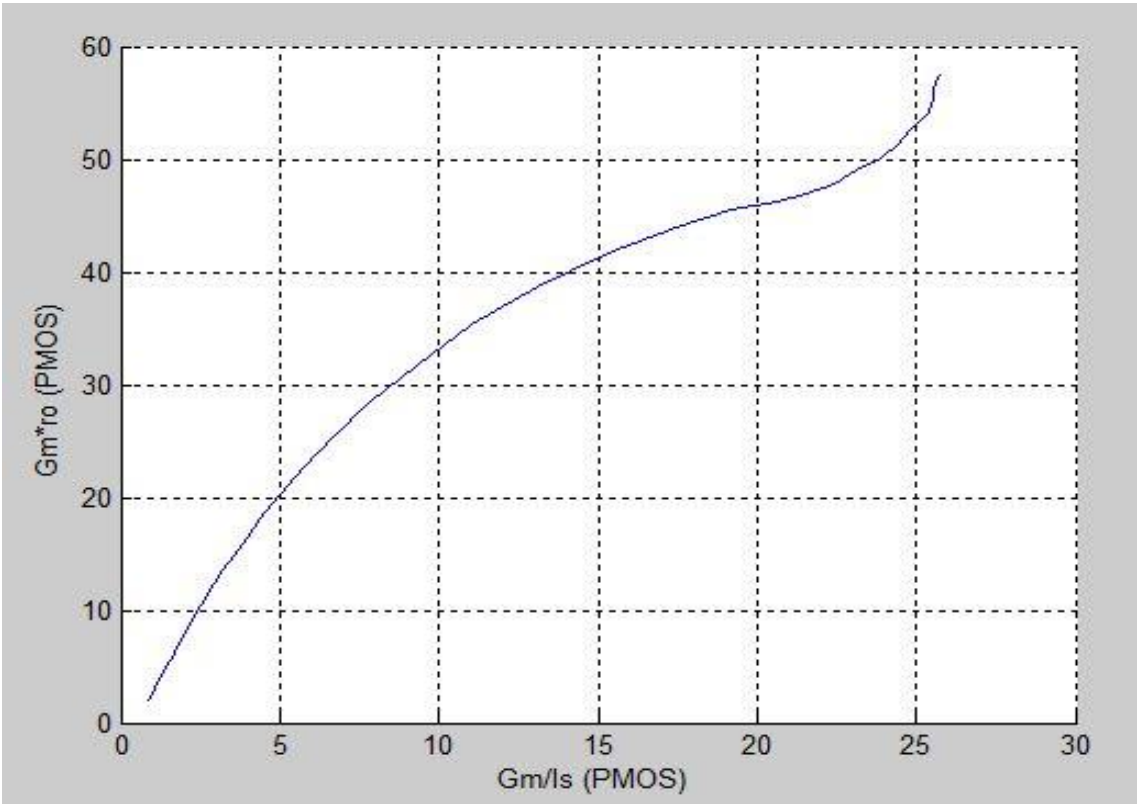


Figure 5.8(b) Gm*r0 vs g_m/I_d plot of PMOS device.

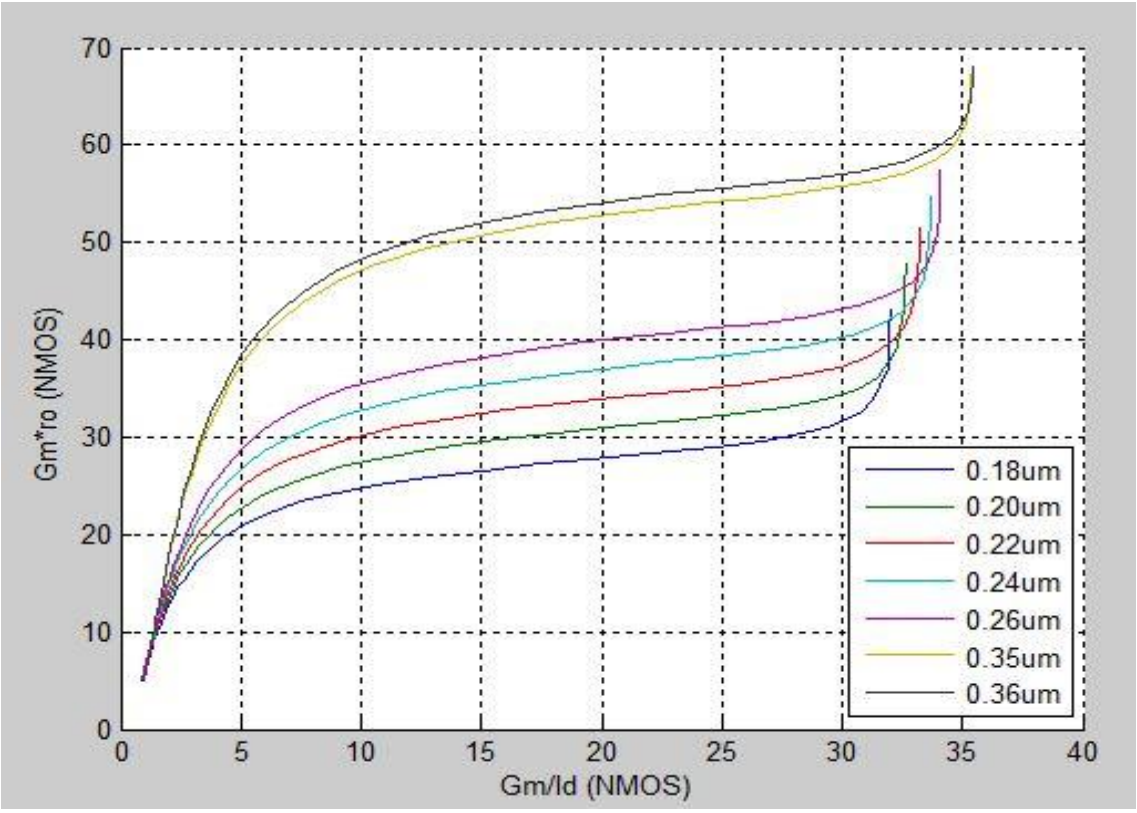


Figure 5.8(c) Gm*r0 vs g_m/I_d plot of NMOS device with different transistor lengths.

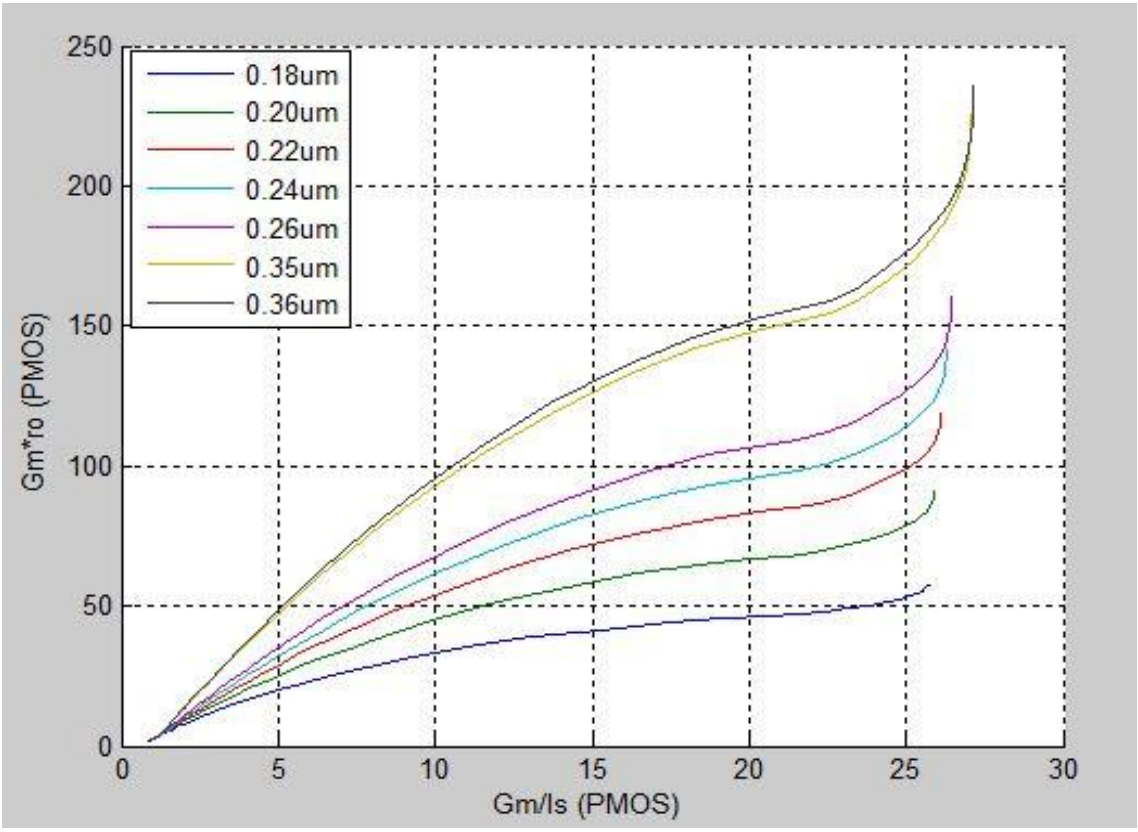


Figure 5.8(d) Gm*r0 vs g_m/I_d plot of PMOS device with different transistor lengths.

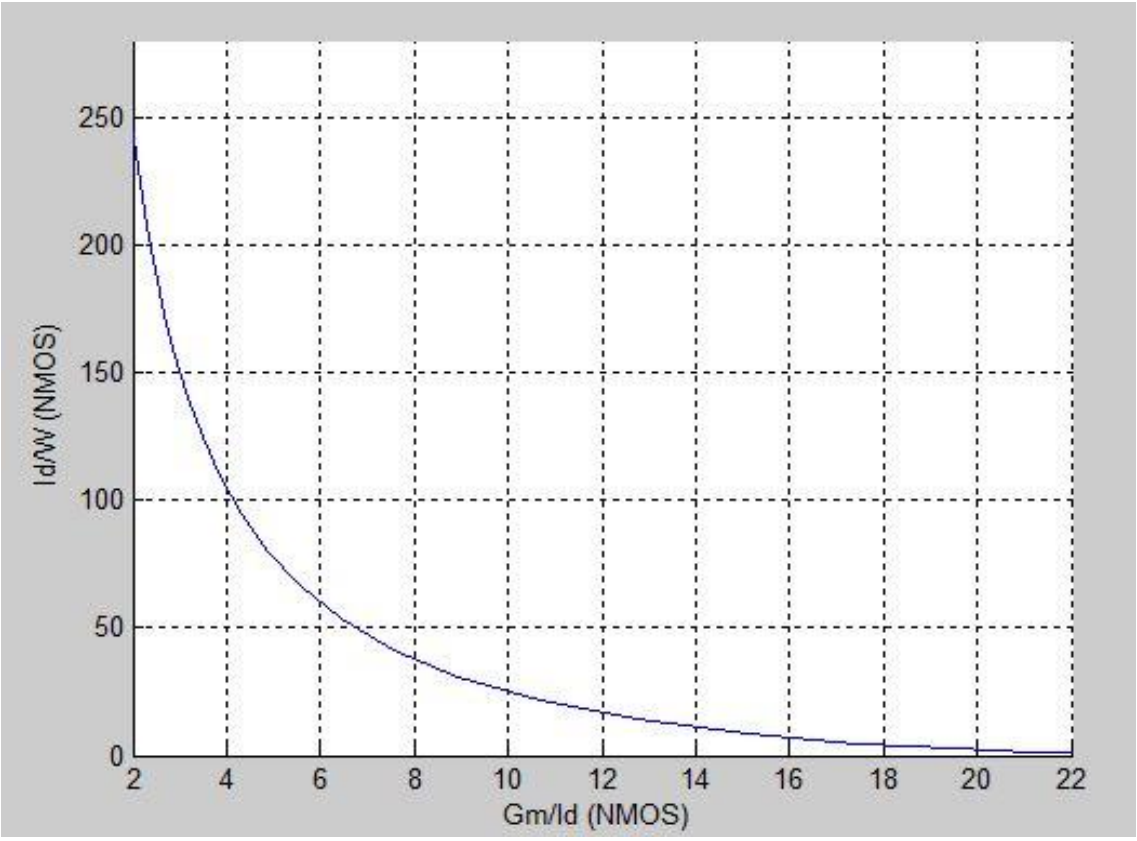


Figure 5.9(a) Id/W vs g_m/I_d Graph plot of NMOS device.

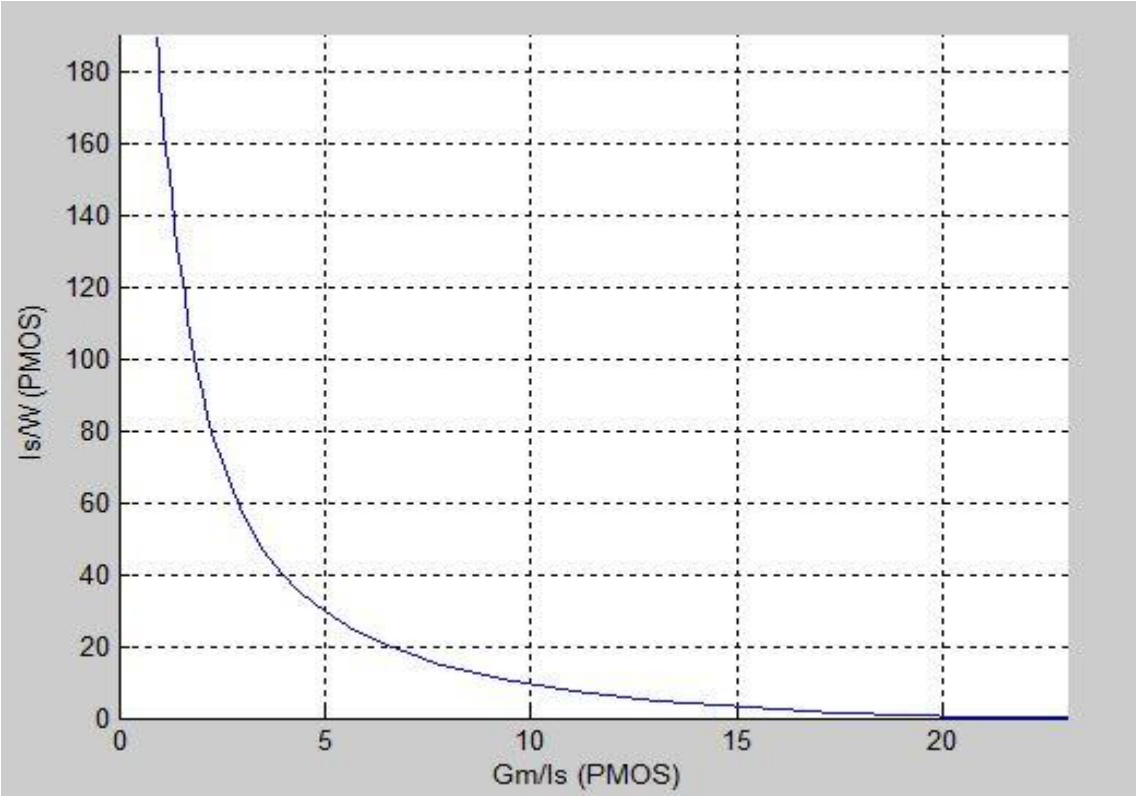


Figure 5.9(b) Id/W vs g_m/I_d plot of PMOS device.

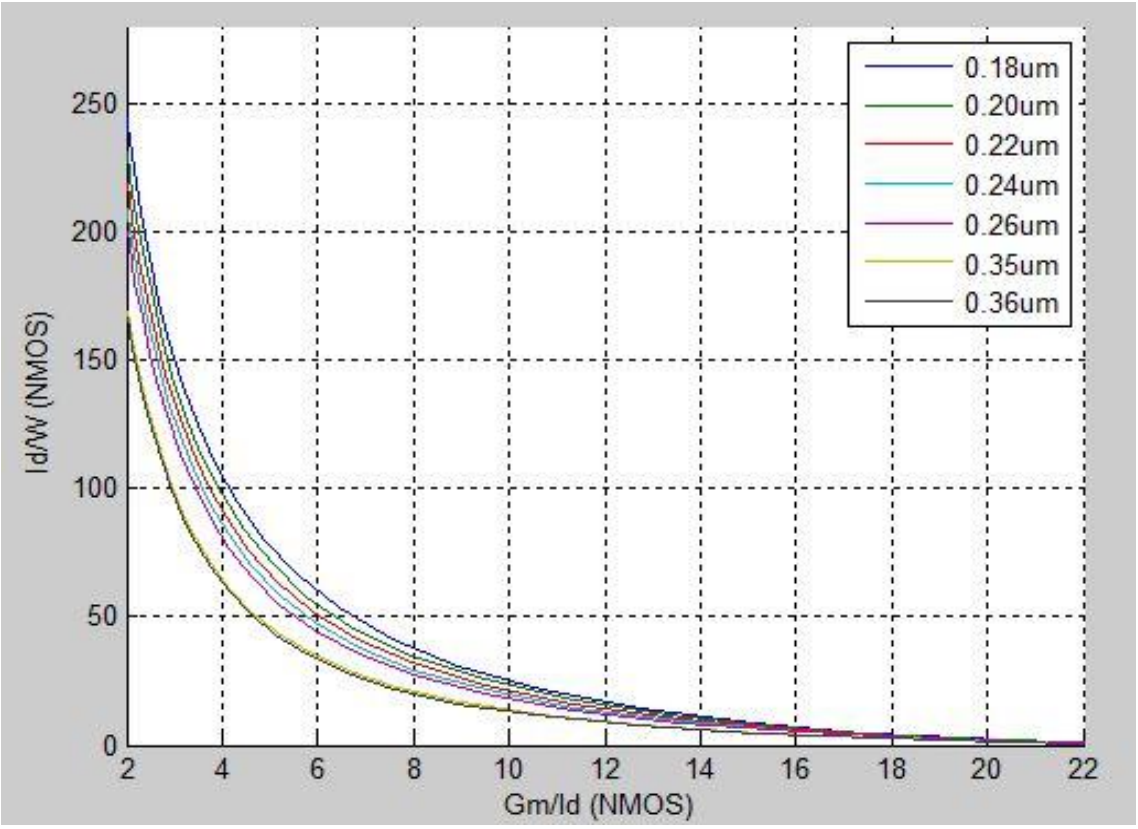


Figure 5.9(c) Id/W vs g_m/I_d plot of NMOS device with different transistor lengths.

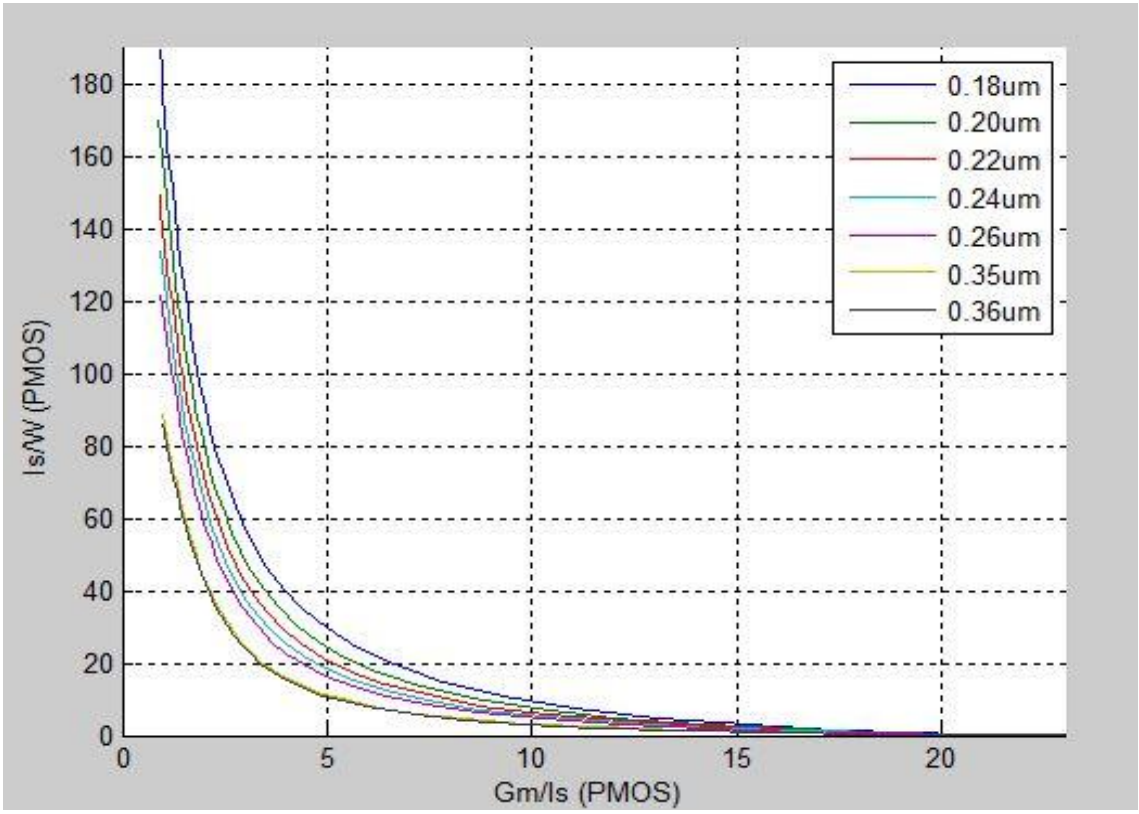


Figure 5.9(d) Id/W vs g_m/I_d plot of PMOS device with different transistor lengths.

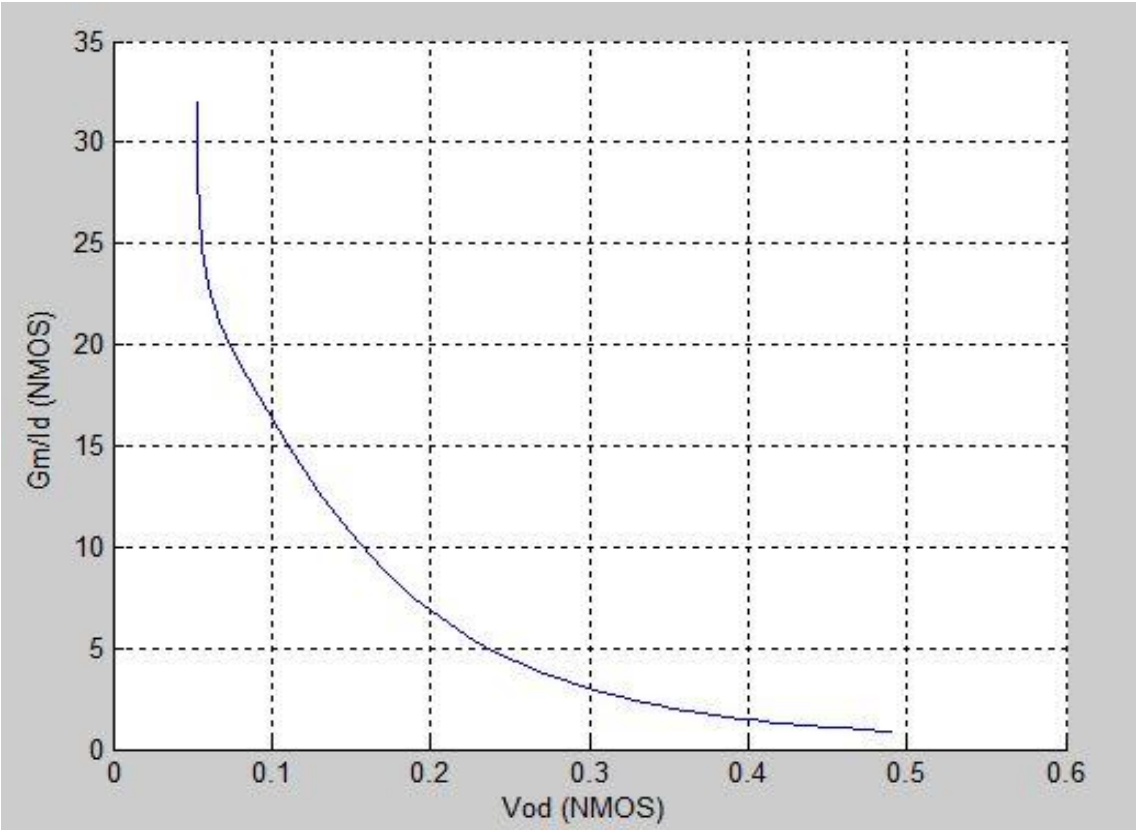


Figure 5.10(a) g_m/I_d vs V_{OD} plot of NMOS device.

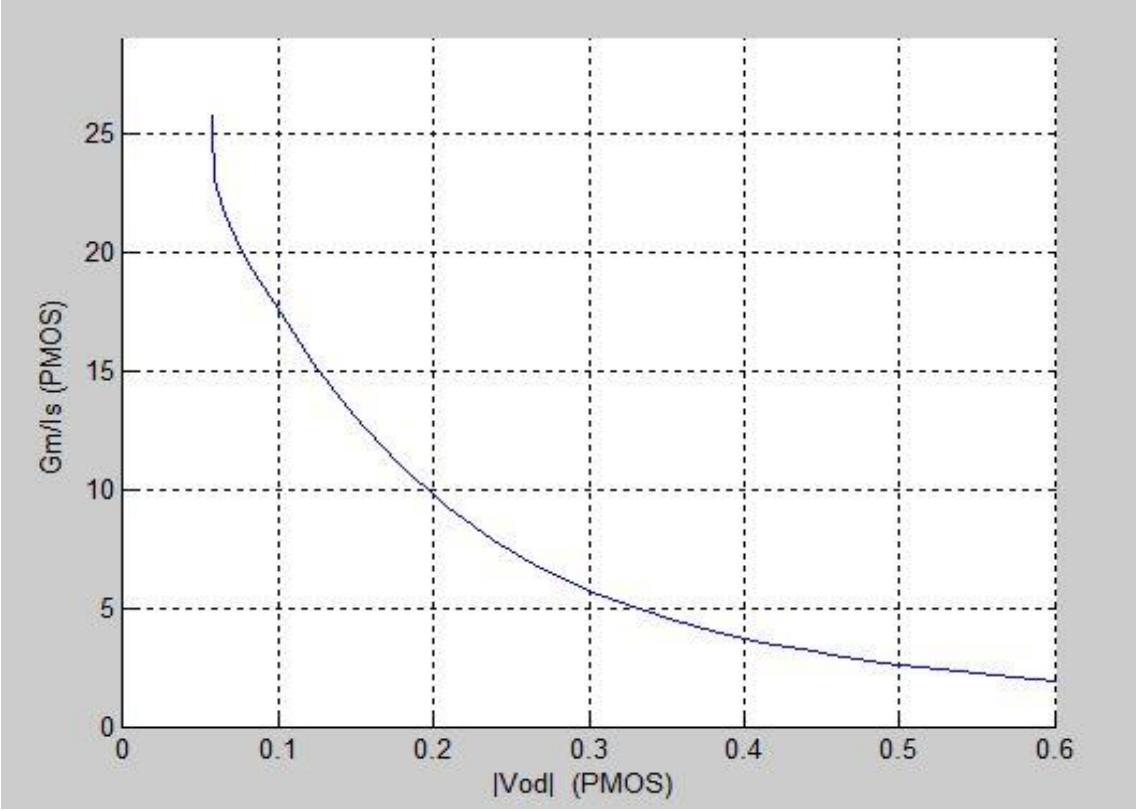


Figure 5.10(b) g_m/I_d vs V_{OD} plot of PMOS device.

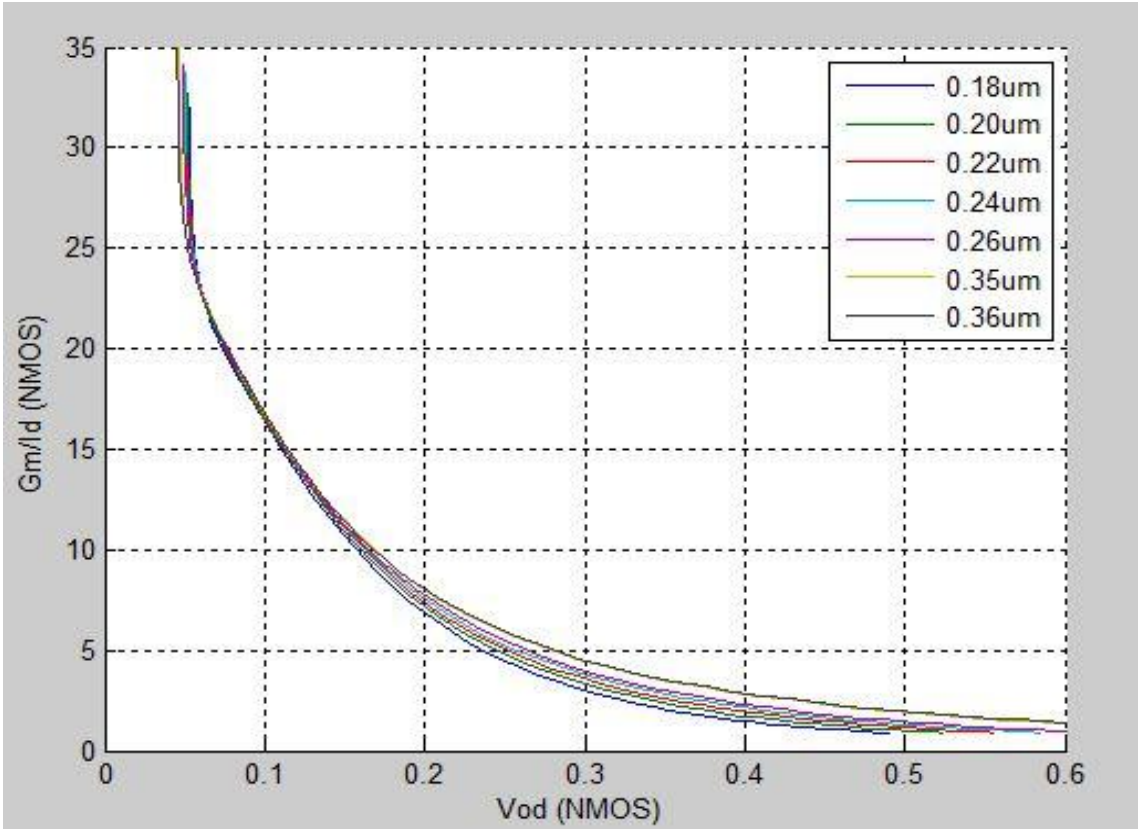


Figure 5.10(c) g_m/I_d vs V_{OD} plot of NMOS device with different transistor lengths.

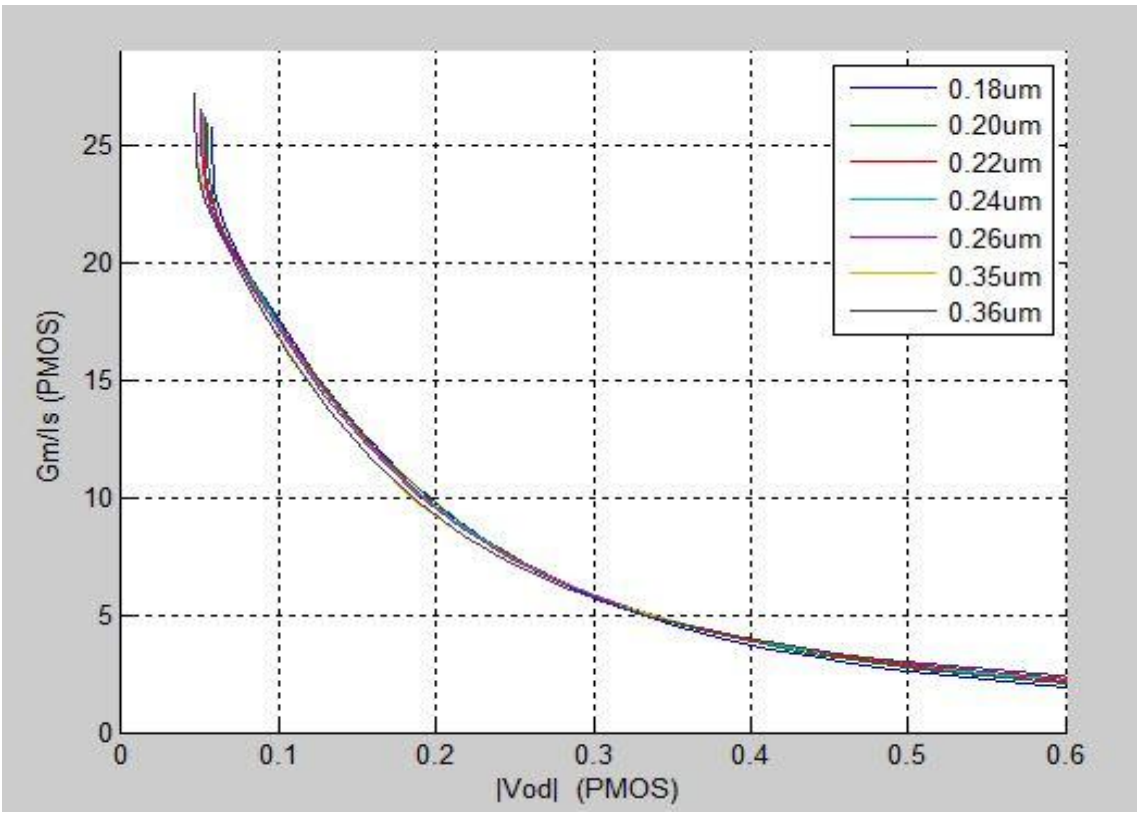


Figure 5.10(d) g_m/I_d vs V_{OD} plot of PMOS device with different transistor lengths.

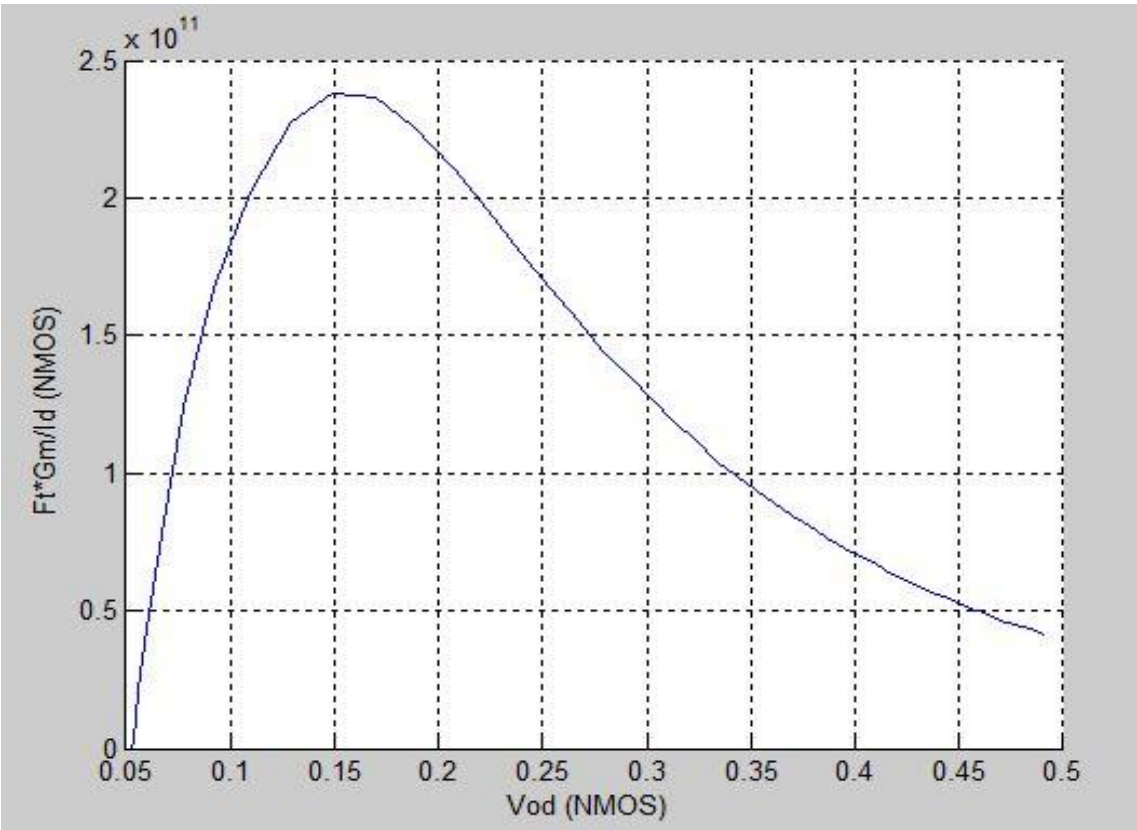


Figure 5.11(a) Ft * (g_m/I_d) vs V_{OD} plot of NMOS device.

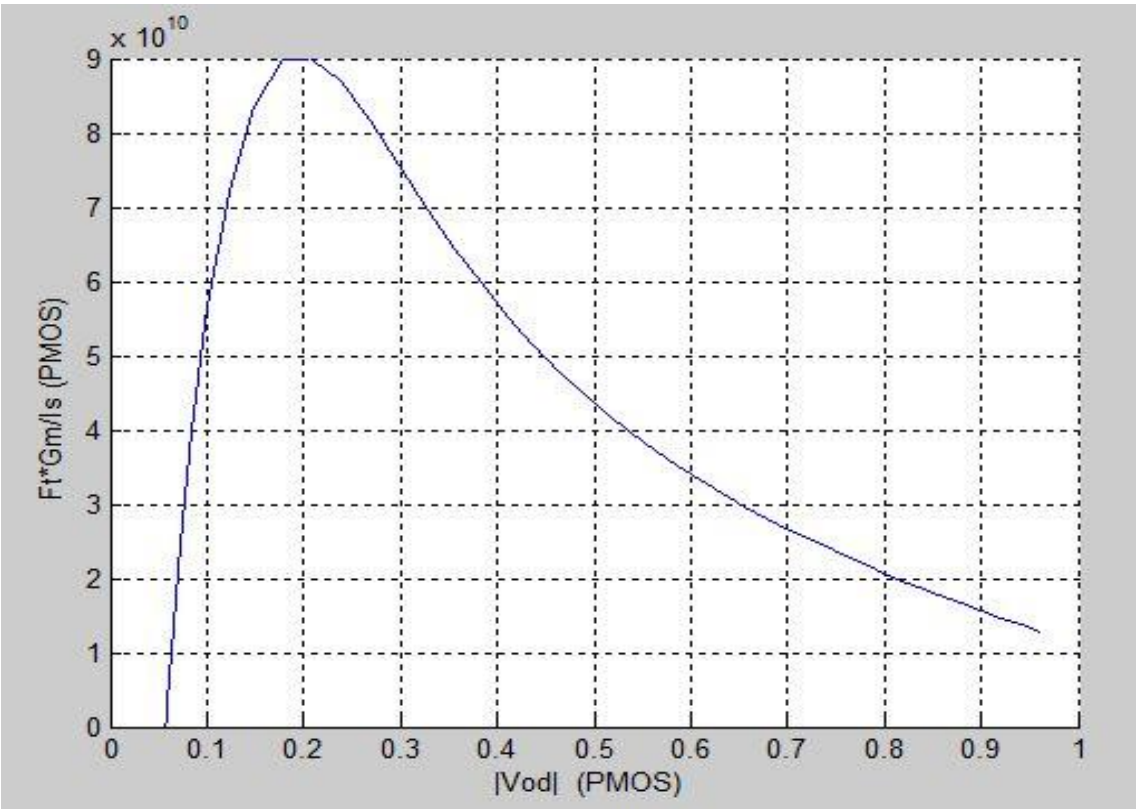


Figure 5.11(b) Ft * (g_m/I_d) vs V_{OD} plot of PMOS device.

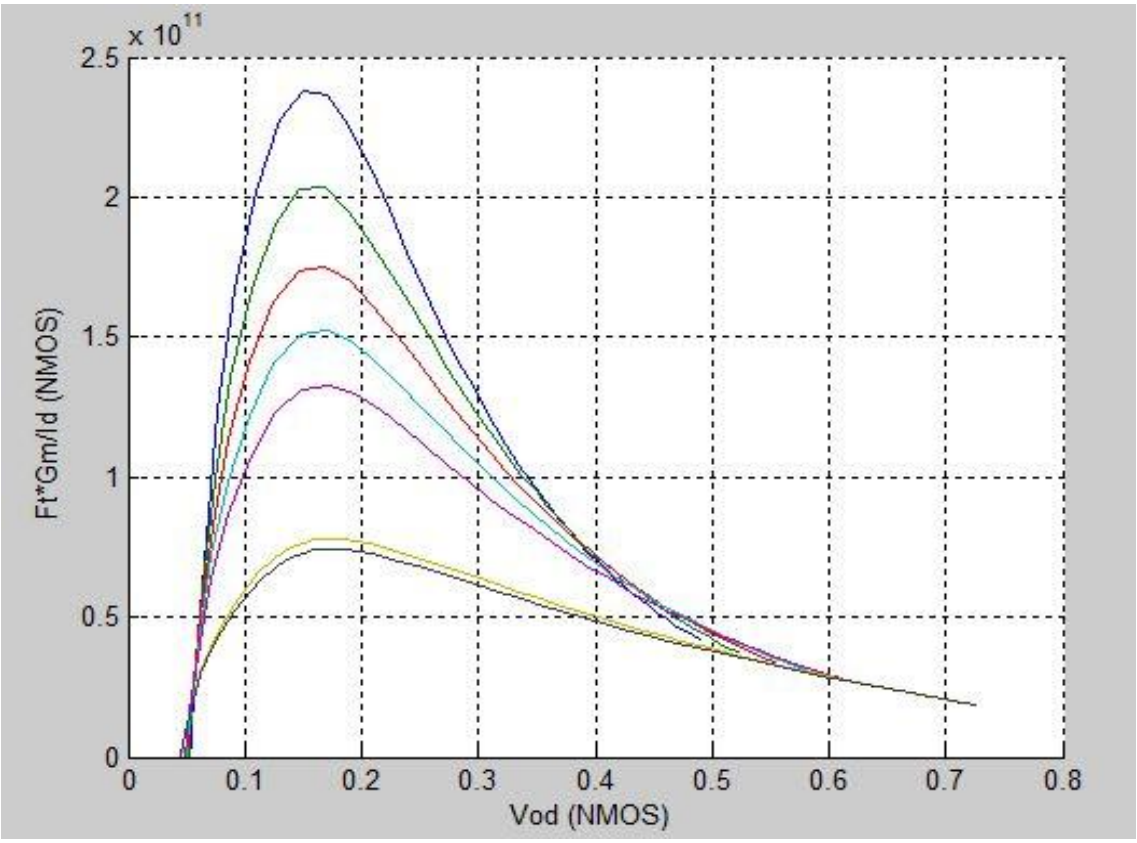


Figure 5.11(c) Ft * (g_m/I_d) vs V_{OD} plot of NMOS device with different transistor lengths.

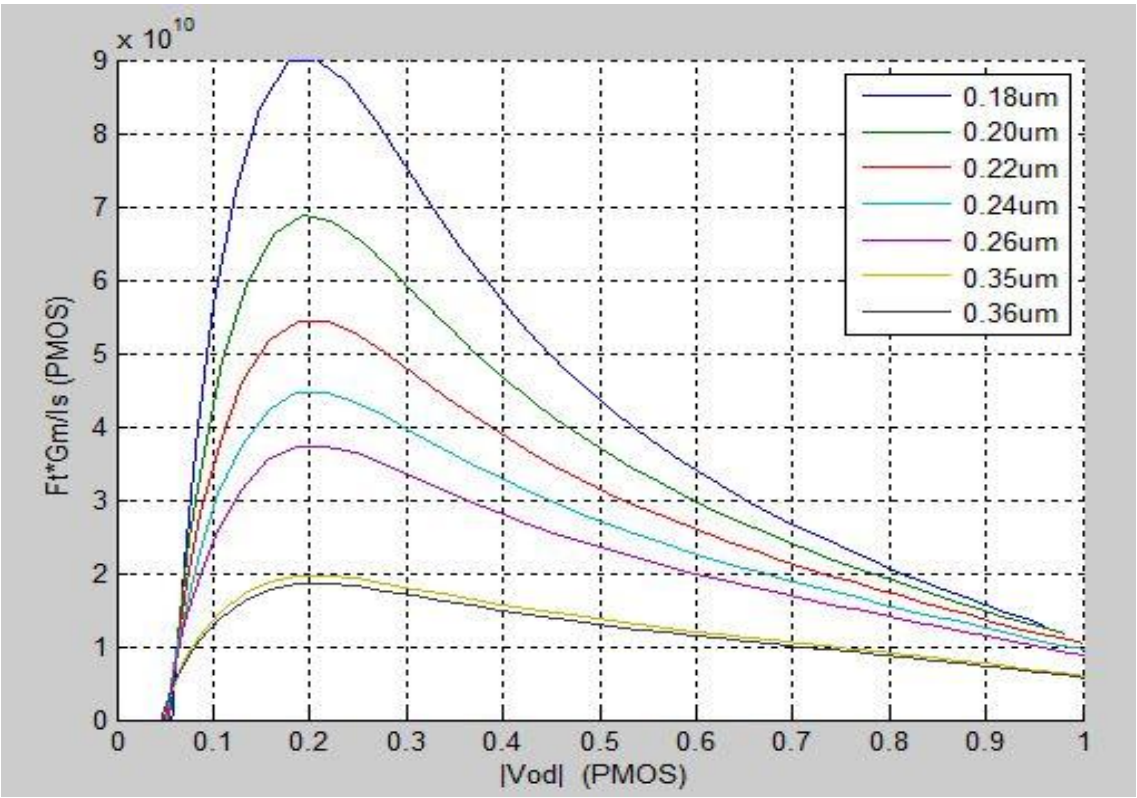


Figure 5.11(d) Ft * (g_m/I_d) vs V_{OD} plot of PMOS device with different transistor lengths.

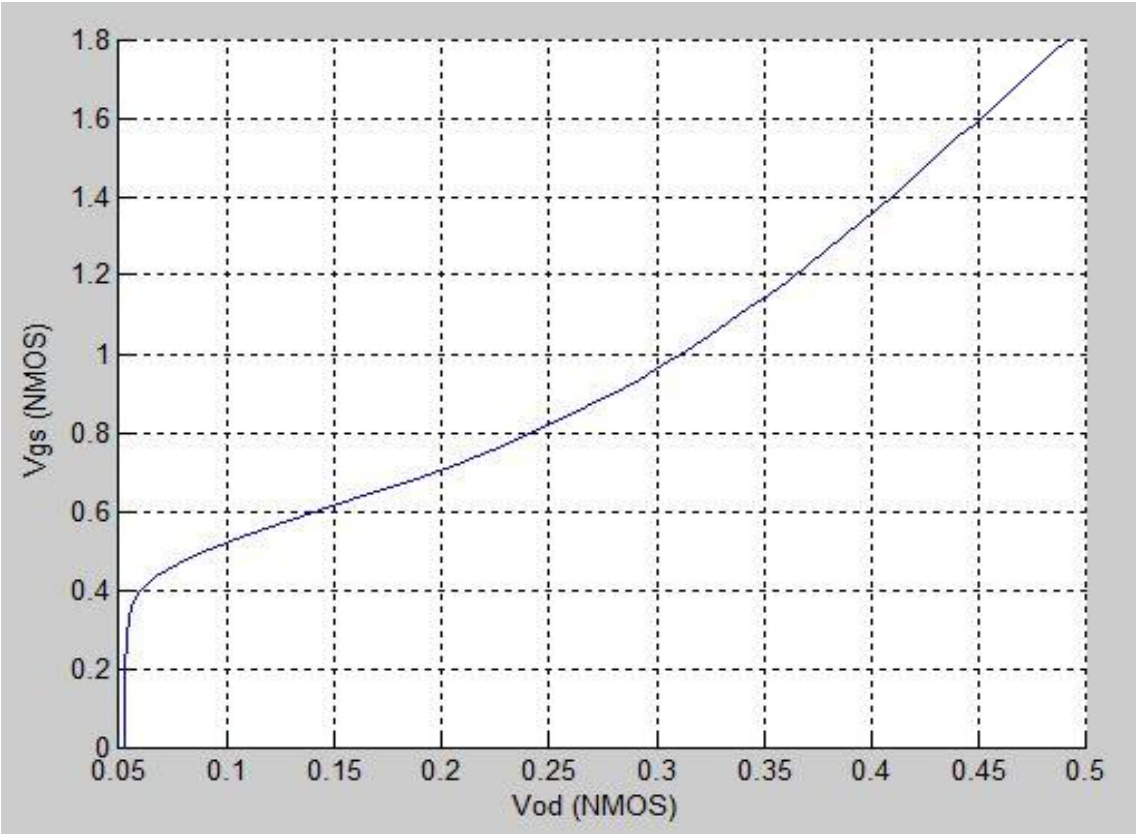


Figure 5.12(a) Vgs vs V_{OD} plot of NMOS device.

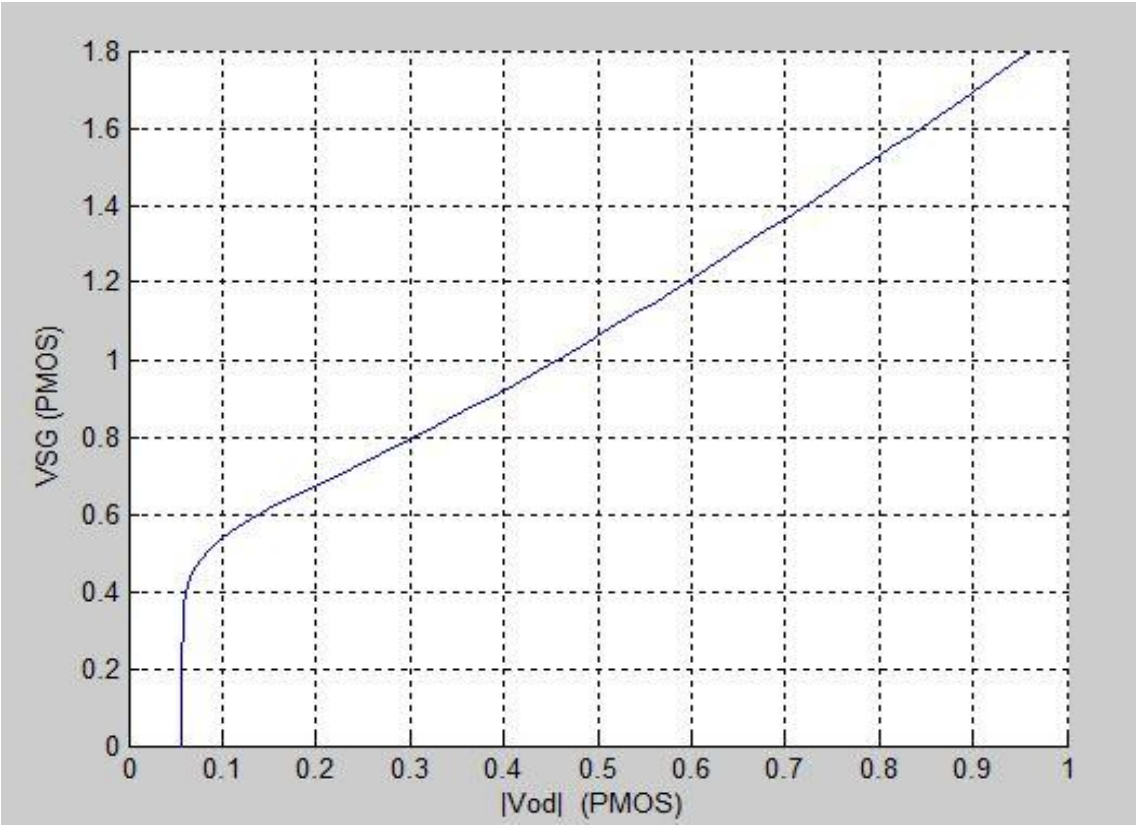


Figure 5.12(b) Vgs vs V_{OD} plot of PMOS device.

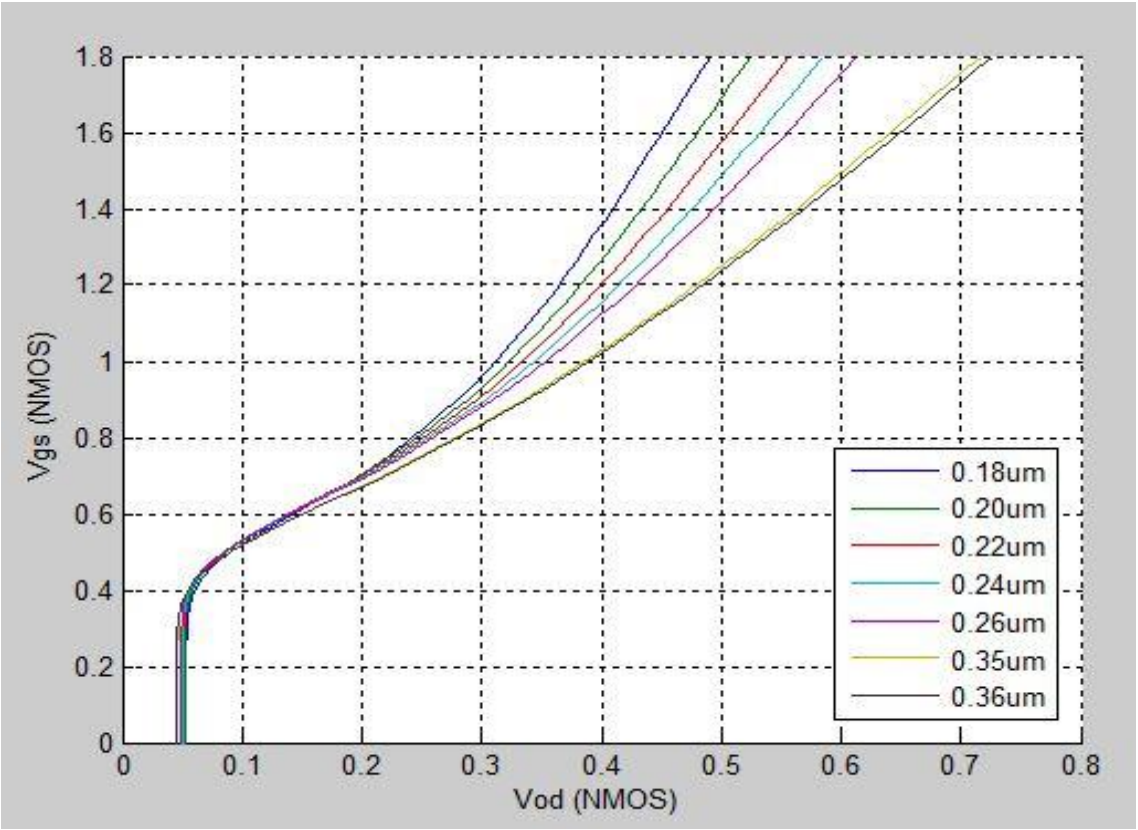


Figure 5.12(c) Vgs vs V_{OD} plot of NMOS device with different transistor lengths.

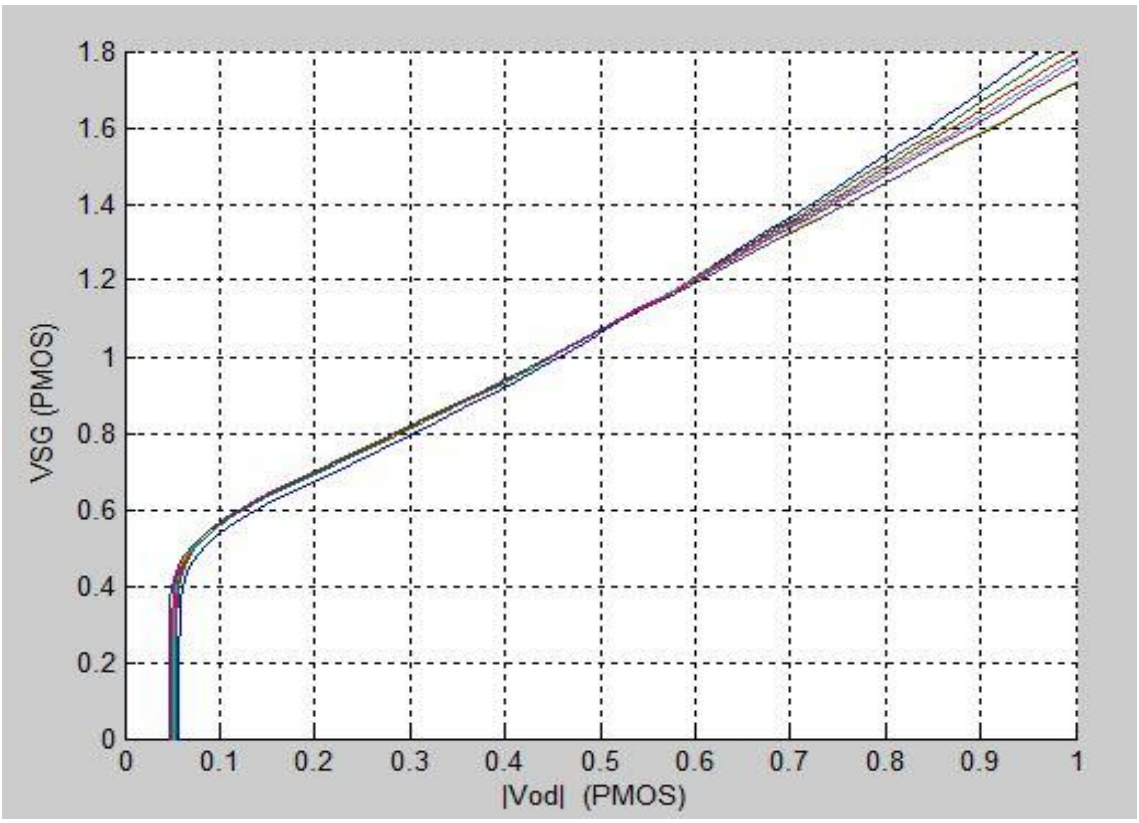


Figure 5.12(d) Vgs vs V_{OD} plot of PMOS device with different transistor lengths.

5.5 GENERAL DESIGN FLOW

Fig. 5.13 shows the general design flow by using pre-simulated plots and the g_m/I_d design method.The above description is just a general design flow using g_m/I_d design method.The design flow may be changed based on the actual constraints, circuit specifications and many other things. The design flow steps are explained below:

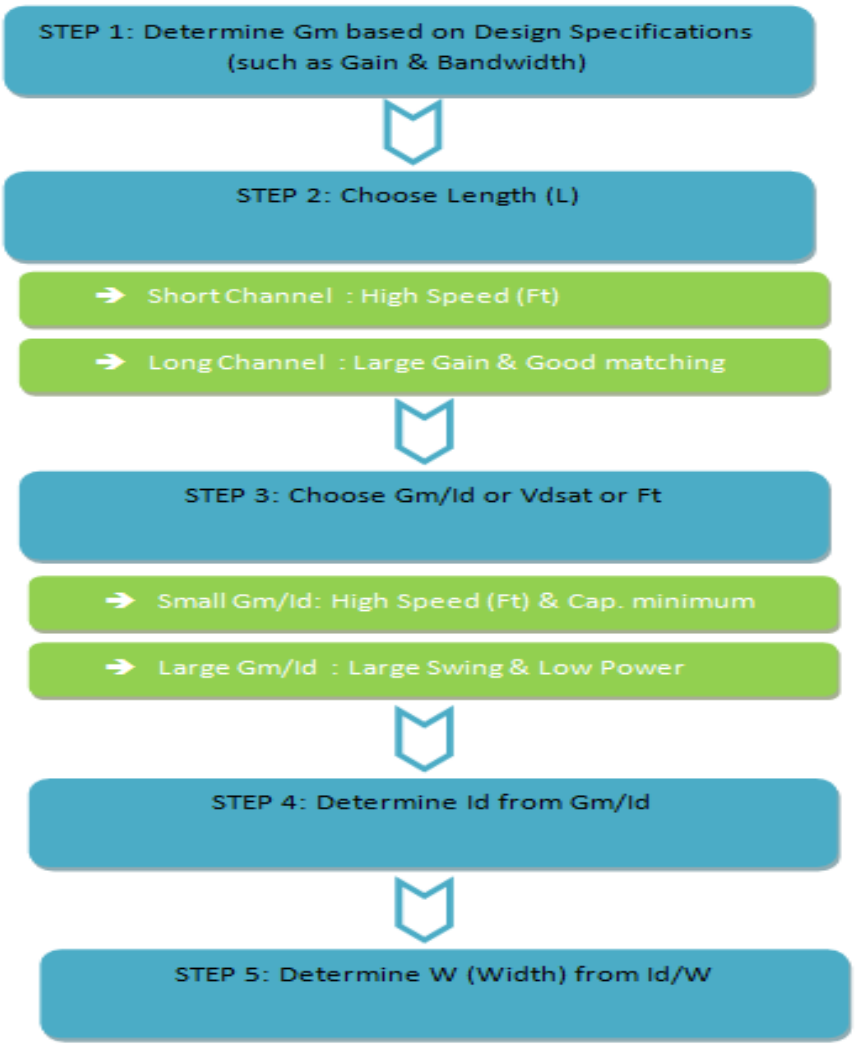


Figure 5.13: General Design Flow.

STEP 1: Determine Trans-conductance (g_m) based on the design specifications:

Here in the first step, trans-conductance is determined based on the specifications provided by the circuit like load capacitance, unity gain frequency, load resistance, & gain etc.

STEP 2: Choose Length (L):

The length of the mosfet is then chosen to meet the specifications like gain and speed requirements of the circuit. The smaller the length of the mosfet, higher the speed but at the cost of smaller gain.

STEP 3: Choose g_m/I_d Ratio (Trans-conductance efficiency):

The g_m/I_d ratio selection is very important. This value decides whether the mosfet will operate in strong inversion, medium inversion or weak inversion. The smaller the g_m/I_d ratio, device will operate in strong inversion and we obtained system with higher speed and minimum capacitance due to small area while higher the g_m/I_d ratio, device will operate in weak inversion and we obtained system with large output swing and low-power consumption.

STEP 4: Determine I_d (Drain Current):

The current can be determined from the g_m/I_d ratio required for the system.

STEP 4: Determine Width (W):

The width of the mosfet can now be determined from the values obtained from the current density (I_d/W) and the drain current for the particular g_m/I_d ratio.

By using the device characterization charts and g_m/I_d design methodology, the gap between hand analysis and the modern device models, can be bridged, as shown in Fig. 5.14 [14]. The discrepancies between g_m/I_d design results and the actual simulations results are usually on the order of 10 ~ 20%, mostly due to the assumptions that we made during the Gm/Id design procedure [13].Even we found the discrepancies in the simulation results, we can always look back to our g_m/I_d derivations to track down the root causes [13]. The square law calculations are based on inappropriate parameters that do not exist or have no significant impacts in the modern spice models [13].

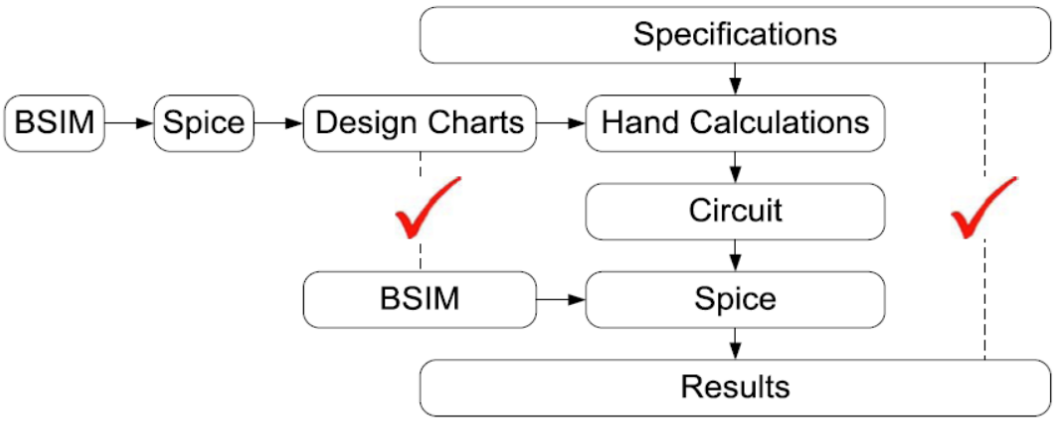


Figure 5.14: Short Channel Device Design Solution. [14]

CHAPTER 6

DESIGN OF HIGH-SPEED, LOW-OFFSET COMPARATOR

The needs of large digital systems have driven the development of modern scaled CMOS processes. Process advances such as lower power supplies and shorter gate lengths which lead to lower power consuming, faster digital circuits can also lead to higher power. For high frequency circuit operation, the trade-off must be made between speed and power dissipation. Speed will be mainly influenced by slew-rate requirements and the load capacitance and load impedance. The lower the load resistance or higher the load capacitance, the more current will be needed to achieve the desired speed of operation. The gain of the comparator will be influence by the speed and power dissipation. The gain could also be increased by increasing the power supply voltage. However, the maximal power supply is limited by the chosen technology. The input impedance of the comparator should ideally be infinite. The low output impedance is important concerning the (minimal) power dissipation within the last stage. Furthermore, the input and output impedances determine how the circuit interacts with the preceding and the subsequent stages.

This chapter introduces the detailed High-Speed, Low-Offset Comparator design in a 0.18µm CMOS process using conventional method and g_m/I_d method and compares the simulation results of both these methods. The chapter describes the designing of individual comparator blocks like current mirror, pre-amplifier, latch, self-biased differential amplifier circuits with conventional as well as g_m/I_d method.

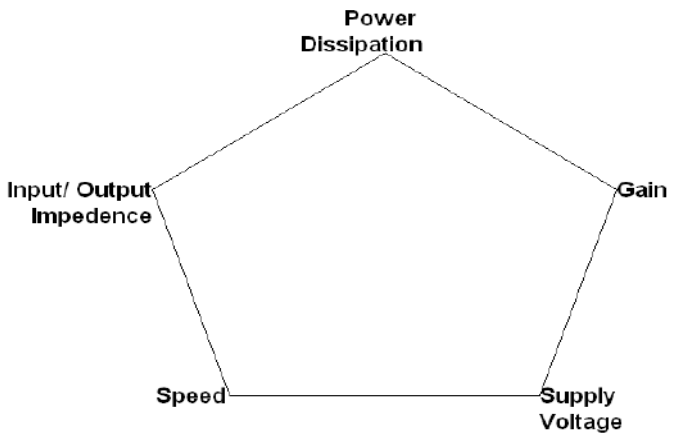


Figure 6.1: The Design trade-offs. [11]

6.1 HIGH-SPEED, LOW-OFFSET COMPARATOR

The Comparator is the critical part of the CBSC circuit and it is used to detect the virtual ground condition. The comparator should change its output as soon as its input crosses the virtual ground voltage.

6.1.1 DESIGN SPECIFICATIONS

Table 6.1 Target specifications for high speed, low offset comparator.

PARAMETERS	VALUES
TECHNOLOGY	CADENCE UMC 180nm CMOS
SUPPLY VOLTAGE	1.8 V
INPUT VOLTAGE RANGE	0.75-1.6 V
GAIN	>33 dB
RESOLUTION	<40 mV
SPEED OR PROPAGATION TIME DELAY	<1.8 ns
OFFSET VOLTAGE	<40 mV
LOAD CAPACITANCE	5 fF

The critical specifications of the comparator are the speed and offset. We require that the offset voltage to be smaller than 40 mV. Clearly to reach this requirement, differential amplifiers, as the ones used in the pre-amplifier of the comparator have an offset voltage of 10 mV to 20 mV, if they are realized in CMOS technology. The resolution of the comparator can be defined as

$$\Delta V_{IN} = \frac{V_{OH} - V_{OL}}{A_V} \tag{6.1}$$

Where A_V is the DC gain and V_{OH} and V_{OL} are the output logic states high and low respectively. With 40 mV, A_V becomes 33 dB. In conclusion, to discriminate voltage differences as small as 40 mV, a minimum gain of 33 dB is required. The response time of the comparator must be smaller be 2 ns. The comparator response time is the sum of the pre-amplifier's delay time, latch's delay time and self-biased amplifier with invertor pair. Neither power dissipation, nor bias current is rigorously specified. Nevertheless, efforts will be made to minimize both quantities. Of course, also the area will be kept as small as possible.

6.2 HIGH-SWING CASCODE CURRENT MIRROR

There are two important factors in choosing a current source. It must have a high input resistance (possibly cascode design), and low Vomin (voltage overhead). This ensures enough headroom for voltage swing. While several different topologies provide the same Vomin, the optimal current source wastes the least amount of power. We choose to use the high-swing cascode; because it has the minimum Vomin of 2Vov (Compliance voltage) and it only has one extra branch of wasted current (minimizes power).This high-swing cascode current mirror will provide 50µA biasing current for the preamplifier with a compliance voltage of 0.25V.

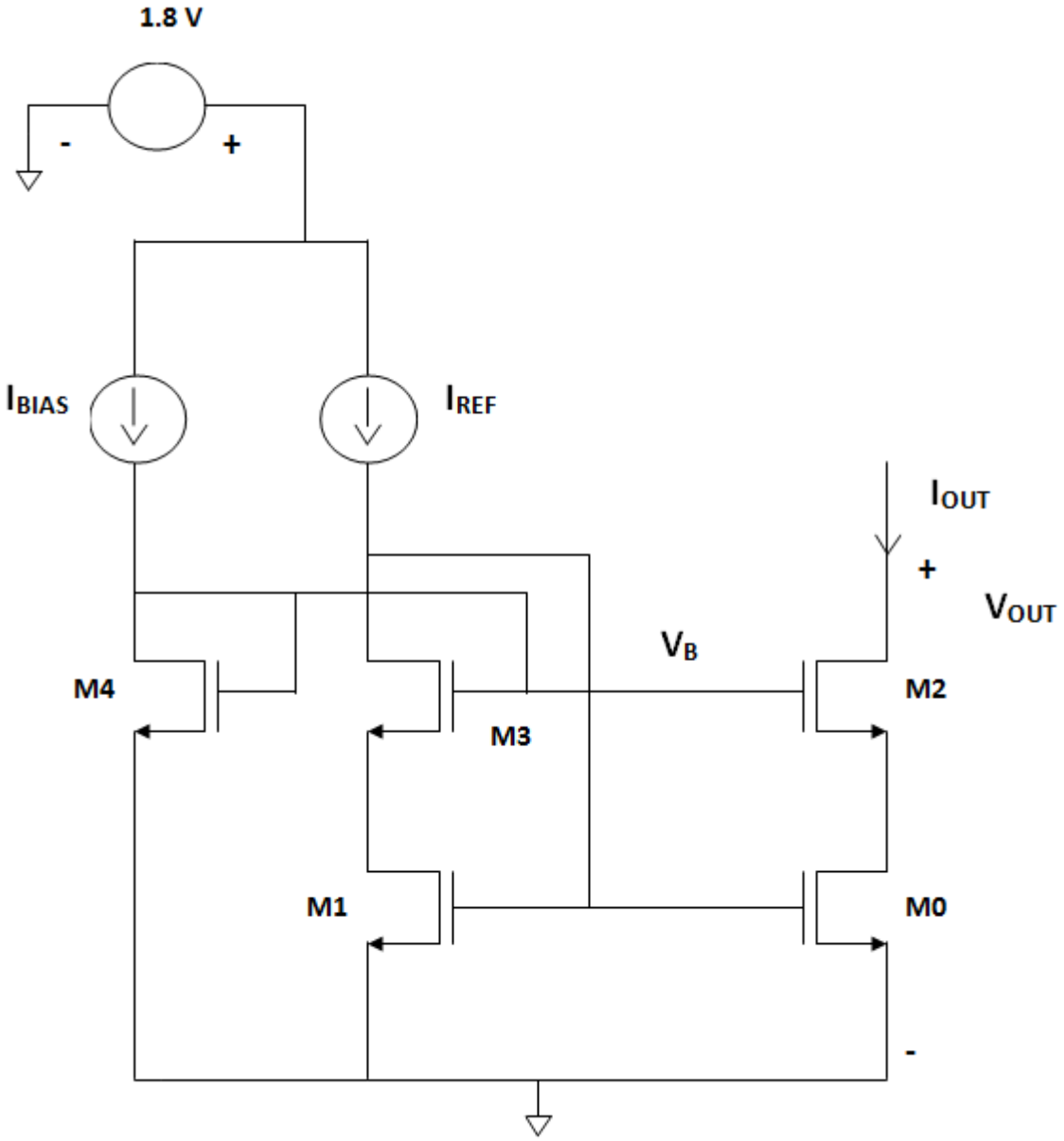


Figure 6.2: Schematic of high-swing cascode current mirror. [14]

6.2.1 DESIGNING BY CONVENTIONAL METHOD

The following equations are used to design the high-swing cascode current mirror. Rout becomes large if all the transistors are in saturation. Therefore we require

$$V_{DS0} = V_{G2} - V_{GS2} > V_{DSat0} \tag{6.2}$$

$$V_{DS2} = V_{OUT} - V_{DS0} = V_{OUT} - V_{G2} + V_{GS2} > V_{DSat2} \tag{6.3}$$

And

$$V_{DS1} = V_{G3} - V_{GS3} > V_{DSat1} \tag{6.4}$$

$$V_{DS3} = V_{GS1} - V_{DS1} = V_{GS1} - V_{G3} + V_{GS3} > V_{DSat3} \tag{6.5}$$

From equation 6.1 and 6.2, we get

$$V_{GS2} + V_{DSat0} < V_{G2} < V_{OUT} + V_{GS2} - V_{DSat2} \tag{6.6}$$

From equation 6.3 and 6.4, we get

$$V_{GS3} + V_{DSat1} < V_{G3} < V_{GS1} + V_{GS3} - V_{DSat3} \tag{6.7}$$

For current mirroring, we need $V_{DS0} = V_{DS1}$

$$V_{DS0} = V_{G2} - V_{GS2} \tag{6.8}$$

and

$$V_{DS1} = V_{G3} - V_{GS3} \tag{6.9}$$

If we know set $V_{G2} = V_{G3} = V_B$, then we must only assure that $V_{GS2} = V_{GS3}$.

$$I_{D2} = \frac{1}{2}\mu_n C_{OX} \left(\frac{W}{L}\right)_2 * [(V_{GS2} - V_{TH2})^2] \tag{6.10}$$

and

$$I_{D3} = \frac{1}{2}\mu_n C_{OX} \left(\frac{W}{L}\right)_2 * [(V_{GS3} - V_{TH3})^2] \tag{6.11}$$

Solving these equations for $V_{GS2} = V_{GS3}$ and by noting that $V_{TH2} = V_{TH3}$, we get

$$\frac{I_{D2}}{I_{D3}} = \frac{(W/L)_2}{(W/L)_3} \tag{6.12}$$

With

$$\frac{I_{OUT}}{I_{REF}} = \frac{(W/L)_0}{(W/L)_1} \tag{6.13}$$

We must therefore require

$$\frac{(W/L)_0}{(W/L)_1} = \frac{(W/L)_2}{(W/L)_3} \tag{6.14}$$

and $$\left(\frac{W}{L}\right)_{0,2} = \frac{2 * I_{OUT}}{\mu_n C_{OX} * (V_{DSat0,2})^2} \quad (6.15)$$

To determine V_B we can use the equations,

$$V_{DSat2} = V_{GS2} - V_{TH2} \quad (6.16)$$

$$V_{GS2} = V_B - V_{DS0} \quad (6.17)$$

$$\Rightarrow V_B = V_{DSat2} + V_{DS0} + V_{TH2} \quad (6.18)$$

The V_B is the biasing voltage needed to properly bias gate voltages of M2 and M3 transistors for accurate mirroring. Here we define the compliance voltage, as the lowest output voltage to keep the output transistors in saturation.

The sizing, current and the overdrive voltage of different transistors, as calculated by conventional method equations are tabulated in table 6.2. The table also compares the simulated results with that of the conventional values. There is gap between theoretical values and simulated results for the current mirror circuit using conventional method.

Table 6.2 Comparison of different parameters of the Current Mirror as calculated by Conventional method and through Simulation.

CURRENT MIRROR **Conventional Method Values**	**L (µm)**	**W (µm)**	**| I_d | (µA)**	**| Vdsat | (V)**
M0	0.18	7.48	60	0.091
M1	0.18	7.48	50	0.092
M2	0.36	9.75	50	0.1128
M3	0.36	9.75	50	0.1128
M4	0.36	0.85	10	0.170
I_{REF} = 50 µA				
I_{BIAS} = 10 µA				
V_B = 0.7 V				
Simulated Results	**L (µm)**	**W (µm)**	**| I_d | (µA)**	**| Vdsat | (V)**
M0	0.18	7.48	49.97	0.108
M1	0.18	7.48	50.00	0.108
M2	0.36	9.75	49.97	0.119
M3	0.36	9.75	50.00	0.119
M4	0.36	0.85	10.00	0.164

6.2.2 DESIGNING BY g_m/I_d METHOD

The design flow followed by the g_m/I_d method in designing the current mirror is shown in figure 6.3.

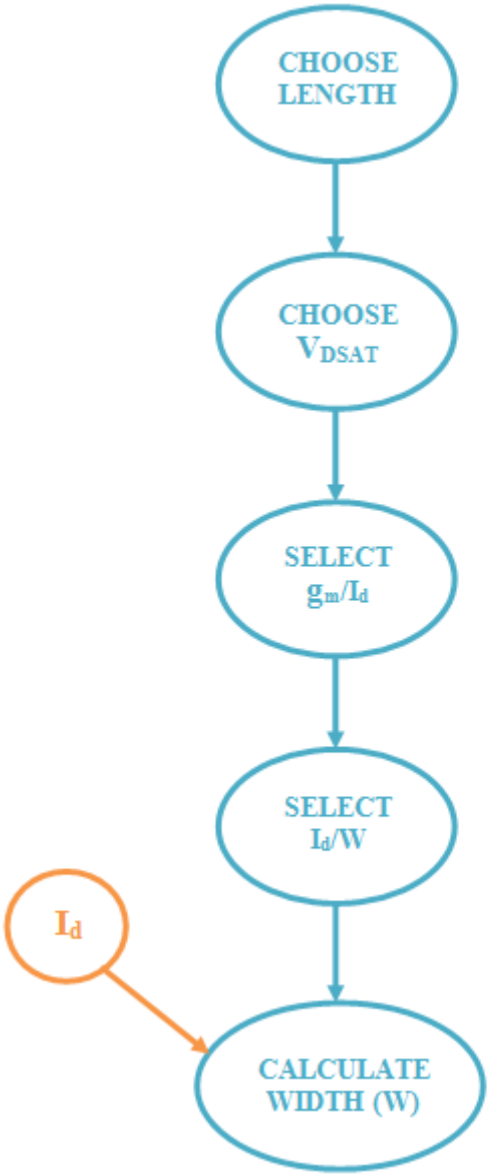


Figure 6.3: g_m/I_d design flow for designing high-swing cascode current mirror.

With the help of design flow, we get the optimized-sizing of the different transistors used in the current mirror.The table 6.3 shows the different parameters of MOS as calculated by the g_m/I_d method and comparison of these values with that of the simulted results.The g_m/I_d method values are very close to that of the simulated results as compared to the conventional method values.

Table 6.3 Comparison of different parameters of the Current Mirror as calculated by g_m/I_d method and through Simulation.

CURRENT MIRROR g_m/I_d Method Values	**L (µm)**	**W (µm)**	**g_m (µS)**	**$\lvert I_d \rvert$ (µA)**	**$g_m / \lvert I_d \rvert$ (1/V)**	**$\lvert V_{dsat} \rvert$ (V)**
M0	0.18	10.36	873	50	17.46	0.09155
M1	0.18	10.36	873	50	17.46	0.0915
M2	0.36	10.83	757.5	50	15.15	0.2781
M3	0.36	10.83	757.5	50	15.15	0.2781
M4	0.36	0.41	75.99	10	7.599	0.2084
I_{REF} = 50 µA						
I_{BIAS} = 10 µA						
V_B = 0.7 V						
Simulated Results	**L (µm)**	**W (µm)**	**g_m (µS)**	**$\lvert I_d \rvert$ (µA)**	**$g_m / \lvert I_d \rvert$ (1/V)**	**$\lvert V_{dsat} \rvert$ (V)**
M0	0.18	10.36	800.7	50.02	16.01	0.09741
M1	0.18	10.36	800.3	50	16.01	0.09741
M2	0.36	10.83	751.3	50.06	15.01	0.115
M3	0.36	10.83	750.2	50	15	0.115
M4	0.36	0.41	72.31	10	7.231	0.226
I_{OUT} = 49.59 at compliance voltage = 0.25 V						

6.2.3 SIMULATION RESULTS:

The current mirror was tested separately. The width W and length L, of the MOS transistors are given in Table 6.3. The input current, I_{REF} & I_{BIAS}, is taken to have DC value of 50 µA &10 µA. Figure 6.4 shows the variation of the output current versus output voltage i.e. output characteristic of the current mirror. Output current follows the input current only after output voltage is greater than compliance voltage. Figure 6.5 shows the output current versus the biasing voltage V_B. This curve indicates the minimum voltage V_B, required at the gate of M2 & M3 for the proper current mirroring action. Figure 6.6 shows the variation of the output current with different biasing voltage V_B. The curve shows, how current mirroring accuracy and output resistance vary with the V_B which then affects the current mirroring. Thus V_B voltage is carefully decided for the good current mirror design.

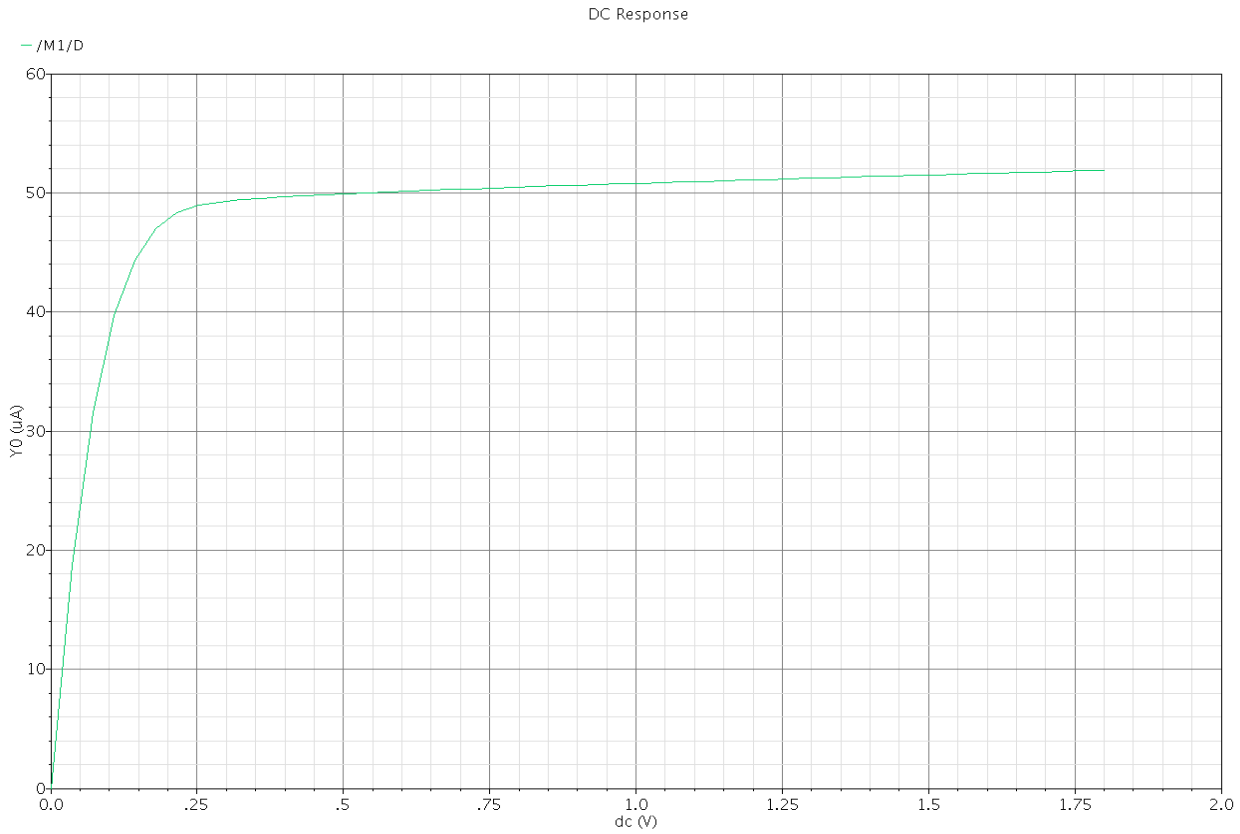


Figure 6.4: Output characteristic of the high-swing cascode current mirror.

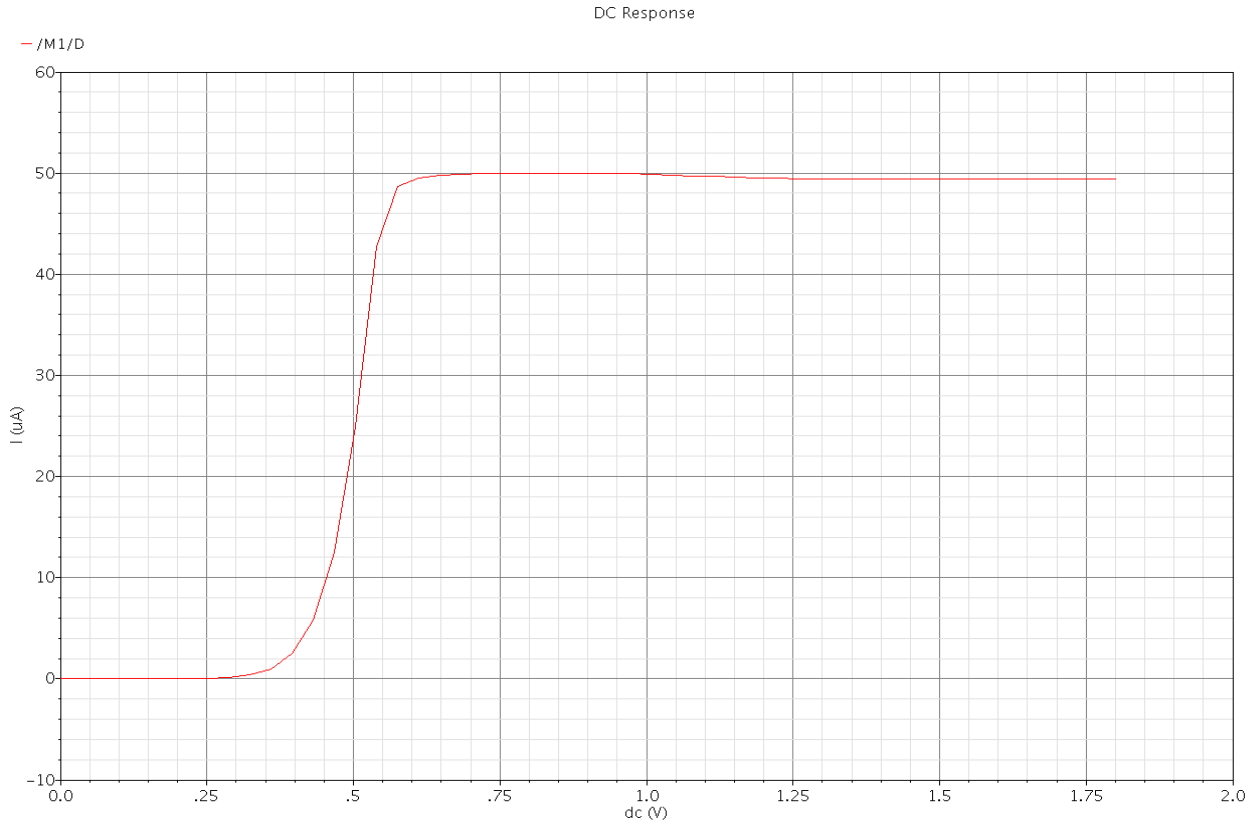


Figure 6.5: I_{out} vs V_B plot of the current mirror.

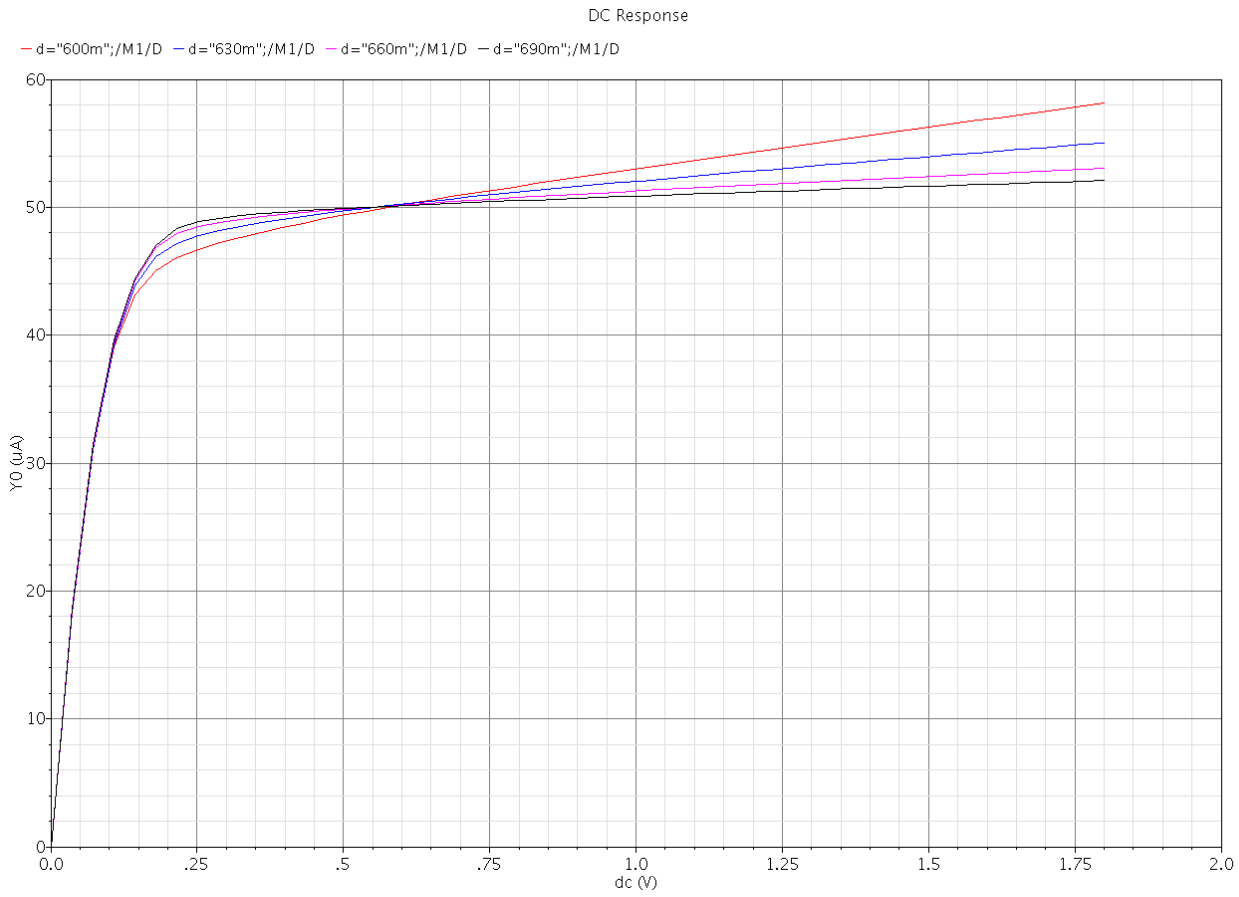


Figure 6.6: Output characteristic of current mirror with different bias voltages V_B.

6.3 PRE-AMPLIFIER:

The first stage of the comparator is the pre-amplifier, as shown in figure 6.7. These are used to amplify the signal before it is fed to the comparator; it helps to relax requirements on comparators resolution and gain. The main design criteria for the pre-amplifier are the gain and bandwidth (cut-off frequency f_{-3dB}). The gain and bandwidth are chosen to be A_v=2.5 and f_{-3dB} =750 MHz. A bias current of 50µA is chosen. The gain-bandwidth product f_{GBW} can be further increased by increasing the bias current. However low power consumption is preferable.

6.3.1 DESIGNING BY CONVENTIONAL METHOD:

The pre-amplifier uses diode connected load. The gain of the amplifier is given by the relation in 6.19

$$A_V = \frac{g_{m5}}{g_{m7}} = \frac{g_{m6}}{g_{m8}} \qquad (6.19)$$

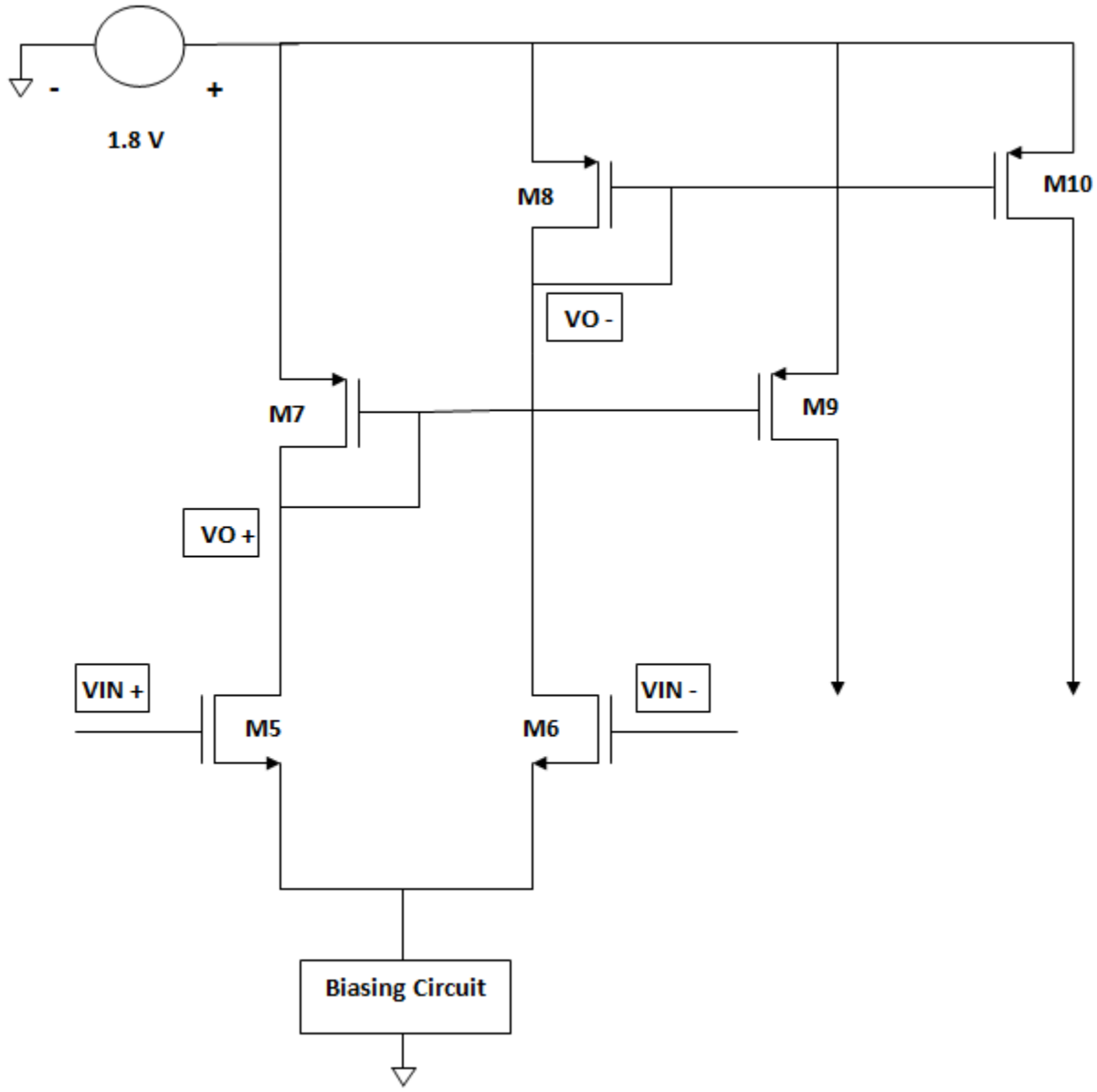


Figure 6.7: Schematic of the Pre-amplifier circuit.

Trans-conductance (g_m) of a transistor is given by 6.20.

$$g_m = \sqrt{u_n C_{ox} \frac{W}{L} * 2 * I_d} \tag{6.20}$$

The f_{-3dB} frequency is given by 6.21.

$$f_{-3dB} = \frac{f_{GWB}}{|A_v|} \tag{6.21}$$

Pre-amplifier is also beneficial in terms of reducing offset. The offset voltage can be significantly reduced by increasing the input transistor width, as offset is inversely proportional to width of the input transistor according to 6.22.

$$\sigma_{os} \approx \frac{1}{\sqrt{W * L}} \qquad (6.22)$$

The sizing, trans-conductance, current and the overdrive voltage of different transistors, as calculated by conventional method equations are tabulated in table 6.4. The table also compares the simulated results with that of the conventional values. There is large gap between theoretical values and simulated results for the pre-amplifier circuit using conventional method.

Table 6.4: Comparison of different parameters of the Pre-amplifier as calculated by Conventional method and through Simulation.

PREAMPLIFIER **Conventional Method Values**	**L (µm)**	**W (µm)**	**g_m (µS)**	**$\lvert I_d \rvert$ (µA)**	**$\lvert V_{dsat} \rvert$ (V)**
M5	0.18	1.87	433	25	0.092
M6	0.18	1.87	433	25	0.092
M7	0.36	8.53	288	25	0.153
M8	0.36	8.53	288	25	0.153
M9	0.36	8.53	288	25	0.153
M10	0.36	8.53	288	25	0.153
Simulated Results	**L (µm)**	**W (µm)**	**g_m (µS)**	**$\lvert I_d \rvert$ (µA)**	**$\lvert V_{dsat} \rvert$ (V)**
M5	0.18	1.87	352	24.83	0.117
M6	0.18	1.87	352	24.83	0.117
M7	0.36	8.53	253	24.83	0.180
M8	0.36	8.53	253	24.83	0.180
M9	0.36	8.53	251	24.63	0.1799
M10	0.36	8.53	251	24.63	0.1799

6.3.2 DESIGNING BY g_m/I_d METHOD:

The design flow followed by the g_m/I_d method in designing the Pre-amplifier is shown in figure 6.8. With the help of design flow, we get the optimized-sizing of the different transistors used in the Pre-amplifier.

The bias current in each branch of differential stage was set to 25 µA. The g_m/I_d ratio of the input differential pair was set to 17.46, in order to achieve the required gain & bandwidth requirement.

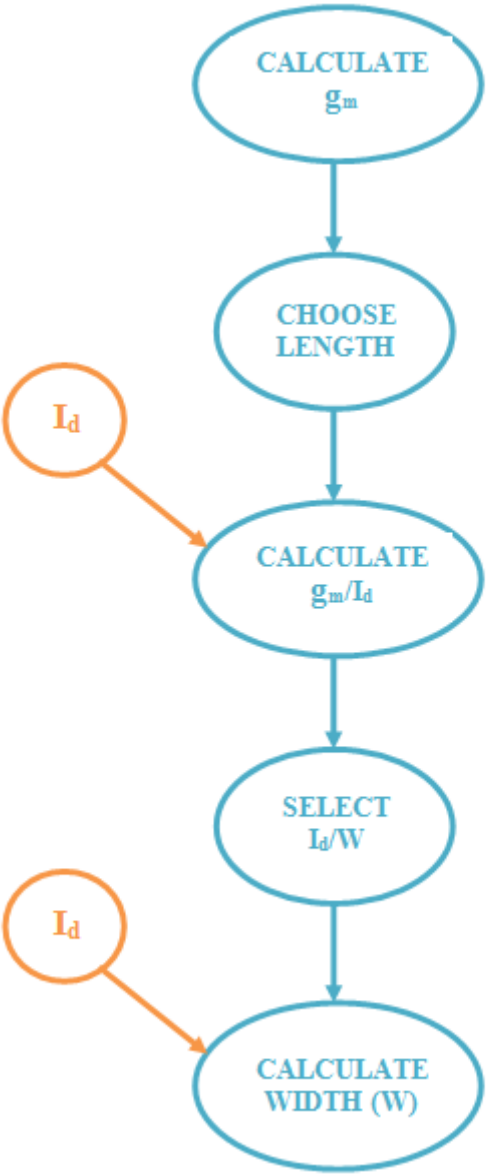


Figure 6.8: g_m/I_d design flow of designing Pre-amplifier.

The current mirror and the load transistors should operate in strong inversion to guarantee good matching and noise properties. Thus, g_m/I_d ratio of the load transistors was set to 6.25. M9 and M10 transistors act as a load for the pre-amplifier circuit. The g_m/I_d ratio of M7, M8, M9 & M10 are equal to minimize the systematic offset. The table 6.5 shows the different parameters of MOS as calculated by the g_m/I_d method and comparison of these values with that of the simulted results.The g_m/I_d method values are very close to that of the simulated results as compared to the conventional method values.

Table 6.5: Comparison of different parameters of the Pre-amplifier as calculated by g_m/I_d method and through Simulation.

PREAMPLIFIER g_m/I_d **Method Values**	**L (µm)**	**W (µm)**	g_m **(µS)**	$\lvert I_d \rvert$ **(µA)**	$g_m / \lvert I_d \rvert$ **(1/V)**	$\lvert V_{dsat} \rvert$ **(V)**
M5	0.18	5.18	436.5	25	17.46	0.0915
M6	0.18	5.18	436.5	25	17.46	0.0915
M7	0.36	3.50	156.25	25	6.25	0.2781
M8	0.36	3.50	156.25	25	6.25	0.2781
M9	0.36	3.50	156.25	25	6.25	0.2781
M10	0.36	3.50	156.25	25	6.25	0.2781
Simulated Results	**L (µm)**	**W (µm)**	g_m **(µS)**	$\lvert I_d \rvert$ **(µA)**	$g_m / \lvert I_d \rvert$ **(1/V)**	$\lvert V_{dsat} \rvert$ **(V)**
M5	0.18	5.18	433.9	24.98	17.37	0.0925
M6	0.18	5.18	433.9	24.98	17.37	0.0925
M7	0.36	3.50	158	24.98	6.326	0.2758
M8	0.36	3.50	158	24.98	6.326	0.2758
M9	0.36	3.50	154.6	24.48	6.317	0.2758
M10	0.36	3.50	154.6	24.48	6.317	0.2758

6.3.3 SIMULATION RESULTS

The Pre-amplifier was tested separately. The width W and length L, of the MOS transistors are given in Table 6.5. The input current I_{BIAS}, is taken to have DC value of 50 µA & the current in each branch of the differential pair is set to 25 µA Figure 6.9 shows the input-output characteristic of the pre-amplifier. This curve shows the variation of the output voltage with the input voltage. Figure 6.10 shows the gain and bandwidth plot of the pre-amplifier circuit. The gain of the pre-amplifier circuit is 2.48 and the bandwidth of the circuit is 879 MHz.

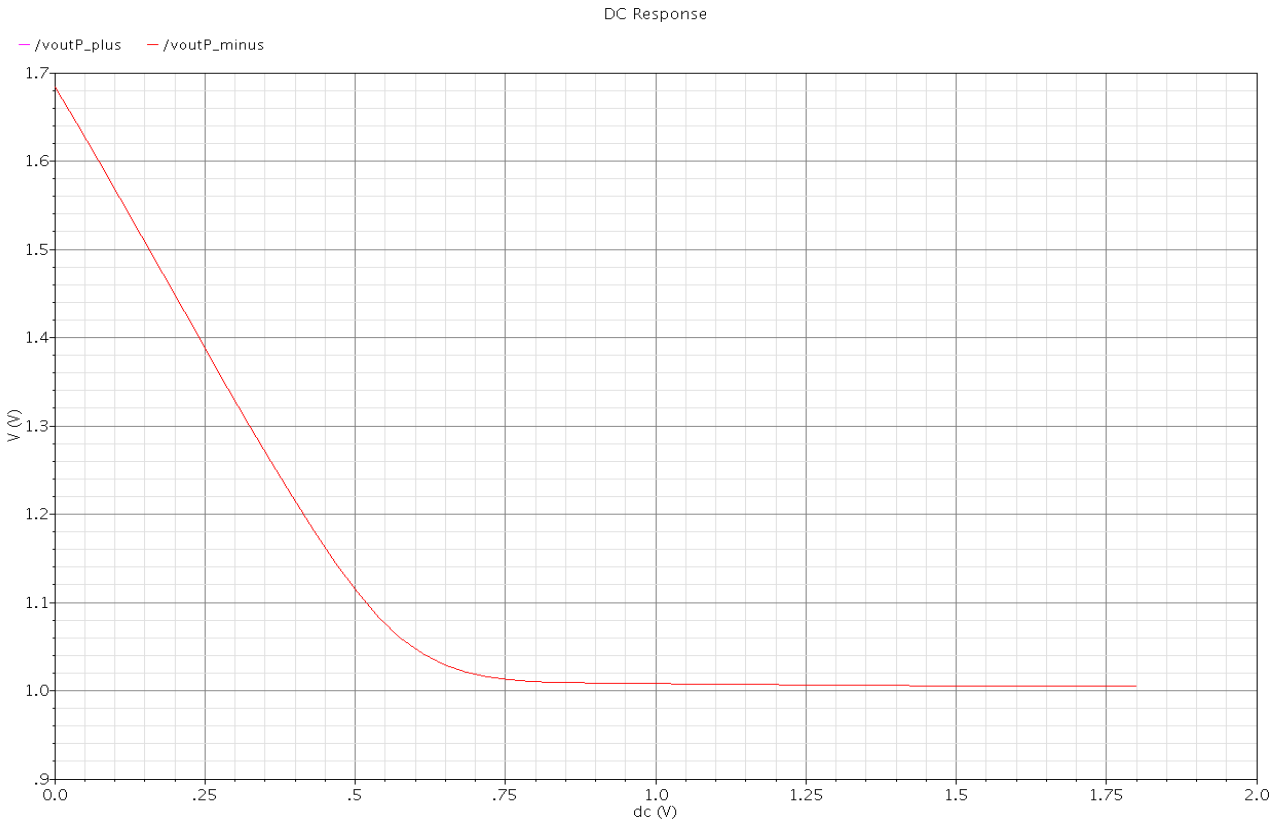


Figure 6.9: Input-Output characteristics of the Pre-amplifier circuit.

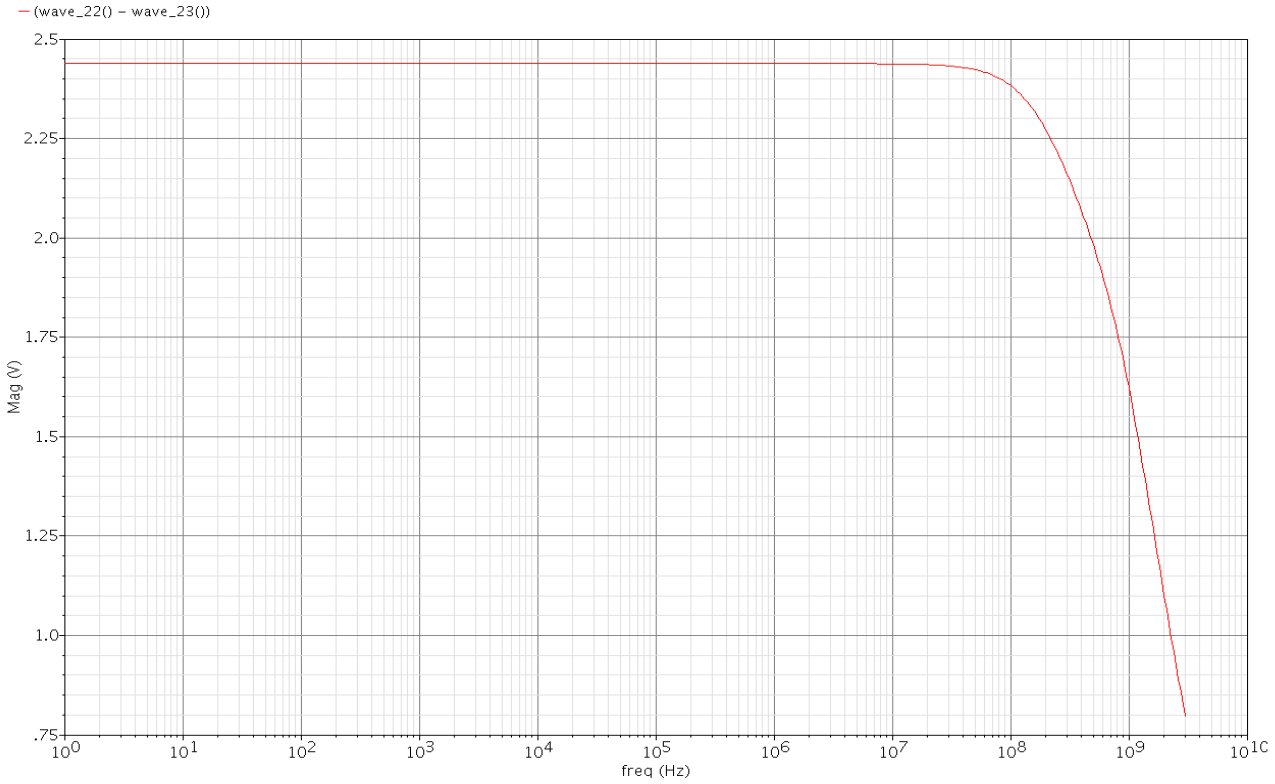


Figure 6.10: Gain & Bandwidth of the Pre-amplifier circuit.

6.4 LATCH:

The latch employs positive feedback to take the differential output from the preamplifiers and to amplify it until the differential output hits the rails.

6.4.1 DESIGNING BY CONVENTIONAL METHOD:

Figure 6.11 shows the schematic of the latch circuit.

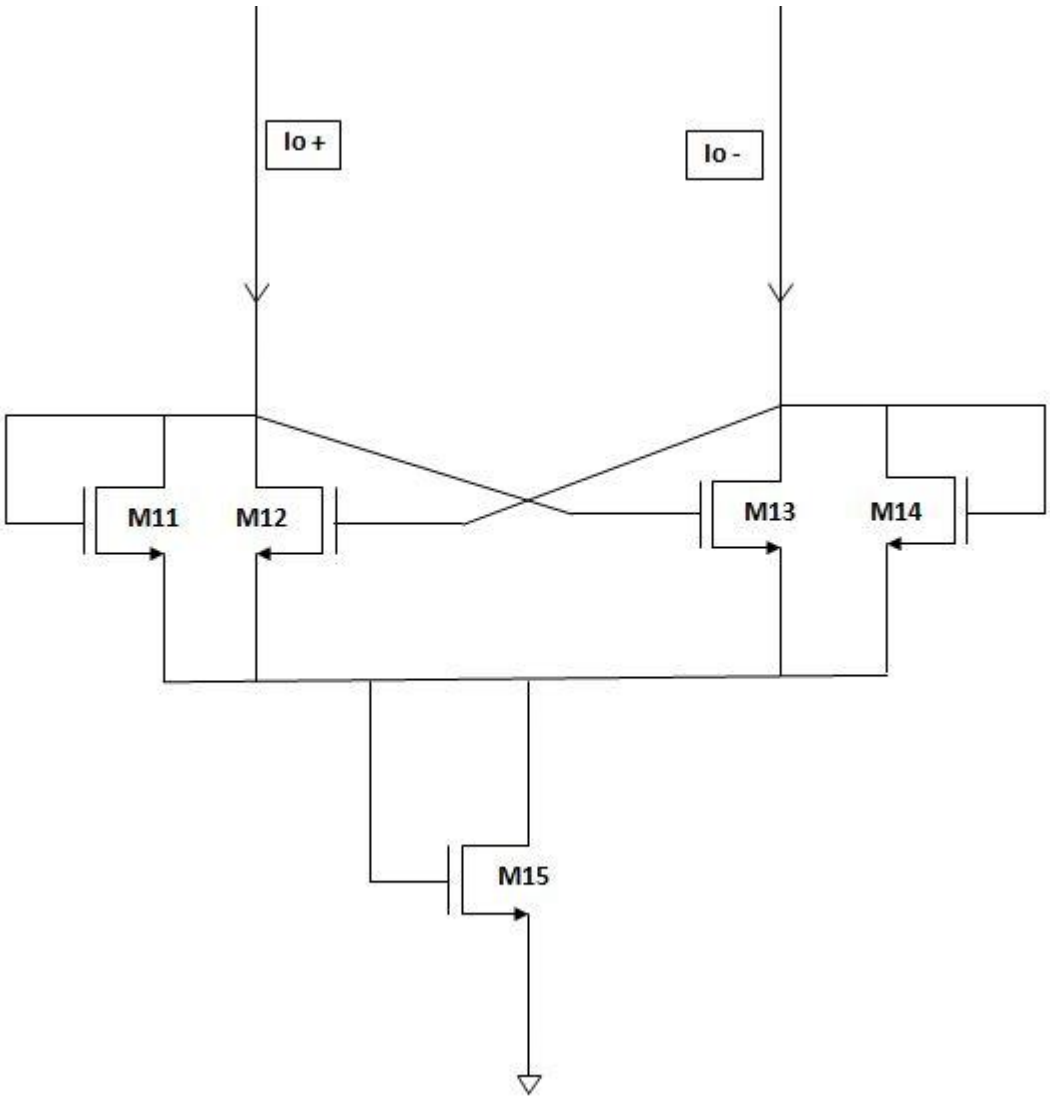


Figure 6.11: Schematic of the Latch circuit.

The sizing of the latch circuit is given in the table 6.6. The trans-conductance, current and the overdrive voltage of different transistors, as calculated by conventional method equations are also tabulated in table 6.6. The table also compares the simulated results with that of the conventional values.

Table 6.6: Comparison of different parameters of the Latch as calculated by Conventional method and through Simulation.

LATCH Conventional Method Values	L (µm)	W (µm)	g_m (µS)	$\lvert I_d \rvert$ (µA)	$\lvert V_{dsat} \rvert$ (V)
M11	0.18	0.27	104	12.5	0.24
M12	0.18	0.27	104	12.5	0.24
M13	0.18	0.27	104	12.5	0.24
M14	0.18	0.27	104	12.5	0.24
M15	0.18	6	695.22	50	0.1438
Simulated Results	**L (µm)**	**W (µm)**	**g_m (µS)**	**$\lvert I_d \rvert$ (µA)**	**$\lvert V_{dsat} \rvert$ (V)**
M11	0.18	0.27	91.75	12.31	0.213
M12	0.18	0.27	91.75	12.31	0.213
M13	0.18	0.27	91.75	12.31	0.213
M14	0.18	0.27	91.75	12.31	0.213
M15	0.18	6	746.1	49.26	0.108

6.4.2 DESIGNING BY g_m/I_d METHOD:

The sizing of the latch transistors is done in such a way that g_m/I_d value of M9 and M10 is equal to the g_m/I_d value of M7 and M8 i.e. 6.25. This will also helps in minimizing the systematic offset. The table 6.7 shows the different parameters of MOS as calculated by the g_m/I_d method and comparison of these values with that of the simulted results.

Table 6.7: Comparison of different parameters of the Latch as calculated by g_m/I_d method and through Simulation.

LATCH g_m/I_d Method Values	L (µm)	W (µm)	g_m (µS)	$\lvert I_d \rvert$ (µA)	$g_m / \lvert I_d \rvert$ (1/V)	$\lvert V_{dsat} \rvert$ (V)
M11	0.18	0.27	111.9	12.5	8.952	0.1696
M12	0.18	0.27	111.9	12.5	8.952	0.1696
M13	0.18	0.27	111.9	12.5	8.952	0.1696
M14	0.18	0.27	111.9	12.5	8.952	0.1696
M15	0.18	6	755	50	15.1	0.1093

Simulated Results	L (µm)	W (µm)	g_m (µS)	$\lvert I_d \rvert$ (µA)	$g_m / \lvert I_d \rvert$ (1/V)	$\lvert V_{dsat} \rvert$ (V)
M11	0.18	0.27	91.52	12.24	7.478	0.2126
M12	0.18	0.27	91.52	12.24	7.478	0.2126
M13	0.18	0.27	91.52	12.24	7.478	0.2126
M14	0.18	0.27	91.52	12.24	7.478	0.2126
M15	0.18	6	742.8	48.96	15.17	0.1083

6.5 SELF-BIASED DIFFERENTIAL AMPLIFIER WITH OUTPUT INVERTOR:

The self-biased differential amplifier or Fully Complementary Self-Biased CMOS Differential Amplifier (CSDA) is shown in figure 6.12.The CSDA is followed by simple inverter shown in figure 6.13.

6.5.1 DESIGNING BY CONVENTIONAL METHOD:

The sizing of the CSDA and output invertor is given in the table 6.6. The trans-conductance,

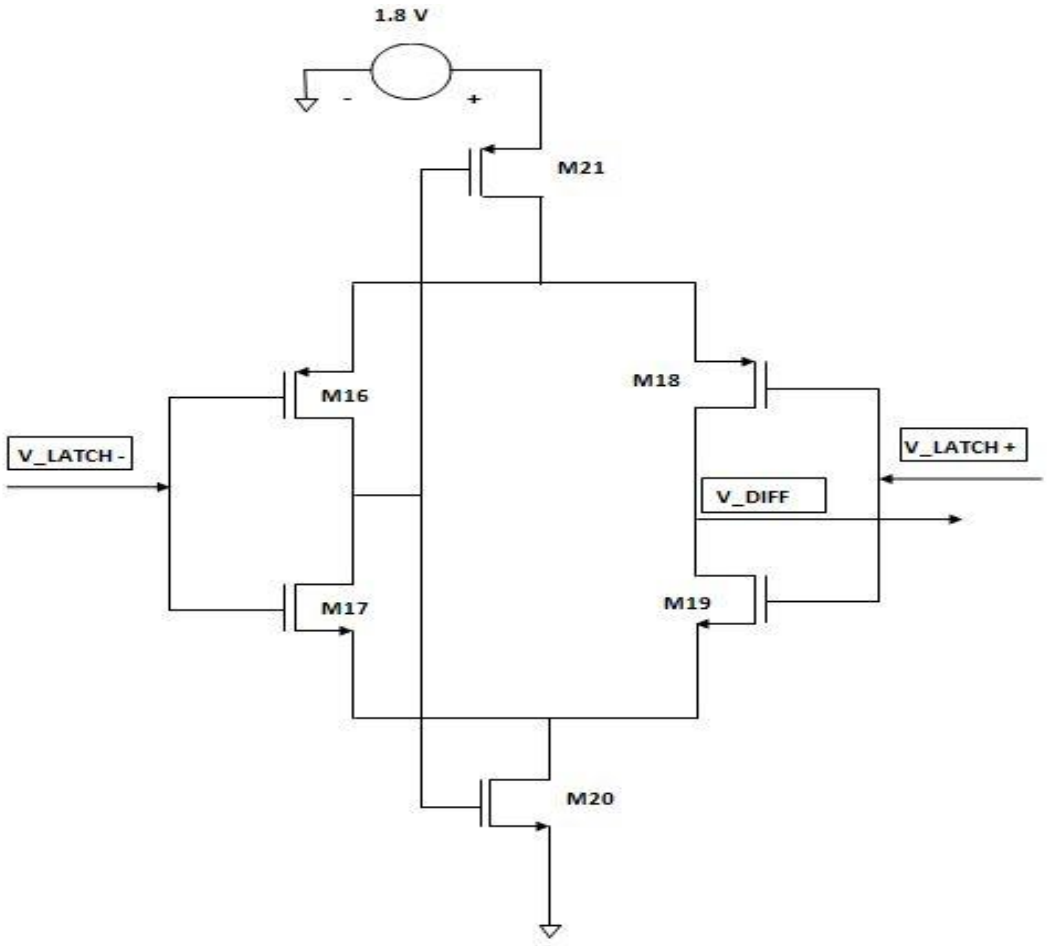


Figure 6.12: Schematic of the Self-biased Differential amplifier (CSDA) circuit.

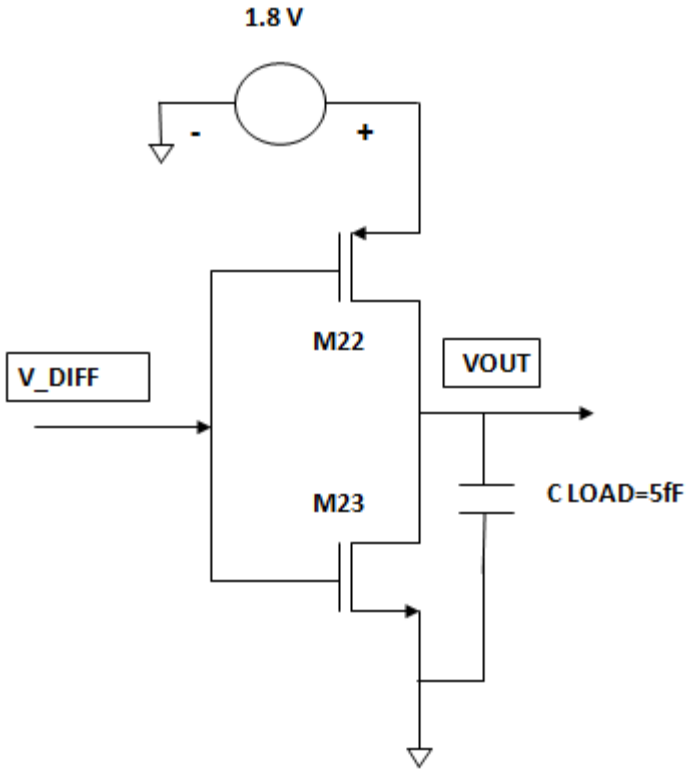


Figure 6.13: Schematic of the output invertor circuit.

The output has the purpose to increase further the gain and make the comparator more precise. Current and the overdrive voltage of different transistors, as calculated by conventional method equations are also tabulated in table 6.8. The table also compares the simulated results with that of the conventional values.

Table 6.8: Comparison of different parameters of the CSDA & Output Invertor as calculated by Conventional method and through Simulation.

CSDA & OUTPUT INVERTOR **Conventional Method Values**	**L (µm)**	**W (µm)**	**g_m (µS)**	**$\lvert I_d \rvert$ (µA)**	**$\lvert Vdsat \rvert$ (V)**
M16	0.18	0.24	58	4.35	0.150
M17	0.18	0.24	85	9.35	0.220
M18	0.18	0.24	58	4.35	0.150
M19	0.18	0.24	85	9.35	0.220
M20	0.18	0.24	50.3	3.27	0.130
M21	0.18	0.24	228	67.29	0.590

M22	0.18	0.36	347	104.39	0.60
M23	0.18	0.36	86.93	6.52	0.15
Simulated Results	**L (µm)**	**W (µm)**	**g_m (µS)**	**$\lvert I_d \rvert$ (µA)**	**$\lvert V_{dsat} \rvert$ (V)**
M16	0.18	0.24	14.99	1.367	0.1535
M17	0.18	0.24	7.021	1.367	0.2179
M18	0.18	0.24	14.99	1.367	0.1535
M19	0.18	0.24	7.021	1.367	0.2179
M20	0.18	0.24	37.54	2.734	0.1345
M21	0.18	0.24	2.852	2.734	0.597
M22	0.18	0.36	6.317	6.069	0.672
M23	0.18	0.36	76.27	6.069	0.142

6.5.2 DESIGNING BY g_m/I_d METHOD:

The sizing of the latch transistors is done in such a way that g_m/I_d value of M9 and M10 is equal to the g_m/I_d value of M7 and M8 i.e. 6.25. This will also helps in minimizing the systematic offset. The table 6.9 shows the different parameters of MOS as calculated by the g_m/I_d method and comparison of these values with that of the simulted results.

Table 6.9: Comparison of different parameters of the CSDA & Output Invertor as calculated by g_m/I_d method and through Simulation.

CSDA & OUTPUT INVERTOR g_m/I_d Method Values	**L (µm)**	**W (µm)**	**g_m (µS)**	**$\lvert I_d \rvert$ (µA)**	**$g_m / \lvert I_d \rvert$ (1/V)**	**$\lvert V_{dsat} \rvert$ (V)**
M16	0.18	0.24	14.70	1.377	10.68	0.1492
M17	0.18	0.24	7.661	1.377	5.564	0.2233
M18	0.18	0.24	14.70	1.377	10.68	0.1492
M19	0.18	0.24	7.661	1.377	5.564	0.2233
M20	0.18	0.24	35.18	2.755	12.77	0.1291
M21	0.18	0.24	2.701	2.755	0.9806	0.469
M22	0.18	0.24	6.262	6.11	1.025	0.4618
M23	0.18	0.24	78.0247	6.11	12.77	0.1291
Simulated Results	**L (µm)**	**W (µm)**	**g_m (µS)**	**$\lvert I_d \rvert$ (µA)**	**$g_m / \lvert I_d \rvert$ (1/V)**	**$\lvert V_{dsat} \rvert$ (V)**
M16	0.18	0.24	15.06	1.377	10.94	0.154

M17	0.18	0.24	7.126	1.377	5.173	0.217
M18	0.18	0.24	15.06	1.377	10.94	0.154
M19	0.18	0.24	7.126	1.377	5.173	0.217
M20	0.18	0.24	37.75	2.755	13.7	0.1348
M21	0.18	0.24	2.878	2.755	1.045	0.597
M22	0.18	0.36	6.367	6.11	1.042	0.672
M23	0.18	0.36	76.59	6.11	12.53	0.1423

6.6 SIMULATION RESULTS OF THE COMPARATOR:

In this section, the comparator that was discussed in the previous section will be analyzed for their offset voltage, gain, propagation time delay, power dissipation using Cadence Spectre and Virtuoso® Analog Design Environment simulation. All the parameters of the Comparator at the schematic level are shown below.

6.6.1 DC ANALYSIS:

For calculating DC analysis, both inputs V_{in+} & V_{in-} are taken as the DC voltage source. An important parameter of the comparator is its offset voltage. Offset voltage of the comparator was measured by taking the value of input, V_{in-}, at 850 mV and the input, V_{in+} of the comparator swept from 0 to 1.8. The temperature is 27℃. From the figure 6.15, we can see that the systematic offset voltage is approximately 5 mV.

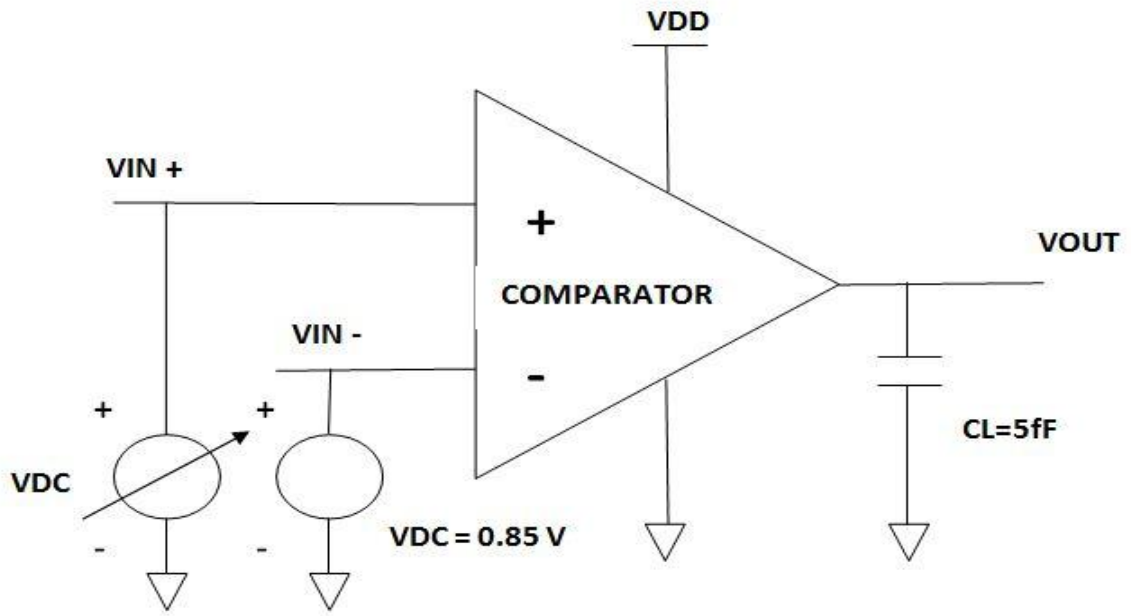


Figure 6.14: Test setup of comparator for DC response.

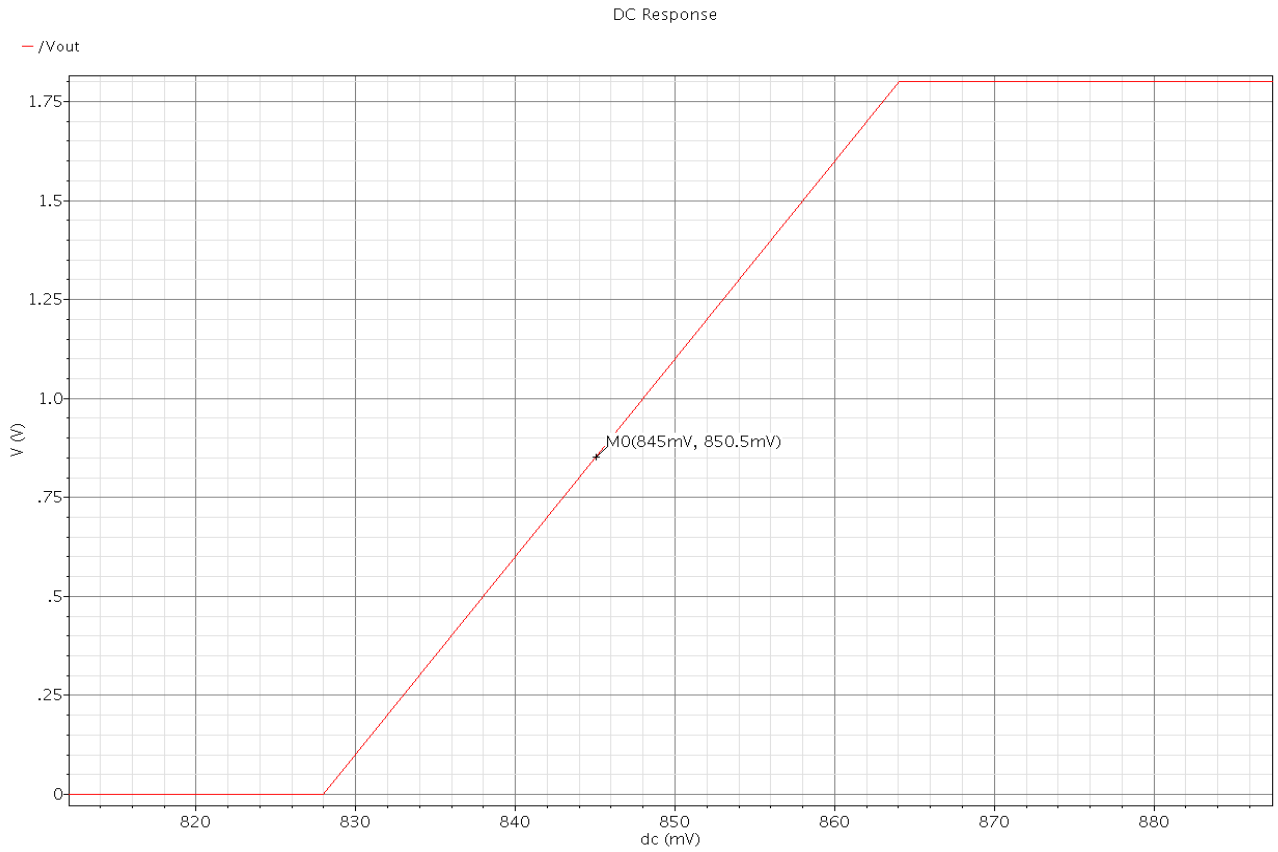


Figure 6.15: DC characteristics of the Comparator.

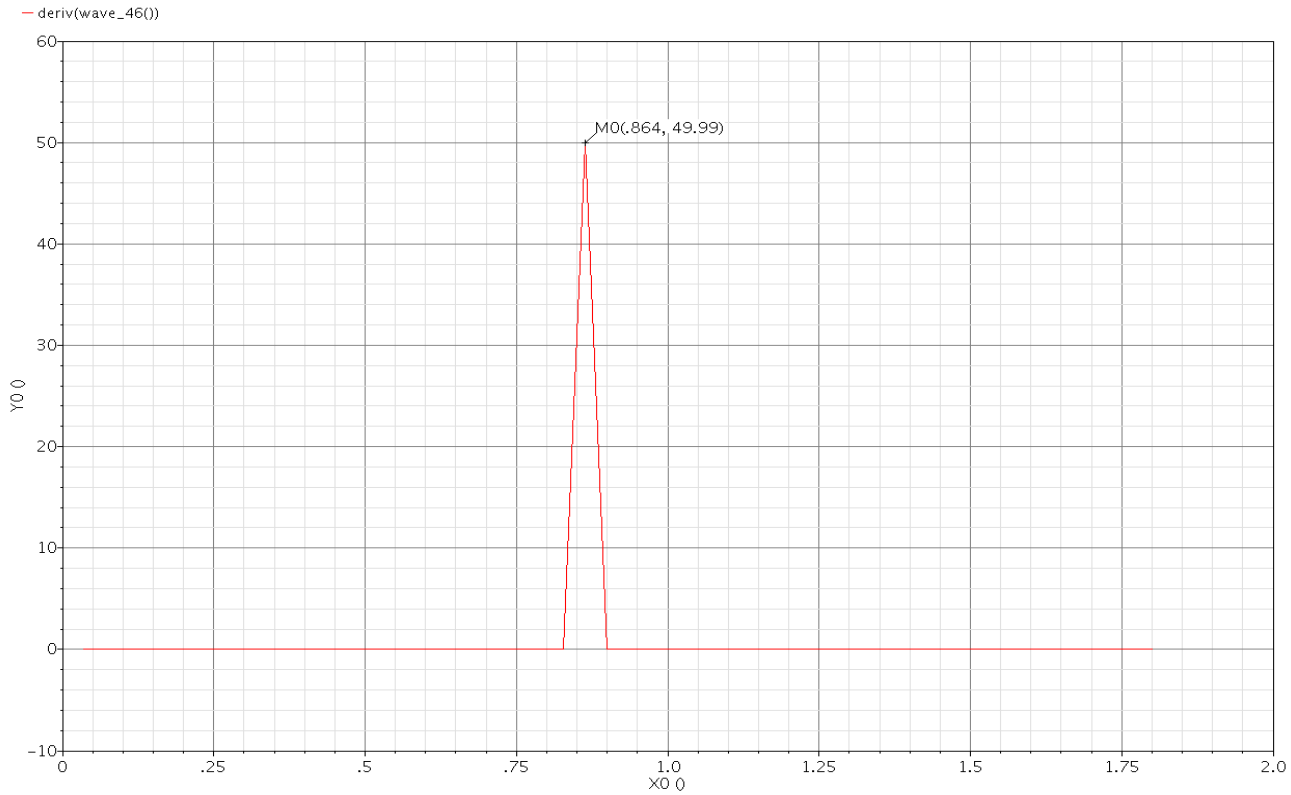


Figure 6.16: Comparator gain as a function of the input voltage.

If we take the derivative of the transfer curve, the gain of the comparator and thus the smallest difference i.e. resolution that can be discriminated between V_{in+} and V_{in-} become known. Figure 6.16 shows the gain of the comparator at about 50 (49.99) so that approximately 36 mV as shown in figure 6.17 is needed to make the comparator output changes logic levels.

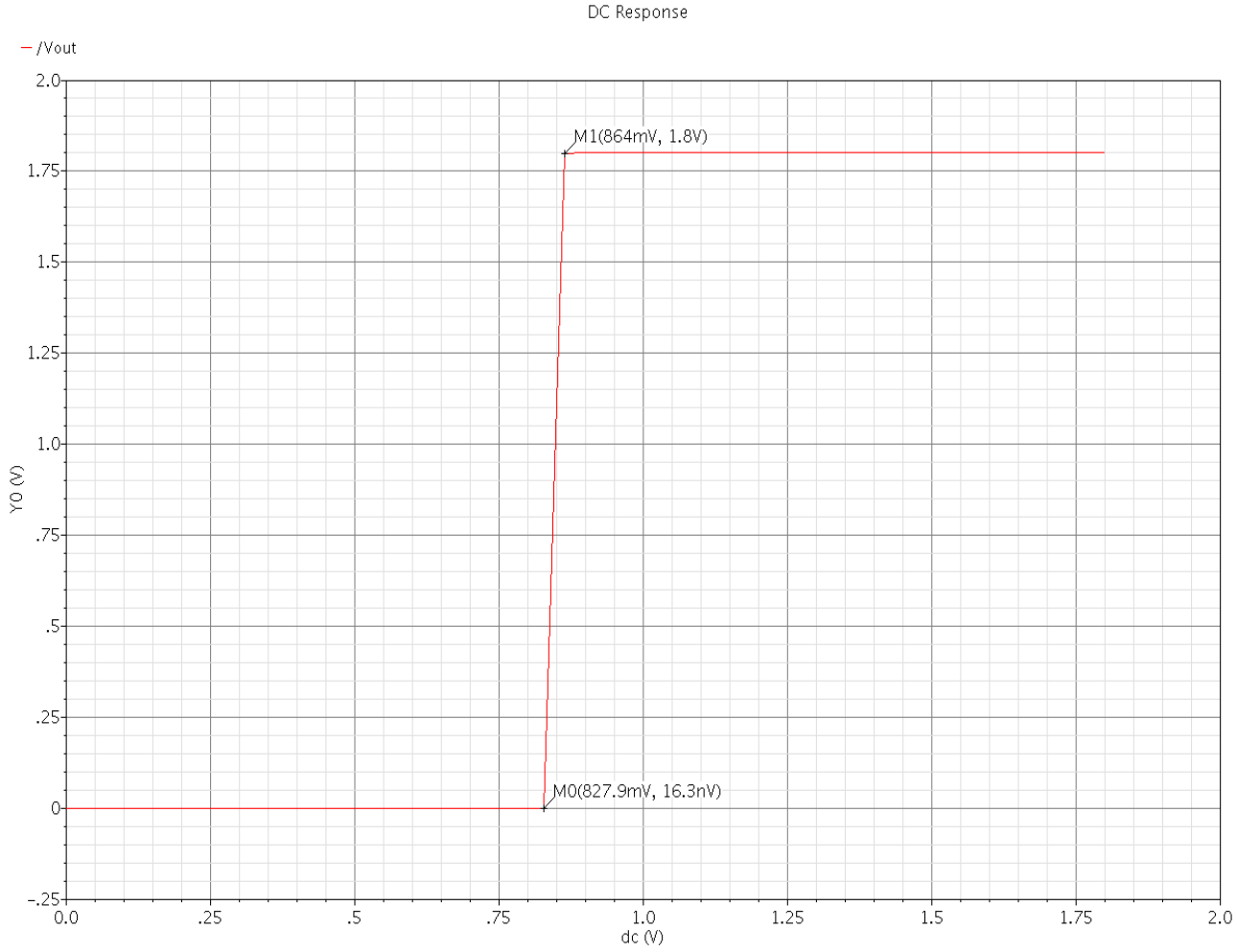


Figure 6.17: Comparator output as a function of the input voltage.

6.6.2 AC ANALYSIS:

For calculating AC analysis, the input voltage V_{in+} is the AC voltage source and V_{in-} is taken as the DC voltage source, as shown in figure 6.18. Using the AC analysis, we find pre-amplifier gain and bandwidth. Figure 6.19 shows the obtained Gain and Bandwidth of the pre-amplifier are 7.898 dB and 879 MHz respectively.

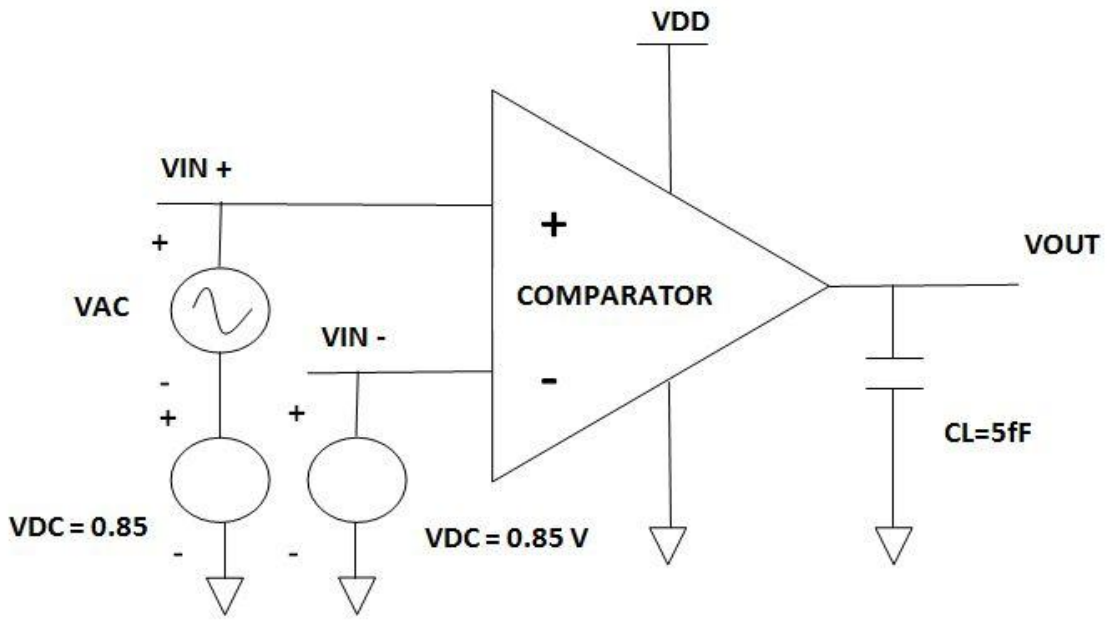


Figure 6.18: Test setup of comparator for AC response.

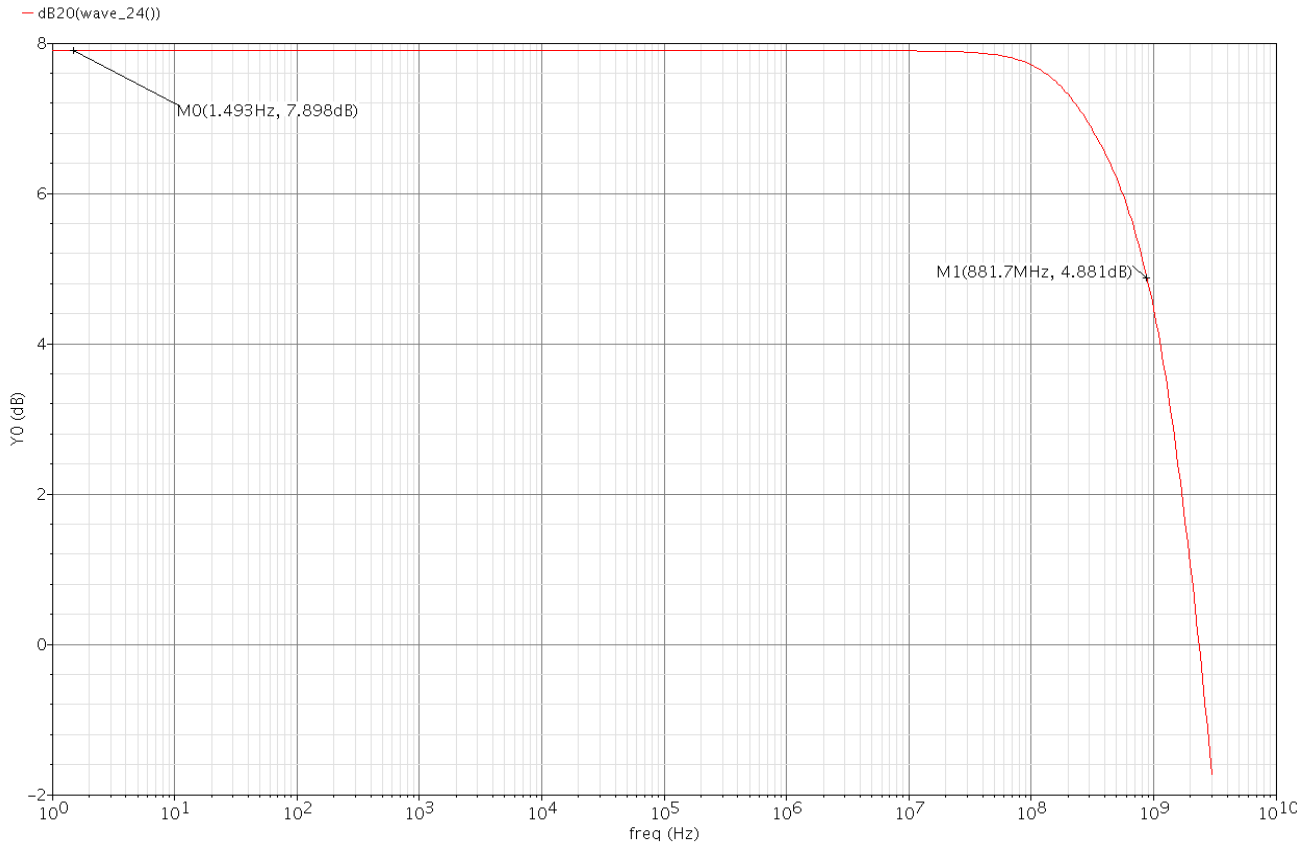


Figure 6.19: AC response of the Comparator.

6.6.3 TRANSIENT ANALYSIS:

For observing the transient response of comparator a AC voltage source of 40mV and 100MHz frequency is applied to the input, V_{in+} and the V_{in-} was set to 850 mV. We are driving the V_{in+} input of the comparator 40 mV over the V_{in-}.The transient response of the comparator is shown in the figure 6.20.

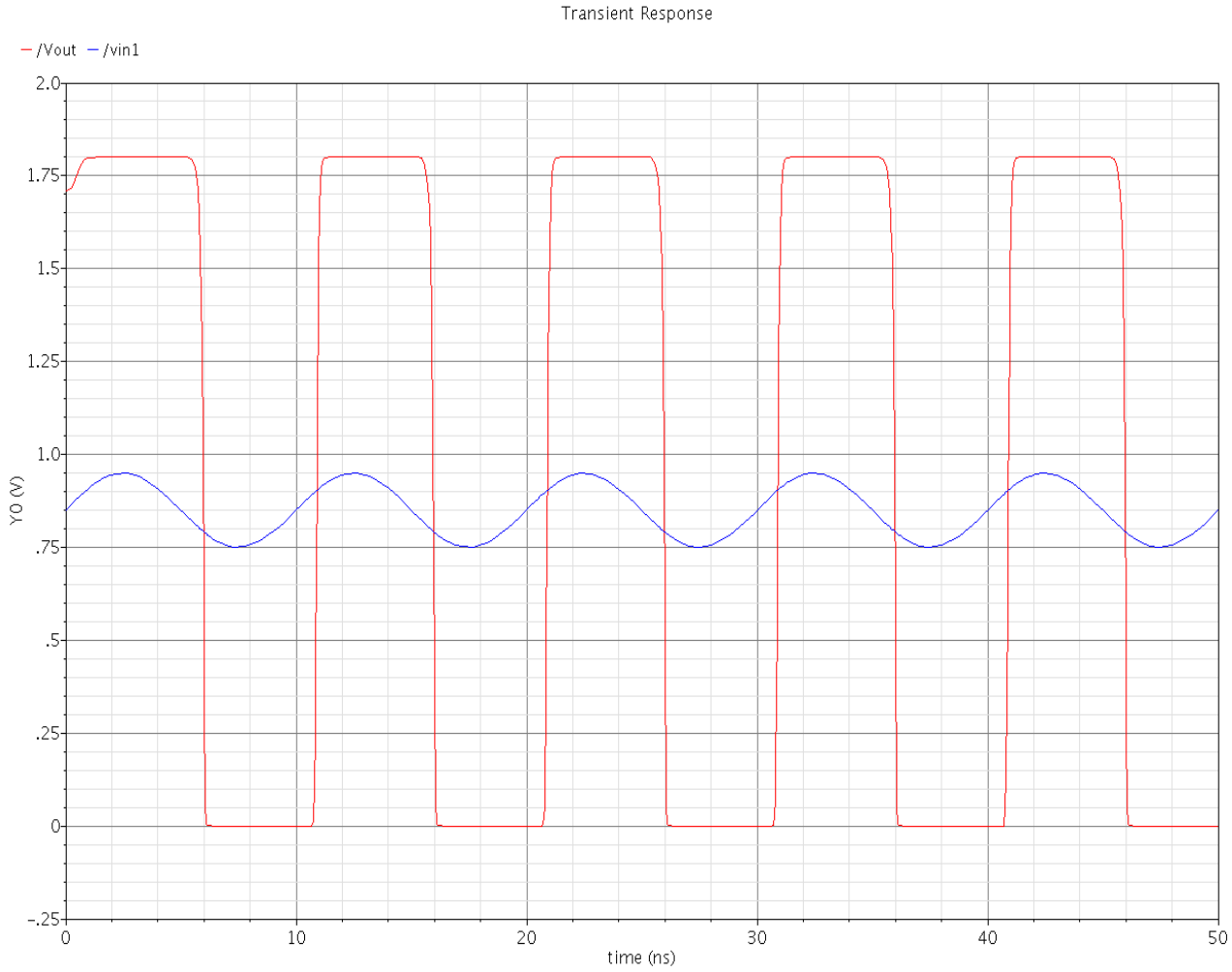


Figure 6.20: The transient response of the Comparator.

Figure 6.21 shows the variation of the comparator output voltage with that of the variation in input voltage. The comparator delay is dependent upon the input voltage; this is shown in figure 6.21.The transient analysis is also used to calculate the delay of the comparator. Here, the given input pulse is 0 to 1.8 V to one of the input of the comparator and other input is given reference voltage of 0.85 V. Figure 6.22 is used for calculating the delay of the Comparator. The propagation time delay, for the comparator obtained from the above figure 6.21 is 0.643 ns. The power dissipation of the comparator is 0.223 mW.

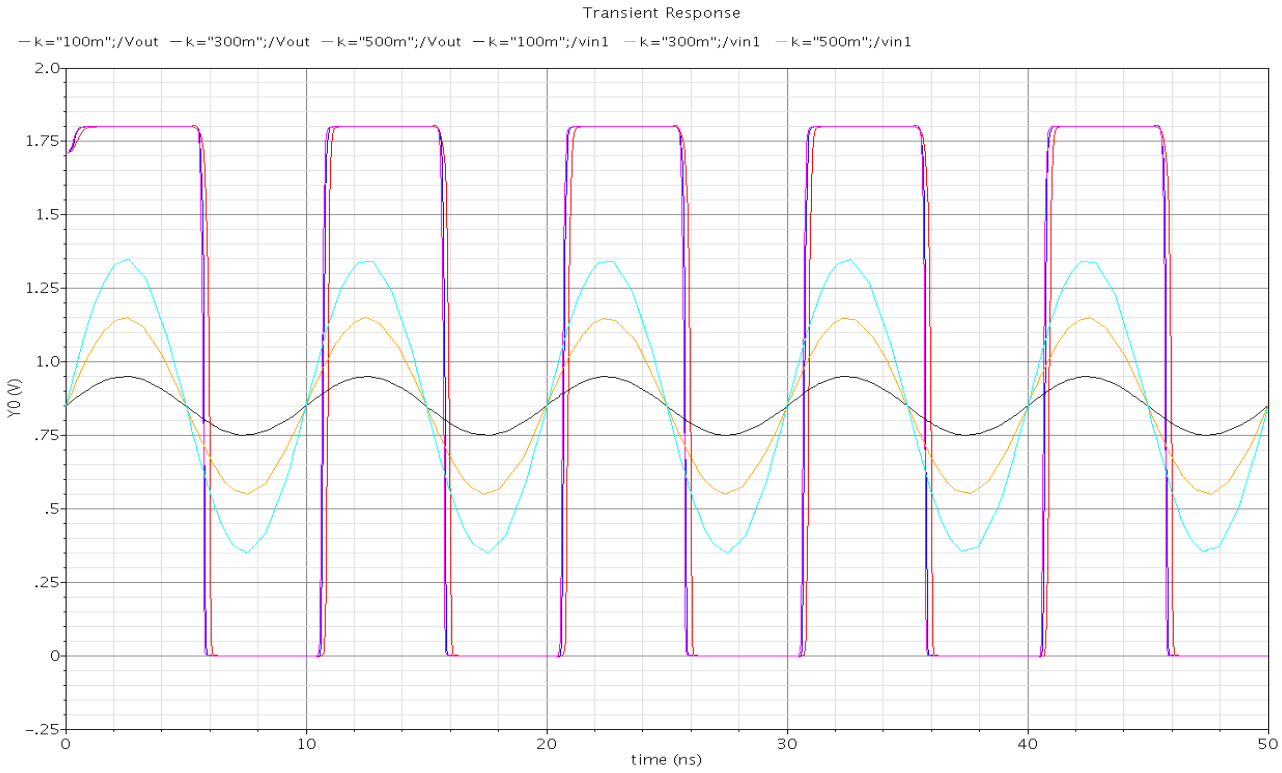


Figure 6.21: Variation of the Comparator output voltage with input voltage.

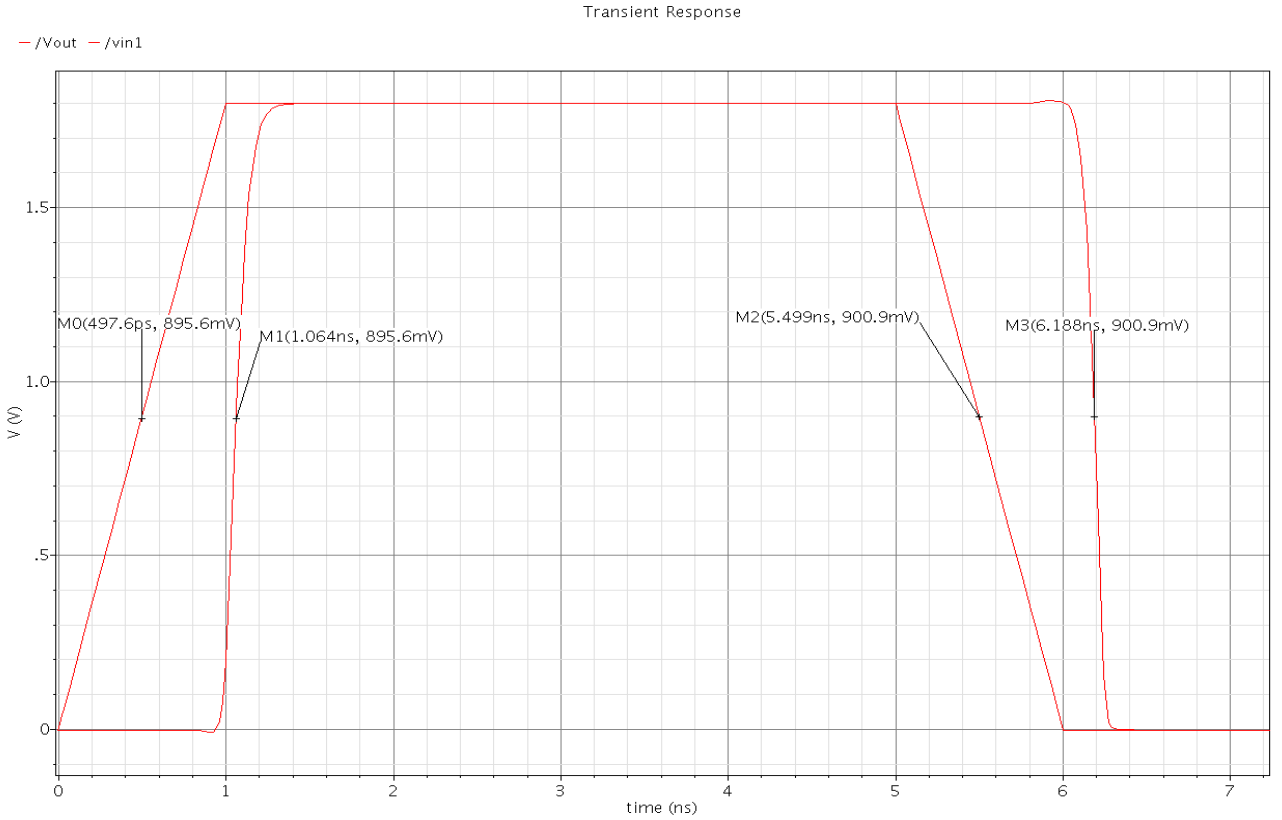


Figure 6.22: Output voltage of the comparator when input step voltage is applied.

CHAPTER 7

LAYOUT DESIGN

This chapter describes the layout design of various blocks of Comparator. The UMC 0.18 µm CMOS technology with 1P6M process technology file is used to draw all the layouts. The Virtuoso layout editor, Assura verification tool and Assura XRC are used for layout, DRC/LVS and parasitic extractions, respectively. The layouts of various building blocks of the Comparator such as cascode current mirror, pre-amplifier, latch, comparator without load capacitance and comparator with load capacitance are shown in Figures 7.1(a)- (c), 7.2(a)-(c), 7.3(a)-(b), 7.4(a)- (b), and 7.5(a)- (c) respectively.

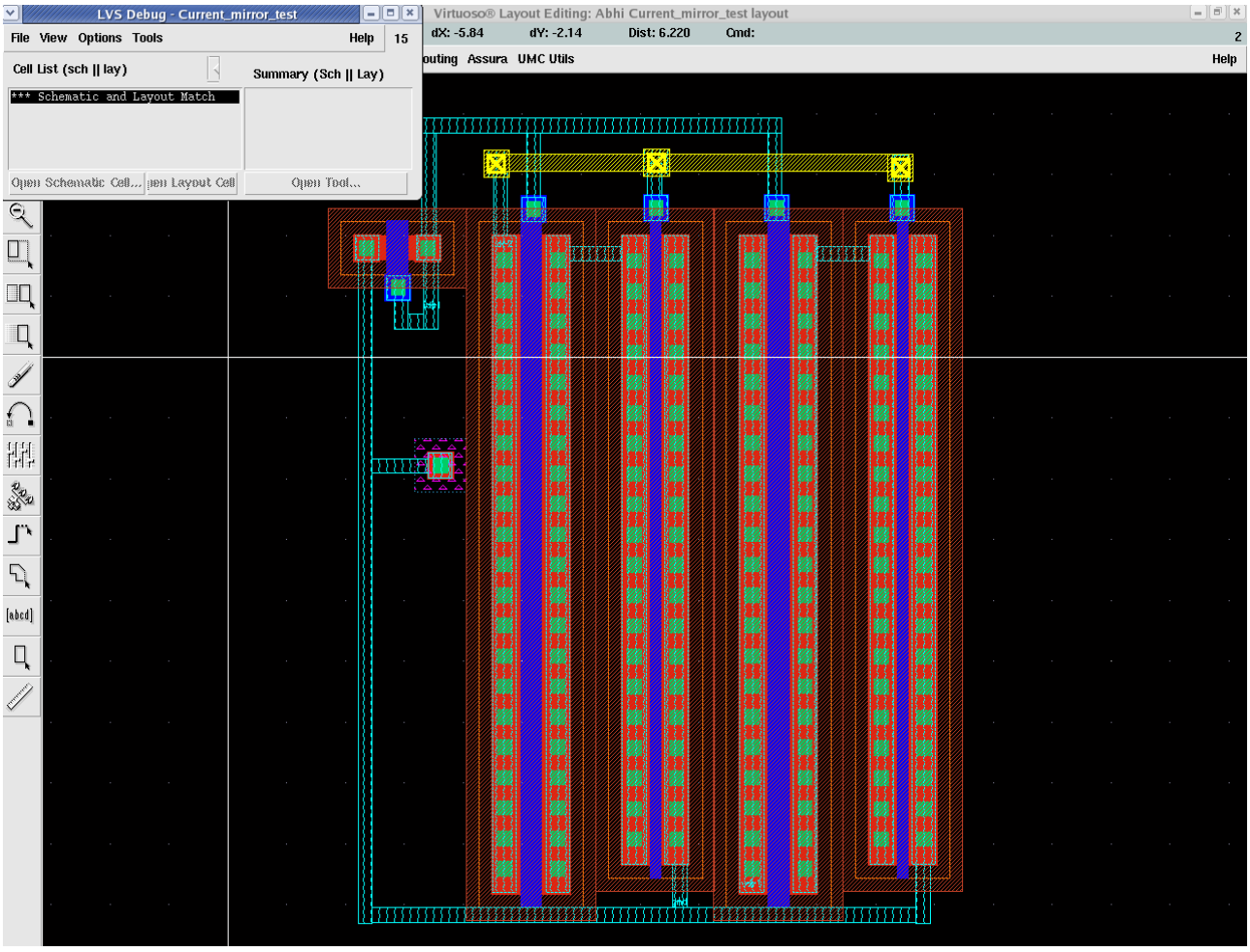


Figure 7.1(a): Layout of the high-swing cascode current mirror.

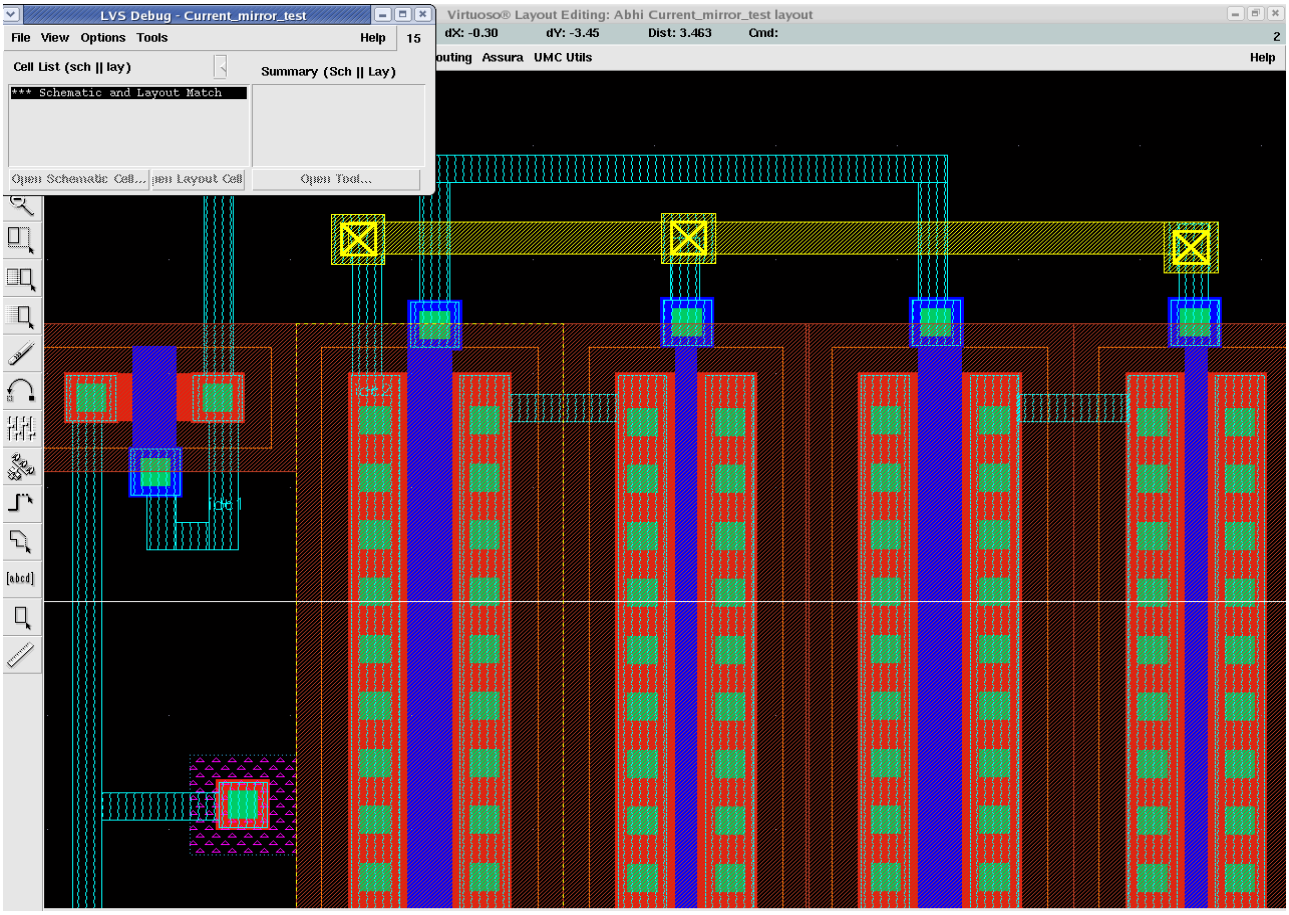


Figure 7.1(b): Layout vs Schematic match of high-swing cascode current mirror.

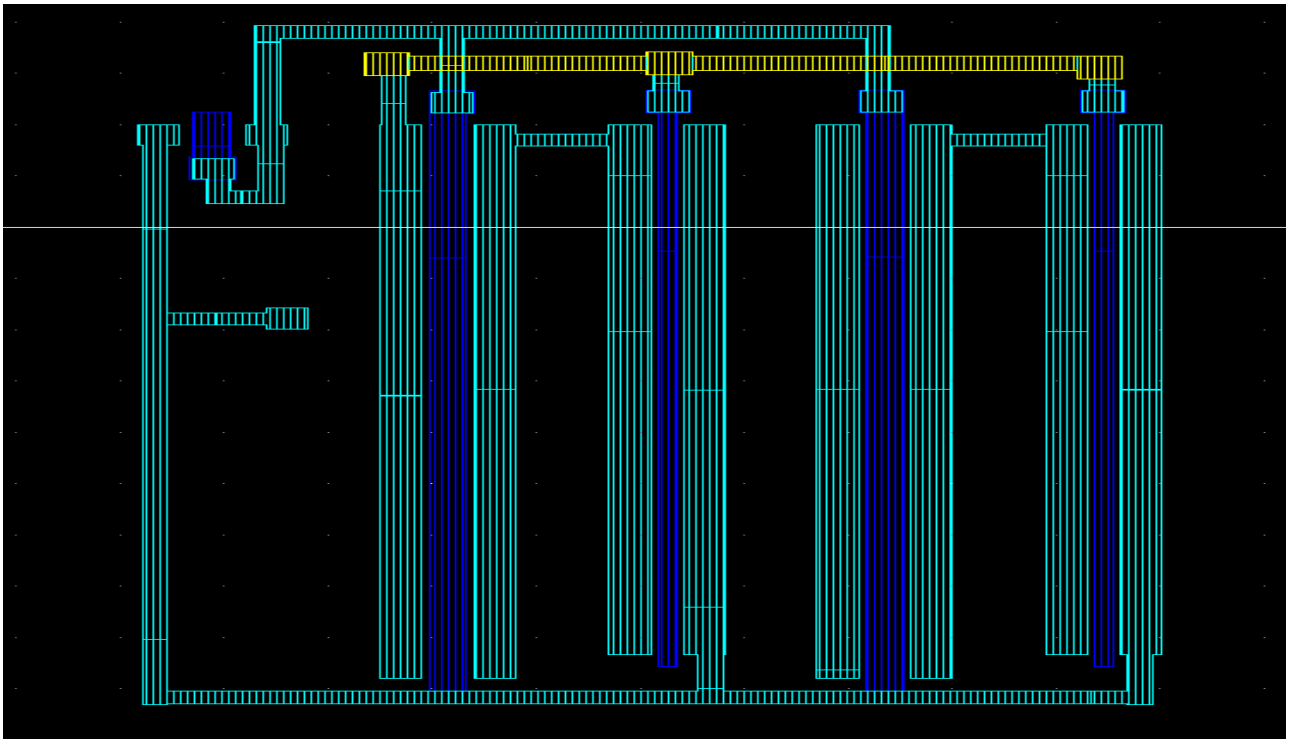


Figure 7.1(c): RCX extracted view of high-swing cascode current mirror.

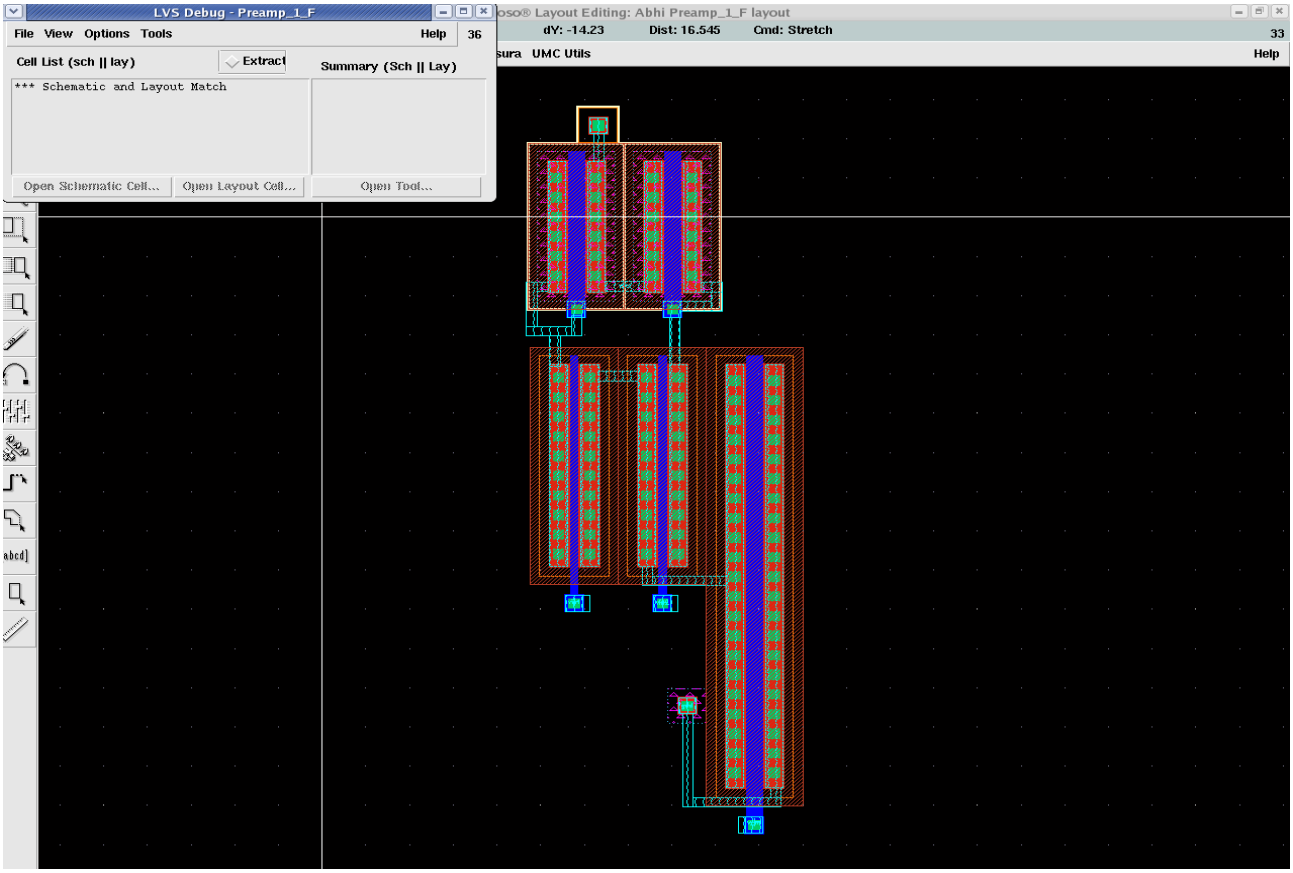


Figure 7.2(a): Layout of the Pre-amplifier circuit.

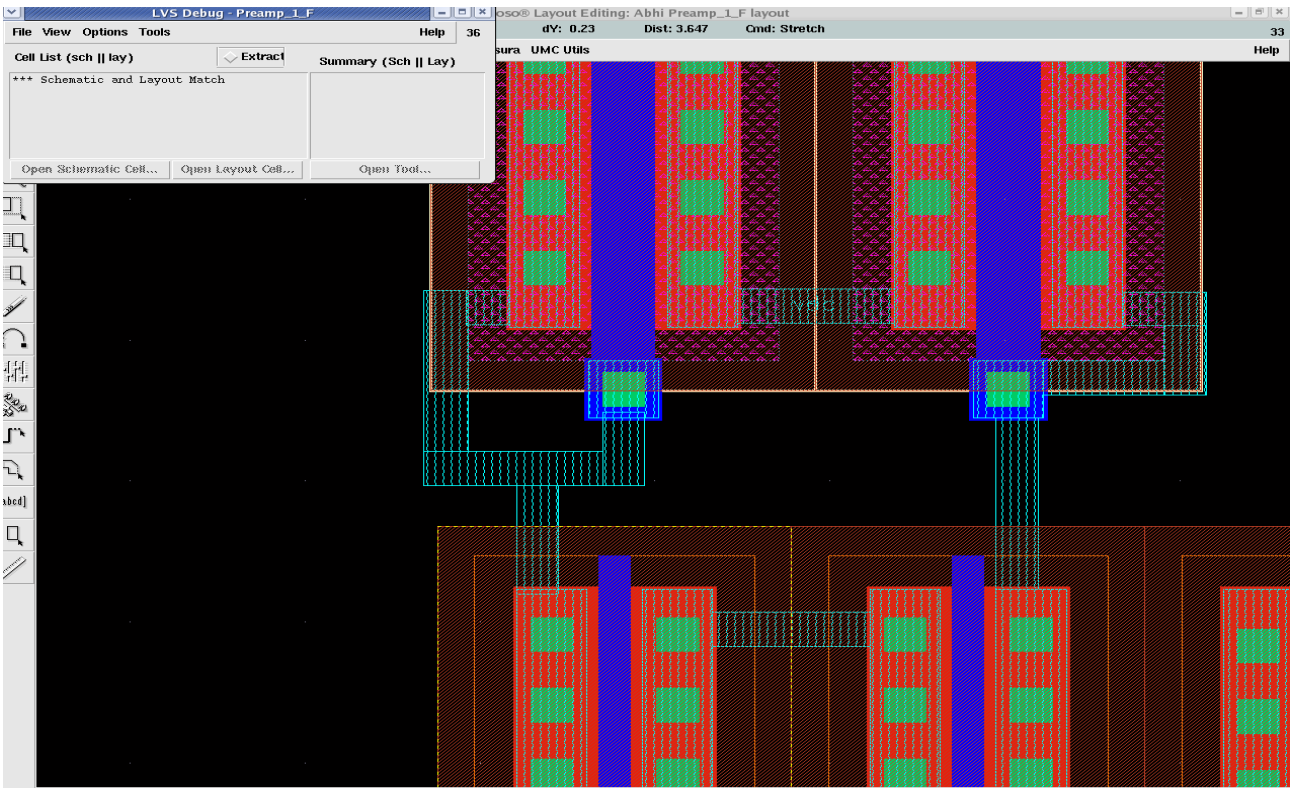


Figure 7.2(b): Layout Vs Schematic match of the Pre-amplifier circuit.

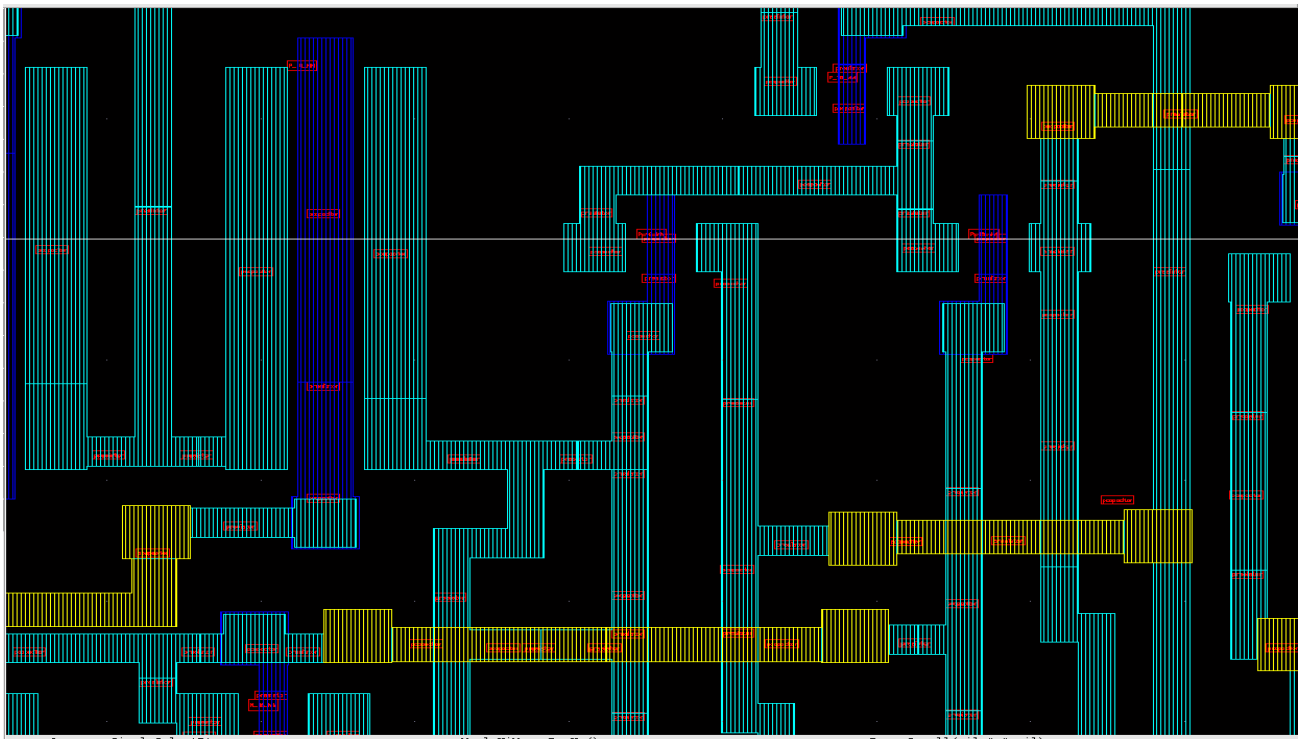


Figure 7.2(c): RCX extracted view of the Pre-amplifier circuit.

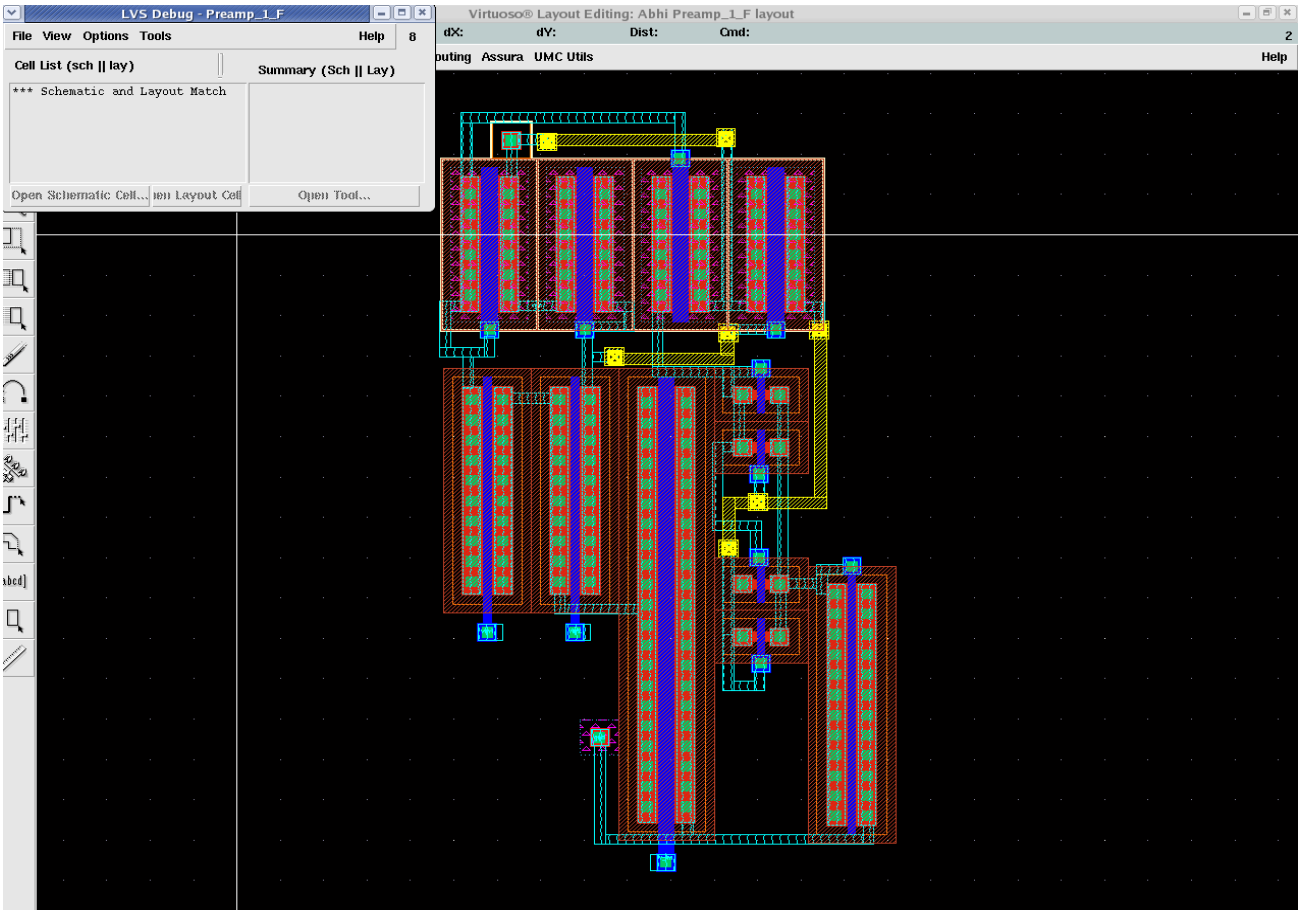


Figure 7.3(a): Layout of the Pre-amplifier with latch circuit.

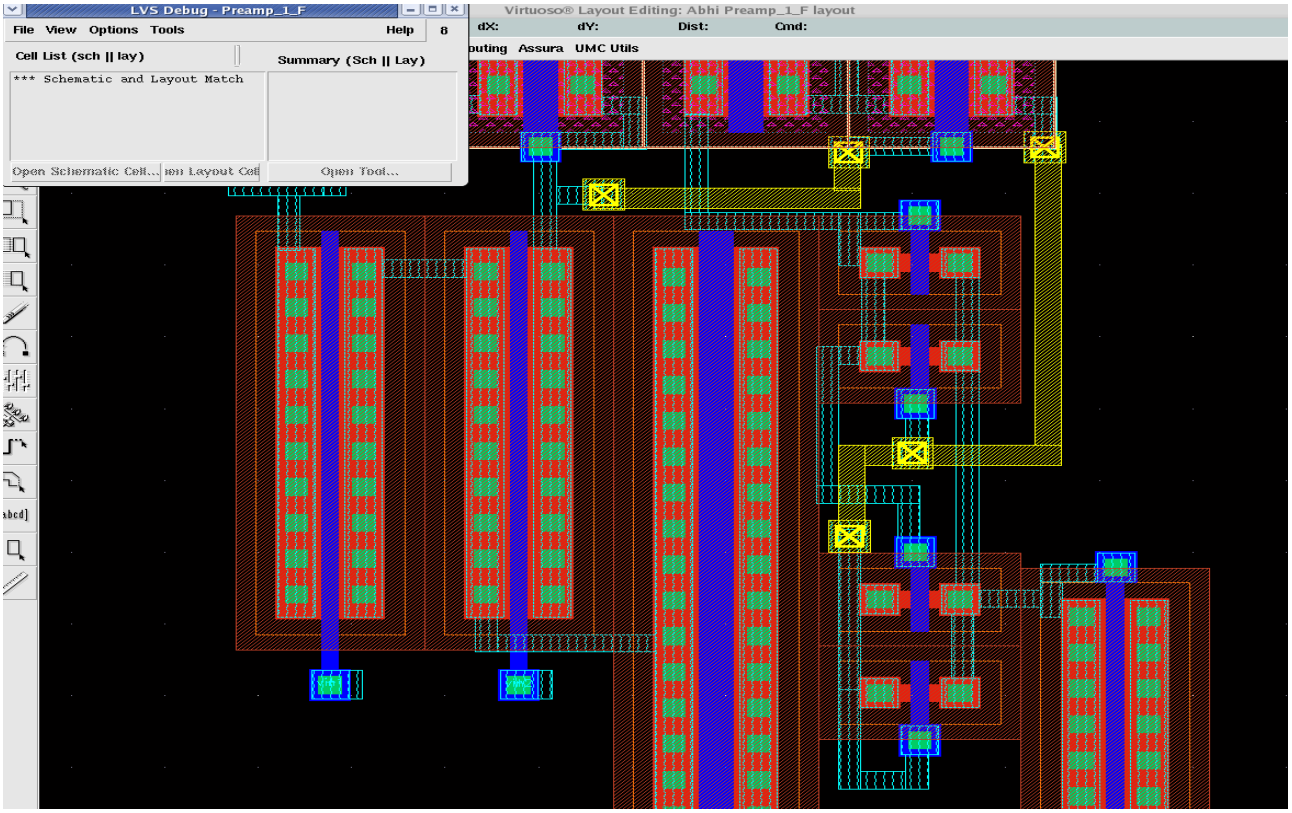


Figure 7.3(b): Layout vs Schematic match of the Pre-amplifier with latch circuit.

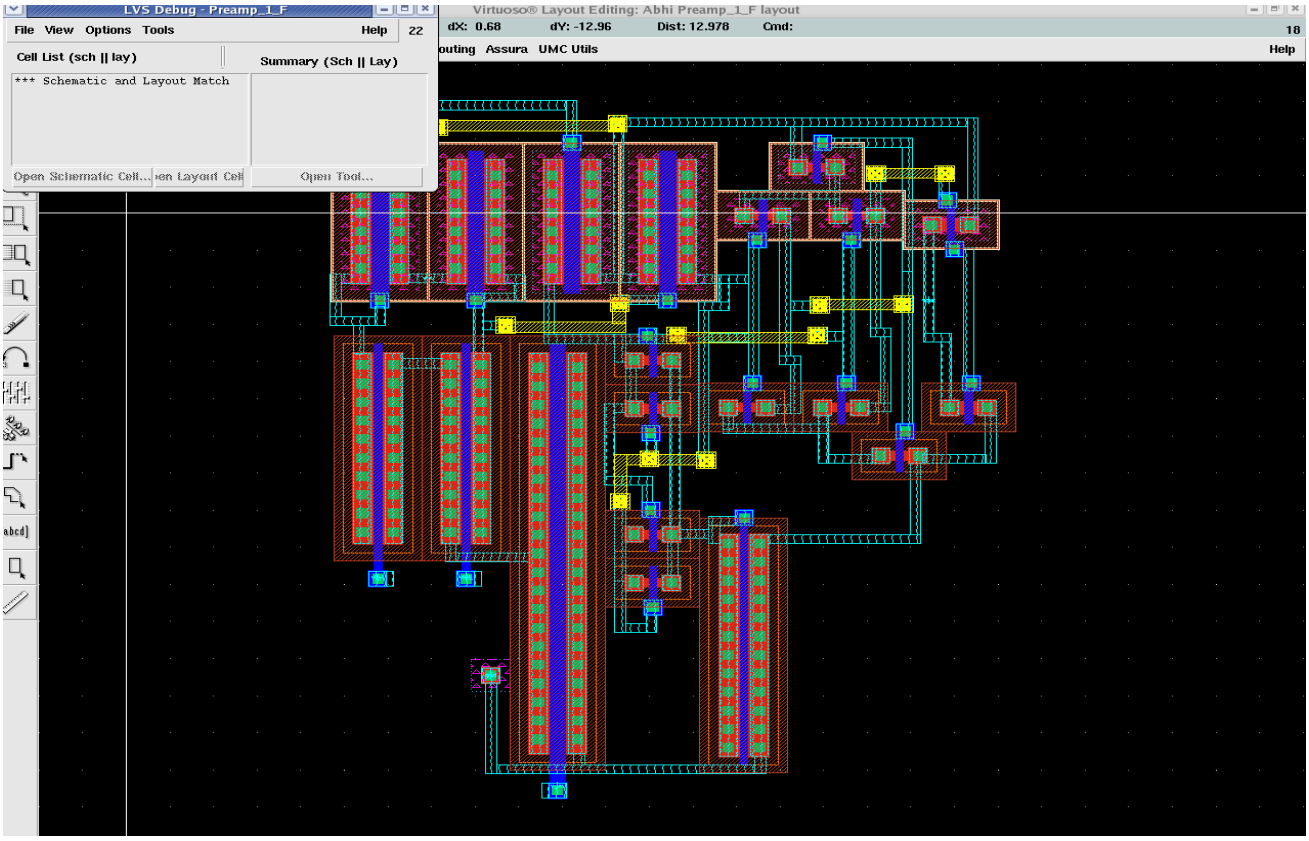


Figure 7.4(a): Layout of the Comparator without load capacitance.

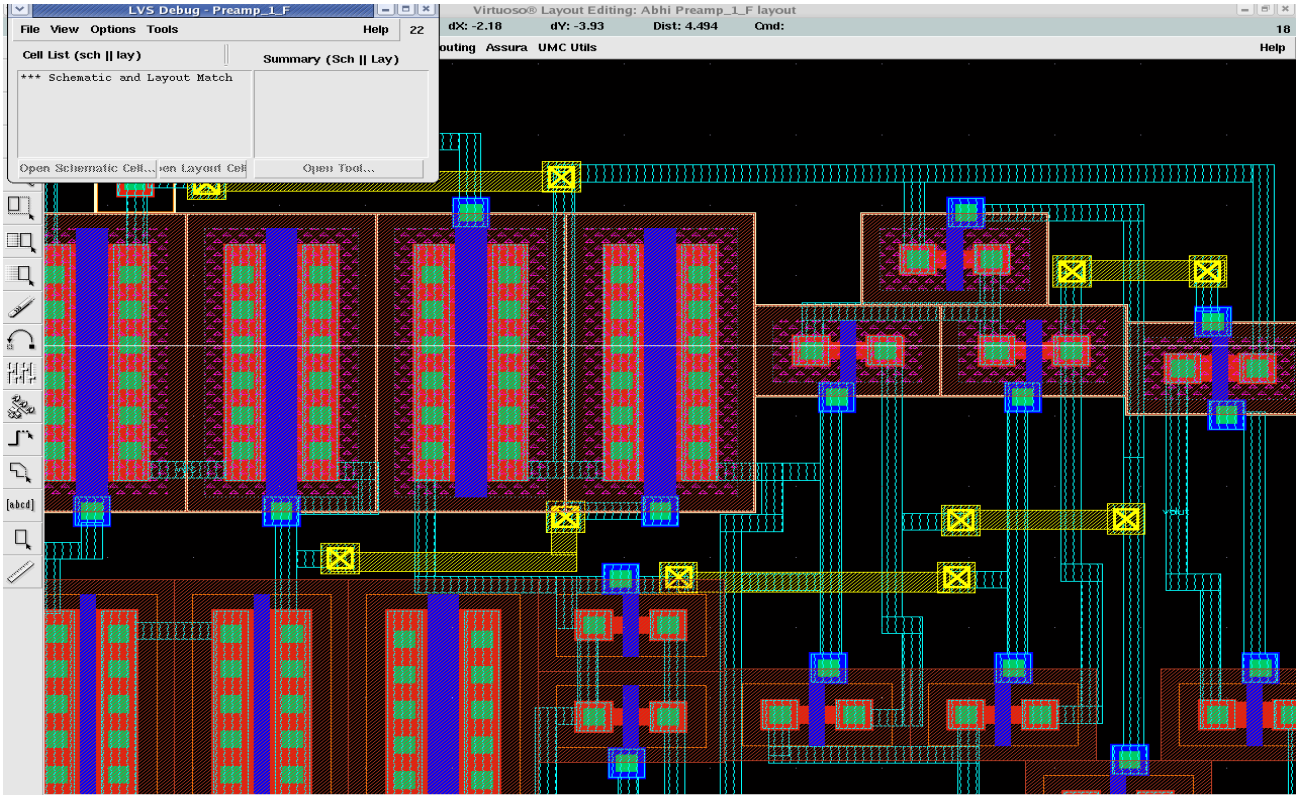


Figure 7.4(b): Layout vs Schematic match of the Comparator without load capacitance.

.

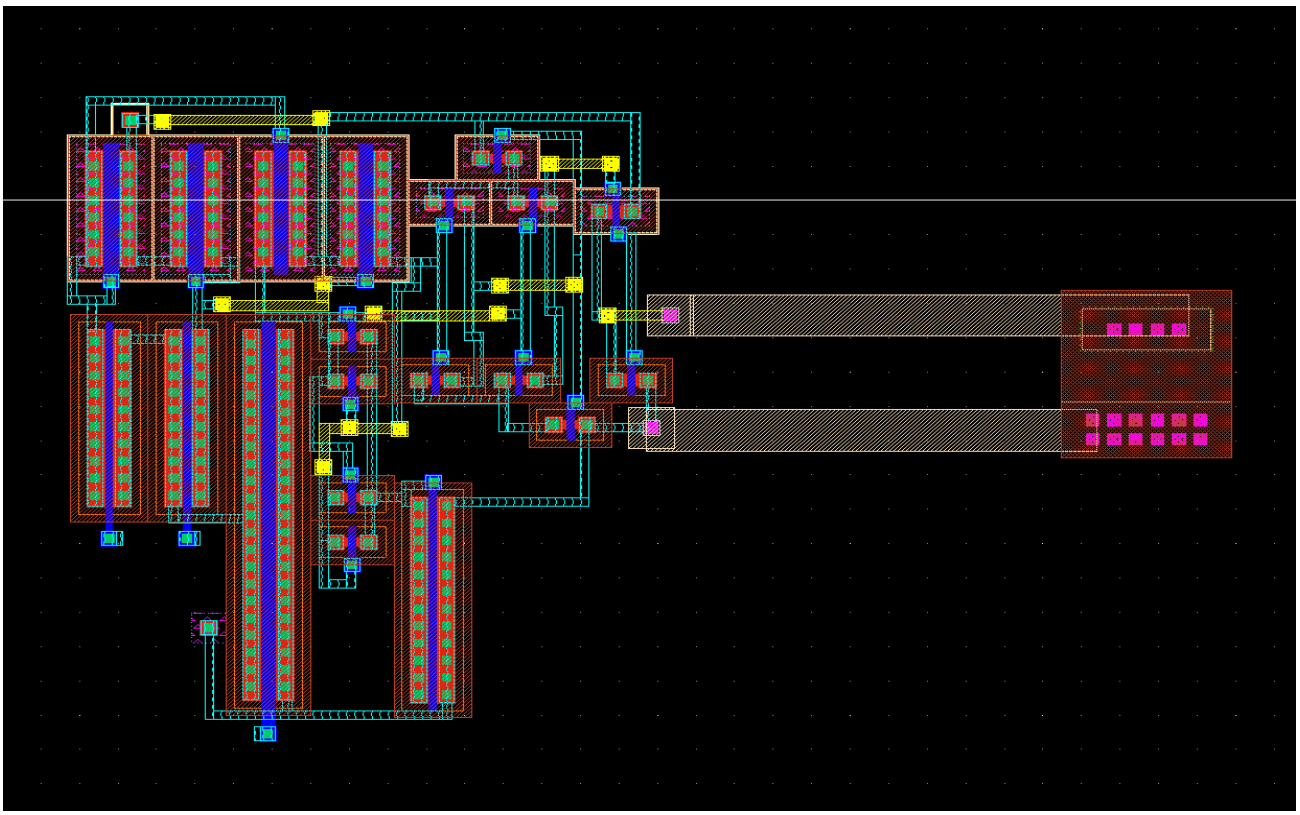


Figure 7.5(a): Layout of the Comparator with load capacitance.

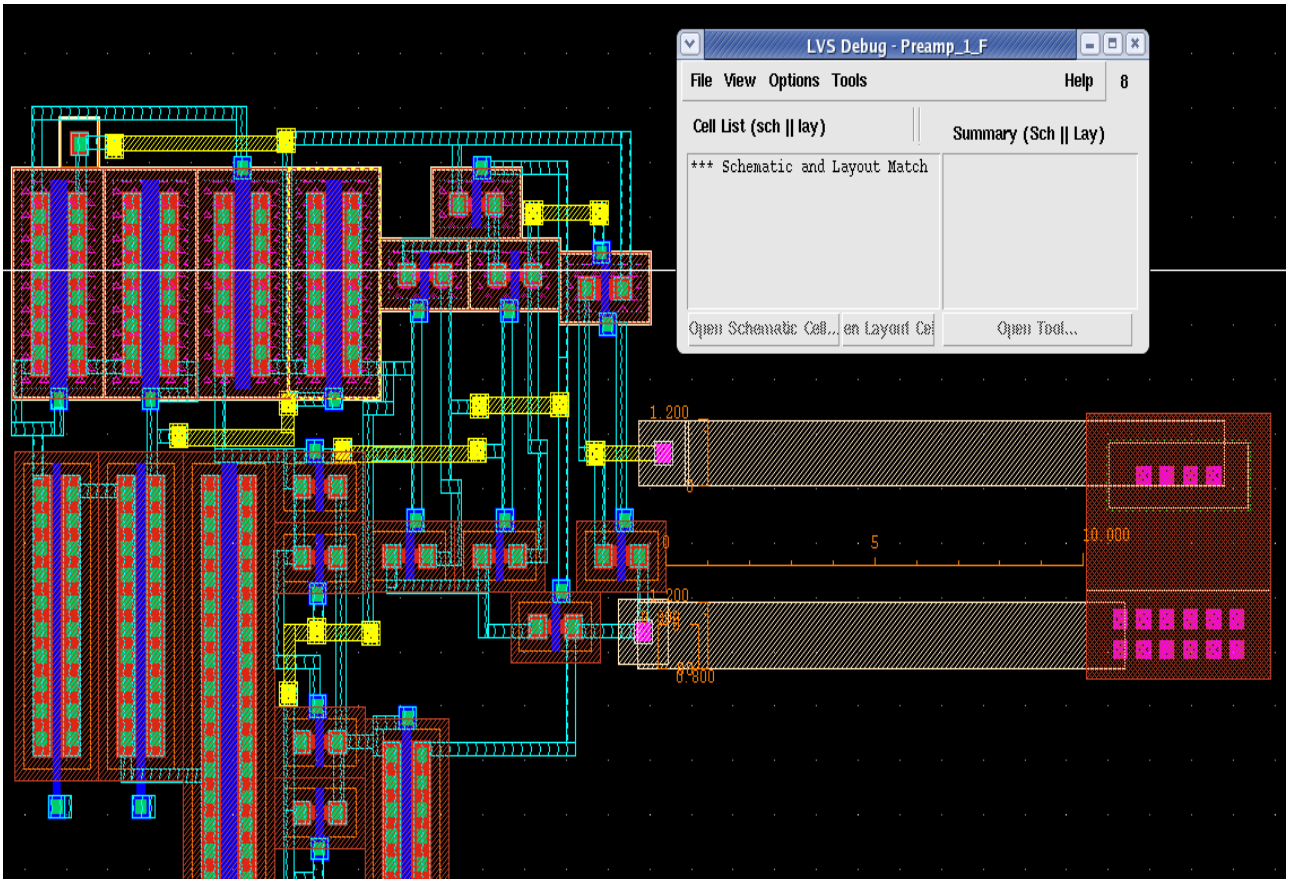


Figure 7.5(b): Layout Vs Schematic match of the Comparator with load capacitance.

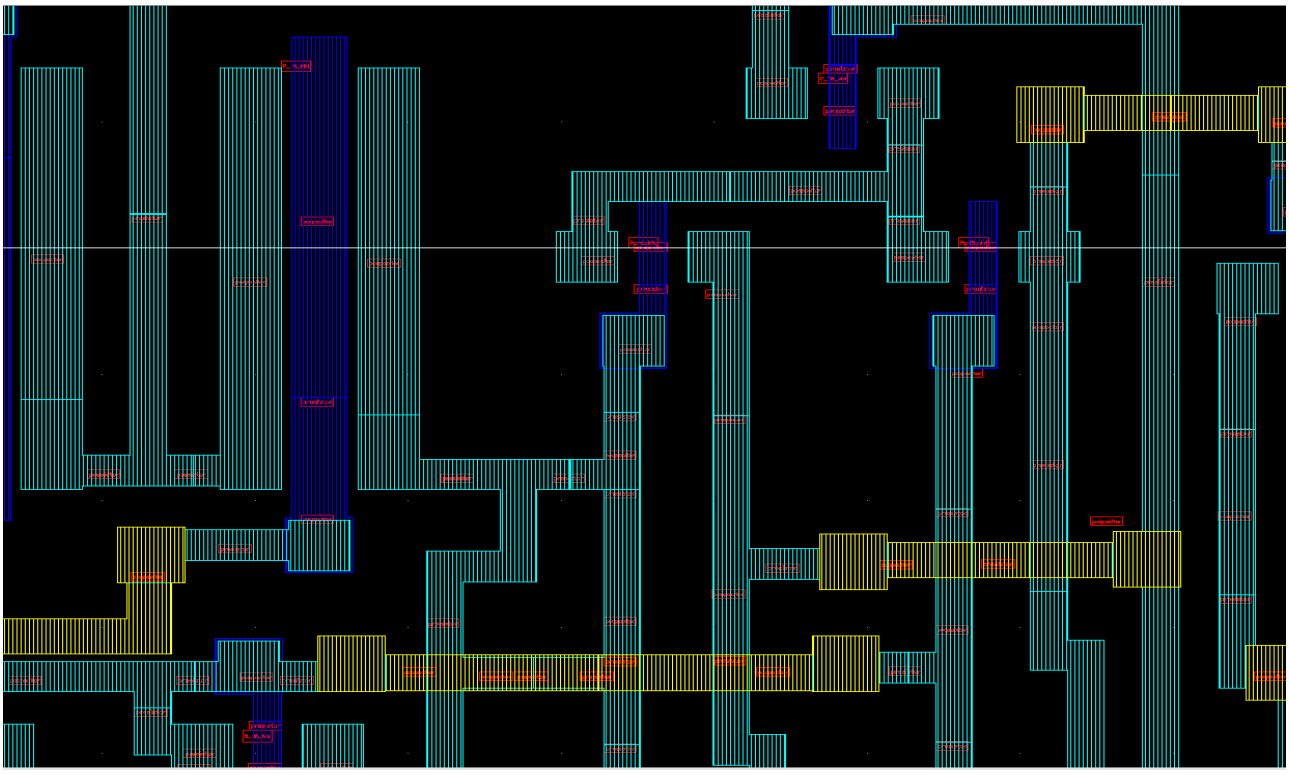


Figure 7.5(c): RCX extracted view of the Comparator with load capacitance.

CHAPTER 8

CONCLUSION AND FUTURE SCOPE

8.1 CONCLUSION

In scaled CMOS technologies, analog circuit design becomes more challenging. For modern nano-scale process technologies, creating high-performance, low power circuits are getting more difficult as the minimum geometries and the supply voltage decreases. One alternate solution to overcome these problems, has been suggested as Comparator-Based Switched-Capacitor circuits (CBSC). This CBSC structure takes advantage of the increased speed, high gain and low power consumption in modern CMOS process technologies without the use of high gain amplifiers.

The role of the comparator is of critical importance to the accuracy of the CBSC circuits. The work of this thesis is to design high-speed, low-offset comparator, for implementing comparator-based switched capacitor circuits using conventional as well as using g_m/I_d technique. A high-performance comparator has been developed using g_m/I_d technique which has propagation delay of 0.643ns, offset voltage of 5mV, resolution of 36mV and power dissipation of 0.223mW. The comparator has been designed and simulated using 180nm CMOS technology process parameters in Cadence® Virtuoso Analog Design Environment to validate its performance. Layout of the comparator has been designed using Cadence® Virtuoso Layout XL Design Environment.

Each of the separate components of the comparator is designed with conventional technique as well as g_m/I_d technique. The results of the g_m/I_d technique are very close to that of the simulation results, as compared to the conventional technique.

8.2 FUTURE SCOPE

Some suggestions and ideas for future work:

- A further optimized design (shorter delay and low offset voltage) of the comparator in the CBSC circuits can improve accuracy.

- Auto-zeroing technique can be used to further reduce the offset voltage in the comparator.
- Design a single ended as well as differential CBSC gain stage.
- Noise, offset and non-linearity analysis of the CBSC circuits.
- Apply the concept of comparator based switched capacitor in an application like switched capacitor filter, integrator in sigma-delta ADC and simulate the circuit.

REFERENCES

1. Charles G. Sodini and Hae-Seung Lee, "Analog-to-Digital Converters: Digitizing the Analog World," in *Proc. IEEE*, Feb. 2008, pp. 323-334.
2. John K. Fiorenza, Todd Sepke, Peter Holloway, Charles G. Sodini, Hae-Seung Lee, "Comparator-Based Switched-Capacitor Circuits for scaled CMOS technologies", *IEEE Journal of Solid State Circuits*, vol. 41, no. 12, pp. 2658 – 2668, Dec 2006.
3. Farhad Alibeygi Paarsan, Ahmad Ayatollahi, "A Comparator-Based Switched-Capacitor Integrator using a new charge control circuit", *IEEE International SOC Conference*, Sept. 2008,pp 139 – 142.
4. Seyed Yahya Mortazavi, Abdolreza Nabavi and Parviz Amiri, "High-accuracy Comparator-Based Switched-Capacitor structure", *IEICE Electronic Express*, vol. 7, no.5, March 10, 2010 .
5. Kim-Fai Wong, Sai-Weng Sin, Seng-Pan U and R.P. Martins, "Level-Shifting Variable Current Charging Technique for High Speed Comparator-Based Switched-Capacitor Circuits" *IEEE International Midwest Symposium on Circuits and Systems* (MWSCAS), Aug. 2010, pp.566-569.
6. Majid Zamani, Massoud Dousti, Mehdi Taghizadeh and Amir Hossein Abdollahi Sai-Weng Sin, Seng-Pan U and R.P, "A Fourth-Order, Low-pass,MASH Modulator with CBSC Technique in 0.18μm CMOS", CCECE 2011 .
7. Majid Zamani, Massoud Dousti and Amir Hossein Abdollahi Nohoji, "A 10-bit ,20-MS/s, Fully Differential Single Transfer Phase CBSC Pipelined ADC in 0.18μm "*International Conference on Electronic Devices, Systems and Applications* (ICEDSA) Aug. 2011, pg. 77-82.
8. R. Gregorian, K. W. Martin, G. C. Temes, "*Switched-Capacitor Circuit Design*", in *Proc. IEEE*, vol. 71, no. 8, pp. 941-966, Aug. 1983.
9. Behzad Razavi, "*Design of Analog CMOS Integrated Circuits*," Tata McGraw-Hill, Inc., 2002.
10. Philip E. Allen and Douglas R. Holberg, "*CMOS Analog Circuit Design*", 2nd Edition, Oxford University Press, 2010.
11. Baker, R. Jacob, "*CMOS circuit design, layout, and simulation*", 2nd Edition, IEEE Press etc., 2005.
12. Marcio Cherem Schneider and Carlos Galup-Montoro, "*CMOS Analog Design using*

All-Region MOSFET Modeling", 1st Edition, Cambridge University Press, 2010.

13. P. Jespers, "*The g_m/I_d Methodology, a sizing tool for low-voltage analog CMOS Circuits"*, Boston, MA: Springer, 2009.
14. B.Murman, *Advanced Analog Integrated Circuit Design*, Stanford University, Winter 2011.https://ccnet.stanford.edu/cgibin/course.cgi?cc=ee214b&action=handout_download&handout_id=ID12930295874606.
15. B.Murman, *Analog Integrated Circuit Design*, Stanford University, autumn 2007/08. http://www.scribd.com/doc/88716494/Stanford-Ee214-Reader.
16. B. Boser, *Analog Circuit Design with Submicron Transistors*, Class Notes, University of California, Berkeley, 2004. http://www.ewh.ieee.org/r6/scv/ssc/May1905.pdf.
17. Bernhard Boser. "Analog Circuit Design with Submicron Transistors". *IEEE SSCS Meeting, Santa Clara Valley*, May 2005. http://www.ewh.ieee.org/r6/scv/ssc/May1905.pdf.
18. F. Cortes and S. Bampi, "Anaysis and Design of Amplifiers and Comparators in CMOS 0.35μm Technology," *Microelectronics Reliability*, vol. 44, no. 4, Sept. 2004.