DESIGN AND ANALYSIS OF A LOW POWER TRI-GATE TRAPEZOIDAL FINFET

Dissertation submitted in partial fulfilment of the requirements

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In

VLSI Design

Submitted by

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July, 2015

CERTIFICATE

I hereby declare that the work which is being presented in the thesis entitled, "**DESIGN AND ANALYSIS OF A LOW POWER TRI-GATE TRAPEZOIDAL FINFET**" in partial fulfilment of the requirement for the award of degree of Master of Technology (VLSI Design) at the electronics and Communication Engineering Department of Thapar University, Patiala, is an authentic record of my own work carried out under the supervision of Mr. Arun Kumar Chatterjee, Assistant Professor, ECED. The matter presented in this dissertation has not been submitted in any other University/Institute for the award of any other degree.

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It is certified that the above statement made by the student is correct to the best of my Knowledge and belief.

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Abstract

In the recent years non-planer tri-gate (TG) field-effect transistors (FETs) such as FinFETs has been considered as the best option for the sub-50 nm regime of MOSFETs due to their better gate control, reduced short channel effects (SCEs), better scalability and improved performance over bulk planar MOSFETs. This dissertation work presents the design and comparison of a Trapezoidal FinFET (Tz-TGFinFETs) and Rectangular FinFET (ReTGFinFET's) using COGENDA GENIUS VISUAL TCAD tool.

Firstly, a ReTGFinFET structure has been studied for different substrate doping concentration. Next, by varying the ReTGFinFET's sidewall inclination angle a trapezoidal FinFET has been obtained. This structure has been studied taking different inclination angles. Various parameters such as threshold voltage, transconductance, drain current, has been calculated and compared with those of rectangular FinFET. It is observed that the trapezoidal FinFET gives better performance and reduced corner effect for an optimum doping concentration as compared to the rectangular FinFET.

Further in multifin FinFET, to show the effect of doping concentration over threshold voltage an analytic expression have been obtained and validated by numerical simulations.

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LIST OF ABBREVIATIONS

MOSFET	Metal oxide semiconductor field effect transistor
CMOS	Complementary Metal oxide semiconductor field effect transistor
NMOSFET	N-channel Metal oxide semiconductor field effect transistor
PMOSFET	P-channel Metal oxide semiconductor field effect transistor
SCE	Short channel effect
DIBL	Drain induced barrier lowering
GIDL	Gate induced drain leakage
SOI	Silicon on insulator
PDSOI	Partially depleted silicon on insulator
FDSOI	Fully depleted silicon on insulator
DGFET	Double gate field effect transistor
ITRS	International technology roadmap for semiconductors
TzFinFET	Trapezoidal FinFET
ReFinFET	Rectangular FinFET
IC	Integrated circuit
EOX	Equivalent oxide thickness
MgFET	Multiple gate field effect transistor

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Chapter 1

Introduction

The origin of modern MOS device is way back in 1959. Silicon metal-oxide-semiconductor field effect transistor (MOSFET) Figure 1.1 is one of the most important devices in the semiconductor industry. Its first practical demonstration was found in 1960 [1]. The MOSFET has been used in monolithic integrated circuits (ICs) over bipolar junction transistors to serve as a basic switching element for digital logic and as an amplifying device for analog applications as well as digital applications because of its several advantages. The size of the MOSFET has been shrunk by many orders of magnitude over the past fifty years. The trend since came to be known as 'Moore's Law' [2]. Figure 1.2 shows a plot of the actual growth versus growth according to Moore's law.

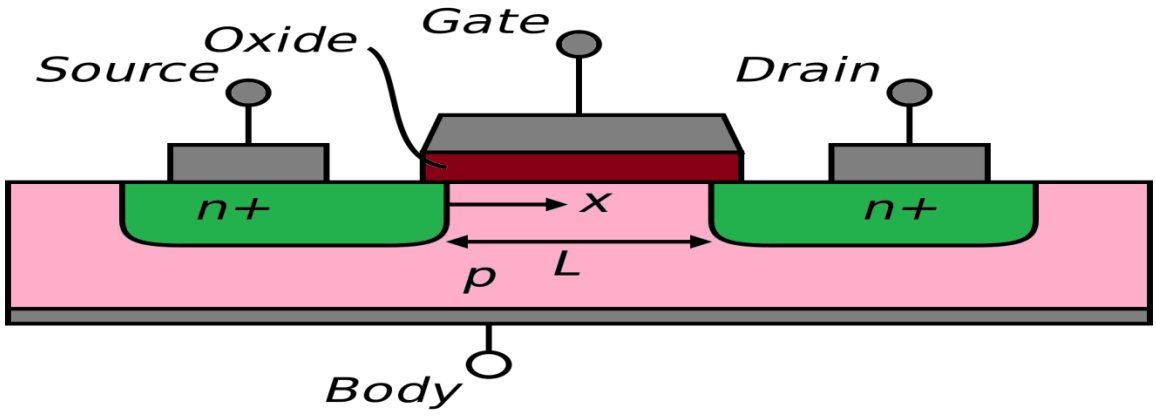


Figure 1.1 Schematic Representations of MosFETs

From Figure 1.2 we can say that the actual growth is always greater than what predicted by Moore's law. So a time came when this law doesn't holds well and we require adapting new technologies. Basically MOSFETs can be classified in to two categories. Enhancement and depletion type MOSFETs. Further N-type and P-type are the subdivision. Commonly used is the N-type enhancement MOSFETs. Figure 1.3 shows the evolution of different processors and increase in the number of transistor counts in them.

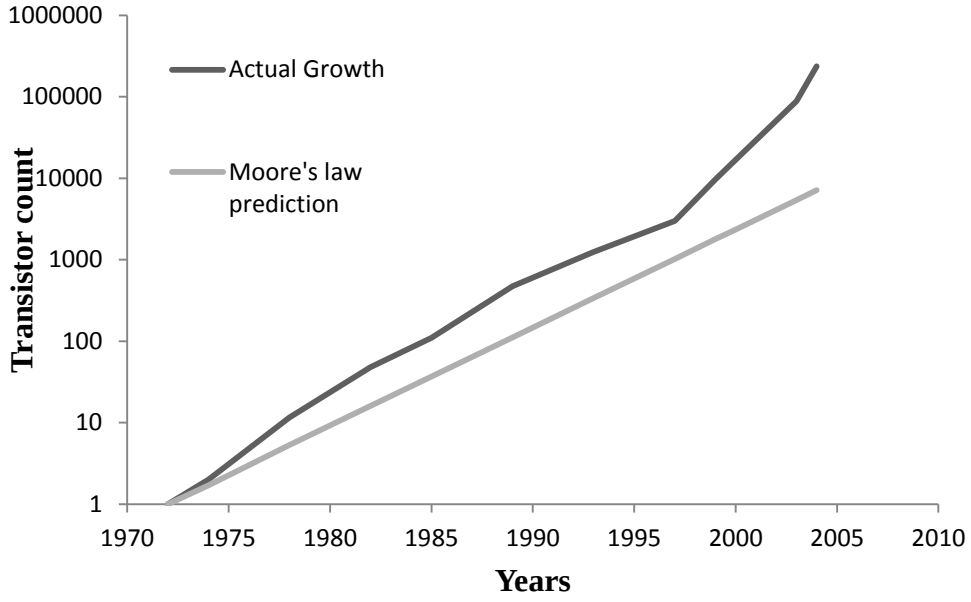


Figure 1.2 Plot for the growth of number of transistors count during past decades as per Moore's law and Actual growth.

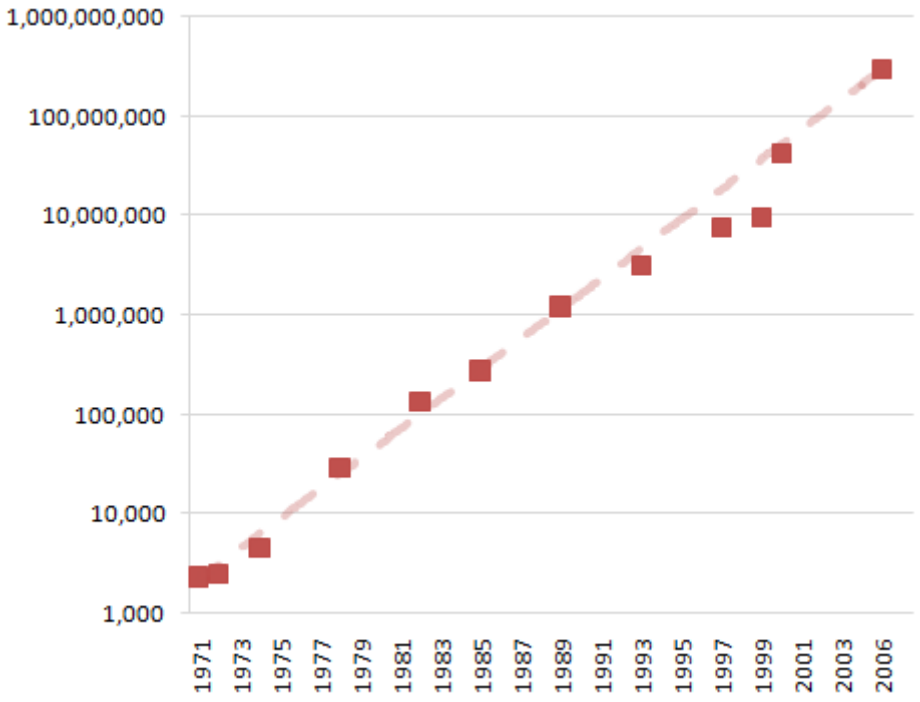


Figure 1.3 Evolution of different processors and IC's

1.1 CHALLENGES IN MOSFET DEVICE SCALING

The scaling of CMOS transistors has finally reached the boundary at size of 22 nm. They frequently cite that CMOS transistors are approaching atomistic and quantum mechanical physical boundaries [3].

Furthermore, the concern is not only about the incompleteness of the devices itself to continue operate steadily but also the impulsion from the economic and technology point of view. Silicon-based microelectronic devices have revolutionized our world in the past five decades. The need for higher computing speed and power at cheaper cost has increased by leaps and bounds in past several years. The Moore's Law holds even 50 years later and it has become more like a self-fulfilling prophecy. But now it reaches to its limits for the conventional MOSFET devices. So the New device structures was required to extend the Moore's law [4]. There are several important factors that could challenge CMOS from being used in future. We can divide these challenges into five different categories as shown below.

- **Physical challenges:** As the device dimension reduces, increment of tunnelling and leakage currents also increases, which impacts the performance and functionality of CMOS devices.
- **Material challenges:** These come from the inability of the dielectric material and wiring materials to provide reliable insulation to device and conduction, respectively with continued scaling.
- **Power-thermal challenges**: As the density of Transistors ever increasing number of transistors integrated per unit-area also increases, which demands for larger power consumption and higher thermal dissipation.
- **Technological challenges:** These are the results from the inability of lithography-based techniques to provide the resolution below the wavelength of the light to manufacture to CMOS devices.
- **Economic challenges**: As the technology enhances the cost of production, fab, and testing that may reach a point where it will be not affordable from economic point of view.

1.2 SHORT CHANNEL EFFECTS IN CONVENTIONAL DEVICES

Figure 1.4 shows the schematic of conventional planar bulk transistor. Traditionally, as the channel length L_g is decreased, the thickness of oxide T_{ox} should also be reduced I proportion to maintain required capacitive coupling between the inversion channel and the gate terminal. This helps us to control the short channel effects (SCEs)[5] such as velocity saturation, threshold voltage roll-off, sub-threshold slope degradation and drain induced barrier lowering (DIBL), which act combined to increase the off-state transistor leakage current. While the scaling of $L_{g,}$ we have to take care of corresponding increase in body doping density N_A and effective decrease in source/drain junction depth X_j. By doing this we can achieve reduction in the leakage path below the inversion channel. This scaling technique has worked very well for several years but in the recent past the conventional CMOS technology is approaching to its physical limits whereby further scaling leads to have a negative impact on the device

performance [6] such that thin gate oxide T_{ox} loses its ideal insulating property and there is significant increase in gate current through direct quantum tunnelling of carriers across the oxide. This results in an increase in the on-state leakage current. With the increase in body doping, it leads to reduction in carrier mobility due to the large vertical electric fields. The large vertical field created at source/drain junction due to the high body doping also leads to large band-to-band tunnelling current which ultimately increase off-state leakage. Increased body doping also leads to larger body and junction capacitances making the transistor switching slower which is not at all acceptable. The random dopant fluctuations are also exacerbated due to the presence of heavy body doping [7]. The reduced junction depths increase the source/drain resistance which reduces the current drive of the transistor. To solve these scaling issues, two different paths can be proposed. The first path involves the introduction of new technologies and new materials into the conventional planar bulk MOSFET technology to allow further scaling of transistors and to boost the performance of scaled transistors. The second path involves adoption of new transistor architectures such as ultra-thin body FETs and multi-gate FETs which inherently have superior electrostatic control over the inversion channel. In order to study the circuit level advamtages and reliability of these two CMOS scaling technological solution, timely understanding and modeling of the associated device physics and device behaviour is required.

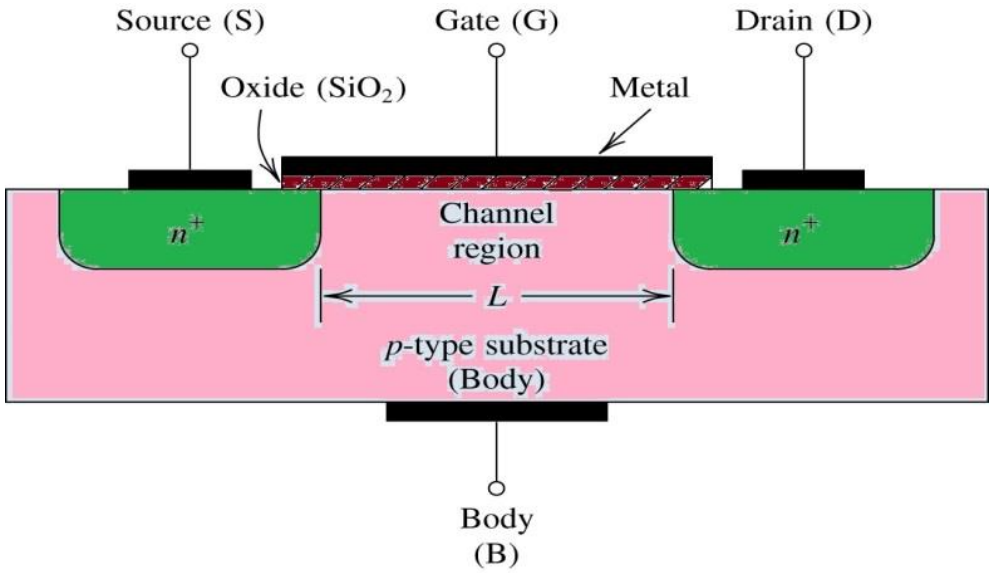


Figure 1.4 Schematic view of conventional MOSFET

1.2.1 SUBTHRESHOLD LEAKAGE

In order to reduce internal electric fields and power consumption in a MOS device, low power supply levels are required by short channel transistors according to scaling rules. To maintenance the

performance, commensurate scaling of the transistor threshold voltage is done. When the gate voltage is below the threshold voltage, sub-threshold or weak inversion current flows between drain and source in a MOS transistor. There is an exponential relation between gate voltage and the drain current. On a semi-log plot of Id versus Vg, this relation gives a straight line.

1.2.2 DRAIN INDUCED BARRIER LOWERING

This occurs when the source and drain depletion regions interact with each other andlower the source potential barrier near the channel surface. Carriers are then injected into the channel surface by the source. DIBL[8] becomes more severe at shorter channel lengths and high drain voltages. DIBL can be reduced by higher surface and channel doping and shallow source/drain junction depths. The higher doping reduces the depletion widths of source and drain and prevents them from interacting with each other.

1.2.3 PUNCHTHROUGH

Extremely low substrate doping results in even larger depletion depths and an increase in the penetration of drain electric field through the channel to the source, thus, making the DIBL effect stronger. As a result, barrier to the carriers decreases and more and more carriers enter the channel leading to a drastic increase in the current. The current is so high that it becomes impossible to turn off the device. Punch through is of two types:

- **SURFACE PUNCHTHROGH**: In this the current flows through the surface.
- **BULK PUNCHTHROUGH**: In this the current follows the subsurface path.

1.2.4 HOT CARRIER INJECTON INTO THE GATE OXIDE

In a short channel transistor, the electric field is very high near the Si- Sio2interface, due to which electrons or holes can gain sufficient energy and enter into the oxide layer by crossing the interface potential barrier. This effect is called hot-carrier injection. The probability of the injection from Si to is more for electrons than holes, as the effective mass of electrons is lower than that of holes, and the barrier height for holes (4.5eV) is more than that for electrons (3.1eV).

1.3 ADVANCED PLANAR BULK MOSFETS STRUCTURES

Even though planar bulk MOSFET technology is reached to its physical limits of scaling, new technologies have been introduced. Researchers worldwide are trying to extend bulk MOSFET scaling

through introduction of new materials and technologies. In order to reduce the problem gate leakage with decreasing oxide thickness (Sub-micron regime), high-k insulators are being introduced into the gate stack [9]. Benefits from the high-k gate dielectric are the dielectric constant is higher than that of silicon dioxide and thus it can generate a larger gate capacitance even with a physical thickness larger than that of silicon dioxide. The larger physical thickness suppresses direct tunnelling of carriers through the gate dielectric reducing the gate current by several orders of magnitude. Figure 1.5 shows the evolution of the different structures through the past several years.

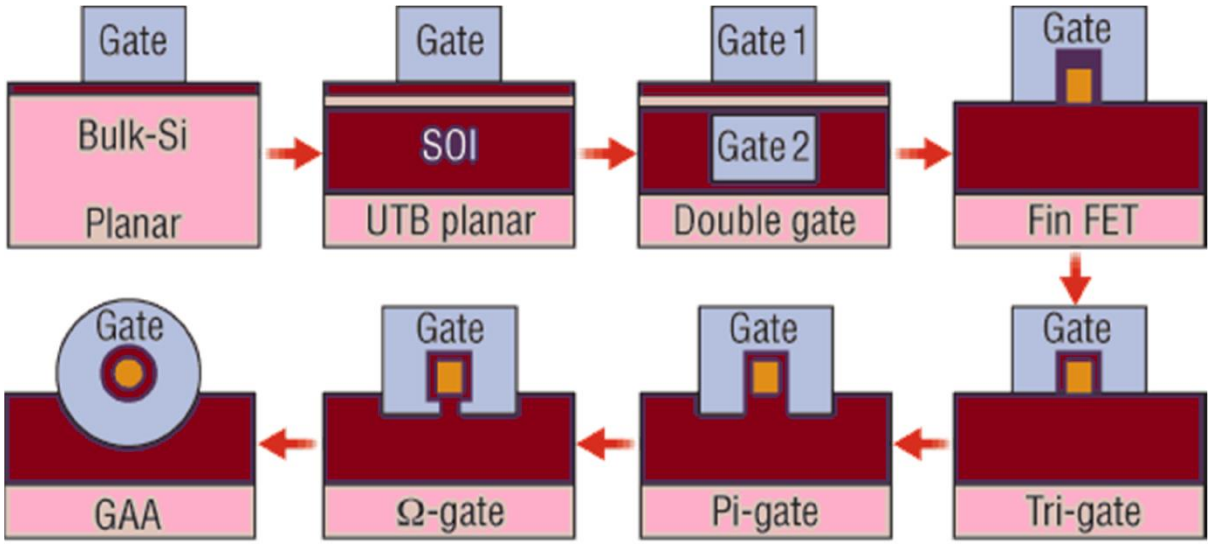


Figure1. 5 Evolution of different structures for MOSFETs

1.3.1 SILICON ON INSULATOR TECHNOLOGY

With Silicon-On-Insulator(SOI) [10] transistors are formed in thin layers of silicon that are mot connected to the main substrate of the wafer and insulated by a layer of electrical insulator, usually silicon dioxide. The thickness of silicon layer ranges from several microns to few nanometres for high-performance devices. The idea of Isolating the active transistor from the rest of the silicon substrate reduces the electrical current leakage. Since the area of electrically active silicon is limited to the immediate region around the transistor,

A fully depleted SOI MOSFET has a thinner top silicon layer, so the channel is completely depleted of the majority carriers. Hence, the SOI layer is much smaller than the depletion width of the device and its potential is tightly controlled by the gate. That means that there is no neutral region of the body of the MOSFET that can be charged. The advantage of FD SOI [11] MOSFET includes the elimination of the floating-body effect and better short channel behaviour. For Partially Depleted SOI device Figure 1.6 the SOI layer thickness is thicker than the maximum depletion width of the gate. Usually the silicon

film thickness is more than 50nm, which mitigate the constraint on device threshold voltage and its sensitivity. Also PD SOI devices make the manufacturing easier and the process and device design are much more compatible than with traditional bulk CMOS. In general, PD SOI device is optimal for high speed and is being targeted for applications where highest clock rates are needed. The major issue of the partially depleted device is the floating body effect [12].

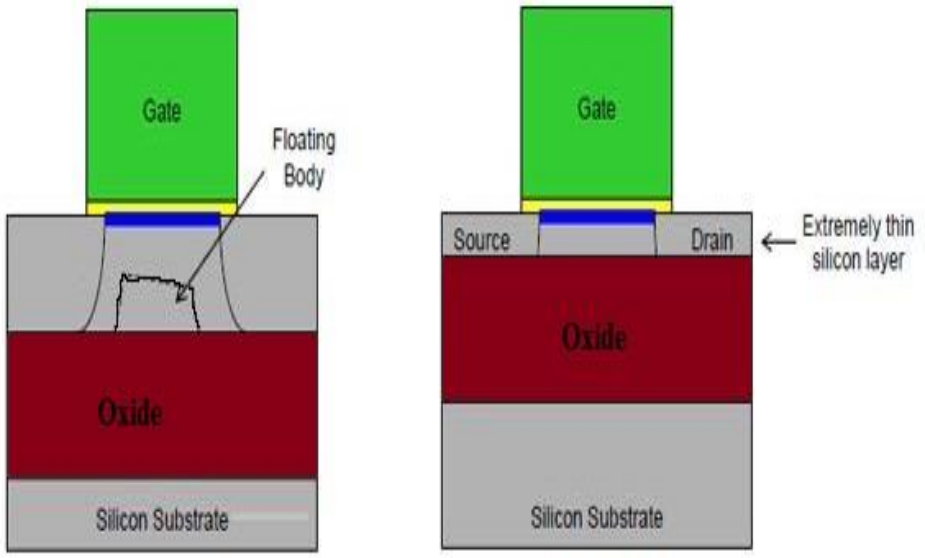


Figure 1.6 Partially depleted and fully depleted Structures

1.3.2 MULTI-GATE FETS

A promising alternative to extend CMOS scaling beyond 32nm node is the introduction of a new FET architecture, the Multi-gate (MG) FET [13]. MG-FETs can be thought of as an extension to the ultra-thin body FETs or the fully-depleted SOI FETs but with more gates around the thin silicon body. MG-FETs offer stronger electrostatic control of the inversion channel through the use of multiple gates. This method reduces the detrimental short channel effects (SCEs) and makes the MG-FETs more scalable than the planar bulk CMOS. Double gate, triple gate structures are at the top of the electronic industry.
One of the most feasible multi-gate configurations in terms of being manufacturable is the FinFET. Figure 1.7 and Figure 1.8 shows the FinFET structure where the gate controls the channel along the silicon sidewalls of the fin. In the Figure 1.7 the double gate is shown which covers the inversion channel from the two sides and triple gate structure which cover the gate from all three sides is shown in Figure 1.8.

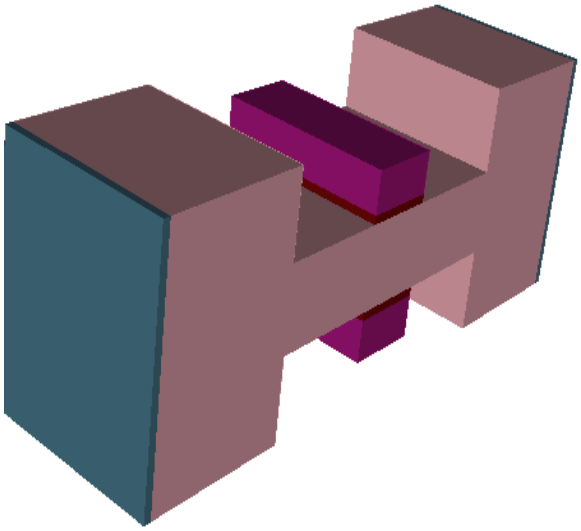


Figure 1.7 Schematic of Double-gate MosFET

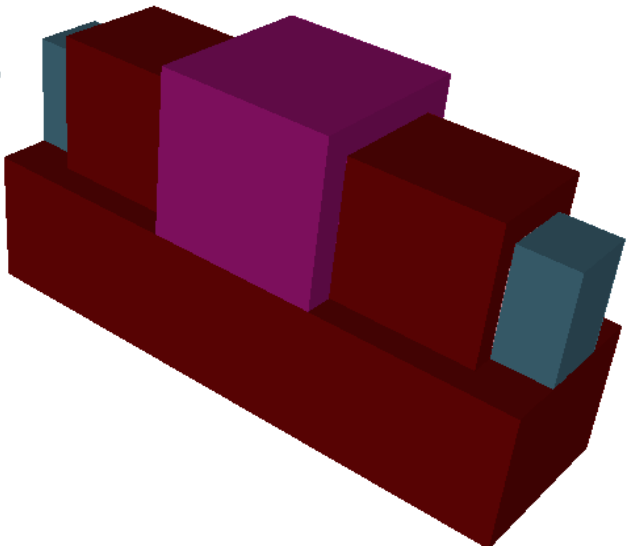


Figure 1.8 Schematic of tri gate rectangular FinFET

1.3.3 NANOWIRE FINFETS

The basic problems of nano MOSFETs beyond sub-10nm channel length are the electrostatic limits, source-to-drain tunnelling, carrier mobility degradation, process variations, and static leakage. The trend toward nano gate length structure MOSFETs requires a more and more effective control of the channel. It appears that non-classical device architectures can extend the CMOS lifetime and provide solutions to continue scaling. In case of silicon-based CMOS technologies, planar MOSFETs are limited to scaling beyond 15 nm technology node as further scaling gives negative impacts. As simple scaling of silicon CMOS becomes increasingly complex and expensive, there is considerable interest of increasing performance by the use of strained channels which can improve carrier mobility and drive current in a device. Multi-gate MOSFETs based on the concept of volume inversion are widely recognized as one of the most effective solutions for short channel effects. Also rectangular or cylindrical nanowire MOSFETs has been proposed in the literature as a useful structure for SCEs reduction. The nanowire (NW) transistors [14] can be seen as the ultimate integration of the innovative nano devices and is one of the candidates which have gained significant attention from both the device and circuit developers because of its potential for building highly dense and high performance electronic circuits. Figure 1.9 shows the 3-D view of nano wire and Figure 1.10 shows the cross sectional view of the nanowire.

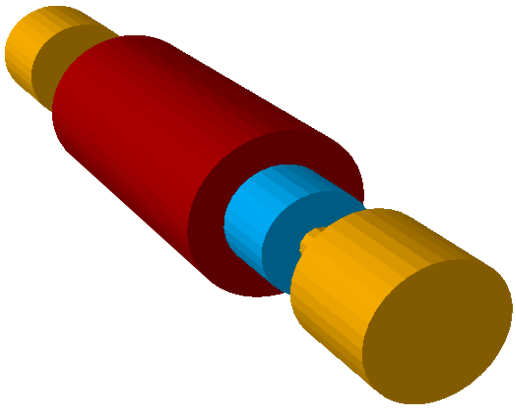


Figure 1. 9 3D view of nano-wire FinFET

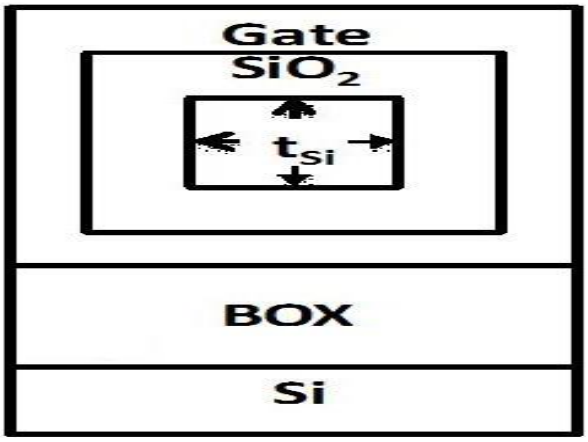


Figure 1.10 cross sectional view of nano -wire

1.4 THESIS ORGANIZATION

This thesis comprises of five chapters out of which the first chapter is introduction. A brief description of work done by various researchers throughout the world has been given in second chapter under the heading of LITERATURE SURVEY. The third chapter includes the basic concepts related to FinFET and its advance structures. The fourth chapter includes the impact of inclined walls of trapezoidal FinFET on various electrostatic parameters like drain current, mobility and so on. In fifth chapter TCAD simulation analysis and comparison between tri-gate rectangular and trapezoidal FinFET is done and all the results are shown. Finally, the sixth chapter gives the conclusion and future scope..

Methodology used for the work is explained by the below flow chart.

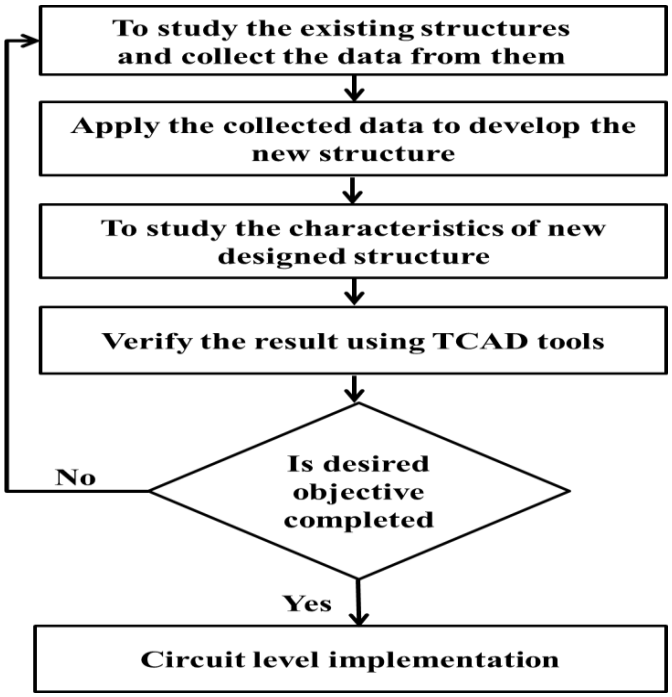


Figure 1.11 Methodology used for the research work

Chapter 2
Literature Survey

Gordon E. Moore, in 1998 [14] concentrated on the scaling of the device. Statement made under this "With unit cost falling as the number of components per circuit rises, by 1975 economics may dictate squeezing as many as 65 000 components on a single silicon chip". By integrated electronics, He suggested that all the various technologies which are referred to as microelectronics today as well as any additional ones that result in electronics functions supplied to the user as irreducible units. These technologies were first investigated in the late 1950's. The article was to scale down device hardware to incorporate progressively complex electronic capacities in constrained space with least weight. A few methodologies advanced, including smaller scale gathering methods for individual parts, dainty film structures, and semiconductor integrated circuits.

Kaushik Roy et al. , in 2003 [15] suggested focus on constant scaling of channel length, gate oxide thickness, and limit voltage in the profound sub-micrometer regime prompts high spillage current which is turning into a genuine concern in light of the powerful scattering it prompts. Consequently, it is necessary to identify different leakage components and to carefully model them so as to reduce the leakage power. This paper reviews the different transistor intrinsic leakage mechanisms, including sub-threshold leakage, drain-induced barrier lowering, punch through, gate induced drain leakage, hot carrier injection into the oxide, and gate oxide tunnelling. The paper also discusses channel engineering techniques including halo doping and retrograde doping as a means to ameliorate the short-channel effects for continuous scaling down of CMOS devices. Finally, the paper explains various circuit-level techniques to reduce leakage power.

Vishwas Jaju et al. , in 2004 [16] explained the issues related to silicon-on-insulator technology. SOI technology gives a good alternative to bulk CMOS processes which are reaching their limits in terms of device miniaturization and fabrication. Different types of SOI MOSFETs have been presented and the related physical concepts have been evaluated. The advantages of SOI MOSFETs have been discussed with the stress on Double Gate MOSFETs. The technological challenges in realizing this new device structure have also been presented. Double Gate MOSFETs provide excellent short channel effect immunityand exhibit a near ideal sub-threshold slope which make them the ultimate scalable device

structure. Different structures such as Thin Body FD SOI with raised source and drain, Halo Doped SOI MOSFET, Ground Plane FDSOI MOSFET, Multiple Gate SOI MOSFET have also been discussed.

Anurag Chaudhry and M. Jagadesh Kumar, in 2004 [17] examined the performance degradation of a MOS device fabricated on silicon-on-insulator (SOI) due to the undesirable short-channel effects (SCE) as the channel length is scaled to meet the increasing demand for high-speed high-performing ULSI applications. The study assesses late recommendation to dodge the SCE in SOI MOSFETs and a short assessment of qualities and shortcomings particular to every endeavor is introduced. Another device structure called the double material entryway (DMG) SOI MOSFET is talked about and its adequacy in smothering SCEs, for example, channel actuated hindrance bringing down (DIBL), channel length tweak and hot-transporter impacts, all of which influence the unwavering quality of ultra-little geometry MOSFETs, is surveyed.

Qian Xie et al. , in 2013 [18] analysed the 2-D short-channel effect in ultrathin SOI MOSFETs. An empirical, channel length dependent scale length is extracted from the lateral field slope of a series of numerically simulated devices. We show how this scale length is related to the short-channel threshold voltage roll-off and minimum channel length with and without a substrate bias. The advantage of a converse substrate predisposition is explored and saw as far as the field and dispersion of reversal charge in the silicon film. Specifically, how a mass like short channel impact is accomplished when a gathering layer is framed at the back surface. Besides, the impact of a high-κ door separator is considered and scaling ramifications talked about

M. Zakir Hossain et al. , in 2011 [19] studied that FinFET devices are comprehensively investigated owing to the projection for application in the CMOS integrated circuits fabrication. Deducing MOSFET size have great influence on electrostatic characteristic. The indiscriminate variations of the characteristics lead to a divergence effect which is imperative from the point of view of design and manufacture. We have considered just n-channel device. The practices of hole m0bility of multigate gadgets is obviously of extraordinary significance. Electron mobility of n-channel FinFET has reenacted regarding viable electric field. Mobility degradation has been seen with more thinner silicon film, at higher electric field, which can be ascribed to "volume inversion" in FinFET. In this paper, distinctive sorts of electrical attributes have been reenacted for diverse working areas and distinctive channel lengths furthermore for diverse oxide thickness. The considerations are illustrated with measurement

data of a series of devices and with distributions of the parameters extracted from these data. The analytical expressions in this work can be useful tool in device design and optimization.

Meng-Hsueh Chiang et.al in 2006 [20] showed the dependence of the threshold voltage (*V*T) on channel doping for extremely scaled devices is investigated. This work is focused on the fundamental *V*T issue and its physical insight into the impact of the doping density on device characteristics. We find that the threshold voltage is, in fact, insensitive to doping over a wide range of doping density and such insensitivity is further extended by band gap narrowing in nano-scale MOSFETs via analytical analyses and two-dimensional numerical device simulations (2003 *Taurus-MEDICI User Guide* (Mountain View, CA:Synopsis Inc.)). This result particularly suggests the scalability and feasibility of nano-scale double-gate MOSFETs.

Pankaj kumar pal et.al in 2014 [21] proposed a general change in performance of Gate-Source/Drain underlap FinFET structure by presenting the idea of double k spacer in the middle of gate and source. By improving the underlap length, He showed the affectability of double k spacer width. in width of high-k shows an observable upgrades in On-Off current proportion (Ion/Ioff). The proposed structure is confirmed by TCAD simulations of underlap FinFET device with vary deceiving physical parameters such as spacer width, spacer material and so forth and improves the width of the high-k and low-k spacer. The proposed device construction modeling upgrades gate control over channel and can be utilized to design low power advanced circuits.

R T Bhleret et al. , in2009 [22] showed trapezium is often a better approximation for the FinFET cross-section shape, rather than the design-intended rectangle. The frequent width variations along the vertical direction, caused by the etching process that is used for fin definition, may imply in inclined side walls and the inclination angles can vary in a significant range. These geometric variations may cause some important changes in the device electrical characteristics. This work analyzes the influence of the FinFET sidewall inclination angle on some relevant parameters for analog design, such as threshold voltage, output conductance, transconductance, intrinsic voltage gain(*AV*), gate capacitance and unit-gain frequency, through 3D numeric simulation. The intrinsic gain is affected by alterations in transconductance and output conductance. The results showthat both parameters depend on the shape, but in different ways. Transconductance depends mainly on the sidewall inclination angle and the fixed average fin width, whereas the output conductance depends mainly on the average fin width and is weakly dependent on the side wall inclination angle. The simulation results also show that higher

voltage gains are obtained for smaller average fin widths with inclination angles that correspond to inverted trapeziums, i.e. For shapes where the channel width is larger at the top than at the transistor base because of the higher attained transconductance. When the channel top is thinner than the base, the transconductance degradation affects the intrinsic voltage gain. The total gate capacitances also present behaviour dependent on the sidewall angle, with higher values for inverted trapezium shapes and, as a consequence, lower unit-gain frequencies.

Xixiang Feng et al., in 2014 [23] clarified around a semi two-dimensional investigative model for trapezoidal fin field-impact transistors (FinFETs) with non-uniform doping profiles is created. The annoyance technique, joined with a variable change strategy, is connected to settle the nonlinear Poisson's equations analytically. Our approach lumps the depletion and inversion terms together to capture the effects of nonlinear coupling and spatial variation of an arbitrary doping profile. Trapezoidal boundary conditions are reformulated accordingly and a continuous analytic current–voltage (I–V) model for doped trapezoidal FinFETs is derived. More accurate prediction of the surface potential and the I–V characteristics is achieved by setting the operating point of a Taylor expansion at the channel surface and introducing the higher-order correction. The short-channel effect is also studied and verified with technology computer-aided design (TCAD) simulations, which indicates a high accuracy of this new model.

Nikolaos Fasarakis et al. in 2014 [24] proposed an analytical compact model for the drain current of undoped or lightly doped nanoscale FinFETs with trapezoidal cross section. The compact model of rectangular FinFETs is extended to trapezoidal FinFETs using equivalent nonplanar device parameters and corner effects. The model has been validated by comparing the results with those of 3-D numerical device simulations. The very good accuracy of the drain current and transcapacitances makes the proposed model suitable for implementation in circuit simulation tools.

Hyohyun Nam in 2014 [25] investigated the impact of the current flow shape in both rectangular and tapered FinFETs on threshold voltage variation induced by work-function variation depending on the real fin shape in a FinFET(i.e., rectangular versus tapered fin), by performing extensive 3-D TCAD simulations. It is found that if a FinFET has two independent (versus single and bulky) current flow in the channel, the extended gate area should be(should not be) included in calculating the ratio of average grain size to gate area (RGG) to agree with a previously validated FinFET RGG plot. Depending on the current flow shape in a FinFET, the RGG calculation should be refined.

N. Fasarakis in 2011 [26] proposed, an analytical compact model for the threshold voltage Vt of double-gate (DG) and tri-gate (TG) FinFETs. The DG FinFET V_t model is extended to TG FinFET V_t model using effective parameters capturing the electrostatic control of the top gate over the short-channel effects. The results of the model are compared with the results of a numerical device simulator for a wide range of the channel length, the fin height and the fin width. The overall results reveal the very good accuracy of the proposed model. The V_t model has been validated by developing a Verilog-A code and comparing the results derived by the Spectre simulator and the Verilog-A code with simulation results.

Tamara Rudenko et al. 2008 [27] discussed the experimental study of the effective mobility in the long-channel undoped triple-gate FinFETs. The mobility behaviour in FinFETs is studied as compared with that in quasi-planar very wide fin FETs made on the same wafers and as a function of the fin width. Devices with two types of the gate dielectrics are investigated. New bits of knowledge about the bearer transport in triple-entryway FinFETs are acquired utilizing a watchful examination of the outcomes for different balance widths. Specifically, it is demonstrated that the model treating the triple-door FinFET as far as the (100) top and (110) sidelong channels is not superbly exact for portraying the vehicle properties in genuine FinFETs with moderately limited balances; at low and moderate inversion charge densities, this is due to different inversion carrier distributions (and, thus, non-identical scattering rates for various fin widths), and at high charge densities, it is presumably due to fin rounding which results in ambiguous crystallographic orientation, different from the postulated (100) and (110).

Andreas Tsormpatzoglou et.al in 2008 [28] derived a simple analytical expression of the 3-D potential distribution along the channel of lightly doped silicon trigate MOSFETs in weak inversion, based on a perimeter weighted approach of symmetric and asymmetric double-gate MOSFETs. The analytical solution is compared with the numerical solution of the 3-D Poisson's equation in the cases where the ratios of channel length/silicon thickness and channel length/channel width are ≥ 2. Good agreement is achieved at different positions within the channel. The perimeter-weighted approach fails at the corner regions of the silicon body; however, by using corner rounding and undoped channel to avoid corner effects in simulations, the agreement between model and simulation results is improved. By using the extra potential induced in the silicon film due to short-channel effects, the subthreshold drain current is determined in a semi analytical way, from which the subthreshold slope, the drain-induced barrier lowering, and the threshold voltage are extracted.

Vaidy Subramanian et al. in 2006 [29] has compared the digital and analog figures-of-merit of FinFETs and planar bulk MOSFETs and found that FinFETs possess the following key advantages over bulk MOSFETs: reduced leakage, excellent sub-threshold slope, and better voltage gain without degradation of noise or linearity. This makes them appealing for advanced and low-recurrence RF applications around 5 GHz, where the execution force exchange off is essential. Then again, in high-recurrence applications, planar mass MOSFETs is seen to hold the favorable position over FinFETs because of their higher crest transconductance. However, this comes at a cost of a reduced voltage gain of bulk MOSFETs.

Yawei Jin et al. in 2007 [30] evaluated the dynamics of the threshold voltage calculation for the tri-gate architecture of device. The 3-D poison's equation with eight boundary conditions is solved analytically and an analytical threshold model for tri-gate Si MOSFET device is developed. TCAD simulation result of the same device structure is also presented and it agrees well with our threshold analytical model. Furthermore, this analytical threshold model is capable of doing rudimentary first order comparisons of the threshold voltage with respect to device dimensions and semiconductor material type.

Debajit Bhattacharya and Niraj K. Jha in 2014 [38] has discussed the challenges in the nanometer regime, FinFETs and Trigate FETs. Attributable to the vicinity of various (two/three) gates, FinFETs/Trigate FETs have the capacity to handle short-channel impacts (SCEs) better than routine planar MOSFETs at profoundly scaled technological nodes and consequently empower proceeded with transistor scaling. In this paper, we explore on FinFETs from the bottommost device level to the highest building design level. We review distinctive sorts of FinFETs, different conceivable FinFET asymmetries and their effect, and novel rationale level and building design level trade-offs offered by FinFETs. We also review analysis and optimization tools that are available for characterizing FinFET devices, circuits, and architectures.

Xinghai Tang, Vivek K. De. and James D. Meindl in 1997 [39] examined the intrinsic fluctuations in threshold voltage, subthreshold swing, saturation drain current and subthreshold leakage of ultra-small-geometry MOSFET's due to random placement of dopant atoms in the channel using novel physical models and a Monte Carlo simulator. In particular, using the device technology and the level of integration projections of the National Technology Roadmap for Semiconductors for the next 15 years,

standard and maximum deviations of threshold voltage, drive current, subthreshold swing and subthreshold leakage are shown to escalate to 40 and 600 mV, 10 and 100%, 2 and 20 mV/dec, and 10 and 10^8%, respectively, in the 0.07 m, 0.9 V complementary metal oxide-semiconductor (CMOS) technology generation with 1.3–64 billion transistors on a chip in 2010. While these deviations can be reduced to some degree by selecting optimal values of channel width, the associated penalties in dynamic and static power and in packing density demand improved MOSFET structures aimed at minimizing parameter deviations.

Chapter3
Basic Concepts of FinFETs

3.1 FinFET

As the devices are scaled down, planar transistors have brought several detrimental effects such as gate oxide tunnelling, increment of leakage currents and enhancement of Short-Channel-Effects. Several independent studies conducted over the past decade which has suggested various devices architectures that offers better solution for short channel effects and allow transistors to shrink below sub100 nm regime. Double-gate MOSFET is becoming an intense subject of VLSI research because in theory, it can be scaled to the shortest channel length possible for a given gate oxide thickness.But the difficulty in fabrication of DG MOSFET(Double gate MOSFET) is encountered due to the misalignment of top gate and the back gate. Hence to eliminate the misalignment of gates in DG MOSFET, FinFET considered one of the most promising candidates for future generation transistor technologies due to their excellent electrostatic integrity such as Low leakage current, improved short-channel effect, high performance resulting from the undoped channel structure, high carrier mobility and reduction of random dopant fluctuation. The structure for FinFET is shown in the Figure 3.1. With the scaling of the devices, the fins needed to be thinner due to which scattering of dopants increases. Hence, lightly doped fins are preferred to reduce the scattering or random dopant fluctuations [7][39].

In the recent study by the Intel, it is shown that tri-gate transistors are in fact trapezoidal as shown in Figure 3.2l and almost triangular in cross-section. It was not clear by that time whether the non-vertical sides to the fins were a non-critical manufacturing aftermath or deliberately engineered by Intel, What were its impact on electron mobility or other device parameters. There was a lot of speculation about the possible advantages and disadvantages of the trapezoidal shaped FinFET such as corner effect, threshold voltage, mobility and so on.

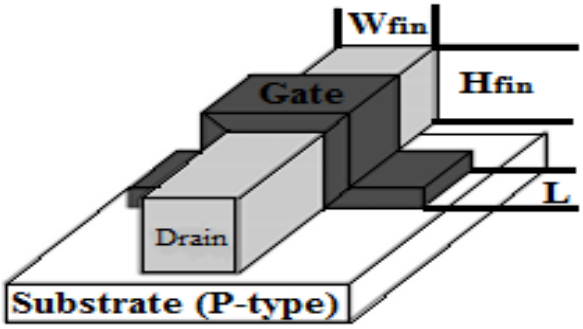


Figure 3.1 Schematic of Rectangular FinFET

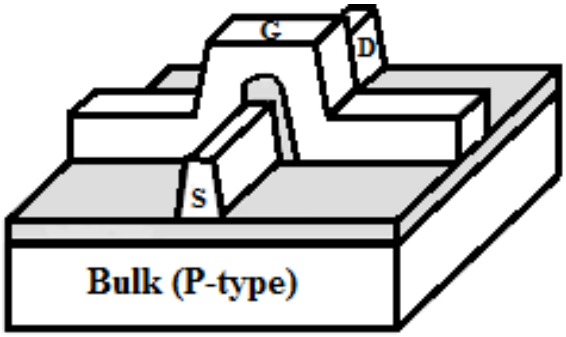


Figure3.2 Schematic of Trapezoidal FinFET

3.2 Types of FinFETs

Modern FinFETs are 3D structures that rise above the planar substrate, giving them more volume than a planar gate for the same planar area. Given the excellent control of the conducting channel by the gate, which "wraps" around the channel [31], very little current is allowed to leak through the body when the device is in the off state. This allows the use of lower threshold voltages, which results in optimal switching speeds and power

The different ways in which the gate electrode can be wrapped around the channel region of a transistor are shown in the Figure 3.3. All the structure has its own advantages.

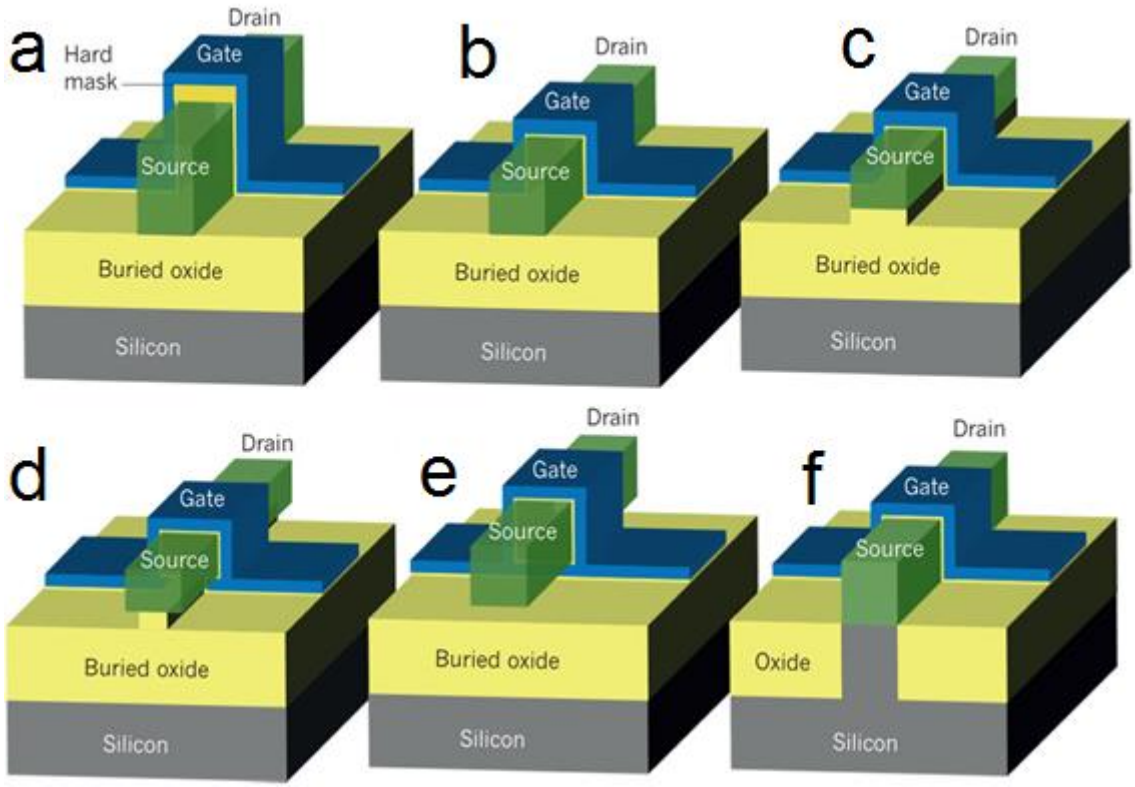


Figure 3.3 Different structures of tri gate FinFET from a to f different configuration of gate wraping around the channel

In the above Figure:

a, A silicon-on-insulator (SOI) fin field-effect transistor (FinFET). The 'hard mask' is a thick dielectric that prevents the formation of an inversion channel at the top of the silicon 'fin'. Gate control is exerted on the channel from the lateral sides of the device

b, SOI triple-gate (or tri-gate) MOSFET. Gate control is exerted on the channel from three sides of the device (the top, as well as the left and right sides).

c, SOI Π-gate MOSFET. Gate control is improved over the tri-gate MOSFET shown in b because the electric field from the lateral sides of the gate exerts some control on the bottom side of the channel.

d, SOI Ω-gate MOSFET. Gate control of the bottom of the channel region is better than in the SOI Π-gate MOSFET. The names Π gate and Ω gate reflect the shape of the gates.

e, SOI gate-all-around MOSFET. Gate control is exerted on the channel from all four sides of the device.

f, A bulk tri-gate MOSFET. Gate control is exerted on the channel from three sides of the device (the top, the left and the right). In this case, there is no buried oxide underneath the device.

3.3 FABRICATION STEPS OF FINFETS

FinFETs broadly can be classified into two types: SOI and Bulk-Si FinFETs. Due to the presence of buried oxide, SOI FinFETs have many advantages, such as easier realization, lower leakage current, higher speed. Compared with SOI FinFETs, Bulk-Si FinFETs possess advantages of low cost, low defect density, no floating-body effect, and good heat dissipation. The fabrication steps of FinFET are shown below in Figure 3.4.

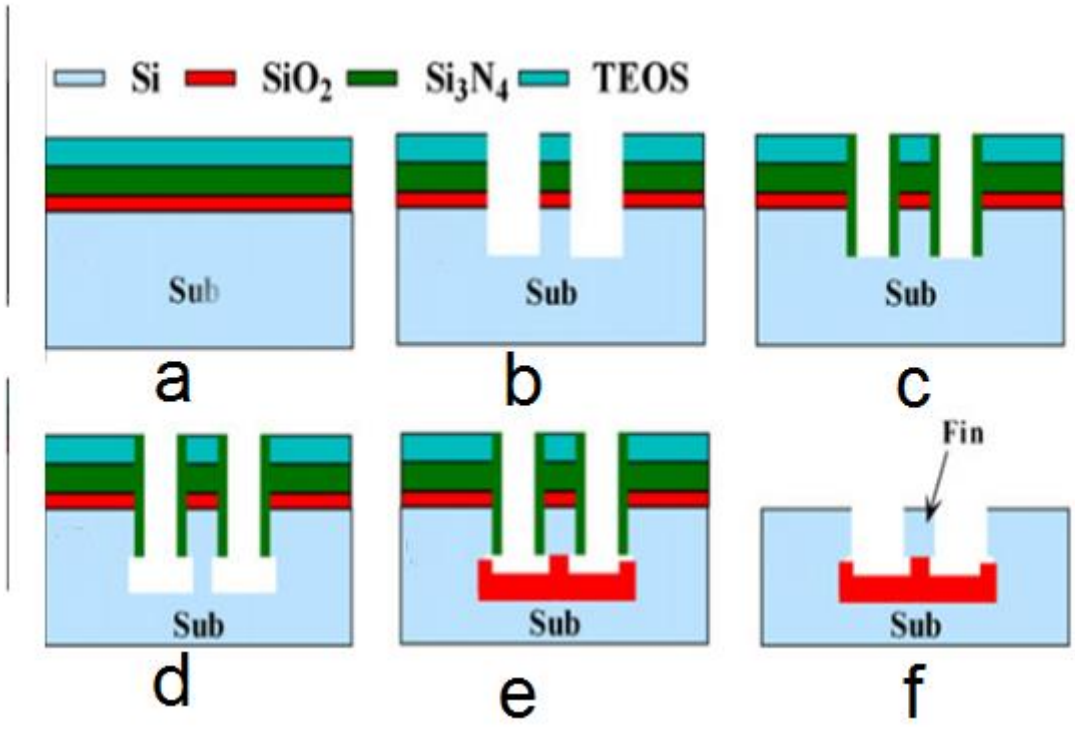


Figure 3.4 FinFET processing steps.

In the above figure 3.4 following steps are used for the manufacturing of FinFET.

- **a.** Buffer oxide /Si3N4/TEOS layer deposition
- **b.** E-beam lithography and etching of two neighbouring grooves.

c. Deposition and etching to form Si3N4 spacer

d. Anisotropic etching of silicon using Si3N4 as hard mask

e. Isolation oxidation using Si3N4 as the shielding layer

f. Stripping Si3N4 and TEOS to form fins

3.4 COMPARISION OF OFF CURRENT IN FINFET AND OTHER STRUCTURES.

From the Figure 3.5 it is clear that the off current is lesser in tri-gate structure as compare to double gate .This reason for this in double gate channel is surround only from two sides but in case of tri-gate , three sides are responsible for channel formation so it provides better control as compare to any other structures.

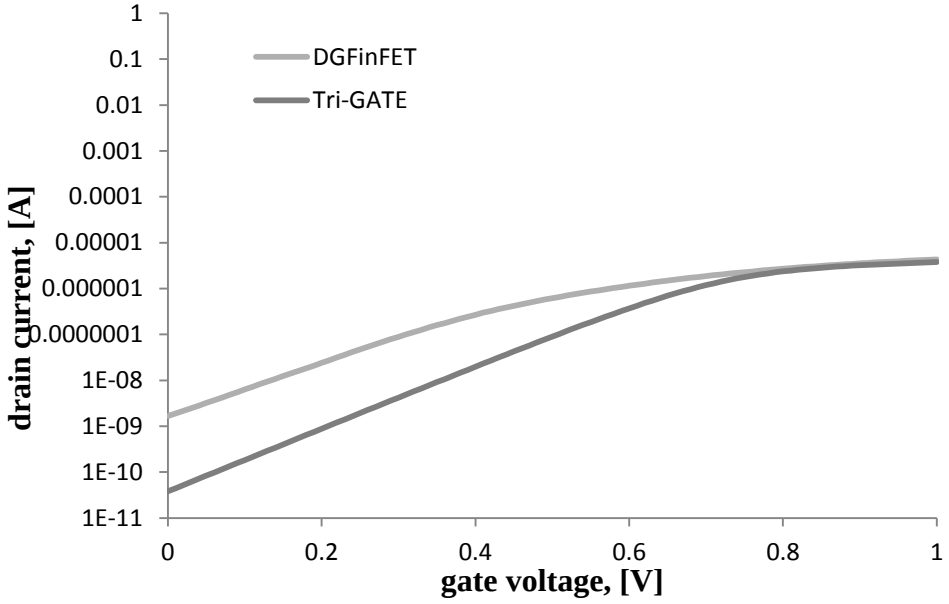


Figure 3.5 Off current in Trigate Finfet and Double gate mosfet structure

3.5 ADVANCE FINFET STRUCTURES

In order to reduce the short channel effects there are several changes made to the structure of Trigate FinFET structure such as Round edge FinFET, trapezoidal FinFET.

3.5.1 TRAPEZOIDAL FINFET

3.5.1.1 IMPACT OF INCLINED WALLS OF A TRAPEZOIDAL FINFET

Several independent studies conducted over the past decades which have suggested new and new devices architectures which offer better solution for short channel effects and allow transistor to shrink

bellow sub 100 nm regime. Many researchers suggested the functionality of the rectangular FinFET. There are several compact models which are developed for the rectangular FinFET. In the recent study by the Intel[32-33] it is shown that tri-gate transistors are in fact trapezoidal almost triangular in cross-section as shown in Figure 4. It is not clear by that time whether the non-vertical sides to the fins are a non-critical manufacturing aftermath or are deliberately engineered by Intel and what is its impact on electron mobility or other device parameters. There is a lot of speculation about the possible advantages and disadvantages of the trapezoidal shaped FinFET, or almost triangular, shaped 'bulk' FinFET.

3.5.1.2 THRESHOLD VOLTAGE CHANGE DUE TO INCLINED WALLS

The threshold voltage value which is the most important electrical parameter in modelling of MOSFETs can be extracted from either measured drain current or capacitance characteristics of a MOSFET. There are some of the most common methods which are available to measure the threshold voltage [12]. Here in this paper we have used maximum transconductance method which suggest that the value of gate voltage at which first derivative of transconductance i.e. $dg_m/dv_g=d^2I_d/dV_g^2$ is maximum is the threshold voltage of the device. The threshold voltage equation for rectangular trigate FinFET is given by equation 1[34].

Where

$$V_t = V_{fb} - \frac{1}{\left(1-\left(A_1 - A_2\right)\right)} \times \left(A_1(V_{bi} + V_d) + A_2 V_{bi} - V_{th} \ln\left[\frac{Q_{th} N_a}{n^2{}_i W_{fin}} \right] \right) \quad (1)$$

$V_{fb} = \varphi_{ms} - V_t \ln\left(\frac{N_a}{n_i}\right)$ is the flat band voltage and N_a is doping concentration of silicon channel, V_{bi} is built in potential across the source and drain junctions given by equation 2.

$$V_{bi} = \frac{kT}{q} \ln\left(\frac{N_a N_d}{n^2{}_i} \right) \quad (2)$$

where Q_{th} is the minimum carrier charge density which is required to turn it on in the strong inversion condition. The analytic expression for Q_{th} is presented in Appendix. It is a function of the device natural length. We can extend the equation (1) of the threshold voltage for the trapezoidal FinFET by doing appropriate changes to A_1 and A_2 as follows.

The parameters A1 and A2 of trapezoidal FinFET for threshold voltage detection can be expressed as a function of device natural length given by

$$A_1 = \frac{2H_{fin}A_{1,sym} + W_{fin}A_{1,asym}}{W_{fin} + 2H_{fin}} \tag{3}$$

$$A_2 = \frac{2H_{fin}A_{2,sym} + W_{fin}A_{2,asym}}{W_{fin} + 2H_{fin}} \tag{4}$$

where

$$W_{fin} = \frac{W_{fin,Top} + W_{fin,Botttom}}{2} \tag{5}$$

$$Q_{th} = \frac{2V_{th}}{q} \times \frac{C^2_{ox}}{C_{si}} \tag{6}$$

Where Q_{th} is minimum carrier sheet density required to turn on in the strong inversion condition.

$$A_{1,sym} = \frac{\exp\left(\left.L + Z_{min}\right/\beta_{sym}\right) - \exp\left(\left.L - Z_{min}\right/\beta_{sym}\right)}{\exp\left(\frac{2L}{\beta_{sym}} - 1\right)} \tag{7}$$

$$A_{2sym} = \frac{\exp\left(\left.2L - Z\right/\beta_{sym}\right) - \exp\left(\left.Z_{min}\right/\beta_{sym}\right)}{\exp\left(\frac{2L}{\beta_{sym}} - 1\right)} \tag{8}$$

$$A_{1,asym} = \frac{\exp\left(\left.L + Z_{min}\right/\beta_{asym}\right) - \exp\left(\left.L - Z_{min}\right/\beta_{asym}\right)}{\exp\left(\frac{2L}{\beta_{sym}} - 1\right)} \tag{9}$$

$$A_{2,asym} = \frac{\exp\left(\left(2L - Z_{min}\right)/\beta_{asym}\right) - \exp\left(Z_{min}/\beta_{asym}\right)}{\exp\left(\frac{2L}{\beta_{sym}} - 1\right)} \quad (10)$$

Where

$$\beta_{sym} = \frac{1}{2}\sqrt{W_{fin}\left(\frac{\varepsilon_{si} t_{ox}}{\varepsilon_{ox}} + z - \frac{z^2}{W_{fin}}\right)} \quad (11)$$

$$\beta_{asym} = \frac{1}{2}\sqrt{H_{fin}\left(\frac{2\varepsilon_{si} t_{ox}}{\varepsilon_{ox}} + 2x - \frac{x^2}{H_{fin}}\right)} \quad (12)$$

For most Leakey path (at which potential is minimum) we consider [24]

$z=W_{fin}/4$

$x=H_{fin}/4$

The is the location of minimum potential in the channel is given by z_{min}.

$$Z_{min} = \frac{L}{2} - \frac{\beta_{eff}}{2} \times \ln\left(\frac{\left(V_{bi} + V_{fb} - V'g\right)\left(\exp\left(1/\beta_{eff}\right) - 1\right) + V_d\left(\exp\left(1/\beta_{eff}\right)\right)}{\left(V_{bi} + V_{fb} - V'g\right)\left(\exp 1/\beta_{eff} - 1\right) - V_d}\right) \quad (13)$$

β_{sym} and β_{asym} is the characteristic field penetration length at the effective conductive path. For Re-TGFinFET we consider both the case of symmetric and asymmetric DGFinFET. The effective natural length is given by

$$\beta_{eff} = \frac{1}{\sqrt{\left(\frac{1}{\beta_{sym}}\right)^2 + \left(\frac{0.5}{\beta_{asym}}\right)^2}} \quad (14)$$

3.5.1.3 CORNER EFFECT ANALYSIS IN ROUND CORNER AND TRAPEZOIDAL FINFET

The corner Effect can be defined as the leakage at the interface of top and side gate[35]. It is caused by the increase of inversion charge carriers inthe proximity of the corners, which ultimately leads to leakage current. In tri gate FinFET corner effect is one of the most undesirable effects which is the main cause of the leakage. There are several methods which are used to solve this problem such as corner rounding technique as shown in Figure 3.6a.

With the round corner the impact of the effective electric field is lesser as compared to other structures.There are several other solution for reducing the corner effect such as Trapezoidal FinFET Figure 3.6b. In order to evaluate the sidewall inclination angle influence on the corners, net charge concentration and electric field was chosen as an electrostatic parameter. The effect of charge carrier in the corners is less as we increase the inclination angle. Effective electric field is lesser at the corners as the angle of inclination increases. This indicates that influence of corner effect is less in trapezoidal FinFET as compare to rectangular FinFET. Also the corner effect becomes less significant as the channel doping decreases. This is because in that case, carrier can be more uniformly distributed across the top and side gate plane interface.

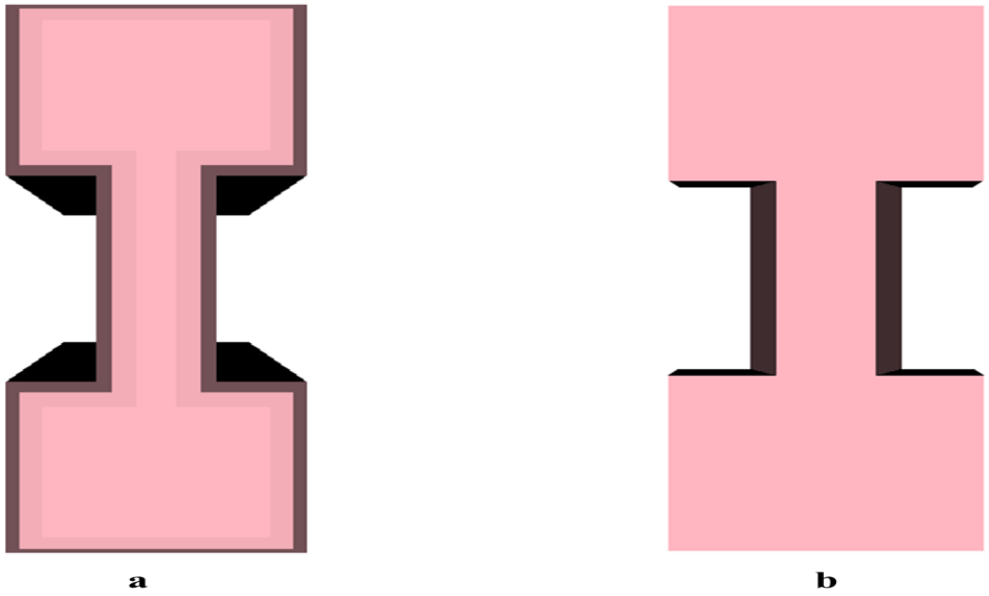


Figure 3.6 3D view of round corner and trapezoidal FinFET.

From the Figure 3.7 it is clear that the charge density present at the corners are lesser in round corner and in trapezoidal FinFET as compare to rectangular FinFET. So the leakage at the corners also becomes less.

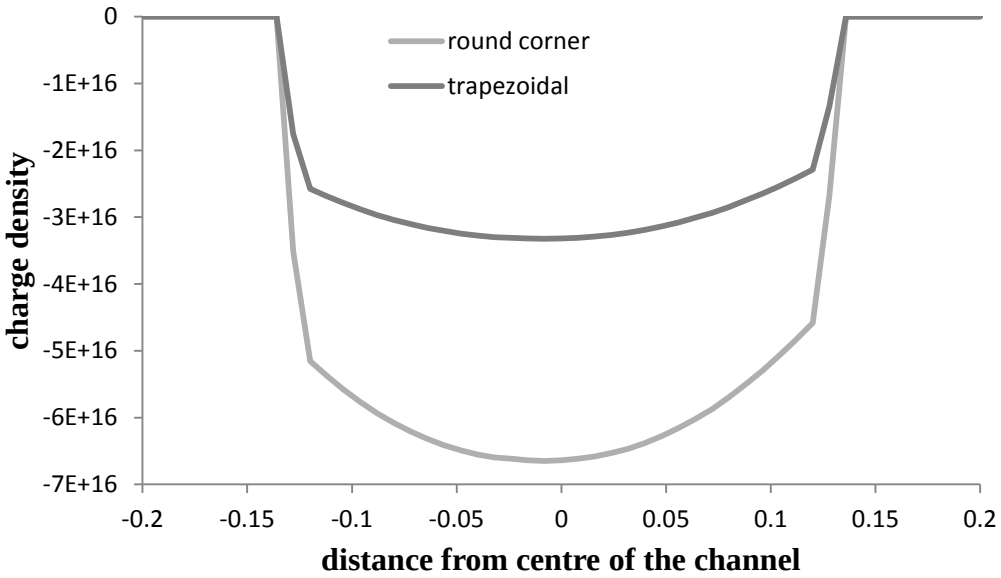


Figure 3.7 Effect of charge density at the corners.

3.5.1.4 Multi-FinFinFET

In FinFETdue to thinner fins the drain current is reduced as the charge carriers participating in the on current are lesser. So to increase the drain current, we have to increase the thickness of the Fins However the increased thickness of Fins leads to increase in short channel effects. Hence, a new structure multi-finFinFET is used. In this structure by increasing the number of fins on the same substrate the effective width of the Fins increases without increase in the short channel effects as shown in Figure 3.8

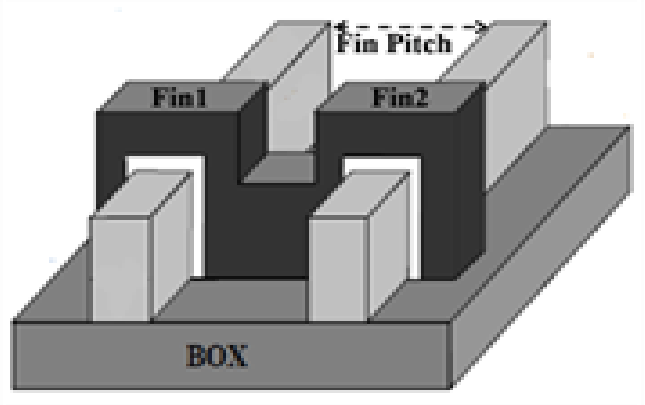


Figure 3.8Schematic view ofMultigateMOSFET

The threshold voltage equation for the Tri-gate rectangularFinFETis given by the equation 15 [34]

$$V_t = V_{fb} - \frac{A_{1,TG}\left(V_{bi}+V_d\right)+A_{2,TG}V_{bi}}{1-\left(A_{1,TG}-A_{2,TG}\right)} + \frac{V_{th}}{1-\left(A_{1,TG}-A_{2,TG}\right)}\ln\frac{\left(Q_{th}N_a\right)}{n_i{}^2 w_{fin}} \qquad (15)$$

A_1 and A_2 are the function of device natural length given in [26]. $V_{fb} = \varphi_{ms} - V_{th}\ln\left(\frac{N_a}{n_i}\right)$ is flat band voltage, φ_{ms} is the work function difference between metal and silicon, Vbi is built in potential calculated by $V_{bi} = V_{th}\ln\frac{N_d}{n_i}$.

In this model the effect of depletion charges is neglected. If the substrate is highly doped than the effect of depletion charges should be considered which affects the built in potential as well as threshold voltage, thus this effect should be modified as explained below. The modified Vt and Vbiare given by Eqs. (16) and (17).

$$V'_t = V_{fb} - \frac{A_{1,TG}\left(V'_{bi}+V_d\right)+A_{2,TG}V_{bi}}{1-\left(A_{1,TG}-A_{2,TG}\right)} + \frac{V_{th}}{1-\left(A_{1,TG}-A_{2,TG}\right)}\ln\frac{\left(Q_{th}N_a\right)}{n_i{}^2 w_{fin}} + \frac{Q_d}{C_d} \qquad (16)$$

$$V'_{bi} = V_{th}\ln\left(\frac{N_a N_d}{n_i{}^2}\right) \qquad (17)$$

Na and Nd are acceptor and donor charge densities and ni is intrinsic silicon charge concentration, Qi is the inversion charge, and Qd is the depletion charges and C_d is depletion capacitance of the order of femto farad given as:

$$Q_d = 0.5qN_a W_{fin},\ C_d = \frac{C_{si}C_{box}}{C_{si}+C_{box}}$$

$A_{1,TG}$, $A_{2,TG}$ are the parameters which are the functions of natural length and channel length as given in the and it has finite values for short channel devices but for long channel devices values their values are 0.

Qth is the minimum inversion charges required to form the channel is given by Eq.18.

$$Q_{th} = \frac{2V_{th}}{q} \times \frac{C^2 ox}{C_{si}} \qquad (18)$$

Where C_{si} and C_{ox} is capacitance of oxide and silicon respectively which is given as $C_{ox} = \varepsilon_{ox}/t_{ox}$ and $C_{si} = \varepsilon_{si}/W_{fin}$.

Chapter 4
Result and Discussion

In this dissertation work, we performed a simulation analysis to see the impact of the non-vertical sidewalls by varying the angle of inclination as shown in Figure 4.2 on the performance of the FinFET using 3-D TCAD simulator COGENDA GENIUS. Table 1 which follows the device dimensions according to ITRS 2013 roadmap and Figure 4.1 shows the device nomenclature. For the simulation we have drift-diffusion, mobility, density-gradient and quantum correction models being turned on. Density-gradient theory provides a macroscopic approach to modeling quantum transport that is particularly well adapted to semiconductor device analysis and engineering. Enhanced Lombardi mobility model was activated which accounts for mobility degradation at Si-Sio_2 interface. To find accurate threshold voltage maximum transconductance method is used.

Table 4.1 Parameters used for simulations

Parameters	Value used
Top silicon width W_{FinTop}	16 nm
Silicon height H_{Fin}	30 nm
Gate-oxide thickness	1 nm
Gate work function	4.5 eV
Channel length	50 nm
Source/drain doping	1e20 cm^{-3}
Channel doping	1e16, 1e17, 1e18 cm^{-3}

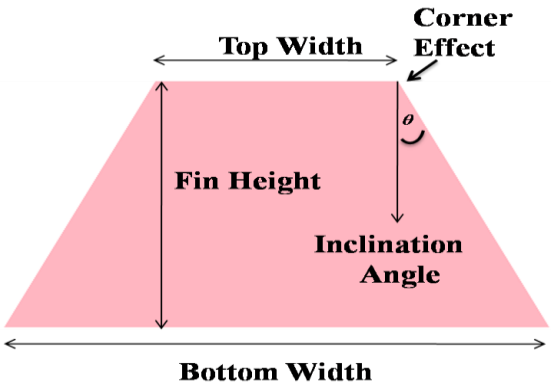


Figure 4.1 Device nomenclature

While simulation we switch on the different models such as Drift-Diffusion (DDML1) is the fundamental solver of GENIUS code for lattice temperature keeps constant though out the solve

procedure. The primary function of DDML1 is to solve the following set of partial differential equations, namely Poisson's equation, along with the hole and electron continuity equations:

MOBILITY MODELS:

The family of mobility models are the unified mobility models. The effect of high transverse and parallel E-field is an integral part in the design of these mobility models. As a result, these models are recommended for silicon MOSFET simulation. On the other hand, the availability of the unified models is limited to a few materials, such as silicon and silicon-germanium.

LOMBARDI SURFACE MOBILITY MODEL

Along an insulator-semiconductor interface, the carrier mobility's can be substantially lower than in the bulk of the semiconductor due to surface-related scattering. If no surface degradation is considered, the drain-source current may exceed about 30% for MOS simulation. The Lombardi mobility model Lombardi1988 is an empirical model that is able to describe the carrier mobility in the MOSFET inversion layer. The Lombardi model consists of three components

μ_B, The doping-dependent bulk mobility. This component mainly accounts for the ionized impurity scattering.

μ_{AC}, The mobility degradation due to acoustic phonon scattering in the inversion layer. Due to the quantum confinement in the potential well at the interface, this mobility degradation is a strong function of the transverse electric field.

μ_{SR}, The mobility degradation due to the surface roughness scattering. This component is also a strong function of the transverse electric field.

To obtain the final value of carrier mobility, the three components are combined using the Matthiessen's rule: $\mu_S^{-1} = \mu_B^{-1} + \mu_{AC}^{-1} + \mu_{SR}^{-1}$

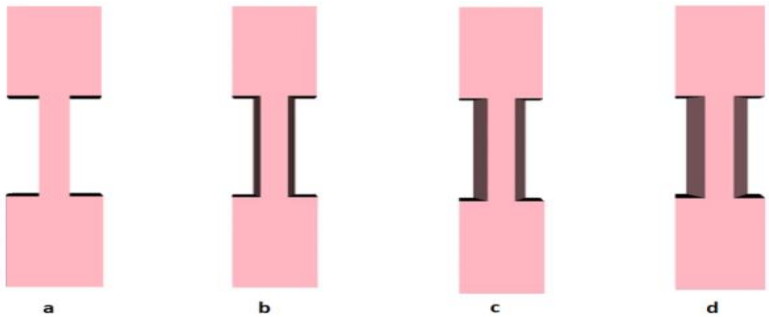


Figure 4.2.FinFET's structures. (a) rectangular shaped, (b) trapezoidal shaped with angle θ_1 (c) trapezoidal shaped with angle θ_2 (d) trapezoidal shaped with angle θ_3 where ($\theta_1 < \theta_2 < \theta_3$) and θ is the angle between top gate and side walls of the FinFET

4.1 THRESHOLD VOLTAGE CHANGE DUE TO INCLINED WALLS

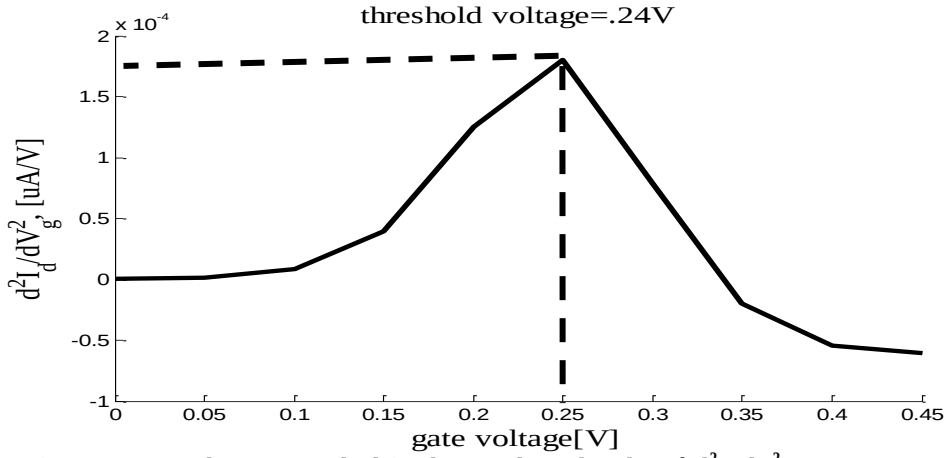


Figure 4.3a Maximum transconductance method implemented on the plot of d^2I_d/dV^2_g versus V_g.Gate-voltage at which d^2I_d/dV^2_g exhibits a maximum value is equal to threshold voltage of device. Here L=50nm, H=30nm,Wtop=16nm,Wbot=16nm,V_d=0.05V, Na=1E17, (Rectangular FinFET)

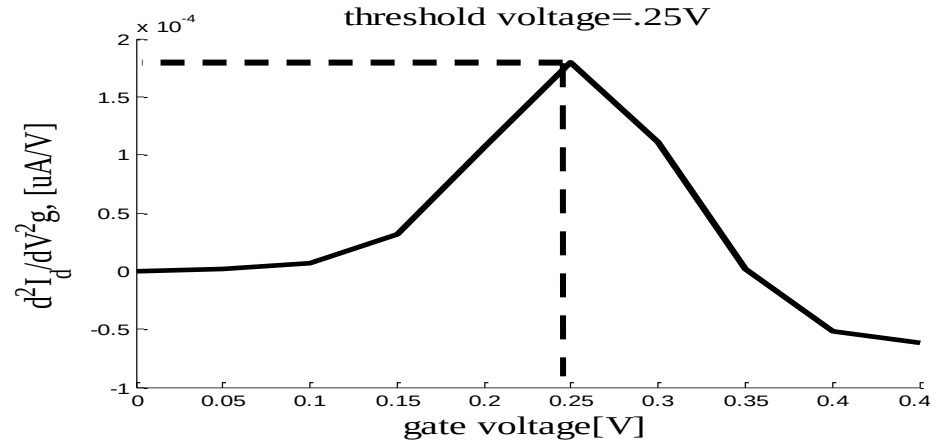


Figure 4.3b Maximum transconductancemethod implemented on the plot of d^2I_d/dV^2_g versus V_g. Gate-voltage at which d^2I_d/dV^2_g exhibits a maximum value is equal to threshold voltage of device. Here L=50nm, H=30nm, Wtop=16nm, Wbot=24nm, V_d=0.05V, Na=1E17, (Trapezoidal FinFET)

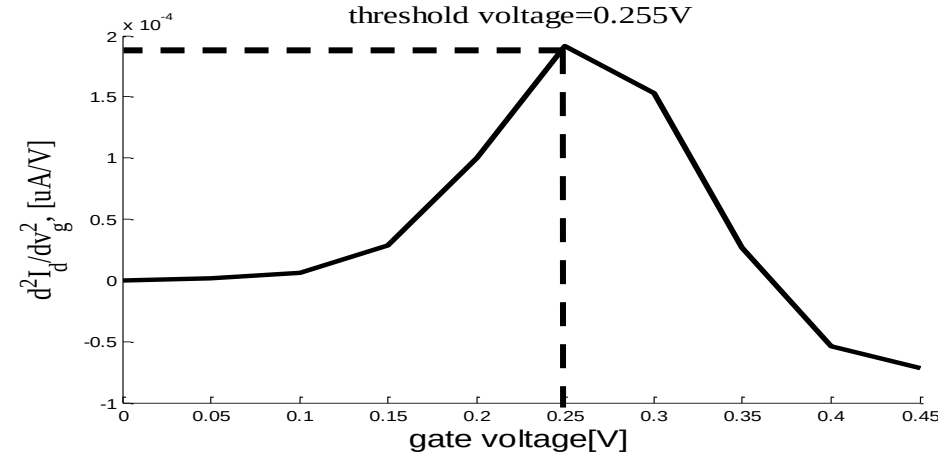


Figure 4.3c Maximumtransconductance method implemented on the plot of d^2I_d/dV^2_g versus V_g. Gate-voltage at which d^2I_d/dV^2_g exhibits a maximum value is equal to threshold voltage of device. Here L=50nm, H=30nm, Wtop=16nm, Wbot=30nm, V_d=0.05V, Na=1E17, (Trapezoidal FinFET)

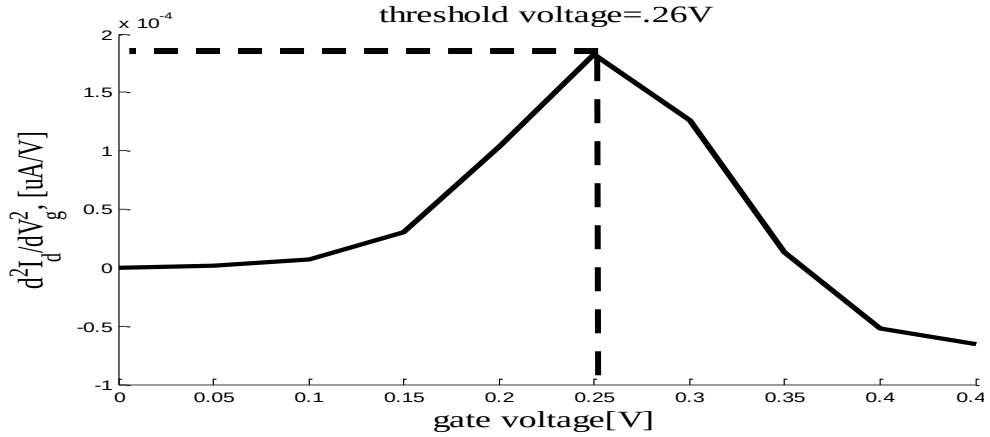


Figure 4.3d Maximum transconductance method implemented on the plot of d^2I_d/dV^2_g versus V_g. Gate-voltage at which d^2I_d/dV^2_g exhibits a maximum value is equal to threshold voltage of device. Here L=50nm, H=30nm, Wtop=16nm, Wbot=35nm, Vd=0.05V, Na=1E17, (Trapezoidal FinFET)

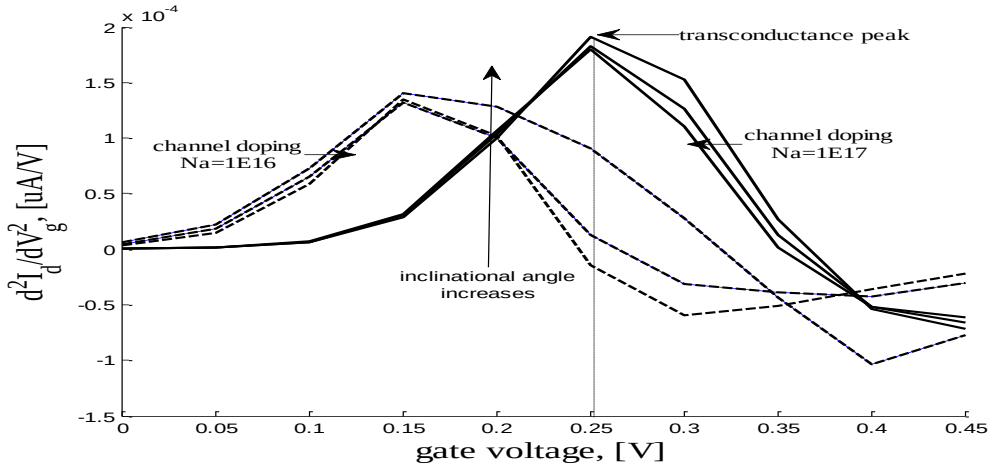


Figure 4.4.Maximum transconductance method implemented on the plot of d^2I_d/dV^2_g versus V_g. for two different doping levels. Here L=50nm,H=30nm,Wtop=16nm,Wbot=24nm to 35nm,N_a=1E16 to 1E17,Vd=.05V (Trapezoidal FinFET).

Table 2 Comparison between threshold voltage for different angle of inclination and for two doping levels.

Angle of inclination	Threshold voltage Na=1E16	Threshold voltage Na=1E17
0^0	0.15V	0.24V
9.46^0	0.16V	0.25V
13.40^0	0.165V	0.255V
18^0	0.17V	0.26V

It can be observed from the Figure 4.1 to 4.4 that the threshold voltage depends on the inclination angle and on the channel doping level. This is because of the dependence on the composition of charges present in the silicon-film. In the recent years, structures used for the rectangular FinFET typically, the (1 1 0) sidewalls crystallographic orientation and the variation on the sidewall angles leads to a change

in the surface crystallographic orientation. Which ultimately leads to change in the carrier mobility and threshold voltage. It is also found that as we change the shape from rectangular to trapezoidal the position of minium potential is also shifted which is a function of the width of the FinFET. and Figure 4.5 and Figure 4.6 show the electron density across the channel of the FinFET. The electron concentration data is taken from the cross section far from the drain at half of channel length and it can be seen that for smaller inclination angle electron concentration value is more as compare to higher inclination angle which ultimately leads to more corner effect in smaller inclination angle FinFET than higher inclination angle FinFET. There are two types of charges present in the silicon film, depletion charge and inversion charge. For both doping levels the electron concentration is above 10^{16} cm^{-3}.

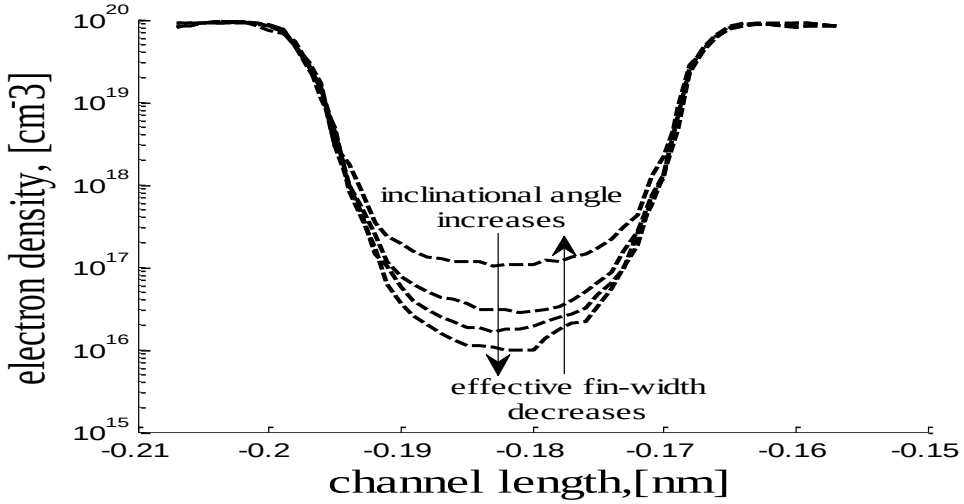


Figure 4.5 Electron density as a function of angle of inclination. Channel doping=1E18, V_d=0.05V, L=50nm, H=30nm,W_{top}=16nm, Wbot=24nm to 35nm.(Trapezoidal FinFET). Angle increases from top to bottom as (0°, 9.46°,13.40°,18°)

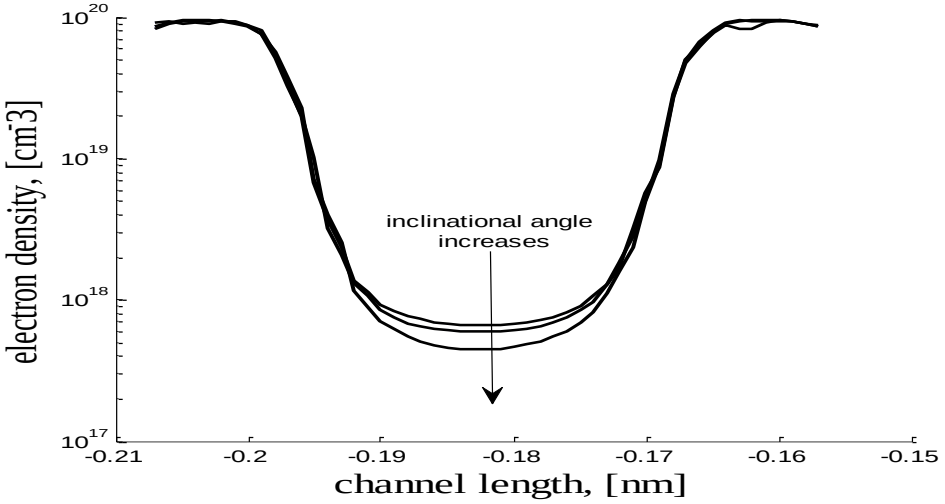


Figure 4.6 Electron density as a function of angle of inclination. Channel doping=1E16, V_d=0.05V, L=50nm, H=30nm,W_{top}=16nm,W_{bot}=24 nm to 35 nm (Trapezoidal FinFET).). Angle increases from top to bottom as (9.46°,13.40°,18°)

From the Figure 4.5 and Figure 4.6 we can easily understand that in silicon film charges mostly composed of depletion charge for the device with a doping level of 10^{17} cm^{-3} and for the device with doping level 10^{16} cm^{-3}, minority carriers are responsible for the charge composition as the depletion charge density is now limited 10^{16} cm^{-3}. In both the cases during volume inversion there is a difference in the charge distribution profile. Thisis because as we increases the channel doping concentration the carrier concentration increase near the corners and decreases in the center of the device. The main consequence of this phenomena is threshold voltage variation and it depends upon the variation in fin-width.

4.2 FinFET

4.2.1 Rectangular FinFET

- **FinFET layout**

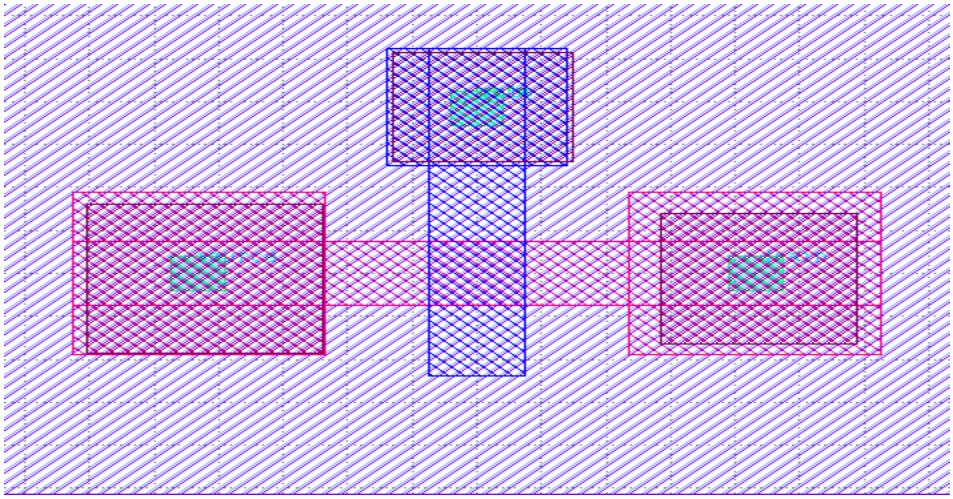


Figure 4.7 Rectangular FinFET Layout

- **3D view of rectangular FinFET.**

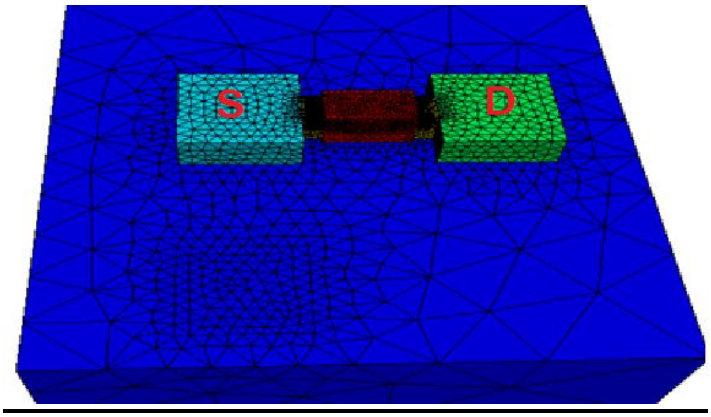


Figure 4.8 3D view of rectangular FinFET

❖ 3D view of round corner FinFET.

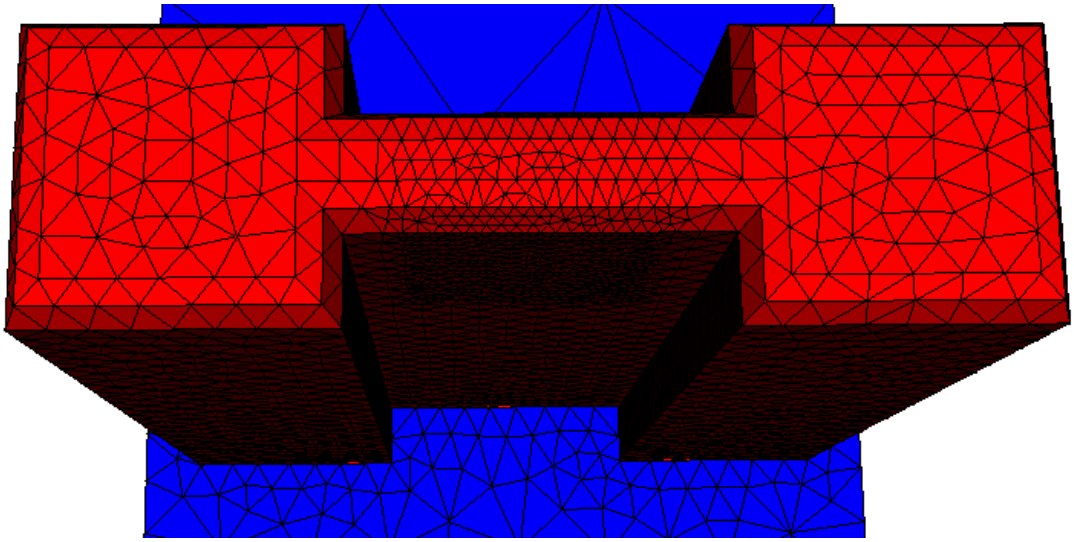


Figure 4.9 3D view of Round corner FinFET

❖ 3D view of Trapezoidal FinFET.

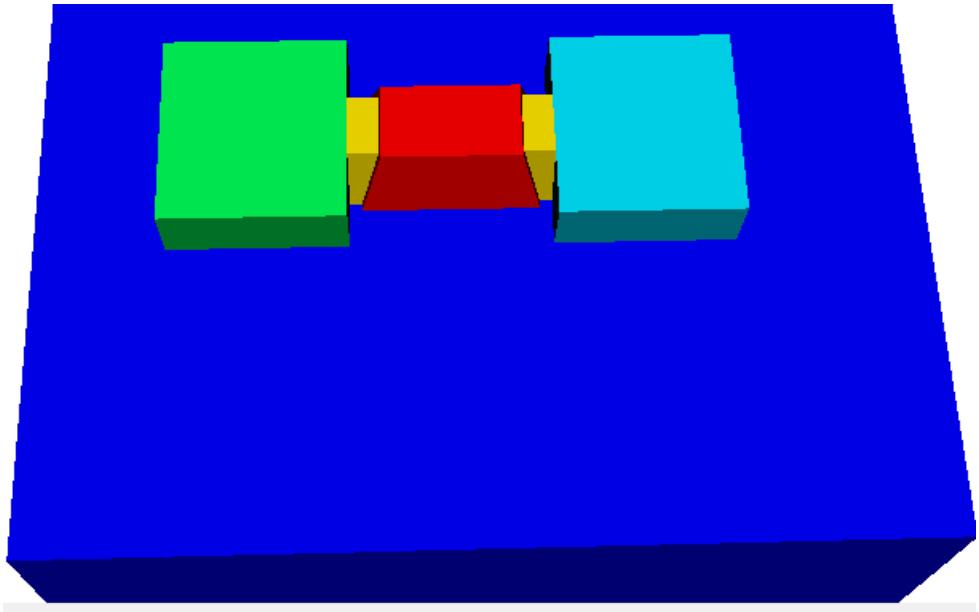


Figure 4.10 3D view of trapezoidalFinFET

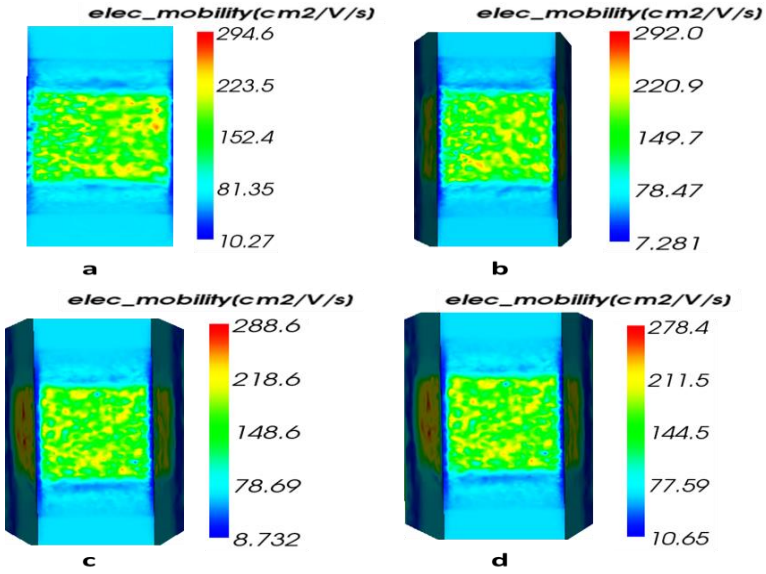


Figure 4.11 Maximum achievable electron mobility in linear region for different structures. (a) rectangularFinFET and from (b) to (d) trapezoidal FinFET with increasing angle of inclination.Vd=.05V,channel doping Na=1E18cm-3, H=30nm, L=50nmand t_{ox} =1nm.to 35nm.(Trapezoidal FinFET).

Table4.2 Comparison between electron mobility for different angle of inclination and with two doing levels.

Angle of inclination	Channel doping=1E18, Mobility $cm^2/V/S$	Channel doping=1E16, Mobility $cm^2/V/S$
0^o	149.68	688.71
9.46^o	142	620.72
13.40^o	140	585.64
18^o	136	579.52

Figure 4.11 shows the mobility of electron through the surface of different structures of trapezoidal FinFET. It can be seen that the mobility decrease as the angle of inclination increases. As the geometry of the device changed from rectangular to trapezoidal different crystal planes are exposed which have a huge impact on mobility.

4.3 CORNER EFFECT ANALYSIS AND RESULTS

The corner Effect can be defined as the leakage at the interface of top and side gate[17]. It is caused by the increase of inversion charge carriers in the proximity of the corners, which ultimately leads to leakage current. Two main factors which influence corner effect is the electric field and the carrier concentration. In this work we analyse the effect of both on device structure. Figure 4.12. shows the net

charge distribution throughout the structure. In order to evaluate the sidewall inclination-angle influence on the intensity of the corner effects, the net charge concentration and electric field was chosen as an electrostatic parameter. It is clear from the Figure 4.12. the effect of charge carrier in the corners is less as we increase the inclination angle.

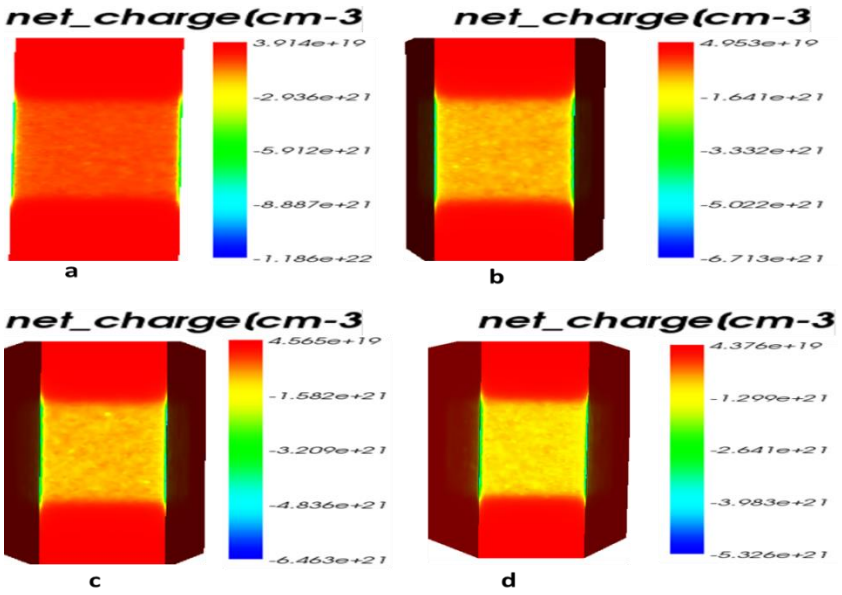


Figure 4.12 net charge present at the corner of the FinFET, (a) rectangular FinFET, from (b) to (d) trapezoidal FinFET with increasing angle of inclination.,channel doping Na=1E18 cm-3, H=30nm,,L=50nm,and Vd=.05V.

This indicates that influence of corner effect is less in trapezoidal FinFET as compare to rectangular FinFET. Also the corner effect become less significant as the channel doping decreases. This is because in that case, carrier can be more uniformly distributed across the top and side gate plane interface

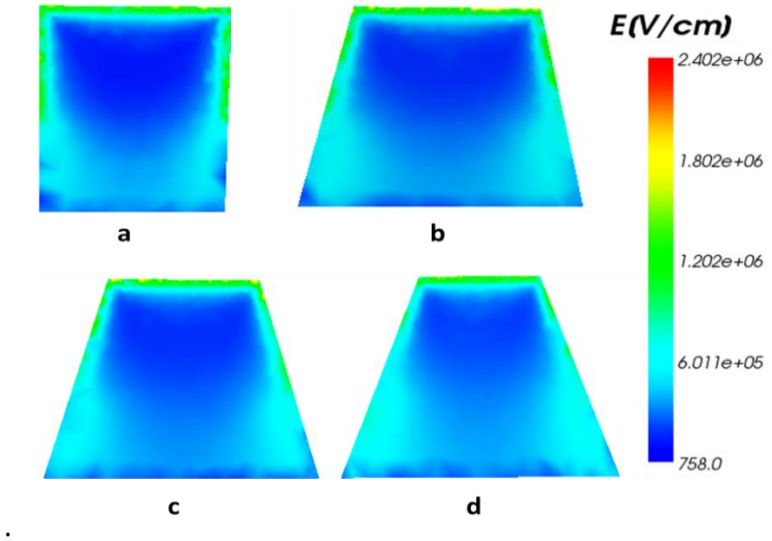


Figure 4.13Simulated distribution of electric field, (a) rectangular FinFET, from (b) to (d) trapezoidal FinFET with increasing angle of inclination,channel doping Na=1E18 cm-3, H=30nm,,L=50nm,and Vd=.05V.

4.4 IMPACT OF INCLINED FINS ON DRAIN CURRENT

There are several drain current models have been proposed for rectangular shaped FinFET. Tthese models can be extended for the trapezoidal shaped FinFET.The simulation result for transfer characteristics and output characteristics is shown in Figure 4.14.a and 4.14.b and 4.14.c. From Figures it is clear that for smaller inclination angle drain current for rectangular FinFET is more compare to trapezoidal FinFET.also from figure can see that rectangular FinFET have better short channel effects but corner effect is lesser in trapezoidal Finfet as the angle of inclination increases

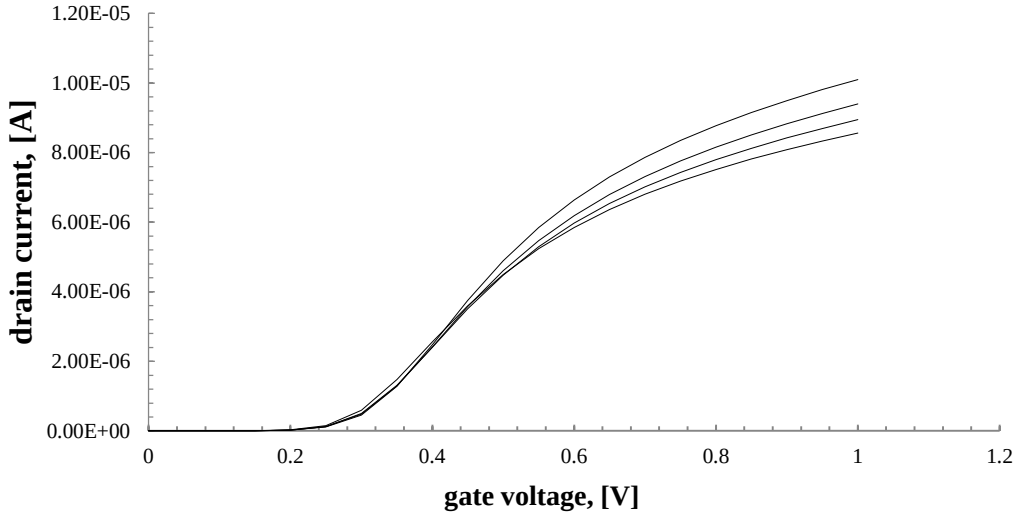


Figure 4.14.a Simulated result for drain current versus gate voltage, (with increasing angle of inclination).,channel doping Na=1E18 cm-3, H=30nm,L=50nm,and Vd=.05V.(linear region) Top ones are for trapezoidal FinFET with decreasing angle of inclination and bottom is for rectangular FinFET.

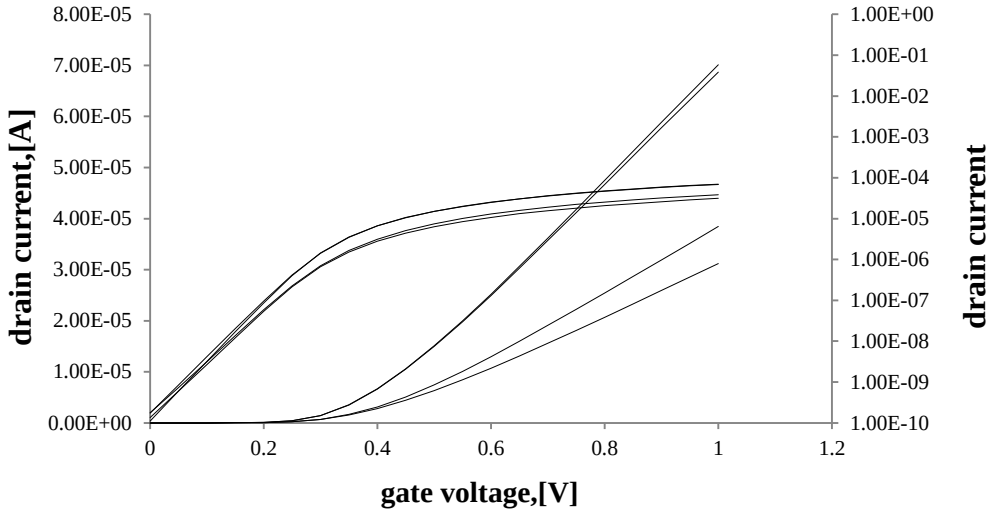


Figure 4.14.b Simulated result for drain current versus gate voltage, (with decreasing angle of inclination).,channel doping Na=1E18 cm-3, H=30nm,,L=50nm,and Vd=1V.(saturation region).Top ones for rectangular FinFET and bottom is for trapezoidal FinFET with increasing angle of inclination.

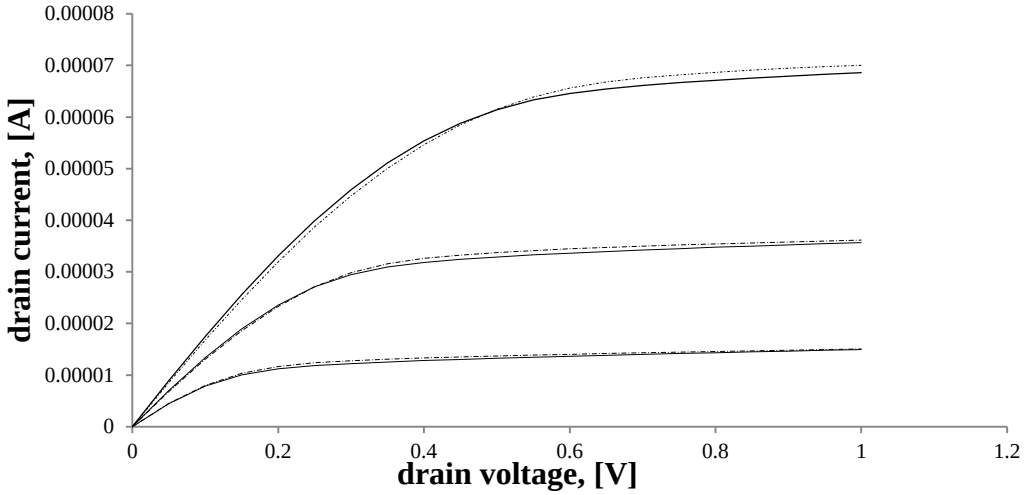


Figure 4.14.c Simulated result for drain current versus drain voltage, channel doping Na=1E18 cm-3, H=30nm, L=50nm and Vd=1V. Solid line for trapezoidal FinFET($\theta = 9.36$),and dotted for rectangular FinFET.

Table 4.3 Comparison between Ion/Ioff ratio for different angle of inclination and with three doing levels.

Angle of inclination	Channel doping=1E17 $cm^{-3,}$ Ion/Ioff	Channel doping=1E18$cm^{-3,}$ Ion/Ioff	Channel doping=5E18 $cm^{-3,}$ Ion/Ioff
9.46^o	147486	405315	14393395
13.40^o	149472	577032	18827586
18^o	276830	749745	15771929

Table4.4 Comparison between DIBL for different angle of inclination and with three doing levels.

Angle of inclination	Channel doping=1E17 $cm^{-3,}$, DIBL	Channel doping=1E18 $cm^{-3,}$, DIBL	Channel doping=5E18 $cm^{-3,}$, DIBL
9.46^o	0.014285	0.057142	0.02857
13.40^o	0.042857	0.042587	0.02857
18^o	0.042857	0.042587	0.07142

4.5 CHANNEL UNDERLAP TECHNIQUR FOR LEAKAGE REDUCTION

This technique shows overall improvement in leakage current of double gate FinFET with Gate-Source/Drain underlap method. A new structure introduced by the concept of dual-*k* spacer between gate and source. Here we optimize the underlap length; we analyse the effect of different spacer width on leakage current.Simulation results shows improvement in the $\left(I_{on}/I_{off}\right)$ as we change the device physical parameters such as spacer width, spacer material and length. With the introduction of this structure gate shows a very good control over the channel as the fringing field increases at the underlap.

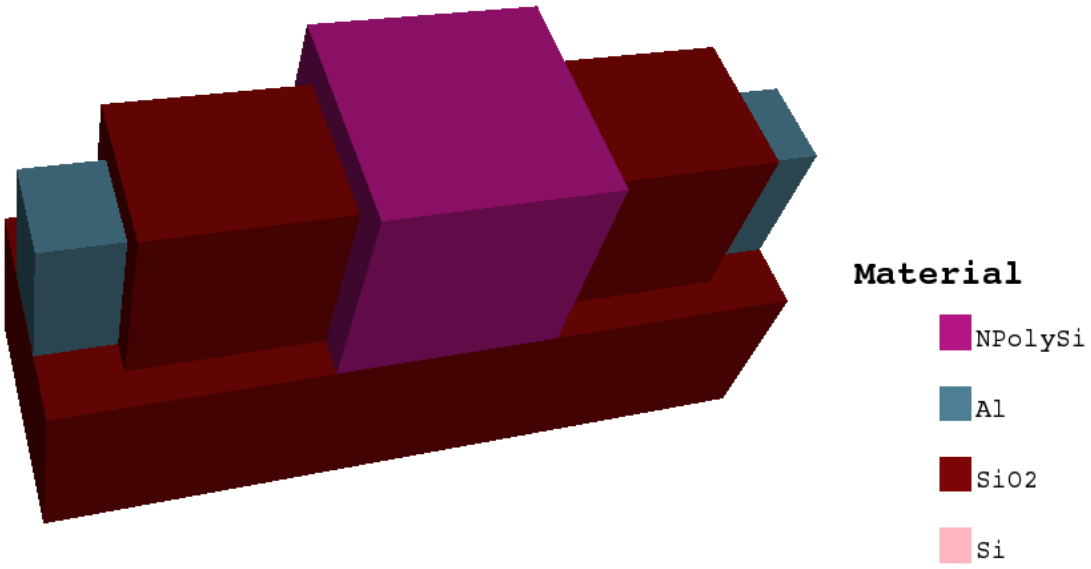


Figure 4.15 3D view of tri gate FinFET.

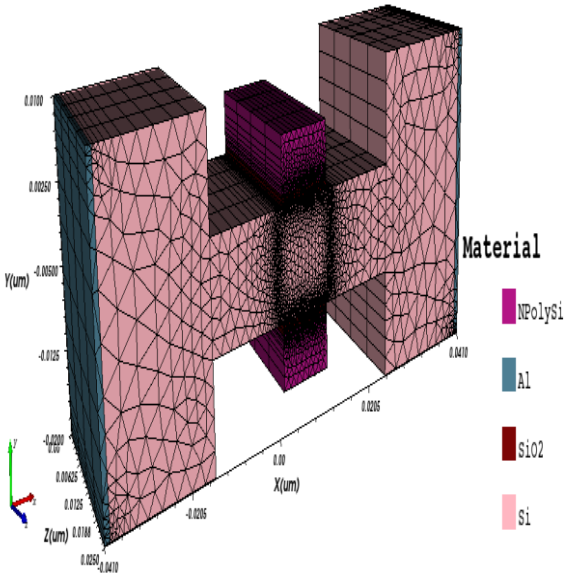
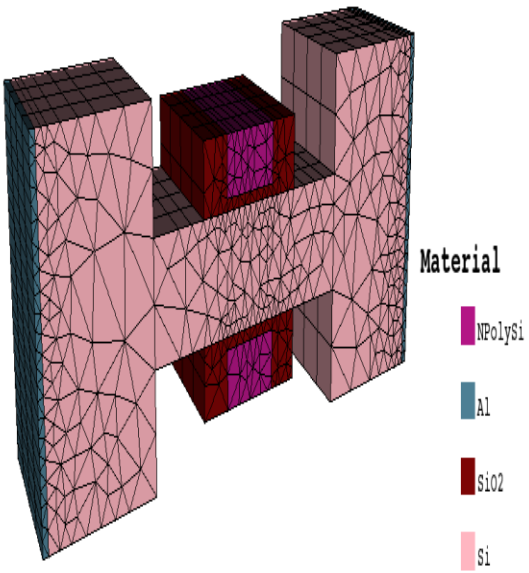


Figure 4.16 3D view of Double gate Figure



4.17 3D view of Double gate with space

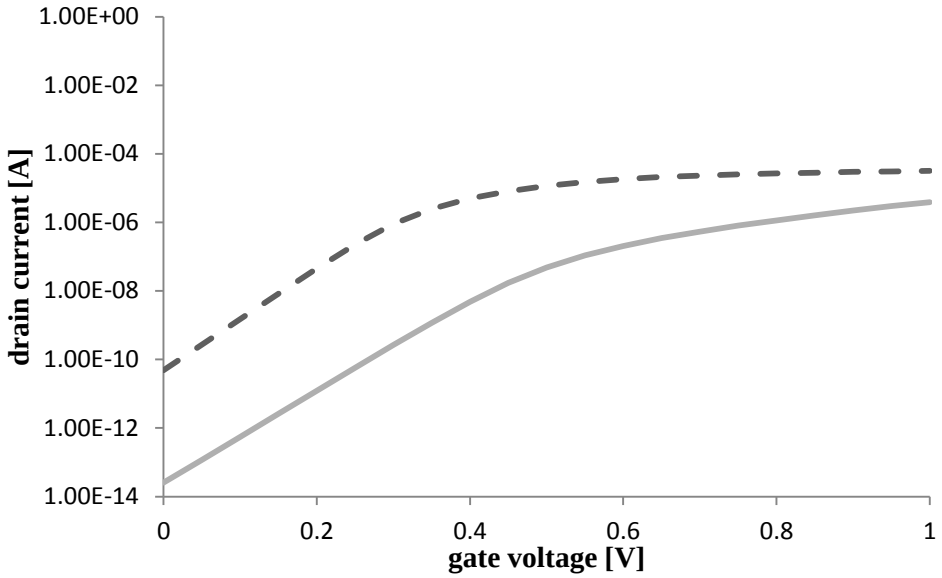


Figure4.18 Id-Vg plot with two different spacer material for triple-gate structure dashed line is for SiO2 and solid line for Nitride material

From the above results and structures it is clear that drive current, leakage current, and their ratio are optimized with the use of the high-*k* spacer and underlap length. This technique is useful for reducing the leakage.

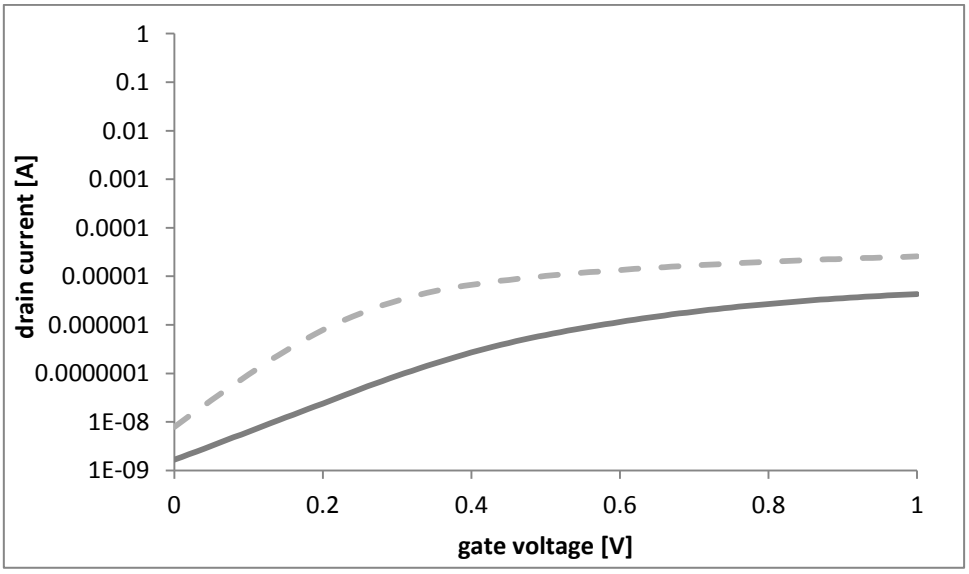


Figure 4.19 Id-Vg plot with two different spacer material for double-gate structure dashed line for Sio2 and solid line is for Nitride material.

4.6 DEPLETION CHARGE EFFECTS IN MULTI-FIn FINFET

If the substrate is highly doped then the effect of depletion charges should be considered which affects the built in potential at the source/drain and channel junction which in turn

changes the threshold voltage as shown in equation 16. Figure 4.20 shows the changes in the drain current due to depletion charge effects,

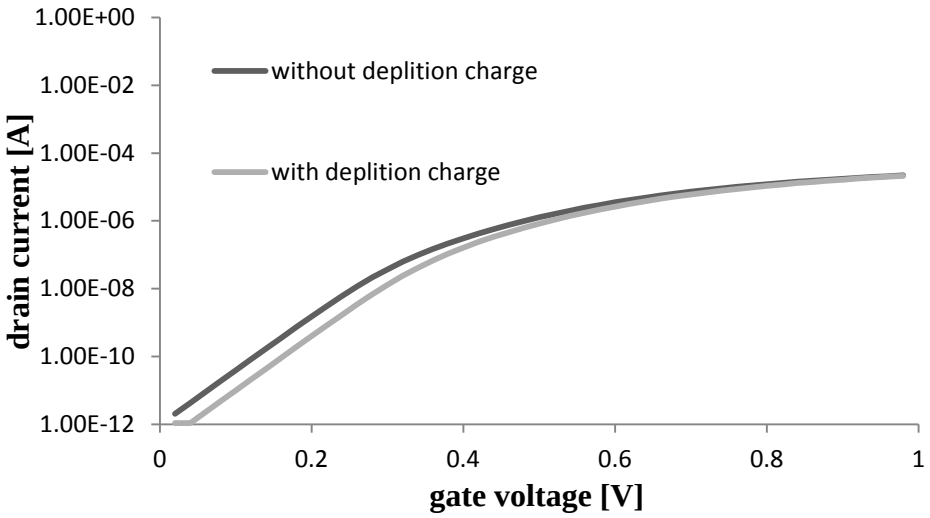


Figure 4.20 Simulation result of threshold voltage change due to depletion charge effect. Here source/drain doping is 1e20 cm^{-3} and substrate doping is 1e18 cm^{-3}. H_{fin}=20nm, W_{fin}=30nm, Oxide thickness is 1nm and channel length is 50nm.

From Figure 4.21 it can be seen that threshold voltage increases due to QMEs, the reason behind this is inversion charge distribution changes quantum mechanically giving a peak of charge inside the substrate at a distance away from SIO2-Si interface. Due to QMEs the effective thickness of the gate oxide layer increases which reduces the oxide coupling and results in increased leakage current.

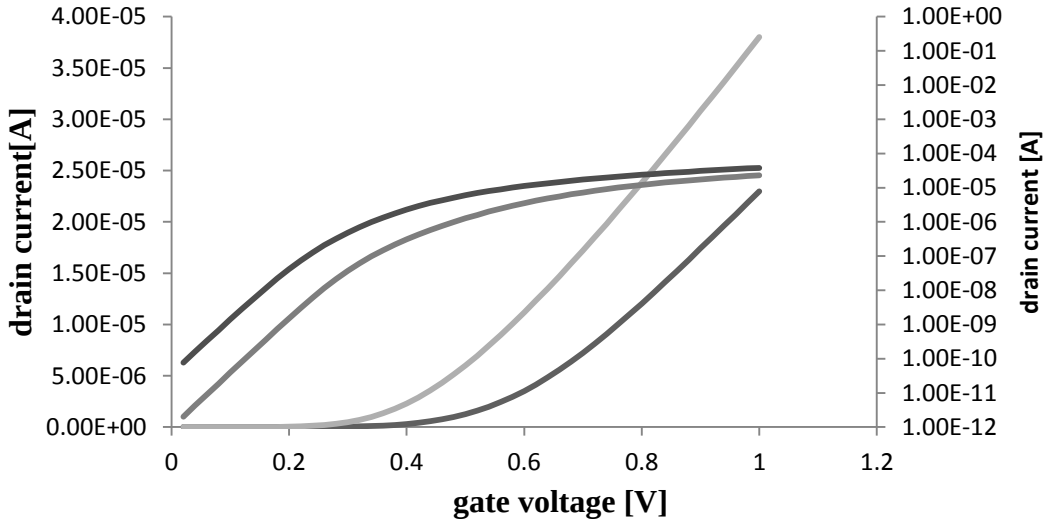


Figure 4.21. Drain current versus gate voltage including quantum effects, Comparison of drain current using classical and quantum equation. Gray line represent quantum simulation and black line represent classical simulation.Vd=0.5 V, Vg from 0 to 1V. Change in threshold voltage of 0.1V is observed due to quantum mechanical effect

Chapter 5
Conclusion and Future Scope

Conclusion

In this dissertation work, a trapezoidal FinFET has been designed considering different doping concentration and simulated on TCAD tool Cogenda genius. Various parameters such as threshold voltage, mobility, electric field, charge density has been evaluated and compared with those of rectangular shaped FinFET. It has been observed that the ratio of the Ion/Ioff increases significantly in trapezoidal FinFET as compare to rectangular FinFET. This indicates that trapezoidal FinFET, if employed in electronic circuitry could be a major source of performance enhancement.

Further, corner effect result in large leakage current in FinFETs. In a trapezoidal FinFET due to side wall inclination angle, the electric field at the corner is significantly reduced resulting in a comparatively lower corner effect. This suggests that a trapezoidal FinFET could be beneficial in controlling large power dissipation in the present scenario of nano scale regime.

Future Scope

We observe that as the inclination angle of trapezoidal FinFET changes, change in the threshold voltage occurs. So making fin shape an excellent candidate for multi-threshold FinFET design. Multi-threshold FinFETs can be constructed by manufacturing different fin shapes with different inclination angle within a single IC which can be very useful in many other analog applications.

Publications

- Gaurav Musalgaonkar and Arun Chatterjee "TCAD simulation analysis and comparison between tri-gate rectangular and trapezoidal finfet", *Journal of electron device* Vol. 21, 2015, pp. 1881-1887.

- Gaurav Musalgaonkar and Arun Chatterjee "TCAD simulation and analysis of drain current and threshold voltage in single fin and multi-fin finfet" Communicated in *Journal of engineering science and technology.*

- Gaurav Musalgaonkar and Arun Chatterjee "Performance and design optimization of rectangular FinFET using tapered shape structure" Communicated in *STM journals.*

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Appendix

❖ GENIUS CODE FOR RECTANGULAR TRI-GATE FINFET

```
#=================================================================================
# GENIUS Example. Build NMOS with TET mesh
#=================================================================================

GLOBAL    T=300 DopingScale=1e18

# Create an initial simulation mesh

MESH      Type = S_Tet4  tetgen="pzAq"
X.MESH    WIDTH=0.001  N.SPACES=1
X.MESH    WIDTH=0.008  N.SPACES=4
X.MESH    WIDTH=0.001  N.SPACES=5
X.MESH    WIDTH=0.001  N.SPACES=5
X.MESH    WIDTH=0.02  N.SPACES=20
X.MESH    WIDTH=0.001  N.SPACES=5
X.MESH    WIDTH=0.001  N.SPACES=5
X.MESH    WIDTH=0.008  N.SPACES=4
X.MESH    WIDTH=0.001  N.SPACES=1
Y.MESH    DEPTH=0.002  N.SPACES=2
Y.MESH    DEPTH=0.01  N.SPACES=5
Y.MESH    DEPTH=0.002  N.SPACES=2
Z.MESH    WIDTH=0.002  N.SPACES=2
Z.MESH    WIDTH=0.01  N.SPACES=5

# Specify oxide and silicon regions
REGION    Label=NSpc      Material=Ox X.MIN=0.0  X.MAX=0.042 Y.MIN=0.0  Y.MAX=0.014
Z.min=0 Z.max=0.012
REGION    Label=NGate     Material=Al X.MIN=0.01  X.MAX=0.032 Y.MIN=0.0  Y.MAX=0.014
Z.min=0.0 Z.max=0.012
REGION          Label=NOxide          Material=Ox   X.MIN=0.01     X.MAX=0.032   Y.MIN=0.001
Y.MAX=0.013 Z.min=0.001 Z.max=0.012
REGION          Label=NSiliconL       Material=Si   X.MIN=0.001     X.MAX=0.01   Y.MIN=0.002
Y.MAX=0.012 Z.min=0.002 Z.max=0.012
REGION          Label=NSiliconM       Material=Si   X.MIN=0.01     X.MAX=0.032   Y.MIN=0.002
Y.MAX=0.012 Z.min=0.002 Z.max=0.012
REGION          Label=NSiliconR       Material=Si   X.MIN=0.032     X.MAX=0.041   Y.MIN=0.002
Y.MAX=0.012 Z.min=0.002 Z.max=0.012
REGION          Label=NSource         Material=Al   X.MIN=0.0      X.MAX=0.001   Y.MIN=0.002
Y.MAX=0.012 Z.min=0.002 Z.max=0.012
REGION          Label=NDrain          Material=Al   X.MIN=0.041     X.MAX=0.042   Y.MIN=0.002
Y.MAX=0.012 Z.min=0.002 Z.max=0.012
```

```
DOPING    Type=analytic
PROFILE       Type=Uniform   Ion=Acceptor     N.PEAK=1E18   X.MIN=0.001     X.MAX=0.041
Y.MIN=0.002  Y.MAX=0.012 Z.min=0.002 Z.max=0.012
PROFILE       Type=Uniform   Ion=Donor     N.PEAK=1E20   X.MIN=0.001     X.MAX=0.01
Y.MIN=0.002 Y.MAX=0.012 Z.min=0.002 Z.max=0.012
PROFILE       Type=Uniform   Ion=Donor     N.PEAK=1E20   X.MIN=0.032     X.MAX=0.041
Y.MIN=0.002  Y.MAX=0.012 Z.min=0.002 Z.max=0.012

PMI Region=NGate Type=basic real<AFFINITY>=4.4 Print=1


METHOD    Type=Poisson
SOLVE

EXPORT CgnsFile='op13.cgns'  vtk='op13.vtu'
```

❖ **PYTHON SCRIPT FOR RECTANGULAR FINFET IN LINEAR REGION**

```
# do global settings
Global T=300 DopingScale=1.0000000000000000e+20 Z.Width=1 ResistiveMetal=true

# do import source
IMPORT TIF3D="./nmos_16nm.tif3d"

# do boundary settings
Boundary ID=drain Type=solderpad res=10
Boundary ID=gate Type=solderpad res=10
Boundary ID=gnd Type=solderpad res=10
Boundary ID=source Type=solderpad res=10
Boundary ID=sub Type=ohmiccontact res=10

VSource Type=VDC ID=drainConstVConst=0.05
VSource Type=VDC ID=gndConstVConst=0
VSource Type=VDC ID=sourceConstVConst=0
VSource Type=VDC ID=subConstVConst=0

PMI Region=npoly Type=Basic real<AFFINITY>=4.5 print=1

Method Type=Poisson damping=Potential ns=Basic
Solve
Method Type="DDML1" damping=Potential ns=Basic
Solve Type=Equilibrium
Method Type="DDML1" NS=Basic ls=MUMPS
Solve Type=DC Label="ramp1" VScan=drain VStart=0 VStop=0.05 VStep=0.01
out.prefix="idvglinramp1"
Attach Electrode=drain Vapp=drainConst
Attach Electrode=gndVapp=gndConst
Attach Electrode=source Vapp=sourceConst
Attach Electrode=sub Vapp=subConst
##Hook Load=vtk
Solve Type=DC Label=result VScan=gate VStart=0 VStop=1 VStep=0.05 out.prefix=idvglin
Export VtkFile="idvglinresult.vtu" CgnsFile="idvglinresult.cgns"
```

❖ **PYTHON SCRIPT FOR RECTANGULAR FINFET IN SATURATION REGION**

```
# do global settings
Global T=300 DopingScale=1.0000000000000000e+20 Z.Width=1 ResistiveMetal=true

# do import source
IMPORT TIF3D="./nmos_16nm.tif3d"

# do boundary settings
Boundary ID=drain Type=solderpad res=10
Boundary ID=gate Type=solderpad res=10
Boundary ID=gnd Type=solderpad res=10
Boundary ID=source Type=solderpad res=10
Boundary ID=sub Type=ohmiccontact res=10
```

```
VSource Type=VDC ID=drainConstVConst=1.0
VSource Type=VDC ID=gndConstVConst=0
VSource Type=VDC ID=sourceConstVConst=0
VSource Type=VDC ID=subConstVConst=0

PMI Region=npoly Type=Basic real<AFFINITY>=4.5 print=1

Method Type=Poisson damping=Potential ns=Basic
Solve
Method Type="DDML1" damping=Potential ns=Basic
Solve Type=Equilibrium
Method Type="DDML1" NS=Basic ls=MUMPS
Solve Type=DC Label="ramp1" VScan=drain VStart=0 VStop=1.0 VStep=0.05
out.prefix="idvgsatramp1"
Attach Electrode=drain Vapp=drainConst
Attach Electrode=gndVapp=gndConst
Attach Electrode=source Vapp=sourceConst
Attach Electrode=sub Vapp=subConst
##Hook Load=vtk
Solve Type=DC Label=result VScan=gate VStart=0 VStop=1 VStep=0.05 out.prefix=idvgsat
Export VtkFile="idvgsatresult.vtu" CgnsFile="idvgsatresult.cgns"
```