STUDY THE PERFORMANCE ANALYSIS OF MULTI WALLED CARBON NANOTUBE BASED VLSI INTERCONNECTS

Dissertation submitted in partial fulfillment of the requirements
for the award of the degree of

Master of Technology

In

VLSI Design

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July, 2014

CERTIFICATE

I hereby declare that the work which is being presented in the dissertation entitled, **"Study the Performance Analysis of Multi Walled Carbon Nanotube based VLSI Interconnects"** in partial fulfillment of the requirement for the award of degree of Master of Technology (VLSI Design) at the Department of Electronics and Communication Engineering, Thapar University, Patiala, is an authentic record of my own work carried out under the supervision of Dr. Mayank Kumar Rai, Assistant Professor, ECED.

The matter presented in this dissertation has not been submitted in any other University/Institute for the award of any other degree.

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ACKNOWLEDGEMENTS

I take this opportunity to express my profound sense of gratitude and respect to all those who helped me through the duration of this dissertation. I acknowledge with gratitude and humility my indebtedness to **Dr. Mayank Kumar Rai, Assistant Professor,** Department of Electronics and Communication Engineering, Thapar University, Patiala, under whose guidance I had the privilege to complete this dissertation. I wish to express my deep gratitude towards him for providing individual guidance and support throughout the dissertation work.

I convey my sincere thanks to **Head of the Department, Dr. Sanjay Sharma** as well as **PG Coordinator, Dr. Kulbir Singh, Associate Professor, ECED**, entire faculty and staff of Electronics and Communication Engineering Department for their encouragement and cooperation.

My greatest thanks are to all who wished me success especially my family. Above all I render my gratitude to the Almighty who bestowed ability and strength in me to complete this work.

Mohit

ABSTRACT

The rapid growth in the VLSI technology is mainly due to the continuous reduction in the feature size of device. With the fast developments in the VLSI technology and design, the clock speeds are increasing and clock frequency is reaching in the Gigahertz range. This high speed transmission of signals in high speed applications is enlisting demands on interconnect performance and stressing the previously negligible effects in interconnects such as ringing, signal delay, reflections, crosstalk, etc.

As we move into the deep sub-micron level, the channel length of the device decreases to tens of nanometres with the scaling of technology. At this resolution, the die size and device density of the circuit increases rapidly. This increase makes the requirement of long interconnects in VLSI chips. Long interconnects lead to increase in propagation delay of the signal. The area required for the device (MOSFET) has reduced to such an extent that it is insignificant when compared to the surface area required for interconnect, vias and contact routing. This makes the modern VLSI chips more interconnect limited as they have started to dominate on some of the most relevant factors of the digital integrated circuits such as reliability, speed and energy consumption. Therefore, a precise and deep analysis of the behaviour of interconnect is very essential in designing of the VLSI chip. Accurate modelling of on-chip wiring which includes all the parasitic-induced delays and stray coupling is essential to the circuit designer. The parasitic effects increase as the technology is going in deep sub-micron level because of the increase in die size and interconnect lengths along with increasing speed of the chips. Interconnects are predicted to be responsible for 70-80% of the signal delay in high-speed systems. This delay has to be accounted for during the designing process of the chip, failing to which can lead to logic glitches in digital circuits and distortions in analog circuits, ultimately leading to failure of the circuit. Hence it is extremely important for the designers to include the interconnect sub circuitry during the simulation process as efficiently as possible.

In this dissertation work, the impedance parameters of copper and MWCNT interconnects at different interconnect lengths are calculated and their effect on performance of interconnect is analysed and compared. The impedance parameters for MWCNT interconnect at different diameters of MWCNTs are also calculated and their effect on the performance of interconnect is analysed. Performance analysis in terms of propagation delay and power dissipation reveal that MWCNT is a more preferable choice compared to copper at

global interconnects. Both power and delay of MWCNT increases as the line length increases. Also, the performance of MWCNT at different tube diameters indicate that propagation delay improves as the tube diameter increases. Performance analysis in terms of propagation delay and power dissipation at global lengths, reveal that MWCNT performs better than optical interconnects up to a certain length after which the performance of optical interconnect is better.

Piece-wise transient analysis is carried out for interconnect at global length. Analytical model using alpha-power law of CMOS inverter driving a π-RLC interconnect has been used to predict the response of the circuit for a fast ramp input signal. The results show that there is an agreement between the results extracted and SPICE simulation results. The discharging time is same for both cases.

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ABBREVIATIONS

AR	Aspect Ratio
IC	Integrated Circuit
LSI	Large Scale Integration
CMOS	Complementary Metal Oxide Semiconductor
CNT	Carbon Nanotube
EM	Electo-Magnetism
FET	Field Effect Transistor
GNR	Graphene Nanoribbon
MLGNR	Multilayer Graphene Nanoribbon
GaAs	Gallium Arsenide
GHz	Giga Hertz
MFP	Mean Free Path
MSI	Medium Scale Integration
MWCNT	Multi Walled Carbon Nanotube
RC	Resistance-Capacitance
RLC	Resistance-Inductance-Capacitance
SPICE	Simulation Program with Integrated Circuit Emphasis
SWCNT	Single Walled Carbon Nanotube
VLSI	Very Large Scale Integration

CHAPTER

1

Introduction

1.1 Motivation

The fast growth in the VLSI technology is mainly due to the continuous reduction in the feature size of device. Feature size is the minimum length of the channel of the transistor (MOSFET). Due to the rapid growth in die size and chip density, the length of interconnects in increasing and so is their packing density. Moreover, their packing is becoming increasingly complex. With the fast developments in the VLSI technology and design, the clock speeds are increasing and clock frequency is reaching in the Gigahertz range.

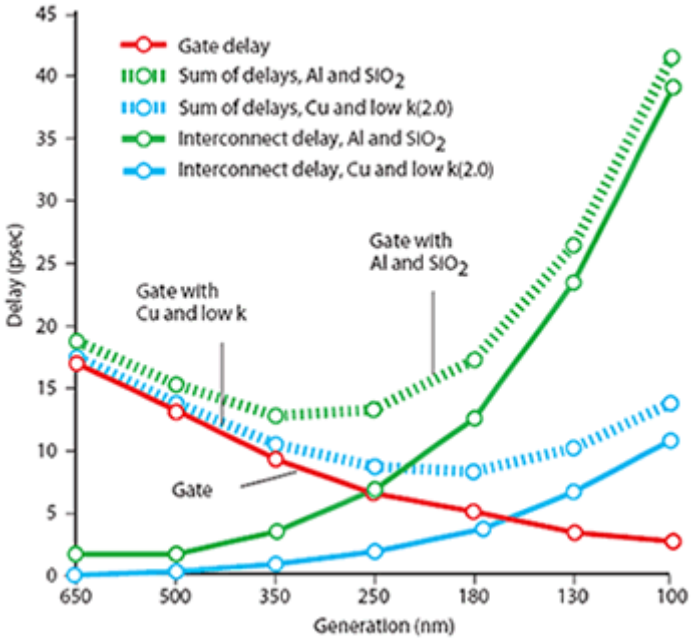

Figure 1.1 Effect of scaling on signal delay in high speed systems [1].

This high speed transmission of signals in high speed applications is enlisting demands on interconnect performance and stressing the previously negligible effects in interconnects such as ringing, signal delay, reflections, crosstalk, etc. [1].

Fig. 1.1 shows the effect of scaling on the global interconnect delay. It is observed that the delay increases as the cubic power of the scaling factor [1]. Interconnects are predicted to be responsible for approximately 70 to 80% of the delay in signal in high speed systems. This delay has to be accounted for during the designing process of the chip, failing to which can lead to logic glitches in digital circuits and distortions in analog circuits, ultimately leading to failure of the circuit. Hence it is extremely important for the designers to include the interconnect sub circuitry during the simulation process as efficiently as possible.

1.2 Statement of problems

Following objectives have been carried out in this dissertation report:

1) Study the performance of Multi Walled Carbon Nanotube (MWCNT) as VLSI interconnect at global lengths.
2) Study the effect of length of interconnect on performance of MWCNT based interconnect.
3) Study the effect of tube diameter in the bundle on performance of MWCNT based interconnect.
4) Compare the performance of MWCNT with copper interconnects at 22nm technology node.
5) Compare the performance of MWCNT with optical interconnects at 22nm technology node.
6) Study the analytical model for delay prediction of a CMOS invertor driving a load.

1.3 Organization of report

Chapter 2 begins with the literature review of different interconnect technologies. Literature review of models for interconnect delays, repeater technologies has been done. Problems faced by copper with scaling of technology are reviewed in this chapter. The potential of CNTs as a future VLSI interconnect is also reviewed in the last section of this chapter.

Chapter 3 starts with the basic introduction to interconnect parameters and analysis. The effect of scaling on key performance parameters of interconnect are discussed. Concept of repeaters and repeater model are briefly discussed. Different configurations of repeaters and their design methodologies are discussed in brief. The effect of various parameters on performance of interconnect is discussed. In the next section the properties of CNT which makes it a potential candidate for future VLSI applications are discussed briefly. Finally, optical interconnect systems are discussed in brief.

Chapter 4 is mainly focused on analytical delay prediction model for CMOS invertor driving interconnect. Alpha-power law MOS model is used to model the CMOS inverter and analytically extract the response of interconnect and is compared to SPICE simulated results.

Chapter 5 compares the performance in terms of propagation delay and power dissipation of MWCNT with copper at global lengths of interconnect. Also the performance analysis on the basis of delay and power is carried out for different tube diameters at global length. Finally the performance comparison based on delay and power dissipation between MWCNT and optical interconnect is carried out for global lengths.

Chapter 6 gives the conclusion and future scope of this dissertation.

CHAPTER

2

Literature Survey

2.1 Introduction

With the advent of scaling the effect of interconnect lines is becoming significant on the overall performance of integrated circuits. Increasing die size and increasing chip densities makes long interconnects lines and dense packaging common in VLSI chips. As the feature size of device reduces, it is required to scale the interconnect dimensions as well. Various delay models for interconnects have been developed for accurately analysing them. For long interconnects, repeaters are required to make the delay linear with length and to mitigate the effect of resistance, inductance and capacitance. Performance of various repeater configuration have been analysed and compared. Repeater models for mathematical analysis and prediction of repeater response have been developed. Study of carbon nanotubes and their various parameters has been done to analyse their potential for future VLSI applications. Equivalent circuit models have been developed to accurately analyse the impedance parameters related to CNTs. Also, study of CNTs as VLSI interconnects for different technology nodes at global, semi-global and local lengths has been done. Performance of CNT based interconnect has been compared with that of copper and other interconnects at different levels of interconnect.

2.2 Interconnect delay model

The transmission-line effects play a significant role in defining the interconnect delays and system performance as the feature size decreases to the submicron dimension [2]. Several techniques have been suggested for the delay analysis of interconnects. An interconnect line may be modelled in different ways in order to find analytical expressions for the propagation delay and the output waveform shape. Adler and E. G. Friedman [3] utilized Elmore [4] delay model to derive an expression for the propagation delay when a load is modelled simply by a resistor in series with a capacitor (RC model). Elmore delay approximation signifies the first moment of the transfer function. Elmore's expression approximates the mid-point of the *monotonic step response* waveform by the mean of the impulse response as [3]:

$$\tau_{Di} = \int_0^\infty t.v(t)dt \quad (2.1)$$

For the general topology of this *RC* tree network, this formula can be modified as [3]:

$$\tau_{Di} = \sum_{j=1}^{N} C_j \sum_{for\ all\ k \in j} R_k \quad (2.2),$$

which is the Elmore delay at node *i* of this *RC* tree, which has the following path definitions:

- P_i denotes the unique path from the input node to node *i*, *i* = 1,2,3, ... , N.
- $P_{ij} = P_i \cap P_j$ denotes the portion of the path between the input and the node *i*, which is common to the path between the input and node *j*.

The limitation of Elmore delay is that it cannot accurately estimate the delay for RLC interconnects, i.e. interconnects in which inductive impedance cannot be ignored (Kahng and Muddu, 1996[5]). This is chiefly due to the fact that the Elmore delay does not cover non-monotonic responses which can occur in RLC circuits. This impreciseness of Elmore delay is critical to current performance-driven routing methods which try to optimize interconnect section lengths and widths as well as driver and buffer sizes. In Friedman's model, the driving transistor was always considered to operate in linear mode and only the simplified case of step input was studied. Pillage *et al.* [6] replaced the RC output load by an "effective" capacitance, which was calculated by in iteration procedure based on simplified assumptions for the shape of the output response. The real output waveform was approximated by the charging/discharging of the net effective capacitance up to a certain point and capturing of the remaining portion of the output response is achieved by a simple resistive model. Sakurai [7] suggested the response and delay calculation for the distributed RC line. He used the Heaviside expression over the poles of the transfer function to calculate the time-domain response from the transfer function. Then he used a single pole to approximate the response and observed the variation of delay with respect to load and source parameters. His heuristic delay formula is nearly identical to the Elmore delay equation. Therefore, it buffers of the same constraints related to Elmore delay model mentioned above. Krauter *et al.* [8] proposed the use of higher order moments to improve the Elmore delay model; this work led to an empirical net delay model equal to the sum of the first moment (M 1) and its standard deviation $\sqrt{|M_1^2 - M_2|}$. Kahng *et al.* [9] used this delay model only to realize that it is not accurate for several source and load parameters. In another approach proposed by Dartu, Menezes, Pileggi [10], a time-varying Thevenin equivalent model is used for the approximation of the gate delays. They replaced the gate by an equivalent circuit model consisting of a linear voltage source and a linear resistor with their values determined using empirical factors, leading to a reduction in

accuracy. In case the output load is not purely capacitive, an effective capacitance for the RC load is used. RC models are highly inaccurate mostly because they are based on basic assumptions for the transistor operation and use simple load models for the representing the interconnect lines. Kahng *et al.* [9]) obtained a good and simple approximation of an interconnect line and studied various combinations of first and second moments, from which they incorporated inductance effects while assuming step input when developing their first delay analytical model of RLC interconnects. The developed solutions showed that their proposed analytical delay model estimates are within 15% of the SPICE delays while Elmore delay [4] estimates can vary as much as 50% from the SPICE-computed delays. Also, they found that when a π-model is used, RLC model achieves an accuracy better than 3% in delay calculations, which the L-model achieves in 100 segments. For this reason, π-model is often used in SPICE simulations instead of large number of segments as a rational approximation of distributed RC. Sakurai [7], made the first attempt to model the interconnect line by a π-circuit, however the driving transistor was replaced by a simple resistor. Ismail and Friedman [11] introduced a simple controllable delay formula for RLC trees. They tried to preserve the useful characteristics of the Elmore delay model while maintaining the same accuracy characteristics. This delay model with the closed-form expressions considers all damping conditions of an RLC circuit including the under damped response, which was not considered by the Elmore delay due to the non-monotonic nature of the response. They have given an empirical relationship for the propagation delay of a CMOS gate driving a distributed resistive inductive capacitive load, which gives an error within 5 percent of AS/X simulations. These solutions are presented for the 50% delay, rise time, overshoots and settling time of signals in an RLC tree. Errors in propagation delay over 35% and use of larger area results of neglecting inductance in on-chip interconnects. The CMOS devices are modelled as discrete RC components.

2.3 Repeaters for long interconnects

For delay minimization, there is need for effective driver circuits that can discharge capacitances with sufficient speed to compensate for the increase in load in VLSI circuits especially due to large fan-outs and the long interconnects. Repeater is used to minimize the interconnect response time by mitigating the effect of resistance and capacitance (Bakoglu [1]). To optimally drive resistive-capacitive interconnect to reduce the delay Bakoglu and Meindl [12] proposed various types of repeaters viz. uniform, cascaded and cascaded tapered repeaters. They utilized Elmore approach to evaluate delay in interconnections with repeaters inserted in between. They have shown that delay of interconnect with repeaters inserted in between

becomes a linear function of line length. They have modelled MOSFETs as discrete resistance and capacitance depending upon the geometric dimensions. For the cascaded buffer, they derived the optimum value of tapering factor to be "e" the base of natural logarithm. However, this method is useful both for capacitive loads and when interconnect resistance is small and driver resistance is dominant but it is not adequate when interconnect resistance is comparable to or larger than driver resistance. Decoupling of a large capacitance from the critical path in order to minimize the total overall delay of the critical path is another important advantage of inserting repeaters within interconnect tree. Venkutesan, Davis and Meindl [13] presented novel compact expressions for:

(1) Time delay
(2) Peak crosstalk for coupled lines
(3) Optimum number and size of repeaters
(4) Time delay for repeater-inserted distributed RC and RLC lines.

For practical ranges of line parameters, the maximum error for time delay and crosstalk, and SPICE simulations are 2% and 10% respectively. These expressions that describe rigorously derived the transient response of a high-speed interconnect with on-chip global interconnect boundary conditions in a series of four papers [13-16]. Simplified expressions enable physical insight and accurate estimation of transient response, time delay, and overshoot for high-speed global interconnects with the inductance included. The CMOS inverter is the simplest buffer or repeater in VLSI interconnects. Sakurai and Newton [17] gave alpha-power MOS model for current voltage characteristics for short channel MOSFETs. They included the effect of slope of input slope and parasitic drain/source resistance effects. They showed that in short channel CMOS inverter, the delay becomes less sensitive to the slope of input waveform and to the variation in power supply voltage as compared to the MOSFET based on Shockley's square law model. Adler and Friedman [3] performed repeater design to reduce both delay and power in interconnects using α-power law model for short channel devices and the current voltage characteristics of MOSFETs. They stated that uniform repeaters outperform tapered buffers and tapered buffer repeaters when driving even relatively low RC loads. They demonstrated that 4 percent decrease in input to output delay can be traded off for a 40 percent saving in area and 15 percent saving in power. Chatzigeorgiou and Nikolaidis [18] modelled the propagation delay and short circuit power dissipation by single equivalent transistor aboriginal of complex CMOS gates using the α-power law MOS model. It was found that the

execution speed of their method was 70 times faster than SPICE simulation for 0.5μm technology and 300 times faster compared to SPICE for a 0.35μm technology. Kaushik, *et al.* [19] presented an analytical method with emphasis on the short-circuit power dissipation for an inverter driving π-LC load with impressive accuracy.

2.4 CNT as future interconnect

F. Kreupl *et al.* [20] showed that carbon nanotubes are much less susceptible to electro migration (EM) problems that plague the copper interconnects due to the strong sp^2 bonding (like graphite) and thus they can carry very high current densities without getting damaged. Metallic single walled CNT bundles are able to carry extremely high current densities of the order of $10^9/cm^2$ while Cu interconnects have a current carrying capacity of $10^6 A/cm^2$ due to M effect. A single-wall nanotube results in a very high contact resistance and high characteristic impedance, and hence a bundle of closely packed parallel CNTs is preferably used above a ground plane, as proposed by F. Kreupl *et al.* [20] and J. Li *et al.* [21]. Srivastava *et al.* [22], [23], Li *et al.* [21], [24] and Massoud, *et al.* [25] compared the performance in terms of propagation delay of the CNT bundle interconnect and copper interconnect for local, semi-global and global interconnects. Results show that the performance of CNT bundle interconnect improves over copper as the line length increases for different levels of interconnects. The pitch influences semi global and global relative performance of CNT as it does in case of local lengths as reported by K. Banerjee and N. Srivastava [23]. For the local interconnects, the influence of pitch on delay of CNT bundle is considerable. It can be summarized that the ratio of CNT bundle to Cu interconnect propagation delay is increased when the pitch increases. Li *et. al.* [26] proposed to use large migration tolerant bundles of CNTs as vias to get sufficient current for ultra-large-scale integrated (ULSI) interconnections. They suggest that there is no visible degradation of the via current with time and that the total resistance of the CNT bundle via is about three orders of magnitude lesser than that of a single CNT. CNT bundle vias are expected to effectively replace copper vias for future ULSI interconnections. Thiruvenkatesan *et al.* [27] studied the effects of copper interconnect and carbon nanotube interconnect using a carry-save-adder-array multiplier. The performance of critical delay with respect to device technology is presented and it showed that the delay ratio of CNT bundle to that of Cu wire reaches its minimum for CNT in the semi-global level.

Vivo *et al.* [28] described a new model based on Multi Walled CNTs, suitable for the 32 and 22 nm technology, where they evaluated the upper and lower confines of the time-delay due to the variations of some of the physical and dimensional characteristics of a nano

interconnects. The results are compared with those of scaled down copper-based structures, indicating that the CNT interconnect has better performance. Mayank Kumar Rai and Sankar Sarkar [29] addressed the influence of tube diameter on single walled carbon nanotube (CNT) bundle interconnect delay and power output in VLSI application. They found that single-walled carbon nanotube (SWCNT) bundle interconnects are of lower delay than copper interconnect due to low resistance and inductance. Power dissipation decreases with increase in tube diameter of the constituent SWCNT. Resistance and inductance of CNT increases with increase in tube diameter. On the other hand, with increase in tube diameter interconnect capacitance decreases. There is a trade-off between delay and power dependence on tube diameter. S. Sarkar *et al.* [30] show that CNT shows better relative performance for longer interconnects in 32 nm and 22 nm nodes. They have reviewed all the possible parameters to explore the applicability of CNTs as future interconnects. Thus, as technology nodes shrink in the future, CNT has become the most prospective material of future.

Kaustav Banerjee *et al.* [31] presented a compact equivalent circuit model of MWCNTs for the first time and compare the performance of MWCNT with SWCNT and copper interconnects at all interconnect levels. A comparison of resistivity among MWCNTs with various diameters, Cu wires with different dimensions, and SWCNT bundles with different chirality is shown. It is shown that at intermediate and global levels the MWCNT interconnects can achieve smaller signal delay than copper interconnects and it improves with technology scaling and increasing line length. It is also shown that SWCNT can surpass the performance of MWCNT if highly dense and high metallic-fraction bundles of SWCNT are used.

Azad Naeemi *et al.* [32], derived compact physical models for conductivity of MWCNT interconnects and show that for MWCNTs shorter than the critical length, the conductivity decreases as diameter increases, whereas for MWCNTs longer than the critical length, conductivity increases with increase in diameter. For long lengths, MWCNTs can have conductivities significantly larger than that of copper or even SWCNT bundles. However, for short lengths, SWCNT bundles have more than two times higher conductivities compared to MWCNTs.

Azad Naeemi and James D. Meindl [33], presented equivalent circuit models for the resistance of single and multi-wall carbon nanotubes that include various electron–phonon scattering mechanisms as well as changes in the number of conduction channels as a function of temperature. For single and few-wall nanotubes, the temperature coefficient of resistance (TCR) is always positive and increases with length. It reaches $1/(T - 200\ K)$ for lengths much

larger than the electron mean free path. For MWCNs with large diameters (>20 nm), TCR varies from $-1/T$to$+0.66/(T-200\ K)$ as the length varies from zero to very large values.
Yehia Massoud *et al.* [34], developed an equivalent RC circuit model for MWCNT interconnect that captures both DC conductance and high frequency impedance due to capacitive effects and find that MWCNT-based interconnect can have substantially less delay than copper wires in global interconnect applications.

Ashok Srivastava *et al.* [35], proposed a circuit model of the MWCNT based on one dimensional fluid model, which describes the electron transport in SWCNT. The performances of MWCNT and SWCNT in high frequency (RF/microwave) applications are then simulated using these models and compared with performance of Copper interconnect which show that MWCNT interconnects can have higher transmission efficiency and lower reflection losses than that of SWCNTs and Copper interconnects.

Manoj Kumar Majumder *et al.* [36], compared the area for equivalent number of SWCNTs in bundle and shells in MWCNTs. For same propagation delay performance, the area occupied by SWCNT bundle is more than the MWCNTs for a specified interconnect length.

H. J. Li *et al.* [37], studied the electric transport properties of an individual vertical MWCNT *in situ* at room temperature in a scanning electron microscope chamber and found that the single MWCNT has a large current-carrying capacity and the maximum current can reach 7.27 mA and a very low resistance of about 34.4Ω and a high conductance of about $(460–490)G_0$ was obtained which implied a multichannel quasi-ballistic conducting behaviour occurring in the MWCNTs with large diameter, which can be credited to the participation of multiple walls in electrical transport and the large diameter of the MWCNTs.

Maria Sabrina Sarto *et al.* [38], derived the equivalent single-conductor model of a MWCNT interconnect from the rigorous formulation of the complex multiconductor transmission-line propagation equations analytically and a new accurate approximated expression of the equivalent quantum capacitance is proposed. The proposed model is solved in both the frequency and time domains.

Sankar Sarkar *et al.* [39], analysed the effect of driver size and number of shells on propagation delay for MWCNT interconnects at 22 nm technology node using an equivalent circuit model of MWCNT for estimation and analysis. The delay through MWCNT is compared with through that of copper interconnects for various driver sizes and different number of MWCNT shells. It is observed that the delay ratio of MWCNT to copper decreases with increase in length for different and the number of shells. Also, the delay ratio increases with reduction in number of shells.

Krishna C. *et al.* [40], compared CNT and Optical interconnects with copper interconnects at different levels. It is found that at local level, CNT bundles have smaller latency than copper for a given geometry, which can be further improved by optimizing its geometry. At semi-global level, optical interconnects have the lowest latency and highest possible bandwidth density using WDM while CNT has better latency than copper. At high switching activity optical interconnects are highly power efficient while for lower activity they are so only up to a critical value. At switching activity less than 20% and low bandwidth, CNT is most efficient.

2.5 Conclusion

With technology advancement various researchers have worked on different fields related to interconnect. As the feature size keeps reducing, older models of interconnect delay become inefficient and less accurate and new models have been developed. New repeater insertion techniques and repeater models are developed over the years for keeping up with the scaling. Recent research in the area of interconnect materials shows that the CNT proves the promising alternative of copper in deep sub-micron technology nodes.

CHAPTER

3

Carbon Nanotube as VLSI interconnect

3.1 Introduction

With technology scaling into the deep sub-micron level, the channel length of the device decreases to tens of nanometres [41]. At this resolution, the die size and device density of the circuit increases rapidly. This increase makes the requirement for long interconnects a must in VLSI chips. Long interconnects lead to increase in propagation delay of the signal. The area required for the device (MOSFET) has reduced to such an extent that it is insignificant when compared to the surface area required for interconnect, vias and contact routing. This makes the modern VLSI chips more interconnect limited as they have started to dominate on some of the most relevant factors of the digital integrated circuits such as reliability, speed and energy consumption. Therefore, a precise and deep analysis of the behaviour of interconnect is very essential in designing of the VLSI chip. Accurate modelling of on-chip wiring which includes all the parasitic-induced delays and stray coupling is essential to the circuit designer. The parasitic effects increase as the technology is going in deep sub-micron level because of the increase in die size and interconnect lengths along with increasing speed of the chips. Interconnects are predicted to be responsible for 70-80% of the signal delay in high-speed systems. This delay has to be accounted for during the designing process of the chip, failing to which can lead to logic glitches in digital circuits and distortions in analog circuits, ultimately leading to failure of the circuit. Hence it is extremely important for the designers to include the interconnect sub circuitry during the simulation process as efficiently as possible.

3.2 Problems with existing materials of VLSI interconnect

Scaling of technology over the years has led to increase in device density, ultimately leading to increase in interconnect current density. Initially aluminium was used as a material for interconnects. The advantages of aluminium as interconnect are as follows [42].

1. Good ohmic contact with silicon.
2. Good adherence on silicon dioxide.
3. Good conductivity.

As the interconnect current density increased over the years, aluminium seemed to fail in providing good performance. Apparently as the interconnect density increases, electro migration takes place in aluminium.

Copper is a good substitute for aluminium due to its higher conductivity and higher resistance to electro migration. The melting point of copper is higher than that of aluminium providing copper with higher thermal stability. Copper can withstand five times more current density than aluminium while providing the same performance [43]. Due to these advantages copper is a good choice for interconnect material for sub-micron and deep sub-micron high performance chips. As the technology is further scaled, the cross-sectional area of copper interconnects decreases appreciably due to which effects like surface roughness and grain boundary scattering become significant leading to increased resistivity. This causes increase in propagation delay, power dissipation and electro migration [30, 43].
The problems which arise with scaling down of feature size are discussed.

1. **Electro migration:** Electro migration is caused by the gradual movement of ions in a conductor due to the due to the transfer of momentum between the conducting electrons and the diffusing metal atoms. It can eventually lead to loss of connection or circuit failure. The resistivity of copper to electro migration is high. Continuous scaling can lead to high current densities. Under such conditions, interconnects can experience electrical failure due to electro migration.

2. **Grain boundary effect:** Grain boundaries are the internal interfaces that separate neighbouring disoriented single crystals in a polycrystalline solid [44]. The interface between two grains, or crystallites, which are disoriented with respect to each other in a polycrystalline material is called a grain boundary. Grain boundary areas contain the atoms that have been perturbed from their original lattice sites, dislocations and impurities that have migrated to lower energy grain boundary. Grain boundaries are defects in the crystal structure which tends to decrease the electrical and thermal conductivity of the material. Copper has a crystalline structure normally, but when it is engineered for use it becomes polycrystalline in nature. This new structure is made up of many small single crystals having different orientation with respect to each other. Grain boundary causes scattering of electrons leading to reduction in mobility of electrons. The resistance of such conductor is inversely proportional to the size of grains. The smaller the grains, the larger will be the resistance and electrons would travel slowly.

3. **Surface scattering:** As the wire dimensions are decreasing, the electron mean free path becomes comparable to the wire dimensions causing scattering from the interface. The mobility of electrons decreases as the dimensions decrease. The mathematical expression that governs the scattering theory leads up to the following expression for surface-scattering-dependent resistivity [44].

$$\frac{\rho_s}{\rho_o} = 1 + \frac{3}{4}(1-p)\frac{l}{d} \tag{3.1}$$

Figure 3.1 Surface scattering [45].

Here p is the fraction of electrons scattered specularly at the surface, l is the mean free path of electron, d is the wire width. It can be observed that an increase in scattered electron or a decrease in wire width increases the resistivity and hence the resistance of copper.

4. **Diffusion Barrier Width:** Copper diffuses into neighbouring dielectric silicon as it is very mobile in SiO_2. This causes contamination of silicon devices and damage in FETs. To prevent this, copper wires are surrounded by a diffusion barrier. Due to the high resistivity of this diffusion barrier, the effective resistivity of the copper wire increases. With the scaling of technology, the cross sectional area of copper wire decreases, but due to reliability constraints the diffusion barrier does not scales as rapidly.

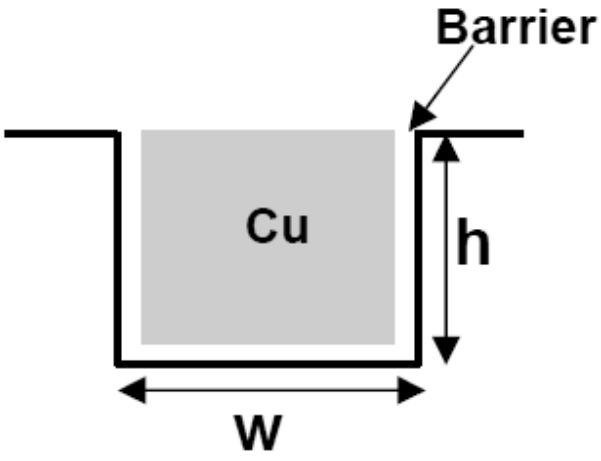

Figure 3.2 Cross-sectional view of interconnect showing barrier deposited [44].

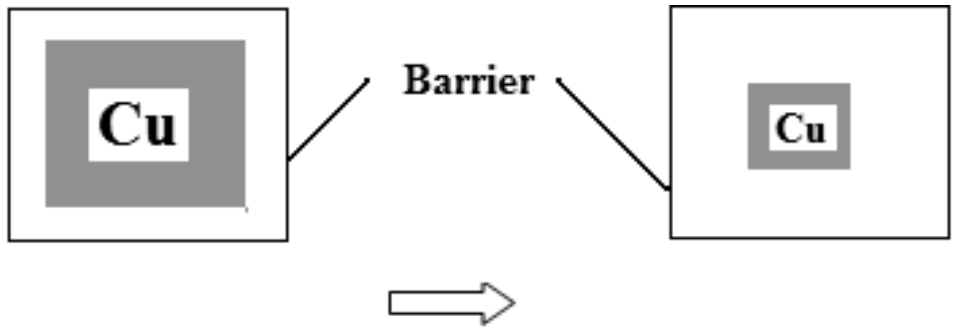

Figure 3.3 Variation in barrier width with scaling of interconnect [44].

This gradually leads to larger fraction of the cross sectional area being occupied by the diffusion barrier. This ultimately leads to an increase in the resistivity of wire.

3.3 Interconnect

Interconnects are basically conducting wires used for electrically connecting the components on chip. A VLSI interconnect is a thin film of conducting material that provides electrical connection between two or more nodes of the circuit/system formed in the silicon chip [30]. Basically all the interconnections among transistors of a chip are made using interconnects. In deep submicron technology, interconnect plays an important role in determining the performance of the circuit. The associated impedance parameters, i.e. inductance and capacitance affect the performance of interconnect at this technology. As feature size in decreasing along with the scaling down of the supply voltage and threshold voltage, the interconnect dimensions must also be reduced to gain full advantage of the scaling. With scaling, the chip density in increasing and so is the interconnect density. Due to this compact packing there is interference between nearby interconnects due to coupling effect.

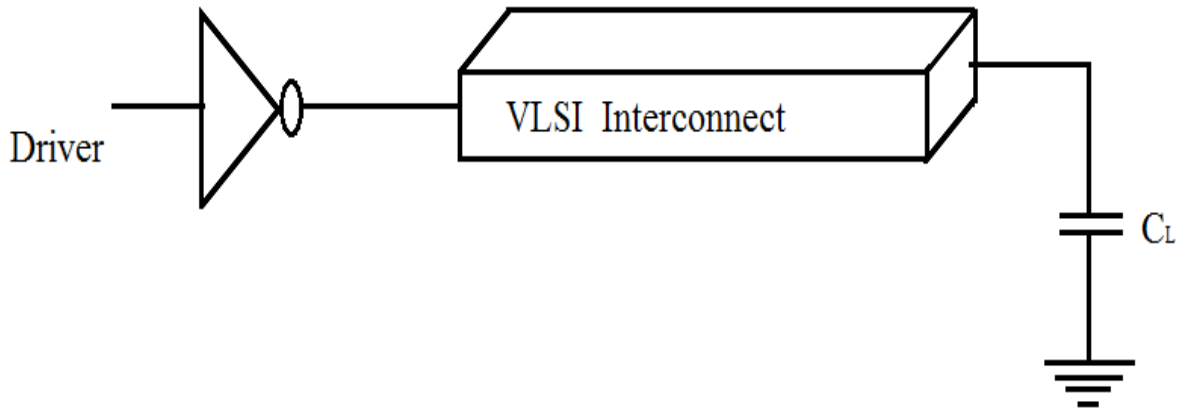

Figure 3.4 A VLSI interconnect with a driver and a load.

3.4 Types of interconnects

Interconnects are categorized on the basis of their length as local, semi-global and global.

Local interconnects: These interconnects are lowest level of interconnects. These are used in localized region of a chip to provide electrical path between nearby nodes. They commonly connect gates, sources and drains in MOSFETs. In MOSFET technology, polycrystalline silicon, a local interconnect, also serves as gate electrode material. Silicidal drain, source and gate regions also serve as local interconnects [46].

Semi-global interconnects: These interconnects are used for conducting nodes which are at distances more than those of local interconnects but lesser than those of global interconnects. These are usually used to connect devices within a block.

Global interconnects: These interconnects are used for connecting nodes which are at considerable distance from each other. These usually connect between blocks which include power, ground and clocks. These often travel large distances between different devices and through different parts of the circuit.

Ohmic contacts are used to connect interconnect with active regions and with devices in the silicon substrate. Silicon dioxide layer, a high resistivity dielectric, is usually used to separate the active regions and first level global interconnects. Electric contact is made between interconnect and the active region through openings in the dielectric layer. Simultaneously during processing, contacts may be made between the first level of global interconnects and the local interconnects, as the same dielectric layer separates them. The dielectric layer separating one global level interconnect level from another is called inter level dielectric (ILD).

3.5 Delay analysis

Designers for high speed applications are constantly driven by the motivation to have high clock speeds while simultaneously reducing the cross section of the lines as well as packing them together. Reducing the wire cross section results in considerable resistive lines. Based upon the factors such as clock speed, signal rise and fall time, nature of the structure, etc. interconnects can be modelled as lumped (RC or RLC), distributed (frequency independent/dependent RLCG parameters, coupled, lossy), full-wave models or measured linear sub-networks.

In the past, interconnect models were generally restricted to ***RC tree networks***. RC tree networks are RC circuits with no floating capacitors, capacitors from all nodes to ground and

no resistors to ground. The signal delay was estimated by using Elmore delay through RC network which provided a dominant time constant approximation for monotonic step responses [47].

At higher operating frequencies, the electrical length of interconnect becomes a significant fraction of the operating wavelength of the signal wavelength due to which signal-distorting effects arise unlike at low frequencies [2]. Consequently, the conventional lumped impedance interconnect model becomes insufficient and transmission line models are required. At higher frequency range, inductance starts to come into effect and lumped RC model becomes inadequate. An ***RLC*** model has to be espoused [8].

Unfortunately, the Elmore delay model is incapable of accurately estimating the delay of RLC interconnect lines and trees [47]. This is mainly due to the fact that Elmore delay does not cover non-monotonic responses which may occur in RLC circuits [5]. Over the time various closed-form analytical expressions for delay prediction of RLC trees were proposed, viz, Sakurai Delay model [47], Kahng and Muddu delay model [5], Ismail *et. al.* analytical delay model [47] and Meindl *et. al.* delay model [13-16]. Some other variations of the delay models are also present.

3.6 Methods for improving Interconnect delay

It is impossible to grow millions of transistors on a chip using only one level of copper interconnects. Moreover, copper itself would introduce excessive delay when chips get larger and minimum cross section area is reduced.

Multilayers of interconnects are partial solution to this problem. Layers of copper in horizontal and vertical directions interconnected through vias between the levels enable global communication without the need of polysilicon or diffusion wires. Also the cross sectional area of the upper layer interconnects can be optimized to reduce their RC constants. This also reduces the chip area as much of the chip area is occupied by interconnects [1].

Repeaters are recurrently inserted to minimize the response time of interconnect by mitigating the effect of capacitance and resistance. Repeaters divide the interconnection into smaller subsections, making the time delay linear with length [12]. Various models of interconnect delay estimation for repeater inserted RLC interconnect lines have been derived by researcher [3, 17, 48].

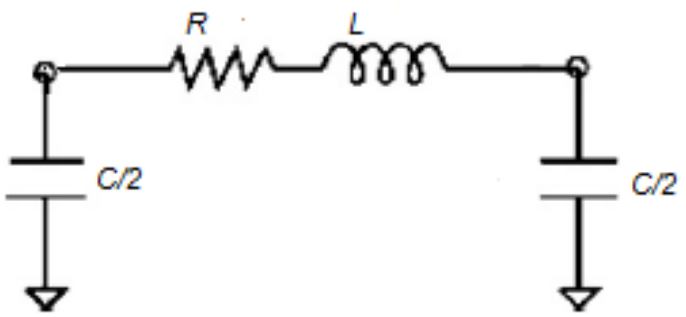

Figure 3.5 RLC interconnect model [2].

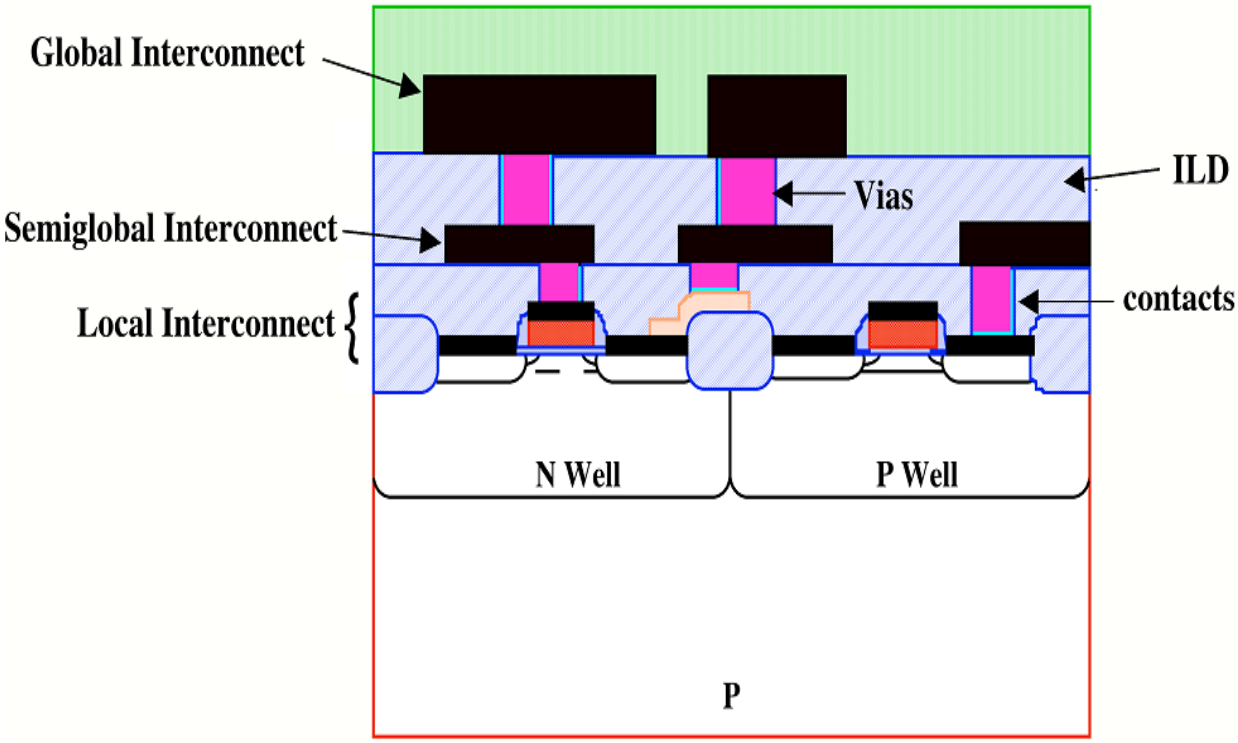

Figure 3.6 Levels of interconnect [46].

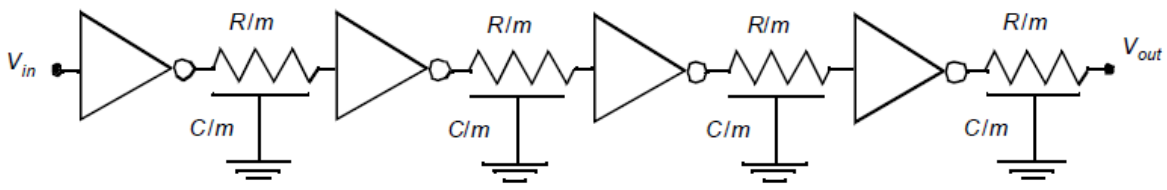

Figure 3.7 Distributed RC network with repeaters inserted [12].

3.7 Factors affecting Interconnect delay

There are various factors defining the shape and structure that affect the performance of interconnect in terms of power and delay. Replacing aluminium with copper and silicon dioxide

with low dielectric constant (low k) materials can reduce interconnect delay. Although low k materials have increasing current densities which makes them more prone to dielectric breakdown [49].

There is a trend to increase the line width in order to improve signal speed, which leads to smaller pitch due to reduction of spacing between two lines [50]. This in turn leads to a continuous increase in the capacitance and resistance, thus contradicting the improvement in interconnect delays, even causing higher RC delays.

In deep submicron technology, designers prefer high aspect ratio (ratio of interconnect thickness to width) as it decreases the inter-line capacitance. The adverse effect is that as the aspect ratio increases, the two dimensional fringing fields and capacitances between nearby lines becomes considerable and after a certain point there are no advantages of increasing aspect ratio [49].

3.8 Interconnect Parasitics

There are three types of parasitic effects which arise in interconnect, resistive, capacitive and inductive. These three influence the signal integrity and degrade the performance of the circuit. The basic geometry of interconnect is shown in Fig. 3.8.

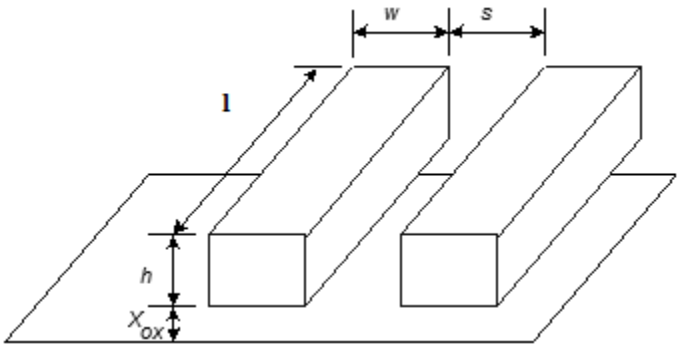

Figure 3.8 Basic Geometry of interconnect over the ground plane.

It is representing interconnect line that has a length *l*, width *w* and height *h*. It is at a height X_{ox} from the ground plane.

Line resistance

The resistance of the line from one end to other end is calculated by using the standard equation.

$$R = \frac{\rho l}{A} = \frac{\rho}{h}\left(\frac{l}{w}\right) = R_s\left(\frac{l}{w}\right) \tag{3.2}$$

Here ρ is the resistivity of the material, *A* is the cross sectional area of interconnect and *l* is the length of interconnect. Metals are used as interconnect materials due to their small resistivity.

A more useful expression for line resistance for use in chip design is based on sheet resistance having units of ohms for the layer. It is defined by:

$$R_s = \frac{\rho}{h} \tag{3.3}$$

It is the end to end resistance of a square section of material with *d*=*w* seen from the top. The sheet resistance is useful as it can be easily measured in a laboratory on a test structure. Once the value of *Rs* is calculated, then the total resistance of a line with width *w* and span *d* is given by:

$$R = R_s n \tag{3.4},$$

where *n=1/w* is the number of squares of dimensions *w*x*w* through which the current flows.

Line capacitance

The capacitance acts as a limiting factor during high speed signal transmission in interconnect. The cross sectional geometry of interconnect over ground plane is shown in Fig. 3.10.

The total capacitance of the line is given by:

$$c_{int} = c'L \tag{3.5}$$

Here,

$$c' = \frac{\varepsilon_{dielectric} W}{X_{OX}} \tag{3.6}$$

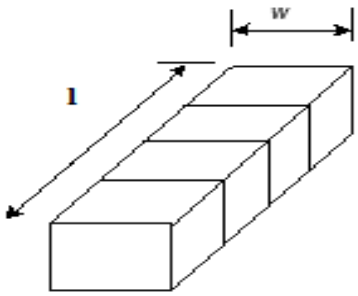

Figure 3.9 Line divided into sections for calculation of line resistance.

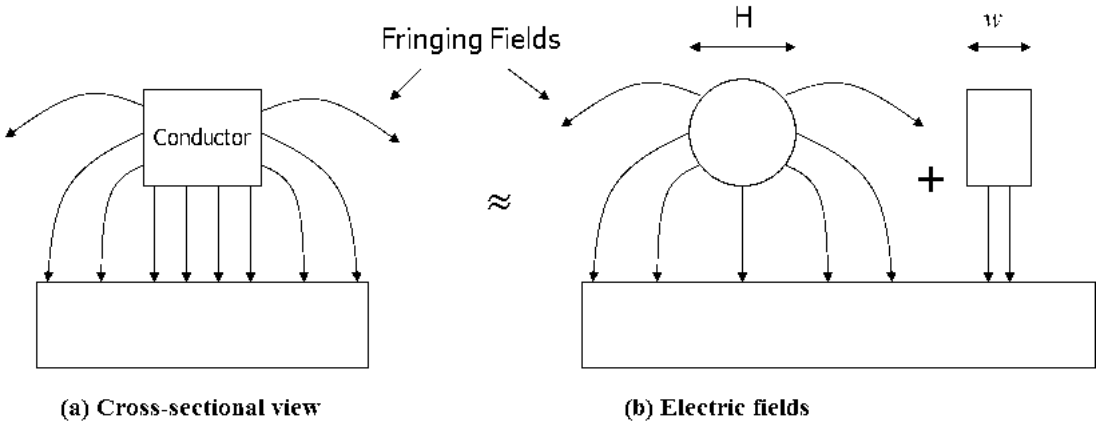

Figure 3.10 Interconnect capacitance (a) shows C_{pp} (b) shows effect of C_{fringe} [41].

However this formula ignores the presence of fringing fields at the edges. A more accurate expression is:

$$c_{wire} = c_{pp} + c_{fringe} = \frac{\varepsilon_{dielectric}}{X_{OX}} w + \frac{2\pi\varepsilon_{dielectric}}{\log\left(\frac{X_{OX}}{h}\right)} \quad (3.7),$$

where c_{pp} is the parallel plate capacitance and c_{fringe} is the fringing field capacitance.

Line inductance

In high speed applications, as we move towards clock frequency of Giga Hertz range, inductance starts to come into effect considerably. The inductance can be calculated from its definition as:

$$\Delta V = L\frac{di}{dt} \quad (3.8)$$

In high performance VLSI design methodologies, the importance of inductance increases as the technologies scale. It is essential to include inductance in the impedance model when implementing repeaters to drive RLC trees in high speed.

3.9 Interconnect models

Interconnect models are electrical models used to estimate the real behaviour of the wire as a function of its parameters in order to study the parasitic effects in interconnect. These models may be very simple or very complex depending upon the various effects that are being included and the accuracy required from the model.

3.9.1 Lumped model

Even though the circuit parasitics are distributed over the length of interconnect, for the fast observation of their effects of while looking at limited aspects of the circuit behaviour, it is useful to lump all the different fractions of the parasitics into a single element.

3.9.1(a) Lumped RC model

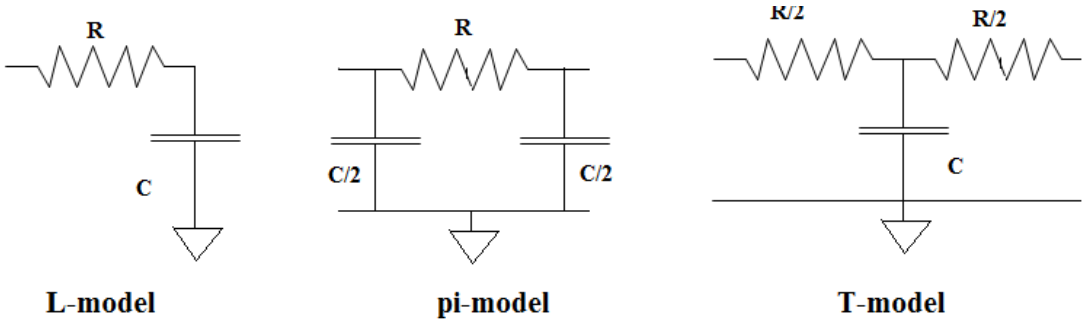

Figure 3.11 Different RC Lumped interconnect model configurations [6].

When the inductive component of interconnect is small and the frequencies are in low to medium range, inductance of the wire may be ignored and only the resistance and capacitance component of the wire may be considered. Thus the model is lumped to RC model. The different configurations of RC interconnect model are shown in Fig. 3.11. The pi model makes a good approximation of the interconnect line achieving better accuracy in estimating the output waveform and delay calculations.

3.9.1(b) Lumped RLC model

With the use of low resistive materials and as we move towards Giga Hertz frequency range, inductance starts to come into effect considerably. Thus the component of inductance cannot be ignored and the lumped RC model becomes inadequate. A model which has resistive, capacitive as well as inductive effect has to be adopted. The RLC model is shown.

3.9.2 Distributed RC line

The lumped RC model is not useful when considering all the aspects of circuit behaviour as it is highly inaccurate. A distributed RC model is more appropriate for a RC line. The distributed RC line can be shown by a multi-stage RC ladder network. The individual elements can be defined by:

$$R_N = \frac{R}{N} \quad and \quad C_N = \frac{C}{N} \tag{3.9}$$

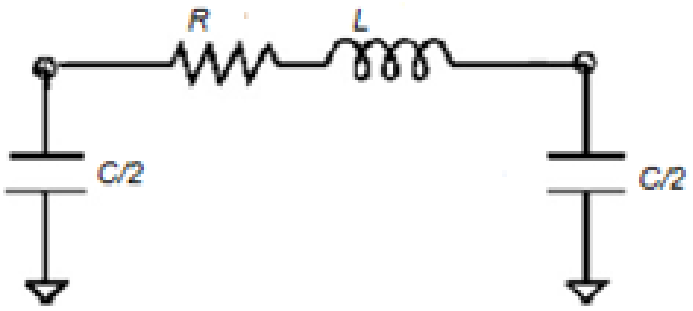

Figure 3.12 Lumped RLC interconnect model [2].

The distributed RC ladder is observed to show more accurate results. However the increase in nodes results in the increase in circuit simulation time.

3.9.3 Pi model

Fig. 3.13 shows the π-RLC model for interconnect line the equivalent impedance is given by:

$$R_{eq} = \left(R_1 + sL_1 + \frac{1}{sC_2}\right) \| \left(\frac{1}{sC_1}\right) \tag{3.10}$$

Thus the driving point admittance is given by:

$$Y_{eq} = \frac{1}{R_{eq}} \tag{3.11}$$

$$Y_{eq} = sC_1 + \frac{sC_2}{1 + sC_2(R_1 + sL_1)}$$

Expanding the given equation, we get

$$Y_{eq} = s(C_1 + C_2) - s^2R_1C_2^2 + s^3(R_1^2C_2^3 - L_1C_2^2) + \cdots \tag{3.12}$$

Similar to the driving point admittance approximation for the RLC interconnection tree, the entire tree is approximated with an equivalent open-ended RLC line whose impedance parameters are equal to the total respective impedance parameters. The admittance of an open ended RLC line can be expressed as [34]:

$$Y(s) = \frac{tanh\theta}{Z_o} \tag{3.13}$$

Here propagation constant,

$\theta = \sqrt{(R_t + sL_t)sC_t}$ and characteristic impedance, $Z_o = \sqrt{\frac{(R_t+sL_t)}{sC_t}}$.

Thus *Y(s)* can be expressed as:

$$Y(s) = sC_{tot} - \frac{s^2R_{tot}C_{tot}^2}{3} + s^3\left(\frac{2R_{tot}^2C_{tot}^3}{15} - \frac{L_{tot}C_{tot}^2}{3}\right) + \cdots \tag{3.14}$$

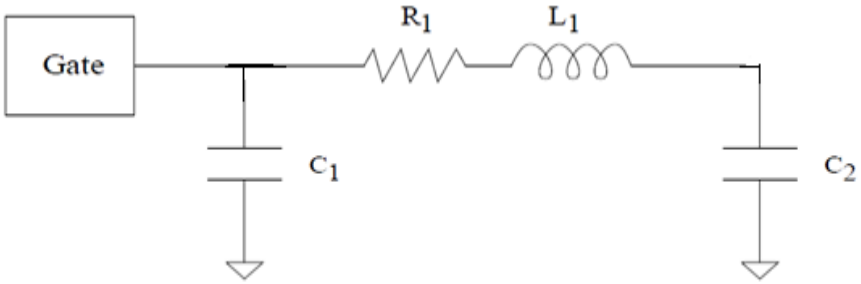

Figure 3.13 π model of interconnect [9].

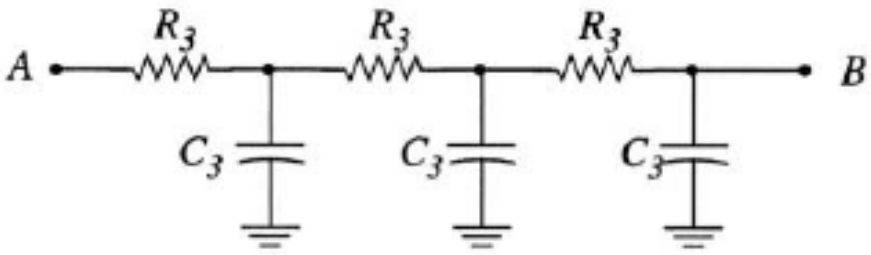

Figure 3.14 Distributed RC line model [9].

The general expression for driving point admittance is given by [57]:

$$Y(s) = \sum_{i=1}^{\infty} A_i s^i$$

$$Y(s) = sA_1 + s^2A_2 + s^3A_3 \ldots \tag{3.15}$$

Comparing the eqns. 3.12 and 3.15, we get

$$A_1 = C_1 + C_2, A_2 = -R_1C_2^2, A_3 = R_1^2C_2^3 \tag{3.16}$$

The inductance components of the π-model are obtained by matching the inductive terms in the third moment of driving point admittance. The values of R_1, C_1 *and* C_2 can be obtained as:

$$R_1 = -\frac{A_3^2}{A_2^3}, \quad C_1 = A_1 - \frac{A_2^2}{A_3}, \quad C_2 = \frac{A_2^2}{A_3} \tag{3.17}$$

Putting the values of A_1, A_2 *and* A_3 in eqn 3.12, the values of impedance parameters can be found as given below.

$$R_1 = \frac{12}{25}R_{tot}, \quad L_1 = \frac{12}{25}L_{tot}, \quad C_1 = \frac{1}{6}C_{tot}, \quad C_2 = \frac{5}{6}C_{tot} \tag{3.18}$$

The resultant π-model is as shown in Fig. 3.15

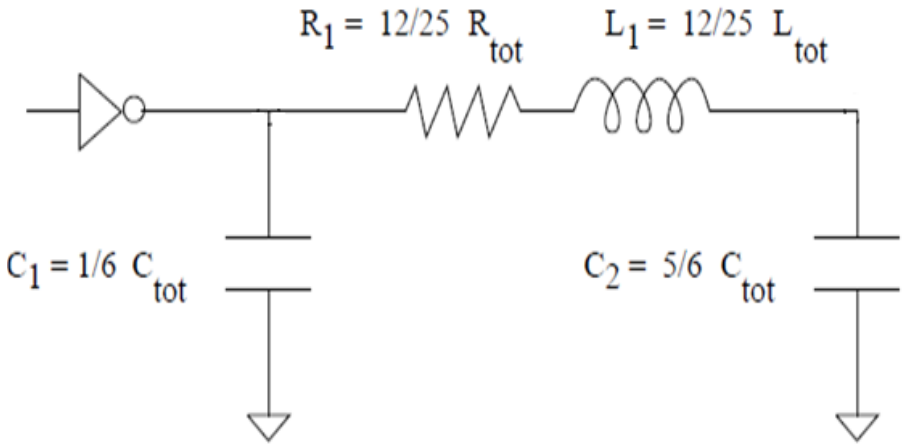

Figure 3.15 RLC π model for interconnect [9].

3.9.4 Repeater model

Bakoglu and Meindl expressed the propagation delay through interconnect with *k* minimum-size invertors as [12]:

$$T = k\left[0.7\frac{R_o}{h}\left(\frac{C_{int}}{k} + hC_o\right) + \frac{R_{int}}{k}\left(0.4\frac{C_{int}}{k} + 0.7hC_o\right)\right] \tag{3.19}$$

Here C_o and R_o are the input capacitance and output resistance of the invertor. The aspect ratios of invertors are increased by a factor of h to improve the propagation delay. The optimum number of repeaters k required to minimize the net propagation delay is found by setting dT/dK equal to zero.

$$k = \sqrt{\frac{R_{int}C_{int}}{2.3R_oC_o}} \tag{3.20}$$

The optimum value of transistor sizing h is found by setting dT/dh equal to zero.

$$h = \sqrt{\frac{R_oC_{int}}{R_{int}C_o}} \tag{3.21}$$

The optimized delay obtained is formulated as:

$$T = 2.3\sqrt{R_oC_oR_{int}C_{int}} \tag{3.22}$$

3.10 Scaling of interconnect lines and device

The design of high-density VLSI chip requires that the packing density of MOSFETs used in the circuits is as high as possible and thus, that the sizes of the transistors are as small as possible. The reduction in the size of transistors, i.e., the dimensions of the MOSFETs, is commonly known as scaling. The operational characteristics of the MOS transistors are expected to change with the reduction of its dimensions. Some physical limitations eventually restrict the extent of scaling that is practically achievable. Scaling is of two types; *constant-field scaling* and *constant-voltage scaling.* Scaling of MOSFET is concerned with the systematic reduction of overall dimensions of the devices, as allowed by the technology, while preserving the geometric ratios found in larger devices. The proportional scaling of devices results in reduction in the total silicon area occupied by the circuit, thus increasing the overall functional density of the IC. To explain the scaling, a constant *scaling factor S* is introduced (S>1). All the dimension; horizontal and vertical, are then divided by this scaling factor to obtain the scaled device [51].

3.10.1 Constant-field Scaling

In this scaling the magnitude of internal electric fields in the MOSFET is preserved, while the dimensions are scaled down by a factor of *S*. All the potentials must be scaled down proportionally in order to achieve this by the scaling factor. Table 3.2 shows the scaling factors for all the significant dimensions, potentials and doping densities of the MOS transistor. The

power is reduced by S^2, which is one of the most attractive feature of constant-field scaling. The area is also reduced by the same factor [51].

Table 3.1: Effect of Constant-field scaling on key parameters [51]

Quantity	Before Scaling	After Scaling
Channel length	L	L'=L/S
Channel width	W	W'=W/S
Gate oxide thickness	t_{ox}	$t_{ox}'=t_{ox}/S$
Junction depth	x_j	$x_j'=x_j/S$
Power supply voltage	V_{DD}	$V_{DD}'=V_{DD}/S$
Threshold voltage	V_{T0}	$V_{T0'}=V_{T0}/S$
Doping densities	N_A N_B	$N_A'=S.N_A$ $N_B'=S.N_B$
Oxide capacitance	C_{ox}	$C_{ox}'=S.C_{ox}$
Drain current	I_D	$I_D'=I_D/S$
Power dissipation	P	$P'=P/S^2$
Power density	P/Area	P/Area'=P/Area

3.10.2 Constant-Voltage Scaling

The scaling of voltages may not be very practical in all the cases, which is suggested by *constant-field scaling.* The peripherals and interface circuitry may require certain levels of input and output voltages, which would require multiple power supply voltages and complicated level shifter arrangements. For such reasons, *constant-voltage* scaling is usually preferred over *constant-field* scaling.

In *constant-voltage* scaling, all the dimensions of MOSFET are reduced by a factor of *S*, similar to that in full scaling. The power supply voltage and the terminal voltages are kept unchanged. The doping densities are increased by the factor of S^2 in order to preserve the charge-field relations [51]. Table 3.2 shows the *constant-voltage* scaling of main dimensions, voltages and densities.

Table 3.2: Effect of Constant-voltage scaling on key parameters [51]

Quantity	Before Scaling	After Scaling
Dimensions	W,L,t_{ox},x_j	Reduces by S times

Voltages	V_{DD},V_T	Remain unchanged
Doping densities	N_A,N_D	Increase by S^2 times
Oxide capacitance	C_{ox}	C_{ox}'=S.C_{ox}
Drain current	I_D	I_D'=S.I_D
Power dissipation	P	P'=S.P
Power density	P/Area	P'/Area=S^3.(P/Area)

3.10.3 Interconnect Scaling

As the device dimensions are scaled, the interconnection dimensions need also to be reduced. A simple and direct approach to do this is to scale all cross-sectional dimensions, width, length, height, separation (*w,l,h,s*) by the same factor *S* as used for the scaling of the device. The scaling of various dimensions of interconnects are given in table 3.3. As can be seen from the table, the line response and the line drop voltage remains constant after scaling. The current density increases which ultimately may lead to serious device performance problems like electro migration.

Table 3.3: Scaling of local interconnects lines for constant-field

Quantity	**Ideal Scaling**	**Quasi-ideal scaling**	**Constant-R scaling**
Dimensions (w,h,L,s)	1/S	1/S	1/√S
Dimension (h,X_{OX})	1/S	1/√S	1/√S
Line resistance (R)	S	1/√S	1
Line capacitance (C_{int})	1/S	$1/S^{3/2}$	1/S
RC delay	1	1/√S	1/S
Line current density	S	√S	1/S

It can be advantageous to deviate from ideal scaling. Scaling interconnects and field-oxide thickness by factors smaller than *S* lowers the *RC* delay. Two alternative approaches of scaling in order to minimize the propagation delay are presented along with ideal scaling in table. In

"quasi-ideal" scaling of local interconnects, all horizontal dimensions are scaled by the scaling factor *S* to improve the overall packing density by the scaling factor. The vertical dimensions, on the other hand, are reduced only by the factor $\sqrt{S}$. This is done in order to maintain a small *RC* time constant, and thus the delay reduces by the same factor. In case of "constant-R" scaling, all the cross-sectional dimensions are reduced only by the factor $\sqrt{S}$ and thus, propagation delay is reduced by *S*.

Long interconnects are more difficult to scale because of the added load introduced by their increasing chip size. The scaling of various dimensions of interconnect in long-distance interconnects is shown in table 3.4. It is assumed that maximum long-distance or block-to-block interconnection line increases by the factor of S_c. The line response time rises drastically in long-distance interconnects as a result of scaling, a considerable amount of delay and performance of the circuits may suffer from technological advancement.

In *constant-dimension* scaling of long-distance interconnects, all cross-sectional dimensions are held constant, and propagation delay increases by S_c^2 as the chip size grows. In *constant-delay* scaling, the cross-sectional dimensions of long-distance interconnects are increased in such a way that the improvement in *RC* delay per unit length negates the effect of increasing chip size and total delay remains constant.

Table 3.4: Scaling of long interconnects for constant field

Quantity	**Ideal Scaling**	**Constant Dimension**	**Constant Delay**
Dimensions (w,L,h,s,X_{OX})	1/S	1	S_c
Dimensions (L_{max})	S_c	S_c	S_c
Line resistance (R)	S^2. S_c	S_c	1/ S_c
Line capacitance (C_{int})	S_c	S_c	S_c
RC Delay	S^2 .S_c	S_c^2	1

3.11 Role of Repeaters

Repeaters are intermediate buffers in the interconnect line. They are circuits that can discharge and charge capacitances with sufficient speed, thereby reducing propagation delay. The use of repeaters divides interconnect into smaller sub-sections, thus making the delay linear with

length. Repeaters are inserted in order to minimize the interconnect response time by lessening the effect of resistance and capacitance. The delay of a wire increases as a quadratic function of its length. This is major problem in global interconnects as their signal delay tends to be dominated by the *RC* effect. With the scaling of technology, this becomes even more serious as the length of global interconnects increase with the die size. This can lead to requirement of multiple clock cycles for the signal to reach from one end to another. Proper synchronization becomes a challenge under such circumstances.

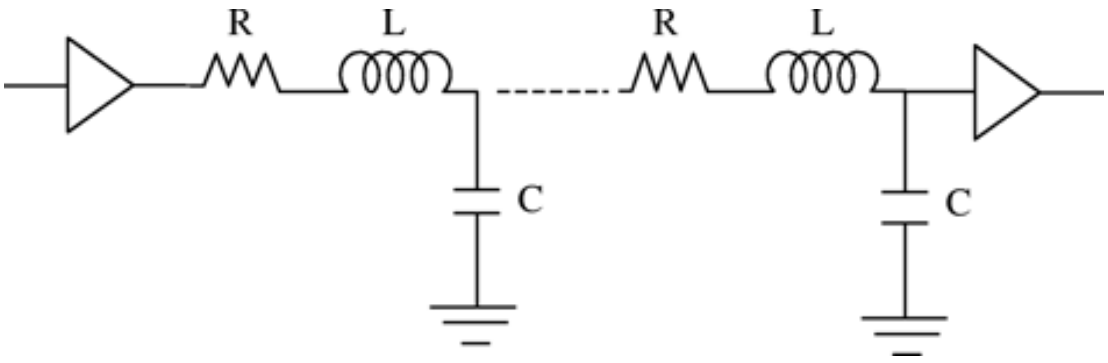

Figure 3.16 Distributed RLC circuit model [3].

3.11.1 Repeater Design

The different types of repeaters are given below.

- **i.** *Uniform minimum sized*: In this type the NMOSFET has the smallest *W/L* ratio possible in the technology, i.e., 1. The PMOSFET has the *W/L* ratio of 3.
- **ii.** *Optimized repeater*: In this type, the size of the repeaters is increased in order to optimize their performance in terms if delay.
- **iii.** *Variable tapered repeater*: This type of repeaters have sequence of drivers that gradually increase in size. This type of repeaters are used when the output capacitive load is very large. It contains tapered cascaded buffers, consisting of optimum number of repeaters in a stage and an accordingly tapering factor.

All the different types of repeaters are shown in Fig. 3.17. The variable tapered repeater when applied to interconnect optimizes the sum total of delay caused by charging the input capacitances of cascaded drivers, thus decreasing the interconnect propagation delay. The total interconnect delay is then given by the expression:

$$T = 2.3(n-1)fR_oC_o + \left(\frac{2.3R_o}{f^{n-1}} + R_{int}\right)C_{int} \qquad (3.23)$$

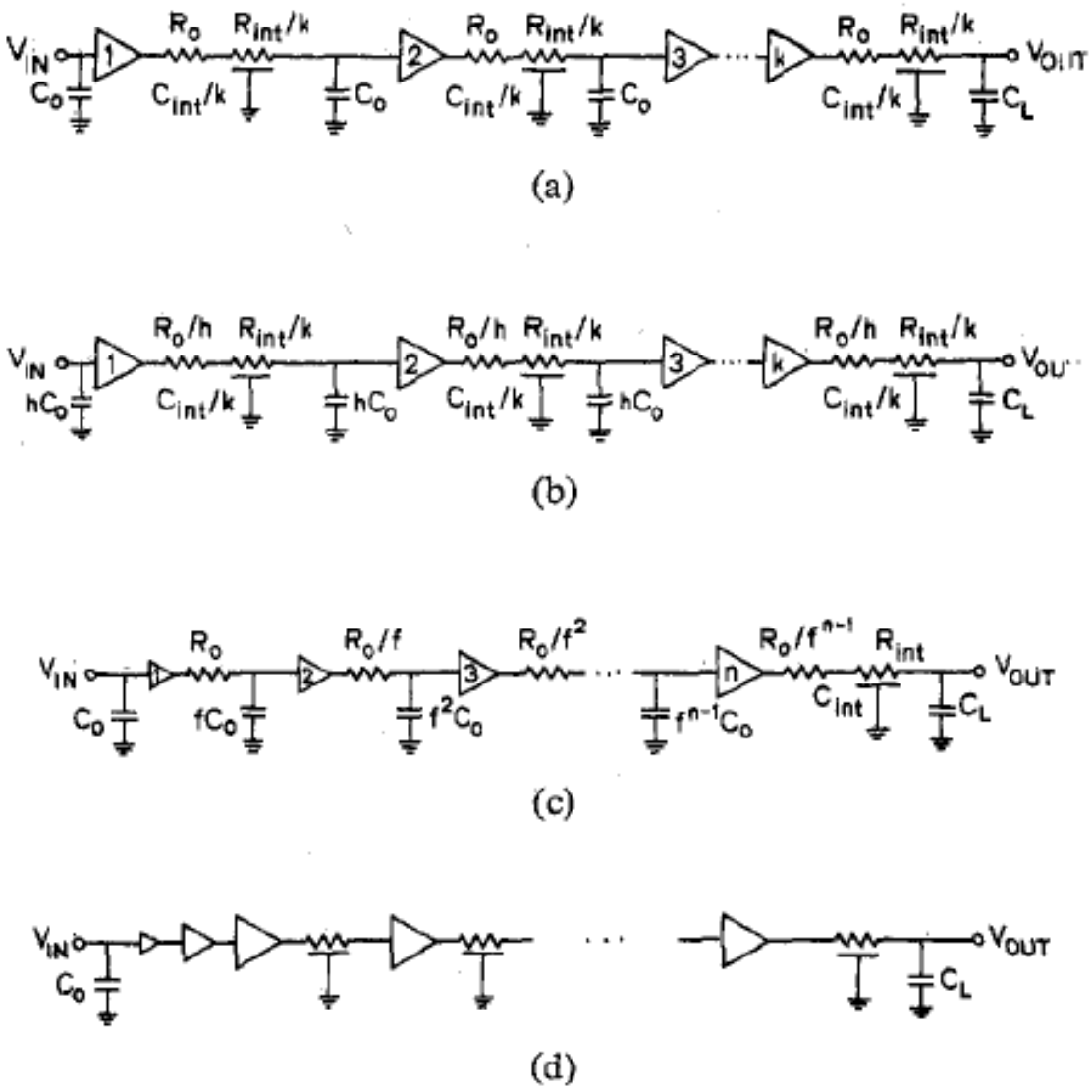

Figure 3.17 Different types of repeaters (a) Minimum size (b) Optimal repeater (c) Cascaded driver repeater (d) Optimal repeater with first stage cascaded [12].

Here, *f* is the optimum value of tapering factor for the cascaded buffer. We derive the optimum value of tapering factor by setting the value of *dT/dn* to zero.

3.12 Effect of parameters on interconnect performance

3.12.1 Effect of dielectric

The interline capacitance of interconnects is given by the following expression.

$$C = \frac{\varepsilon_{dielectric} wL}{X_{OX}} \tag{3.24}$$

It can be seen that the value of dielectric constant (*k*) of the dielectric material between interconnects effects the value of capacitance. Replacing silicon dioxide with low-*k* materials can reduce interconnect delay by decreasing the value of capacitance. The disadvantage of low-

k materials is that they are more prone to dielectric breakdown due to increasing current densities that occur due to scaling.

3.12.2 Pitch of Interconnect

Pitch of interconnect is defined as the sum of interconnect width *w* and the spacing between the two adjacent interconnect lines *s*. It is expressed as:

$$Pitch = w + s \tag{3.25}$$

The width of interconnect is increased to improve the speed of interconnect. The line resistance decreases as the width of interconnect is reduced. Increasing the interconnect width reduces the space between two adjacent interconnect lines.

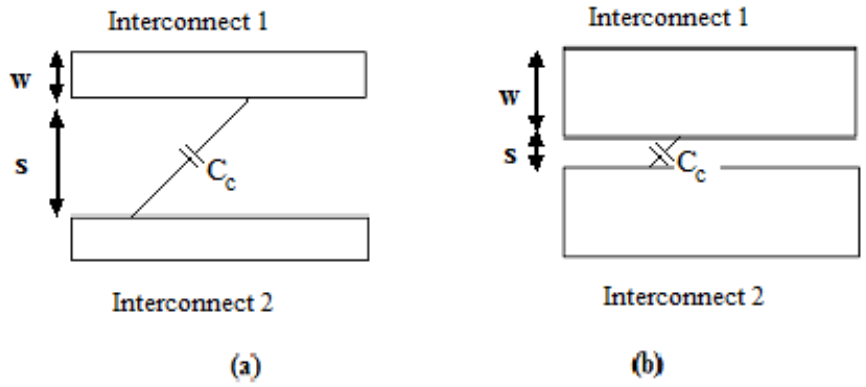

Figure 3.18 Variation of width between two coupled interconnects, C_c shows coupling capacitance between them, (a) small wire width and large spacing (b) large wire width and small spacing.

This results in increase in coupling capacitance, thus increasing inter-line capacitance.

$$C_{pp} = \frac{\varepsilon_{dielectric} hL}{s} \tag{3.26}$$

Thus very closely packed interconnects negates the improvement in interconnect speed [18]. Another disadvantage of smaller pitch is increase in the signal noise.

3.12.3 Length of interconnect

As the length of interconnect increases, the impedance components, i.e., resistance, inductance and capacitance per unit length increase. This increases the delay of interconnect severely, particularly in global interconnects [45]. Scaling of technology further aggravates this problem as the die size increases.

3.12.4 Aspect Ratio

Aspect ratio of interconnect is defined as the ratio of height of interconnect *h* to the width of interconnect *w*.

$$AR = \frac{h}{w} \tag{3.27}$$

Older technologies had A/R<<3, which was achieved by reducing the height of interconnect. In deep sub-micron technologies, this ratio is kept around the value of 2 as higher interconnect height decreases inter-line capacitance. The problem with this is that as A/R increases, the fringing fields and coupling capacitances become considerably large and after a certain point, no gain comes out of increasing aspect ratio. As a result of this, the capacitance per unit length of interconnects in a multilevel interconnect scheme approaches a lower limit of 2pF/cm [49].

3.13 Carbon Nanotube

Carbon nanotubes (CNT) are graphene sheets rolled up into cylinders with diameter of order of nanometres [52]. Depending upon the direction in which they are rolled up, they demonstrate different conducting properties. Their extremely desirable properties like high mechanical and thermal stability, high thermal conductivity and large current carrying capacity have aroused research interest in their applicability as future VLSI interconnects. Carbon nanotubes have some other useful properties as well. CNTs are incredibly tough fibres. They are very sharp and thus can be used as probe tips for scanning probe microscopes and field-emission sources for lamps and displays [22]. The fabrication process of nanotubes eliminates all the dangling bonds, which strictly supports conduction of electrons within the tube. Depending upon the direction in which they are rolled, they are either metallic or semiconducting in nature.

Over the time, use of materials with lower resistivity for interconnects and dielectric materials with low-*k* value has been the method adopted to reduce the *RC* delay of interconnects. Aluminium was replaced by low resistivity material copper and SiO_2 with low-*k* materials in order to do the same. Now as we move further into the deep sub-micron technology, several disadvantages of these materials arise such as electro migration, surface scattering, grain boundary effect, etc. This causes the need for these materials to be substituted by more suited materials in a sense that they are more compatible with the smaller technologies. Carbon nanotube (CNT) is one such potential candidate. They are classified as:

On the basis of conductivity as:

- Metallic.
- Semiconducting.

On the basis of Chirality as:

- Armchair.
- Zigzag.

- Chiral.

On the basis of structure as:

- Single Walled Nanotubes (SWCNT).
- Multi Walled Nanotubes (MWCNT).

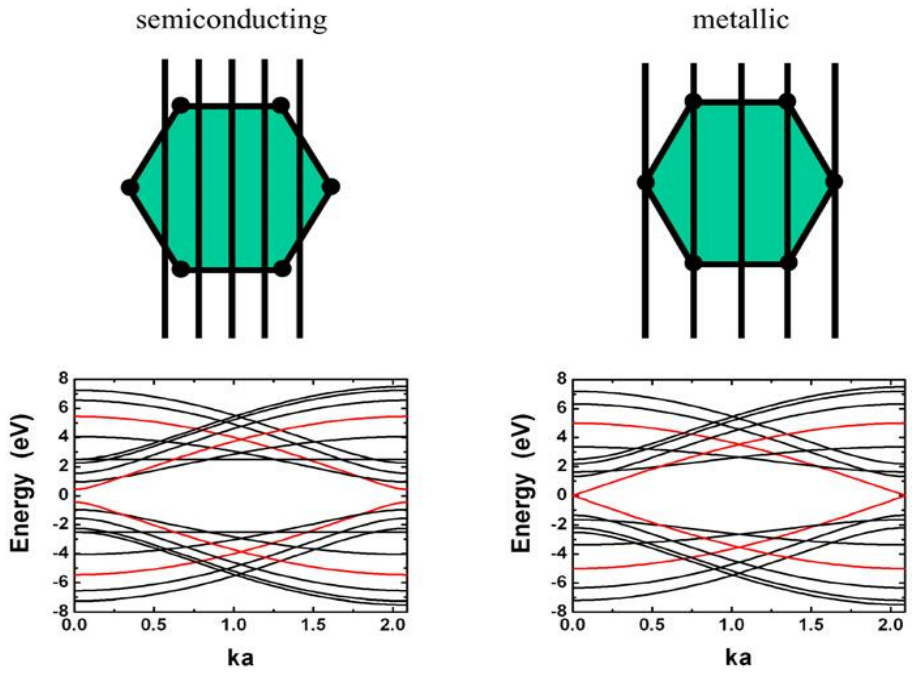

Figure 3.19 Illustration of allowed wave vector lines leading to semiconducting and metallic CNTs and examples of band structures for semiconducting and metallic CNTs [53].

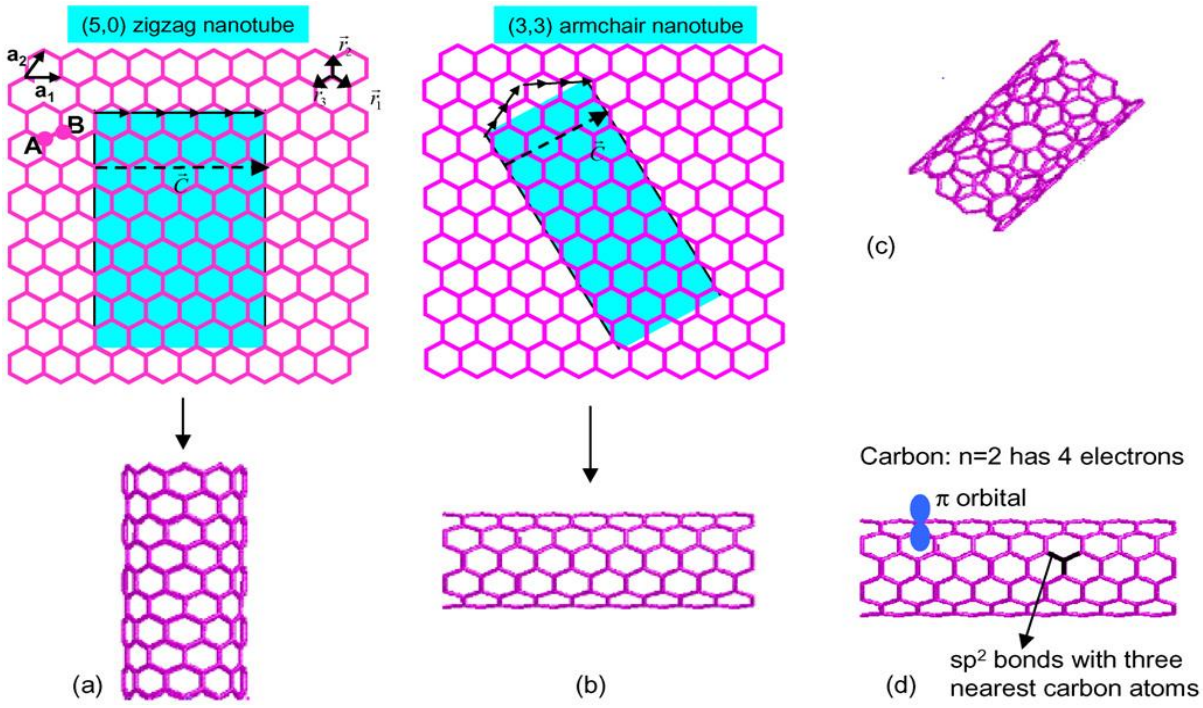

Figure 3.20 (*a*) *a*1 and *a*2 are the lattice vectors of graphene. (*b*) Creation of a (*n, n*) armchair nanotube. (*c*) A (*n,m*) chiral nanotube. (*d*) The bonding structure of a nanotube [53].

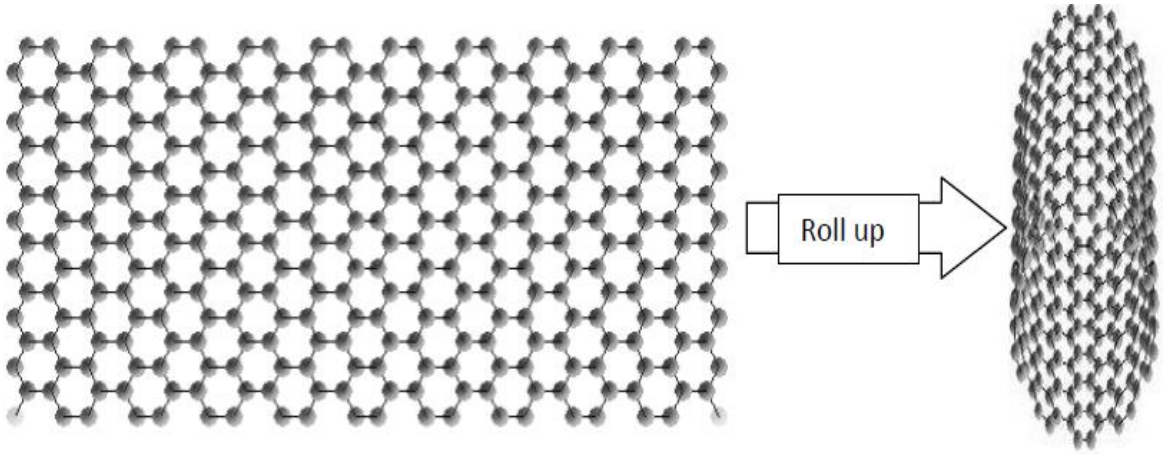

Figure 3.21 Single Walled Carbon nanotube made by rolling up graphene sheet [22].

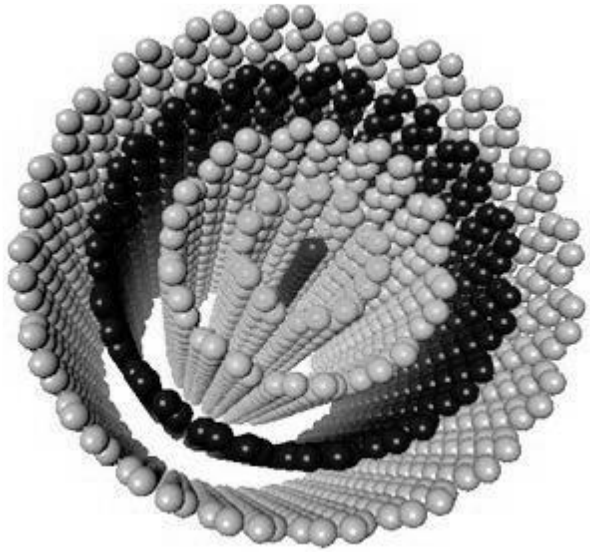

Figure 3.22 Multi Walled CNT structure [22].

3.13.1 Classification of CNTs on the basis of structure

Single walled nanotube is, as the name suggests, a single layer of graphene rolled up to make a cylinder with diameter in the range of 0.7 to 10nm. Based on the chirality in which they are folded, CNTs may be metallic or semiconducting. This chirality has to be controlled during the growth or CNTs. This is not easy to control during growth of CNT bundles. Thus a SWCNT bundle may have any ratio of metallic and semiconducting CNTs. Only the metallic CNTs contribute in current conduction [22].

Multi walled nanotube consists of grapheme sheets rolled up into concentric shells separated by a distance of 0.34nm, which is the Vander Waals gap. Multi-walled CNTs have large diameter of shells due to which the shells are conducting even if they are semiconducting because at room temperature the energy gap between the Fermi level and Conduction band edge (E_C) is smaller than 0.0258 eV. Moreover, due to large density of states in large diameter

shells, this energy gap is very small even if it exceeds 0.0258 eV [31]. The electrons in these sub-bands have reasonable probability (f_i) to appear at E_f following the Fermi-Dirac distribution function. As the MWCNT have many large diameter shells, they can have large number of conducting channels.

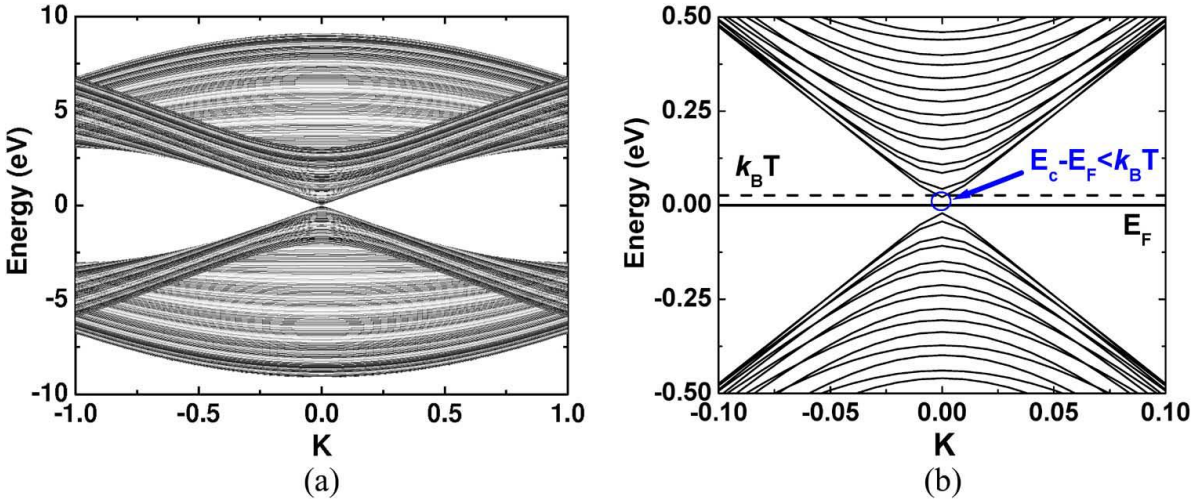

Figure 3.23 (a) Band structure of a zigzag (256, 0) carbon nanotube, and (b) the band structure after zoom in for clarity. K is the normalized wave vector. Each line denotes a sub-band of CNT shell. In the circular area (around K = 0), the energy difference between the conduction band edge (Ec) and Fermi-level EF is smaller than kBT [31].

3.13.2 CNT as VLSI interconnect

Carbon nanotubes are usually many micrometres long and have diameter of the order of nanometres. Hence they can fit well as interconnects in sub-micron range devices. The unique electrical properties of CNTs such as their extremely low resistance are derived from their one dimensional character and unique electronic structure of graphite. Resistance is a result of defects in crystal, impurity atoms or due to vibrating atoms in a crystal. In case of CNTs the electrons are not easily scattered because CNTs are 1D systems.

The transport of electrons in CNTs are ballistic over long nanotube lengths, helping them to carry currents over long distances without any heating. On the other hand, in copper, electrons travel approximately 40 to 50 nm before being scattered. The low resistance reduces the power dissipation in circuits, which is one of the main concerns in chip designing. High current densities of 10^{10} A/cm^2 have been reported in CNTs without any damage even at high temperature of 250^{o}C, thereby eliminating the electro migration concerns that copper suffers from. As CNT has no dangling bonds, there is no need to grow an extra film on its surface and there is no need to restrict the gate insulator to silicon dioxide. This enables the use of other superior materials to insulate the gate terminal of the transistor, ultimately resulting in faster device.

The high resistance associated with an isolated CNT necessitates the use of bundle of CNTs in parallel conducting to form interconnect. Also a single CNT results in a very high contact resistance and thus a bundle is preferred over a ground plane. Due to lack of control over the chirality, a bundle of CNTs contain both metallic as well as semi-conducting CNTs. Only metallic CNTs contribute to current conduction. Due to the presence of imperfect metal-CNT contacts, there is an additional resistance known as contact resistance. This resistance is very high in the range of tens of kilo ohms. This resistance can be high enough to mask the effect of low resistive line. The advantages of CNT over copper are as follows:

1. The transport of electrons in CNT is one dimensional resulting in ballistic conduction with no scattering and very less power dissipation in the form of heat as compared to copper. This allows high current densities in CNTs even at elevated temperatures without any damage such as electro migration, which is observed in copper.
2. There are no dangling bonds in CNTs which need to be satisfied and thus there is no need for chemical passivation as in copper.
3. The strong covalent bonds between carbon atoms in graphene provide high thermal and mechanical stability to CNT and resistance to electro migration. High current densities of 10^{10} A/cm^2 have been reported in CNTs without any damage.
4. The diameter of CNT is controlled during fabrication by chemistry.

3.13.3 Multi Walled Carbon Nanotube as VLSI interconnect

Multi-walled CNTs have large diameter of shells due to which the shells are conducting even if they are semiconducting because at room temperature the energy gap between the Fermi level and Conduction band edge (E_C) is smaller than 0.0258 eV. Moreover, due to large density of states in large diameter shells, this energy gap is very small even if it exceeds 0.0258 eV [31]. The electrons in these sub-bands have reasonable probability (f_i) to appear at E_f following the Fermi-Dirac distribution function. As the MWCNT have many large diameter shells, they can have large number of conducting channels. Until recently MWCNTs had not been reported to exhibit conductance values comparable to SWCNT, thus, were considered to less desirable than SWCNTs for interconnect applications. This can be attributed to the fact that in the early experiments, only the outermost shell in MWCNTs was contacted with metal, whereas the inner shells were isolated from the contact, and therefore had little effect on the conductance. As the MWCNT have many large diameter shells, they can have large number of conducting channels.

3.13.3.1 Equivalent circuit model of Multi Walled Carbon Nanotube

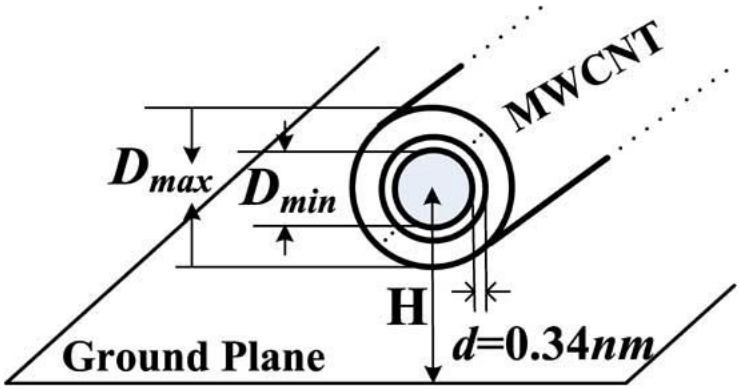

Figure 3.24 Geometry of MWCNT over the ground plane [31].

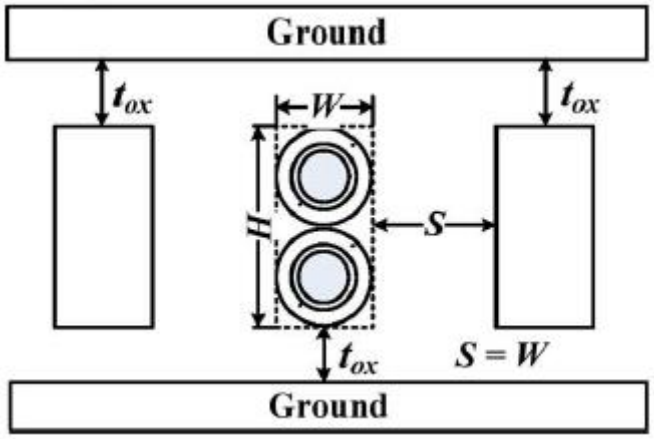

Figure 3.25 Cross section of interconnect [31].

A bundle of MWCNT interconnect over a ground plane is shown in Fig. 3.24. The packing of MWCNTs to form the bundle is shown in Fig. 3.25. The CNTs are packed in parallel to conduct in parallel inside interconnect. An isolated MWCNT is equivalent to a tandem of RLC circuit, comprising of components of resistance, capacitance and inductance. P. J. Burke [54] proposed equivalent circuit model for an isolated CNT and CNT bundle based on Luttinger Liquid theory to obtain the expressions for resistance, capacitance and inductance elements. Based on this model, Kaustav Banerjee *et. al.* developed this model for MWCNT interconnects to obtain the expressions for impedance components of interconnect.

3.13.3.1(a) ***Isolated MWCNT shell:*** Fig. 3.26 shows the equivalent circuit model of an isolated MWCNT shell with contact resistance, quantum resistance, scattering resistance R_{MC}, R_Q and R_S respectively, kinetic inductance L_K and magnetic inductance L_M, quantum capacitance C_Q

and electrostatic capacitance C_E [31]. All these impedance expressions are for per unit length of interconnect.

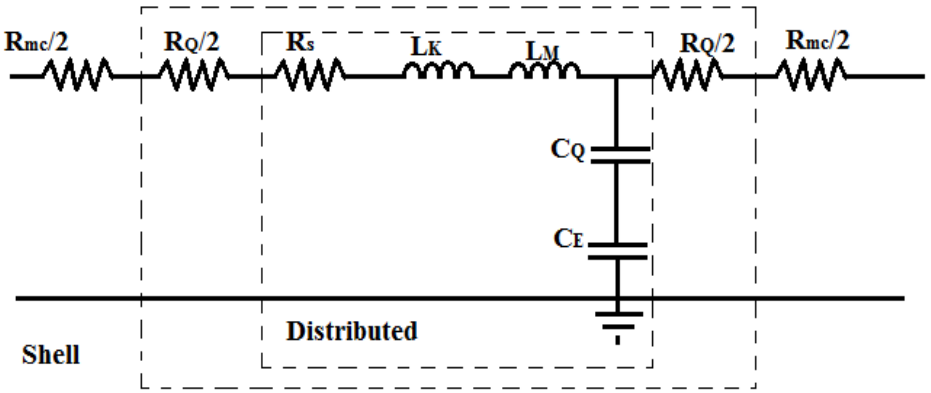

Figure 3.26 Equivalent circuit model of an isolated MWCNT shell [31].

3.13.3.1(b) ***Isolated MWCNT:*** Fig. 3.27 shows the equivalent circuit model of an isolated MWCNT with *p* shells. The maximum diameter, i.e., the diameter of the outermost shell is D_{max} and the diameter of the innermost shell is D_{min} [31]. The number of shells *p* is given by:

$$p = 1 + inter\left[\frac{D_{max} - D_{min}}{2d}\right] \quad (3.28),$$

where *d=0.34nm.*

The diameter of the i'th shell is given by:

$$D_i = D_{max} - 2d(i-1) \quad (3.29)$$

The number of conducting channels of the i'th shell is given by:

$$N_{shell}(D_i) = aD_i + b \quad (3.30),$$

where $a=0.0612nm^{-1}$ and $b=0.425$.

The mean free path of the i'th shell is given by:

$$\lambda_o = 1000D_i \quad (3.31)$$

The magnetic inductance per unit length of the t'th shell present at a distance *y* from the ground plane is given by:

$$L_m = \frac{\mu}{2\pi}\log(\frac{y}{Di}) \quad (3.32)$$

The kinetic inductance per channel is given by:

$$L_{k\ channel} = \frac{h}{4e^2 v_f} \quad (3.33)$$

The kinetic inductance per unit length for the i'th shell is formulated as:

$$L_{k\ shell} = \frac{L_{k\ channel}}{aD_i + b} \quad (3.34)$$

The effective inductance L_{EFF} of the MWCNT interconnect can be obtained from the series-parallel combination of the kinetic inductance and magnetic inductance elements.

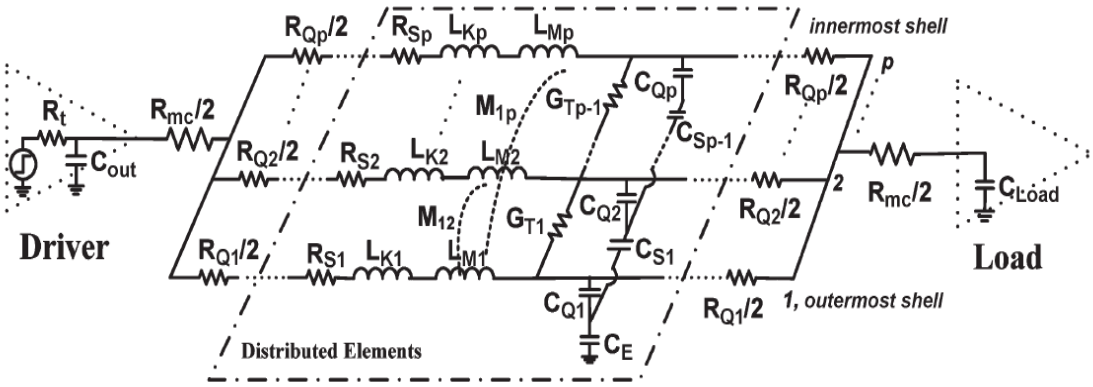

Figure 3.27 Equivalent circuit model of an isolated MWCNT with *p* shells [31].

The quantum capacitance per unit length present due to electrostatic energy stored in CNT when it carries a current per channel is given by:

$$C_{Q\ channel} = \frac{4e^2}{hv_f} \tag{3.35}$$

The quantum capacitance per unit length for the i'th shell is given by:

$$C_{Q\ shell} = C_{Q\ channel}(aD_i + b) \tag{3.36}$$

The electrostatic capacitance per unit length present between the outermost shell of MWCNT and ground plane is given by:

$$C_E = \frac{2\pi\epsilon}{\log\left(\frac{y}{D_{max}}\right)} \tag{3.37}$$

The shell to shell capacitance per unit length is given by:

$$C_s = \frac{2\pi\epsilon}{\ln(Dout - Din)} \tag{3.38}$$

The net effective capacitance C_{eff} can be obtained by the parallel and series combinations of quantum capacitance, shell to shell coupling capacitances and electrostatic capacitances of individual shells.

The resistance per unit length for the i'th shell can be obtained using Eq. (3.39), where *h* is the Planck's constant, λ_0 is the mean free path of electron in the shell, N_{shell} is the number of conducting channels of the shell.

$$R_S = \frac{h}{2e^2 N_{shell}}\left(\frac{1}{\lambda_0}\right) \tag{3.39}$$

3.13.3.1(c) ***MWCNT bundle:*** The expression for number of MWCNTs in a bundle of width *w* and height *h* is given by [31]:

$$n_{CNT} = \frac{wy}{D_{max}.D_{max}} \tag{3.40}$$

The resistance of MWCNT bundle is divided among the parallel MWCNTs inside the bundle and thus the net effective resistance of MWCNT bundle is formulated as:

$$R_{eff} = \frac{R_{CNT}}{n_{CNT}} \tag{3.41}$$

The net effective capacitance of the MWCNT bundle can be obtained by the expression given as:

$$C_{bundle} = n_{CNT} C_{eff} \tag{3.42}$$

Similarly the net effective inductance of the MWCNT bundle is given by:

$$L_{CNT} = \frac{L_{EFF}}{n_{CNT}} \tag{3.43}$$

3.14 Future VLSI interconnects

As the technology is scaled down the need for a substitute for copper as interconnect material rises. Proposed possible replacements for metal interconnects are as follows.

1. Graphene Nano-ribbons.
2. Optical Interconnects.
3. Carbon Nanotubes.

Graphene Nano-Ribbons are strips made out of graphene sheets with proper chirality and width of the order of nanometres. They can be metallic or semiconducting depending on the geometry just like nanotubes. They have larger mean free path compared to copper and have large current densities. GNRs are believed to be more controllable from fabrication point of view due to planar structure of graphene, which can be patterned using high resolution lithography. They are believed to be best for the local level of interconnects. Due to high resistance of single GNR layer, it is required to use multiple graphene layers. It is believed that if perfect specularity can be achieved then GNRs can outperform CNT interconnects [55].

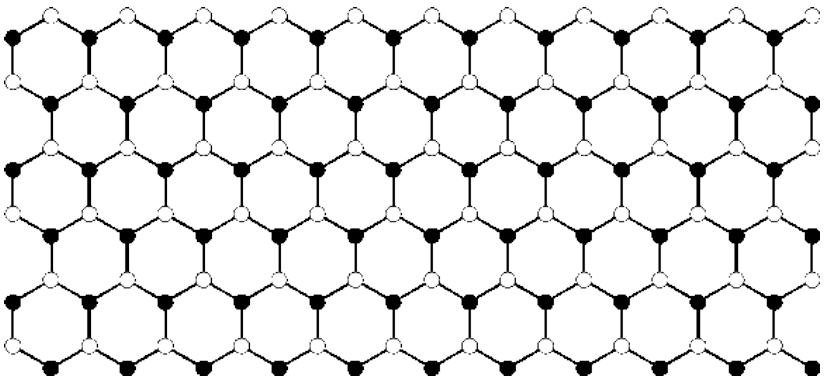

Figure 3.28 Graphene Nano Ribbon [55].

The term optical interconnect is assumed to deal with data transmission inside an electronic device or system using light. It can be compared with optical communication which refers to optical data transmission between distant and independent systems. Optical interconnection refers to the data transmission in which the data signal is transmitted as a modulation of optical carrier wave (light) through an optically transparent media such as optical fibre, planar optical waveguide or air. Nearly all optical data links actually function at the near-infrared wavelength range between 800 nm and 1600 nm. Optical communications through fibre has long been the technology of choice for high-speed long-distance data links. Gradually, as the capacity requirements have increased, the optical links have emerged into shorter distance applications, such as fibre-to-the-home and even into fibre-optic interconnects between boards and cabinets inside electronic equipment which is referred as optical interconnects [56].

3.15 Optical interconnects

Optical interconnects provide a lossless medium to the signal over long distances. The advantage comes at a price of extra circuitry required for the transmission and receiving the signal. The electrical signal is required to be converted to light via the use of a LASER so that it can be coupled into the optical interconnect. This is done using a transmitter. At the other end, light signal is converted into electrical signal using photo-detectors so that it can be decoded precisely. This extra circuitry for transmitter and receiver takes up considerable silicon area in the chip. Most of the delay and power dissipation of an optical interconnect occurs in these circuits. It is due to this reason that optical interconnects are preferred for chip to chip communication in a system. However, with the advancement of technology, wave division multiplexing techniques and increasing bandwidth density, optical interconnects are a potential candidate for future interconnects [58].

3.15.1 Optical interconnect system

The optical interconnect system consists of a transmitter for converting the electrical signal into light signal using a LASER and coupling the light signal into the optical interconnect, optical interconnect to guide the signal and a receiver to convert the light signal into electric signal [30]. The transmitter and receiver circuits are discussed in the following sections.

***Transmitter*:**

The transmitter consists of an electro-optical modulator and a corresponding driving circuit. A typical laser driver for VCSEL consists of a super-buffer followed by a current mirror circuit as shown in Fig. 3.29. The super-buffer is used to drive the large capacitance output at high

speeds. The super-buffer is a set of cascaded invertors with the next invertor larger in size from the previous invertor by a constant factor of β. The value of β is typically between 3 and 4. The first invertor is minimum sized invertor and the last invertor drives the modulator of VCSEL [58]. The total power dissipated by the super-buffer is given by [58]:

$$P_{sb} = C_{total} V_{DD}^2 \frac{BR}{2} \tag{3.44}$$

Here C_{total} is the total capacitance of the super-buffer and is given as [58]:

$$C_{total} = \left(C_{load} - C_{in,min}\right) + \sum_{k-0}^{n-1} \left(C_{in,min} + C_{out,min}\right) \beta^k \tag{3.45}$$

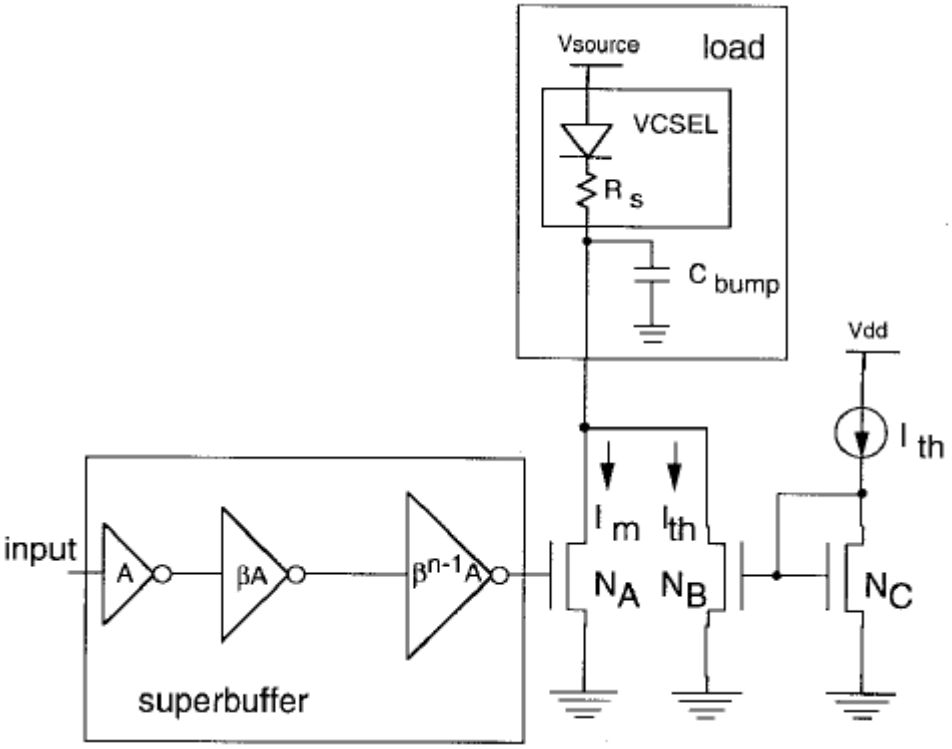

Figure 3.29 Output driving stage of CMOS driver connected to VCSEL [58].

Here $C_{in,min}$ and $C_{out,min}$ are the input and output capacitances of a minimum size invertor. C_{load} is the load capacitance of the super-buffer that includes the capacitance of the modulator and parasitic capacitances.

The modulation current is assumed to be high enough at high speeds such that the bias point of VCSEL is high above the threshold, thus decreasing the turn-on time. Also the values of modulation current and bias current are selected such that the VCSEL never operates below its threshold, thus ensuring that turn-on time for VCSEL in minimum. The total power dissipated in the transmitter circuit is due to super-buffer, VCSEL and the modulator circuit.

The total LASER current is equal to the sum of threshold current I_{th} and average modulation current I_m. The total power dissipated in VCSEL and the output stage is formulated as [58]:

$$P_{CMOS,VCSEL} = I_{total} V_{source} \tag{3.46}$$

$$P_{CMOS,VCSEL} = \left[I_{th} + \frac{I_m}{2}\right][V_{th} + R_s I_m + (V_{DD} - V_{tn}] \tag{3.47}$$

***Receiver*:**

The receiver consists of a photo-detector which converts the light signal to current signal followed by a trans-impedance amplifier *TIA* which converts the current signal to voltage signal. This voltage signal is then amplified by voltage amplifier and the resulting signal is given to a decision circuit which determines the output of the circuit.

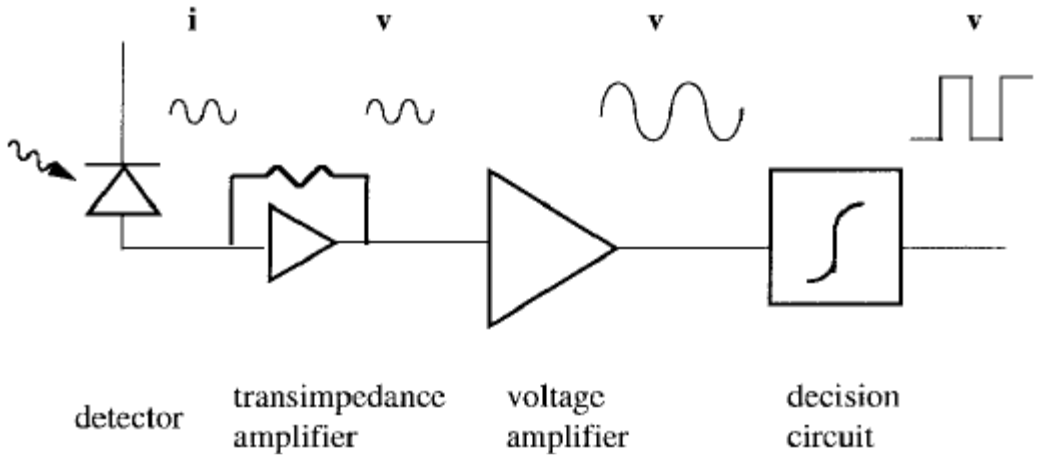

Figure 3.30 Block diagram of the receiver circuit [58].

Fig. 3.30 shows the block diagram of the receiver circuit.

The response time of the photo-detector is dependent on the carrier transit time and RC charging time of the capacitance at detector and is given as [59]:

$$T_r = (\tau_{tr}^2 + \tau_{RC}^2)^{1/2} \tag{3.48}$$

Here, $\tau_{tr} = \frac{X}{v}$ *and* $\tau_{RC} = 2.2RC$ (3.49)

The delay of TIA is given by the following expression and it is included in the optical link. It is calculated by supposing the system to be one-pole system [59].

$$T_D = \frac{0.693}{2\pi\Delta f} \tag{3.50}$$

Here Δf is the bandwidth requirement.

Thus the total delay of the optical receiver can be formulated as [59]:

$$t_{rx} = 0.315\sqrt{(2.2RC)^2 + \left(\frac{X}{v}\right)^2} + \frac{0.693}{2\pi\Delta f} \quad (3.51)$$

3.16 Nanotube Vias

Researchers have been able to design CNT vias due to the ability of growing nanotubes at specific sites [23]. Vias are defined as the interconnections between levels of interconnects in chips. CNTs have been proposed as the alternative for metal plugs as vias. Copper vias are prone to deterioration due to current crowding and electro migration. One solution is the use of large mitigation tolerance CNTs as vias. CNT bundles can be used as vias to get enough current for LSI interconnections.

3.17 Conclusion

Carbon nanotubes are a potential candidate for future VLSI interconnects compared to copper due to their unique properties and resistance to effects like electro migration and diffusion barrier width. More controlled fabrication process is required to control the chirality of CNTs so that more tubes contribute to current conduction. GNR and optical interconnects are other potential candidates for chip to chip and on-chip interconnects.

CHAPTER

4

Analytical Results

4.1 Introduction

It is necessary to model interconnects as transmission lines in deep-submicron technology. Thus highly accurate RLC models are required for the analysis of VLSI interconnects. RC model is a limiting case of RLC model where the inductance is neglected [3]. Elmore delay model is an example of RC model as already discussed in previous chapters. However Elmore delay model is highly inaccurate when frequency is increasing resulting in increase in inductive impedance [9]. Various interconnect models have been discussed in detail in the previous chapters. These models are used to model interconnect as a transmission line.

Along with the requirement to model interconnects, there is a need to model the CMOS invertor/repeater driving them. The CMOS invertor is the simplest buffer or repeater in VLSI interconnects. Alpha power MOS model for the current voltage characteristics for short channel MOSFET was given by Newton and Sakurai [17]. Kaushik ,*et. al.* presented an analytical model for a CMOS invertor driving a RLC load [19]. The alpha-power law MOS model has been used to derive the delay performance of a CMOS invertor which is driving a RLC interconnect load. A π-RLC interconnect model is used for both copper and MWCNT in 22nm technology to calculate the delay mathematically.

4.2 Piecewise Transient Analysis for π-segment RLC

A CMOS invertor driving a π-segment RLC circuit is shown in Fig. 4.1. Alpha power law MOS model is used to model the invertor [19]. The drain current under different regions of operations of NMOSFET is formulated as [17]:

$$I_d = \begin{cases} 0; & V_{GS} \le V_{T0}: \quad cut-off\ region \\ k_l(V_{GS}-V_{T0})^{\frac{\alpha}{2}}V_{DS}; & V_{DS} < V_{DSAT} \quad : linear\ region \\ k_S(V_{GS}-V_{T0})^{\alpha}; & V_{DS} \ge V_{DSAT} \quad : saturation\ region \end{cases}$$

Here α is known as the velocity saturation index, k_l and k_S are the trans-conductance parameters in the linear and saturation regions of the transistor respectively, V_{DSAT} and V_{To} are the drain-saturation voltage and the zero bias threshold voltage respectively.

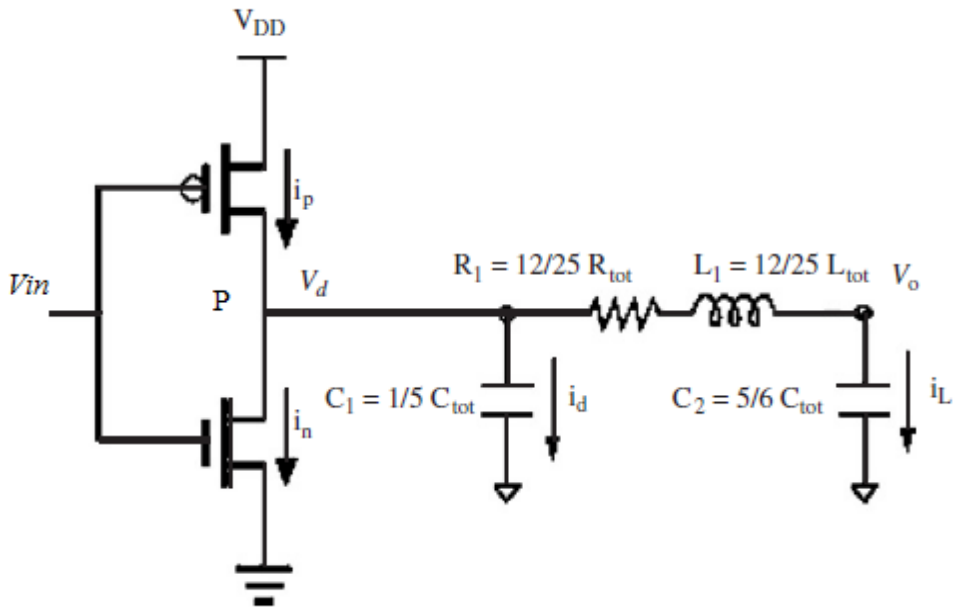

Figure 4.1 A CMOS buffer driving a π model RLC interconnect line [19].

The input signal is assumed to be fast ramp [19]. The analytical expression for the output voltage is obtained for four different regions of operation of the transistor for the input signal. Apply KCL at the node *p*,

$$i_n + i_d + i_L - i_p = 0 \tag{4.1}$$

Now, as the input signal is rising, the NMOS will start discharging the voltage at the output node via the RLC circuit and the output voltage level starts decreasing. Thus the NMOS will go from the cut-off region to the saturation region to the linear region. Hence accordingly the four regions are suggested for the operation of discharging of the output.

Region 1 ($0<t<t_1$):

In this time interval the NMOSFET is in cut-off region until the input signal level reaches to the value equal to the threshold voltage *($V_{GS}=V_{To}$)* of NMOS and it is turned ON. Thus the eqn (4.1) reduces to:

$$i_d + i_L = 0 \tag{4.2}$$

Where

$$i_d = C_1 \frac{dV_d}{dt} \qquad \text{and} \qquad i_L = C_2 \frac{dV_0}{dt} \tag{4.3}$$

Here V_d is the drai-source voltage across the NMOS and V_0 is the output voltage at the load.
Substituting the value of V_d

$$V_d = LC_2\frac{d^2V_o}{dt^2} + RC_2\frac{dV_o}{dt} + V_o \tag{4.4}$$

We get

$$a\frac{d^3V_o}{dt^3} + b\frac{d^2V_o}{dt^2} + \frac{dV_o}{dt} = 0 \tag{4.5}$$

Here

$$a = \frac{C_1C_2L}{C_1 + C_2} \tag{4.6}$$

$$b = \frac{C_1C_2R}{C_1 + C_2} \tag{4.7}$$

$$t_1 = \frac{V_{T0}}{V_{DD}}\tau \tag{4.8}$$

Here the initial conditions are

$$V_o(0) = V_{DD},\ \frac{dV_o}{dt}(0) = 0,\quad \frac{d^2V_o}{dt^2}(0) = 0 \tag{4.9}$$

Solving the differential equation, we get

$$Vo = V_{DD} \tag{4.10}$$

Thus the output remains equal to V_{DD} up to time t_1.

Region 2 ($t_1<t<\tau$):
During this time interval, the NMOS operates in the saturation region.
Input signal is expressed as

$$V_{in} = \frac{V_{DD}}{\tau}t \tag{4.11}$$

Apply KVL at node *p*,

$$i_n + i_d + i_L = 0 \tag{4.12}$$

We get by substituting,

$$a\frac{d^3V_o}{dt^3} + b\frac{d^2V_o}{dt^2} + \frac{dV_0}{dt} + \frac{K_S}{C_1 + C_2}\left(\frac{V_{DD}}{\tau}t - V_{T0}\right)^{\alpha} = 0 \tag{4.13}$$

This equation cannot be solved analytically. Thus to obtain an analytical expression for the output, current i_n is approximated by a second-order Taylor series at time $t=\tau/2$ as:

$$\frac{i_n}{C_1 + C_2} = A_0 + A_1 t + A_2 t^2 \tag{4.14}$$

The initial conditions are,

$$V_o(0) = V_{DD},\ \frac{dV_o}{dt}(0) = 0,\quad \frac{d^2V_o}{dt^2}(0) = 0 \tag{4.15}$$

Solving the differential equation, we get

$$V_o(t) = K_1 t^3 + K_2 t^2 + K_3 t - K_4 e^{-\frac{(b-M)t}{2a}} - K_5 e^{-\frac{(b+M)t}{2a}} + C[3] \tag{4.16}$$

Here,

$$M = \sqrt{b^2 + 4a} \tag{4.17}$$

$$K_1 = -\frac{A_2}{3} \tag{4.18}$$

$$K_2 = A_2 b - \frac{A_1}{2} \tag{4.19}$$

$$K_3 = 2aA_2 - 2b^2 A_2 - A_0 + bA_1 \tag{4.20}$$

$$K_4 = \frac{2aC[2]}{b - M} \tag{4.21}$$

$$K_5 = \frac{2aC[1]}{b + M} \tag{4.22}$$

C[1], C[2] and C[3] are integration constants.

Region 3 ($\tau<t<t_2$):

During this region, the input has reached V_{DD} and NMOS is still in saturation. The differential equation for the output is:

$$a\frac{d^3V_o}{dt^3} + b\frac{d^2V_o}{dt^2} + \frac{dV_o}{dt} + A_3 = 0 \tag{4.23}$$

Here,

$$A_3 = \frac{K_s}{C_1 + C_2}(V_{DD} - V_{T0})^{\alpha} \tag{4.24}$$

$$K_S = \frac{I_{D0}}{(V_{DD} - V_{T0})^{\alpha}} \tag{4.25}$$

Using the initial conditions,

$$V_o(0) = V_{DD},\ \frac{dV_o}{dt}(0) = 0,\quad \frac{d^2V_o}{dt^2}(0) = 0 \tag{4.26}$$

We get,

$$V_o(t) = C[6] - A_3 t - K_6 e^{-\frac{(b-M)t}{2a}} - K_7 e^{-\frac{(b+M)t}{2a}} \tag{4.27}$$

Here,

$$K_6 = \frac{2aC[5]}{b-M} \tag{4.28}$$

$$K_7 = \frac{2aC[4]}{b+M} \tag{4.29}$$

C[4],C[5] and C[6] are integration constants.

Region 4 ($t>t_2$):

During this region, $V_{in}=V_{DD}$ and the NMOS operates in the linear region. The differential equation describing the output is expressed as:

$$a\frac{d^3V_o}{dt^3} + K_8\frac{d^2V_o}{dt^2} + K_9\frac{dV_o}{dt} + K_{10}V_o = 0 \tag{4.30}$$

Here,

$$K_8 = \frac{nLC_2}{C_1+C_2} + b \tag{4.31}$$

$$K_9 = \frac{nRC_2}{C_1+C_2} + 1 \tag{4.32}$$

$$K_{10} = \frac{n}{C_1+C_2} \tag{4.33}$$

$$n = K_L(V_{DD}-V_{T0})^{\frac{\alpha}{2}} \tag{4.34}$$

$$K_L = \frac{I_{D0}}{V_{DD}(V_{DD}-V_{TH})^{\frac{\alpha}{2}}} \tag{4.35}$$

Solving the differential equation using the boundary conditions, we get

$$V_o(t) = C[7]e^{-\frac{\frac{1}{12}\left(\beta^{2/3}-12aK_9+4K_8^2+4K_8\beta^{1/3}+i\sqrt{3}\beta^{2/3}+i12\sqrt{3}aK_9-i4\sqrt{3}K_8^2\right)t}{a\beta^{1/3}}} + C[8]e^{-\frac{\frac{1}{12}\left(-\beta^{\frac{2}{3}}+12aK_9-4K_8^2-4K_8\beta^{\frac{1}{3}}+i\sqrt{3}\beta^{\frac{2}{3}}+i12\sqrt{3}aK_9-i4\sqrt{3}K_8^2\right)t}{a\beta^{\frac{1}{3}}}} + C[9]e^{-\frac{-\frac{1}{6}\left(-\beta^{\frac{2}{3}}+12aK_9-4K_8^2+2K_8\beta^{\frac{1}{3}}\right)t}{a\beta^{\frac{1}{3}}}} \tag{4.36}$$

Here,

$$\beta = 36aK_8K_9 - 108a^2K_{10} - 8K_8^3 + 12a(12aK_9^3 - 3K_8^2K_9^2 - 54aK_8K_9K_{10} + 81a^2K_{10}^2 + 12K_8^3K_{10})^{\frac{1}{2}} \quad (4.37)$$

C[7],C[8] and C[10] are propagation constants.

4.2.1 Analytical Delay prediction for CNT

The rise time of the input ramp signal is 1ns. The total time of output fall is 2.34ns. The CNT bundle parasitics were calculated using the expressions described in the previous chapter. Using these expressions, the values of all impedance factors are calculated for a line length of 1000μm. Table 4.1 shows the parameters used for this calculations.

The output voltage plotted against time is shown in Fig. 4.2. A SPICE simulated waveform is also plotted in the same graph. The difference between the analytical and SPICE waveform results are the error in the analytical model.

Table 4.1: Parameters used for calculation in analytical model [31]

Parameters	**Value**
Technology	22nm
V_{DD}	0.7V
Length of interconnect	1000μm
Width of interconnect	32nm
Thickness of interconnect	96nm
Oxide thickness	76.9nm
K_{ILD}	2.05
Aspect ratio of driver	40
V_{T0} of NMOS	0.369V
Velocity saturation index	1

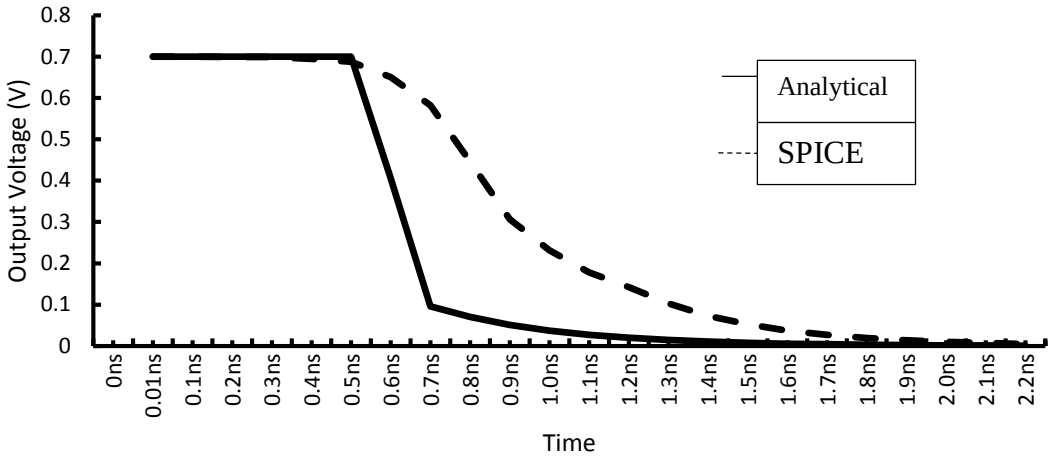

Figure 4.2 Analytical v/s SPICE delay for MWCNT bundle interconnect.

4.3 Conclusion

Analytical model is used to extract the transient response of CMOS inverter driven π-RLC interconnect. Alpha power law model is used to model CMOS inverter transistors and fast ramp input is considered for analytical and simulation operation. The results show that there is an agreement between the results extracted using analytically and SPICE simulation. The discharging time is same for both cases. This is attributed to the fact that alpha-power law is not accurate for technologies less than 90nm [60]. Thus, new improved models are required to predict the response more accurately.

CHAPTER

5

Influence of tube parameters on delay and power dissipation

5.1 Introduction

The impedance parameters for copper and MWCNT interconnects at different lengths of interconnect are calculated and their effect on performance of interconnect is analysed and compared. Also the impedance parameters for MWCNT interconnect at different diameters of MWCNTs are calculated and their effect on the performance of interconnect is analysed. The equivalent circuit models presented in the previous chapters are used to calculate the equivalent impedance parameters. For calculating the values of resistance, inductance and capacitance, programs have been developed in MATLAB R2010a. All the MWCNTs are assumed to be perfectly metallic and having compact packing, i.e., high density in the interconnect bundle.
For analysing the effect of change in length on the performance of interconnect, the length of the MWCNT interconnect is varied from 400um to 1000um with a 100um step while its maximum diameter D_{max} is kept constant at minimum value, i.e., 32nm for global interconnect and its width and height are also kept constant at their respective minimum values, i.e., 32nm and 96nm respectively for *A/R* equal to 3.

For analysing the effect of change in diameter of tube on the performance of interconnect, the maximum diameter D_{max} of interconnects in the MWCNT bundle is varied from 8nm to 32nm with a 2nm step while the width and height of interconnect are kept at minimum values, i.e., 32nm and 96nm for global level respectively and the length of interconnect is kept constant at 1000um.

The performance of MWCNT interconnect is also compared in terms of delay and power to optical interconnect at different lengths of interconnect. The length of interconnect is varied from 400µm to 1000µm with 100µm steps and then from 1000µm to 10000µm with 1000µm steps. Optical interconnect with WDM value of 0.6µm is used. For the sake of comparison the same clock frequency is used as in MWCNT.

The values of equivalent impedance parameters are calculated for these cases. The observations are discussed. The simulation parameters used for these calculations are given in Table 5.1.

Table 5.1: Simulation parameters used for calculation at 22nm technology [31]

Parameters	CNT	Copper
V_{DD}	0.7V	0.7V
Width of global interconnect (w)	32nm	32nm
Aspect ratio for global	3	3
Thickness for global (H)	96nm	96nm
Width of local and semi-global interconnect (w)	22nm	22nm
Aspect ratio for local and semi-global	2	2
Length (L)	1000μm	1000μm
ILD thickness	76.8nm	76.8nm
K_{ILD}	2.05	2.05

5.2 Impedance Analysis

The effects of change in length of interconnect and tube diameter on the impedance parameters are discussed in this section.

5.2.1 Influence of interconnect length

Fig. 5.1, 5.2 and 5.3 show the effect of change of interconnect length on the impedance parameters. It is observed that the values of resistance, inductance and capacitance increase as the line length increase. Similar effects are observed in copper. The impedance parameters affect the delay and power dissipation of interconnect. Thus the variation in the length of interconnect affects the performance of interconnect.

Resistance: Quantum resistance, scattering resistance and contact resistance are the three components of resistance that contribute to the net resistance of interconnect. As can be seen from the expression provided in the previous chapters, the scattering resistance is a function of line length. Thus the scattering resistance increases as the length of interconnect exceeds the mean free path of the electron.

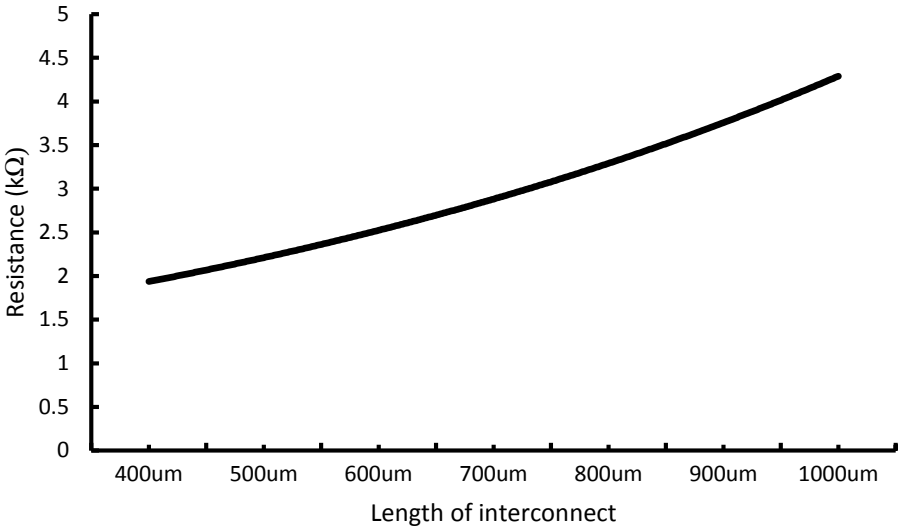

Figure 5.1 Effect of change of interconnect length on resistance.

This can be seen in Fig. 5.1. If the length of interconnect is smaller than the mean free path of electron in tube, then only quantum resistance and contact resistance exists and the electron transport is ballistic.

Inductance: Kinetic inductance and magnetic inductance are the two components of the inductance of interconnect, as already discussed in the previous chapters. As the line length increases, the inductance of interconnect increases as the number of inductance elements increase while the value of inductance elements per unit length remain same.

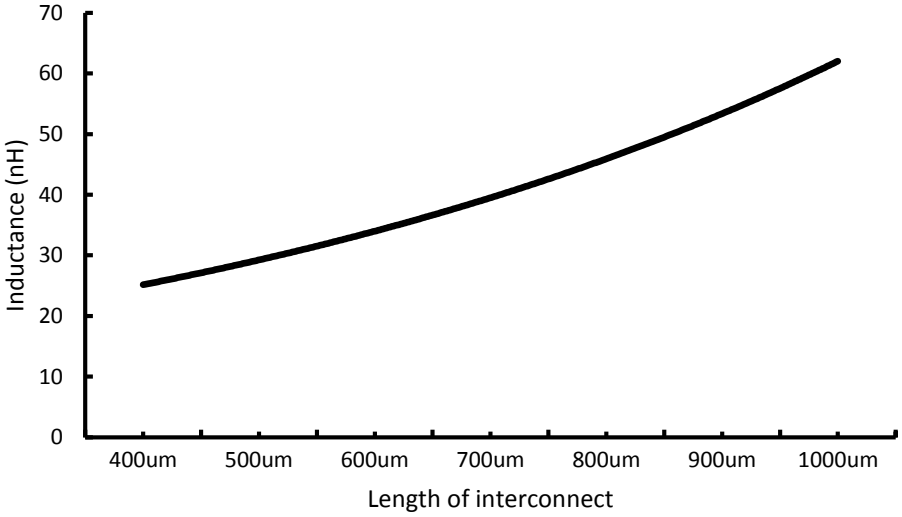

Figure 5.2 Effect of change of interconnect length on inductance.

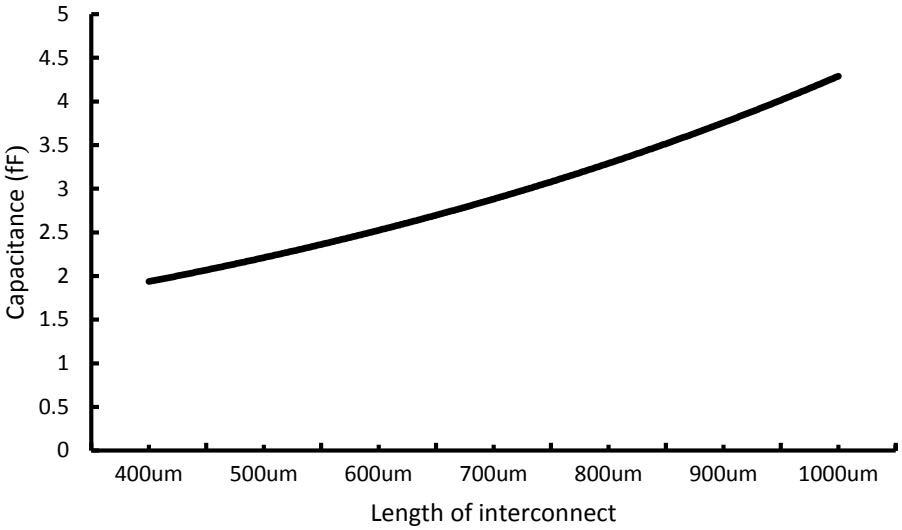

Figure 5.3 Effect of change of interconnect length on capacitance.

This means there are more number of inductance elements as the line length increases. This is shown in Fig. 5.2.

Capacitance: Quantum capacitance, electrostatic capacitance, shell to shell coupling capacitance are the three components of capacitance as already discussed. The net effective capacitance of the line increases as the line length increases. This is shown in Fig. 5.3 and is due to increase in number of capacitive elements in the line as its length increases.

5.2.2 Influence of tube diameter

Resistance: The effect of change of tube diameter in the bundle on resistance of interconnect is shown in Fig. 5.4. It can be seen from the equation of resistance that it is function of mean free path and the number of channels, both of which are a function of tube diameter. Both the mean free path of electrons and the number of conducting channels per shell are directly proportional to the diameter of shell as can be seen from their expressions in previous chapters. Thus the resistance decreases as the tube diameter increases.

Inductance: Fig. 5.5 shows the effect of increase of diameter to the net effective inductance of interconnect. As can be seen from their expressions shown in previous chapters, both kinetic inductance and magnetic inductance are inversely proportional to diameter of shell. Thus the net effective inductance increases as the tube diameter increases.

Capacitance: As can be seen from the equation of capacitances, they are directly proportional to the diameter of shell. The electrostatic capacitance between the outermost shell and ground

plane in particular contributes majorly to the net effective capacitance. Thus the capacitance increases with increase in tube diameter as can be seen in Fig. 5.6.

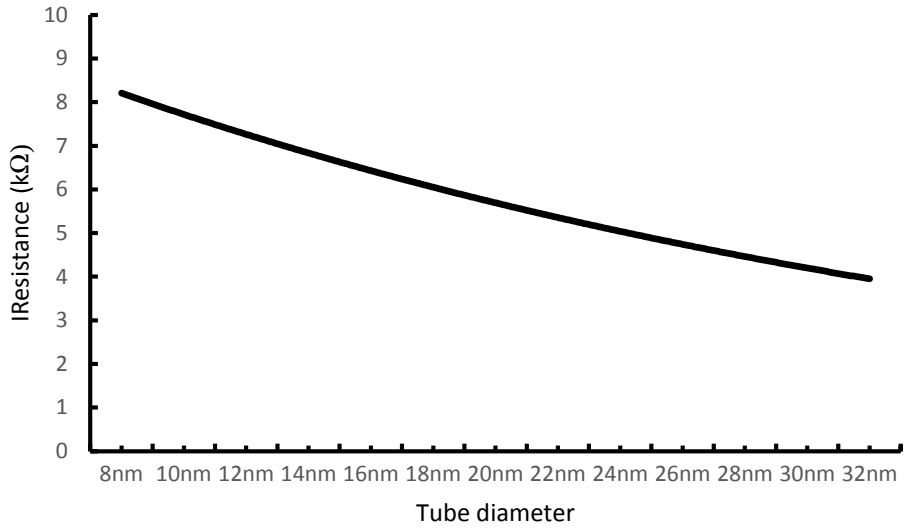

Figure 5.4 Effect of change in tube diameter on resistance of interconnect.

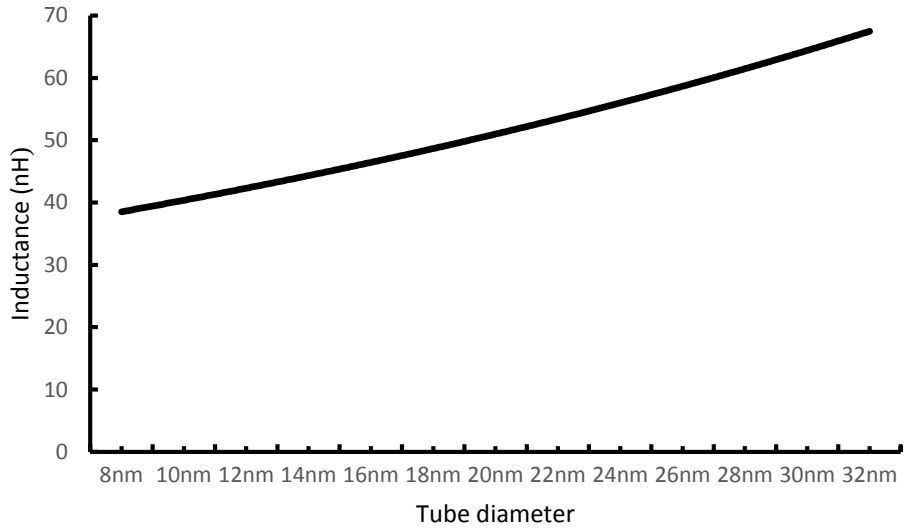

Figure 5.5 Effect of change in tube diameter on inductance of interconnect.

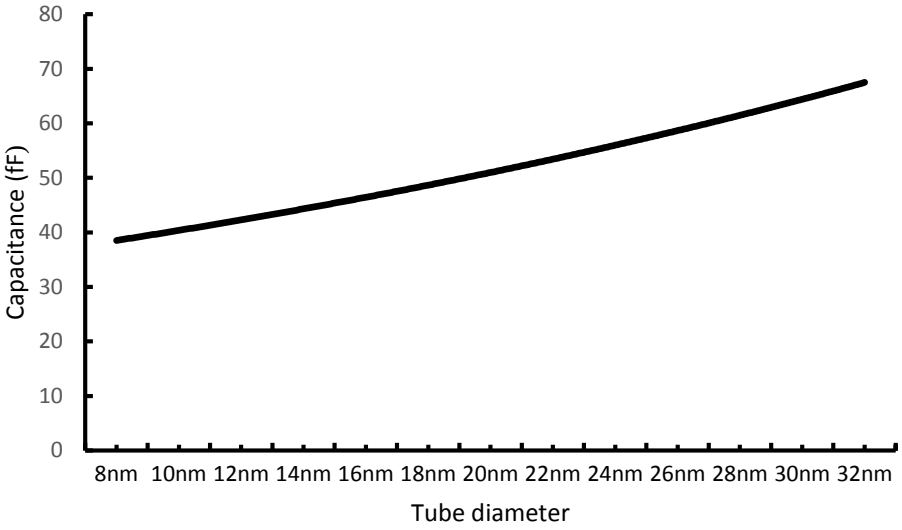

Figure 5.6 Effect of change in tube diameter on capacitance of interconnect.

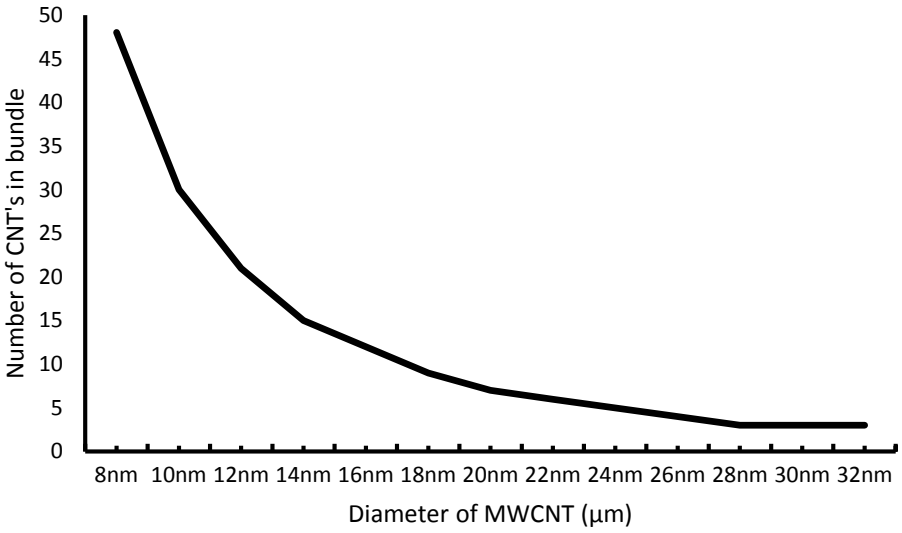

Figure 5.7 Variation in number of CNTs in a bundle with tube diameter.

5.3 Aspect Ratio

The Lumped RLC model for interconnect is used to find the optimum driver aspect ratio *A/R*. The optimum driver aspect ratio for driving interconnect 1000µm long with width 32nm and aspect ratio equal to 3 at the global level is calculated. Rise time, fall time, average delay and power dissipation for different aspect ratios were calculated for different aspect ratios ranging from 10 to 100 with step size of 10. The schematics for the circuit were drawn using Tanner EDA tool S-Edit 12 (Schematic Capture) version 12.5. Simulations were done using Tanner

EDA tool T-Spice 12 (Circuit Simulator) version 12.5. All simulations were done for 22nm technology. 90% delay is calculated using SPICE simulated results. Values of various parameters were calculated using their expression given below.

Feature size λ = 11nm.

Width of transistor $W = \lambda(A/R)$ (5.1)

Area of source/drain $AS/AD = 5\lambda W$ (5.2)

Perimeter of source/drain $PS/PD = 10\lambda + 2W$ (5.3)

After the values to all the parameters are given, the input signal is defined. Here the input signal is a square wave of amplitude 0.7V, time period 10ns, rise time and fall time of 1ns. The rises time and fall times are calculated from the simulation graph. The average delay is calculated and is equal to the mean of the rise time and fall time. This is done for all aspect ratios. The aspect ratio which has the minimum delay and average power dissipation is selected as the optimum aspect ratio. Further work is performed with this aspect ratio.

5.4 Optimum number of Repeaters

Once the aspect ratio is fixed, the number of optimum repeaters is calculated. For this interconnect RLC distributed model is used. The resistance, inductance and capacitance gets divided in this model as shown in Fig. For *n* repeaters, the value of R, L and C gets divided by *n*+1 among the model. The rise time, fall time and average delay is calculated for different number of repeaters from simulation. The number of repeaters which give the minimum average delay is selected as the optimum number of repeaters. It is observed that the delay decreases as the number of repeaters is increased up to a point after which the delay starts increasing and so does power dissipation.

5.5 Performance analysis of MWCNT at global length of interconnect

The equivalent circuit of interconnect formed by CNT bundle is used to SPICE-simulate signal propagation down the MWCNT interconnect for 22nm technology node at different lengths. The clock speed is 100MHz. Simulation is carried out for copper interconnects for same technology and lengths at the same clock speed. For the sake of comparison the load capacitance is kept same for both the cases. Optimum number of repeaters has been found out to get the optimum performance for both MWCNT and copper.

5.5.1 Propagation delay analysis

The 90% delay has been extracted for both MWCNT and copper interconnects using SPICE simulation results. Predictive Technology Model (PTM) has been used for CMOS driver [61]. Copper interconnect propagation delay is used to normalize corresponding MWCNT delays. This ratio will be referred to as normalized delay from now on. The variation of this normalized delay with line length is shown in Fig. 5.8. It is observed that the normalized delay decreases with increase in interconnect length. This is due to the dominance of lower value of resistance and inductance in MWCNT as compared to copper counterpart.

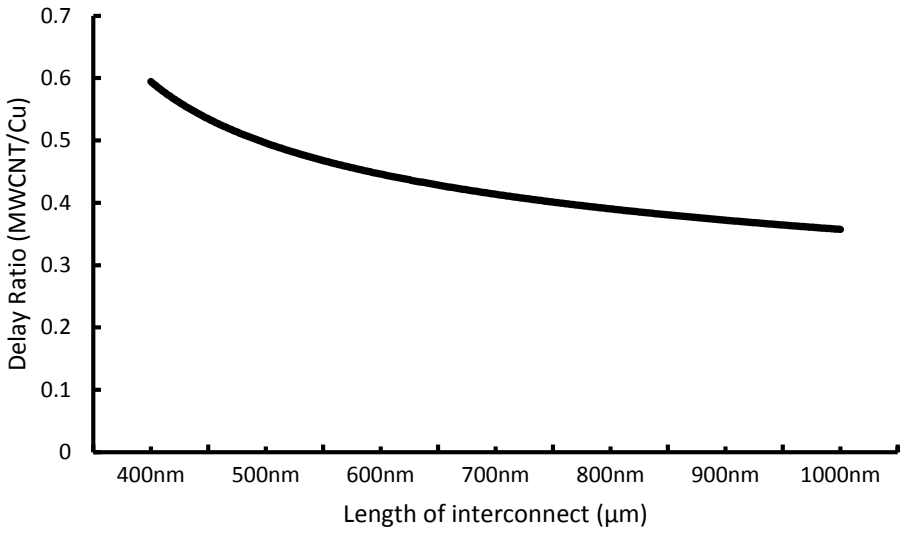

Figure 5.8 Delay ratio as a function of interconnect length.

5.5.2 Power dissipation analysis

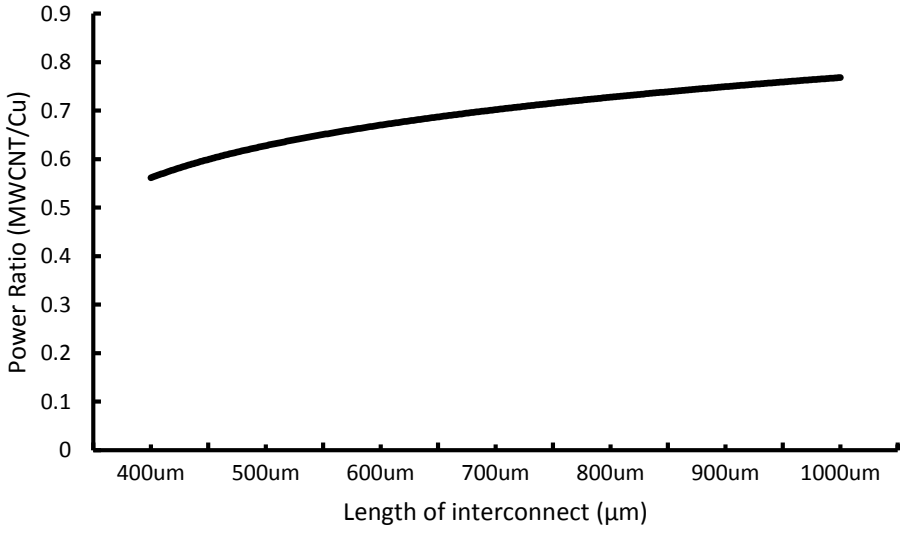

Figure 5.9 Power ratio as a function of interconnect length.

The ratio of power dissipation in MWCNT and copper interconnects at different line lengths has been illustrated in Fig. 5.9. It has been seen that the MWCNT is of lower power dissipation for all semi global and global length interconnect. Result also reveals that the ratio increases with increase in interconnect length. This is due to the fact that as the line length increases, the capacitance becomes more dominating in MWCNT.

5.5.3 Power Delay Product analysis

Fig. 5.10 shows Power Delay product *PDP* as a function of line length. It is observed that PDP decreases nominally because the decrease in propagation delay is little but more dominating than increase in power dissipation. This is attributed to the fact that decrease in resistance is more prominent than increase in capacitance.

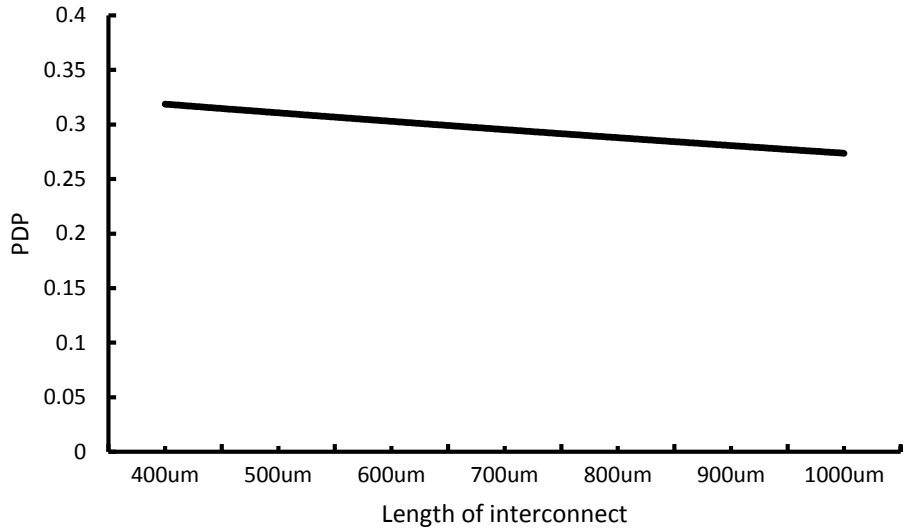

Figure 5.10 Power-Delay product as a function of interconnect length.

5.6 Influence of tube diameter on performance of MWCNT interconnect

5.6.1 Propagation delay

90% delay has been calculated using SPICE simulated results at different tube diameters inside the bundle. Power dissipation is also observed for the same. Fig. 5.11 shows the variation of propagation delay through interconnect at different tube diameters. It is observed that the delay is decreasing as the tube diameter increases. This is due to the fact that the resistance of interconnect decreases as the diameter increases.

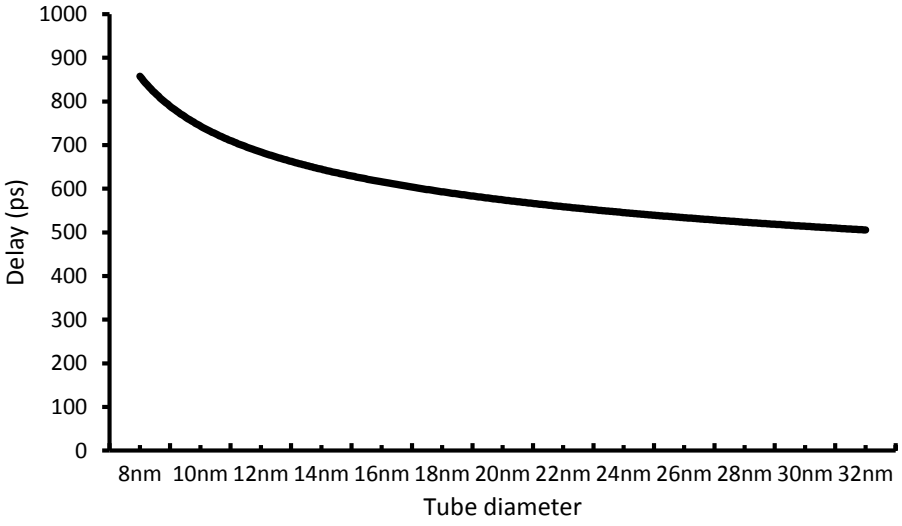

Figure 5.11 Propagation delay as a function of tube diameter.

5.6.2 Power dissipation

Fig. 5.12 shows the power dissipation as a function of tube diameter. It is observed that power increases as the tube diameter increases. The increase in power dissipation is due to increase in capacitance of interconnect due to which dynamic power dissipation increases.

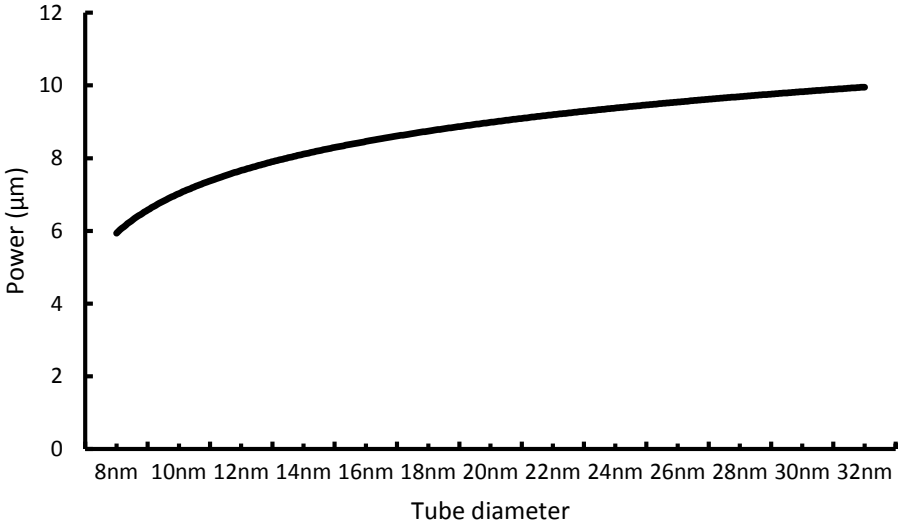

Figure 5.12 Power dissipation as a function of tube diameter.

5.6.3 Power Delay product

Fig. 5.13 shows the power delay product *PDP* as a function of tube diameter. It is observed that *PDP* remains almost constant and independent of the tube diameter. This is because the

effect of resistance, i.e., decrease in delay, and the effect of capacitance, i.e., increase in power dissipation are moderate and thus negate each other.

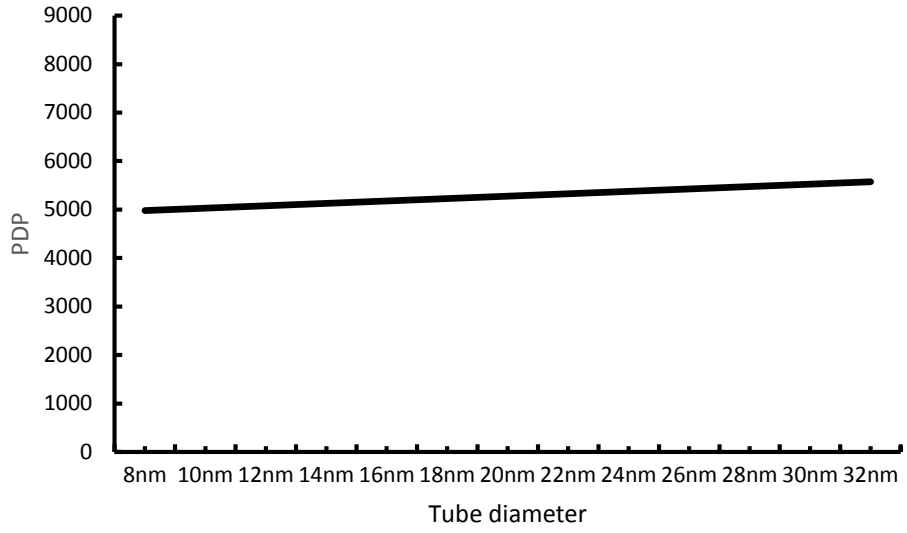

Figure 5.13 Power-Delay product as a function of tube diameter.

5.7 Comparison of MWCNT with optical interconnects at global lengths

Optical interconnects are a potential candidate for future VLSI interconnects. They have been discussed in brief in the previous chapters. In this section, the performance in terms of propagation delay, power dissipation and PDP of MWCNT is compared to optical interconnects.

5.7.1 Propagation delay analysis

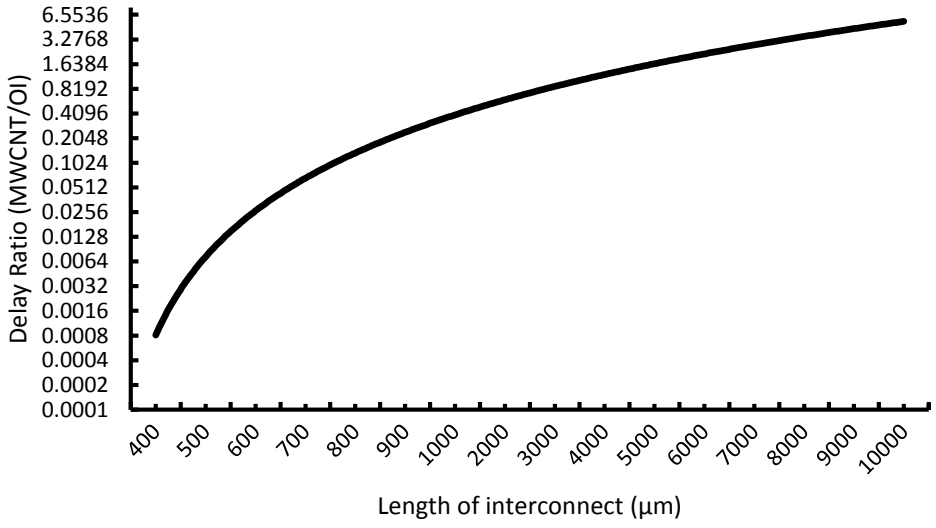

Figure 5.14 Delay ratio as a function of interconnect length.

The delay through MWCNT interconnect and optical interconnect at different interconnect lengths is calculated. Delay through optical interconnect is used to normalize the MWCNT delay. Fig. 5.14 shows this normalized delay as a function of interconnect length. It can be seen that the ratio increases as the length increases and it becomes greater than unity as the length becomes greater than 2000μm. This shows that after this length, optical interconnect gives better delay than MWCNT and before this length, MWCNT is better in terms of delay. This is attributed to the fact that impedance parameters of MWCNT increase linearly with length, and thus, delay increases likewise, whereas the delay in optical interconnect increases by very small amount with increase in length.

5.7.2 Power analysis

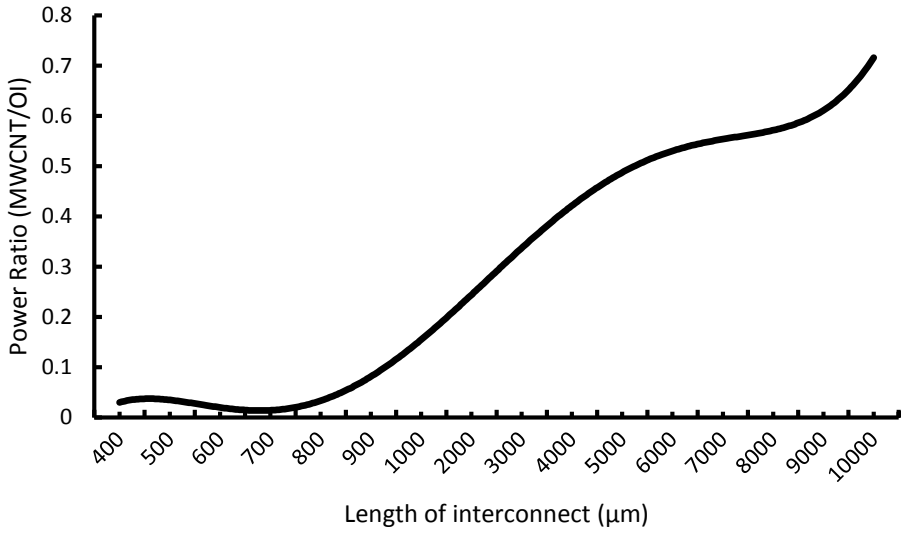

Figure 5.15 Power ratio as a function of interconnect length.

SPICE simulations are used to calculate power dissipation for optical interconnect and MWCNT interconnect at different lengths of interconnect. Power dissipation in optical interconnect is used to normalize power dissipation in MWCNT. This normalized power is shown in Fig. 5.15. It can be seen that the ratio increases as the line length increases. It is because in MWCNT, capacitance increases with length while power dissipation in optical interconnect is independent of the line length as the line is lossless. The transmitter and receiver circuitry is the source of power dissipation in optical interconnect system.

5.7.3 Power Delay Product analysis

Power delay product is shown as a function of line length at global lengths in Fig. 5.16. It is seen that it increases with line length. This is because both delay and power increase as a function of length due to the combined effect of impedance parameters, i.e., resistance, inductance and capacitance.

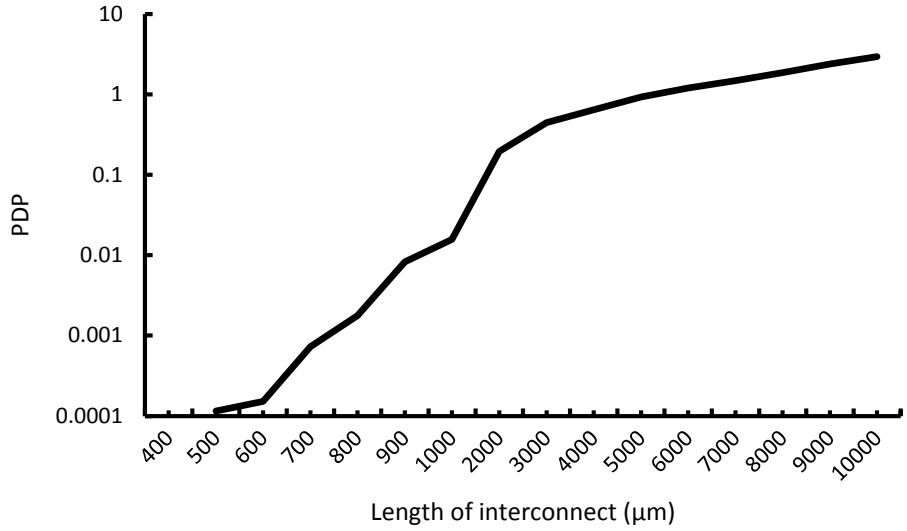

Figure 5.16 Power-Delay product as a function of interconnect length.

5.8 Conclusion

Performance analysis in terms of propagation delay and power dissipation at 22nm technology node for global lengths indicate that MWCNT is a more preferable choice for global interconnects compared to copper. The performance of MWCNT increases as the line length increases. Also the performance of MWCNT at different tube diameters indicate that propagation delay improves as the tube diameter increases. Performance analysis in terms of propagation delay and power dissipation between MWCNT and optical interconnects at global lengths reveal that MWCNT performs better than optical interconnects up to a certain length after which the performance of optical interconnect is better.

CHAPTER

6

Conclusions and Future Scope

6.1 Introduction

All the analysis are carried out in this dissertation at 22nm technology for global lengths of interconnects. SPICE simulations are carried out using 54 level model files given in appendix A1. Predictive Technology model (PTM) is used to model the CMOS driver. Propagation delay comparisons are done for 90% delay.

6.2 Carbon nanotube as VLSI interconnect

Carbon nanotubes are a potential candidate for future VLSI interconnects due to their unique properties and resistance to effects like electro migration and diffusion barrier width which affect copper and degrade its performance with scaling. More controlled fabrication process is required to control the chirality of CNTs so that more tubes contribute to current conduction. Optical interconnects are a potential candidate for chip to chip interconnects and on-chip interconnects and should be studied for the same.

6.3 Analytical results

Piece-wise transient analysis was performed for interconnect at global length. Analytical model using alpha-power law for MOS model driving a π-RLC interconnect has been used to predict the response of the circuit for a fast ramp input signal. The results show that there is a marginal difference between the voltage levels of analytical results and SPICE simulated results during discharging process. The discharging time is same for both cases. Driver interconnect model using alpha-power MOS model was used and it is shown that the trend of predicted output deviated from the SPICE simulated waveform. Improved models are required to predict the response of circuit more accurately for smaller technologies

6.4 Influence of tube parameters on delay and power dissipation

Performance analysis in terms of propagation delay and power dissipation between MWCNT and copper interconnects at global lengths indicate that MWCNT is a more preferable choice

for global interconnects. The performance of MWCNT increases as the line length increases. For global lengths of interconnect, densely packed MWCNT bundle interconnect show better results than their copper counterparts in spite of the presence of imperfect metal-nanotube contacts. Also the performance analysis in terms of propagation delay and power dissipation for different tube diameters at global length of interconnect is carried out. The analysis of MWCNT at different tube diameters indicate that propagation delay improves as the tube diameter increases. Performance analysis in terms of propagation delay and power dissipation between MWCNT and optical interconnects at global lengths reveal that MWCNT performs better than optical interconnects up to a certain length after which the performance of optical interconnect is better. The choice of interconnect could be made on this critical value of length. For interconnects longer than this critical value, optical interconnects could be used and for lengths shorter than this value, MWCNT could be used. Optical interconnects should be preferred when chip area is not a critical issue, or when chip area is easily available.

6.5 Future scope

Many materials have been proposed by researchers as potential candidates for future VLSI interconnects, carbon nanotubes being one of them, others are Graphene Nano Ribbon (GNR) and optical interconnects. GNRs show potential for high performance for local level of interconnects and need to be analysed on all key parameters. Optical interconnects show great potential in the global level of interconnects. Crosstalk and noise immunity are still to be analysed. Integration of waveguides, detector and receiver on a chip is a key field of research for optical interconnects. Use of different interconnect materials inside the bundle such as Mixed CNT interconnect, in which there are SWCNTs and MWCNTs connected in parallel to form the interconnect, are being emphasized. Interesting and productive research on these kind of interconnects on the basis of cross-talk, temperature dependence of performance and cross-talk could be carried out.

List of Publications

Mohit, Mayank Kumar Rai, "Performance analysis of Multi Walled Carbon Nanotube interconnect for future VLSI applications", *Proc. International conference on Innovations in Electrical, Electronics and Computer Science Engineering*, pp. 38-41, June 2014.

REFERENCES

[1] H. B. Bakoglu, “Circuits, interconnections and Packaging for VLSI”, *Addison-Wesley, Reading* , MA, 1990.

[2] Y.I. Ismail, E.G. Friedman, “Effects of inductance on the propagation delay and repeater insertion in VLSI circuits”, *IEEE Trans. VLSI Syst*. Vol. 8 pp. 195–206, 2000.

[3] Adler, V. and Friedman, E.G., “Repeater design to reduce delay and power in resistive interconnects”, *IEEE Transactions on Circuits and Systems-II: Analog and Digital Signal Processing*, Vol. 45 No. 5, pp. 607-16, 1998.

[4] W. C. Elmore, “The transient response of damped linear networks with particular regard to wide-band amplifiers”, *Journal of Applied Physics*, Vol. 19, pp. 55–63, Jan. 1948.

[5] A.B. Kahng, S. Muddu, “Efficient gate delay modeling for large interconnect loads”, *IEEE Multi-Chip Module Conf.*, pp. 202–207, 1996.

[6] F. Dartu, N. Menezes, J. Qian, L.T. Pillage, “A gate-delay model for high-speed CMOS circuits”, *Proceedings of the 31st IEEE Conference on Design Automation*, pp. 576– 580, 1994.

[7] T. Sakurai, "Closed form expression for interconnection delay, coupling and crosstalk in VLSI's", *IEEE Trans. Electron Devices*, Vol. 40, pp.118 – 124, 1993.

[8] B. Krauter, B. Tutuianu, J. Willis, and L.T. Pileggi, "The Elmore Delay as a Bound for RC Trees with Generalized Input Signals", in *Proc. DAC*, pp. 364-369, 1995.

[9] A. B. Kahng, S. Muddu, and E. Sarto, "On switch-factor based analysis of coupled RC interconnects", *Proc. DAC*, pp. 79 - 84, 2000.

[10] F. Dartu and L. T. Pileggi, "Calculating worst-case gate delays due to dominant capacitance coupling", *Proc. DAC*, pp. 46 – 51, 1997.

[11] Y. I. Ismail and E. G. Friedman, “Sensitivity of Interconnect Delay to On-Chip Inductance”, *ISCAS*, pp. 403-409, 2000.

[12] Bakoglu, H.B. and Meindl, J.D., “Optimal interconnection circuits for VLSI”, *IEEE Transactions on Electron Devices*, Vol. 32 No. 5, pp. 903-9, 1985.

[13] Davis, J.A., Meindl, J.D., "Compact distributed RLC interconnect models—Part I: single line transient, time delay and overshoot expressions", *IEEE Trans. Electron Dev.* Vol. 47 , pp. 2068–2077, 2000.

[14] J.A. Davis, J.D. Meindl, "Compact distributed RLC interconnect models—Part II: coupled line transient expressions and peak crosstalk in multilevel interconnect networks", *IEEE Trans. Electron Dev.* Vol. 47, pp. 2078–2087, 2000.

[15] R. Venkatesan, J.A. Davis, J.D. Meindl, "Compact distributed RLC interconnect models—Part III: transients in single and coupled lines with capacitive load termination", *IEEE Trans. Electron Dev.* Vol. 50, pp. 1081–1093, 2003.

[16] R. Venkatesan, J.A. Davis, J.D. Meindl, "Compact distributed RLC interconnect models—Part IV: unified models for time delay, crosstalk, and repeater insertion", *IEEE Trans. Electron Dev.* Vol. 50, pp. 1094–1102, 2003.

[17] Sakurai, T. and Newton, A.R., "Alpha power law MOSFET model and its applications to CMOS inverter delay and other formulas", *IEEE Journal of Solid State Circuits*, Vol. 25 No. 2, pp. 584-94, 1990.

[18] A. Chatzigeorgiou, S. Nikolaidis, I. Tsoukalas, "Modelling CMOS gates driving RC interconnect loads", *IEEE Trans. Circuits Systems—II: Analog Digital Signal Process*. 48 (4), pp. 413–418, 2001.

[19] B.K. Kaushik, S. Sarkar, R.P. Agarwal, "Waveform analysis and delay prediction for a CMOS gate driving RLC interconnect load", *Integration, the VLSI journal* 40, pp. 394–405, 2007.

[20] F. Kreupel, AP Graham , G. S Duesberg, W. Steinhogl, M. Liebau, E. Unger and W. Honlein, "Carbon Nanotubes in Interconnect Applications", *Microelectronic Engineering*, Vol. 64, pp. 399-408, 2002.

[21] J Li, Q Ye, A. M. Cassell, H. T. Ng, R Stevens, J Han and M Meyyapan, " Bottom-up Approach of Carbon Nanotube Interconnects", *Applied physics Letters*, Vol 82, no. 15, pp 2491, April 2003.

[22] Navin Srivastava and Kaustav Banerjee, "Performance analysis of CNT interconnects for VLSI applications", *IEEE/ACM Intl. Conf. on ICCAD*, pp. 383-390, 2005.

[23] N. Srivastava, R.V. Joshi and K. Banerjee, "Carbon Nanotube Interconnects: Implications for Performance, Power Dissipation and Thermal Management", *IEDM*, pp. 257-260, 2005.

[24] J Li, Q Ye, A.M. Cassell, J. Koehne , H T Ng, J Han and M Meyyapan, "Carbon Nanotube interconnects: A Process Solution", *IEEE International Interconnect Tech Conference*, pp. 271, 2007.

[25] Y. Massoud and A. Nieuwoudt, *IEEE Symp*. Circuits Syst., pp. 792, 2009.

[26] H. Li, N. Srivastava, J. Mao, W. Yin and K. Banerjee, "Carbon Nanotube Vias: A Reality Check", *IEEE Transactions on Electron Devices*, Vol. 65 No. 6, pp. 207-10, 2007.

[27] C. Thiruvenkatesan, J. Raja, "Studies on the Application of Carbon Nanotube as Interconnects for Nanometric VLSI Circuits", *ICETET* 09, pp. 162-167, 2009.

[28] B. Vivo, P. Lamberti, G. Spinelli, V. Tucci, "Reliable bounds for the propagation delay in VLSI nano interconnects based on Multi Wall Carbon Nano Tubes", *IEEE*, pp. 149-152, 2010.

[29] Mayank Kumar Rai and Sankar Sarkar, "Influence of tube diameter on carbon nanotube interconnect delay and power output", 2011, *Phys. Status Solidi A*, pp. 1–5.

[30] Mayank Kumar Rai, Nivedita and Sankar Sarkar, "Carbon Nanotube Based Interconnects for VLSI Application", IE (I) *Journal-ET*, Vol. 91, pp. 3-6, 2011.

[31] Hong Li, Wen-Yan Yin, Kaustav Banerjee and Jun-Fa Mao, "Circuit Modeling and Performance Analysis of Multi-Walled Carbon Nanotube Interconnects", *IEEE Transactions on Electron Devs*, Vol. 55, no. 6, June 2008.

[32] Azad Naeemi and James D. Meindl, "Compact Physical Models for Multiwall Carbon-Nanotube Interconnects", *IEEE Electron Device Letters*, Vol. 27, No. 5, May 2006.

[33] Azad Naeemi and James D. Meindl, "Physical Modeling of Temperature Coefficient of Resistance for Single and Multi-Wall Carbon Nanotube Interconnects", *IEEE Electron Device Letters*, Vol. 28, No. 2, February 2007.

[34] Arthur Nieuwoudt and Yehia Massoud, "RC Circuit Model for Multi-Walled Carbon Nanotubes", Proceedings of the *7th IEEE International Conference on Nanotechnology*, Hong Kong, August 2 - 5, 2007.

[35] Yao Xu, Ashok Srivastava and Ashwani K. Sharma, "A Model of Multi-Walled Carbon Nanotube Interconnects".

[36] Manoj Kumar Majumder, B. K. Kaushik and S. K. Manhas, "A Comparative Analysis of Single Walled CNT Bundle and Multi Walled CNT as Future Global VLSI Interconnects", Proceedings published by *International Journal of*

Computer Applications® (IJCA) International Conference on Networks and Computer Communications (ETNCC) 2011.

[37] H. J. Li, W. G. Lu, J. J. Li, X. D. Bai, and C. Z. Gu, "Multichannel Ballistic Transport in Multiwall Carbon Nanotubes", *Physical Review letters* 95, 086601, 2005.

[38] Maria Sabrina Sarto and Alessio Tamburrano, "Single-Conductor Transmission-Line Model of Multiwall Carbon Nanotubes", *IEEE Transactions on Electromagnetic compatibility*, Vol. 52, no. 2, May 2010.

[39] Yograj Singh Duksh, Brajesh Kumar Kaushik, Sankar Sarkar and Raghuvir Singh, "Effect of Driver Size and Number of Shells on Propagation Delay in MWCNT Interconnects", *ICDeCom, International Conference* on 24-25 Feb. 2011.

[40] Kyung-Hoae Koo, Hoyeol Cho, Pawan Kapur and Krishna C. Saraswat, "Performance Comparisons between Carbon Nanotubes, Optical, and Cu for Future High-Performance On-Chip Interconnect Applications", *IEEE Transaction on Electron Devices*, Vol. 54, no. 12, December 2007.

[41] John P. Uyemura, "Introduction to VLSI Circuits and Systems", *Wiley, John & Sons, Inc.*, 2002.

[42] Mayank Kumar Rai and Sankar Sarkar, "Carbon Nano Tube as VLSI Interconnect", *Electronic Property of Carbon Nanotube*, chapter 22, June 2011.

[43] Naeemi et al., "Performance comparison between carbon nanotube and copper interconnects for giga scale integration (GSI)", *Electron Device letters*, Vol. 26, No. 2, pp. 84-86, 2005.

[44] W. Steinhogl, et al., "Size-dependent Resistivity of Metallic Wires in the Mesoscopic Range", *Physical Review B*, Vol. 66, 075414, 2002.

[45] P. Kapur, J.P. Vittie and K. C. Saraswat, "Technology and Reliability Constrainted Future Copper Interconnects-Part I: Resistance Modelling", *IEEE Transactions on Electron Devices*, Vol. No. 49, pp. 590-597, 2002.

[46] Online available: http://www.stanford.edu/class/ee311/NOTES/InterconnectScaling.pdf.///Scaling of interconnect EE 311 Notes/Prof Saraswat.

[47] Wai-Kai Chen, Design automation, languages, and simulations, *CRC Press*, 2003.

[48] El-Moursy, M.A. and Friedman, E.G., "Optimum wire sizing of RLC interconnect with repeaters", *Integration, the VLSI journal*, Vol. 38, pp. 205-225, 2004.

[49] Schaper, L , Amey, D., "Improved Electrical Performance Required for Future MOS", *ITCHM*, Vol. 6, pp. 283 – 89, 1983.

[50] Deodhar, V.V. and Davis, J.A., "Voltage scaling and repeater insertion for high throughput low-power interconnects", *ISCAS* '05‖, Vol. 5, pp. 349-352, 2005.

[51] Kang, S.M. and Leblebici, Y., "CMOS Digital Integrated Circuits – Analysis and Design", *TMH, New York*, 2003.

[52] Mayank Kumar Rai and Sankar Sarkar, "Influence of tube diameter on carbon nanotube interconnect delay and power output", *PSS A* Vol. 208, pp. 735-739, 12 January 2011.

[53] F. Leonard and M. P. Anantram, "Physics of carbon nanotube electronic devices", IPP *Reports on Progress in Physics*, 69, pp-507-561, 2006.

[54] P J Burke, "Luttinger Liquid Theory as a Model of the Gigahertz Electrical Properties of Carbon nanotubes", *IEEE Transactions on Nanotechnology*, Vol 1, no 3, pp. 129-144, 2002.

[55] Chuan Xu, Hong Li and Kaustav Banerjee, "Graphene Nano-Ribbon (GNR) Interconnects: A Genuine Contender or a Delusive Dream?" Department of Electrical and Computer Engineering, University of California, Santa Barbara, CA 93106, USA.

[56] David A. B. Miller "*Optical Interconnects" IAA Workshop*, Stanford University, 2008.

[57] A. Naeemi and J. D. Meindl, "Monolayer metallic interconnects: promising candidates for short local interconnects", *Electron device letters*, Vol. 26, No. 8, pp. 544-546, 2005.

[58] O. Kibar, D. A. V. Blerkom, C. Fan and S. C. Esener, "Power minimization and technology comparison for Digital free-space optoelectronic interconnection", *Journal of Lightwave Tech.*, Vol. 17, no. 4, April 1999.

[59] Y. Li, E. Towe, and M. W. Haney, "Special issue on optical interconnections for digital systems," *Proc. of the IEEE*, Vol. 88, no. 6, pp. 723-727, June 2000.

[60] Z. Qi, M. R. Stan, "Accurate back-of-the-envelope transistor model for deep sub-micron MOS", *IEEE International Conference on Microelectronic System Education*, 2007.

[61] Predictive Technology Model[Online].www.eas.asu.edu/ ptm/.

A.1

Appendix

.model nmos nmos level = 54

+version = 4.0 binunit = 1 paramchk= 1 mobmod = 0

+capmod = 2 igcmod = 1 igbmod = 1 geomod = 1

+diomod = 1 rdsmod = 0 rbodymod= 1 rgatemod= 1

+permod = 1 acnqsmod= 0 trnqsmod= 0

+tnom = 27 toxe = 6.5e-010 toxp = 4e-010 toxm = 6.5e-010

+dtox = 2.5e-010 epsrox = 3.9 wint = 5e-009 lint = 1.35e-009

+ll = 0 wl = 0 lln = 1 wln = 1

+lw = 0 ww = 0 lwn = 1 wwn = 1

+lwl = 0 wwl = 0 xpart = 0 toxref = 6.5e-010 xl = -9e-9

+dlcig = 1.35e-009

+vth0 = 0.3692 k1 = 0.2 k2 = 0 k3 = 0

+k3b = 0 w0 = 2.5e-006 dvt0 = 1 dvt1 = 2

+dvt2 = 0 dvt0w = 0 dvt1w = 0 dvt2w = 0

+dsub = 0.078 minv = 0.05 voffl = 0 dvtp0 = 1e-011

+dvtp1 = 0.1 lpe0 = 0 lpeb = 0 xj = 7.2e-009

+ngate = 1e+023 ndep = 1.2e+019 nsd = 2e+020 phin = 0

+cdsc = 0 cdscb = 0 cdscd = 0 cit = 0

+voff = -0.13 nfactor = 2.3 eta0 = 0.0045 etab = 0

+vfb = -1.058 u0 = 0.0181 ua = -5e-010 ub = 1.7e-018

+uc = 0 vsat = 200000 a0 = 1 ags = 0

+a1 = 0 a2 = 1 b0 = 0 b1 = 0

+keta = 0.04 dwg = 0 dwb = 0 pclm = 0.06

+pdiblc1 = 0.001 pdiblc2 = 0.001 pdiblcb = -0.005 drout = 0.5

+pvag = 1e-020 delta = 0.01 pscbe1 = 2.0e+009 pscbe2 = 1e-007

+fprout = 0.2 pdits = 0.01 pditsd = 0.23 pditsl = 2300000

+rsh = 5 rdsw = 60 rsw = 30 rdw = 30

+rdswmin = 0 rdwmin = 0 rswmin = 0 prwg = 0

+prwb = 0 wr = 1 alpha0 = 0.074 alpha1 = 0.005

+beta0 = 30 agidl = 0.0002 bgidl = 2.1e+009 cgidl = 0.0002

+egidl = 0.8 aigbacc = 0.012 bigbacc = 0.0028 cigbacc = 0.002

+nigbacc = 1 aigbinv = 0.014 bigbinv = 0.004 cigbinv = 0.004

+eigbinv = 1.1 nigbinv = 3 aigc = 0.0213 bigc = 0.0025889

+cigc = 0.002 aigsd = 0.0213 bigsd = 0.0025889 cigsd = 0.002

+nigc = 1 poxedge = 1 pigcd = 1 ntox = 1

+xrcrg1 = 12 xrcrg2 = 5

+cgso = 7e-011 cgdo = 7e-011 cgbo = 0 cgdl = 7.5e-013

+cgsl = 7.5e-013 clc = 1e-007 cle = 0.6 cf = 1.1e-010

+ckappas = 0.6 ckappad = 0.6 vfbcv = -1 acde = 1

+moin = 15 noff = 1 voffcv = 0

+kt1 = -0.154 kt1l = 0 kt2 = 0.022 ute = -1.1

+ua1 = 1e-009 ub1 = -1e-018 uc1 = -5.6e-011 prt = 0

+at = 33000

+fnoimod = 1 tnoimod = 0 noia = 6.25e+041 noib = 3.125e+026

+noic = 8.75e+009 em = 41000000 af = 1 ef = 1

+kf = 0 tnoia = 1.5 tnoib = 3.5 ntnoi = 1

+jss = 1.2e-006 jsws = 2.4e-013 jswgs = 2.4e-013 njs = 1

+ijthsfwd= 0.1 ijthsrev= 0.1 bvs = 10 xjbvs = 1

+jsd = 1.2e-006 jswd = 2.4e-013 jswgd = 2.4e-013 xjbvd = 1

+pbs = 1 cjs = 0.0018 mjs = 0.5 pbsws = 1

+cjsws = 1.2e-010 mjsws = 0.33 cjswgs = 2.1e-010 cjd = 0.0018

+cjswd = 1.2e-010 mjswd = 0.33 pbswgd = 1 cjswgd = 2.1e-010

+mjswgd = 0.33 tpb = 0 tcj = 0 tpbsw = 0

+tcjsw = 0 tpbswg = 0 tcjswg = 0 xtis = 3

+dmcg = 0 dmci = 0 dmdg = 0 dmcgt = 0

+dwj = 0 xgw = 0 xgl = 0

+rshg = 0.4 gbmin = 1e-010 rbpb = 5 rbpd = 15

+rbps = 15 rbdb = 15 rbsb = 15 ngcon = 1

.model pmos pmos level = 54

+version = 4.0 binunit = 1 paramchk= 1 mobmod = 0

+capmod = 2 igcmod = 1 igbmod = 1 geomod = 1

+diomod = 1 rdsmod = 0 rbodymod= 1 rgatemod= 1

+permod = 1 acnqsmod= 0 trnqsmod= 0

+tnom = 27 toxe = 6.7e-010 toxp = 4e-010 toxm = 6.7e-010

+dtox = 2.7e-010 epsrox = 3.9 wint = 5e-009 lint = 1.35e-009

+ll = 0 wl = 0 lln = 1 wln = 1

+lw = 0 ww = 0 lwn = 1 wwn = 1

+lwl = 0 wwl = 0 xpart = 0 toxref = 6.7e-010 xl = -9e-9

+dlcig = 1.35e-009

+vth0 = -0.25399 k1 = 0.2 k2 = -0.01 k3 = 0

+k3b = 0 w0 = 2.5e-006 dvt0 = 1 dvt1 = 2

+dvt2 = -0.032 dvt0w = 0 dvt1w = 0 dvt2w = 0

+dsub = 0.1 minv = 0.05 voffl = 0 dvtp0 = 1e-011

+dvtp1 = 0.05 lpe0 = 0 lpeb = 0 xj = 7.2e-009

+ngate = 1e+023 ndep = 4.4e+018 nsd = 2e+020 phin = 0

+cdsc = 0 cdscb = 0 cdscd = 0 cit = 0

+voff = -0.13 nfactor = 2.3 eta0 = 0.0037 etab = 0

+vfb = -1.058 u0 = 0.0023 ua = -5e-010 ub = 1.6e-018

+uc = 0 vsat = 78000 a0 = 1 ags = 1e-020

+a1 = 0 a2 = 1 b0 = 0 b1 = 0

+keta = -0.047 dwg = 0 dwb = 0 pclm = 0.1

+pdiblc1 = 0.001 pdiblc2 = 0.001 pdiblcb = 3.4e-008 drout = 0.6

+pvag = 1e-020 delta = 0.01 pscbe1 = 2e+009 pscbe2 = 9.58e-007

+fprout = 0.2 pdits = 0.08 pditsd = 0.23 pditsl = 2300000

+rsh = 5 rdsw = 60 rsw = 30 rdw = 30

+rdswmin = 0 rdwmin = 0 rswmin = 0 prwg = 0

+prwb = 0 wr = 1 alpha0 = 0.074 alpha1 = 0.005

+beta0 = 30 agidl = 0.0002 bgidl = 2.1e+009 cgidl = 0.0002

+egidl = 0.8 aigbacc = 0.012 bigbacc = 0.0028 cigbacc = 0.002

+nigbacc = 1 aigbinv = 0.014 bigbinv = 0.004 cigbinv = 0.004

+eigbinv = 1.1 nigbinv = 3 aigc = 0.012731 bigc = 0.00115

+cigc = 0.0008 aigsd = 0.012731 bigsd = 0.00115 cigsd = 0.0008

+nigc = 1 poxedge = 1 pigcd = 1 ntox = 1

+xrcrg1 = 12 xrcrg2 = 5

+cgso = 7e-011 cgdo = 7e-011 cgbo = 0 cgdl = 3e-011

+cgsl = 3e-011 clc = 1e-007 cle = 0.6 cf = 1.1e-010

+ckappas = 0.6 ckappad = 0.6 vfbcv = -1 acde = 1

+moin = 15 noff = 1 voffcv = 0

+kt1 = -0.14 kt1l = 0 kt2 = 0.022 ute = -1.1

+ua1 = 1e-009 ub1 = -1e-018 uc1 = -5.6e-011 prt = 0

+at = 33000

+fnoimod = 1 tnoimod = 0 noia = 6.25e+041 noib = 3.125e+026

+noic = 8.75e+009 em = 41000000 af = 1 ef = 1

+kf = 0 tnoia = 1.5 tnoib = 3.5 ntnoi = 1

+jss = 2e-007 jsws = 4e-013 jswgs = 4e-013 njs = 1

+ijthsfwd= 0.1 ijthsrev= 0.1 bvs = 10 xjbvs = 1

+jsd = 2e-007 jswd = 4e-013 jswgd = 4e-013 xjbvd = 1

+pbs = 1 cjs = 0.0015 mjs = 0.5 pbsws = 1

+cjsws = 9.4e-011 mjsws = 0.33 cjswgs = 2e-010 cjd = 0.0015

+cjswd = 9.4e-011 mjswd = 0.33 pbswgd = 1 cjswgd = 2e-010

+mjswgd = 0.33 tpb = 0 tcj = 0 tpbsw = 0

+tcjsw = 0 tpbswg = 0 tcjswg = 0 xtis = 3

+dmcg = 0 dmdg = 0 dmcgt = 0 xgw = 0

+xgl = 0

+rshg = 0.1 gbmin = 1e-012 rbpb = 50 rbpd = 50

+rbps = 50 rbdb = 50 rbsb = 50 ngcon = 1