Design and Simulation of Low Power and Stable 7T SRAM Cell

Thesis submitted in the partial fulfilment of requirement for the award of degree of

Master of Technology

in

VLSI Design and CAD

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Declaration

I, Nikhil Puri, hereby certify that the work which is being presented in this thesis entitled "**Design and Simulation of Low Power and Stable 7T SRAM Cell** " in partial fulfillment of the requirements for the award of degree of Master of Technology in VLSI Design and CAD from Thapar University (Deemed to be University), Patiala, is an authentic record of my own work carried out under the supervision of Mr. Arun Kumar Chatterjee.

The matter presented in this thesis has not been submitted in any other University / Institute for the award of any other degree.

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Abstract

As the feature sizes decrease, understanding of circuit variations becomes essential to effectively design robust circuits. As the memory devices and circuits are further scaled down various issues come up like stability, leakage and area. It is important to continue looking for alternatives to improve upon the available research. To overcome these challenges, researchers have proposed different topologies for SRAMs with 5T ,7T, 8T and 9T SRAM designs. These designs improve the cell stability but suffer from bitline-leakage, noise, placing constraints on the number of cells shared by each bitline. These designs also have substantial area overhead when compared to the traditional 6T design except the 5T SRAM design.

In this work, the published SRAM designs are characterized using commercial CMOS 180 nm models and are compared based on critical SRAM parameters like read stability, write stability, bitline leakage and read-write delays. Furthermore, a 7T SRAM Cell design is proposed that enhances data stability and simultaneously addresses the bitline leakage problem. The goal is to improve the parameters of the cache memory array without adding too much area overhead. The design metrics for the 7T cell are discussed in detail and performance and stability are evaluated. It is shown that although the area of the memory array has increased by 13% but the performance has increased considerably. The new cell also has 30% lower total leakage current and 50% more stability during read.

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CHAPTER 1 INTRODUCTION

1.1 Overview

The era of low power microelectronics began with the invention of the transistor in the late 1940's and came of age with the invention of the integrated circuit in the late 1950's. - James D. Meindl [1]

To continue to grow according to the Moore's law, we need to continuously be able to reduce the cost per transistor or the cost per function performed by a microchip. And with this in mind, low power electronics was conceived. In search for better alternatives so as to reduce power consumption in a chip, we moved from transistor-transistor logic (TTL) and emitter coupled logic (ECL) to complementary metal oxide semiconductor (CMOS) technology.

Initially working with CMOS was excellent since unlike earlier technologies, there was almost negligible static power dissipation. But as we continue to scale down the technology and continue to shrink the transistor sizes, inherent parasitic passive elements have started to surface and disturbed our harmony with standard CMOS logic style. As we continue to reduce both the supply voltage and threshold voltage of a MOSFET, subtheshold leakage is bound to increase [1-2]. Low power electronics is especially important in the domain of memory design.

Since memory is one component found on almost every digital system that involves some processing no matter how small. Currently we memories constitute a large portion of the chip area and if we can reduce the power consumption of memories, we will be able to affect a almost all types of systems.

Memory is a very important part of a computer system. Modern memory system implements the concept of the memory hierarchy. While a flat memory built using a single technology and single concept is lucrative for its simplicity, a well-implemented hierarchy allows a memory system to approach simultaneously the performance of the fastest component, the cost per bit of the cheapest component, and the energy consumption of the most energy-efficient component. A memory in terms of computer hardware is a storage unit. There are many different types of hardware used for storage, such as magnetic hard drives and tapes, optical discs such as CDs and DVDs, and electronic memory in form of integrated memory or stand-alone chips. In this thesis, only the electronic memory has been discussed, and more specifically, random access memories (RAM).

Since the birth of modern computing systems, storage technologies have been an active area of research. Today, a number of memory devices of different types coexist. Though the primary functionality of every type of memory device is to allow storage and retrieval of data, they differ in terms of certain core characteristics. A typical embedded system contains a mixture of different types of memory devices, each chosen to play a specific role in the memory hierarchy. However, the choice of the type of memory device to be used for a certain purpose is more often than not governed by the intended application of the embedded system which in turn drives its cost and performance requirements. Memory is at a premium in an embedded system, of whatever type it may be. Thus, a good embedded programmer recognizes the need to minimize the memory footprint of his program.

1.2 Types of memories

I have listed various types of memories using a table given below. It gives an overview of all basic types of commercial memories.

Read-Write Memory		Non-Volatile Read-Write Memory	Read-Only Memory
Random Access	**Non-Random Access**	EPROM E^2PROM FLASH	Mask-Programmed Programmable (PROM)
SRAM DRAM	FIFO LIFO Shift Register CAM		

Figure 1.1: Types of memories

My focus is mainly on the random access memories because this is the area where any improvement would lead to an improvement in memory hierarchy. Many types of memory devices exist today for use in an embedded device. From an embedded programmer's point of view, they fall into three broad categories:

1.2.1 Read Only Memory (ROM)

Read Only Memory [2], as the name suggests, is a class of storage medium that allows data to be only read, but not written or modified. In certain ROMs changing the data is completely impossible, whereas in others, data can be changed but slowly and with the help of external circuitry. Most ROMs are non-volatile in nature, that is, written data is retained even if the power supply to the device is switched off. ROMs are essential for storing data, since they are non-volatile. However, if large amounts of data need to be stored, the existing ROM technologies become increasingly cost prohibitive. Hence, ROMs are used to store only small pieces of software, close to the processor. Also, since data in a ROM cannot be altered, they do not support self-altering programs. ROM or Masked ROM Simply, a ROM or a Masked ROM refers to a storage device which is fabricated along with the data permanently stored in it (hardwired), and thus can never be modified. These types of ROMs have been in use since the first solid state electronic computers came by. They are still used extensively to store the Initial Boot Loader or firmware programs in computing and embedded systems.

1. Programmable ROM (PROM)

A PROM[2] is one step up from a masked ROM. A PROM when purchased is in an un programmed state. Once the software program that needs to be written onto the PROM has been decided, a special device known as a device programmer is used to load the the program onto the PROM. Once programmed, the contents of the PROM cannot be changed. Due to this characteristic, a PROM belongs to the class of One Time Programmable (OTP) devices.

2. Erasable and Programmable ROM (EPROM)

An EPROM[2] can be programmed multiple times, unlike the PROM. To reprogram an EPROM, it needs to be exposed to an high-intensity ultraviolet light source. A small window on top of an EPROM chip allows the light to reach the underlying circuitry, which then resets, erasing the contained data. Since they can be reprogrammed, EPROMs find use in ROM software development and testing. However, if large amounts of data need to be stored, the existing ROM technologies become increasingly cost prohibitive.

1.2.2 Random Access Memory (RAM)

A Random Access Memory device allows reading and writing data, from and to, any random memory location at any point in time. In other words, the worst case time taken to access any random memory location is a constant and is the same for even the first memory location of the RAM.

1. Static RAM (SRAM)

The two type of RAMs discussed here differ as per the lifetime of the data they store. Static RAMs[2] or SRAMs hold data as long as they are powered on. This is due to the underlying memory cell technology, which uses a group of transistors, specifically MOSFETs to store the 0 or 1 logic state, which is retained till the power supply is on. It is still volatile though; as soon as the power is off, the data is lost.

2. Dynamic RAM (DRAM)

A memory cell in a Dynamic RAM or DRAM[2] on the other hand, uses a capacitor as the data storage element (charged state denoting 1, 0 otherwise), with help from a transistor acting as a gate. Since a capacitor gradually loses its charge, if not recharged, data in a DRAM needs to be refreshed periodically, for it to be held. Since charging a capacitor takes away time and power, DRAMs have higher access time as well as power requirement as compared to SRAMs. However, what makes DRAMs popular is their cost advantage. Given that each memory cell needs only 1 transistor (as opposed to 6 transistors in an SRAM), a DRAM can store more data as compared to an SRAM (approximately 4-6 times more[2]), on a given area of silicon. The refresh overhead is a small price to pay for the larger storage capacity and is often transparently handled by a simple hardware controller or software. Thus, computing devices which do not have a high speed requirement or do not mind increased power consumption, use DRAMs (often in the form of Synchronous DRAMs, or SDRAMs), whereas speed and power critical applications tend towards using SRAMs

1.2.3 Hybrid Memory

With the huge amount of research that has gone into storage technologies, the line between ROMs and RAMs has considerably blurred. Today, there exist several types of memory devices that combine the best features of both ROMs and RAMs. They are categorized under hybrid memories. Most of them are non-volatile, as well as allow Random Access, albeit with a few distinguishing features brought about by the storage technology used.

1. Electrically Erasable and Programmable ROM (EEPROM)

An EEPROM[2] as the name suggests, are derivatives of EPROM which allow the memory to be reprogrammed through electrical circuitry in place (without needing exposure to ultraviolet rays as in the case of an EPROM). Thus they can even handle self-altering programs.

2. Flash

Flash memories[3] are specialized EEPROMs which combine the best features from all worlds. They are fast (faster reads than writes), use a low-cost manufacturing process, are non- volatile, provide higher density for storage and can be electrically programmed in-circuit. There are two types of flash memories in use, NAND and NOR. The NOR type flash memory allows true Random Access, which makes it ideal to replace older technologies like EPROM and even battery powered RAMs. On the other hand NAND flash devices are cheaper and are used for general purpose storage.

3. Non-Volatile (NVRAM)

Whereas EEPROMs have descended from ROMs, an NVRAM[2] is the next logical step for an SRAM. Due to their really low power requirement to allow retention of data, SRAMs, often powered with a battery, act as a pseudo non-volatile, random-access memory device. They are understandably called Pseudo Static RAMs (PSRAMs) or Non-Volatile RAMs (NVRAMs). NVRAMs are costly (cost of SRAM, plus the battery), so in real life applications their use is restricted to storing small amount of critical (but alterable) data, as for example, the network configurations for a mobile device.

1.3 Memory Hierarchy

A typical Embedded System consists of several different types of memory. As we now understand, different types of memory differ in terms of access speed and cost. Typically, high speed memory devices cost more and thus can be used only sparsely, to provide specialized functionality. On the other hand, cheaper and slower memory devices are used for generic purposes, in larger quantities. This situation is expressed as the memory hierarchy[2]. The following types of storage / memory devices feature in the memory hierarchy of a typical embedded system.

1. Primary Storage

Often called the Main Memory of the system, typically a RAM where the instructions and data has been loaded. The main memory is interfaced to the Processor through dedicated data and address buses. The amount of primary storage is magnitudes larger that the on-chip memory and is used for general purpose program execution.

2. Secondary Storage

These are typically, non-volatile memory devices which are externally interfaced to the CPU using specialized and slower (than dedicated system buses) interfaces. The CPU uses a section of the primary storage to read / write data from / to the secondary storage device. The size of the secondary storage is governed by the size of program instructions and data to be stored permanently and is typically at least ten times the size of the primary memory.

3. On-Chip Memory

This type of memory is embedded inside the processor's die, is directly accessible to the processor and consequently has the fastest access times. CPU Registers and Internal RAM/ROM fall into this category. On-Chip Memories are the costliest and smallest in size.

Advantages

On-chip memory is the fastest, highest throughput, lowest latency memory possible in an FPGA-based embedded system. It typically has a latency of only one clock cycle. Also, pipelining can also be implemented during memory transactions, making a throughput of one transaction per clock cycle typical.

Another advantage of on-chip memory is that it requires no additional board space or circuit-board wiring because it is implemented on the FPGA directly.

Disadvantages

While on-chip memory is very fast, it is somewhat limited in capacity. Because most on-chip memory is volatile, it loses its contents when power is disconnected.

Best Applications

The following sections describe the best uses of on-chip memory and consequently of SRAM.

1. Cache

Because it is low latency and high speed, on-chip memory functions very well as cache memory for microprocessors. For example, the Nios II processor uses on-chip memory for its instruction and data caches. The limited capacity of on-chip memory is usually not an issue for caches because they are typically relatively small.

2. Look up Tables (LUT)

For some software programming functions, particularly mathematical functions, it is sometimes fastest to use a LUT to store all the possible outcomes of a function, rather than computing the function in software. On-chip memories work well for this purpose as long as the number of possible outcomes fits reasonably in the capacity of on-chip memory available.

1.4 Caches

The speed at which a processor can execute instructions and interpret data is far higher than the time taken to access a memory location. Thus, the presence of slower memory devices can indeed be a bottleneck to the performance of the processor and the system as a whole.

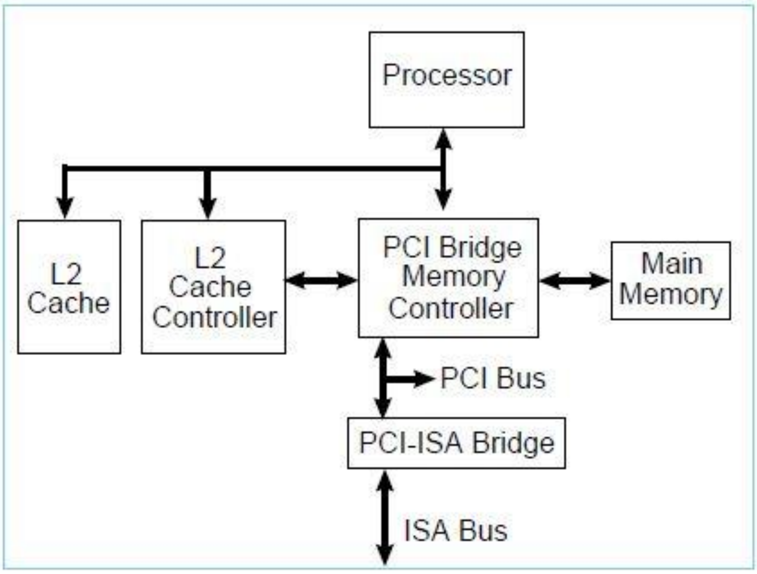

Figure 1.2: Cache Hierarchy[3]

A well designed embedded system should perform as if all the memory were fast. The cache found on-board the processor is termed as the Level 1 cache or simply the L1 Cache. The cache in between the primary memory and the CPU is called the Level 2 or the L2 Cache. More levels of caches maybe found depending on the application and cost requirement of the Embedded System. As can be seem that SRAM or on –chip memory is an important component of ASIC design, we will be considering the various design fundamentals involved with its design. Cache is used as the fast memory and due to high speed requirements SRAM is used as cache memory. Caches can be found at different levels in the memory hierarchy.

1.5 Basic Block diagram of RAM

Address Bus

The Address Bus[4] is a set of signals lines of wires that carries the address of the memory location of interest. For both reading and writing the same address is specified. The address bus is split into higher and lower order bits which correspond to the column and row (line) number of the memory location. More the number of address lines, more memory locations can be addressed. In order to address 2 memory locations, each of 1 byte length, you will need just 1 line (Address 0 & 1, corresponding to the signal on the line being low & high). Thus mathematically speaking, given n number of address lines, a maximum of 2n unique memory locations can be addressed. For a 32-bit address bus, a maximum of 232 bytes or 4096 Megabytes or 4 Gigabytes of unique memory locations can be addressed.

Data Bus

Data Bus[4] is set of signals carry the data to and from the memory. Most modern memory interfaces use the same signal lines for both reading and writing data, with an additional 1 bit signal (Read / Write) specifying the action to be taken. Some memory interfaces use separate lines for reading and writing data. Such interfaces allow data to read and written simultaneously. The data bus width determines the number of data bits that can be read or written at one time. Thus, a 16-bit bus will need to transmit data 4 times in order to read/write 64 bits, whereas a 32-bit bus will need just 2 transfers.

Chip Selects

A typical memory contains than an array or multiple banks of memory devices, each occupying its own unique space in the memory map. In order to select a specific memory bank, a special signal called a Chip Select[4] is used. Thus, Chip Selects act as additional address pins.

Control Signals

Depending on the type and functionality of the memory device, it may have additional control signals. A RAM memory device features a Read/Write signal line which indicates the intended action to be taken on the addressed memory location.

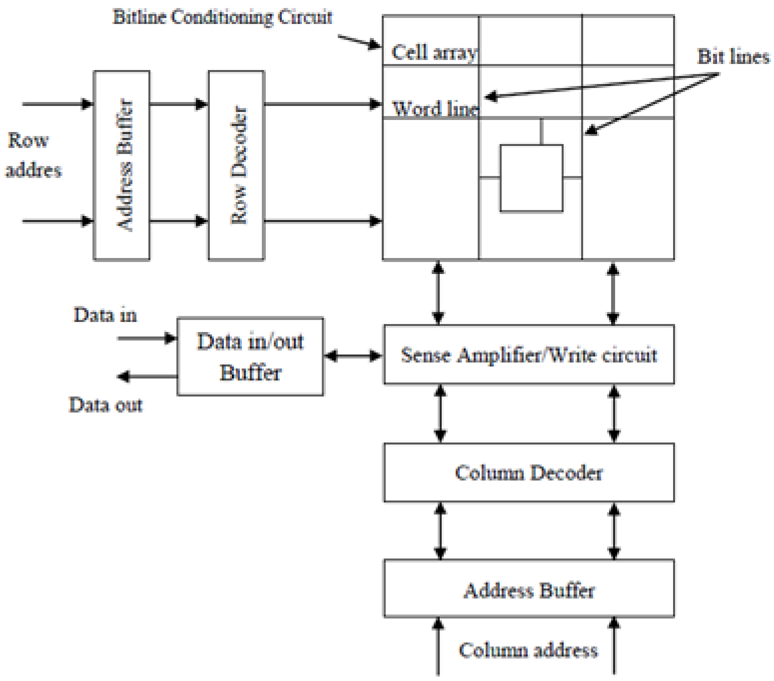

Figure 1.3: Block diagram of complete SRAM structure [5]

If the signal indicates a Read, the data is read from the memory location and fed onto the data bus. Whereas, if a Write is initiated, the data at the memory location is updated with the value from the data bus. Since, a ROM memory allows only read operations; it would not feature a separate Read/Write signal line. It is implicit that all accesses are made for reading data.

1.6 Design Considerations for SRAM

SRAM cell design considerations are important for a number of reasons.

- The designing of an SRAM cell is directly proportional to stability and robustness RAM operation.
- Due to major efforts in increasing the on-chip storage capacity, memory designers are motivated to increase the packing density. So, an SRAM cell must be as small as possible while meeting the stability, speed, power and yield constraints
- The layout of cell mainly determines the critical area of SRAM, which limits chip yield. Meeting the design corners requires much understanding of the involved trade-offs. Especially in scaled technology the cell stability is very important.

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- First and foremost it has to be reliable and stable. This is of course true for all memories, but is especially important for cache due to the more extreme performance requirements and area limitations. If embedded in a microprocessor, there is little space for redundancy (extra memory blocks used if certain memory units have defects), and because of the size and complexity of the chips the costs are very high for each chip. Faulty memories cannot be afforded and a high yield (percentage of working chips on a wafer) is therefore extremely important. Secondly the memory has to have high performance. The sole purpose of cache is to speed up the operation of the CPU by bridging over the performance gap between main memory and the CPU
.
- Another important requirement is low power consumption. Today's advanced microprocessors use a lot of power and get very hot as a result. With increasing memory sizes these contribute with more and more power loss. This is especially important in mobile applications where prolonging battery life strongly depend on minimizing power loss. Low power architectures are therefore chosen for cache memories and low leakage is taken into account when the sizing is done.

All of these reasons together with effort towards simple operation in already complex circuits have made the 6T SRAM the choice of the day for advanced microprocessor caches.

1.7 Objective of the Thesis

The objective of this thesis to study various aspects of SRAM cell design. To study and analyze the shortcomings in the currently used SRAM cells and the other different proposed SRAM cells. The thesis aims to find possible solutions to the above shortcomings. Various aspects of cells have been studied and measured and a new improved novel SRAM cell has been proposed.

1.8 Outline of the Thesis

In **chapter 2**, some basic concepts of memory are discussed. Also, 6T SRAM cell has been described in detail. Along with this literature survey containing various SRAM cells has been summarised.

In **chapter 3**, a novel new 7T SRAM cell has been proposed. Complete description of the cell, along with the read-write operations has been given.

Chapter 4 contains all the results and comparison that have been simulated to achieve the new SRAM cell.

Chapter 5 concludes the thesis and future scope of this thesis has been given.

In previous chapter it has been shown that there are various considerations while designing SRAM cells. Currently lot of research is going on to find newer designs for SRAM cells so as to give better performance. Previously, performance and area were the two main factors involved in memory cell design, but recently power has become an increasingly more important design consideration. Ideally, an SRAM cell is fast and dissipates low leakage power. But this is in contrast with a fundamental technology trade off between transistor speed and leakage: the lower the threshold voltage of a transistor, the faster it becomes and the more leakage power it dissipates. Conventional high-performance SRAM cells use a symmetric configuration of six transistors of identical threshold voltage to achieve fast access latency. As the supply voltage is scaled down, the transistor threshold voltage is also scaled to maintain performance. As a result, leakage power increases rapidly due to the exponential relationship between leakage and Vt. Asymmetrical SRAM cells, on the other hand, reduce leakage while maintaining performance comparable to traditional cells.

2.1 Existing SRAM Technologies

2.1.1 4T2R SRAM

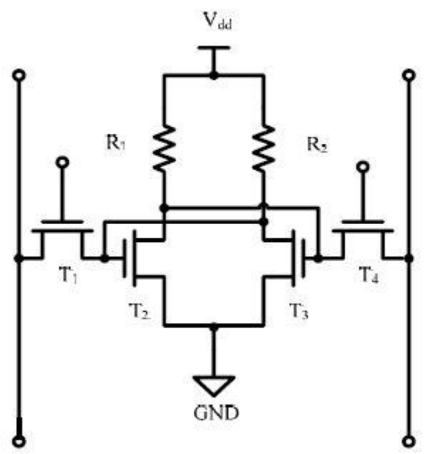

Figure 2.1: 4T2R SRAM cell [2]

This SRAM cell consists of two cross coupled inverters and two access transistors. The access transistors are connected to the bit lines. During write, the value to be stored is sent via the bit lines and when the WL goes high, the value through bit lines is stored in the cell at nodes X and Y as shown. Similarly, during read when WL goes high, the value stored at X and Y is passed onto the bit lines

2.1.2 6T SRAM

The conventional 6T SRAM bitcell consists of two cross-coupled inverters and two access transistors as shown in Figure 2.2. Four transistors (N1, P1,N2 and P2) comprise cross-coupled CMOS inverters which form a latch and store either a '1' or a '0'. Two NMOS transistors (N3 and N4) function as the access transistors that isolate the cell from the bitlines during the hold state and provide access to the cell during the read and write operations. A careful trade-off between cell area, robustness and speed has to be made during the design of SRAM cells.

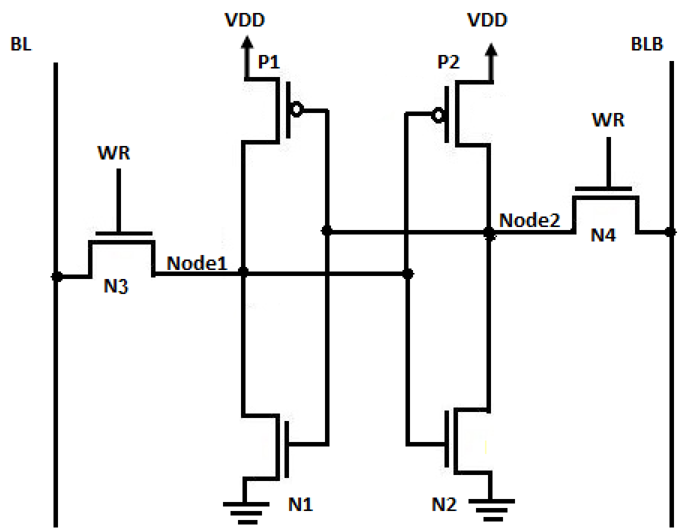

Figure 2.2: 6T SRAM Cell [2]

Read Operation

Prior to the start of the read operation, both the bitlines BL and BLB are precharged to Vdd. After the bitlines are precharged, the read operation is initiated by asserting the wordline to Vdd; thereby connecting the two bitlines to the internal nodes of the cell. Based on the voltage stored at the two nodes of the bitcell, the bitline adjacent to the node containing '0' is discharged and the other bitline is held at '1'. The sense amplifier reads out the correct value stored in the bitcell.

Write Operation

Prior to the start of the write operation, one of the bitlines is precharged to VDD and the other bitline is driven to ground. The bitline adjacent to the node containing ‘0’ is precharged to ‘1’ and the bitline adjacent to the node containing ‘1’ is precharged to ‘0’. After the bitlines are precharged, the write operation is initiated by activating the wordline; thereby connecting the two bitlines to the internal nodes of the cell. When the voltage at node ‘q’ falls below the switching-threshold of the inverter pair (N2-P2), the state of the inverter N2-P2 toggles; in this case from ‘0’ to ‘1’ and the new values are written to the cell. The ease with which the node voltage at ‘q’ decreases to a value lesser than the switching threshold of the adjacent inverter (N2-P2), translates to the writability of the cell. The conditions for a successful write operation can be derived using the current equations at the node q The write ability depends on the pull-up ratio (PR) of the SRAM cell (Equation 2.1). The Pull-Up Ratio is defined as the size ratio between the PMOS pull-up transistors (P1, P2) and the NMOS access transistors (N3, N4).

For the present nanometre regime, the typical value of the pull-up ratio has to be lesser than or equal to ~1 in order to guarantee a successful write operation [2] [6].

This is the basic commercially used SRAM cell. Apart from this, a lot of research is currently going on for improving upon this cell.
That has been covered in the next section.

2.1.3 Issues with existing technologies-

1. There are strict constraints on the sizing of transistors to be able to maintain the data stability and functionality of a standard 6T SRAM cell.
2. In both the above technologies, there is a lot of wastage in power since the probability of discharging of any one of the bit lines is 1. So in any write case, the power from one of the bit lines will be discharged and thereby causing more power dissipation.

   As according to the formula of dynamic or switching power dissipation –

$$P = \alpha_{BL} C_{BL} V^2 F_{write}$$

For which $\alpha_{BL = 1.}$

3. Since we’re scaling down the technology so, to reduce power compensation for above cells, we are making them work in the sub-threshold region. But there are some issues faced by 6T SRAM in sub-threshold region. It has been shown that write ability of the cell fails due to decreased signal levels and increased variations.
4. It has also been shown that read SNM also comes down heavily because of the interference from the bit lines and hence more prone to flipping the state of the cell.

2.2 Performance metrics of SRAM

- Static Noise Margin (SNM) – SNM is the measure of stability of the SRAM cell to hold its data against noise. SNM of SRAM is defined as minimum amount of noise voltage present on the storing nodes of SRAM required to flip the state of cell [6]. SNM can be computed as the length of the side of a maximum square nested between the two voltage transfer characteristic (VTC) curves (i.e., for each back to back inverters) of SRAM cell [7].

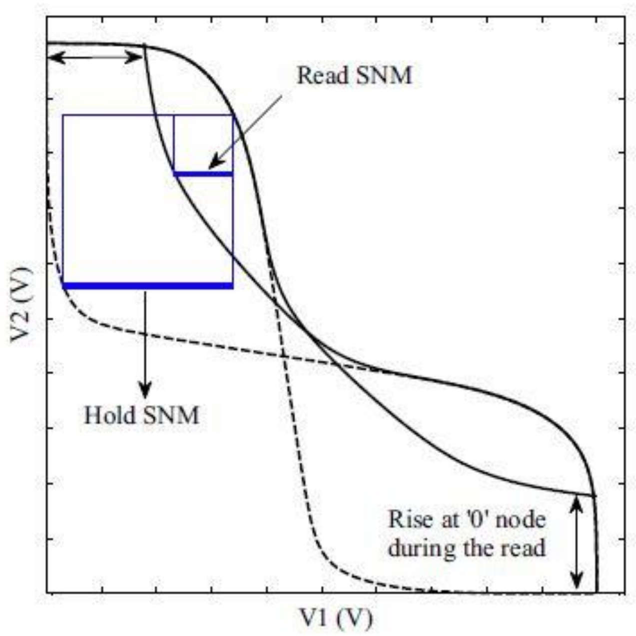

Figure 2.3: SNM of SRAM [7]

SNM can be categorized into two types: Hold SNM and Read SNM. Hold SNM is the SNM of the cell when wordline is LOW or disabled, meaning that the cell is in standby mode. However, the read SNM is more critical than the hold SNM because the SRAM

- Write Margin – Write margin[8] the measure of the ability to write data into the SRAM cell. In a write operation, two operations take place. Firstly discharging of node storing '1' and pull up transistor PMOS and access transistor NMOS are responsible for the discharging of the node '1'. Secondly charging of node '0' through pull up transistor PMOS. Write margin voltage is the maximum noise voltage present of bit lines during successful write operation. When noise voltage exceeds the write margin voltage, and then write failure occurs.

- Access Time – Access time[7] is defined as the time required for accessing the data from the RAM cell. It is determined by time period of Word line 'WL' pulse. This is an important metric because it determines the speed of memory circuits. We want to reduce the access time of RAM cell to make it faster to work with high speed computing systems. The variations due to aging effect, process variations etc. change the behaviour of RAM cell which results access time failure.

- Leakage – Leakage[9] is defined the power consumption of RAM cell in standby mode. To reduce the leakage power, the supply voltage of cell is reduced. The voltage of node storing logical 1 also comes down with lowering of supply voltage. For example, in SRAM, due to leakage, if the voltage of node storing logical 1 goes below the trip of right inverter, then data flips in the standby mode.

2.3 Power consumption in SRAMs

Identification of different components that contribute to the power consumption of an SRAM unit is critical to minimize the overall power consumption. The power consumption of the SRAM unit can be divided into two major terms; static and dynamic.

$$P_{Total} = P_{Static} + P_{Dynamic}$$

Static power consumption[10] is the amount of power that is consumed by the unit to retain the data. Unlike many passive memory devices, an SRAM cell needs to be powered to keep the data. Although the amount of power that a cell consumes to retain the data is relatively small, when a plurality of cells are implemented, the total static power consumption can become significant. The static power is also referred to as leakage power in digital circuit design since the static power consumption is due to the leakage current passing through the circuit when there is no activity:

$$P_{Static} = P_{Leakage} = I_{Leakage} \times V_{dd}$$

Dynamic power consumption[10] of the SRAM unit is especially important when the speed of operation is high. The long interconnects with high capacitive loading require a significant amount of charge for their voltage variation. Owing to the interconnects regular pattern and predictable switching activity factor, α, the power consumption associated with the interconnects that undergo a full swing voltage variation can be accurately calculated using the famous dynamic power consumption equation [4]:

$$P_{Dynamic} = \alpha f C_{Interconnect} V_{dd}^2$$

where f is the frequency of operation, Cinterconnect is the interconnect capacitance and Vdd is the supply voltage.

2.3.1 Static power consumption

The static power consumption in an SRAM unit is mainly due to the leakage current in SRAM cells. According to [11],among different leakage current mechanisms, the subthreshold leakage of the transistors are the prominent source of the leakage current in an SRAM cell. The next important leakage current in the SRAM cells for currently available technologies is the gate induces drain leakage (GIDL) which is usually more than one order of magnitude smaller than the subthreshold leakage in the 180nm CMOS technology.

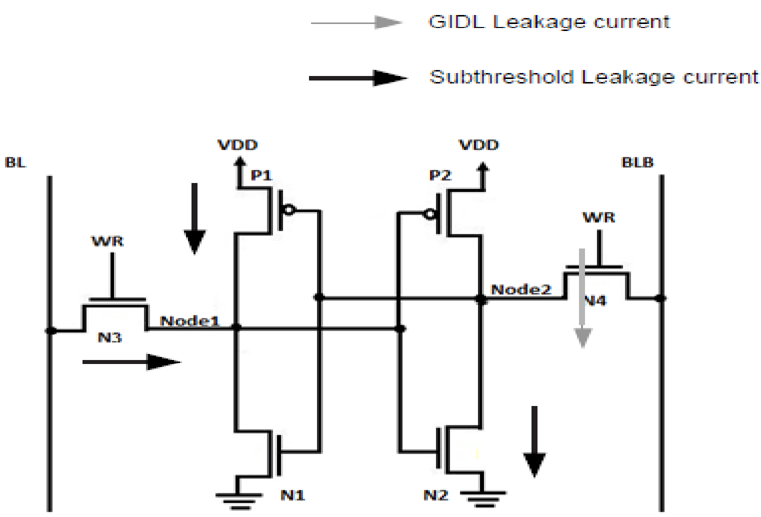

Figure 2.4: Leakage currents in a non-accessed cell [16]

2.4 Literature Survey

2.4.1 5T SRAM Cell

Ingvar Carlson in [12], proposed an 8T SRAM bitcell design shown in Figure 2.5. In a normal 6T cell both storage nodes are accessed through NMOS pass. This is necessary for the writing of the cell since none of the internal cell nodes can be pulled up from a stored ’0’ by a high on the bit line. If this was not the case an accidental write could occur when reading a stored ’0’. However, if the bit lines are not precharged to VCC this is no longer true. With an intermediate precharge voltage, VPC, the cell could be constructed so that a high on the bitline would write a ’1’ into the cell, but a precharged bitline with a lower voltage would not. Also a low on the bitline could write a ’0’ into the cell, whereas the intermediate precharge voltage would not, thus giving the cell a precharge voltage window where correct operation is assured. This would eliminate the need for two NMOS transistors, since the cell now can be written both high and low from one side. In turn, that would also result in one less bitline. From a high density point of view this is very attractive. Figure 2.4 shows the structure of the proposed, resulting five-transistor (5T) SRAM cell. With one less bitline the 5T cell also shares a sense amplifier between two cells . This further reduces the area giving the 5T memory block an even greater advantage over the 6T SRAM.

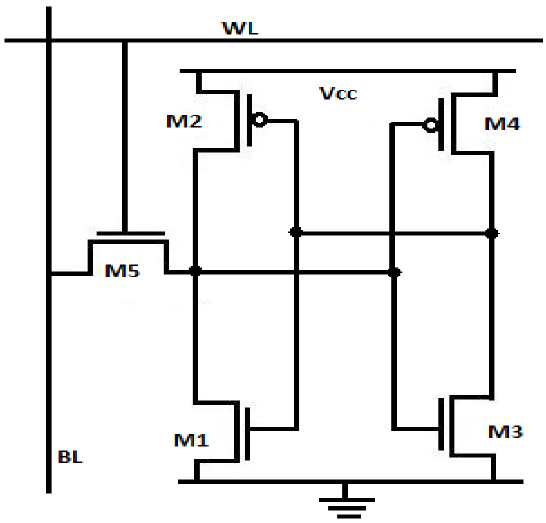

Figure 2.5: 5T SRAM Cell [12]

Read Operation

The operation scheme when reading a 5T cell is very similar to the 6T SRAM. Before the onset of a read operation, the wordline is held low (grounded) and the bitline is precharged.

However, the bitline is not precharged to VCC, but to another value, VPC. This value is carefully chosen according to stability and performance. Figure 2.6 shows the simplified schematic corresponding to the onset of a read ’0’ operation. Note that the bitline now has been precharged to VPC.

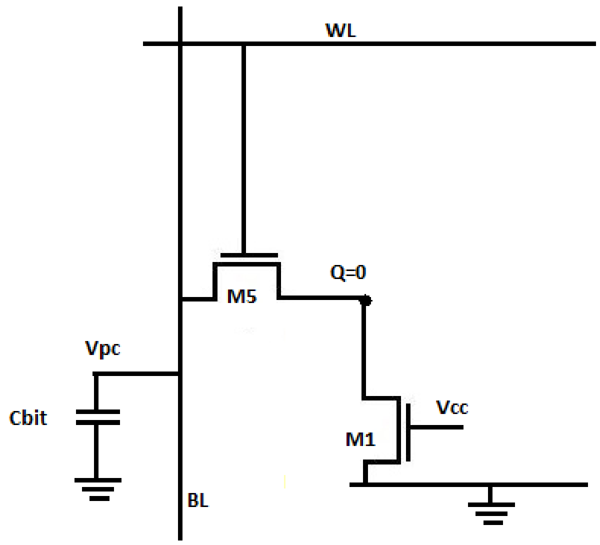

Figure 2.6: 5T SRAM Read [12]

One drawback of the intermediate precharge value is the apparent problem of obtaining this voltage. One obvious way is to supply this voltage externally. During precharge, one bitline is grounded and the other bitline, connected to the same sense amplifier, is charged to a value VCC-VTN obtained from a diode-coupled NMOS. These bitlines are then equalized during the address decoding through a NMOS transistor and the correct precharge voltage is obtained. The next phase of the read operation scheme is to pull the wordline high and at the same time release the bitline. This turns on the access transistor M5 and connects the storage node to the bitline. If reading a ’0’, BL will now be pulled down through the transistor combination M5-M1. If instead a ’1’ is to be read, the situation is slightly different from the 6T case. Another apparent difference between the 5T SRAM and the 6T SRAM is how the sensing of the stored value is done. While the 6T cell has two bitlines and the stored value is sensed differentially the 5T cell only has one bitline. Depending on the value stored, the 5T bitline is either raised or lowered.

Write Operation

Writing in the 5T SRAM cell differs from the 6T cell mainly by the fact that it is done from only one bitline. For the 5T cell the value to be written is held on the bitline, and the wordline is asserted. Since the 6T cell was sized so that a ’1’ could not be written by a high voltage on the bitline , the 5T cell has to be sized differently.

2.4.2 7T SRAM Cell

Ramy E. Aly in [13], has proposed a 7T SRAm cell to improve upon the power savings of 6T cell. 7T SRAM cell depends on cutting off the feedback connection between the two inverters, inv1 and inv2, before a write operation. The feedback connection and disconnection is performed through an extra NMOS transistor and the cell only depends on BL _bar to perform a write operation as shown.

Write Operation

The write operation starts by turning N5 off to cut off the feedback connection. BL_bar carries complement of the input data, N3 is turned on, while N4 is kept off as shown in figure 2.7. N3 transistor transfers the data from BL_bar to Q2 which drives inv2, P2 and N2, to develop Q, the cell data. Similarly, drives inv1, and , to develop Qbar which equals if data is “0” and slightly higher than if data is “1.”

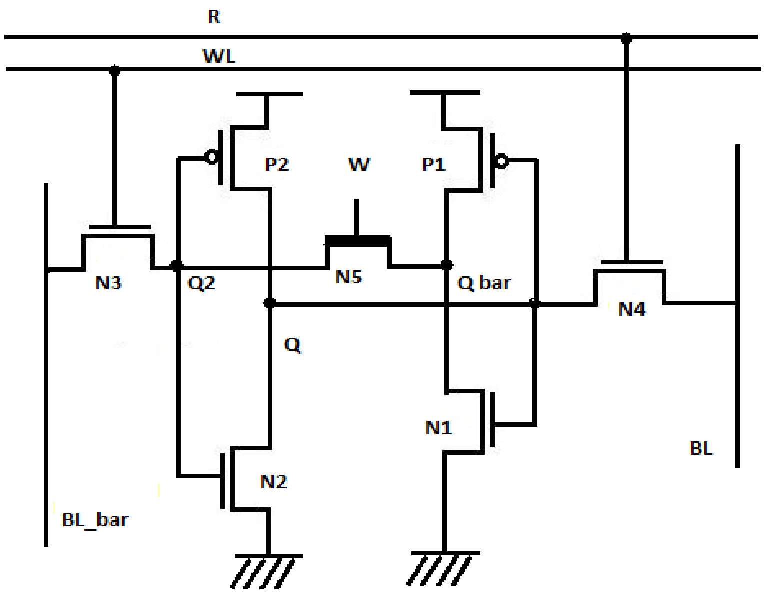

Figure 2.7: 7T SRAM Cell [13]

Then, is turned off and is turned on to reconnect the feedback link between the two inverters to stably store the new data. Both BL and BL_bar are precharged "high." Using the proposed write scheme, BL_bar is kept "high" to write "0" with negligible power consumption and careful transistor sizing is essential to guarantee a stable write "0" operation as explained below. To store "1" in the cell, _ is discharged to "0" with comparable power consumption to the conventional 6T cell. To store a "0" in the cell, there is no need to discharge BL_bar and BL therefore, the activity factor of discharging BL_bar is less than 1 and depends on the percentage of writing "1."

Read Operation

Both and signals are turned on, while is kept on. When , the read path consists of N2 and N4, and behaves like a conventional 6T cell. In this critical side, the three transistors are connected in series which reduces the driving capability of the cell unless these transistors are carefully sized.

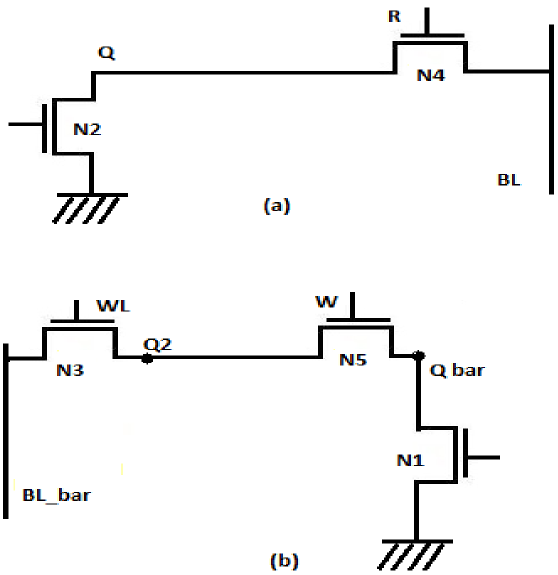

Figure 2.8: 7T SRAM Read [13]

2.4.3 8T SRAM Cell

In 6T SRAM, The fundamental stability problem occurs during the read operation. L. Chang in [14], proposed an 8T SRAM bitcell design shown in Figure 2.9 to solve this issue. In order to reduce leakage power consumption by reducing worst case VDS of M5 and M6 pass transistor, pre-charge voltage for bit-lines is kept much lower than the cell supply voltage When the pass transfer transistors (M5 & M6,Fig 2.9) are turned on, which pull the '0' logic node to a poor ’0’ level and ‘1’logic node to a poor ‘1’ logic level, it may lead to flip the cell data. In this 8T SRAM cell, three extra transistors are used to separate the read and write current path and avoid accidental cell flipping during read operation.

Write Operation: In the proposed cell, single bitline is used for write operation which reduces write power consumption compared to 6T SRAM write operation. During write ‘1’ operation, M5 turns-on by enabling the ‘write word line signal’. As the ‘Bit Line’ is charged to logic ‘1’, the ‘Q’ node starts charging and turns on M1 which leads to flip ‘Qbar’ node to logic ‘0’ . Now ‘Qbar’ node helps enabling the M4 which facilitates writing good logic ‘1’ at ‘Q’ node. On the other hand, during write ‘0’ operation, the ‘Bit Line’ is charged to logic ‘0’ and M5 turns-on by enabling ‘write word line’ signal. The ‘Q’ node starts dis-charging and turns on M2 which in turn flipped ‘Qbar’ node to logic ‘1’. Now ‘Qbar’ node helps turning M3 on, which facilitates discharging ‘Q’ node properly and consequently logic ‘0’ is obtained at ‘Q’ node.

Read Operation: Read operation is performed by using MOSFETs M6, M7 and M8. Node ‘Qbar’ is connected to the gates of M7 and M8. In this case, a current flows in and out of the read circuit by turning on transistor M6 using Read Word Line. The cell data is read by sensing the Bit-Line voltage fluctuation using differential current mode sense amplifier.

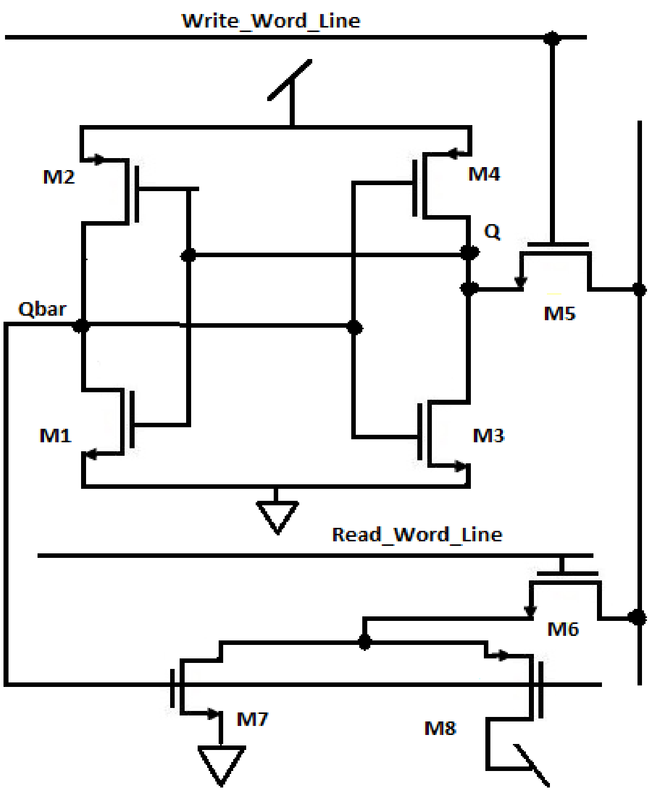

Figure 2.9: 8T SRAM Cell [14]

During read ‘1’ operation, M5 and M6 are turned off and on respectively. As ‘Qbar’ node stores ‘0’ logic, it enables the M8 (PMOS) transistor which in turn charges the Bit Line through M8 and M6. The sense amplifier detects the bit swing and output ‘1’ is obtained. During read ‘0’ operation, Read Word Line signal enables the M6 and as ‘Qbar’ node stores logic ‘1’, so it turns on M7 (NMOS) which discharges the Bit-Line through M7 and M6. This effect builds a voltage difference between the Bit Line and the local reference line which is sensed by the differential amplifier, and logic ‘0’ is obtained at the output. The 8T SRAM cell uses one bit-line but has to provide one extra word-line (Read Word Line) for read operation, so the cost of the wire connection is almost the same as that of the conventional 6T SRAM cell.

2.4.4 9T SRAM Cell

A 9T SRAM cell with enhanced data stability and reduced leakage power consumption is was proposed by Zhiyu Liu[15]. The upper sub-circuit of the new memory cell is essentially a 6T SRAM cell with minimum sized devices (composed of N1, N2, N3, N4, P1, and P2 with W = Wmin and L = Lmin). The two write access transistors (N3 and N4) are controlled by a write signal (WR). The data is stored within this upper memory sub-circuit. The lower sub-circuit of the new cell is composed of the bit-line access transistors (N5 and N6) and the read access transistor (N7). The operations of N5 and N6 are controlled by the data stored in the cell. N7 is controlled by a separate read signal (RD).

Write Operation

During a write operation, WR signal transitions high while RD is maintained low, N7 is cut off. The two write access transistors N3 and N4 are turned on. In order to write a “0” to Node1, BL and BLB are discharged and charged, respectively. A “0” is forced into the SRAM cell through N3. Alternatively, for writing a “0” to Node2, BL and BLB are charged and discharged, respectively. A “0” is forced onto Node2 through N4.

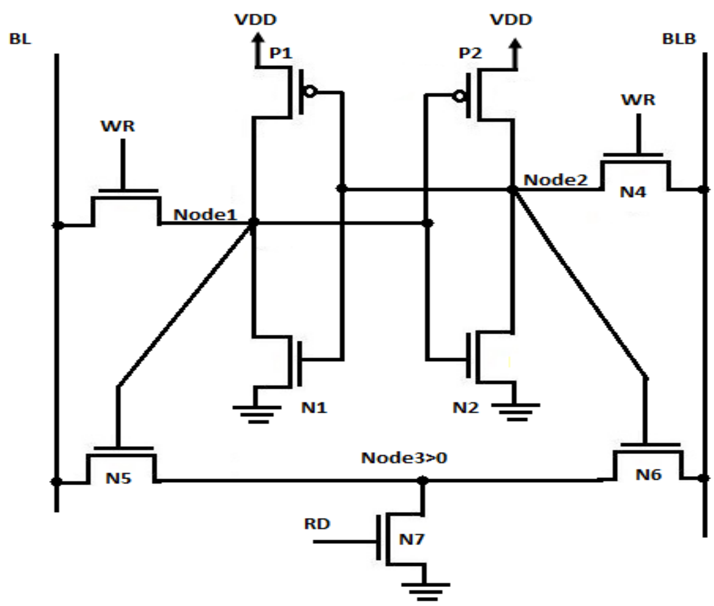

Figure 2.10: 9T SRAM Cell [15]

Read Operation

During a read operation, RD signal transitions high while WR is maintained low. The read access transistor N7 is activated. Provided that Node1 stores "1", BL is discharged through N5 and N7. Alternatively, provided that Node2 stores "1", the complementary bitline (BLB) is discharged through N6 and N7

As shown in chapter 2 many different SRAM cells have been proposed over the years. In this thesis, all these cells have been designed and simulated on 180nm technology in MentorGraphics Design Architect. The key to the microprocessor cache market is high performance, high stability and small area. With the excellent performance and stability of the 6T SRAM, it has been dominating even though the stability and leakage power along with its high area are some of its issues. It has been shown that this cell has advantage both from the stability as well as static power dissipation point of view.

3.1 Cell Structure

In the standard 6T cell, two cross coupled inverters are used to store the data. And in fact in all other SRAM cells described in previous chapter consist of two inverters. The cross coupled scheme provides the natural feedback required for storing the data.

In 6T cell both storage nodes are accessed through NMOS pass-transistors. Also, the read operation occurs through the same two NMOS access transistors which causes reduction in Read Signal to Noise Margin. So, in the new SRAM cell proposed, it has been taken care of as described below.

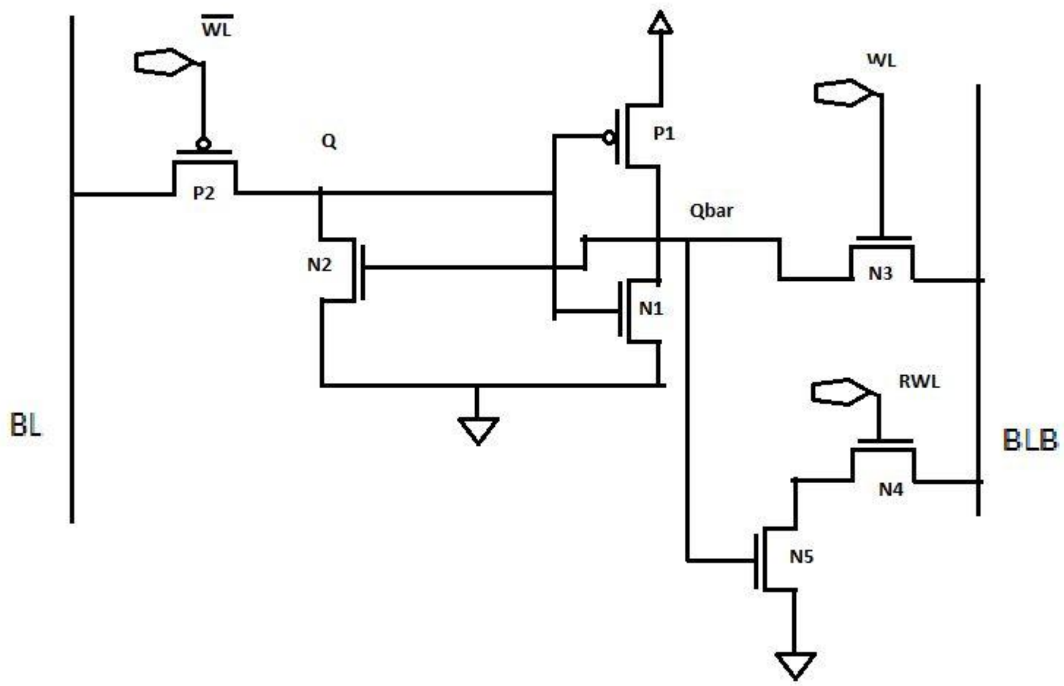

Figure 3.1: Proposed 7T SRAM Cell in 180 nm CMOS technology

In the new cell, there is only one inverter which is sufficient to store the data. The other bit can be stored on the node of another transistor and blocked there. From a high density and low leakage point of view this is very attractive. Figure 4.1 shows the structure of the proposed, resulting Seven-transistor (7T) SRAM cell. As can be seen in the figure, transistors N1 and P1 form a CMOS inverter. P2 and N3 are the access transistors. The transistor N2 is used to hold the value of Q in its place along with the inverter. The write bitline WL and inverse of it i.e. $\overline{W}$ and the pass transistors P2 and N3 are used for transferring new data into the cell. Alternatively, the read wordline RWL and transistors N4 and N5 are used for reading data from the cell. Two separate control signals, read wordline RWL and write wordline WL, are used for controlling the read and write operations, as shown in Figure 3.1. The proposed 7T SRAM cell does not have any strict sizing constraints for the read operation which will be discussed in next section. In the next sections the operation of the cell is discussed.

3.2 Read Operation

Prior to a read operation, BLB is precharged to VDD. To start the read operation, RWL transitions to VDD while WL is maintained at VGND and WL_Bar is maintained at VDD. Transistors P2 and N3 remain switched off during the read operation. If a '1' is stored at node Qbar, N5 is turned on and BLB is discharged through the transistor stack formed by N4 and N5, as illustrated in Figure 3.2. . Alternatively, if a '0' is stored at node Qbar, N5 remains turned off and BLB is maintained at VDD, as illustrated in Figure 3.3.

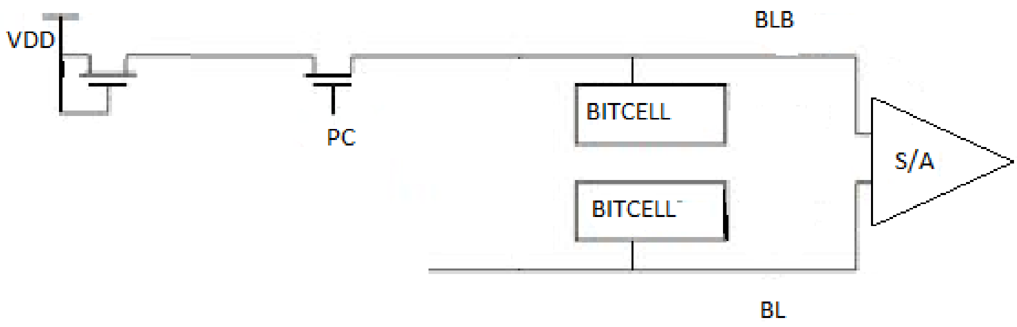

Figure 3.2: Internal bitline precharge scheme

As discussed in the section 2.3.2, the read operation imposes sizing constraints on the transistors of the 6T SRAM bitcell. The cell ratio has to be at least more than the minimum value in order to guarantee a successful read operation in a 6T SRAM cell. However, the 7T

SRAM cell's read discharge path is completely isolated from the two nodes of the SRAM bitcell that store the data. Hence, there are no sizing constraints imposed due to the read operation in the proposed 7T SRAM cell. The sizing of the transistors N4 and N5 depend on the desired read performance and maximum cell area. In order to boost the read performance, the widths of transistors N4 and N5 can be increased. However, since increased device size results in increased SRAM cell area, a careful trade off between the read performance and cell area is required.

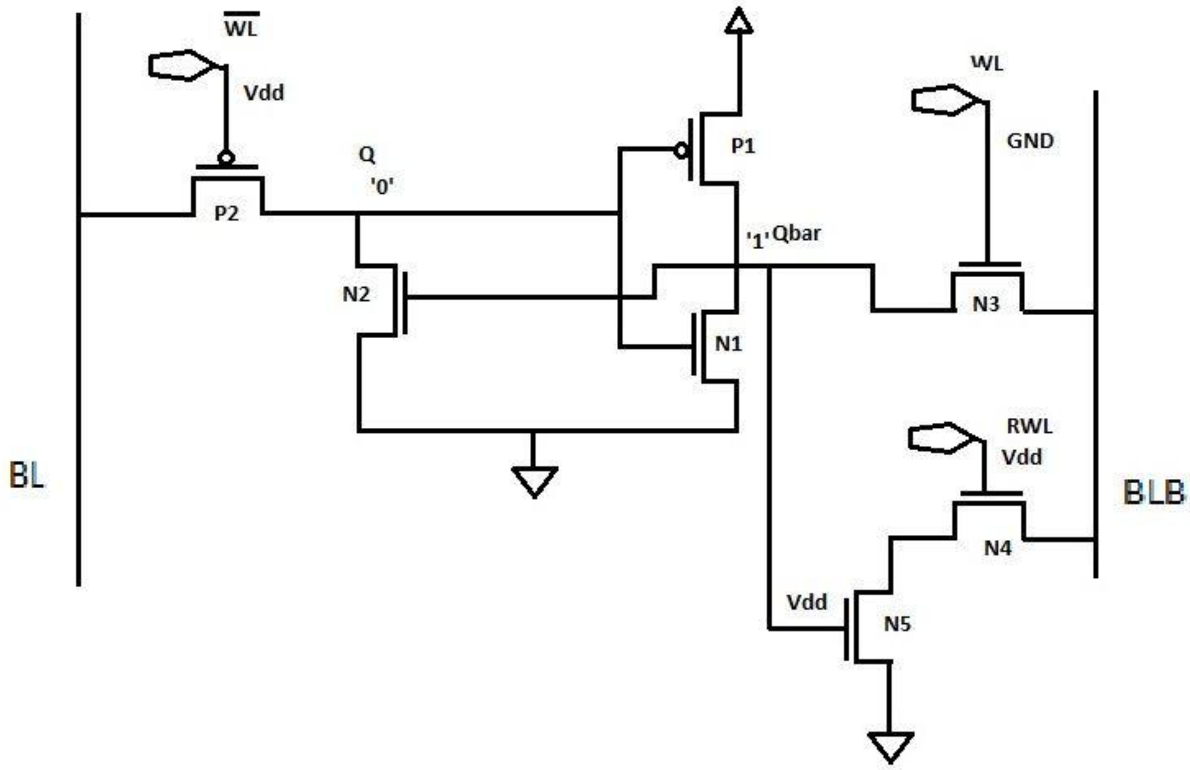

Figure3.3: Proposed 7T SRAM cell during the read operation when Qbar = '1'

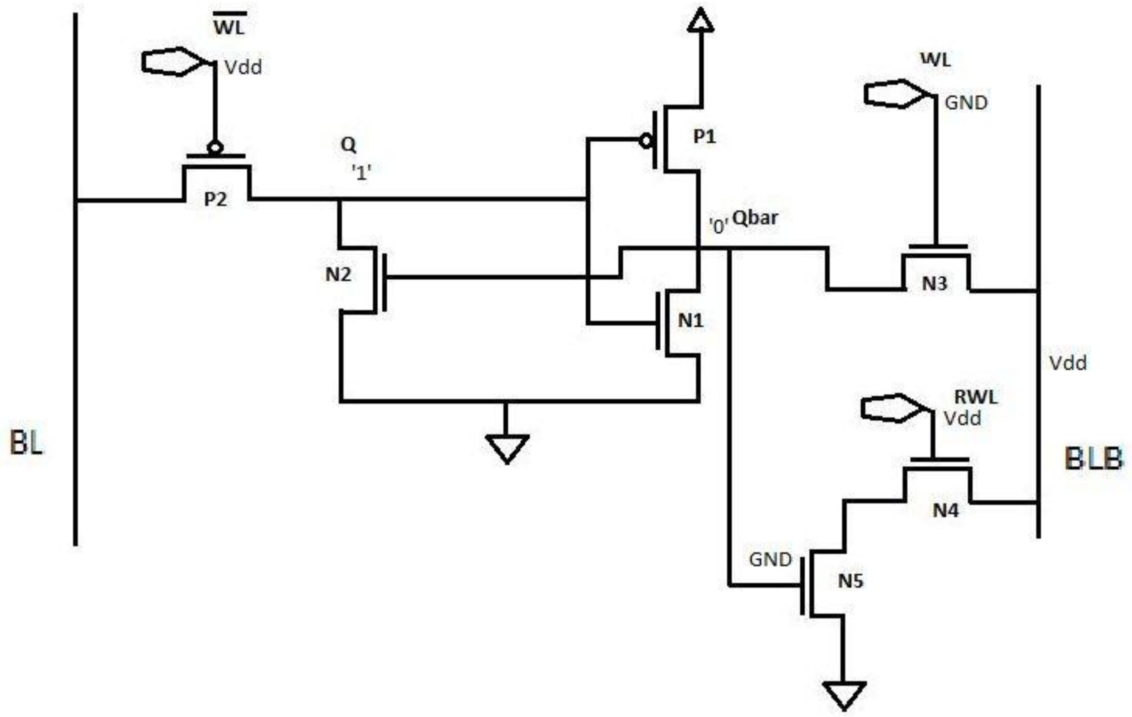

Figure3.4: Proposed 7T SRAM cell during the read operation when Qbar = ‘0’

3.3 Write Operation

Prior to a write operation the BL is charged (discharged) to VDD (VGND) in order to force a ‘1’(‘0’) onto node Q, while BLB is discharged (charged) to VGND (VDD) in order to force a ‘0’(‘1’) onto node Qbar. To start the write operation, the write signal WL transitions to VDD while the signal at the gate of P2 i.e. WL_Bar is maintained at VGND. The data is forced onto node Q through the bitline access transistor P2 and onto Qbar through the Bitline Bar access transistor N3, as shown in Figures 3.4 and 3.5. During the retention period, when the cell is neither accessed for read or write operations, both the word lines, WL and RWL remain at ‘0’ , consequently WL_Bar remains at '1'. The sizing constraints on the proposed design exist only for the write operation. In order to perform a successful write operation, the voltage at the node Q should decrease below the switching threshold of the adjacent inverter. The equations for a successful write operations can be derived as shown in the Equations 3.1 and 3.2.

$$Cell\ Ratio = \frac{W_{P2}}{L_{P2}} \div \frac{W_{N2}}{L_{N2}}$$

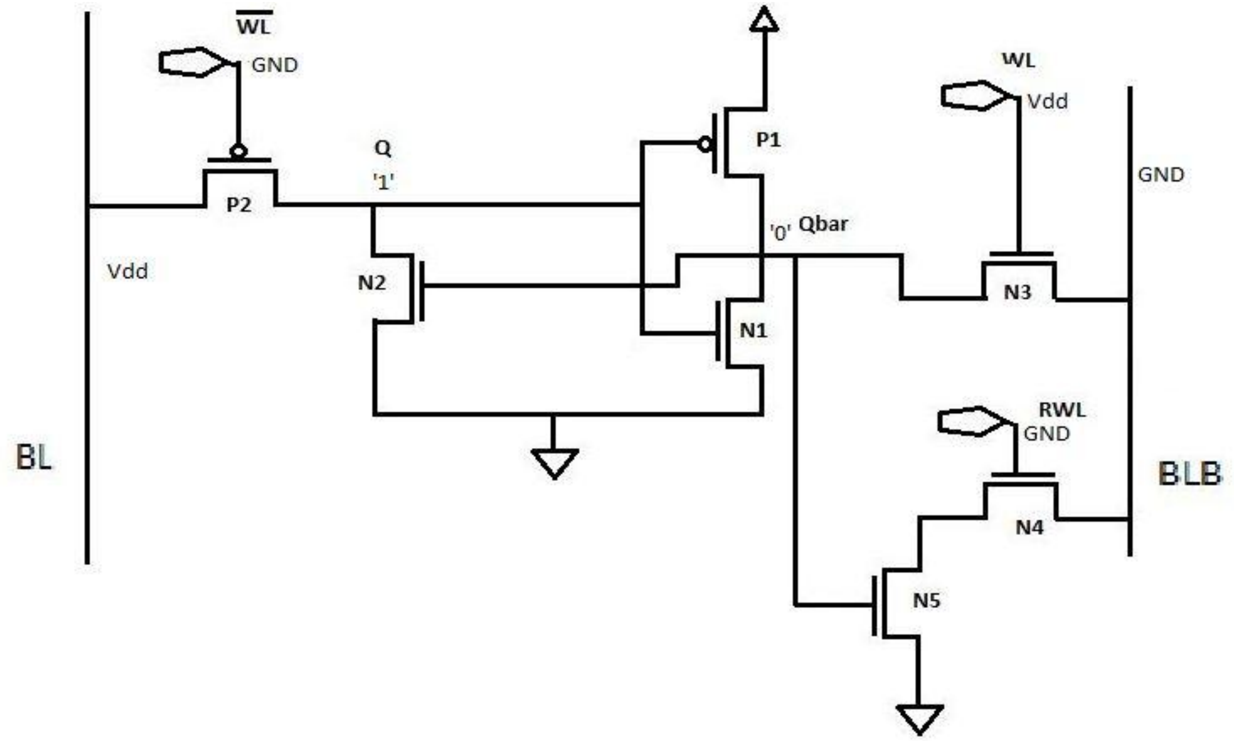

Figure3.5: Proposed 7T SRAM cell during the write ‘1’ operation

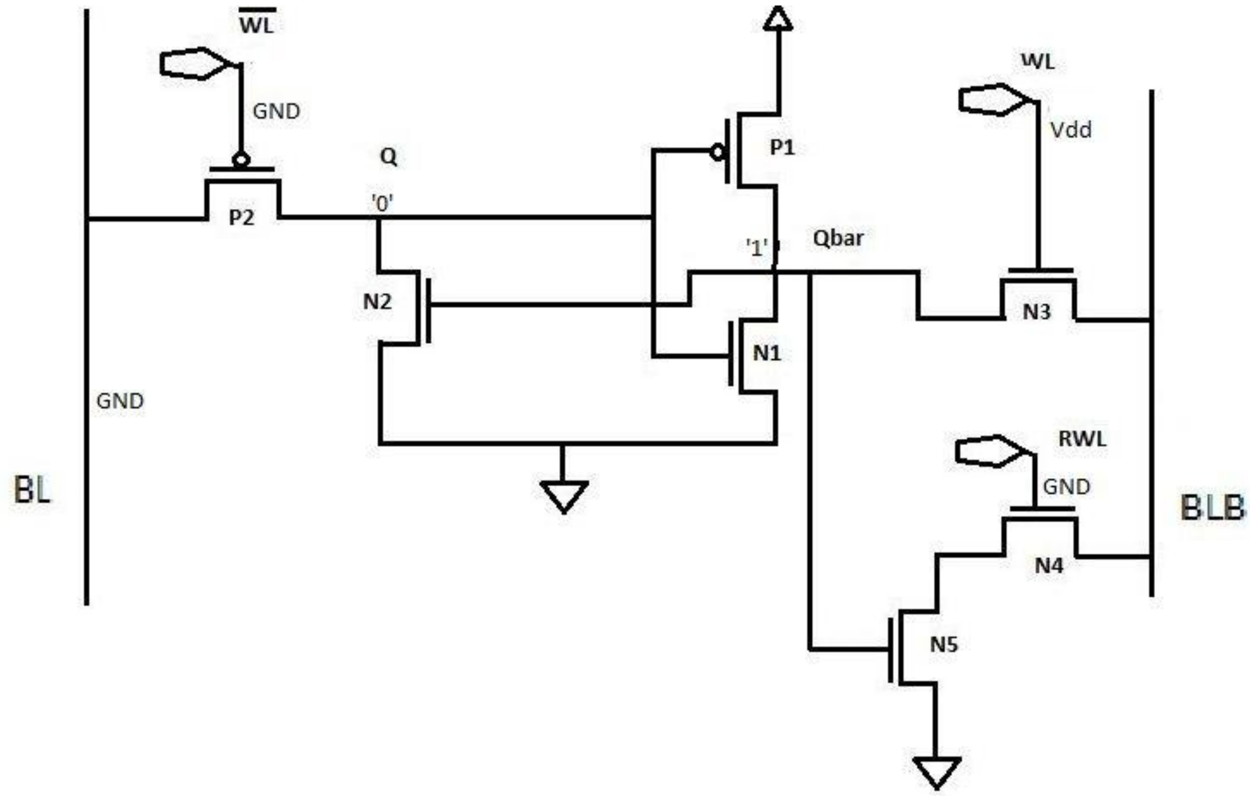

Figure3.6: Proposed 7T SRAM cell during the write ‘0’ operation

3.4 Static Noise Margin

SNM is the measure of stability of the SRAM cell to hold its data against noise. SNM of SRAM is defined as minimum amount of noise voltage present on the storing nodes of SRAM required to flip the state of cell Static Noise margin of MOS transistor was calculated analytically by Seevnick. et al.(1987) [17]. He derived explicit analytic expression of static-noise margin as a function of device parameters and supply voltage. SNM can be computed as the length of the side of a maximum square nested between the two voltage transfer characteristic (VTC) curves (i.e., for each back to back inverters) of SRAM cell as shown

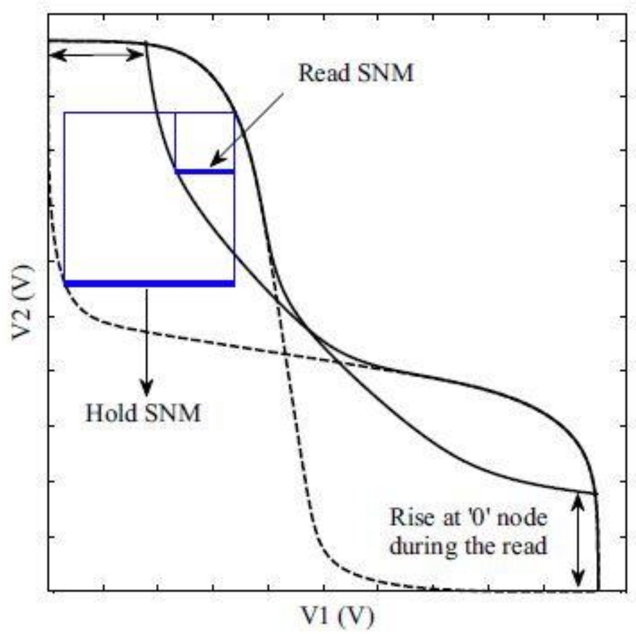

Figure 3.7: Hold SNM of 6T SRAM cell [17]

The static-noise margin of the proposed cell in hold state is almost equivalent to that of other cells including 6T cell, but it is during the read and write that the noise margin is important and should be considered.

3.4.1 Read Noise Margin

The proposed 7T SRAM cell enhances the read stability by employing a read discharge path that is completely isolated from the internal nodes of the cell. Based on the voltage at node ‘Qbar’, the BLB is conditionally discharged through the N4-N5 transistor stack during a read operation. Since the read path is isolated from the write path, the data stability is thereby significantly improved when compared with the conventional 6T SRAM cell design. Also, the inverse node 'Qbar' is connected to gate of N5 and not N4 although it could have been functionally correct. This is due to the caution taken so as to protect it against any sudden changes occurring in the BLB which might be transferred to 'Qbar' through charge injection.

3.4.2 Write Noise Margin

The proposed cell has greater write noise margin as well, because during write, the currents from BL and BLB have to fight against one less transistor i.e. the load transistor of one of the inverter. So, the new cell has more writability to say the least.

3.5 Bitline Leakage

In the standard 6T cell and all the other cells discussed in this thesis, the problem of bitline leakage is significant. The 8T and 9T cells attempt to address the problem of leakage by using the stack effect. But these cells only achieve a partial success in preventing the leakage current from the bitline and through the cell during the idle state that is, when the cell is just holding the data stored in it. In the proposed 7T design, the problem of static power dissipation has been addressed by reducing one transistor in one of the cross coupled inverters as shown below.

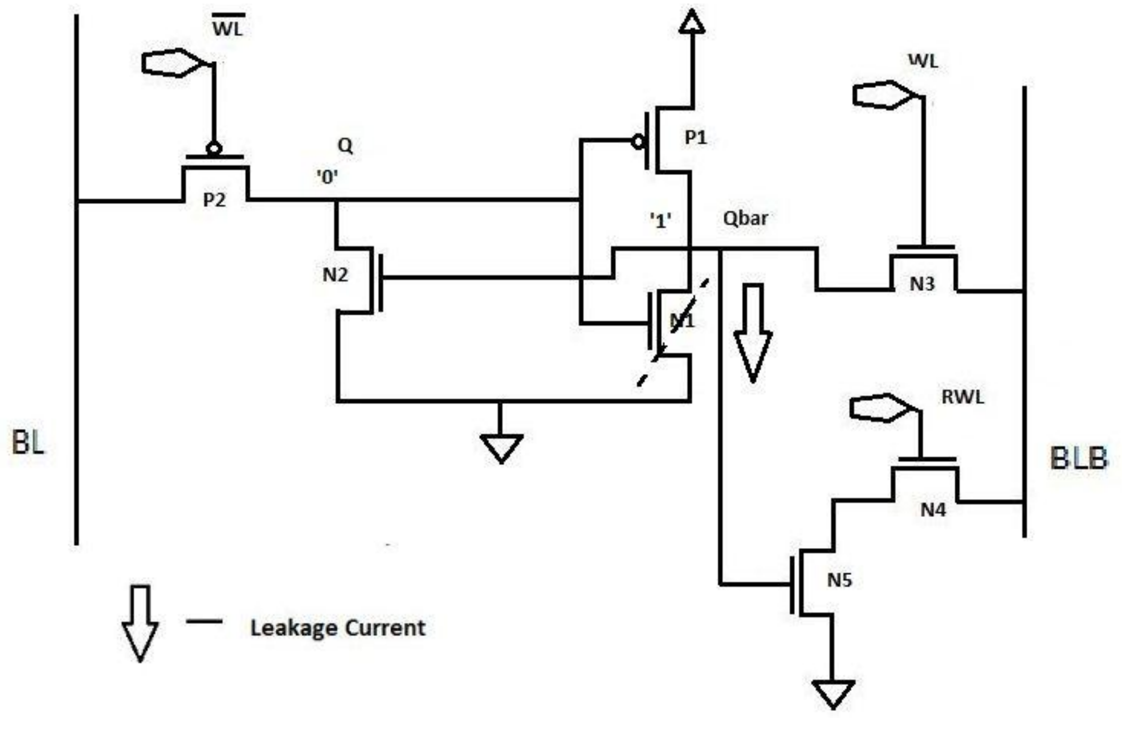

Figure 3.8: Bitline Leakage from N1 only when '0' is stored

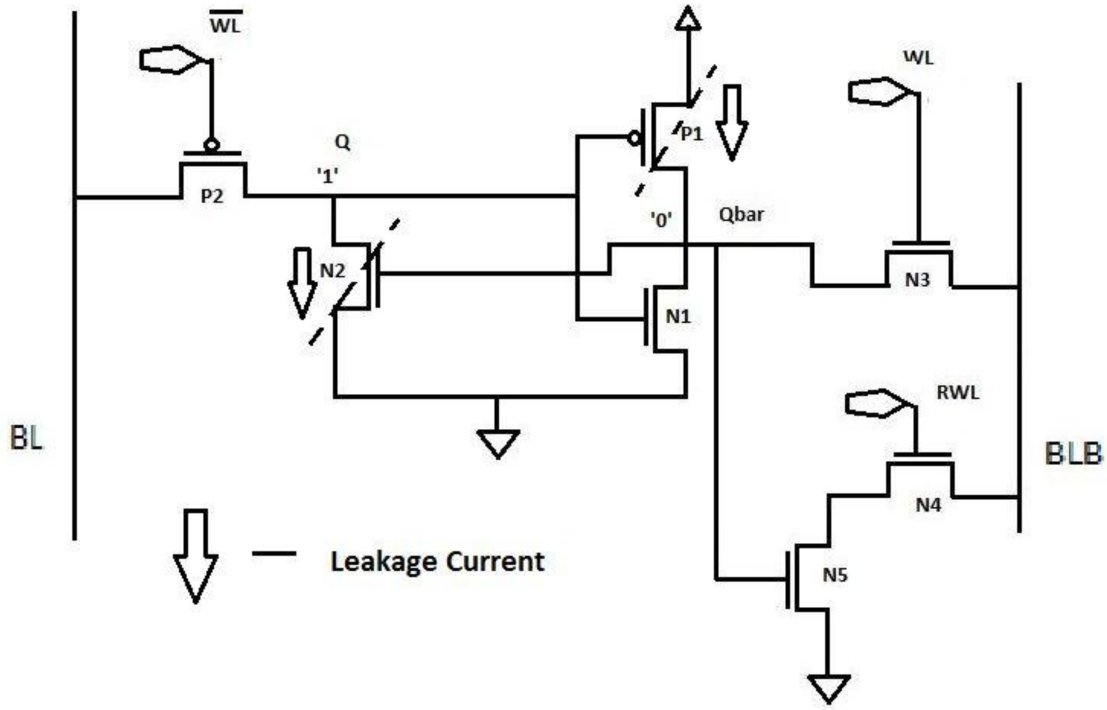

Figure 3.9: Bitline Leakage from P1 and N2 when '1' is stored

So, these are some of the features in the proposed 7T SRAM cell. All the results along with sizing constraints are discussed in the next chapter of the thesis.

4.1 Simulation Setup

This section describes the simulation framework used for this thesis. The 6T SRAM cell is initially evaluated for successful read and write operations. The schematic used for this analysis is shown in Figure 4.1. The precharge circuitry consists of two transistors a1 and a2, both of which are tied to V_{dd}. In this setup the maximum possible voltage on the bitlines is V_{dd}. This type of precharge circuitry is more suitable for differential voltage sensing amplifier since the bitline voltages initially start at V_{dd}. This voltage is needed for a proper biasing and output swing of the differential amplifier [1]. The write circuitry consists of four transistors e1, e2, e3 and e4. The write enable 'wr en' signal drives transistors e1 and e3. Transistors e2 and e4 are operated by the signals 'data' and 'not data'. The 'wr en', 'data' and 'not data' are used simultaneously to precharge or discharge the bitlines during the write operation. The read circuitry consists of a differential voltage sense amplifier as shown in Figure 4.1. The bit value stored in the SRAM cell is obtained on the 'sense out' signal.

At the onset of the read operation, the transistors in the SRAM cell draw current from the highly capacitive column. The slow drop in bitline voltage could cause long read access times. In order to reduce the read access time, the memory is designed so that a minimum voltage change on one or the other bitline is required to detect the stored value. The sense amplifier detects this change in voltage and detects the right bit value stored in the SRAM cell. For the setup shown in Figure 4.1, a differential voltage sense amplifier is used. This sense amplifier attenuates common-mode noise and amplifies the differential-mode signals. This is important because any noise that is common to both the bitlines should not be amplified.

4.2 Stability

1. Read Static Noise Margin

Analytical modeling of SRAM cell stability is not an entirely new concept. First time, E. Seevinck, F.List and J. Lohstroh in 1987 characterized the cell robustness by modeling the SNM of back-to-back inverters of the SRAM cell. The SNM can be found analytically by solving the Kirchhoff equations and applying one of the mathematically equivalent noise margin criteria [19].

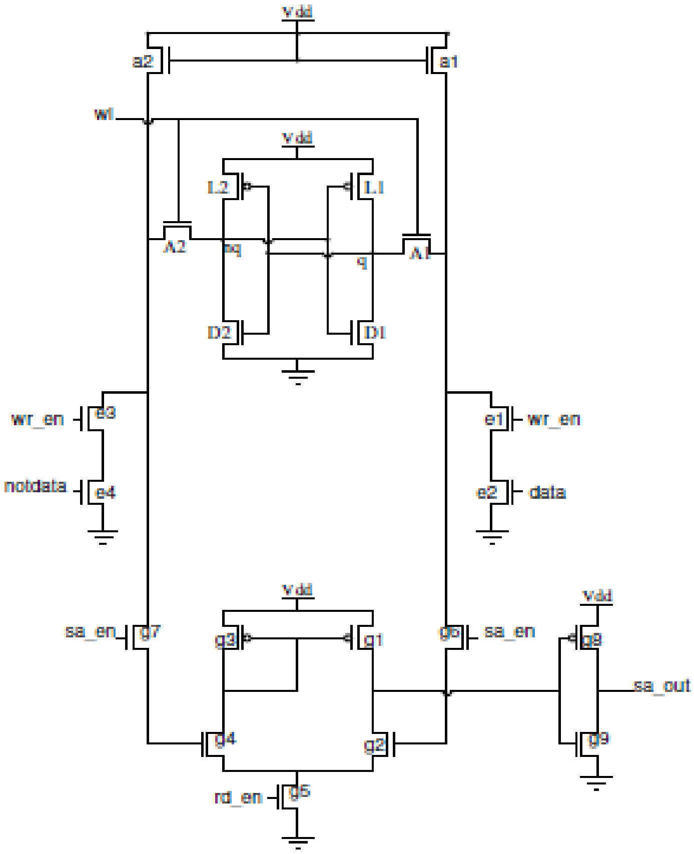

Figure 4.1: Schematic of 6T SRAM cell along with write and sense-amplifier circuitry [18]

Figure 4.2 below demonstrates the schematic diagram for SNM MentorGraphics simulations. To simulate the SNM of this memory cell, two bitlines and the wordline of the cell are kept at V DD . This SNM is also called read SNM and the mentioned set-up for simulation suits to the read operation (see also Figure 2.12). Two equal dc voltage sources, V N are placed between inverters indicating the dc noise sources. These voltages are swept from 0 to $V_{DD}/2$ (i.e. 0.9 V) or more until the cell storage data flips. Cell is more vulnerable during read operation when wordline is active. When SNM of cell goes below the pre-defined target SNM of cell, the read failure may occur. The butterfly curves obtained by plotting the VTCs of the inverters of the 6T SRAM cell present valuable information regarding the stability of the SRAM cell during the read and hold states. It is clear that the eye of the butterfly curve during the read access is less than the case when the SRAM is held in the hold state as discussed earlier.

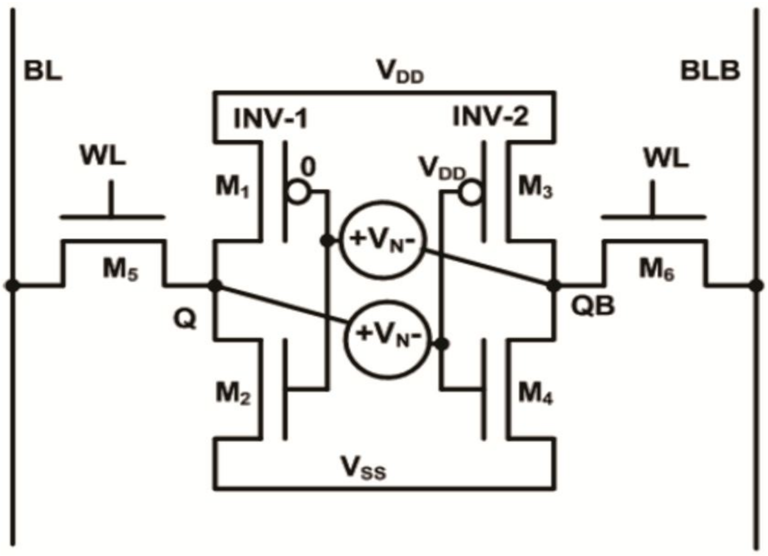

Figure 4.2: Simulation setup for read SNM [21]

Lower SNM means that the cell is vulnerable to noise and the cell contents can be easily destroyed. The SNM is lower during the read access because the VTC is degraded by the increase in voltage at the node containing ‘0’ due to the voltage divider action across the access transistor (A1, A2) and drive transistor (D1, D2). Hence, one of the main considerations of SRAM sizing is to minimize the voltage rise at the node containing ‘0’ at the onset of the read operation. Figure 4.3 illustrates the read SNM of 6T SRAM cell with and without the presence of noise.

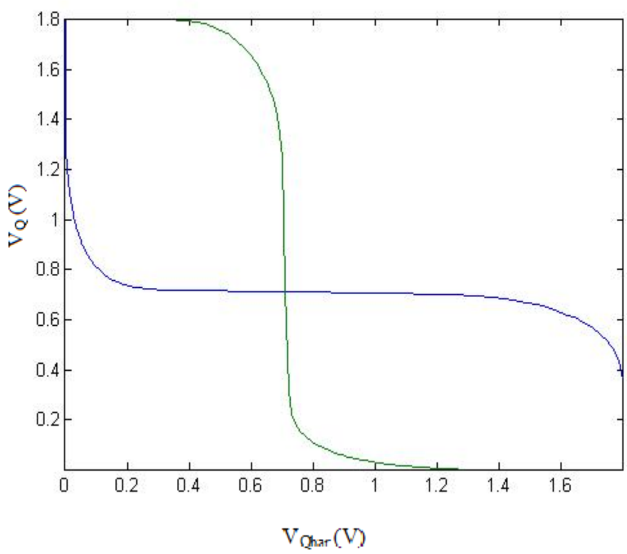

Figure 4.3: Hold SNM of SRAM cell without Noise.

The VTCs of a stable SRAM cell which store a ‘0’ or a ‘1’ are bistable—i.e., the VTCs have three points of intersection among which there are two points which indicate the stability of the cell. It can be observed that when the noise is greater than the SNM of the cell, the curves meet at only one point which indicates the loss of content (‘1’ or ‘0’) stored in the cell.

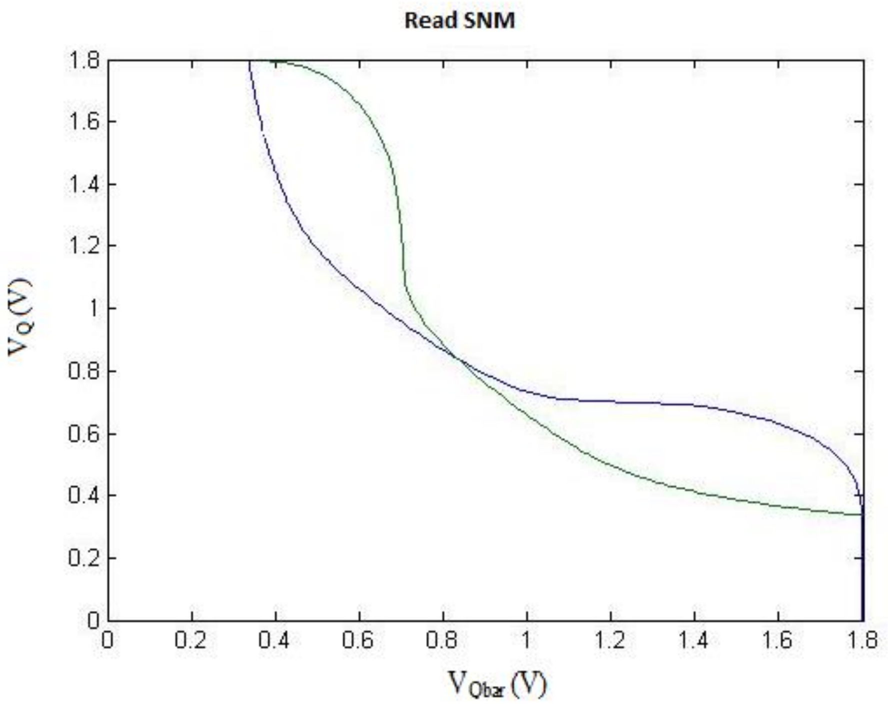

Figure 4.4: Reduced Read SNM of SRAM cell due to Noise

Cell Ratio	Read SNM (mV)
2	200
3	223
4	236
5	246

Table 4.1: Cell Ratio versus Read SNM Comparison for 6T

The cell ratio (CR) represented by Equation 2.1 is defined as the ratio of the dimensions of the driver transistor to that of the access transistor.

$$Cell - Ratio = \frac{W_{driver}}{L_{driver}} \div \frac{W_{access}}{L_{access}} \tag{2.1}$$

The rise of voltage at the node containing ‘0’ in the 6T SRAM cell depends on the cell ratio of the cell. The impact of cell ratio on the read SNM of the 6T SRAM cell is illustrated in Table 4.1. It can be observed that larger CRs provide improved stability but at the expense of larger cell area. A smaller CR ensures a more compact cell with moderate speed and stability. The dependence of the read SNM on the operating voltage and the process corners can reveal valuable information about the stability margins of the SRAM cell in consideration. Scaling down of supply voltage from one technology node to the other reduces the read SNM. The impact of supply voltage scaling on 6T SRAM read stability is illustrated in Figure 4.5.

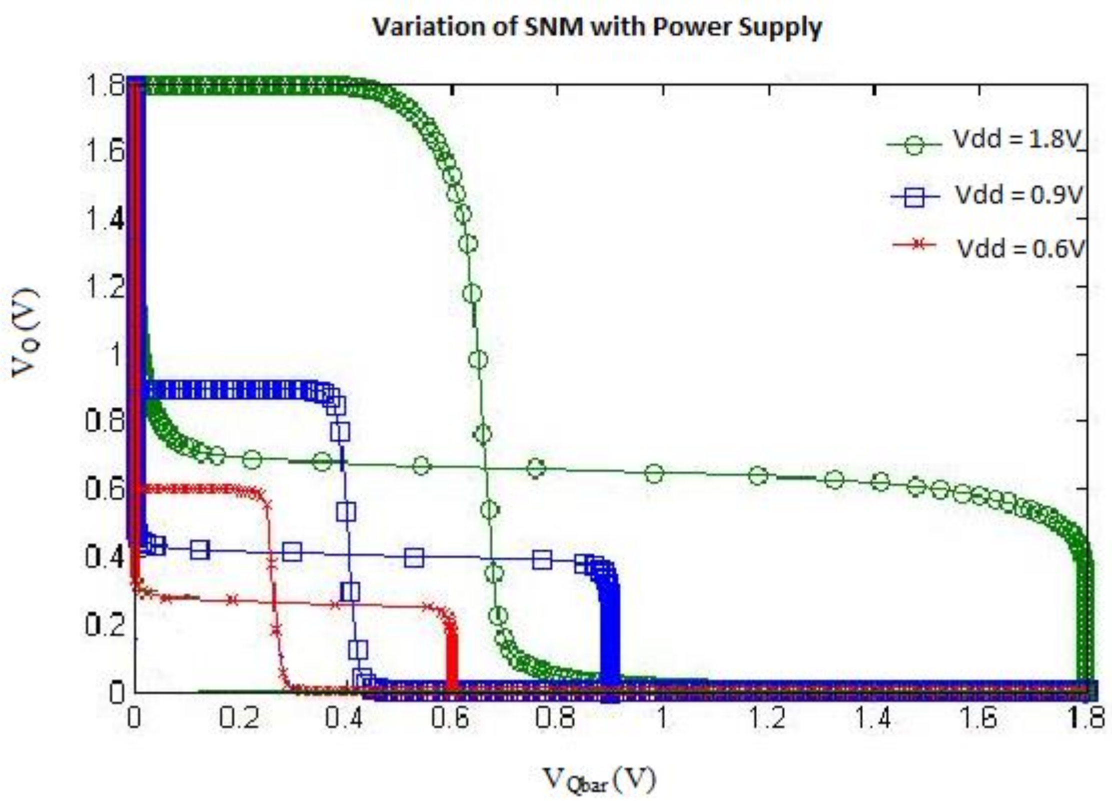

Figure 4.5: Variation of SNM with Power Supply(V_{dd})

It is clear that the eye of the butterfly curves for the SRAMs with lesser supply voltage is smaller, which translates to lesser read SNM and hence the cells are more susceptible to process or environmental variations at reduced supply voltages. As discussed in section 2.1, it is important to assess the impact of environmental variations on the circuit performance and stability. Modern SoCs are often subjected to operations which could greatly vary the on-die temperature. The impact of temperature on the cache stability is illustrated by Figure 4.6. The read SNM decreases with increase in temperature, as illustrated in Figure 4.6. It is evident that worst case read SNM occurs at the FS (Fast NMOS and Slow PMOS) process corner. This is because at the onset of the read operation, the voltage rise at the node containing ‘0’ would be more at the FS corner when compared to the nominal case due to the relatively strong NMOS transistors. Similarly, the SF (Slow NMOS and Fast PMOS) is the best case process corner since the ΔV is least compared to the other process corners.

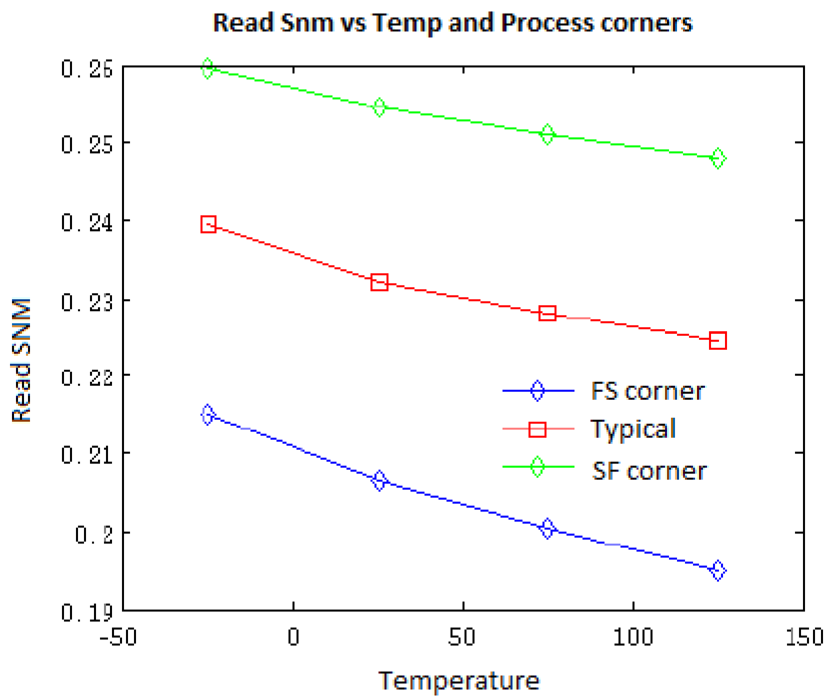

Figure 4.6: Read SNM vs. Temperature and Process Corners

2. Write Noise Margin

Write Noise Margin (WSNM) is measured by using VTC curves, which are obtained from the dc simulation of sweeping the input of the inverters of the SRAM cell [21]. In this section of thesis, four existing static approaches for measuring write margin have been introduced. The most common static approach uses SNM as a criterion. The cell is set in the write operation as shown. Write SNM (WSNM) is measured using butterfly (or VTC) curves , which are obtained from a dc simulation sweeping the input of the inverters (QB and Q). For a successful write, only one crosspoint should be found on the butterfly curves, indicating that the cell is monostable. WSNM for writing ‘1’ is the width of the smallest square that can be embedded between the lower-right half of the curves. WSNM for writing ‘0’ can be obtained from a similar simulation. The final WSNM for the cell is the minimum of the margin for writing ‘0’ and writing ‘1’. A cell with lower WSNM has poorer write ability.

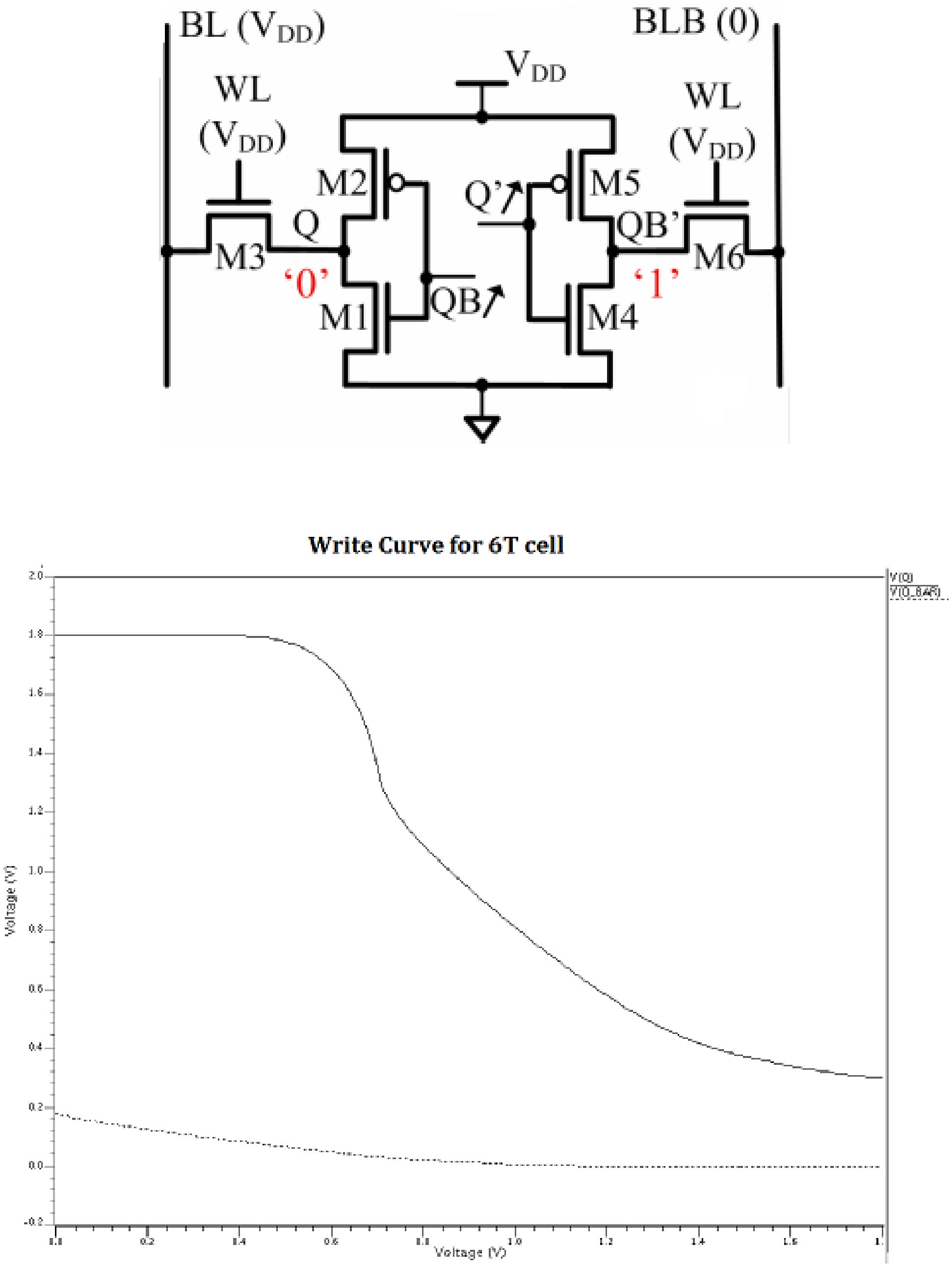

Figure 4.7: Circuit 1 to calculate Write Noise Margin[21]

Second definition of write margin measures the WL voltage on the half-cell holding ‘1’ [3], which we call VWLR. The authors showed that VWLR is inversely proportional to the access transistor mismatch over a wide PVT range. Figure 3a shows the circuit setup. The WL (WLL) and the input of the left half-cell are always VDD so Q remains at its lowest dc value due to a read and connects to the input of the right half-cell. The voltage of WLR, the WL at the right half-cell, is swept from 0 to VDD during dc simulation. The write margin is defined as the margin between VDD and the critical WLR value at which QB reaches the switching point of the left half-cell, VML. We can get the VML value, which is 0.474V, from previous VTC curve. Figure 3b shows that the VWLR write margin for this cell is 0.237V

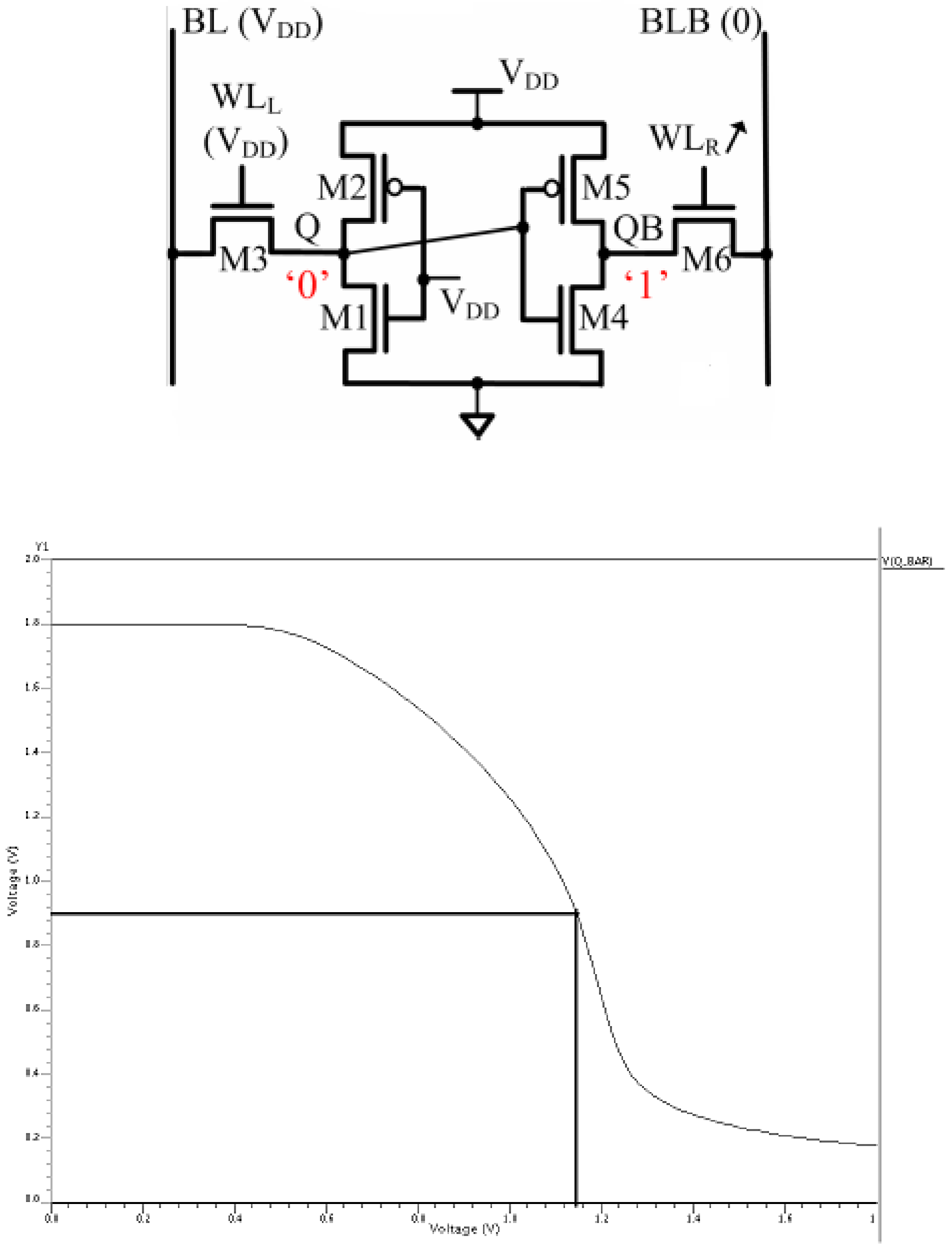

Figure 4.8: Circuit 2 to calculate Write Noise Margin[22]

Another static method uses an N-curve, which was first proposed by [4] for read stability. [5] extended the use of the N-curve to be a measure of write ability. The unique feature of the N-curve is the use of the current information. In Figure 4a, the cell initially holds ‘0’ and both the two bitlines are clamped to VDD. A dc sweep on node ‘1’ (QB) is performed to get the current curve through the dc source (Iin). Figure 4b shows the Iin curve for the example cell. The current curve crosses over zero at three points A, B and C from left to right. The curve between C and B is the relevant part for write ability. [5] defined the voltage difference between C and B as the write trip voltage (WTV), defined the negative current peak between C and B as the write-trip current (WTI), and stated that a higher WTV or WTI implies a smaller write margin.

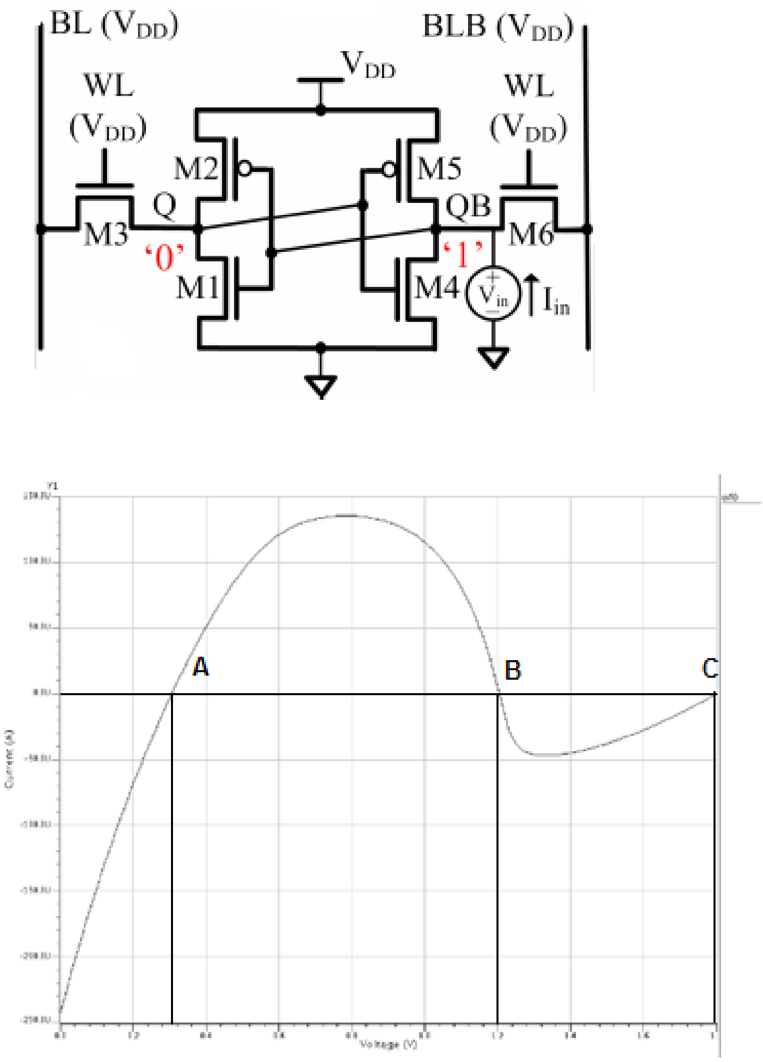

Figure 4.9: Circuit 3 to calculate Write Noise Margin [23]

It should be noted that WTI actually is the current when VBL reaches the trip point as using the BL method. But these two metrics are not equal. Because of different access transistor strength, cells with the same VBL value might have different WTI values and vice versa.

The final static method is an improvement over the previous WL method [6]. Instead of only sweeping the WL at the side holding '1', this approach sweeps the WL at both sides simultaneously to replicate a real write operation, where a WL pulse drives both of the access transistors. The write margin is defined as the difference between VDD and the WL voltage when the nodes Q and QB flip (see Figure 5). We call this metric VWL.

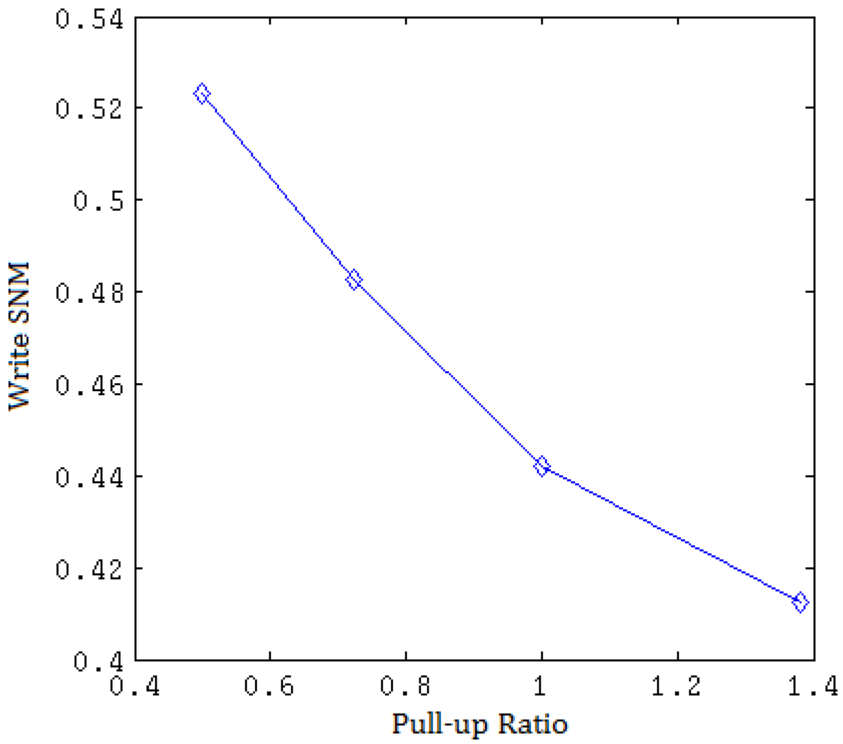

Figure 4.10: Pull-up ratio versus read SNM

Supporting Work

All the SRAM cells are sized to occupy minimum area and are designed and verified for successful read, write and hold functionality. The cells are designed using commercial 180 nm CMOS models. All the simulations are performed at FS process corner which is the worst-case process corner and 125 C temperature.

Static Noise Margin

With increased device variability in nanometre scale technologies, SRAM becomes increasingly vulnerable to noise sources. The wider spread of local mismatch leads to reduced SRAM reliability. For the demand of minimizing power consumption during active operation, supply voltage scaling is often used. However, SRAM reliability is even more suspect at lower voltages. Static Noise margin was defined earlier as the measure of stability of the SRAM cell to hold its data against noise. Since the basic structure for storing the data is almost same so, hold SNM is same for all the cells. However, due to different read mechanisms, the Read SNM varies and has been discussed here.

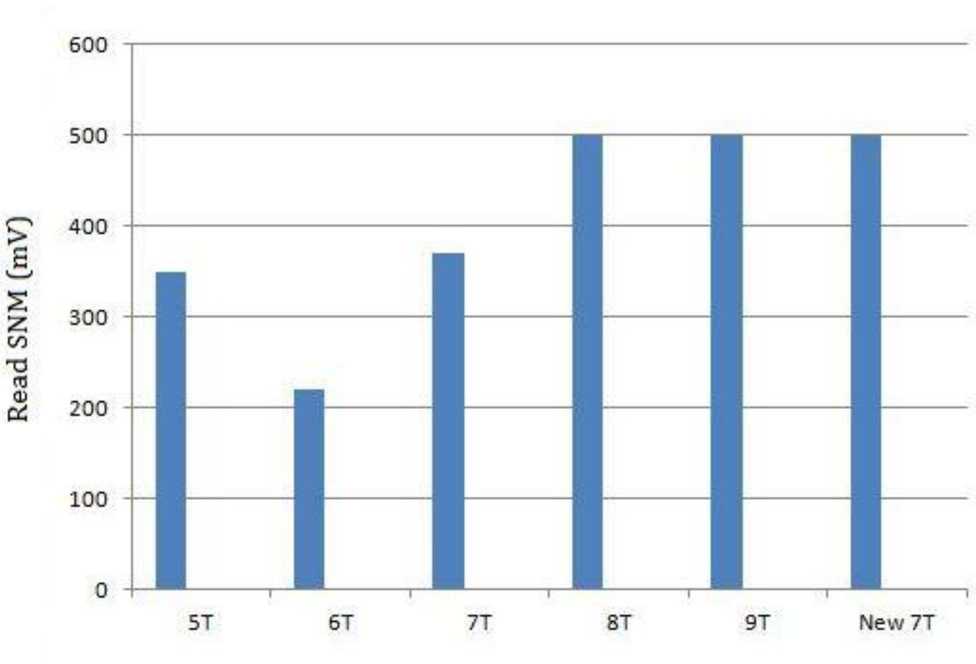

Figure 4.11: Comparison of Read Static Noise Margin for Different SRAM Cells

The read SNMs of the SRAM cells are compared in Figure 4.10. The read SNM of 6T cell is 56% lower than read SNM of the 8T SRAM, 9T SRAM and the New 7T SRAM cell proposed in this thesis. However, when compared to 5T SRAM cell, 6T read SNM is only 37% lower than that of 5T SRAM while when compared to 7T SRAM, 6T read SNM is 41% lower. This can be attributed to the fact that during the read operation the internal nodes of the 5T SRAM are not completely isolated from the read discharge path whereas that of in case of 7T one of the internal node is partially isolated due to presence of another transistor in between. The other three SRAM cells have their internal nodes completely decoupled from the read discharge path. It can also be observed that the read SNMs of the three cells 8T SRAM, 9T SRAM and New 7T SRAM cell are identical. This is because the basic circuit that responds to the SNM simulation is same for all the three SRAMs—i.e., the 6T bitcell of the corresponding cell is completely isolated from the read buffer and acts as a 6T SRAM in hold state.

Write Noise Margin

Read stability of a cell is important and was discussed in the previous section. But apart from the read stability, the write stability is also very important concept. Write Noise Margin is the measure of writability of the cell, i.e. how easily can the cell be written to. Various methods to calculate the write noise margin were discussed before in this chapter. The writability of various cells was measured and shown below.

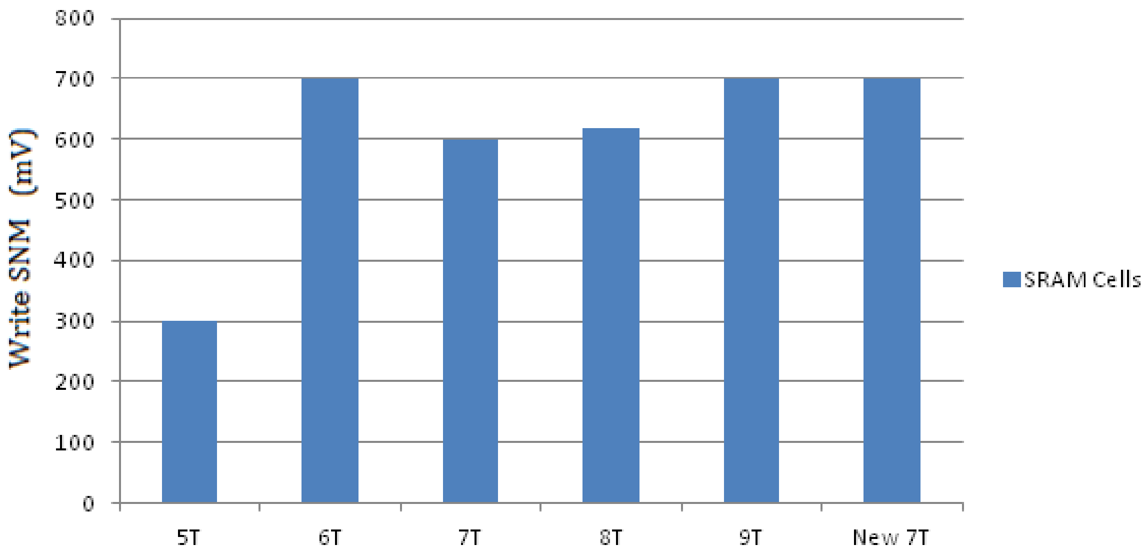

Figure 4.12: Comparison of Write Static Noise Margin for Different SRAM Cells

As seen the 6T and 9T cell have almost the same writability because their basic structure is same with only the read operation being different in the 9T cell. The 5T cell has almost 57% lower writability than 6T and 9T because of single sided read and write. Due to just a single bitline, it has to fight against two cascaded inverters to flip the data while in 6T and 9T, double sided operation aids the write. The new 7T proposed in this thesis has higher WNM than 6T since it has double sided write operation i.e. both data and inverted data are fed via

BL and BLB, but still the write has to go through only one inverter effectively. So, the new 7T has greater writability. Due to greater writability, the speed of the new 7T is also, comparable to that of the other cells in spite of one less inverter. This is discussed in next section.

4.3 Delays

Access times are the times that it takes for the read and write operations of the SRAM cell to complete. Two access times that are important are the read access and the write access times.

We want to reduce the access time of RAM cell to make it faster to work with high speed computing systems. Read Access Time is the time required to read the data from the cell and is calculated as the time delay between 50% WL activation to when the sense amplifier has reached 90% of its full swing. Now a days, sense amplifiers reach their 90% output as soon as the difference between the input voltages exceeds 150 mV. Below are the read and curves for the proposed 7T SRAM cell.

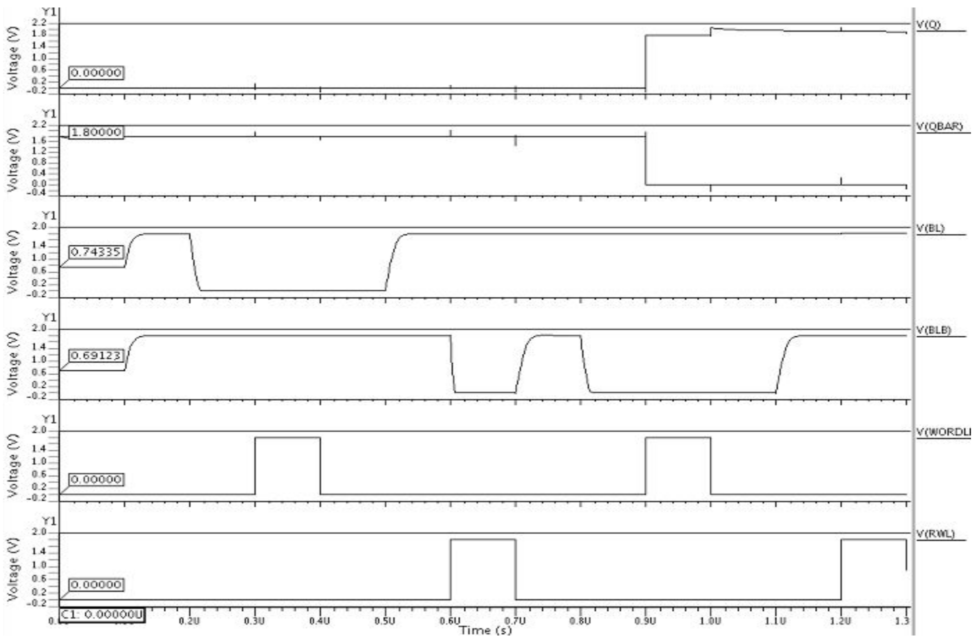

Figure 4.13: Timing Diagram of Read and Write for the proposed 7T cell

The write delay of various SRAM cells has been compared in figure 4.12. As shown below the write delay is dependent on the load that bitlines have to face when writing into the cell.

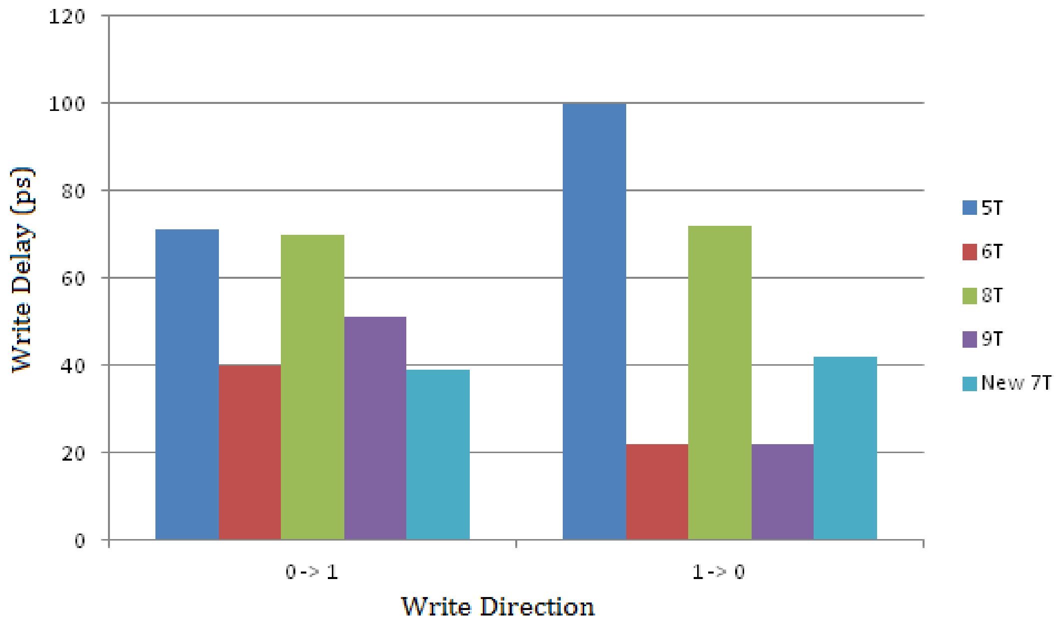

Figure 4.14: Comparison of Write Delays for different SRAM Cells

In the chart above, two different write delays are shown. One is when '0' is already stored in the cell and '1' has to be written and the second category is for the opposite case. From the chart above, it is clear that the 5T has highest write delay for writing '0' as well as for writing '1' and hence is worst cell for this speed although it does has an advantage of less area. The 8T cell is also not very good. But 9T and 7T have delays comparable to 6T for the '0' to '1' case. But suffer in the '1' to '0' case.

Similarly the comparison of read delays is also shown. Read is a really long procedure since it requires a sense amplifier circuit as well. As shown in the figure 4.14 read delay for 6T is very high while reading '1' as well as while reading '0'. This is because although double ended sensing is used in 6T, but one of the bit line has to discharge through the stack of driver and access transistors. Read delay for all the SRAM cells employing single sided read is almost negligible for any one of the values i.e. either '0' or '1'. 8T has 10ps read '0' delay but high read '1' delay. 9T has almost same read delay for both '0' and '1'. The proposed new 7T SRAM cell has negligible read '1' delay but has a read '0' delay which is very less. So, even for read the new 7T SRAM cell is very fast.

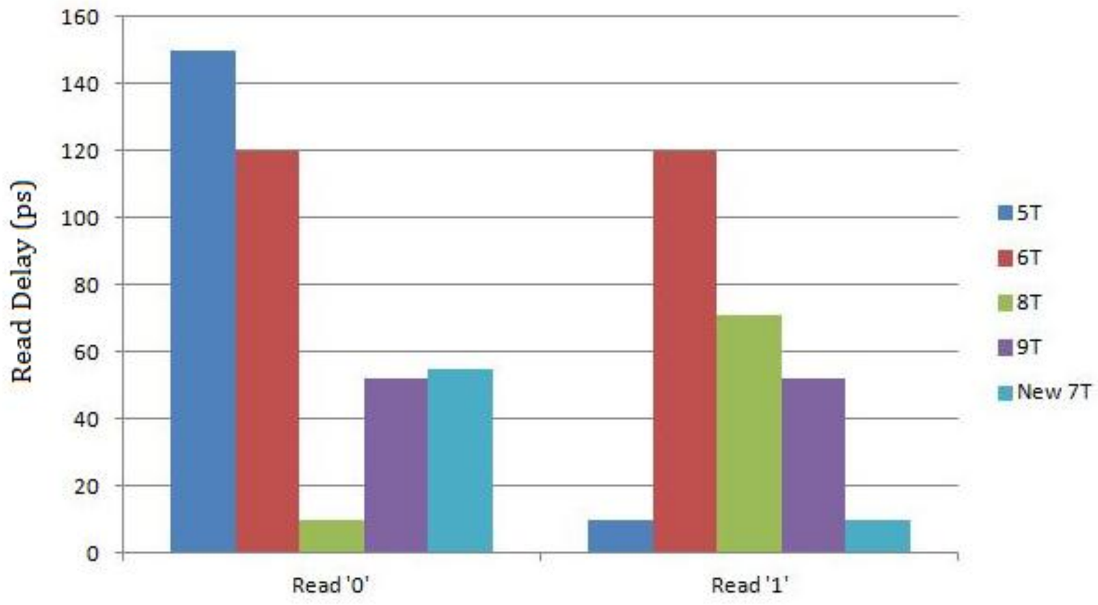

Figure 4.15: Comparison of Read Delays for different SRAM Cells

4.4 Leakage

The static power consumption in an SRAM unit is mainly due to the leakage current in SRAM cells. Leakage is defined the power consumption of RAM cell in standby mode. Figure 4.15 shows the comparison of leakage currents of different SRAM cells including the 6T and the proposed 7T cell. Leakage of any SRAM cell depends on which transistors are in OFF mode during the hold state. This is due to the fact that only the OFF transistors are leakers during the hold state of SRAM cell. As was shown earlier in this chapter in 6T cell, at any time during hold i.e. while holding '0' or '1', two transistors of the holding cell, remain off. These two transistors form the source of leakage along with the two access transistors. As shown in the chart in figure 4.15 all the older cells have a similar leakage profile while storing both '0' and '1'. This is because their basic storage element has same transistors for storing both bit and inverted bit. i.e. have a symmetric structure. The new 7T proposed in this thesis however has an asymmetric structure and thus shows different amount of leakage for different data. It is clear from the structure of the new cell that while storing '1', only one transistor is leaking in contrast to opposite situation. Hence, the new 7T SRAM has up to

30% lower leakage current, which is very advantageous for low power and battery operated devices, proving again that the new 7T cell is better.

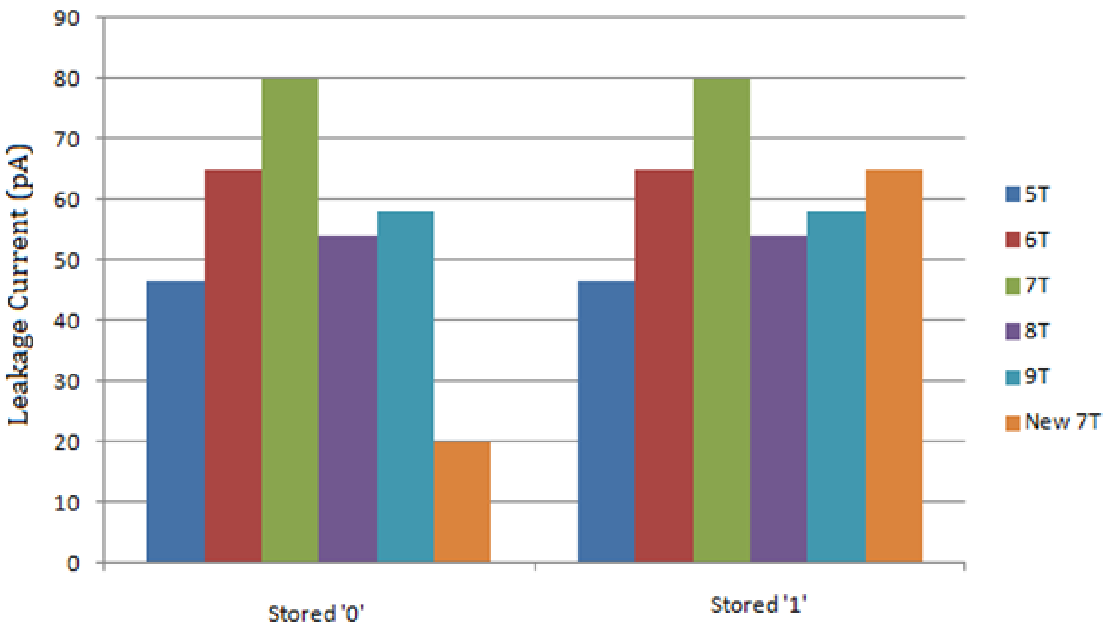

Figure 4.16: Comparison of Leakage currents in hold state for different SRAM Cells

4.5 Sizing and Layout

Sizing of the new 7T SRAM cell proposed in this thesis has been done keeping in mind the cell stability issues. Since read operation is isolated from the cell, so there is no issue of read stability in the new cell.

SRAM	5T SRAM	6T SRAM	7T SRAM	8T SRAM	9T SRAM	New 7T SRAM
No. of MOSFETs	5	6	7	8	9	7
No. of WL	1	1	2	2	2	2
No. of BL	1	2	2	1	2	2

Table 4.2: Area overhead comparison of different SRAM cells

For write stability, care has to be taken that while writing '0', voltage at Q should not exceed switching point of the inverter, but since a PMOS access is used which has a higher resistance than the driver NMOS transistor, this issue was solved inherently. Also, for writing

'1', the NMOS transistor has to be turned off, this was inherently ensured by a stronger access transistor at Qbar. But keeping the access transistors minimum sized severely affects the write delay . So, for speeding up the write and increasing writability, the sizes of access transistors were increased as shown. The sizes were determined by tradeoffs between area and speed.

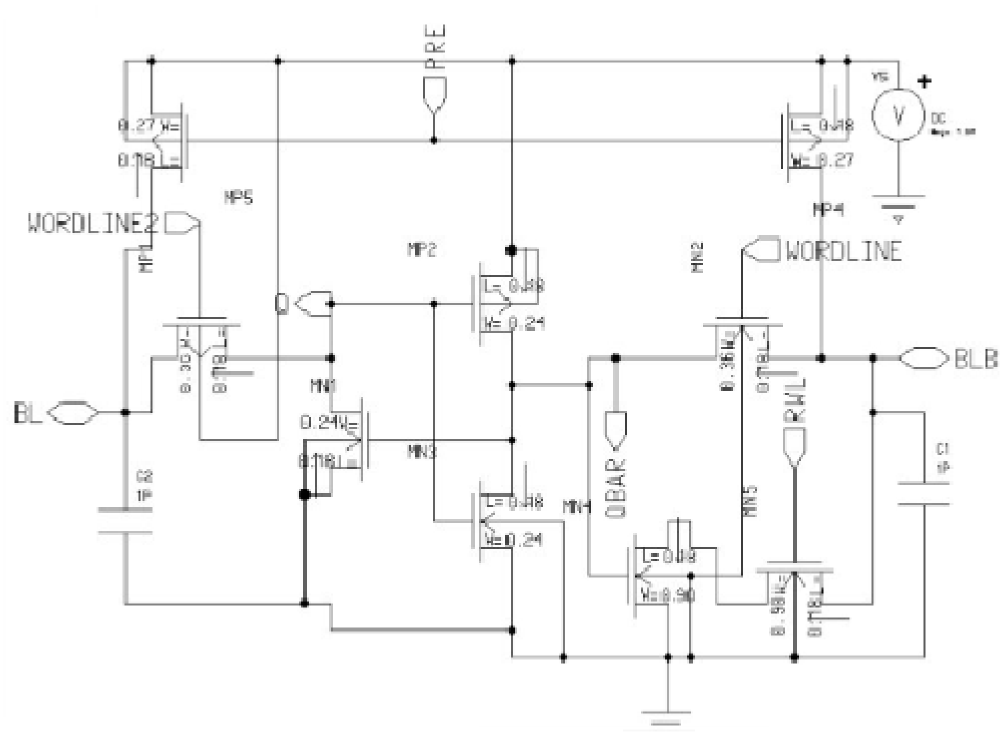

Figure 4.17: Seven-transistor SRAM cell with final sizes

The bitcell area is an important parameter for cache design since it directly relates to the cache footprint, array density and the overall SoC cost. The previous-published SRAM bitcells have a substantial area overhead when compared to the traditional 6T SRAM cell. It can be observed that in spite of the 8T (33% area overhead) and 9T cells (56% area overhead) they offer better read and write stability compared to the conventional 6T cell. The proposed 7T cell exhibits better area savings when compared to 8T[24] and 9T[34] cells. Even though the proposed 7T SRAM has 13% area overhead compared to the conventional 6T SRAM cell, it outperforms the 6T SRAM cell when the read, write static noise margins and bitline leakage values are compared. The 5T SRAM cell has two less transistors than the proposed 7T cell but it is also important to notice that the 5T SRAM cell lower stability and consumes more bitline leakage power.

CHAPTER 5 CONCLUSION AND FUTURE WORK

Conclusion

In this thesis, various SRAM cell structures have been simulated and analyzed with regard to stability, i.e. read noise margin and write noise Margin, read and write delays, leakage and area along with some other parameters. In the present work, the 5T [12], 7T [13], 8T [14], 9T [15], SRAM cells are designed and simulated for correct functionality. All these cells are successful in addressing the read stability problem associated with the 6T SRAM cell. 9T [15], was found to be the best among them. However, the cells suffer from bitline leakage problem which results in a wrong value being read by the sense-amplifier and also places constraints on the number of cells that can be accommodated on the bitlines. It was found that there is still scope for improvement as far as the memory cell was concerned.

In this thesis, a novel 7T SRAM cell is proposed which drastically reduces leakage power dissipation, even when most of the cache is holding live data most of the time. The proposed 7T cell simultaneously addresses the read stability as well as the bitline leakage problems. The 7T cell is designed and simulated for successful read and write operations. The butterfly curves for the proposed cell are plotted and the read/hold SNMs are evaluated and it is proved that the read SNM of the proposed design is better than that of the 6T SRAM cell. As can be seen in the data given in chapter 4 that Read SNM of proposed cell is equal to that of 9T cell which is 56% greater than that of 6T cell. Also, Write SNM of proposed cell has been found to be same as that of both 6T and 9T cells. The new cell, although requires an additional bitline over the conventional memory cell (6T), and adds to area overhead but improves in all other aspects. But here also, it is still better than 9T cell since proposed cell adds only 13% area as compared to 56% overhead of 9T cell. The bitline leakage power consumption by the current design is evaluated and compared with the previous designs. The proposed cell has 37% lower standby leakage than 6T and 29% lower leakage than 9T SRAM cell. And this leakage continues to improve as on an average cache holds more zeroes than ones. So, from the above results, we can conclude that 9T cell is the best solution among all the other cells compared and the proposed 7T SRAM cell has better parameters than both 6T and 9T functionally.

Future Work

The proposed 9T SRAM cell can be further improved. Some suggestions for future work are:

1. Read and write-assist techniques can be explored which could give a better read and write performance for the proposed design. During the read operation, the RWL voltage which drives the transistors on the read discharge path can be boosted to improve the read performance.

2. The rapid growth of battery operated handheld devices like cell phones, GPS devices, music players etc have increased research in decreasing the power consumption of these devices. These devices typically use low power SoCs. Since the caches make up the bulk of the transistors on SoCs, it is imperative that the cache design incorporates techniques to reduce the power consumption. The proposed SRAM can be investigated for sub-threshold operation.

3. The Monte Carlo simulations were not present in the tool available in the lab. So, Monte Carlo simulations can be performed to check for process variation.

4. Cell has been designed in 180nm CMOS technology which is used less now a days, so a porting to a 65 nm technology could be done to evaluate the impact of scaling on the 7T SRAM cell.

5. Some lw power techniques can also be applied to 7T SRAM for example MTCMOS and VTCMOS to reduce power dissipation even further.

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+rsc= 0                 rdc= 0

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+Eta0= 8.5000000        Etab= 0.00           Dsub= 2.8000000

+Pclm= 2.0000000        Pdiblc1= 0.1200000   Pdiblc2= 8.0000000E-05
+Pdiblcb= 0.1450000     Drout= 5.0000000E-02 Pscbe1= 1.0000000E-20
+Pscbe2= 1.0000000E-20  Pvag= -6.0000000E-02 Delta= 1.0000000E-02
+Alpha0= 0.00           Beta0= 30.0000000

+kt1= -0.3700000        kt2= -4.0000000E-02  At= 5.5000000E+04
+Ute= -1.4800000        Ua1= 9.5829000E-10   Ub1= -3.3473000E-19
+Uc1= 0.00              Kt1l= 4.0000000E-09  Prt= 0.00

+Cj= 0.00138            Mj= 1.05             Pb= 1.24
+Cjsw= 1.44E-09         Mjsw= 0.43           Php= 0.841
+Cta= 0.00093           Ctp= 0               Pta= 0.00153
+Ptp= 0                 JS=1.50E-08          JSW=2.50E-13
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+N=1.0	Xti=3.0	Cgdo=2.786E-10
+Cgso=2.786E-10	Cgbo=0.0E+00	Capmod= 2
+NQSMOD= 0	Elm= 5	Xpart= 1
+Cgsl= 1.6E-10	Cgdl= 1.6E-10	Ckappa= 2.886
+Cf= 1.058e-10	Clc= 0.0000001	Cle= 0.6
+Dlc= 3E-08	Dwc= 0	Vfbcv= -1