"Modeling and Performance Analysis of Mixed CNT Bundle as VLSI interconnect"

A Thesis Submitted in Partial Fulfillment of the Requirement for the Award of the Degree of

Master of Technology
In
VLSI Design

Submitted By

Arvind Thakur

Roll No: 601562005

Under Supervision of

Dr. Karmjit Singh Sandha

Assistant Professor

ELECTRONICS AND COMMUNICATION ENGINEERING DEPARTMENT

THAPAR UNIVERSITY, PATIALA, PUNJAB

JUNE, 2017

DECLARATION

I, Arvind Thakur hereby declare that the work presented in this thesis entitled "**Modeling and Performance Analysis of Mixed CNT Bundle as VLSI interconnect**" in partial fulfillment of the requirement for the award of degree of Master of Technology in VLSI Design submitted at Electronics and Communication Engineering Department, Thapar University, Patiala is an authentic record of my own work carried out by me under supervision of **Dr.Karmjit Singh Sandha**(Assistant Professor, ECED, Thapar University) from 2015 to 2017. The matter presented in this has not been submitted either in part or full to any other university or institute for the award of any other degree.

Date 21-08-2017

Arvind Thakur
Roll. No. 601562005

It is certified that the above statement made by the candidate is correct to the best of my knowledge and belief.

Date 21-08-2017.

DR. KARAMJIT SINGH SANDHA
Assistant Professor
ECED, Thapar University
Patiala

ACKNOWLEDGEMENT

This report has only been possible with the constant guidance and expertise of Dr. Karmjit Singh Sandha, Assistant Professor, Electronics and Communication Engineering Department, Thapar University, Patiala and I would like to take this opportunity to express my sincere gratitude to him.

I am also thankful to Dr. Alpana Agarwal, Head of ECE Department, for providing us the adequate infrastructure for carrying out the work.

I am also thankful to Dr. Hem Dutt Joshi, PG Coordinator as well as Dr. Anil Arora, Program Coordinatorand the entire faculty and staff of Electronics and Communication Engineering Department for th**e** motivation and inspiration that triggered me for the work.

I would also like to thank my friends Ashima and Caffey who always motivated me and have more or less contributed to the preparation of this report. I will be always indebted to them.

Last but not the least, I would like to thank my parents for their years of unyielding love and encourage. They have always wanted the best for me and I admire their determination and sacrifice.

ABSTRACT

The bottleneck in the VLSI circuit is an interconnect delay. With the downscaling in the technology nodes, interconnect delay dominates the gate delay. In the semiconductor industry device size is decreasing year by year and the numbers of components on the integrated chips are increasing, each year. With the scaling in the technology nodes, it was observed by the researcher that there is a problem of grain boundary scattering, surface scattering and electro migration in Copper (Cu) as interconnect. So there is great necessity of alternative material which is better than Cu interconnect. As the Cu interconnect is prone to issues with downscaling in technology, Carbon nanotubes (CNTs) are one of the good selection to Cu for VLSI interconnect as it has high current carrying capacity and large thermal conductivity.

In this research work, mixed CNT bundle as an interconnect for very large scale integration (VLSI) circuits is analyzed. Using the hierarchical modelling, MCC model of mixed CNT is developed. The mixed CNT bundle contains both MWCNTs and SWCNTs. The performance of mixed CNT bundle is better than MWCNT bundle at intermediate, global and local levels. The propagation delay and power delay product (PDP) is estimated at intermediate, global and local levels for mixed CNT bundle using Tanner EDA tool and simulation is done using SPICE files. Due to the insertion of SWCNTs surrounding (side-walls and corners) the MWCNT, the conductivity is increased because the SWCNTs increases the density of shells and therefore, decrease in the overall effect of resistance and inductance of MWCNTs connected vertically in parallel to each other. The structure is analyzed for different technology nodes i.e. 32nm, 22nm and 16nm at differentinterconncts lengths. Based on the comparative result, it is observed that the overall propagation delay and the power delay product (PDP) of mixed CNT are decreased as compared to SWCNT and MWCNT interconnect

TABLE OF CONTENTS

LIST OF ACRONYMS

VLSI	Very Large Scale Integration
IC	Integrated Circuit
CNT	Carbon Nanotube
SWCNT	Single-Walled Carbon Nanotube
MWCNT	Multi-Walled Carbon Nanotube
MCB	Mixed CNT Bundle
MCC	Multi Conductor Circuit
ESC	Equivalent Single Conductor
MTL	Multi Conductor Transmission Line
PDP	Power Delay Product

LIST OF FIGURES

LIST OF TABLES

CHAPTER 1
INTRODUCTION

The advancement in technology has major impact is in the field of electronics. In the semiconductor industry device size is decreasing year by year and the number of components on the integrated chip are increasing every year. Gorden Moore, the co-founder of Fairchild Semiconductor and Intel made an observation that chip performance doubled in every two years. According to Moore's Law, the number of transistors per integrated circuit doubles every 18 months and this increase the chip performance. Moore estimated that this trend will be followed in the upcoming future; however the rate at which the technology has advanced, his expectations have long been surpassed and now deep sub-micron technology level has been reached. For last few decades Moore's law has been the motivating force behind the semiconductor industry and this will dramatically increase the required power, and decrease the relative cost exponentially.

The downscaling of technology effects power dissipation and propagation delay of the device. The propagation delay is determined by the delay caused due to logic gates, interconnect wires and fan-out loads on wire [1]. Gate delays are independent of device sizing, so for the submicron technologies gate delay has decreased significantly. The small device size increases the number of transistors on the chip and the results in increased power dissipation and large wire delays [2].

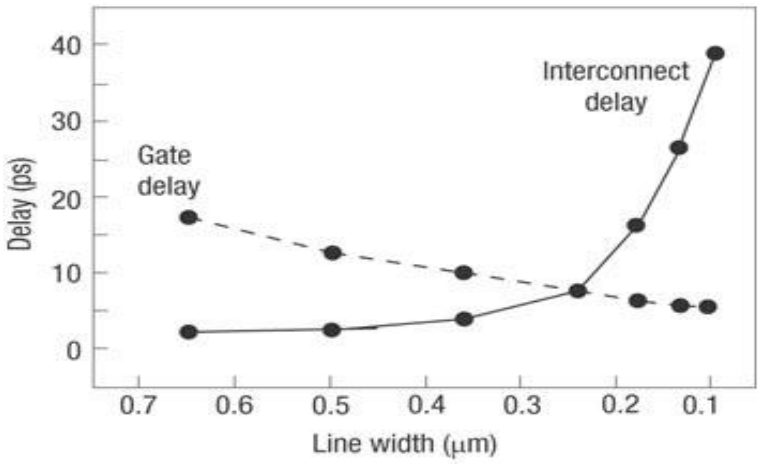

Figure1.1 Transistor gate delay and interconnect delay with IC fabrication technology [3]

From Figure 1.1, it is observed that with the reduction in line width (device size) of integrated circuits, gate delay decreases and interconnect delay dominates the gate delay.

This chapter is a introduction to the importance of interconnects at the submicron technology level, use of copper as an interconnect and the development of carbon nanotube as an interconnect to overcome the disadvantages of copper.

1.1 VLSI INTERCONNECTS

The thin film conducting material which offer an electrical path between the nodes of the circuit formed on the chip is defined as a VLSI interconnect. It can also be defined as a set of conducting wires that are needed to connect the transistor to perform the circuit function and these set of wire which connect the device on chip are called Interconnect [4, 5].

The basic operation of an interconnect is to distributes the clock, power supply, I/O and other interlinking signals in an integrated circuits. The basic structure of interconnect is shown in Figure 1.2

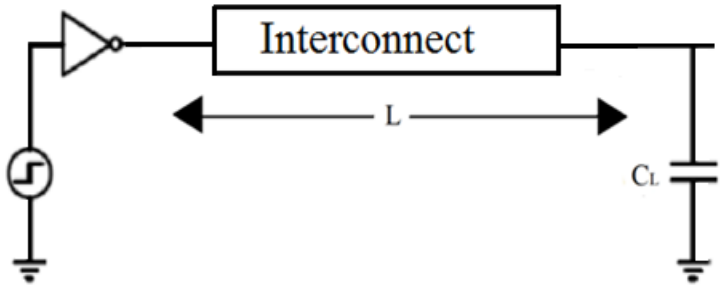

Figure1.2 The basic structure of an interconnect [6]

Classification of an interconnect on the basis of length are as following [5, 7].

1.1.1 Local interconnects

Local interconnects connects gates and transistors with each other within a functional block. The length of these interconnects are of few hundred nanometers.

1.1.2 Intermediate interconnects

These interconnects are longer , wider as compared to the local interconnects in order to provide lower resistance, intermediate interconnects are used to provide clock distribution as well as signal distribution within a few functional block (intra-module) and are valid up to atypical lengths up to 0.5 to 1 mm.

1.1.3 Global interconnects

Global interconnect provides clock and input-output signals between functional blocks. The top one or two layers are occupied by the global interconnects. The length of global interconnects maybe as long as half of the chip parameter starting from few thousand micrometers (μm) i.e. few millimetres (mm).

Earlier Aluminium was used as a material for interconnect in integrated circuits (ICs) and it proved to be a good choice because of its following properties

- Resistivity is low
- Deposition ofAluminium is easy
- Dry etching
- Does not contaminate Si
- Adhesion to dielectrics is excellent

The other advantage of Aluminium was its good ohmic connection with the silicon But with the reduction of device size, the current density of interconnect increased. The disadvantage of Aluminium interconnect was that at high current density, electron migration effect was observed. Electron migration is a process in which high current density causes alteration of shape of conductor which eventually leads to breaking of conductor [4, 7, 8]. At such a stage there was a need of better interconnect. So copper came as a strong contender for interconnect.

1.2COPPER AS AN INTERCONNECT

The first alternative for the problems faced by Aluminium was to change material itself and so the Copper was introduced as a replacement. The improved electron-migration resistance of the copper conductor as interconnect [9] resulted in high current density of copperconductor as compared to that of Aluminium. Copper replaced Aluminium as a VLSI interconnects as it could withstand five times larger current density when compared with Aluminium. The combinations of increase in conductivity of interconnect material along with the improvement in its electron migration proved very useful. Due to all these advantages copper become the promising candidate for μm technology. To analyze Copper as interconnect, first of all there is a need to understand its structure as shown in Figure 1.3, in which a copper as an interconnect bar of width ‘W’, thickness ‘H’ and length ‘L’ is placed at a height ‘Y’ above the ground plane. The gap between ground plane and interconnect is filled with a dielectric material.

To analyze Copper as interconnect, first of all there is a need to understand its structure as shown in Figure1.3, in which a copper as an interconnect bar of width ‘W’, thickness ‘H’ and length ‘L’ is placed at a height ‘Y’ above the ground plane. The gap between ground plane and interconnect is filled with a dielectric material.

Using Figure1.3, the values of resistance, capacitance and inductance of a Copper interconnect are defined as:

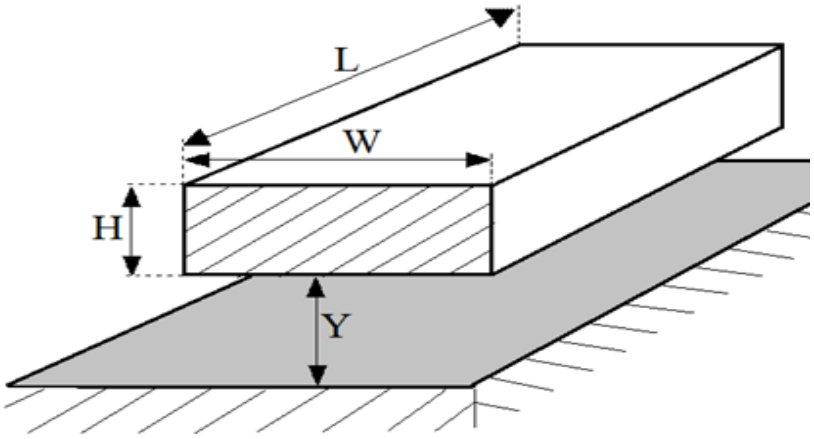

Figure1.3 An insight to an interconnect Structure [1]

1.2.1 Resistance

The parasitic resistance of an interconnect line has a significant influence on the propagationdelay of a signal. Parasitic resistance of interconnect depends on the resistivity of usedmaterial (e.g., Copper, Aluminium or Gold) and the dimensions of interconnect [1]. Thecontacts made by interconnects contributes to contact resistance. From the interconnect line shown in Figure 1.3, the parasitic resistance is given as:

$$R_{Cu} = \frac{\rho L}{WH} \qquad (1.1)$$

Where ρ, W, L and H are the characteristic resistivity of material, width, length and thickness of the interconnect line, respectively and unit of R_{Cu} is in kΩ.

1.2.2 Inductance

In a rectangular conductor the inductance is produced due to the changing of current in thewire. In this a magnetic-field is created due to the change in current flow which induces avoltage, thus producing an inductance called self-inductance [10, 11]and is given by the formula: $L_{Cu} = \frac{\mu}{2\pi} L\left[\ln\left(\frac{2L}{W+H}\right) + \frac{1}{2} + 0.22\left(\frac{W+H}{L}\right)\right]$ (1.2)

Here W, L and H are the width, length and height of the rectangular wire, respectively whilethe μ is the permeability of the wire and the unit of L_{Cu} is in pH.

1.2.3Capacitance

Now the interconnect line is considered as a conducting plate which is parallel to a groundplane acting as another plate, both separated by a distance Y filled by a dielectric material ofpermittivity (ε). As a signal is passed through the interconnect it acquires some charge andacts as a parallel plate capacitance. However the thickness of interconnect (H) is quite noticeable therefore creating fringing electric fields which contributes to another type

ofcapacitance called as fringing capacitance. So the total capacitances C_{Cu} is the summation ofboth parallel plate capacitances and fringing capacitance is given as:

$$C_{Cu} = \varepsilon\left\{\frac{W}{Y} + \frac{\pi\left(1-0.0543\frac{H}{2Y}\right)}{\ln\left[1+\frac{2Y}{H}+\sqrt{\frac{2Y}{H}}.\left(\frac{2Y}{H}+2\right)\right]} + 1.47\right\}L \quad (1.3)$$

The unit of C_{Cu} is aF.

Using these RLC parameters a simple RLC circuit driven by CMOS inverter is obtainedwhich is used for estimating the propagation delay of an interconnect line. With the further scaling of technology nodes, the resistivity of copper interconnect isincreased due to surface roughness phenomenon and grain boundary scattering as shown in Figure 1.4. The increase in resistivity increases the power dissipation and propagation delay [11, 12].

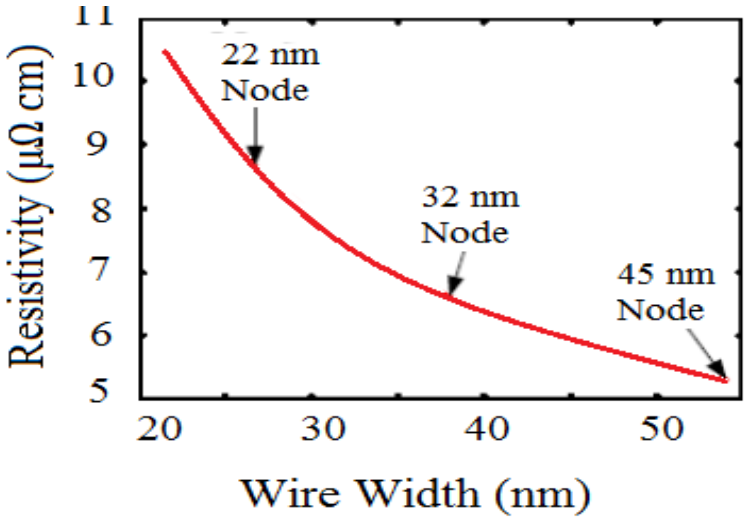

Figure1.4 Change in Cu interconnects resistivity with respect to technology node[1]

To solve these problems, researches are going on to replace copper with other materials. Themost promising candidate for replacing copper as VLSI interconnect and to overcome itsdisadvantages is carbon nanotube (CNT) [7, 13].

1.3CARBON NANOTUBES (CNT) AS INTERCONNECTS

The CNTs are grown by rolling atomic layer of graphite(graphene). The atomic layer is rolled in the hollow cylindrical shape with the diameters in the order of nanometres as shown in Figure 1.5.

Based on the directions in which CNTs are rolled, there are different chirality arrangements of an interconnect such as armchair (metallic),zigzag (mostly semiconductor) and chiral (mostly semiconductor) as shown in Figure 1.6 [13, 14].

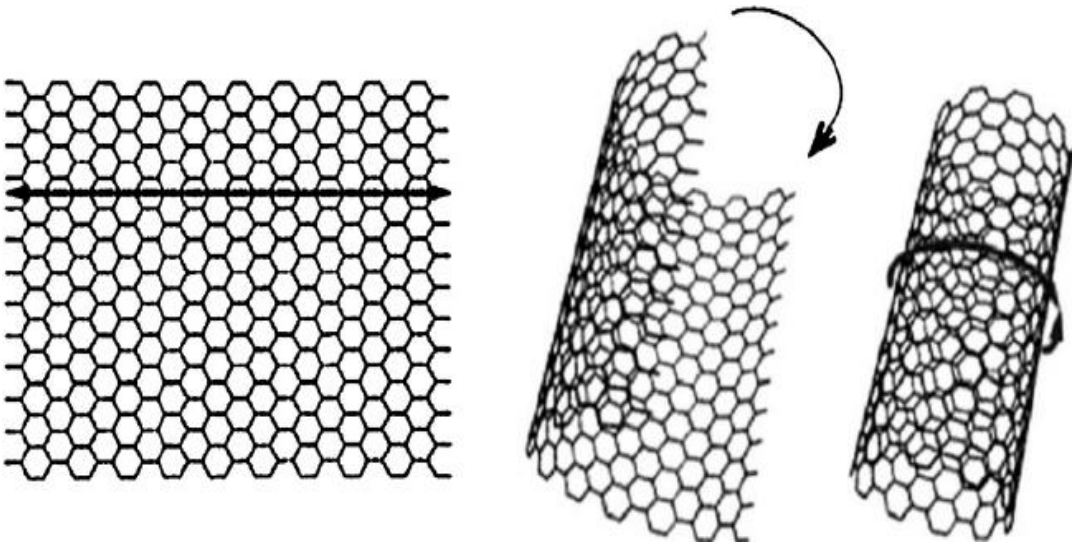

Figure 1.5 Formation of CNT from graphene sheet

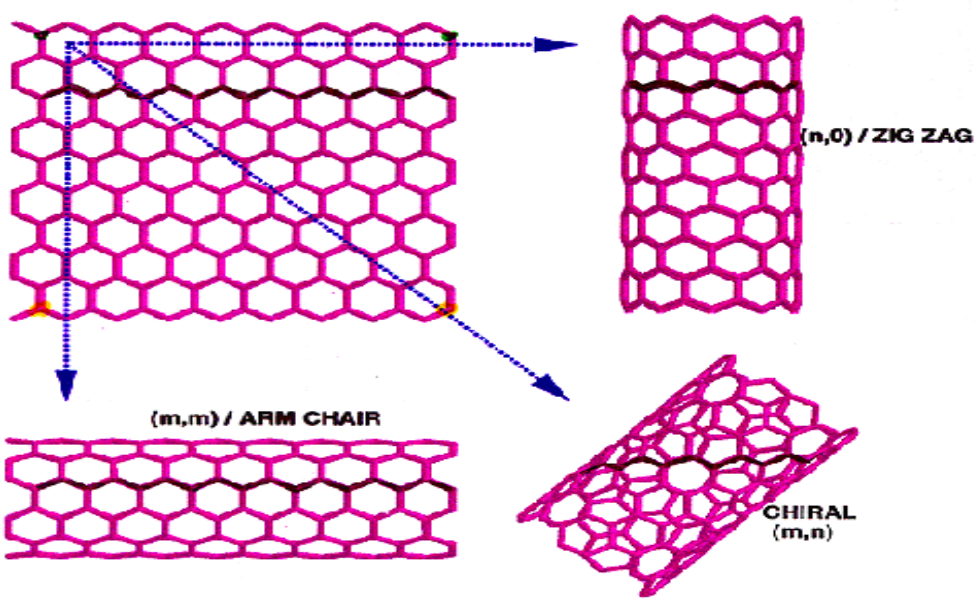

Figure1.6 Direction of rolling of Graphene sheet to obtain desired structure of Metallic (armchair structure) or semi-conducting (zigzag structure) [14]

The main attractive properties of carbon nanotube (CNT) are high current carrying capability, good mechanical and thermal stability and high thermal conductivity [4, 8].

Another advantage of CNTs over copper is that CNT has a long mean free path (MFP)ranging in several micrometers whereas copper has only 40 nm MFP at room temperature,which provides less resistance for short length interconnects [15]. CNTs due to these properties have attracted researchers for its applicability as future VLSI interconnects [4].

On the basis of number of shells CNTs are classified into three categories:

(a) Single-Walled CNT (SWCNT): consists of single cylindrical shell.

(b) Multi-Walled CNT (MWCNT) : consists of multiple concentric cylindrical shells

(c) Mixed CNT: consists of single-walled and multi-walled CNT

1.3.1 Single-Walled Carbon Nanotubes (SWCNTs)

SWCNTs are hollow cylindrical tubes whose diameter ranges from 0.4 to4 nm. These are made from a single graphene layer wrapped in a form of tube [16, 17]. The structure of SWCNT is shown in Figure 1.7. With their discovery in the early 90s, there have been a lot of researches in exploring the electrical properties and on different methods for using this technology in field of electronics. SWCNTs are distinguished based on its chirality and can either be metallic or semiconductor based on the direction in which it is rolled. The difference lies at the point where two ends of the graphene sheets are joined forming zig-zag (mostly semiconducting) or arm-chair (metallic) structure [14, 18] as seen in Figure 1.6. SWCNT has a drawback that its growth type is not controllable, it may having metallic or semiconducting properties and this growth type is not determined before its formation. SWCNTs having metallic properties are better conductor than Copper[15, 17] and this is not true that SWCNTs always have semiconductor properties.

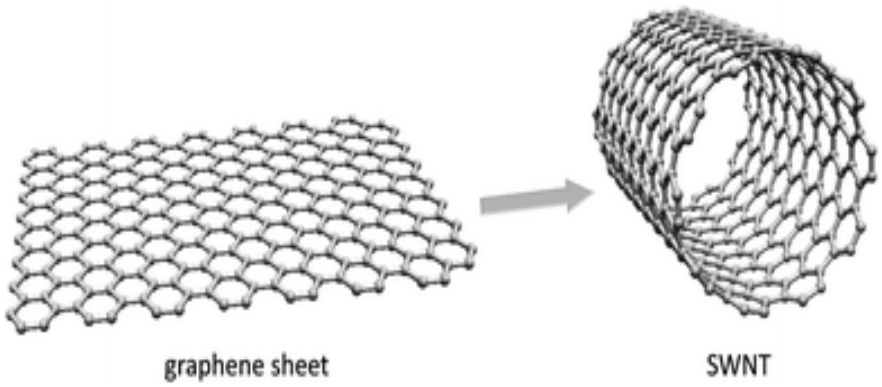

Figure1.7 Structure of SWCNT[19]

MWCNTs are utilized to avoid above problem as these are always act as metal conductor [20]. MWCNTs are having similar current carrying capabilities to that of SWCNTs. But due to the simple fabrication and better control on the growth process than that of SWCNTs these

are preferred over SWCNTs whereas the structure of SWCNT is uncomplicated and can be easily modelled as compare to MWCNTs. However, for the effective study of MWCNTs as an interconnect few models of MWCNTs have been suggested [5, 21].

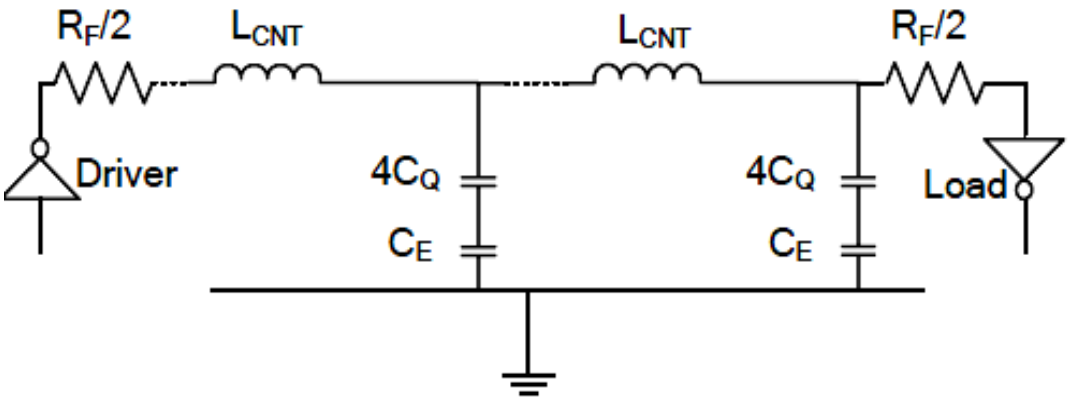

Figure 1.8 Equivalent single conductor circuit diagram for an isolated SWCNT[22]

In Figure 1.8, R_F is the fundamental resistance related to SWCNT, which is decreased to half of total at both the ends, L_{CNT} is the total inductance related to SWCNT which is comprising of magnetic inductance and kinetic inductance. C_E is the electrostatic capacitance between the interconnect and the ground plane. C_Q is the quantum capacitance of the channel, as there are 4 channels in single SWCNT, so it will be multiplied by 4.As the resistance of SWCNT is very high, it cannot be used alone and is always used in bundles. There are three types of bundles: flat CNT array, dense CNT bundle and sparse CNT bundle as shown in Figure 1.9.

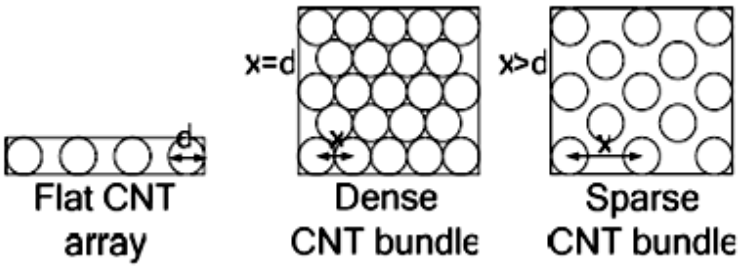

Figure 1.9 Flat CNT array and CNT bundles with varying density of metallic CNTs[16]

1.3.2 Multi-Walled Carbon Nanotubes (MWCNTs)

MWCNTs are made of multiple coaxial cylindrical CNT shells as shown in Figure 1.10 with different diameters of each shell, each contiguous shell is separated by a minimum difference of 0.34nm which is the Vander Waal gap. MWCNT have different chiralities based on their rollingdirection, i.e. shells in MWCNT can be semiconductor or metallic but all together actssimilar to the metal conductor but with lower resistivity and better MFP[23, 24].

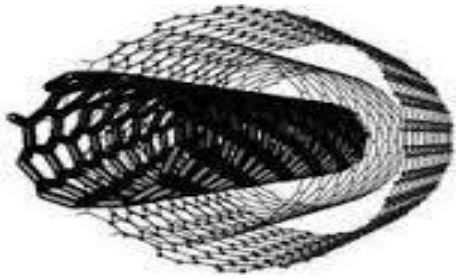

Figure 1.10 Structure of MWCNT[24]

In Figure 1.11,R_{mc} is lumped imperfect contact resistance and R_Q is the lumped quantum resistance per shell, R_S is distributed scattering resistance which is comes into effect when the length of CNT becomes more than mean free path of CNT, $L_k$is kinetic inductance, L_M is magnetic inductance , M is mutual inductance, and $C_Q$is quantum capacitance per shell. Only the outermost shell has electrostatic capacitance $C_E$with the ground. For the entire MWCNT, the shell-to-shell capacitance C_S have only $p-1$ distributed components.

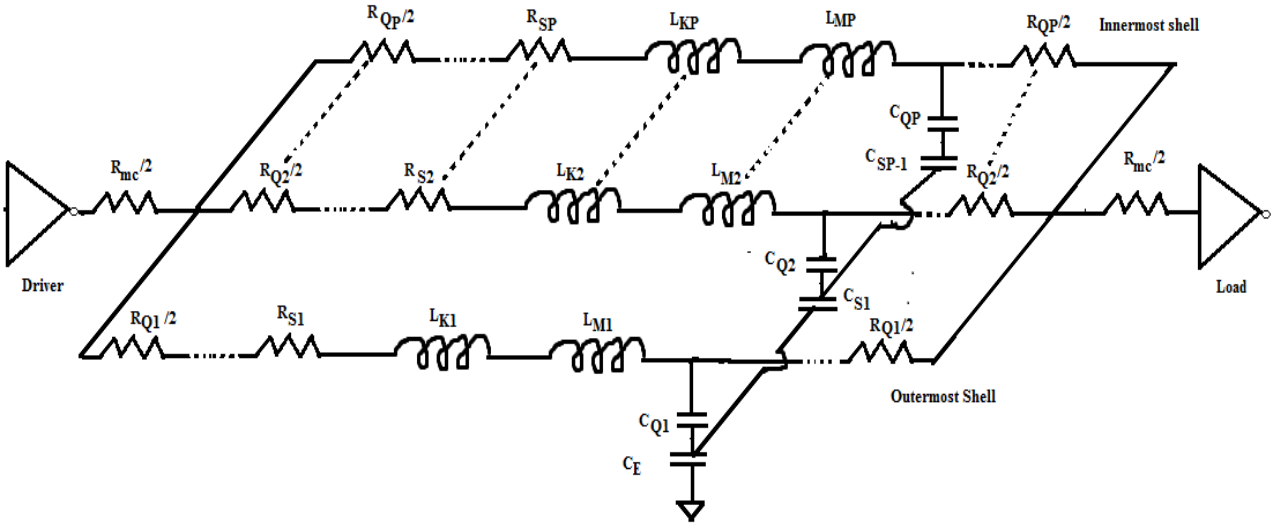

Figure1.11 Equivalent distributed circuit model of an MWCNT with p shells[25]

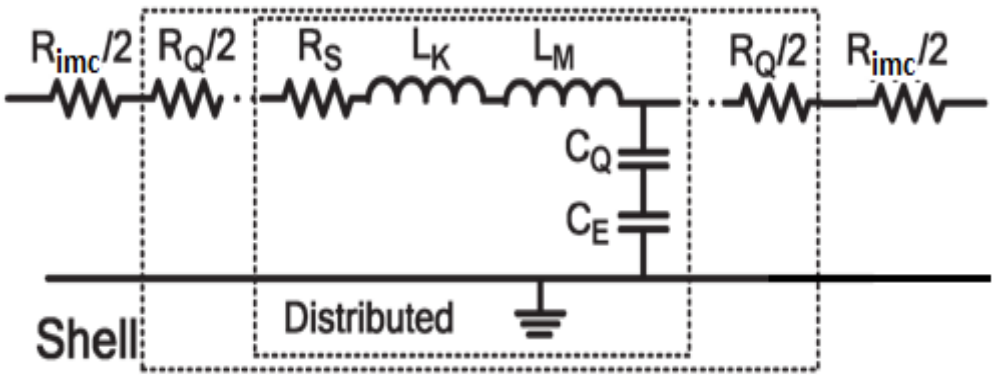

Figure 1.12 Equivalent Single conductor circuit model for CNT[26]

1.3.3 Mixed carbon nanotubes

The recent researches on nanotubes shows that SWCNTs have more advantageous material properties than MWCNTs. To decrease the effect of resistance of single SWCNT, it cannot be used alone so the parallel bundles of SWCNTs are used more.

However, mixed CNT bundle (MCB)is a combination of SWCNT and MWCNT. A realistic nanotube bundle is a mixed bundle of single-walled and multi-walled CNTs and its structure is shown in Figure 1.13.

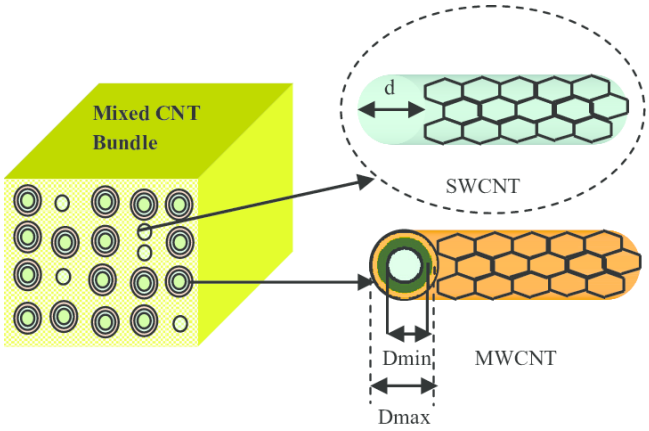

Figure 1.13 A mixed CNT bundle consisting of MWCNTs with shells of various diameters d $(D_{\min} \le d \le D_{\max})$ and SWCNTs of diameter d[20]

Earlier studies have presented some new structures of MWCNT [27] and new hierarchical model has been developed to do the complicated analysis of mixed CNT bundle by developing equivalent single conductor (ESC) models for the structures of bundled SWCNT and MWCNT interconnects.

1.4MODELING OF MIXED CNT AS AN INTERCONNECT

1.4.1 Parameters of Mixed CNT model

Mixed CNT bundle is a combination of two types of tubes one is SWCNT and second is MWCNT. A mixed CNT bundle is composed of SWCNTs having diameter'd' and MWCNTs having different diameter varies from D_{min} to D_{max}. MWCNT consists of two or more SWCNTs of different diameters.

1.4.2 Number of channels, shells

Each shell of CNT has number of conducting channels which gives the path to an electron to move. Due to the spin and sub-lattice degeneracy of electron, the conducting channels are created in CNT. In a single shell the number of conducting channels is given by the equation:

$$N_{shell}(D_i) \approx a.D_i + b,\ D_i > 3nm \tag{1.4}$$

whereD_i denotes the diameter of the shell, a = 0.0612 nm^{-1} and b = 0.425. The ratio of $D_{\min}/D_{\max}$ is between 0.3 to 0.8, but for our convenience we assumed it to be 0.5.

ρdenotes the number of shells in MWCNT [25] and is obtained by the equation:

$$\rho = 1 + Inter\left[\left(\frac{D_{\max} - D_{\max}/2}{2d}\right)\right] \tag{1.5}$$

where 'Inter[.]' denotes that only integer part is considered , 'd' denotes the minimum distance between the two shells i.e. the van der waals gap.

The numbering of shells is done from the outermost shell to the innermost shell as 1,2,3…….i….p (innermost shell).

$$D_i = D_{\max} - 2d(i-1) \qquad ,1 \le i \le p \tag{1.6}$$

The outermost shell's diameter depends on the technology node used. Various other parameters such as number of shells, minimum height to centre of interconnect from ground plane etc. also depends on the technology node used.

1.4.3 R, L, C parameters for Mixed CNT

1.4.3.1 *Resistance*

Resistance arises due to the scattering of electrons while moving through a conducting medium because of the impurities and defects.

The fundamental resistance of SWCNT ($R_{F\,\text{swcnt}}$) and MWCNT ($R_{\text{F mwcnt}}$) is the combined effect of two resistances one is quantum resistance (R_Q) second is scattering resistance (R_S). When the mean free path (λ) of an electron is much greater than that of the length of medium, contact quantum resistance comes into effect which is mainly due to the ballistic transport phenomena. Because of the collision with walls the motion of the electrons are altered and this is not due to scattering. However the scattering resistance (R_S) is mainly induced in the CNT when the length of an interconnect is greater than the electron mean free path [15].

Fundamental Resistance of SWCNT [27] can be obtained by equations:

$$R_{F\,\text{swcnt}} = \frac{h}{4e^2} \qquad l \le \lambda \qquad (k\Omega) \tag{1.7}$$

$$R_{F\,\text{swcnt}} = \frac{h}{4e^2}\frac{l}{\lambda} \qquad l > \lambda \qquad (k\Omega) \tag{1.8}$$

Fundamental Resistance of MWCNT [25] is obtained by equation:

$$R_{F\,\text{mwcnt}} = R_Q + R_S.l = \frac{\text{h}}{2\text{e}^2.N} + \frac{h}{2e^2.N}.\frac{l}{\lambda} \qquad (k\Omega) \qquad (1.9)$$

Where $\frac{h}{4e^2} = 6.45\ (k\Omega)$ and l, N, λ are the lengths, conducting channels in shell and mean free path, respectively. However it is observed practically that the value of resistance of CNT is much higher than the resistance calculated by using the above formula. This is because of the imperfect contact resistance (R_{imc}), as the combined effect of overall resistance is increased. The imperfect contact resistance varies from 0 to hundreds of $k\Omega$ for different growth processes. The contact resistance (R_{imc}) of MWCNT is very small than that of equivalent resistance observed at global length.

1.4.3.2 *Inductance*

CNT consists of two types of inductances one is magnetic inductance i.e. $L_{M\,\text{swcnt}}$,. $\text{L}_{\text{M mwcnt}}$ for SWCNT and MWCNT, respectively. Second is kinetic inductance i.e. $L_{K\,\text{swcnt}}$, $L_{K\,\text{mwcnt}}$ for SWCNT and MWCNT, respectively.Due to the magnetic fields, the magnetic inductance is developed by an isolated current carrying interconnect of diameter 'd' placed at distance 'Y' from the ground plane. While the kinetic inductance is obtained by using the expression for the kinetic energy stored in the conducting channel of the CNT.

The magnetic and kinetic Inductances of SWCNT is given as:

$$L_{\text{M swcnt}} = \frac{\mu}{2\pi}\ln\left(\frac{y}{d}\right) \qquad (pH/\mu m) \qquad (1.10)$$

$$L_{K\,\text{swcnt}} = \frac{h}{2e^2 v_F} \qquad (nH/\mu m) \qquad (1.11)$$

Magnetic and kinetic inductances of MWCNT are given as:

$$L_{M\ \text{mwcnt}} = \frac{\mu}{2\pi}\cosh^{-1}\left(\frac{2y}{D_i}\right) \qquad (pH/\mu m) \qquad (1.12)$$

Here, in MWCNT there are N parallel conducting channels for each shell which increases an effective kinetic inductance $\left(L_K/_{shell}\right)$ for each shell. Therefore the effective kinetic inductance of MWCNT is given as:

$$L_K/_{channel} = \frac{h}{2e^2 v_F}.\frac{1}{2} \qquad (nH/\mu m) \qquad (1.13)$$

$$L_K/shell = \frac{L_K/channel}{N} \quad (1.14)$$

It is observed that the magnetic inductance is more than that of kinetic inductance [25]. Hence we can say that the kinetic inductance has significant affect on the delay analysis of an interconnect when compared to that of magnetic inductance.

1.4.3.3*Capacitance*

The mixed CNT capacitance is mainly due to the combined capacitances effect of SWCNT and MWCNT. The SWCNT capacitance is mainly due to the electrostatic capacitance $(C_{E\,\text{swcnt}})$ and quantum capacitance $(C_{Q\,\text{swcnt}})$ and the MWCNT capacitance is mainly caused due to quantum capacitance $(C_{Q\,\text{mwcnt}})$, coupling (shell-to-shell) capacitance $(C_{S\,\text{mwcnt}})$, electrostatic capacitance $(C_{Q\,\text{swcnt}})$.

The electrostatic capacitance is based on the distance 'y' from ground plane and the diameter 'd' of the tube. Whereas, The quantum capacitance is arises due to the quantum electrostatic energies stored in the nanotube when it carries current.

So, the capacitances of SWCNT is given as

$$C_{E\,\text{swcnt}} \approx \frac{2\pi\varepsilon}{\cosh^{-1}\left(\frac{2y}{d}\right)} \quad \text{, for } y > 2d \quad \left(aF/\mu m\right) \quad (1.15)$$

$$C_{Q\,\text{swcnt}} = \frac{2e^2}{hv_F} \quad \left(aF/\mu m\right) \quad (1.16)$$

The capacitances of MWCNT is calculated using formula:

$$C_{E\,\text{mwcnt}} = \frac{2\pi\varepsilon}{\cosh^{-1}\left(\frac{2y}{D_{max}}\right)} \quad \text{, for } y > 2D_{max} \quad \left(aF/\mu m\right) \quad (1.17)$$

$$C_{Q\,\text{mwcnt}}/channels = 2 \times \frac{2e^2}{hv_F} \quad \left(aF/\mu m\right) \quad (1.18)$$

$$C_{Q\,\text{mwcnt}}/shell = C_{Q\,\text{mwcnt}}/channels \times N \quad (1.19)$$

However, co-axial capacitance formula is used to find out the shell-to-shell capacitance per unit length (C_S) given as:

$$C_{s\,\text{mwcnt}} = \frac{2\pi\varepsilon}{\ln\left(D_{out}/D_{in}\right)} \quad \left(aF/\mu m\right) \quad (1.20)$$

where, D_{in} and D_{out} are the inner and outer shell diameter of adjacent shells.

1.5 ORGANIZATION OF THESIS

The organization of thesis is as follows:-

CHAPTER 1 – This chapter gives an introduction to CNT as an interconnect. Parameters required for the analysis of MWCNT and mixed CNT as an interconnect is also studied in this chapter.

CHAPTER 2 –This chapter presents a brief description of the research that has been reported in the literature in the field of interconnects.

CHAPTER 3 - This chapter describes the methodology used for evaluating the objectives.

CHAPTER 4 – Describes the proposed mixed CNT structure and its analytical modeling.

CHAPTER 5– In this chapter simulation results for various parameters are obtained for MWCNT and mixed CNT.

CHAPTER 6 – Based on results obtained, this chapter describes the conclusion and future scope with respect to the work done.

CHAPTER 2

LITERATURE SURVEY

P. J. Burke et al. [22]proposed a technique in which luttinger liquid collective modes are excited in CNT at gigahertz frequency. The magnetic and kinetic inductance, fundamental resistance, electrostatic and quantum capacitance have been calculated by modelling the nanotubes as a transmission line. Using the concept of interacting electrons in one dimension the model of CNT interconnect is described. The impedance parameters are calculated considering the spin less electrons. The two types of modes of channels namely charge and spin mode in 1-D quantum wire are also discussed.

Ashok Srivastava et al.[28]described the 1-D fluid theory and interconnect models for SWCNT, MWCNT and SWCNT bundle. The applications of 1-D fluid model are examined and the comparison is done between the CNT models and the Cu interconnects of very large scale integration (VLSI) circuits. The S-parameters are studied which shows that there is low reflection losses and higher transmission losses. With the rise in the number of CNTs the overall performance gets increased. Complementary CNT-FET inverter pair is used for the theoretical modelling of the CNT and to study the computer aided simulations. It is observed that the CNTs i.e. SWCNT bundle and MWCNT bundle are better than that of copper interconnect.

Wolfgang Hoenlein et al. [15]described that the unique features of carbon nanotubes (CNT) make them a potential candidate for the applications in the field of microelectronics. The catalyst based chemical vapour deposition (CVD) growth is most suitable technique for the growth of carbon nanotube and also for the carbon nanotube vias which are well suited for the applications in microelectronics. Field effect transistors (FETs) are made using semiconducting single walled carbon nanotube and are known as carbon nanotube field effect transistors (CNTFETs). These carbon nanotube field effect transistors are good applicant for the transistor devices with extraordinary features as compared to the silicon metal oxide semiconductor field effect transistors (MOSFETs). The two field effect transistors i.e. CNTFETs and MOSFETs are compared and their integration issues have been discussed.

NavinSrivastavaet et al. [5]described that with the reduction in feature size of the transistor, the speed of the transistor has increased but the case is not same with interconnects. The problems faced by interconnects when the feature size is reduced below 90 nm technology node have been discussed. The problems faced by copper with the scaling down of

technology are also discussed. The main cause of these problems is increase in resistivity of Cu interconnects because of surface roughness and boundary scattering. The effect of electro migration due to increased current density and their impact on the interconnect delay have also been discussed. It is also discussed that the emerging technologies such as carbon nanotubes, 3-D ICs, optical interconnect can replace copper.

MahmudurRahman et al. [13] described the electrical properties of carbon nanotubes as an interconnect in VLSI circuits have been analyzed. Accordingly, the effectiveness of metallic SWNT interconnect has been studied using Raman spectroscopy for its outstanding ballistic conductivity, low resistance and low capacitance. The performance analysis of SWCNT bundle based on RLC parameters is discussed. Impact of Resistivity on MWCNT, SWCNT bundles with full and one-third metallic portion is studied and by using this result, the paper concludes that metallic interconnects is the future of VLSI technologies

A Naeemiet et al. [29]discussed the model for CNT and also the formulas for the propagation delay of CNT and Cu interconnects have been derived. It is also shown that the latency of single level of nanotubes above a ground plane is larger than that of a copper wire for all practical lengths because its wave propagation speed is very small. The latency of nanotubes bundle is small for longer lengths. Beyond some critical length the resistance of the CNT bundle becomes more than that of Cu wire. It is also shown that the improvement in the performance of CNT is a function of length and with the increase in electron mean free path the overall performance is improved.

Arijit Ray chowdhury et al. [30]described that the semiconducting carbon nanotubes (CNTs) are used in the deep nanometer field due to its extraordinary characteristics. CNTs are the successors to silicon in the field effect transistors (FETs) as CNTs provide channel material for ultrahigh performance. On the other side CNTs are considered as the alternative material for interconnects in deep nanometer field. For CNT as an interconnect, a RLC model has been developed. Improved reliability and high current densities and are the main characteristics of metallic single walled CNTs. The effective RLC model of metallic SWCNTs is presented and the effect of SWCNTs on the performance of digital very large scale integration (VLSI) design has been analysed.

Francesco Ferranti et al. [31]described that the modeling of single-walled carbon nanotubes (SWCNTs) can be carried out using the multi-conductor transmission line (MTL) formulation. It is presented that SWCNTs can be used for the applications of very large scale integration interconnect. In the conventional methods, to decrease the complexity of the

model precision gets reduced as the length of an interconnect increases. It is shown that the proposed model of SWCNT interconnects of large lengths is better than conventional methods. By using the rational model identification technique the complexity of the MTL model is reduced while the accuracy over a large frequency range is maintained.

N.srivastava et al. [32] discussed the carbon nanotube as an interconnect in the field of very large scale integration (VLSI) circuits. The equivalent circuit parameters of CNT interconnect are calculated using model based on the geometry and the performance of CNT bundle. The applicability of CNT as an VLSI interconnect is analysed and shown that it is better than that of copper interconnect for millimetre long global interconnects.

ShouvikMusavvir et al. [33]analysed the propagation delay of SWCNT bundle and comparison is done with copper wire. By considering all the physical and practical phenomenon the equivalent circuit model and equations are derived for SWCNT bundle and copper interconnect. This RLC model is used to analyse the propagation delay of both SWCNT bundle and copper interconnect at different lengths. The propagation delay is mostly affected by the electrostatic capacitance. The comparison between copper and SWCNT bundle shows that for global and intermediate lengths CNT gives better performance and for local lengths copper gives better response.

Manoj Kumar Majumder et al.[34] compared MWCNT and SWCNT bundle interconnects at deep submicron technologies. The propagation delay for both the interconnects at different global lengths have been calculated. It is also analysed that the propagation delay of an interconnect is directly proportional to the length irrespective of the type of CNT interconnect. As the length of an interconnect increases the propagation delay also increases. To show the similar performance the area occupied by the MWCNT is less than that of SWCNT for the different lengths of an interconnect. It is shown that MWCNTs are better interconnect than SWCNTs.

Hong Li et al. [25] analysed the performance of MWCNT-based interconnect and the structural differences between the SWCNT and MWCNT have been discussed. The RLC parameters are calculated to study the impact of parasitic parameters and based on these parameters an ESC model of a MWCNT has been derived. The variation in parameters due to the quantum and intershell effects are also discussed. The delay analysis proved the effectiveness of MWCNT over SWCNT and copper at intermediate and global levels. The impact of imperfect contact resistance and the role of interconnects aspect ratio on its propagation delay are also discussed. It is observed that for a long length interconnect

(mainly global or intermediate levels), the delay caused by MWCNT is much lower than that caused by copper whereas for short local interconnects copper is better than MWCNTs.

Feng Liang et al. [35] described that 50% time delay analysis is performed to find out the optimal number of repeaters. Finite difference time domain (FDTD) method on a derived ESC model for interconnects at both intermediate and global levels is used. CMOS gate as a driver for interconnect line is used. The propagation time delay at different lengths and at different technology nodes (14nm and 22nm) have been shown. The optimum number of repeaters essential for MWCNT and copper at intermediate and global length is analysed. It is observed that the propagation time delay in MWCNT is much less than that of copper interconnect at global and intermediate level. The number of repeaters used by MWCNT interconnect is one third of that used by copper interconnect at similar geometrical dimensions in order to reduce the time delay.

HosseinSheikhassadi et al. [36]presented an efficient and accurate RC model for both MWCNT and MWCNT bundle. The delay analysis is performed based on Elmore delay model. The various parameters of MWCNT are discussed and are transformed for MWCNT bundle based model. The delay based SPICE simulation was focused on interconnects at global lengths with one MWCNT, a bundle with 3 MWCNTs arranged parallel and a bundle of 9 MWCNT arranged in 3 rows and 3 columns. The scattering resistance is inversely proportional to the mean free path (MFP) of the electrons and as it reduces, the overall resistance increases and therefore the propagation delay also increases. The proposed model when compared with equivalent model of MWCNT, the difference between the delays is observed using the two models and is found to be less than 2% for both MWCNT and its bundles.

B.K. kaushik et al. [37]analysed the multi-walled CNT for different number of shells. The equivalent single conductor (ESC) model is also introduced for MWCNT interconnect with different number of shells. For the different number of shells of MWCNT, the propagation delay and power dissipation is compared and it is observed that MWCNT with greater number of shells have higher performance in terms of propagation delay and power dissipation.

Min Tang et al. [17] described an effective way for study and simulating the complex MWCNT interconnect using ESC model. The effectiveness and the accuracy of ESC model were tested by comparing the simulation results obtained by ESC model to that of multi conductor model (MCC). The impact of imperfect resistance along with the tunnelling

conductance of MWCNT was also studied for MCC model. It is also stated that the accuracy of the system is largely dependent on the value of imperfect contact resistance i.e. lower the values better the accuracy level. The number of repeaters used by MWCNT at a particular length is one third of thatused by copper in order to reduce the time delay.

MortezaGholipour et al. [6] explained propagation delay of the multi walled carbon nanotubes (MWCNT). Semi-analytical model for numerical analysis of delay at various technology nodes based on the parameters of ITRS 2005 has been proposed. An effective model of MWCNT has been presented and delay at various lengths and at different technologies has been simulated. The impact of repeaters in deduction of delay has been explained. The simulation concludes that MWCNT is faster than that of copper at intermediate and global level. The results of delay estimation obtained by semi analytical model are very close to the simulation results which proves the efficiency of the proposed model. The proposed model also examines the impact of repeaters on interconnect delay and by estimating the optimal number of repeaters the interconnect delay is minimized. It is also concluded that at a particular length MWCNT requires lesser repeaters than copper especially at global lengths.

Junfa Mao et al. [38] investigates modelling and fast simulation analysis of MWCNT for global interconnects. A effective realization of MCC model into ESC model is also provided. Bothintershelltunneling conductance and imperfect contact resistance are studied in the paper. On the basis of ESC model a highly efficient approach based on delay extraction algorithm has
been proposed for fast simulations of MWCNT interconnect. The proposed ESC model provides an accurate 50% time delay estimation, its accuracy and efficiency has been demonstrated by numerical analysis. On analyzing ESC and MCC models for different locations of imperfect contact resistance, it was observed that the electrical properties of MWCNT interconnect are affected, this effect can be by introduction of intershell tunnelling conductance in model analysis.

Wei Wang et al. [9]analysed that the superior conductivity and advanced current carrying capabilities of carbon nanotube (CNT) bundle make them suitable in the field of deep nanometer interconnect applications. A CNT bundle consisting both single-walled and multi-walled CNTs is known as mixed carbon nanotube bundle. A diameter dependent model is introduced to observe the conductance of both single walled and multi walled CNTs. This model is also used to analyse the mixed CNT bundles and it is proved that the mixed CNT

bundles can give two to five times better conductance performance over Cu by selecting the appropriate parameters i.e. width, density and metallic ratio of tube.

TafseerAlam et al. [39]presented capacitive analysis for the mixed CNT bundles as interconnects.The analysis has been done for various process parameters i.e. average diameter, ratio of inner to outer diameter and CNT bundle probability. When CNT bundle is used as an interconnect, capacitance of bundle gets decreased. With the downscaling of technology, the reduction in capacitance of CNT bundle increases and capacitance of CNT bundle remains less than Cu interconnect. It is shown that for intermediate and global interconnects mixed CNT bundle is alternative to copper interconnect at deep submicron technology nodes (nanometer level).

B. K. Kaushik et al. [40]presented an RLC model for mixed CNT bundle and its performance has been analysed on the basis of crosstalk delay and power dissipation. There are two different structures for mixed CNT bundle that contains SWCNT, DWCNT and MWCNT. Structure1 consists of SWCNT and DWCNT whereas structure 2 consists of SWCNT and MWCNT. The comparison between them is done on the basis of their power dissipation and crosstalk delay. The propagation delay under the effect of crosstalk and power dissipation have been calculated for different bundled structures of mixed CNT, SWCNT and DWCNT at global interconnect length. It has been observed that the structure 2 has better performance than that of structure 1 due to the decrease in the parasitic resistance and inductance in structure 2 as the reduction is more by introducing MWCNT as compared to SWCNT and DWCNT.

P.S. Mallick et al. [27]described that with the downscaling of technology the design complexity of transistors is increasing and for this the carbon nanotube is better alternative to Cu interconnects because of its excellent thermal and electrical properties. The single-walled CNT, double-walled CNT and mixed CNT bundles have been discussed and analysed. The two different configurations of mixed CNT i.e. one with single-walled CNT and other with double-walled CNT have been modelled. It is observed that the Double-walled CNT bundle has better delay performance as compared to single-walled CNT. The mixed CNT bundles have better delay performance than both single-walled and double-walled CNT.

Nisarg D. Pandya et al. [41] proposed a model of mixed CNT bundle interconnect. The two different structures of mixed CNT bundle are proposed in which both MWCNT bundle and SWCNT bundle are modelled to give ESC model of mixed CNT interconnect. In the first structure of mixed CNT, MWCNTs are present at boundary and SWCNTs are located at

centre portion of bundle and in the second structure of mixed CNT, SWCNTs are at boundary and MWCNTs are located at the centre portion of bundle. When both the structure are compared, it is observed that first structure has less crosstalk delay, propagation delay and power dissipation than second structure.

P. Uma Sathyakam et al. [42]presented the modelling hierarchy for mixed CNT bundle (MCB) interconnect. The ESC model of MCB interconnect is developed by modelling SWCNTs and MWCNTs. The two ESC model of MCB are combined to give multi-conductor transmission line model (MTL). Using the transient analysis, the delay of interconnect in both the ESC models is calculated and it is observed that propagation delay of mixed CNT bundle is less than SWCNT bundle and MWCNT bundle.

M.K Majumder et al. [43]described the importance of carbon nanotubes in the field of interconnects. There are various reasons due to which the mixed CNT bundles are frequently preferred over single-walled CNTs and multi-walled CNTs. However, the growth of both the compact packed bundles i.e. SWCNTs having uniform diameter and MWCNTs having identical number of shells is challenging to control during its fabrication process. Hence, a realistic CNT bundle known as mixed CNT bundle (MCB) which consists of both SWCNTs and MWCNTs is discussed. On the basis of the distribution probability of carbon nanotubes having different diameters, a multi-conductor transmission line (MTL) and a simplified equivalent single conductor (ESC) model have been developed. The propagation delay, crosstalk and power dissipation for MCBs having different tube densities are analysed by using the equivalent single conductor model. It is observed that the MCB with higher tube density shows better results for the overall crosstalk and delay with a very small increase in power

CHAPTER 3

PROPOSED METHODOLOGY

The mathematical analysis is done using MATLAB in order to obtain various impedance parameters values at different technology nodes for different lengths and different diameters of Cu, SWCNT bundle, MWCNT bundle and mixed CNT bundle.

At a particular technology node, the different values of impedance parameters (resistance, inductance and capacitance) are obtained at different lengths and different diameters and then these values of impedance parameters are compared with each other. The results obtained from MATLAB are provided to lumped and distributed models of interconnects. The simulations of these lumped and distributed models are carried out in Tanner EDA tool. These simulations are done at different driver sizes of transistors so as to obtain the optimum driver size which provides the minimum propagation delay of an interconnect.

3.1 TECHNOLOGY AND SIMULATION PARAMETERS

Table 3.1 ITRS 2013 based simulation parameters for global interconnects [1]

Technology node	**32**	**22**	**16**
Width W(nm)	**40**	**28**	**18**
Thickness H(nm)	**120**	**84**	**54**
Aspect Ratio (A/R)	**3**	**3**	**3**
Oxide Thickness Y(nm)	**93.6**	**65.5**	**40**
V_{dd} **(volts)**	**0.9**	**0.8**	**0.7**
Dielectric Constant ($\in_r$)	**2.77**	**2.59**	**2.31**
$D_{ratio}(D_{min}/D_{max})$	**0.5**	**0.5**	**0.5**
ρ_{cu} $(\mu\Omega.cm)$	**3.66**	**4.2**	**5.69**

The interconnect parameters based on the technology node are considered according to ITRS 2013 as shown in Table 3.1 and based on these parameters equivalent model of proposed mixed CNT is derived. It is seen from Table 3.1 that the aspect ratio of interconnect at global level is considered to be 3. The proposed global level interconnect consists of a mixed CNT bundle which has 3 MWCNTs connected vertically in parallel to each other and SWCNTs having diameter of 1nm are inserted in between the gaps surrounding (side-walls and corners) the 3 MWCNTs. An ESC model of proposed mixed CNT interconnect is derived using mathematical analysis and is simulated using SPICE simulator in order to study propagation delay and power delay product (PDP).

3.2 ANALYSIS OF AN INTERCONNECT DELAY

One of the most important aspects of performance analysis is delay analysis. The delay of an interconnect due to the impedance parameters (resistance, inductance and capacitance) of an interconnect is determined as:

Delay (τ) = $\frac{\tau_{PHL} + \tau_{PLH}}{2}$ (3.1)

Where$\tau_{PHL}$is given as fall time while is τ_{PLH}given as rise time. For the analysis the length (L) of interconnect is considered to be at global level and is driven by a CMOS inverter with a digital signal of 50% duty cycle. CMOS inverters are based on PTM parameters [3].Capacitive load (C_L) is considered at output whose value may range from 1fF to 10Ff [2].

3.3 INSERTION OF REPEATERS (OR BUFFERS) IN INTERCONNECT

It is seen that almost all the parameters (RLC) and propagation delay are dependent on length ofan interconnect.

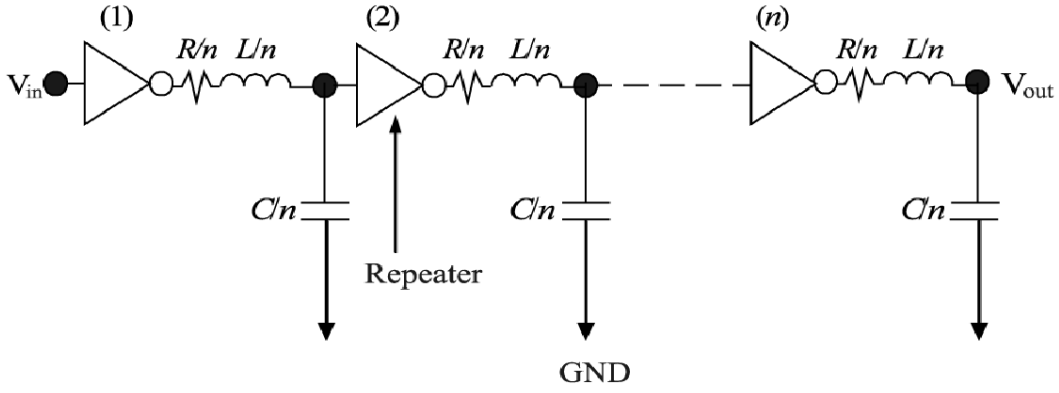

Figure 3.1 Distributed model of ESC circuit with repeaters inserted in between [44].

Thus the increase in length ofan interconnect increases the value of RLC parameters which further increase the propagation delay of an interconnect. For the global length (L >500μm) the R, L, C parameters and propagation delay may be verylarge and may produce an error i.e. propagation delay may be larger than ON time andunwanted output may be observed for a fixed frequency of signal. Therefore to avoid thiserror, it is needed to minimize the length of an interconnect.In order to minimize the length of a distributed network ‘n’number of buffers is inserted as shown in Figure 3.1. Inserting ‘n’ buffers will divide the lumped ESC model in ‘n’ segments thus reducing the length by ‘n’ times. This also reduces RLC by factor of ‘n’ foreach segment. This reduces the overall delay of an interconnect but the power consumed increases,thus a trade off is required between them. The number of repeaters can be varied in order to obtain minimum delay [4, 5].

CHAPTER 4
PROPOSED MIXED CNT INTERCONNECTS

4.1 INTRODUCTION

The analysis of mixed CNT bundle as an interconnect for very large scale integration (VLSI) circuits is done in this chapter. The mixed CNT bundle contains both MWCNTs and SWCNTs. A multi conductor circuit (MCC) model of the proposed mixed CNT is developed based on the interconnect geometry. From the MCC model, the equivalent circuit parameters for the mixed CNT bundle are calculated and equivalent single conductor (ESC) model is developed. Using the ESC model, the performance of the mixed CNT bundle interconnect at intermediate, global and local level at different technology nodes is compared with MWCNT bundle. It is shown that the performance of mixed CNT bundle is better than MWCNT bundle at intermediate, global and local levels.

The equivalent resistance, inductance and capacitance for the analytical model are calculated using equations of mixed CNT bundle. Depending on values of resistance, capacitance, and inductance analytical model is developed. The propagation delay and power delay product (PDP) is calculated at intermediate, global and local levels for mixed CNT bundle using Tanner EDA tool and simulation is done using SPICE files. The resulting values of propagation delay and PDP of mixed CNT bundle compared with MWCNT bundle.

4.2 PHYSICAL STRUCTURE OF PROPOSED MIXED CNT

The simple structure of MWCNT as an interconnect based on the ITRS parameters is shown in Figure 4.1 which is modified to a new structure by inserting the SWCNTs at the corners and side-walls of previous structure. As interconnect is of Rectangular shape and MWCNTs are of spherical shape so the area of rectangular shaped interconnect is not covered fully. Hence we inserted the SWCNTs of 1nm in between the gaps of rectangular shaped interconnect.

The physical structure of proposed mixed CNT bundle is shown in Figure 4.2. The mixed CNT bundle contains both SWCNT and MWCNT. The diameters of SWCNT and MWCNT inside the bundle follow the normal distributions depending upon process control and conditions during CNT synthesis [13]. From Table 3.1, it is seen that aspect ratio of interconnect is considered to be 3. Therefore, in the proposed mixed CNT bundle, 3 MWCNTs are connected vertically in parallel to each other and SWCNTs are inserted surrounding (side-walls and corners) the MWCNTs. In Figure 4.2, W and H are the width and

height of mixed CNT interconnects, respectively. It is placed at a ‘y’ distance from the ground. The spacing between two adjacent mixed CNT interconnect is S.

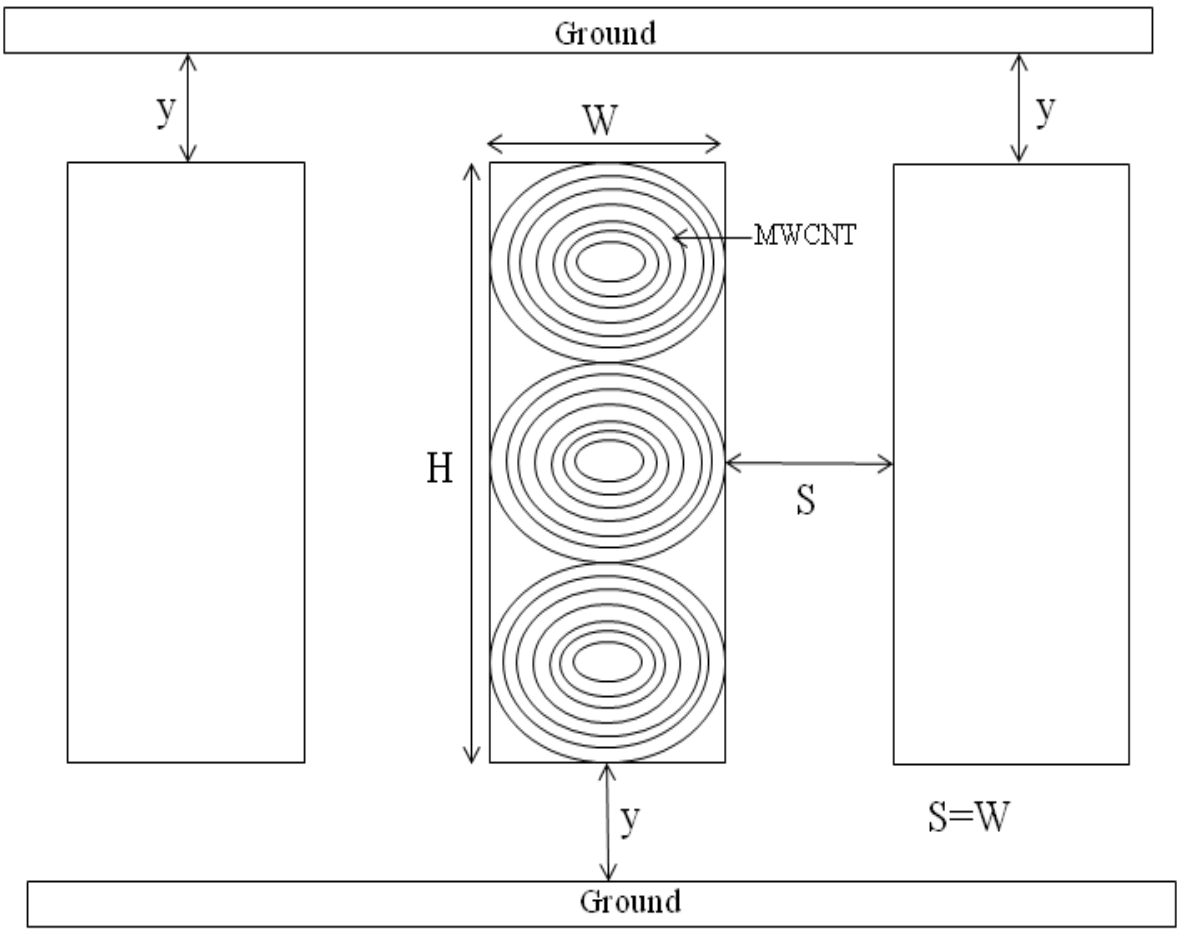

Figure 4.1 Structure of MWCNT interconnect.

Due to the insertion of SWCNTs surrounding (side-walls and corners) the MWCNT, the conductivity is increased because the SWCNTs decreases the overall effect of resistance and inductance of MWCNTs connected vertically in parallel to each other. The SWCNTs are inserted parallel to MWCNTs and it is known that in parallel combination the overall resistance effect is decreased but due to the parallely inserted SWCNTs the capacitive effect is increased in mixed CNT bundle which has opposite effects on the performance of an interconnect. But the rate of decrease of both resistance and inductance is more than the rate of increase of capacitance. Therefore, the effect of increased capacitance is compensated by the decrease in resistance of an interconnect.

The change in overall inductance value in the proposed model is very small so it will not contribute much in the overall performance of an interconnect. The performance of an interconnect is mainly effected by the resistance and the capacitance.

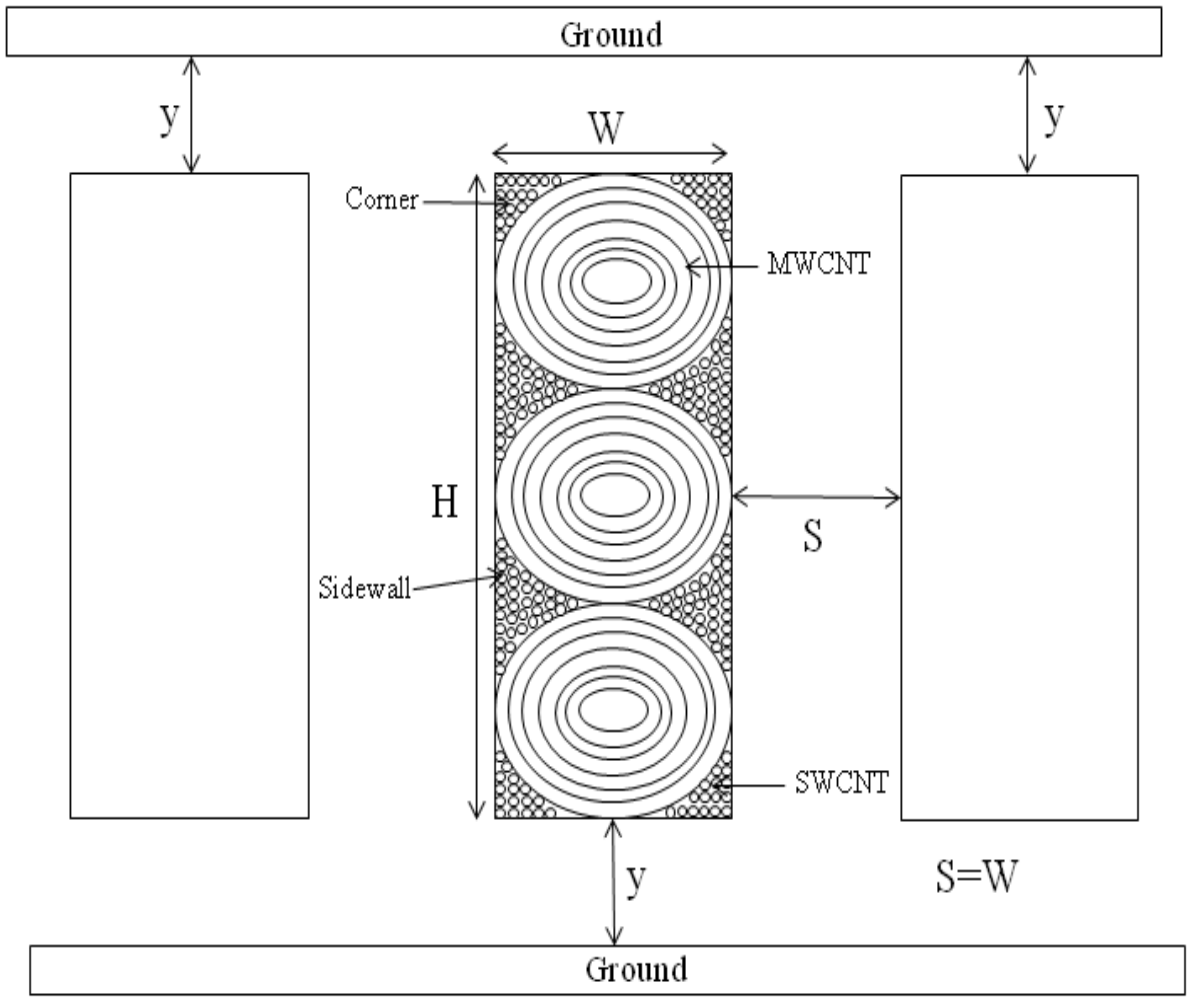

Figure 4.2 Structure of mixed CNT interconnect in advanced IC design.

Here, the structure is analyzed at different technology nodes i.e. 32nm, 22nm, 16nm for different lengths. For each technology node the diameter of the MWCNT is different so the numbers of SWCNTs inserted around the MWCNTs are different. The number of SWCNTs to be inserted is calculated by using the equation:

$$(X'-X_0)^2 + (\mathrm{Y'}-\mathrm{Y}_0)^2 = R^2 \qquad (4.1)$$

where X_0, Y_0 are the center co-ordinates of the MWCNT and R is the radius of the MWCNT. SWCNTs inserted are of 1nm diameter. The value of X' is calculated for each value of $\mathrm{Y'}$ = 1nm, 2nm, …… Y_0 nm.

The value of X' gives the number of SWCNTs that can be placed parallely to each other for each value of $\mathrm{Y'}$. So, the total number of SWCNTs to be inserted around the MWCNTs is calculated.

Table 4.1 shows the effective number of SWCNTs with the variation in value of $\mathrm{Y'}$ at 32nm technology node.

Table 4.1 Effective Number of SWCNTs at 32nm technology node

Y' (nm)	X' (number of SWCNTs)
1	13
2	11
3	9
4	8
5	6
6	5
7	4
8	4
9	3
10	2
11	2

Table 4.2 shows the effective number of SWCNTs with the variation in value of Y' at 22nm technology node.

Table 4.2 Effective Number of SWCNTs at 22nm technology node

Y' (nm)	X' (number of SWCNTs)
1	8
2	6
3	5
4	4
5	3
6	2
7	1
8	1

Table 4.3 shows the effective number of SWCNTs with the variation in value of Y' at 16nm technology node.

Table 4.3 Effective Number of SWCNTs at 16nm technology node

Y' (nm)	X' (number of SWCNTs)
1	4
2	3
3	2
4	1

4.3 MULTI-CONDUCTOR CIRCUIT (MCC) MODEL OF PROPOSED MIXED CNT STRUCTURE

A multi-conductor circuit (MCC) model is developed to calculate the equivalent circuit parameters for a mixed CNT bundle. This model is used to compare the performance of proposed mixed CNT with MWCNT bundle at local, intermediate and global level.The MCC model of mixed CNT is a combination of MCC model of MWCNT and SWCNT. So, using the hierarchical modeling, MCC model of mixed CNT is developed as shown in Figure 4.3. In MCC model of mixed CNT it is shown that the resistance of SWCNT and MWCNT are connected in parallel with each other which decreases the overall propagation delay and the connected in parallel with each other which decreases the overall propagation delay and the power delay product (PDP) of mixed CNT.

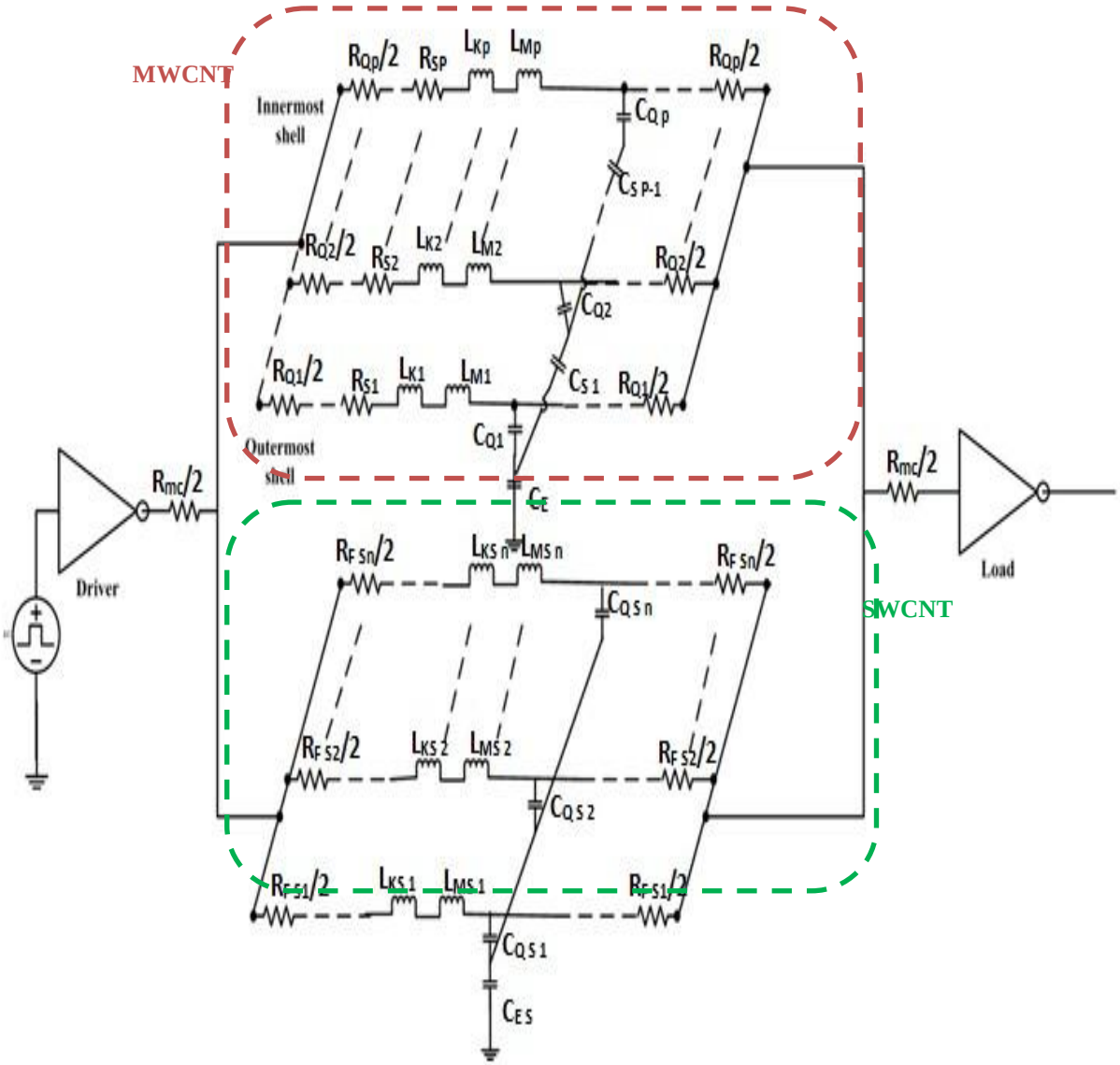

Figure 4.3 MCC model of proposed mixed CNT

4.4 REALIZATION OF ESC MODEL FROM MCC MODEL OF PROPOSED MIXED CNT STRUCTURE

By combining the equivalent single conductor (ESC) model of SWCNT and MWCNT bundle, ESC model of mixed CNT has been obtained. The equivalent RLC parameters of ESC model are used to analyse the performance of mixed CNT.

As seen in upper part of Figure 4.3, *p* represents the different shells of MWCNT of proposed mixed CNT each connected in parallelto each other. In order to obtain equivalent Resistance, Capacitance and Inductance so as to evaluate ESC model we need to drive an expression in order to obtain thesevalues. The ESC model of MWCNT bundle is shown in Figure 1.12.The realization is based on the assumption that all the shells are parallel and separated by afixed distance Vander Waal distance of 0.34nm[1, 2].The resulting equivalent Scattering Resistance (R_S) and Quantum Contact Resistance (R_Q) isformulated as :

$$R^{-1} = \sum_{i=1}^{p} \left(R_{Q\,\mathrm{i}} + R_{s\,\mathrm{i}}\right)^{-1} \qquad \text{for(i} = 1, 2, \ldots\ldots\text{.p)} \tag{4.2}$$

Similarly the equivalent Magnetic Inductance (L_M) and Kinetic Inductance (L_K) is formulated
as :

$$L^{-1} = \sum_{i=1}^{p} \left(L_{K\,\mathrm{i}} + L_{M\,\mathrm{i}}\right)^{-1} \qquad \text{,for(i} = 1, 2, \ldots\ldots\ldots\text{.p)} \tag{4.3}$$

The derivation of equivalent Capacitance is slightly difficult and has to be done in parts. The obtained simplified circuit for evaluating Capacitance is shown in Figure 4.4.

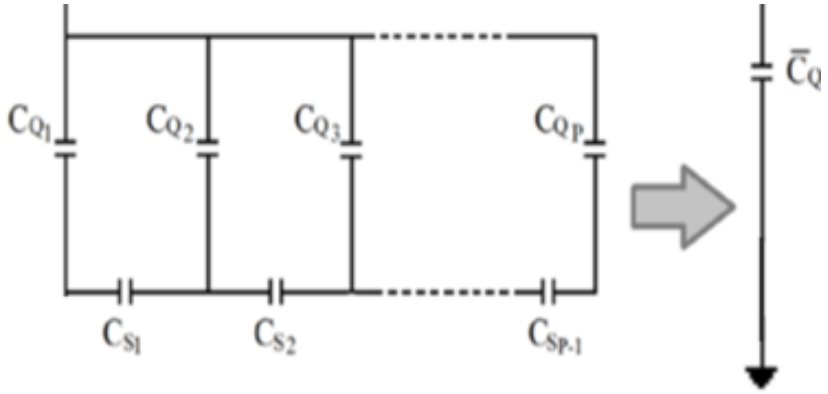

Figure 4.4 Realization of equivalent capacitance[45]

Let $\overline{C_Q}$ be the equivalent capacitance, C_{Qj} is the Quantum Capacitance and C_S is the scattering Capacitance

$$\overline{C_Q} = C_1, \tag{4.4}$$

Where C_1 is calculated in a recursive way:

$$C_p = C_{Qp} \tag{4.5}$$

$$C_{j-1} = (C_j^{-1} + C_{S(j-1)}^{-1})^{-1} + C_{Q(j-1)} \quad ,\text{for}(i = p,.....3, 2) \tag{4.6}$$

The total capacitance in ESC model is taken as:

$$C = (C_1^{-1} + C_E^{-1})^{-1} \tag{4.7}$$

The equivalent values of resistance, inductance and capacitance obtained are used to put in the ESC model of proposed mixed CNT.Similarly, the equivalent resistance, inductance and capacitance parameters of SWCNTs present in the proposed structure of mixed CNT are used to put in the ESC model of proposed mixed CNT.

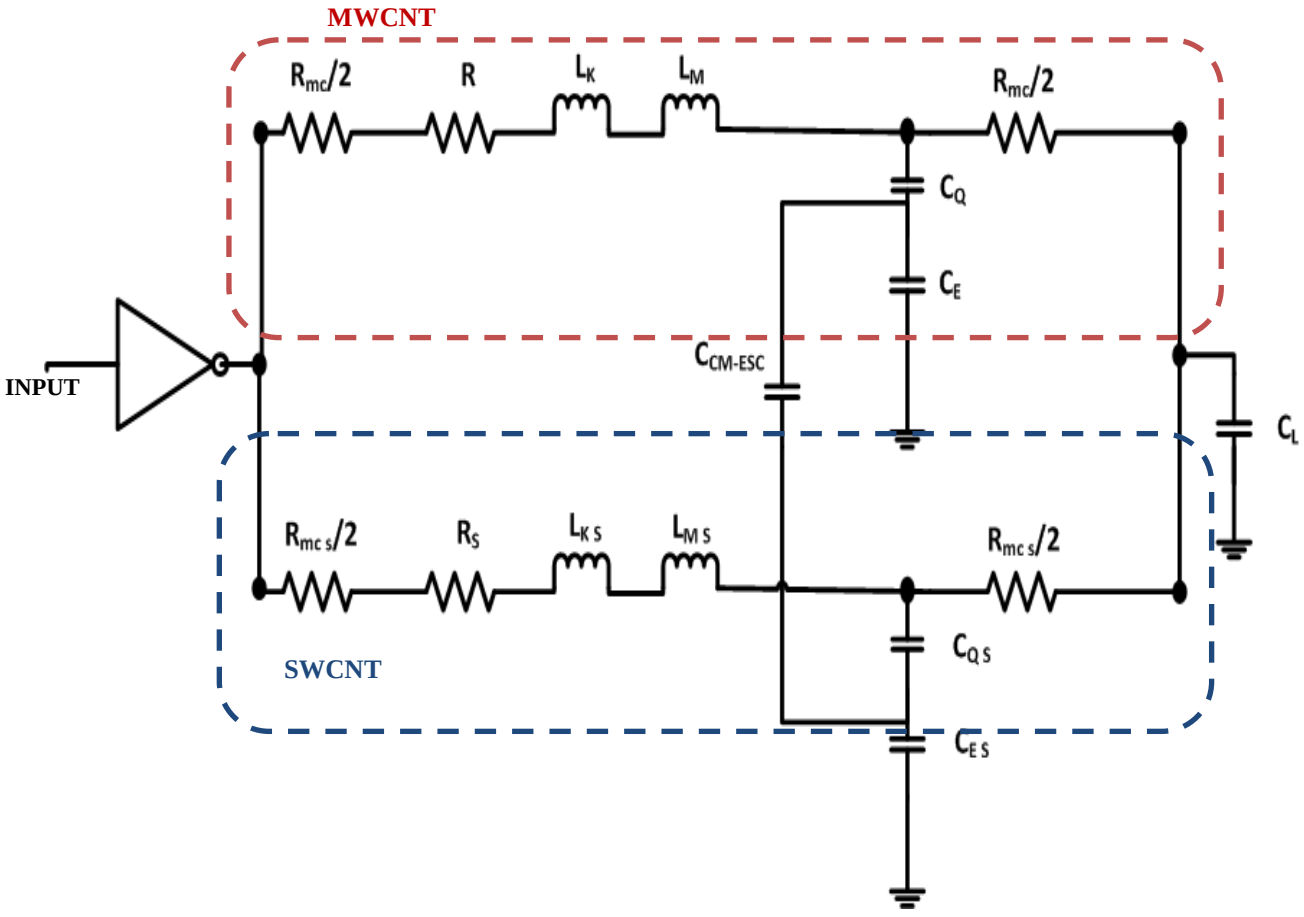

Figure 4.5 Equivalent single conductor circuit model for proposed mixed CNT.

As shown in the lower portion of above Figure 4.3, 'n' represents the number of SWCNTs each connected in parallel to each other in the proposed mixed CNT structure. Here, in this case the realization is based on the assumption that all the SWCNTS are of similar diameter of 1nm in order to obtained the equivalent RLC so as to evaluate ESC model we need to

drive an expression in order to obtain these values. The resulting equivalent fundamental resistance is formulated as:

$$R_S = \frac{R_F}{n} \tag{4.8}$$

Similarly, the equivalent Magnetic Inductance (L_{MS}) and Kinetic Inductance (L_{KS}) is formulated as:

$$L_S = \frac{\mathrm{L_{MS}} + L_{KS}}{n} \tag{4.9}$$

Similarly, the overall capacitance is taken as:

$$\overline{C_{QS}} = n \times C_{Qs} \tag{4.10}$$

$$C_{swcnt} = \left(C_{QSwcnt}{}^{-1} + C_{E\,s}{}^{-1}\right)^{-1} \tag{4.11}$$

Now, the ESC circuit model for proposed mixed CNT bundle (MCB) is obtained by the combination of ESC model of SWCNT and MWCNT bundle as shown in the Figure 4.5.

In the proposed ESC model the capacitance known as coupling capacitance C_{CM-ESC} is experienced between the SWCNT and MWCNT interconnects:

$$C_{CM-ESC} = \frac{\pi \varepsilon l}{\cosh^{-1}(s_p / D_a)} \tag{4.12}$$

where s_p and $\mathrm{D_a}$ are the spacing between the two bundled structures and average diameter of SWCNT and MWCNT bundle, respectively.

In this chapter new mixed CNT structure is proposed by inserting SWCNTs at the corners and side-walls of the MWCNT. Due to the insertion of SWCNTs, the conductivity of mixed CNT is increased because the SWCNTs increases the density of shells and therefore, decreases the overall effect of resistance and inductance of MWCNTs connected vertically in parallel to each other. The effective number of SWCNTs to be inserted for different technology nodes i.e. 32nm, 22nm and 16nm are calculated. Using the hierarchical modelling, MCC model of mixed CNT is developed and equivalent ESC model is obtained.

CHAPTER 5
RESULTS AND DISCUSSIONS

In order to prove that at local, intermediate and global level performance of proposed mixed CNT bundle is better than the MWCNT at different technology nodes and the obtained results for proposed mixed CNT bundle are needed to be compared with the results for MWCNT as an interconnect at respective technology nodes.

5.1 ANALYZING MWCNT AS AN INTERCONNECT

In this section, the impact of variation of other parameters such as driver size, load, contactresistance, on the delay is also analyzed for the better understanding of MWCNT asinterconnect. Further observation of the impact of repeaters on reduction of delay is alsodone. The RLC parameters for MWCNT are obtained using equation 1.4- 1.19, and a MCCmodel is realized. Based on the MCC model, an ESC model is derived using by using equations 4.2-4.7.

The Tables 5.1 given below gives the values of derived RLC parameters of an ESC model.Simulations are performed on this derived ESC model.

In this case a ESC model for MWCNT at global length of 1000μm is considered, fewparameters are assumed to be as:

$Length = 1000\mu$m;

$C_L = 5\%$ of equivalent capacitance;

$MFP(\lambda) = 1000.D_i$;

$v_F = 8 \times 10^5$;

$D_{\min} to\ D_{\max}$ ratio $= 0.5$;

The other parameters are based on ITRS 2013 (Table 3.1). And the simulations are carried to evaluate delay based on equation 3.1.

5.1.1 Optimum Driver size

For the SPICE simulation of ESC model a CMOS inverter as a driver is considered using PTM model file [46]. As it is known that in a CMOS inverter the size of a PMOS is 3 times that of NMOS and is fixed, however the W/L ratio (driver size) of the CMOS can be varied in order to achieve a size with minimum propagation delay. The simulation results to studythe impact of driver size can be seen in Table 5.2 and in Figure 5.1

The RLC value at 1000μm is taken as:

Table 5.1 RLC values for ESC model simulation at 32nm, 22nm and16nm technology nodes for global length of 1000μm.

Technology node	R (Ω)	L (nH)	C (fF)
32nm	174.807	3.263	423.576
22nm	464.625	6.142	295.056
16nm	148.252	12.63678	190.027

Table 5.2 Delay analysis for different driver size at 32nm, 22nm and16nm technology nodes for global length of 1000μm.

Driver size $(W/L$ of NMOS$)$	Delay (ns)		
	32nm	22nm	16nm
10	12.246	7.276	7.655
20	6.7801	4.307	5.174
30	4.9760	3.325	4.366
40	4.1035	2.818	3.981
50	3.5698	2.546	3.746
60	3.2274	2.345	3.596
70	2.9618	2.204	3.483
80	2.7812	2.096	3.401
90	2.6293	2.014	3.341

It is interesting to observe that propagation delay changes while changing driver size. As thedriver size increases propagation delay decreases initially till it reaches to a certain value andafter that it tends to increase. The driver size at which the propagation delay reaches itsminimum value is called as optimum driver size, at this point the impedance of interconnectline matches with the driver thus experiencing minimum propagation delay.

However thesimulation results also shows that as the technology node is becoming smaller the optimum driver size required also decreases as seen in Figure 5.1

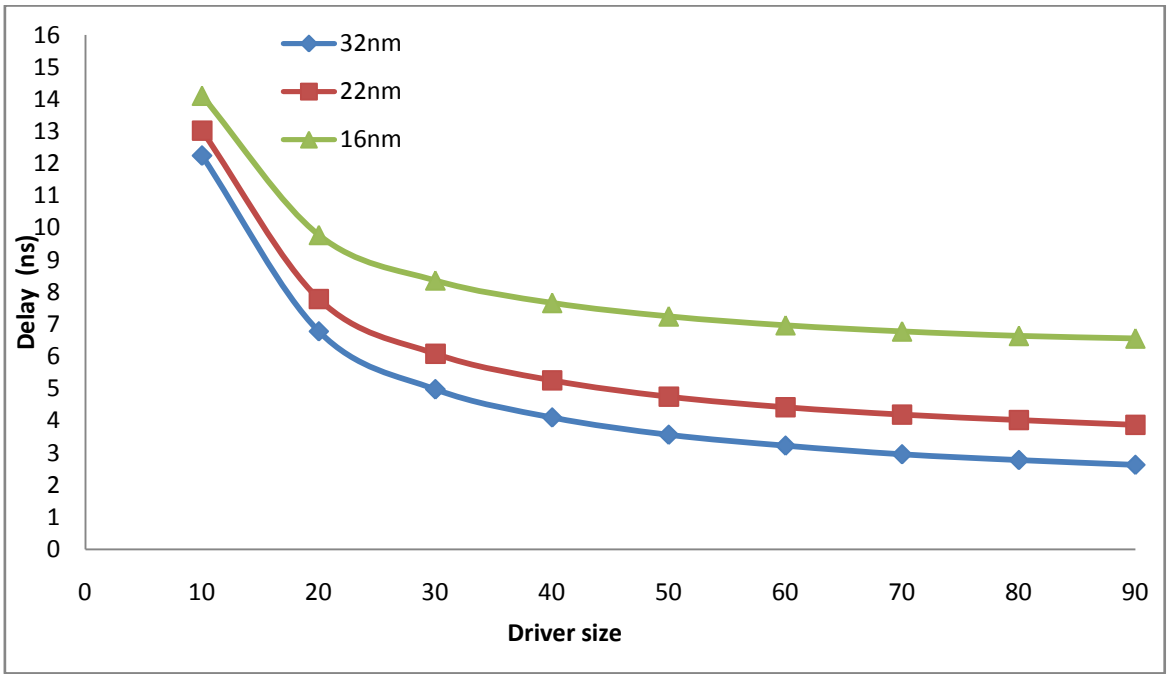

Figure 5.1 Impact of CMOS Driver size on MWCNT interconnects delay at global length of 1000μm for 32nm, 22nm and 16nm technology nodes.

5.1.2 Frequency determination

The simulation results carried out for different operating frequencies but at fixed length andtechnology node shows that propagation delay of the interconnect is immune to varyingoperating frequencies i.e. propagation delay is independent to the changes in operatingfrequencies and therefore remains unchanged for a fixed length and technology node.However, the maximum operating frequency of interconnect do depends on its propagationdelay and load capacitor (C_L) which depicts the input capacitance of the fan-out gates actingas a load to the interconnect line. The reason for the dependency of maximum operatingfrequency on propagation delay is that, the output of interconnect is measured across a loadcapacitor (C_L), the time required by interconnects to charge or to discharge the capacitor (C_L)denotes its propagation delay if the operating frequency is set above its maximum value (obtained by equation 5.1) i.e. if the half time period is set below the propagation delay, theload capacitor (C_L) will not be able to charge upto 90% or discharge upto 10% of the inputsignal, therefore a corrupted signal is obtained at the output across the load capacitor (C_L). Now, let the operating frequency $f = \frac{1}{\mathrm{T}}$, where T is the time period of

the signal with 50% duty cycle. Then the relation between propagation delay and maximum operating frequency is given by:

$$\frac{T_{\min}}{2} > Delay \Leftrightarrow \frac{1}{Delay} > 2 f_{\max} \quad (5.1)$$

For irregular duty cycle, the time period should be set such that Delayshould always besmaller than T_{ON} or T_{OFF} (whichever is small).For the above cases the value of load capacitance (C_L) was kept constant at 1fF.But the value of load capacitance (C_L) ranges from 1fF to 10fF and as its value increases thepropagation delay also increases as observed in Table 5.3.

Table 5.3 Impact on delay with variation of Load Capacitance (C_L) at 32nm, 22nm And 16nm technology node at 1000μm length.

C_L (fF)	Delay (ps)		
	32nm	22nm	16nm
1	2298.9	2998.2	4369.5
4	2300.7	3001.8	4378.3
7	2302.4	3005.4	4386.9
10	2304.1	3008.9	4401.5

5.1.3 Repeaters (or Buffers) insertion

Repeaters are nothing but the buffers or inverters used in order to reduce the propagationdelay. The role of repeaters is to reduce the length of interconnect into 'N' segments, whereN represent number of repeaters and as it is already shown that propagation delay isdependent on Length of interconnect and therefore insertion of repeaters results in reductionof propagation delay. The repeater insertion causes reduction in the distributed parameters ofinterconnects by the factor of N as seen in Figure 5.2for the simulation of ESC model the repeaters used are CMOS inverters and length ofinterconnect is considered to be 1000μm. The simulation results in Figure 5.2. For the value 'N'at which the propagation delay reaches to its minimum value is considered to be optimumnumber of repeaters to be inserted.

Table 5.4 Delay variations due to insertion of repeaters at 32nm, 22nm and16nm technology nodes at 1000μm length.

No. of Repeaters	Delay (ns)		
	32nm	22nm	16nm
5	3.198	4.740	8.154
7	2.702	3.798	6.126
9	2.426	3.281	5.027
11	2.275	2.977	4.365
13	2.214	2.838	4.149

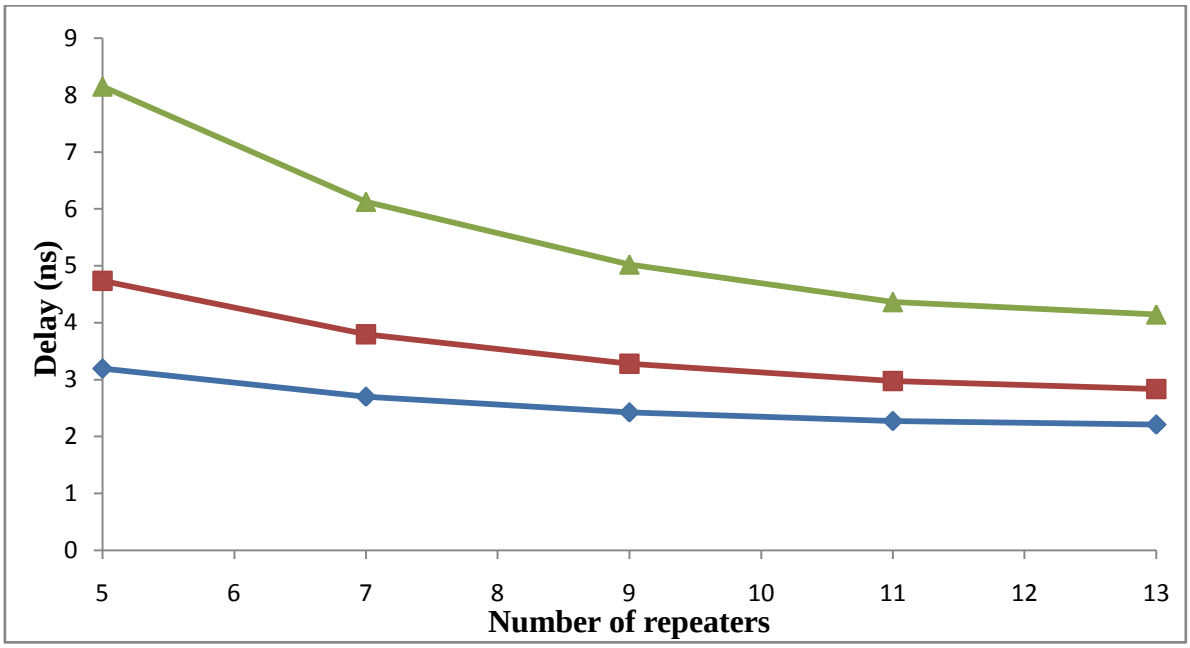

Figure 5.2 Impact of Repeaters on propagation delay of MWCNT interconnect at global length of 1000μm for 32nm, 22nm and16nm technology nodes.

From Table 5.4 and Figure 5.2 it is seen that as the number of repeaters inserted in an interconnect lineincreases the delay initially tends to decrease but after a certain value it again increases. This trend is because delay has a direct relation between the interconnect parameters and length,initially delay is dominated by length and with insertion of repeaters the overall length isdivided into small length sections. For certain number of repeaters the delay of interconnectis minimum, this gives the value of optimum number of repeaters to be

inserted. As thenumber of repeaters to be inserted is increased further, the domination of length isovershadowed by domination of the interconnect parameters on delay analysis and now theincrease in delay is due to the interconnect parameters.

5.1.4 Impact of length and technology scaling on the propagation delay and power delay product (PDP) of MWCNT

The RLC parameters of interconnect are intrinsic in nature and therefore varies with length. This variation of RLC with respect to length is directly proportional in nature. As RLC parameters increases with increase in length, it altogether results in increase of propagation delay. However the impact of scaling on delay is slightly different. As it can be seen in that as technology node is scaled down, there is a increase in resultant propagation delay and power delay product. It is important to note that the rate of increase of propagation delay and power delay product with respect to length varies differently for different technology node.

32nm technology node

Table 5.5 Variations in parameters with respect to Length for 32nm technology node.

Length (μm)	R (Ω)	L (nH)	C (fF)	Delay (ns)	PDP (uW. ns)
100	22.433	0.32630	42.358	0.2337	14.8257
500	90.119	1.63189	211.788	1.0949	260.4803
1000	174.807	3.26379	423.576	2.4647	1112.2356
1500	259.914	4.89569	635.364	4.2628	2869.1214
2000	344.174	6.52759	847.151	6.2740	5539.8937
2500	428.858	8.15948	1058.939	8.7507	9051.9341

Based on above Tables and figures shown below, it is observed that when the length of an interconnects is increased its propagation delay also increases. This is because the intrinsic parameters of MWCNT are direct functions of length i.e. as the length increases the values of these parameters also increase as seen in Table 5.5-5.7. And as it is known that delay is directly proportional to these RLC parameters, therefore it also increases.

22nm technology node

Table 5.6 Variations in parameters with respect to Length for 22nm technology node.

Length (μm)	R (Ω)	L (nH)	C (fF)	Delay (ns)	PDP (uW.ns)
100	55.632	0.6143	29.506	0.2594	8.401
500	237.429	3.0718	147.528	1.1895	163.182
1000	464.625	6.1436	295.056	3.3144	849.622
1500	691.818	9.2154	442.584	5.5971	2192.306
2000	919.009	12.2872	590.112	8.9331	4420.975
2500	1146.199	15.3590	737.64	12.872	7355.213

16nm technology node

Table 5.7 Variations in parameters with respect to Length for 16nm technology node.

Length (μm)	R (Ω)	L (nH)	C (fF)	Delay (ns)	PDP (uW.ns)
100	167.173	1.2636	19.003	0.2801	6.799
500	751.687	6.3183	95.014	1.4914	112.081
1000	1482.252	12.6360	190.027	4.7990	736.222
1500	2212.812	18.9551	285.041	8.9295	2039.051
2000	2943.37	25.2595	380.054	14.7610	4254.942
2500	3673.926	31.5919	475.068	22.4170	6887.419

Another observation is made (from figure 5.3, 5.4) that the rate of increase in propagation delay and PDP is exponential even when the rate of increase of length is linear. This is so because the rate of increase in RLC parameters product with respect to length is also exponential which results in exponential increase in delay. It is also interesting to see that rate of exponential rise varies with technology i.e. smaller the technology node sharper the rise

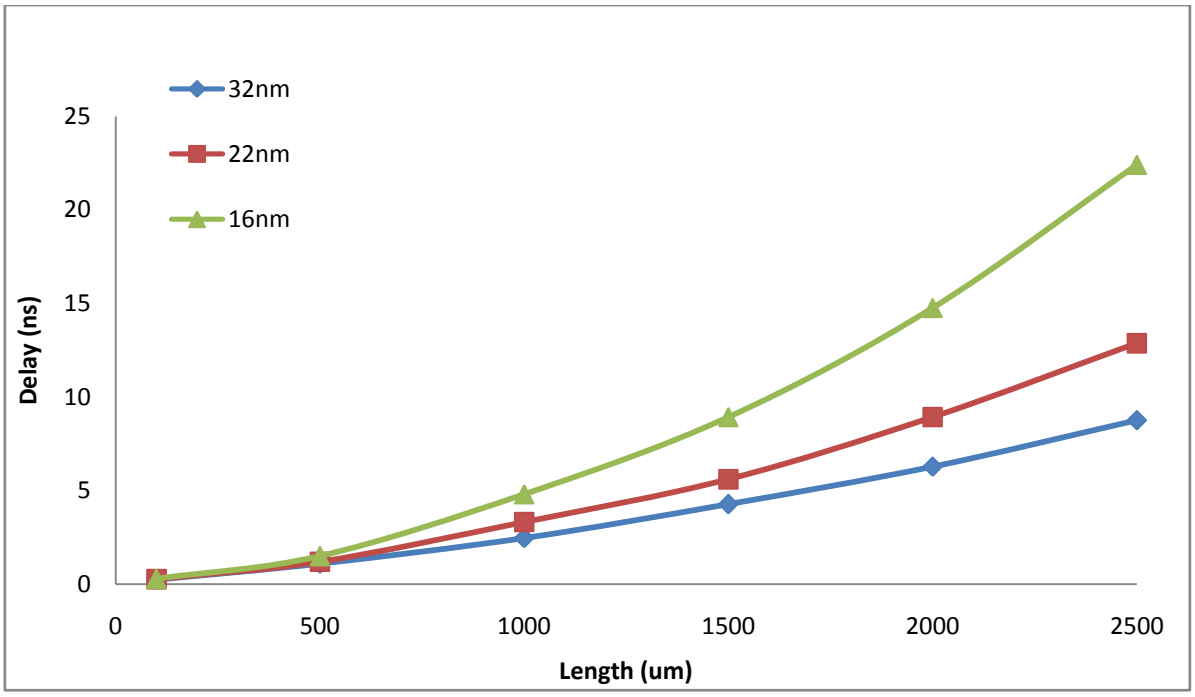

Figure 5.3 Variation of delay in MWCNT at different Lengths for different technology node.

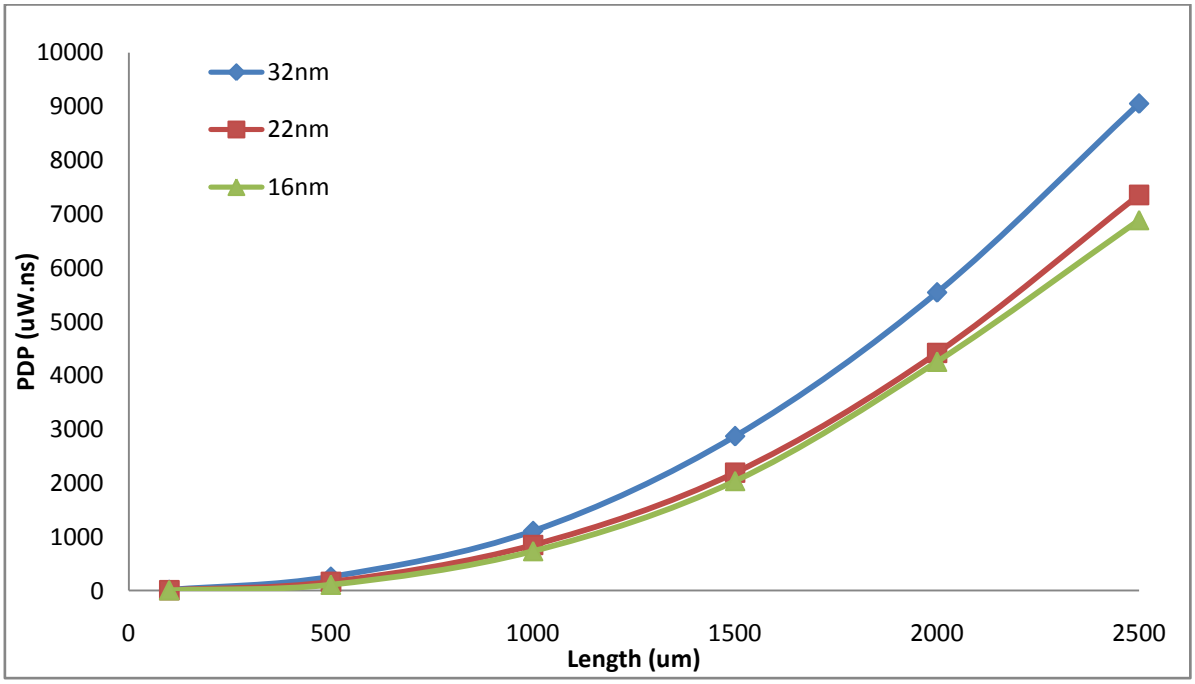

Figure 5.4 Variation of PDP in MWCNT at different Lengths for different technology node.

.5.2ANALYZING THE PROPOSED MIXED CNT BUNDLE AS AN INTERCONNECT

The RLC parameters for proposed mixed CNT are obtained by the combination of SWCNT and MWCNT using equations 1.4-1.20 and a MCCmodel is realized. Based on the MCC model, an ESC model is derived by using equations 4.1-4.11.

By considering the previous defined ITRS parameters (in Table 3.1), in the mixed CNT, the variation SWCNTs surrounding (side-walls and corners) the MWCNTs bring in the equivalent RLC parameters, propagation delay and power delay product is studied. In Table 5.8-5.10, the propagation delay and power delay product for proposed mixed CNT is shown with respect to length at different technology nodes.

32nm technology node

Table 5.8 Variation in parameters with respect to Length for 32nm technology node

Length (μm)	R (Ω)	L (nH)	C (fF)	Delay (ns)	PDP (uW.ns)
100	18.321	0.1423	46.2183	0.2228	13.6802
500	76.564	0.7118	231.0915	1.0735	246.499
1000	149.189	1.4237	462.1830	2.2103	985.304
1500	221.799	2.1355	693.274	4.0699	2719.77
2000	294.406	2.8474	924.3660	5.9853	5253.862
2500	367.012	3.5592	1155.457	8.2443	8484.646

22nm technology node

Table 5.9 Variation in parameters with respect to Length for 22nm technology node

Length (μm)	R (Ω)	L (nH)	C (fF)	Delay (ns)	PDP (uW.ns)
100	45.467	0.3079	31.650	0.23749	7.248
500	199.382	1.5395	158.252	1.1495	152.326
1000	391.523	3.0790	316.499	2.9826	783.535
1500	583.644	4.6186	474.757	5.1561	2087.724
2000	775.76	6.1581	633.009	8.3436	4180.418
2500	967.874	7.6977	791.261	11.993	6967.273

16nm technology node

Table 5.10 Variations in parameters with respect to Length for 16nm technology node.

Length (μm)	R (Ω)	L (nH)	C (fF)	Delay (ns)	PDP (uW.ns)
100	132.545	0.7035	20.290	0.2421	6.076
500	608.68	3.5178	101.448	1.4051	109.357
1000	1203.474	7.0356	202.896	4.0773	634.305
1500	1798.235	10.5534	304.344	7.9434	1845.771
2000	2392.996	14.0668	405.792	13.126	3880.422
2500	3582.504	17.5890	507.24	19.141	6223.906

From the Figures 5.5 and 5.6, it is observed that the rate of increase in delay is also exponential even when the rate of increase of length is linear. This is so because the rate of increase in RLC parameters product with respect to length is also exponential which results in exponential increase in delay. It is also interesting to see that rate of exponential rise varies with technology i.e. smaller the technology node sharper the rise.

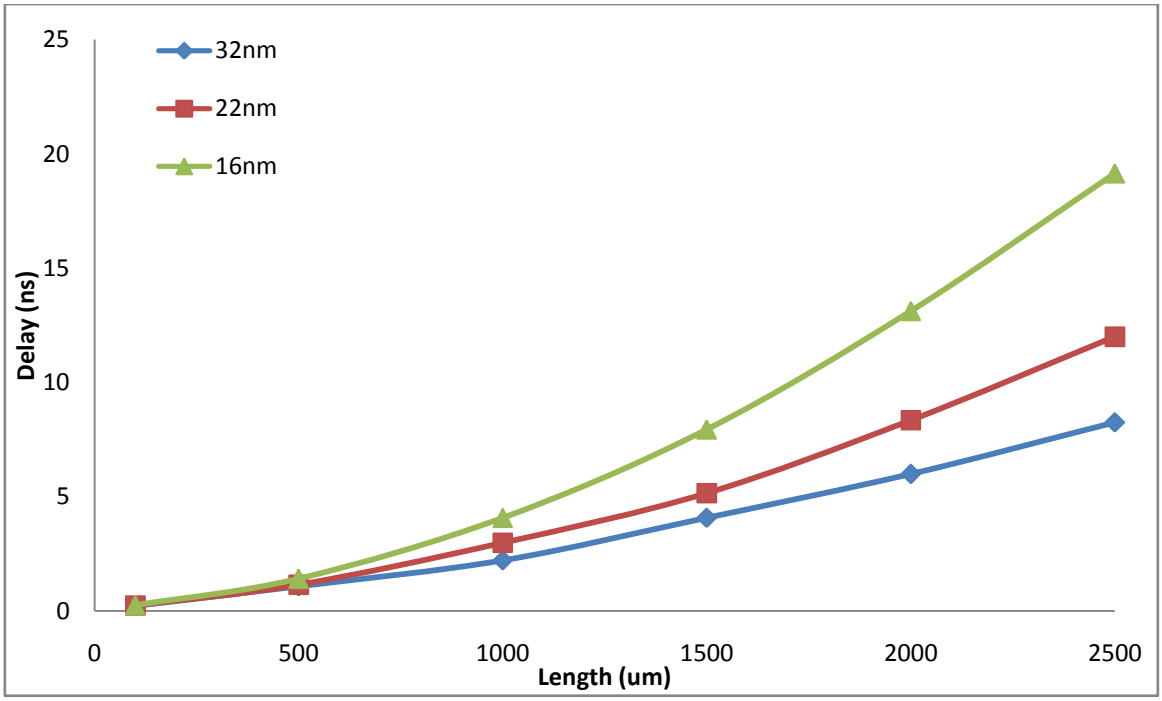

Figure 5.5 Variation of delay in mixed CNT at different Lengths for different technology node.

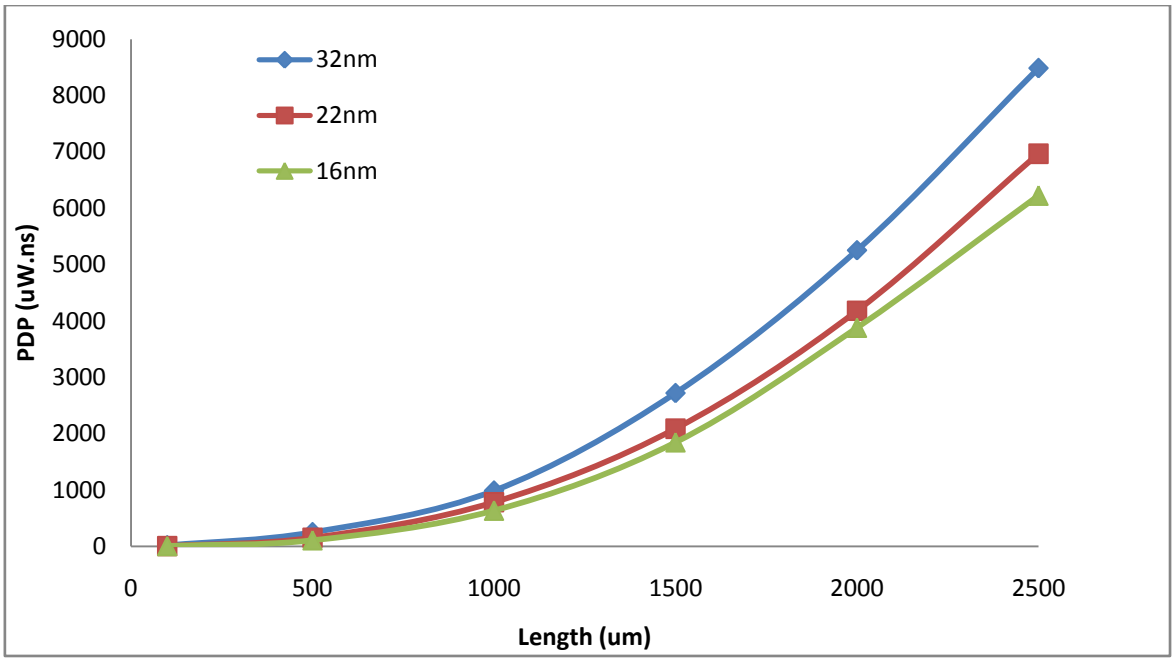

Figure 5.6 Variation of PDP in mixed CNT at different Lengths for different technology node.

5.3 PERFORMANCE COMPARISON OF PROPOSED MIXED CNT WITH MWCNT

The propagation delay and PDP of proposed mixed CNT is compared with MWCNT using the equivalent RLC parameters of both the interconnects at different technology nodes.

5.3.1 Propagation Delay comparison at different technology nodes

The comparisons of propagation delay at 32nm, 22nm and 16nm technology nodes between proposed mixed CNT and MWCNT interconnect is shown in Figures 5.7-5.9.

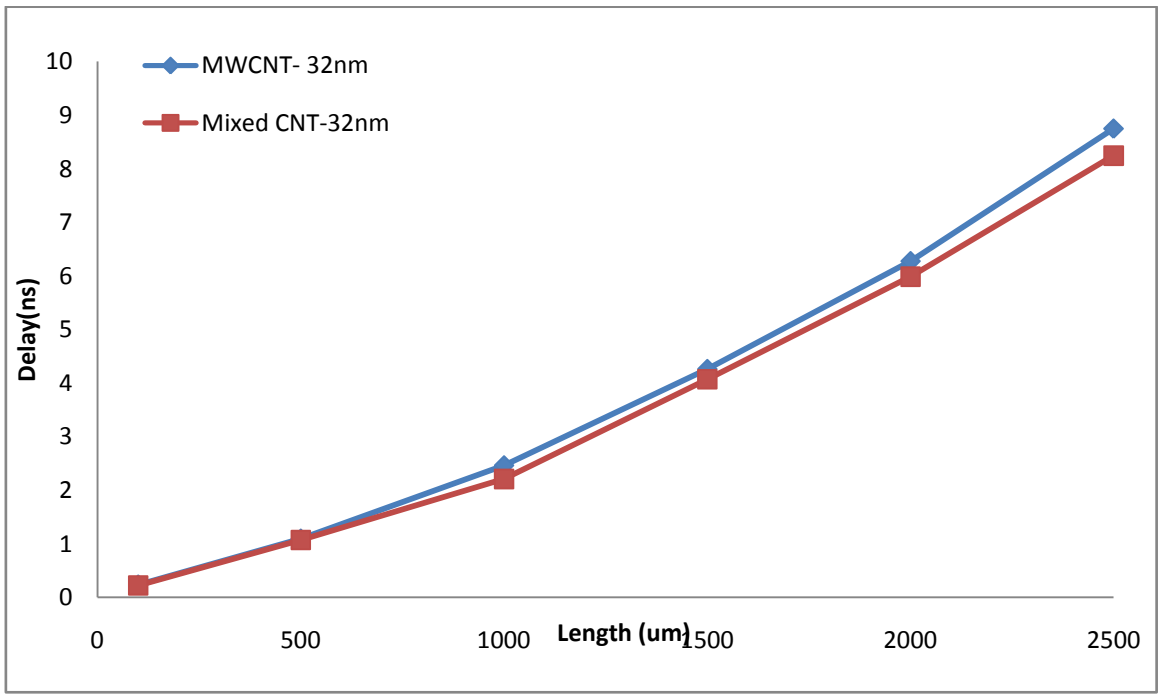

Figure 5.7 Comparison of propagation Delay at 32nm technology node.

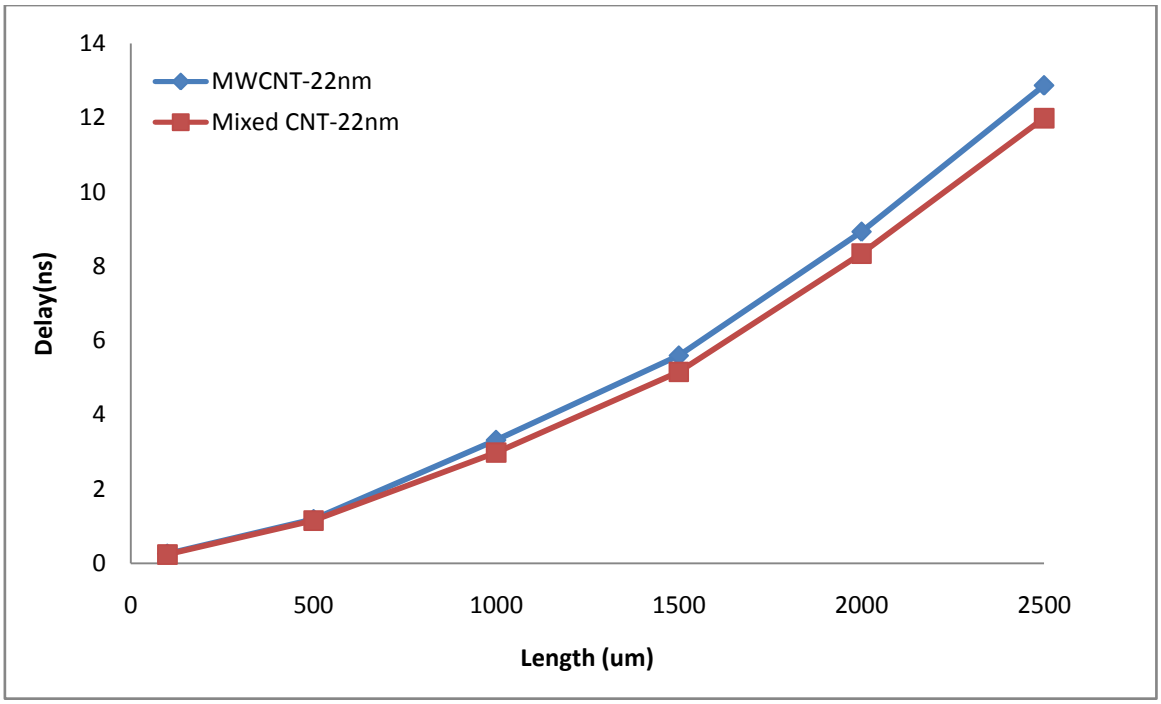

Figure 5.8 Comparison of propagation Delay at 22nm technology node.

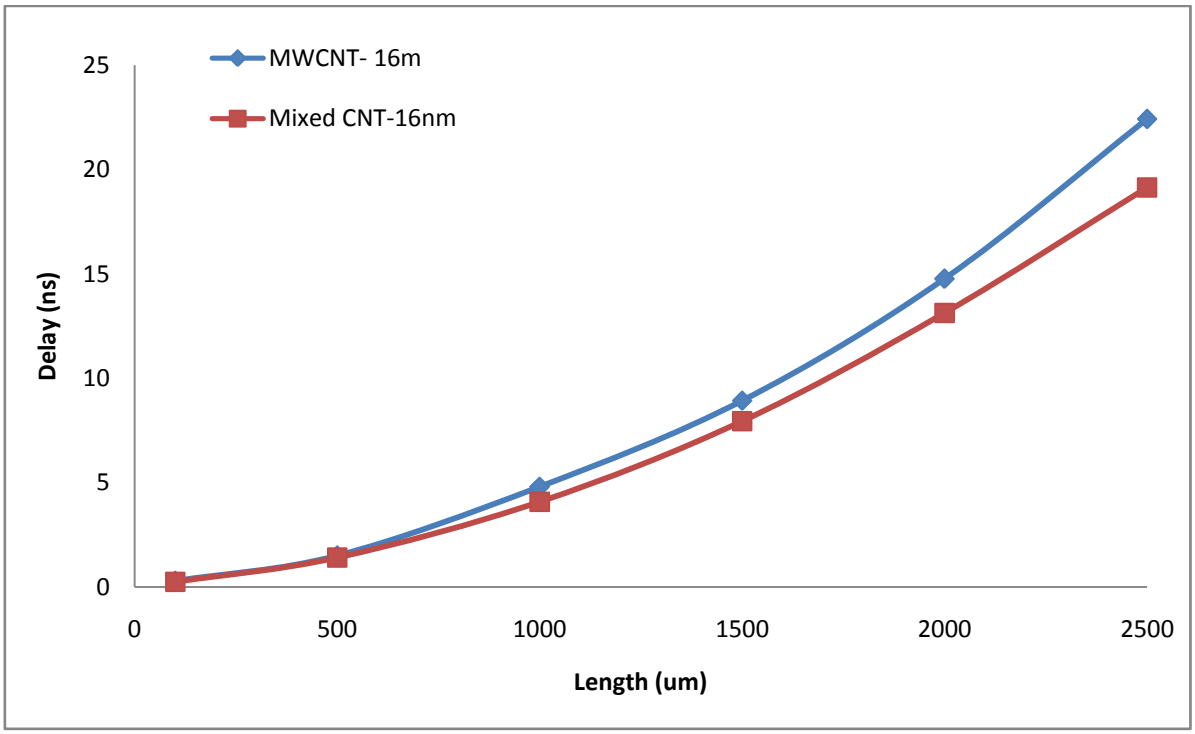

Figure 5.9 Comparison of propagation Delay at 16nm technology node

From the Figures 5.7-5.9, it is observed that the difference between the propagation delays of proposed mixed CNT and MWCNT interconnects increases with the increase in length at 32nm, 22nm and 16nm technology node. Also, the propagation delay of proposed mixed CNT structure is less than MWCNT.

5.3.2 Power Delay Product (PDP) comparison at different technology nodes.

The comparisons of power delay productat 32nm, 22nm and 16nm technology nodes between proposed mixed CNT and MWCNT interconnect is shown in Figures 5.10-5.12.

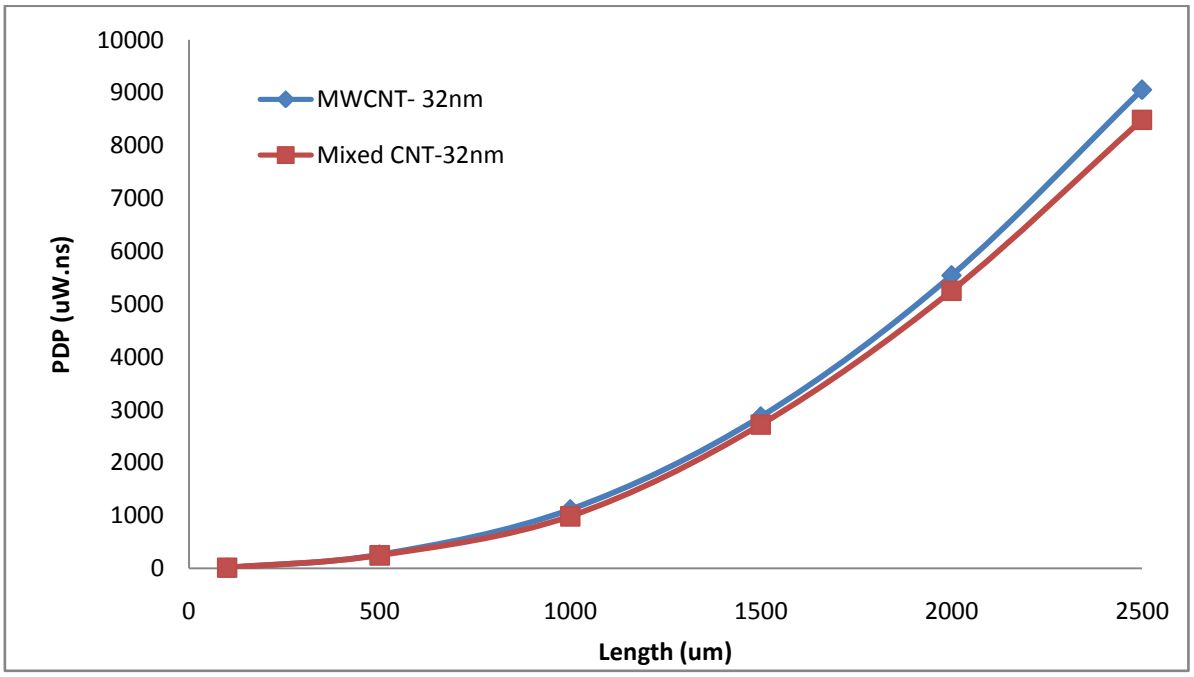

Figure 5.10 Comparison of PDP at 32nm technology node.

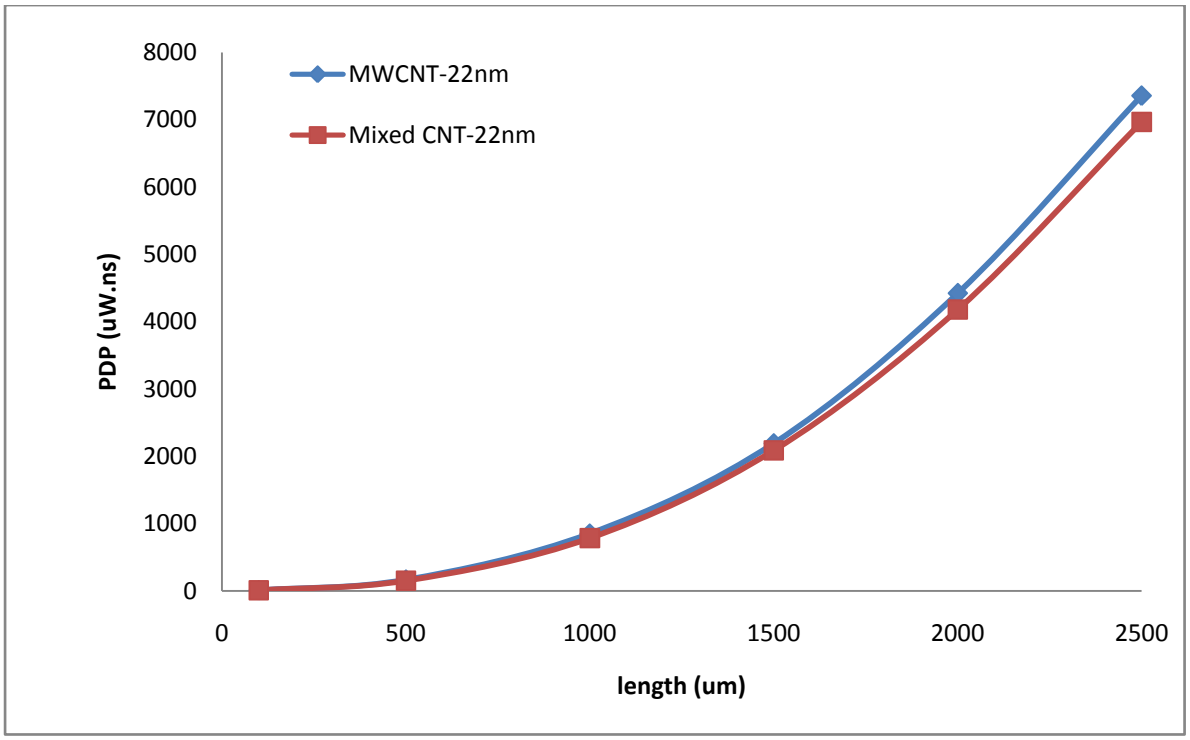

Figure 5.11 Comparison of PDP at 22nm technology node.

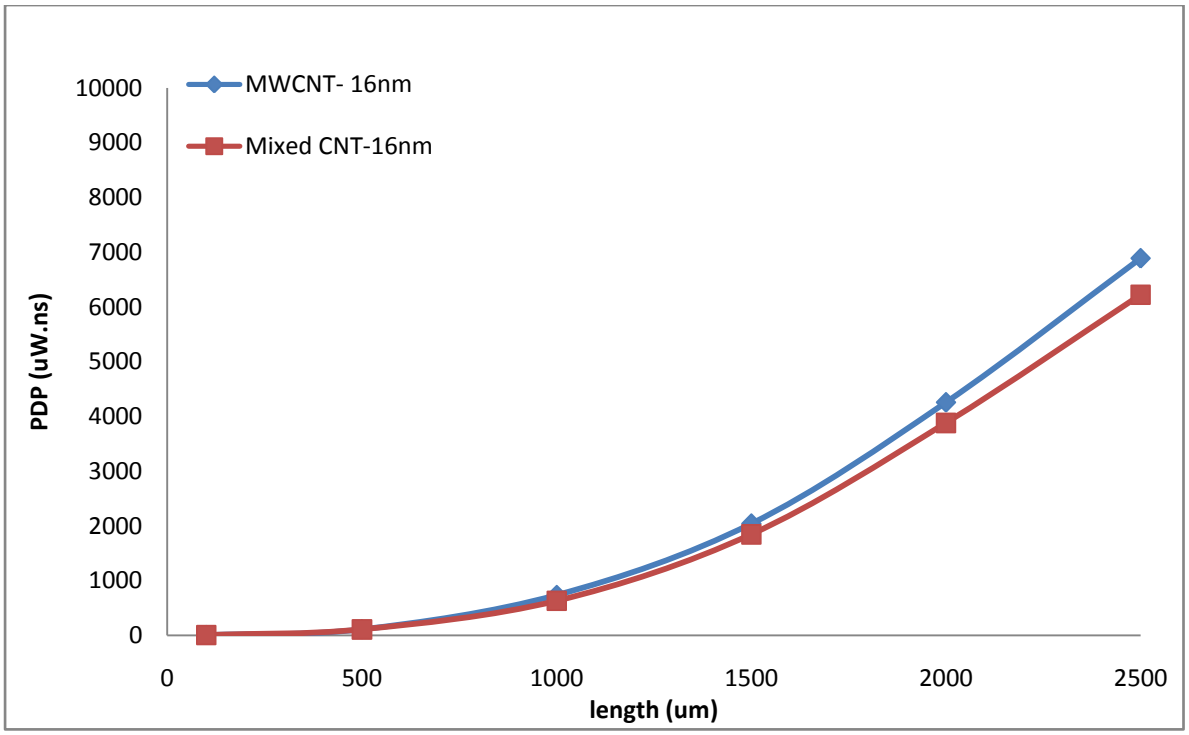

Figure 5.12 Comparison of PDP at 16nm technology node.

From the Figures 5.10-5.12, it is observed that the difference between the power delay product of proposed mixed CNT and MWCNT interconnects increases with the increase in length at 32nm, 22nm and 16nm technology node. Also, the power delay product of proposed mixed CNT structure is less than MWCNT.

In this chapter MWCNT and mixed CNT as an interconnectare analysed by considering the optimum driver size and optimum number of repeaters. The propagation delay and PDP of proposed mixed CNT are compared with MWCNT using the equivalent RLC parameters of both the interconnects for different technology nodes at different lengths. From the comparison it is observed that the proposed mixed CNT bundle has less propagation delay and the power delay product (PDP) than MWCNT bundle. So, it is concluded that mixed CNT is better than MWCNT.

CHAPTER 6

CONCLUSION AND FUTURE SCOPE

6.1 CONCLUSION

As the Cu interconnect is prone to issues with downscaling in technology, Carbon nanotubes (CNTs) are one of the good replacement to Cu interconnect.The mixed CNT bundle contains both MWCNTs and SWCNTs. Using thehierarchical modelling, MCCmodel of mixed CNT is developed. The realization of mathematical model to convert MCC model into Equivalent single conductor (ESC) model for the better performance of parameters. The performance of mixed CNT bundle as an interconnect for very large scale integration (VLSI) circuits is analyzed in this thesis. The conductivity of MWCNT is less but with the insertion of SWCNTs surrounding (side-walls and corners) the MWCNT, the overall conductivity of mixed CNT is increased which further reduces the resistance and inductance of mixed CNT.The performance of mixed CNT bundle is compared with MWCNT bundle at length100 μm to 2500 μm using the RLC parameters of ESC model. The structure is analyzed at different technology nodes i.e. 32nm, 22nm, 16nm for different lengths. The obtained results show that as length increases, propagation delay also increases. This increase in propagation delay can be significantly reduced by inserting optimum number of repeaters. Use of optimum driver size also helps in reduction of propagation delay. The propagation delay and power delay product (PDP) is calculated at length 100 μm to 2500 μm for mixed CNT bundle using Tanner EDA tool and simulation is done using SPICE files. Based on the comparison with MWCNTbundle it is concluded that the proposed mixed CNT bundle has less propagation delay and the power delay product (PDP) then MWCNT bundle. So, it is concluded that mixed CNT is better than MWCNT.

6.2 FUTURE SCOPE

The influence of temperature on the performance of mixed CNT bundle is ignored in this report and required to be studied in future. More effective CNT growth techniques are also needed to be developed and studied in order to increase the performance. The work presented in this report is at 32nm, 22nm and 16nm technology nodes and this can be extended to 10nm technology node in future.

REFERENCES

[1] S.-M. Kang and Y. Leblebici, *CMOS digital integrated circuits*: Tata McGraw-Hill Education, 2003.

[2] D. Sylvester and K. Keutzer, "Getting to the bottom of deep submicron," in *Proceedings of the 1998 IEEE/ACM international conference on Computer-aided design*, 1998, pp. 203-211.

[3] M. R. Baklanov and K. Maex, "Porous low dielectric constant materials for microelectronics," *Philosophical Transactions of the Royal Society of London A: Mathematical, Physical and Engineering Sciences,* vol. 364, pp. 201-215, 2006.

[4] B. Wei, R. Vajtai, and P. Ajayan, "Reliability and current carrying capacity of carbon nanotubes," *Applied Physics Letters,* vol. 79, pp. 1172-1174, 2001.

[5] N. Srivastava and K. Banerjee, "Interconnect challenges for nanoscale electronic circuits," *JOM Journal of the Minerals, Metals and Materials Society*, vol. 56, pp. 30-31, 2004.

[6] M. Gholipour and N. Masoumi, "Efficient model for delay estimation of MWCNT interconnects," in *Microelectronics (ICM), 2011 International Conference on*, 2011, pp. 1-4.

[7] K. Banerjee and N. Srivastava, "Are carbon nanotubes the future of VLSI interconnections?," in *Proceedings of the 43rd annual Design Automation Conference*, 2006, pp. 809-814.

[8] P. G. Collins, M. Hersam, M. Arnold, R. Martel, and P. Avouris, "Current saturation and electrical breakdown in multiwalled carbon nanotubes," *Physical review letters,* vol. 86, p. 3128, 2001.

[9] S. Haruehanroengra and W. Wang, "Analyzing conductance of mixed carbon-nanotube bundles for interconnect applications," *IEEE Electron Device Letters,* vol. 28, pp. 756-759, 2007.

[10] K. Singh and B. Raj, "Influence of temperature on MWCNT bundle, SWCNT bundle and copper interconnects for nanoscaled technology nodes," *Journal of Materials Science: Materials in Electronics*, vol. 26, pp. 6134-6142, 2015.

[11] A. Maffucci, G. Miano, and F. Villone, "Performance comparison between metallic carbon nanotube and copper nano-interconnects," *IEEE Transactions on Advanced Packaging*, vol. 31, pp. 692-699, 2008.

[12] N. Srivastava and K. Banerjee, "A comparative scaling analysis of metallic and carbon nanotube interconnections for nanometer scale VLSI technologies," in *Proc. 21st Intl. VLSI Multilevel Interconnect Conf*, 2004, pp. 393-398.

[13] M. Rahman and A. A. Chowdhury, "Analyzing carbon nanotube interconnects in VLSI application," in *Computer and Information Technology (ICCIT), 2010 13th International Conference on*, 2010, pp. 237-240.

[14] P. L. McEuen, M. S. Fuhrer, and H. Park, "Single-walled carbon nanotube electronics," *IEEE transactions on nanotechnology*, vol. 99, pp. 78-85, 2002.

[15] W. Hoenlein, F. Kreupl, G. S. Duesberg, A. P. Graham, M. Liebau, R. V. Seidel, *et al.*, "Carbon nanotube applications in microelectronics," *IEEE Transactions on components and packaging technologies*, vol. 27, pp. 629-634, 2004.

[16] N. Srivastava and K. Banerjee, "Performance analysis of carbon nanotube interconnects for VLSI applications," in *Proceedings of the 2005 IEEE/ACM International conference on Computer-aided design*, 2005, pp. 383-390.

[17] M. Tang, J. Lu, and J. Mao, "Study on equivalent single conductor model of multi-walled carbon nanotube interconnects," in *Microwave Conference Proceedings (APMC), 2012 Asia-Pacific*, 2012, pp. 1247-1249.

[18] P. Murugeswari, A. Kabilan, M. Vaishnavi, and C. Divya, "Performance analysis of single-walled carbon nanotube and multi-walled carbon nanotube in 32nm technology for on-chip interconnect applications," in *Computing, Communication and Networking Technologies (ICCCNT), 2014 International Conference on*, 2014, pp. 1-6.

[19] D. Rossi, J. M. Cazeaux, C. Metra, and F. Lombardi, "Modeling crosstalk effects in CNT bus architectures," *IEEE Transactions on Nanotechnology*, vol. 6, pp. 133-145, 2007.

[20] L. Shang, M. Liu, S. Tanachutiwat, and W. Wang, "Analyzing mixed carbon nanotube bundles: A current density study," in *Circuits and Systems, 2008. ISCAS 2008. IEEE International Symposium on*, 2008, pp. 173-176.

[21] K. Koziol, B. O. Boskovic, and N. Yahya, "Synthesis of carbon nanostructures by CVD method," in *Carbon and Oxide Nanostructures*, ed: Springer, 2010, pp. 23-49.

[22] P. J. Burke, "Luttinger liquid theory as a model of the gigahertz electrical properties of carbon nanotubes," *IEEE Transactions on Nanotechnology*, vol. 99, pp. 129-144, 2002.

[23] H. J. Li, W. Lu, J. Li, X. Bai, and C. Gu, "Multichannel ballistic transport in multiwall carbon nanotubes," *Physical review letters*, vol. 95, p. 086601, 2005.

[24] M. Nihei, D. Kondo, A. Kawabata, S. Sato, H. Shioya, M. Sakaue, *et al.*, "Low-resistance multi-walled carbon nanotube vias with parallel channel conduction of inner shells [IC interconnect applications]," in *Interconnect Technology Conference, 2005. Proceedings of the IEEE 2005 International*, 2005, pp. 234-236.

[25] H. Li, W.-Y. Yin, K. Banerjee, and J.-F. Mao, "Circuit modeling and performance analysis of multi-walled carbon nanotube interconnects," *IEEE Transactions on electron devices,* vol. 55, pp. 1328-1337, 2008.

[26] K. Singh and B. Raj, "Temperature-dependent modeling and performance evaluation of multi-walled CNT and single-walled CNT as global interconnects," *Journal of Electronic Materials,* vol. 44, p. 4825, 2015.

[27] P. Mallick, "Mixed CNT bundles as VLSI interconnects," in *Communication and Signal Processing (ICCSP), 2016 International Conference on*, 2016, pp. 0987-0990.

[28] A. Srivastava, Y. Xu, and A. K. Sharma, "Carbon nanotubes for next generation very large scale integration interconnects," *journal of nanophotonics,* vol. 4, pp. 041690-041690-26, 2010.

[29] A. Naeemi, R. Sarvari, and J. D. Meindl, "Performance comparison between carbon nanotube and copper interconnects for gigascale integration (GSI)," *IEEE Electron Device Letters,* vol. 26, pp. 84-86, 2005.

[30] A. Raychowdhury and K. Roy, "Modeling of metallic carbon-nanotube interconnects for circuit simulations and a comparison with Cu interconnects for scaled technologies," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems,* vol. 25, pp. 58-65, 2006.

[31] F. Ferranti, G. Antonini, T. Dhaene, L. Knockaert, and A. Orlandi, "Compact and accurate models of large single-wall carbon-nanotube interconnects," *IEEE Transactions on Electromagnetic Compatibility,* vol. 53, pp. 1025-1033, 2011.

[32] N. Srivastava, H. Li, F. Kreupl, and K. Banerjee, "On the applicability of single-walled carbon nanotubes as VLSI interconnects," *IEEE Transactions on Nanotechnology,* vol. 8, pp. 542-559, 2009.

[33] S. Musavvir, P. Chowdhury, and S. M. Mominuzzaman, "Delay analysis of SWCNT bundle interconnect for different technology nodes," in *Electrical and Computer Engineering (ICECE), 2016 9th International Conference on*, 2016, pp. 275-278.

[34] A. Naeemi, R. Sarvari, and J. D. Meindl, "Performance comparison between carbon nanotube and copper interconnects for GSI," in *Electron Devices Meeting, 2004. IEDM Technical Digest. IEEE International*, 2004, pp. 699-702.

[35] F. Liang, G. Wang, and W. Ding, "Estimation of time delay and repeater insertion in multiwall carbon nanotube interconnects," *IEEE Transactions on Electron Devices*, vol. 58, pp. 2712-2720, 2011.

[36] H. Sheikhassadi and N. Masoumi, "A RC model for multiwalled carbon nanotubes as interconnects," in *EUROCON-International Conference on Computer as a Tool (EUROCON), 2011 IEEE*, 2011, pp. 1-4.

[37] M. K. Majumder, P. K. Das, B. Kaushik, and S. Manhas, "Optimized delay and power performances for multi-walled CNT in global VLSI interconnects," in *Computers and Devices for Communication (CODEC), 2012 5th International Conference on*, 2012, pp. 1-4.

[38] M. Tang and J. Mao, "Modeling and fast simulation of multiwalled carbon nanotube interconnects," *IEEE Transactions on Electromagnetic Compatibility*, vol. 57, pp. 232-240, 2015.

[39] T. Alam, R. Dhiman, R. Chandel, and D. Solanki, "Mixed carbon nanotube bundle: Capacitance analysis and comparison with copper interconnect," in *Emerging Trends in Electrical and Computer Technology (ICETECT), 2011 International Conference on*, 2011, pp. 697-701.

[40] M. K. Majumder, B. Kaushik, S. Manhas, and J. Kumar, "Analysis of crosstalk delay and power dissipation in mixed CNT bundle interconnects," in *Communications, Devices and Intelligent Systems (CODIS), 2012 International Conference on*, 2012, pp. 361-364.

[41] N. D. Pandya, M. K. Majumder, B. Kaushik, and S. Manhas, "Performance Comparision of Mixed CNT Bundle in Global VLSI Interconnect," in *Communication Systems and Network Technologies (CSNT), 2012 International Conference on*, 2012, pp. 790-793.

[42] P. U. Sathyakam and P. Mallick, "Transient analysis of mixed carbon nanotube bundle interconnects," *Electronics letters*, vol. 47, pp. 1134-1136, 2011.

[43] M. K. Majumder, J. Kumar, V. R. Kumar, and B. K. Kaushik, "Performance analysis for randomly distributed mixed carbon nanotube bundle interconnects," *Micro & Nano Letters*, vol. 9, pp. 792-796, 2014.

[44] H. Bakoglu and J. D. Meindl, "Optimal interconnection circuits for VLSI," *IEEE Transactions on Electron Devices*, vol. 32, pp. 903-909, 1985.

[45] K. Singh and B. Raj, "Performance and analysis of temperature dependent multi-walled carbon nanotubes as global interconnects at different technology nodes," *Journal of Computational Electronics*, vol. 14, pp. 469-476, 2015.

[46]*Predictive Technology Model (PTM).* [Online]. Available: http://ptm.asu.edu/

LIST OF PUBLICATIONS

Arvind Thakur and K.S. Sandha "Modelling and Performance Analysis of Mixed CNT Bundle as VLSI Interconnect," Communicated for the possible publication in IET Circuits, Devices & Systems journal.

Turnitin Originality Report

601562005 by Arvind Thakur

From xyz (kss)

Processed on 17-Jul-2017 16:13 IST
ID: 831345635
Word Count: 15208

Similarity Index	Similarity by Source	
10%	Internet Sources:	5%
	Publications:	5%
	Student Papers:	5%

sources:

1 2% match (student papers from 11-Jul-2017)
Submitted to Thapar University, Patiala on 2017-07-11

2 1% match (Internet from 14-Mar-2010)
http://www.ece.ucsb.edu/Faculty/Banerjee/pubs/TED_hong_08.pdf

3 1% match (publications)
Singh, Karmjit, and Balwinder Raj. "Influence of temperature on MWCNT bundle, SWCNT bundle and copper interconnects for nanoscaled technology nodes", Journal of Materials Science Materials in Electronics, 2015.

4 1% match (publications)
Kumar, Mekala Girish, Yash Agrawal, and Rajeevan Chandel. "Carbon Nanotube Interconnects – A Promising Solution for VLSI Circuits", IETE Journal of Education, 2016.

5 1% match (publications)
SpringerBriefs in Applied Sciences and Technology, 2015.

6 1% match (publications)
K. Banerjee. "Performance analysis of carbon nanotube interconnects for VLSI applications", ICCAD-2005 IEEE/ACM International Conference on Computer-Aided Design 2005, 2005

7 < 1% match (student papers from 15-Jul-2016)
Submitted to Thapar University, Patiala on 2016-07-15

8 < 1% match (Internet from 22-Apr-2003)
http://www.ece.ndsu.nodak.edu/~jezerr/design/resources/ezusb_trm1-9.pdf

9 < 1% match (publications)
Majumder, Manoj Kumar, Pankaj Kumar Das, Vobulapuram Ramesh Kumar, and Brajesh Kumar Kaushik. "Crosstalk Induced Delay Analysis of Randomly Distributed Mixed CNT Bundle Interconnect", Journal of Circuits Systems and Computers, 2015.

10 < 1% match (Internet from 20-Apr-2012)
http://gdeepak.com/thesisme/Thesis%20Complexity%20Analysis%20Involving%20Heterogeneous%20System.pdf

11 < 1% match (Internet from 27-Apr-2003)
http://www.mmat.ubc.ca/units/bioh/people/bouffard/files/master.pdf

12 < 1% match (Internet from 11-Oct-2010)
http://www.hindawi.com/journals/jnm/2009/486979.html

13 < 1% match (student papers from 24-Jun-2015)
Submitted to Thapar University, Patiala on 2015-06-24

14 < 1% match (publications)
Wei Wang. "Analyzing mixed carbon nanotube bundles: A current density study", 2008 IEEE International Symposium on Circuits and Systems, 05/2008

15 < 1% match (Internet from 20-Oct-2013)
http://www.coursehero.com/file/2112478/schnellandrewr200608mast/

16 < 1% match (Internet from 20-Apr-2012)

http://gdeepak.com/thesisme/Cache-Aware%20And%20Cache%20Oblivious%20Algorithms.pdf

17 < 1% match (Internet from 29-Mar-2015)
http://archive.org/stream/ost-engineering-carbon_nanotubes/Carbon_Nanotubes_djvu.txt

18 < 1% match (publications)
Majumder, Manoj Kumar, Pankaj Kumar Das, and Brajesh Kumar Kaushik. "Delay and crosstalk reliability issues in mixed MWCNT bundle interconnects", Microelectronics Reliability, 2014.

19 < 1% match (student papers from 23-Apr-2015)
Submitted to University of Central Florida on 2015-04-23

20 < 1% match (Internet from 02-Nov-2009)
http://www.dmphotonics.com/Trestles%20CW%20TiSapphire%20laser%20illuminates%20carbon%20nanotube%20field%20effect%20transis

21 < 1% match (publications)
Subash, S., J. Kolar, and M. Chowdhury. "A New Spatially Rearranged Bundle of Mixed Carbon Nanotubes as VLSI Interconnection", IEEE Transactions on Nanotechnology, 2011.

22 < 1% match (Internet from 23-Jul-2012)
http://dspace.thapar.edu:8080/dspace/bitstream/123456789/181/1/8044102.pdf

23 < 1% match (Internet from 27-Feb-2014)
http://www.hipc.org/hipc2011/studsym-papers/1569508519.pdf

24 < 1% match (Internet from 11-May-2011)
http://www.facweb.iitkgp.ernet.in/~pabitra/facad/06CS6004t.pdf

25 < 1% match (Internet from 06-Nov-2002)
http://www.cs.rutgers.edu/~djimenez/cs505/lecture1.html

26 < 1% match (student papers from 09-Jul-2017)
Submitted to Thapar University, Patiala on 2017-07-09

27 < 1% match (Internet from 01-Mar-2011)
http://www.scribd.com/doc/33102271/sriimurali-prjct

28 < 1% match (Internet from 06-Oct-2010)
http://www.faqs.org/patents/app/20090315631

29 < 1% match (publications)
Raychowdhury, Arijit Roy, Kaushik. "Modeling of metallic carbon-nanotube interconnects for circuit simulations and a comparison with Cu ", IEEE Transactions on Computer-Aided Desi, Jan 2006 Issue

30 < 1% match (Internet from 23-Jul-2012)
http://dspace.thapar.edu:8080/dspace/bitstream/123456789/149/1/8043103.pdf

31 < 1% match (publications)
"Carbon Nanotubes Market Size, Share, Trends, Growth, Analysis and Forecast to 2022.", M2 Communications, March 29 2016 Issue

32 < 1% match (Internet from 17-Jan-2013)
http://dspace.thapar.edu:8080/dspace/bitstream/10266/2076/1/satnamsinghbhullar.pdf

33 < 1% match ()
http://vsp2.ecs.umass.edu/icdg/publications/pdffiles/thesis_proposal/amaheshw_ms.pdf

34 < 1% match (Internet from 22-Aug-2013)
http://ijcsce.org/wp-content/uploads/2013/06/IJCSCSESI040713.pdf