I_{DDQ} Testing of Two Stage CMOS Operational Amplifier

A Thesis Submitted in partial fulfillment of the

requirements for the award of degree of

Master of Technology

in

VLSI Design & CAD

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July-2009

CERTIFICATE

I hereby certify that the work which is being presented in the thesis entitled, **"I_{DDQ} Testing of Two Stage CMOS Operational Amplifier"**, in partial fulfillment of the requirements for the award of degree of **Master of Technology in VLSI Design and CAD** at **Thapar University**, Patiala, is an authentic record of my own work carried out under the supervision of **Ms. Alpana Agarwal, Asst. Professor,** and refers other researcher's work which are duly listed in the reference section.

The matter embodied in this thesis has not been submitted for the award of any other degree of this or any other university.

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This is to certify that the above statement made by the candidate is correct and true to the best of my knowledge.

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ACKNOWLEDGEMENT

First of all, I would like to express my gratitude to Ms. Alpana Agarwal, Asst. Professor, ECED, Thapar University, Patiala, for her patient guidance and support throughout this Thesis work. I am truly very fortunate to have the opportunity to work under her as a student. It was both an honor and a privilege to work with her. She also provides help in technical writing and presentation style and I found this guidance to be extremely valuable.

I am thankful to Dr. A. K. Chatterjee, Professor and Head, Electronics and Communication Engineering Department and also to Mr. Mohd Iliyas, Lecturer, Electronics and Communication Engineering Department for their motivation and inspiration that triggered me for my thesis work.

I am also thankful to all my friends who devoted their valuable time and helped me in all possible ways towards successful completion of this work. I do not find enough words with which I can express my feeling of thanks to the entire faculty and staff of ECED, Thapar University, Patiala, for their help, inspiration and moral support which went a long way in successful completion of my work. I thank all those who have contributed directly or indirectly to this work.

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ABSTRACT

Since the birth of semiconductor industry, current measurement based testing of electronics components has always been an integral part of the testing. It is used to detect gross shorts and is generally referred to as static I_{DD} test. The present form of quiescent current (I_{DDQ}) measurement based testing for CMOS VLSI, known as I_{DDQ} testing used for the detection of bridging faults. I_{DDQ} testing refers to the integrated circuit (IC) testing method based upon measurement of steady state power-supply current. I_{DDQ} stands for quiescent I_{DD}, or Quiescent power-supply current. It is little more than 15-years since the idea of I_{DDQ} testing was first proposed. Many semiconductor companies now consider I_{DDQ} testing as an integral part of the overall testing for all IC's.

In this thesis, a two stage CMOS operational amplifier is designed and Design for Testability method for this two-stage CMOS amplifier, based on I_{DDQ} testing, for improving fault-coverage and testability is discussed. This test method takes the advantage of good fault coverage. Fault detection is achieved using a simple Built in Current Sensor (BICS), which introduces insignificant performance degradation of the Circuit under Test (CUT), to monitor the power supply quiescent current changes in the CUT. The testability has also been enhanced in the testing procedure using a simple fault-injection technique. The approach is attractive for its simplicity, robustness, cost effectiveness and capability of Built in Self Testing (BIST) implementation. It can also be generalized other CMOS analog and mixed-signal integrated circuits.

The technology used is TSMC 0.35um, 3.3V CMOS N-well process for the designing of CMOS Op-amp. The value of the load capacitance is taken as 3pF.

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INTRODUCTION

1.1 Background

With the growing use of analog circuits in commercial mixed-signal integrated circuits and systems, testing of analog integrated circuits is considered as one of the most important problems in analog and mixed-signal integrated circuit design. Testing of analog system is an experiment in which the analog system is exercised and its resulting response is analyzed to ascertain whether it behaves correctly. If incorrect behavior is detected, a second goal of a testing experiment may be to diagnose, or locate, the cause of the misbehavior. Diagnosis assumes knowledge of the internal structure of the system under test. A major difficulty in analog testing is the typically large number of specifications that need to be tested. Unlike digital systems, many of these specifications may take continuous values, once again, requiring the use of more expensive analog test equipment. In addition, to measure all the specifications, multiple test setups are often utilized, which greatly increases the test time and cost. The test development efforts for analog circuits today are disproportionally high due to lack of widely accepted automation methods. The evaluation of a particular test input and measurement setup requires the determination of the probabilistic detection of all faults in the circuit. This evaluation step is the most time consuming step during analog test development.

Analog circuits have traditionally been tested for critical specifications [1] e.g., ac gain over a range of frequencies, common-mode rejection ratio, signal-to-noise ratio, linearity, slew rate, due to the lack of simple fault models. The functional testing usually results in longer test times because of redundant testing. It does not provide either a good test quality or a quantitative measure of test effectiveness or fault coverage. Reducing test time by optimizing the functional test set while achieving the desired parametric fault coverage has also been studied [2]. However, the technique needs a reasonably large number of sample circuits for collecting the test data.

Analog CMOS circuits have also been tested by varying the supply voltage in conjunction with the inputs [3]. This technique aims to sensitize faults by causing the transistors to switch between different regions of operation. A ramped power supply voltage has been used to test faults in op-amp circuits. In [4], an ac supply voltage has

been used for improving the fault coverage. Although these techniques have achieved high fault coverage, the number of faults injected was quite small. Using this idea of varying supply voltage and combining it with supply current monitoring [5], larger analog circuits have been tested for short circuit fault detection. But the method suffers from the fact that, gate-source shorts that have negligible effect on supply current and gate-source shorts of transistors which do not switch their mode of operation to any applied stimulus, could not be detected. Other testing methods for analog circuits include dc testing, power-supply quiescent current (I_{DDQ}) monitoring and digital signal processing techniques [6].

1.2 Testing Methodology

In this thesis, Design for Testability method for a two-stage CMOS amplifier, based on I_{DDQ} testing, for improving fault-coverage, and testability is discussed. This test method takes the advantage of good fault coverage through the use of I_{DDQ} testing. Fault detection is achieved using a simple Built in Current Sensor (BICS), which introduces insignificant performance degradation of the Circuit under Test (CUT), to monitor the power supply quiescent current changes in the CUT. The testability has also been enhanced in the testing procedure using a simple fault-injection technique. The approach is attractive for its simplicity, robustness and capability of Built in Self Testing (BIST) implementation. It can also be generalized other CMOS analog and mixed-signal integrated circuits.

1.3 Advantages of I_{DDQ} Testing

In CMOS integrated circuits, the dominant failures are due to gate oxide shorts (GOS). GOS are unexpected connections between the gate and the drain, source, or channel (substrate, p-well, and n-well) that are caused by pinholes in the gate oxide layer. These faults initially may not cause functional failure but will first appear as parametric drifts and can manifest into potential defects over a period of time [7]. Gate oxide shorts can cause degraded signals and can increase leakage currents in CUT. Leakage current based I_{DDQ} testing will detect these parametric drifts before they actually change the circuit behavior. In [8,9], data exists that show that a device that fully passes the logic functional tests but fail the I_{DDQ} test, fall in a significant category that functionally fail more frequently earlier than its normal life. Current testing also is an invaluable tool for

detecting faults in devices that contain both analog and digital functions on a single substrate [10]. This testing combines the advantages of simple signal analysis procedure, functional as well as defect-oriented testability, cost effectiveness, easy implementation and applicability to large class of mixed-signal circuits.

1.4 Thesis Organization

Following the introduction (**Chapter 1**) the **Chapter 2** provides an overview of testing of analog circuits, I_{DDQ} testing, development in I_{DDQ} testing, need of I_{DDQ} testing.

Chapter 3 discusses the overview of op-amp, op-amp parameters, the basic structure and operation of a two-stage CMOS operational amplifier. And also discusses the various calculation steps taken to design the final design. In this chapter the various iterations have been pointed out and the equations followed to implement the design.

Chapter 4 explains the various physical defects, concept of I_{DDQ} testing, design and implementation of the built-in current sensor. The mechanism of fault simulation and fault detection in the amplifier using the BICS is explained.

Chapter 5 describes the simulation results, process corner results, fault detection, coverage of the amplifier and design considerations for the I_{DDQ} testing method. Finally Layout and LVS report are included.

Chapter 6 provides a summary of the work presented and scope for future work.

Chapter-2

LITERATURE SURVEY

Digital systems are much easier and smaller to design than comparable analogue circuits. This is one of the main reasons why digital systems are more common than analog systems. An analog circuit must be designed by hand, and the process is much less automated than for digital systems. Also, because the smaller the integrated circuit (chip) the cheaper it is, and digital systems are much smaller than analog, therefore a digital system is cheaper to manufacture than an analog one, generally. But, there are some applications, where it is very difficult or even impossible to replace analog functions with their digital counterparts regardless of advances in technology. Thus, analog circuits are gaining importance day by day. Testing of these circuits is needed because testing has to keep pace with circuits design development to provide the required quality of production.

2.1 Testing of Analog circuits

Testing of analog circuits is an experiment in which the analog circuit is exercised and its resulting response is analyzed to ascertain whether it behaves correctly. If incorrect behavior is detected, a second goal of a testing experiment may be to diagnose, or locate, the cause of the misbehavior. Diagnosis assumes knowledge of the internal structure of the system under test. A major difficulty in analog testing is the typically large number of specifications that need to be tested. Unlike digital systems, many of these specifications may take continuous values, once again, requiring the use of more expensive analog test equipment. In addition, to measure all the specifications, multiple test setups are often utilized, which greatly increases the test time and cost. The test development efforts for analog circuits today are disproportionally high due to lack of widely accepted automation methods. The evaluation of a particular test input and measurement setup requires the determination of the probabilistic detection of all faults in the circuit. This evaluation step is the most time consuming step during analog test development.

After designing an analog integrated circuit, it is fabricated, and tested. If it fails the test, then there must be a cause for the failure. Either (a) the test was wrong, or (b) the fabrication process was faulty, or (c) the design was incorrect, or (d) the specification

had a problem. Anything can go wrong. The role of testing is to detect whether something went wrong and the role of diagnosis is to determine exactly what went wrong, and where the process needs to be altered. Therefore, correctness and effectiveness of testing is most important for quality products (another name for perfect products). If the test procedure is good and the product fails, then we suspect the fabrication process, the design, or the specification. A well thought out test strategy is crucial for economical realization of products.

The benefits of testing are quality and economy. These two attributes are not independent and neither can be defined without the other. Quality means satisfying the user's needs at a minimum cost. A good test process can weed out all bad products before they reach the user. However, if too many bad items are being produced then the cost of those bad items will have to be recovered from the price charged for the few good items that are produced. It will be impossible for an engineer to design a quality product without a profound understanding of the physical principles underlying the processes of manufacturing and test.

Realizing of VLSI chips is shown in Fig 2.1. Requirements are the user needs satisfied by the chip. They are often derived from the function of the particular application, for example controlling fuel injection in a car, controlling a robot arm, or processing pictures from a space shuttle. One sets down the specifications of various types, which include function (input output characteristics), operating characteristics (power, frequency, noise, etc.), physical characteristics (packaging, etc.), environmental characteristics (temperature, humidity, reliability, etc.), and other characteristics (volume, cost, price, availability, etc.). The objective of design is to produce data necessary for the next steps of fabrication and testing [11]. Design has several stages. The first, known as architectural design, produces a system-level structure of realizable blocks to implement the functional specification.

The second, called logic design further decomposes blocks into logic gates. Finally, the gates are implemented as physical devices (e.g., transistors) and a chip layout is produced during physical design. The physical layout is converted into photo masks that are directly used in the fabrication of silicon VLSI chips. Fabrication consists of processing silicon wafers through a series of steps involving photo resist, exposure through masks, etching, ion implantation, etc. Impurities and defects in materials,

equipment malfunctions, and human errors are some causes of defects. The likelihood and consequences of defects are the main reasons for testing. Another very important function of testing is the process of diagnosis. It must to find what went wrong with each faulty chip, be it in fabrication, in design, or in testing or, in using unrealizable specifications.

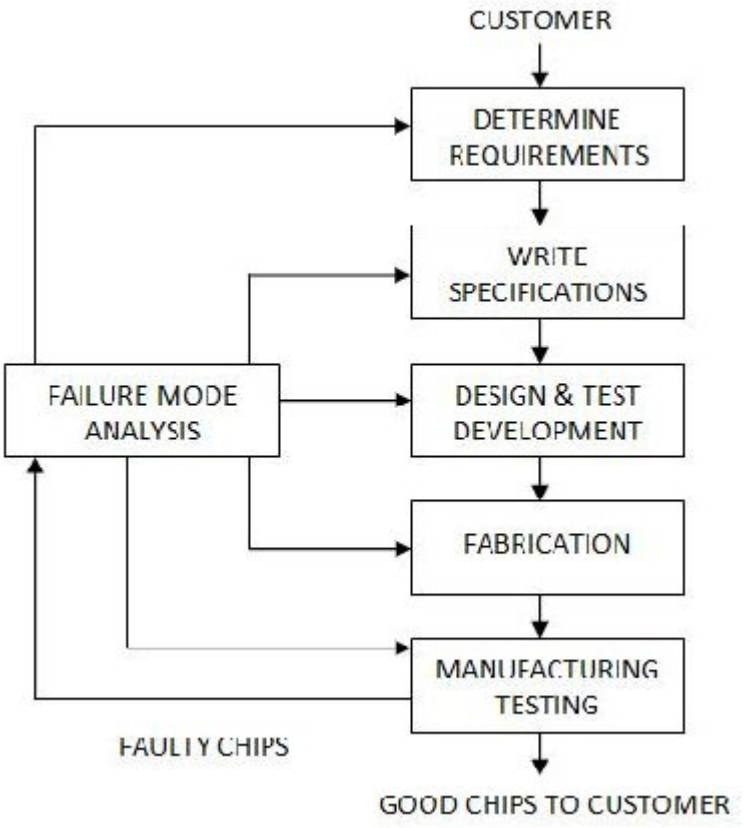


Fig 2.1 VLSI realization process

The faulty chip analysis is called Failure Mode Analysis (FMA). Failure mode analysis or faulty chip analysis uses many different test types, including examination through optical and electron microscopes, to determine the failure cause and fix the process. From above Fig 2.1, the arrows out of the failure mode analysis block represent the corrective actions applied to the faulty steps of the realization process. Considering the process as a pipeline (or assembly line) with the flow direction from top to bottom, so the effort between the point where error occurred and the point of testing, where it was detected, is wasted. At the time the error is detected, the portion of the pipeline between these two points is filled with faulty product which will be either reworked or discarded.

Wasted effort and material adds to the product cost. Testing should, therefore, be placed closest to the point of error.

2.1.1 Faults in Analog domain

The faults in the analog domain can be classified into two major types, catastrophic faults, which are opens and shorts at the layout or transistor level, and parametric faults, which are defined as out-of-tolerance deviations in the process, circuit, or system parameters [12]. Catastrophic faults typically result in the complete malfunction of the circuit, making them relatively easier to detect. Marginal parametric faults, on the other hand, are much harder to detect due to their continuous nature and the masking effect of the within-tolerance variations in other circuit parameters [13-15]. The continuous characteristic of the parametric faults spectrum, the process variations and their masking effects are major difficulties limiting the development of efficient test generation for parametric faults [16]. Based on the observation that test evaluation requires injecting many parametric and catastrophic faults into the circuit and analyzing the masking effect of process variations, a fault injection and simulation technique is developed for analog circuits that is specifically geared toward information reuse.

The generating task of analog structural tests is more difficult [16]. The main sources of this difficulty are that,

(a) parametric faults cannot be enumerated as in the digital domain since their spectrum is continuous,
(b) parametric fault coverage is accurate as long as the fault list is representative of this continuous spectrum of faults,
(c) the continuous nature and the non-linearity of analog circuit characteristics make the test generation problem more complex to deal with, causing the lack of an adequate fault-model similar to stuck-at faults in digital testing,
(d) Process variations introduce uncertainty on circuit parameters and characteristics, and induce fault masking.

The detect ability of faults in the analog domain is probabilistic as it depends on the exact values of the remaining circuit parameters [17]. In order to evaluate the coverage of a test input, a large number of circuit instances needs to be considered for each fault, where all circuit parameters other than the faulty parameter vary within their tolerances. The determination of which test inputs and setups detect a given set of faults is the most

time consuming step in analog test development (also referred to as fault simulation). Tests can be classified into fault detection, fault location or fault prediction. In the manufacturing process or during maintenance, a quick check is needed to pass the good parts and reject the bad parts for maximum product throughput. Therefore, only fault detection is needed to evidence the faults. At other times, fault location is needed to detect failed modules or components for repair. Fault prediction is used mainly with highly reliable products or safety related products. Fault prediction continuously monitors the Circuit under Test (CUT) to identify whether any of its elements are about to fail allowing for a preventive repair. The choice between fault location and fault detection calls for a compromise. Fault location needs better isolation of the components and provides better test coverage. It may be used during both production and repair, but it may slow down the testing process and the throughput.

2.1.2 Fault and Fault modeling

In the context of fault diagnosis, a fault is understood as any kind of malfunction in the system that leads to an unacceptable anomaly in the overall system performance. A fault in a system can be very costly in terms of loss of production, equipment damage and economic setback. Faults are developed in a system due to normal wear and tear, design or manufacturing defects or improper operation leading to stress beyond endurable limits. In many cases degradation in the performance of the system is sustained for some duration before it actually "fails". In many other cases a system continues to operate with a failed component resulting in degraded performance.

The variety of fault modes that can occur may be classified as,

(a) Abrupt (sudden) faults, i.e., step-like changes.
(b) Incipient (slowly developing) faults, e.g., drift or bias.

Typically, abrupt faults play an important role in safety-critical applications (e.g. in power plants, transportation systems and drug manufacturing systems, etc,), where a system failure have to be detected early enough so that disastrous consequences arising due to failures can be avoided by early system reconfiguration. On the other hand, incipient faults are of major relevance in connection with maintenance problems where early detection of worn out components is required. In this case faults are typically small and not as easy to detect, but the detection time is of minor importance and may therefore be large. In the study of fault diagnosis the construction of a fault dictionary

using fault simulation techniques are widely used for choosing the test strategy. Some methodologies use schematics as the starting point to generate fault lists in fault simulation. For example, when a fault list is generated, every component is either shorted, or opened, shorted to power, shorted to ground in single fault situation, or a large number of different fault combinations are considered in multiple fault cases. The disadvantage of doing so is that it neglects the physical layout information of the circuitry and hence it could generate some unrealistic faults in the lists or a prohibitively large fault list. Therefore very often a single fault assumption is made.

A failure mode is the effect by which a failure is observed, while a failure mechanism is the chemical, physical, or metallurgical process, which leads to component failure. In electronic components, there exist different failure modes such as open circuit, short circuit, degraded performance and functional failures. Degradation faults depend mainly on variations of certain parameters of the components used in a circuit from its nominal values. This may be due to manufacturing defects, process variations, change in the environment or ambient temperature and/or wear out due to aging. Functional faults, on the other hand, are based on the fact that a circuit may continue to function, but some of its performance specifications may lie outside their acceptable ranges.

An effective fault model is a fundamental issue for a successful analog test and diagnosis strategy. The fault list is the set of all modelled faults and the test generated by the test process should detect all modelled faults. Realistic analog fault models can be achieved by knowing the behaviour of the circuit. In general, an analog IC under test can have the following three outcomes,

(a) **Catastrophic (hard) failure**: The circuit is not functioning at all.

(b) **Unacceptable performance degradation**: In this case, the circuit is still functioning, but some of its performance specifications lie outside their acceptable range. Performance degradation is usually referred to as a soft failure.

(c) **Acceptable performance**: The circuit is functioning and all its performance parameters are within their specification ranges. In this case, the circuit is said to be correct. From above, faults in analog ICs are generally classified in to the following two categories,

(i). Catastrophic (hard) faults: Catastrophic faults are all those changes to the circuit that cause the circuit to fail catastrophically. These faults include shorts, opens or large variations of a design parameter like forward beta (β) in

Bipolar Junction Transistors (BJTs) and width and length of MOS Field Effect Transistors (MOSFETs). Catastrophic faults are caused by major structural deformations or extreme out-of range parameters and lead to failures that manifest themselves in a completely malfunctioning circuit. Electro-migration and particle contamination phenomena occurring in the conducting and metallisation layers are the major causes of opens and bridging shorts.

(ii). Parametric (soft) faults: parametric faults are those changes that cause performance degradation of the circuit. These faults are due to the process fluctuations. These faults involve parameters' deviations from their nominal value that can consequently quit their tolerance band. Parametric faults are due to out-of-specification parameter deviations and so depend on the acceptability band defined by tolerances of process parameters.

As analog faults are continuous in mode they can take an infinite number of values and so, the only difference between catastrophic and parametric faults depend on the concept of "totally malfunctioning circuit". In addition, faults considered catastrophic at one description level may become parametric at a higher one. Further, a good knowledge of the probability of occurrence of all possible defects is necessary for actual fault coverage estimation by a test methodology. As described above faults in analog ICs can be classified into two categories, catastrophic faults or hard faults and parametric faults or soft faults.

Therefore the taxonomy of analog faults can be represented as shown in Fig 2.2. There is a region of acceptable behaviour around nominal range. Beyond this region, there is circuit performance that does not meet design specification, but does not cause complete circuit failure. Finally there are faults that render the circuit inoperable. Since both hard faults and soft faults can take on infinitely many varieties, there are infinitely many analog faults. Consequently, we must choose a subset of faults, which will lead to the best possible fault list.

2.1.3 Test stimulus generation

The determination of a test pattern usually involves feedback from a fault model. In a first step a list of all faults considered by the fault model is made. In the second step a test pattern is assumed and all faults detected by it are removed from the fault list.

Repeating this step for new test patterns progressively reduces the fault list. Towards the end of the iteration process the contribution of new pattern decreases, since the fault list becomes small. One new pattern may be needed to remove one single fault from the list, while other new patterns do not make any contribution at all. Although an exhaustive application of this deterministic algorithm promises the detection of all detectable faults, the duration of the search process and the length of the resulting test pattern may be excessive. A balance between coverage and cost must be found at this point.

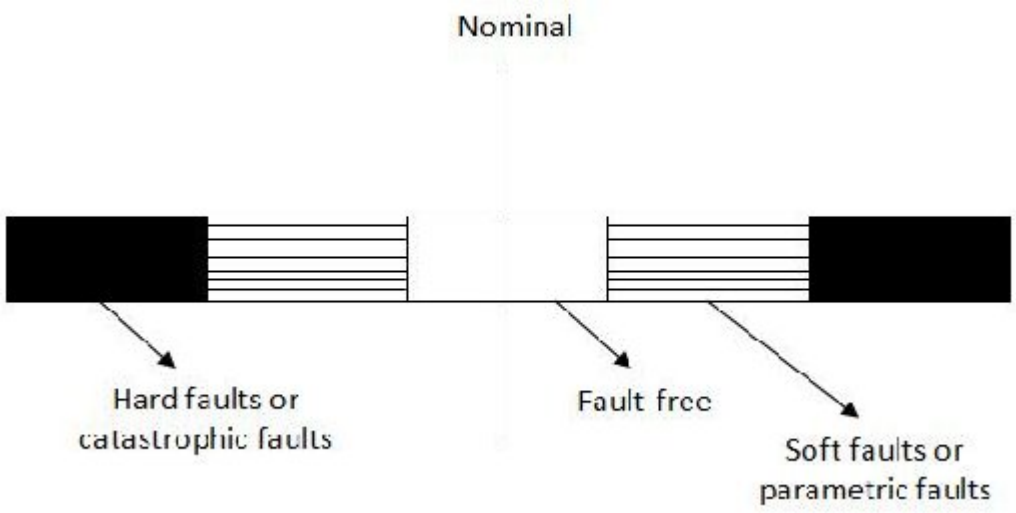


Fig 2.2 Taxonomy of analog faults

A special case of the deterministic test is the exhaustive test, for which all possible test patterns are applied. While this test produces the best possible coverage, it is impracticable for a complete VLSI chip. Considering the partitioning method a sum of exhaustive tests can be applied progressively to all parts of the circuit. This method is called pseudo exhaustive test .Test pattern generation for the exhaustive and pseudo-exhaustive test is trivial and does not involve fault simulation. In a completely different approach a fixed number of test patterns are generated without feedback from the fault model. The sequence of test patterns is called pseudo-random, because it has some important properties of a random sequence, while being totally predictable and repeatable. The coverage of the test sequence is checked by fault simulation. This process of analysing coverage via a fault simulation is called fault grading. If a sufficient coverage level has been reached, the set is accepted; otherwise a new one is generated. One drawback of this pseudo-random algorithm is that the required length of the test

sequence is often hard to determine a priori. Statistical frameworks have been derived for this purpose.

Although a sequence found by this approach does not necessarily have the best test coverage possible, it has advantages over the deterministic search,

(a) For a reasonable coverage limit the determination of a sequence is extremely fast.
(b) The random patterns can easily be generated on-chip by a hardware random generator.
(c) Random patterns have been shown to have much better coverage for non-target defects, i.e., faults that are not considered by the fault model [11].
(d) Since cost is an extremely critical issue in every design, the deterministic approach may have to be terminated at a quite early iteration stage. In this case the results of the random approach with comparable cost may be superior.

First, the Circuit under Test (CUT) must be simulated using a suitable test stimulus generator and then the output of the CUT must be analysed. There are two distinctly different approaches for the generation of the most commonly used test stimulus like the sinusoidal waveform, and the square, triangular, pulse, etc. waveforms. The first approach employs a positive feedback loop consisting of an amplifier and an RC or LC frequency selective network. These circuits which generate sinusoidal waveforms utilising resonance phenomena are known as linear oscillators. Circuits that generate the square, triangular, pulse, etc. waveforms are called nonlinear oscillators or function-generators.

2.1.4 Fault diagnosis

The general idea is to test the response of the circuit at a given frequency. Deviations in circuit parameters caused by any fault will affect the output response, either in its amplitude or phase. The test engineer must supply a minimum number of excitation frequencies in order to detect various component faults. As shown in Fig 2.3 the test of an electronic circuit is a stimulus/response measurement. In the first step a test pattern is applied to the circuit to bring it to a defined initial state or exercise some functionality. In the second step the circuit processes the test pattern and in the third step the circuit's response is checked. This test procedure is repeated for different test patterns by a test controller. Basically a test signal is applied to the circuit under test (CUT) and the response of the system is analysed. The analyser matches the response or responses to a

pre-existing knowledge base and classifies the behaviour of the CUT. A precision analog test stimulus generator is an essential component of the fault detection and diagnosis scheme of analog integrated circuits.

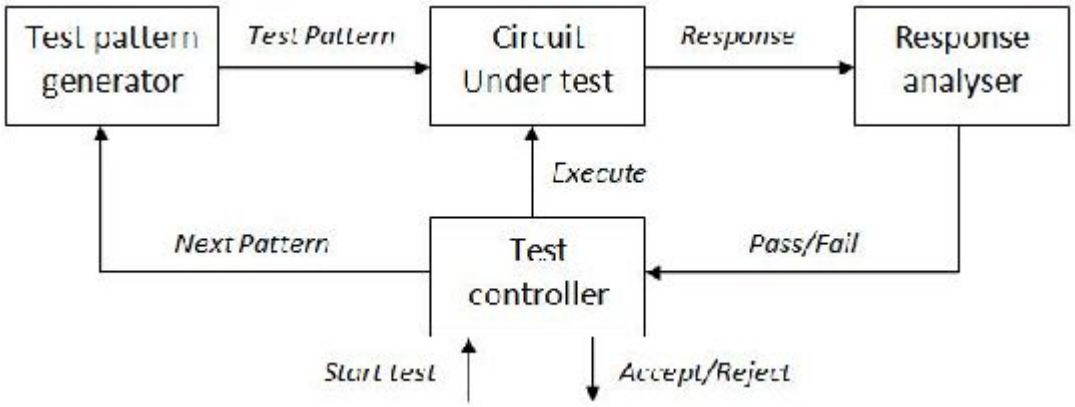


Fig 2.3 Architecture of a typical fault diagnostic set-up

One problem central to testing is the determination of an optimal test pattern fulfilling the following essential requirements,

(a) Detection of (ideally) all defects assumed in the fault model,
(b) Ease of generation/storage (low overhead) and
(c) Compactness (short test stimulus generation time).

This stimulus generator depends on the type of test measurement to apply. Four categories of measurements can be distinguished,

(a) **DC static measurements**: They include the determination of the DC operating points, DC bias and DC offset voltages and DC gains. DC faults are detected by a single set of steady state inputs.
(b) **AC dynamic measurements**: They measure the frequency response of the circuit under test. The input stimulus is usually a sine waveform with variable frequency. Harmonic spectral analysis can be performed using DSP techniques.
(c) **Time domain measurements**: They use pulse signals (square wave, step and pulse trains), ramps or triangular waveforms as the input stimuli of the circuit. Some of the parameters derived are slew rate, rise and delay times.
(d) **Noise measurements**: They measure the variation in the signal that appears at the circuit's output when the input is set to zero.

Depending on the circuit, some or all of these measurements may be required. The output response of the Circuit under Test (CUT) contains all the necessary diagnostic information. This information can now be processed (or analysed) in a number of ways to extract measures of various parameters. Those will provide the desired diagnosis of the CUT.

2.2 I_{DDQ} Testing of Analog Circuits

I_{DDQ} testing of analog circuits refers to the integrated circuit (IC) testing method based upon measurement of steady state power-supply current. I_{DDQ} stands for quiescent I_{DD}, or quiescent power-supply current. Today, the majority of IC's are manufactured using complementary metal–oxide–semiconductor (CMOS) technology. In steady state, when all switching transients are settled-down, a CMOS circuit dissipates almost zero static current. The leakage current in a defect-free CMOS circuit is negligible (on the order of few nano amperes). However, in case of a defect such as gate-oxide short or short between two metal lines, a conduction path from power-supply (V_{DD}) to ground (GND) is formed and subsequently the circuit dissipates significantly high current. This faulty current is a few orders of magnitude higher than the fault-free leakage current. Thus, by monitoring the power-supply current, one may distinguish between faulty and fault-free circuits [18].

2.2.1 History of I_{DDQ} Testing

Since the birth of semiconductor industry, Current measurement based testing of electronics components has always been an integral part of the testing. It is used to detect gross shorts and is generally referred to as static I_{DD} test. The present form of quiescent current (I_{DDQ}) measurement based testing for CMOS VLSI, known as I_{DDQ} testing, was first publicly proposed in 1981 for the detection of bridging faults [19-21]. Around the same time, researchers at IBM also proposed the monitoring of switching current to detect transient failures (noise related failures) in memory devices [22]. In the following couple of years, a number of labs reported that monitoring quiescent current is an effective method to detect various physical defects such as bridging, gate oxide shorts, inter-gate shorts, stuck-on faults, etc [23-25]. In this early stage, besides government/defense labs (such as Sandia Labs), few commercial semiconductor manufacturers included I_{DDQ} testing as part of their overall test program [26]. It is worth mentioning that commercial semiconductor manufacturers have always measured static

I_{DD} as part of the parametric test as an integral part of the overall testing. Although, it can be considered as single I_{DDQ} measurement, by almost every manufacturer even today, this test is identified by a different name (static I_{DD} test, I-test, easy current test, etc.) and considered separately from I_{DDQ} testing, which implies multiple measurements.

By the mid 1980s, semiconductor manufacturers started to recognize I_{DDQ} testing as an effective means to detect physical defects. It is worth noticing that long before CMOS became the mainstream, semiconductor companies were aware of the limitations of the stuck-at fault model that many physical defects do not map onto stuck-at faults [27-28]. Thus, besides having less than 100% stuck-at fault coverage during testing, conventional testing in the voltage environment was not sufficient for higher quality and a testing method targeted toward layout/process oriented defects was needed. Such testing gained acceptance in mid 1990s after I_{DDQ} testing was recognized as a cost-effective method. While most of the work in mid 1980s on current measurement was based upon off-chip measurement circuitry, around 1989 proposals appeared for on-chip current sensors.

In the early 1990s, I_{DDQ} testing started to gain acceptance in the commercial semiconductor industry. The defect oriented simulation method such as Inductive Fault Analysis clearly showed why many defects do not map onto stuck-at faults and not detected by the conventional testing [29-30]. Particularly, as the minimum feature size became less than 1.0 μm, particle defects and bridging became the dominant cause of failure. Since I_{DDQ} testing provides physical defect oriented testing, it gained acceptance. Other reasons were the cost-effective testing mechanism requiring little work by the circuit designer, negligible or no area overhead or increase in die-size and a small number of vectors in the I_{DDQ} test set. Since late 1980s, many papers started to appear in conferences and journals describing various aspects of I_{DDQ} testing.

By the mid–1990s, many companies developed CAD tools for I_{DDQ} vectors and a number of EDA and semiconductor companies such as Sunrise (now View Logic), Crosscheck (now Duet), System Science (now Synopsys), Ford Microelectronics, LSI Logic, Lucent, IBM, etc. also commercialized these tools. Some of these tools selected I_{DDQ} vectors from a functional test set, while a few tools also included an I_{DDQ} ATPG. The fault models used in these tools are stuck-at, pseudo stuck-at, toggle coverage and bridging fault models. Since I_{DDQ} testing is oriented toward physical defects, few people also considered I_{DDQ} testing as part of the reliability testing, although many considered it as a

supplement to the functional/logic testing. In mid 1990s, a number of studies were conducted to correlate the effectiveness of I_{DDQ} testing with conventional reliability screenings (stress testing). These studies prompted a few companies such as Intel, LSI Logic, etc. to use I_{DDQ} testing as a supplement to reliability screening and reduced their standard burn-in time on some products. In 1996, Semiconductor Research Corporation (SRC) task force identified I_{DDQ} and defect oriented testing as one of the key test methodologies with other methodologies such as Core test for the late 1990s and into the 21st century. This task force recommended that the SRC sponsored university research be guided in that direction. The report of this task force has been used widely in industry to fund independent university research. It is expected that sponsored research on various aspects of I_{DDQ} testing will continue as well as its use in commercial industry will continue to increase.

2.2.2 Need of I_{DDQ} Testing

There are various reasons which describe need of I_{DDQ} testing. The primary reason is that it is extremely cost effective and uses root cause of problem (physical defect) to identify a bad part. For IC manufacturers, this is an attractive, low cost supplemental test to the functional and stuck-at fault based testing. All the factors in the test cost, such as additional design effort and area, test generation effort, simulation time and test application time, are relatively very small compared to the testing in voltage environment. While increasing the stuck-at fault coverage from 80% to 90%–95% in voltage environment may double the test cost, adding a small I_{DDQ} test set is relatively inexpensive and may provide equivalent (sometimes better) benefits. The fault coverage by functional and stuck-at test vectors becomes asymptotic (depending upon circuit and test effort, it is in 90%–99% range), but, after that it requires a large number of additional vectors to get incremental advantage. However, fault coverage can quickly be raised, approaching to 100%, by adding a small I_{DDQ} test set to the functional and stuck-at test set. With the available data, it appears that more than 95% fault coverage can be achieved cost-effectively by adding I_{DDQ} test set of about 20 vectors to the functional and stuck-at test set with 80%–85% coverage. Increasing fault coverage beyond that requires adding a large number of I_{DDQ} vectors or increasing functional and stuck-at coverage by logic testing or both. It should also be noticed that I_{DDQ} testing does not check the functionality and hence it is not a replacement of functional testing; it should always be used as a supplemental test.

Another advantage of I_{DDQ} testing is that it provides massive observability, thus, the test generation effort is very low compared to logic testing. I_{DDQ} testing requires only fault sensitization. Hence, the fault propagation effort during test generation is not needed. It also provides very high detectability capability per I_{DDQ} vector.

A further reason is that as the minimum feature size shrinks, many defects of no consequence in large geometry become catastrophic in smaller geometry. For example, a particle of size 0.5 m causing extra metal was relatively unimportant when metal pitch was 2.0 m, the same defect in a technology with 0.25- m metal pitch most likely will cause a catastrophic short between metal lines (bridging). Logic testing is quite limited in detection of bridging while I_{DDQ} testing is ideally suited for this. There are reports that I_{DDQ} testing can also detect defects that do not cause catastrophic failures but only timing related faults (such as resistive bridging and sub-threshold leakage).

Another example is the gate-oxide which is generally grown by dry thermal oxidation between 850^{o} C to 950^{o} C. For a 200-Å-thick gate-oxide, ±10 Å variation in the thickness as well as presence of some micro-pores, pin-holes and nonstichiometry oxide at the $Si–SiO_2$ interface may be acceptable. But the same variation in thickness and quality will result into catastrophic failure in technology with 50–60-Å thick gate-oxide. Conventional logic based testing using the stuck-at fault model is quite limited in detection of these defects. On the other hand, I_{DDQ} testing is specifically suitable to detect these and many other process oriented defects. Thus, in some sense, due to the absence of any other testing method to detect process oriented defects, I_{DDQ} testing is needed.

Chapter-3

DESIGN OF TWO STAGE CMOS OPERATIONAL AMPLIFIER

Complementary metal oxide semiconductor (CMOS) operational amplifier is a core element of almost all analog and mixed signal systems. CMOS op amps and a few passive components can be used to realize such important functions as summing and inverting amplifiers, integrators, and buffers. The combination of these functions and comparators can result in many complex functions, such as high-order filters, signal amplifiers, analog-to-digital (A/D) and digital-to-analog (D/A) converters, input and output signal buffers, and many more.

This chapter discuss about Ideal op amps and its parameters ideal values, basic op amp structure and its parameters such as gain bandwidth product, common mode rejection ratio, power supply rejection ratio *etc.*, and the design of two stage CMOS operational amplifier in detail.

3.1 Ideal Operational Amplifier

Ideally op amp is differential amplifier with two inputs and one output, infinite gain, infinite input resistance so that no loading effect can occur and zero output resistance.

The Thevenin amplifier model is shown in Fig 3.1 below, showing standard op amp notation. It amplifies the voltage difference, $V_d = V_p - V_n$, on the input port and produces a voltage, V_o, on the output port that is referenced to ground [31-32].

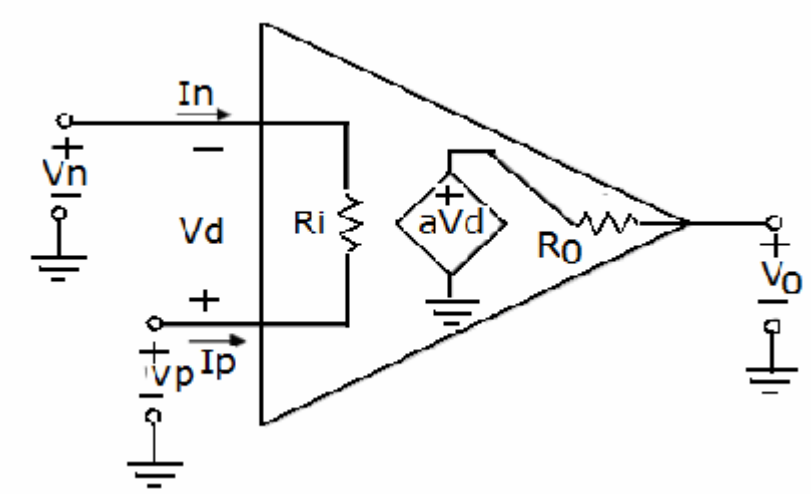


Fig 3.1 Standard Op-amp Notation

The ideal op amp model was derived to simplify circuit calculations and is commonly used by engineers in first order approximation calculations. The ideal model makes three simplifying assumptions,

(a). Gain is infinite $A_v = \infty$

(b). Input Resistance is infinite $R_i = \infty$

(c). Output Resistance is zero $R_o = 0$.

Applying these assumptions to Fig 3.1 results in the ideal op amp model shown in Fig 3.2

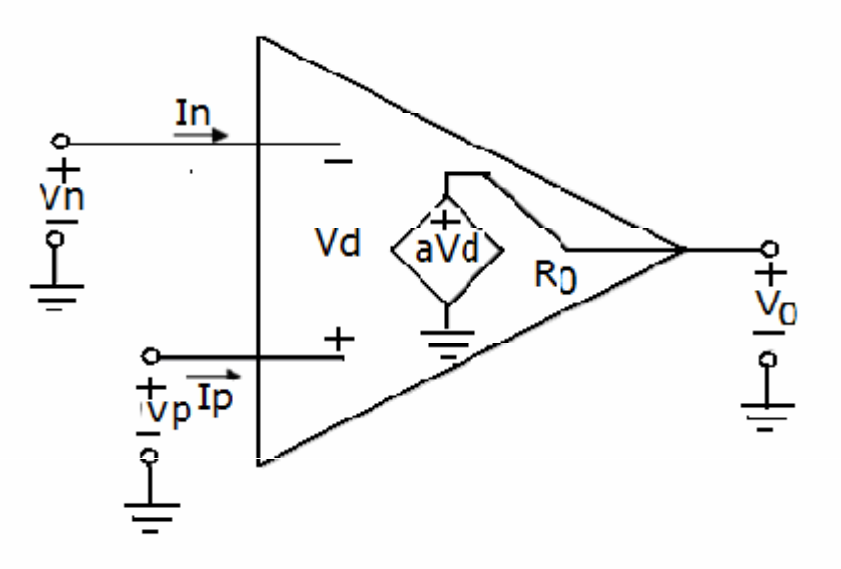


Fig 3.2 Ideal Op-amp Model

Other simplifications can be derived using the ideal op amp model,

(a). $I_n = I_p = 0$

Because $R_i = \infty$ we assume $I_n = I_p = 0$. There is no loading effect at the input.

(b). $V_o = A_v \times V_d$

Because $R_O = 0$ there is no loading effect at the output.

(c). $V_d = 0$

If the op amp is in linear operation, V_o must be a finite voltage. By definition, $V_o = A_v \times V_d$. Rearranging, $V_d = V_o / A_v$. Since $A_v = \infty$, $V_d = V_o / \infty = 0$. This is the basis of the virtual short concept.

(d). Common mode gain = 0

The ideal voltage source driving the output port depends only on the voltage difference across its input port. It rejects any voltage common to V_n and V_p.

(e). Bandwidth = ∞

(f). Slew Rate = ∞

No frequency dependencies are assumed.

(g). Drift = 0

There are no changes in performance over time, temperature, humidity, power supply variations, etc.

3.2 Basic Operational Amplifier

It can be defined as a "high-gain differential amplifier". By high it means a value that is adequate for the application, typically in the range of 10^1 to 10^5. Since op amps are usually employed to implement feedback system, their open loop gain is chosen according to the precision required of the closed loop circuit.

Up to two decades ago, most op amps were designed to serve as "general-purpose" building blocks, satisfying the requirement of many different applications. In contrast, today's op amp design proceeds with the recognition that the trade-offs between the parameters eventually require a multi-dimensional compromise in the overall implementation, making it necessary to know the adequate value that must be achieved for each parameter [33]. The op amp has several performance parameters those are discussed below.

3.3 Operational Amplifier Performance Parameters

Large signal voltage amplification, A_v: The open loop gain of an op amp determines the precision of the feedback system employing the op amp. The required gain can be adjusted according to the application. Trading with the parameters such as speed and output voltage swings, the minimum required gain must therefore be known. A high open loop gain is also necessary to suppress nonlinearity. It is denoted by A_v, it is the ratio of the peak-to-peak output voltage swing to the change in input voltage required to drive the output.

$$A = \frac{V_{(\quad)}}{V} \tag{3.1}$$

Differential voltage Amplification, A_{VD}: The ratio of the change in the output to the change in differential input voltage producing it with the common-mode input voltage held constant.

$$A = \frac{\Delta}{\Delta} \quad , \qquad (3.2)$$

Unity gain bandwidth, UGB: The range of frequencies within which the open-loop voltage amplification is greater that unity (Fig 3.3).

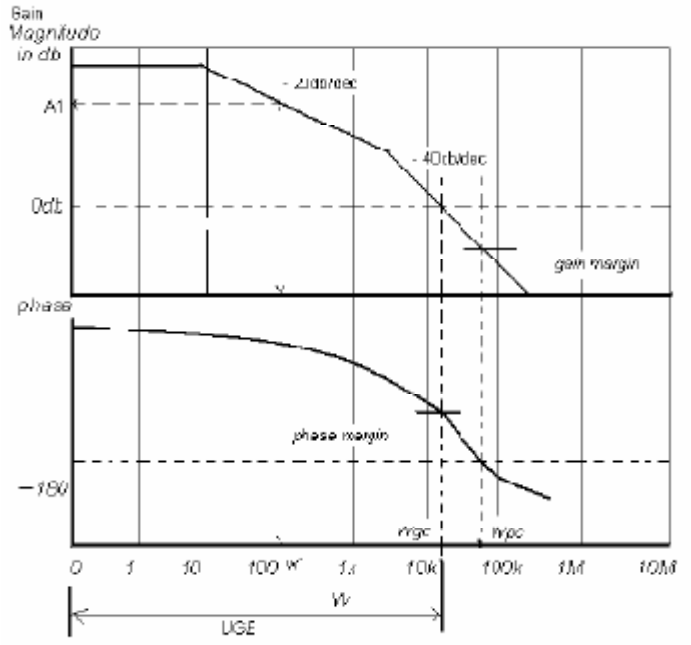


Fig 3.3 Unity Gain Bandwidth (UGB), Gain Margin (GM) and Phase Margin (PM)

Gain bandwidth product, GBW: The product of the open-loop voltage amplification and the frequency at which it is measured. From Fig 3.3, Gain bandwidth product is

$$GBW = A \times \omega \qquad (3.3)$$

Maximum-output swing Bandwidth, BOM: The range of frequencies within which the maximum output voltage swing is above a specified value.

Common-mode rejection ratio, CMRR: The relative sensitivity of an op-amp to a difference signal as compared to common-mode signal is called common mode rejection ratio (CMRR). I.e. it is the ratio of differential voltage amplification to common-mode voltage amplification. CMRR falls off as the frequency increases.

$$\text{CMRR} = \frac{\text{A}}{\text{A}} \tag{3.4}$$

Note: This is measured by determining the ratio of a change in input common-mode voltage to the resulting change in input offset voltage.

Supply voltage rejection ratio, SVRR: The absolute value of the ratio of the change in supply voltages to the change in input offset voltage.

$$\text{SVRR} = \Delta\text{V} \quad \pm/\Delta\text{V} \tag{3.5}$$

Slew rate, SR: The average time rate of change of the closed-loop amplifier output voltage for a step-signal input.

$$\text{SR} = \frac{\text{dv}}{\text{dt}} \tag{3.6}$$

In op amps we trade power consumption for noise and speed. To increase slew rate, the bias currents within the op amp are increased.

Gain margin, GM: The reciprocal of the open-loop voltage amplification at the lowest frequency at which the open-loop phase shift is such that the output is in phase with the inverting input.

Phase margin, PM: The absolute value of the open-loop phase shift between the output and the inverting input at the frequency at which the modulus of the open-loop amplification is unity.

Gain and phase margins are measures of stability for a feedback system, though often times only phase margin is used rather than both. Based the magnitude response of the loop gain, $|A_v|$, gain margin is the difference between unity and $|A_v (W_{180°})|$ where $W_{180°}$ is the frequency at which the loop gain phase, is -180°, called as Phase crossover frequency. Phase margin is the phase difference between phase of A_v (W_0dB) and -180° where W_0dB is the frequency at which $|A_v|$ is unity,called Unity gain frequency (Fig 3.3).

Common-mode input voltage range, V_{ICR}: The range of common-mode input voltage that if exceeded may cause the operational amplifier to cease functioning properly.

Maximum peak output voltage swing, V_{OM}: The maximum positive or negative voltage that can be obtained without waveform clipping when quiescent dc output voltage is zero.

Maximum peak-to-peak output voltage swing, V_O(PP): The maximum peak-to-peak voltage that can be obtained without waveform clipping when quiescent dc output voltage is zero.

Input resistance, R_i: It is the resistance between inverting and non-inverting terminals of operational amplifier. That is, it is the resistance between the input terminals with either input grounded.

Differential input resistance, R_{id}: The small-signal resistance between two ungrounded input terminals (Fig 3.4).

Output resistance, R_o: The resistance between an output terminal and ground.

Input offset voltage, V_{io}: The dc voltage that must be applied between the input terminals to force the quiescent dc output voltage to zero or other level, if specified.

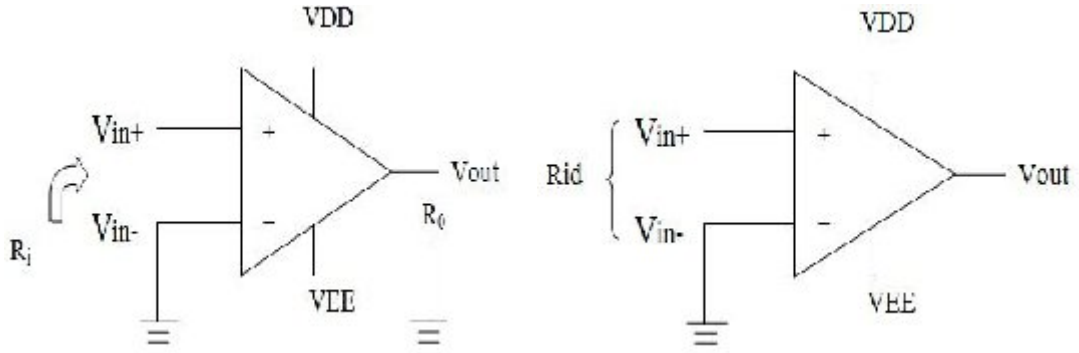


Fig 3.4 Showing R_i, R_{id} and R_o

Input offset current, I_{io}: The difference between the currents into the two input terminals with the output at the specified level (Fig 3.5).

$$I = (I - I) \quad (3.7)$$

Input bias current, I_B: Depending on the type of input transistor, the bias current can flow in or out of the input terminals. The input current is modeled as current sources, I_{b+} and I_{b-}, in parallel with the positive and negative input terminals.

$$I = (I + I) / 2 \quad (3.8)$$

It is the average of the currents into the two input terminals with the output at the specified level (Fig 3.5).

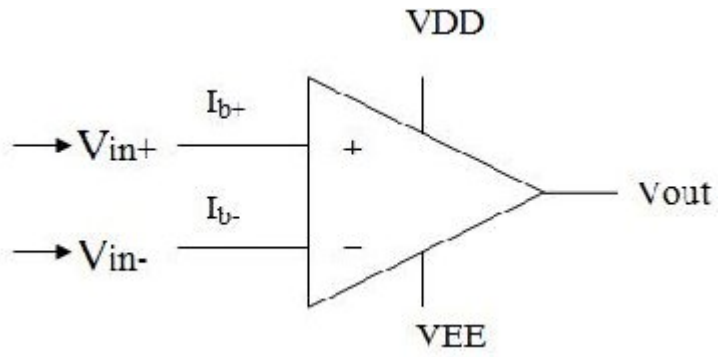


Fig 3.5 Op-amp Input Bias Current and Input Offset Current

3.4 Design of a CMOS Operational Amplifier

The design of a CMOS operational amplifier consists of three functional building blocks as shown in Fig 3.6. First, there is an input differential gain stage that amplifies the voltage difference between the input terminals, independently of their average or common-mode voltage. Most of the critical parameters of the op-amp like the input noise, common-mode rejection ratio (CMRR) and common mode input range (CMIR) are decided by this stage.

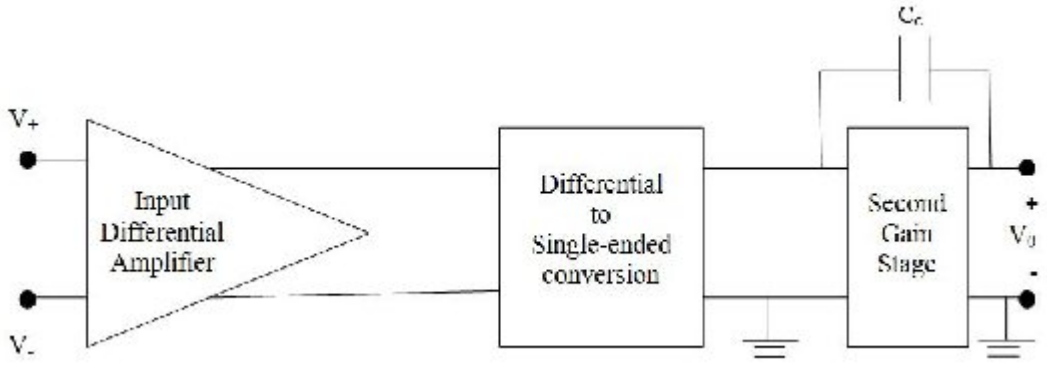


Fig 3.6 Block Diagram of an Integrated Operational Amplifier

The differential to single-ended conversion stage follows the differential amplifier and is responsible for producing a single output, which can be referenced to ground. The differential to single-ended conversion stage also provides the necessary bias for the second gain stage. Finally, additional gain is obtained in the second gain stage which is normally a common-source gain stage that has an active load. Capacitor, C_C is included between the differential and the common-source stages to ensure stability when the amplifier is used with feedback. An output stage can be added to provide a low output

resistance and the ability to source and sink large currents, but in this design it is not employed since it is not necessary in the present work. In the following subsections, the description as well as the design methodology of each of the stages mentioned above is presented.

3.4.1 A Two Stage CMOS Amplifier

Fig 3.7 shows the circuit diagram of a two-stage, internally compensated CMOS amplifier used for the testing. The circuit provides good voltage gain, a good common-mode range and good output swing.

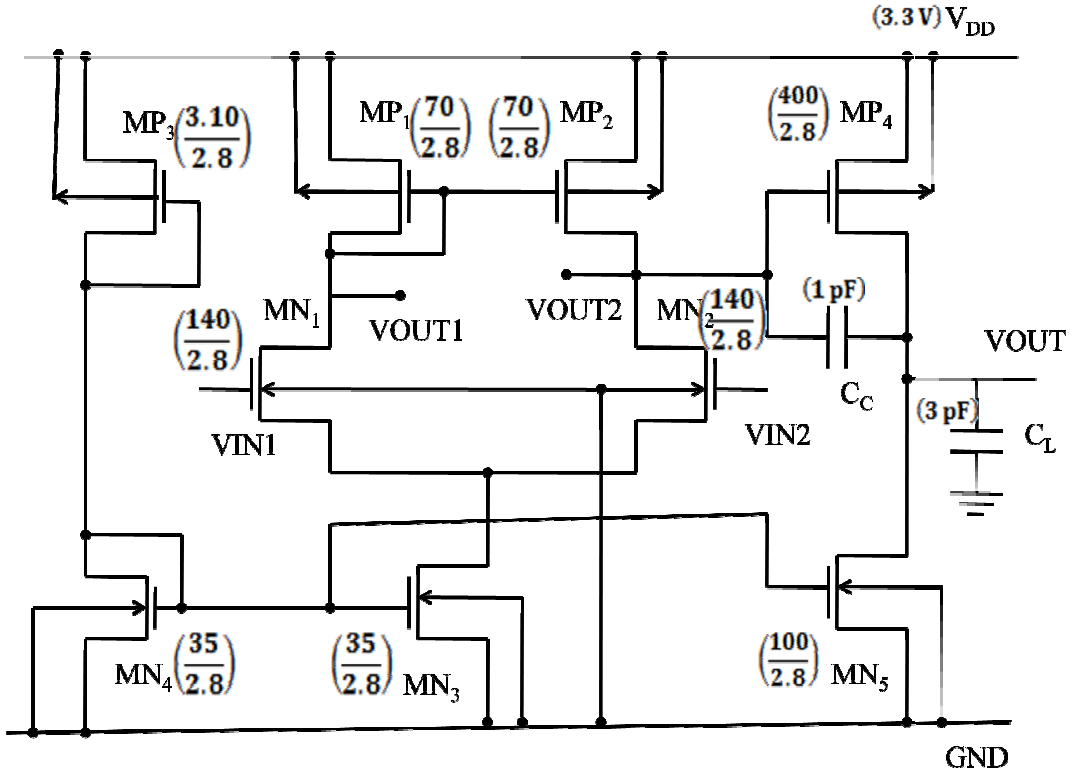


Fig 3.7 A Two Stage CMOS Operational Amplifier

The first stage in Fig 3.7 consists of a n-channel differential pair MN_1-MN_2 with an p-channel current mirror load MP_1-MP_2 and a n-channel tail current source MN_3. The second stage consists of an n-channel common-source amplifier MN_5 with a p-channel current-source load MP_4. The high output resistances of these two transistors equate to a relatively large gain for this stage and an overall moderate gain for the complete amplifier. Because the op-amp inputs are connected to the gates of MOS transistors, the input resistance is essentially infinite when the amplifier is used in internal applications.

The sizes of the transistors were designed for a bias current of 30μA to provide for sufficient output voltage swing, output-offset voltage, slew rate, and gain-bandwidth product.

The following design procedure assumes that specifications for the following parameters are given, (a) Gain at dc, $A_V(0)$ (b) Gain bandwidth, GB (c) Input common-mode range (ICMR), (d) Load capacitance, C_L (e) Slew rate, SR (f) Output voltage swing (g) Power dissipation, P_d.

The design procedure begins by choosing a device length to be used throughout the circuit. This value will determine the value of the channel length modulation parameter λ, which will be a necessary parameter in the calculation of amplifier gain. Having chosen the nominal transistor device length, one next establishes the minimum value for the compensation capacitor C_C. It is given by,

$$C \quad > \quad \frac{2.2}{10} \quad C \tag{3.9}$$

The minimum value for the tail current I_{MN3} based on slew-rate requirements is given by,

$$I \qquad = \mathrm{SR}(C\ ) \tag{3.10}$$

The aspect ratio of MP_1 can now be determined by using the requirement for positive input common-mode range. It is given by,

$$S \quad = \quad \frac{W}{L}$$

$$= \frac{I}{(K \quad)[V \quad - V \quad (\max) - |V \qquad |(\max) + V \quad (\min)]} \tag{3.11}$$

If the value determined for S_{P1} is less than one, then it should be increased to a value that minimizes the product of W and L. this minimizes the area of the gate region, which in turn reduces the gate capacitance.

Requirements for the Transconductance of the input transistors can be determined from knowledge of C_C and GB. The Transconductance g_{mN1} can be calculated using the following equation,

$$g \qquad = \mathrm{GB}\,(C\ ) \tag{3.12}$$

The aspect ratio S_{N1} is directly obtainable from g_{mN1} as shown below,

$$S \quad = \quad \frac{W}{L} \quad = \frac{g}{(K \quad)(I \quad)} \tag{3.13}$$

And V_{DSN3} is given as,

$$V \quad = V \quad (\min) - V \quad - \frac{I}{\beta} \quad - V \quad (\quad) \tag{3.14}$$

The aspect ratio S_{N3} can be calculated as,

$$S \quad = \quad \frac{W}{L} \quad = \frac{2(I \quad)}{K \quad (V \quad)} \tag{3.15}$$

At this point, the design of the first stage of the op amp is complete.

For a phase margin of 60°, the location of the output pole is assumed to be placed at 2.2 times GB. Based on this assumption transconductance g_{mP4} can be determined as,

$$g \quad = 2.2(g \quad) \frac{C}{C} \tag{3.16}$$

To complete the design of MP_4, first is to achieve proper mirroring of the first stage current mirror load (i.e., MP_1 and MP_2). This requires that $V_{SGP2} = V_{SGP4}$.

$$S \quad = S \quad \frac{g}{g} \tag{3.17}$$

Knowing g_{mP4} and S_{P4} will define the dc current I_{MP4} using the following equation,

$$I \quad = \frac{g}{(2)(K \quad) \frac{W}{L}} = \frac{g}{2K \quad S} \tag{3.18}$$

The device size of MN_5 can be determined from the balance equation given bellow,

$$S \quad = \quad \frac{W}{L} \quad = \quad \frac{W}{L} \quad \frac{I}{I} \quad = S \quad \frac{I}{I} \tag{3.19}$$

At this point in the design procedure, the total amplifier gain of the two stage CMOS operational amplifier is given by,

$$A \quad = \frac{(2)(g \quad)(g \quad)}{I \quad (\lambda \quad + \lambda \quad)I \quad (\lambda \quad + \lambda \quad)} \tag{3.20}$$

If the gain is too low, a number of things can be adjusted (like aspect ratios of transistors, drain currents, inverter, inverter load etc.) to get improved gain.

3.4.2 Current Mirrors

Current mirrors are used extensively in MOS analog circuits both as biasing elements and as active loads to obtain high AC voltage gain [34-35]. Enhancement mode transistors remain in saturation when the gate is tied to the drain, as the drain-to-source voltage (V_{DS}) is greater than the gate-to-source voltage (V_{GS}) due to the threshold voltage (V_{th}) drop, i.e.,

$$V \quad \geq V \quad - V \tag{3.21}$$

Based on Eq. (3.21), constant current sources are obtained through current mirrors designed by passing a reference current through a diode-connected (gate tied to drain) transistor.

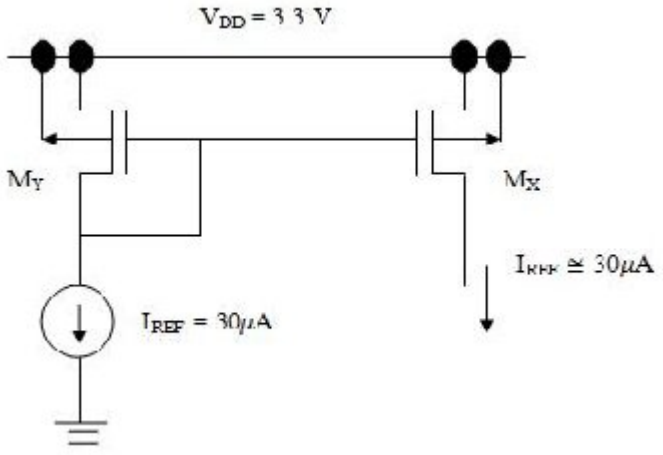


Fig 3.8(a) p-MOS Current Mirror

Fig 3.8(a) and (b) show the p-MOS and n-MOS current mirrors design. A p-MOS mirror serves as a current source while the n-MOS acts as a current sink. The voltage developed across the diode-connected transistor is applied to the gate and source of the second transistor, which provides a constant output current. Since both the transistors have the same gate to source voltage, the currents when both transistors are in the saturation region of operation, are governed by the following equation (3.22) assuming matched transistors. The current ratio I_{OUT}/I_{REF} is determined by the aspect ratios of the transistors. The reference current that was used in the design is 30µA. The desired output current is 30µA. For the p-MOS current mirror, it can be written as,

$$\frac{I}{I} = \frac{\frac{W}{L}}{\frac{W}{L}} \tag{3.22}$$

For $(W_X/ L_X) = (W_Y/ L_Y)$,

$$I_{OUT} = 1 \times I_{REF} = 30\ \mu A \tag{3.23}$$

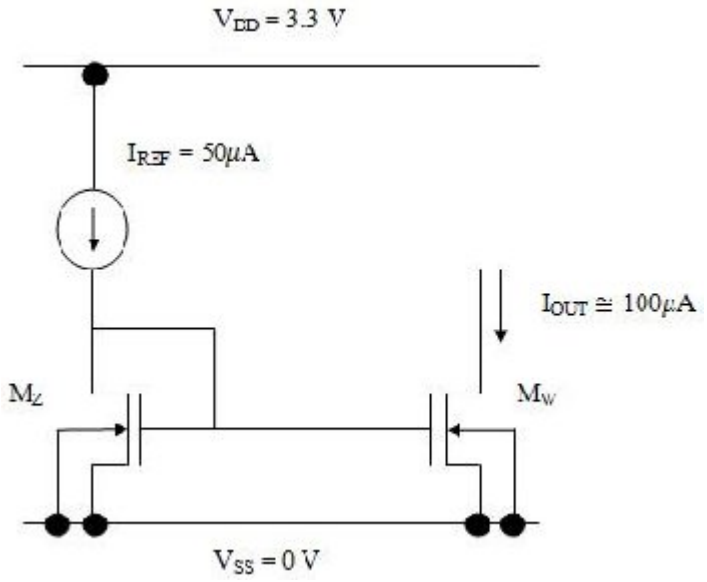


Fig 3.8(b) n-MOS Current Mirror

Hence for identical sized transistors, the ratio is unity, which means that the output current mirrors the input current. Because the physical channel length that is achieved can vary substantially due to process variations, the accurate ratios usually result when devices of the same channel length are used, and the ratio of currents is set by the channel width. For the n-MOS current mirror design shown in Fig 3.8(b),

$$\frac{I}{I} = \frac{\frac{W}{L}}{\frac{W}{L}} \tag{3.24}$$

For $(W_W/ L_W) = 2 \times (W_Z/ L_Z)$,

$$I_{OUT} = 2 \times I_{REF} = 2 \times 50\ \mu A = 100\ \mu A \tag{3.25}$$

3.4.3 Active Resistors

There are two active resistors used in the design. Firstly, the reference current that is applied to the current mirror is obtained by means of an active resistor. The resistor here

is obtained by simply connecting the gate of a MOSFET to its drain as shown in Fig 3.9(a). This connection forces the MOSFET to operate in saturation in accordance with the equation,

$$I \quad = \{\beta\,(V \quad - V \quad)\ \}/\,2 \qquad (3.26)$$

Where β is the transconductance parameter, V_{th} is the threshold voltage and V_{GS} is the gate-source voltage. Since the gate is connected to the drain, current I_{DS} is now controlled directly by V_{DS} and therefore the channel transconductance becomes the channel conductance. The small signal resistance is given by

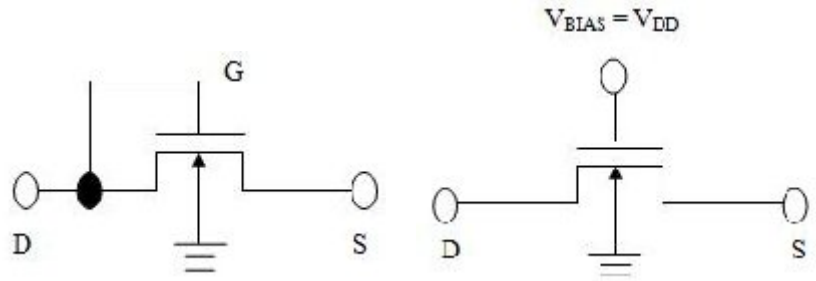
$$r \quad = \frac{r}{(1 + g \quad r \quad)} \cong \frac{1}{g} \qquad (3.27)$$

where g_m is the transconductance of the MOS transistor. It is described by the following equation.

$$g \quad = \frac{\delta I}{\delta V} \qquad = \quad \overline{2\beta I} \qquad (3.28)$$

It is to be noted that the trans-conductance of a MOS increases as the square root of the drain current. Hence, MOS amplifiers need several stages to achieve large gains.

The second active resistor shown in Fig 3.9(b) has been used to realize the nulling resistance to reduce the effects of the right hand plane zero in the transfer function. The gate of this transistor M_K is biased at V_{DD}. Its small signal output resistance is obtained from equation (3.27).



(a) **(b)**

Fig 3.9 Active Resistors(a) Gate Connected to Drain and (b) Gate Connected to V_{DD}

The NMOS differential pair needs to be biased by a constant current source, which is provided by the 30μA current source. The same current is supplied to the two stages of

the operational amplifier by the n-channel current mirrors MN_3, MN_4, MN_5 which provide the bias current for the two stages. In the differential amplifier stage, differential amplification is accomplished and differential to single-ended conversion is done. Thus, the output is taken only from one of the drains of the transistors. The p-channel devices MP_1 and MP_2 which are the load for the n-channel devices, also aid in the single-ended conversions. The second stage provides the additional gain. It is once again biased by a current source, which is also used to maximize the gain of the second stage. To get a high gain with reasonable high output resistance, the minimum channel length used is 2.8μm and the maximum width of the transistor used is 400μm. Transistor MP_4 is critical to the frequency response, is biased at I_{MP4} =- 90μA and has $(W/L)_{P4} = (W/L)_{max} \cong 143$. The second stage is biased at $I_{MN5} \cong 90\mu A$ to avoid input offset voltage. Transistors MP_1 and MP_2 are dimensioned according to,

$$\frac{\frac{W}{L}}{2\ \frac{W}{L}}_{,} = -\frac{I}{I} = \frac{90\ \mu A}{30\ \mu A} = 3$$

$$\frac{W}{L}_{,} = \frac{1}{6}\ \frac{W}{L} \cong 23.80 \qquad (3.29)$$

Choose the smallest device length that will keep the channel modulation parameter constant and give good matching for current mirrors. The channel length is chosen to be L=2.8μm. Therefore, W ≅ 70μm for the transistors MP_1 and MP_2. To obtain the bias current of 15μA, a MOS transistor is used with appropriate value of width (which is the MOSFET simulating resistors). Large W/L ratios for the transistors in the operational amplifier are obtained by using the following technique. Multiple numbers (n) of transistors are connected in such a way that the effective W/L ratio is n times the W/L ratio of each transistor. In present design, n=6 for transistors MP_1 and MP_2, and n=32 for transistor MP_4. The technique reduces the required area, in comparison to a device laid out in a straight forward manner. The benefit of this technique is reduced junction capacitance, and is well characterized [34]. The simplicity, modularity and predictability of the device overcome the penalty of associated area.

Chapter-4

I_{DDQ} TESTING OF TWO STAGE CMOS OPERATIONAL AMPLIFIER

I_{DDQ} Testing is a method for testing CMOS ICs for the presence of manufacturing faults. It relies on measuring the supply current (I_{DD}) in the quiescent state. This chapter discusses important physical defects commonly seen in the design of CMOS circuits and I_{DDQ} testing. It also describes the design and implementation of BICS used to detect faults in a two stage CMOS operational amplifier.

4.1 Physical Defects

In CMOS technology, the most commonly observed physical failures are bridges, opens, stuck-at-faults and gate oxide shorts (GOS). These defects create indeterminate logic levels at the defect site [36]. Very large-scale integrated circuits processing defects cause shorts or break in one or more of the different conductive levels of the device [37]. This section discusses the physical defects that cause an increase in the quiescent current.

4.1.1 Open Faults

Analysis of physical defects from fabs as well as Inductive Fault Analysis suggests that approximately 40% defects are open. Open defects are much more difficult to detect by logic testing. Also, I_{DDQ} testing does not necessarily detect them. Examples of open defects include line open, line thinning (it may or may not be a partial open at the time of testing), resistive vias, open vias, etc.

Logic gate inputs that are unconnected or floating inputs are usually in high impedance or floating node-state and cause elevated I_{DDQ} [38]. Fig 4.1 shows a 2-input NAND with open circuit defects. Node V_N is in the floating node-state caused due to an open interconnect. For an open defect, a floating gate may assume a voltage because of parasitic capacitances and cause the transistor to be partially conducting. Hence, a single floating gate may not cause a logical malfunction. It may cause only additional circuit delay and abnormal bus current [38]. In Fig 4.1, when the node voltage (V_N), reaches a steady state value, then the output voltage correspondingly exhibits a logically stuck behavior and this output value can be weak or strong logic voltage. Open faults, however, may decrease or may cause only a small rise in I_{DDQ} current, which the off-chip

current sensor may not detect because of its low-resolution. It can be detected using Built in current sensors (BICS).

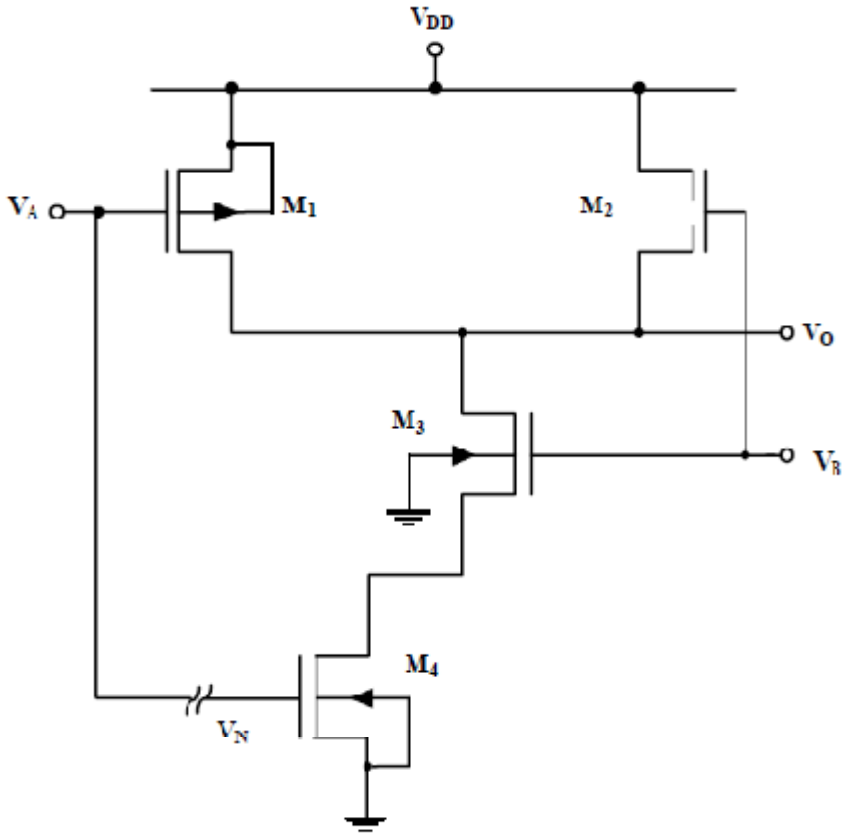


Fig 4.1 Floating Input and Open FET – Open Circuit Defects

An open source or open drain terminal in a transistor may also cause additional power-bus current for certain input states. Another open fault shown in Fig 4.1 is an open FET (M_2). In the scope of this work, only bridging faults have been dealt for I_{DDQ} testability. I_{DDQ} testing cannot detect some of the opens which result in decrease of the quiescent current.

4.1.2 Bridging Faults

Bridges can be defined as undesired electrical connections between two or more lines in an integrated circuit, resulting from extra conducting material or missing insulating material. When I_{DDQ} measurements are used, a bridge is detected if the two nets, which comprise it, have opposite logic values in the fault-free circuit [39] and are connected by a bridge due to the introduction of the fault in the circuit. Bridging faults can appear

either at the logical output of a gate or at the transistor nodes internal to a gate. Bridge between the outputs of independent logic gates or an inter-gate bridge can also occur. Bridging fault could be between the following nodes (1) drain and source, (2) drain and gate, (3) source and gate, and (4) bulk and gate. Fig 4.2 shows an example of possible drain to source and gate to source bridging faults in an inverter chain in the form of low resistance bridges R_1 and R_2, respectively. Resistance Bridge, R_3 is an example of inter-gate bridge. Fig 4.3 shows examples of gate to source and gate to drain bridges in an NAND gate circuit. Bridging defect cannot be modeled by the stuck-at model approach, since a bridge often does not behave as a permanent stuck node to a logic value [39]. I_{DDQ} testing using BICS is an effective method of detecting bridging shorts.

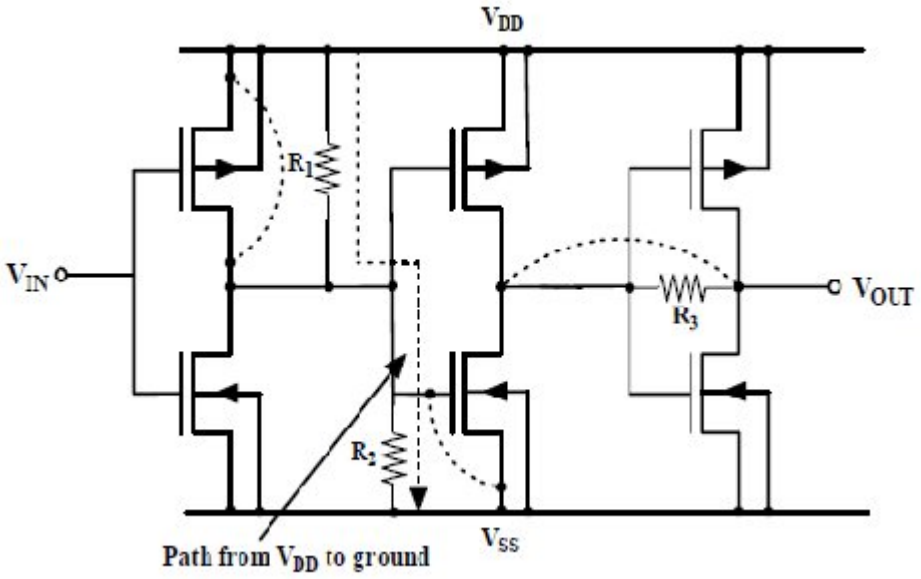


Fig 4.2 Drain-Source, Gate-Source and Inter-Gate Bridging Faults in an Inverter Chain

4.1.3 Gate Oxide Faults

The Gate-oxide defects include pinholes and micro pores, dendrites, trapped charge due to hot-carriers, non-stichiometric Si–SiO_2 interface and direct short to diffusion. Some of these defects occur during the oxidation or other thermal processes, while other defects may occur due to electrostatic discharge or overstress (ESD/EOS). In the majority of cases, gate-oxide defects cause reliability degradation such as change in transistor threshold voltage and increased switching delay, only in some cases (such as avalanche

breakdown and subsequent short) it causes a logical failure. However, in general, logic testing does not detect gate oxide defects, primarily due to difficulty in fault-effect propagation. I_{DDQ} testing, on the other hand, is very effective in detecting these defects as they cause high current dissipation in the circuit.

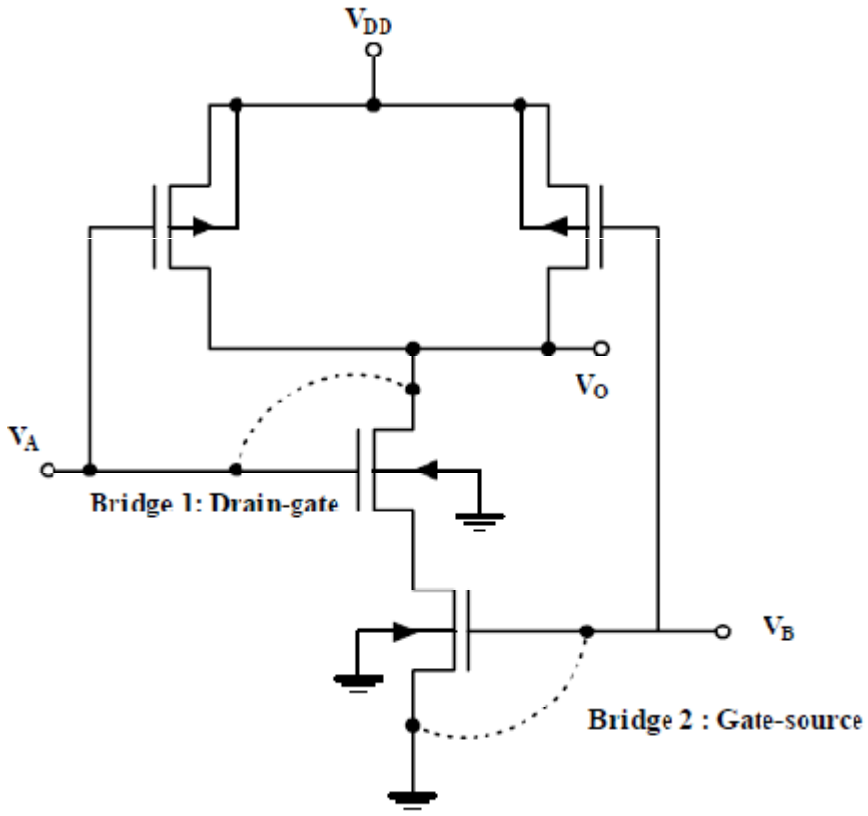


Fig 4.3 Bridging Defects

4.2 I_{DDQ} Testing

I_{DDQ} means quiescent current I_{DD}, or quiescent power supply current. It is power supply current in quiescent state. Quiescent state is that state, when the circuit is not switching and inputs are held at static values. I_{DDQ} testing uses the principle, that there is no static current path between the power supply and ground, except for a small amount of leakage. The presence of faults, under the right conditions, can increase this quiescent current by an order of magnitude which can be used to detect the fault. This testing is little more complex than just measuring the supply current. I_{DDQ} testing of CMOS ICs is very efficient for improving test quality. The test methodology based on the observation of quiescent current on power supply lines allows a good coverage of physical defects

such as gate oxide shorts, floating gates, bridging faults, partial defects (defects that do not affect the logic of circuit, but may affect reliability), some delay faults and some stuck-open faults which are not very well modeled by the classic fault models, or undetectable by conventional logic tests [36, 40]. It has been recognized as the single most sensitive test method to detect CMOS IC defects.

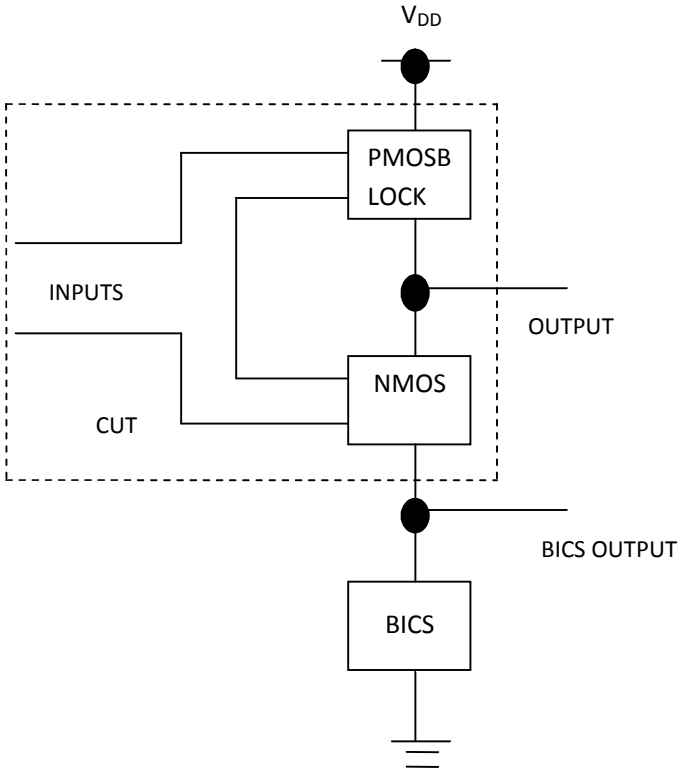


Fig 4.4 Block Diagram of I_{DDQ} Testing

The major advantage of current-based testing is that it does not require propagation of a fault effect to be observed at the output, it requires only exercising the fault model and then measuring the current from the power supply. The fault effect observance is the measurement of current, and the detection criteria are the current flow value exceeding some threshold limit. The current passing through the V_{DD} or GND terminals is monitored during the application of an input stimulus. In the quiescent state the circuit draws a very low current (micro-amp levels), for certain input states this current may raise to an abnormal level due to the presence of defects. Current fluctuations can be monitored using on-chip or off-chip current sensors. On-chip or built-in current sensors (BICS) have speed and resolution enhancements over off-chip current sensors mainly because the large transient currents in the output drivers are by-passed and a few

parasitic are encountered. On-chip current testing is both time efficient and sensitive. Moreover, on-chip current tests can also be used as an on-line testing tool, and is important when components are to be used in high reliability systems. For high speed and high sensitivity, unaffected by large pad currents, a fast built-in current testing circuit is desired [38]. In the present work, a simple design of a built-in current sensor is presented to detect bridging faults in a two-stage CMOS amplifier circuit. A simple method for the fault injection has been used to simulate physical defects present in a chip.

The block diagram of the I_{DDQ} testing with BICS is shown in Fig 4.4. Essentially, I_{DDQ} testing technique adds a BIC sensor in series with V_{DD} or GND lines of the circuit under test. A series of input stimuli is applied to the device under test while monitoring the current of the power supply (V_{DD}) or ground (GND) terminals in the quiescent state conditions after the inputs have changed and prior to the next input change [41]. Typically, sub threshold current in the transistors, which are 'off' in a CMOS static circuit should be negligibly small. However, in some cases, due to charge presence in a gate oxide or latch-up, the sub-threshold current may be large enough to become an essential component of I_{DDQ}. The BICS can be designed to detect this current also.

4.2.1 I_{DDQ} Testing of Fault Inverter

Ideally, in a static CMOS circuit, quiescent current should be zero except for associated p-n junction leakage currents. Any abnormal elevation of current should indicate presence of defects. To assure low stand-by power consumption, many CMOS integrated circuit manufacturers include I_{DDQ} testing with other traditional DC parametric tests.

Fig 4.5 shows how an I_{DDQ} test can identify defects. The current in static CMOS is not constant during transient. When an output transition occurs, a peak of I_{DDQ} current is observed. This peak is due to charging and discharging of the load capacitance at the output circuit and corresponds to the short circuit. When the transition is completed, the circuit is in the quiescent state. I_{DDQ} is very sensitive to physical faults in the circuit.

Let us evaluate current testing in CMOS circuits in the presence of bridging faults. Two nodes connected by a bridge must be driven to opposite logic levels under fault-free conditions for bridging fault to occur. In Fig 4.5, a typical bridge is one between the node V_{O1} and V_{DD}. To detect this defect, input pattern must drive the node V_{O1} to the logic

low value (‘0’), as this node is assumed to be bridged with the power rail. Thus, a path from power to ground appears allowing the existence of an abnormal high I_{DDQ} current. I_{DDQ} value is directly dependent on the resistance offered by the conducting path and hence on the size of the transistors in the conducting path.

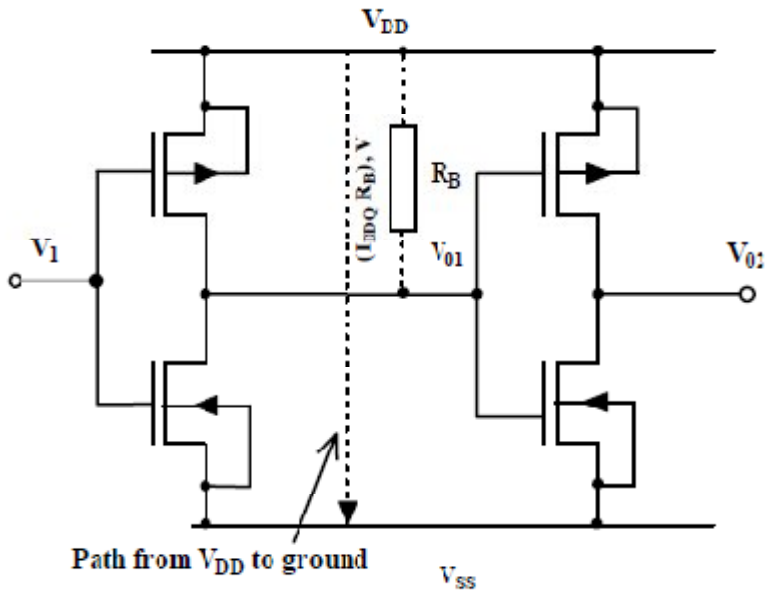


Fig 4.5 Bridging Fault Causing $I_{DDQ}R_B$ Drop and a Path to the Ground

The presence of the physical fault causing the high abnormal current can be effectively detected by I_{DDQ} testing using BICS. A set of realistic bridges have been modeled between adjacent metal lines in a two-stage CMOS amplifier circuit at three different (conducting levels), to examine the effect on the value of I_{DDQ} and detect the presence of the fault using the BICS.

4.3 Design and Implementation of the BICS

Different BICS (Built in current sensors) schemes are there for detection of the abnormal I_{DDQ} current and the physical faults commonly observed. While most BICS designs concentrate on mere detection of the fault, some can detect the location of the fault as well. The entire design is divided into n sub-blocks (SB) where n equals the number of outputs. The divided SB’s are checked individually through their corresponding output and a faulty area is easily detected by observing the outputs. The performance impact of a BICS on a circuit under test (CUT) is the key issue to be considered when designing BICS. Insertion of the BIC sensor between CUT and GND involves series voltages, and

these voltages could degrade the performance of the CUT. A large number of earlier BICS are based on voltage amplifiers such as differential amplifiers or sense amplifiers. The stability of the BICS is limited in this case since the quiescent point (Q-point) of an amplifier may not be stable and can vary with the change of dc supply voltage, V_{DD}. The detection time and hardware overhead is increased due to the extra hardware required to stabilize the Q-point.

Characteristics required for a good BIC sensor are,

(a). Detection of abnormal static and dynamic characteristics of the CUT.

(b). Minimal disturbance of the static and dynamic characteristics of the CUT.

(c). The design should be simple and compact to minimize the additional area necessary to build it.

(d). The I_{DDQ} test should have good resolution and speed.

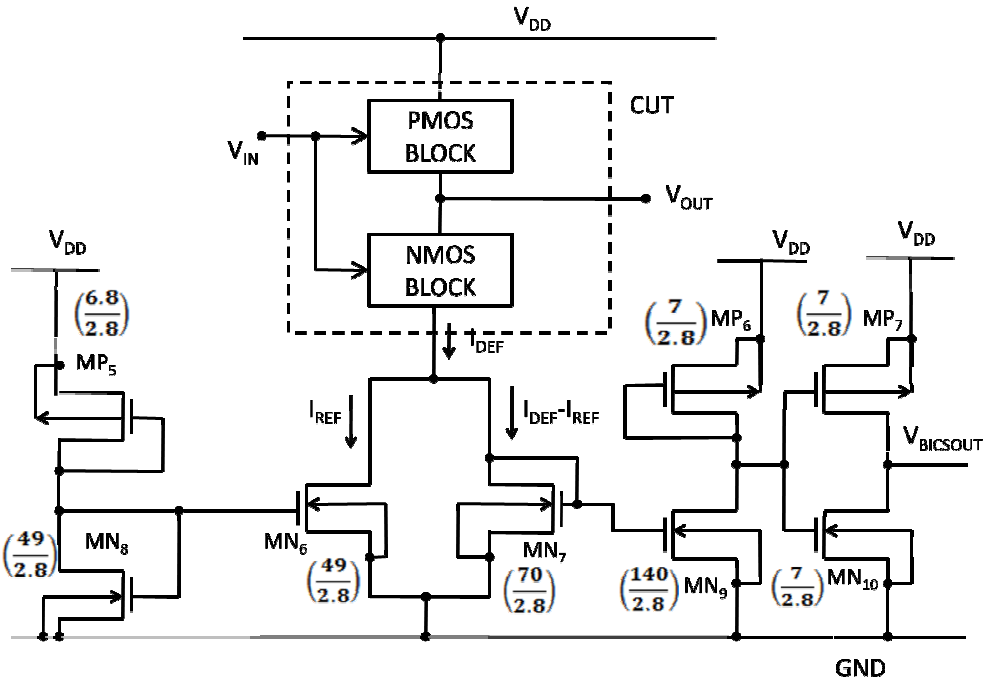


Fig 4.6 CMOS Built in Current Sensor Circuit with the Circuit under Test

To overcome problems of slow detecting time, resolution, instability of the BICS and large impact on the CUT performance, the current-mode circuit design approach has been adopted using a single power supply. In this work, simple design of a BICS employing current mirrors and current differential amplifier has been used. It has minimum area over head in the chip and no impact on over all performance. A simple

design of a BIC sensor built into the two-stage operational amplifier is presented using the current mode design. It determines whether the circuit quiescent current is below or above a threshold level.

The CMOS circuit diagram of the built-in current sensor with the CUT is shown in Fig 4.6. It consists of a current differential amplifier (MN_6, MN_7) and two current mirror pairs (MN_6, MN_8 and MN_7, MN_9). The n-MOS current mirror (MN_6, MN_8) is used to mirror the current from the constant current source which is used as the reference current I_{REF} for the BICS. I_{REF} is the current coming from the CUT when there is no fault present. The current mirror (MN_7, MN_9) is used to mirror the difference current (I_{DEF} - I_{REF}) to the current inverter, which acts as a current comparator. (I_{DEF} - I_{REF}) is the amount of current increased in the CUT due to the presence of fault. The differential pair (MN_6, MN_7) calculates the difference current between the reference current I_{REF} and the defective current I_{DEF} from the CUT. The W/L size of the n-MOS current mirror (MN_6, MN_8) is set to 49/2.8. The size of MN_7 is set to 70/2.8 and MN_9 is set to 140/2.8. Therefore $I_{MN7} = I_{DEF}-I_{REF}$. The constant reference current is set to approximately the same value as the quiescent state current when the CUT is fault free. In the present design, the reference current, I_{REF} is set to 150μA. The output inverter buffer has an aspect ratio $((W/L)_P / (W/L)_N)$ of 1/1 to counter capacitive parasitic at the output node and detect the presence of the physical fault through the PASS/FAIL flag($V_{BICSOUT}$) at the output.

The BICS is inserted in series with GND of the circuit under test. During the testing the I_{DDQ} current from the CUT is flows into the BICS and the n-MOS current mirror pair replicates the reference current to the current differential amplifier which assigned a value nearly same as the fault-free current. This mirrored reference current is compared with defective current I_{DEF} current coming from the CUT. The output of the current comparator, which is in the form of PASS/FAIL, will detect the presence of the fault. The difference current is converted to a voltage by mirroring it and getting the drop of V_{DS} across the transistor MN_9. If the difference current is large, then it turns-on MN_9 heavily and forces its output node pulled-down to logic ‘0’. This low voltage is applied to CMOS inverter, it shows PASS/FAIL ($V_{BICSOUT}$) output ‘1’, indicating presence of defects in CUT. If the difference current is small, then it is unable to turn on MN_9, and output node is pulled up to logic ‘1’. This high voltage is applied to inverter, which shows PASS/FAIL ($V_{BICSOUT}$) output ‘0’, indicating absence of defects in the CUT.

4.4 Fault Models, Simulation and Detection

For analog CMOS circuits, faults can be classified into either catastrophic or parametric. Research results claim that 80- 90% of observed analog faults are catastrophic faults which consist of shorts or opens in diodes, transistors, resistors and capacitors. Moreover, the yield losses in CMOS process are primarily due to catastrophic faults [18]. It is known that when 100% of catastrophic faults are detected by a test method, the majority of parametric faults depending on the deviation value of the parametric faults can also be detected. As parametric faults are concerned, a tolerance band of ±5% is used. This implies that if the values of parameters to be observed in the testing process appropriate to particular faults are within the tolerance band, these faults will be considered as tolerable and cannot be detected.

The primary reason for a fault is a defect in the integrated circuit. A manufacturing defect causes unacceptable discrepancy between its expected performance at circuit design and actual IC performance after physical realization [38]. A defect may be any spot of missing or extra material that may occur in any integrated circuit layer. Two nodes are connected if there is at least one path of conducting transistors between them. If the two nodes are at opposite potentials under fault-free conditions, a conducting path between them will increase the I_{DDQ} current due to fault in the circuit. After transient switching, each node in a digital circuit is one of the following four states,

(a). V_{DD} state: This state occurs when the node is connected to V_{DD}.

(b). GND state: This state occurs when the node is connected to GND.

(c). Z state: The high-impedance state occurs when the node is neither V_{DD} nor GND connected.

(d). X state: This state occurs when the node is both V_{DD} and GND connected [38].

The ‘X’ state should never occur in fault-free CMOS integrated circuits. Many defects cause an X state to occur in CMOS integrated circuits. Thus, we can view testing as a way to detect the X state, which causes detectable abnormal steady state current.

In this work, fifteen faults are injected in the CUT (Two Stage CMOS Op-amp), eight faults are bridging faults and seven faults are open faults (Fig 4.7). Bridging faults MN_4 drain-source short (defect 1-MN4DSS), MN_5 drain-source short (defect 2-MN5DSS),

MN_5 gate-drain short (defect 3-MN5GDS), MP_4 drain-source short (defect 4-MP4DSS), MP_4 gate-drain short (defect 5-MP4GDS), MN_3 drain-source short (defect 6-MN3DSS), MN_3 gate-drain short (defect 7-MN3GDS) and MP_3 drain-source short (defect 8-MP3DSS) are introduced in the CMOS operational amplifier. Here, defect 6(MN3DSS) and defect 8(MP3DSS) show an increase in quiescent current and hence they are I_{DDQ} testable.

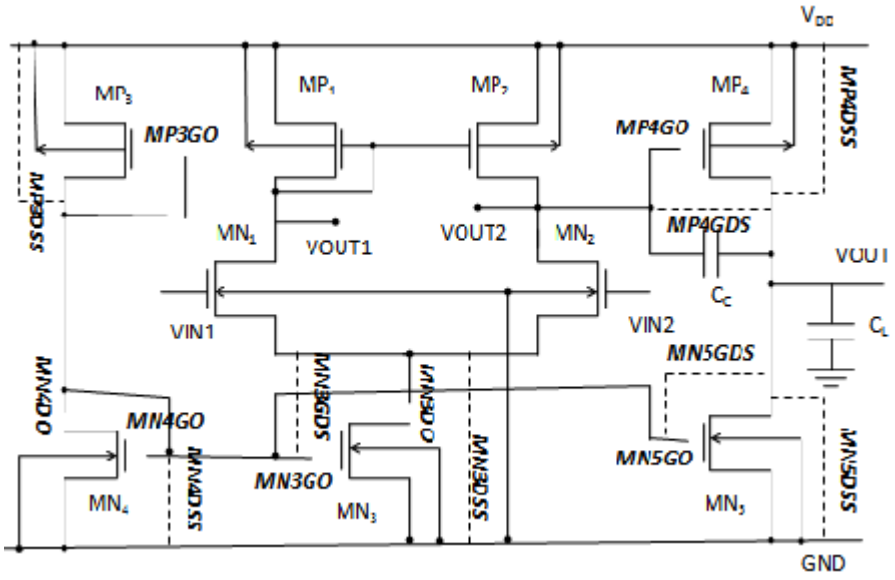


Fig 4.7 Two Stage CMOS Op-amp with Fifteen Injected Faults

Open circuit faults MN_3 gate open (defect 9-MN3GO), MN_4 gate open (defect 10-MN4GO), MP_3 gate open (defect 11-MP3GO), MN_5 gate open (defect 12-MN5GO), MP_4 gate open (defect 13-MP4GO), MN_4 drain open (defect 14-MN4DO) and MN_3 drain open (defect 15-MN3DO) are introduced in the CMOS operational amplifier. Here, defect 10(MN4GO), defect 11(MP3GO) and defect 14(MN4DO) show an increase in quiescent current and hence they are I_{DDQ} testable. The results are presented in the next chapter.

Chapter-5

SIMULATION RESULTS AND LAYOUT

This chapter discusses the simulation results of two stage CMOS operational amplifier with built in current sensor circuit, process corner results, fault detection, fault coverage of I_{DDQ} testing. And also includes layout, LVS report and PEX report.

5.1 Simulated Two Stage Operational Amplifier Results

Two stage CMOS operational amplifier has been designed and simulated in a standard 0.35 um CMOS technology (Sec 3.4.1 and Fig 3.7). The power consumption 495 microwatt and the value of compensation capacitor C_C=1pF. When the input common-mode voltage, V_{icm}, is lower than 0.591V, the NMOS differential pair is off. The input common mode voltage is 1.65 volt.

This design provided a gain of 46dB from first stage and 39dB from second stage making overall gain as 85dB with a common mode rejection of 95.5dB. ICMR is between 0 V to 3.237 V. Unity gain bandwidth obtained was 33.13MHz. Slew rates obtained were 25.926V/uS for positive transition and 18.887V/uS for negative transition. The positive PSRR is 88.72 dB and negative PSRR is 95.15 dB.

5.1.1 AC Response

In Fig 5.1, one method of measuring the AC performance is presented. In this configuration, the amplifier is open loop, and the AC small signal is applied between the V_{i1} and V_{i2} input terminals. Fig 5.2 shows frequency response of operational amplifier.

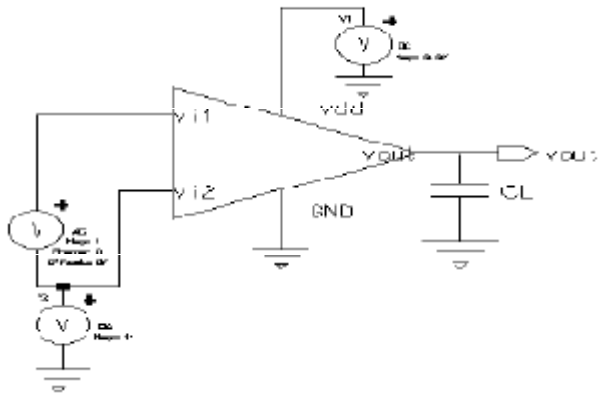


Fig 5.1 Configuration for simulating the open loop frequency response of Op-amp

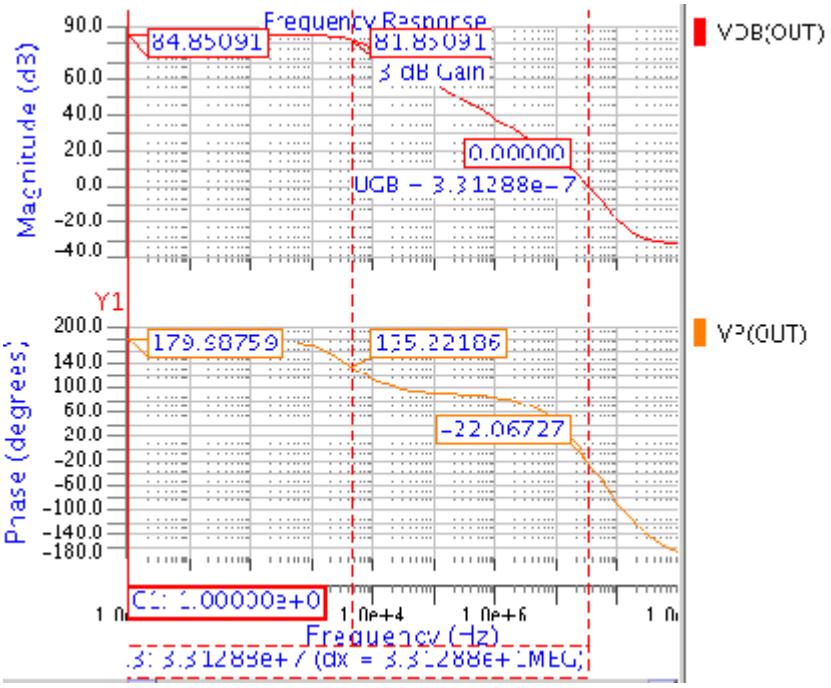


Fig 5.2 frequency response of CMOS Op-amp

5.1.2 Transient Results

A transient simulation of the amplifier in open loop gain configuration with the sinusoidal signal at the input with a 1.65 volt dc bias.

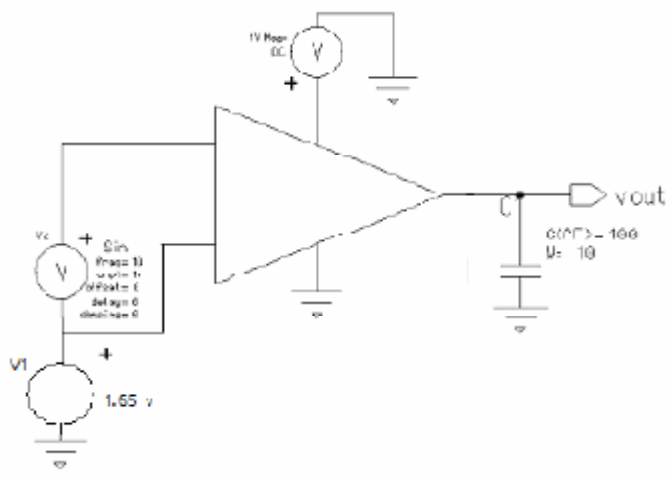


Fig 5.3 Schematic for Simulation of the Transient Response

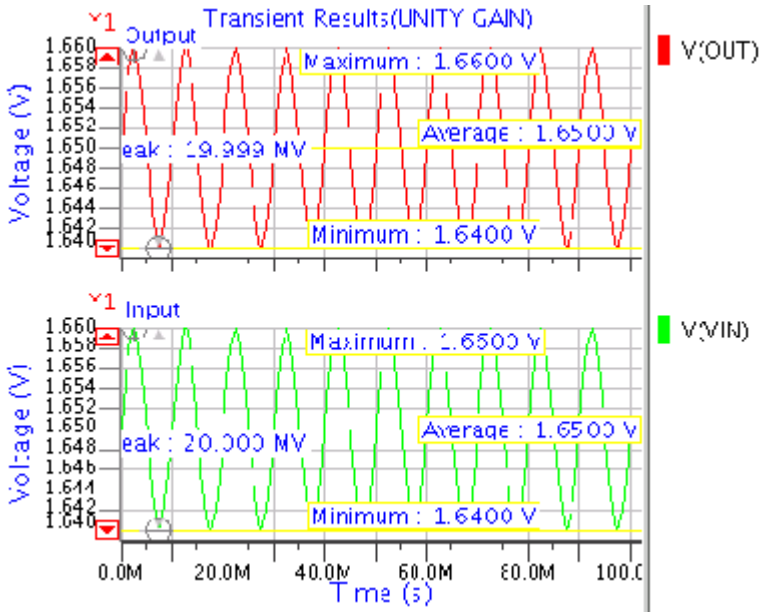


Fig 5.4 Output and Input signals for Transient Analysis(with unity gain)

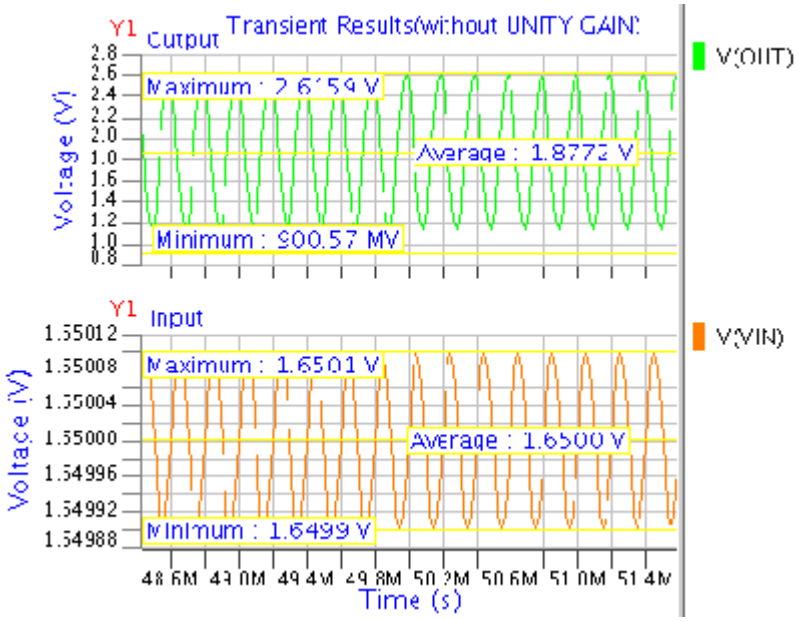


Fig 5.5 Output and Input signals for Transient Analysis(without unity gain)

5.1.3 Step Response In Fig 5.6, a step from ground to V_{DD} is applied at the input with unity feedback configuration. As was measured, the amplifier's slew rate is 25.926 V/us for the rising edge and 18.887 V/us for the falling edge (shown in Fig 5.7).

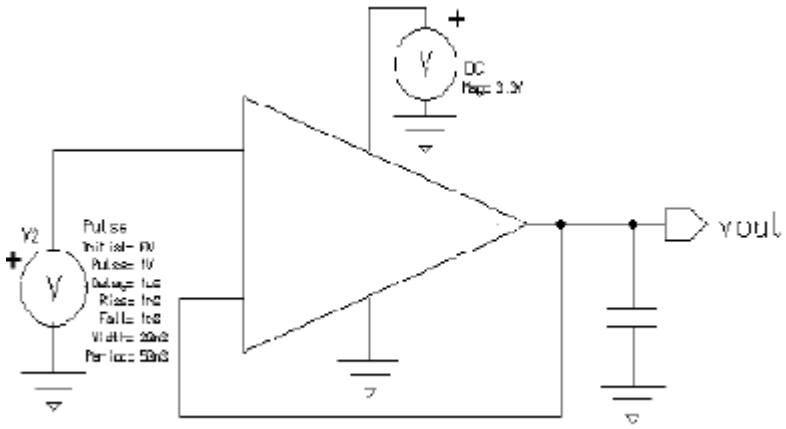


Fig 5.6 Schematic for the Simulation and Measurement of Slewrate

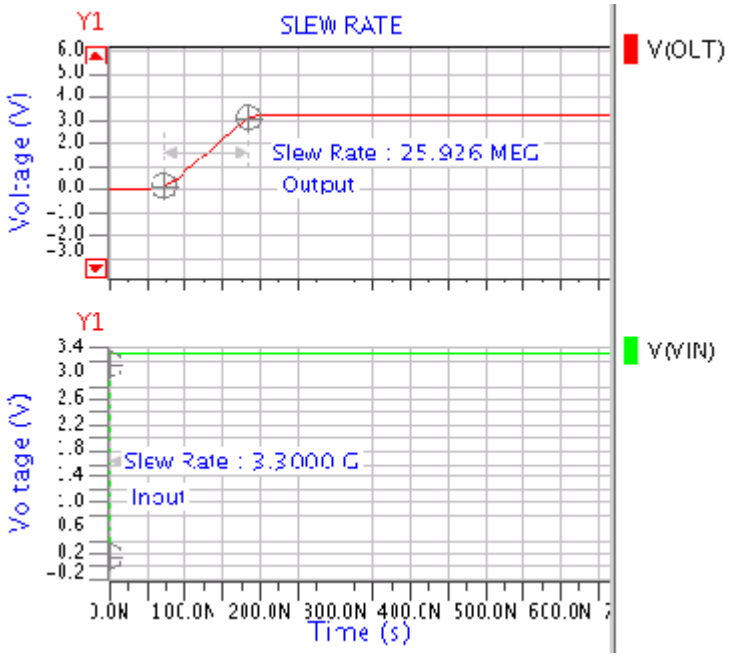


Fig 5.7 Slew rate with Unity Gain configuration

5.1.4 Settling Time

Op-amp is biased as shown in Fig 5.6. Fig 5.8 show settling time for different tolerance values (1% , 5% , 10% etc.,).

For 1% tolerance, settling time is 199.30nS.

For 5% tolerance, settling time is 185.60nS.

For 10% tolerance, settling time is 177.84nS.

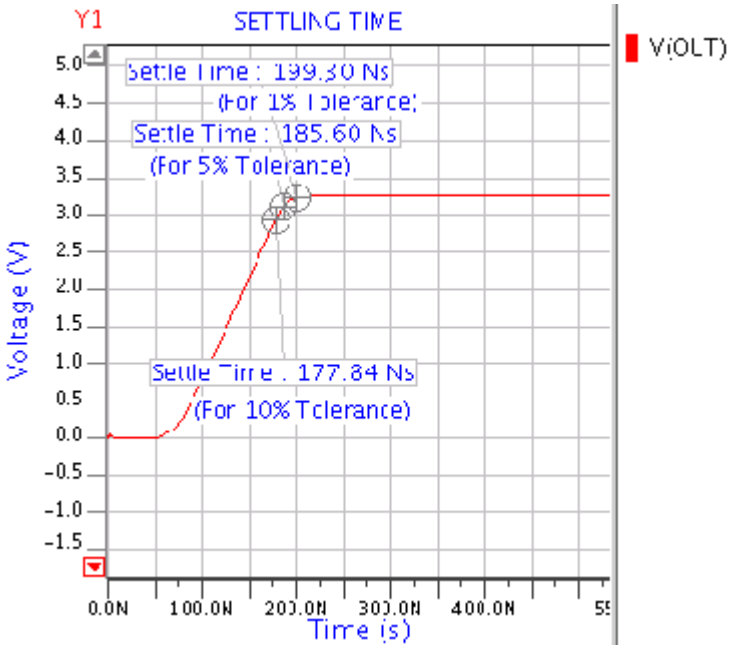


Fig.5.8 Settling time for the different Tolerance values with Unity Gain Configuration

5.1.5 Common Mode Rejection Ratio

In order to simulate common mode rejection, first the common mode gain is calculated. For common mode gain the same ac signal is applied with 1.65 dc bias at both the terminal. The magnitude of ac source is 1 volt. Now measure the output. This is the common mode gain. This gain is now subtracted from the differential mode gain to find the common mode rejection ratio. Fig.5.9 shows biasing for common mode gain.

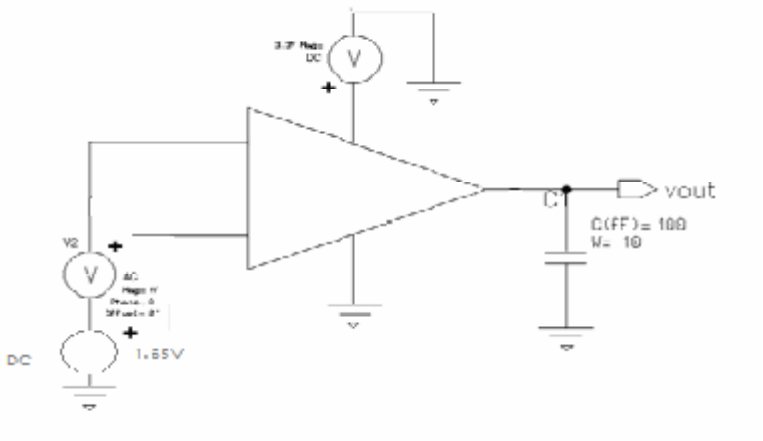


Fig.5.9 Schematic for the Simulation of CMRR

Fig 5.10 and Fig 5.11 show common mode gain and common mode rejection ratio respectively.

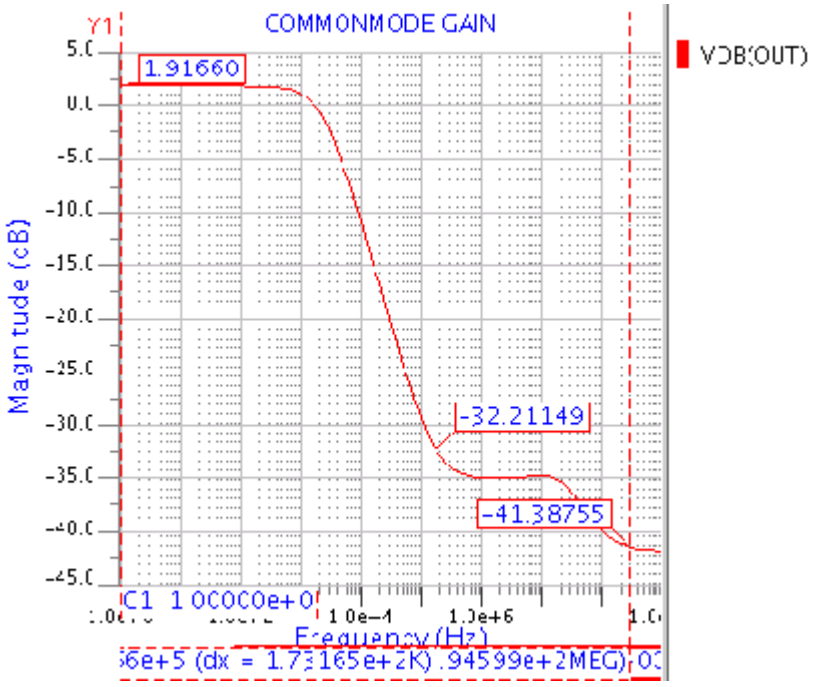


Fig.5.10 Common Mode Gain

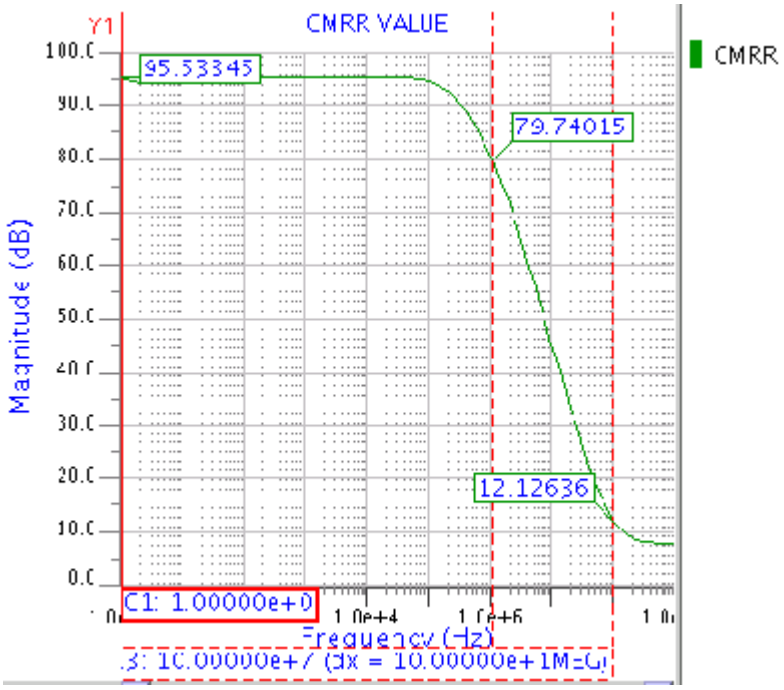


Fig 5.11 Common Mode Rejection Ratio

5.1.6 Power Supply Rejection Ratio

PSRR was measured by placing a 1V AC signal on the power supply where the amplifier is in unity gain feedback configuration. PSRR is equal to the ratio of the AC signal at the output node to the AC signal on V_{DD}. The low frequency positive PSRR is 88.42 dB while negative PSRR is 84.85 dB. At high frequency PSRR decreases.

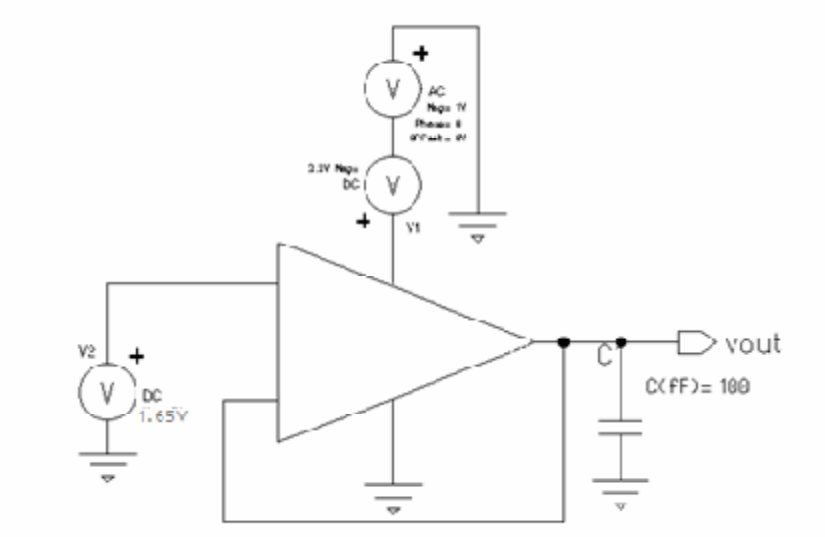


Fig 5.12 Schematic for the Simulation of PSRR

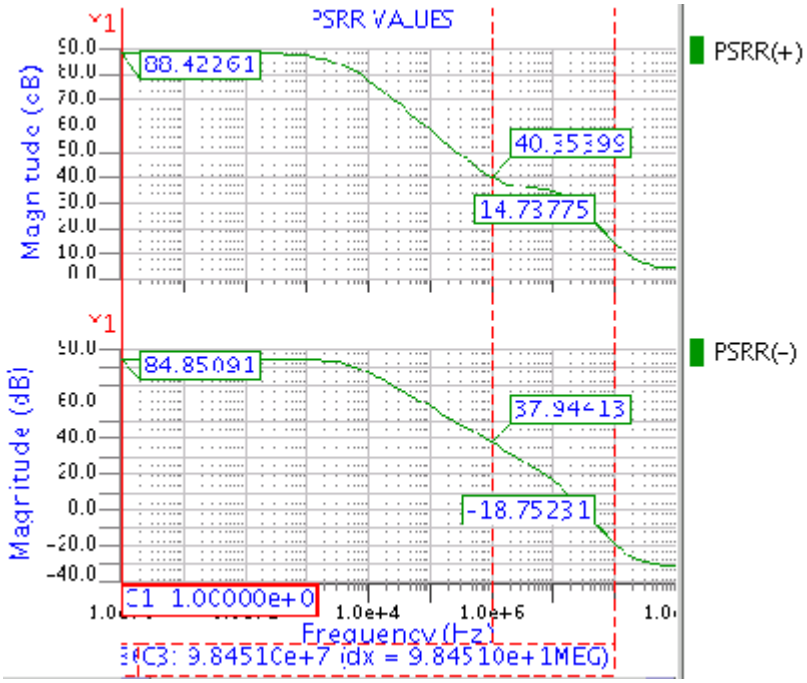


Fig 5.13 Positive and negative PSRR

5.1.7 Input Output Characteristics Using Unity Gain Configuration

For linearity test op-amp is biased in the unity gain follower configuration as shown in Fig 5.14. Now input dc voltage is varied from 0 volt to 3.3 volt. Now the input and output is compared. The op-amp is linear for input for which output match with input.

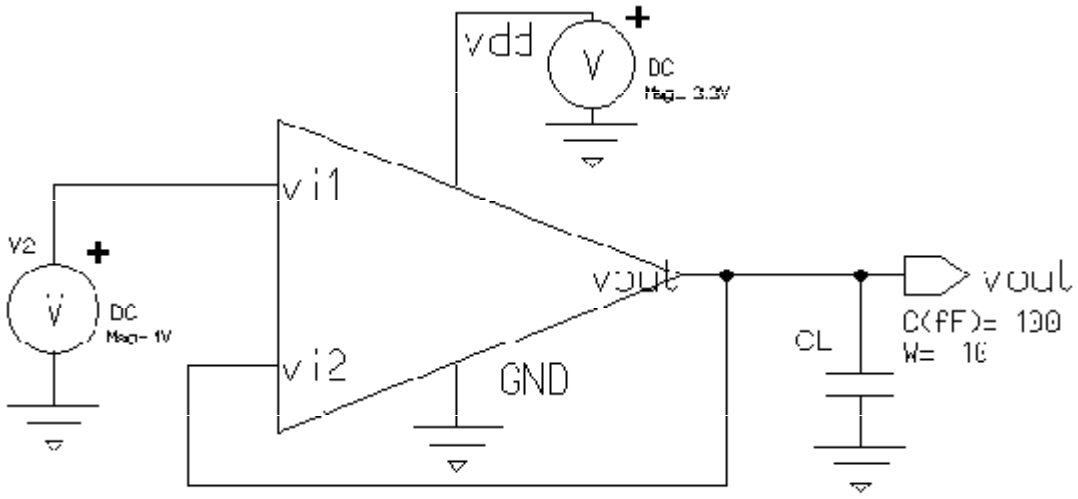


Fig 5.14 Schematic for the Simulation of input Common-mode range

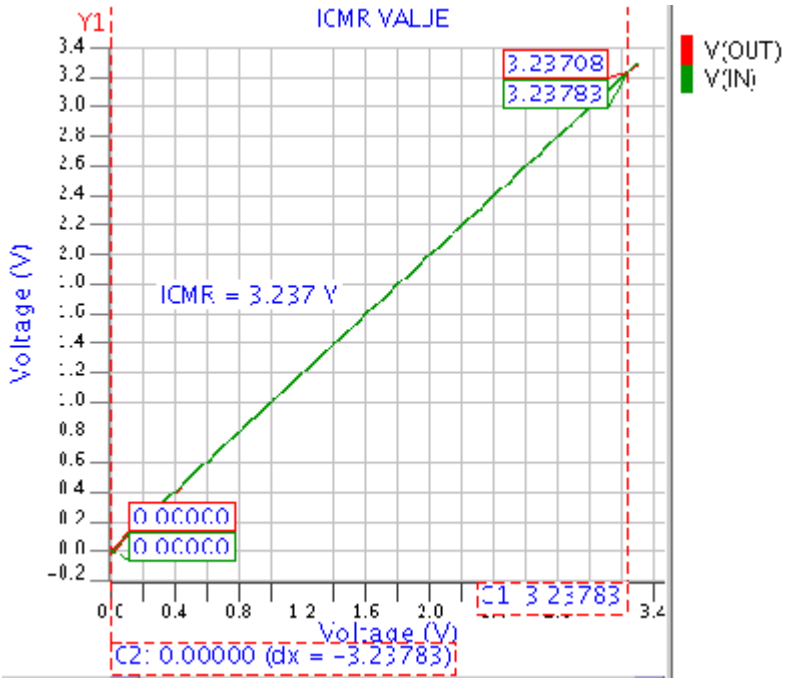


Fig 5.15 Linearity test

5.1.8 Effect of Variation of Compensation Capacitance

The effect of load compensation on frequency response is shown in Fig 5.16.

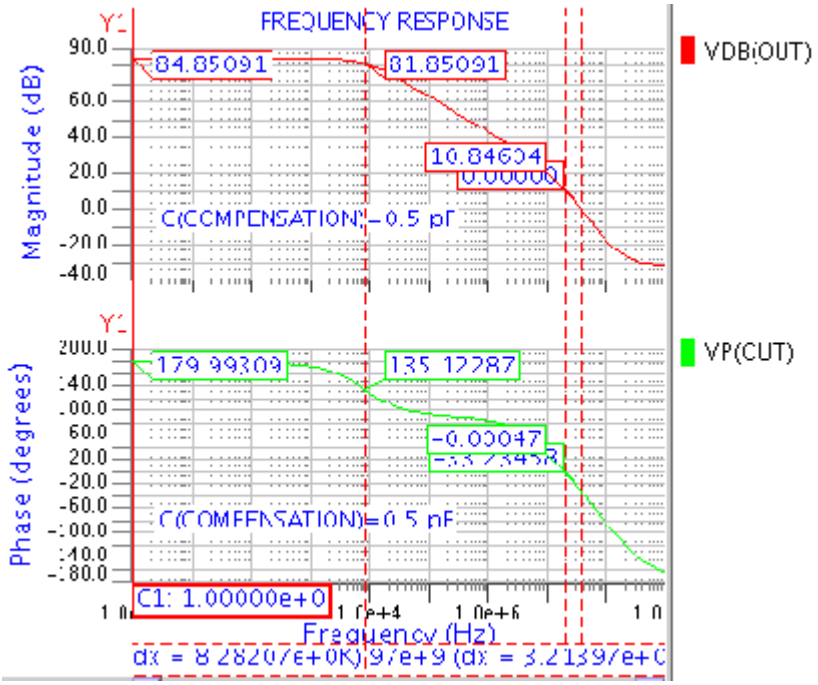


Fig 5.16(a)

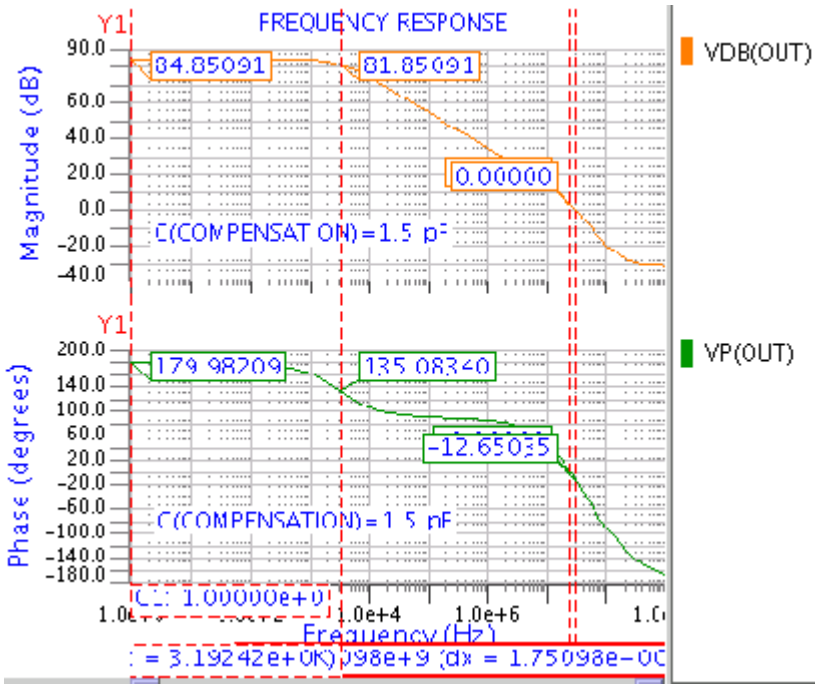


Fig 5.16(b)

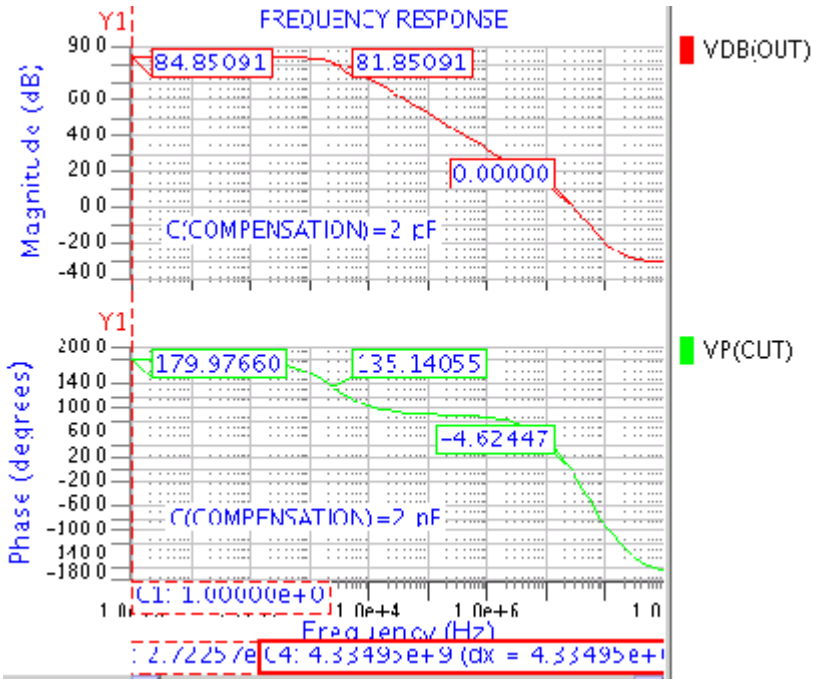


Fig 5.16(c)

Fig 5.16 Frequency Response plot at different compensation capacitance values (a) 0.5 pF (b) 1.5 pF (c) 2.0 pF

The effect of load compensation on common mode gain is shown in Fig 5.17.

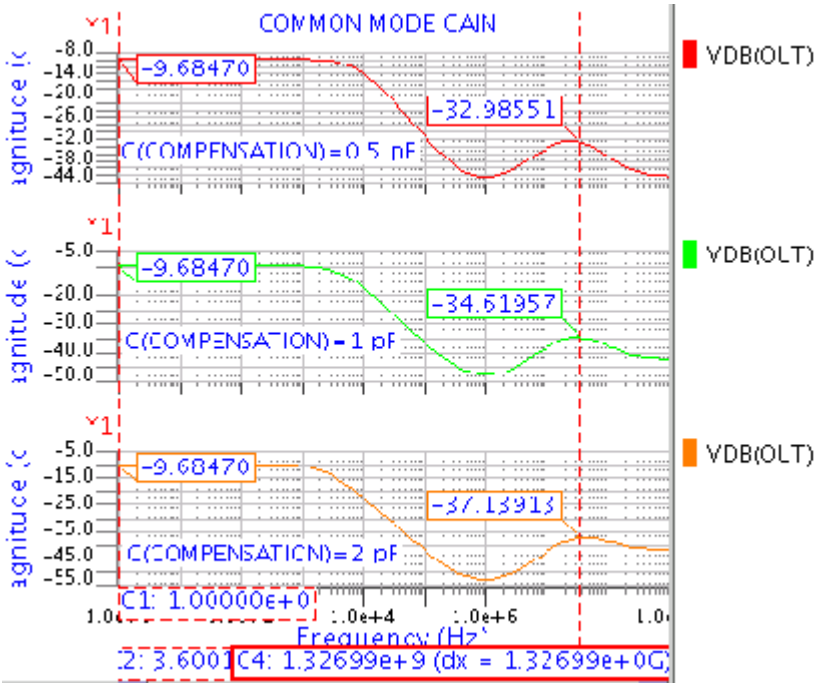


Fig 5.17 Common mode Gain at different compensation capacitance values 0.5 pF, 1.0 pF and 2.0 pF

5.1.9 Effect of Variation of Load Capacitance

The effect of load capacitance on frequency response is shown in Fig 5.18.

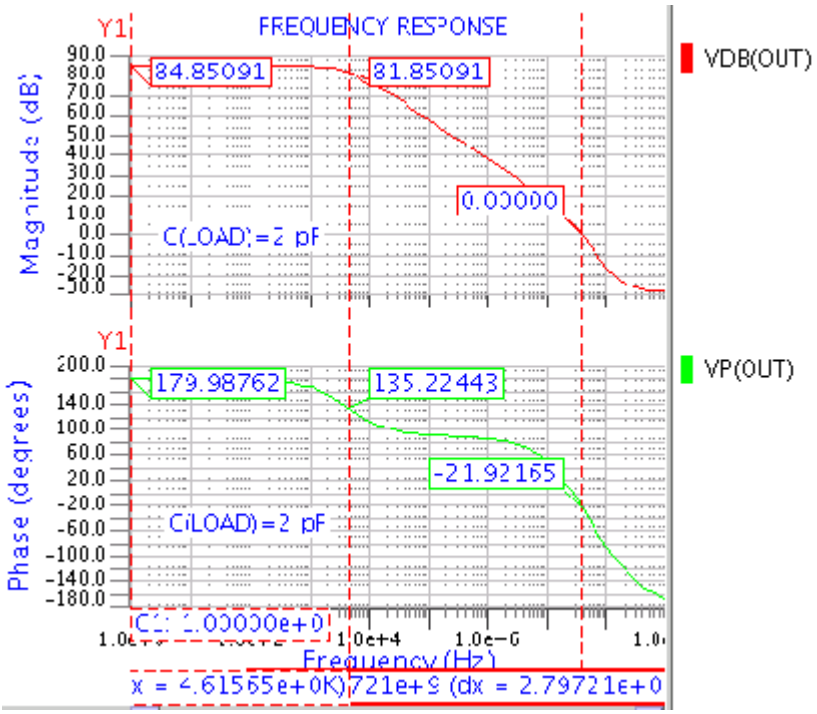


Fig 5.18(a)

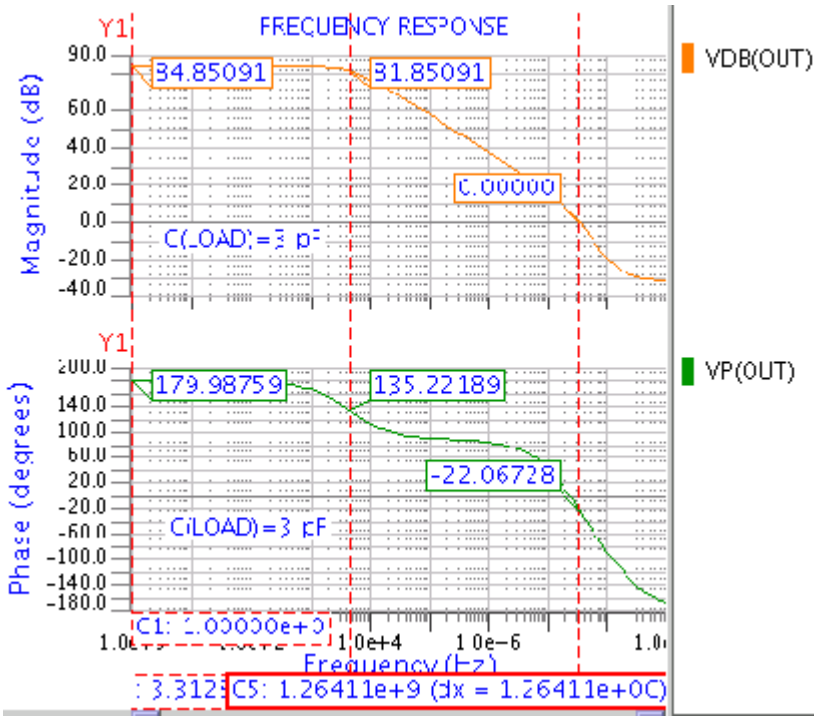


Fig 5.18(b)

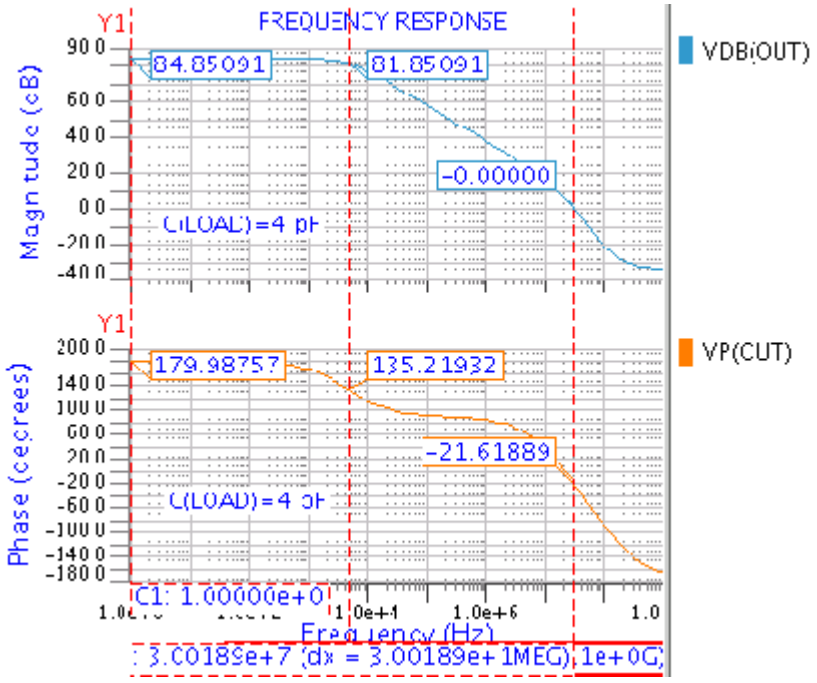


Fig 5.18(c)

Fig 5.18 Frequency Response plot at different Load capacitance values (a) 2 pF (b) 3 pF (c) 4 pF

The effect of load capacitance on common mode gain is shown in Fig 5.19.

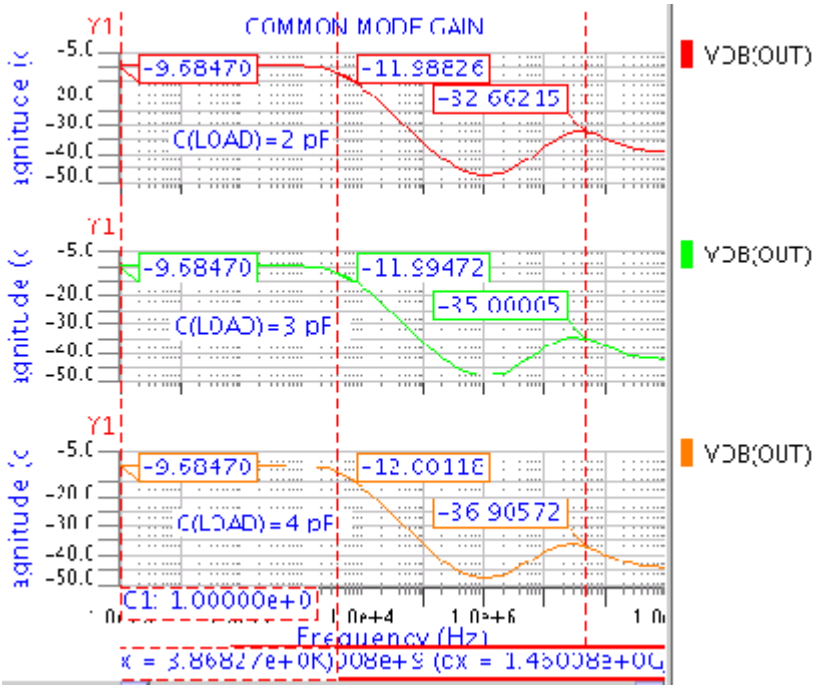


Fig 5.19 Common mode Gain at different Load capacitance values 2 pF, 3 pF and 4 pF

5.2 Simulated Two Stage Operational Amplifier with BICS Circuit Results

Fig 5.20 shows the circuit diagram of the two stage CMOS operational amplifier with built in current sensors circuit (BICS).

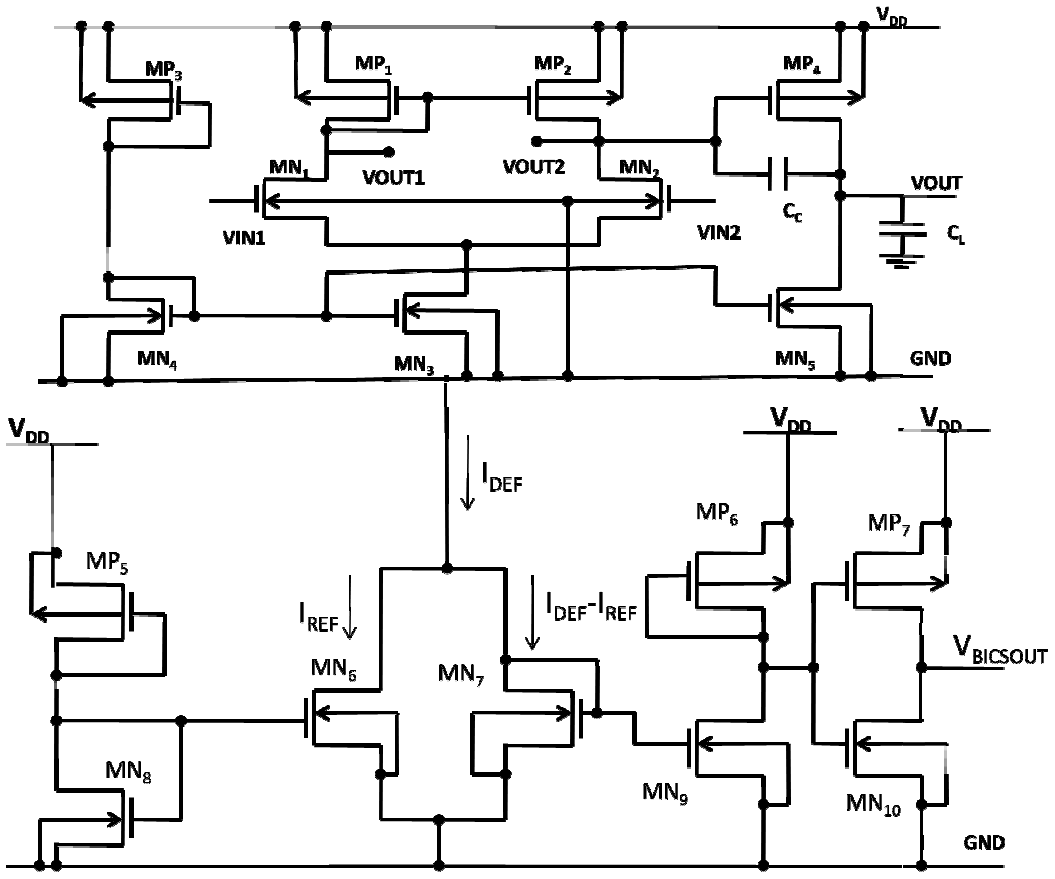


Fig 5.20 Circuit Diagram of a Two Stage CMOS Op-amp with BICS Circuit

5.2.1 AC Response

Fig 5.21 shows frequency response of two stage CMOS operational amplifier with BICS.

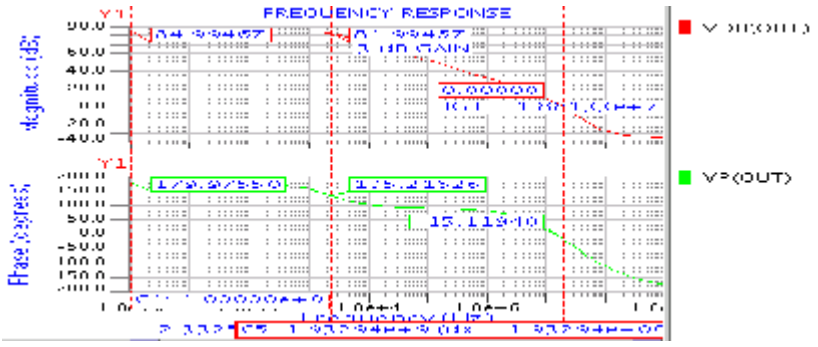


Fig 5.21 Frequency response of CMOS Op-amp with BICS

5.2.2 Common mode Gain

Fig 5.22 shows common mode gain of two stage CMOS operational amplifier with BICS.

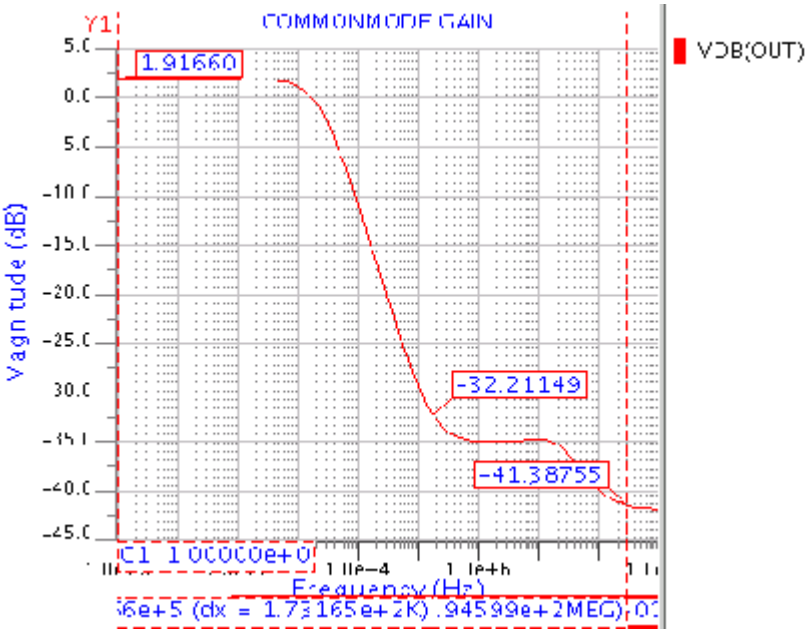


Fig 5.22 Common mode Gain of CMOS Op-amp with BICS

5.2.3 Common Mode Rejection Ratio

Fig 5.23 shows common mode rejection ratio of two stage CMOS operational amplifier with BICS.

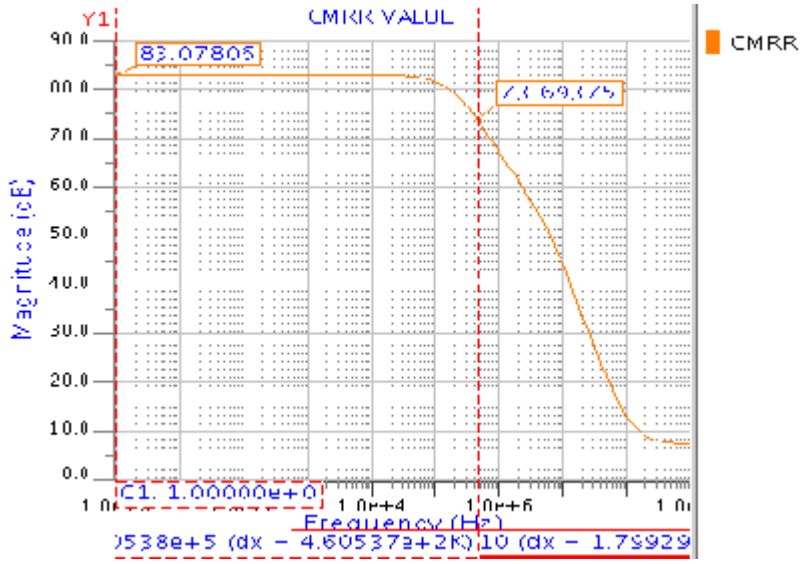


Fig 5.23 CMRR of CMOS Op-amp with BICS

5.2.4 Power Supply Rejection Ratio

Fig 5.24 shows power supply rejection ratio of two stage CMOS operational amplifier with BICS.

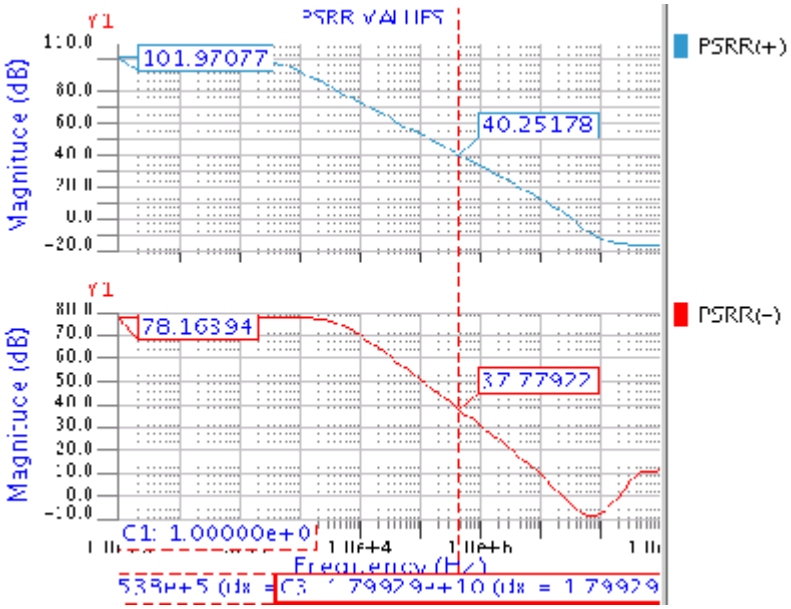


Fig 5.24 PSRR of CMOS Op-amp with BICS

5.2.5 Input Common Mode Range

Fig 5.25 shows input common mode range of two stage CMOS operational amplifier with BICS.

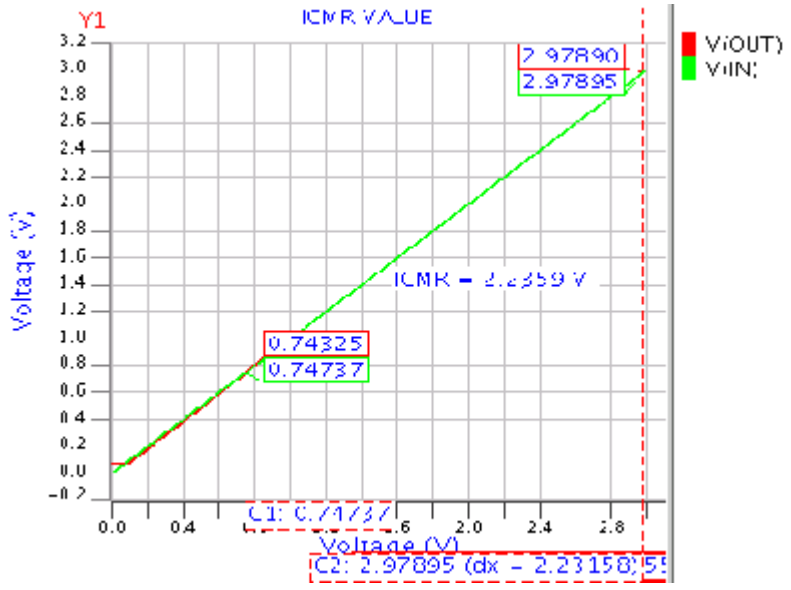


Fig 5.25 ICMR of CMOS Op-amp with BICS

5.2.6 Slew Rate

Fig 5.26 shows slew rate for the rising edge of two stage CMOS operational amplifier with BICS.

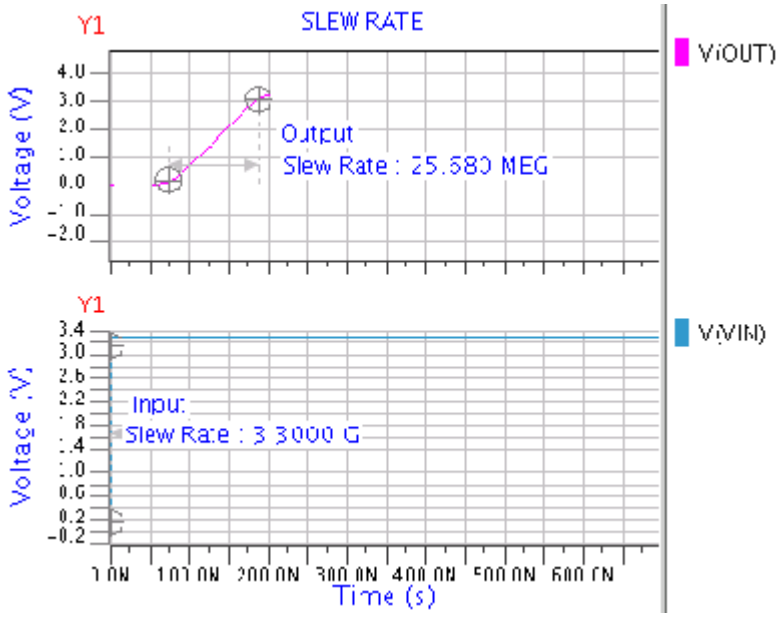


Fig 5.26 Slew Rate of CMOS Op-amp with BICS

5.3 Process Corner Simulation

In this section, Process corner simulation has been done on CMOS operational amplifier. The parasitic effects can make a big problem if any process parameter varies during fabrication process. Thus it is necessary to check the circuit performance at every expected corner of the process variation. The simulation done considering all probabilities of process parameter variation is called as process corner simulation.

Here in this simulation process parameter like oxide thickness, mobility and electrical parameter threshold voltage are considered with variations of 20% in each.

5.3.1 AC Response

The following figures (from Fig 5.27 and Fig 5.28) show process corner simulation for AC analysis of the two stage CMOS op-amp.

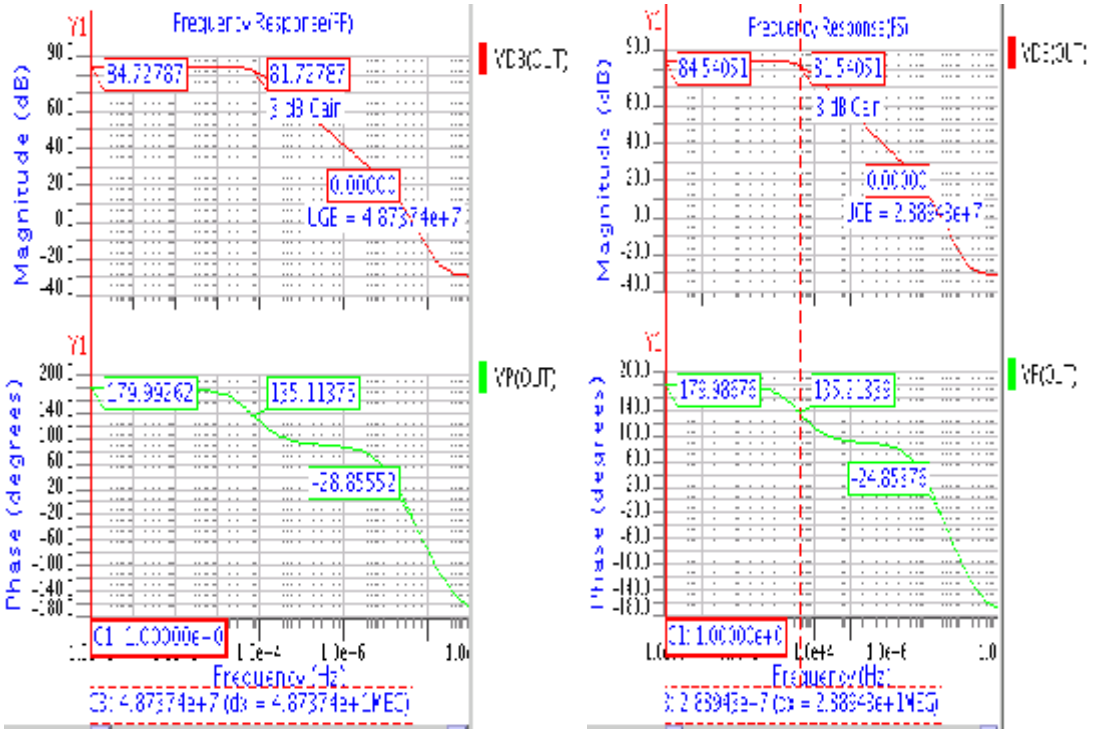


Fig 5.27 Process corner –FF and FS simulation for AC analysis

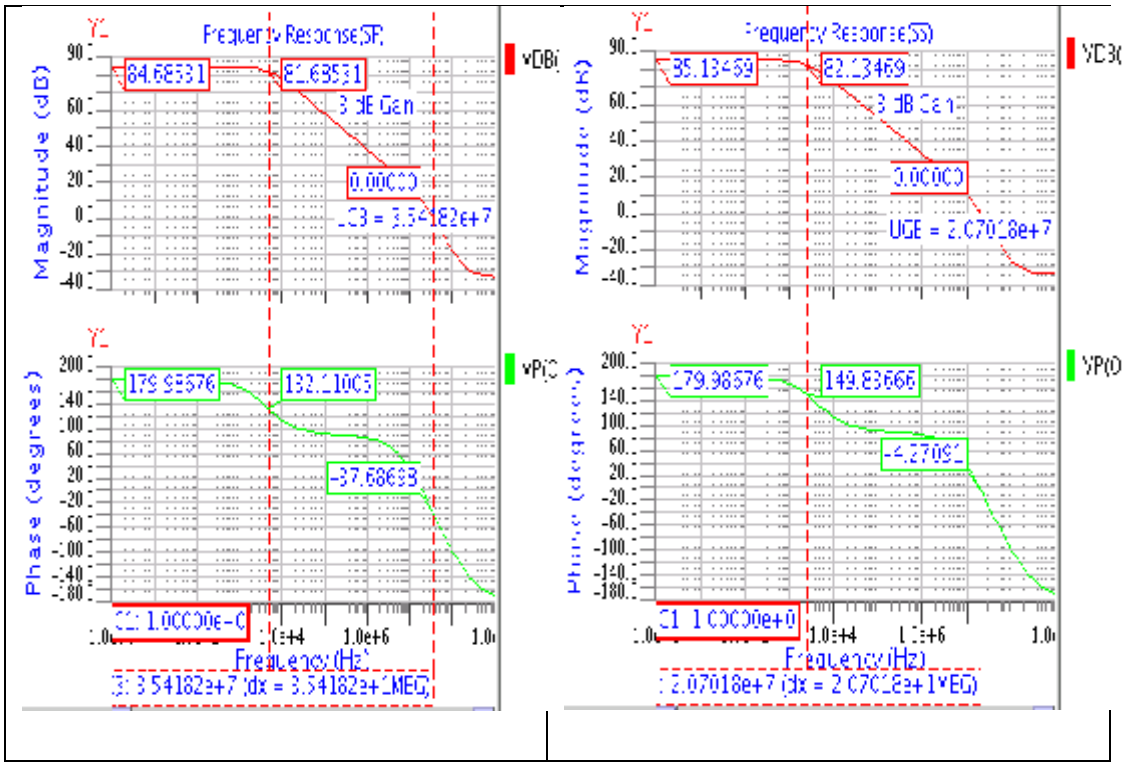


Fig 5.28 Process corner –SF and SS Simulation for AC analysis

5.3.2 Transient Analysis

The following figures (from Fig 5.29 to Fig 5.30) show process corner simulation for Transient analysis of the two stage CMOS op-amp.

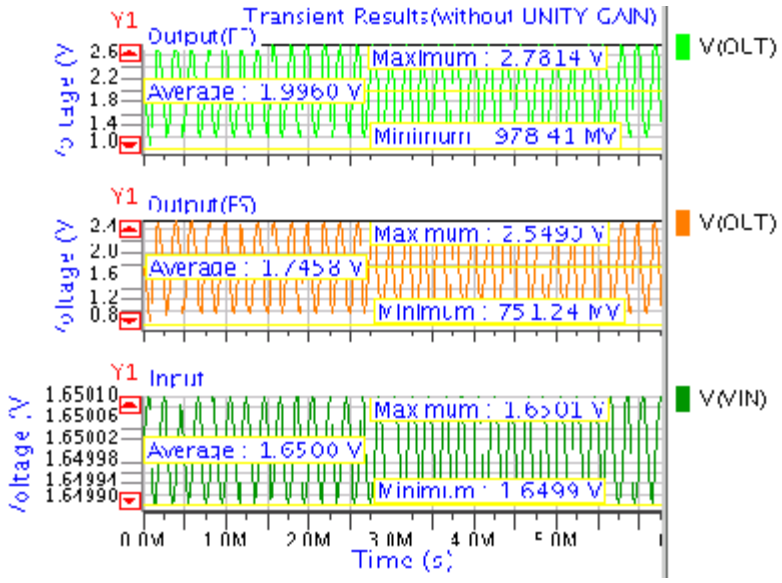


Fig 5.29 Process corner –FF and FS simulation for Transient analysis

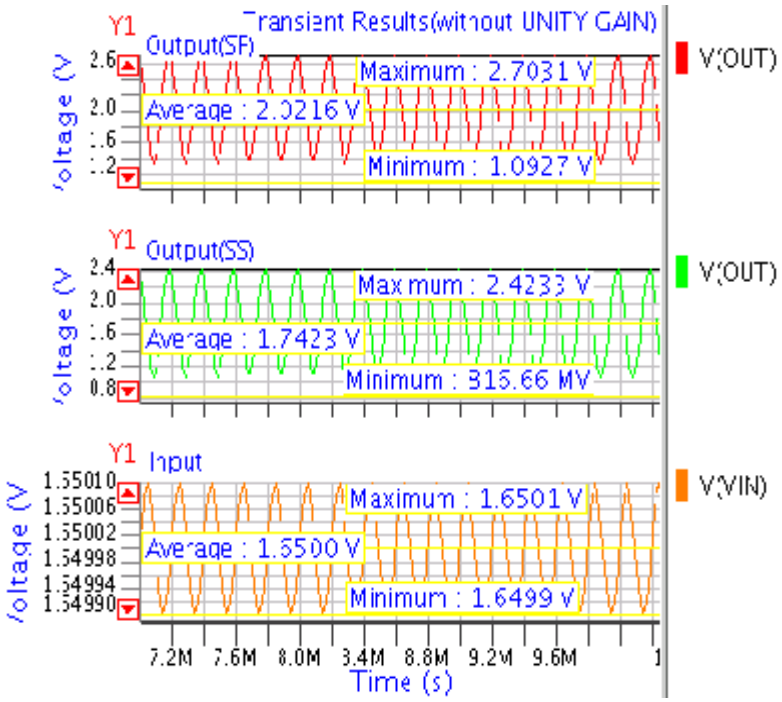


Fig 5.30 Process corner –SF and SS simulation for Transient analysis

5.3.3 CMRR

The following figures (from Fig 5.31 to Fig 5.32) show process corner simulation for common mode rejection ratio of the two stage CMOS op-amp.

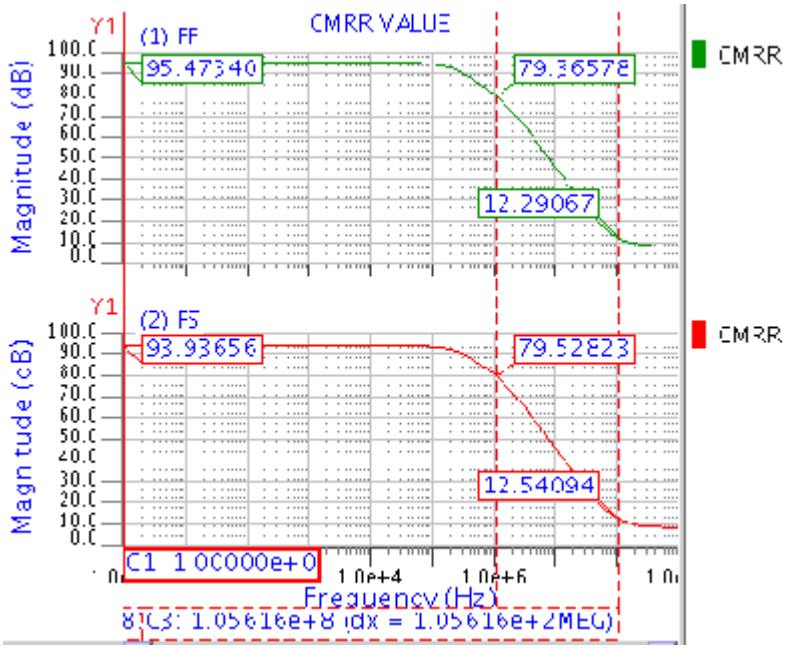


Fig 5.31 Process corner –FF and FS simulation for CMRR

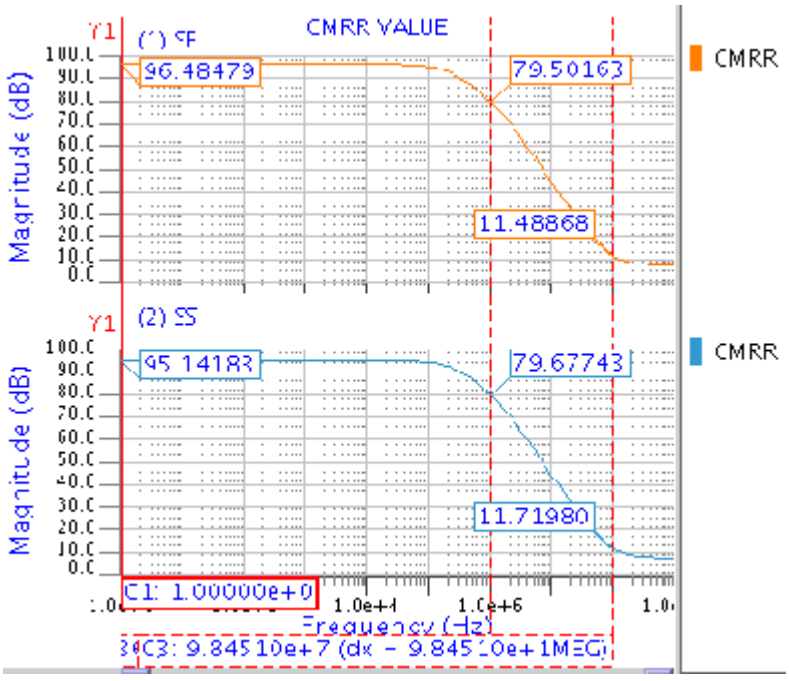


Fig 5.32 Process corner –SF and SS simulation for CMRR

5.3.4 PSRR

The following figures (from Fig 5.33 to Fig 5.36) show process corner simulation for power supply rejection ratio of the two stage CMOS op-amp.

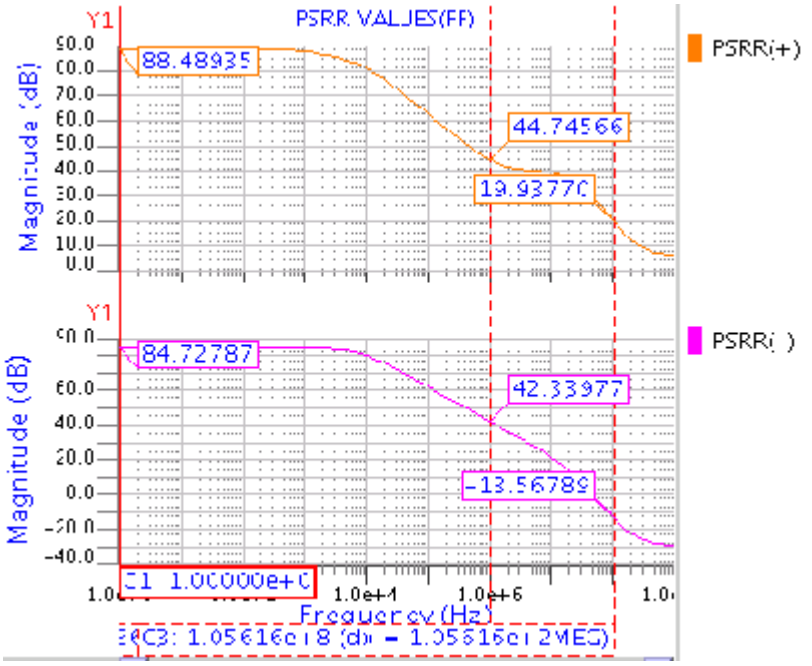


Fig 5.33 Process corner –FF simulation for PSRR(+) and PSRR(-)

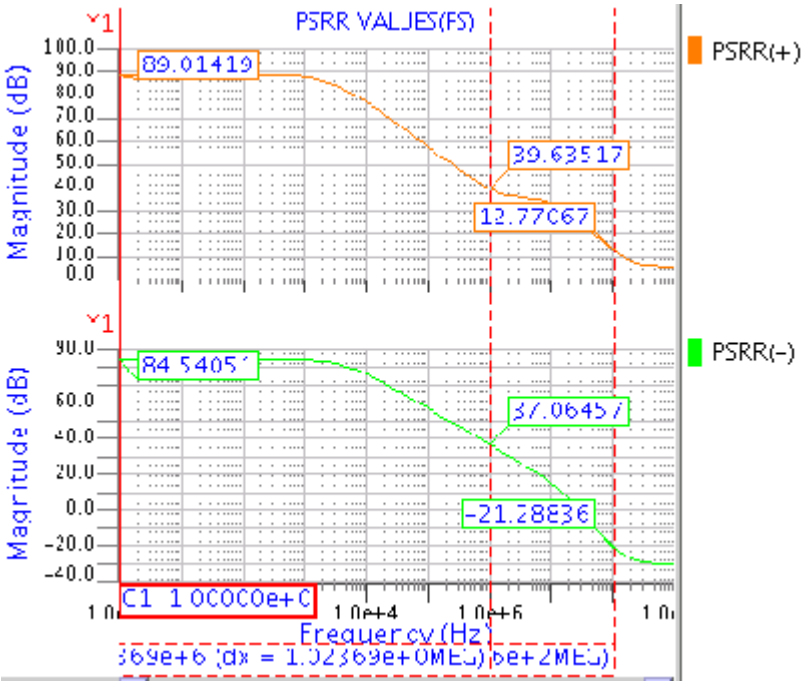


Fig 5.34 Process corner –FS simulation for PSRR(+) and PSRR(-)

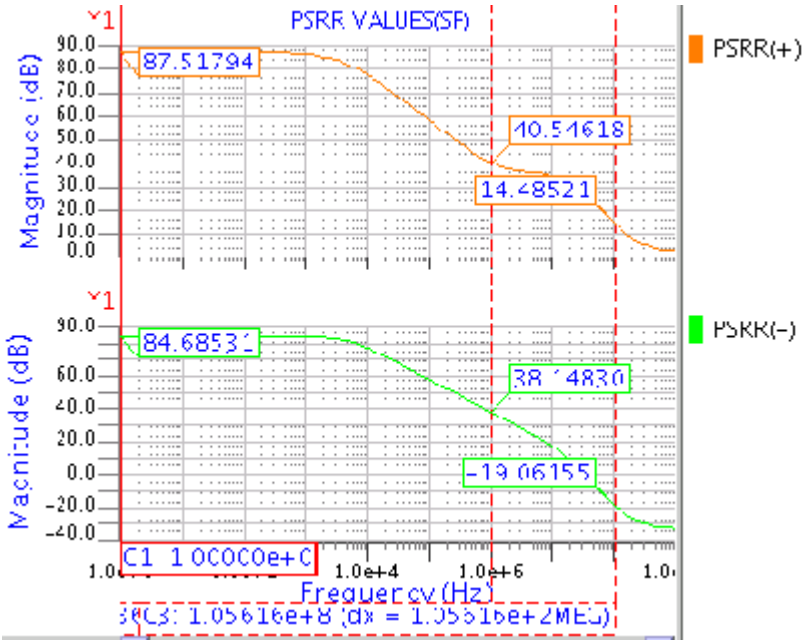


Fig 5.35 Process corner –SF simulation for PSRR(+) and PSRR(-)

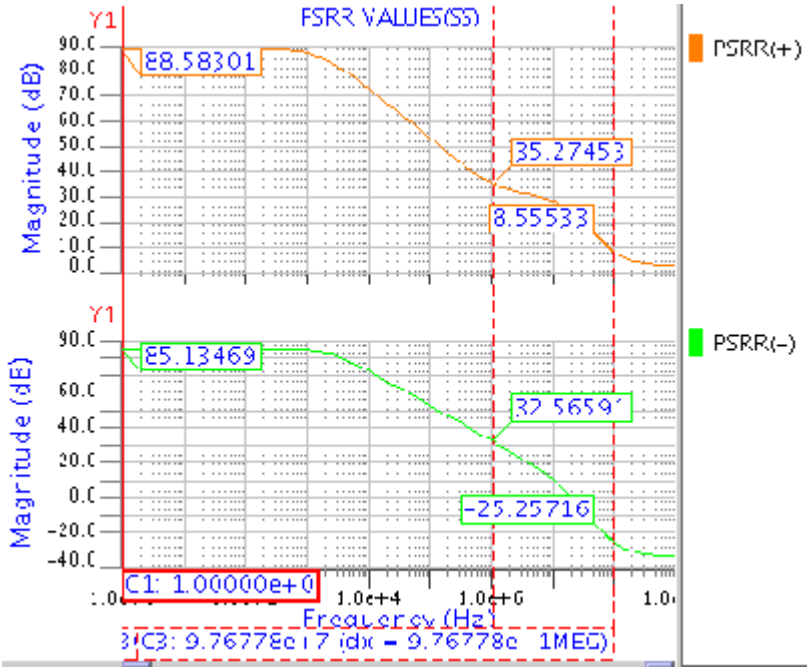


Fig 5.36 Process corner –SS simulation for PSRR(+) and PSRR(-)

5.3.5 ICMR

The following figures (from Fig 5.37) show process corner simulation for input common mode range of the two stage CMOS op-amp.

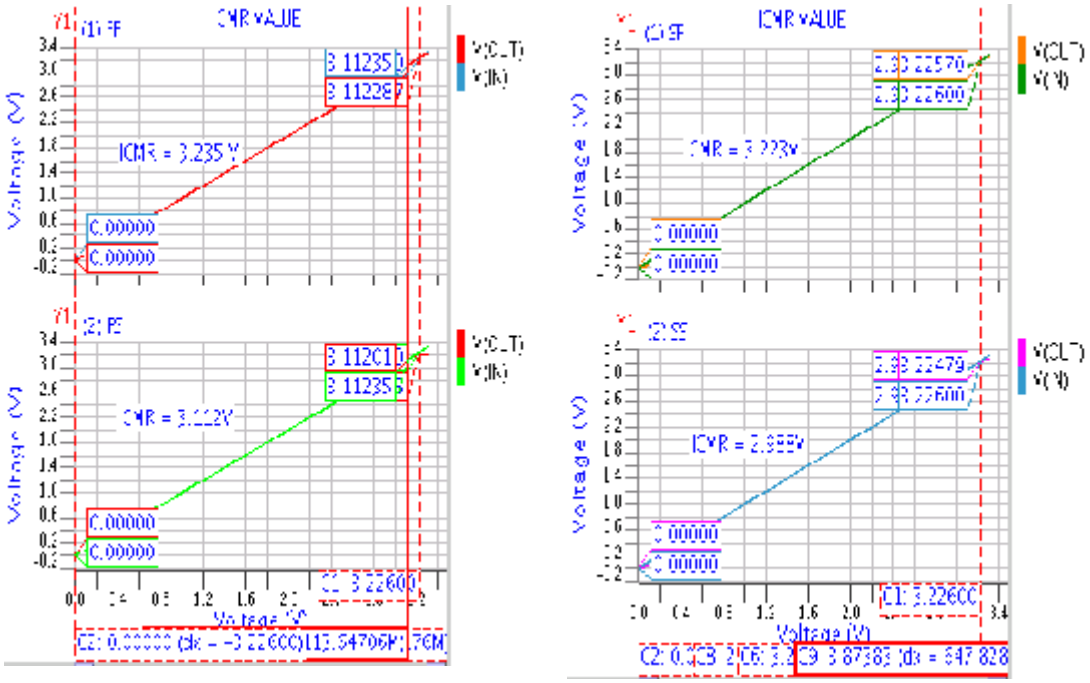


Fig 5.37 Process corner –FF, FS, SF and SS simulation for ICMR

5.3.6 Slew Rate

The following figure (Fig 5.38) shows process corner simulation for slew rate of the two stage CMOS op-amp.

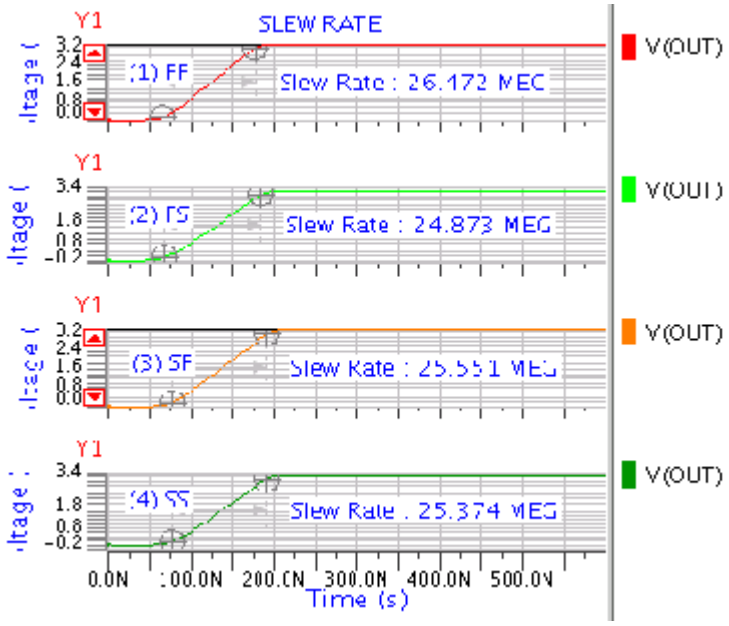


Fig 5.38 Process corner –FF, FS, SF and SS simulation for Slew rate

Simulation results of two stage CMOS op-amp without BICS circuit, with BICS circuit and Process corner are listed in Table 5.1.

Table 5.1: Simulation results of CMOS Op-amp without BICS circuit, with BICS circuit and Process Corner

Specification Parameters	**2-Stage CMOS Op-amp (without BICS circuit)**	**2-Stage CMOS Op-amp (with BICS circuit)**	**Process Corner**			
			FF simulation	**FS simulation**	**SF simulation**	**SS simulation**
UnityGain Bandwidth (UGB)(MHz)	33.129	18.813	48.737	28.894	35.418	20.702
Low Frequency Gain(dB)	84.851	84.995	84.728	84.540	84.685	85.135
CMRR(dB)	95.533	83.080	95.473	93.937	96.485	95.142
+PSRR/ -PSRR(dB)	88.423/ 84.851	101.970 / 78.164	88.489/ 84.728	89.014/ 84.540	87.518/ 84.685	88.583/ 85.135
ICMR(V)	3.237	2.236	3.235	3.112	3.223	2.988
SLEW RATE(V/uS)	25.926	25.680	26.472	24.873	25.551	25.374

5.4 Simulated I_{DDQ} Testing Results

In the two stage CMOS op-amp (Sec 4.4 and Fig 4.7) with BICS circuit (Sec 5.2 and Fig 5.21), fifteen faults are injected in the circuit out of which eight are bridge faults and remaining are open circuit faults. The testable faults which can be detected by IDDQ testing are defect -6(MN3DSS), defect-8(MP3DSS), defect-10(MN4GO), defect -11(MP3GO) and defect-14(MN4DO). Effect of individual fault on circuit is discussed in the following sections.

5.4.1 Fault free circuit

When there are no defects in the circuit, the output of BICS circuit is a low value, indicating that circuit is fault free. Value of I_{REF} is 150uA and (I_{DEF}-I_{REF}) is 4.0uA. And the value of BICS output is 17.54mV, a low voltage (Fig 5.39).

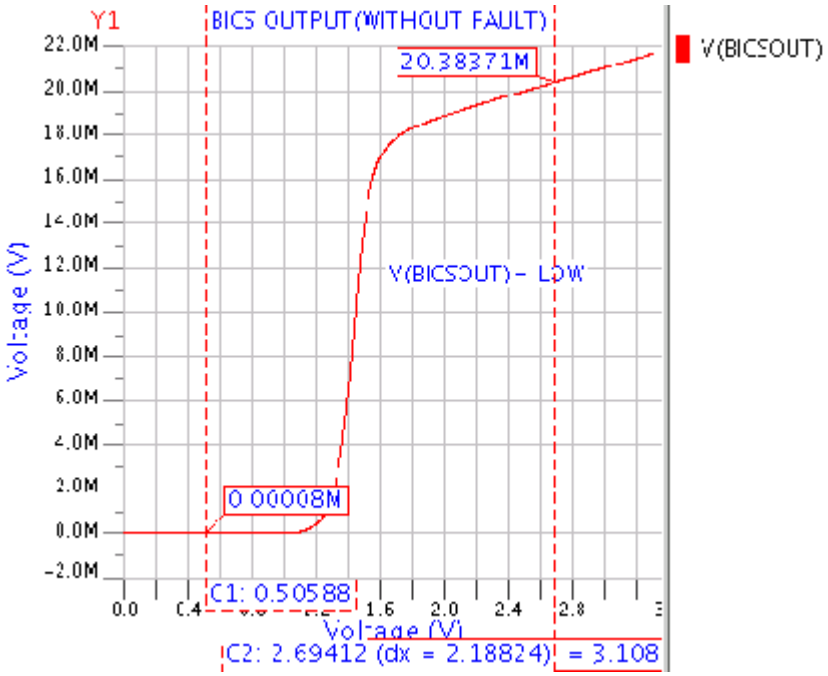


Fig 5.39 BICS output when there are no faults in the circuit

5.4.2 With defect -1(MN4DSS)

Defect -1(MN4DSS) is a bridging fault. It is a short between drain and source of MN_4 transistor. When this fault is present the value of (I_{DEF}-I_{REF}) is 230pA. And the value of BICS output is 1.2310uV, a low value (Fig 5.40) instead of high value. Hence, this fault is undetectable by I_{DDQ} testing.

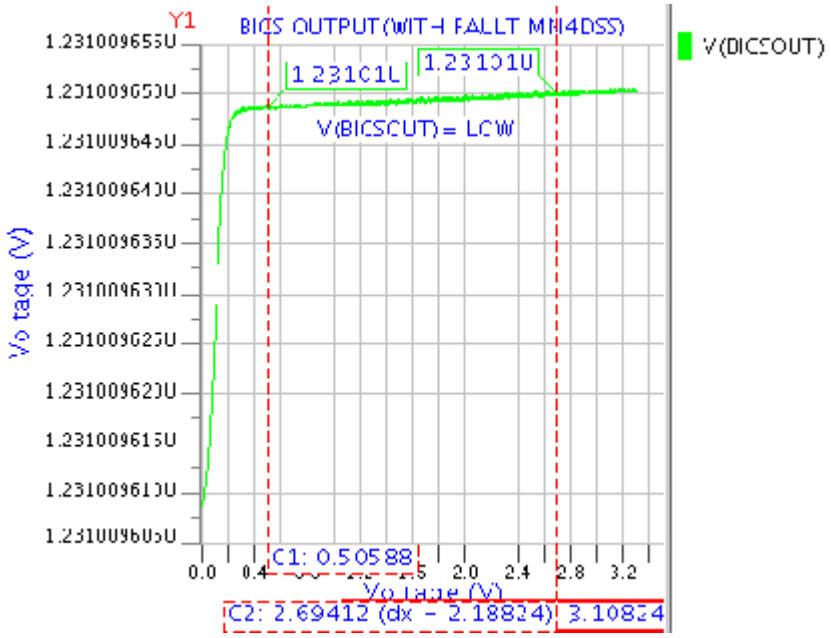


Fig 5.40 BICS output with MN4DSS (defect-1) fault

5.4.3 With defect -2(MN5DSS)

Defect -2(MN5DSS) is a bridging fault. It is a short between drain and source of MN_5 transistor. When this fault is present the value of (I_{DEF}-I_{REF}) is 5.8476uA. And the value of BICS output is 25.3742mV, a low value (Fig 5.41) instead of high value. Hence, this fault is undetectable by I_{DDQ} testing.

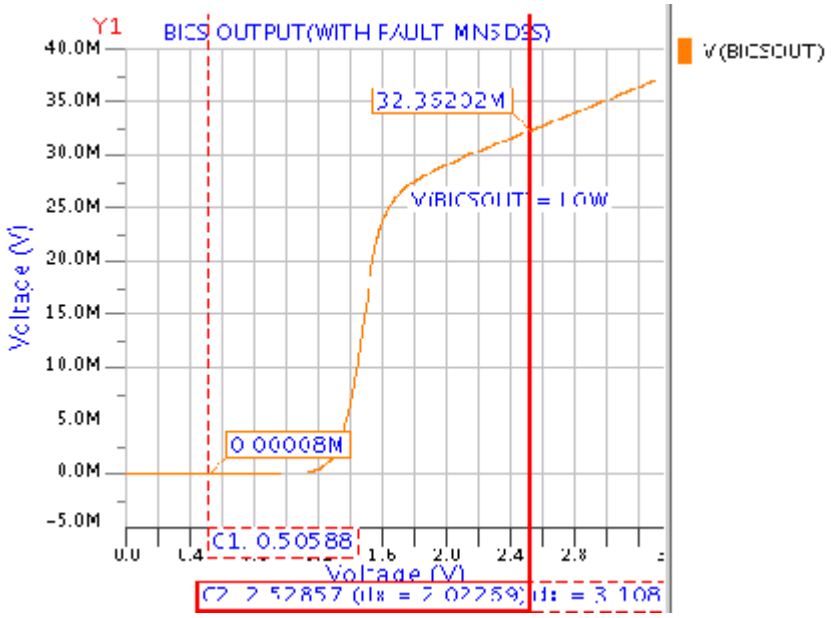


Fig 5.41 BICS output with MN5DSS (defect-2) fault

5.4.4 With defect -3(MN5GDS)

Defect -3(MN5GDS) is a bridging fault. It is a short between gate and drain of MN_5 transistor. When this fault is present the value of (I_{DEF}-I_{REF}) is 6.3371uA. And the value of BICS output is 27.6386mV, a low value (Fig 5.42) instead of high value. Hence, this fault is undetectable by I_{DDQ} testing.

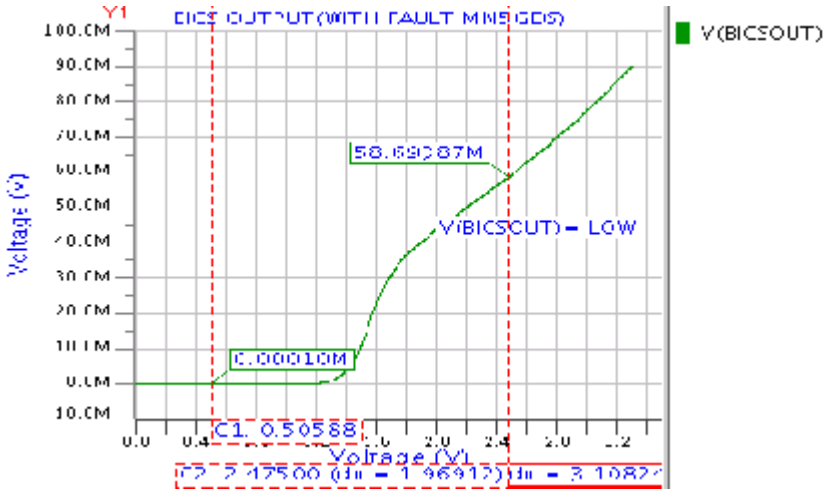


Fig 5.42 BICS output with MN5GDS (defect-3) fault

5.4.5 With defect -4(MP4DSS)

Defect -4(MP4DSS) is a bridging fault. It is a short between drain and source of MP_4 transistor. When this fault is present the value of (I_{DEF}-I_{REF}) is 5.3572uA. And the value of BICS output is 23.1348mV, a low value (Fig 5.43) instead of high value. Hence, this fault is undetectable by I_{DDQ} testing.

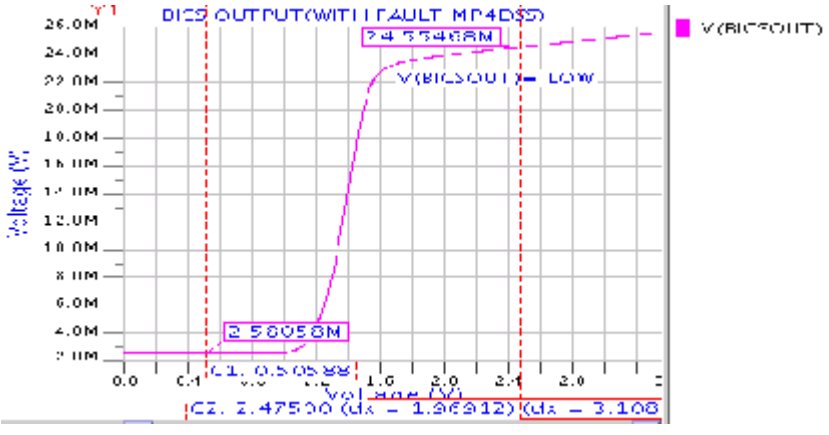


Fig 5.43 BICS output with MP4DSS (defect-4) fault

5.4.6 With defect -5(MP4GDS)

Defect -5(MP4GDS) is a bridging fault. It is a short between gate and drain of MP_4 transistor. When this fault is present the value of (I_{DEF}-I_{REF}) is 4.6543uA. And the value of BICS output is 19.9748mV, a low value (Fig 5.44) instead of high value. Hence, this fault is undetectable by I_{DDQ} testing.

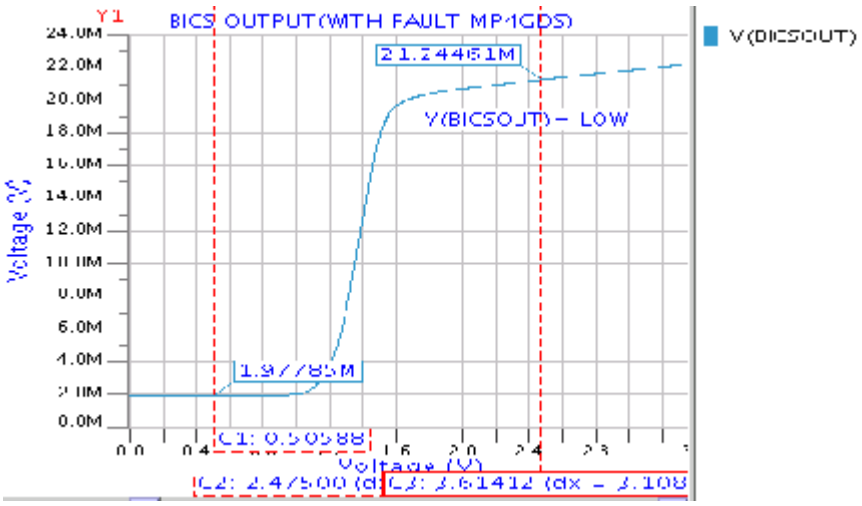


Fig 5.44 BICS output with MP4GDS (defect-5) fault

5.4.7 With defect -6(MN3DSS)

Defect -6(MN3DSS) is a bridging fault. It is a short between drain and source of MN_3 transistor. When this fault is present the value of (I_{DEF}-I_{REF}) is 77.7060uA. And the value of BICS output is 3.2723V, high value (Fig 5.45) indicating the presence of defect in the circuit. Hence, this fault is detectable by I_{DDQ} testing.

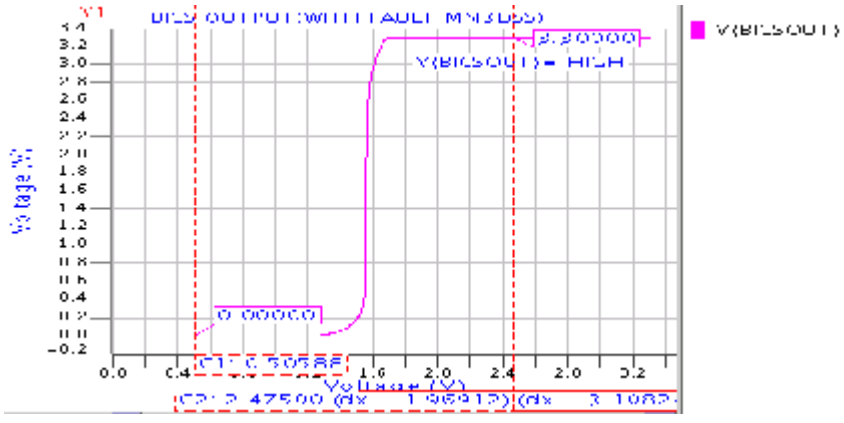


Fig 5.45 BICS output with MN3DSS (defect-6) fault

5.4.8 With defect -7(MN3GDS)

Defect -7(MN3GDS) is a bridging fault. It is a short between gate and drain of MN_3 transistor. When this fault is present the value of (I_{DEF}-I_{REF}) is 34.57pA. And the value of BICS output is 197.10nV, a low value (Fig 5.46) instead of high value. Hence, this fault is undetectable by I_{DDQ} testing.

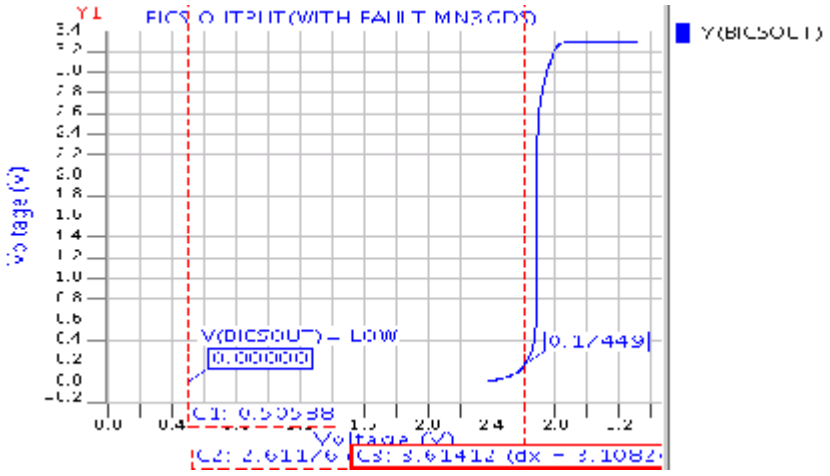


Fig 5.46 BICS output with MN3GDS (defect-7) fault

5.4.9 With defect -8(MP3DSS)

Defect -8(MP3DSS) is a bridging fault. It is a short between drain and source of MP_3 transistor. When this fault is present the value of (I_{DEF}-I_{REF}) is 896.62uA. And the value of BICS output is 3.3V, high value (Fig 5.47) indicating the presence of defect in the circuit. Hence, this fault is detectable by I_{DDQ} testing.

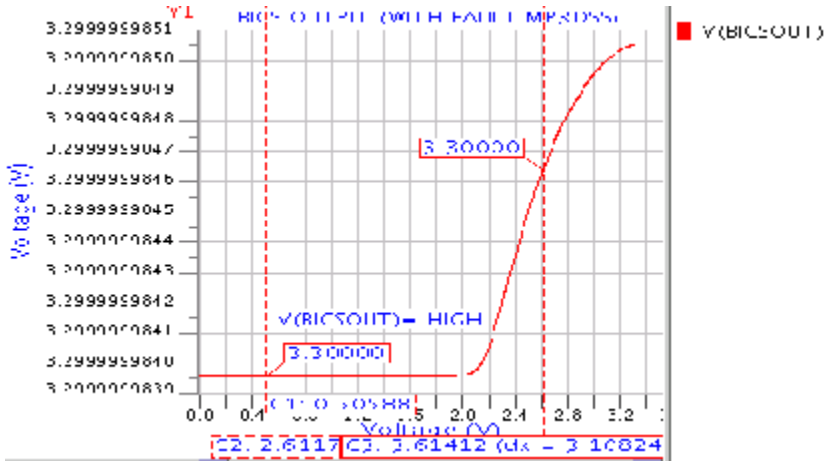


Fig 5.47 BICS output with MP3DSS (defect-8) fault

5.4.10 with defect -9(MN3GO)

Defect -9(MN3GO) is an open circuit fault. It is a fault due to gate open of MN_3 transistor. When this fault is present the value of (I_{DEF}-I_{REF}) is 11.58pA. And the value of BICS output is 74nV, a low value (Fig 5.48) instead of high value. Hence, this fault is undetectable by I_{DDQ} testing.

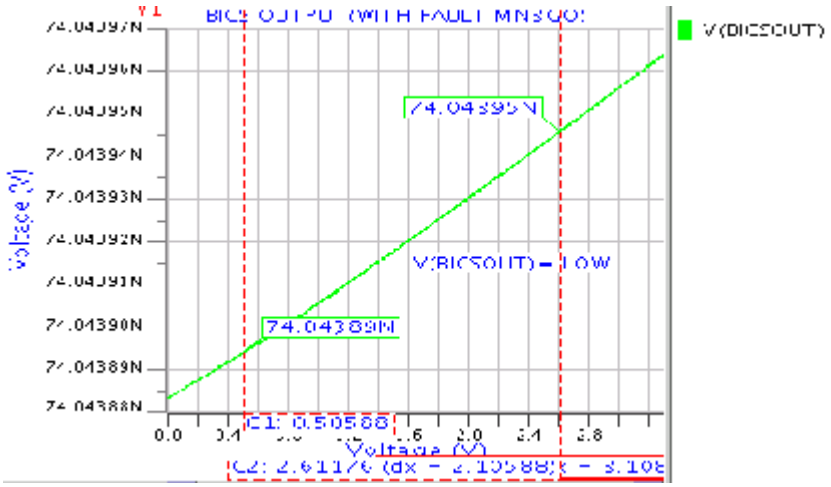


Fig 5.48 BICS output with MN3GO (defect-9) fault

5.4.11 with defect -10(MN4GO)

Defect -10(MN4GO) is an open circuit fault. It is a fault due to gate open of MN_4 transistor. When this fault is present the value of (I_{DEF}-I_{REF}) is 95.76uA. And the value of BICS output is 3.289V, high value (Fig 5.49) indicating the presence of fault in the circuit. Hence, this fault is detectable by I_{DDQ} testing.

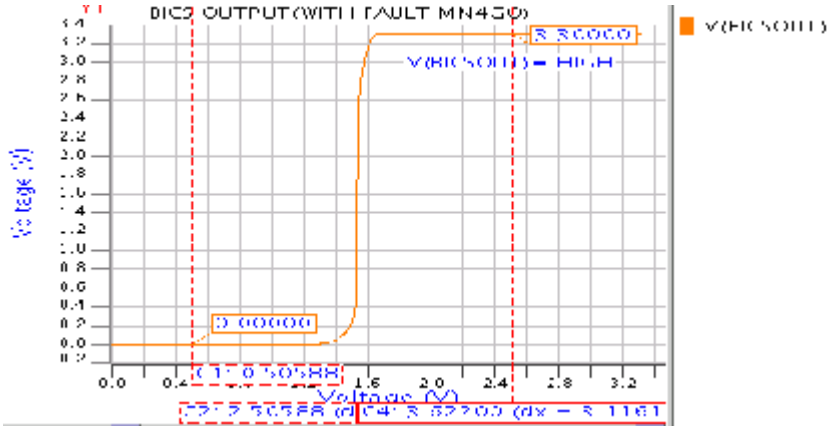


Fig 5.49 BICS output with MN4GO (defect-10) fault

5.4.12 with defect -11(MP3GO)

Defect -11(MP3GO) is an open circuit fault. It is a fault due to gate open of MN_3 transistor. When this fault is present the value of (I_{DEF}-I_{REF}) is 95.82uA. And the value of BICS output is 3.2895V, high value (Fig 5.50) indicating the presence of fault in the circuit. Hence, this fault is detectable by I_{DDQ} testing.

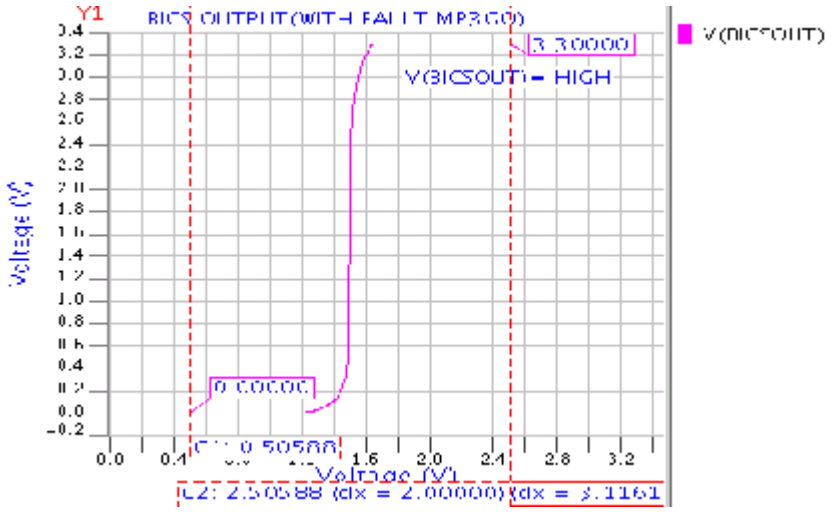


Fig 5.50 BICS output with MP3GO (defect-11) fault

5.4.13 with defect -12(MN5GO)

Defect -12(MN5GO) is an open circuit fault. It is a fault due to gate open of MN_5 transistor. When this fault is present the value of (I_{DEF}-I_{REF}) is 126pA. And the value of BICS output is 685.11nV, a low value (Fig 5.51) instead of high value. Hence, this fault is undetectable by I_{DDQ} testing.

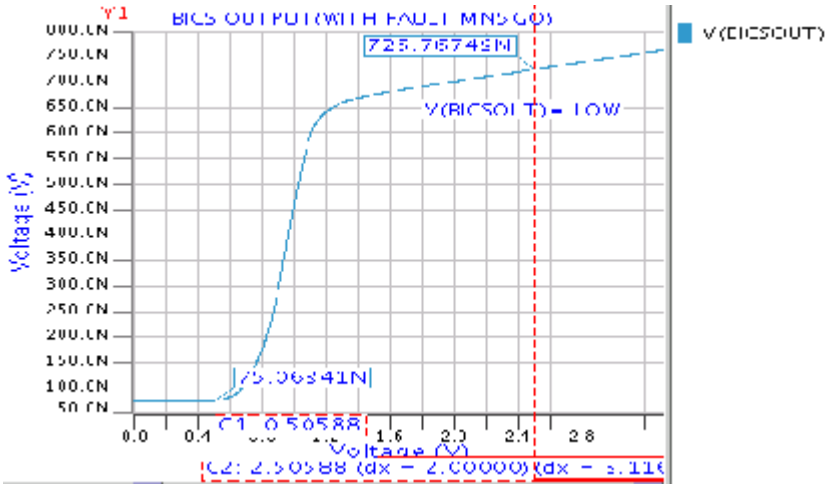


Fig 5.51 BICS output with MN5GO (defect-12) fault

5.4.14 with defect -13(MP4GO)

Defect -13(MP4GO) is an open circuit fault. It is a fault due to gate open of MP_4 transistor. When this fault is present the value of (I_{DEF}-I_{REF}) is 5.35uA. And the value of BICS output is 23.10mV, a low value (Fig 5.52) instead of high value. Hence, this fault is undetectable by I_{DDQ} testing.

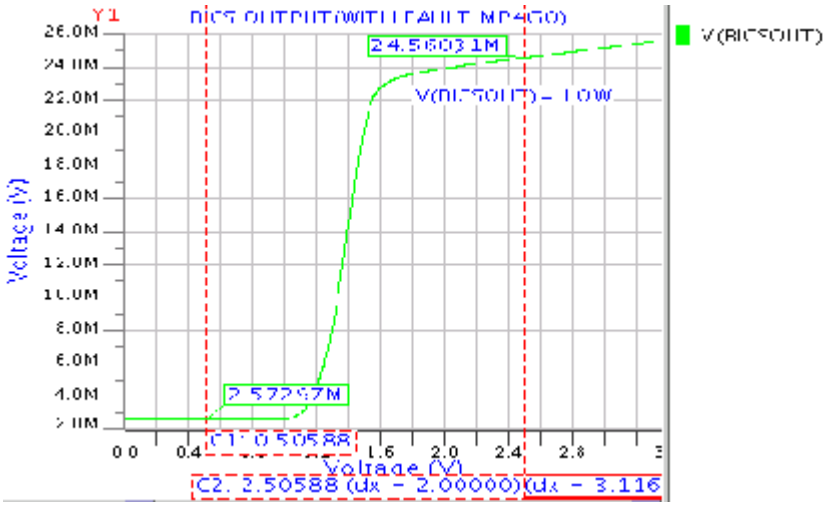


Fig 5.52 BICS output with MP4GO (defect-13) fault

5.4.15 with defect -14(MN4DO)

Defect -14(MN4DO) is an open circuit fault. It is a fault due to drain open of MN_4 transistor. When this fault is present the value of (I_{DEF}-I_{REF}) is 97.93uA. And the value of BICS output is 3.2928V, high value (Fig 5.53) indicating the presence of fault in the circuit. Hence, this fault is detectable by I_{DDQ} testing.

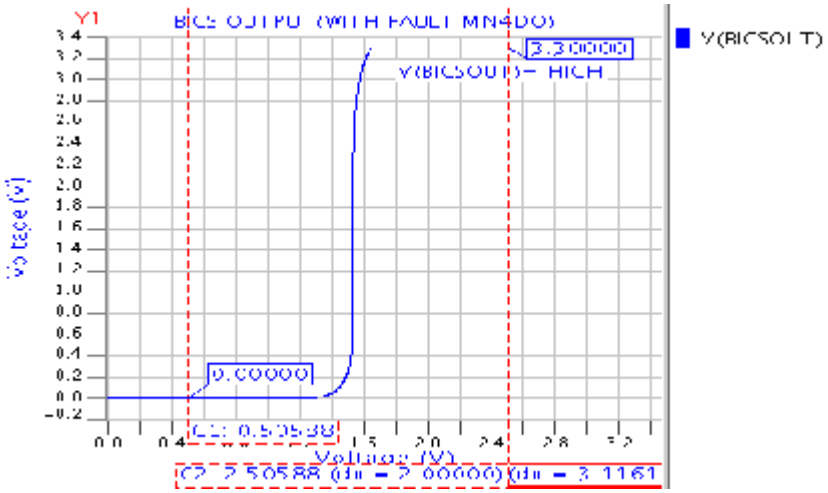


Fig 5.53 BICS output with MN4DO (defect-14) fault

5.4.16 with defect -15(MN3DO)

Defect -15(MN3DO) is an open circuit fault. It is a fault due to drain open of MN_3 transistor. When this fault is present the value of (I_{DEF}-I_{REF}) is 11.58pA. And the value of BICS output is 74nV, a low value (Fig 5.54) instead of high value. Hence, this fault is undetectable by I_{DDQ} testing.

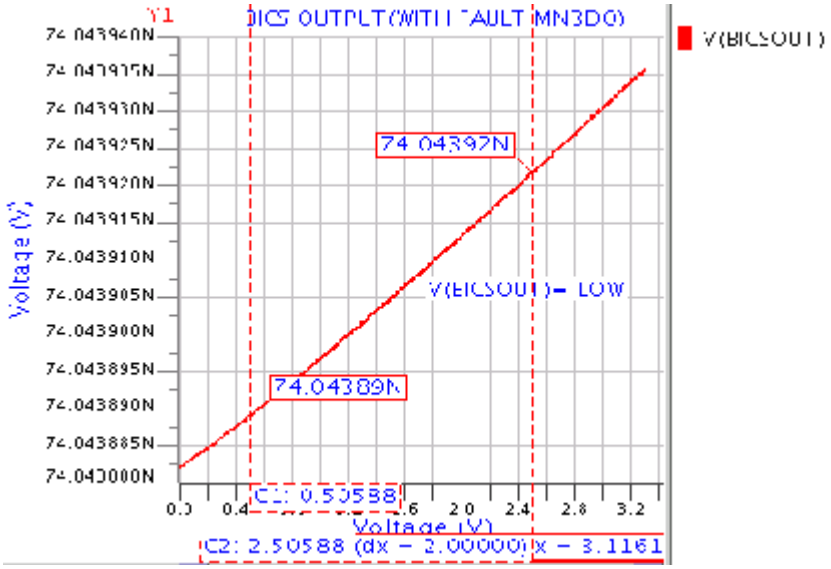


Fig 5.54 BICS output with MN3DO (defect-15) fault

Total fifteen faults are injected into the two stage CMOS op-amp with BICS circuit. Among them eight are bridging faults and seven are open circuit faults. Five faults (two bridging faults and three open circuit faults) are detected by I_{DDQ} testing method.

5.5 Analog Layout

When low-level or high-precision circuitry is being designed, a lot of care is usually given to the details of the circuit schematic and how the signal runs are routed. In doing layouts for digital circuits, the speed and the area are the two most important issues. In contrast, in doing layout for analog circuits, everything should be considered simultaneously.

In addition to the speed and the area, other equally critical considerations should be taken into account. In analog layout more care has to be taken as the circuit performance changes drastically due to noise, mismatches, crosstalk and shielding required to protect critical nodes from being disturbed. Without proper layout, the mismatches and the

coupled noise would be quite large and would significantly degrade the performance of the amplifiers. Analog layout issues are discussed in bellow sections [42].

5.5.1 Matching of Devices

Device mismatch is too often treated as part of the black art of analog design. Random device mismatch plays an important role in the design of accurate analog circuits. The device mismatch is due to number factors like local process variation, global lithographic variations, local lithographic variations and process gradients. These factors affect all devices transistors, resistor, capacitors, and therefore similar techniques can be used to match all elements. During fabrication phase mismatch in physical parameters like doping concentration (N_a), mobility (μ), oxide thickness (t_{ox}) and layout dimensions (W, L) gives origin to mismatch in electrical parameter like V_T and β thus mismatch in I_D.

Matching of individual devices is of paramount concern in analog circuit design. Infect almost all of the 'analog layout techniques' are actually methods for improving matching between different devices on a chip. Matching is important because most analog circuit designs use a ratio based design technique. Some common techniques that help improve device matching are MULTI-GATE FINGER LAYOUT and COMMON-CENTROID LAYOUT.

Use of transistor fingering for large and critical transistors is always beneficial. In fingering the transistor is “fingered” into multiple transistors that are connected in parallel. The folded transistors reduce the source/ Drain junction area and the gate resistance. The gate resistance can be reduced by decomposing the transistor into more parallel fingers. Common-centroid layout [43] refers to a layout style in which a set of devices has a common center point. This is used to minimize the effect of linear process gradients (e.g. oxide thickness) in a circuit.

Example: Consider that a transistor 'A' has 'M' fingers and can be represented by 'M' instances of the letter 'A'. For example 'AAAA' represents a transistor 'A' that has 4 fingers.

Now consider the layout of two transistors, 'A' and 'B'. One structure is: AABB. The problem with this structure is that the transistor 'A' will have a different oxide capacitance (which affects transconductance) than 'B' because of oxide gradients.

For instance, if the oxide thickness at the center of the structure is T_{ox}, and there is an oxide gradient DEL, the average oxide thickness for 'A' and 'B' is

$$T_{ox}\text{ (A, average)} = [T_{ox} - 2DEL]/2 + [T_{ox} - DEL]/2 = T_{ox} - 3DEL/2$$

$$T_{ox}\text{ (B, average)} = [T_{ox} + 2DEL]/2 + [T_{ox} + DEL]/2 = T_{ox} + 3DEL/2$$

Now consider the following layout:

ABBA

The average oxide thickness will now be:

$$\text{Tox (A, average)} = [\text{Tox} - 2DEL]/2 + [\text{Tox} + 2DEL]/2 = \text{Tox}$$

$$\text{Tox (B, average)} = [\text{Tox} - DEL]/2 + [\text{Tox} + DEL]/2 = \text{Tox}.$$

5.5.2 Layout of Two Stage CMOS Op-amp with BICS Circuit

Layout of the two stage CMOS op amp with BICS circuit is shown in the Fig 5.55. LVS report and PEX report are presented in Annexure.

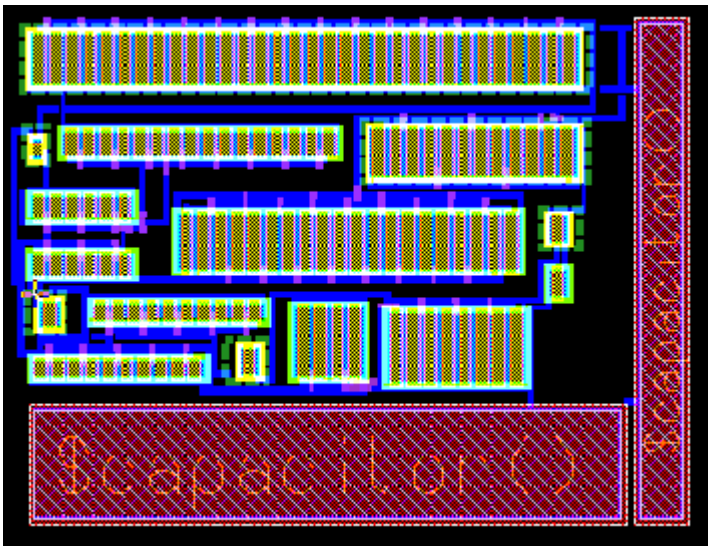


Fig 5.55 Layout of Two Stage CMOS Op-amp with BICS Circuit

Chapter-6

CONCLUSION AND FUTURE SCOPE OF WORK

6.1 Conclusion

In the present work, a two stage CMOS operational amplifier has been designed with BICS circuit. It is tested using I_{DDQ} Test method. This testing method uses built in current sensors for the detection of quiescent power supply current. Different faults like bridge faults, open faults are injected in the two stage CMOS operational amplifier for testing purpose. Among those faults some faults which increases quiescent power supply current to reasonable amount are detected by I_{DDQ} testing. This method is attractive because of its simplicity and robustness. It is a high quality supplemental test that can improve overall fault coverage without incurring significant test development cost. I_{DDQ} testing is very effective in detection of bridging, gate-oxide defects and open faults. Simple design-for-test effort to switch-off static current dissipating logic can significantly enhance the design suitability for I_{DDQ} testing. With each technology shrink, I_{off} increases.

6.2 Future Scope

I_{DDQ} testing can still be used successfully in deep submicron technologies with a method such as substrate bias, lower V_{DD} and lower temperature. By dividing any design circuit into number of blocks and adding built in current sensor circuit to each individual block to monitor changes in quiescent power supply current it is possible to find the faults and their location resulting in fault isolation. This method can easily be extendable to built in self test because it doesn't require external test stimuli and uses a simple measurement.

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ANNEXURE

(1) LVS Report

LVS report checks the all connections in schematic with layout.

```
                  ##################################################
                  ##                                              ##
                  ##         C A L I B R E    S Y S T E M         ##
                  ##                                              ##
                  ##             L V S   R E P O R T              ##
                  ##                                              ##
                  ##################################################


REPORT FILE NAME:          layout.lvs.report
LAYOUT NAME:               layout.calibre.gds
SOURCE NAME:
/home/bsuman/opampbics3c/opampbics3c.src.net ('opampbics3c')
RULE FILE:                 /home/bsuman/_tsmc035.rules_
LVS MODE:                  Mask
RULE FILE NAME:            /home/bsuman/_tsmc035.rules_
CREATION TIME:             Sun Jul  5 16:12:53 2009
CURRENT DIRECTORY:         /home/bsuman
USER NAME:                 bsuman
CALIBRE VERSION:           v2006.2_30.26    Fri Jul  7 22:37:10 PDT
2006


**********************************************************************
****************************************
                              OVERALL COMPARISON RESULTS
**********************************************************************
****************************************


                        #       ###################       _   _
                       #        #                 #       *   *
                    #   #       #     CORRECT     #         |
                     # #        #                 #       \___/
                      #         ###################


----------------------------------------------------------------------
----------------------------------------

INITIAL NUMBERS OF OBJECTS
--------------------------

                Layout    Source         Component Type
                ------    ------         --------------
 Ports:             13        13

 Nets:             142        13    *
```

Instances:	81	10	*	MN (4 pins)
	48	7	*	MP (4 pins)
	2	2		C (2 pins)
Total Inst:	131	19		

NUMBERS OF OBJECTS AFTER TRANSFORMATION

	Layout	Source	Component Type
Ports:	13	13	
Nets:	13	13	
Instances:	10	10	MN (4 pins)
	7	7	MP (4 pins)
	2	2	C (2 pins)
Total Inst:	19	19	

* = Number of objects in layout different from number in source.

****
****
LVS PARAMETERS
****
****

o LVS Setup:

```
   // LVS COMPONENT TYPE PROPERTY
   // LVS COMPONENT SUBTYPE PROPERTY
   // LVS PIN NAME PROPERTY
   // LVS POWER NAME
   // LVS GROUND NAME
   LVS CELL SUPPLY                        NO
   LVS RECOGNIZE GATES                    ALL
   LVS IGNORE PORTS                       NO
   LVS CHECK PORT NAMES                   NO
   LVS IGNORE TRIVIAL NAMED PORTS         NO
   LVS BUILTIN DEVICE PIN SWAP            YES
   LVS ALL CAPACITOR PINS SWAPPABLE       NO
   LVS DISCARD PINS BY DEVICE             NO
   LVS SOFT SUBSTRATE PINS                NO
   LVS INJECT LOGIC                       NO
   LVS EXPAND UNBALANCED CELLS            YES
   LVS EXPAND SEED PROMOTIONS             NO
   LVS PRESERVE PARAMETERIZED CELLS       NO
   LVS GLOBALS ARE PORTS                  YES
   LVS REVERSE WL                         NO
```

```
LVS SPICE PREFER PINS                    NO
LVS SPICE SLASH IS SPACE                 YES
LVS SPICE ALLOW FLOATING PINS            YES
LVS SPICE ALLOW UNQUOTED STRINGS         NO
LVS SPICE CONDITIONAL LDD                NO
LVS SPICE CULL PRIMITIVE SUBCIRCUITS     NO
LVS SPICE IMPLIED MOS AREA               NO
// LVS SPICE MULTIPLIER NAME
LVS SPICE OVERRIDE GLOBALS               NO
LVS SPICE REDEFINE PARAM                 NO
LVS SPICE REPLICATE DEVICES              NO
LVS SPICE STRICT WL                      NO
// LVS SPICE OPTION
LVS STRICT SUBTYPES                      NO
LAYOUT CASE                              NO
SOURCE CASE                              NO
LVS COMPARE CASE                         NO
LVS DOWNCASE DEVICE                      NO
LVS REPORT MAXIMUM                       50
LVS PROPERTY RESOLUTION MAXIMUM          32
// LVS SIGNATURE MAXIMUM
// LVS FILTER UNUSED OPTION
// LVS REPORT OPTION
LVS REPORT UNITS                         YES
// LVS NON USER NAME PORT
// LVS NON USER NAME NET
// LVS NON USER NAME INSTANCE

// Reduction

LVS REDUCE SERIES MOS                    NO
LVS REDUCE PARALLEL MOS                  YES
LVS REDUCE SEMI SERIES MOS               NO
LVS REDUCE SPLIT GATES                   YES
LVS REDUCE PARALLEL BIPOLAR              YES
LVS REDUCE SERIES CAPACITORS             YES
LVS REDUCE PARALLEL CAPACITORS           YES
LVS REDUCE SERIES RESISTORS              YES
LVS REDUCE PARALLEL RESISTORS            YES
LVS REDUCE PARALLEL DIODES               YES
LVS REDUCTION PRIORITY                   PARALLEL

// Filter

LVS FILTER  sch_filter_direct_open  OPEN SOURCE DIRECT
LVS FILTER  sch_filter_direct_short  SHORT SOURCE DIRECT
LVS FILTER  sch_filter_mask_open  OPEN SOURCE MASK
LVS FILTER  sch_filter_mask_short  SHORT SOURCE MASK
LVS FILTER  lay_filter_direct_open  OPEN LAYOUT DIRECT
LVS FILTER  lay_filter_direct_short  SHORT LAYOUT DIRECT
LVS FILTER  v  OPEN
LVS FILTER  i  OPEN
LVS FILTER  e  OPEN
LVS FILTER  f  OPEN
LVS FILTER  g  OPEN
```

```
*************************************************************************
****************************************
                                INFORMATION AND WARNINGS
*************************************************************************
****************************************


                  Matched    Matched    Unmatched    Unmatched
Component
                   Layout     Source       Layout       Source
Type
                  -------    -------    ---------    ---------    --
-------
   Ports:              13         13            0            0

   Nets:               13         13            0            0

   Instances:          10         10            0            0
MN(N)
                        7          7            0            0
MP(P)
                        2          2            0            0
C(NOTCHEDROW)
                  -------    -------    ---------    ---------
   Total Inst:         19         19            0            0


o Statistics:

   129 isolated layout nets were deleted.

   124 layout mos transistors were reduced to 12.
     112 mos transistors were deleted by parallel reduction.


o Isolated Layout Nets:

      (Layout nets which are not connected to any instances or
ports).

   14(-8.000,164.500) 15(-2.100,244.600) 16(10.100,-40.700)
17(17.900,244.600)
   18(37.900,244.600) 19(57.900,244.600) 20(77.900,244.600)
21(97.900,244.600)
   22(117.900,244.600) 23(137.900,244.600) 24(157.900,244.600)
25(177.900,244.600)
   26(197.900,244.600) 27(217.900,244.600) 28(237.900,244.600)
29(243.500,-96.900)
   30(257.900,244.600) 31(277.900,244.600) 32(297.900,244.600)
33(317.900,244.600)
   34(337.900,244.600) 35(357.900,244.600) 36(377.900,244.600)
37(395.300,137.200)
   38(397.900,244.600) 39(415.300,137.200) 40(417.900,244.600)
41(435.300,137.200)
   42(437.900,244.600) 43(455.300,137.200) 44(457.900,244.600)
45(475.300,137.200)
   46(477.900,244.600) 47(495.300,137.200) 48(497.900,244.600)
49(515.300,137.200)
```

```
   50(517.900,244.600) 51(535.300,137.200) 52(537.900,244.600)
53(555.300,137.200)
   54(557.900,244.600) 55(575.300,137.200) 56(577.900,244.600)
57(595.300,137.200)
   58(597.900,244.600) 59(604.300,58.500) 60(615.300,137.200)
61(617.900,244.600)
   62(-2.500,19.100) 63(-2.500,86.500)


o Initial Correspondence Points:

   Ports:        vout gnd vpa vdd vb vob vy voa vc vin1 vin2 vx va


*************************************************************************
****************************************
                                          SUMMARY
*************************************************************************
****************************************

Total CPU Time:      0 sec
Total Elapsed Time:  0 sec
```

(2) PEX Report

After successful completing the LVS, PEX checks the all components values in schematic with layout and give information about parasitic if they come into picture.

```
* File: layout.pex.netlist

* Created: Sat Jul 11 00:29:39 2009
* Program "Calibre xRC"
* Version "v2006.2_30.26"
*
.include "layout.pex.netlist.pex"
.subckt opampbics3c  VDD VB GND VX VOB VY VOA VC VOUT VA VIN2 VIN1
VPA
*
* VPA VPA
* VIN1      VIN1
* VIN2      VIN2
* VA  VA
* VOUT      VOUT
* VC  VC
* VOA VOA
* VY  VY
* VOB VOB
* VX  VX
* GND GND
* VB  VB
* VDD VDD
MN3__1 N_VY_MN3__1_d N_VX_MN3__1_g N_VB_MN3__1_s N_GND_MN3__1_b n
L=2.8e-06
+ W=5.84e-06 AD=6.424e-12 AS=7.008e-12
MN6__1 N_VX_MN6__1_d N_VX_MN6__1_g N_VB_MN6__1_s N_GND_MN3__1_b n
L=2.8e-06
+ W=5.84e-06 AD=6.424e-12 AS=7.008e-12
MN4__1 N_VB_MN4__1_d N_VA_MN4__1_g N_GND_MN4__1_s N_GND_MN3__1_b n
L=2.8e-06
+ W=4.9e-06 AD=5.39e-12 AS=5.88e-12
MN3__2 N_VY_MN3__2_d N_VX_MN3__2_g N_VB_MN3__2_s N_GND_MN3__1_b n
L=2.8e-06
+ W=5.84e-06 AD=7.008e-12 AS=7.008e-12
MN6__2 N_VX_MN6__2_d N_VX_MN6__2_g N_VB_MN6__2_s N_GND_MN3__1_b n
L=2.8e-06
+ W=5.84e-06 AD=7.008e-12 AS=7.008e-12
MN4__2 N_VB_MN4__2_d N_VA_MN4__2_g N_GND_MN4__2_s N_GND_MN3__1_b n
L=2.8e-06
+ W=4.9e-06 AD=5.88e-12 AS=5.88e-12
MN10__1 N_VOUT_MN10__1_d N_VX_MN10__1_g N_VB_MN10__1_s
N_GND_MN3__1_b n
+ L=2.8e-06 W=6.26e-06 AD=6.886e-12 AS=7.512e-12
MN3__3 N_VY_MN3__3_d N_VX_MN3__3_g N_VB_MN3__3_s N_GND_MN3__1_b n
L=2.8e-06
+ W=5.84e-06 AD=7.008e-12 AS=7.008e-12
MN6__3 N_VX_MN6__3_d N_VX_MN6__3_g N_VB_MN6__3_s N_GND_MN3__1_b n
L=2.8e-06
+ W=5.84e-06 AD=7.008e-12 AS=7.008e-12
```

```
MN4__3 N_VB_MN4__3_d N_VA_MN4__3_g N_GND_MN4__3_s N_GND_MN3__1_b n
L=2.8e-06
+ W=4.9e-06 AD=5.88e-12 AS=5.88e-12
MN10__2 N_VOUT_MN10__2_d N_VX_MN10__2_g N_VB_MN10__2_s
N_GND_MN3__1_b n
+ L=2.8e-06 W=6.26e-06 AD=7.512e-12 AS=7.512e-12
MN3__4 N_VY_MN3__4_d N_VX_MN3__4_g N_VB_MN3__4_s N_GND_MN3__1_b n
L=2.8e-06
+ W=5.84e-06 AD=7.008e-12 AS=7.008e-12
MN6__4 N_VX_MN6__4_d N_VX_MN6__4_g N_VB_MN6__4_s N_GND_MN3__1_b n
L=2.8e-06
+ W=5.84e-06 AD=7.008e-12 AS=7.008e-12
MN4__4 N_VB_MN4__4_d N_VA_MN4__4_g N_GND_MN4__4_s N_GND_MN3__1_b n
L=2.8e-06
+ W=4.9e-06 AD=5.88e-12 AS=5.88e-12
MN5__1 N_VA_MN5__1_d N_VA_MN5__1_g N_GND_MN5__1_s N_GND_MN3__1_b n
L=2.8e-06
+ W=4.9e-06 AD=5.39e-12 AS=5.88e-12
MN10__3 N_VOUT_MN10__3_d N_VX_MN10__3_g N_VB_MN10__3_s
N_GND_MN3__1_b n
+ L=2.8e-06 W=6.26e-06 AD=7.512e-12 AS=7.512e-12
MN3__5 N_VY_MN3__5_d N_VX_MN3__5_g N_VB_MN3__5_s N_GND_MN3__1_b n
L=2.8e-06
+ W=5.84e-06 AD=7.008e-12 AS=7.008e-12
MN6__5 N_VX_MN6__5_d N_VX_MN6__5_g N_VB_MN6__5_s N_GND_MN3__1_b n
L=2.8e-06
+ W=5.84e-06 AD=7.008e-12 AS=7.008e-12
MN4__5 N_VB_MN4__5_d N_VA_MN4__5_g N_GND_MN4__5_s N_GND_MN3__1_b n
L=2.8e-06
+ W=4.9e-06 AD=5.88e-12 AS=5.88e-12
MN5__2 N_VA_MN5__2_d N_VA_MN5__2_g N_GND_MN5__2_s N_GND_MN3__1_b n
L=2.8e-06
+ W=4.9e-06 AD=5.88e-12 AS=5.88e-12
MN10__4 N_VOUT_MN10__4_d N_VX_MN10__4_g N_VB_MN10__4_s
N_GND_MN3__1_b n
+ L=2.8e-06 W=6.26e-06 AD=7.512e-12 AS=7.512e-12
MN3__6 N_VY_MN3__6_d N_VX_MN3__6_g N_VB_MN3__6_s N_GND_MN3__1_b n
L=2.8e-06
+ W=5.84e-06 AD=6.424e-12 AS=7.008e-12
MN6__6 N_VX_MN6__6_d N_VX_MN6__6_g N_VB_MN6__6_s N_GND_MN3__1_b n
L=2.8e-06
+ W=5.84e-06 AD=6.424e-12 AS=7.008e-12
MN4__6 N_VB_MN4__6_d N_VA_MN4__6_g N_GND_MN4__6_s N_GND_MN3__1_b n
L=2.8e-06
+ W=4.9e-06 AD=5.88e-12 AS=5.88e-12
MN5__3 N_VA_MN5__3_d N_VA_MN5__3_g N_GND_MN5__3_s N_GND_MN3__1_b n
L=2.8e-06
+ W=4.9e-06 AD=5.88e-12 AS=5.88e-12
MN10__5 N_VOUT_MN10__5_d N_VX_MN10__5_g N_VB_MN10__5_s
N_GND_MN3__1_b n
+ L=2.8e-06 W=6.26e-06 AD=7.512e-12 AS=7.512e-12
MN4__7 N_VB_MN4__7_d N_VA_MN4__7_g N_GND_MN4__7_s N_GND_MN3__1_b n
L=2.8e-06
+ W=4.9e-06 AD=5.88e-12 AS=5.88e-12
MN5__4 N_VA_MN5__4_d N_VA_MN5__4_g N_GND_MN5__4_s N_GND_MN3__1_b n
L=2.8e-06
+ W=4.9e-06 AD=5.88e-12 AS=5.88e-12
```

```
MN10__6 N_VOUT_MN10__6_d N_VX_MN10__6_g N_VB_MN10__6_s
N_GND_MN3__1_b n
+ L=2.8e-06 W=6.26e-06 AD=7.512e-12 AS=7.512e-12
MN4__8 N_VB_MN4__8_d N_VA_MN4__8_g N_GND_MN4__8_s N_GND_MN3__1_b n
L=2.8e-06
+ W=4.9e-06 AD=5.88e-12 AS=5.88e-12
MN5__5 N_VA_MN5__5_d N_VA_MN5__5_g N_GND_MN5__5_s N_GND_MN3__1_b n
L=2.8e-06
+ W=4.9e-06 AD=5.88e-12 AS=5.88e-12
MN10__7 N_VOUT_MN10__7_d N_VX_MN10__7_g N_VB_MN10__7_s
N_GND_MN3__1_b n
+ L=2.8e-06 W=6.26e-06 AD=7.512e-12 AS=7.512e-12
MN4__9 N_VB_MN4__9_d N_VA_MN4__9_g N_GND_MN4__9_s N_GND_MN3__1_b n
L=2.8e-06
+ W=4.9e-06 AD=5.88e-12 AS=5.88e-12
MN2__1 N_VOA_MN2__1_d N_VIN1_MN2__1_g N_VY_MN2__1_s N_GND_MN3__1_b n
L=2.8e-06
+ W=1.4e-05 AD=1.54e-11 AS=1.68e-11
MN5__6 N_VA_MN5__6_d N_VA_MN5__6_g N_GND_MN5__6_s N_GND_MN3__1_b n
L=2.8e-06
+ W=4.9e-06 AD=5.88e-12 AS=5.88e-12
MN10__8 N_VOUT_MN10__8_d N_VX_MN10__8_g N_VB_MN10__8_s
N_GND_MN3__1_b n
+ L=2.8e-06 W=6.26e-06 AD=7.512e-12 AS=7.512e-12
MN4__10 N_VB_MN4__10_d N_VA_MN4__10_g N_GND_MN4__10_s N_GND_MN3__1_b
n
+ L=2.8e-06 W=4.9e-06 AD=5.39e-12 AS=5.88e-12
MN1__1 N_VOB_MN1__1_d N_VIN2_MN1__1_g N_VY_MN1__1_s N_GND_MN3__1_b n
L=2.8e-06
+ W=1.4e-05 AD=1.68e-11 AS=1.68e-11
MN5__7 N_VA_MN5__7_d N_VA_MN5__7_g N_GND_MN5__7_s N_GND_MN3__1_b n
L=2.8e-06
+ W=4.9e-06 AD=5.88e-12 AS=5.88e-12
MN10__9 N_VOUT_MN10__9_d N_VX_MN10__9_g N_VB_MN10__9_s
N_GND_MN3__1_b n
+ L=2.8e-06 W=6.26e-06 AD=7.512e-12 AS=7.512e-12
MN1__2 N_VOB_MN1__2_d N_VIN2_MN1__2_g N_VY_MN1__2_s N_GND_MN3__1_b n
L=2.8e-06
+ W=1.4e-05 AD=1.68e-11 AS=1.68e-11
MN5__8 N_VA_MN5__8_d N_VA_MN5__8_g N_GND_MN5__8_s N_GND_MN3__1_b n
L=2.8e-06
+ W=4.9e-06 AD=5.88e-12 AS=5.88e-12
MN10__10 N_VOUT_MN10__10_d N_VX_MN10__10_g N_VB_MN10__10_s
N_GND_MN3__1_b n
+ L=2.8e-06 W=6.26e-06 AD=7.512e-12 AS=7.512e-12
MN2__2 N_VOA_MN2__2_d N_VIN1_MN2__2_g N_VY_MN2__2_s N_GND_MN3__1_b n
L=2.8e-06
+ W=1.4e-05 AD=1.68e-11 AS=1.68e-11
MN5__9 N_VA_MN5__9_d N_VA_MN5__9_g N_GND_MN5__9_s N_GND_MN3__1_b n
L=2.8e-06
+ W=4.9e-06 AD=5.88e-12 AS=5.88e-12
MN10__11 N_VOUT_MN10__11_d N_VX_MN10__11_g N_VB_MN10__11_s
N_GND_MN3__1_b n
+ L=2.8e-06 W=6.26e-06 AD=7.512e-12 AS=7.512e-12
MN2__3 N_VOA_MN2__3_d N_VIN1_MN2__3_g N_VY_MN2__3_s N_GND_MN3__1_b n
L=2.8e-06
+ W=1.4e-05 AD=1.68e-11 AS=1.68e-11
```

```
MN5__10 N_VA_MN5__10_d N_VA_MN5__10_g N_GND_MN5__10_s N_GND_MN3__1_b
n
+ L=2.8e-06 W=4.9e-06 AD=5.39e-12 AS=5.88e-12
MN10__12 N_VOUT_MN10__12_d N_VX_MN10__12_g N_VB_MN10__12_s
N_GND_MN3__1_b n
+ L=2.8e-06 W=6.26e-06 AD=7.512e-12 AS=7.512e-12
MN1__3 N_VOB_MN1__3_d N_VIN2_MN1__3_g N_VY_MN1__3_s N_GND_MN3__1_b n
L=2.8e-06
+ W=1.4e-05 AD=1.68e-11 AS=1.68e-11
MN10__13 N_VOUT_MN10__13_d N_VX_MN10__13_g N_VB_MN10__13_s
N_GND_MN3__1_b n
+ L=2.8e-06 W=6.26e-06 AD=7.512e-12 AS=7.512e-12
MN1__4 N_VOB_MN1__4_d N_VIN2_MN1__4_g N_VY_MN1__4_s N_GND_MN3__1_b n
L=2.8e-06
+ W=1.4e-05 AD=1.68e-11 AS=1.68e-11
MN10__14 N_VOUT_MN10__14_d N_VX_MN10__14_g N_VB_MN10__14_s
N_GND_MN3__1_b n
+ L=2.8e-06 W=6.26e-06 AD=7.512e-12 AS=7.512e-12
MN7__1 N_VB_MN7__1_d N_VB_MN7__1_g N_GND_MN7__1_s N_GND_MN3__1_b n
L=2.8e-06
+ W=1.75e-05 AD=1.925e-11 AS=2.1e-11
MN2__4 N_VOA_MN2__4_d N_VIN1_MN2__4_g N_VY_MN2__4_s N_GND_MN3__1_b n
L=2.8e-06
+ W=1.4e-05 AD=1.68e-11 AS=1.68e-11
MN10__15 N_VOUT_MN10__15_d N_VX_MN10__15_g N_VB_MN10__15_s
N_GND_MN3__1_b n
+ L=2.8e-06 W=6.26e-06 AD=7.512e-12 AS=7.512e-12
MN7__2 N_VB_MN7__2_d N_VB_MN7__2_g N_GND_MN7__2_s N_GND_MN3__1_b n
L=2.8e-06
+ W=1.75e-05 AD=2.1e-11 AS=2.1e-11
MN2__5 N_VOA_MN2__5_d N_VIN1_MN2__5_g N_VY_MN2__5_s N_GND_MN3__1_b n
L=2.8e-06
+ W=1.4e-05 AD=1.68e-11 AS=1.68e-11
MN10__16 N_VOUT_MN10__16_d N_VX_MN10__16_g N_VB_MN10__16_s
N_GND_MN3__1_b n
+ L=2.8e-06 W=6.26e-06 AD=6.886e-12 AS=7.512e-12
MN7__3 N_VB_MN7__3_d N_VB_MN7__3_g N_GND_MN7__3_s N_GND_MN3__1_b n
L=2.8e-06
+ W=1.75e-05 AD=2.1e-11 AS=2.1e-11
MN1__5 N_VOB_MN1__5_d N_VIN2_MN1__5_g N_VY_MN1__5_s N_GND_MN3__1_b n
L=2.8e-06
+ W=1.4e-05 AD=1.68e-11 AS=1.68e-11
MN7__4 N_VB_MN7__4_d N_VB_MN7__4_g N_GND_MN7__4_s N_GND_MN3__1_b n
L=2.8e-06
+ W=1.75e-05 AD=1.925e-11 AS=2.1e-11
MN1__6 N_VOB_MN1__6_d N_VIN2_MN1__6_g N_VY_MN1__6_s N_GND_MN3__1_b n
L=2.8e-06
+ W=1.4e-05 AD=1.68e-11 AS=1.68e-11
MN2__6 N_VOA_MN2__6_d N_VIN1_MN2__6_g N_VY_MN2__6_s N_GND_MN3__1_b n
L=2.8e-06
+ W=1.4e-05 AD=1.68e-11 AS=1.68e-11
MN2__7 N_VOA_MN2__7_d N_VIN1_MN2__7_g N_VY_MN2__7_s N_GND_MN3__1_b n
L=2.8e-06
+ W=1.4e-05 AD=1.68e-11 AS=1.68e-11
MN8__1 N_VC_MN8__1_d N_VB_MN8__1_g N_GND_MN8__1_s N_GND_MN3__1_b n
L=2.8e-06
+ W=1.75e-05 AD=1.925e-11 AS=2.1e-11
```

```
MN1__7 N_VOB_MN1__7_d N_VIN2_MN1__7_g N_VY_MN1__7_s N_GND_MN3__1_b n
L=2.8e-06
+ W=1.4e-05 AD=1.68e-11 AS=1.68e-11
MN8__2 N_VC_MN8__2_d N_VB_MN8__2_g N_GND_MN8__2_s N_GND_MN3__1_b n
L=2.8e-06
+ W=1.75e-05 AD=2.1e-11 AS=2.1e-11
MN1__8 N_VOB_MN1__8_d N_VIN2_MN1__8_g N_VY_MN1__8_s N_GND_MN3__1_b n
L=2.8e-06
+ W=1.4e-05 AD=1.68e-11 AS=1.68e-11
MN8__3 N_VC_MN8__3_d N_VB_MN8__3_g N_GND_MN8__3_s N_GND_MN3__1_b n
L=2.8e-06
+ W=1.75e-05 AD=2.1e-11 AS=2.1e-11
MN2__8 N_VOA_MN2__8_d N_VIN1_MN2__8_g N_VY_MN2__8_s N_GND_MN3__1_b n
L=2.8e-06
+ W=1.4e-05 AD=1.68e-11 AS=1.68e-11
MN8__4 N_VC_MN8__4_d N_VB_MN8__4_g N_GND_MN8__4_s N_GND_MN3__1_b n
L=2.8e-06
+ W=1.75e-05 AD=2.1e-11 AS=2.1e-11
MN2__9 N_VOA_MN2__9_d N_VIN1_MN2__9_g N_VY_MN2__9_s N_GND_MN3__1_b n
L=2.8e-06
+ W=1.4e-05 AD=1.68e-11 AS=1.68e-11
MN8__5 N_VC_MN8__5_d N_VB_MN8__5_g N_GND_MN8__5_s N_GND_MN3__1_b n
L=2.8e-06
+ W=1.75e-05 AD=2.1e-11 AS=2.1e-11
MN1__9 N_VOB_MN1__9_d N_VIN2_MN1__9_g N_VY_MN1__9_s N_GND_MN3__1_b n
L=2.8e-06
+ W=1.4e-05 AD=1.68e-11 AS=1.68e-11
MN8__6 N_VC_MN8__6_d N_VB_MN8__6_g N_GND_MN8__6_s N_GND_MN3__1_b n
L=2.8e-06
+ W=1.75e-05 AD=2.1e-11 AS=2.1e-11
MN1__10 N_VOB_MN1__10_d N_VIN2_MN1__10_g N_VY_MN1__10_s
N_GND_MN3__1_b n
+ L=2.8e-06 W=1.4e-05 AD=1.68e-11 AS=1.68e-11
MN8__7 N_VC_MN8__7_d N_VB_MN8__7_g N_GND_MN8__7_s N_GND_MN3__1_b n
L=2.8e-06
+ W=1.75e-05 AD=2.1e-11 AS=2.1e-11
MN2__10 N_VOA_MN2__10_d N_VIN1_MN2__10_g N_VY_MN2__10_s
N_GND_MN3__1_b n
+ L=2.8e-06 W=1.4e-05 AD=1.54e-11 AS=1.68e-11
MN8__8 N_VC_MN8__8_d N_VB_MN8__8_g N_GND_MN8__8_s N_GND_MN3__1_b n
L=2.8e-06
+ W=1.75e-05 AD=1.925e-11 AS=2.1e-11
MN9 N_VPA_MN9_d N_VC_MN9_g N_GND_MN9_s N_GND_MN3__1_b n L=2.8e-06
W=7e-06
+ AD=7.7e-12 AS=7.7e-12
MP6 N_VX_MP6_d N_VX_MP6_g N_VDD_MP6_s N_VDD_MP6_b p L=2.8e-06
W=3.1e-06
+ AD=3.41e-12 AS=3.41e-12
MP5__1 N_VOUT_MP5__1_d N_VOB_MP5__1_g N_VDD_MP5__1_s N_VDD_MP5__1_b
p L=2.8e-06
+ W=1.25e-05 AD=1.375e-11 AS=1.5e-11
MP7 N_VA_MP7_d N_VA_MP7_g N_VDD_MP7_s N_VDD_MP7_b p L=2.8e-06
W=6.8e-06
+ AD=7.48e-12 AS=7.48e-12
MP5__2 N_VOUT_MP5__2_d N_VOB_MP5__2_g N_VDD_MP5__2_s N_VDD_MP5__1_b
p L=2.8e-06
+ W=1.25e-05 AD=1.5e-11 AS=1.5e-11
```

```
MP5__3 N_VOUT_MP5__3_d N_VOB_MP5__3_g N_VDD_MP5__3_s N_VDD_MP5__1_b
p L=2.8e-06
+ W=1.25e-05 AD=1.5e-11 AS=1.5e-11
MP5__4 N_VOUT_MP5__4_d N_VOB_MP5__4_g N_VDD_MP5__4_s N_VDD_MP5__1_b
p L=2.8e-06
+ W=1.25e-05 AD=1.5e-11 AS=1.5e-11
MP5__5 N_VOUT_MP5__5_d N_VOB_MP5__5_g N_VDD_MP5__5_s N_VDD_MP5__1_b
p L=2.8e-06
+ W=1.25e-05 AD=1.5e-11 AS=1.5e-11
MP5__6 N_VOUT_MP5__6_d N_VOB_MP5__6_g N_VDD_MP5__6_s N_VDD_MP5__1_b
p L=2.8e-06
+ W=1.25e-05 AD=1.5e-11 AS=1.5e-11
MP5__7 N_VOUT_MP5__7_d N_VOB_MP5__7_g N_VDD_MP5__7_s N_VDD_MP5__1_b
p L=2.8e-06
+ W=1.25e-05 AD=1.5e-11 AS=1.5e-11
MP5__8 N_VOUT_MP5__8_d N_VOB_MP5__8_g N_VDD_MP5__8_s N_VDD_MP5__1_b
p L=2.8e-06
+ W=1.25e-05 AD=1.5e-11 AS=1.5e-11
MP5__9 N_VOUT_MP5__9_d N_VOB_MP5__9_g N_VDD_MP5__9_s N_VDD_MP5__1_b
p L=2.8e-06
+ W=1.25e-05 AD=1.5e-11 AS=1.5e-11
MP5__10 N_VOUT_MP5__10_d N_VOB_MP5__10_g N_VDD_MP5__10_s
N_VDD_MP5__1_b p
+ L=2.8e-06 W=1.25e-05 AD=1.5e-11 AS=1.5e-11
MP5__11 N_VOUT_MP5__11_d N_VOB_MP5__11_g N_VDD_MP5__11_s
N_VDD_MP5__1_b p
+ L=2.8e-06 W=1.25e-05 AD=1.5e-11 AS=1.5e-11
MP5__12 N_VOUT_MP5__12_d N_VOB_MP5__12_g N_VDD_MP5__12_s
N_VDD_MP5__1_b p
+ L=2.8e-06 W=1.25e-05 AD=1.5e-11 AS=1.5e-11
MP5__13 N_VOUT_MP5__13_d N_VOB_MP5__13_g N_VDD_MP5__13_s
N_VDD_MP5__1_b p
+ L=2.8e-06 W=1.25e-05 AD=1.5e-11 AS=1.5e-11
MP3 N_VC_MP3_d N_VC_MP3_g N_VDD_MP3_s N_VDD_MP3_b p L=2.8e-06 W=7e-
06
+ AD=7.7e-12 AS=7.7e-12
MP5__14 N_VOUT_MP5__14_d N_VOB_MP5__14_g N_VDD_MP5__14_s
N_VDD_MP5__1_b p
+ L=2.8e-06 W=1.25e-05 AD=1.5e-11 AS=1.5e-11
MP5__15 N_VOUT_MP5__15_d N_VOB_MP5__15_g N_VDD_MP5__15_s
N_VDD_MP5__1_b p
+ L=2.8e-06 W=1.25e-05 AD=1.5e-11 AS=1.5e-11
MP5__16 N_VOUT_MP5__16_d N_VOB_MP5__16_g N_VDD_MP5__16_s
N_VDD_MP5__1_b p
+ L=2.8e-06 W=1.25e-05 AD=1.5e-11 AS=1.5e-11
MP5__17 N_VOUT_MP5__17_d N_VOB_MP5__17_g N_VDD_MP5__17_s
N_VDD_MP5__1_b p
+ L=2.8e-06 W=1.25e-05 AD=1.5e-11 AS=1.5e-11
MP5__18 N_VOUT_MP5__18_d N_VOB_MP5__18_g N_VDD_MP5__18_s
N_VDD_MP5__1_b p
+ L=2.8e-06 W=1.25e-05 AD=1.5e-11 AS=1.5e-11
MP5__19 N_VOUT_MP5__19_d N_VOB_MP5__19_g N_VDD_MP5__19_s
N_VDD_MP5__1_b p
+ L=2.8e-06 W=1.25e-05 AD=1.5e-11 AS=1.5e-11
MP5__20 N_VOUT_MP5__20_d N_VOB_MP5__20_g N_VDD_MP5__20_s
N_VDD_MP5__1_b p
+ L=2.8e-06 W=1.25e-05 AD=1.5e-11 AS=1.5e-11
```

```
MP1__1 N_VOA_MP1__1_d N_VOA_MP1__1_g N_VDD_MP1__1_s N_VDD_MP1__1_b p
L=2.8e-06
+ W=1.168e-05 AD=1.2848e-11 AS=1.4016e-11
MP5__21 N_VOUT_MP5__21_d N_VOB_MP5__21_g N_VDD_MP5__21_s
N_VDD_MP5__1_b p
+ L=2.8e-06 W=1.25e-05 AD=1.5e-11 AS=1.5e-11
MP2__1 N_VOB_MP2__1_d N_VOA_MP2__1_g N_VDD_MP2__1_s N_VDD_MP1__1_b p
L=2.8e-06
+ W=1.168e-05 AD=1.4016e-11 AS=1.4016e-11
MP5__22 N_VOUT_MP5__22_d N_VOB_MP5__22_g N_VDD_MP5__22_s
N_VDD_MP5__1_b p
+ L=2.8e-06 W=1.25e-05 AD=1.5e-11 AS=1.5e-11
MP2__2 N_VOB_MP2__2_d N_VOA_MP2__2_g N_VDD_MP2__2_s N_VDD_MP1__1_b p
L=2.8e-06
+ W=1.168e-05 AD=1.4016e-11 AS=1.4016e-11
MP5__23 N_VOUT_MP5__23_d N_VOB_MP5__23_g N_VDD_MP5__23_s
N_VDD_MP5__1_b p
+ L=2.8e-06 W=1.25e-05 AD=1.5e-11 AS=1.5e-11
MP1__2 N_VOA_MP1__2_d N_VOA_MP1__2_g N_VDD_MP1__2_s N_VDD_MP1__1_b p
L=2.8e-06
+ W=1.168e-05 AD=1.4016e-11 AS=1.4016e-11
MP5__24 N_VOUT_MP5__24_d N_VOB_MP5__24_g N_VDD_MP5__24_s
N_VDD_MP5__1_b p
+ L=2.8e-06 W=1.25e-05 AD=1.5e-11 AS=1.5e-11
MP1__3 N_VOA_MP1__3_d N_VOA_MP1__3_g N_VDD_MP1__3_s N_VDD_MP1__1_b p
L=2.8e-06
+ W=1.168e-05 AD=1.4016e-11 AS=1.4016e-11
MP5__25 N_VOUT_MP5__25_d N_VOB_MP5__25_g N_VDD_MP5__25_s
N_VDD_MP5__1_b p
+ L=2.8e-06 W=1.25e-05 AD=1.5e-11 AS=1.5e-11
MP2__3 N_VOB_MP2__3_d N_VOA_MP2__3_g N_VDD_MP2__3_s N_VDD_MP1__1_b p
L=2.8e-06
+ W=1.168e-05 AD=1.4016e-11 AS=1.4016e-11
MP5__26 N_VOUT_MP5__26_d N_VOB_MP5__26_g N_VDD_MP5__26_s
N_VDD_MP5__1_b p
+ L=2.8e-06 W=1.25e-05 AD=1.5e-11 AS=1.5e-11
MP2__4 N_VOB_MP2__4_d N_VOA_MP2__4_g N_VDD_MP2__4_s N_VDD_MP1__1_b p
L=2.8e-06
+ W=1.168e-05 AD=1.4016e-11 AS=1.4016e-11
MP5__27 N_VOUT_MP5__27_d N_VOB_MP5__27_g N_VDD_MP5__27_s
N_VDD_MP5__1_b p
+ L=2.8e-06 W=1.25e-05 AD=1.5e-11 AS=1.5e-11
MP1__4 N_VOA_MP1__4_d N_VOA_MP1__4_g N_VDD_MP1__4_s N_VDD_MP1__1_b p
L=2.8e-06
+ W=1.168e-05 AD=1.4016e-11 AS=1.4016e-11
MP5__28 N_VOUT_MP5__28_d N_VOB_MP5__28_g N_VDD_MP5__28_s
N_VDD_MP5__1_b p
+ L=2.8e-06 W=1.25e-05 AD=1.5e-11 AS=1.5e-11
MP1__5 N_VOA_MP1__5_d N_VOA_MP1__5_g N_VDD_MP1__5_s N_VDD_MP1__1_b p
L=2.8e-06
+ W=1.168e-05 AD=1.4016e-11 AS=1.4016e-11
MP5__29 N_VOUT_MP5__29_d N_VOB_MP5__29_g N_VDD_MP5__29_s
N_VDD_MP5__1_b p
+ L=2.8e-06 W=1.25e-05 AD=1.5e-11 AS=1.5e-11
MP2__5 N_VOB_MP2__5_d N_VOA_MP2__5_g N_VDD_MP2__5_s N_VDD_MP1__1_b p
L=2.8e-06
+ W=1.168e-05 AD=1.4016e-11 AS=1.4016e-11
```

```
MP5__30 N_VOUT_MP5__30_d N_VOB_MP5__30_g N_VDD_MP5__30_s
N_VDD_MP5__1_b p
+ L=2.8e-06 W=1.25e-05 AD=1.5e-11 AS=1.5e-11
MP2__6 N_VOB_MP2__6_d N_VOA_MP2__6_g N_VDD_MP2__6_s N_VDD_MP1__1_b p
L=2.8e-06
+ W=1.168e-05 AD=1.4016e-11 AS=1.4016e-11
MP5__31 N_VOUT_MP5__31_d N_VOB_MP5__31_g N_VDD_MP5__31_s
N_VDD_MP5__1_b p
+ L=2.8e-06 W=1.25e-05 AD=1.5e-11 AS=1.5e-11
MP4 N_VPA_MP4_d N_VC_MP4_g N_VDD_MP4_s N_VDD_MP4_b p L=2.8e-06 W=7e-
06
+ AD=7.7e-12 AS=7.7e-12
MP1__6 N_VOA_MP1__6_d N_VOA_MP1__6_g N_VDD_MP1__6_s N_VDD_MP1__1_b p
L=2.8e-06
+ W=1.168e-05 AD=1.2848e-11 AS=1.4016e-11
MP5__32 N_VOUT_MP5__32_d N_VOB_MP5__32_g N_VDD_MP5__32_s
N_VDD_MP5__1_b p
+ L=2.8e-06 W=1.25e-05 AD=1.375e-11 AS=1.5e-11
C2 N_VOUT_C2_pos N_GND_C2_neg 3.00655p
C1 N_VOB_C1_pos N_VOUT_C1_neg 1.00224p
*
.include "layout.pex.netlist.LAYOUT.pxi"
*
.ends
*
*
```