DESIGN OF LOW POWER HIGH PERFORMANCE SOI DRAM CELL

Submitted in the partial fulfillment of requirement for the award of the Degree of

MASTER OF TECHNOLOGY

IN

VLSI DESIGN AND CAD

Submitted by

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CERTIFICATE

I hereby certify that the work which is being presented in the thesis entitled **"Design of Low Power High Performance SOI DRAM Cell"** in partial fulfillment of the requirements for the award of the degree of Master of Technology in VLSI Design and CAD at the Electronics and Communication Engineering Department, Thapar University , Patiala, is an authentic record of my own work carried out under the supervision of Mr. Arun Kumar Chatterjee, Assistant Professor, ECED.

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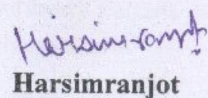

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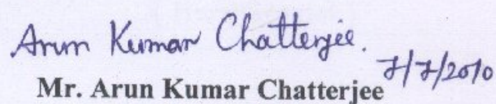

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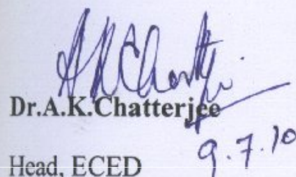

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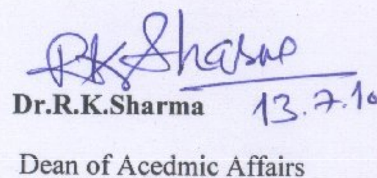

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(**Harsimranjot**)

ABSTRACT

In this thesis, the analysis and design of Dynamic Random Access Memory (DRAM) cell for low leakage have been done. For the analysis , fully-depleted SOI DRAM cell has been considered. For the design of fully-depleted SOI DRAM cell, an nMOSFET as access transistor and the floating body cell as a storage device have been considered at 30 nm process technology.

Various DRAM cell structures such as three-transistor memory cell, one-transistor one-capacitor memory cell, capacitorless one-transistor floating body cell and two-transistor floating body cell have explored.

Various leakage mechanisms, such as subthreshold leakage, Gate–induced drain leakage, punchthrough and PN junction reverse bias leakage for an access transistor have been focused. Process level techniques for leakage reduction, such as lightly doped drain, retrograde well and halo doping have been discussed and employed in the SOI DRAM cell.

Process and device simulation of fully depleted SOI DRAM cell have been carried out using the ATHENA/ATLAS packages of SILVACO. The fully depleted SOI DRAM cell structure has been generated using ATHENA and then it is used as input to device simulator ATLAS for its electrical characterization.

Leakage reduction from 2.25 nA to 10 pA in fully depleted SOI DRAM cell has been achieved using above mentioned process level techniques.

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CHAPTER 1

INTRODUCTION

Semiconductor memories are usually considered to be the most vital microelectronic component of digital logic system design, such as computers and microprocessor-based applications ranging from satellites to consumer electronics. Therefore, advances in the fabrication of semiconductor memories including process enhancements and technology developments through the scaling for higher densities and faster speeds.

Dynamic Random Access Memory (DRAM) is the most cost efficient and common type of random access memory for personal computers and workstations. Providing high-density storage has long been recognized as the principal function of the DRAMs. The term “dynamic” is used because the leakage phenomenon inherent in DRAM necessitates the periodic refreshment for the purpose of data retention. The first DRAM was proposed in 1970 with a capacity of 1 Kb. Since then, DRAMs have been the major driving force behind VLSI technology development. DRAM market has achieved an unprecedented six-fold increase in memory capacity in the last three decades - from the 1-Kbit level in 1970 to the 1- to 4-Gbit level today, as shown in Figure (1.1)[1]-[2].

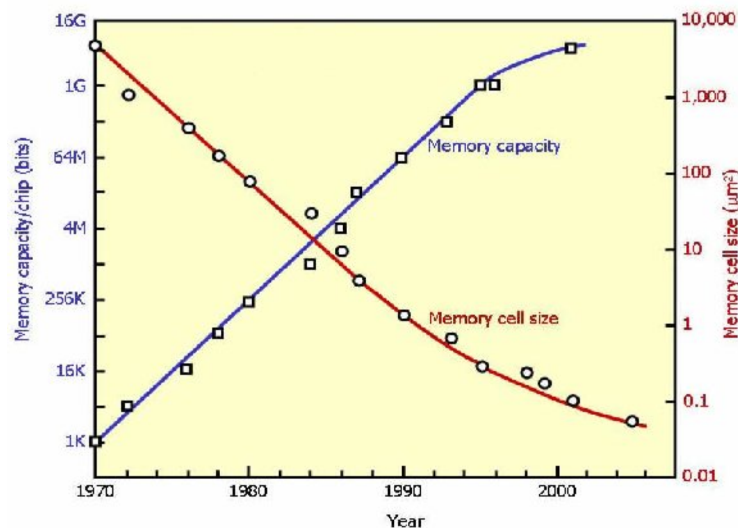

Figure 1.1: Trends in the memory cell size and memory capacity of DRAMs [1]-[2].

In this, when we design the memory chip, the memory aspect ratio should be taken into consideration. The evaluation of the dimensions of the storage array shows that its height is approximately 128,000 times larger than its width ($20^{20}/2^{3}$), assuming the shape of the basic storage cell is approximately square which is almost always the case. Obviously, this results in a design that can not be implemented. Besides the bizarre shape factor, the resulting design is also extremely slow. The vertical wires connecting the storage cells to the inputs/outputs become successively long. This increases the delay since the delay of interconnect line increases linearly with its length.

To address the above problem, memory arrays are organized so that the vertical and horizontal dimensions are of the same order of magnitude; thus the aspect ratio approaches unity. Multiple words are stored in single row and are selected simultaneously. To route the correct word to the input/output terminals, an extra piece of circuitry called the column decoder is needed. The address word is partitioned into a column address (A_0 to A_{K-1}) and a row address (A_K to A_{L-1}). The row address enables one row of the memory for R/W, while the column address picks one particular word from the selected row.

The horizontal select line that enables a single row of cells is called the word line, while the wire that connects the cells in a single column to the input/output circuitry is named the bit line.

The area of the large memory modules is dominated by the size of the memory core. Thus, it is crucial to keep the size of the basic storage cell as small as possible. Semiconductor memory cells therefore reduce the cell area by trading off some desired properties of digital circuits, such as noise margin, logic swing, input/output isolation, fan-out or speed. While a degradation of some of those properties is allowable within the confined domain of the memory core where the noise levels can be tightly controlled, this is not acceptable when interfacing with the external or surrounding circuitry.

It is common to reduce the voltage swing on the bit lines to a value substantially below the supply voltage. This reduces both the propagation delay and the power consumption.

1.1.LITERATURE SURVEY

The trends in the DRAM cell structures since its evolution have been presented and described in this chapter. This chapter reviews the DRAM cell structures such as: Three transistor memory (3T) cell, One -Transistor One -Capacitor memory (1T-1C) cell, Capacitorless One-Transistor floating body cell and Two-Transistor floating body cell.The characteristics, read/write operations and limitations of all these cell designs have been described.

1.1. Basic Memory Architecture

A memory chip is composed of three blocks: a memory cell array, a peripheral circuit, and an input/output (I/O) interface circuit. A memory cell array comprising a matrix of 2^X rows and 2^Y columns can store binary information of 2^{X+Y} bits. Any cell can be accessed at random with the same speed by selecting both the corresponding row and column.

1.1.1. Memory Cell Array

The basic array structured memory organization is shown in figure (1.1).In the memory organization, there are memory cell arrays, sense amplifiers and row and column decoders. In the memory, any word can be selected for reading and writing by providing the address word. The address word is partitioned into a column address (A_0 to A_{K-1}) and a row address (A_K to A_{L-1}). The row address enables one row of the memory for R/W, while the column address picks one particular word from the selected row. Multiple words are stored in single row and are selected simultaneously. Any cell can be accessed at random with the same speed by selecting both the corresponding row and column .To route the correct word to the input/output (I/O) terminals, an extra circuitry called the column decoder is needed. The concept is shown in figure (1.2).The horizontal select line that enables a single row of cells is called the word line, while the wire that connects the cells in a single column to the I/O circuitry is called the bit line. When design the memory chip, the memory aspect ratio should be taken into consideration. The distortion in aspect ratio results in a design that can not be implemented. Besides the bizarre shape factor, the resulting design is also extremely slow. To solve this problem, memory arrays are organized so that the aspect ratio approaches unity.

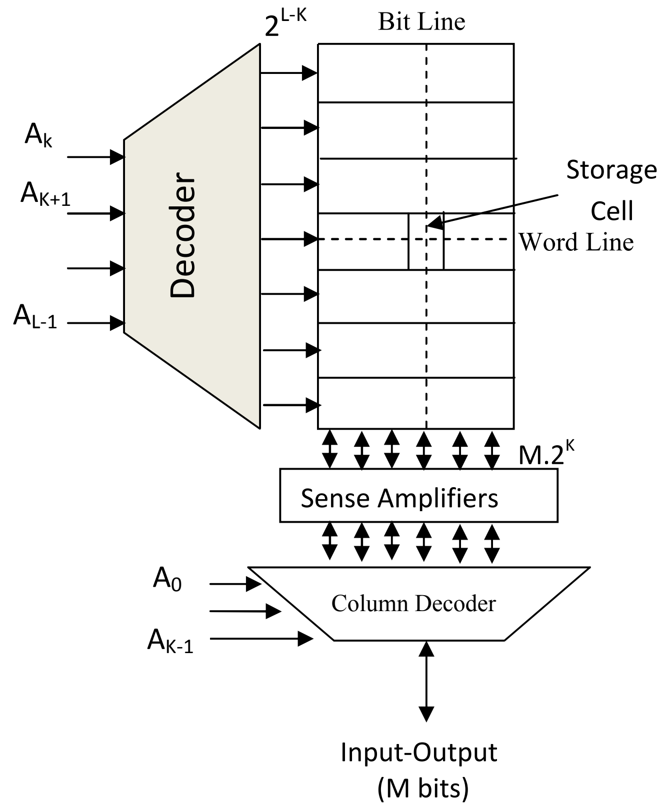

Figure 1.2:- Array-structured memory organization [3].

The area of the large memory modules is dominated by the size of the memory core. Thus, it is crucial to keep the size of the basic storage cell as small as possible. The architecture of figure (1.1) works well for memories up to a range of 64 Kbits to 256 Kbits. Larger memories start to suffer from serious speed degradation as the length, capacitance and the resistance of the word and bit lines become excessively large. In larger memories one extra dimension is added to address space.. The memory is partitioned into P smaller blocks. The composition of each of the individual blocks is identical to one of the figure (1.1). A word is selected on the basis of row and column addresses that are broadcast to all the blocks. An extra address word called the block address, selects one of the P blocks to be read or written. This approach has a dual advantage.

1. The length of the local word and bit lines is kept within bounds, resulting in faster access times.

2. The block address can be used to activate only the addressed block. Non-active blocks are put in power saving mode resulting in a substantial power saving .

1.1.2. The Peripheral Circuitry

The memory peripheral circuitry has a tremendous impact on the robustness, performance and power consumption of the memory unit. This block bridges between the memory array and the I/O interface so that they can communicate with each other. It sends write data to a memory cell in the memory array under the control of the interface circuit, or sends read data from the memory cell to the interface circuit. Any cell can be accessed at random with the same speed by selecting both the corresponding row and column The peripheral circuitry are address decoders, sense amplifiers, voltage regulators, drivers/buffers and timing control unit.

1.1.3. The Input / Output (I/O) Interface Circuit

This converts external signals, such as addresses, clocks and control signal to the corresponding internal signals that activate the peripheral circuit. In addition, it outputs read data from the array as the data output of the chip. Address buffers in The I/O interface circuit generate N and M sets of complementary row and column address signals, respectively, through the use of (N + M) external address signals. Data input and output buffers, a write control buffer, and control clock circuits are also typical components of the I/O interface circuit.

1.2. DRAM Cell Designs

The DRAM cell array usually covers 50 - 60% of the total chip area, and decreasing the cell size is the most efficient way to reduce the DRAM chip size. In early CMOS DRAM storage cell design, three-transistor and four-transistor cells were used in 1-Kb and 4-Kb generations. Later, one-transistor cell, providing smaller cell size and low cost, became the industry standard. In further attempts to scale the memory cell size, the concept of capacitorless single transistor cell was proposed. This concept utilizes the floating body effect of SOI MOSFET. This section describes all these cell structures and their read and write operations.

1.2.1. Three-Transistor (3T) Memory Cell

The three-transistor cell is shown in figure (2.2) formed the core of the first popular MOS semiconductor memories such as the first 1-Kbit memory from Intel.

Read/Write Operation

The cell is written to by placing the appropriate data value on BL1 and asserting the write-word line (WWL). The data is retained as charge on capacitance C_s once WWL is lowered. To read the data, the read-word line (RWL) is raised. The storage transistor (M_2) is either on or off depending upon the stored value. The BL2 is precharged to either V_{DD} or V_{DD} – V_{T}.. The series connection of M_2 and M_3 pulls BL2 low when a 1 is stored.BL2 remains high when'0' is stored. The inverse value of the stored signal is sensed on the bit line. The most common approach to refreshing the cell is to read the stored data, put its reverse on BL1, and assert WWL in consecutive order

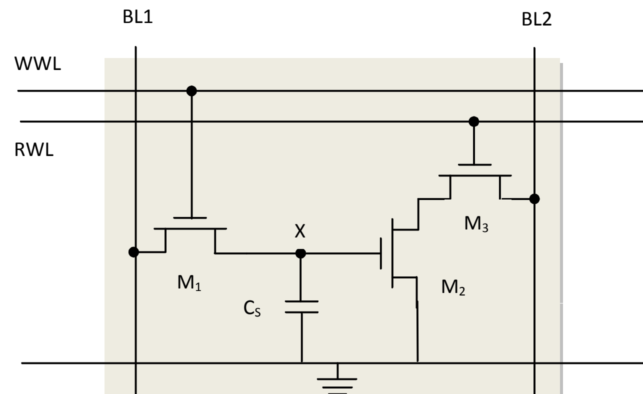

Figure 1.3:- Three-transistor dynamic memory cell[3].

Properties of the 3T cell are as follows:

1. Unlike SRAM cell, there is no constraints on the device ratios. The choice of device sizes is solely based on performance and reliability considerations.
2. Reading the 3T cell contents is nondestructive.

3. No special process steps are needed. The storage capacitance is nothing more than the gate capacitance of the readout device.
4. There is a threshold voltage loss when writing a '1' at the storage node; this reduces the current flowing through M_2 during a read operation and increases the read access time. Bootstrapping the word line voltage is the solution.

1.2.2. One-Transistor One-Capacitor (1T-1C) Memory Cell

The schematic for one-transistor one-capacitor (1T-1C) DRAM cell is shown in figure (2.3). It consists of a MOSFET (also referred to as the array-access transistor or transfer device) in series with a storage capacitor. The word line (WL) contacts the gate of the access transistor, and the bit line (BL) contacts the source/drain of the access transistor that is not connected to the storage capacitor. The bit line has a capacitance C_{BL}, including the parasitic load of connected circuits.

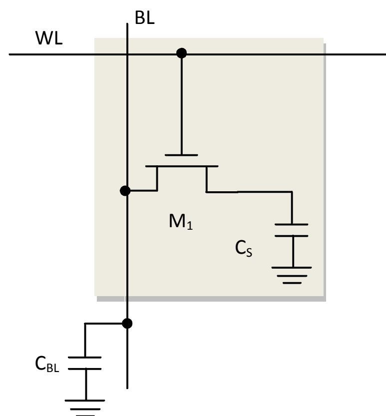

Figure 1.4:- One-transistor dynamic memory cell [3].

Read/Write Operation

During a write cycle, the data value is placed on bit line BL, and data is written by turning on the transfer device by raising the word line and writing a high or low voltage level onto the storage capacitor via the bit line. Depending on the data value, the cell capacitance is either charged or discharged. Data is stored by turning off the transfer device by lowering the word

line, trapping the voltage/charge on the storage capacitor. Before a read operation is performed, the bit line is precharged to a voltage V_{PRE}, midway between the high and low levels. The transfer device ia then turned on by asserting the word line. Upon asserting the word line, charge redistribution takes place between the bit line and storage capacitance. This results in a voltage change on the bit line, the direction of which determines the value of the data stored. The magnitude of the swing is given by the expression [3],

$$\Delta \quad = \quad - \quad = (\quad - \quad) \frac{\quad}{+}$$

where C_{BL} is the bit line capacitance, V_{BL} is the potential of the bit line after the charge redistribution, and the V_{BIT} the initial voltage over the cell capacitance C_S. As the cell capacitance is normally one or two orders of magnitude smaller than the bit line capacitance, the voltage change is very small, typically around 250 mV for state-of-the-art memories. Upon asserting the word line, charge redistribution takes place between the bit line and storage capacitance. The ratio $C_S/(C_S + C_{BL})$ is called the charge-transfer ratio and ranges between 1% and 10%.Amplification of Δ to the full voltage swing is necessary if functionality is to be achieved. The cross sectional view of conventional planar capacitor DRAM cell is shown in the figure(1.5) given below.

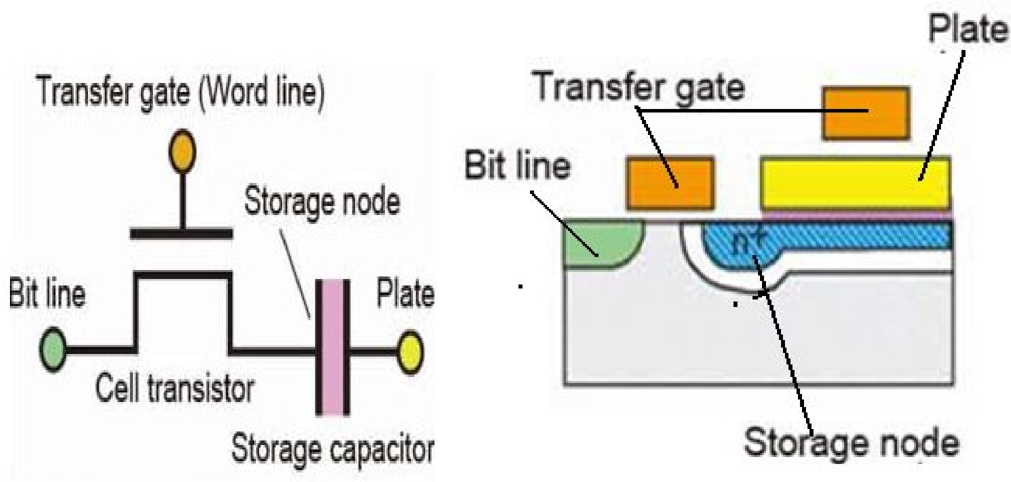

Figure 1.5:-Cross-sectional view of conventional planar capacitor DRAM cell[4].

The characteristics of 1T cell are:-

1. A 1T DRAM requires a sense amplifier for each bit line to be functional. The DRAM memory cells are single ended; it complicates the design of the sense amplifier.
2. The readout of the 1T DRAM cell is destructive and data refreshing is necessary.
3. It requires an extra capacitance.. For reliability, the charge-transfer ratio is kept large, with the minimum value of the capacitance ranging around 30 fF. Fitting that large of a capacitance in as small an area is challenge to DRAM designs.
4. When writing a 1 into the cell, a threshold voltage is lost, which reduces the available charge. This charge loss can be circumvented by bootstrapping the word lines.

Limitations

Scaling of cell size poses processing complexity due to the capacitors.

1.2.2.1. Three dimensional cell structures

Advanced cell structure design activities therefore focused on how to arrange these two components (one transistor and one capacitor) by using advanced processing techniques to meet the design criteria. The major effort has been to use the third dimension in the cell structure.

1.2.2.1.1. Stacked Capacitor Cell (STC Cell)

One approach is to stack the capacitor over the access transistor (STC cell), Figure (1.6) [5]. Advantages of this cell are the use of the space over the transistor for the storage capacitor area,

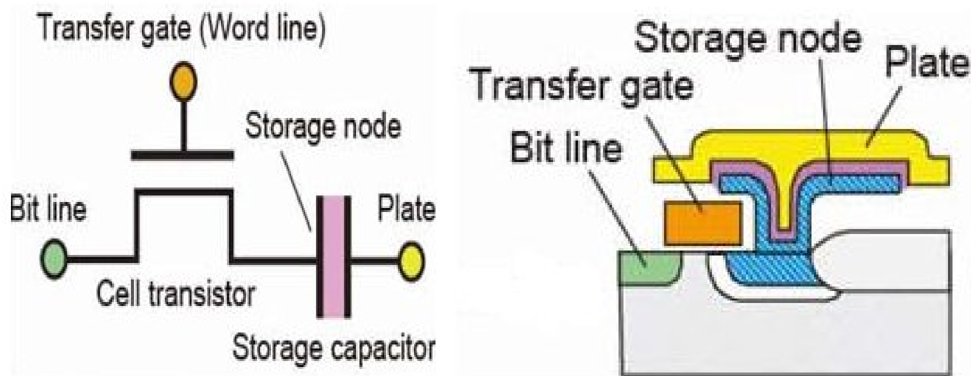

Figure 1.6:-Cross-sectional view of stacked capacitor DRAM cell [4].

low soft error rate, and the configuration is particularly suitable for the use of a high dielectric-constant insulator between two poly layers without the dielectric contacting the bulk silicon.

The difficulties are how to manage the large surface topography and how to keep high dielectric breakdown between poly layers with scaled insulator thickness. Another difficulty for the cell is that one buried contact without self-alignment is needed for the capacitor connection per cell, thus making the cell area hard to scale. In moving toward higher density DRAMs, the cell storage area will be restricted unless the capacitor storage polysilicon electrode is made thick enough to increase the sidewall areas for charge storage or a low leakage, very high dielectric-constant storage insulator can be used.

1.2.2.1.2.Trench Capacitor Cell

Another approach is to use a trench capacitor cell, Figure (1.7) [5]. Since all four sidewalls and the bottom of the trench can be used for the capacitor electrode, the storage area is greatly enhanced with even reduced planar surface area for the capacitor.

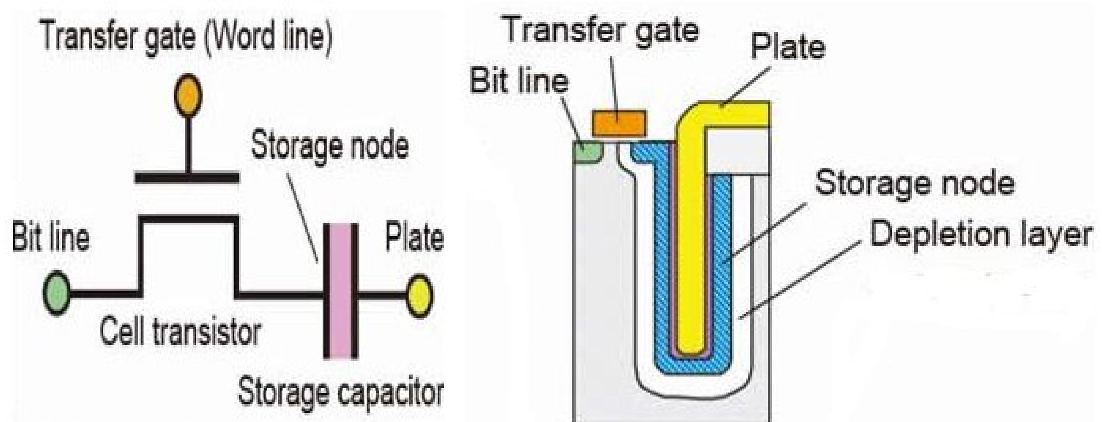

Figure 1.7:-Cross-sectional view of trench capacitor DRAM cell [4].

However, there are some design concerns in this original trench capacitor structure. Because the signal charge is stored at the trench surfaces in the bulk silicon, the expanded storage area results in high susceptibility to minority- carrier leakage disturbance, leading to high leakage and soft error rate. Moreover, unless a deep isolation is used, the minimum distance between trenches and from the trench storage node to the active devices of adjacent cells is limited

because of possible junction punchthrough. One solution is to increase the background doping concentration to narrow the depletion region; however, this increases the electric field around the junction, which may cause avalanching. Another solution is to form Hi-C doping profiles at the trench surfaces by using more complicated sidewall doping techniques, though the trench spacing can still be limited by the diffusion depths of doping profiles and depletion regions.

Limitations of three-dimensional cell structures

DRAM is much denser than SRAM but the capacitor poses the problem as the device shrinks. The capacitor can not shrink much because it must stay large enough to store a detectable amount of charge while the transistors continue to scale into the infinitesimal. The growing mismatch between the size of transistors and that of capacitors has led to strange-looking arrangements, such as capacitors built as narrow trenches having a depth many times greater than the chip's transistors. Another configuration has relatively enormous fin-shaped capacitors built above the silicon in the area that usually holds the chip's wiring. In both the cases,the aspect ratio of the cell structure is distorted. Both arrangements are too expensive to put any logic chip, requiring several extra manufacturing steps [6].

1.3. Capacitorless One-Transistor Floating Body Cell (1T FBC)

1.3.1. Z-RAM

Many companies (Intel, Toshiba, IBM, STMicroelectronics, and others) have investigated floating body memories. However, Innovative Silicon, Inc. (ISi) – a memory technology company founded in 2002 – recognized that a conventional approach to creating a floating body memory was unlikely to lead to a manufacturable product. Instead, the company stepped back from product development and refocused its efforts on researching some of the more fundamental aspects of floating body memories.

Those efforts have resulted in Z-RAM, a revolutionary new type of floating body memory. Although functionally similar to other floating body memories, Z-RAM improves upon them by storing a significantly larger charge in a smaller transistor. This increased amount of

charge greatly improves the amount of time the memory can retain its state, as well as the signal margin between a ‘1’ and a ‘0’ state. Other improvements include faster read and write speeds while simultaneously reducing write power.

Read/Write Operation

Previous approaches to floating body memories have used the MOS transistor to pass current and create charge in the body using impact ionization. Although memory functionality can be demonstrated, the amount of charge created is insufficient to create a robust and manufacturable memory device.

Z-RAM utilizes the bipolar transistor intrinsic in the SOI MOS structure to create charge (Figure (1.8)). This approach allows a much larger charge to be created and stored due to the increased capacitance of the memory cell.

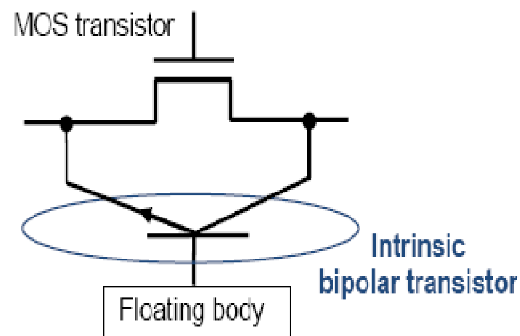

Figure 1.8:- Intrinsic Bipolar Transistor [9].

If we consider an n-channel device, the N+ source, the P-type body and the N+ drain form the emitter, base and collector respectively of an NPN bipolar transistor. The body of the MOS transistor is the base of the bipolar transistor and is used as a storage node.

To write a ‘1’ into a Z-RAM memory cell, the intrinsic bipolar transistor is triggered, causing current to flow throughout the transistor body. This differs significantly from MOS behavior where current flows only at the interface. Charge collects at the interface due to the slight bias at the gate. The impact ionization effect used to create an excess of majority carriers in the floating body is more efficient in this bipolar bit cell structure, charging the body quickly, resulting in a very rapid write time. Z-RAM memory is read using a similar mechanism which senses the bipolar current through the transistor.

The signal margins of the Z-RAM cell are superior to other floating body memories due to the large current gain available from the bipolar device. By innovative Silicon's estimates, replacing the conventional memory with Z-RAM would shrink a chip. That would boost the number of chips per wafer and cut the final cost of the chip almost in half [6].

Limitations of 1T floating body cell design:

Although the removal of the external capacitor reduces area overhead and the process complexities, the scaling of this 1T-DRAM has its own specific challenges.

- The 1T-FBC signal margin (ΔI_{DS}) is restricted because the attainable ΔV_t is fundamentally limited. Thus, wide devices and several parallel fins are needed to increase the current to get acceptable ΔI_{DS}, and this undermines the memory density actually achievable.
- It requires the bias-induced accumulation, which complicates the cell/chip design, undermines reliability, and sacrifice layout area.
- It relies on current based sensing of the stored data, which is less desirable than conventional voltage based sensing because of varying ΔI_{DS}, and hence, more complex sensing circuitry and added power consumption.

1.4. Two-Transistor Floating Body Cell (2T FBC)

The major disadvantage of restricted signal margin in 1T FBC can be overcome by a novel two-transistor (2T) FBC that can be yield much better signal margin and density, while offering other significant advantages over the 1T cell([10],[11]). The 2T FBC concept is conceived from an insightful understanding of the basic IT FBC operation.

A memory array based on the 2T FBC is shown in Figure (1.9). The cell comprises transistors T1 and T2, with the body (B1) of T1 connected to, or driving the gate (G2) of T2; in essence, B1 is a floating gate on T2. The write/erase operations are done by charging/discarging the floating body of T1, as in the 1T FBC. But the stord data are read via T2 with $\Delta V_{GS2} = \Delta V_{BS} > \Delta V_T$, which implies about a $2 \times (1/2r)$ density increase for the same current-signal margin. Two bit lines are needed : one (BL1) connecting all drain nodes

of the T1 transistors in a column of the DRAM array for programming the cells, and the other (BL2) connecting all drain nodes of the T2 transistors in the column to sense the data. Preffered voltage sensing at the (precharged) drain node of T2 can be used, which exploits the amplification of V_{BS} by T2 will be turned on and off by V_{BS} corresponding to the charged discharged T1 body. Since T2 inverts, stored '0' and '1' correspond to the T1 body being charged and discharged respectively.

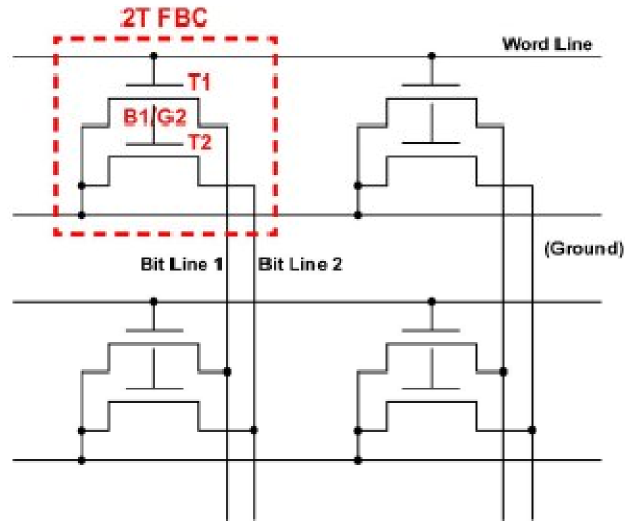

Figure 1.9:- The basic 2T Floating Body Cell [10].

Appropriate WL pulsing for 'read' is needed to raise the BL1 voltage to a level sufficiently above or below V_T of T2 for stored '0' or '1'. This operation is confirmed by the predicted transient drain voltage (BL2) of T2, which needs to be precharged before reading. Indeed, with the T1 body charged (stored '0'),BL2 drops quickly to 0 V, as V_{B1} turns on T2. With the T1 body discharged (stored '1'), BL2 remains at its precharged value as V_{B1} remains well below V_T. The efficient reads of both '0' and '1' are done with reasonable WL and BL1 voltage pulsing. The 2T concept is compatible with any SOI technology, like the 1T FBC.

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CHAPTER 2

CONCEPTS OF FLOATING BODY CELL

2.1. SOI MOSFET

As CMOS goes nanoscale, the integration of standard 1T/1C DRAMs becomes very challenging because the required value of the capacitor imposes a minimal area and because the leakage of the access transistor must remain low. As a consequence, alternative memory devices, dense and functional at nanoscale, are devices of great interest for sub–65–nm CMOS generations. In this context, floating-body MOSFETs stand as a very promising architecture.

This floating body memory cell uses a floating body of partially depleted (PD) silicon-on-insulator (SOI) MOSFET as a storage node rather than using an external capacitor. Therefore, this 1T-DRAM does not need a complicated storage capacitor and this means that the cell has a good process compatibility with logic devices. As bulk silicon devices are now starting to face a number of critical limitations, SOI devices become extremely attractive because of the advantages in high speed, low power dissipation and extended scalability. This concept of floating body effect can allow the DRAM cell to be scaled down in depth with less area occupied. The primary advantages of SOI DRAM's are the superior soft error rate and static data-retention time, which promise for higher integration density than bulk-Si DRAM's.

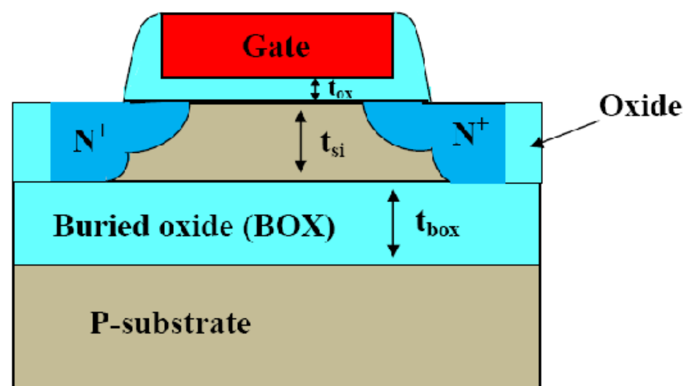


Figure 2.1:- cross sectional view of an SOI nMOSFET[7].

2.1.1 Fully-depleted SOI MOSFET

In this,the retention time can be improved. The buried oxide eliminates the source and drain junction leakages and also isolates each cell from every other cell in the array. The two mechanism are there static and dynamic. By static operation, we mean the mode when the bit line voltage remains at midway between high and low levels. In the dynamic mode,the bit line voltage is swinging between the high and low values. In DRAM built with FDSOI devices, the leakage current in the junction is negligible in static mode. Irrespective of what value the cell is storing, no holes accumulate in the body to increase the body potential. The reason for this is that the source body potential barrier is very low in FDSOI and all holes injected will easily be swept into the source without increasing the body potential. Due to this, when bit line voltage changes no diffusion mechanism in FDSOI to discharge the storage capacitor. This provides long retention time.

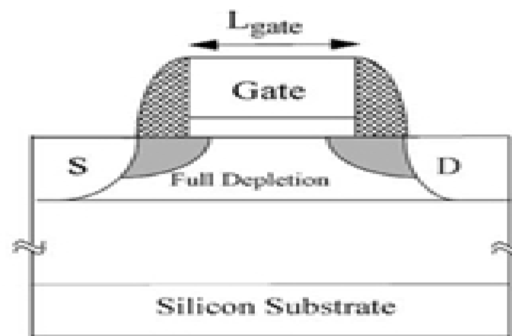


Figure2.2:- Schematic of a FDSOI MOSFET [21].

2.1.2. Partially-Depleted SOI MOSFET

In this device, during the static mode negligible junction current flows because of dielectric isolation. However, in a cell that stores high value, holes get accumulated in the floating body of the device. The accumulated holes increase the body potential and as a result decrease the threshold voltage and thus cause more subthreshold leakage. When the bit line swings dynamically more effect appear due to floating body. When the bit line voltage goes low to write ‘0’ into another cell connected to the same bit line, the source-to-body potential barrier decreases. The accumulated holes in the body diffuse into the source and electrons

diffuse from the source into body. The electrons injected into the body are collected by the drain resulting in a leakage current which discharges the storage capacitor to zero.

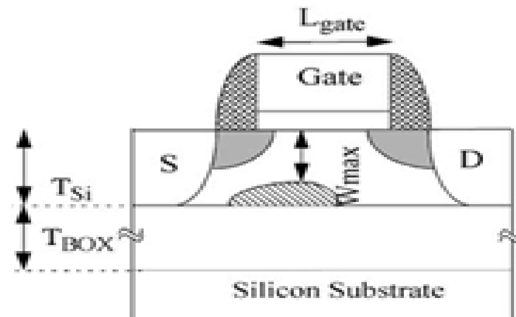


Figure 2.3:-Schematic of PDSOI MOSFET [21].

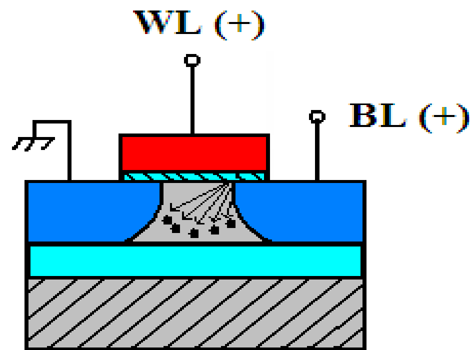
2.2. Capacitorless One-Transistor Floating Body Cell (FBC)

The most fundamental device-design issue is the choice between a fully depleted device versus a partially depleted device. In a fully depleted device, ultrathin (< 50 nm or so) silicon film is used so the depletion layer extends through the entire film. The advocated advantages include the elimination of the floating-body effect and better short-channel behavior. However, the claimed better short-channel behavior stems from the reduced source/drain junction depth and is traded against the source/drain series resistance. Furthermore, the requirement that the silicon film thickness always remain well below the depletion width dictates a low device threshold voltage V_t with high sensitivity to process and thickness variations and stringent control of the film thickness to within 5–10 nm, which impose severe limitations on the manufacturability of the device. A partially depleted device (with film thickness around 150 nm) alleviates the constraint on V_t and its sensitivity, allowing the channel doping profile to be tailored for any desired V_t and thus easing the manufacturing problem. The major issue of the partially depleted device is the “floating-body effect” and the resulting parasitic bipolar effect. The floating region under the MOS device channel acts as the base of the parasitic lateral bipolar device, with the base current supplied by impact ionization. The floating body has been known to introduce a kink in the DC I–V characteristics, lower the at high drain bias, degrade breakdown voltage, and cause hysteresis and instability during dynamic operations.

Read/Write Operation

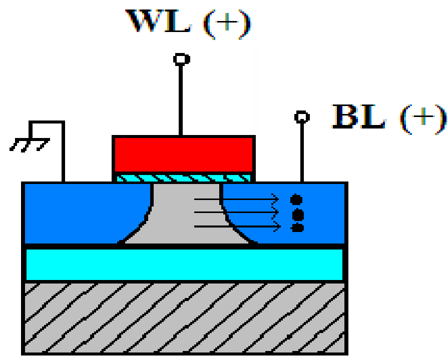
The floating body cell consists of a MOSFET whose body is electrically floating and is used as a storage node of electric charge. An nMOSFET formed on PD-SOI were chosen as a candidate to realize this concept. For this DRAM cell, a logic state is defined by creating an excess or a shortage of the majority carriers (ΔQ) inside the body of the transistor. This causes a shift in the body potential ΔV_b below or above its equilibrium given by $\Delta V_b = \Delta Q/C_{si}$, where C_{si} is the silicon body capacitance. As a result, there is a shift in the threshold voltage ΔV_t, which is directly proportional to ΔV_b. The state is read by sensing the drain current, which has two different levels corresponding to the ΔV_t shift, and this distinguishes the two states.

The operation principle of the FBC is also explained as shown in Figure (2.4). The cell senses whether the majority carriers (holes) accumulate in the floating-body as the threshold voltage (V_t) changes. For write operation, the source of the FBC is biased to 0 V (GND), the drain is connected to a bit line (BL), and the gate is connected to a word line (WL). To write data, the nMOSFET is operated in saturation leading to impact ionization which injects holes into the body. When excess holes exist in the floating body and V_t lowers, the cell state can be regarded as "1".



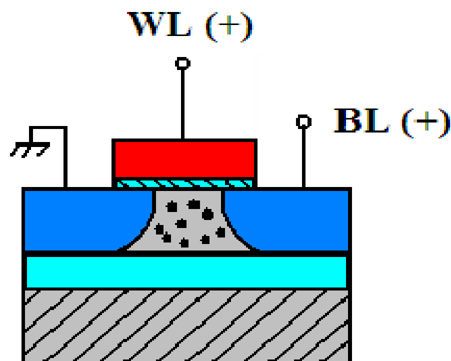
(a) '1' write

To write data "0", the p-n junction between the body and the drain is forward-biased, ejecting the stored holes from the body. When excess holes are swept out of the floating body by a forward bias and V_t becomes higher, the cell state can be regarded as "0". To read the data, the nMOSFET is operated in a linear ohmic region so as to keep the data state "0".



(b) ‘0’ write

From being violated by impact ionization, it leads to a drain current difference due to the body effect depending on the number of holes stored in the body. This difference can be read and sensed. The drain current difference ΔI_{ds}, which is the current for the data state “1” I_1 minus the current for the data state “0” I_0, is a function of the WL bias. By performing a read operation in the linear current region, the 1T-DRAM cell achieves the nondestructive read operation during a refresh interval. However, the FBC is volatile and needs to be refreshed, because holes are generated in the body of the data state “0” through the PN junction reverse-bias leakage current between the body and the source/drain and they need to be bailed out in order to maintain the difference in the number of holes between the data “1” and the data “0”.



(c) Read

Figure 2.4:- The principle of the FBC during write “1” and “0” and read [7].

Several designs of this cell based on both partially depleted (PD) and fully depleted (FD) SOI technologies have been proposed.

CHAPTER 3

LEAKAGE MECHANISMS AND REDUCTION TECHNIQUES IN SOI DRAM CELL

In DRAM, every memory cell experiences leakage current which consumes part of the stored charge. As the DRAM cell size shrinks, the leakage increases. The duration till the stored signal can be read out successfully is called data retention time .The product refresh time is determined by the minimum retention time. Therefore, to maintain the desired data retention time, the leakage current must be kept within the acceptable limit. In this chapter, various leakage currents responsible for data degradation in SOI DRAM cell are discussed.

DRAM data retention time can be expressed as [12]:

$$T_{ret} = \frac{C_S \cdot \frac{1}{2} V_{CC} - \Delta V_{BL} \cdot (C_S + C_{BL})}{I_{Leak}} \quad \ldots\ldots(2)$$

.

where T_{ret} is the retention time and C_S, C_{BL} , I_{LEAK} , V_{CC} and ΔV_{BL} are the storage capacitance, bit line capacitance, total leakage current, bitline operation voltage, and sense voltage, respectively. From the above equation, we can see that the retention time depends strongly on the storage capacitance, bit line capacitance and cell leakage. In order to retain the data for longer time, it is required to reduce the leakage as much as possible. With DRAM scaling. the leakage must be kept as low as 1 fA per cell for each technology generation to maintain the required retention time [12]. So, the leakage reduction of a DRAM cell is very important design issue.

There are several leakage current components, that degrade the stored signal in a fully depleted SOI DRAM cell [12], [13]:

(a). Gate-induced drain leakage (GIDL);
(b). Junction leakage from storage node;
(c). Subthreshold leakage of the cell transistor;
(d). Parasitic vertical transistor leakage;
(e). Isolation leakage between the neighboring cells;
(f). Capacitor node dielectric leakage current;
(g). Gate leakage;
(h). Passing word line leakage;

The sum of all leakages determines the total leakage current and therefore limits the maximum data retention time of the specific cell.

High leakage current in deep-submicrometer regimes is also becoming a significant contributor to power dissipation of CMOS circuits. Consequently, the identification, modeling and minimization of different leakage components of individual cells is very important aspect of cell designing for the improvement of data retention time and for estimation and reduction of leakage power, especially for low-power applications. In this thesis, DRAM access transistor's intrinsic leakage mechanisms specifically sub threshold leakage, GIDL and punch through have been focused.

3.1. DRAM Access Transistor Leakage Mechanisms

Transistor off-state current (I_{OFF}) is the drain current when the gate voltage is zero. I_{OFF} is influenced by the threshold voltage, channel physical dimensions, channel/surface doping profile, drain/source junction depth, gate oxide thickness and V_{DD}. In long-channel devices, I_{OFF} is dominated by leakage from the drain-well and well-substrate reverse biased pn junctions. Short-channel transistors require lower power supply levels to reduce their internal electric fields and power consumption. This forces a reduction in the threshold voltage that causes substantially large increase in I_{OFF}. This increase is due to the weak inversion state leakage and is a function of V_T. In figure (4.2), six short-channel leakage mechanisms are illustrated. I_1 is the reverse-bias pn junction leakage; I_2 is the sub threshold leakage; I_3 is the GIDL; I_4 is the channel punch through

current; I_5 is the oxide tunneling current and I_6 is the gate current due to hot carrier injection.

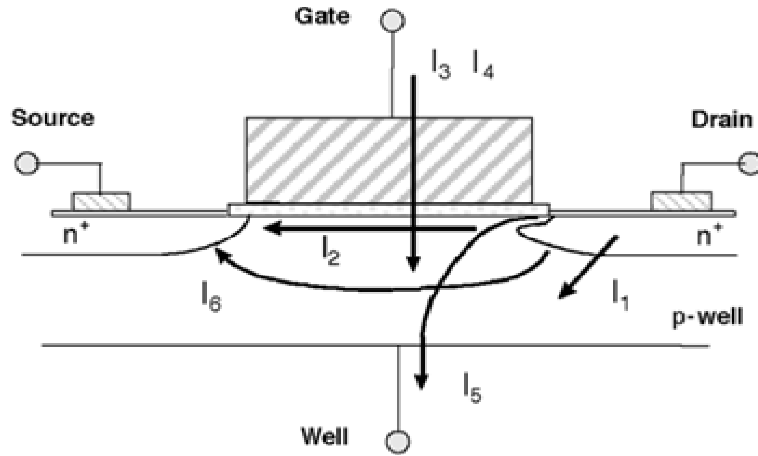


Figure 3.1:-Leakage current mechanisms of deep-submicrometer transistors [14].

3.1.1. PN Junction Reverse Bias Current (I_1)

Drain and source to well junctions are typically reverse biased, causing pn junction leakage current. A reverse-bias pn junction leakage has two main components: one is minority carrier diffusion/drift near the edge of the depletion region; the other is due to electron-hole pair generation in the depletion region of the reverse-biased junction [14]. For an MOS transistor, additional leakage can occur between the drain and well junction from gated diode device action (overlap of the gate to the drain-well pn junctions) or carrier generation in drain to well depletion regions with influence of the gate on these current components. PN junction reverse-bias leakage is a function of junction area and doping concentration. If both n and p regions are heavily doped band-to-band tunneling (BTBT) dominates the pn junction leakage.

3.1.1.1. Band-to-Band Tunneling Current

High electric field (10^6 V/cm) across the reverse-biased pn junction causes significant current to flow through the junction due to tunneling of electrons from the valence band of the p region to the conduction band of the n region. For the tunneling to occur, the total

voltage drop across the junction has to be more than the band gap. The tunneling current density is given by [14],

$$J_{b-b} = A \frac{EV_{app}}{E_g^{1/2}} exp\left(-B \frac{E_g^{3/2}}{E}\right) \quad ......(3)$$

Where,

$$A = \frac{\sqrt{2m^*}\, q^3}{4\pi^3 \hbar^2} \quad ......(4)$$

$$B = \frac{4\sqrt{2m^*}}{3q\hbar} \quad ......(5)$$

where m' is effective mass of electron; E_g is the energy-band gap; V_{app} is the applied reverse bias; E is the electric field at the junction; q is the electronic charge; and h is1/2π times Planck's constant. Assuming a step junction, the electric field at the junction is given by [14],

$$E = \sqrt{\frac{2q\, N_a N_d (V_{app} + V_{bi})}{\varepsilon_{si}\ (N_a + N_d)}} \quad ......(6)$$

where N_a and N_d are the doping in the p and n side, respectively; ε_{si} is permittivity of silicon; and V_{bi} is the built In voltage across the junction. In scaled devices, high doping concentrations and abrupt doping profiles cause significant BTBT current through the drain-well junction.

3.1.2. Subthreshold Leakage (I_2)

Subthreshold or weak inversion conduction current between source and drain in an MOS transistor occurs when gate voltage is below threshold voltage, V_{th}. In the weak inversion, the minority carrier concentration is small, but not zero. Let us consider that the source of the n-channel MOSFET is grounded, $V_g < V_{th}$, and the drain to source

voltage $|V_{ds}| \geq 0.1$ V. For such weak inversion condition, V_{ds} drops almost entirely across the reverse biased substrate-drain pn junction. As a result, the variation of the electrostatic potential Φ_s at the semiconductor surface along the channel is small. The component of the electric field vector E, along the channel, is also small. With both the number of mobile carriers and the longitudinal electric field small, the drift component of the subthreshold drain-to-source current is negligible. Therefore, unlike the strong inversion region in which the drift current dominates, the subthreshold conduction is dominated by the diffusion current. The carriers move by diffusion along the surface. Weak inversion typically dominates modern device off-state leakage due to the low V_{th} . The weak inversion current can be expressed based on the following [14]:

$$I_{ds} = \mu_0 C_{ox} \frac{W}{L}(m-1)(v_T)^2 \times e^{(V_g - V_{th})/mv_T} \times \left(1 - e^{-v_{DS}/v_T}\right) \quad \ldots\ldots(7)$$

where

$$m = 1 + \frac{C_{dm}}{C_{ox}} = 1 + \frac{\frac{\varepsilon_{si}}{W_{dm}}}{\frac{\varepsilon_{ox}}{t_{ox}}} = 1 + \frac{3t_{ox}}{W_{dm}} \quad \ldots\ldots(8)$$

where V_{th} is the threshold voltage, and $v = KT/q$ is the thermal voltage. C_{ox} is the gate oxide capacitance; μ_o is the zero bias mobility; and m is the subthreshold swing coefficient (also called body effect coefficient). W_{dm} is the maximum depletion layer width, and t_{ox} is the gate oxide thickness. C_{dm} is the capacitance of the depletion layer. In long-channel devices, the subthreshold current is independent of the drain voltage for V_{DS} larger than a few v_T . On the other hand, the dependence on the gate voltage is exponential. The inverse of the slope of the $\log_{10}(I_{ds})$ versus V_{gs} characteristic is called the subthreshold slope (S_t) [14] and is given by

$$S_t = \left(\frac{d(\log_{10} I_{ds})}{dV_{gs}}\right)^{-1} = 2.3\frac{mkT}{q} = 2.3\frac{kT}{q}\left(1 + \frac{C_{dm}}{C_{ox}}\right) \quad \ldots\ldots(9)$$

Subthreshold slope indicates how effectively the transistor can be turned off (rate of decrease of I_{OFF}) when V_{gs} is decreased below V_{th}. As device dimensions and the supply

voltage are scaled down to enhance performance, power efficiency, and reliability, subthreshold characteristics may limit the scalability of the supply voltage. The parameter S_t is measured in millivolts per decade of the drain current. For the limiting case of $t_{ox} \rightarrow 0$ and at room temperature, $S_t \approx$ 60 mV/decade. Typical S_t values for a bulk CMOS process can range from 70 to 120 mV/decade. A low value for subthreshold slope is desirable. It can be seen from the preceding expression (9) that S_t can be made smaller by reducing t_{ox} or a lower substrate doping concentration. Changes in lower temperature or a substrate bias also modifies S_t .The factors affecting the subthreshold current are described in the following subsections.

3.1.2.1. Drain-Induced Barrier Lowering

In long-channel devices, the source and drain are separated far enough that their depletion regions have no effect on the potential or field pattern in most part of the device. Hence, for such devices, the threshold voltage is virtually independent of the channel length and drain bias. In a short-channel device, however, the source and drain depletion width in the vertical direction and the source drain potential have a strong effect on the band bending over a significant portion of the device. Therefore, the threshold voltage, and consequently the subthreshold current of short-channel devices, vary with the drain bias. This effect is referred to as drain induced barrier lowering (DIBL). One way to describe it is to consider the energy barrier at the surface between the source and drain. Under off conditions, this potential barrier prevents electrons from flowing to the drain. For a long channel device, the barrier height is mainly controlled by the gate voltage and is not sensitive to V_{DS}. The barrier of a short-channel device reduces when the depletion regions of the drain and the source interact with each other near the channel surface and when ahigh drain voltage is applied, it further lowers the barrier height, resulting in further decrease of the threshold voltage and increase of subthreshold current. The source then injects carriers into the channel surface (independent of gate voltage). The surface DIBL typically occurs before the deep bulk punch through. DIBL does not change the subthreshold slope, but does lower V_{th}. Higher surface and channel doping and shallow source/drain junction depths reduce the DIBL effect on the subthreshold leakage current.

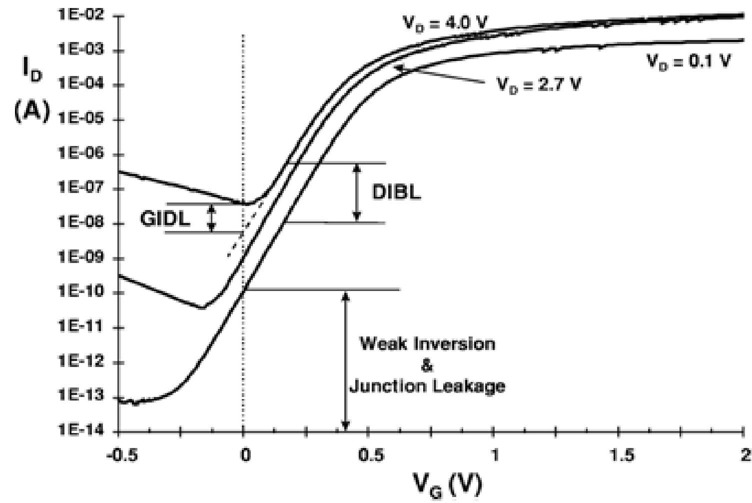


Figure 3.2:- N-channel I_D vs.V_G curve showing DIBL, GIDL, weak inversion and pn junction reverse-bias leakage components [14].

Figure 4.3 illustrates the DIBL effect as it moves the $I_D - V_G$ curve up and to the left as the drain voltage increases. DIBL can be measured at constant V_G as the change in I_D for a change in V_D.

3.1.2.2. Body Effect

Reverse biasing well-to-source junction of a MOS transistor widens the bulk depletion region and increases the threshold voltage. The effect of body bias can be considered in the threshold voltage equation [14],

$$V_{th} = V_{fb} + 2\psi_B + \frac{\sqrt{2\varepsilon_{si} q N_a (2\psi_B + V_{bs})}}{C_{ox}} \quad \text{......(10)}$$

Where V_{fb} is the flat-band voltage; N_a is the doping density in the substrate; and $\psi_B = (KT/q)\ln(N_a / n_i)$ is the difference between the Fermi potential and the intrinsic potential in the substrate.

The subthreshold leakage of an MOS device including weak inversion, DIBL, and body effect, can be modeled as [14],

$$I_{subthreshold} = A \times e^{1/m\upsilon_T(V_G - V_S - V_{tho} - \gamma' \times V_S + \eta V_{DS})} \times \left(1 - e^{-\upsilon_{DS}/\upsilon_T}\right) \quad ......(11)$$

where

$$A = \mu_0 C'_{ox} \frac{W}{L_{eff}} (\upsilon_T)^2 e^{1.8} e^{-\Delta V_{th}/\eta \upsilon_T} \quad ......(12)$$

V_{tho} is the zero bias threshold voltage. The body effect for small values of source to bulk voltages is linear and is represented by the term $\gamma' V_s$ in (11), where γ' is the linearized body effect coefficient, η is the DIBL coefficient, C_{ox} is the gate oxide capacitance, μ_0 is the zero bias mobility, and m is the subthreshold swing coefficient of the transistor. ΔV_{th} is a term introduced to account for transistor-to-transistor leakage variations.

3.1.2.3. Narrow Width Effect

The decrease in gate width modulates the threshold voltage of a transistor, and there by modulates the subthreshold leakage. In the LOCOS gate MOSFET, the existence of the fringing field causes the gate-induced depletion region to spread outside the defined channel width and under the isolations. This results in an increase of the total depletion charge in the bulk region above its expected value. The threshold voltage of MOS can be defined using depletion approximation as [14].

$$V_{th} = V_{fb} + \phi_s + \frac{Q_B}{C_{ox}} \quad ......(13)$$

where V_{fb} is the flat-band voltage; Φ_s is the surface potential; C_{ox} is the capacitance across the oxide; and Q_B is the depletion charge in the bulk. Due to narrow-width effect, Q_B increases by ΔQ_B . This effect becomes more substantial as the channel width decreases, and the depletion region underneath the fringing field is comparable to the classical depletion formed by the vertical field. This results in increase of threshold voltage due to narrow-channel effect. This narrow-width effect can be modeled as an increase in V_{th} by the amount V_{NCE} given by [14],

$$V_{NCE} - \frac{\pi q N_{sub} x_{d,max}^2}{2C_{ox}W_{eff}} - 3\pi \frac{t_{ox}}{W_{eff}} \phi_s \quad ......(14)$$

where N_{sub} is the substrate doping; $X_{d.max}$ is the maximum vertical depletion width; C_{ox} is the capacitance across the oxide; W_{eff} is the effective width; t_{ox} is the oxide thickness; and Φ_s is the surface potential. The second way that narrow-width modulates the threshold voltage is due to the fact that the channel doping is higher along the width dimension in LOCOS gates. Due to the channel stop, dopants encroach under the gate. Hence, a higher voltage is needed to completely invert the channel.

A more complex effect is seen in trench isolation devices, known as inverse-narrow width effect. In the case of trench isolation devices, depletion layer cannot spread under the oxide isolation. Hence, the total depletion charge in the bulk does not increase ($\Delta Q_B \approx 0$), thereby eliminating the increase in the threshold voltage. On the other hand, due to the two-dimensional (2D) field-induced edge fringing effect at the gate edge, formation of an inversion layer at the edges occurs at a lower voltage than the voltage required at the center. Moreover, the overall gate capacitance (C_T) now includes the sidewall capacitance (C_F) due to overlap of the gate with the isolation oxide. This increases the overall gate capacitance. Overall gate capacitance is therefore given by $C_T = C_{ox} W + 2 C_F$, which is greater than C_{ox} given in eqn.(14). Hence, the overall V_{th} reduces.

3.1.2.4. Effect of Channel Length and V_T –rolloff

Threshold voltage of MOSFET decreases as the channel length is reduced. This reduction of threshold voltage with reduction of channel length is known as V_{th} rolloff. The principal reason behind this effect is the presence of 2D field patterns in short-channel devices instead of one-dimensional (1D) field patterns in long-channel devices. This 2D field pattern originates from the proximity of source and drain regions [14]. There are depletion regions surrounding the source and drain junctions. In long channel devices, since the source and drain are far apart, their depletion regions do not have much effect on the potential profile or field pattern in most parts of the channel. However, in the case of short-channel devices, source-to-drain distance is comparable to the depletion width in the vertical direction. As a result, source drain depletion width has a more pronounced effect on potential profiles and

field patterns. The source and drain depletion regions now penetrate more into the channel length, resulting in part of the channel being already depleted. Thus, gate voltage has to invert less bulk charge to turn a transistor on. In other words, for the same gate voltage, there is more band bending in the Si–SiO_2 interface in a short-channel device as compared with a long-channel one. Consequently, the threshold voltage is lower for a short-channel device. The effect of the source drain depletion region is more severe at a high drain bias. High drain bias results in more depletion charge in the channel from the drain and source, resulting in further decrease of the threshold voltage, and hence, larger subthreshold current.

3.1.2.5. Effect of Temperature

Temperature dependence of the subthreshold leakage current is important, since digitalvery large scale integration (VLSI) circuits usually operate at elevated temperatures dueto the power dissipation (heat generation) of the circuit. Two parameters increase thesubthreshold leakage as temperature is raised:

1) S_t linearly increases with temperature; and

2) the threshold voltage decreases.

3.1.3. Gate Induced Drain Leakage (I_3)

GIDL is due to high field effect in the drain junction of an MOS transistor. When the gate is biased to form an accumulation layer at the silicon surface, the silicon surface under the gate has almost same potential as the p-type substrate. Due to presence of accumulated holes at the surface, the surface behaves like a p region more heavily doped than the substrate. This causes the depletion layer at the surface to be much narrower than elsewhere as shown in Figure 3.3(a). The narrowing of the depletion layer at or near the surface causes field crowding or an increase in the local electric field, thereby enhancing the high field effects near that region. When the negative gate bias is large (i.e., gate at zero or negative and drain at V_{DD}), the n^+ drain region under the gate can be depleted and even inverted as shown in Figure 3.3(b). This causes more field crowding and peak field increase, resulting in a dramatic increase of high field effects such as avalanche multiplication and BTBT.

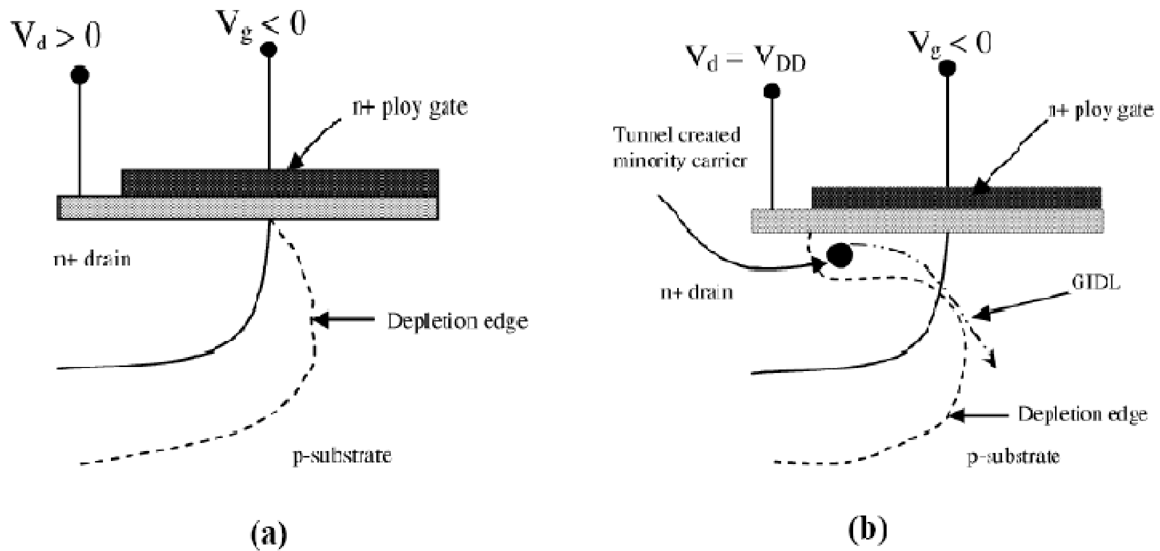


Figure 3.3:- Condition of the depletion region near the drain-gate overlap region of an MOS transistor when (a) surface is accumulated with low negative gate bias; (b) n+ region is depleted or inverted with high negative bias.

The possibility of tunneling via near-surface traps also increases. As a result of all these effects, minority carriers are emitted in the drain region underneath the gate. Since the substrate is at a lower potential for minority carriers, the minority carriers that have been accumulated or formed at the drain depletion region underneath the gate are swept laterally to the substrate, completing a path for the GIDL. Thinner oxide thickness and higher V_{DD} (higher potential between gate and drain) enhance the electric field and therefore increase GIDL. The impact of drain and well doping on GIDL is rather complicated. At low drain doping, the electric field is not high enough to cause tunneling. At very high drain doping, the depletion width—and, therefore, the tunneling volume—are limited, causing less GIDL. Hence, GIDL is worse for moderate drain doping, where both the electric field and depletion width (tunneling volume) are considerable. The narrowing of the depletion layer at or near the surface causes field crowding or an increase in the local electric field, Very high and abrupt drain doping is preferred for minimizing GIDL, as it provides lower series resistance required for high transistor drive currents.

3.1.4. Punchthrough (I_4)

In short-channel devices, due to the proximity of the drain and the source, the depletion regions at the drain-substrate and source-substrate junctions extend into the channel. As the channel length is reduced, if the doping is kept constant, the separation between the depletion region boundaries decreases. An increase in the reverse bias across the junctions (with increase in V_{ds}) also pushes the junctions nearer to each other. When the combination of channel length and reverse bias leads to the merging of the depletion regions, punchthrough is said to have occurred. In submicrometer MOSFETs, a V_{th} adjust implant is used to have a higher doping at the surface than that in the bulk. This causes a greater expansion of the depletion region below the surface (due to smaller doping there) as compared to the surface. Thus, the punchthrough occurs below the surface. An increase in the drain voltage beyond the value required to establish the punchthrough lowers the potential barrier for the majority carriers in the source. Thus, more of these carriers crossthe energy barrier and enter into the substrate, and the drain collects some of them. The net effect is an increase in the subthreshold current. Furthermore, punchthrough degrades the subthreshold slope. The device parameter commonly used to characterize the punchthrough is the punchthrough voltage V_{PT} , which estimates the value of V_{ds} for which the punchthrough occurs at $V_{gs} = 0$. It is roughly estimated as the value of the V_{ds} for which the sum of the widths of the drain and source depletion regions is equal to effective channel length [14],

$$V_{BT} \propto N_B \left(L - W_j\right)^3 \qquad \ldots\ldots(15)$$

where N_B is the doping concentration at the bulk; L is the channel length; W_j and is the junction width.The most suitable method for controlling the punchthrough is to use additional implants. The narrowing of the depletion layer at or near the surface causes field crowding or an increase in the local electric field, A layer of higher doping at a depth equal to that of the bottom of the junction depletion regions is one possible solution. Another approach could be to form a halo implant at the leading edges of the drain and source junctions.

3.1.5. Tunneling into and through Gate Oxide (I_5)

Reduction of gate oxide thickness results in an increase in the field across the oxide. The high electric field coupled with low oxide thickness results in tunneling of electrons from substrate to gate and also from gate to substrate through the gate oxide, resulting in the gate oxide tunneling current.

When a positive bias is applied to the gate, due to the small oxide thickness, which results in a small width of the potential barrier, the electrons at the strongly inverted surface can tunnel into or through the SiO_2 layer and hence give rise to the gate current. On the other hand, if a negative gate bias is applied, electrons from the n^+ polysilicon can tunnel into or through the oxide layer and give rise to the gate current. The mechanism of tunneling between substrate and gate polysilicon can be primarily

divided into two parts, namely:

(1) Fowler–Nordheim (FN) tunneling

(2) Direct tunneling.

In the case of FN tunneling, electrons tunnel through a triangular potential barrier, where as in the case of direct tunneling, electrons tunnel through a trapezoidal potential barrier. The tunneling probability of an electron depends on the thickness of the barrier, the barrier height, and the structure of the barrier. Therefore, the tunneling probabilities of a single electron in FN tunneling and direct tunneling are different, resulting in different tunneling currents.

3.1.6. Injection of Hot Carriers from Substrate to Gate Oxide (I_6)

In a short-channel transistor, due to high electric field near the Si–SiO_2 interface, electrons or holes can gain sufficient energy from the electric field to cross the interface potential barrier and enter into the oxide layer. This effect is known as hot-carrier injection. The injection from Si to SiO_2 is more likely for electrons than holes, as electrons have a lower effective mass than that of holes, and the barrier height for holes(4.5 eV) is more than that for electrons (3.1 eV) [14].

3.2. Process Level Techniques For Leakage Reduction In Capacitorless SOI Dram Cell

The reduction in leakage current has to be achieved using both process- and circuit-level techniques. At the process level, leakage reduction in transistors can be achieved by controlling the dimensions (length, oxide thickness, junction depth, etc.) and doping profile in transistors. At the circuit level, threshold voltage and leakage current of transistors can be effectively controlled by controlling the voltages of different device terminals [drain, source, gate, and body (substrate)]. In this chapter, we will consider major process techniques for leakage control and reduction.

3.2.1. Channel Engineering for Leakage Reduction

Based on constant field scaling, the short channel effects can be kept under control by scaling down the vertical dimensions, for example, gate insulator thickness, junction depth, along with the horizontal dimensions, while also proportionally decreasing the applied voltages. The substrate doping concentration should increase to decrease the depletion width proportionally. The principle of constant field scaling lies in scaling the device voltages and the device dimensions (both horizontal and vertical) by the same factor, *K* (>1), such that the electric field remains unchanged. Constant electric field assures the reliability of the scaled device in terms of hot-carrier injection.

To minimize short channel effects, a sufficiently large aspect ratio (AR) of the device is required [14]. AR is defined as,

$$AR = \frac{dimension_{lateral}}{dimension_{vertical}} \qquad \ldots\ldots(16)$$

For a MOSFET, AR can be expressed as,

$$AR = \frac{L}{\left[t_{ox}\left(\frac{\varepsilon_{si}}{\varepsilon_{ox}}\right)\right]^{1/3} W_{dm}^{1/3} X_j^{1/3}} \qquad \ldots\ldots(17)$$

where ε_{si} and ε_{ox} are silicon and oxide permittivities; and L , t_{ox} , W_{dm} and X_j are channel length, gate oxide thickness, depletion depth, and junction depth, respectively. From eqn.(17), we can see that reducing t_{ox} , W_{dm} and X_j will reduce the short channel effects of a MOSFET.A key parameter is the maximum gate depletion width, W_{dm} , within which mobile carriers (holes in the case of nMOSFETs) are swept away by the applied gate field. For uniformly doped case

$$W_{dm} = \sqrt{\frac{4\varepsilon_{si}KT\ln\left(\frac{N_a}{n_i}\right)}{q^2 N_a}} \qquad \ldots\ldots(18)$$

where n_i is the intrinsic carrier concentration.

In addition to gate oxide thickness and junction scaling, another technique to improve short-channel characteristics is well engineering. By changing the doping profile in the channel region, the distribution of the electric field and potential contours can be changed. The goal is to optimize the channel profile to minimize the OFF-state leakage while maximizing the linear and saturated drive currents of MOSFET. Super steep retrograde wells and halo implants have been used as a means to scale the channel length and increase the transistor drive current without causing an increase in the OFF-state leakage current.

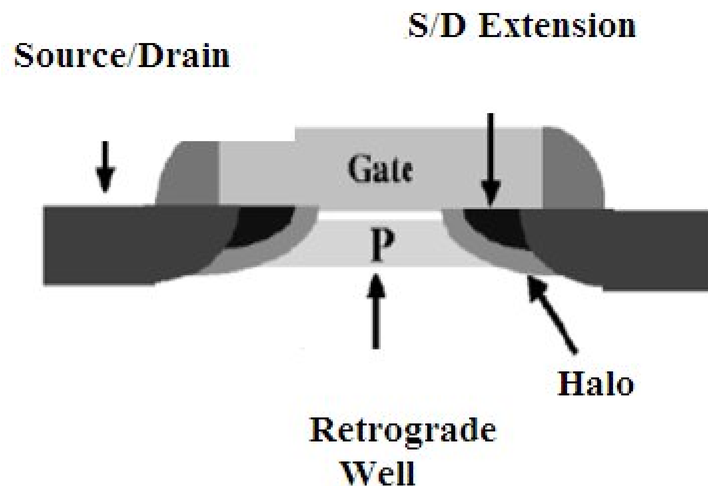


Figure 3.4: Graphical representation of different aspects of well engineering [14].

Figure 3.4 is a schematic representation of the transistor regions that are affected by the different types of well engineering. Retrograde well engineering changes the 1Dcharacteristics of the well profile by creating a retrograde profile toward the Si–SiO_2surface. The halo profile creates a localized 2D dopant distribution near the S/D extension regions. The use of these two techniques to increase the device performance, while keeping leakage to a tolerable limit, is discussed in the following subsections.

3.2.1.1. Retrograde Doping

To maintain acceptable OFF-state leakage with continually decreasing channel lengths, both the oxide thickness and the gate-controlled depletion width in silicon,

$$W_{dm} = \sqrt{\frac{4\varepsilon_{si}\psi_B}{qN_a}} \quad \text{……(19)}$$

must be reduced in proportion to the channel length to offset the degradation in short channel effects for extremely small devices. This requires an increase in the channel doping concentration (N_a). This leads to a higher threshold voltage for a uniformly doped channel, according to the following [14]:

$$V_{th} = V_{fb} + 2\psi_B + \frac{\sqrt{4\varepsilon_{si}qN_a\psi_B}}{C_{ox}} \quad \text{……(20)}$$

However, if the threshold voltage is not scaled, the device performance for low supply voltages will degrade due to the large reduction in gate drive. To reduce the gate controlled depletion width while fulfilling the V_{th} reduction trend, retrograde doping can be used.

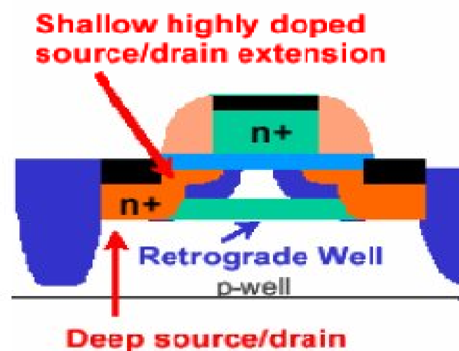


Figure 3.5:Schematic showing retrograde well[14].

Retrograde channel doping is a vertically non uniform, low-high channel doping. It is used to improve the short channel effects and to increase surface channel mobility by creating a low surface channel concentration followed by a highly doped subsurface region. The low surface concentration increases surface channel mobility by minimizing channel impurity scattering while the highly doped subsurface region acts as a barrier against punchthrough. For the same gate depletion width (W_{dm}), the surface electric field and the total depletion charge of an extreme retrograde channel is one-half that of a uniformly doped channel. This reduces the threshold voltage and improves mobility. Retro grade channel doping allows the threshold voltage (V_{th}) to be decoupled from the gate controlled depletion width (W_{dm}). However, the body effect coefficient and the subthreshold slope are still coupled to the gate depletion width (W_{dm}).

3.2.1.2. Halo Doping

The most important device change over the past decade to control subthreshold current was the addition of large angle implants called "halos". Halo doping or non uniform channel profile in a lateral direction was introduced below 0.25-μm technology node to provide another way to control the dependence of threshold voltage on channel length [14]. The halo implant is a high angle implant of well type dopant species introduced into the device after transistor gate patterning (for example, p-type dopant implanted into the p-well of nMOSFET). Typically the same lithography step as the source/drain extension implant is used. Because of the high halo implant angle, multiple implants with rotations are needed to ensure uniform doping on all sides of channel.

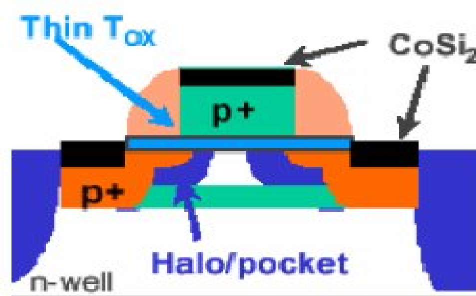


Figure 3.6: Schematic showing halo doping[14].

For n-channel MOSFETs, more highly p-type doped regions are introduced near the two ends of the channel as shown in figure (3.4). Under the edges of the gate and at the end of the channel, point defects are injected during sidewall oxidation. These point defects gather doping impurities from the substrate, thereby increasing the doping concentration near the source and drain end of the channel. More highly doped p-type substrate near the edges of the channel reduces the charge-sharing effects from the source and drain fields, thus reducing the width of the depletion region in the drain-substrate and source-substrate regions. As the channel length is reduced, these highly doped regions consume a larger fraction of the total channel.

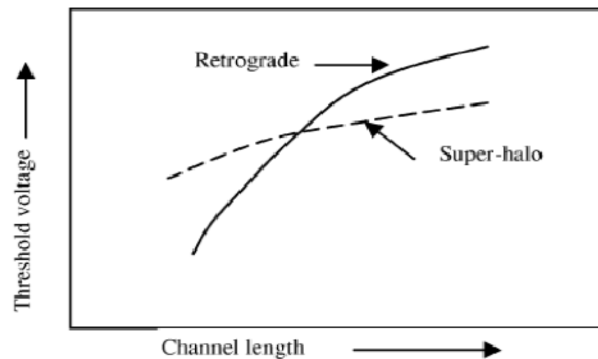


Figure 3.7: Short channel threshold voltage roll-off for retrograde and superhalo [14].

Reduction of charge-sharing effects reduces the threshold voltage degradation due to channel length reduction. Thus, threshold voltage dependence on channel length becomes more flat as shown in figure 3.6. Hence, the off-current becomes less sensitive to channel length variation. The reduction in drain and source junction depletion region width also reduces the barrier lowering in the channel, thus reducing DIBL. Since the channel edges are more heavily doped and junction depletion widths are smaller, the distance between source and drain depletion regions is larger. This reduces the punchthrough possibility. The higher doping near the channel edges causes larger BTBT and higher GIDL. The BTBT currents in the high-field region near the drain ultimately limit the halo doping level.

CHAPTER 4

PROCESS STEPS FOR FABRICATION OF CAPACITORLESS FD SOI DRAM CELL

This chapter describes the process steps for the fabrication of capacitorless SOI DRAM cell. The 2D process simulation has been done using ATHENA package of SILVACO.The first step in modeling any simulation structure is specifying its initial grid. The correct specification of a grid is critical in process simulation. The number of nodes in the grid N_p has a direct influence on simulation accuracy and time. A finer grid should exist in those areas of the simulation structure where ion implantation will occur, where p-n junction will be formed, or where optical illumination will change photoactive component concentration [15].

For the SOI DRAM cell structure, deep-submicron 30nm nMOSFET as the access transistor and the buried oxide layer as the storage device have been considered for the analysis. The physical parameters for the nMOSFET has been specified according to the International Technology Roadmap for Semiconductors (ITRS) [19]. Table (4.1) illustrates values of the physical parameters of 30nm nMOSFET taken into consideration for the design.

Table 4.1:- Physical parameters for the design of 0.18 µm nMOSFET [19].

Physical Parameter	Value
Technology Node	30 nm Technology
DRAM Bits/Chip	1Gbit
Minimum Supply Voltage (volts)	1.2 –1.5
Minimum Logic Vdd (volts)	1.2 –1.5
Polysilicon Deposit (nm)	100
Gate Length (nm)	30 nm
Gate Oxide Thickness (nm) (equivalent)	3–4
Channel Dopant Concentration	$3x10^{18}$ cm^{-3}

Initial Substrate doping concentration	B = 8x 10^{12} cm^{-3}
Source/Drain implant Doping Concentration	As = 3 x 10^{15} cm^{-3} E = 60 keV
V_{th} Adjust Implant Doping Concentration	B = 12 x 10^{12} cm^{-2}, E = 45 keV
LDD Implant Doping Concentration	As = 1 x 10^{15} cm^{-2} E = 30 keV
Final Rapid Thermal Anneal (RTA)	850–1000°C/1 sec

B => Boron, As => Arsenic, E => Energy

As per the first step in the process flow, the grid has been specified and then the cleaned silicon substrate is lightly doped with boron with concentration of 10^{12}/cm^3. This is shown in figure (4.1).

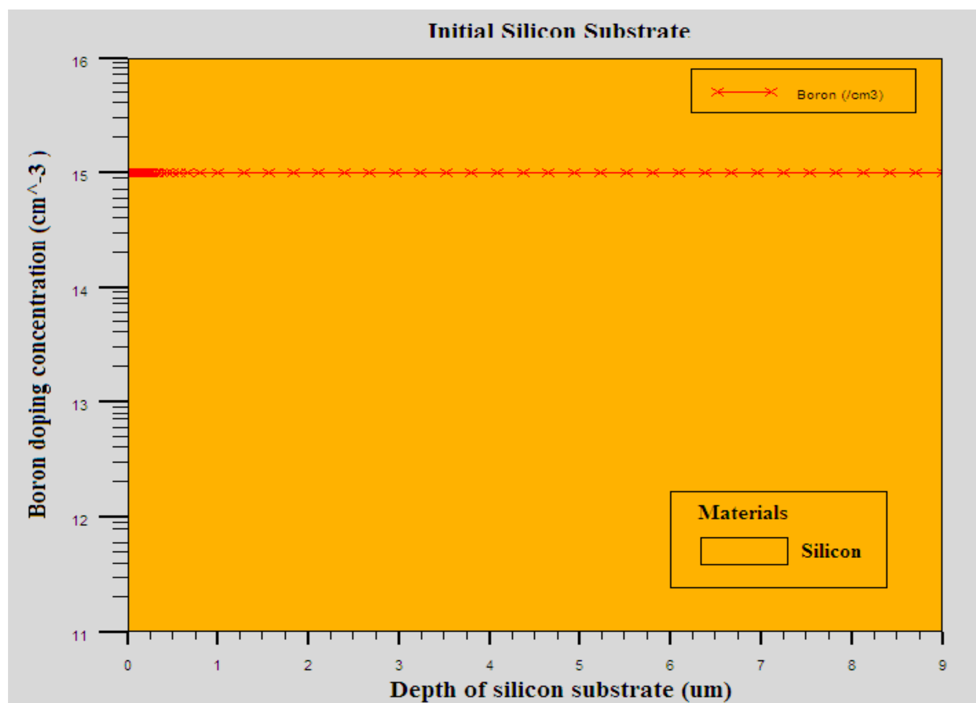


Figure 4.1:- Initial silicon substrate.

Then the substrate surface is typically covered by a pad insulator such as oxide layer. Oxide layer is then etched to get the required thickness. Then the silicon substrate is etched up to

depth of 0.02 µm using reactive ion etching [17]. A node dielectric (silicon dioxide is chosen in this case) is then deposited on the top of the pad insulator. This is shown in figure (4.2).

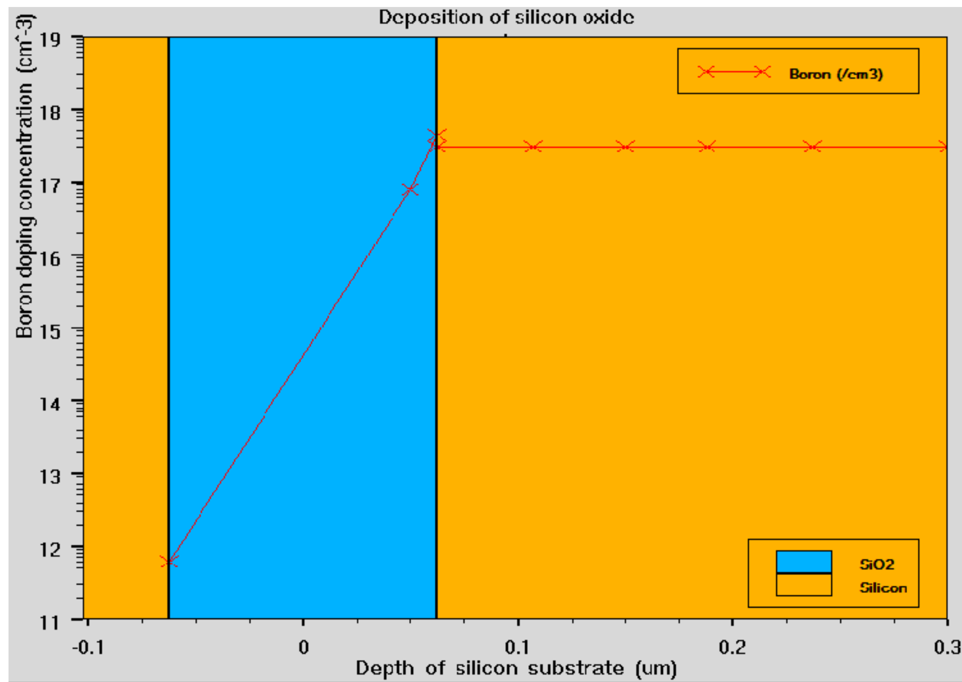


Figure 4.2:- Deposition of Silicon Oxide.

A layer of polysilicon is deposited on this dielectric, thereby covering the top surface of the pad insulator shown in figure (4.3).

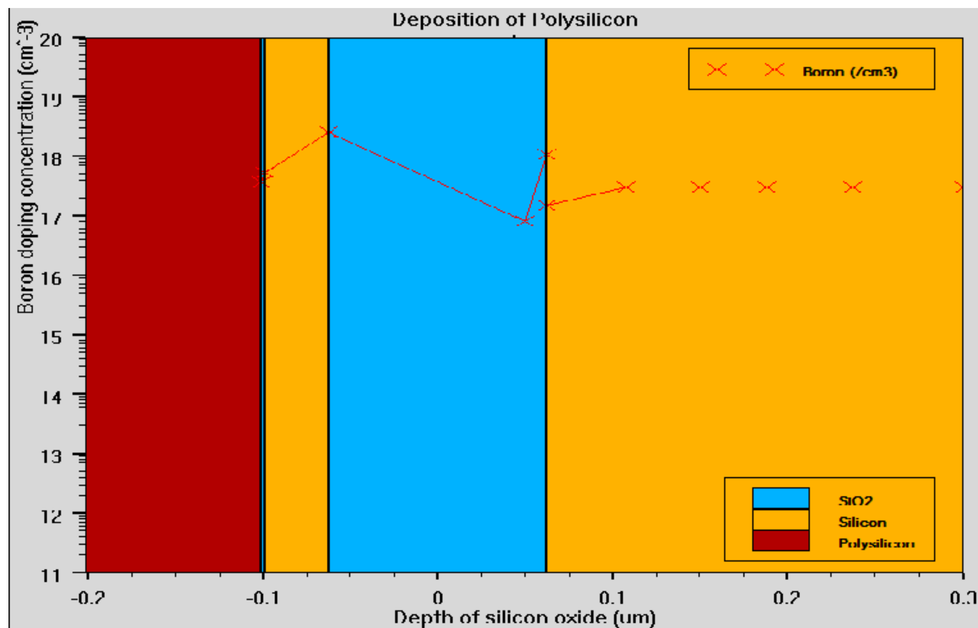


Figure 4.3:- Deposition of Polysilicon

The polysilicon is etched. The node dielectric is then removed from the top surface. This is shown in figure (4.4)

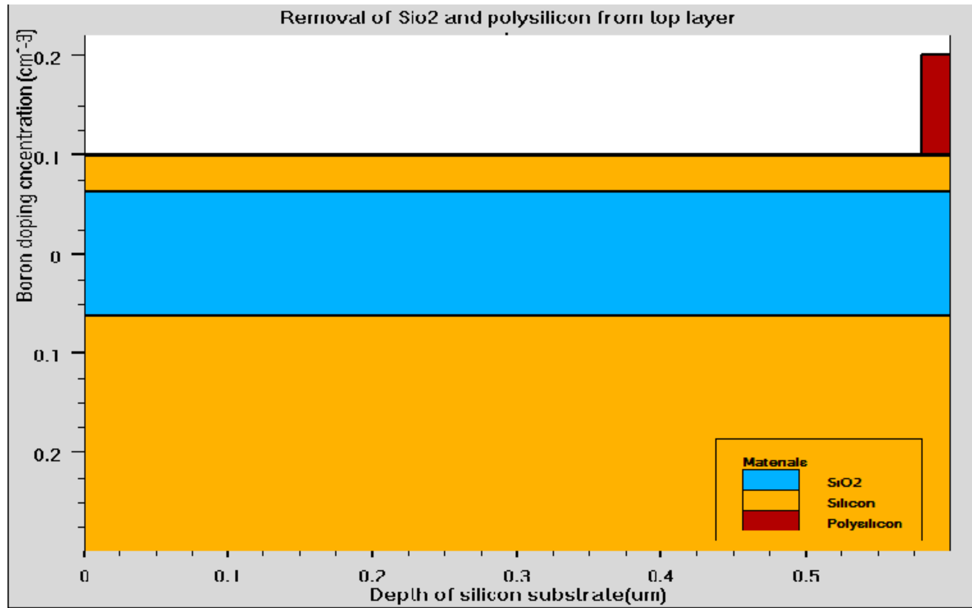


Figure 4.4:- Removal of SiO2 and Polysilicon from top layer

An SOI nMOSFET is to be formed . However, scaling-down has resulted in the development of short-channel effects. Therefore, it has been attempted to extinguish the short-channel effect by providing the channel region of MOSFET with a semiconductor region having the same conductivity type as that of the substrate (retrograde-well). The p-well is formed using a boron implantation with an energy of E = 200 keV and a dose of D=8 x $10^{12}/cm^2$. By applying such a moderate energy implant without drive-in diffusion, a retrograde well profile is achieved which suppresses parasitic bipolar devices (latch-up immunity). The concentration of boron has increased a few nanometers below the silicon surface. Thus a low-to-high doping channel profile is observed. The low concentration at channel region improves surface mobility.

Gate oxide of thickness 0.007 nm is grown over the substrate. The gate oxide thickness has been approximately linearly scaled with channel length, with the ratio of gate length L_G to the thickness t_{ox} being maintained at approximately 45 [18].

A low-energy ion implantation (boron implant of about 12 x 10^{12} /cm^2 with energy E = 45keV) is done to slightly dope the well region below the gate electrode to adjust the V_{th} of the device. Primarily this implant, in combination with the previous p-well implant and the gate oxide capacitance, determines the final threshold voltage value. The figure (4.5) shows the doping profile after this V_{th} adjust implant and figure (4.6) shows the boron concentration along the depth of the substrate.

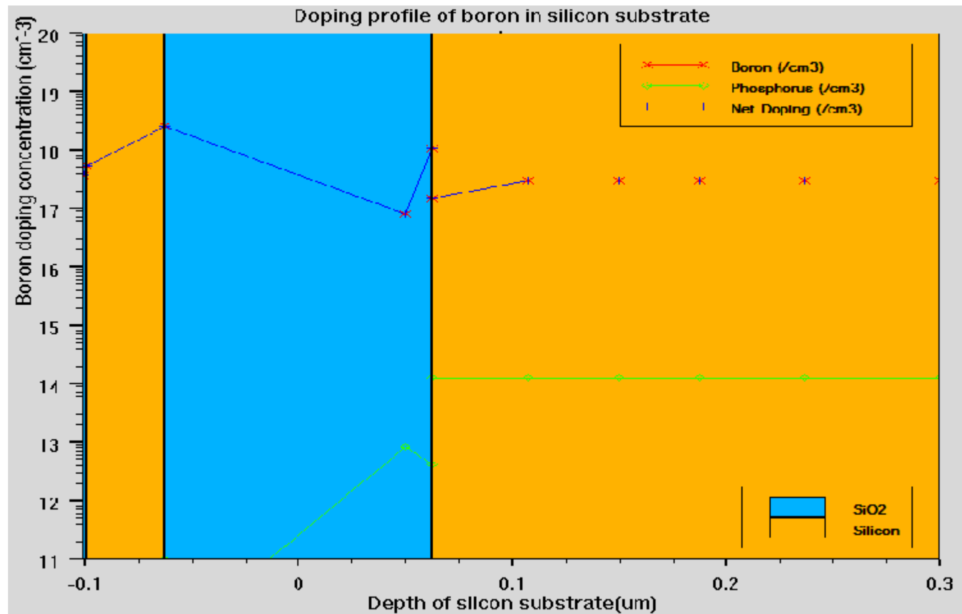


Figure 4.5:- Doping profile of substrate after V_{th} adjust implant

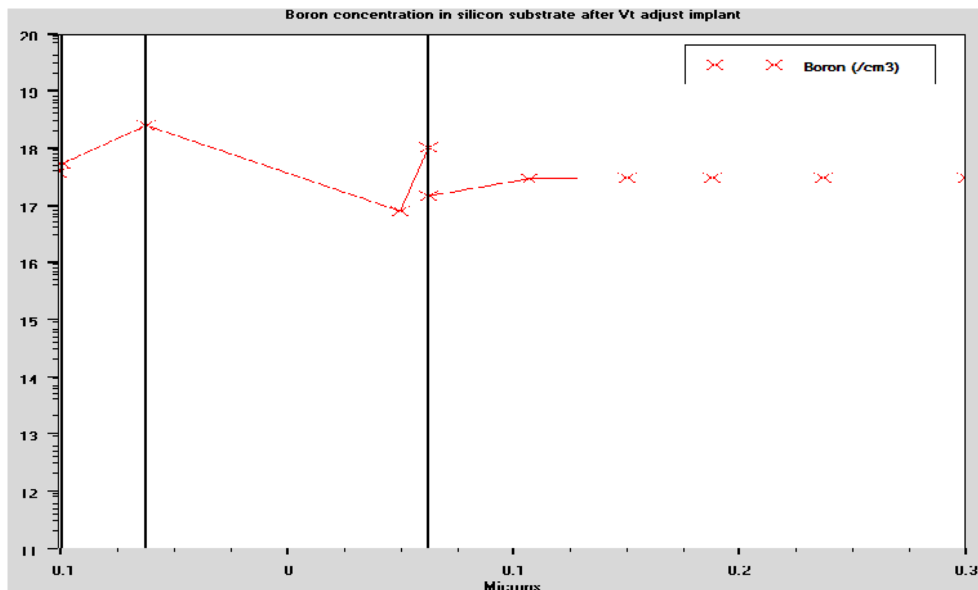


Figure 4.6:- Boron concentration in silicon substrate after V_{th} adjust implant.

A heavily n+ doped polysilicon layer of 200 nm thickness is deposited. Now after the lithography step the gate contact with length 0.18 µm is formed. Now the step of polysilicon doping and the formation of lightly doped drain is done. Implant dose and energy needed to be selected carefully and controlled to produce a desired graded drain junction.

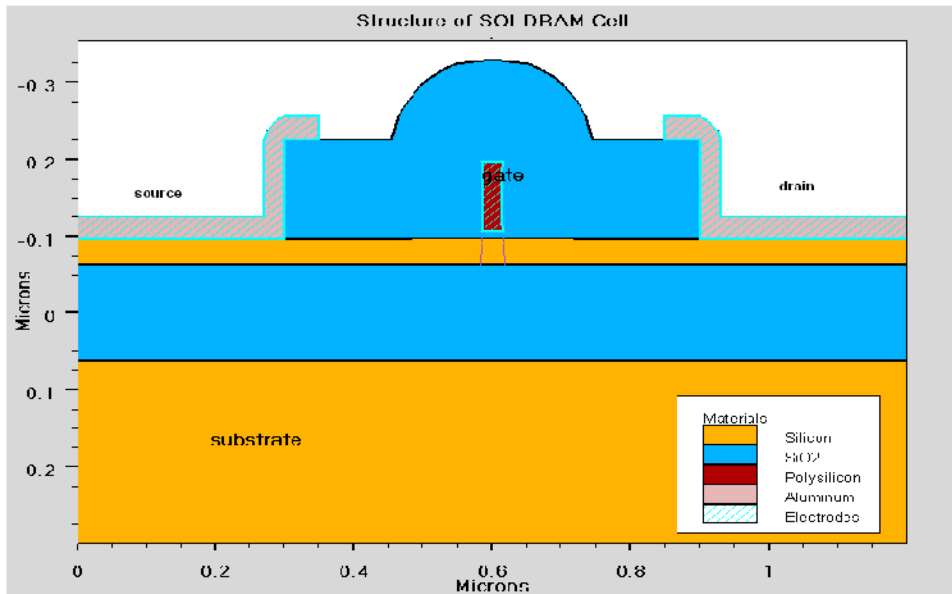


Figure 4.7(a):-Complete Stucture of SOI MOSFET

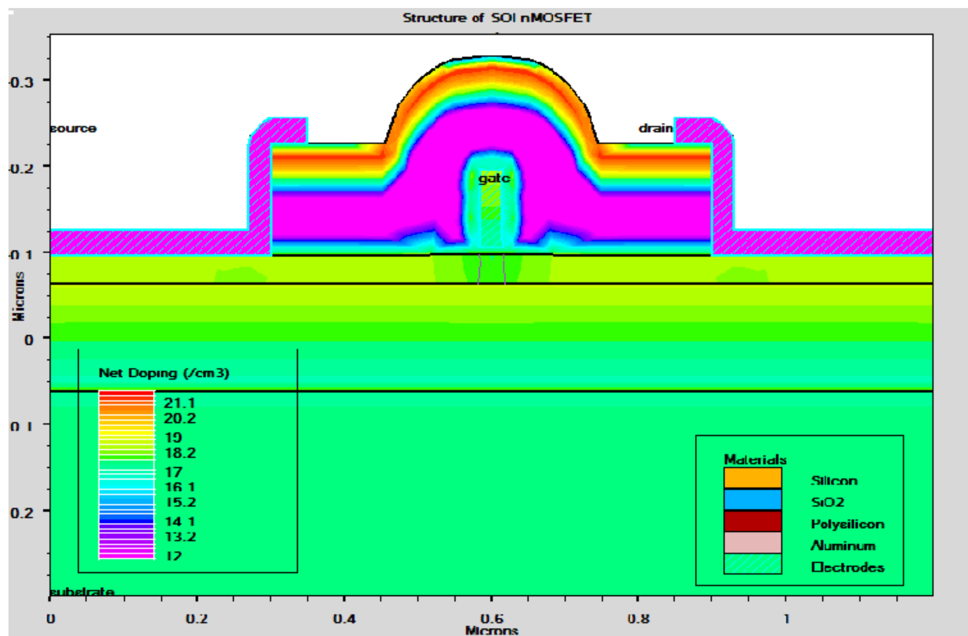


Figure 4.7(b):-Complete Stucture of SOI MOSFET.

The complete structure of SOI DRAM cell is shown in figure (4.7).Arsenic implant with 3 x $10^{15}/cm^2$ dose at 30 keV was used. In comparison to conventional devices, light doped drain in modern devices reduces the electric field at the oxide semiconductor interface. The Light doped drain reduces the GIDL and hot electron effects. The thin oxide layer is removed and about 100 nm oxide is deposited by low pressure chemical vapor deposition (LPCVD) and an isotropically etched so that oxide spacers at the polysilicon edges are created. A high dose (5 x 10^{15} cm^{-2}) of aluminium is implanted with60 keV to build the low resistance of source and drain regions. To activate the implanted dopants without too much diffusional redistribution, a rapid thermal annealing (RTA) step is necessary; e.g. 1 seconds at about 1000°C for nMOSFET.. Finally, the nMOSFET is contacted using aluminum. A buried strap region (formed by diffusion of dopants from polysilicon) connects the drain with the polysilicon. The collar serves to prevent the charge leakage from the capacitor at the buried strap junction.

CHAPTER 5

RESULTS AND CONCLUSION

5.1. Results and discussion

Process and device simulation of capacitorless SOI DRAM cell has been carried out using the ATHENA/ATLAS packages of SILVACO. The capacitorless SOI DRAM cell structure has been generated using ATHENA and then it is used as input to device simulator ATLAS for its electrical characterization [19]. With device simulation, the effect of process parameters and its variation on the electrical characteristics of DRAM cell is studied

.

Process-level techniques such as LDD implantation, and halo doping in DRAM cell in 30 nm technology has been employed for leakage reduction. Leakage reduction from 2.25 nA to 10 pA has been achieved.

Figure 5.1 below shows the subthreshold characteristics of a DRAM cell in which nMOSFET is fabricated with LDD implantation done and without halo doping and retrograde well. At $V_g = 0$ V, off-state leakage $I_{ds} = 2.25$ nA has been observed.

Figure 5.2 below shows the subthreshold characteristics of a DRAM cell in which nMOSFET is fabricated with LDD implantation, and without halo implantation. At $V_g = 0$ V, off-state leakage $I_{ds} = 10$ pA has been observed. Leakage reduction has been achieved.

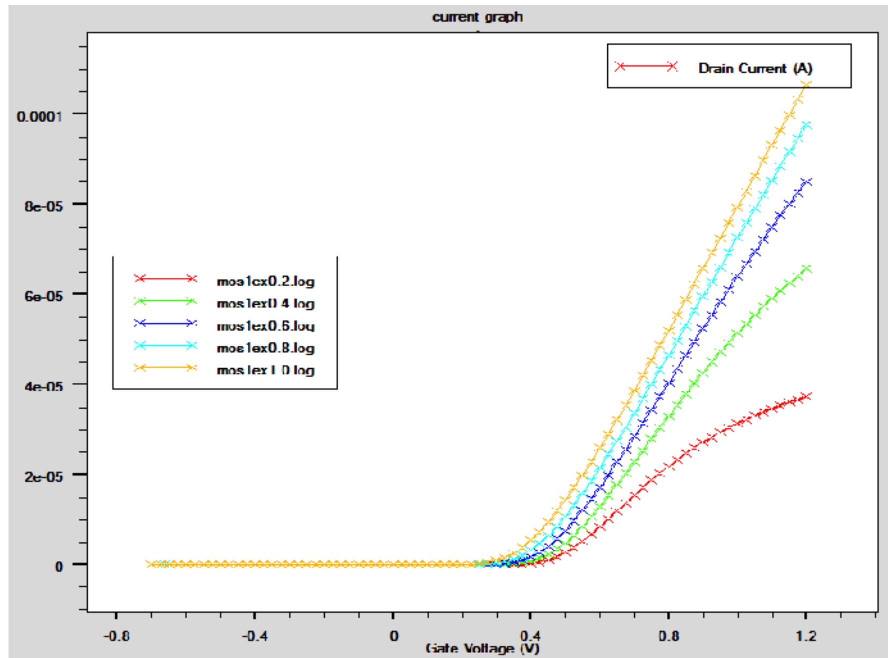


Figure 5.1:- I_D Vs V_g Curve in Saturation.

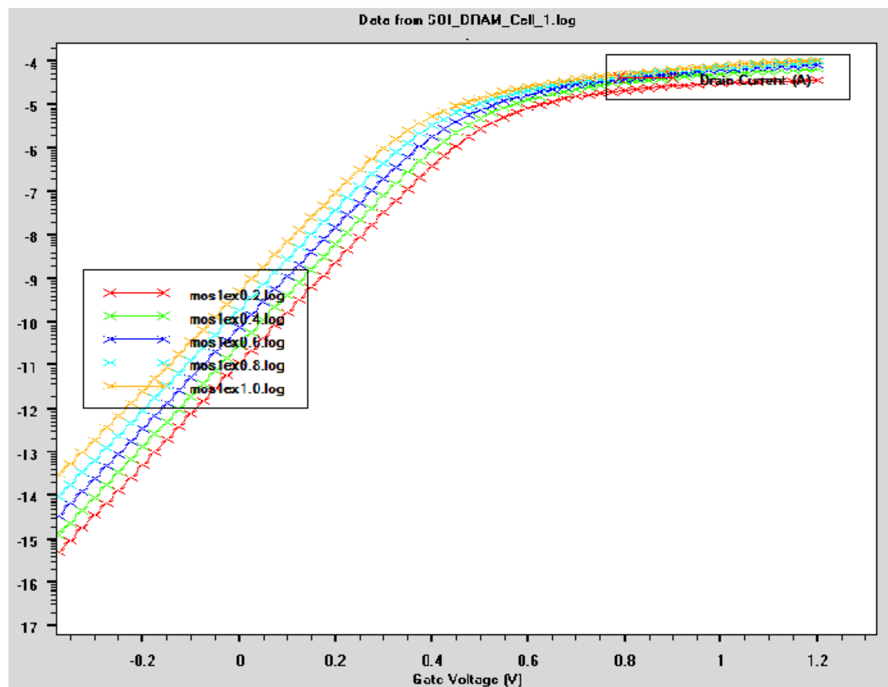


Figure 5.2:- Log I_D Vs V_g for fixed V_{DS} & V_{SB}.

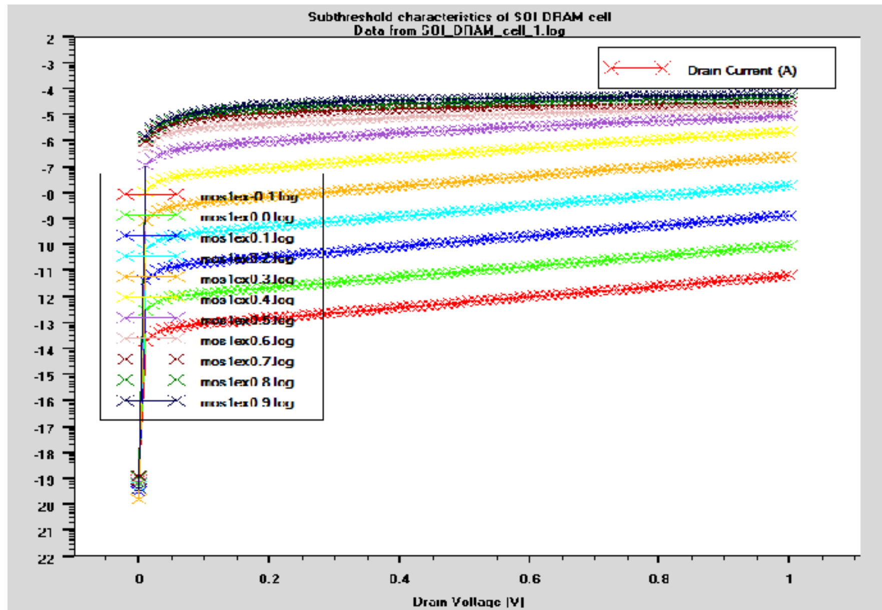


Figure 5.3: Log I_D Vs V_D characteristics

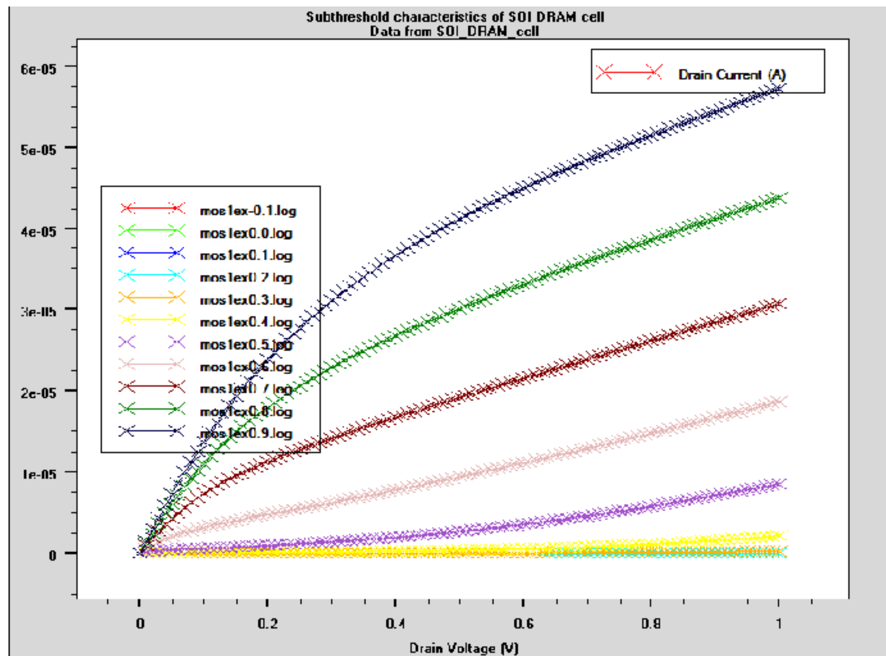


Figure 5.4: I_D Vs V_D characteristics of SOI DRAM Cell.

5.2. Conclusion and Future Scope

Leakage current analysis of SOI capacitorless dynamic random access memory cell has been done. For the analysis, 30 nm submicron nMOSFET as access transistor and the floating body cell as storage device have been designed. For this a low leakage access transistor has been modeled and simulated using ATHENA/ATLAS packages of SILVACO. It has been found that process techniques such as lightly doped drain (LDD) implantation and halo doping in DRAM cell in 30 nm technology reduce the leakage current significantly. A leakage current of 2.25 nA is found in DRAM at 0.18 μm while by using LDD, retrograde well and halo doping simultaneously in DRAM cell we found that the leakage current is reduced to10 pA. Thus these leakage reduction techniques reduce the refreshing rate and hence the power consumption of DRAM cell efficiently.

As we are approaching the physical limits of MOSFET scaling and the demand for higher density, efficiency and performance of DRAMs are continuously increasing, research on other alternatives to conventional device and process is accelerating. Some of the techniques under investigation are strained silicon, high-k gate dielectric, gate stack engineering and non-planar MOSFET.

This thesis work features the use of bulk technology for the fabrication of DRAM cell. The benefits of SOI over Z-RAM technology, Double Gate SOI DRAM can be investigated as future work. The DRAM using the floating body cell can be used as a high-speed memory and as an alternative to Z-RAM because SOI devices are having the advantages in high speed, low power dissipation and extended scalability.

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APPENDIX

Silvaco's products enables device technology engineers to design and predict the fabrication and performance of semiconductor devices via physics-based simulation.

Simulators

- ATHENA provides the two-dimensional simulation of semiconductor processing.
- ATLAS provides the two- and three-dimensional simulation of the electrical, optical and thermal characteristics of semiconductor devices.
- MERCURY provides the fast and accurate characterization of the electrical behavior of MESFET and HEMT devices.
- Mocasim provides transport parameters via Monte Carlo simulation.

Support Tools

- DeckBuild provides an integrated run-time enviroment for Silvaco simulators and tools.
- Optimizer provides interactive capability to optimize various process and device characteristics as well as calibrate model parameters.
- DevEdit provides a GUI-based and command-line structure and mesh editor.
- TonyPlot provides interactive visualization for one- and two-dimensional devices and Characteristics.
- TonyPlot3D provides interactive visualization for three-dimensional devices.
- VWF provides an automated wafer manufacturing enviroment for TCAD simulations.

ATHENA Process Simulation

ATHENA is a general purpose 2D semiconductor process simulation framework. ATHENA simulates various fabrication processes in a wide variety of semiconductor materials. It's an indispensable tool for all segments of semiconductor manufacturing market.

Deep Submicron Transistors and Memory Cells

Advanced implant and RTA diffusion models for shallow junction formation are indispensable for design and optimization of deep-submicron CMOS devices

RF electronics

ATHENA simulates basic processes in various wide band-gap materials used in RF electronics.

- ATHENA provides an easy to use, modular, and extensible platform for simulating ion implantation , impurity diffusion diffusion, physical etching and deposition, all diffusion lithography,material oxidation and silicidation.
- Fast and accurate simulation of all critical process steps used in CMOS, bipolar, SiGe/SiGeC SiC, GaAs, SOI , optoelectronics and power device technologies
- Extensive hierarchy of physical models for most technological steps allows accurately predict and optimize all individual process steps as well as the whole porcess flow.
- Physical etching and deposition models allow to accurately simulate the topology evolution during complex processes such as multi-level metalization, deep trench etching, APCVD, LPCVD and ion milling.

ATLAS Device Simulation

The ATLAS Device Simulation Framework enables to device technology engineers to predict the electrical, optical, and thermal behavior of semiconductor devices via simulation. ATLAS provides a physics-based, easy to use, modular, and extensible platform to analyze DC, AC, and time-domain responses for all semiconductor-based technologies in two and three dimensions.

- Accuractely characterizes devices for electrical, optical, and thermal performance without costly split-lot experiments.
- Solves yield and process variation problems for optimal combinations of speed, power density, breakdown, leakage, luminosity, and reliablility.
- Easy to use and powerful input syntax.
- Full integration with the ATHENA process simulation software, DevEdit structure editor, and comprehensive visualization package.