Design of 10-bit Track and Hold Circuit Using Bootstrapped Switch

A dissertation submitted in partial fulfillment of the requirement for the award of degree of

Master of Technology

in

VLSI Design

Submitted By:

Parul

Roll No. 601461016

Under the supervision of:

Dr. Alpana Agarwal

Associate Professor, ECED

Thapar University, Patiala

Department of Electronics & Communication Engineering

Thapar University, Patiala-147004

CERTIFICATE

I, hereby declare that the thesis entitled **"Design of 10-bit Track and Hold Circuit using Bootstrapped Switch"** in the partial fulfillment of the requirement for the award of degree of M.Tech (VLSI Design) submitted in Electronics and Communication Department of Thapar University, Patiala is an authentic record of my own work carried out under the supervision and guidance of **Dr. Alpana Agarwal, Associate Professor, ECED.**

To the best of my knowledge, the matter embodied in this thesis work has not been submitted for award of any other degree at this or any other university.

Date: 13/07/2016

Place: PATIALA

Parul

Roll No. - 601461016

It is certified that the above statement made by the student is correct to the best of my knowledge and belief.

Date: 13/07/2016

Alpana Agarwal

Associate Professor, ECED

Countersigned By:

Head of Department
Thapar University, Patiala

Dean of Academic Affairs
Thapar University, Patiala.

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Parul

601461016

ABSTRACT

Digitalization is bringing revolutionary changes in each area of modern technology like telecommunication, consumer electronic appliances *etc*. The role of ADCs and DACs are significant in interfacing digital electronics with analog world. The Track and Hold (T/H) Circuit is the front end of all ADCs as it ensures the accurate digitization of a constant analog value at the output terminal. A low performance T/H can degrade the performance of its subsequent circuitry. So, it is essential to have a good T/H circuit. This work presents and discusses a new architecture of a low power Opamp-less fully differential Track and Hold circuit in 180 nm CMOS technology. This circuit uses the concept of bootstrapping to achieve a constant on-resistance. With this idea, the gate-to-source voltages of transmission gate are made independent to the input signal amplitude and thus made the circuit linear. The circuit is optimized for the following performance parameters: Total Harmonic Distortion (THD), Signal-to-Noise and Distortion Ratio (SNDR), Spurious Free Dynamic Range (SFDR) and Effective Number of Bits (ENOB), Power dissipation and on-resistance. The circuit is designed to work on the maximum sampling frequency of 100MHz. For input signal of 5.3125MHz and sampling frequency of 20MHz, it achieves THD of −60.44dB with SNDR of 60.28dB. The SFDR for the proposed circuit comes out to be 60.78dB with 9.7 effective number of bits. It uses a power supply of 1.8V and dissipates power not more than −41.1dBm. All the simulations and parameter calculations are done in CADENCE ®VIRTUOSO ANALOG DESIGN ENVIRONMENT and the value of parameters are verified in MATLAB also.

Table of Contents

List of Acronyms

Acronym	Expansion
ADCs	Analog-to-Digital Converters
T/H	Track and Hold
S/H	Sample and Hold
MOS	Metal Oxide Semiconductor
nMOS	n- channel Metal Oxide Semiconductor
pMOS	n- channel Metal Oxide Semiconductor
CMOS	Complementary Metal Oxide Semiconductor
THD	Total Harmonic Distortion
SNDR, SINAD	Signal to Noise and Distortion Ratio
SNR	Signal-to-Noise Ratio
SFDR	Spurious Free Dynamic Range
rms	Root Mean Square
FFT	Fast Fourier Transform
ENOB	Effective Number of Bits
QVCO	Quadrature Voltage Controlled Oscillator
THA	Track and Hold Amplifier
BiCMOS	Bipolar Complementary Metal Oxide Semiconductor
Op-amp	Operational Amplifier
DFT	Discrete Fourier Transform
DC	Direct Current

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List of Symbols

Symbol	Description
C_H	Hold Capacitor
V_{IN}	Input Analog Signal
V_{DD}	Supply Voltage
W	Width of Transistor
L	Length of Transistor
Q_{ch}	Channel Charge
C_{ox}	Oxide Capacitance
V_{TH}	Threshold Voltage
ΔV	Error Voltage
V_{OUT}	Output Voltage
γ	Body Effect Coefficient
C_{ov}	Overlap parasitic capacitance per unit width
I_L	Leakage Current
V_{pp}	Peak-to-Peak Voltage Amplitude
$R_{on,tg}$	On-Resistance Transmission Gate
K	Transconductance Parameter
V_{GS}	Gate to Source Voltage
$V_{battery}$	Battery Voltage
V_{cm}	Input Common-Mode Voltage
V_{inp} , V_{inn}	Input Signals
CLK, CLKB	Clock Signal

V_{d1}, V_{d2}	Single ended outputs from Transmission Gate
V_{outp}, V_{outn}	Single ended outputs from Output Buffer
f_{in}	Input Signal Frequency
F_s	Sampling Frequency
N_{FFT}	Number of Samples in FFT

Chapter 1

Introduction

1.1 Introduction

Digital Integrated Circuits are the base of modern technology. High-tech devices like smart phones, tablets, laptops, microprocessors and microcontrollers are based on digital circuits. But, the physical signals like sound, atmospheric pressure and temperature etc. are analog ones. Thus, we require a mechanism using which the continuous analog signals can be converted into digital ones so that it can further be processed by digital circuits. This is done using Analog-to-Digital Converters (ADCs). ADC is an analog device that converts a continuous analog signal (that may have infinite number of levels or values) to digital number (that has finite number of levels) which represents the signal's amplitude. Analog to Digital Converters (ADCs) have an important role in interfacing the digital and analog circuit world.

1.2 Need of Track and Hold Circuit

Prior to the quantization process in ADC, sampling of continuous time signal is done. Sampling involves a process in which a continuously varying signal is initially converted to a discrete time signal. The value of the signal is measured at distinct time-intervals and provided as an input to ADC for further conversion process. If ADC uses a continuous varying signal, then the fluctuations can disturb the conversion process and may lead to wrong digital outputs. The Track and Hold (T/H) circuit has two modes of operation:

a. Track Mode: In this mode, the output tracks or follows the input analog signal.
b. Hold Mode: In Hold mode, the output holds a value for some predetermined period of time. This time must be greater than the time taken by ADC to complete its conversion process. Otherwise, the ADC may give erroneous results. [1]

Thus, Track and Hold circuit is an important building block in circuit design.

1.3 Track and Hold Circuit Vs Sample and Hold Circuit

The ideal sampling responses of T/H and S/H circuits are shown in fig. 1.1.

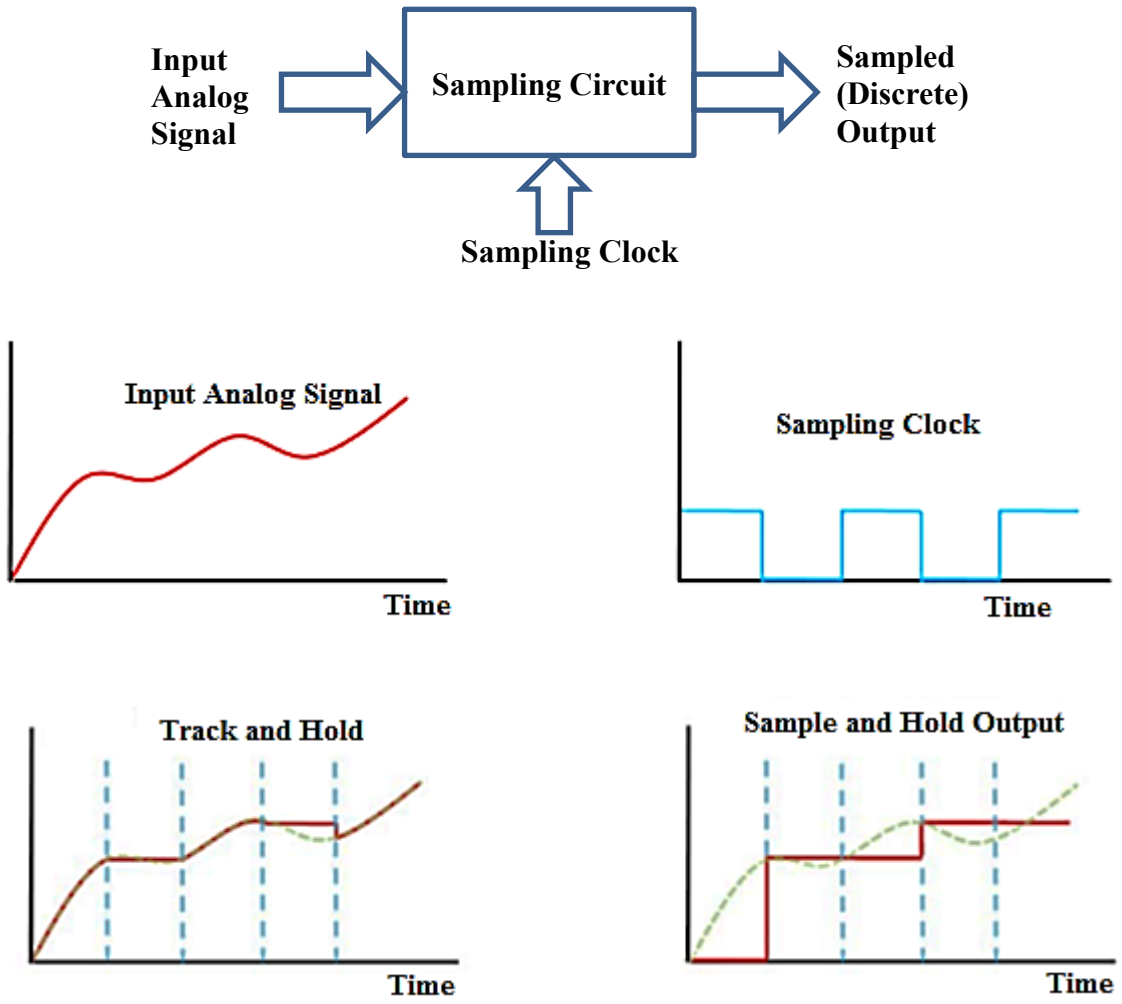

Fig. 1.1 Ideal Sampling Response of Track and Hold and Sample and Hold Circuit

The input analog signal is sampled at fixed intervals of time and then stored across a capacitor for some fixed period. In T/H circuit, the output follows the input signal before hold state while in S/H circuit; a staircase waveform is produced at the output. For T/H response of fig.1.1, the high level or rising edge of clock shows the tracking mode while the low level or falling edge defines the hold mode. For S/H circuit, the falling edge is defining the sampling instant and sampled data is being hold for one clock cycle.

1.4 Basic T/H Circuit Architecture and Operation

All T/H circuit has four major components: Input amplifier, Capacitor (energy storage device), Switch and its control circuitry and output buffer. The block diagram of T/H circuit is shown in fig. 1.2.

a. **Input Amplifier:** The main function of input amplifier is to provide high impedance to the input signal source (buffering action). It also provides a high current gain so as to charge the capacitor.
b. **Capacitor:** It is the heart of T/H circuit. In track mode, the capacitor's voltage follows the input signal amplitude with some bandwidth limiting and delay. In hold mode, the switch will disconnect the input signal source from the main operating circuitry and capacitor will retain the voltage it encountered just before the switch gets opened. [3]
c. **Switching Circuits:** The simplest switches used in T/H circuits are: nMOS transistor, pMOS transistor or, transmission gate. Switch and its control circuitry alternatively switches the T/H circuit between track and hold modes.
d. **Output Buffer:** The main purpose behind using output buffer is to offer high impedance to the hold capacitor so that it will not discharge the voltage ahead of time.

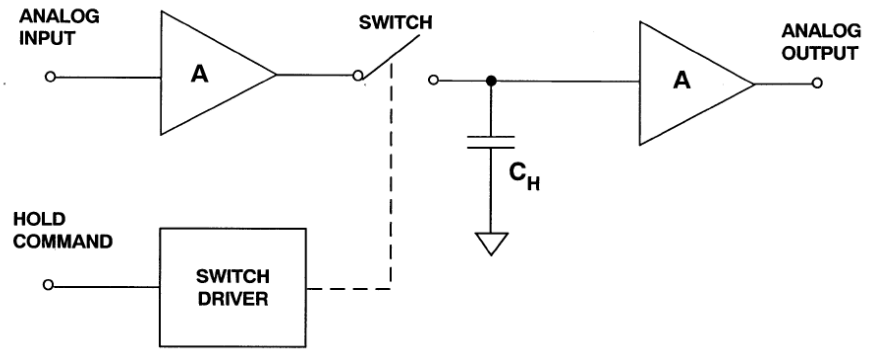

Fig. 1.2 Block Diagram of Track and Hold Circuit [4]

The simples T/H circuit in MOS technology is shown in fig. 1.3, where CLK represents the clock signal used for switching between track and hold mode, V_{IN} is the analog input signal, M1 is the nMOS transistor acting as a switch, C_H is the hold capacitor and V_{OUT} is the sampled output. [2]

When CLK is High, nMOS transistor goes into linear region if the input is less than the clock signal amplitude by at least one threshold. The drain and source terminals of transistor act as short-circuit. So, the output follows the input signal (TRACK MODE)

and the charge at the input node goes onto the hold capacitor through the transistor's channel. When CLK is low, M1 goes into cut-off and thus input and output nodes are disconnected. So, C_H holds the input signal amplitude encountered at the falling edge of

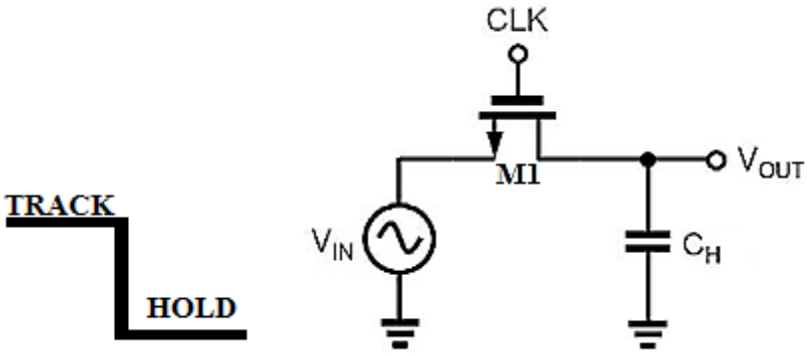

Fig.1.3 Simplest Open Loop T/H circuit in MOS technology[5]

CLK (HOLD MODE) till the next rising edge of CLK. This is the ideal working of T/H circuit but practically there are some limitations like charge injection, clock feedthrough and pedestal error etc. [3]

1.5 Limitations in T/H Circuit

There are a number of factors that contribute to the non-idealities in T/H circuit like the practical circuit design limitations and the intrinsic device noise etc. These non-idealities are described as:

a. Charge Injection: When a MOS transistor is in ON state and operating in linear region, the potential difference between its drain and source terminal is negligibly small. In this state, mobile charge carriers are present in channel region. When the transistor goes to OFF state, this charge will flow out through the drain and source junctions. This is shown in Fig. 1.4.

When the switch is ON, the inversion charge stored by the transistor in its channel region is given as

$$Q_{ch} = WLC_{ox} (V_{DD} - V_{in} - V_{TH})$$

Where W and L are width and effective channel length of transistor, C_{ox} is oxide capacitance, V_{TH} is threshold voltage of capacitor, and $V_{DD} - V_{in}$ denotes the gate-to-

source voltage of transistor. When the transistor gets OFF, Q_{ch} is injected towards source and drain. The input source absorbs the charge injected towards left side, and thus this charge does not create any error.

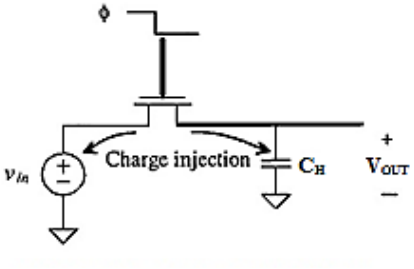

Fig. 1.4 Charge Injection Phenomenon [5]

The charge injected towards right side affects the voltage of capacitor and thus produces an error voltage. If half of total inversion charge is injected towards right side, then error voltage is given as

$$\Delta V = \frac{WLCox\,(V_{DD} - V_{in} - V_{TH})}{2C_H}$$

Practically, fraction of charge that is injected to source and drain terminals depends on the transition time of clock. If transition time is less, then inversion charge disappears quickly. Thus, the equal amount of charge is injected on both the terminal irrespective of the value of output impedance. If transition time is large, the charge injected on each terminal is a complex function of impedance at each terminal with respect to ground. [5] The nMOS has electrons as charge carriers; a negative pedestal at the output appears due to charge injection phenomenon.

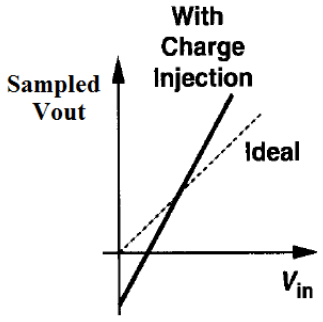

Fig. 1.5 Input Output Characteristics of Sampling Circuit with Charge Injection [5]

Ideally, $V_{OUT} = V_{in}$. With charge injection, the output voltage becomes

$$V_{OUT} = V_{in} - \frac{WLCox\,(V_{DD} - V_{in} - V_{TH})}{2}$$

$$V_{OUT} = V_{in}\,(1 + \frac{WLCox}{C_H}) - \frac{WLCox}{C_H}\,(V_{DD} - V_{TH})$$

Considering Body effect, the output voltage is given as

$$V_{OUT} = V_{in}\,(1 + \frac{WLCox}{C_H}) + \gamma(\frac{WLCox}{C_H})\ (\sqrt{2\phi_B + V_{in}}) - \frac{WLCox}{C_H}\,(V_{DD} - V_{TH0} + \gamma\sqrt{2\phi_B})$$

In all, charge injection leads to three types of voltage error in switched capacitor circuits. These are:

i. Gain Error
ii. Non-linearity
iii. DC Offset

Charge Injection Cancellation: Charge Injection effect can be cancelled by using a dummy switch as shown in fig. 1.6. Here M1 is the sampling switch and M2 is dummy switch. Only one out of two switches will be in ON state at a time. When CK=0, M1 gets OFF and M2 gets ON. The inversion charge injected by M1 on hold capacitor will be absorbed by M2 to create its own channel.

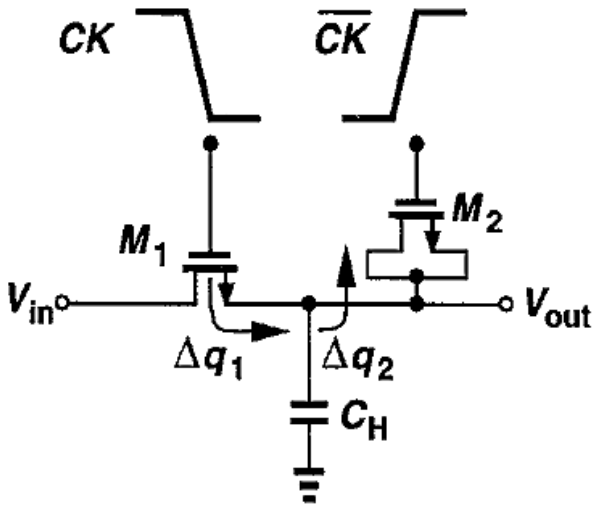

Fig.1.6 Charge Injection Cancellation [5]

The error voltage on hold capacitor will be zero if the charge injected by transistor M1, Δq_1 is completely absorbed by M2, Δq_2. If M1 injects half of inversion charge towards right side, so

$$\Delta q_1 = \frac{\text{WLCox}\,(V_{DD} - V_{in} - V_{TH})}{2}$$

and, $\Delta q2 = \text{WLCox}\,(V_{DD} - V_{in} - V_{TH})$. For $\Delta q_1 = \Delta q_2$, W_2 must be equal to $0.5W_1$ and $L_2 = L_1$. [5]

Another method to reduce the charge injection is to use a transmission gate which has both nMOS and pMOS in parallel. The charge packets injected by both MOS are of opposite polarity and thus will cancel out each other.

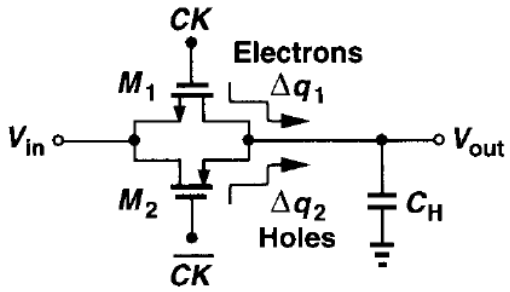

Fig.1.7 Transmission Gate Reducing the Effect of Charge Injection [5]

b. Clock Feedthrough: Due to the presence of gate-source and gate-drain overlap parasitic capacitances, a MOS transistor couples the transitions in clock to sampling capacitor. It leads to an error in the output voltage. This error voltage is given as

$$\Delta V = V_{CK}\,\frac{W\,C_{ov}}{W\,C_{ov} + C_H}$$

Where C_{ov} is overlap parasitic capacitance per unit width (W). The above equation shows that the error voltage is independent of input signal source. So, it leads to dc offset error.

Clock Feedthrough Suppression: Using a dummy switch having half of aspect ratio as that of main sampling switch, clock feedthrough suppression is possible. [5]

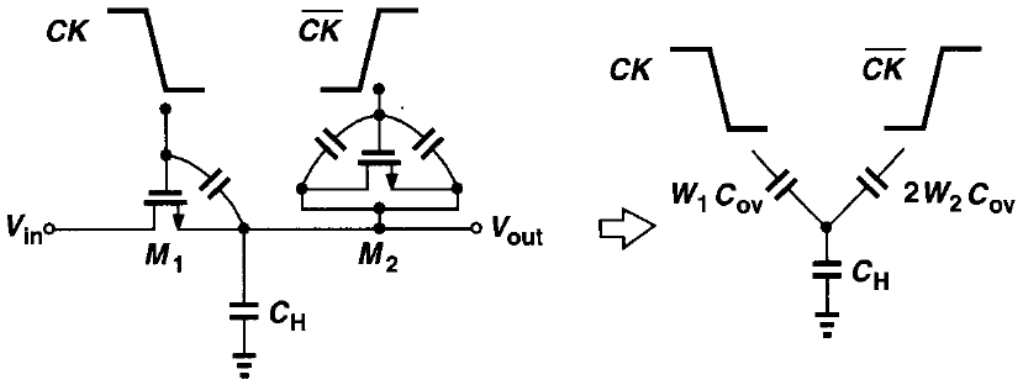

Fig.1.8 Clock Feedthrough Suppression Technique [5]

Using this configuration, the total charge at the output is zero.

$$-V_{CK}\frac{W_1 C_{ov}}{W_1 C_{ov} + C_H + 2W_2 C_{ov}} + V_{CK}\frac{2W_2 C_{ov}}{W_1 C_{ov} + C_H + 2W_2 C_{ov}} = 0$$

1.6 Specifications of Track and Hold Circuit

a. Total Harmonic Distortion (THD): THD is the ratio of root mean square (rms) value of harmonics of input signal to rms of fundamental signal itself.

If power signals,

$$THD\ (\%) = 100 \times \sqrt{\frac{P_2 + P_3 + P_4 + \cdots + P_n}{P_1}}$$

Here, P_n is in watts.

For voltage signals,

$$THD\ (\%) = 100 \times \sqrt{\frac{{V_2}^2 + {V_3}^2 + {V_4}^2 + \cdots + {V_n}^2}{{V_1}^2}}$$

Here, V_n represents rms voltage.

b. Signal-to-Noise Ratio (SNR): SNR is the ratio of signal power to the noise power. It is generally expressed in decibels (dB).

$$SNR = \frac{P_{signal}}{P_{noise}}$$

where P represents the average power. Also,

$$SNR_{dB} = 10log_{10}(SNR)$$

$$SNR_{dB} = P_{signal_{dB}} - P_{noise_{dB}}$$

If SNR is high, it is easier to isolate the signal from noise. If SNR is zero, it means that the desired signal is indistinguishable from the noise. So, a high value of SNR is desirable. SNR can be either positive or negative when expressed in dB scale. If SNR is negative, it means that the signal power is lesser than the noise power. [4]

c. Signal-to-Noise and Distortion Ratio (SINAD): SINAD is the ratio of total power of signal i.e. desired signal, distortion and noise to the power of unwanted signal i.e. distortion and noise. Unwanted signal includes harmonics but excludes the dc component. Higher the value of SINAD better is the quality of the signal.

$$\boldsymbol{S}INAD = \frac{P_{signal} + P_{noise} + P_{distortion}}{P_{noise} + P_{distortion}}$$

It is generally expressed in dB.

Both SNR and SINAD are calculated from FFT. For SNR calculation, signal harmonics are not considered. So, only noise terms are left along with original signal. Practically, first five harmonics are excluded as they are dominant. SNR gets degrade at high frequencies, but the rate of degradation is less as compared to that of SINAD.

d. Spurious Free Dynamic Range (SFDR): It is defined as the ratio of rms value of the fundamental signal to the rms value of worst spur in the frequency domain. This spur may not be a harmonic component of the input signal. It is also known as the dynamic range. [4]

SFDR can be represented

a. with respect to input signal amplitude level.

b. with respect to Full scale.

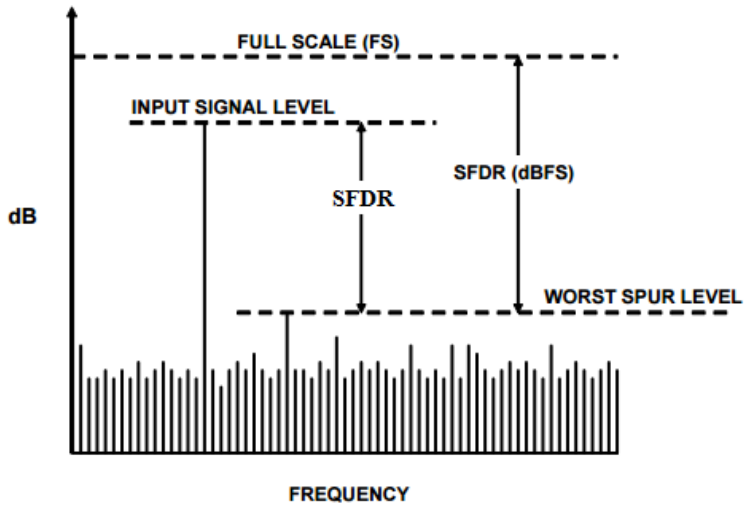

Fig.1.9 Spurious Free Dynamic Range

SFDR specifies the smallest signal power that can be distinguished from large interfering signal.

$$SFDR = 20\ \log\frac{rms\ value\ of\ Fundamental}{rms\ of\ Highest\ Spur}$$

e. **ENOB (Effective Number of Bits):** It also measures the dynamic performance of the circuit. The number of bits used to represent analog value defines the resolution of a circuit. But, all real circuits have noise and distortions. Thus, ENOB represents the resolution of an ideal circuit having same resolution as the circuit under consideration. Mathematically, the relation between Effective number of bits and SINAD is described by the following equation

$$ENOB = \frac{SINAD - 1.76dB}{6.02}$$

This equation is valid for a full-scale input signal. If signal level is less, both SINAD and ENOB decrease. For reduced input signal level, the equation will become

$$ENOB = \frac{SINAD - 1.76dB + 20\log\frac{Full\ Scale\ amplitude}{Input\ Amplitude}}{6.02}$$

ENOB normalizes to full scale due to this additional factor regardless of the input signal value. [4]

f. Droop Rate: It defines the rate of change of output voltage level per unit time in hold mode. As soon as the circuit undergoes transition from track to hold mode, the measurement begins immediately. It occurs due to the leakage from the hold capacitor. The leakage current consists of bias current and switch leakage current.

$$Droop\ Rate = \frac{dV_{OUT}}{dT}\left(\frac{Volts}{Sec}\right) = \frac{I_L}{C_H}$$

Here I_L is the leakage current of hold capacitor, C_H. Generally, an output buffer is added to reduce the leakage current.

g. Settling Time: Settling time (in Hold Mode) is defined as the time needed by the output voltage to settle within a specified error band after hold phase has started. The error band can be .01%, .1% or 1% of full scale input. It is one of the components that decide the maximum sampling frequency for the circuit.

h. Aperture Time: It is the time delay when the hold command is applied and the input signal and the hold capacitor get completely disconnected.

i. Aperture Jitter: The uncertainty in aperture time with sample-to-sample variations is known as aperture jitter.

1.7 Open Loop Vs Close Loop Architecture

In open loop architecture, voltage followers are used as input and output buffers as shown in fig. 1.10. As there is no feedback between the output and input buffers, thus the settling and acquisition time are lesser. So, this configuration is comparatively faster.

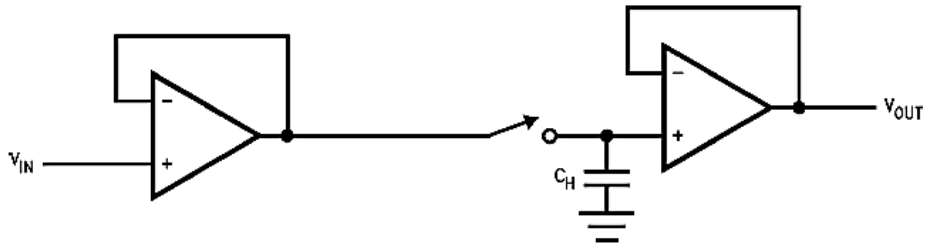

Fig. 1.10 Open Loop Architecture

The disadvantage of this configuration is in its accuracy. Due to the absence of feedback, the dc error of both amplifiers adds up and affects the accuracy of the circuit.

Closed Loop Architecture has a feedback path between output and input as shown in fig. 1.11. Due to feedback, the accuracy improves on the cost of speed.

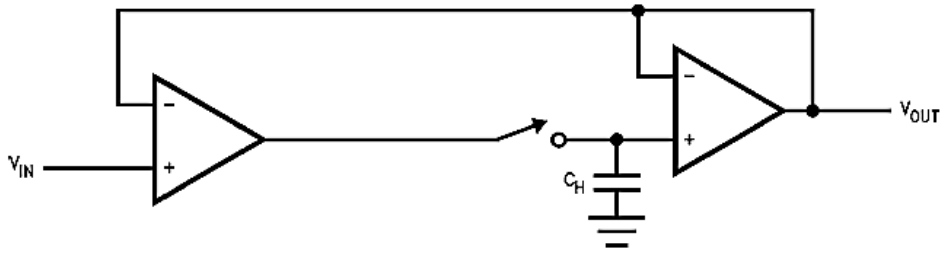

Fig. 1.11 Close Loop Architecture

The organization of the thesis work is as follow:

Chapter1 gives a basic introduction of Track and Hold Circuit. It discusses the basic architecture and working of the circuit. It also explains its limitations and the techniques used to overcome them.

Chapter 2 discusses the different work done on Track and Hold Circuit and the techniques adopted to suppress the limitations discussed above. It describes the literature review of different architectures of T/H and the optimization of its performance parameters.

Chapter 3 discusses the proposed circuit with the detailed explanation of its architecture and working. It shows the transient response of the circuit along with its various performance parameters. It also shows the behavior of parameters with variation in input signal frequency, amplitude and sampling frequency.

Chapter 4 concludes the discussion and explains the future scope of the proposed circuitry.

Chapter 2

Literature Review

[1] Shunli Ma, Hao Yu, Junyan Ren: A 32.5GS/s Sampler with Time-Interleaved Track-and-Hold Amplifier in 65nm CMOS [6].

This architecture is based on switched source follower having active inductors as load. It has very high speed for track and low feed-through in hold mode consuming very small area of 0.07mm^2. To cancel out the clock feed through problem, an additional transistor controlled by clock signal is used. This work is done in 65nm CMOS technology and power consumption of the circuit comes out to be 211mW. This circuit operates at 3.3V of power supply and draws 60.1 mA of current. Due to time-interleaved structures with two channels, double sampling rate is attained. For this QVCO i.e. quadrature voltage controlled oscillator is used to generate an on-chip in-phase clock. Using QVCO, this structure can be implemented for four channel time-interleaved structure. Through S-parameters calculations, the output and input return losses are better than −10dB up to sampling frequency of 40GHz. The input compression point of THA is measured at 1GHz and comes out to be −6dBm. By sweeping the input frequency from 1 to 16GHz, a nearly flat curve up to 10GHz is obtained. It shows that THA is linear with respect to input signal. The bandwidth of 19.3GHz is attained in track mode due to the usage of active inductors. For input signal of 6GHz and sampling rate of 32.5GS/s, the peak THD and SFDR are −37dB and 37.42dB respectively.

[2] Gregor Tretter, David Fritsche et al: A 55GHz Bandwidth Track-and-Hold Amplifier in 28nm Low-Power CMOS. [7]

This work presents switched capacitor based track and hold amplifier in 28nm low-power CMOS process. This circuit consists of an input buffer with an input matching network, the track and hold core, an output buffer with a driver stage. Switched Capacitor topology suffers from low-pass behavior at high frequencies, but allows large amplitude signals. By increasing the amplitude of signal at high frequencies, low-pass problem is overcome. Another methodology adopted to increase the small-signal bandwidth is the frequency

compensation technique. It increases the bandwidth to 70GHz (30% increase). The 3-dB corner frequency for large signals comes out to be 55GHz. Thus, this Track and Hold amplifier can be used with a 100GS/s time-interleaved ADC. For input signal having peak-to-peak amplitude of 400mV and frequency of 50GHz, THD is found to be –32dB. For this signal, the power consumption is 73mW from two power supply domains of 1.4V and 1.75V. The THA uses 1.4V power supply while clock buffer circuitry is connected to 1.75V supply. THD is increasing with the amplitude of the input signal. This chip consumes an active area of $0.03mm^2$.

[3] Yu-Cheng Liu et al: Design and Analysis of CMOS High Speed High Dynamic-Range Track-and-Hold Amplifiers [2]

This work presents two track and hold amplifiers having very high dynamic range and high speed. One THA is implemented in 65nm CMOS technology, and other in 90nm CMOS technology. The architecture of THA in 65nm technology with a power supply of 1.8V is based on cascade buffers with high inductive peaking. Moderate transistor transconductance, conductor loss and lossy silicon substrate limits the bandwidth of CMOS circuits. To extend the bandwidth and to compensate the high frequency loss, inductive peaking is used. It has good linearity and wide bandwidth. The maximum input signal bandwidth is 7GHz, having Total Harmonic Distortion and spurious Free Dynamic Range of –44.5dB and 44.6dB respectively. The power consumption comes out to be 197mW. The chip area needed for this circuit is $0.9 \times 1mm^2$. The droop rate is 0.17mV/ps with peak-to-peak amplitude of 400mV and sampling rate of 10GS/s. The THA in 90nm technology is designed using distributed buffers with a power supply of 2.6V. Distributed amplifiers are used in input buffers to get better values of input return loss and bandwidth. It consumes 216mW of dc power. The maximum input signal bandwidth is 19GHz, having Total Harmonic Distortion and spurious Free Dynamic Range of –44.5dB and 47.5dB respectively. It needs chip area of $1 \times 0.64mm^2$. The output power is greater than –22dBm sampling frequencies of 6GS/s and 12GS/s over entire range of bandwidth. The circuit has high sampling rate, high linearity, high SFDR, less chip area and broad bandwidth. This circuit is useful for front end sample and hold application like broadband data converter.

[4] Heather Orser, Anand Gopinath: A 20GS/s 1.2V 0.13µm CMOS switched Cascode Track and Hold Amplifier. [3]

This architecture uses a differential distributed amplifier as an input amplifier and to increase the bandwidth of the Track and Hold circuit. The distributed amplifier's output is fed as an input to THA core circuitry. The output of THA core drives output buffer of resistance 50Ω. It is operating at a power supply of 1.2V and thus consumes very low power of 71mW. It is implemented in 130nm CMOS technology. The sampling rate of THA is 20GS/s. The full scale input voltage is 0.2Vppd, which is quite less. It is due to the usage of low power supply voltage which imposes restriction of voltage headroom. THA attains 3-dB bandwidth of 1.8GHz and droop rate of .002mV. Due to non-linearity of the amplifier, the effective number of bits is not high, but it can be used for ADCs with 6 bits of resolution. The area occupied by the chip is .09mm^2. Using S-parameters, output and input return losses were calculated from dc to 13.5GHz of frequencies. The output return loss is better than −15dB. The input return loss is better than −10dB from 100MHz to 13.5 GHz frequencies. The minimum Spurious Free Dynamic Range for input frequencies up to 4GHz with sampling rate of 20GS/s comes out to be 30dB. The maximum SFDR is 34dB.

[5] He-Gong Wei et al: A Rapid Power-Switchable Track and Hold Amplifier in 90nm CMOS. [8]

This paper presents a complete differential Track and Hold amplifier with a power switchable feature. The open loop architecture gives high speed and accuracy but consumes a lot of static power. A power switchable THA withdraws negligible power when the circuit is at rest i.e. static power consumption is zero. It has bootstrapped network to enhance the linearity of the circuit. To increase the accuracy and speed, a unity gain buffer is added between bulk of source follower and the input terminal. It is designed in 90nm CMOS technology with a power supply of 1.2V. Power Switchable technique does not require any extra voltage headroom. So, it has large input voltage swing of 0.8Vpp. With this technique, the sampling speed and accuracy of the circuit is also increased. For an input signal with having peak to peak amplitude of 0.8V, frequency of 40.6MHz and sampling frequency of 100MS/s, Spurious Free dynamic

range of 70dB is achieved. For a load capacitance of 2.5pF, the circuit consumes power of 2.97mW. The total harmonic distortion of THA and SNDR are 60dB and 61dB respectively. The active area of the chip is 0.18×0.13 mm^2.

[6] Shouri Chatterjee, Peter R. Kinget: A 0.5V 1-Msps Track-and-Hold Circuit with 60dB SNDR. [9]

This architecture of differential Track and Hold circuit operates on a very low power supply voltage of 0.5V. The input and output common mode voltage of the circuit is half of the power supply i.e. 0.25V. It is a fully differential circuit designed in 250nm Bi-CMOS process. All transistors have threshold voltage of 0.6V. It is a true low-voltage design i.e. the voltage at all the nodes in the circuit are less than the power supply. No clock boosting and voltage boosting technique is being used. For sampling frequency of 1MHz, it has the dynamic range of 60dB. The current flown through the circuit is 600µA, and thus the total power consumption is 300µW, which is quite less as compared to other track and hold amplifiers. For input frequency of 495 kHz, the peak SNDR is 57dB. It has hold mode droop rate of 7.6µV/µsec on differential output. The track mode bandwidth of the circuit is 3.9MHz. The chip area of the circuit is 0.16mm^2. Two cascaded Track and hold circuits can be used as a sample and hold circuit. One works as master and other as slave. When hold phase of master T/H circuit will end, the slave undergoes transition from track to hold mode. Both will be ON for a short time when both are in track mode. Both are operated with same clock frequency.

[7] L-H Wang et al: A 5 bit, 10 GSamples/s Track-and-Hold Circuit with input feedthrough cancellation. [10]

This work presents a track and hold circuit with additional feature of input feedthrough cancellation. On using a T/H circuit with input signal feedthrough in an ADC, it will degrade the overall performance of the system. To cancel out the effect of input signal feedthrough, analog adder is used. It has fully differential sampling circuit topology. Two source coupled pairs are used to design analog adder. It increases the linearity of the system and enhances the bandwidth also. Using this technique, the output SNDR is improved from 22.5dB to 49dB. An output buffer is also designed by two source-coupled

pairs connected in cascade. The first pair is realized with inductor shunt peaking technique. It also increases the bandwidth of the circuit. The second pair uses resistance as load. This T/H circuit is designed in 180nm CMOS technology. For 2.5GHz input sinusoidal signal and T/H circuit operating at a sampling frequency of 10GSamples/s, the effective number of bits is 5. Maximum Total harmonic distortion and SFDR are –37.7dB and 38.4dB respectively. The chip area is 1.5×0.82 mm^2. The power consumed by the circuit is 200mW.

[8] Huseyin Dinc et al: A 1.2 GSamples/s Double Switching CMOS THA with -62dB THD. [11]

This paper presents the Track and Hold Amplifier with negligible hold mode feedthrough problem. To overcome this problem, cross-coupled capacitor technique is generally used but it requires the matching of feed-forward capacitors and cross coupled capacitors. This work presents double switching switched buffer Track and Hold Amplifier circuit. Without using the cross coupled capacitors, it provides good hold mode isolation. It uses a switching input buffer. The power and area used by this technique is quite less as compared to other techniques. It reduces power by 20 – 30%. Chip 1 and chip 2 dissipates power of 150mW and 183mW. With an output buffer, it will increase. The clock buffer consumes 100mW and 75mW of power respectively. For analog circuitry, 3.3V power supply is used while for digital circuitry, power supply voltage is 1.8V. The circuit is implemented in 180nm CMOS technology. With a sampling frequency of 1.1GHz and input signal of 400mV with Nyquist frequency, THD is less than –60dB. The second chip provides a SFDR of 62dB with a sampling frequency of 1.6GHz and Nyquist input frequency. To preserve signal integrity in first chip, conservative shielding approach is used. The layout parasitics in second chip are smaller and thus its performance is better at high frequencies. The other reason behind better performance at high frequency is the usage of small load resistors, but it leads to increase in power dissipation. The power dissipation in clock buffer of second chip is quite less. Thus, both the chips have almost same power consumption. The limitation is that the chips can have the input signal swing of 0.5 V_{pp} as the circuits telescopic cascade structure and NMOS transistors only. This can be improved by using low V_T transistors.

[9] T.-S, Lee et al: Design Techniques for low voltage high-speed pseudo differential CMOS Track and Hold Circuit with low hold pedestal. [12]

This paper presents a low voltage and low hold pedestal Track and Hold Circuit. It uses the concept of Miller effect during the hold mode of operation of Track and Hold circuit. This circuit has pseudo- differential double sampled configuration. This circuit can be used in low voltage applications. It is designed in 350nm CMOS technology. The main factor that made it possible to implement a low voltage THA is the bootstrapped switches having rail to rail operation. A 1.5V power supply is being used which leads to a total power consumption of 2.3mW. With a differential input signal with range of –0.4 to +0.4V, the maximum value of differential hold pedestal is 0.8mV. Generally hold pedestal depends on the input signal, but this dependency is reduced with clocks having shorter transition time. It is due to the reason that the miller feedback used in the circuit works better at shorter clock transitions. The possible full scale value of input signal is 0.8 V_{pp}. For a sinusoidal signal of 0.8 V_{pp}, THD varies from -55dB to -45 dB in input signal frequency sweeps from 2MHz to 12 MHz From dc to 8MHz frequency range, Effective number of bits are greater than 8. With increase in input signal frequency, THD is decreasing. THD Vs input signal amplitude is plotted and it is shown that with increase in signal amplitude, THD value is decreasing. It degrades to –60dB to –45dB, when differential input voltage varies from 0.2 to 1.2 $V_{pp.}$

[10] N. Tchamov et al: Differentially pre-compensated GHz-range low-voltage track and Hold. [13]

This paper presents a differential Open-loop Track and Hold circuit for high speed applications. It is pre-compensated T/H circuit with switched source follower. It uses a power supply of 1.5V and is implemented in 130nm CMOS technology. It can be used for low voltage wireless applications. For an input signal of 400MHz and sampling rate of 2.2GS/s, it dissipates power of 1.2mW. A Track and Hold circuit has two major problems: Non-linearity and sampling jitter. A pre-compensation technique is used to overcome it. The first stage is a comparator triggered by input signals. Next stage is sampling switch. For the input and clock signals specified above, the hold mode feedthrough is –28dB. The performance of whole circuitry is linear and has low jitter at

high sampling frequency. It withdraws a current of 0.14mA for comparator and 0.63mA for sampling switch. This Track and Hold circuit can be implemented in SiGe/BiCMOS or Bipolar process.

[11]. S.L. Morton et al: Ku-Band sub-sampling track-and-hold amplifier with 8 ENOB resolution. [14]

This paper presents a Track and Hold amplifier for input signal with frequencies in Ku band. It is a wideband subsampling THA having maximum sampling rate of 2.5GS/s. It follows the architecture of emitter follower as this concept has good sampling approach. This circuit has three stages: emitter-degenerated differential amplifier, emitter follower switch and output buffer. To reduce hold mode feedthrough, a feedback path is provided from output buffer to input cell. Due to this feedback, a high linearity is offered by the circuit at high frequency. With dual tone inputs having frequencies of 12.6 and 12.602GHz and input level of 1dBFS, SFDR comes in range of 59 - 63dB. It is a track and hold circuit with master/slave architecture. For input signal with frequencies up to 2.6GHz, it gives a SNR of 59dB. A single T/H circuit has 49dB of SNR with bandwidth of 14GHz. Up to 2.6GHz frequencies; the clock jitter problem is negligible for the proposed circuit. But, in Ku-band, it degrades the performance. The value of SNR degrades by 6dB at 10GHz frequency as compared to that at 2.6GHz. Thus, low jitter clocks can be used in Ku-band and hence effective number of bits is 8. The power dissipation of Master/slave T/H circuit is 2.5W while a single T/H circuit consumes only 1.5W of power.

[12] Horokazu Yoshizawa et al.: Switched Capacitor Track and Hold Amplifiers with Low sensitivity to Op-amp Imperfections. [15]

This work presents two op-amp based switched capacitors track-and-hold circuits. They have very small gain error in spite of the fact that the op-amp has imperfections. The dc gain and gain bandwidth of op-amp are 46dB and 2.4MHz for the input signal with frequencies in range of 180 Hz to 10 kHz and sampling frequency of 31.2 kHz. All the components of circuits are sized to have a closed-loop gain of 10. To overcome the limitation of op-amp imperfections, concept of continuous time correlated double scheme

is used. A continuous signal path is created which works in track mode. It tells the voltage at output nodes in hold mode. Due to this prediction, an additional advantage of accuracy is obtained for low amplifier gains. Total Harmonic Distortion of more than -70dB is calculated for the proposed circuits. On replacing MOS switches with the ideal ones, THD of –85dB is achieved. As the proposed circuits have less gain errors, so the distortions are also less due to gain squaring. It is due to the fact that MOS switches have parasitic capacitances and the clock feedthrough effect which degrades THD. It uses a power supply of 3V and dissipated 340µW of power. The circuits are designed in 1.2µm CMOS technology. These Track and hold amplifiers have small gain error in entire frequency range.

Chapter 3

Design Methodology and Simulation Results for proposed Track and Hold Circuit

3.1 Introduction

This chapter explains the architecture and working of the proposed Track and Hold circuit and its clock circuitry. After that, various simulation results of the circuit are shown. The parameters like Total Harmonic Distortion, Signal to Noise Ratio (SNR), Spurious Free Dynamic Range (SFDR), Signal to Noise and Distortion Ratio (SNDR) and DC Power Consumption are calculated and plotted varying the input signal frequency.

3.2 Architecture of Proposed Track and Hold Circuit

The proposed Track and Hold Circuit has output buffer, hold capacitor and switch circuitry. A simple transmission gate is used as a switch along with the concept of bootstrapping. A bootstrapped switch is one that has its on-resistance independent of input signal source. A transmission gate has on-resistance given by

$$R_{on,tg} = \frac{1}{2k_p\,(V_{SG,p} - |V_{T,p}|) + 2k_n(V_{GS,n} - V_{T,n})}$$

Here $V_{SG,n}$ and $V_{SG,p}$ are the source-to-gate and gate-to-source voltages of pMOS and nMOS respectively, V_T is the threshold voltage of MOS transistor, k is the transconductance parameter given by $k = \mu C_{ox}\frac{W}{2L}$ (W and L are channel width and length, C_{ox} is oxide capacitance per unit area and μ is the mobility). The input signal source is applied at one terminal (either source or drain) of MOS transistors of transmission gate. So, the overdrive voltage component in above equation will make the transmission gate non-linear. The on-resistance, $R_{on,tg}$ will vary with the input signal amplitude. Fig. 3.1 shows the proposed bootstrapped Track and Hold circuit. The circuit is implemented in fully differential mode in 180nm CMOS technology.

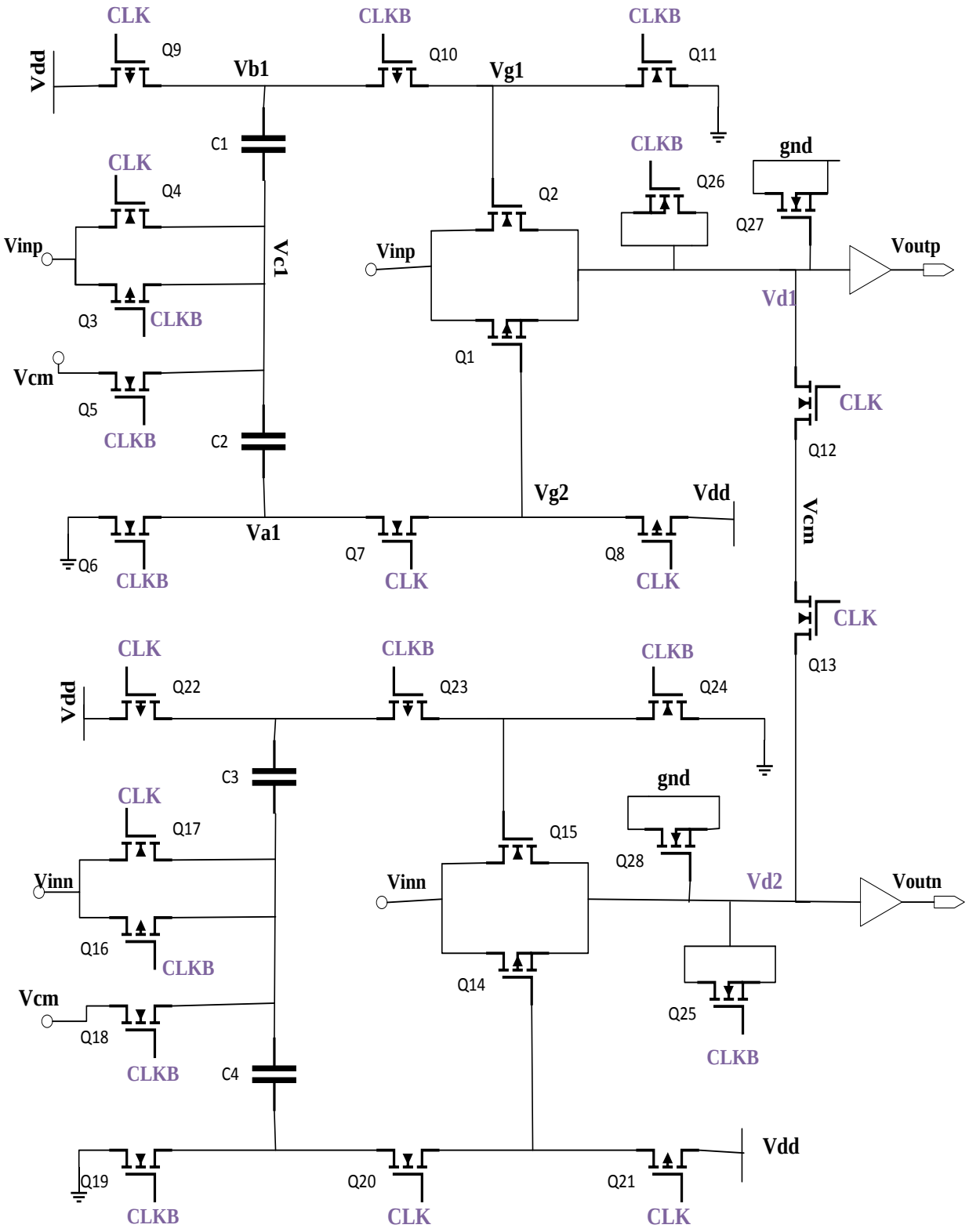

Fig. 3.1 Proposed Track and Hold Circuit

For proper functioning of a simple transmission gate

$$V_{GS,n} = \begin{cases} V_{dd}, & For\ Track\ Mode \\ 0, & For\ Hold\ Mode \end{cases} \quad (1)$$

$$V_{GS,p} = \begin{cases} 0, & For\ Track\ Mode \\ V_{dd}, & For\ Hold\ Mode \end{cases} \quad (2)$$

In fig. 3.1, Q1,Q2 and Q14,Q15 form a pair of transmission gate. Input is applied at drain and source terminals of MOS transistors. Thus, for nMOS transistor Q1 (and Q15)

$$V_{GS,n} = V_{G,n} - V_{inp} \quad (3)$$

$V_{G,n}$ is the gate voltage of nMOS transistor and V_{inp} is the applied input signal as shown in fig. 3.1. $V_{GS,n}$ will be input independent if $V_{G,n}$ has input signal as one of its component. Similarly, the gate voltage of pMOS transistor must contain V_{inp} .

To meet this requirement, input signal has to be superimposed on to the gate voltages of transistors forming transmission gate specified by equation (1) and (2). For this, virtual battery voltages ($V_{battery}$) are created using capacitors C1, C2, C3 and C4. This virtual voltage is added with the input ac signal and applied to the gate voltages of transmission gate. Thus, gate voltage is

$$V_G = V_{battery} + V_{inp}$$

The voltage $V_{battery}$ is the voltage specified in equation (1) and (2) for nMOS and pMOS respectively.[16]- [18]. This is the bootstrapping concept to use a precharged capacitor as a virtual battery, which will ultimately provide a first order approximated linear on-resistance, over the whole input range. [19]-[21]

Table 3.1 shows the different symbols used for signals in Track and Hold Circuit shown in fig. 3.1.

Table 3.1 Description of Symbols used in Schematic

Symbol	**Description**
V_{inp}, V_{inn}	Differential Input Voltage Signal

$\mathbf{V_{cm}}$	Input Common-Mode Voltage
CLK, CLKB	Clock Signal
$\mathbf{V_{dd}}$	Power Supply
$\mathbf{V_{d1}}$, $\mathbf{V_{d2}}$	Single ended outputs from Transmission Gate
$\mathbf{V_{outp}}$, $\mathbf{V_{outn}}$	Single ended outputs from Output Buffer

3.3 Working OF Track and Hold Circuit

The working of Track and Hold Circuit is controlled by two clock signals, CLK and CLKB. CLKB is the complement of CLK signal. Fig. 3.2 shows the two control signals circuitry.

Fig. 3.2 Clock Circuitry

The delay between the two control signals is almost negligible. CLK and CLKB signals are shown in fig. 3.3

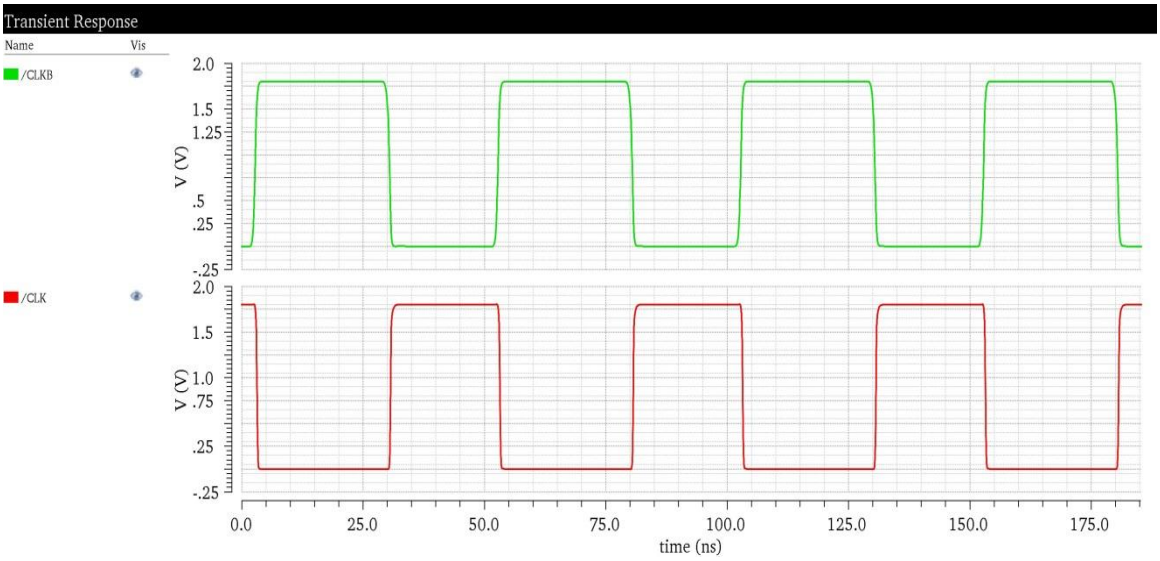

Fig. 3.3 Clock Signals

The working of the circuit is explained as follow. When CLK = 0 (and CLKB = 1),

Q5, Q6, Q8, Q9, Q11, Q26: Transistors will be in ON state

Q1, Q2, Q3, Q4, Q7, Q10: Transistors will be in OFF state

As Q5 is ON, the voltage at node V_{c1} will be the input common node voltage. This voltage is applied to the capacitor's bottom plate. Through Q6, the node V_{a1} gets shorted to ground. As Q9 also conducts in this mode, the node V_{b1} gets connected to power supply. So, the top plates of capacitor C1 and C2 get connected to V_{dd} and ground.

Through Q8, the gate voltage of transistors Q1 becomes V_{dd}, which turns it OFF. Similarly, the gate voltage of Q2 gets connected to ground through Q11 and does not conduct. This ultimately brings the transmission gate in OFF state. Thus, the input source, V_{inp} gets disconnected from the node V_{d1}. This is the HOLD mode of operation.

When CLK = 1 (CLKB = 0),

Q1, Q2, Q3, Q4, Q7, Q10: Transistors will be in ON state

Q5, Q6, Q8, Q9, Q11, Q26: Transistors will be in OFF state

The transistors Q3 and Q4 are ON and hence input voltage get superimposed on the bottom plates of capacitors C1 and C2. At this stage, Q6 and Q9 are OFF, hence V_{a1} and V_{b1} are not connected to ground and V_{dd} respectively. Here V_{a1} is the input signal superimposed over ground level and transferred to the gate terminal of Q1 through Q7. Similarly, V_{b1} is the input signal superimposed over power supply i.e. V_{dd} and transferred to the gate terminal of Q2 through Q10. So, Q1 and Q2 start conducting and the output node V_{d1} tracks the input signal. This is the TRACK mode of operation. The charge at input node gets transferred to hold capacitor through the channel of transistors of transmission gate.

The input signal (V_{in}) has two components: dc component (V_{cm}) and ac signal. This ac component is being superimposed over the gate voltages of Q1 and Q2.

Assuming,

$$V_{in} = V_{cm} + \text{ac component}$$

$$\text{ac component} = V_{in} - V_{cm}$$

The equation for different node voltages are given as

$$V_{a1} = \begin{cases} 0, \ CLK = 0 \\ 0 + (V_{in} - V_{cm}), CLK = 1 \end{cases} \quad (4)$$

$$V_{b1} = \begin{cases} Vdd, \ CLK = 0 \\ Vdd + (V_{in} - V_{cm}), CLK = 1 \end{cases} \quad (5)$$

$$V_{c1} = \begin{cases} V_{cm}, \ CLK = 0 \\ (V_{in} + V_{cm}), CLK = 1 \end{cases} \quad (6)$$

$$V_{g1} = \begin{cases} 0, \ CLK = 0 \\ V_{dd} + (V_{in} - V_{cm}), CLK = 1 \end{cases} \quad (7)$$

$$V_{g2} = \begin{cases} V_{dd}, \ CLK = 0 \\ (V_{in} - V_{cm}), CLK = 1 \end{cases} \quad (8)$$

The output node voltages are given as

$$V_{d1} = \begin{cases} V_{inp}, \ CLK = 1 \\ HOLD \ , CLK = 0 \end{cases} \quad (9)$$

$$V_{d2} = \begin{cases} V_{inn}, \ CLK = 1 \\ HOLD \ , CLK = 0 \end{cases} \quad (10)$$

For fully differential circuit,

Differential input, $V_{in,diff} = V_{inn} - V_{inp}$

Differential Output, $V_{d,diff} = V_{d1} - V_{d2}$

The gate-to-source voltage of Q1 in track mode is given as,

$$V_{GS,n} = V_{dd} + (V_{in} - V_{cm}) - V_{in}$$

$$V_{GS,n} = V_{dd} - V_{cm}$$

Thus, gate-to-source voltage of Q1 only depends on the power supply and the input common mode voltage. It is independent of input signal.

Similarly, for Q2

$$V_{GS,p} = (V_{in} - V_{cm}) - V_{in}$$

$$V_{GS,p} = (-V_{cm})$$

The source-to-gate voltage of Q2 depends only on the input common mode voltage and independent of input signal. Thus, the on-resistance of transmission gate becomes

$$R_{on,tg} = \frac{1}{2k_p\,(V_{SG,p} - |V_{T,p}|) + 2k_n(V_{GS,n} - V_{T,n})}$$

$$= \frac{1}{2k_p\,(-V_{cm} - |V_{T,p}|) + 2k_n(V_{dd} - V_{cm} - V_{T,n})}$$

This is independent of input signal amplitude and depends only on power supply, the input common mode voltage, threshold voltage and transconductance parameter. So, the proposed Track and Hold circuit has linear on-resistance with respect to input ac signal.

The transistors Q27 and Q28 are working as hold capacitors for the circuit. The transistors Q25 and Q26 are used as dummy switch for cancelling the charge injection effect of transistors Q12 and Q13 on the node voltages Vd1 and Vd2. B1 and B2 are output buffers which offer high impedance to the hold capacitors so as to prevent them from discharging ahead of time in hold mode.

Except transistors Q25, Q26, Q27 and Q28, all nMOS transistors have their bulk terminal connected to ground. All pMOS transistors have their substrate terminal connected to Vdd except Q1 and Q14.

3.4 Transistor Sizing and Other Component Values

The aspect ratio of all the transistors used in the schematic is given in Table 3.2.

Table 3.2 Description of Components Used in Proposed Design

Components (Symbol)	**Description**
Q1, Q14	24µ/180n
Q2, Q15	16µ/180n
Q3, Q4, Q5, Q8, Q9, Q16, Q17, Q18, Q21, Q22,	400n/180n
Q6, Q11, Q19, Q24	1.2µ/180n
Q7, Q10, Q20, Q23	800n/360n
Q12	800n/20µ
Q13	800n/1.4µ
Q25, Q26	400n/20µ
Q27, Q28	20µ/20µ
C1, C2, C3, C4	4pF
Vdd	1.8V

3.5 Simulation and Results

The simulation results with their detailed explanation are presented in this section. The results include output waveforms, THD, SFDR, SNDR and SNR with respect to input frequency. The variations of these parameters with sampling frequency are also shown. Also, the graphs of dc power consumption Vs input frequency are presented and

explained. It also explains the concept of coherent sampling. Finally, maximum achievable values of all the parameters are shown in table.

This work is designed in 180nm CMOS technology and all the simulation work is done using CADENCE ®VIRTUOSO ANALOG DESIGN ENVIRONMENT. The parameters like THD, SNDR, SNR and SFDR are calculated by exporting data from Cadence to MATLAB.

Fig. 3.4 shows the signals at the nodes V_{a1}, V_{b1} and V_{c1} with clock (CLK). The simulations are done with input signal of frequency 2MHz and amplitude of 600mV. The sampling frequency is 20MHz. The dc level of input signal is 0.9V. At 591ns, CLK=1 i.e. Track mode is ON. The ac amplitude of input signal, V_{inp} is 1.17315V - 0.9V = 0.27315V. The node voltage V_{c1} is following the input signal as described by equation (6). Similarly, the voltage V_{a1} should be the ac amplitude i.e. 0.27315V according to equation (4). The fig. 3.4 shows the value of V_{a1} as .283mV which is nearer to 273mV. As described in equation (5), V_{b1} should be 1.8 + .27315 = 2.07315V. The value of V_{b1} in plot is nearer to this value.

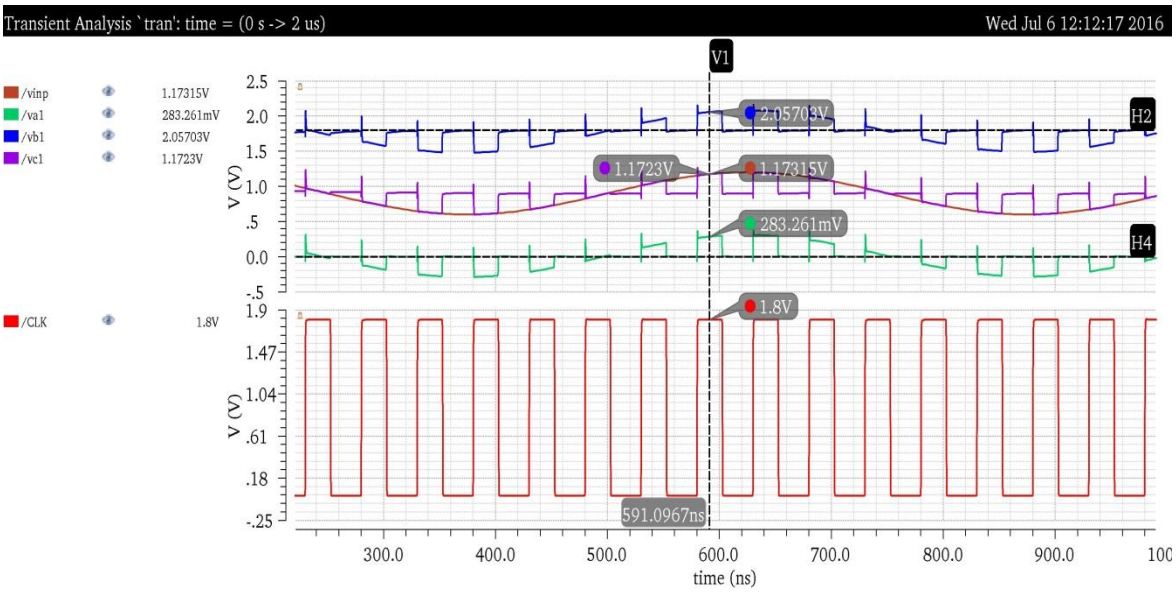

Fig 3.4 Waveforms of nodes V_{a1}, V_{b1} and V_{c1} in Transient Response of Proposed THA

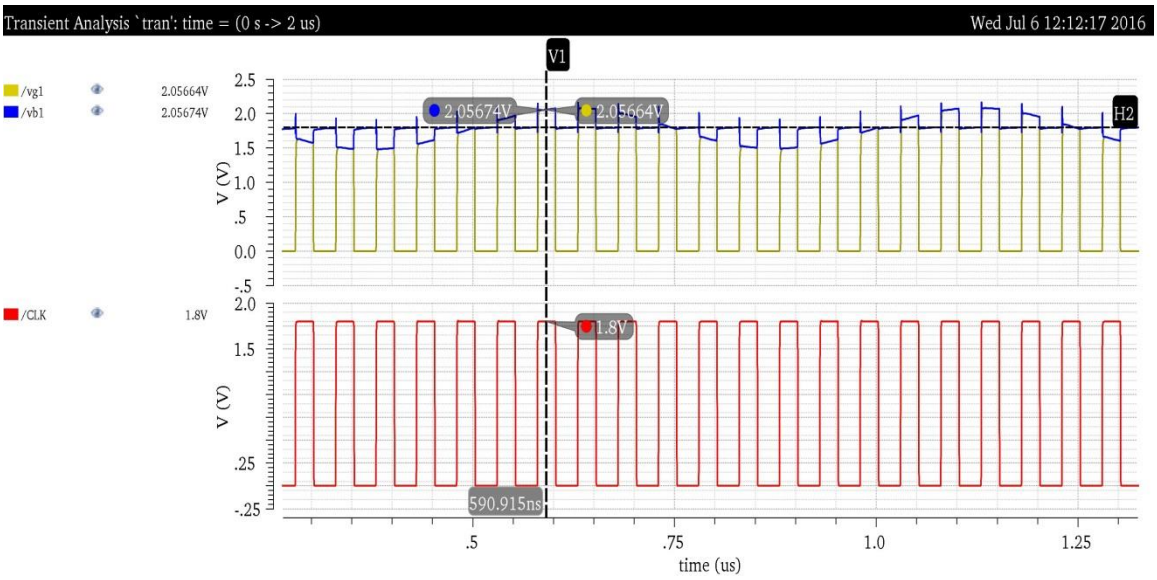

Fig. 3.5 Waveforms of nodes V_{g1}, V_{b1} in Transient Response of Proposed THA

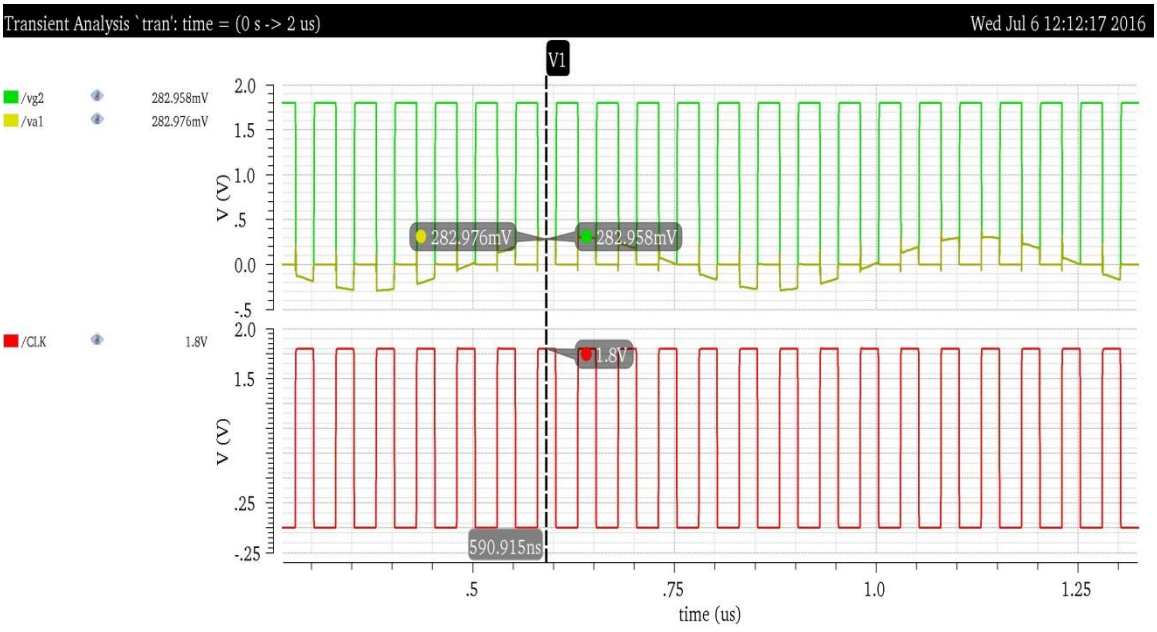

Fig. 3.6 Waveforms of nodes V_{g2}, V_{a1} in Transient Response of Proposed THA

In Track mode, the node voltage V_{g1} follows V_{b1}as explained by equations (5) and (7). This is also shown in fig. 3.5. Similarly, in Track mode, the node voltage V_{g2} follows V_{a1} as explained by equations (4) and (8). Fig. 3.6 shows the same fact.

Single ended and Differential Output waveforms are shown in fig. 3.7 and 3.8 respectively.

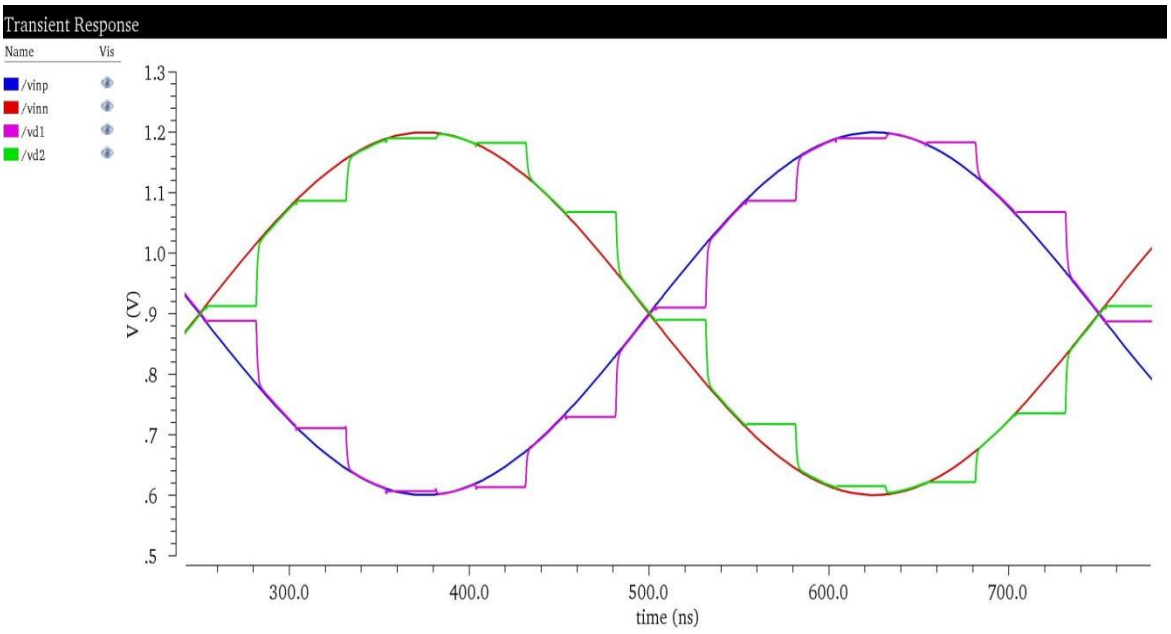

Fig. 3.7 Single ended Output Waveforms of Proposed THA Circuit for input signal with V_{p-p} of 600mV and frequency of 2MHz and sampling frequency of 20MHz

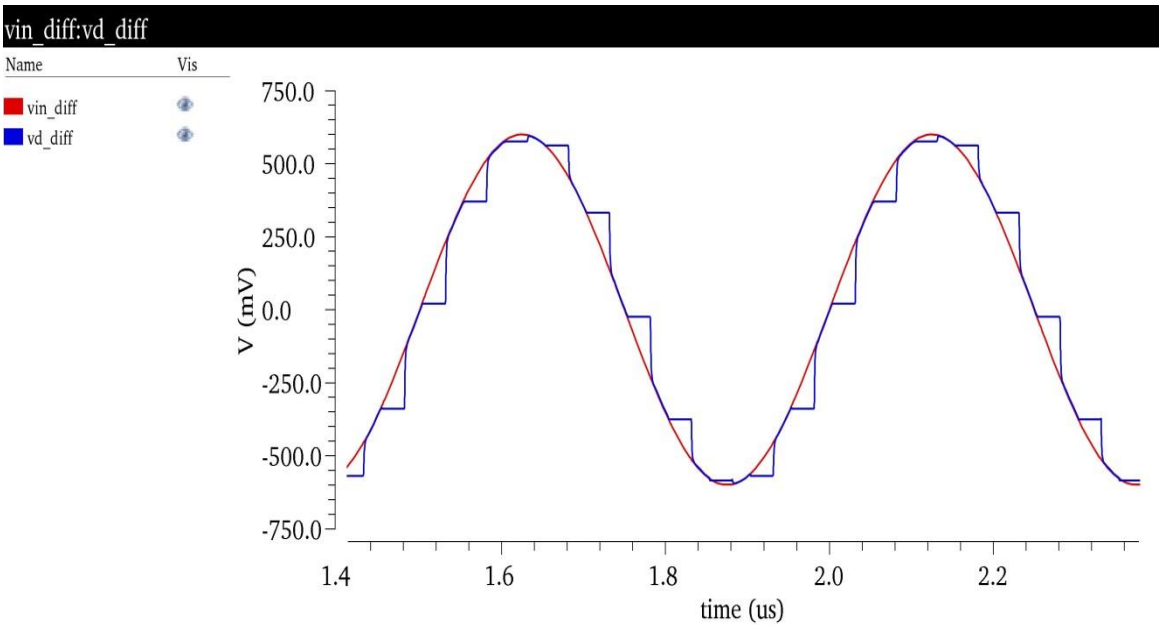

Fig. 3.8 Differential Output Waveforms of Proposed THA Circuit for input signal with V_{p-p} of 600mV and frequency of 2MHz and sampling frequency of 20MHz

The input signals (V_{inp}, V_{inn}) are having peak-to-peak amplitude of 600mV. So, the differential signal (V_{in_diff}) has swing of 1.2V.

Concept of Coherent Sampling

For calculation of SFDR, THD and SNDR, the time-domain signal is converted to its frequency domain. Discrete Fourier Transform (DFT) and Fast Fourier Transform (FFT) show the frequency spectrum of a transient signal. Here, FFT is used to calculate different parameters of Track and Hold Circuit.

Coherent Sampling specifies the relation between sampling frequency (Fs), input frequency of signal (f_{in}), number of samples (N_{FFT}) and number of cycles in sampled set (M). N_{FFT} is selected in such a way so that it becomes an integer with a power of 2. The resolution of FFT is directly proportional to the value of number of samples. The coherent sampling relation is given as

$$\frac{f_{in}}{F_s} = \frac{M}{N_{FFT}}$$

where M should be a prime integer.

All the values of input signal frequencies and sampling frequencies taken for calculating the parameters satisfy the condition of coherent sampling.

Let f_{in} = 2MHz, F_S = 20MHz, N_{FFT} = 1024.

Thus,

$$M = \frac{f_{in}}{F_s} \times N_{FFT}$$

$$= \frac{2}{20} \times 1024 = 102.4$$

The nearest prime number is 103. So, the value of M should be 103.

Thus, input frequency should be

$$f_{in} = \frac{M}{N_{FFT}} \times F_s$$

$$= \frac{103}{1024} \times 20 = 2.0117MHz$$

For input signal with frequency of 2.0117MHz and peak-to-peak amplitude of 200mV, transient response is plotted in CADENCE. Using the value function in calculator of Cadence, the interpolated waveform is plotted. The data of this wave is exported in tabular form as .csv format. In MATLAB, .csv file is used as input for PRETTYFFT code and FFT is plotted. This FFT is used to calculate the parameters of Track and Hold Circuit. For the same input combinations, waveform is plotted in CADENCE Waveform Viewer and the results are verified.

Fig. 3.9 shows the Fast Fourier Transform of the Track and Hold output for input signal with frequency of 2.0117MHz and sampling frequency of 20MHz. The FFT is generally shown between dc to half of sampling frequency (10 MHz).

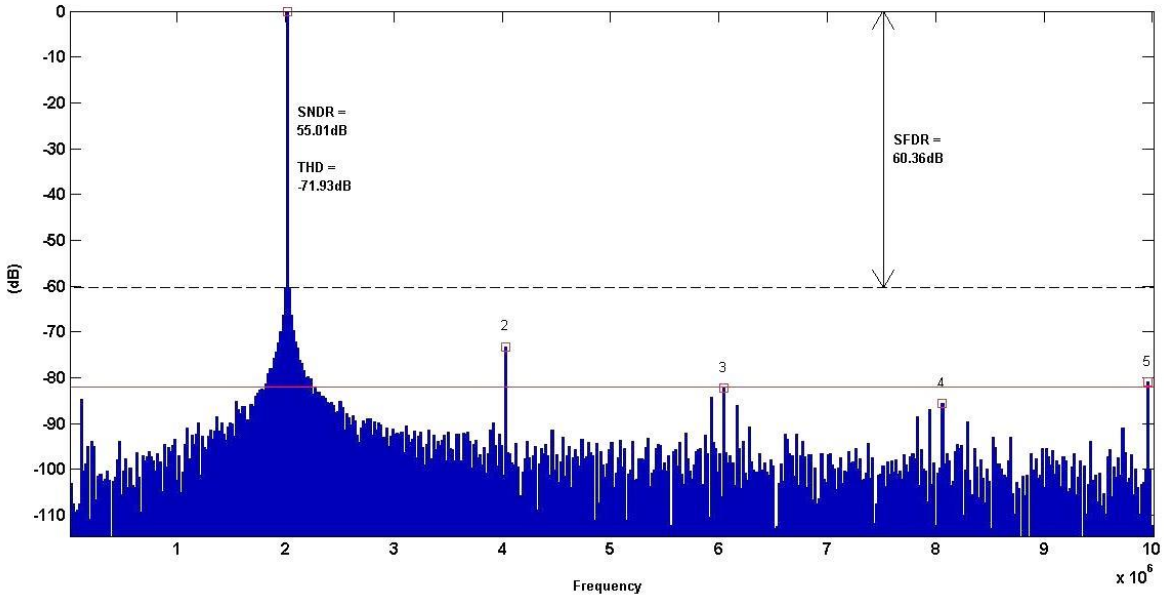

Fig. 3.9 Fast Fourier Transform of output signal of THA circuit for input with frequency of 2.0117MHz ,V_{P-P} = 200mV and sampling frequency of 20MHz

The peak near 2MHz shows the input signal component. In differential configuration, the even harmonics should not be present. But, the exact differential configuration is not possible to achieve. Moreover, there are non-linearities in the circuit. Thus, even harmonics don't eliminate completely but get suppressed by a large amount. The first even harmonic near 4MHz is suppressed by more than 70dB.

Spurious-Free Dynamic Range:

This is one of the most important parameter that tells the fidelity of the circuit. It specifies the non-linearity in the system. Higher the value in dB, lower is the non-linearity in the circuit.

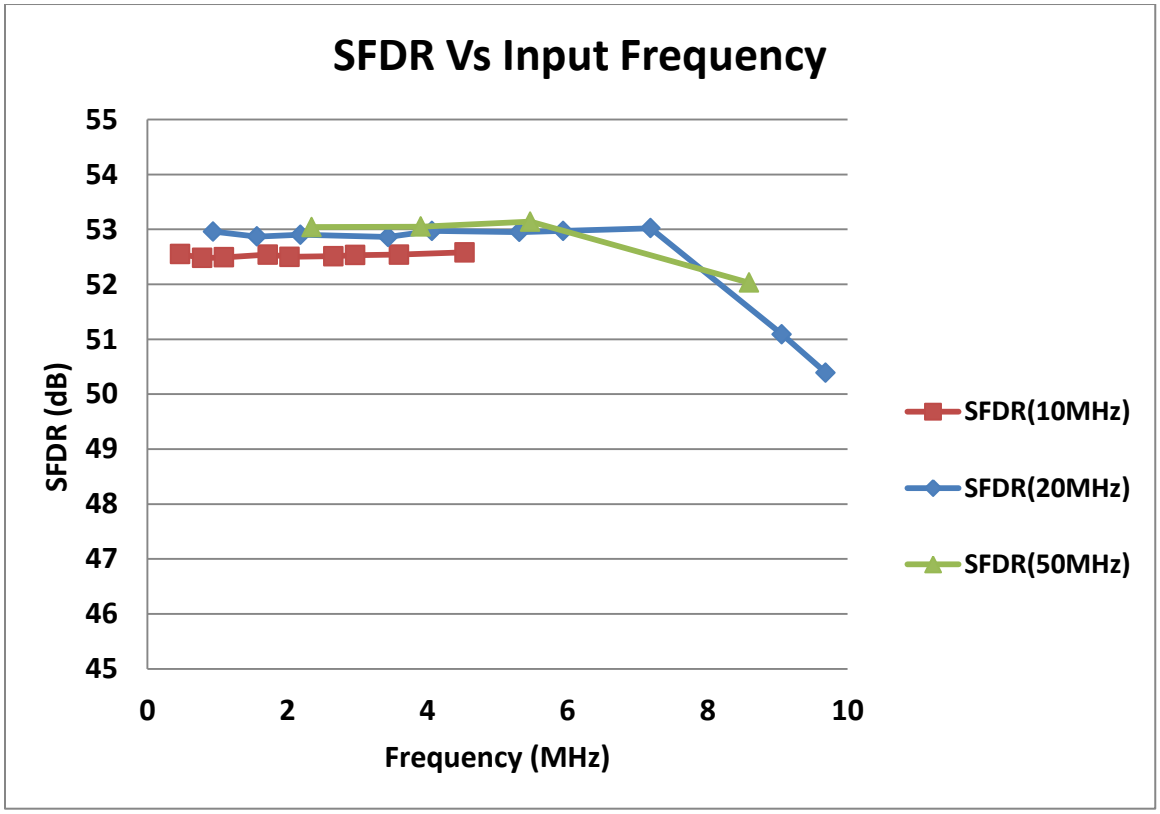

Fig. 3.10 SFDR of THA Vs Input Signal Frequency for input signal with peak-to-peak amplitude of 600mV.

It measures the lowest energy input signal that is distinguishable from the highest spur in the system. Any signal having strength below SFDR cannot be a pure signal. Fig. 3.9

shows that the output signal spectrum has SFDR of 60.36dB. Fig. 3.10 shows the variations in SFDR Vs Input signal frequency. The input signal is having the peak-to-peak amplitude of 600mV. SFDR is almost constant near low frequencies but decreases at high frequency. It means at high input signal frequency, the spur in output signal has more strength and thus the value of SFDR decreases. This trend in variation of Spurious Free Dynamic Range is followed at all the sampling frequencies. The values of SFDR Vs Input signal frequency for sampling frequencies of 10, 20 and 50 MHz are shown in graph of fig 3.10. The values of SFDR for three sampling frequencies revolved around 53dB. The maximum SFDR of 53.14dB is achieved with a sampling frequency of 50MHz.

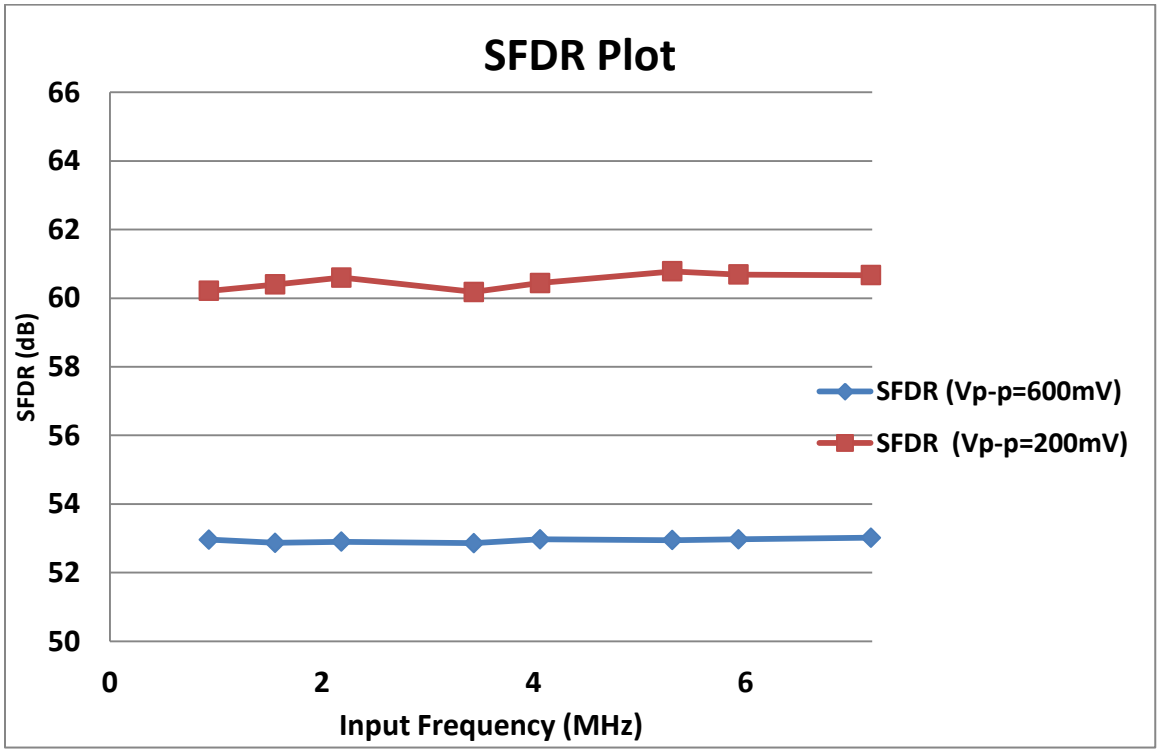

Fig. 3.11 SFDR of THA Vs Input Signal Frequency for input signal with sampling Frequency of 20MHz.

Fig. 3.11 shows the variation in SFDR for peak to peak input signal amplitude of 200mV and 600mV at sampling frequency of 20MHz. It shows that with increase in signal amplitude, SFDR decreases. It is because the non-linear effects of transistors are more at

larger signal amplitude. The maximum achieved SFDR are 60.78dB and 53dB for V_{P-P} of 200mV and 600mV respectively.

SFDR is measured at different sampling frequencies and the result is shown in fig. 3.12. The performance of circuit degrades at high sampling frequencies due to non-idealities of transistors. The clock feedthrough is an important factor that puts constraint on the operating sampling frequency of the circuit. If high bandwidth is desirable, then small hold capacitors are needed. But, noise requirements should also be considered as it constraints the minimum value of hold capacitor. Small hold capacitors lead to droop and leakage problems at high frequencies and ultimately lead to reduction in the resolution of the circuit. Due to the non-idealities of the circuit, SFDR and THD reduce with increase in sampling frequency. For a constant input signal frequency, SFDR is approximately constant for low sampling frequencies but decreases to a large extent at high sampling frequencies.

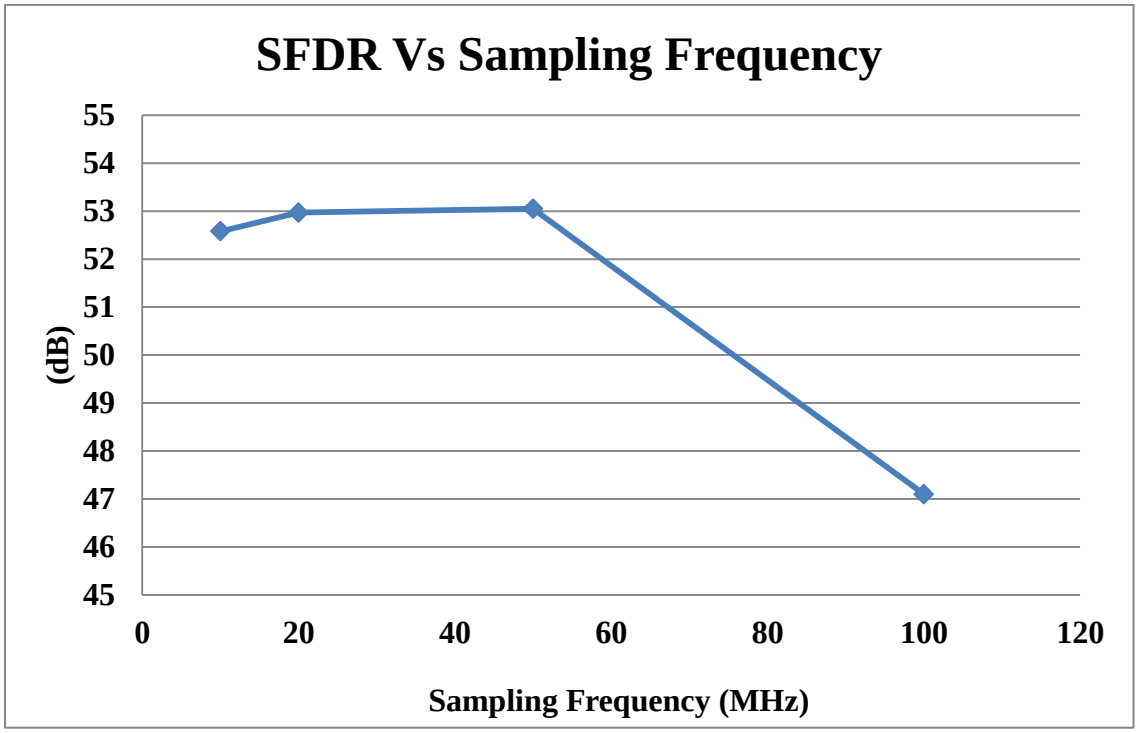

Fig. 3.12 SFDR of THA Vs Sampling Frequency for input signal with Frequency of 5MHz

SNDR: Signal to Noise and Distortion Ratio (SNDR) is calculated varying the input signal frequency. The results are shown in fig. 3.13. It shows that SNDR degrades with increase in input signal frequency and this trend is followed at each sampling frequency. Fig. 3.13 shows the results for sampling frequencies of 10, 20 and 50 MHz.

Fig. 3.14 shows the plot of SNDR vs input signal frequency for input signal amplitude of 200mV and 600mV. For V_{P-P} of 200mV, the value of SNDR is about 60dB while for amplitude of 600mV, its value lies in range of 48 to 53dB. It shows that with increase in signal amplitude, SNDR degrades. It occurs due to increase in non-idealities of transistors with increase in signal amplitude.

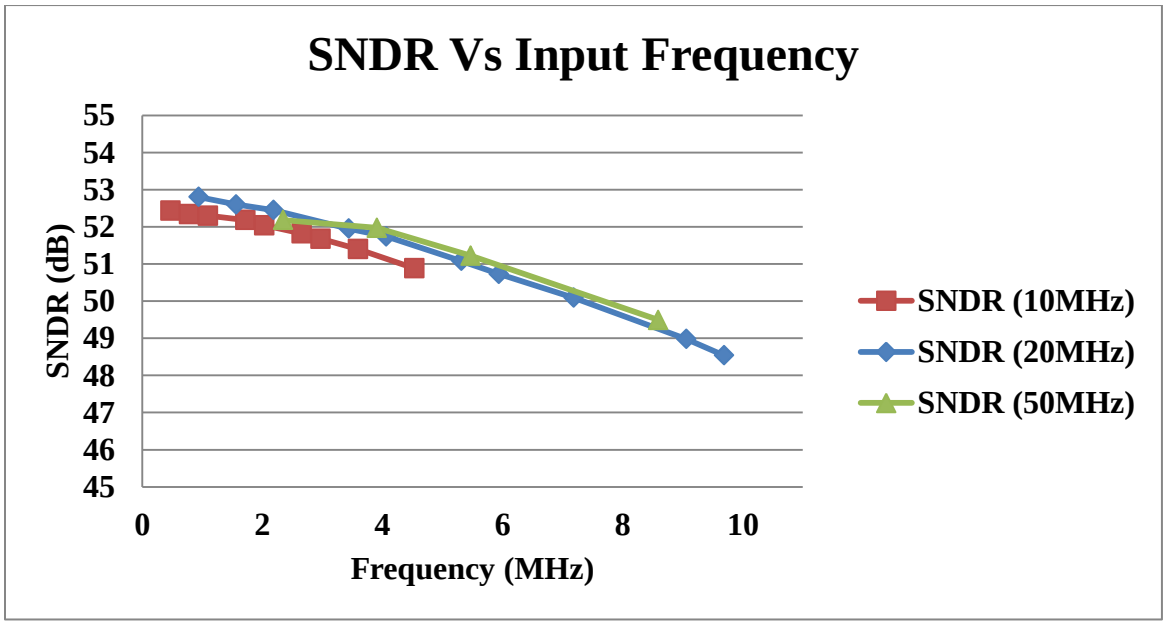

Fig. 3.13 SNDR of THA Vs Input Signal Frequency for input signal with peak-to-peak amplitude of 600mV.

Signal to Noise and Distortion Ratio is also calculated for different sampling frequencies keeping the input signal constant. The simulation and further calculations are done for an input signal with amplitude of 600mV and frequency of about 5MHz. The results are shown in fig. 3.15. The value of SNDR varies a little in low frequency range. From dc to 50MHz frequency range, SNDR is about 53dB. But for 100MHz, it degrades to a value of 40.17dB.

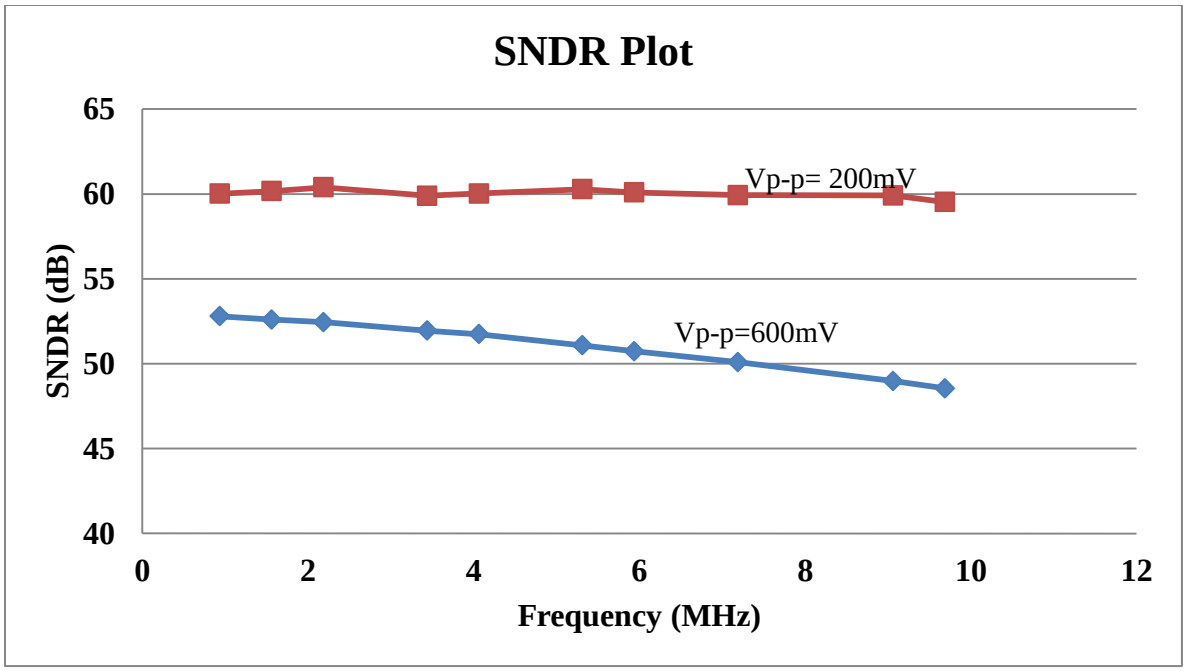

Fig. 3.14 SNDR of THA Vs Input Signal Frequency for input signal with sampling Frequency of 20MHz.

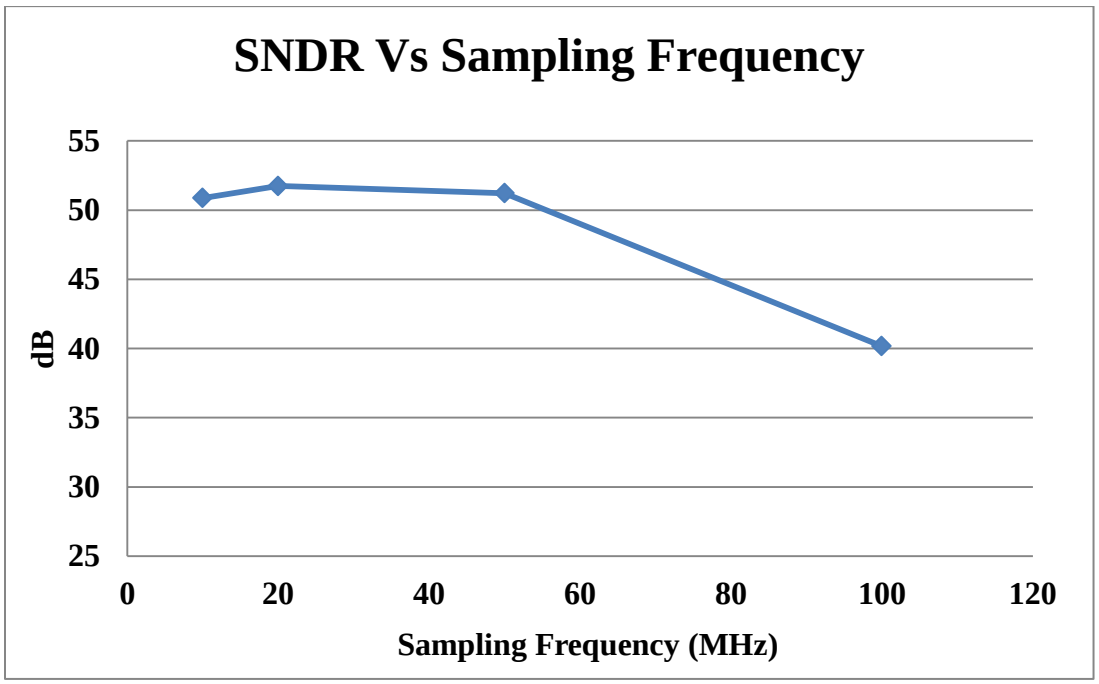

Fig. 3.15 SNDR of THA Vs Sampling Frequency for input signal with Frequency of 5MHz

Total Harmonic Distortion: Total Harmonic Distortion is calculated varying the input signal frequency. The results are shown in fig. 3.16. The input signal amplitude is having amplitude of 600mV. With increase in signal frequency, the strength of harmonics gets increase due to enhancing effect of non-idealities of circuit and thus THD decreases. This trend is followed at each sampling frequency. THD for sampling frequencies of 10, 20 and 50 MHz are shown in plot below.

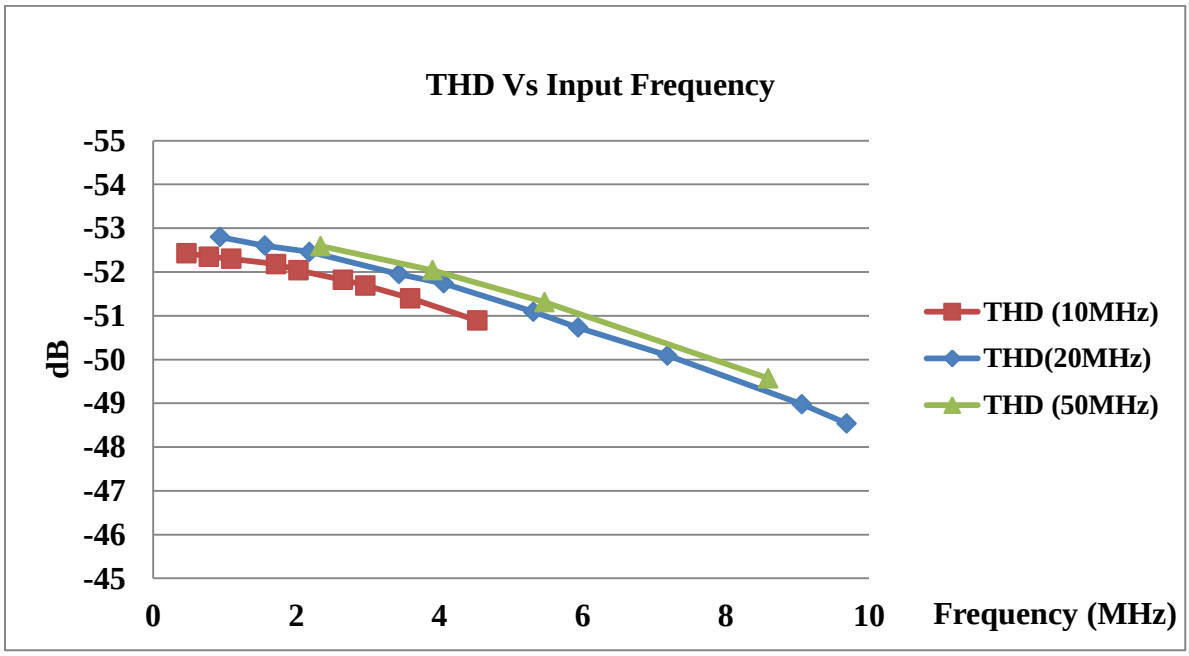

Fig. 3.16 THD of THA Vs Input Signal Frequency for input signal with peak-to-peak amplitude of 600mV.

Total Harmonic Distortion also depends on the amplitude of input signal. Fig. 3.17 shows the plot of THD vs input signal frequency for signal amplitudes of 200mV and 600mV. The sampling frequency is fixed at 20MHz. For V_{P-P} of 200mV, THD is about 60dB while for amplitude of 600mV, its value lies in range of 48.54 to 52.8dB. It shows that with increase in signal amplitude, distortions increases and hence THD reduces.

The dependency of THD on the sampling frequency is shown in fig. 3.18. The input signal with amplitude of 600mV and frequency of 5MHz is chosen for simulation and further calculations. THD value is near to –51dB up to frequency of 50MHz. At high frequency, it decreases to –49.3dB.

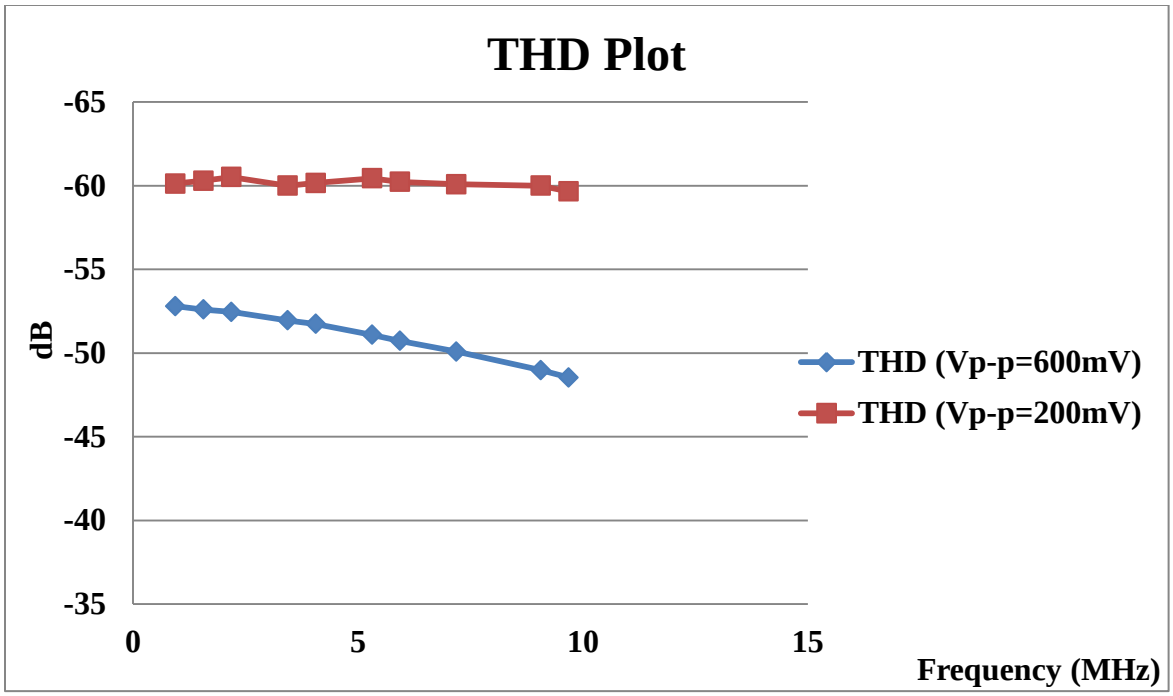

Fig. 3.17 THD of THA Vs Input Signal Frequency for input signal with sampling Frequency of 20MHz.

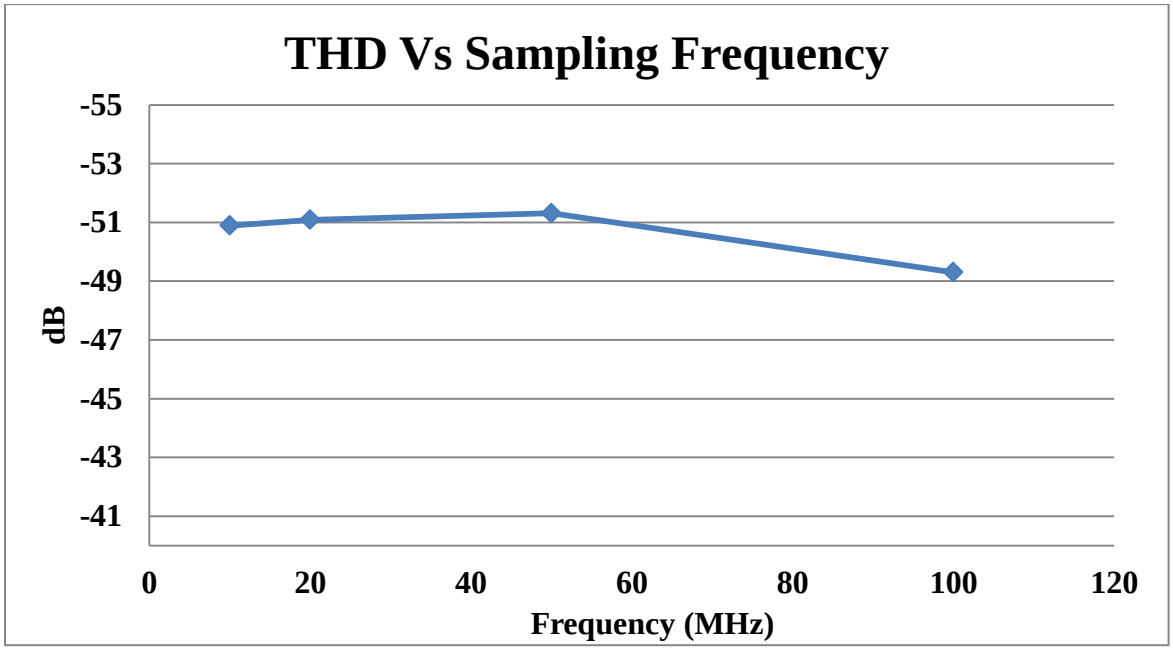

Fig. 3.18 THD of THA Vs Sampling Frequency for input signal with Frequency of 5MHz

DC Power Consumption:

Fig 3.19 shows the measured output power vs input signal frequency. The sampling frequency of THA is fixed at 20MHz for the simulation. The input signal has amplitude of 200mV. The output power is greater than –41.32dBm in frequency range of 1 to 5MHz.

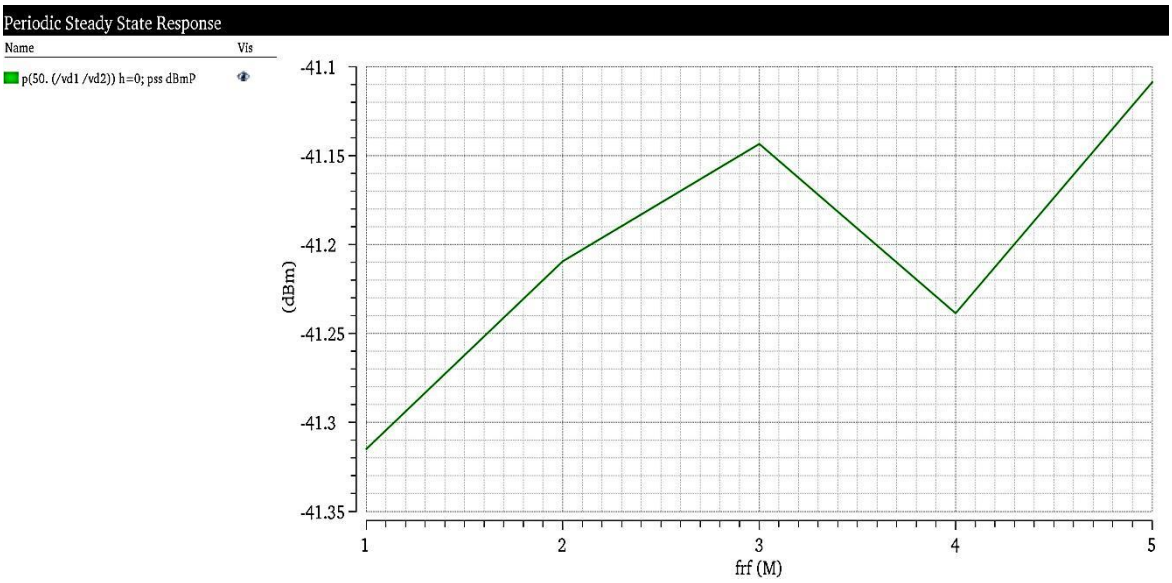

Fig. 3.19 Output Power Vs Input Signal Frequency

On-Resistance of Transmission Gate:

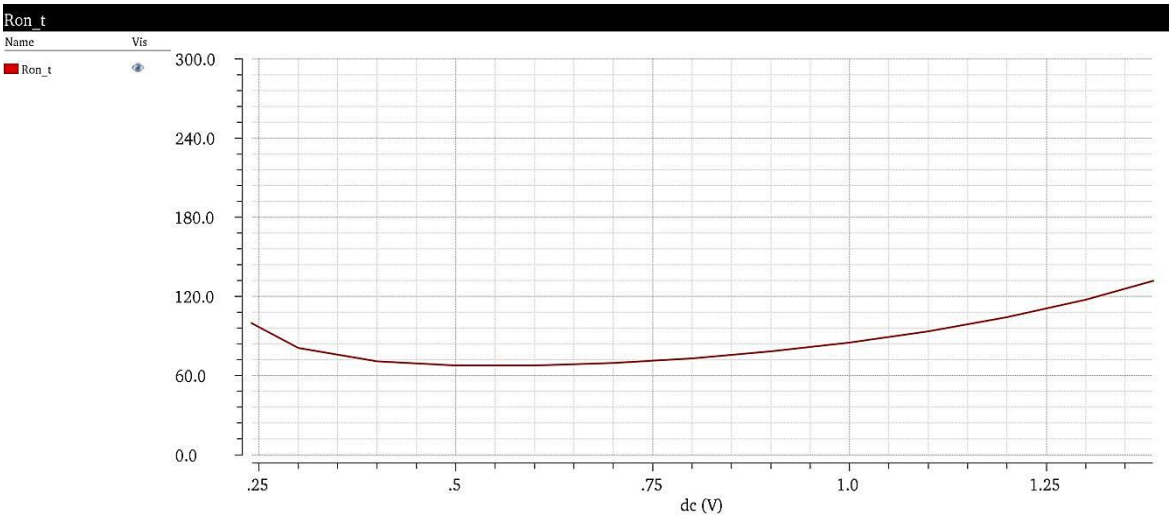

Fig. 3.20 On-Resistance of Transmission Gate in Proposed Track and Hold Circuit

The on-resistance curve of bootstrapped switch is shown in fig. 3.20. The resistance varies in the range of 60 to 130Ω when input voltage is swept. The curve is not perfectly horizontal due to the non-linearities of the transistors. But, by using the concept of bootstrapping, the non-idealities have reduced to a large extent.

The performance summary of Proposed Track and Hold Circuit is given in Table 3.3. The parameters are calculated for input signal of frequency 5.3125MHz with V_{pp} of 200mV and sampling frequency of 20MHz.

Table 3.3 Performance Parameters of T/H

Technology	180nm
Power Supply	1.8V
THD	–60.44dB
Effective Number of Bits	9.7
SNDR	60.28dB
SNR	74.69dB
SFDR	60.78dB
Maximum Sampling Frequency	100MHz
Power Consumption	< –41.1dBm
On-Resistance	60 to 130 Ω

Chapter 4

Conclusion and Future Scope

A new architecture of Low power Track and Hold Circuit has been proposed using the concept of bootstrapping. Op-amp which consumes a lot of power has not been used as a component in design which results in low power dissipation. The reduction in power supply from 2.7V as reported in [22] to 1.8V helps in saving the power. The on-resistance of switch comes in range of 60 to 130 Ω which is much less than 440 Ω reported in [22]. Apart from this, the total harmonic distortion has been reduced to a large extent. Only –60.44dB of distortion is observed at sampling frequency of 20MHz. This circuit provides the resolution of 9 bits. The proposed T/H achieves SFDR and SNDR of 60.78dB and 60.28dB respectively.

The future scope for the proposed circuit is explained as follow.

1. The current work can be extended to achieve more linear on-resistance of the switch.
2. For reducing power, this circuit can be designed in lower process technology. But, the challenges of non-idealities and short channel effects have to be faced.
3. The operation at high frequency degrades the performance of proposed T/H circuit. Hence, new technique is needed to get better THD, SNDR and SFDR.

Chapter 5

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