

# **Design of 10-Bit Dual Slope ADC for ISFET based pH Meter**

*A thesis submitted in partial fulfillment of the  
requirement for the award of degree of*

**Master of Technology  
in  
VLSI Design & CAD**

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## CERTIFICATE

This is to certify that thesis report entitled “**Design of 10-Bit Dual Slope ADC for ISFET based pH Meter**” is being submitted by **Nidhi Agrawal** in partial fulfillment of the degree of **Master of Technology in VLSI Design & CAD** of Thapar University, Patiala embodies work under my supervision at **Central Electronics Engineering Research Institute, Pilani (Rajasthan)** during the training period from January 2010 to June 2010.

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## Declaration

I hereby certify that the work which is being presented in the thesis entitled, "**Design of 10-bit Dual Slope ADC for ISFET Based pH meter**" in partial fulfillment of the requirement for the award of degree of M. Tech. (VLSI Design and CAD) at Electronics and Communication Engineering Department of Thapar University, Patiala, is an authentic record of my own work carried out under the supervision of **Mr. Anil Kumar Saini**, Scientist, IC Design Group, CEERI, Pilani and **Ms. Alpana Agarwal**, Assistant Professor, ECED, Thapar University, Patiala.

The matter presented in this thesis has not been submitted in any other University/Institute for the award of any degree.

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Nidhi Agrawal

## **ABSTRACT**

In this thesis work, a 10-bit Dual slope ADC for ISFET based pH sensor has been designed which consumes low power and have high resolution. This is implemented and simulated with Cadence tool in UMC 0.18 $\mu$ m technology with a 3.3V power supply. Different types of ADC are given in literature and they are used according to the intended application. In the biomedical field, accuracy is main concern so dual slope ADC is a best choice. Dual slope ADC is very popular due to its simplicity and higher accuracy. In this ADC there is no need of any DAC which reduces the cost of ADC.

In ISFET based pH meter, a discrete value is available to the input of ADC corresponding to the pH solution so there is no requirement of any sample and hold circuitry. This ADC has three main components: Integrator, comparator and control logic. In the ISFET based pH meter input to the integrator comes from the temperature compensation circuitry, which has upper range output so for an integrator design, an N-channel input two stage operational amplifier is taken in use because an n channel-input two stage operational amplifier have ICMR near to power supply and provide high gain. To achieve the high resolution, a cascaded comparator has been designed which enhance the resolution while keeping the ability of low power consumption. For controlling the whole operation of ADC, Melay state machine based control logic has been designed.

To display the digital output of ADC on LCD, a 3 ½ LCD display driver circuitry has been designed. This LCD display, shows the value of pH from 2 to 12.

Layouts of all the components have been designed and post layout simulation and process corner simulation has done successfully.

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## List of Abbreviations and Symbols

Symbol	Quantity	Units
$K_p$	PMOS process trans-conductance parameter	$A/V^2$
$K_n$	NMOS process trans-conductance parameter	$A/V^2$
CMRR	Common mode rejection ratio	dB
ICMR	Input common mode range	V
UGB	Unity gain bandwidth	Hz
$C_L$	Load capacitance	F
$C_C$	Compensation capacitance	F
$I_D$	Drain current	A
L	Channel length	$\mu\text{m}$
W	Channel width	$\mu\text{m}$
LVS	Layout Vs Schematic	
SR	Slew rate	$V/\mu\text{s}$
SNR	Signal-to-noise ratio	dB
$V_{DS}$	Drain source voltage	V
$V_{GS}$	Gate source voltage	V
$V_{DD}$	Positive supply	V
GND	Negative supply	V
$V_{tn}$	NMOS threshold voltage	V
$V_{tp}$	PMOS threshold voltage	V
FF	Fast-Fast	
SS	Slow-Slow	
FS	Fast-slow	
SF	Slow-Fast	
$V_{d,sat}$	Saturation voltage	V
ADC	Analog to digital convertor	

DAC	Digital to analog convertor	
$A_0$	DC open loop Gain	dB
$gm$	Trans-conductance	$\Omega^{-1}$
LSB	Least significant bit	
MSB	Most significant bit	
INL	Integral nonlinearity	
DNL	Differential nonlinearity	
N	Number of bits	
C	Binary to BCD conversion	

# Chapter 1

## Introduction

---

### 1.1 Background

Microfabricated semiconductor devices are essential components of many biochemical sensors today, and show great potential for advanced devices in the future. Ion-sensitive Field Effect Transistor (ISFET) based sensor is one of the chemical sensor which have a very fast response time, high sensitivity, micro size, robustness and the potential for on-chip circuit integration. Because of the advantages, the ISFET can be widely used in many areas especially in biomedical areas such as medical diagnostics, monitoring clinical or environmental samples and bioprocess control and testing of food products. ISFET was first introduced in 1970 by Bergveld which was used for the measurement of ion-concentration of given solution [1-6]. For the most recent of 30 years, the development of ISFET is very fast. The ISFET based pH sensor fabrication compatible with standard MOS technology.

This ISFET gives the output of milivolts range. In order to capture the response of the ISFET sensors, it is necessary for the ISFET to be accompanied by an analogue interface circuit. The basic building blocks of ISFET based pH sensor system are ISFET sensing readout circuitry, Temperature compensation circuitry and Analog to digital convertor.

There are different type of ADCs are discussed in literature which are used according to their application. Based on the speed, accuracy and power dissipation ADC are divided in to three categories: High speed ADC, medium speed, low speed ADC. Flash type ADC has maximum speed but due to use of resistors it consumes a lot of power and has less accuracy. Low speed analog to digital converters are integrating type ADC, which provide higher accuracy, low power consumption and low cost.

## 1.2 Motivation

Biomedical devices work on very low frequency, so speed is not an important factor. In these types of application main concern is on accuracy, resolution and power dissipation, therefore integrating type ADCs are very useful. There are two types of integrating ADCs reported: single slope, dual slope ADC. In single slope ADC, accuracy depends on the accuracy of resistance and capacitance. It has low noise immunity due to single slope. So to remove the dependency on resistance and capacitance, there is a need for dual slope ADC. The main advantage of the dual slope is that its conversion accuracy is independent from R, C and CLK because any one of them affects in both integration phases equally than they will eliminate the effect automatically. In this ADC, there is no need for any DAC so less hardware is needed.

The present work addresses the designing of low power and high resolution 10-bit Dual Slope analog to digital converter with 3 ½ LCD display for ISFET based pH sensor. Dual slope ADC provides higher accuracy and low power dissipation. The main components of Dual slope ADC are integrator, comparator and control logic. In this Dual slope ADC design I have chosen a four stage regenerative latch comparator due to its high resolution.

In integrating type ADC integrator plays an important role. For making this, there is a need for operational amplifier and some passive components such as resistance and capacitance. In this, two stage operational amplifier has been selected due to its high gain and low noise. Different types of comparators have been discussed in literature which is used according to the application. In this ADC a preamplifier based regenerative latch comparator has been chosen so that kick back noise will be eliminated.

The output of ISFET based pH sensor is in analog form, therefore to display ADC output on LCD, there is a need to convert it into digital form. Hence an ADC (analog to digital converter), binary to seven segment decoder and a LCD driver is used.

## 1.3 Organization of Thesis Work

Chapter 1: This chapter contains the basic idea about what is ISFET based pH meter and what is the advantage of Dual slope ADC over others. This chapter also contains the chapter wise description of report structure.

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Chapter 2: This chapter contains the description of different types of ADCs and a comparative study of different ADC is given. The architectures of different type of comparators like single clocked, double clocked and static comparators and operational amplifiers are also discussed.

Chapter 3: In this chapter, starts with the analysis of dual slope ADC, Specification and designing of N-channel two stage op-amp, regenerative latch comparator and control logic for dual slope ADC. It also describes the designing of a non-inverting integrator for dual slope ADC. At last the layouts of all the components of dual slope ADC are shown.

Chapter 4: This chapter contains the simulation results for different major architectures that have been tried for use in final architectures. Finally the results of pre layout simulation, post layout simulation and process corner simulation are also discussed.

Chapter 5: This chapter presents the designing of 3 ½ LCD driver circuitry for displaying the output of ADC on seven segment LCD display. This LCD display shows the value of pH from 2 to 12.

Chapter 6: This chapter concludes all the work which has been designed in brief and further possible improvements have been suggested.

## Chapter 2

### Literature Survey

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This chapter examines a number of various types of ADCs for speed, resolution and power dissipation and different components which are used in ADC. With the advantages of small size, rapid reaction time, high sensitivity, batch processing, small size and single chip integration Ion-Sensitive Field Effect Transistor (ISFET)-based pH sensor is increasingly being applied in biomedical field.

#### 2.1 ISFET

An ISFET was introduced by P. Bergveld in 1970 and the first reported ISFET device was using a  $\text{SiO}_2$  as a gate insulator layer [1]. The ion-selective field effective transistor (ISFET) has features of sensing the ion concentration. It can be implemented by CMOS technology. An ISFET is an ion sensitive FET which is used to measure the ion concentration in solution.

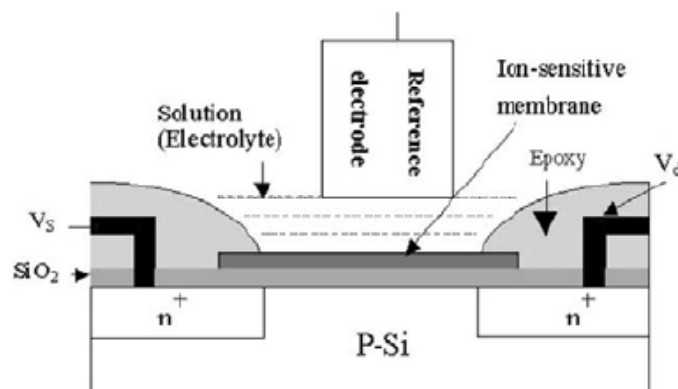


Figure 2.1: Cross section of ion sensitive field effect transistor [1].

The ISFET is similar to MOSFET device where the gate metal electrode of the MOSFET is replaced by an electrolyte, which is in contact with the reference electrode, i.e., the silicon gate oxide is directly exposed to aqueous electrolyte solution. An external reference electrode is required for a stable operation of an ISFET. The cross section view of ISFET is shown in figure 2.1.

## 2.2 Building Blocks of ISFET Based pH Meter

ISFET based pH meter consists of six major blocks, including ISFET sensing readout circuitry, Temperature compensation circuitry, Analog to digital convertor, two points calibration circuitry, LCD/LED driver and programmable bandgap reference which are shown in figure 2.2.

The ISFET readout circuit is used for reading out the pH response of ISFET [1].

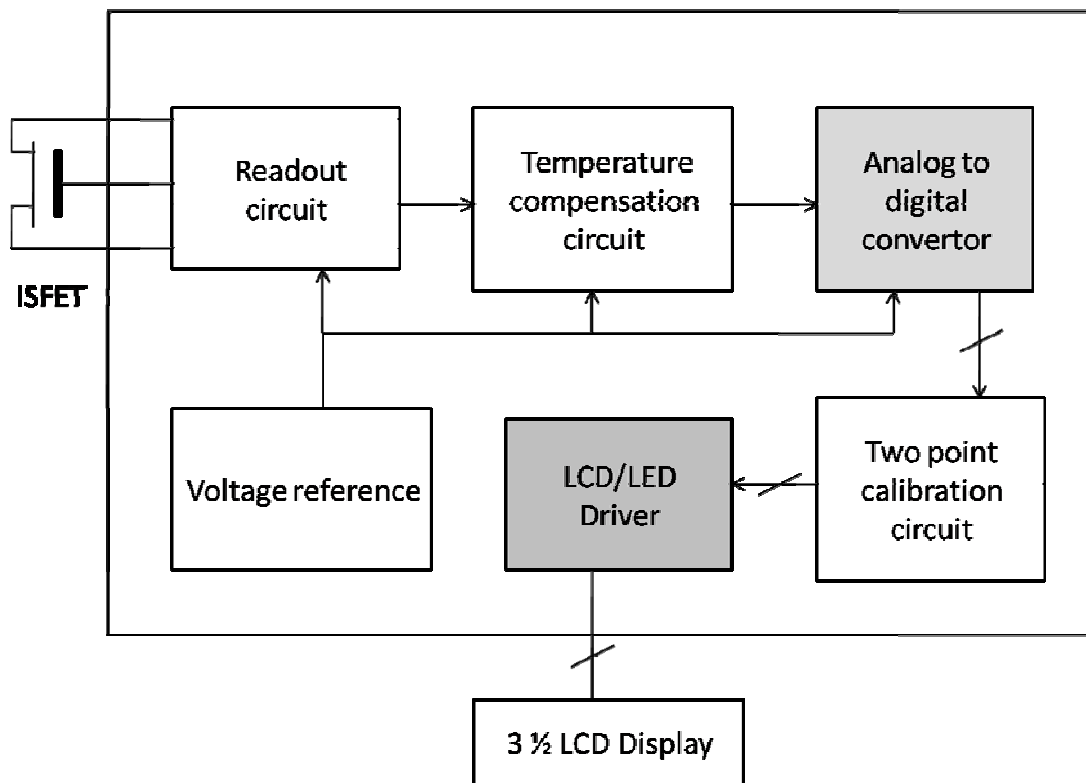


Figure 2.2: Block diagram of ISFET based pH meter [1].

It detects the ion concentration of the solution with features of Constant drain-source Voltage and Constant drain Current (CVCC) operation mode, and floating reference electrode. For the threshold voltage, MOS to be reliable temperature sensors, it has good linearity and

reproducibility, and hence can be used on temperature compensation of ISFET. This  $V_T$  extractor has positive temperature and ISFET has negative temperature coefficient. Now the outputs of both ( $V_T$  extractor & ISFET) are fed into a summing amplifier to mutually offset their temperature coefficient and to produce a temperature independent signal. In the pH sensor the output is in form of analog but everything is digitized. So there is need of analog to digital convertor (ADC).

To assure whether the measured value is correct, a two point calibration algorithm based on the standard pH4 and pH7 buffer solution is used. Finally to display the ADC output on a LCD, there is a need of LCD driver circuitry [5].

### **2.3 Need of Analog to Digital Convertors**

For most device monitoring and control applications, a computer needs to have the capability of measuring analog input voltages as well as producing analog output voltages with a DAC. Most processing equipment today are digital in nature and they work with signals which are represented as binary values. In a digital or binary representation, a signal is represented by a word, which is composed of a finite number of bits. Analog to digital convertors allow the use of sophisticated digital signal processing systems to process analog signals, which are common in the real world. Many modern electronic systems require conversion of signals from analog to digital or from digital to analog form. Circuits for performing these functions are now required in numerous common consumer devices such as digital cameras, cellular telephones, wireless data network equipment, audio devices such as MP3 players and video equipment such as Digital Video Disk (DVD) players, High definition Digital Television (HDTV) and other products. ADCs form an essential link in the signal processing pathway at the interface between the analog and digital domains [8]. Advances in ADC technology have increased the speed, lowered the cost, reduced the power requirements of ADCs and resulted in an increase in the ADC's applications.

### **2.4 Types of Analog to Digital Convertors**

There are different types of architectures available for Analog to Digital converters. These types vary in speed, power dissipation and accuracy. Among the most common ones that are commercially available are:

- Flash type ADC
- Successive Approximation Type ADC
- Digital Ramp type ADC
- Single Slope type ADC
- Dual Slope type ADC
- Sigma Delta ADC

### 2.4.1 Flash ADC

Flash ADCs, also known as parallel ADCs, are the fastest way to convert an analog signal to a digital signal but it requires much more circuitry than the other type of ADCs. The ADC flash architecture uses a set of  $2^N - 1$  comparators to directly measure an analog signal to a resolution of  $N$  bits [26].

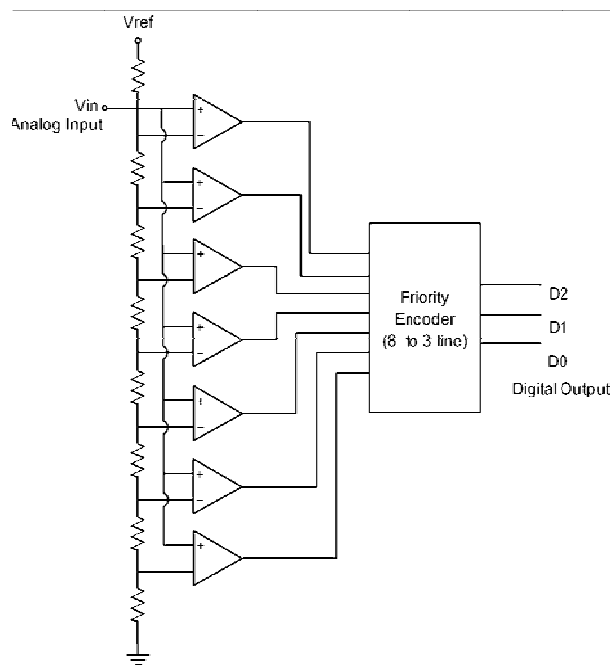


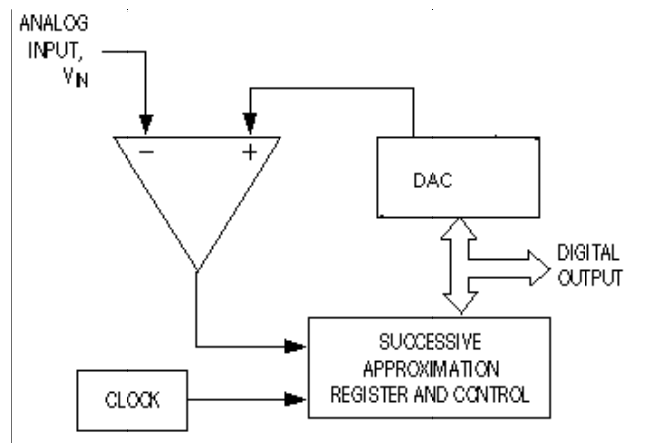
Figure 2.3: Flash ADC [6].

Figure 2.3 shows a 3-bit flash ADC, for instance, the analog input is fed into 7 comparators, each of which is biased to compare the input to a discrete transition value. The flash architecture has the advantage of being very fast, because the conversion occurs in a single ADC cycle. They are

suitable for applications requiring very large bandwidths. The disadvantage of this approach is that it requires a large number of comparators, resistors and consumes a lot of power. It has less accuracy due to use of large number of resistance. The flash ADC uses no clock signal, because no timing or sequencing is required. The conversion takes place continuously.

### 2.4.2 Successive Approximation ADC

Successive approximation register (SAR) ADC is one of the most widely used types of ADC. It has more complex circuitry than digital ramp ADC but a much shorter conversion time. SAR convertors have a fixed value of conversion time that is not dependent on the value of the analog input. The conversion technique based on a successive approximation register is shown in figure 2.4, also known as bit-weighting conversion, employs a comparator to weigh the applied input voltage against the output of an N-bit digital to analog converter (DAC). Using the DAC output as a reference, this process approaches the final result as a sum of N weighting steps, in which each step is a 1-bit conversion [6].



**Figure 2.4: Successive Approximation ADC [15].**

Initially all bits of SAR are set to 0. Then, beginning with the most significant bit, each bit is set to 1 sequentially. If the DAC output does not exceed the input signal voltage, the bit is left as a 1. Otherwise it is set back to 0. It is kind of a binary search. The processing of each bit takes one clock cycle, so that the total conversion time ( $t_c$ ) for an N-bit SAR will be N clock cycles. This ADC can be very useful when the analog input changing at a relatively fast rate.

### 2.4.3 Digital Ramp ADC

Digital ramp ADC is one of the simplest versions of ADC. It uses a binary counter as the register and allows the clock to increment the counter one step at a time until  $V_{AX} \geq V_S$ . It is called digital ramp ADC because the waveform at  $V_{AX}$  is a step-by-step ramp. It is also referred to as a counter-type ADC is shown in figure 2.5. The analog input signal is connected to the input terminal of a comparator that triggers a binary counter. The counter is connected to a DAC and the output of the DAC is connected to the other input terminal of the comparator. The output of the DAC will increase gradually as the counter is getting incremented. This process will continue until the output of the DAC exceeds the unknown analog input signal, then the comparator output will change and cause the counter to stop and its value at that moment will represent the value of the input analog voltage.

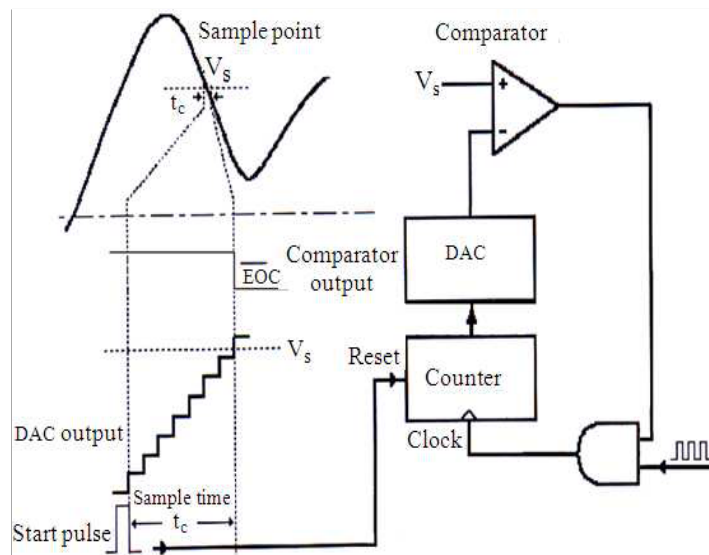


Figure 2.5: Digital ramp ADC [6].

For an  $N$ -bit ADC, maximum conversion time ( $t_c$ ) will be  $(2^N - 1)$  clock cycles. For low speed applications, however, the relative simplicity of the digital ramp ADC is an advantage over the more complex, high speed ADCs. The main disadvantage of the digital ramp ADC method is that conversion time essentially doubles for each bit that is added to the counter, so that

resolution can be improved only at the cost of a longer  $t_c$ . This makes this type of ADC unsuitable for high speed application.

#### 2.4.4 Single Slope ADC

The simplest form of an integrating ADC uses single slope architecture. Here, an unknown input voltage is integrated and the value compared against a known reference value [6]. The time it takes for the integrator to trip the comparator is proportional to the unknown voltage ( $T_{INT}/V_{IN}$ ). In this case, the known reference voltage must be stable and accurate to guarantee the accuracy of the measurement. This ADC has the advantage of simplicity of operation. The main disadvantage of single slope ADC is that its accuracy depends on the accuracy of value of R and C.

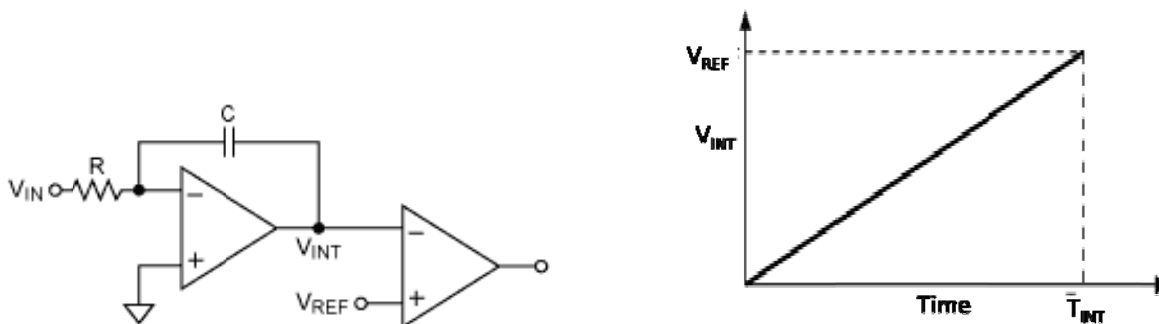


Figure 2.6: Single slope ADC [16].

#### 2.4.5 Dual Slope ADC

To overcome the accuracy problem which encountered in single slope ADC, a dual slope ADC has been designed. In this ADC, a current proportional to the input voltage, charges a capacitor for a fixed time interval  $T$  charge. At the end of this interval the device resets its counter and applies an opposite polarity (negative) reference voltage to the integrator input. With this opposite polarity, the capacitor is discharged by a constant current until the voltage at the output of the integrator reaches zero again. The time  $T$  discharge is proportional to the input voltage level and used to enable a counter. The final count provides the digital output, corresponding to the input level. The main advantage of the dual slope is that its conversion accuracy is independent from R, C and CLK of the amplifier because any one of them effect in both integration phase equally than they will eliminate the effect automatically. In this ADC, there is no need of any DAC so less hardware is needed.

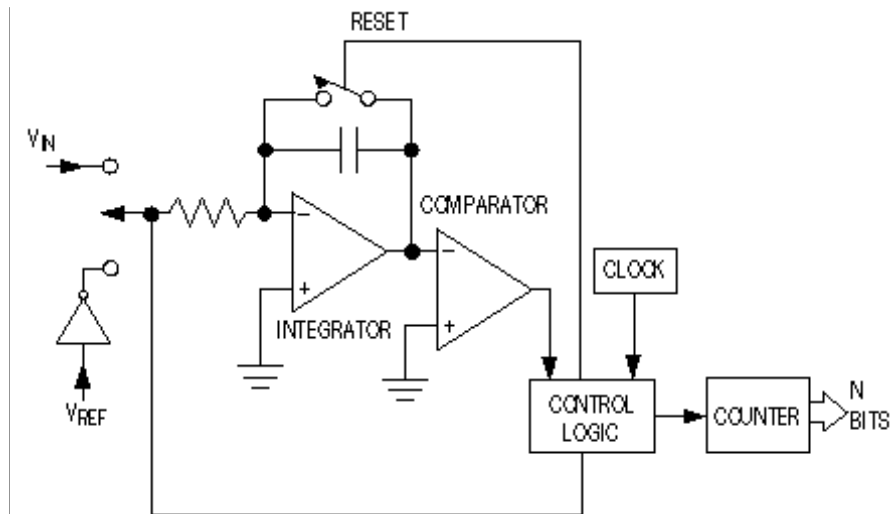


Figure 2.7(a): Dual slope ADC [16].

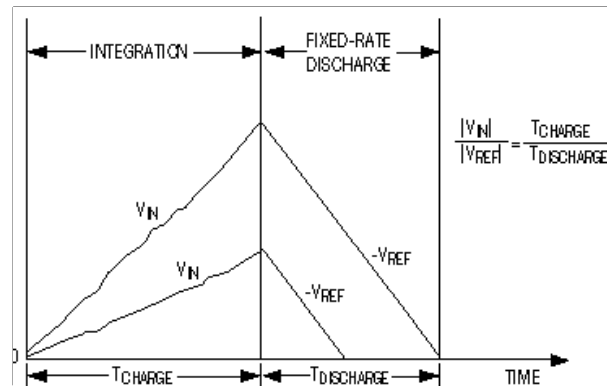
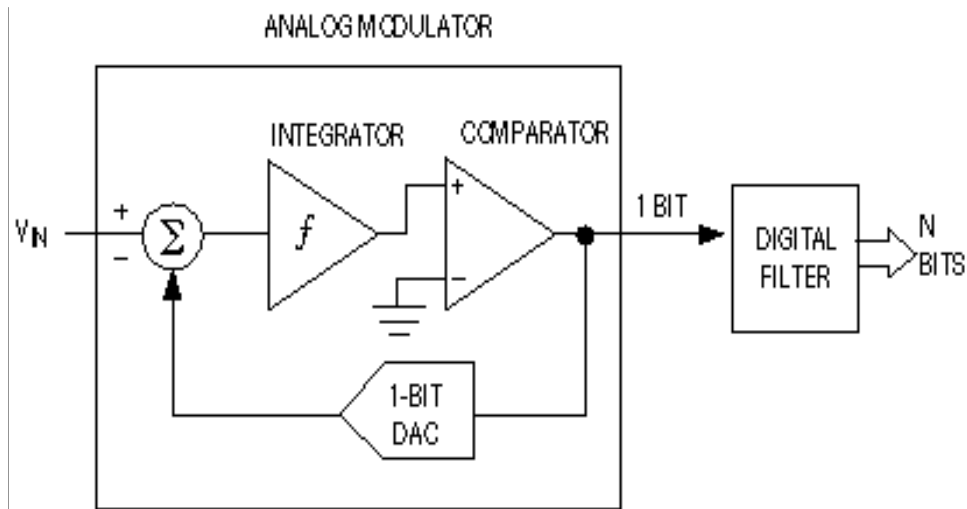


Figure 2.7(b): Waveform of the dual slope ADC [16].

### 2.4.6 Sigma Delta ADC

The Sigma Delta ADC architecture takes a fundamentally different approach from those outlined above. In its most basic form, a sigma delta converter consists of an integrator, a comparator, and a 1-bit DAC [6]. The output of the DAC is subtracted from the input signal. The resulting signal is then integrated, and the integrator output voltage is converted to a 1-bit digital output (1 or 0) by the comparator. The resulting bit becomes the input to the DAC, and the DAC's output is subtracted from the ADC input signal. This closed-loop process is carried out at a very high "over sampled" rate.



**Figure 2.8: Sigma delta ADC [15].**

The digital data coming from the ADC is a stream of ones and zeros, and the value of the signal is proportional to the density of digital ones coming from the comparator. This bit stream data is then digitally filtered and decimated to result in a binary format output. The delta sigma converters perform high-speed, low resolution (1-bit) analog to digital conversions, and then remove the resulting high-level quantization noise by passing the signal through analog and digital filters. It is used for applications with a bandwidth up to 1MHz, such as speech, audio.

## 2.5 Comparison of Different Types of ADCs

**Table 2.1 Performance of different architecture of ADCs.**

ADCs	Speed	Resolution	Power Dissipation	Accuracy
Flash	High	4 – 8	High	Low
Pipelined	Medium	8 – 16	Medium	Low
Successive approximation	Medium	8 – 16	Medium	Low
Digital ramp	Low	10 -16	Medium	Low
Single slope	Low	10 – 18	Low	Low
Dual slope	Low	10 – 18	Low	High
Sigma delta	Low	10 – 24	Low	High

## 2.6 Specifications of Converters

The specification of Converters can be categories in two parts. They are given below:

### 2.6.1 DC Specifications

Static errors, that are those errors that affect the accuracy of the converter when it is converting static (dc) signals, can be completely described by just four terms. These are offset error, gain error, integral nonlinearity and differential nonlinearity. Each can be expressed in LSB units. The DC specifications are based on the input output characteristics of ADCs. These are given below:

#### 2.6.1.1 Integral Nonlinearity

Integral Nonlinearity is the deviation of the values on the actual transfer function from a straight line. This straight line can be either a best straight line which is drawn so as to minimize these deviations or it can be a line drawn between the end points of the transfer function once the gain and offset errors have been nullified. For an ADC the deviations are measured at the transitions from one step to the next. The name integral nonlinearity derives from the fact that the summation of the differential nonlinearities from the bottom up to a particular step, determines the value of the integral nonlinearity at that step.

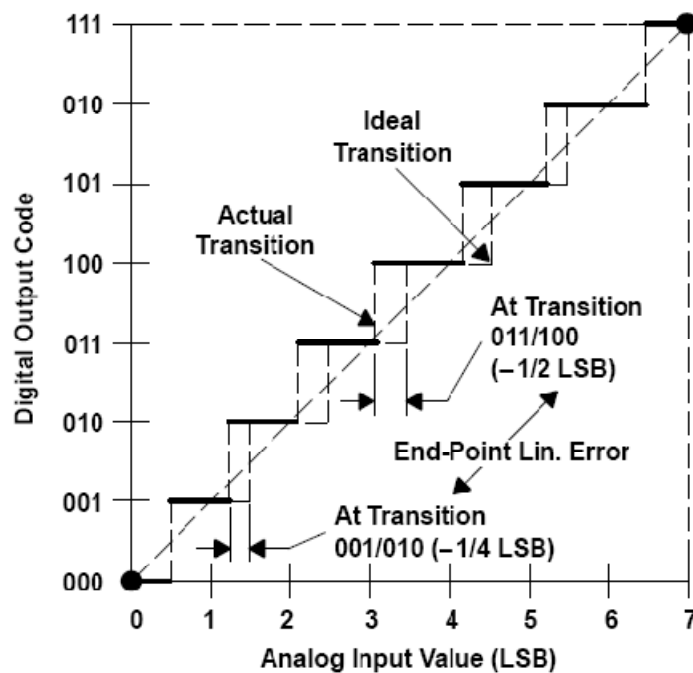


Figure 2.9: Integral nonlinearity [6].

### 2.6.1.2 Differential Nonlinearity

In an ideal converter, the code-to-code transition points are exactly 1 LSB apart. The difference between the ideal 1 LSB and the worst case actual input voltage change between output code transitions is called Differential Nonlinearity.

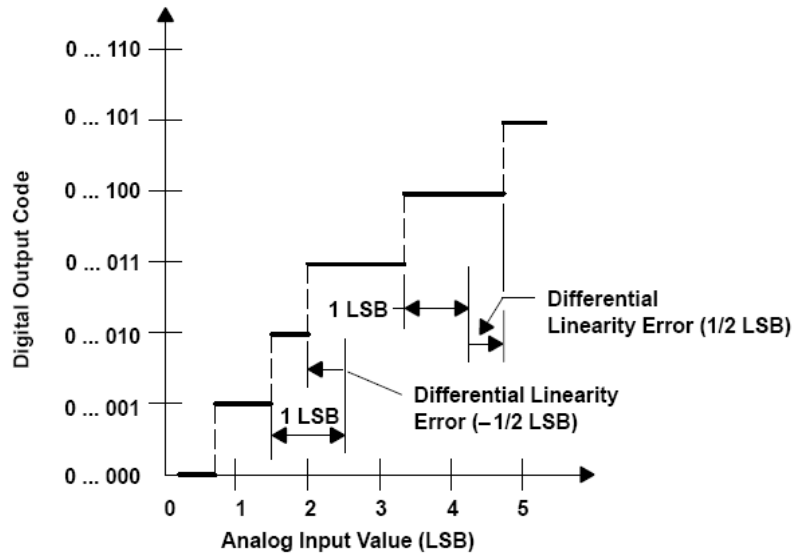


Figure 2.10: Differential Nonlinearity [6].

DNL indicates the deviation from the ideal 1 LSB step size of the analog input signal corresponding to a code-to-code increment. DNL is a static specification, relates to SNR, a dynamic specification. However, noise performance cannot be predicted from DNL performance, except to say that SNR tends to become worse as DNL departs from zero.

### 2.6.1.3 Gain Error

Gain error is a difference between the actual characteristic, and the infinite resolution characteristic, which is proportional to the magnitude of the input voltage. The Gain error can be thought of as a change in the slope of the infinite resolution line above or below a value of 1. In the input-output characteristic gain error can be measured as the horizontal difference in LSBs between actual and ideal finite resolution characteristics at highest digital code.

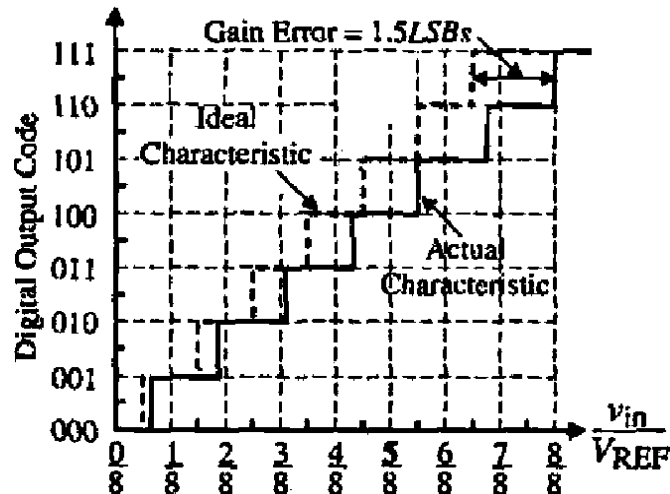


Figure 2.11: Gain error [6].

#### 2.6.1.4 Offset Error

It is the difference between actual and ideal first transition voltage. The term offset, however implies that all conversions are off by an equal amount.

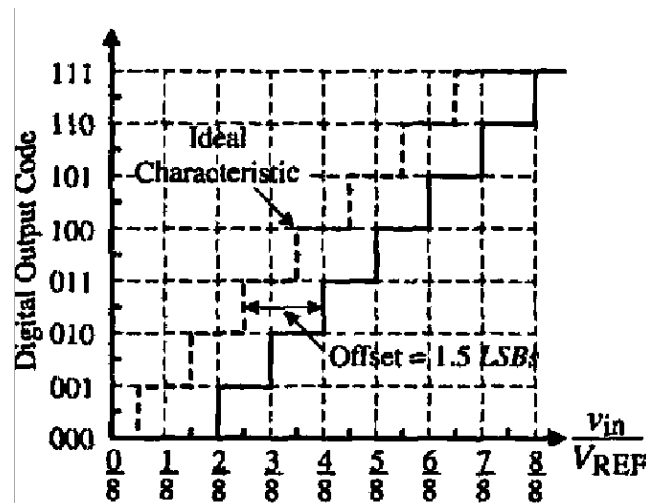


Figure 2.12: Offset error [6].

#### 2.6.1.5 Monotonicity

If the digital code of the convertor increases with increasing analog amplitude, the convertor is called monotonic. Nonmonotonicity in the ADC occurs when a vertical jump is negative. Nonmonotonicity can only be detected by DNL because output is limited to digital codes, all

jumps are integers. Normally vertical jump is 1 LSB. If the vertical jump is 2 LSB or greater, missing output code occurs. This is shown in figure 2.13.

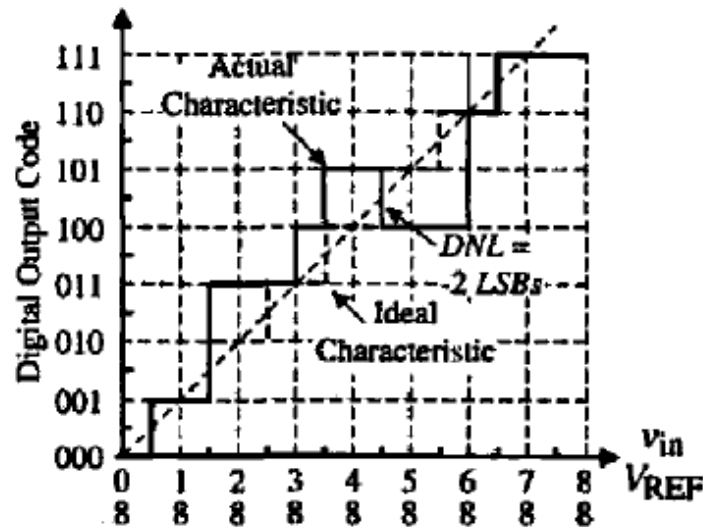


Figure 2.13: Nonmonotonicity of ADC [6].

### 2.6.1.6 Absolute Accuracy (Total) Error

The absolute accuracy or total error of an ADC is the maximum value of the difference between an analog value and the ideal mid step value. It includes offset, gain, and integral linearity errors and also the quantization error in the case of an ADC.

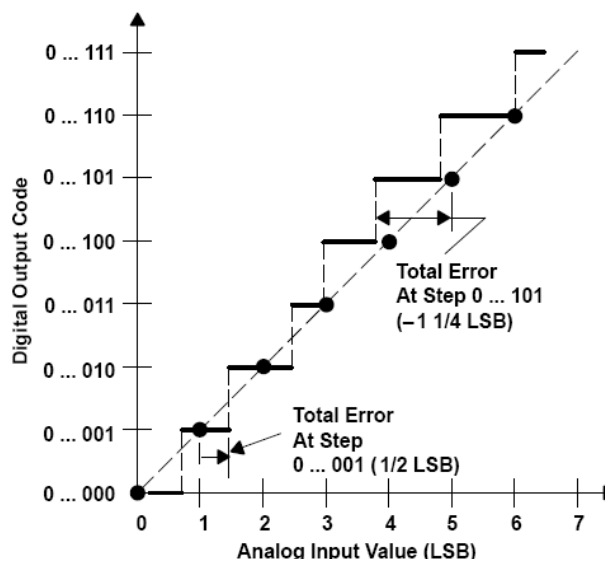


Figure 2.14: Absolute accuracy error [15].

## 2.6.2 Dynamic Specifications

The dynamic specification of converters depends mainly on parasitic capacitances and the op-amps. These specifications are given below:

### 2.6.2.1 Resolution

When an analog signal is digitized, it is represented by a finite number of discrete voltage levels. The resolution of ADC is the smallest analog change that can be distinguished by an ADC. To more accurately replicate the analog signal, the resolution must be increased [6]. Resolution may be expressed in percent of full scale but it typically given in number of bits  $N$ , where the convertor has  $2^N$  possible output states. Using converters with higher resolutions will reduce the quantization error.

### 2.6.2.2 Signal to Noise Ratio

Signal to Noise Ratio (SNR) is the ratio of the output signal amplitude to the output noise level, not including harmonics or dc. SNR usually degrades as frequency increases because the accuracy of the comparator(s) within the ADC degrades at higher input slew rates [15]. This loss of accuracy shows up as noise at the ADC output. In an ADC, noise comes from four sources: (1) quantization noise, (2) noise generated by the converter itself, (3) application circuit noise and (4) jitter.

Quantization noise results from the quantization process, the process of assigning an output code to a range of input values. The amplitude of the quantization noise decreases as resolution increases because the size of an LSB is smaller at higher resolutions, which reduces the maximum quantization error. The theoretical maximum signal to noise ratio for an ADC with a full scale sine wave input derives from quantization noise and is defined as  $6.02N + 1.76$  dB. Where  $N$  is the number of bits. Application circuit noise is that noise seen by the converter as a result of the way the circuit is designed and laid out.

SNR is increased by 6-dB by increasing 1-bit in ADC. SNR performance decreases at higher frequencies because the effects of jitter get worse.

## 2.7 Comparator

The comparator is the basic component mainly used in Analog to Digital Converters. The electrical function of a comparator is to generate an output voltage with value high or low

depending on whether the sign of the input is positive or negative. We can have two different types of input: voltage or current. In the case of voltage, the input voltage is measured with respect to a given reference level. Therefore, the comparator determines whether the amplitude of the input is higher or not than a reference [17]. When the current is the input variable the comparator determines whether the input current is flowing in or out of the input terminal.

In various types of analog to digital conversion, the most important part in the circuit is comparator. The comparator is a circuit that compares an analog signal with another analog signal or reference and outputs a binary signal based on the comparison.

The Comparator is widely used in the process of converting analog signals to digital signals. In analog to digital conversion process, it is first necessary to sample the input. This sampled signal is then applied to a combination of comparators to determine the digital equivalent of the analog signal. In its simplest form comparator can be considered as a 1-bit analog to digital converter. Comparators can be divided into open loop and regenerative comparators. The open loop comparators are basically op-amps without compensation. Regenerative comparators use positive feedback, similar to flip-flops, to accomplish the comparison of the magnitude between two signals. A third type of comparator that emerges is a combination of open loop and regenerative comparators. This combination results in comparators that are extremely fast. Successive stages and a latch take care of further signal amplification.

## 2.8 Characteristics of Comparator

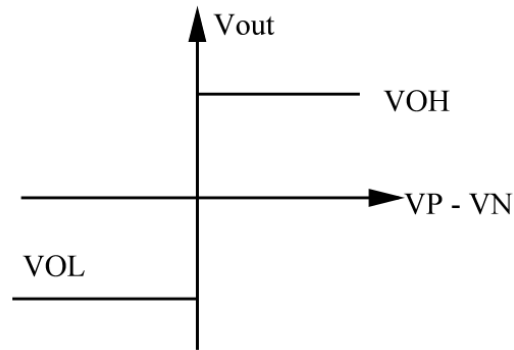
We shall characterize the comparator by following aspect:

- Resolving capability
- Input offset voltage
- Input common mode range
- Speed or propagation time delay
- Power consumption

A comparator was defined as a circuit that has a binary output whose value is based on a comparison of two analog inputs. As shown in the Figure 2.15, the output of the comparator is high ( $V_{OH}$ ) when the difference between the non-inverting and inverting inputs is positive, and low ( $V_{OL}$ ) when this difference is negative. The ideal aspect of the model is the way in which the

output makes a transition between  $V_{OL}$  and  $V_{OH}$ . The output changes state for an input change of  $\Delta V$ , where  $\Delta V$  approaches zero. This implies a gain of infinity, as shown

$$Gain = A_v = \lim_{\Delta V \rightarrow 0} \frac{V_{OH} - V_{OL}}{\Delta V}$$

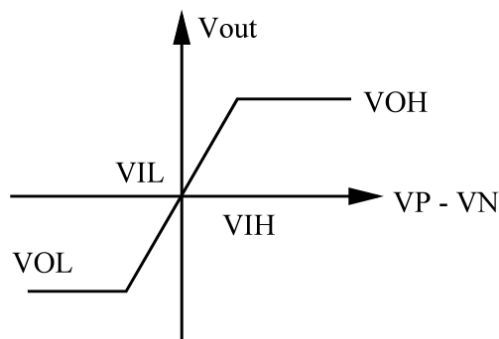


**Figure 2.15: Ideal transfer curve [6].**

Practically, as shown in the Figure 2.16 we have

$$Gain = A_v = \frac{V_{OH} - V_{OL}}{V_{IH} - V_{IL}}$$

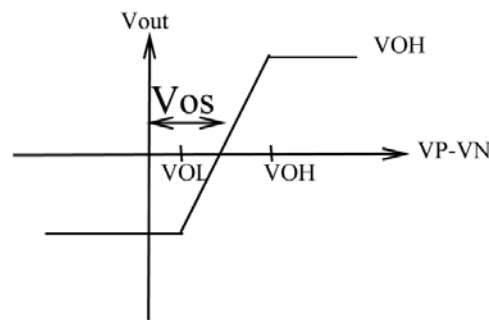
Where  $V_{IH}$  and  $V_{IL}$  represent the input-voltage difference  $VP-VN$  needed to just saturate the output at its upper and lower limit, respectively. This input change is called the resolution of the comparator. Describing comparator operation, for it defines the minimum amount of input change (resolution) necessary to make the output swing between the binary states.



**Figure 2.16: Transfer curve of a comparator with finite gain [6].**

The second non-ideal effect seen in comparator is input offset voltage in Figure 2.17, the output changes as the input difference crosses zero [6]. If the output did not change until the input difference reached a value  $V_{OS}$ , then this difference would be defined as the offset voltage. We can also say that it is the voltage that must be applied to the input to obtain the crossing point between low and high logic level.

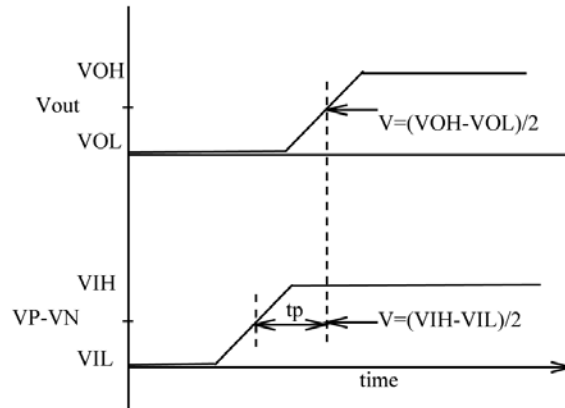
The input to the comparator is usually differential, the input common mode range is also important. The ICMR for a comparator would be that range of input common mode voltage over which the comparator functions normally [6].



**Figure 2.17: Transfer curve of a comparator including input offset voltage [6].**

The characteristic delay between input excitation and output transition is the time response of the comparator. Figure 2.18 shows the response of a comparator to an input as a function of a time. As we can see there is a delay between the input excitation and output response [6]. This time difference is called the Propagation delay time of the comparator. It is very important parameter since it is often the speed limitation in the conversion rate of an ADC. The propagation delay time in comparator generally varies as a function of the amplitude of the input. A larger input will result in a smaller delay time. There is an upper limit at which a further increase in the input voltage will no longer affect the delay. This mode of operation is called slewing or slew rate. If the propagation delay time is determined by the slew rate of the comparator, then this time can be given by

$$t_p = \Delta T = \frac{\Delta V}{SR} = \frac{V_{OH} - V_{OL}}{2 * SR}$$



**Figure 2.18: Propagation delay time of a non-inverting comparator [6].**

In the case where the propagation delay time determined by the slew rate, the most important factor to decrease the propagation time is increasing the sinking or sourcing capability of the comparator.

Power Consumption is the power consumed by comparator. Moreover, the power consumed depends upon the speed specifications. Due to portability and to remove the cooling circuitry, low power operation is a very important quality factor. Therefore a key design task is to achieve the minimum power consumption for a given required speed.

## 2.9 Analog Comparator Architectures

There are different type of analog comparators are given in literature. They are discussed below:

### 2.9.1 Two Stage Open Loop Comparator

As we can see from the previous requirements for a comparator reveal that it requires a differential input and sufficient gain to able to achieve the desired resolution [6]. The operational amplifier can be used as a comparator. Here a two stage CMOS op-amp used as a comparator which is shown in figure 2.19. A simplification occurs because the comparator will generally be used in open loop mode and eliminated the need of compensation capacitor which will be used for designing a high gain two stage op-amp topology. It is preferred so that it has largest bandwidth possible, which will give a faster response.

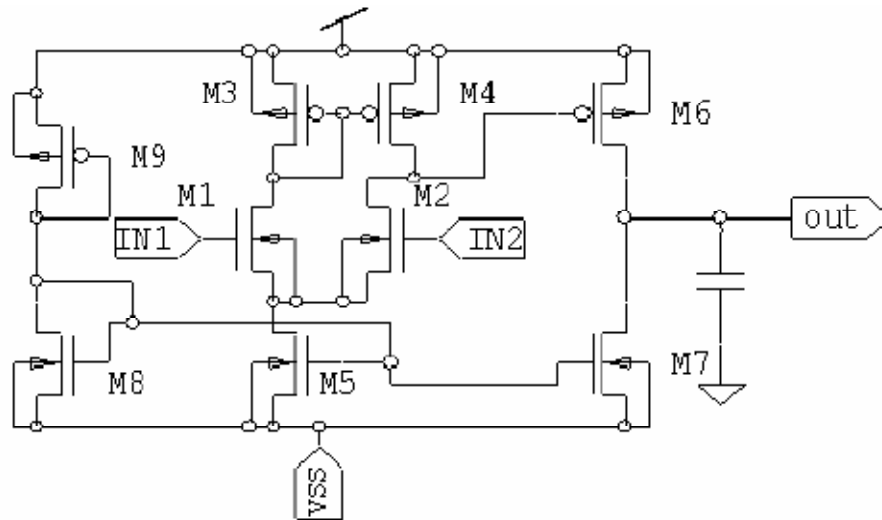


Figure 2.19: Two stage open loop comparator [6].

## 2.9.2 Comparator with Regenerative Positive Feedback

There are mainly two types of regenerative positive feedback comparators:

### 2.9.2.1 Non-clocked Comparator with Regenerative Positive Feedback

In this type of comparator, there is no need of any clock. This comparator consists of three stages which are shown in figure 2.20.

- The input preamplifier
- Feedback or decision stage
- Output buffer.

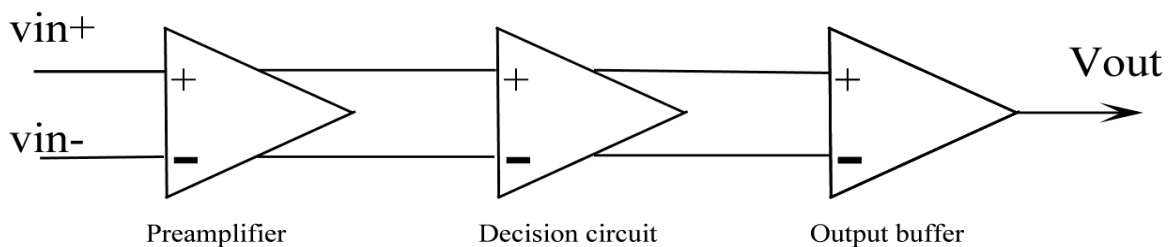


Figure 2.20: Block diagram of a voltage comparator [17].

**Input Preamplifier:** The preamplifier stage (or stages) amplifies the input signal to improve the comparator sensitivity (i.e., increase the minimum input signal which the comparator make a decision) and isolate the input of the comparator to switching noise coming from the positive

feedback stage. In this design trans-conductance sets the gain of the stage, while the input capacitance of the comparator is determined by the size of input transistors. Here the channel length of MOSFETs is taken large (Channel length modulation gives rise to an unwanted offset voltage).

Positive Feedback or decision stage: The decision circuit is the important part of the comparator and should be capable of discriminating mV levels signals. The positive feedback stage is used to determine which of the input signals is larger. The circuit uses positive feedback from the cross gate connection of transistors, to increase the gain as well as speed of the decision circuit.

Output buffer: The final component of comparator is the output buffer or post-amplifier. The main purpose of the output buffer is to convert the output of the decision circuit into a logical signal (i.e. 0 or 3.3V). The output buffer should accept a differential input signal and provide a single ended output. An inverter is added on the output of the amplifier as an additional gain stage and to isolate any load capacitance from the differential to single ended amplifier.

### **2.9.2.2 Clocked Comparator with Regenerative Positive Feedback**

In all type of analog to digital convertors, comparator is an important building block. In ADC most of the power is consumed by comparator, so there is a need to reduce the power consumption of comparator. The design of comparator depends on the intended application. In many low power applications, the comparator is not needed to be always on because sometimes ADCs are not required to operate at their maximum speed. In such cases the comparator is idle for most of the time. To reduce the power consumption the comparator can be switched off for a specific period of time in a clock period. There are two types of clocked comparators: Single clock, double clock comparator.

#### **2.9.2.2.1 Single Clock Comparator**

These types of comparators uses only single clock. There are different types of single clock comparators are given in literature. They use the clock in a different way to reduce the power dissipation.

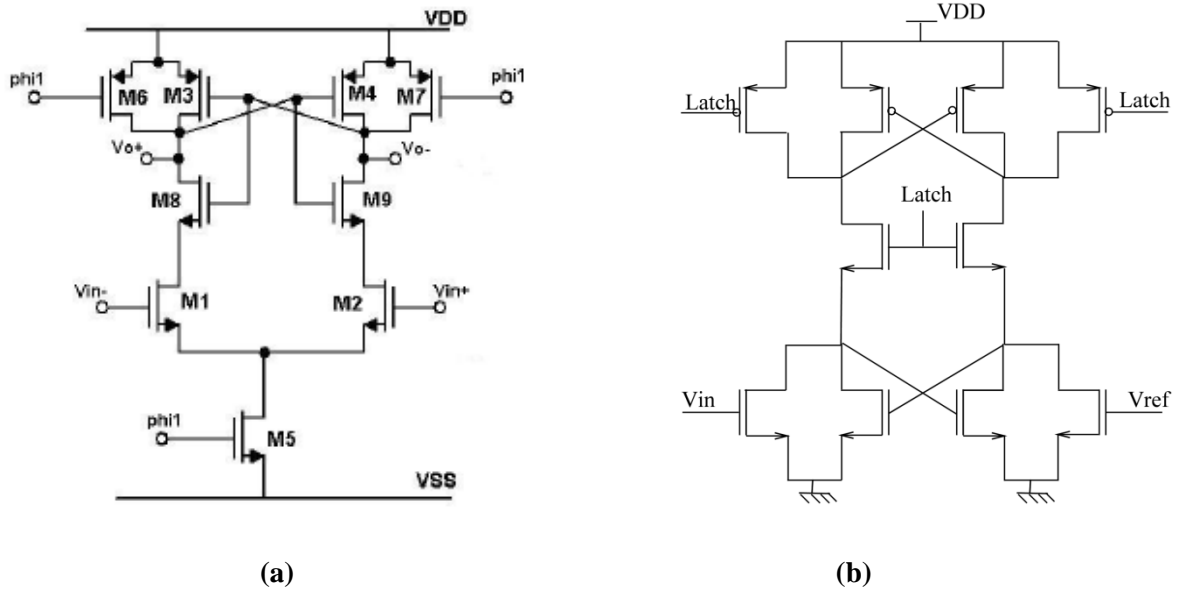


Figure 2.21: Single clock comparators [10].

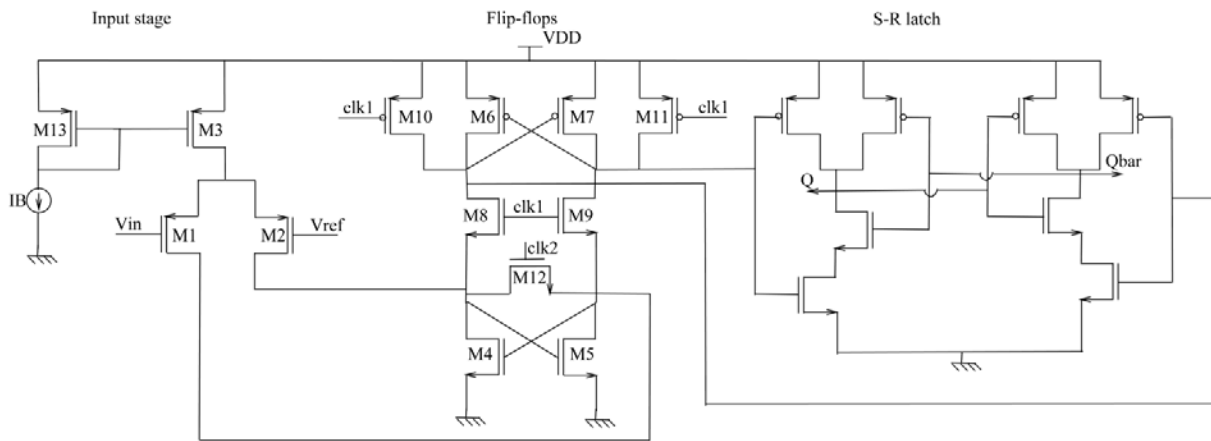
Figure 2.21 shows different types of single clock comparators. In figure 2.21 (a), The track-and latch comparator is composed by an NMOS input differential pair M1-M2, inverters M3,M4,M6,M7 and M4-M9 in positive feedback configuration, pre-charge transistors M6-M7, and by the current source controlled ( $phi1$ ) M5. In the pre-charge phase when  $phi1$  is low, the current of M5 ( $I_{tail}$ ) is turned off and the input drivers are reset [10]. The outputs  $V_{o+}$  and  $V_{o-}$  are pre-charged to  $V_{DD}$ . At the rising edge of the clock  $phi1$ , the evaluation phase, the pre-charge transistors are open and the differential pair is activated, initiating the comparison. It has the advantage of low stand-by dissipation, since it shuts down current consumption after the semi cycle. But this structure has low resolution due to single stage.

Figure 2.21(b) shows the different structure. It consumes less power due to transistor M3a and M3b and has high speed due to double regenerative feedback. But this structure has limited ICMR due to cascading and its resolution is also low because of single stage.

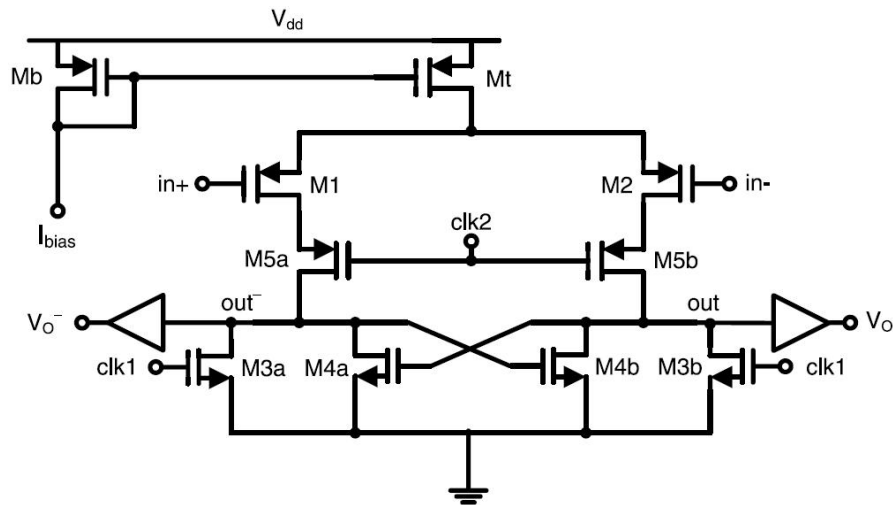
### 2.9.2.2.2 Double Clock Comparator

Figure 2.22(a) shows a two clock comparator. It consists of a differential input pair (M1, M2), a CMOS latch circuit, and an S-R latch. The CMOS latch is composed of a n-channel flip-flop (M4, M5) with a pair of N-channel transfer gates (M8, M9) for reducing direct path dissipation and an N-channel switch (M12) for resetting, and a P-channel flip-flop (M6, M7) with a pair of

P-channel precharge transistors (M10, M11). clk1 and clk2 are the two non-overlapping clocks [7].



(a)



(b)

Figure 2.22: Double clock comparators [3, 7].

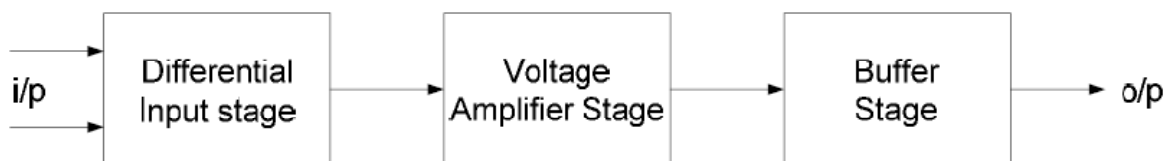
The dynamic operation of this circuit is divided into a reset time interval and a regeneration time interval. In this comparator during evaluation phase transistor M8 and M9 turns on and clock clk1 has similar on and off time, so there is large power dissipation. Figure 2.22(b) shows another type of double clock comparator. This comparator has limited ICMR due to cascade

stage and provides less resolution capability because of single stage [3]. When power dissipation is main concern then this type of comparator is very useful.

## 2.10 Operational Amplifiers

Operational amplifiers (op-amps) are the most versatile and an integral part of many analog and mixed signal systems. General purpose op-amps can be used as buffer, summers, integrators, differentiators, comparators and many other applications. Its performance makes significant impact on the analog systems. It is a fundamental building block for many circuit designs that utilize its high gain, high input impedance and low output impedance. The operational amplifier can be used in two basic configurations: inverting and non-inverting. Basically, there are two choices for the output stages differential or single which are used according to intended application.

Classic op-amp architecture is made up of three stages as shown in Figure 2.23, even though it is referred to as a “two-stage” op-amp, ignoring the buffer stage (third stage). The first stage usually consists of a high gain differential amplifier [18]. This stage has the most dominant pole of the system. A common source amplifier usually meets the specification of second stage, having a moderate gain. The third stage is most commonly implemented as a unity gain source follower with a high frequency and negligible pole.



**Figure 2.23: Typical two-stage op-amp [18].**

Typical op-amp circuits contain many poles. For this reason, op-amp must usually be compensated, that is their open-loop transfer function must be modified such that the closed-loop circuit is stable and the time response is well-behaved. For this, we use different frequency compensation techniques. Frequency compensation is a technique used in amplifiers and especially in amplifiers employing negative feedback. It usually has two primary goals: To avoid unintentional creation of positive feedback and to control overshoot and ringing in the amplifier's step response. In general, stability can be achieved by:

- (1) Minimizing the overall phase shift, thus pushing the phase crossover out.
- (2) Dropping the gain, thereby pushing the gain crossover in.

In a stable system, the gain crossover must occur well before the phase crossover. The first approach requires that the number of poles in the signal path must be minimized by proper design. Since each additional stage contributes at least one pole, this means the number of stages must be minimized, which yields low gain and / or limited output swings [16]. The second approach retains the low frequency gain and the output swings but it reduces the bandwidth by forcing the gain to fall at lower frequencies. If the resultant circuit is still suffers from insufficient phase margin, we then compensate the op-amp.

In an amplifier, if the load capacitance have moderate value, the output pole, will be the closest to the origin, called the “dominant pole”, sets the open-loop 3-dB bandwidth. We must force the loop gain to drop such that the gain crossover point moves toward the origin. For this we simply lower the frequency of the dominant pole by increasing the load capacitance. From the magnitude plots after the compensation, we note that the unity gain bandwidth is equal to the frequency of the first non-dominant pole (the closest pole to the origin after the dominant pole). This indicates that to achieve a wideband in a feedback system employing an op-amp, the first non-dominant pole must be as far as possible. The slew rate is also depends on the unity gain frequency.

## 2.11 General Issues in Designing of Operational Amplifier

Negative feedback is used widely in application in processing of analog signal. Let us consider the negative feedback system shown in Figure 2.24, the closed loop transfer function as:

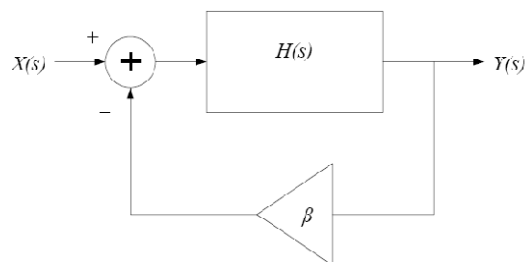


Figure 2.24: Basic negative feedback system [18].

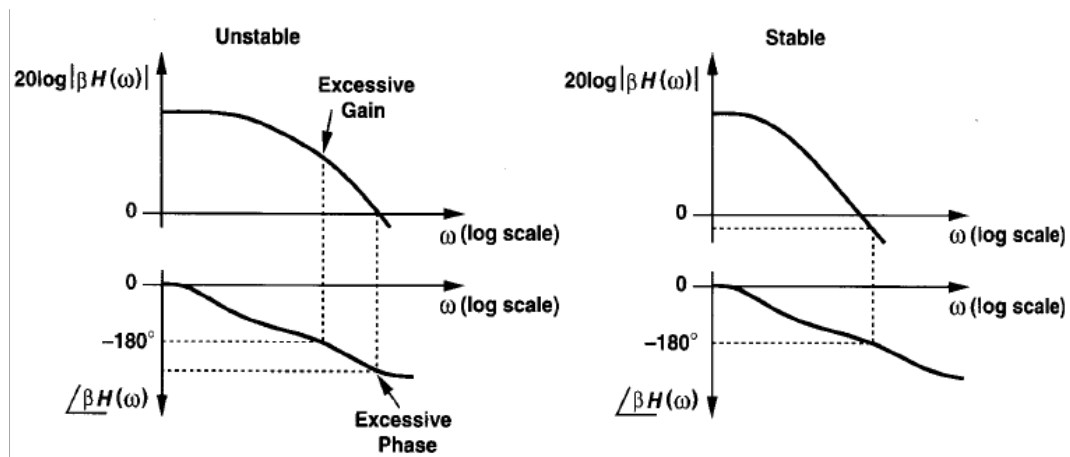
$$\frac{Y}{X}(S) = \frac{H(S)}{1 + \beta H(S)}$$

If  $\beta H(s = j\omega l) = -1$ , the gain goes to infinity, and the circuit can amplify its own noise and may oscillate at frequency  $\omega l$ . This condition can be expressed as:

$$|\beta H(j\omega l)| = 1$$

$$\angle \beta H(j\omega l) = -180^\circ$$

Which is known as “Barkhausen’s Criteria” ( $\beta$  is assumed constant, less than or equal unity and independent of frequency). As negative feedback it introduces  $180^\circ$  of phase shift, and the capacitance within amplifier’s gain stages cause the output signal to lag behind the input signal by  $90^\circ$  for each pole they create. If the sum of these phase lags reaches  $360^\circ$  and gain is sufficient, the feedback signal will be add in phase to the original noise to allow oscillation buildup. The conditions can be summarize as excessive loop gain at frequency for which the phase shift reaches  $-180^\circ$  or, excessive phase at frequency for which the loop gain drops to unity. So to avoid instability we must have  $\beta H$  more positive than  $-180^\circ$  for  $|\beta H| = 1$ .



**Figure 2.25: Bode plots example of loop gain for unstable and stable systems [16].**

In a stable system, the gain crossover point must occur well before the phase cross over point. If  $\beta$  is reduced (less feedback is applied), then the magnitude plots of Figure 2.25 are shifted down, thereby moving the gain cross over closer to the origin and making the feedback system more stable. For the worst case stability ( $\beta = 1$ ), we often analyze the magnitude and phase plots for

$\beta H = H$ .

There are different issues which should have keep in mind before designing of any op-amp.

These are as follows:

- Gain
- Phase margin
- Gain bandwidth
- Input common mode range (ICMR)
- Common mode rejection ratio (CMRR)
- Power supply rejection ratio (PSRR)
- Output swing
- Output resistance
- Offset voltage
- Settling time

Gain: The key function of the op-amp is to generate at the output an amplified replica of the voltage across the input terminals. The ratio of output (voltage or current) to input (voltage or current) is called gain. Ideally, the voltage gain is infinite.

Phase margin: When different stages of op-amp are connected together, the op-amp generally has poor performance and unstable in the unity feedback configuration. Stability is decided by Phase margin. The phase of  $\beta H$  at the gain crossover frequency can serve as a measure of stability: the smaller  $|\beta H|$  at this point, the more stable the system.

Phase margin (PM), defined as:

$$PM = 180^\circ + \angle \beta H(\omega = \omega_1)$$

Where  $\omega_1$  is the gain crossover frequency.

Gain bandwidth: The range of frequencies within which the open-loop voltage amplification is greater than unity. The amplitude bode diagram will display a  $20 \text{ dB/decade}$  roll-off until the gain reaches  $0 \text{ dB}$ . The frequency at which the gain becomes  $0 \text{ dB}$  is called unity gain frequency, with a constant roll-off  $20 \text{ dB/decade}$  of the achieved unity gain frequency equal the product of gain and bandwidth. Therefore, is also named the gain bandwidth product,  $GBW$ .

Common mode rejection ratio: Ideally op-amp has infinite gain if the input voltage difference is zero. Practically, due to noise and other factors, the input difference is not zero. CMRR is the ratio between the differential gain and the common mode gain. A high *CMRR* is a merit factor for any op-amp.

Power supply rejection ratio (*PSRR*): If we apply a small signal in series with the positive or the negative power supply we obtain a corresponding signal at the output with a given amplification ( $A_{PS+}$  or  $A_{PS-}$ ). The ratio between the differential gain and the power supply gain leads to two *PSRRs*. These are two merit factors showing the ability of the op-amp to reject drive signals coming from the power supply. Having a good *PSRR* is an important merit factor. Unfortunately, especially at high frequencies, the *PSRR* achieved is typically quite poor. A typical value of *PSRR* is  $60\text{ dB}$  at low frequencies that decreases to  $20 - 40\text{ dB}$  at high frequencies.

Input common mode range: This is the voltage range that we can use at the input terminal without producing a significant degradation in op-amp performance. Since the typical input stage of an op-amp is a differential pair, the voltage required for the proper operation of the current source and the input transistors limit the input swing. A large input common mode range is important when the op-amp is used in the unity gain configuration. In this case the input must follow the output.

Offset voltage: If the differential input voltage of an ideal op-amp is zero the output voltage is also zero. This is not true in real circuits: various reasons determine some unbalancement due to mismatches, in turn, lead to a non-zero output. In order to bring the output to zero, it is therefore required to apply a proper voltage at the input terminals. Such a voltage is called offset voltage.

Output swing: This is maximum swing of the output node without producing a significant degradation of op-amp performance. Since we have to leave some room for the operation of the devices connected between the output node and the supply nodes, the output swing is only a fraction of  $(V_{DD}-V_{SS})$ . Typically it ranges between  $60\%$  and  $80\%$  of  $(V_{DD}-V_{SS})$ . Within the output swing range the response of the op-amp should match to given specifications and in particular the harmonic distortion should remain below the required level.

Settling time: The time needed for the output of the op-amp to reach a tolerance band is called settling time. Ideally this should be zero.

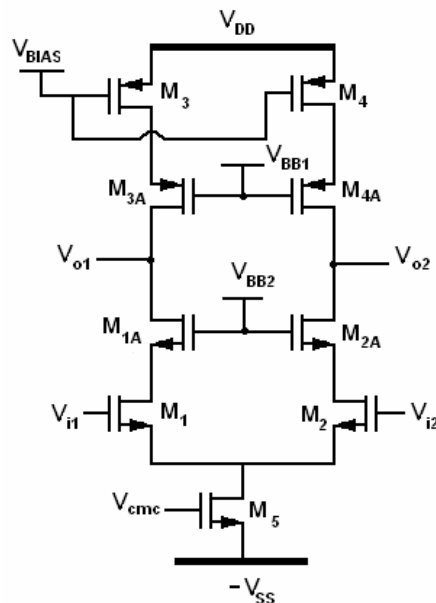
## 2.12 Comparison of Op-amps:

**Table 2.2 Performance of different op-amp topologies [18].**

Op-amp	Gain	Output Swing	Speed	Power Dissipation	Noise
Telescopic	Medium	Medium	Highest	Low	Low
Folded-Cascode	Medium	Medium	High	Medium	Medium
Two-Stage	High	Highest	Low	Medium	Low
Gain-Boosted	High	Medium	Medium	High	Medium

### 2.12.1 Telescopic Op-amp

Cascode configurations may be used to increase the voltage gain of CMOS transistor amplifier stages. This structure has been called a ‘telescopic-cascode’ op-amp because the cascodes are connected between the power supplies in series with the transistors in the differential pair, resulting in a structure in which the transistors in each branch are connected along a straight line. The main potential advantage of telescopic cascode op-amps is that they can be designed so that the signal variations are entirely handled by the fastest-polarity transistors in a given process. In addition to the poor common mode input range calculated another disadvantage of the telescopic-cascode configuration is that the output swing is small.



**Figure 2.26: Fully differential telescopic op-amp [18].**

### 2.12.2 Folded Cascode Operational Amplifier

The name “folded cascode” comes from folding down P-channel cascode active loads of a differential pair and changing the MOSFET’s to N-channels. This op-amp uses cascading in the output stage combined with the differential amplifier to achieve good input common mode range. Thus, the folded cascode op-amp provides self-compensation, good input common mode range, high power supply rejection ratio, and the gain of two stage op-amp. An N-channel folded cascode op-amp is shown in figure 2.27.

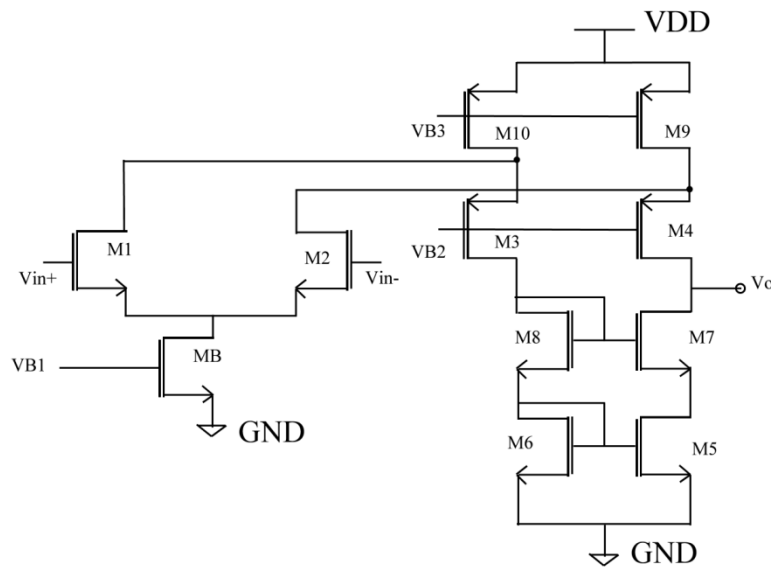


Figure 2.27: N-channel folded cascode op-amp [6].

The main disadvantage of the folded cascode is that it consumes more power as compare to telescopic op-amp.

### 2.12.3 Two stage Operational Amplifiers

A typical CMOS differential amplifier stage is shown in Figure 2.28. Differential amplifiers are often desired as the first stage with high gain and second stage which provide maximum swing. The first stage generally a differential stage but the second stage is typically design as a simple common source stage so it allows maximum output swing. A two stage op-amp consumes low power as compare to folded cascode but provide same ICMR.

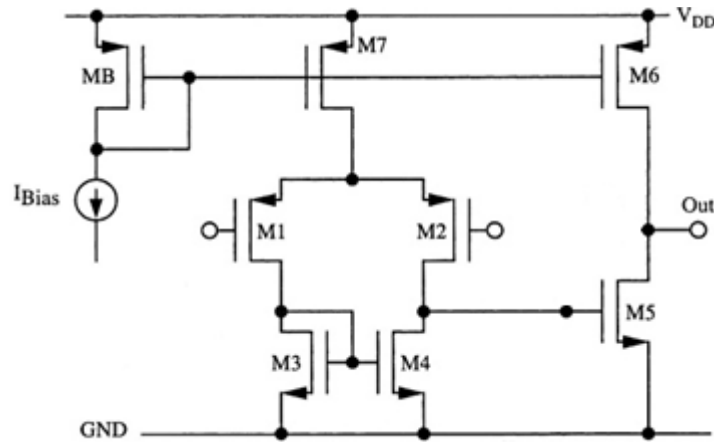


Figure 2.28: Two stage op-amp [16].

### 2.13 Frequency Compensation

The single stage amplifier typically has good frequency response and could achieve a phase margin of 90 degree. However, the dc gain of the single amplifier is generally not high enough and is even less for submicron CMOS transistors. In general, op-amps require at least two gain stages. As a result, op-amp circuits have multiple poles. The poles contribute to the negative phase shift and may cause phase angle  $-180^\circ$ , before the unity gain frequency. The circuit will oscillate due to the negative phase margin. It leads to the necessity of altering the amplifier circuit to increase the phase margin and stabilize the closed loop circuit. This process is called ‘compensation’.

The frequency response of the multistage amplifier is not as good as that of the single stage and this amplifier has a higher probability of oscillation in feedback circuits. One popular way to predict the closed loop stability is by measuring the phase margin (PM) of the open loop gain response. PM must be greater than 0 degree for no oscillation to occur [6]. A good performing amplifier will need a PM of about  $45^\circ$  to  $60^\circ$ . Otherwise, the amplifier may exhibit ringing in the time domain and peaking in the frequency domain.

There are different types of compensation techniques, which are used with operational amplifiers.

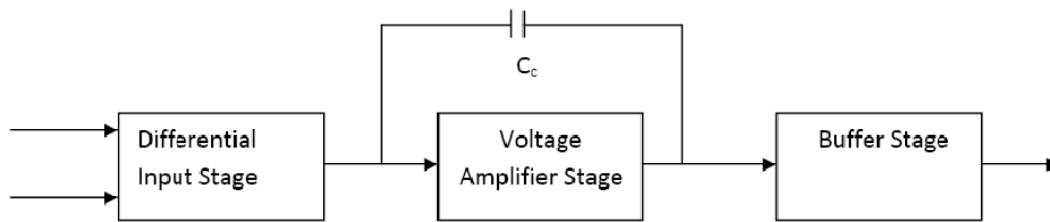
#### 2.13.1: Parallel compensation

Parallel compensation is a classical way to compensate the op-amp. A capacitor is connected in parallel to the output resistance of the gain stage of the amplifier to modify the pole. It is not

generally used in the integrated circuits due to large capacitance value required to compensate the op-amp which costs considerable large die area.

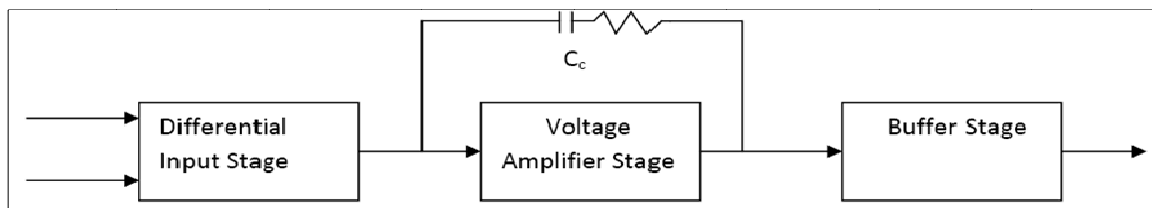
### 2.13.2 Pole Splitting-Single Miller Compensation (SMC)

After designing each stage and connecting them together, an op-amp commonly is unstable in the unity feedback system. Using the measurement technique described, methods to compensate the op-amp can be employed. For a two-stage op-amp Single Capacitor Miller Compensation (SCMC), which significantly reduces the frequency of dominant pole and moves the output pole away from the origin (this effect is called “pole splitting”), is a common technique in op-amp design. In this method, a capacitor,  $C_c$ , is connected in parallel with the second stage, as shown in Figure 2.29.



**Figure 2.29: Implementation of pole-splitting (Miller Compensation) [6].**

Figure 2.29 shows standard SMC topology. As the transistor gain of the second stages increases, the dominant pole decreases and the non-dominant pole increases. In this way the two poles are being split apart and stabilize the feedback amplifiers by greatly narrowing the bandwidth [6]. The simple pole splitting method also introduces a right half plane zero which causes negative phase shift; as a result, the stability is made a little poorer. The zero comes from the direct feed through of the input to the output through the Miller capacitor. To eliminate the RHP zero due to the feed through and increase the phase margin of the op-amp, lead compensation which adds a nulling resistor in series with the compensation capacitor (SMCNR) to increase the impedance of the feed through path is shown in figure 2.30.



**Figure 2.30: Addition of  $R_z$  in series with compensation capacitor [6].**

The effect of the nulling resistor to the position of the poles as well as that of the zero and pointed out the pole splitting would break down if the resistor becomes too large. When the resistor gets very large, there is no pole splitting since the compensation capacitor is actually open circuit.

## Chapter 3

### Design of Dual Slope Analog to Digital Convertor

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In chapter 2 the operating principle and block level circuit configuration of an ISFET based pH meter were discussed. Efficient acquisition of biomedical signals requires proper integration of several low noise, high accuracy and low power analog and digital components. Bio-signals being of the order of few millivolts are severely influenced by noise. Dual slope ADCs are well known for their excellent noise rejection, high accuracies and lower circuit complexities. In this chapter, a high resolution and low power Dual slope ADC for ISFET based pH meter will be designed with 0.18 $\mu$ m UMC technology. This design aims to become the measurement of pH and other biomedical applications where portability and accuracy are main concern.

#### 3.1 Dual Slope ADC

To overcome the problem of accuracy due to dependency on R and C, dual slope has been designed. Dual slope ADC has several advantages over the single slope ADC. The final conversion result is insensitive to errors in the component values that is, any error introduced by a component value during the integrate cycle will be cancelled out during the de-integrate phase. The main components of the dual slope ADC are integrator, comparator, control logic, counter and register.

##### 3.1.1 Operation of the Dual Slope ADC

A dual slope analog to digital convertor which was implemented in this thesis work is described here. The main components of the dual slope ADC are integrator, comparator, multiplexer, control logic, counter and register. Initially when the operation starts, counter is in reset phase and reset\_control signal generated by control logic is also high.

The conversion process starts by switching the start signal at high and switch SW has high logic. In this duration integrator connects to the  $V_{in}$  (input voltage of ADC), capacitor begin to charge and counter will starts to count. This is called input integration state. It is seen that the slope of the voltage at integrator output ( $V_{int}$ ) is proportional to the amplitude of  $V_{in}$ . The voltage  $V_{int}$  (T1) at  $t=T1$  is given by equation (1):

$$V_{int}(T1) = \int_0^{T1} V_{in} dt = T1V_{in} + VT \quad (1)$$

When this counter reaches full scale (hence, for a precise fixed interval T1), the input to the integrator is switched to the reference  $V_{ref}$ . This state is defined as reference integration state. In this period T2, capacitor begins to discharge and counter again starts to count. When the output of the integrator is equal to the  $VT$  (reference voltage of the comparator) then counter will be stopped and a done signal will generates by the control logic. The output of the counter is stored in a register using done signal. The integrator voltage at T1+T2 is obtained by equation (2):

$$V_{int}(T1 + T2) = V_{int}(T1) + \left( - \int_{T1}^{T1+T2} (V_{ref}) dt \right) = VT$$

$$V_{int}(T1 + T2) = V_{int}(T1) - V_{ref}(T2) = VT \quad (2)$$

Using equation (1) and (2) we get

$$T1V_{in} + VT - (T2V_{ref}) = VT$$

$$\frac{T1}{T2} = \frac{V_{ref}}{V_{in}} \quad (3)$$

Where,

$V_{in}$  = Input voltage of dual slope ADC.

$V_{out}$  = Output voltage of integrator.

$VT$  = Reference voltage of the comparator.

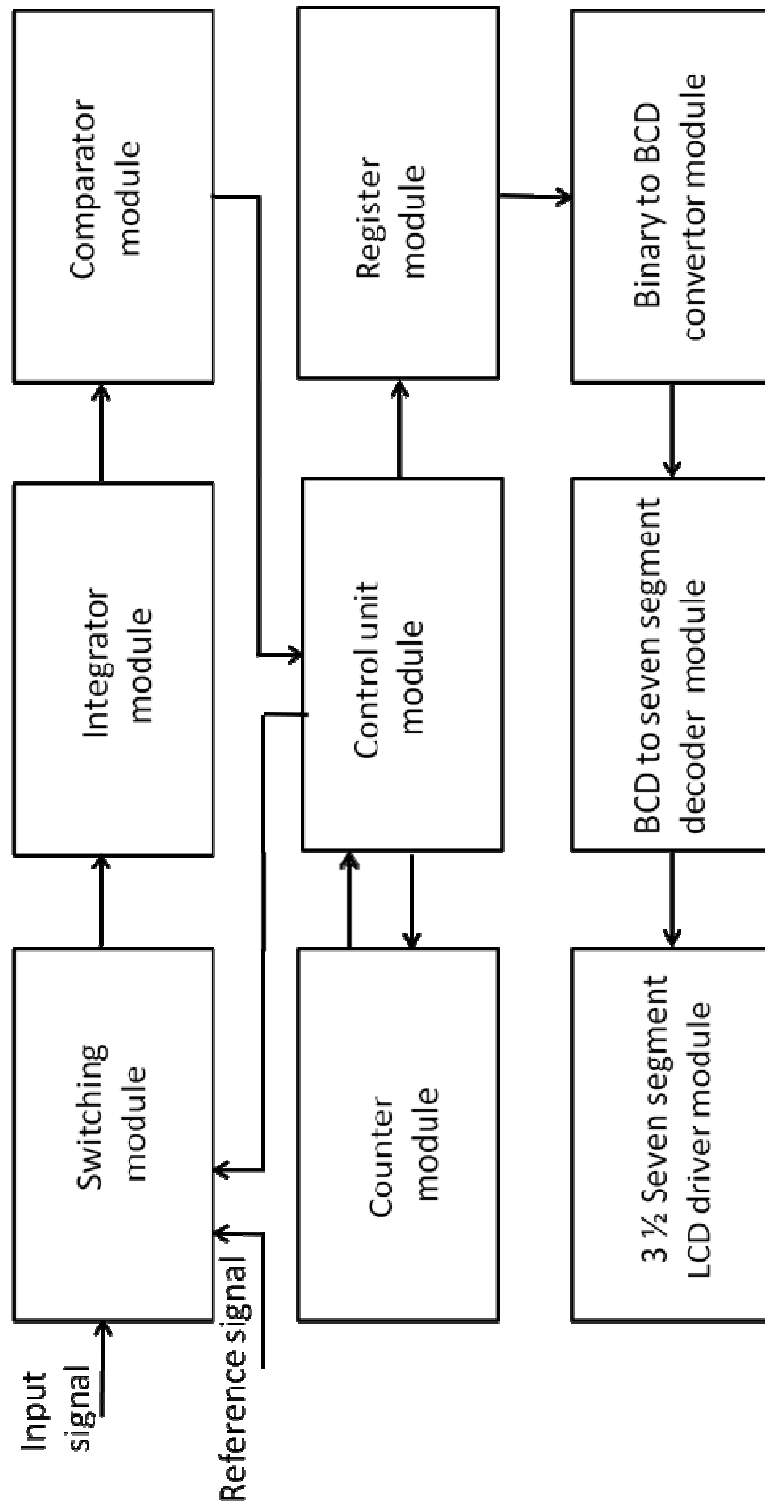


Figure 3.1: Block diagram of dual slope ADC

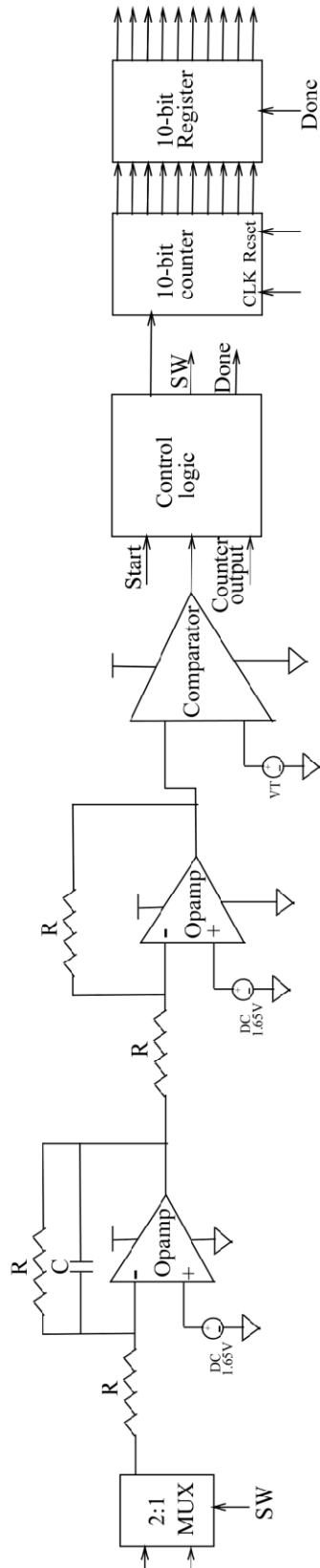


Figure 3.2: Complete schematic diagram of Dual slope ADC.

## 3.2 Design Specifications

The fast evolution of modern VLSI benefits from the fact that people are able to steadily scale down device dimensions with advanced process technology. Nevertheless, the trend to develop portable and battery operated electronic instruments requires low power consumption electronics. Therefore low power supply voltage is a natural choice in modern IC designs to meet above requirements. In this design 3.3V is chosen as the power supply voltage, which is supported by 0.18 $\mu$ m UMC technology. Another target of this design is high resolution, which is chosen as 100 $\mu$ V.

### 3.2.1 Specification of Two Stage Op-amp

Operational amplifier is the key analog component of Dual slope ADC. It was assume that an ideal op-amp with infinite gain has no offset. In general, op-amps are easily available with high gain but not infinite so it leaves the problem of offset. An offset voltage affects the slope of integration. If the offset voltage is  $\Delta V$  then

$$\begin{aligned} \frac{V_{in} + \Delta V}{RC} T1 &= \frac{V_{ref} + \Delta V}{RC} T2 \\ \frac{V_{in} + \Delta V}{RC} T1 - \frac{V_{ref} + \Delta V}{RC} T2 &= 0 \\ \frac{V_{in}}{V_{ref}} &= \left(1 + \frac{\Delta V}{\Delta V_{ref}}\right) \frac{T2}{T1} - \frac{\Delta V}{\Delta V_{ref}} \end{aligned} \quad (4)$$

Equation (4) shows that the effect of offset voltage on the dual slope ADC. Here a high gain op-amp has been designed so that offset voltage will become negligible. In this ADC design, a high gain operational amplifier is required. A high gain operational amplifier forms an integrator together with resistor R and capacitor C in a well known fashion.

### 3.2.1.1 Design Specifications

**Table 3.1 Target specifications of two stage op-amp.**

<b>Specifications</b>	<b>Target value</b>
DC Gain	70 dB
Phase margin	60°
Unity gain bandwidth	5 MHz
Input common mode range	0.7-3.1V
Common mode rejection ratio	>100 dB
Input offset voltage	<50 $\mu$ V
Settling time	1 $\mu$ S
Slew rate	>5V/ $\mu$ S
Power Dissipation	528 $\mu$ W
Load capacitance	2.5 pF
Power supply	3.3 V

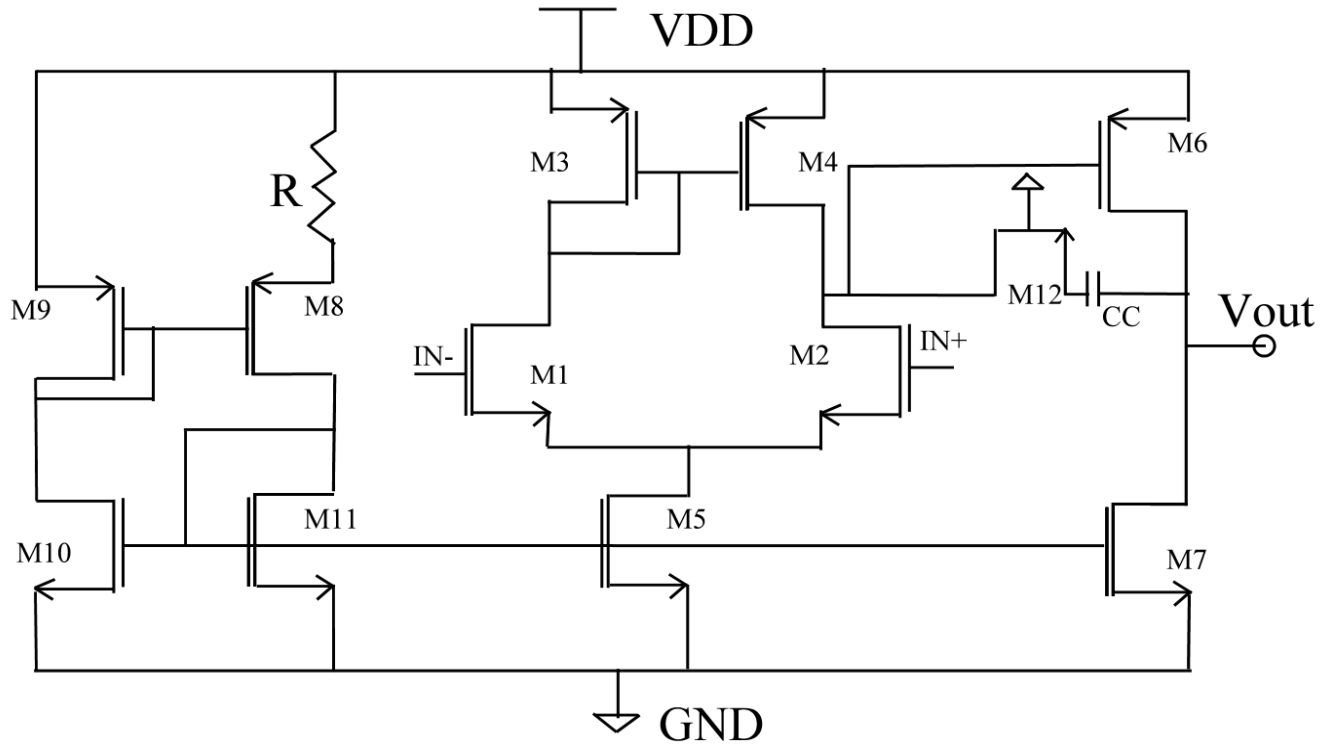


Figure 3.3: N-channel based two stage op-amp.

### 3.2.1.2 Design procedure

Step 1: Determine the value of current in the output stage using slew rate and load capacitance.

$$I7 = I6 = C_L * SR$$

Step 2: Calculate the sizes of transistor M6 and M7 using current and assume that all the transistors are in saturation in saturation region.

$$\frac{W6}{L6} = \frac{2 * I6}{Kp * ((V_{DS})_{sat})^2}$$

$$\frac{W7}{L7} = \frac{2 * I7}{Kn * ((V_{DS})_{sat})^2}$$

Step 3: Now assume the capacitance of first stage C1. Using this value of the output capacitance and slew rate we can find the tail current (bias current).

$$I5 = C_1 * SR$$

Now calculate the value of gate to source voltage of the current mirror load transistors M3 and M4 by using maximum input common mode voltage.

$$V_{SG3} = V_{DD} - (V_{in})_{max} + V_t$$

Using the gate source voltage calculated above we can calculate the sizes of transistor M3 and M4.

$$\frac{W3}{L3} = \frac{W4}{L4} = \frac{I5}{Kp * (V_{SG3} - |V_{tp}|)^2}$$

Step 4: Next step is to calculate the transconductance of input transistors M1 and M2 using gain relation of two stages.

$$g_{m1} = \frac{A_v(0) * (g_{ds2} + g_{ds4})(g_{ds6} + g_{ds7})}{g_{m6}}$$

$$g_{m6} = \sqrt{\frac{2Kp * W6 * I6}{L6}}$$

$$g_{dsi} = \lambda * I_{Di}$$

Using the tranconductance of differential pair and tail current we can calculate the sizes of M1 and M2.

$$\frac{W1}{L1} = \frac{W2}{L2} = \frac{g_{m1}^2}{Kn * I5}$$

Step 5: Next step is to calculate the  $V_{DS5}$  using minimum input common mode voltage.

$$V_{DS5} = (V_{in})_{min} - V_{GS1} - V_{SS}$$

Where

$$V_{GS1} = \sqrt{\frac{I5 * L1}{Kn * W1}} + V_{tn}$$

$$\frac{W5}{L5} = \frac{2 * I5}{Kn * ((V_{DS5})_{sat})^2}$$

For 60° phase margin

$$C_c \geq 0.22C_L$$

### 3.2.2 Integrator

As its name implies, the Integrator is an application of operational amplifier that performs the mathematical operation of Integration. The output responds to change in the input voltage over time and the integrator amplifier produces a voltage output which is proportional to that of its

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input voltage with respect to time. The general block diagram of Integrator is shown in figure 3.4. It uses R and C in feedback fashion.

**Figure 3.4: Block diagram of Integrator.**

### **3.2.3 Regenerative Latch Comparator**

The comparator is an essential component to determine the accuracy of data converters for any portable and implantable biomedical signal processing instrument. Power dissipation, supply voltage scaling, resolution, input range and offset cancellation are the main constraints in any CMOS comparator design. Latched comparators are used extensively in analog and mixed-signal circuits to compare two analog voltages, and generate a binary output. A basic latched comparator consists of a preamplifier followed by a positive feedback latch. The preamplifier provides a moderate gain, which increases resolution, and reduces kickback noise.

Here a comparator uses a four stage architecture, which consists of a preamplifier stage followed by a regenerative latch stage. To convert this double ended output to a single ended, a differential amplifier is used. The last stage is output driver stage, which increase the output driving capability and isolate the differential load capacitances. The input is initially amplified by a differential pair biased at 10  $\mu\text{A}$ .

### 3.2.3.1 Design Specifications

**Table 3.2 Target specification for regenerative latch comparator.**

Parameters	Target Specifications
Resolution	25 $\mu$ V
ICMR	1-3.3V
Load capacitance	1pF
Gain	>80 dB
Offset voltage	<50 $\mu$ V
Speed	<1 $\mu$ S
Power dissipation	580 $\mu$ W
Power supply	3.3V

**Figure 3.5: Schematic of regenerative latch comparator.**

### 3.3 Control Logic

It is an important part of Dual slope ADC. The ADC operation is controlled by the digital block which is made up of a finite state machine. After release of the Reset signal the ADC cycles through four states successively. These states are:

**IDLE** - Idle mode.

**VinINT** - Input signal integration for fixed time.

**VrefINT** - Reference signal Integration for variable time.

**EOV** - End of conversion and digital output transmission.

When the ADC is ready for a new conversion the start signal is high IDLE state switches to the VinINT state during which the input signal is integrated for a fixed time. The integration time depends on the adjusted resolution, applied clock frequency and is equal to  $\tau_{int} = 2N / f_{clk}$ , where N is the number of bits and  $f_{clk}$  is the clock frequency. During this phase, based on the counter output, VinINT switches to the VrefINT state. In the VrefINT state integrator capacitor is discharged for a variable time which depends on the input value. Based on the comparator output, the VrefINT changes to the EOV state and done signal will switch to high and output will be stored in register. After generating the done signal, counter will reset by the reset signal which is generated by the control logic.

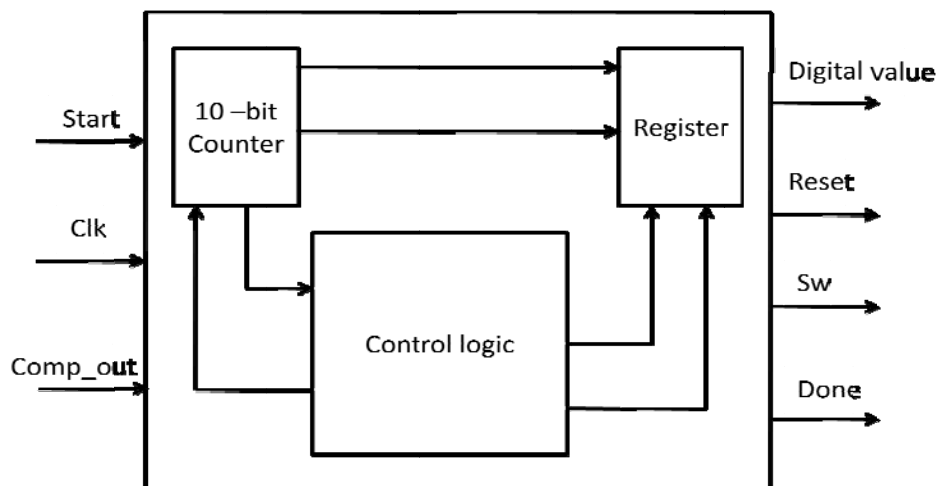
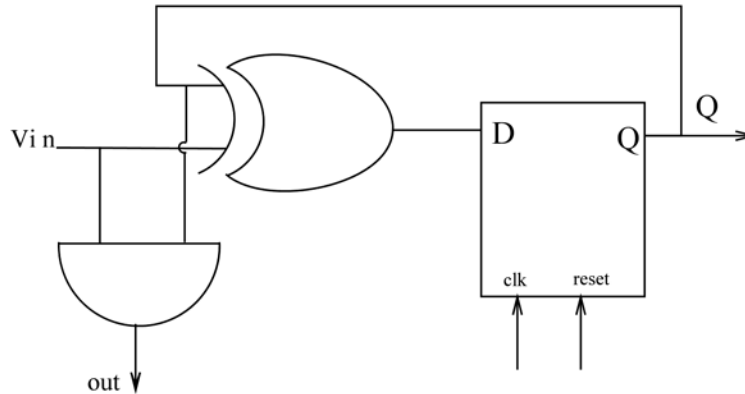


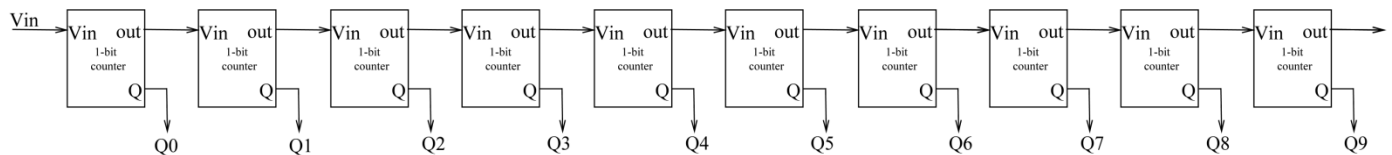
Figure 3.6: Control logic for dual slope ADC.

### 3.3.1 10-bit Counter

Counter is an important part of control logic. For designing of 10-bit dual slope ADC, a 10-bit counter is needed. A 10-bit counter has been designed with the help of 1-bit counter. A 1-bit counter is shown in figure 3.7(a) and a 10-bit counter is shown in figure 3.7(b).



**Figure 3.7(a): Block diagram of 1-bit counter.**



**Figure 3.7(b): Block diagram of 10-bit counter.**

### 3.3.2 10-bit Register

To store the output of 10-bit dual slope ADC, a 10-bit parallel in parallel out register has been designed using D flip-flops. After completion the operation of ADC, a done signal is generated by the control logic. When this done signal switches to high, the value of counter is stored into the register.

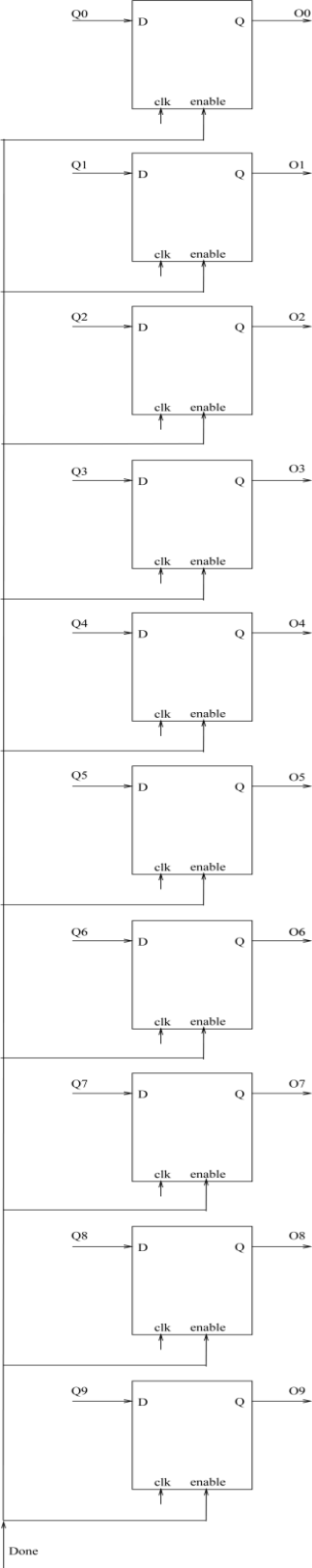


Figure 3.8: Block diagram of 10-bit Register.

### 3.4 Layout Design

The layout of analog integrated circuits often driven by several issues that is generally not important in digital circuits. Analog layout demand many more layout precautions so as to minimize effects such as mismatches and noise. The main problems of layout for analog ICs are device matching and unwanted parasitic reduction. Use of transistor fingering for large and critical transistors is always beneficial. In fingering the transistor is fingered into multiple transistors that are connected in parallel. This also decreases the physical size of device and thus can provide a more compact layout. Minimum size will also reduce the parasitic capacitance. Mismatches can also be minimized by adding dummy transistors in the structure.

For layout design Cadence Virtuoso layout editor is used. DRC, LVS and RCX have been performed by using Cadence Assura.

#### 3.4.1 Layout of Two Stage Op-amp

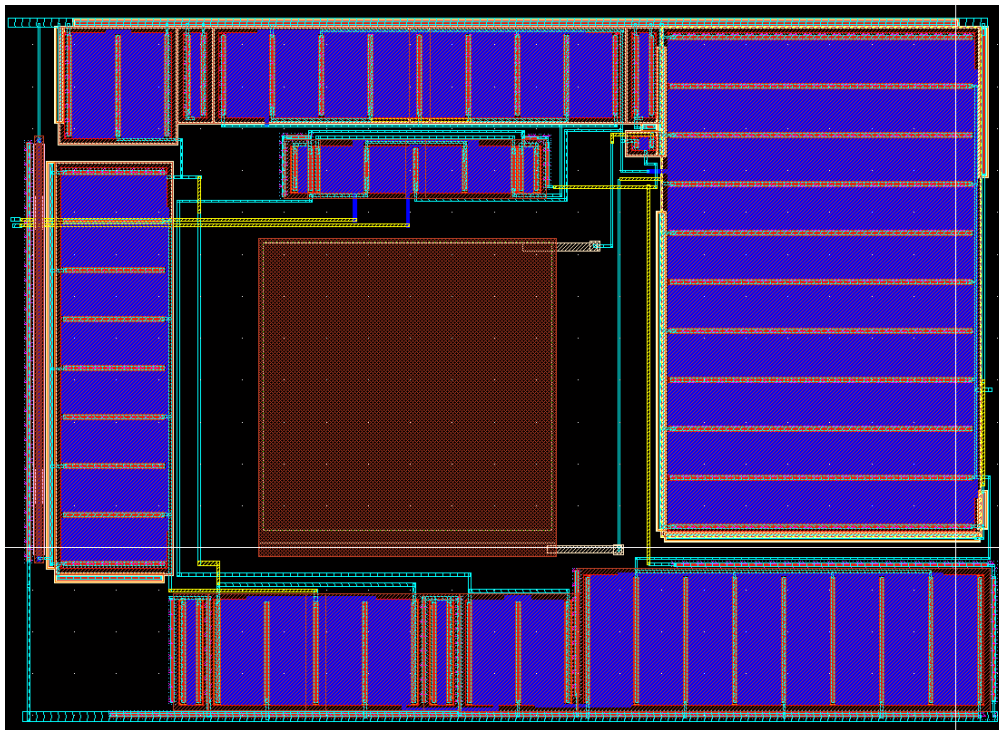


Figure 3.9: Layout of Two Stage Op-amp.

### 3.4.2: Layout of Regenerative Latch Comparator

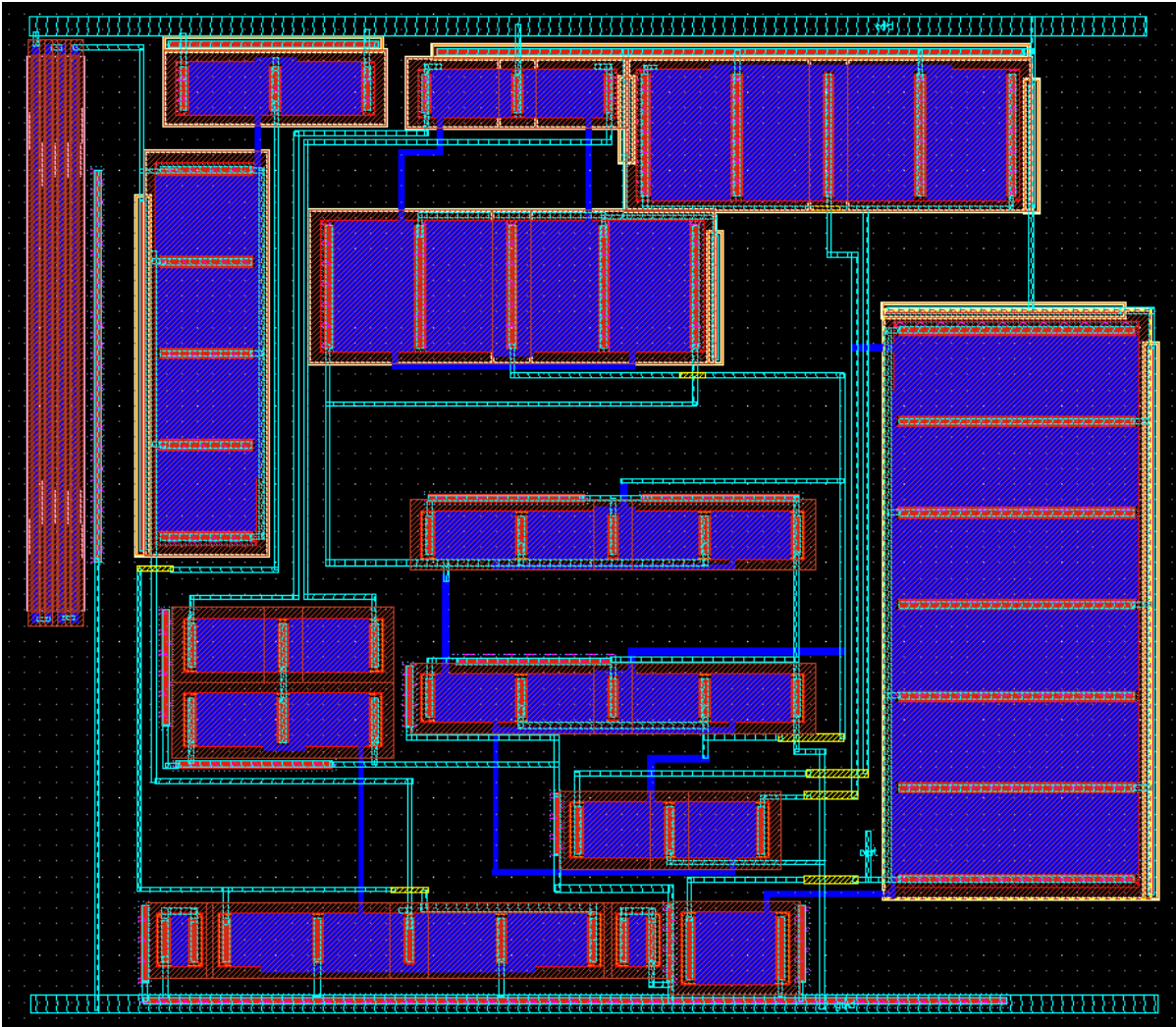


Figure 3.10: Layout of regenerative latch comparator.

### 3.4.3 Layout of 1-bit Counter

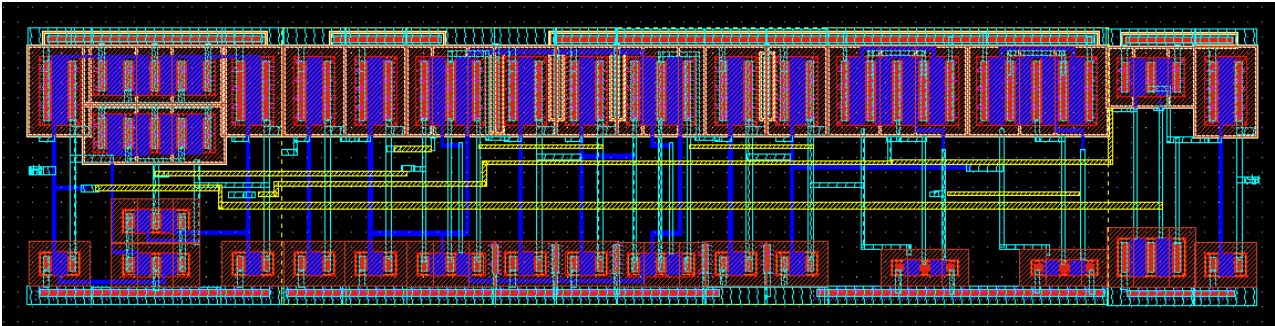


Figure 3.11: Layout of 1-bit counter.

### 3.4.4 Layout of D Flip-flop

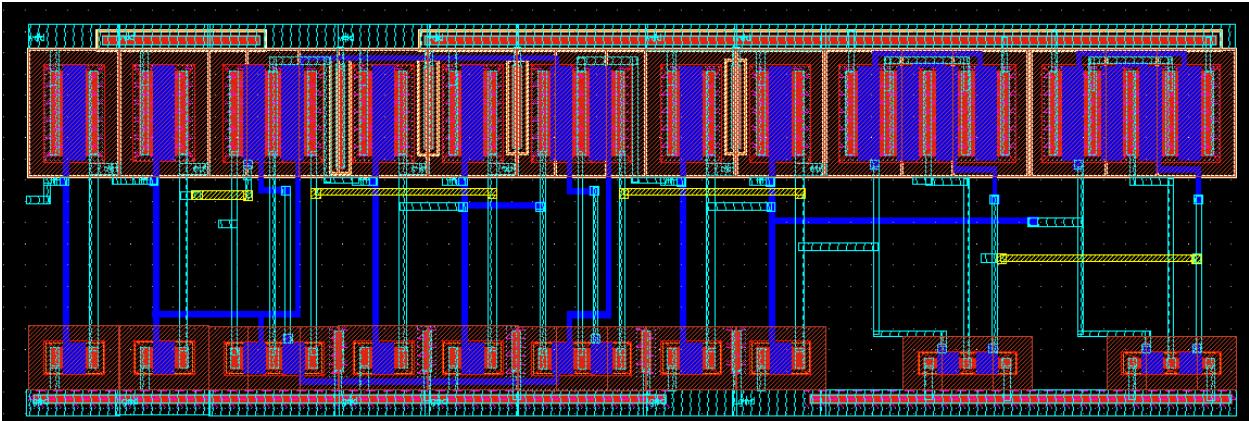


Figure 3.12: Layout of D flip-flop.

### 3.4.5 Layout of 10-bit Counter

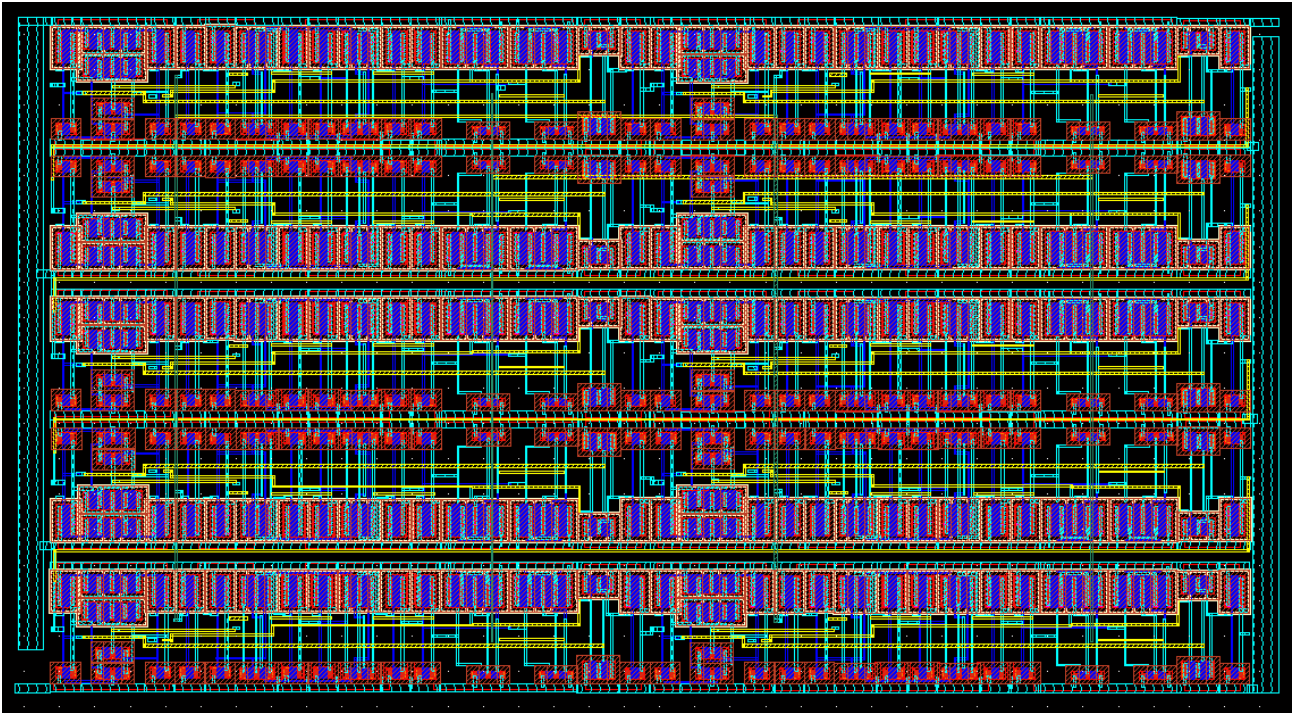


Figure 3.13: Layout of 10-bit counter.

### 3.4.6 Layout of Control Logic

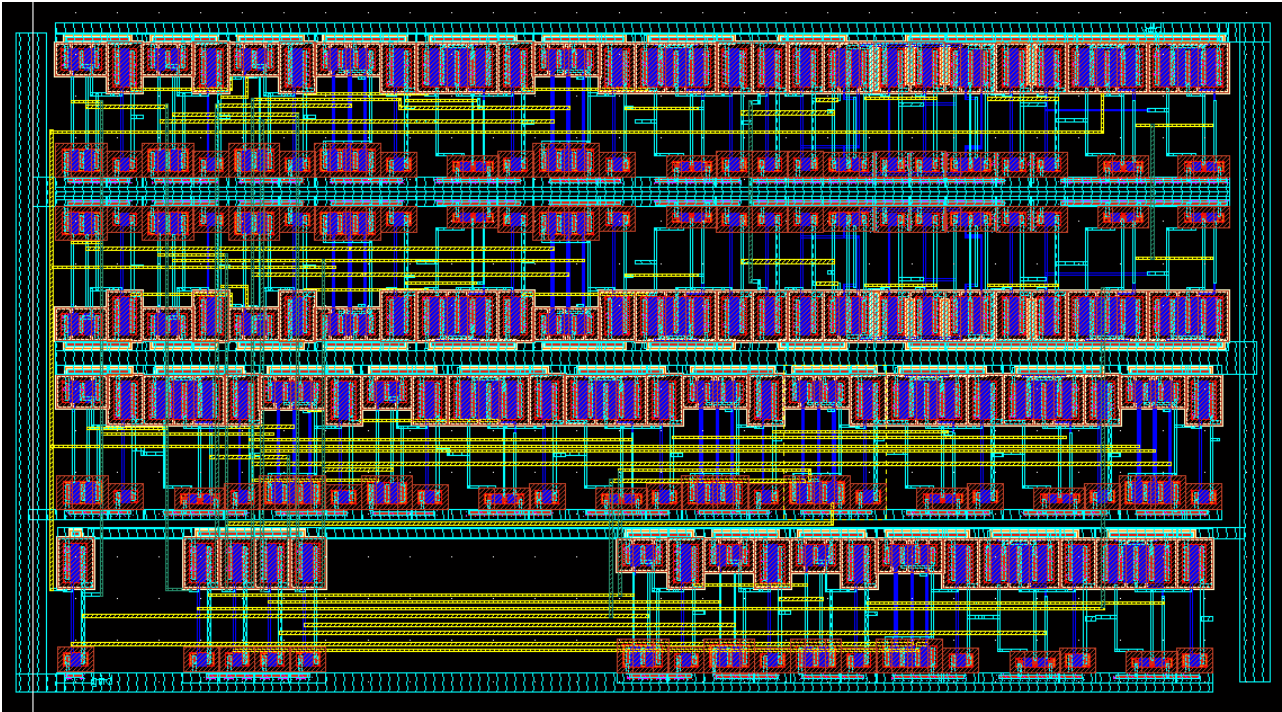


Figure 3.14: Layout of control logic.

# Chapter 4

## Simulation Results

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In this chapter the schematic and layouts of the key components of 10-bit Dual Slope ADC like two stage op-amp, Regenerative latch comparator and counter have been tested for various parameters. The whole design is powered by supply voltage of 3.3V. Test simulations are performed using Spectre simulator. This chapter divided in three sections:

- Schematic simulations
- Post layout simulations
- Process corner simulations

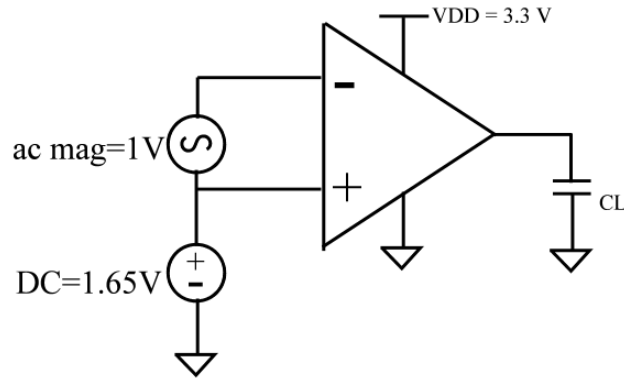
### 4.1 Pre Layout Simulations

#### 4.1.1 Two Stage Operational Amplifier

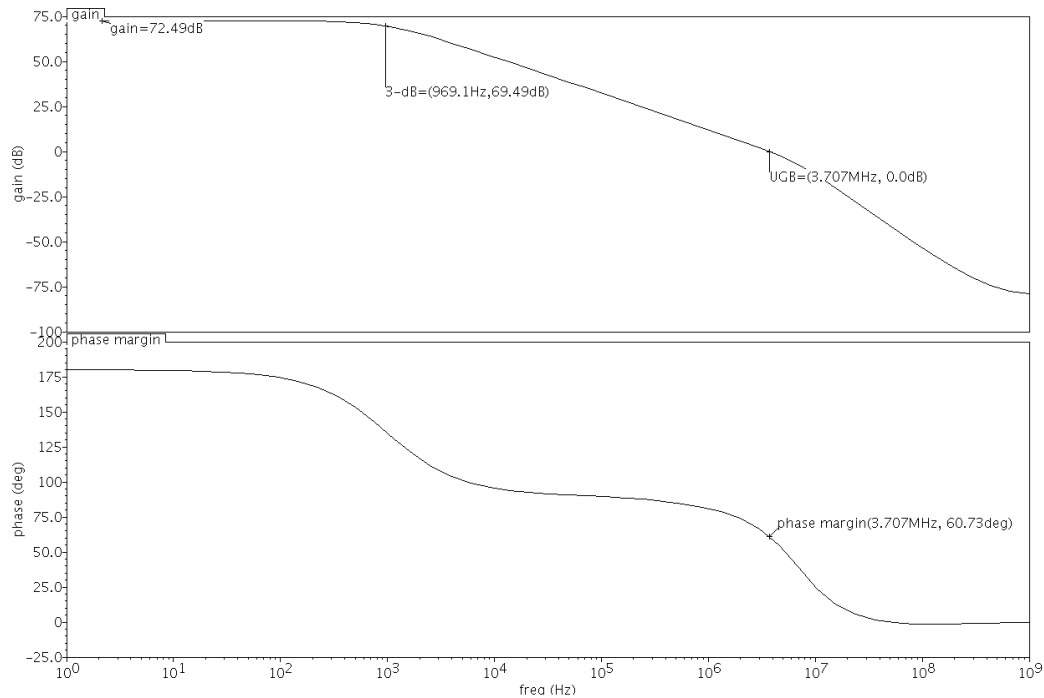
All the parameters of two stage op-amp at schematic level are shown below:

##### 4.1.1.1 AC Response

In this setup sinusoidal signal is applied between two inputs. DC potential is also applied along with the sinusoidal signal in order to provide the bias voltage to the input transistors. In figure 4.1, gain and phase plot for 3.3 V, 27<sup>0</sup>C and for 2.5pF is shown. For a two stage op-amp, open loop gain is 72.49 dB and a phase margin is 60.73<sup>0</sup>. The unity gain bandwidth is 3.71MHZ and f<sub>3dB</sub> bandwidth is 969.5 HZ.



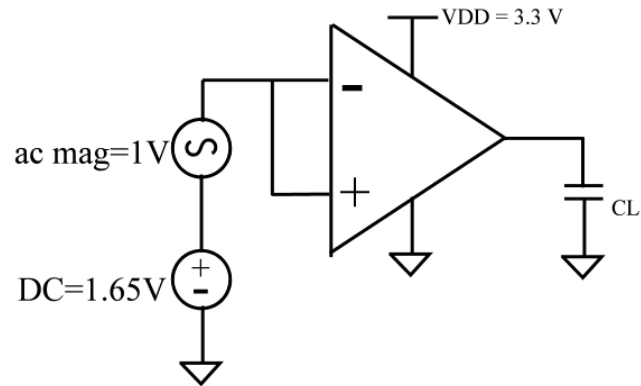
**Figure 4.1: Test setup of AC analysis.**



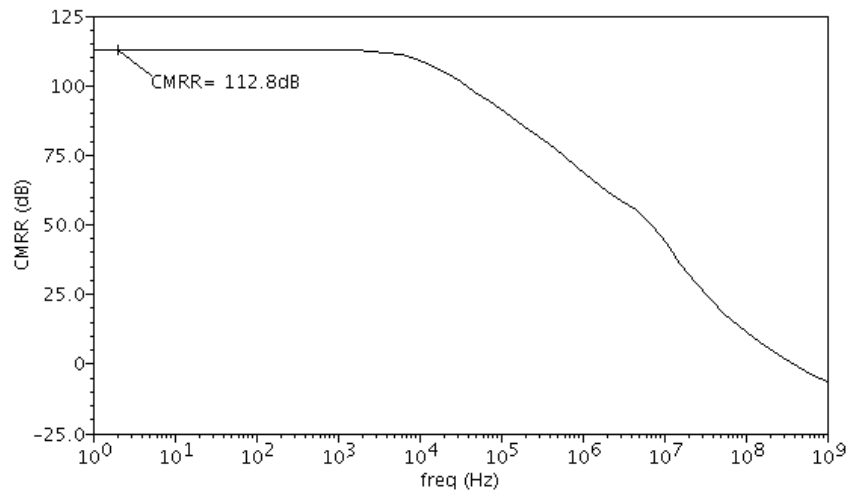
**Figure 4.2: AC response of two stage op-amp.**

#### 4.1.1.2 Common Mode Rejection Ratio (CMRR)

In order to simulate common mode rejection ratio, a 1V AC source is applied to both positive and negative terminal of the op-amp. When simulator sweep the frequency, and both inputs are at equal potential therefore the AC signal at the output will be the common mode gain. The previously calculated gain is divided by this gain to give CMRR. In this design, common mode rejection ratio of 112.8 dB was achieved.



**Figure 4.3: Test setup of common mode rejection ratio.**



**Figure 4.4: CMRR of two stage op-amp.**

#### 4.1.1.3 Input Common Mode Range (ICMR)

For measurement of ICMR, a unity gain configuration is shown in figure. In this case a non-inverting terminal is swept from 0 to 3.3V and inverting terminal is connected to the output. As shown in figure 4.5, when all the transistors are in saturation, the output follows the input in range from 1.1 to 3.15V.

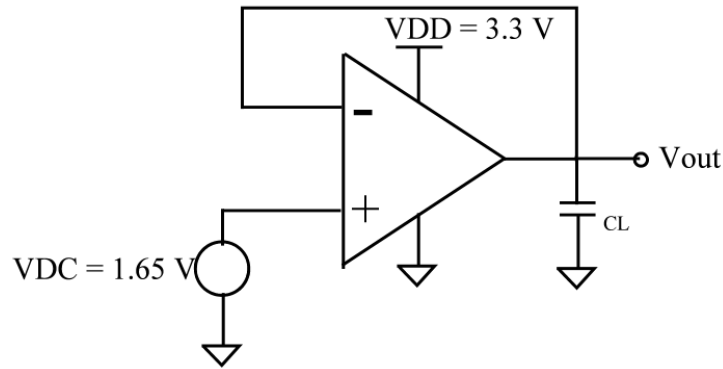


Figure 4.5: Test setup of input common mode range.

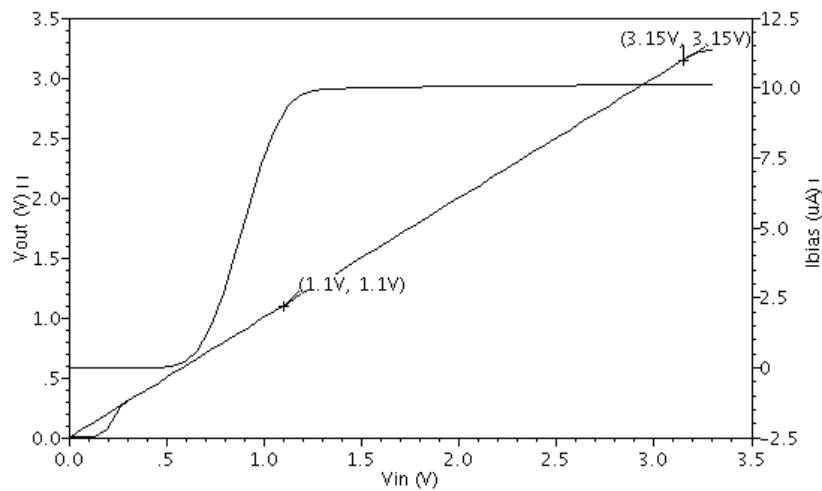


Figure 4.6: ICMR of two stage op-amp.

#### 4.1.1.4 Transient Response

For observing the transient response of the op-amp, a unity gain configuration with the swing at the input from 0 to 3V is shown in figure 4.7.

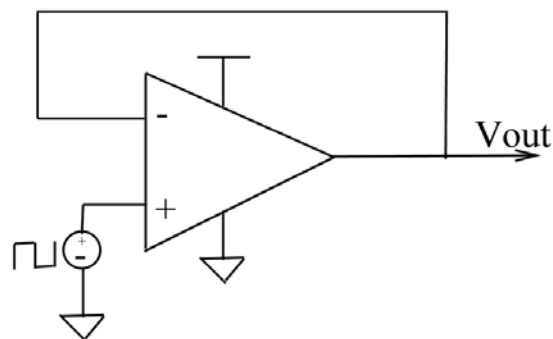
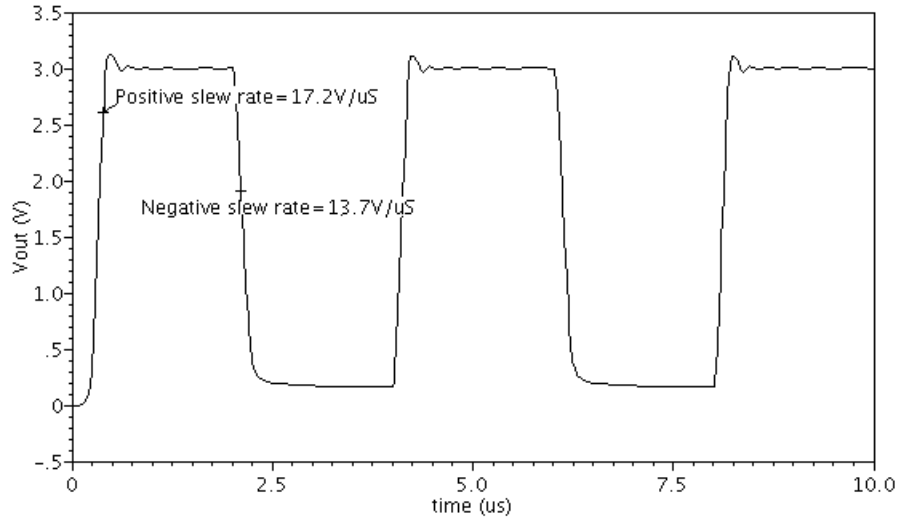
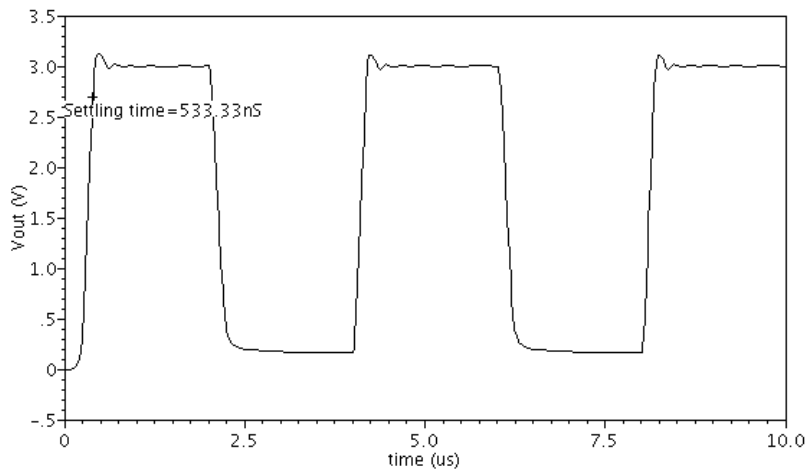


Figure 4.7: Test setup for transient analysis.



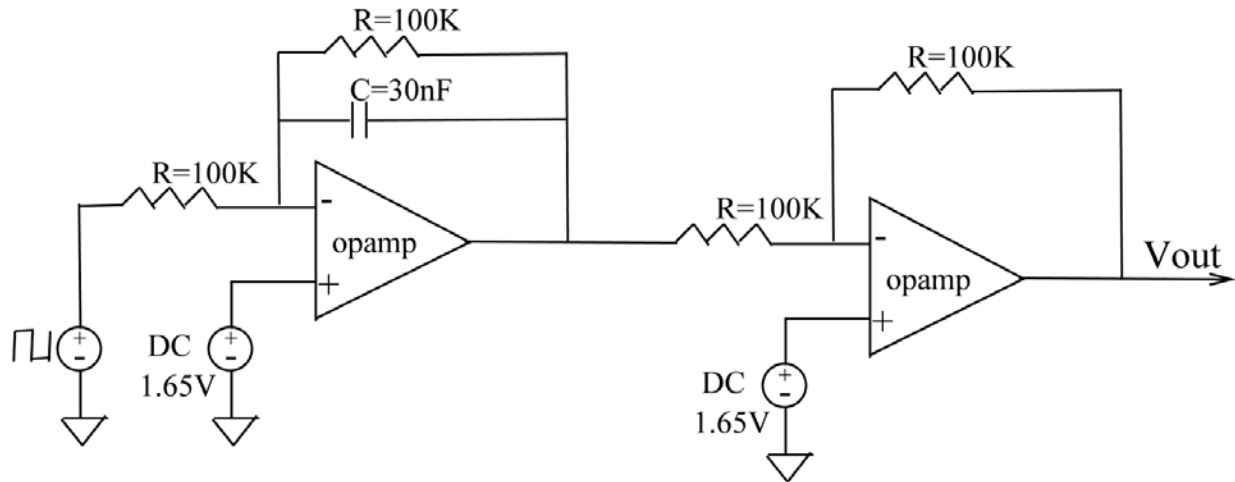
**Figure 4.8: Slew rate of two Stage op-amp.**



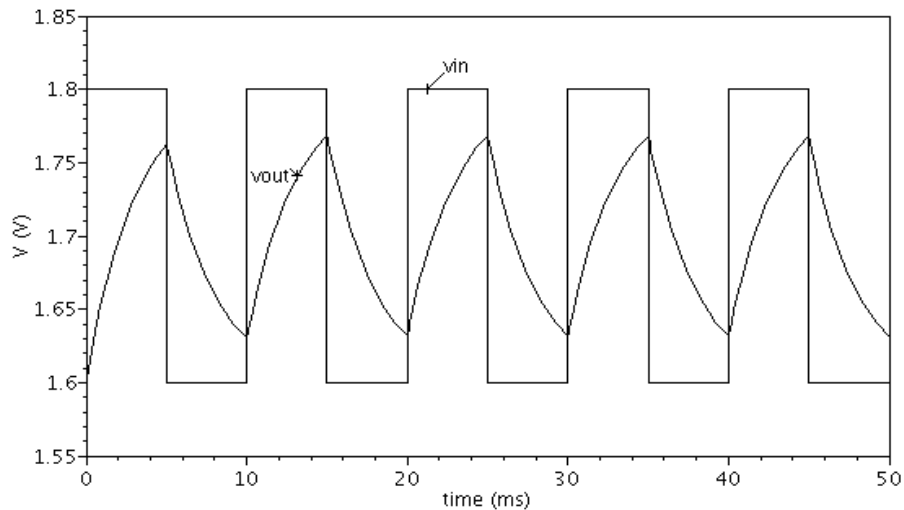
**Figure 4.9: Settling time of two stage op-amp.**

### 4.1.2 Transient Response of Integrator

To measure the response of integrator, a transient source of 200mV is applied to the negative input of the integrator. The positive terminal is set to a fixed DC value 1.65V. The output of the integrator is shown in figure 4.10:



**Figure 4.10: Test setup of non-inverting integrator.**



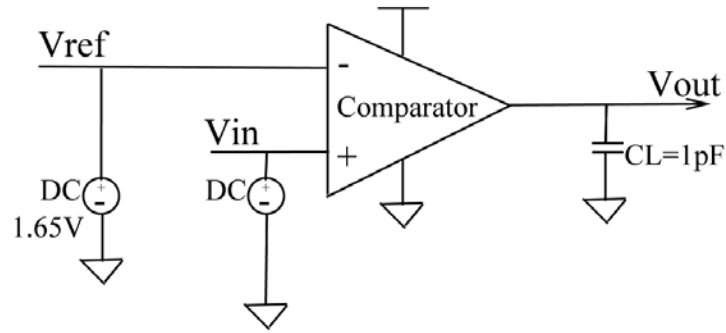
**Figure 4.11: Transient response of the Integrator.**

### 4.1.3 Regenerative Latch Comparator

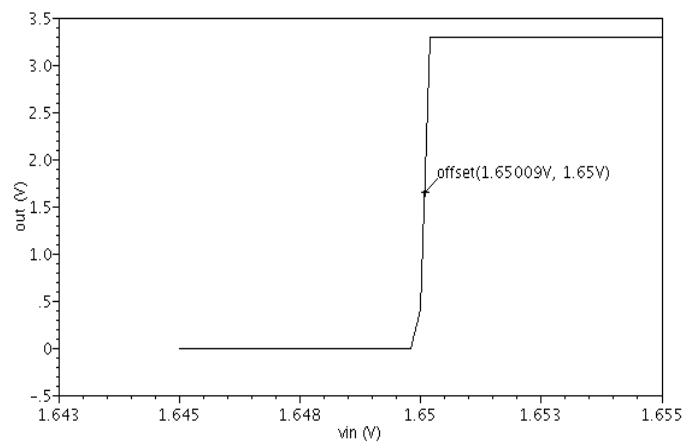
All the parameters of regenerative latch comparator at schematic level are shown below:

#### 4.1.3.1 DC Response

Offset voltage of regenerative latch comparator was measured by taking the value of Reference voltage at 1.65 V and the input of the comparator swept from 1.649 V to 1.651V. We get a systematic offset of 90  $\mu$ V.

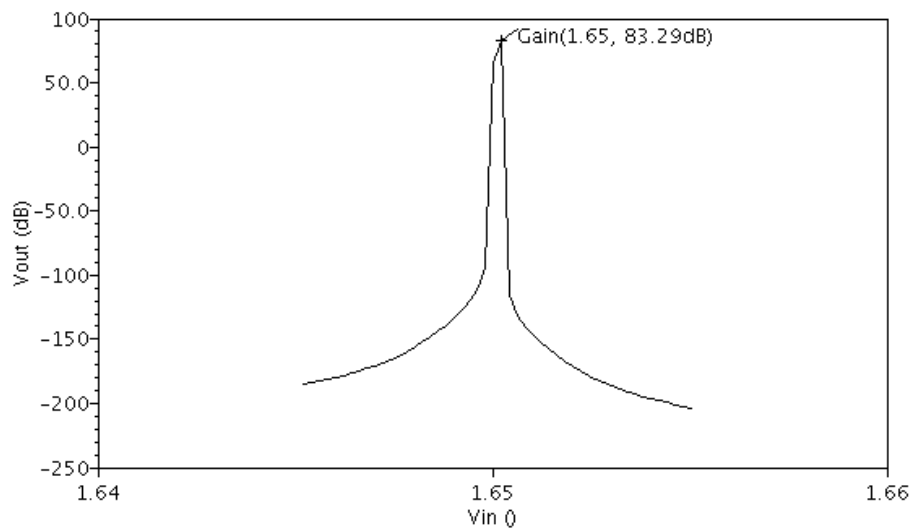


**Figure 4.12: Test setup of comparator for DC response.**



**Figure 4.13: Offset voltage of regenerative latch comparator.**

To measure the gain of comparator, we take the derivative of the transfer curve which is shown in figure 4.2. This comparator provides the gain of 83.29 dB.



**Figure 4.14: Gain of regenerative latch comparator.**

### 4.1.3.2 Transient Response

For observing the transient response of regenerative latch comparator a sinusoidal signal of  $10\ \mu\text{V}$  and  $100\ \text{Hz}$  frequency is applied to the input and the reference voltage was set to  $1.65\ \text{V}$ . The transient response of comparator is shown in figure 4.16.

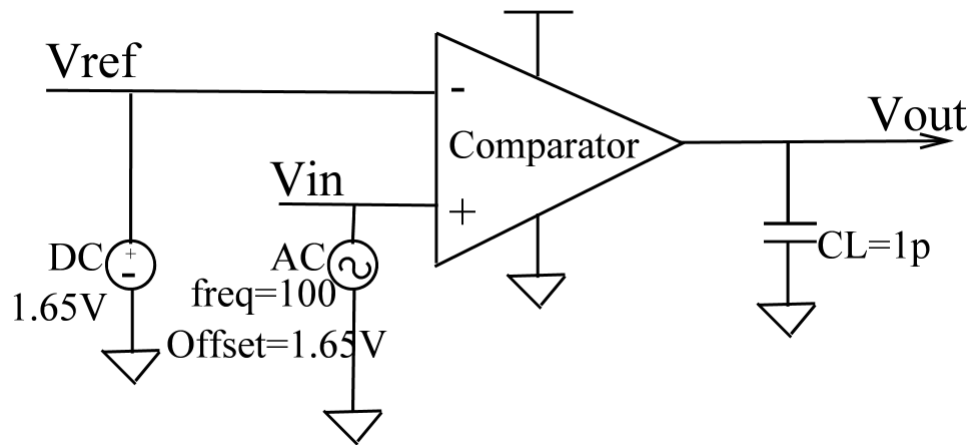


Figure 4.15: Test setup of transient response.

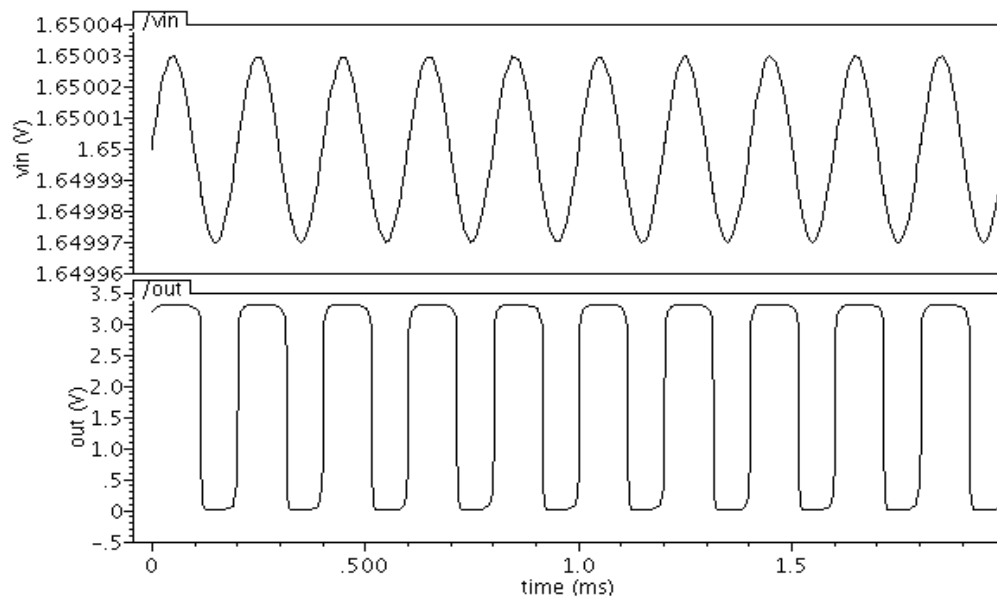


Figure 4.16: Transient response of regenerative latch comparator.

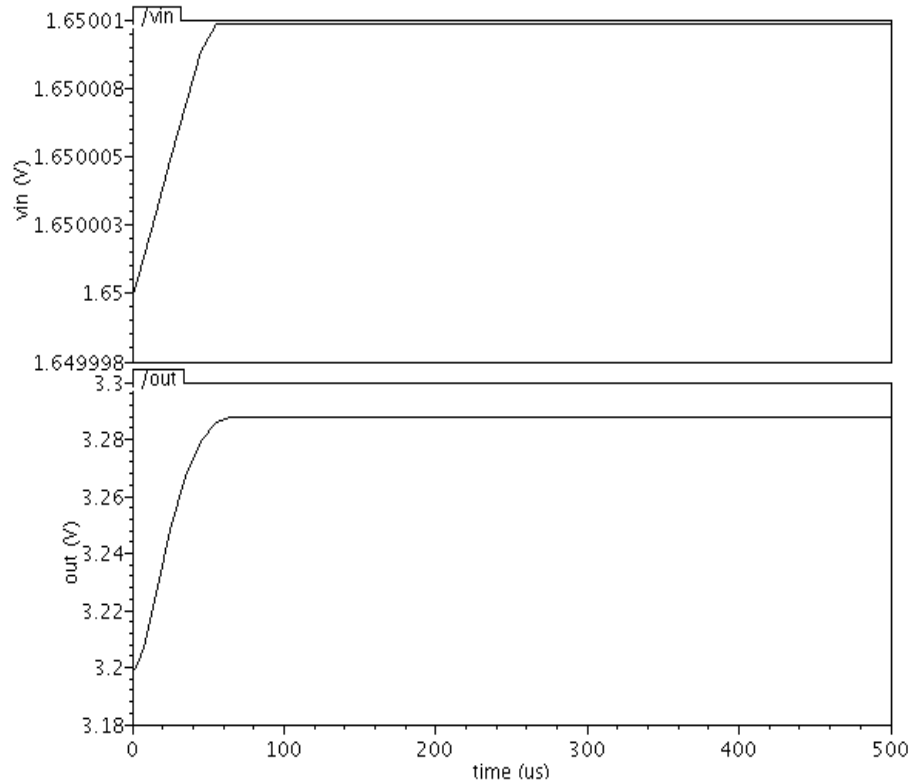


Figure 4.17: Resolution of regenerative latch comparator.

#### 4.1.3.3 Propagation Delay

To calculate the propagation delay of regenerative latch comparator, a 2mS wide pulse and amplitude vary from 1.64V to 1.66V is applied to the input of the comparator. In this duration, reference voltage is set to a fixed voltage 1.65V.

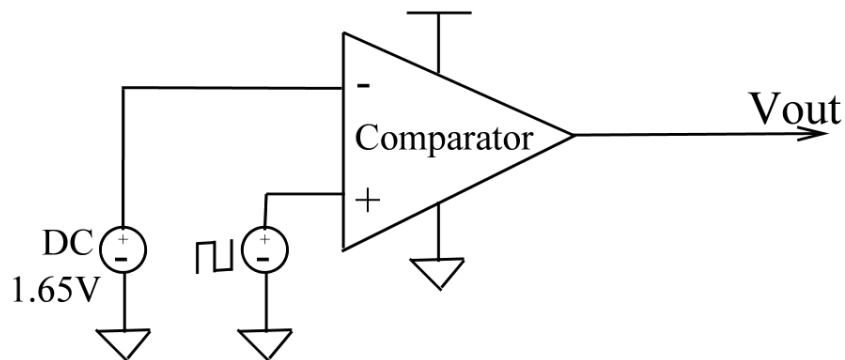


Figure 4.18: Test setup of propagation delay.

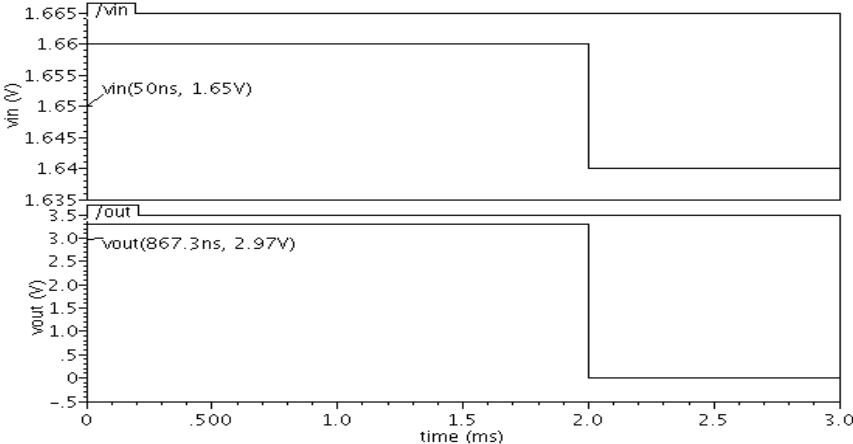


Figure 4.19: Propagation delay of regenerative latch comparator.

### 4.1.4 10-bit Counter

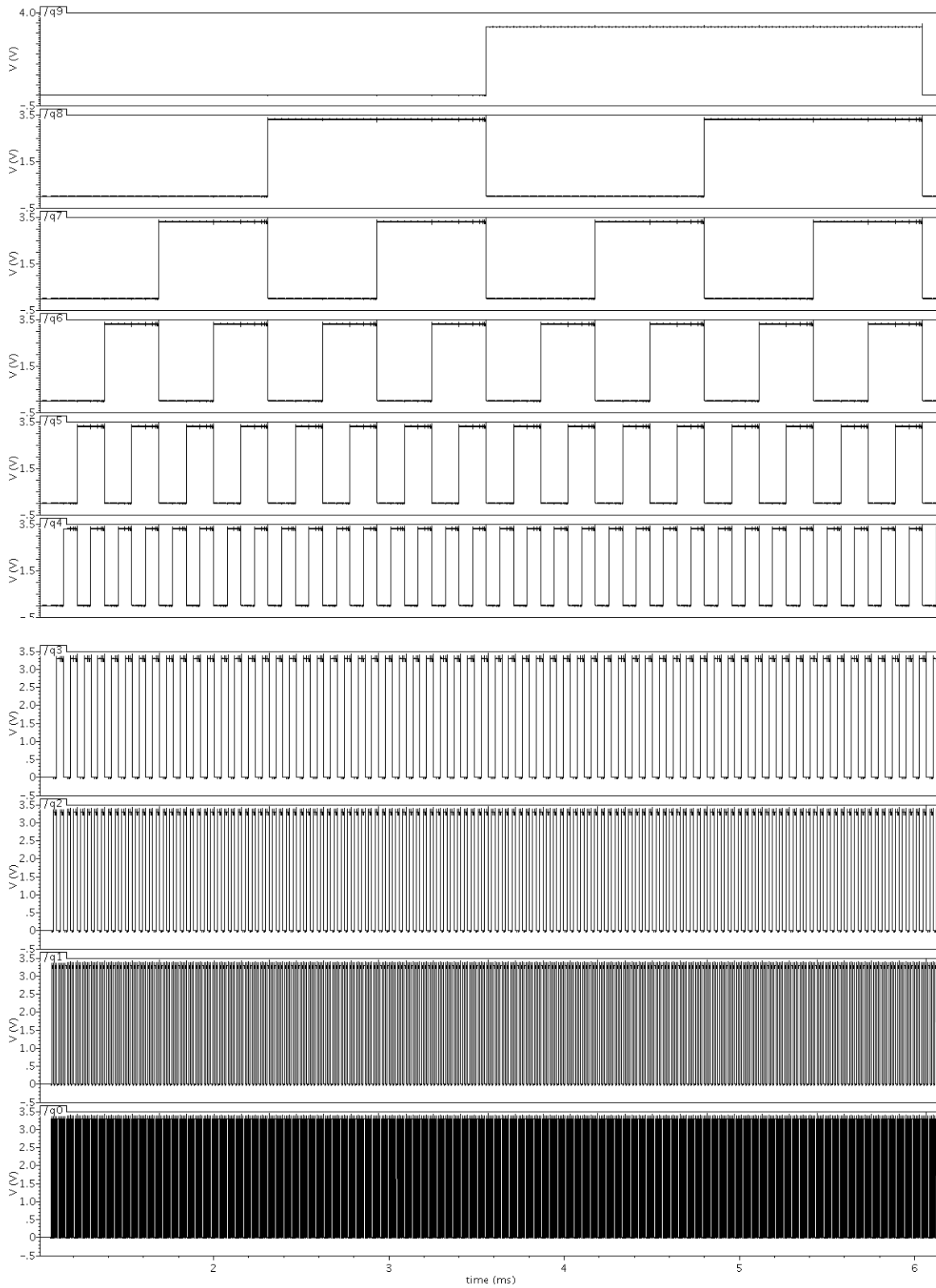


Figure 4.20: Output waveform of 10-bit counter.

### 4.1.5 10-bit Dual Slope ADC

Table 4.1 Simulation results of 10-bit dual slope ADC.

Analog input (Vin in volts)	Reference Voltage (Vref in volts)	ADC output	Total steps
0.71	0.3	0001000110	70
0.8	0.3	0010101101	173
1.2	0.3	0111101011	491
1.49815	0.3	1010001001	651
1.5	0.3	1010001001	651
1.50185	0.3	1010001011	653
2	0.3	1101001110	846
2.5	0.3	1111100111	999
2.55	0.3	1111110100	1012
2.59	0.3	1111111111	1023

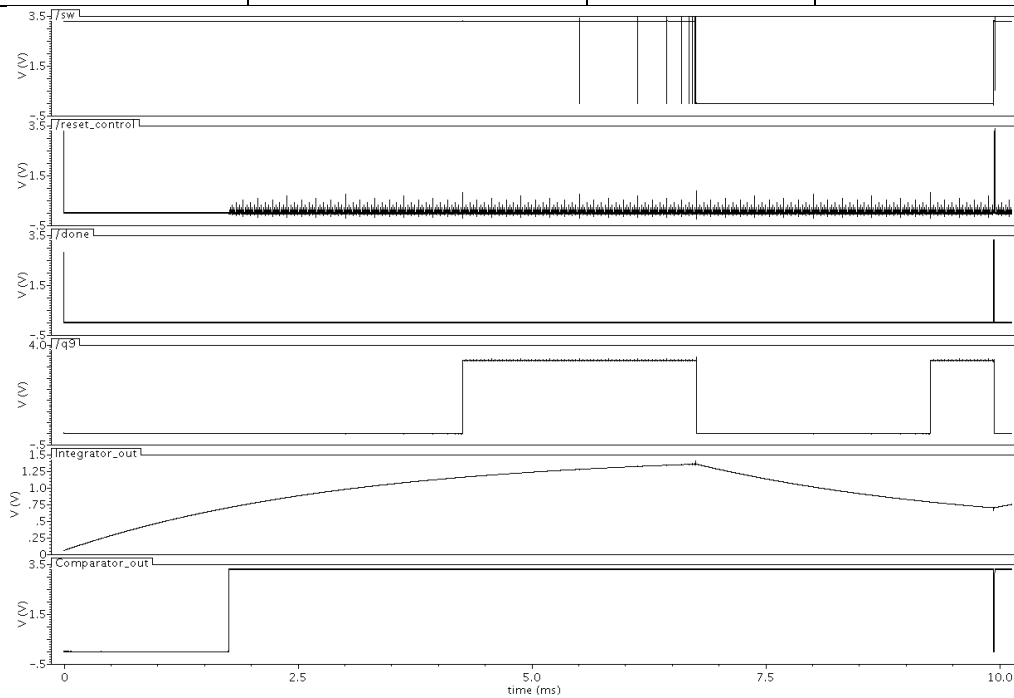


Figure 4.21: Waveform of 10-bit dual slope ADC.

## 4.2 Post Layout Simulation Results

After completing the layouts of op-amp, comparator and counter, it is matched with schematic using LVS simulation. With the successful run of LVS, parasitic and layout netlist extraction simulation have been done using RCX. Post layout simulations have been done using extracted netlist. The simulation results of post layout are given below:

### 4.2.1 Two Stage Op-amp

Different parameters of two stage op-amp for post layout simulation are shows below. The results show that there is a very small negligible variation in performance of op-amp.

#### 4.2.1.1 AC Response

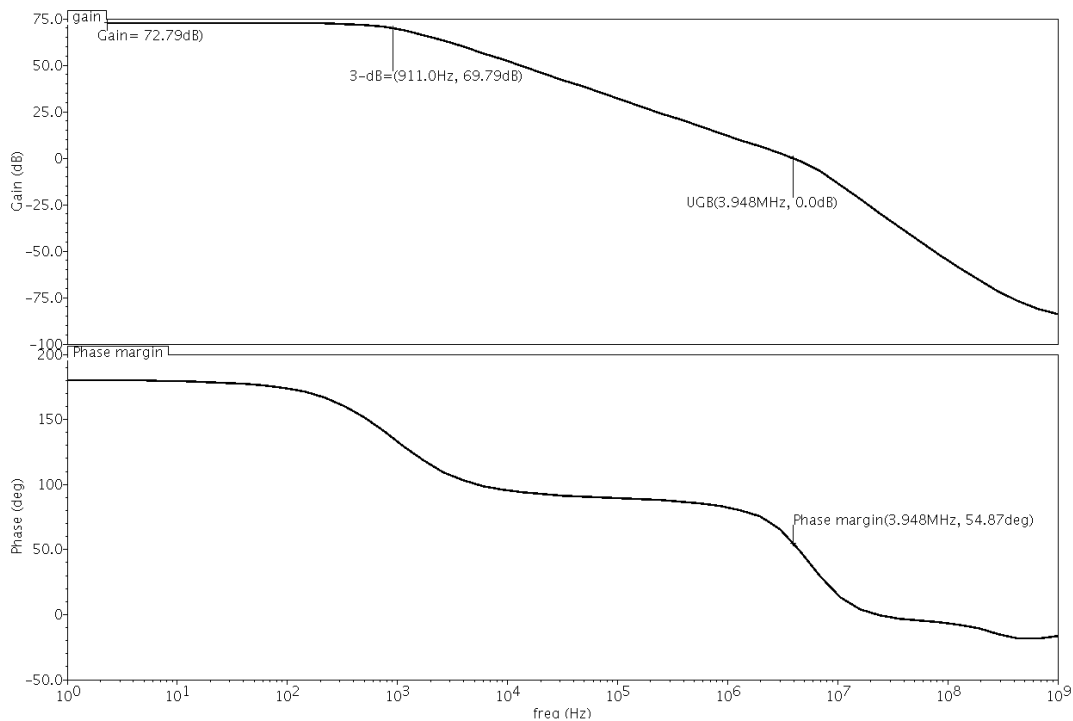


Figure 4.22: Post layout AC response of two stage op-amp.

### 4.2.1.2 CMRR

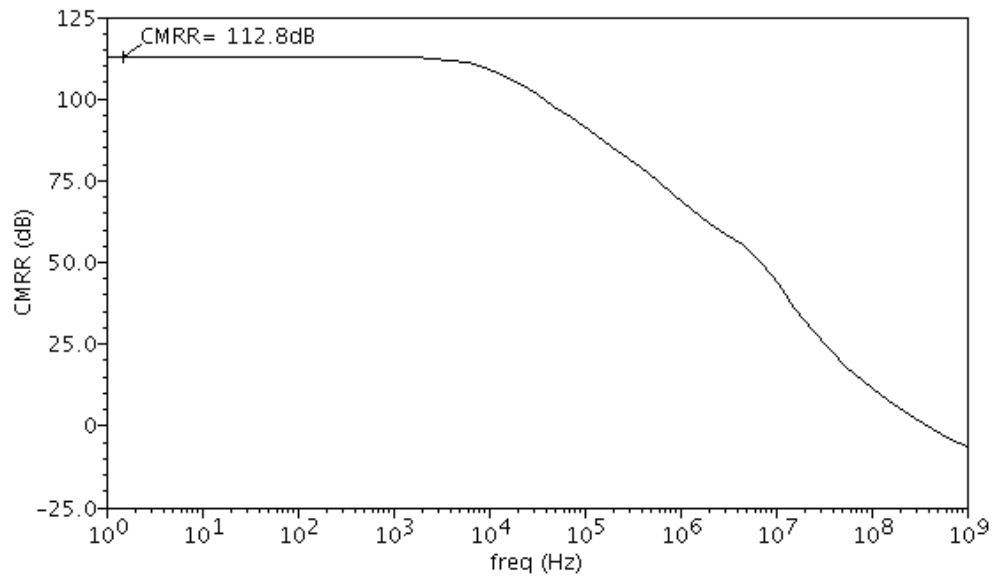


Figure 4.23: Post layout CMRR of two stage op-amp.

### 4.2.1.3 ICMR

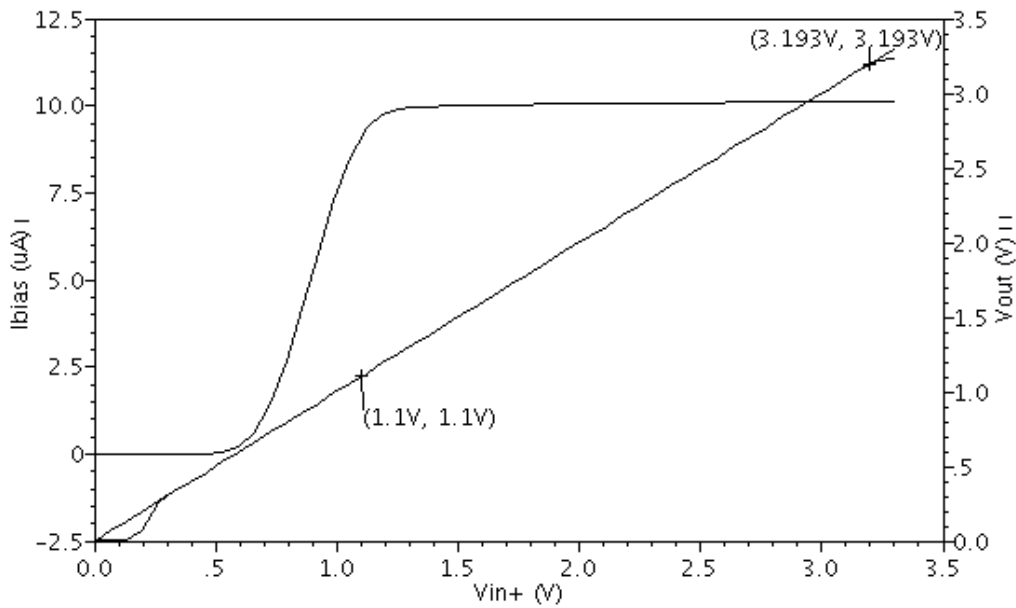


Figure 4.24: ICMR of two stage op-amp.

#### 4.2.1.4 Slew Rate

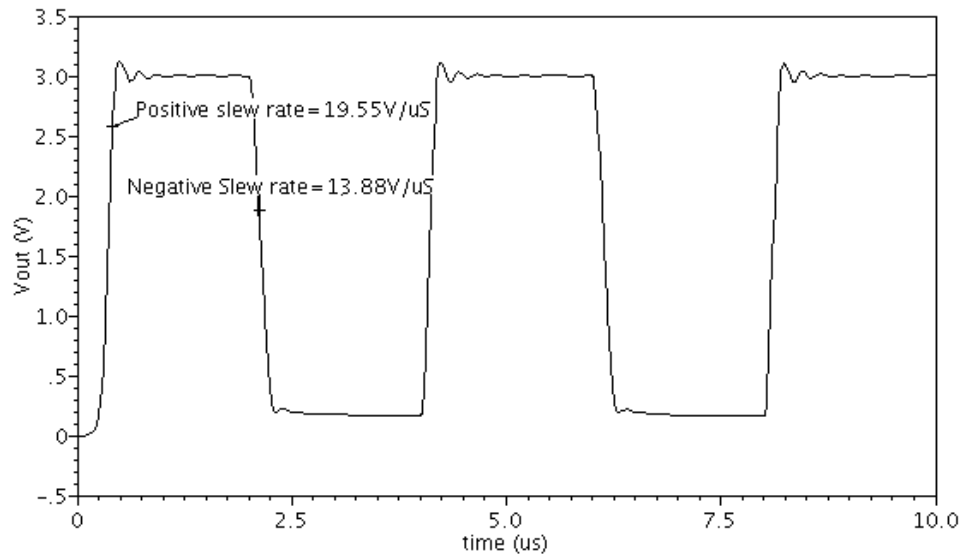


Figure 4.25: Slew rate of op-amp.

#### 4.2.1.5 Settling time

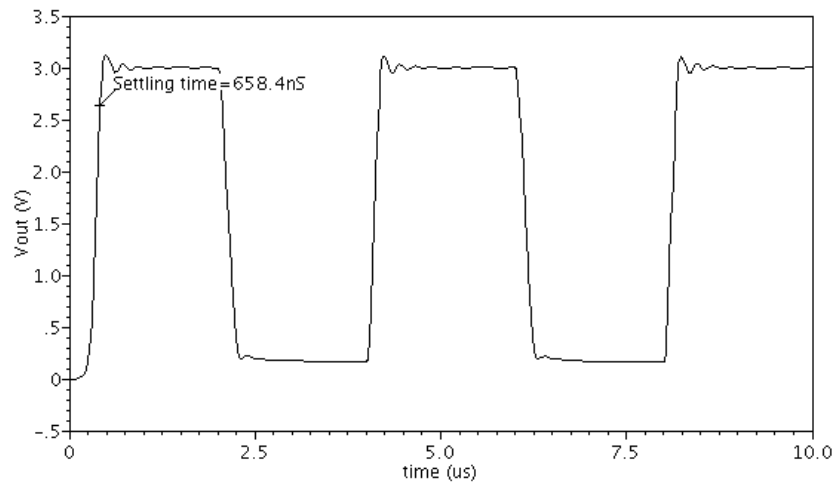


Figure 4.26: Settling time of op-amp.

### 4.2.2 Regenerative Latch Comparator

Different parameters of regenerative latch comparator for post layout simulation are shown below. The results show that there is a very small negligible variation in all performance parameters except power dissipation and propagation delay, yet they are in the desired range.

### 4.2.2.1 Offset voltage

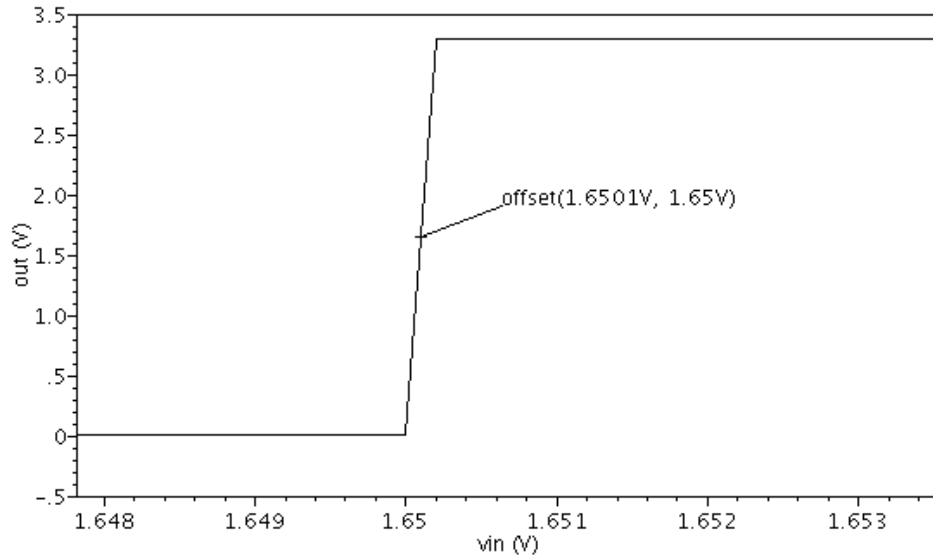


Figure 4.27: Offset voltage of regenerative latch comparator.

### 4.2.2.2 DC Gain

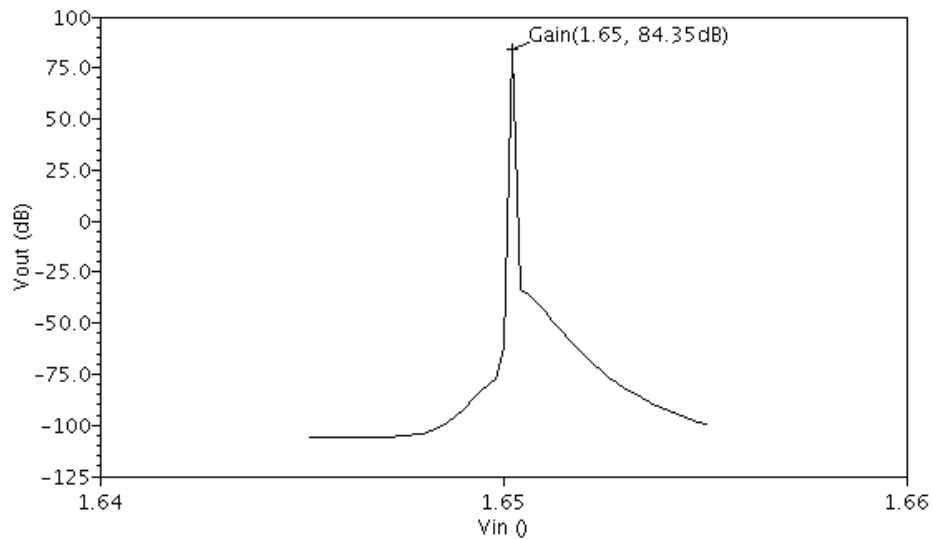


Figure 4.28: Gain of regenerative latch comparator.

### 4.2.2.3 Propagation Delay

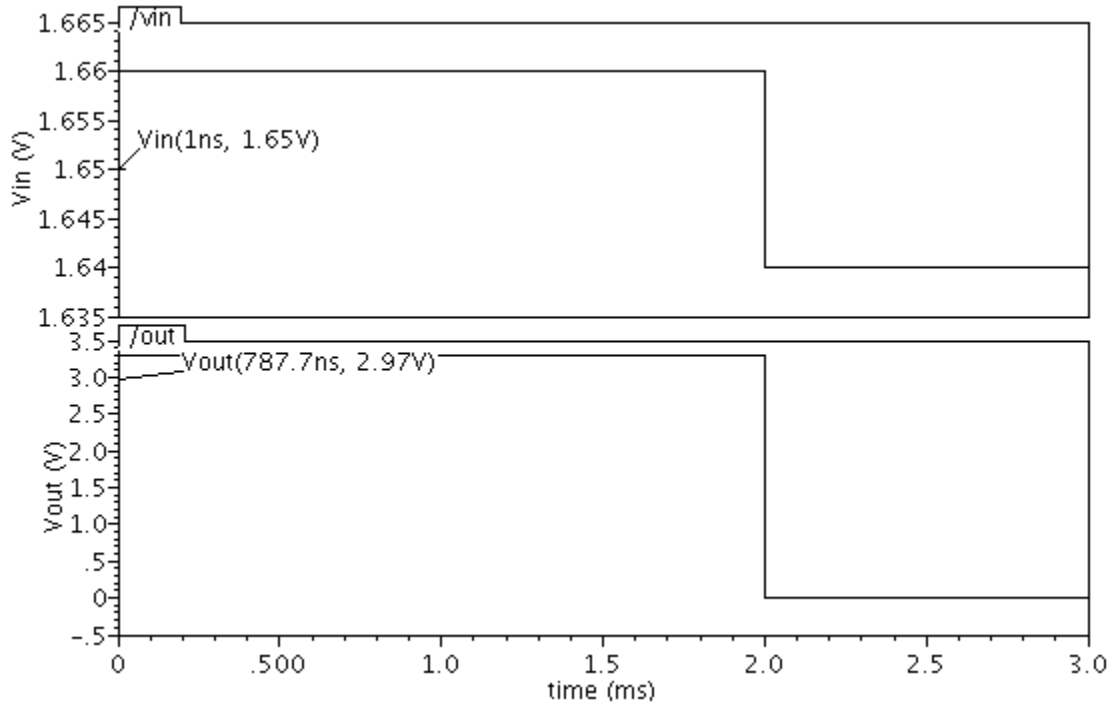


Figure 4.29: Propagation delay of regenerative latch comparator.

### 4.2.2.4 Resolution

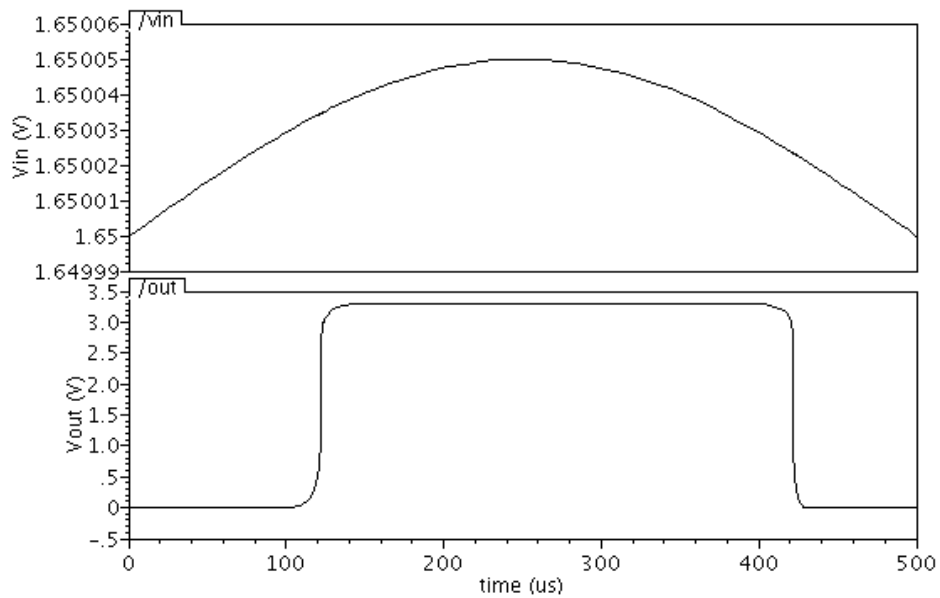


Figure 4.30: Resolution of regenerative latch comparator.

**Table 4.2 Simulation results of regenerative latch comparator.**

Parameter	Schematic results	Post layout simulation
Offset voltage	90 $\mu\text{V}$	100 $\mu\text{V}$
Resolution	10 $\mu\text{V}$	50 $\mu\text{V}$
Input common mode range	0.3 to 3.3V	0.3 to 3.3 V
Propagation delay	817.3 nS	786.7 nS
Power dissipation	581 $\mu\text{W}$	-
Gain	83.29 dB	84.35 dB

**Table 4.3 Simulation results of two stage op-amp.**

Specifications	Target value	Pre layout simulation	Post layout simulation
DC Gain	70 dB	72.5 dB	71.9 dB
Phase margin	60	61.3 deg	55.3 deg
Unity gain bandwidth	5 MHZ	3.86 MHZ	3.9 MHZ
ICMR	0.7- 3.1	0.8– 3.2 V	0.8 – 3.2 V
CMRR	-	112.72 dB	112.76 dB
Input offset voltage	<100 $\mu\text{V}$	14.48 $\mu\text{V}$	14.13 $\mu\text{V}$
Settling time	-	460 nS	480 nS
Slew rate	> 5V/ $\mu\text{S}$	17.2V/ $\mu\text{s}$ (positive) 13.7V/ $\mu\text{s}$ (negative)	19.55V/ $\mu\text{s}$ 13.81V/ $\mu\text{s}$
Power Dissipation	528 $\mu\text{W}$	523 $\mu\text{W}$	521 $\mu\text{W}$
Load capacitance	2.5 pF	2.5 pF	2.5 pF
Power supply	3.3 V	3.3 V	3.3 V

### 4.3 Process Corner Simulation

Process corner simulation deals with the variation in process parameters (Threshold voltage, mobility and oxide thickness) during fabrication. As integrated circuit device geometries shrink and clock speeds increase, the extraction and simulation of parasitic resistance, capacitance and inductance assumes an increasingly important role in physical verification and the production of successful silicon. One naming convention for process corners is to use two letters, where the first letter refers to the NMOS corner and second letter refers to the PMOS corner. There are five possible corners: Typical-typical (TT), Fast-fast (FF), Slow-slow (SS), Fast-slow (FS) and Slow-fast (SF). The first three are called even corners because both PMOS and NMOS are affected evenly and do not adversely effects the logical correctness of circuit.

#### 4.3.1 Process Corner Simulations of Regenerative Latch Comparator

All the parameters of regenerative latch comparator for all four process corners are summarized in table 4.4.

**Table 4.4 Process corner simulation results of regenerative latch comparator.**

<b>Parameter</b>	<b>FF</b>	<b>SS</b>	<b>FS</b>	<b>SF</b>
Gain (dB)	82.7	83.56	83.26	83.28
Offset voltage( $\mu$ V)	80	90	90	90
Resolution( $\mu$ V)	10	10	10	10
Power dissipation( $\mu$ W)	640	533	596	571
Propagation delay( $\mu$ S)	0.945	1.056	1.949	0.992

## Chapter 5

### 3 ½ LCD Driver Circuitry

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A liquid crystal display (LCD) is a thin, flat electronic visual display uses the light modulating properties of liquid crystals (LCs). LCs do not emit light directly. LCDs therefore need a light source and are classified as "passive" displays. Some types can use ambient light such as sunlight or room lighting. There are many types of LCDs that are designed for both special and general uses. They are used in a wide range of applications including: computer monitors, television and instrument panel etc. They are common in consumer devices such as video players, gaming devices, clocks, watches, calculators, and telephones [25]. In most of the applications cathode ray tube (CRT) have replaced by LCDs. They are usually more compact, lightweight, portable, and lower cost. They are available in a wider range of screen sizes than CRT and other flat panel displays.

#### 5.1 Important Features of Liquid Crystal Display

- The first factor is size. An LCD consists primarily of two glass plates with some liquid crystal material between them. There is no bulky picture tube. This makes LCDs practical for applications where sizes (as well as weight) are important.
- In general, LCDs use much less power than their cathode-ray tube (CRT) counterparts. Many LCDs are reflective, meaning that they use only ambient light to illuminate the display. Even displays that do require an external light source (i.e. computer displays) consume much less power than CRT devices.

## 5.2 3 ½ LCD Display

In ISFET based pH meter the ISFET output is in analog form, so to see this output on the seven-segment LCD, there is a need of some components namely analog to digital converter, binary to BCD converter, BCD to seven segment decoder, manipulation circuitry and seven segment LCD display. A complete block diagram of 3 ½ LCD is shown in figure 5.1.

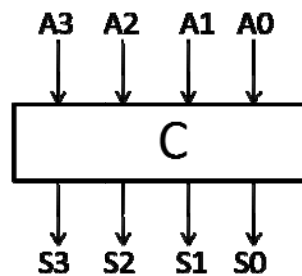
**Figure 5.1: Complete block diagram of 3 ½ LCD display.**

### 5.2.1 Binary to BCD Converter

To display any binary output on the seven segments LCD, there is a need to convert the ADC output to a BCD code. Any BCD code has 4-bit input and display only zero to nine outputs. Figure 5.2 shows the conversion of binary to BCD output.

**Table 5.1 Binary to BCD conversion.**

A3	A2	A1	A0	S3	S2	S1	S0
0	0	0	0	0	0	0	0
0	0	0	1	0	0	0	1
0	0	1	0	0	0	1	0
0	0	1	1	0	0	1	1
0	1	0	0	0	1	0	0
0	1	0	1	1	0	0	0
0	1	1	0	1	0	0	1
0	1	1	1	1	0	1	0
1	0	0	0	1	0	1	1
1	0	0	1	1	1	0	0
1	0	1	0	d	d	d	D
1	0	1	1	d	d	d	D
1	1	0	0	d	d	d	D
1	1	0	1	d	d	d	D
1	1	1	0	d	d	d	D
1	1	1	1	d	d	d	D



**Figure 5.2 (a): Block diagram of binary to BCD conversion (C).**

Where

**Figure 5.2(b): Block diagram of 10-bit binary to BCD converter.**

For a 10-bit binary input, a BCD has 13-bit output and these outputs are divided into units, tens, hundreds and thousands. Units, tens and hundreds have 4-bit but thousands has only 1-bit. When these are connected to LCD, units show the least significant position and thousands connected to the most significant position. In this application, LCD display has been designed to display the value of pH from 2 to 12. Seven segment decoder for units and tens are same but this is different for hundreds.

### 5.2.2 BCD to Seven Segment Decoder

BCD to Seven segment decoder for units is:

$$a0 = S0S1 + S3 + S0S2$$

$$b0 = \overline{S2} + (S0 \text{ xnor } S1)$$

$$c0 = S0 + \overline{S1} + S2$$

$$d0 = (\overline{S0}S1) + (\overline{S2}S0) + (S2\overline{S1}S0) + (S1\overline{S2}S3)$$

$$e0 = S0(S1 + \overline{S2})$$

$$f0 = S3 + (\overline{S0}S1) + (\overline{S1}S2) + (\overline{S0}S1S2)$$

$$g0 = (\overline{S0}S1) + S3 + (\overline{S1}S2) + (S1\overline{S2}S3)$$

BCD to Seven segment decoder for tens is:

$$a1 = (S4S5) + S7 + (S4S6)$$

$$b1 = \overline{S6} + (S4 \text{ xnor } S5)$$

$$c1 = S4 + \overline{S5} + S6$$

$$d1 = (\overline{S4}S5) + (\overline{S6}S4) + (S6\overline{S5}S4) + (S5\overline{S6}S7)$$

$$e1 = S4(S5 + \overline{S6})$$

$$f_1 = S_7 + (\overline{S_4S_5}) + (\overline{S_5S_6}) + (\overline{S_4S_5S_6})$$

$$g_1 = (\overline{S_4S_5}) + S_7 + (\overline{S_5S_6}) + (S_5\overline{S_6S_7})$$

BCD to Seven segment decoder for hundreds is:

$$a_h = (S_{11} \text{ xor } S_8) + (S_{10}S_9) + (\overline{S_{11}S_{10}S_9})$$

$$b_h = S_{11} + (\overline{S_{10}S_8}) + (\overline{S_9S_8}) + (S_9S_{10})$$

$$c_h = S_8 + S_9 + S_{10} + S_{11}$$

$$d_h = (\overline{S_8S_9}) + (S_8\overline{S_{10}S_{11}}) + (\overline{S_8S_9S_{10}})$$

$$e_h = (\overline{S_8S_9}) + (\overline{S_8S_9S_{10}})$$

$$f_h = S_9 + (\overline{S_8S_9S_{11}}) + (\overline{S_8S_9S_{10}})$$

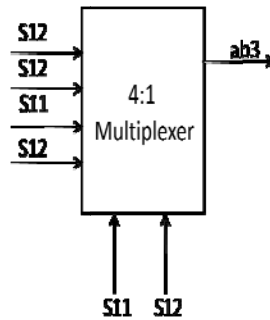
$$g_h = S_9 + (\overline{S_{10}S_{11}}) + (\overline{S_8S_9S_{10}})$$

### 5.2.3 Manipulation Circuitry

In the case of units and tens outputs of seven segment decoder are directly connected to seven segment LCD display but for hundreds and thousands outputs of seven segments are not directly connected to display. In these cases, some manipulation circuitry is required before connecting to display. The main component of this circuitry is multiplexer. Here some OR gates are needed to generate a Selection line.

**Figure 5.3(a): Manipulation circuitry for hundreds.**

BCD to Seven segment decoder for thousands is:



**Figure 5.3(b): Manipulation circuitry for thousands.**

After manipulation circuitry, we can get the desired output. Here three decimal points are available and we can activate any one of them according to application. In this case we will activate the second decimal point. It can display the values from 0 to 12.23 for 10-bit binary output of ADC. Here a0,b0,c0,d0,e0,f0,g0 and a1,b1,c1,d1,e1,f1,g1 are connected after decimal point (at LSB positions), a2,b2,c2,d2,e2,f2,g2 and ab3 are connected before decimal point.

# Chapter 6

## Conclusion and Future Work

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### 6.1 Conclusion

Most of the signal processing equipments are digital in nature and they work with the signal which can be represented in binary code. In biomedical applications, there is an increasing demand of ADCs with higher accuracy. Dual slope ADC is one of the valuable ADC for those purposes due to its high noise immunity, high resolving capability and low cost. In this thesis work, a 10-bit Dual slope Analog to digital convertor for ISFET based pH meter with 3 ½ LCD driver circuitry has been designed and simulated in 0.18  $\mu\text{m}$  CMOS technology using cadence tool. In this ADC design, the circuit does not require any DC external biasing circuit and only need to apply  $V_{DD}$  because all the voltage and current sources have been replaced by supply independent sources. The total power dissipation of dual slope ADC is only 1.25mW with 3.3V supply voltage.

A dual slope ADC consists of four component: Integrator, comparator, control logic and counter. In integrator design, an n-channel two stage op-amp with RC compensation has been taken in use. This op-amp provides DC gain of 72.5dB, phase margin of 61.3deg, power consumption of 523 $\mu\text{W}$ , ICMR from 1.1V to 3.2V and CMRR 112.72dB.

Comparator is an important block of ADC. In this ADC design, a regenerative latch comparator has been designed which consumes 581 $\mu\text{W}$  power while keeping the resolving ability 10 $\mu\text{V}$ . It has very low offset voltage of 90 $\mu\text{V}$  due to its high gain of 83.29dB with propagation delay of 817.1nS. It provides the ICMR from 0.3V to 3.3V.

A control logic for dual slope ADC has been designed using Melay based FSM. Full custom layout of all components has been designed and above mention parameters have also been calculated from layout by extracting it. These parameters are satisfactory but not similar.

In case of comparator, propagation delay is improved but the resolution and gain is decreased as compared to the values which we get from the schematic simulation.

To display the output on ADC, a 3 ½ LCD display driver circuitry has been designed which display the value of pH from 2 to 12.

## **6.2 Future Work**

In the Dual slope ADC linearity performance heavily depends on the Integrator. This dual slope ADC is only suitable for static value. To make it useful for continuous signal, a sample and hold circuitry will be taken in use.

For biomedical application resolution as well as power is main constraints. In All type of ADC, comparator is a foremost power consuming block. To improve the power dissipation, different type of clocked comparators will be designed which consume very low power in order of nW.

This Dual slope ADC will be designed as a configurable multi-mode Dual slope ADC. Configurability of the ADC in term of speed and resolution make this ADC well suited for application existing in the audio frequency range.

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