DESIGN OF LOW POWER CMOS CELL STRUCTURES BASED ON ADIABATIC SWITCHING PRINCIPLE

Thesis submitted towards the partial fulfillment of the requirements for the award of the degree of

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No human investigation can claim to be scientific
if doesn't pass the test of mathematical proof.

— *ALBERT EINSTEIN*

Do all the good you can,
By all the means you can,
In all the ways you can,
In all the places you can,
At all the times you can,
To all the people you can,
As long as ever you can,

— *JOHN WESLEY*

CERTIFICATE

I hereby certify that the work which is being presented in the thesis entitled " **DESIGN OF LOW POWER CMOS CELL STRUCTURES BASED ON ADIABATIC SWITCHING PRINCIPLE** ", in partial fulfillment of the requirements for the award of degree of **Master of Technology in VLSI Design & CAD** at **Thapar University, Patiala**, is an authentic record of my own work carried out under the supervision of **Ms. Alpana Agarwal**, Assistant Professor, Department of Electronics and Communication Engineering and refers other researcher's work which are duly listed in the reference section.

The matter embodied in this thesis has not been submitted for the award of any other degree of this or any other university.

Dated: 30th Jan. '2009.

(SANJAY KUMAR)

This is to certify that the above statement made by the candidate is correct and true to the best of my knowledge.

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Sanjay Kumar

Thapar University, Patiala,
India, 2009

To my wonderful
parents ξ parents-in-law,
for all the love they tried to give me

and

To all the people who loved me: you know who you are

ABSTRACT

The main objective of this thesis is to provide new low power solutions for Very Large Scale Integration (VLSI) designers. Especially, this work focuses on the reduction of the power dissipation, which is showing an ever-increasing growth with the scaling down of the technologies. Various techniques at the different levels of the design process have been implemented to reduce the power dissipation at the circuit, architectural and system level.

Furthermore, the number of gates per chip area is constantly increasing, while the gate switching energy does not decrease at the same rate, so the power dissipation rises and heat removal becomes more difficult and expensive. Then, to limit the power dissipation, alternative solutions at each level of abstraction are proposed.

The dynamic power requirement of CMOS circuits is rapidly becoming a major concern in the design of personal information systems and large computers. In this thesis work, a new CMOS logic family called *ADIABATIC LOGIC*, based on the adiabatic switching principle is presented. The term adiabatic comes from thermodynamics, used to describe a process in which there is no exchange of heat with the environment. The adiabatic logic structure dramatically reduces the power dissipation. The adiabatic switching technique can achieve very low power dissipation, but at the expense of circuit complexity. Adiabatic logic offers a way to reuse the energy stored in the load capacitors rather than the traditional way of discharging the load capacitors to the ground and wasting this energy.

This thesis work demonstrates the low power dissipation of Adiabatic Logic by presenting the results of designing various design/ cell units employing Adiabatic Logic circuit techniques. A family of full-custom conventional CMOS Logic and an Adiabatic Logic units for example, an inverter, a two-input NAND gate, a two-input NOR gate, a two-input XOR gate, a two-to-one multiplexer and a one-bit Full Adder were designed in Mentor Graphics IC Design Architect using standard TSMC 0.35 μm technology, laid out in Mentor Graphics IC Station.

All the circuit simulations has been done using various schematics of the structures and post-layout simulations are also being done after they all have been laid-out by considering all the basic design rules and by running the LVS program. Finally, the analysis of the average dynamic power dissipation with respect to the frequency and the load capacitance was done to show the amount of power dissipated by the two logic families.

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LIST OF SYMBOLS

α	Switching Activity [dimensionless]
C	Load Capacitance [Farads]
E	Energy [Joules]
f	Frequency of operation[Hz]
I_{stat}	Static Current [Amperes]
I_D	Drain Current [Amperes]
pwr	Power Clock [Volts]
P	Power [Watts]
Q	Charge [Coulombs]
R	Resistance [Ohms]
W/L	Aspect Ratio [µm/µm]
t	Time [s]
V_C	Capacitor Voltage [Volts]
V_{DD}	Supply Voltage [Volts]
V_S	Voltage swing of the signal [Volts]
V_{Tn}	Threshold Voltage of NMOS Transistor [Volts]
V_{Tp}	Threshold Voltage of PMOS Transistor [Volts]

NOMENCLATURE

CAL	Clocked Adiabatic Logic.
CMOS	Complementary Metal Oxide Semiconductor.
CVSL	Cascode Voltage Switch Logic.
ECL	Emitter Coupled Logic.
ECRL	Efficient Charge Recovery Logic.
EDP	Energy-Delay Product.
IC	Integrated Circuit.
NERL	NMOS Energy Recovery Logic.
NMOS	n- channel Metal Oxide Semiconductor.
PAL	Pass Transistor Adiabatic Logic.
PFAL	Positive Feedback Adiabatic Logic.
PMOS	p- channel Metal Oxide Semiconductor.
PPS CMOS	Pulse Power Supply CMOS.
SCAL	Source-coupled Adiabatic Logic.
SCRL	Split- Rail Charge Recovery Logic.
T-GATE	Transmission Gate.
TIPS	Tera Instructions per Second.
TSEL	True Single-Phase Adiabatic Logic.

TTL Transistor – Transistor Logic.

ULSI Ultra Large Scale Integration.

VLSI Very Large Scale Integration.

CHAPTER 1 INTRODUCTION

1.1 MOTIVATION

In the past few decades ago, the electronics industry has been experiencing an unprecedented spurt in growth, thanks to the use of integrated circuits in computing, telecommunications and consumer electronics. We have come a long way from the single transistor era in 1958 to the present day ULSI (Ultra Large Scale Integration) systems with more than 50 million transistors in a single chip [1].

The ever-growing number of transistors integrated on a chip and the increasing transistor switching speed in recent decades has enabled great performance improvement in computer systems by several orders of magnitude. Unfortunately, such phenomenal performance improvements have been accompanied by an increase in power and energy dissipation of the systems. Higher power and energy dissipation in high performance systems require more expensive packaging and cooling technologies, increase cost, and decrease system reliability. Nonetheless, the level of on-chip integration and clock frequency will continue to grow with increasing performance demands, and the power and energy dissipation of high-performance systems will be a critical design constraint.

For example, high-end microprocessors in 2010 are predicted to employ billions of transistors at clock rates over 30GHz to achieve TIPS (Tera Instructions per seconds) performance [1]. With this rate, high-end microprocessor's power dissipation is projected to reach thousands of Watts. This thesis investigates one of the major sources of the power/energy dissipation and proposes and evaluates the techniques to reduce the dissipation.

Digital CMOS integrated circuits have been the driving force behind VLSI for high performance computing and other applications, related to science and technology. The demand for digital CMOS integrated circuits will continue to increase in the near future, due to its important salient features like low power, reliable performance and improvements in the processing technology.

1.2 NEED FOR LOW POWER DESIGN

There are various interpretations of the *Moore's Law* that predicts the growth rate of integrated circuits. One estimate places the rate at 2X for every eighteen months. Others claim that the device density increases ten-fold every seven years. Regardless of the exact numbers, everyone agrees that the growth rate is rapid with no signs of slowing down. New generations of processing technology are being developed while present generation devices are at very safe distance from the fundamental physical limits. A need for low power VLSI chips arises from such evolution forces of integrated circuits. The Intel 4004 microprocessor, developed in 1971, had 2300 transistors, dissipated about 1 watts of power and clocked at 1 MHz. Then comes the Pentium in 2001, with 42 million transistors, dissipating around 65 watts of power and clocked at 2.40 GHz [1].

While the power dissipation increases linearly as the years go by, the power density increases exponentially, because of the ever-shrinking size of the integrated circuits. If this exponential rise in the power density were to increase continuously, a microprocessor designed a few years later, would have the same power as that of the nuclear reactor. Such high power density introduces reliability concerns such as, electromigration, thermal stresses and hot carrier induced device degradation, resulting in the loss of performance.

Another factor that fuels the need for low power chips is the increased market demand for portable consumer electronics powered by batteries. The craving for smaller, lighter and more durable electronic products indirectly translates to low power requirements. Battery life is becoming a product differentiator in many portable systems. Being the heaviest and biggest component in many portable systems, batteries have not experienced the similar rapid density growth compared to the electronic circuits. The main source of power dissipation in these high performance battery-portable digital systems running on batteries such as note-book computers, cellular phones and personal digital assistants are gaining prominence. For these systems, low power consumption is a prime concern, because it directly affects the performance by having effects on battery longevity. In this situation, low power VLSI design has assumed great importance as an active and rapidly developing field.

Another major demand for low power chips and systems comes from the environmental concerns. Modern offices are now furnished with office automation equipments that consume large amount of power. A study by *American Council for an Energy-Efficient Economy* estimated that office equipment account for 5% for the total US commercial energy usage in 1997 and could rise to 10% by the year 2004 if no actions are taken to prevent the trend [3].

1.3 THESIS ORGANIZATION

The primary goal of this thesis is to demonstrate a circuit level design approach, for use in designs which demand extreme low power dissipation.

This thesis is organized as follows:

CHAPTER I: INTRODUCTION. This chapter introduces power consumption issues in the area of VLSI. This chapter also summarizes the need of low power design in the today's era of scaling down of technologies and nanotechnology. Finally, this thesis chapter explains organization of the thesis.

CHAPTER 2: SOURCES OF POWER DISSIPATION AND REDUCTION OF ENERGY IN CMOS DIGITAL CIRCUITS. This chapter briefly introduces the different sources of power dissipation that occur in CMOS digital circuits and also the different techniques of reducing power dissipation in CMOS digital circuits and also the tools that have been used in this work.

CHAPTER 3: ADIABATIC SWITCHING – A CIRCUIT LEVEL APPROACH TO LOW – POWER VLSI DESIGN. This chapter explains the principle of adiabatic switching that emerges as a new approach to low power VLSI design. The different mathematical relations of achieving low power dissipation are considered, followed up by a simple circuit configuration of an adiabatic logic gate, noting the differences in the circuit topology of a complementary CMOS logic gate style and an adiabatic logic gate style. Also, considered are the power supplies that are to be used in an adiabatic circuit topology.

CHAPTER 4: OPERATIONAL AND STRUCTURAL DETAILS OF PRACTICAL ADIABATIC CIRCUITS. This chapter focuses on the operational and structural details

of the various practical adiabatic circuits. It presents a detailed account of the steps involved in the implementation of various designs based on adiabatic logic principle.

CHAPTER 5: DESIGN AND ANALYSIS LOW POWER CMOS CELL STRUCTURES. This chapter gives a detailed description of the various design and methodology used in the development of low-power cell structures at the VLSI Design and CAD Laboratory in Thapar University. The analysis and characterization of various combinational logic cells based on fully complementary CMOS logic style and adiabatic switching principle logic style are presented. The power dissipation analysis is done with the variations of both the power clock frequencies and the load capacitance.

CHAPTER 6: PHYSICAL LAYOUT DESIGN AND POST-LAYOUT SIMULATIONS. This chapter discusses the designs of different layouts for all the proposed structures, which are designed in Mentor Graphics IC Station TSMC 0.35 micron Technology and the Layout versus Schematic (LVS) program was executed to perform a comparison of the schematic to the physical layout.

CHAPTER 7: CONCLUSIONS AND FUTURE RESEARCH. This chapter summarizes the major accomplishments of this thesis and presents the scope for future and further research.

CHAPTER 2

SOURCES OF POWER DISSIPATION & REDUCTION OF ENERGY IN CMOS DIGITAL CIRCUITS

Power consumption is one of the basic parameters of any kind of integrated circuit (IC). Power and performance are always traded off to meet the system requirements. Power has a direct impact on the system cost. If an IC is consuming more power, then a better cooling mechanism would be required to keep the circuit in normal conditions. Otherwise, its performance is degraded and on continuous use it may be permanently damaged.

2.1 POWER AND ENERGY DEFINITIONS

It is important at this point, to distinguish between energy and power. The power consumed by a device is, by definition, the energy consumed per unit time. In other words, the energy (E) required for a given operation is the integral of the power (P) consumed over the operation time (T_{op}), hence,

$$E = \int_0^{T_{op}} P(t)dt \tag{2.1}$$

Here, the power of digital CMOS circuit is given by

$$P = C\, V_{DD}\, V_S\, f \tag{2.2}$$

where, C is the capacitance being recharged during a transition. V_{DD} is the supply voltage, V_s is the voltage swing of the signal, and f is the clock frequency. If it is assumed that an operation requires n clock cycles, T_{op} can be expressed as n / f. Hence, Equation (2.1) can be rewritten as

$$E = n\, C\, V_{DD}\, V_S \tag{2.3}$$

It is important to note that the energy per operation is independent of the clock frequency. Reducing the frequency will lower the power consumption but will not change the energy required to perform a given operation [1]. Since the energy consumption is what determines the battery life, it is imperative to reduce the energy rather than just the power. It is, however important to note that the power is critical for heat dissipation considerations.

2.2 OVERVIEW OF POWER DISSIPATION

It is more convenient to talk about power dissipation of digital circuits at this point. Although power depends greatly on the circuit style, it can be divided, in general, into static and dynamic power. The static power is generated due to the DC bias current, as is the case in transistor-transistor-logic (TTL), emitter-coupled logic (ECL), and N-type MOS (NMOS) logic families, or due to leakage currents. In all of the logic families except for the push-pull types such as CMOS, the static power tends to dominate. That is the reason why CMOS is the most suitable circuit style for very large scale integration (VLSI).

CMOS is the logic family preferred in many designs due to following reasons:-

(a) Impeccable noise margins.
(b) Perfect logic levels.
(c) Negligible static power dissipation.
(d) Gives good performance in most cases.
(e) Easy to get a functional circuits.
(f) Lot of tools available to automate the design process.

The power consumed when the CMOS circuit is in use can be decomposed into two basic classes: static and dynamic.

2.2.1 STATIC POWER

The static or steady state power dissipation of a circuit is expressed by the following relation [1]

$$P_{stat} = I_{stat} V_{DD} \tag{2.4}$$

where, I_{stat} is the current that flows through the circuit when there is no switching activity. Ideally, CMOS circuits dissipate no static (DC) power since in the steady state there is no direct path from V_{DD} to ground as PMOS and NMOS transistors are never on simultaneously. Of course, this scenario can never be realized in practice since in reality the MOS transistor is not a perfect switch. Thus, there will always be leakage currents and substrate injection currents, which will give to a static component of CMOS power dissipation. For a sub-micron NMOS device W/L = 10/ 0.5, the substrate injection current is of the order of 1- 100 μA for a V_{DD} of 5 V [2].

Another form of static power dissipation occurs for the so-called Ratioed logic. Pseudo-NMOS is an example of a Ratioed CMOS logic family. In this, the PMOS pull-up is always on and acts as a load device for the NMOS pull-down network. Therefore, when the gate output is in low-state, there is a direct path from V_{DD} to ground and the static currents flow. In this state, the exact value of the output voltage depends on the ratio of the strength of PMOS and NMOS networks – hence the name. The static power consumed by these logic families can be considerable. For this

reason, logic families such as this, which experience static power consumption, should be avoided for low-power design. With that in mind, the static component of power consumption in low-power CMOS circuits should be negligible and the focus shifts primarily to dynamic power consumption.

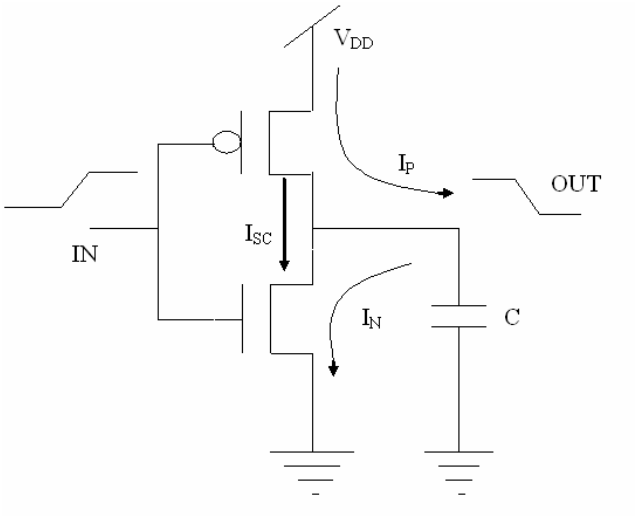


Fig. 2.1. CMOS Inverter for Power Analysis.

2.2.2 DYNAMIC POWER

The dynamic component of power dissipation arises from the transient switching behavior of the CMOS device. At some point during the switching transient, both the NMOS and PMOS devices will be turned on. This occurs for gate voltages between V_{tn} and V_{DD} - V_{tp} . During this time, a short-circuit exists between V_{DD} and ground and the currents are allowed to flow. A detailed analysis of this phenomenon by Veendrick reveals that with careful design of the transition edges, this component can be kept below 10-15% of the total power [2]; this can be achieved by keeping the rise and fall times of all the signals throughout the design within a fixed range (preferably equal). Thus, although short circuit dissipation cannot always be completely ignored, it is certainly not the dominant component of power dissipation in well-designed CMOS circuits. Instead, dynamic dissipation due to capacitance charging consumes most of the power. This

component of dynamic power dissipation is the result of charging and discharging of the parasitic capacitances in the circuit.

The situation is modeled in Figure 2.1, where the parasitic capacitances are lumped at the output in the capacitor C. Consider the behavior of the circuit over one full cycle of operation with the input voltage going from V_{DD} to ground and back to V_{DD} again. As the input switches from high to low, the NMOS pull-down network is cut-off and PMOS pull-up network is activated charging load capacitance C up to V_{DD}. This charging process draws energy equal to CV_{DD}^2 from the power supply. Half of this is dissipated immediately in the PMOS transistors, while the other half is stored on the load capacitance. Then, when the input returns to V_{DD}, the process is reversed and the capacitance is discharged, its energy being in the NMOS network. In summary, every time a capacitive node switches from ground to V_{DD} (and back to ground), energy of CV_{DD}^2 is consumed.

This leads to the conclusion that CMOS power consumption depends on the *switching activity* of the signals involved. We can define *activity*, α as the expected number of zero to one transition per data cycle. If this is coupled with the average data rate, f, which may be the clock frequency in a synchronous system, then the effective frequency of nodal charging is given the product of the activity and the data rate: αf. This leads to the following formulation for the average CMOS power consumption:

$$P_{dyn} = \alpha C V_{DD}^2 f \tag{2.5}$$

This classical result illustrates that the dynamic power is proportional to the switching activity, capacitive loading and the square of the supply voltage. In CMOS circuits, this component of power dissipation is by far the most important accounting for at least 90% of the total power dissipation [2].

So, to reduce the power dissipation, the circuit designer can minimize the switching event, decrease the node capacitance, reduce the voltage swing or apply a combination of these methods. Yet, in all these cases, the energy drawn from the power supply is used only once before being dissipated. To increase the energy efficiency of the logic circuits, other measures can be introduced for recycling the energy drawn from the power supply.

A novel class of logic circuits called ADIABATIC LOGIC offers the possibility of further reducing the energy dissipated during the switching events and the possibility of recycling or reusing some of the energy drawn from the power supply [3]. To accomplish this goal, the circuit topology and the operating principle have to be modified, sometimes drastically. The amount of energy recycling achievable using adiabatic techniques is also determined by the fabrication technology, switching speed and the voltage swing.

2.3 ENERGY-DELAY PRODUCT: A METRIC FOR LOW ENERGY DESIGN

The scaling of V_{DD} is beneficial from the energy point of view but may have serious side effects on the delay. This implies that using the energy as the metric is not sufficient. Horowitz et al. [4] have proposed an alternative which accounts for both energy and delay by using the product of the ENERGY PER OPERATION and the DELAY PER OPERATION. This metric can be used as the basis for design optimization and comparison between different systems.

To minimize the energy-delay product (*EDP*), we need to consider the trends of CMOS scaling and its implications on the delay. The delay of CMOS circuit will most probably increase as the supply voltage increases. This is illustrated below in Figure 2.2. It also shows the energy as a function of V_{DD}.

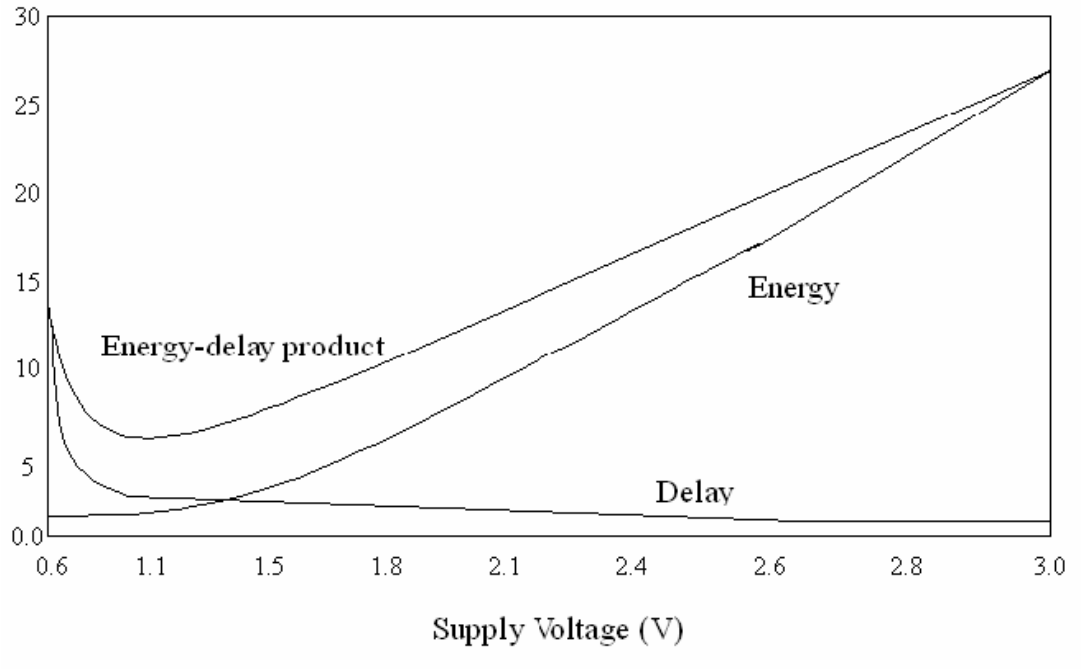


Fig. 2.2. Normalized delay, energy and energy-delay product vs. supply voltage. Delay is normalized to delay value at largest supply voltage (3.0 V), and Energy is normalized to energy value at smallest supply voltage (0.6 V).

The product of the energy and the delay, which is also shown in the same figure, demonstrates the trade-off between the delay and the energy. For low supply voltages, the energy is minimum but the delay is not. Increasing the supply voltage may improve the speed but at the expense of the energy. The *EDP* is a metric that accounts for both and can be used to compare different processes. The closer the minimum of the energy-delay curve to the 1-*V* supply, the better the process is. The optimum supply voltage can also be determined from the *EDP*.

Now, so far we have discussed the energy consumption in digital CMOS circuits. In this section, we would look at the means of reducing the energy/ power in digital CMOS circuits and systems.

2.4 REDUCTION OF POWER SUPPLY

The energy and power consumed by the CMOS digital circuits are sensitive to the power supply voltage as given by:

$$E = CV_{DD}^2 \tag{2.6}$$

$$P = CV_{DD}^2 f \tag{2.7}$$

Reducing the power supply voltage is an efficient approach to lower the energy and power. The power supply voltage is actually the most crucial factor in reducing energy/ power. This will, however, be at the expense of the delay of the circuits. Using the *EDP* as a metric, one can derive the optimum supply voltage that would yield minimum *EDP*.

To simplify the analysis, it will be assumed that the saturation current of deep submicro-meter MOSFETs is proportional to $(V_{GS}\text{-}V_T)^{\alpha}$ [5]. Assuming $V_{GS} = V_{DD}$ (for maximum current) and using the delay expression, it can be shown that the delay becomes $KV_{DD}/ (V_{DD}\text{-}V_T)^{\alpha}$, where K is a constant independent of V_{DD}. The *EDP* can hence be expressed as

$$E \times t_d = const \frac{V_{DD}^3}{(V_{DD} - V_T)^{\alpha}} \tag{2.8}$$

The optimum supply voltage (for minimum *EDP*) can be found from Equation (2.7) and is given by

$$V_{DD(opt)} = \frac{3V_T}{(3-\alpha)} \tag{2.9}$$

The above expression is valid for long-channel and deep sub micrometer devices. For long-channel transistors ($\alpha = 2$), the optimum supply voltage is equal to $3V_T$, which agrees with the result of the analysis presented in [6]. For deep sub micrometer devices with α closer to unity the

optimum voltage is expected to be less than $3V_T$. For example, if $\alpha = 1.5$, then $V_{DD(opt)} = 2V_T$. At any rate, the optimum value for V_{DD} is proportional to the threshold voltage.

So, the conclusion is that the supply voltage must be reduced to minimize the *EDP*. Scaling the supply voltage below the point of minimum *EDP* will cause severe degradation in the delay. The second point is that the optimum supply voltage is related to the threshold voltage.

2.5 REDUCTION OF SWITCHING ACTIVITY

In the previous section, the method for minimizing dynamic power consumption in CMOS digital integrated circuits by supply voltage scaling has been discussed. Another approach to low-power design is to reduce the switching activity and the amount of the switched capacitance to the minimum level required to perform a given task. The measures to accomplish this goal can range from optimization of algorithm to logic design, and finally to physical mask design.

2.5.1 SWITCHING ACTIVITY REDUCTION

Switching activity in CMOS digital integrated circuits can be reduced by algorithmic optimization, architecture optimization, logic topology and circuit optimization. Each of these aspects will be discussed briefly as below [7].

(a) ALGORITHMIC OPTIMIZATION. Algorithmic Optimization depends heavily on the application and on the characteristics of the data, such as the dynamic range, the correlation, statistics of the data transmission and so on. Some of the techniques apply only to applications such as digital Signal Processing (DSP) and cannot be used for general-purpose processing.

(b) ARCHITECTURE OPTIMIZATION. Several architectural techniques have been proposed to reduce the switching activity, such as, ordering of the input signals [7] and delay path balancing to remove glitching. In multi-level logic circuits, the propagation delay from one logic block to the next can cause spurious signal transitions or glitches, as a result of critical races or dynamic hazards. In general, if all input signals of a gate change simultaneously, no glitching occurs. But a dynamic hazard or glitch can occur if input signals change at different times. Thus, a node can exhibit multiple transitions in a single clock cycle before settling to the correct logic level.

2.6 REDUCTION OF SWITCHED CAPACITANCE

The amount of switched capacitance plays a significant role in the dynamic power dissipation of the circuit as is given by Equation (2.5). Hence, the reduction of this parasitic capacitance is a major goal for low-power design of digital integrated circuits. The switching capacitance can be broken down into two categories, the capacitance in dense logic (which includes the transistor parasitic and wire capacitances at the output of the gates) and the capacitances of the busses and a clock network (which is mainly the wire capacitance). In some systems, the capacitance of the busses and a clock network may comprise close to 50% of the overall chip capacitance [7]. An example of such system is the Alpha chip.

At the system level, one of the approaches to reduce the switched capacitance is to limit the use of shared resources. A simple example is the use of a global bus structure for the data transmission between a large numbers of operational modules [6].

The type of logic style used to implement a digital circuit also affects the physical capacitance of the circuit. The physical capacitance is a function of the number of transistors that are required to implement a given function. For example, one approach to reduce the physical capacitance is to

use transfer gates over conventional CMOS logic gates to implement logic functions. Pass-gate logic design is attractive since fewer transistors are required for certain functions such as XOR and XNOR. In many arithmetic operations where binary adders and multipliers are used, pass transistor logic offers significant advantages. Similarly, multiplexers and other key building blocks can also be simplified using deign style.

The amount of parasitic capacitance that is switched (i.e., charged up or charged down) during operation can also be reduced at the physical design level, or mask level. Designing a logic gate with minimum-size transistors certainly affects the dynamic performance of the circuit, and this trade-off between dynamic performance and power dissipation should be carefully considered in critical circuits. Consequently, a standard-cell based design may have considerable overhead in terms of switched capacitance in each cell.

CHAPTER 3

ADIABATIC SWITCHING - A CIRCUIT LEVEL APPROACH TO LOW POWER VLSI DESIGN

The popularity of complementary MOS technology can be mainly attributed to inherently lower power dissipation and high levels of integration. However, the current trend towards ultra low-power has made researchers search for techniques to recover/ recycle energy from the circuits. In the early days, researchers largely focused on the possibility of having physical machines that consume almost zero energy while computing and tried to find the lower bound of energy consumption.

In conventional level-restoring CMOS logic circuits with rail-to-rail output voltage swing, each switching event causes an energy transfer from the power supply to the output node or from the output node to the ground. During a 0-to-V_{DD} transition of the output, the total output charge $Q = C_{load} V_{DD}$ is drawn from the power supply at a constant voltage. Thus, an energy of $E_{supply} = C_{load} V_{DD}^2$ is drawn from the power supply during this transition. Charging the output node capacitance to the voltage level V_{DD} means that at the end of the transition, the amount of stored energy in the output node is $E_{stored} = C_{load} V_{DD}^2 / 2$. Thus, half of the injected energy from the power supply is dissipated in the PMOS network while only one half is delivered to the output node. During a subsequent

V_{DD} -to- 0 transition of the output node, no charge is drawn from the power supply and the energy stored in the load capacitance is dissipated in the NMOS network.

To reduce the dissipation, the circuit designer can minimize the switching events, decrease the node capacitance, reduce the voltage swing, or apply a combination of these methods. Yet in all these cases, the energy drawn from the power supply is *used* only once before being dissipated. To increase the energy efficiency of the logic circuits, other measures can be introduced for *recycling* the energy drawn from the power supply. A novel class of logic circuits called *adiabatic logic* offers the possibility of further reducing the energy dissipated during the switching events, and the possibility of recycling, or reusing, some of the energy drawn from the power supply. To accomplish this goal, the circuit topology and the operation principles have to be modified, sometimes drastically. The amount of energy recycling achievable using adiabatic techniques is also determined by the fabrication technology, switching speed, and the voltage swing.

3.1 PRINCIPLE OF ADIABATIC SWITCHING

The word *ADIABATIC* comes from a Greek word that is used to describe thermodynamic processes that exchange no energy with the environment and therefore, no energy loss in the form of dissipated heat. In real-life computing, such ideal process cannot be achieved because of the presence of dissipative elements like resistances in a circuit. However, one can achieve very low energy dissipation by slowing down the speed of operation and only switching transistors under certain conditions. The signal energies stored in the circuit capacitances are recycled instead, of being dissipated as heat. The adiabatic logic is also known as *ENERGY RECOVERY CMOS* [3].

It should be noted that the fully adiabatic operation of the circuit is an ideal condition which may only be approached asymptotically as the switching process is slowed down. In most practical cases, the energy dissipation associated with a charge transfer event is usually composed of an adiabatic component and a non-adiabatic component. Therefore, reducing all the energy loss to zero may not possible, regardless of the switching speed. With the adiabatic switching approach, the circuit energies are conserved rather than dissipated as heat. Depending on the application and the system requirements, this approach can sometimes be used to reduce the power dissipation of the digital systems.

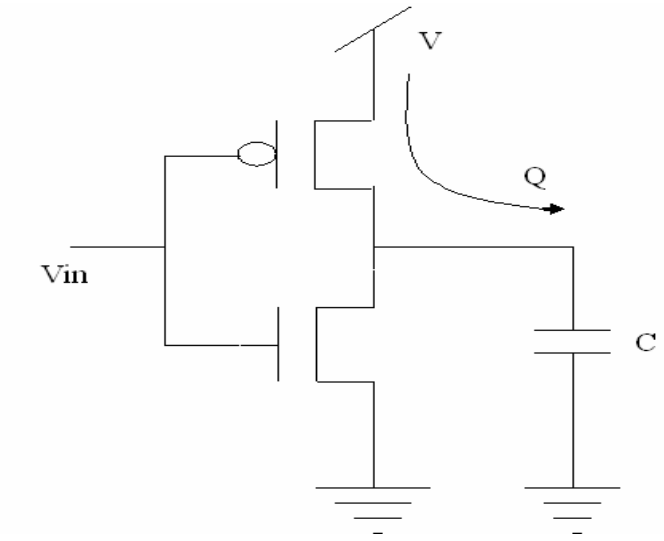


Figure 3.1. (a)

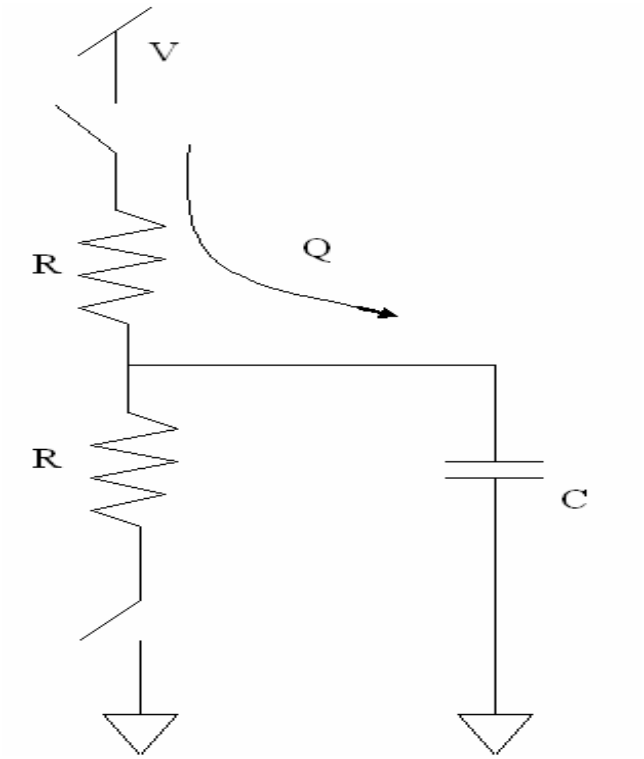


Figure 3.1. (b)

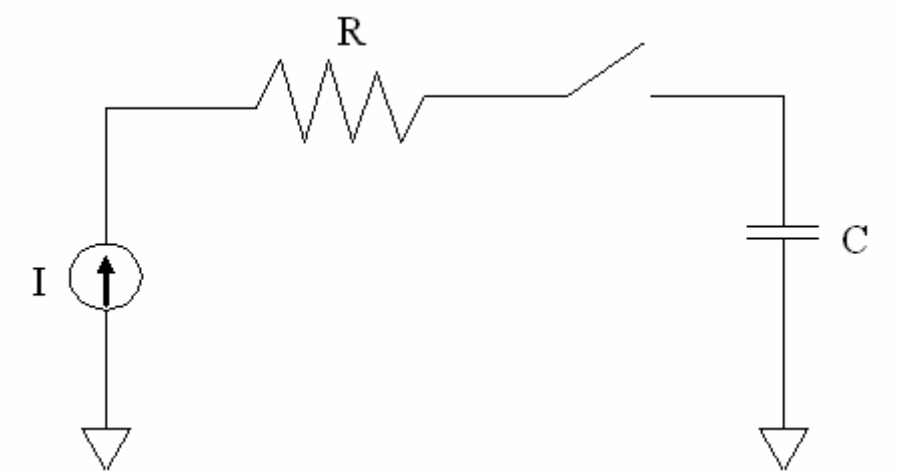


Figure 3.1. (c) Circuit explaining Adiabatic Switching.

Here, the load capacitance is charged by a constant-current source (instead of the constant-voltage source as in the conventional CMOS circuits).

Here, R is the resistance of the PMOS network. A constant charging current corresponds to a linear voltage ramp. Assume, the capacitor voltage V_C is zero initially [12].

$\therefore$ The voltage across the switch = IR

$P(t)$ in the switch = I^2R

$\therefore$ Energy during charge = $(I^2R)\,T$ (3.1)

Also, $\because I = \dfrac{CV}{T} \Rightarrow T = \dfrac{CV}{I}$ (3.2)

$$\therefore E = \left(I^2R\right)T = \left(\frac{CV}{T}\right)^2 RT = \frac{C^2V^2R}{T}$$

Hence, $E = E_{diss} = \left(\dfrac{RC}{T}\right)CV^2 = \left(\dfrac{2RC}{T}\right)\left(\dfrac{1}{2}CV^2\right)$ (3.3)

where, the various terms of Equation (3.3) are described as follows:

E — energy dissipated during charging,

Q — charge being transferred to the load,

C — value of the load capacitance,

R — resistance of the MOS switch turned on,

V — final value of the voltage at the load,

T — time spent for charging.

Now, a number of observations can be made based on Equation (3.3) as follows:

(i) The dissipated energy is smaller than for the conventional case, if the charging time T is larger than $2RC$. That is, the dissipated energy can be made arbitrarily small by increasing the charging time,

(ii) Also, the dissipated energy is proportional to R, as opposed to the conventional case, where the dissipation depends on the capacitance and the voltage swing. Thus, reducing the on-resistance of the PMOS network will reduce the energy dissipation.

3.1.1 ENERGY DISSIPATION IN TRANSISTOR CHANNEL USING AN *RC* MODEL

Let us consider a simple RC model to compute the energy dissipation in a transistor channel while working in the linear region. Consider a PMOS pass transistor, as shown in Fig. 3.3. When the voltage at the power/ clock terminal swings from 0 to V_{DD} to charge node capacitance through a transistor channel, there is a voltage drop (and hence energy dissipation) in the channel due to the channel resistance. The RC model representing such a phenomenon is shown in Figure 3.2. Let us consider the amount of energy dissipated when charging capacitance C from 0 to V_{DD} in time T with a linear power supply voltage of Figure 3.2 (b). We have

$$RC\left(\frac{dV_C}{dt}\right)+V_C=\Phi \tag{3.4}$$

where

$$\Phi=\begin{cases}0 & t<0\\ \left(\frac{V_{DD}}{T}\right)t & 0\le t<T\\ V_{DD} & t\ge T\end{cases}$$

The solution of the above equation is given by

$$V_C = \begin{cases} 0 & t < 0 \\ \Phi - \left(\frac{RC}{T}\right) V_{DD}(1 - e^{-t/RC}) & 0 \le t < T \\ \Phi - \left(\frac{RC}{T}\right) V_{DD}\left(1 - e^{-T/RC}\right) e^{-(t-T)/RC} & t \ge T \end{cases} \tag{3.5}$$

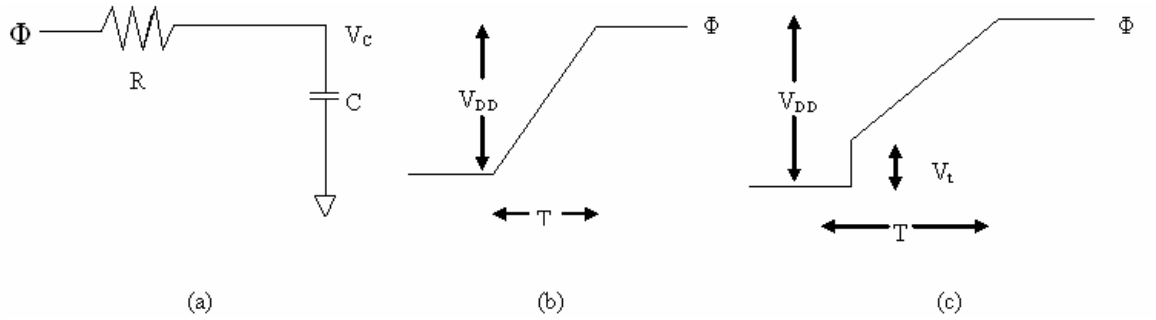


Figure 3.2. An *RC* model.

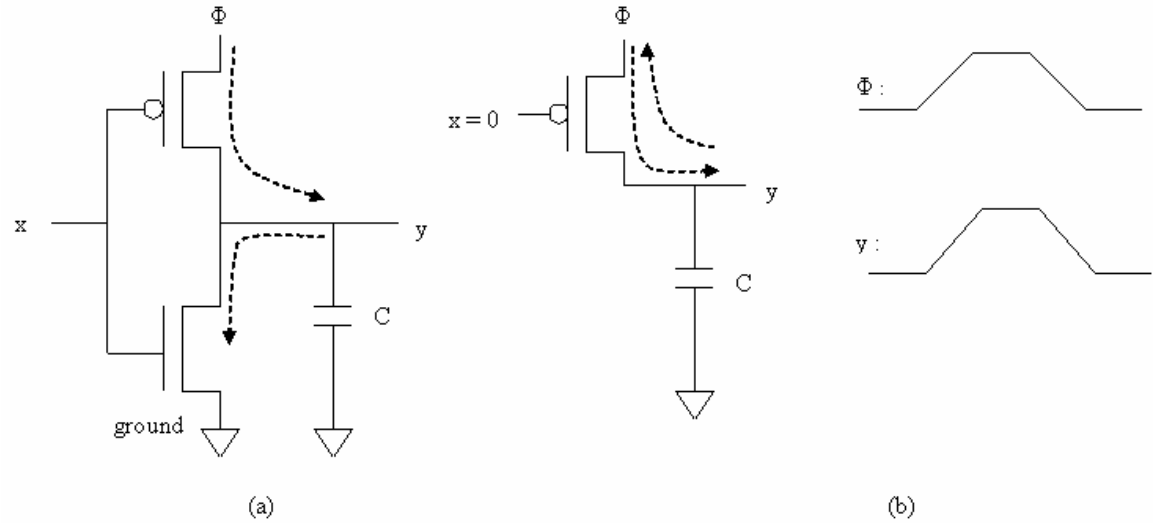


Figure 3.3 Basic Recovery Process.

The energy dissipation in the above charging process can be calculated as follows [23]:

$$E_{linear} = \int_0^{\infty} iV_R\,dt = \int_0^{T} iV_R\,dt + \int_T^{\infty} iV_R\,dt \tag{3.7}$$

The first term of Equation (3.7) can be written as

$$\int_0^T iV_R\,dt = \int_0^T \frac{(\Phi - V_C)^2}{R}\,dt$$

$$= \int_0^T \frac{\left[(V_{DD}/T)RC\left(1 - e^{-t/RC}\right)\right]^2}{R\,dt}$$

$$= \frac{R^2C^2}{T^2} C V_{DD}^2 \int_0^{T/RC} (1 - e^{-t/RC})^2\, d\left(\frac{t}{RC}\right)$$

$$= \left(\frac{RC}{T}\right) C V_{DD}^2 \left[1 - \frac{3}{2}\left(\frac{RC}{T}\right) + 2\left(\frac{RC}{T}\right)e^{-T/RC} - \frac{1}{2}\left(\frac{RC}{T}\right)e^{-2T/RC}\right] \tag{3.8}$$

And the second term can be written as

$$\int_T^{\infty} iV_R\,dt = \int_T^{\infty} \frac{(\Phi - V_C)^2}{R}\,dt$$

$$= \frac{RC}{T^2} C V_{DD}^2 (1 - e^{-T/RC})^2 \int_T^{\infty} e^{-2[(t-T)/RC]}\,dt$$

$$= \left(\frac{RC}{T}\right)^2 C V_{DD}^2 \left[\frac{1}{2}(1 - e^{-T/RC})^2\right] \tag{3.9}$$

Finally we have

$$E_{linear} = \left(\frac{RC}{T}\right) C V_{DD}{}^2 \left(1 - \frac{RC}{T} + \frac{RC}{T} e^{-T/RC}\right) \tag{3.10}$$

Let us consider the two extreme cases.

When $T \gg RC$

$$E_{linear} = \left(\frac{RC}{T}\right) C V_{DD}{}^2 \tag{3.11}$$

and when $T \ll RC$, as in normal CMOS,

$$E_{linear} = \left(\frac{RC}{T}\right) C V_{DD}{}^2 \left\{1 - \frac{RC}{T} + \frac{RC}{T}\left[1 - \frac{T}{RC} + \frac{1}{2}\left(\frac{T}{RC}\right)^2\right]\right\} \tag{3.12}$$

$$= \frac{1}{2} C V_{DD}{}^2 \tag{3.13}$$

It is clear from Equation (3.3) that the energy dissipation through the dissipative medium can be made arbitrarily small by making the transition time T arbitrarily large. This observation also points to the fact that for low-power dissipation, a MOS device (or switch) should not be turned on unless the potential across it is zero or a switch should not be disabled if current is flowing through it. The response voltage V_C over time is shown in Figure 3.4 (a) and the dissipated energy versus RC / T is shown in Figure 3.4 (c).

3.1.2. ENERGY DISSIPATION FROM NON-LINEAR MECHANISM

The above analysis ignores the threshold voltage drop of a transistor. Let us consider Figure 3.2 (c). When the voltage drop Φ at the power terminal swings from 0 to V_{DD} (as shown in the figure) to charge the node capacitance, the PMOS transistor does not turn on until Φ exceeds the threshold voltage V_{th}. There is voltage drop $V_{DS} \approx V_{\text{th}}$ between the drain and source ends when the transistor jumps from the cut-off region to the linear region, which results in the energy dissipation. Since an amount of CV_{th} charge is required the voltage to the V_{th} level, the energy loss due to the threshold voltage can be approximated by

$$E_{\text{th}} \approx \frac{1}{2} C V_{\text{th}}^2 \tag{3.14}$$

Due to the channel resistance, there is still a small voltage drop (and hence energy dissipation) in the channel when the transistor works in the linear region. We use E_{linear} to represent this amount of energy loss.

Let us use the model shown in Figure 3.2 (c) to calculate the energy dissipation. Let us consider charging C from 0 to V_{DD} in time T with the linear power supply voltage of Figure 3.2 (c) (note that the power supply voltage shown in the figure considers the effect of transistor threshold voltage drop). We have

$$RC\left(\frac{dV_C}{dt}\right) + V_C = \Phi \tag{3.15}$$

where Φ is shown in Figure 3.2 (c). The solution of the above equation is given by

$$V_C = \begin{cases} 0 & t < t_0 \\ \Phi - \left(\frac{RC}{T}\right) V_{DD}(1 - e^{(t-t_0)/RC}) + V_{th} e^{-(t-t_0)/RC} & 0 \le t_0 < t < T \\ \Phi - \left(\frac{RC}{T}\right) V_{DD}(1 - e^{-(T-t_0)/RC}) e^{-(t-T)/RC} - V_{th} e^{-(t-t_0)/RC} & t \ge T \end{cases} \quad (3.16)$$

where, $t_0 = (V_{th} / V_{DD})\, T$.

The energy dissipation in the above charging process can be calculated [23] as follows:

$$E_{dissipated} = \int_0^{\infty} i V_R \, dt = \int_0^{T} i V_R \, dt + \int_T^{\infty} i V_R \, dt \quad (3.17)$$

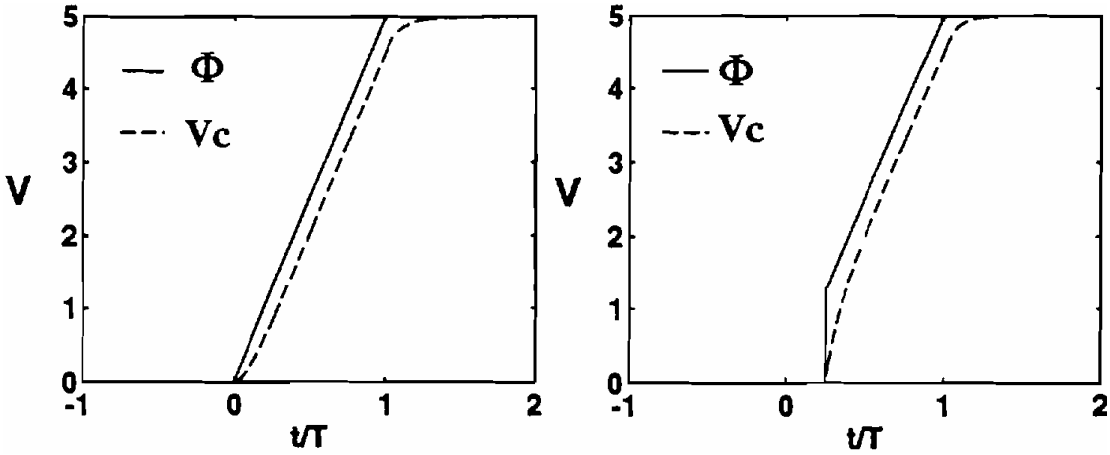
The above equation results in

$$E_{dissipated} = \frac{1}{2} C V_{th}^2 + \left(\frac{RC}{T}\right) C V_{DD}^2 \left(1 - \frac{RC}{\beta T} + \frac{RC}{\beta T} e^{-\beta T/RC}\right) + \left(\frac{RC}{T}\right) C V_{th} V_{DD} \left(\frac{RC}{\beta T} - e^{-\beta T/RC} - \frac{RC}{\beta T} e^{-\beta T/RC}\right)$$

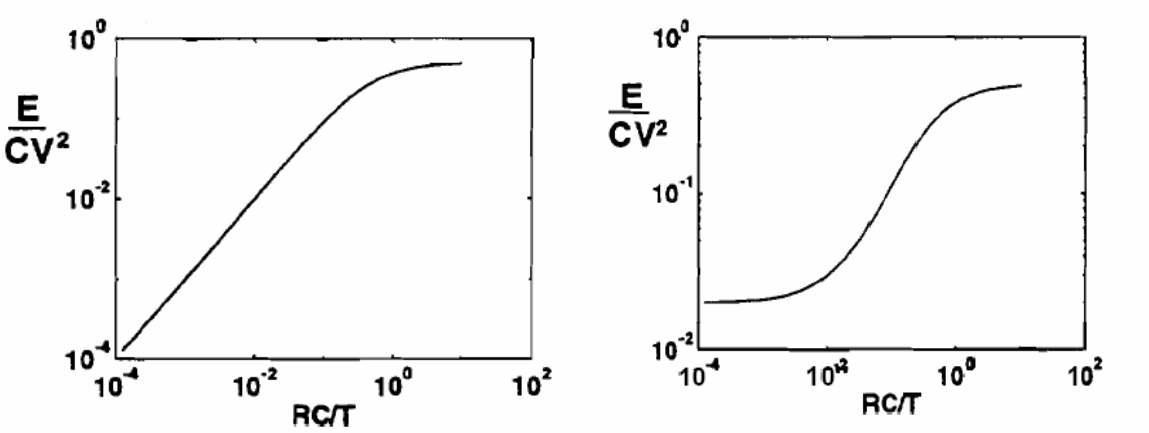
$$= \left(\frac{RC}{T}\right) C V_{DD}^2 + \frac{1}{2} C V_{th}^2 + O\left(\left(\frac{RC}{T}\right)^2\right)$$

$$\approx E_{linear} + E_{non-linear} \quad (3.18)$$

where $\beta = 1 - (V_{th} / V_{DD})$, $E_{linear} = (RC / T)\, C\, V_{DD}^2$, and $O((RC / T)^2)$ represents all other terms of the order of $(RC / T)^2$, which are very small for the energy recovery circuits.



(a) Voltage at RC / T = 0.1 **(b) Voltages at RC / T = 0.1**



(c) Power Dissipation in RC model **(d) Power Dissipation with a Threshold Voltage**

Figure 3.4 Linear and Non-linear Power Dissipation with the RC model [24].

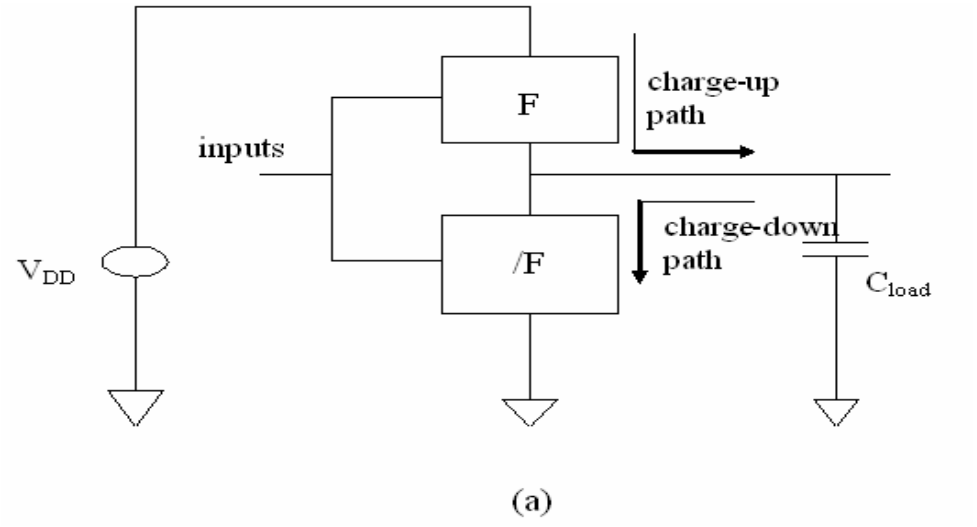
Figure 3.4 (b) and 3.4 (d) show the exact solutions of this RC model with the threshold voltage.

Assume $V_{\text{th}} = 1.2$ V and $V_{DD} = 5$ V; then we have $\left(\frac{1}{2}CV_{th}^{2}\right)\Big/\left(\frac{1}{2}CV_{DD}^{2}\right) = 0.0576$.

Discharging consumes the same amount of energy, and hence, 11.50 % of energy is consumed due to the non-linear mechanism (i.e., the threshold voltage). Since this non-linear dissipation is independent of the transition time, it dominates the power consumption when the operating frequency is low, while linear dissipation is more significant in the higher frequency region.

3.2 A SIMPLE ADIABATIC LOGIC GATE

In the following, we will examine simple circuit configurations which can be used for adiabatic switching. Figure 3.2 shows a general circuit topology for the conventional CMOS gates and adiabatic counterparts. To convert a conventional CMOS logic gate into an adiabatic gate, the pull-up and the pull-down networks must be replaced with complementary transmission-gate (T-gate) networks. The T-gate network implementing the pull-up function is used to drive the true output of the adiabatic gate, while the T-gate network implementing the pull-down function drives the complementary output node. Note that all the inputs should also be available in complementary form. Both the networks in the adiabatic logic circuit are used to charge-up as well as charge-down the output capacitance, which ensures that the energy stored at the output node can be retrieved by the power supply, at the end of each cycle. To allow adiabatic operation, the DC voltage source of the original circuit must be replaced by a pulsed-power supply with the ramped voltage output.



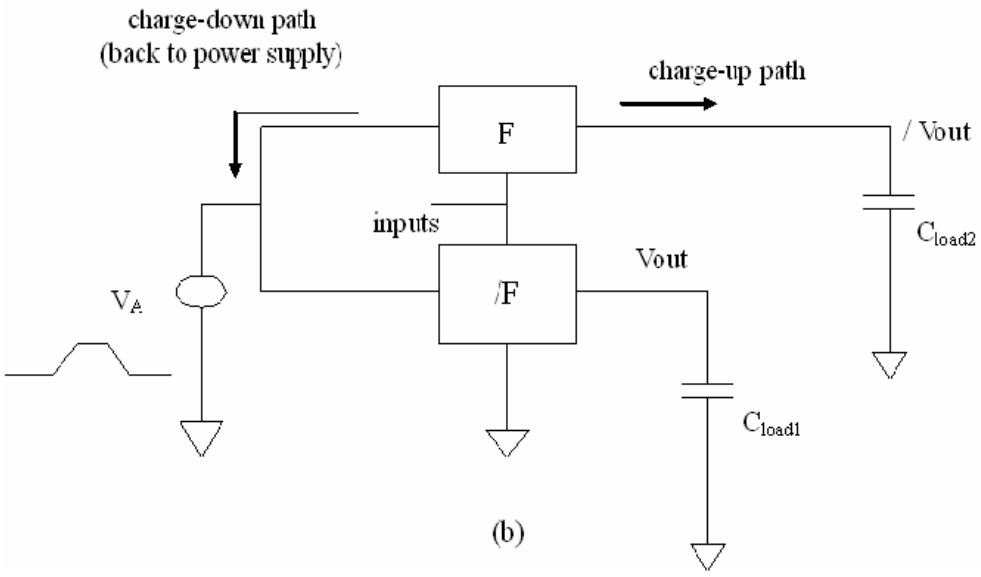


Figure 3.5. (a) The general circuit topology of a conventional CMOS Logic Gate.
(b) The topology of an Adiabatic Logic Gate implementing the same function. Note the difference in charge-up and charge-down paths for the output capacitance.

Note the circuit modifications which are necessary to convert a conventional CMOS logic circuit into an adiabatic logic circuit increase the device count by a factor of two or even more [6].

3.3 ADIABATIC COMPUTING

The energy CV_{DD}^2, which is consumed in the conventional CMOS circuits, is unavoidable since the charge is transferred from the supply and returned to the ground [9]. The current drawn from the supply during a $0 \rightarrow 1$ transition is relatively large because of the large drain-source voltage. If, however, the supply voltage can be varied in a manner that would reduce the drain current, the energy will be significantly reduced. This can be achieved by using adiabatic circuits. Consider the circuit shown in the Figure 3.3. This circuit is sometimes refereed to as a pulse power supply CMOS (or PPS CMOS) [9].

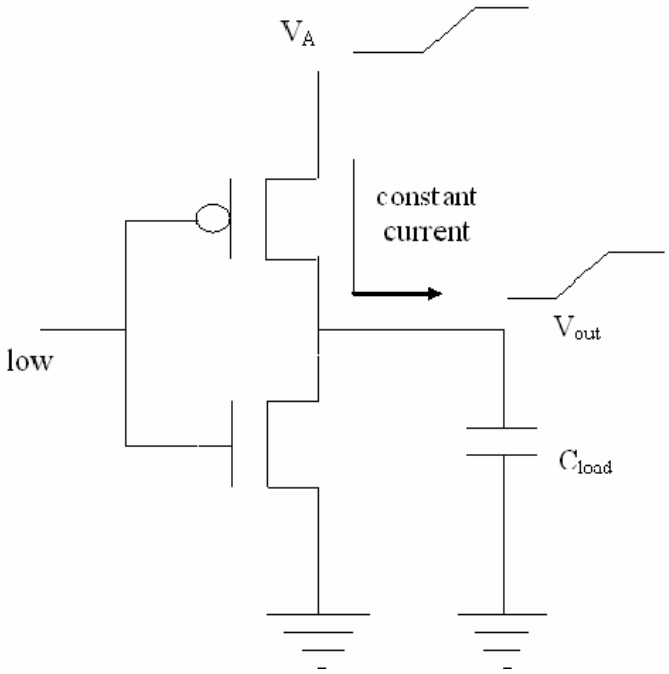


Figure 3.6. Schematic of (Adiabatic) PPS CMOS Inverter [9].

Its topology is very similar to that of the conventional CMOS inverter, except that its supply is driven with a pulsed supply waveform ω.

Let us assume, the input is low and that the output (*out*) was initially low.

With the V_{DD} being low, the drain current = 0.

Now, as the voltage supply V_{DD} ramps up, the output follows the supply voltage V_{DD}.

The drain-to-source voltage is always small and so is the current drawn from the supply.

The adiabatic logic circuit is also known as PULSED POWER SUPPLY (PPS) CMOS.

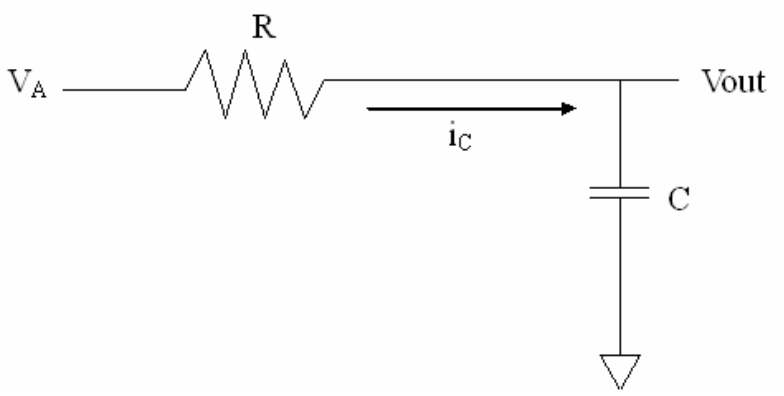


Figure. 3.7. The *RC* model of PPS CMOS Inverter.

Assume that the supply is increasing in steps from 0 to V_{DD}.

Let us first derive the energy per step as follows [11]⇒

Between the i^{th}-step and the next one, the supply voltage changes from V_i to V_{i+1}.

$$I_D = I = C\frac{dV_0}{dt} = \frac{\left(V_{i+1} - V_0\right)}{R} \tag{3.19}$$

Solving this differential equation from $t = t_i$ (when the supply switches to V_{i+1}) to any time $t < t_{i+1}$, we get the following expression for the output voltage as a function of time.

$$V_0 = V_{i+1} - \left(\frac{V_{DD}}{n}\right)e^{-t/RC} \tag{3.20}$$

Here, n is the number of step supply voltage.

Now, substitute from Equation (3.20) into Equation (3.19), we obtain the current expression, which is then used for the derivation of the energy consumed per step $\Rightarrow$

$$E_{step} = \int_0^\infty I^2 R dt = \int_0^\infty \left(\frac{V_{DD}}{nR} e^{-t/RC} \right)^2 R dt$$

$$\Rightarrow \therefore E_{step} = \frac{1}{n^2} \left(\frac{1}{2} C V_{DD}{}^2 \right) \tag{3.21}$$

Thus, the energy consumed for one operation in nE_{step}.

$\therefore$ Theoretically, if n is infinite (i.e., the V_{DD} is a slow ramp), the energy goes to zero.

$$\therefore E_{total} = nE_{step} = \left(\frac{1}{n^2} \right) \left(\frac{1}{2} C V^2 \right) \tag{3.22}$$

The PPS-CMOS can be used for the complex Boolean function implementation.

Hence, the adiabatic circuits are operable only much lesser speeds comparable to SCMOS circuits. Another disadvantage is the requirement of a special type of power supply.

3.4 POWER SUPPLIES FOR ADIABATIC CIRCUITS

The design of a power clock generator is an important part of the whole adiabatic system design. Many studies on adiabatic logic design have been made and various approaches have been proposed. All of them require extra circuitry for one or more time- varying power sources to provide extended charging time. There are methods such as those using either inductive power supplies, step-wise charging through banks of capacitance tanks, or resonant drivers, etc.

3.4.1. PHASES IN AN ADIABATIC POWER SUPPLY

The constant-current source needed for the adiabatic operation is usually a trapezoidal or, sinusoidal voltage source. In an adiabatic circuit, the power supply also acts as a clock. Hence, it is given the term "power clock". A single-phase sinusoidal power-clock can easily be generated using resonant circuits.

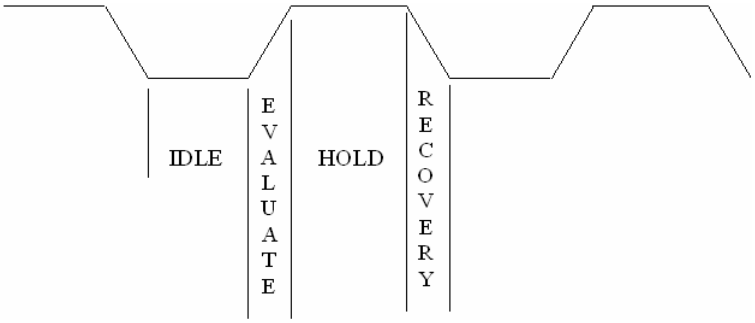


Figure 3.8. Phases in an Adiabatic Power Supply [11].

Figure 3.8 above shows a trapezoidal voltage waveform, which acts as an adiabatic power supply. The four phases of the clock are also shown [11].

Initially, the adiabatic supply is in the IDLE / WAIT phase and the supply voltage is LOW maintaining at the same time the outputs in the LOW state. Then the inputs are set (one goes LOW the other HIGH) and the supply voltage ramps-up. As the inputs are evaluated, the outputs change complementary to each other and the one that goes HIGH follows the power supply until it reaches V_{DD}. At that moment the inputs are returned to the LOW state and after a certain period of time in the HOLD "1" phase, the supply ramps down with the outputs following until the LOW state is reached again. That is, to say, during the IDLE/ WAIT phase, the circuit idles. In the EVALUATE phase, the load

capacitance either charges up or does not, depending upon the inputs to the functional blocks. In the HOLD phase, the output is kept at steady, so that the subsequent stage can evaluate. Finally, in the RECOVERY/ RESET phase, the charge held on the capacitance is recovered.

Any digital system with multiple stages/ cascades based upon the described adiabatic power clocking scheme must have at least four clocks, each leading its previous phase by 90° [11]. Practical adiabatic circuits use sinusoidal power clock. This is an approximation of the trapezoidal waveform with the duration of the hold phase tending to zero.

3.4.2. DESIGN OF AN ADIABATIC POWER SUPPLY

The adiabatic power supply needs an efficient energy recovery design which implies quality factor Q of the power supply to be very high. Not only the Q should be high, it should be proportional to the cycle time so that the energy dissipation in the power supply should also decrease with the frequency. Otherwise, dissipation in the power supply itself will dominate the logic circuit dissipation at lower frequencies. Most preferable technique is to use sinusoidal voltage supply because of its ease to design as compared to the pure trapezoidal wave.

The constant current charging needed can be approximated using a sinusoidal power supply. To account for the non-constant charging current, the dissipation of Equation (3.3) must be multiplied by a constant shape factor ξ (which takes the value $\pi^2 / 8$ for a sine-shaped current). The sinusoidal power supply can be realized using an external inductor. Thus an LC resonant circuit with a resonance frequency of approximately $1/\sqrt{LC}$ is created and the energy is oscillated between the external inductor and the capacitances to be switched.

In inductor based approach [21] energy can be circulated between electrostatic field in the load capacitor and magnetic field in the off-chip inductor. Analysis of this approach [21] shows that by applying sinusoidal ramp, energy saved in the circuit is reduced by the factor of $\pi^2 / 8$ compared to pure trapezoidal wave and the total energy consumption including the power supply is given by

$$E_{\sin usoidal} = C_L V_{dd}{}^2 \left(\pi \sqrt{\frac{\tau_s}{T}} + \frac{\pi^2 \tau_c}{8T} \right) \tag{3.23}$$

where τ_c and τ_s are the time constants of circuit branches of computing part and supply part of the system respectively.

The energy dissipation E_{diss} results for three popular charging waveforms: a step, a linear ramp, and a sine wave are summarized below in Table 3.1.

As it is seen from the Table 3.1, the step input shows the typical ½ CV^2 dissipation. The linear voltage ramp is the most efficient adiabatic source because it is constant current. When the charging time T approaches infinity, the dissipation approaches zero. The sine wave, adjusted to resonate between 0 and V volts with a charging time of T, has been used in place of a linear ramp [11] [16] because it is simple to generate with a resonating inductor and capacitor circuit. The sine is much more efficient than a step input if the period is sufficiently slow, but only $8/\pi^2$ or 81% efficient compared to a ramp with the same rise time.

TABLE 3.1.

THE EFFICIENCY OF THREE POPULAR CHARGING WAVEFORMS.

Source	E_{diss}	
V step (t)	$\int_0^{\infty} \left(V e^{-t/RC} \right)^2 R \, dt$	$\frac{1}{2} CV^2$
V ramp(t) : $I_s = \frac{CV}{T}$	$\int_0^{T} I_s^2(t) R dt$	$\frac{RC}{T} CV^2$
$\frac{V}{2}\left[\sin\left(\frac{\pi}{T} t - \frac{T}{2} \right) + 1 \right]$	$\int_0^{T} \left(\frac{VT^2 \pi C \left(T \sin\left(\frac{\pi t}{T} \right) - RC\pi \cos\left(\frac{\pi t}{T} \right) \right)}{2T^4 + 2\pi^2 R^2 C^2 T^2} \right)^2 R dt$	$\frac{\pi^2}{8} \frac{RC}{T} CV^2$

Thus, adiabatic charging is achieved when a charging waveform is more efficient than $\frac{1}{2}CV^2$ such as with the ramp or sine waveforms. Energy recovery is achieved when some of the $\frac{1}{2}CV^2$ of energy stored on the charged capacitive load is recovered and reused for later charging.

Thus, it is often simpler to reduce the voltage, V, or reduce the switched capacitance, C, in order to save power. However when the limits of C and V have been reached (or they are fixed), adiabatic charging proves to be the powerful tool for reducing the dissipation below $\frac{1}{2}CV^2$.

CHAPTER 4

OPERATIONAL & STRUCTURAL DETAILS OF PRACTICAL ADIABATIC CIRCUITS

A limiting factor for the exponentially increasing integration of microelectronics is represented by the power dissipation. Though CMOS technology provides circuits with very low static power dissipation, during the switching operation currents are generated, due to the discharge of load capacitances that cause a power dissipation increasing with the clock frequency. The adiabatic technique prevents such losses: the charge does not flow from the supply voltage to the load capacitance and then to ground, but it flows back to a trapezoidal or sinusoidal supply voltage and can be reused. Just losses due to the resistance of the switches needed for the logic operation still occur. In order to keep these losses small, the clock frequency has to be much lower than the technological limit.

In the literature, a multitude of adiabatic logic families are proposed [13] - [18]. Each different implementation shows some particular advantages, but there are also some basic drawbacks for these circuits. The following paragraphs below will deal with these different adiabatic logic families. Let’s see the details about each of these.

4.1 DIFFERENT ADIABATIC LOGIC FAMILIES

Practical adiabatic families can be classified as either PARTIALLY ADIABATIC or FULLY ADIABATIC [12]. In a PARTIALLY ADIABATIC CIRCUIT, some charge is allowed to be transferred to the ground, while in a FULLY ADIABATIC CIRCUIT, all the charge on the load capacitance is recovered by the power supply. Fully adiabatic circuits face a lot of problems with respect to the operating speed and the inputs power clock synchronization.

Popular Partially Adiabatic families include the following:

i. Efficient Charge Recovery Logic (ECRL).
ii. 2N-2N2P Adiabatic Logic.
iii. Positive Feedback Adiabatic Logic (PFAL).
iv. NMOS Energy Recovery Logic (NERL).
v. Clocked Adiabatic Logic (CAL).
vi. True Single-Phase Adiabatic Logic (TSEL).
vii. Source-coupled Adiabatic Logic (SCAL).

Some Fully adiabatic logic families include:

i. Pass Transistor Adiabatic Logic (PAL).
ii. Split- Rail Charge Recovery Logic (SCRL).

4.2 EFFICIENT CHARGE – RECOVERY LOGIC (ECRL)

Efficient Charge – Recovery Logic (ECRL) proposed by Moon and Jeong [13], shown in Figure 4.1, uses cross-coupled PMOS transistors. It has the structure similar to Cascode Voltage Switch Logic (CVSL) with differential signaling.

It consists of two cross-coupled transistors *M1* and *M2* and two NMOS transistors in the N-functional blocks for the ECRL adiabatic logic block [13].

An AC power supply *pwr* is used for ECRL gates, so as to recover and reuse the supplied energy. Both *out* and */out* are generated so that the power clock generator can always drive a constant load capacitance independent of the input signal. A more detailed description of ECRL can be found in [13]. Full output swing is obtained because of the cross-coupled PMOS transistors in both precharge and recover phases. But due to the threshold voltage of the PMOS transistors, the circuits suffer from the non-adiabatic loss both in the precharge and recover phases. That is, to say, ECRL always pumps charge on the output with a full swing. However, as the voltage on the supply clock approaches to $|V_{tp}|$, the PMOS transistor gets turned off.

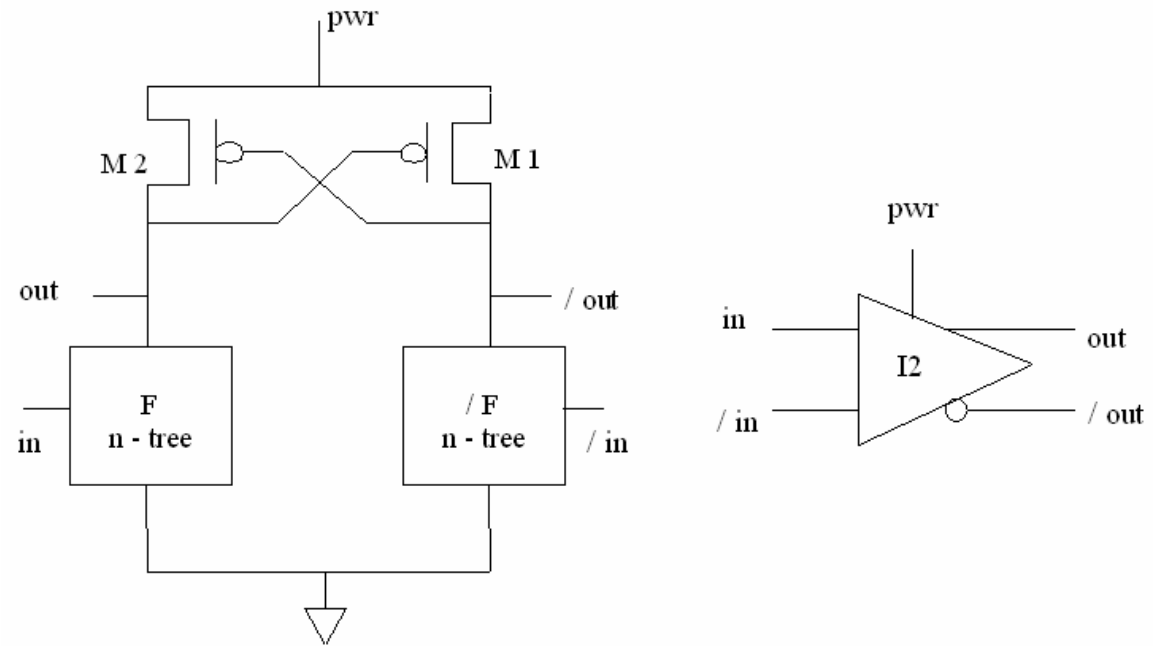


Figure 4.1. The Basic Structure of the Adiabatic ECRL Logic.

So the recovery path to the supply clock to the supply clock is disconnected, thus, resulting in incomplete recovery. V_{tp} is the threshold voltage of PMOS transistor. The amount of loss is given as

$$E_{ECRL} = C|V_{tp}|^2 / 2 \quad (4.2)$$

Thus, from Equation (4.2), it can be inferred that the non-adiabatic energy loss is dependent on the load capacitance and independent of the frequency of operation.

The ECRL circuits are operated in a pipelining style with the four-phase supply clocks. When the output is directly connected to the input of the next stage (which is a combinational logic), only one phase is enough for a logic value to propagate. However, when the output of a gate is fed back to the input, the supply clocks should be in phase. A latch is one of the simplest cases which have a feedback path. The input signals propagate to the next stage in a single phase, and the input values are stored in four phases (1-clock) safely.

Let us assume *in* is at high and *inb* is at low. At the beginning of a cycle, when the supply clock '*pwr*' rises from zero to V_{DD} , *out* remains at a ground level, because *in* turns on F-tree (NMOS logic tree). */out* follows *pwr* through *M1*. When *pwr* reaches $V_{DD,}$ the outputs hold valid logic levels. These values are maintained during the *hold* phase and used as inputs for the evaluation of the next stage. After the *hold* phase, *pwr* falls down to a ground level, */out* node returns its energy to *pwr* so that the delivered charge is recovered. Thus, the clock *pwr* acts as both a clock and power supply.

A major disadvantage of this circuit is the existence of the coupling effects, because the two outputs are connected by the PMOS latch and the two complementary outputs can interfere each other.

4.3 2N-2N2P ADIABATIC LOGIC

This was proposed as a modification to ECRL logic, in order to reduce the coupling effects. Figure 4.2 shows the general schematic of the 2N-2N2P logic. The 2N-2N2P logic [14] uses a cross-coupled latch of two PMOSFETs and two NMOSFETs (*M1-M4*), as shown in the Figure 4.2, instead of only two NMOSFETs as in ECRL logic family. The N-functional block is in parallel with NMOSFETs of the latch and thus occupies additional area, but the primary advantage of 2N-2N2P over ECRL is that the cross-coupled NMOSFETS switches result in non-floating outputs for large part of the recovery phase.

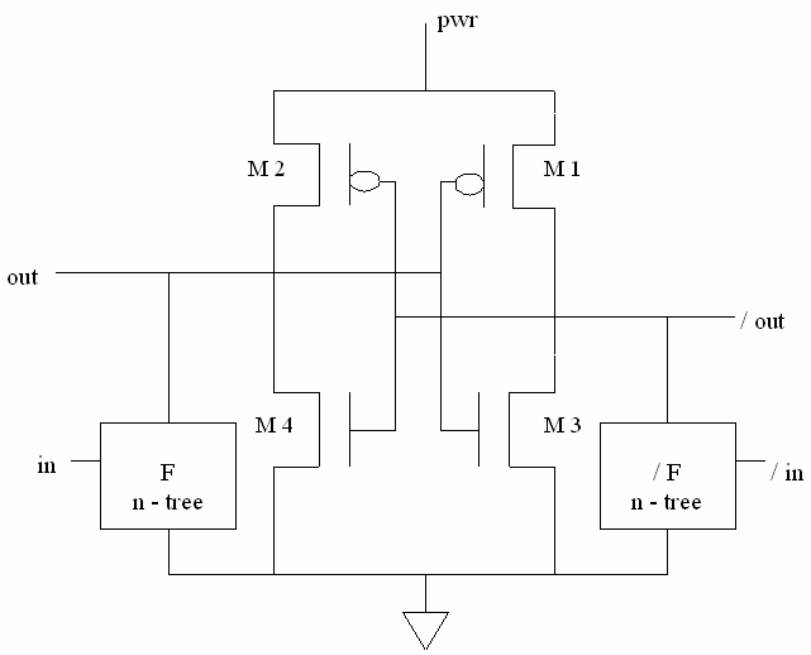


Figure 4.2. The Basic Structure of the Adiabatic 2N-2N2P Logic.

The 2N-2N2P uses two cross-coupled PMOS transistors for both pre-charge and recovery, thus its energy loss per cycle is given by the following expression [14].

$$E_{2N-2N2P} = \left(\frac{2R_P C_L}{T} \right) C_L V_{DD}{}^2 + C_L V_{TP}{}^2 \quad (4.3)$$

Where, C_L is the load capacitance, R_P is the turn-on resistance of PMOS transistors, T is the transition time of the power-clock, and V_{TP} is the threshold of PMOS transistors. In Equation (4.3), the first term represents full-adiabatic energy loss, which can be reduced by lowering the operation frequency, and the second term represents non-adiabatic energy loss, which is independent of operation frequency. From Equation (4.3), it can be seen that the non-adiabatic loss is dependent on the load capacitance. A more detailed description of 2N-2N2P adiabatic logic family can be found in [14].

4.4 POSITIVE FEEDBACK ADIABATIC LOGIC (PFAL)

The partial energy recovery circuit structure named Positive Feedback Adiabatic Logic (PFAL) [15] has been used, since it shows the lowest energy consumption if compared to other similar families, and a good robustness against technological parameter variations. It is a dual-rail circuit with partial energy recovery. The general schematic of the PFAL gate is shown in Figure 4.3. The core of all the PFAL gates is an adiabatic amplifier, a latch made by the two PMOS *M1-M2* and two NMOS *M3-M4*, that avoids a logic level degradation on the output nodes *out* and */out*. The two n-trees realize the logic functions. This logic family also generates both positive and negative outputs. The functional blocks are in parallel with the PMOSFETs of the adiabatic amplifier and form a transmission gate. The two n-trees realize the logic functions. This logic family also generates both positive and negative outputs.

The two major differences with respect to ECRL are that the latch is made by two PMOSFETs and two NMOSFETS, rather than by only two PMOSFETs as in ECRL logic, and that the functional blocks are in parallel with the transmission PMOSFETs. Thus the equivalent resistance is smaller when the capacitance needs to be charged. The

energy dissipation by the CMOS Logic family and Adiabatic PFAL Logic family can be seen as in Figure 4.4.

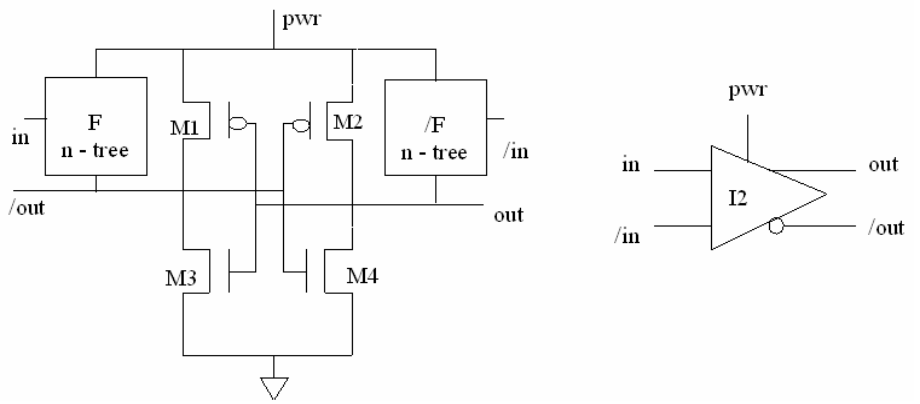


Figure 4.3. The Basic Structure of the Adiabatic PFAL Logic.

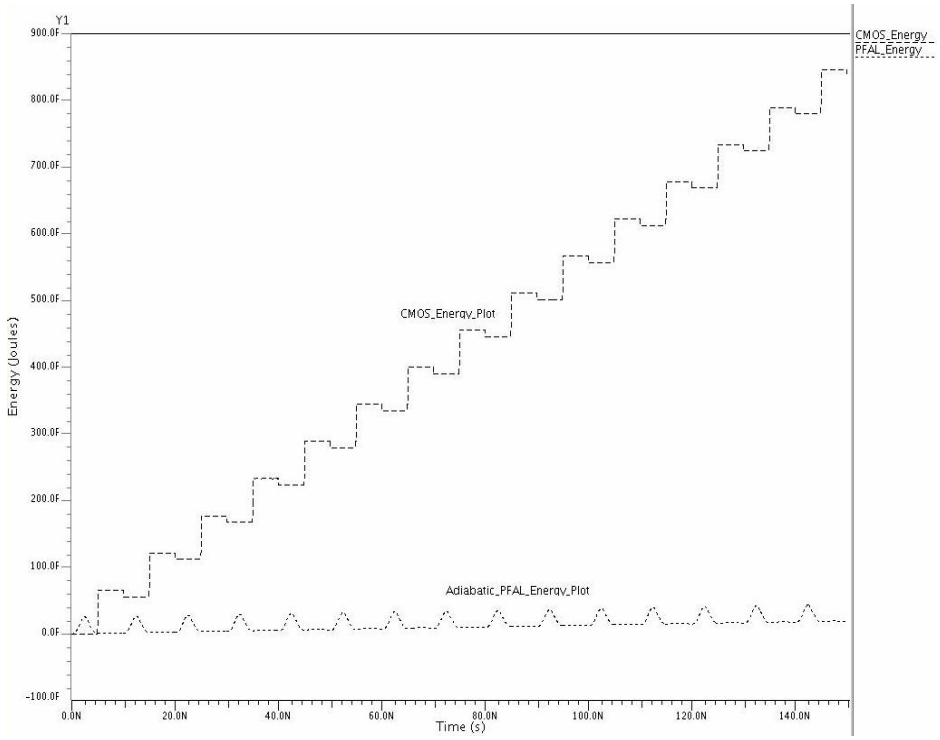


Figure 4.4. Comparison of the Energy Dissipation by CMOS Logic and an Adiabatic PFAL Logic (Simulated with ELDO Simulator of Mentor Graphics Corporation, in Standard TSMC 0.35 *μm* Technology).

PFAL uses a four-phase power-clock *pwr* ø (t) as shown in Figure 3.7: ø (t) rises from 0 to V_{DD} in the EVALUATE PHASE (*E*) and supplies energy to the circuit, then ø (t) returns to 0 in the RECOVERY PHASE (*R*) and the energy flows back from the circuit to the power-clock generator; the HOLD PHASE (*H*) and the IDLE PHASE (*I*) are needed for cascading gates.

4.5 CLOCKED ADIABATIC LOGIC (CAL)

CAL is a dual-rail logic that operates from a single-phase AC power-clock supply [17]. In the adiabatic mode, the power-clock supply waveform is generated using an on-chip switching transistor and a small external inductor between the chip and a low-voltage dc supply.

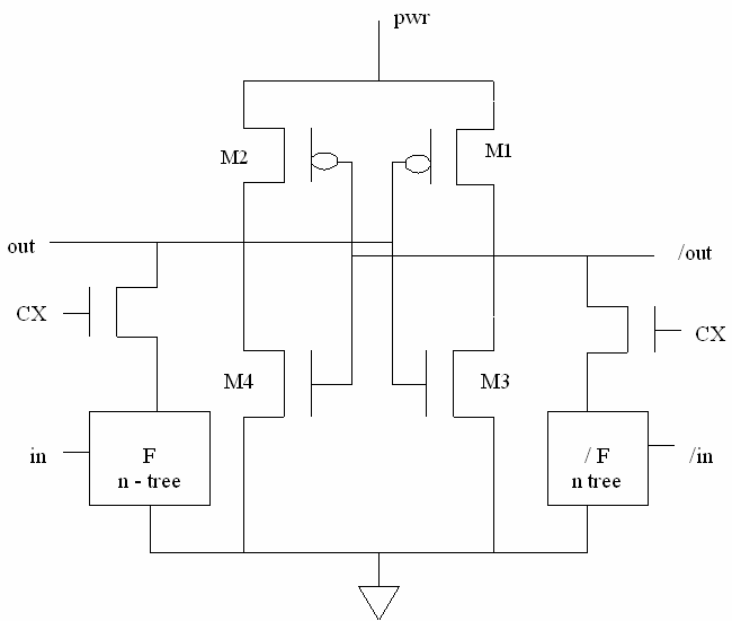


Figure 4.5 The Basic Structure of the Adiabatic CAL Logic.

The basic CAL gate, the inverter, is shown in Fig. 4.4. Cross-coupled CMOS inverters, transistors *M1 – M4*, provide memory function. In order to realize an adiabatic inverter and other logic functions with a single power clock, we introduced auxiliary timing

control clock signal *CX*, as shown in above Figure 4.4. This signal controls the transistors that are in series with the logic trees represented by the functional blocks *F* and */F*. The *CX*-enabled devices allow operation with a single power clock *pwr*.

CHAPTER 5

DESIGN AND ANALYSIS OF LOW POWER CMOS CELL STRUCTURES

All the design structures based on CMOS Logic and Adiabatic Switching Logic are designed and simulated using standard TSMC 0.35 μm CMOS technology and 3.3 V voltage supply at an operating temperature of 27º C. Mentor Graphics Corporation based tool known as IC Design Architect have been used for all the design and analysis. The basic cells, for example, Inverter, Two-Input NAND Gate, Two-Input NOR Gate, Two-Input Exclusive-OR Gate, Two-to-One Multiplexer, One-Bit Full Adder are designed and analyzed with appropriate sizing. The SPICE BSIM 3v3 Version 3.1 MOS Model parameters are given in Appendix A.

5.1 DESIGN AND SIMULATION FOR A CMOS INVERTER

The first basic cell which the VLSI designers implements and analyze is the basic CMOS Inverter. Here also this thesis work starts with the designing of the basic CMOS Inverter of minimum transistor size. The standard TSMC 0.35 μm CMOS technologies have been

used and a load capacitance of 4 *fF* is used. The transient analysis is done by use of the ELDO Simulator of Mentor Graphics Corporation. The basic structure of a CMOS Inverter is shown in Figure 5.1.

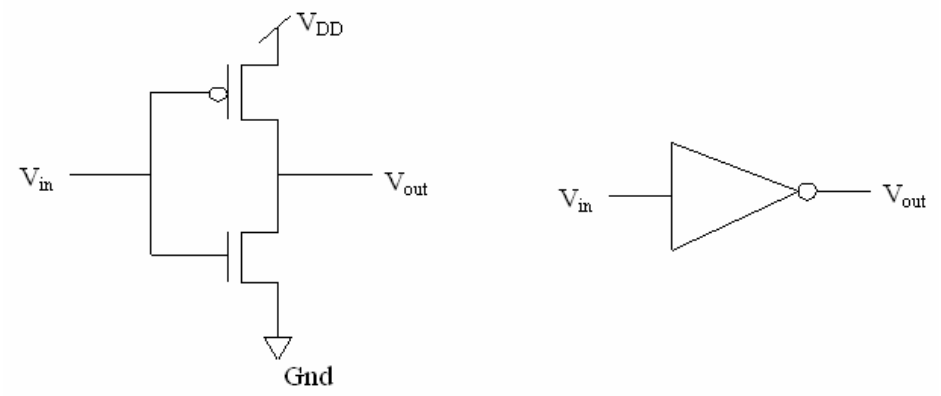
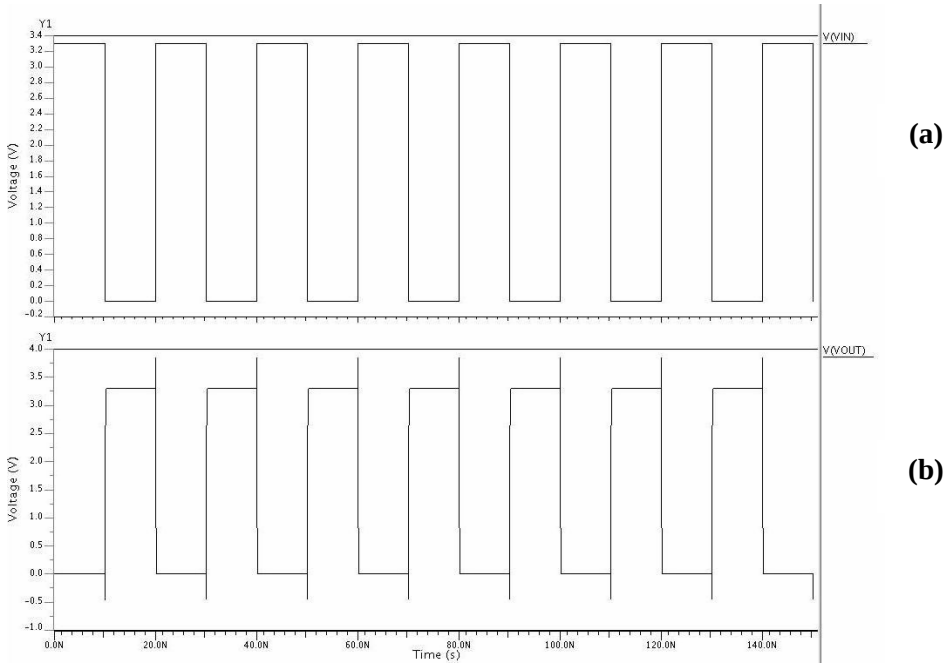


Figure 5.1. The Basic Structure of CMOS Inverter.

The transient simulation results are as shown in the Figure 5.2 below.



(a)

(b)

Figure 5.2. Simulation Results of CMOS Inverter:
(a) Input Signal,
(b) Voltage Waveform of Output Signal.

5.2 DESIGN AND SIMULATION FOR A TWO-INPUT CMOS NAND GATE

The next basic cell to consider is the CMOS-based Two-Input NAND Gate, designed and simulated in the standard TSMC 0.35 μm CMOS Technology and with a load capacitance of 5 fF. The minimum sized NMOS and PMOS transistors have been used for the transient simulations.

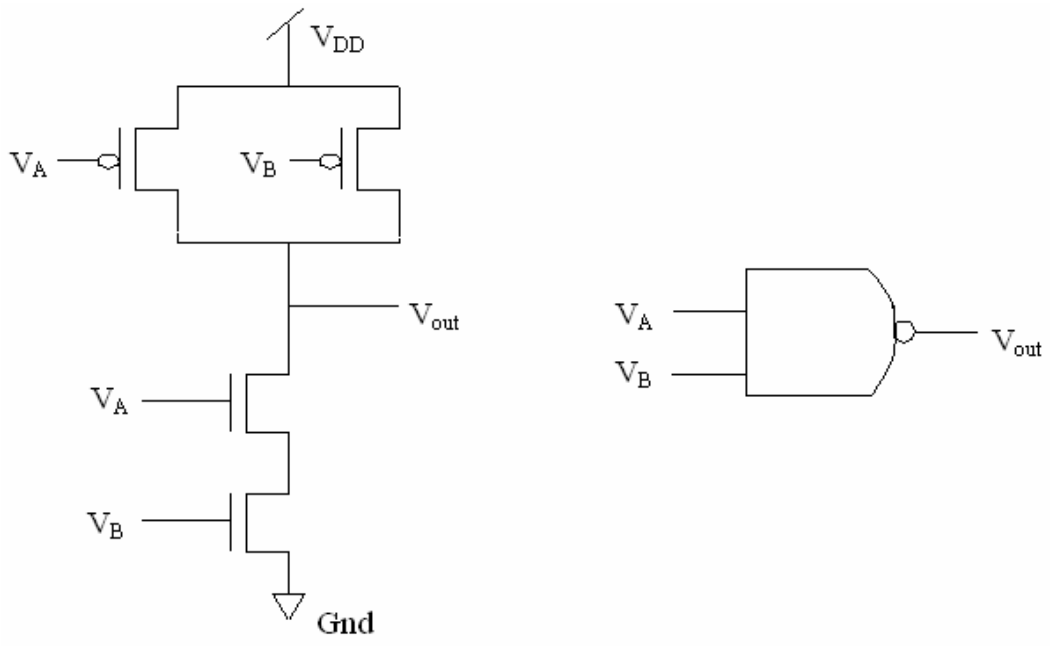


Figure 5.3. The Basic Structure of a Two-Input CMOS NAND Gate.

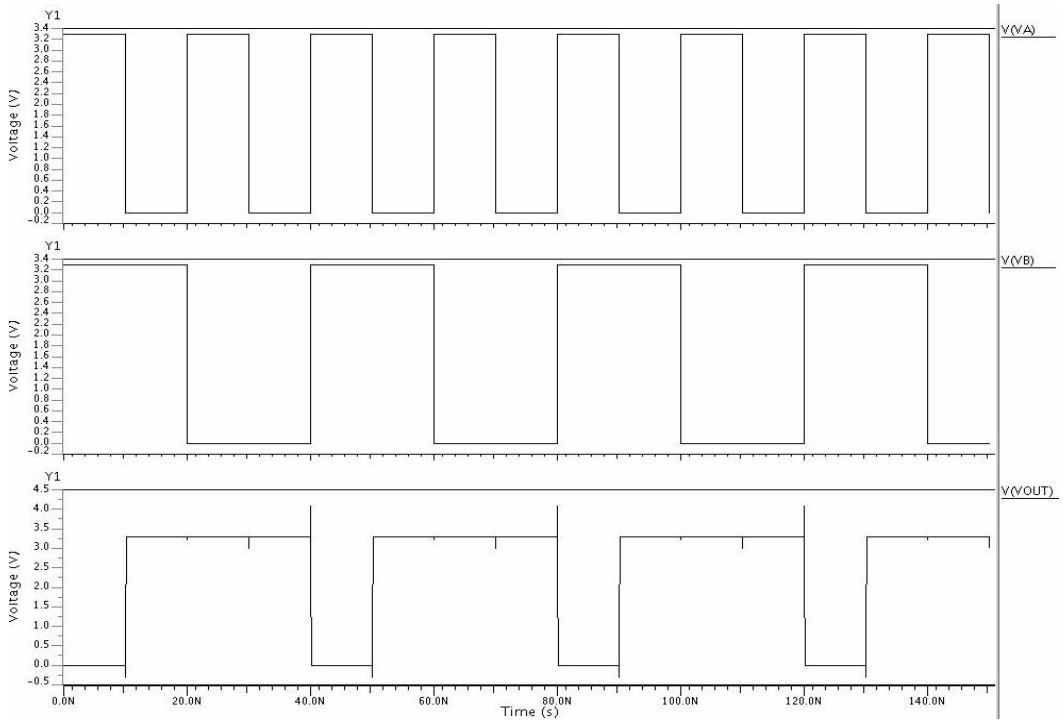


Figure 5.4. Simulation Results of Two-Input CMOS NAND Gate:
(a) Input Signal (VA), (b) Input Signal (VB),
(c) Voltage Waveform of Output Signal (NAND Output).

5.3 DESIGN AND SIMULATION FOR A TWO-INPUT CMOS NOR GATE

The minimum-sized Two-Input CMOS NOR Gate structure is designed in Mentor Graphics IC Design Architect and simulated with the ELDO Simulator driving a capacitive load of 7 *fF*. The basic structure is shown below in Figure 5.5 and the transient simulated results are shown in Figure 5.6, respectively.

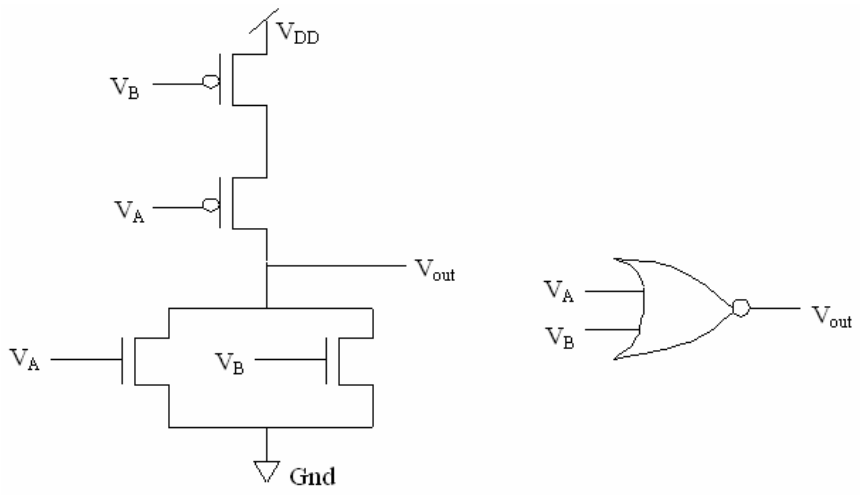
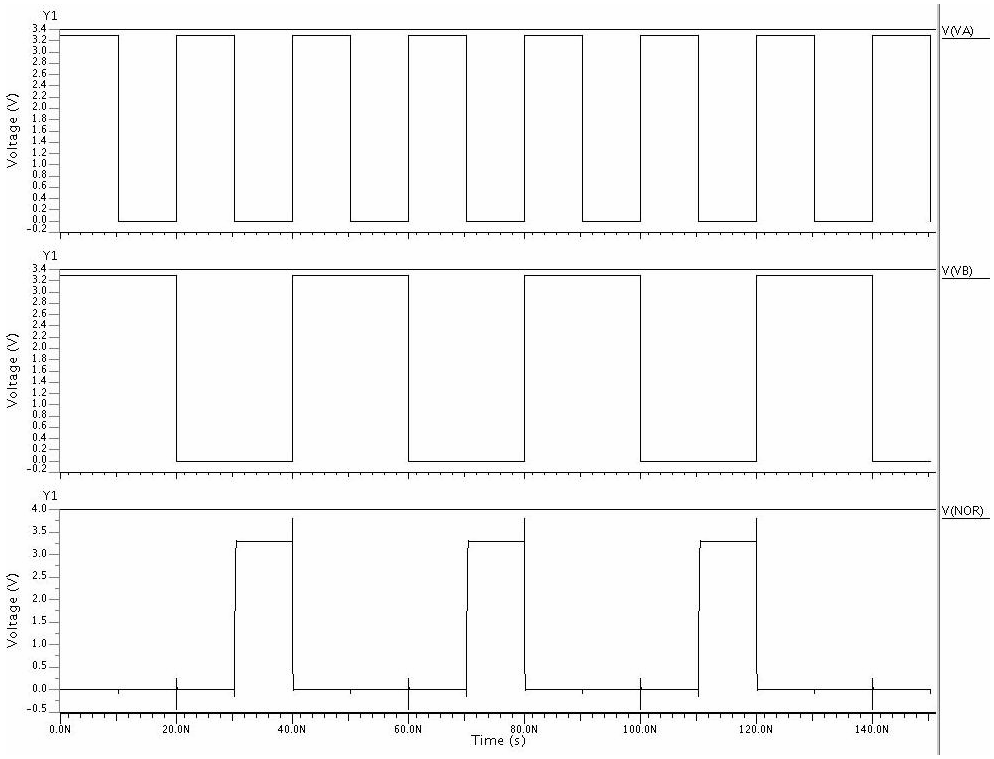


Figure 5.5. The Basic Structure of a Two-Input CMOS NOR Gate.



(a)

(b)

(c)

Figure 5.6. Simulation Results of Two Input CMOS NOR Gate:
(a) Input Signal (VA), (b) Input Signal (VB),
(c) Voltage Waveform of Output Signal (NOR Output).

5.4 DESIGN AND SIMULATION FOR A TWO-INPUT CMOS XOR GATE

The minimum-sized Two-Input CMOS XOR Gate structure is as shown below in Figure 5.7 and ELDO Simulated transient analysis waveforms are also shown in Figure 5.8.

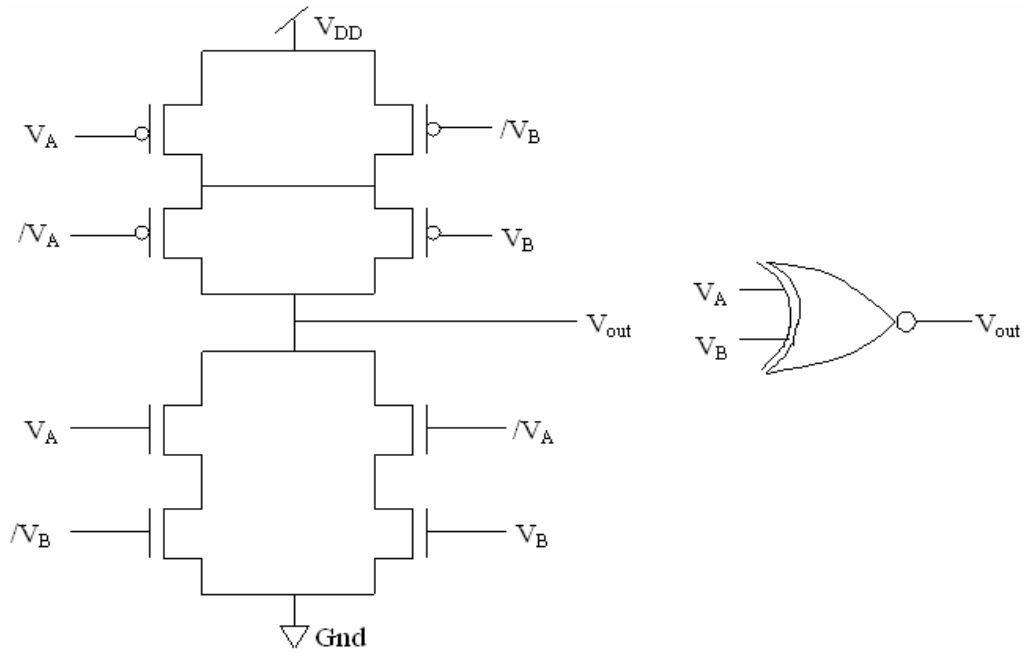


Figure 5.7. The Basic Structure of a Two-Input CMOS XOR Gate.

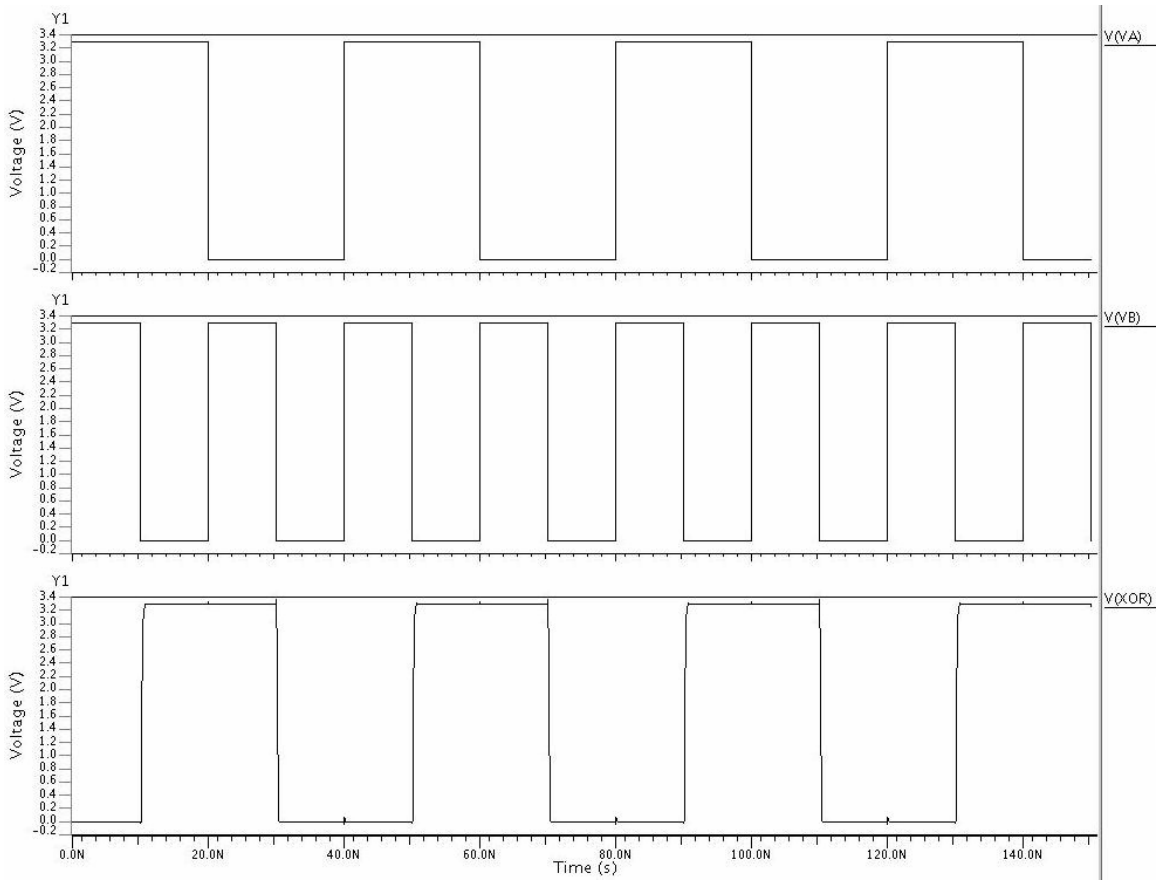


Figure 5.8. Simulation Results of Two Input CMOS XOR Gate:
(a) Input Signal (VA), (b) Input Signal (VB),
(c) Voltage Waveform of Output Signal (XOR Output).

5.5 DESIGN AND SIMULATION FOR A 2-TO-1 CMOS MULTIPLEXER

The CMOS based Two-to-One Multiplexer designed in Mentor Graphics IC Design Architect in Standard TSMC 0.35 μm CMOS Technology was simulated in ELDO Simulator and the transient simulated results are as shown below in Figures 5.9 and 5.10.

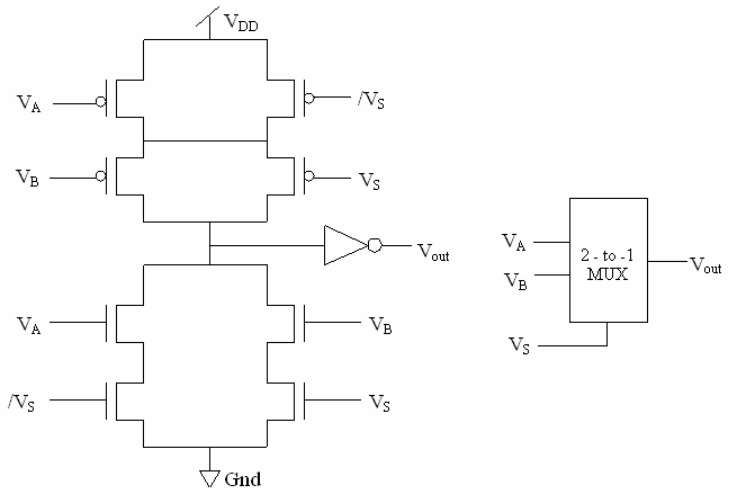


Figure 5.9. The Basic Structure of a Two-to-One CMOS Multiplexer.

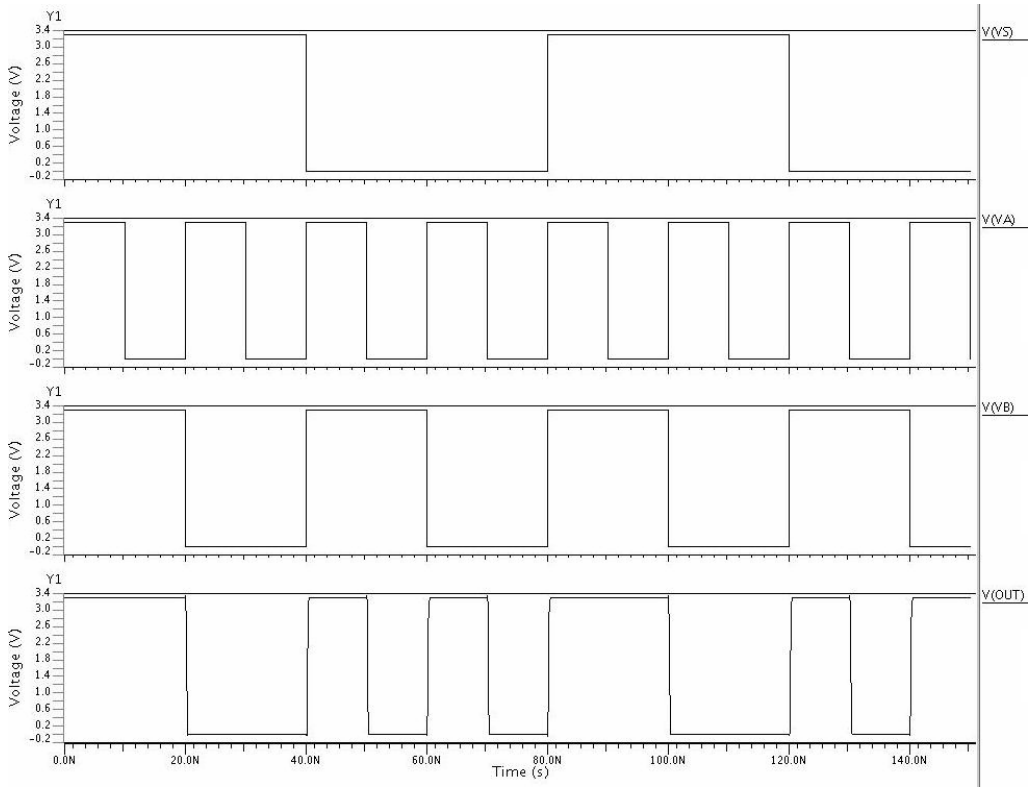


Figure 5.10. Simulation results of a 2:1 CMOS Multiplexer:
(a) Select Signal (VS), (b) Input Signal (VA),
(c) Input Signal (VB), (d) Voltage Waveform of Output Signal.

5.6 DESIGN AND SIMULATION FOR ONE-BIT CMOS FULL ADDER

The CMOS based One-Bit Full Adder is designed in Mentor Graphics TSMC 0.35 μm CMOS Technology and simulated with the ELDO Simulator with the supply voltage of 3.3 V.

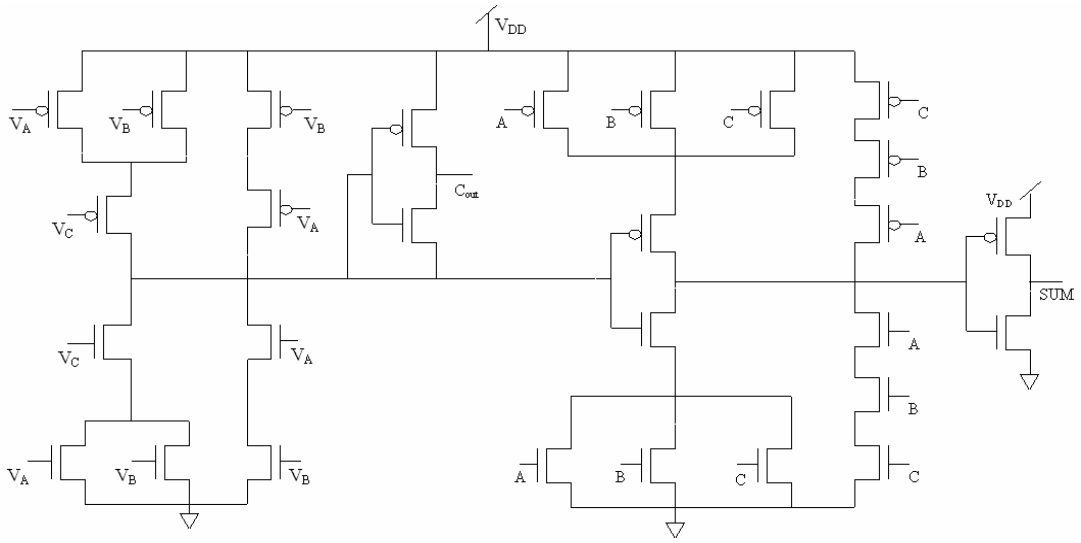


Figure 5.11. The Basic Structure of a One-Bit CMOS Full-Adder.

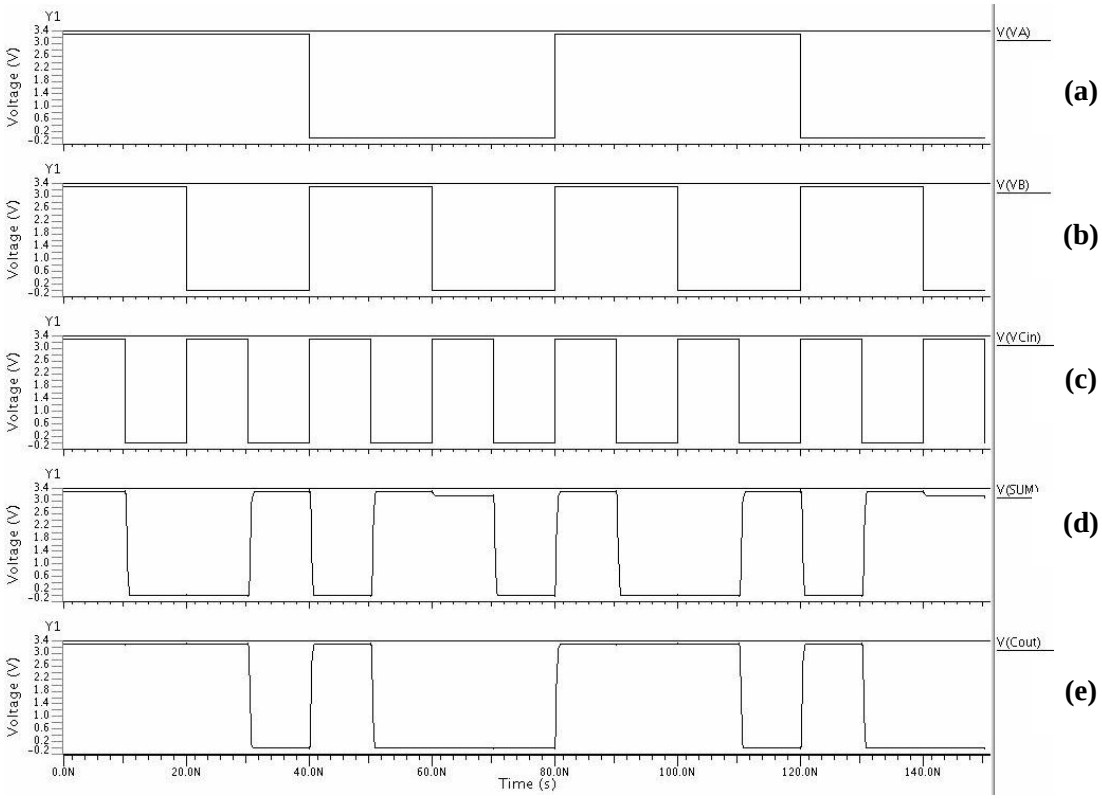


Figure 5.12. Simulation results of One-Bit CMOS Full Adder:
(a) Input Signal (VA), (b) Input Signal (VB),
(c) Input Carry Signal (VC_{in}),
(d) Voltage Waveform of Output (SUM) Signal,
(e) Voltage Waveform of Output (OUTPUT CARRY Signal).

5.7 DESIGN AND SIMULATION FOR AN ADIABATIC PFAL BUFFER / INVERTER

The design of a basic inverter based on an adiabatic switching principle is to be design and analyze first. In this section, a family of a partially adiabatic logic known as Positive Feedback Adiabatic Logic (PFAL) is used for the design of a basic buffer/ inverter. PFAL family is used because of the reason mentioned in the Chapter 4. The minimum size PFAL buffer/ inverter is designed and simulated in the standard TSMC 0.35 μm technology.

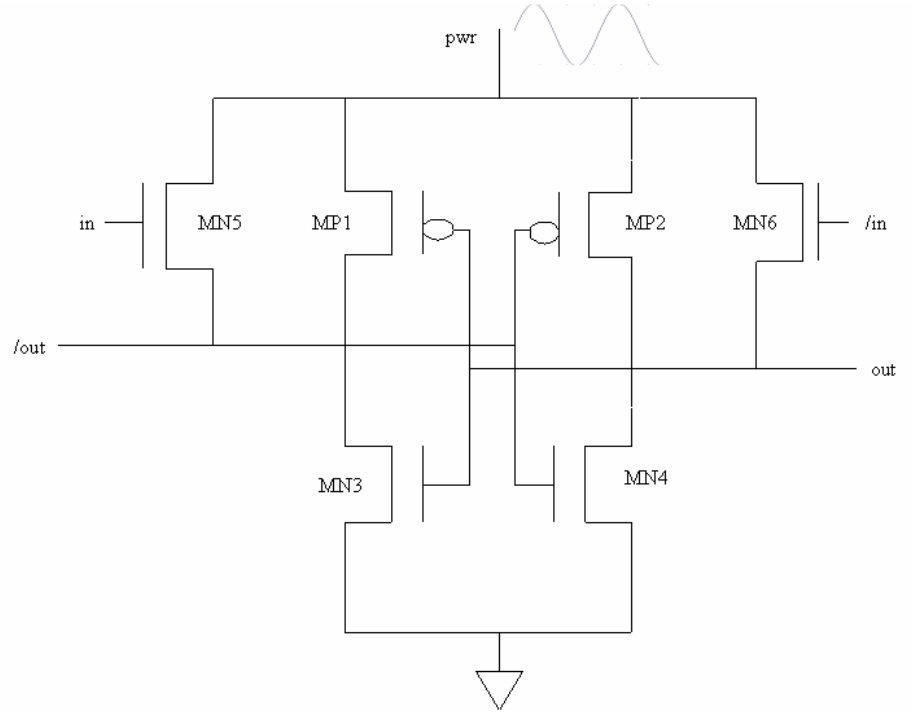


Figure 5.13. The Basic Structure of an Adiabatic PFAL Buffer / Inverter.

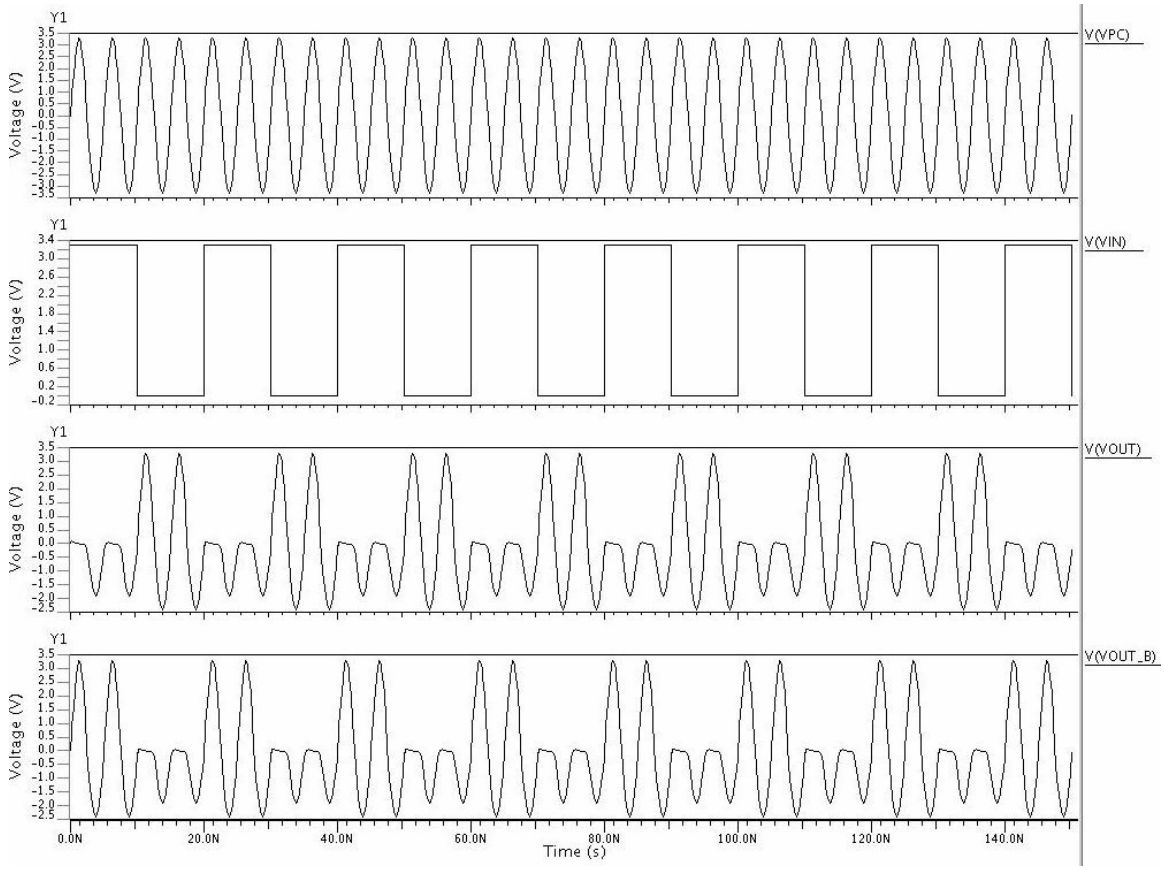


Figure 5.14. Simulation results of an Adiabatic PFAL Buffer / Inverter:
(a) Power Clock signal (VPC),
(b) Input signal (VIN),
(c) Voltage waveform of output signal (VOUT),
(d) Voltage waveform of output signal (VOUT_b) (complemented output).

5.8 DESIGN AND SIMULATION FOR AN ADIABATIC PFAL TWO-INPUT AND / NAND GATE

The partially adiabatic PFAL two-input NAND/ AND gate can be implemented as shown below in the Figure 5.15 using standard TSMC 0.35 μm technology and simulated waveforms is shown in Figure 5.16, respectively.

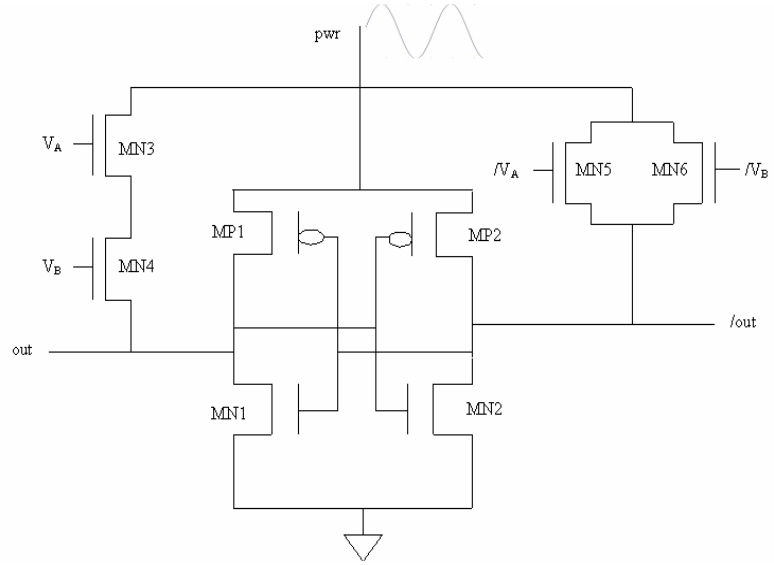


Figure 5.15. The Basic Structure of an Adiabatic PFAL Two-Input AND / NAND Gate.

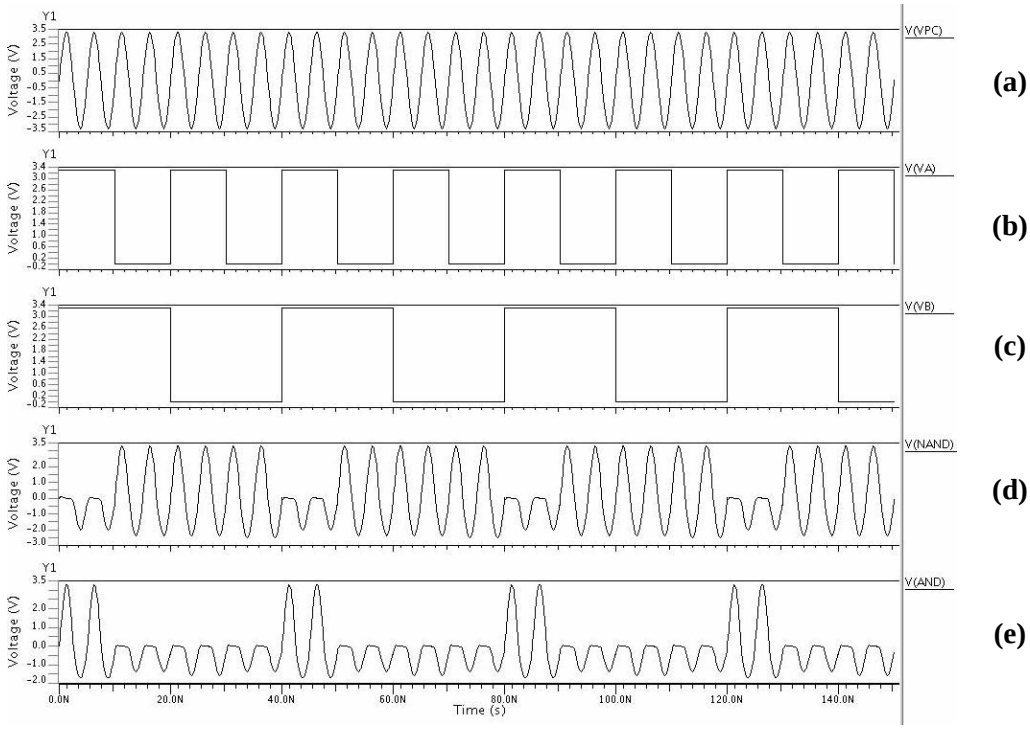


Figure 5.16. Simulation Results of an Adiabatic PFAL Two- Input AND / NAND Gate:
(a) Power Clock Signal (VPC), (b) Input Signal (VA), (c) Input Signal (VB),
(d) Voltage Waveform of an Output Signal (NAND Output),
(e) Voltage Waveform of an Output Signal (AND Output).

5.9 DESIGN AND SIMULATION FOR AN ADIABATIC PFAL TWO-INPUT OR / NOR GATE

A two-input NOR gate functionality can be explained by its adiabatic PFAL structure as shown in Figure 5.17 below and the corresponding ELDO simulated waveforms are shown in Figure 5.18, respectively. The minimum-sized adiabatic PFAL NOR gate has been designed in standard TSMC 0.35 μm technology.

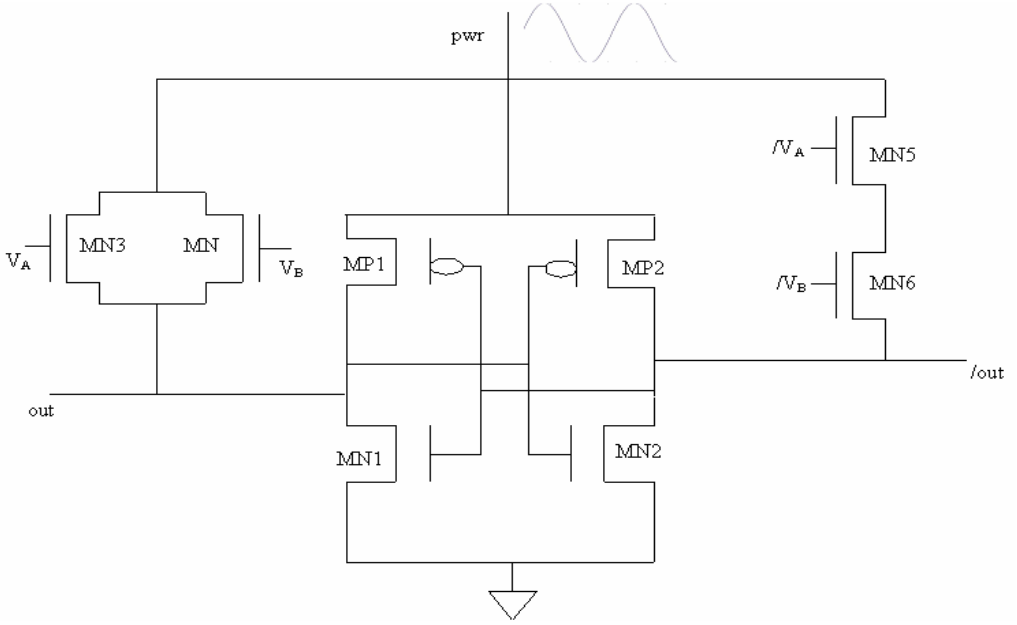


Figure 5.17. The Basic Structure of an Adiabatic PFAL Two-Input OR / NOR Gate.

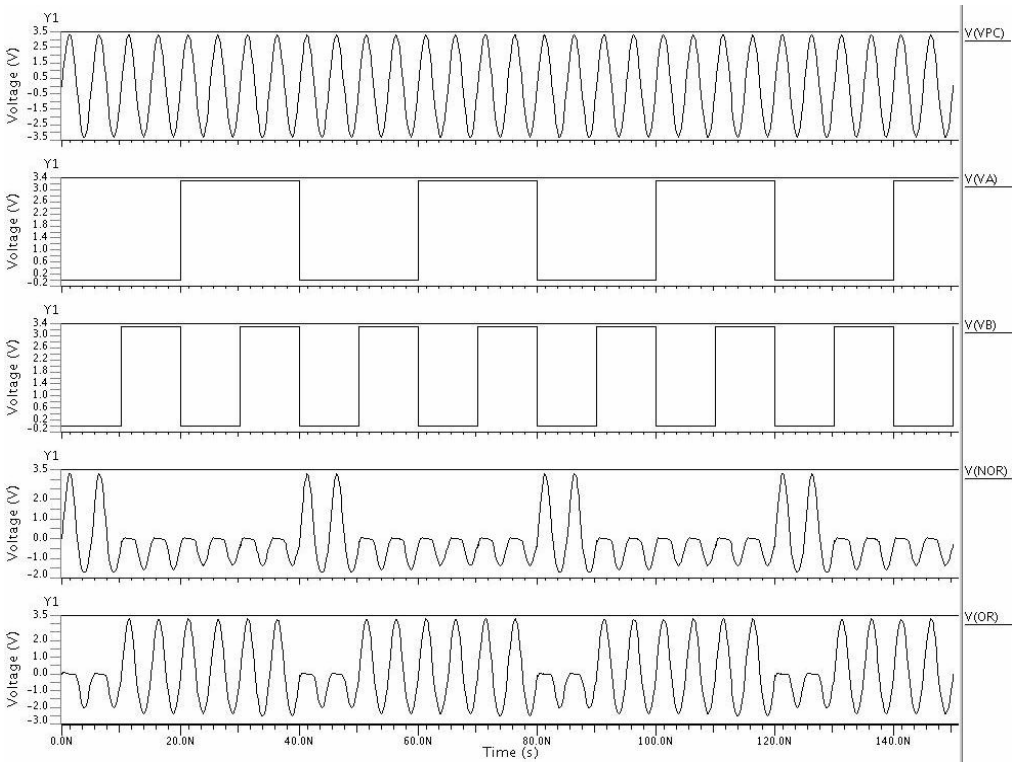


Figure 5.18. Simulation Results of an Adiabatic PFAL Two- Input OR / NOR Gate: (a) Power Clock Signal (VPC), (b) Input Signal (VA), (c) Input Signal (VB), (d) Voltage Waveform of an Output Signal (NOR Output), (e) Voltage Waveform of an Output Signal (OR Output).

5.10 DESIGN AND SIMULATION FOR AN ADIABATIC PFAL TWO-INPUT XOR / XNOR GATE

An adiabatic PFAL exclusive-OR gate is implemented as below in Figure 5.19 and simulated waveforms are as shown in Figure 5.20, respectively. The minimum-sized XOR gate implemented will show lesser power dissipation as compared to the conventional CMOS logic, as will be dealt in later chapters.

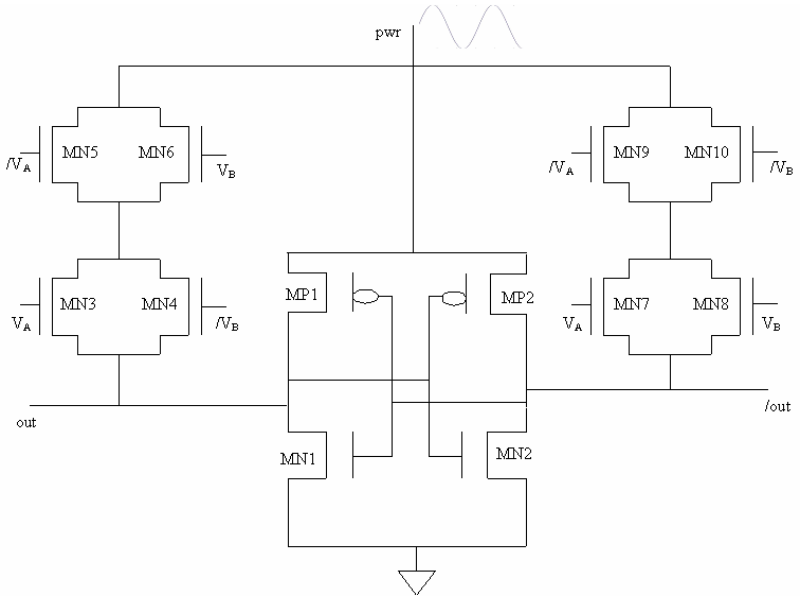
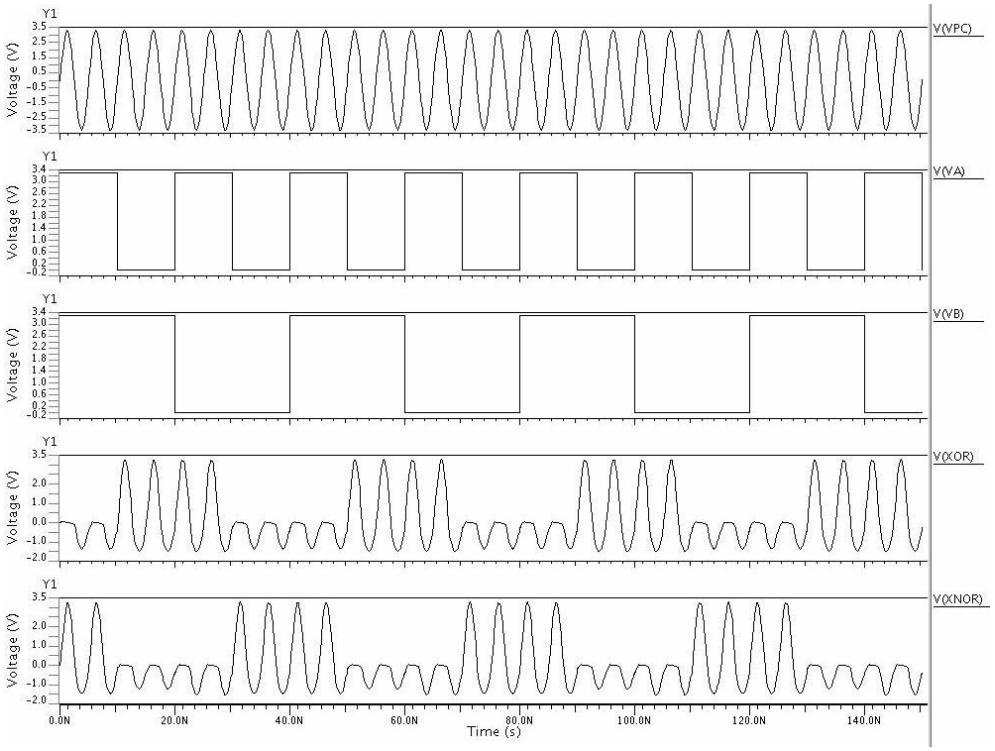


Figure 5.19. The Basic Structure of an Adiabatic PFAL Two-Input XOR / XNOR Gate.



(a)

(b)

(c)

(d)

(e)

Figure 5.20. Simulation Results of an Adiabatic PFAL Two- Input XOR / XNOR Gate:
(a) Power Clock Signal (VPC), (b) Input Signal (VA), (c) Input Signal (VB),
(d) Voltage Waveform of an Output Signal (XOR Output),
(e) Voltage Waveform of an Output Signal (XNOR Output).

5.11 DESIGN AND SIMULATION FOR AN ADIABATIC PFAL 2:1 MULTIPLEXER

An adiabatic PFAL two-to-one Multiplexer can be implemented in standard TSMC 0.35 *µm* technology. It implements the function *F* = (*A*) (*/S*) + (*B*) (*S*) as illustrated in the Figure 5.21, respectively. When the select (*S*) signal is low, it outputs the signal *A* and when the select (*S*) signal is high, it outputs the signal *B*, respectively and its functionality can be proven with the help of the ELDO simulated waveforms as shown in the Figure 5.22.

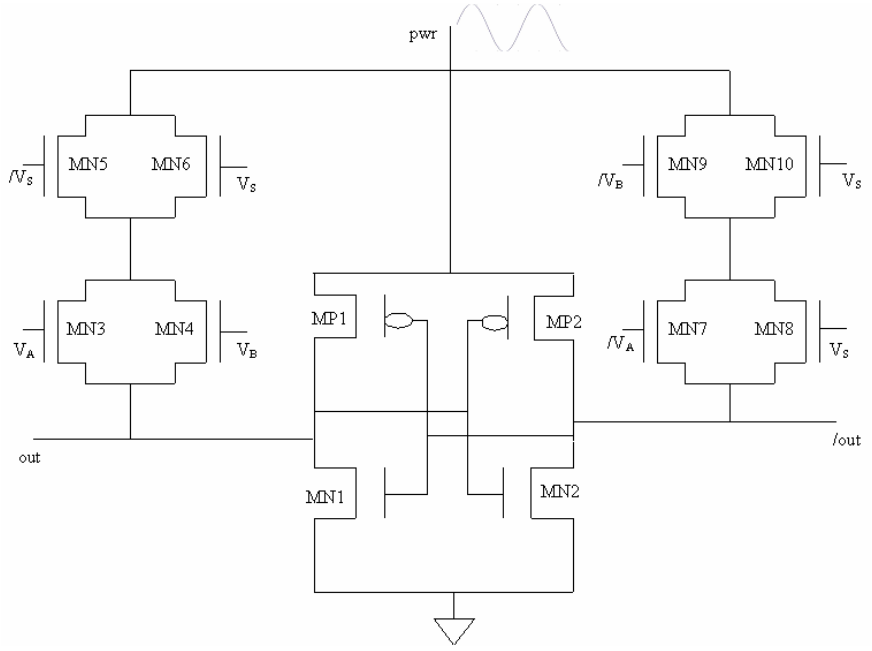


Figure 5.21. The Basic Structure of an Adiabatic PFAL 2:1 Multiplexer [*F* = (*A*) (*/S*) + (*B*) (*S*)].

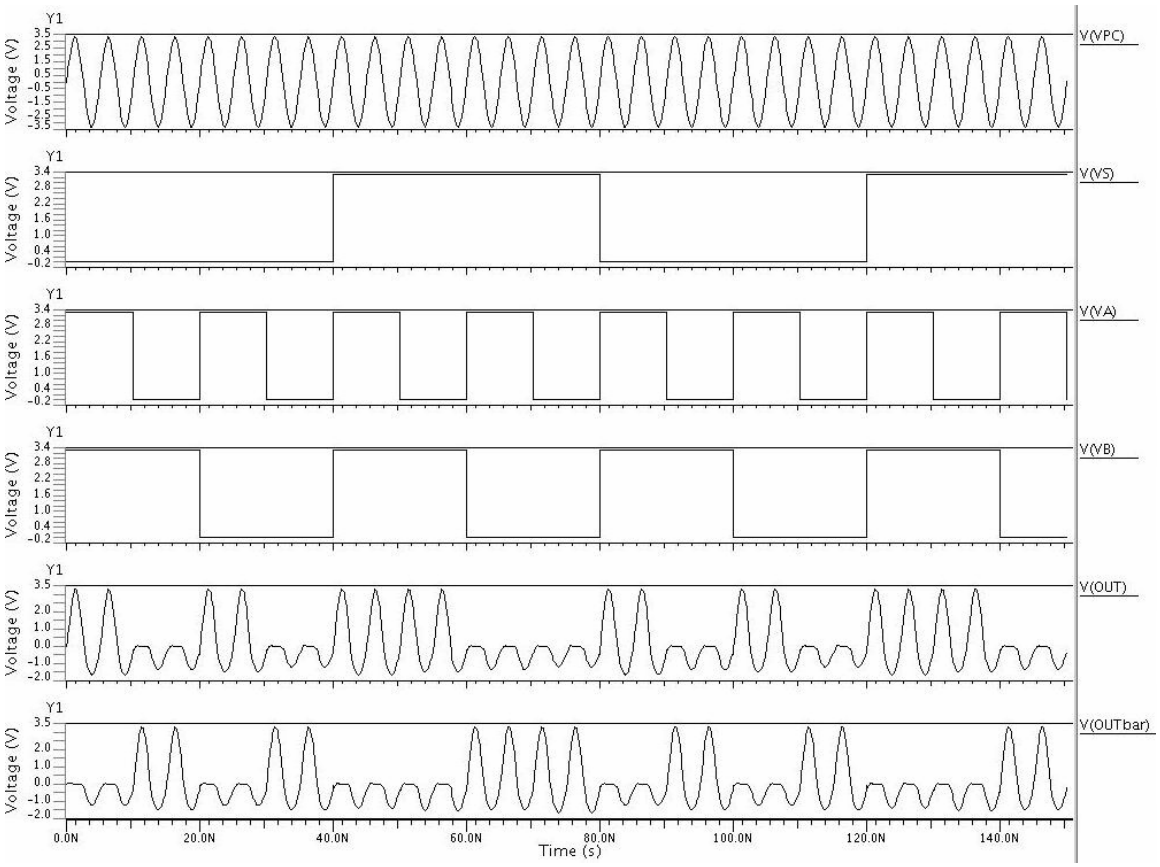


Figure 5.22. Simulation Results of an Adiabatic PFAL 2:1 Multiplexer
[*F* = (*A*) (*/S*) + (*B*) (*S*)]:
(a) Power Clock Signal (VPC), (b) Input Signal (VS), (c) Input Signal (VA),
(d) Input Signal (VB), (e) Voltage Waveform of an Output Signal (OUT),
(f) Voltage Waveform of an Output Signal (OUT_b).

5.12 DESIGN AND SIMULATION FOR AN ADIABATIC PFAL ONE-BIT FULL ADDER

A partially adiabatic logic family PFAL one-bit Full Adder block can be implemented as shown in the Figure 5.23 (for SUM block) and Figure 5.24 (for OUTPUT_CARRY) below, respectively. The minimum-size one-bit full adder is implemented in the standard TSMC 0.35 *μm* technology and simulated in the ELDO simulator, respectively.

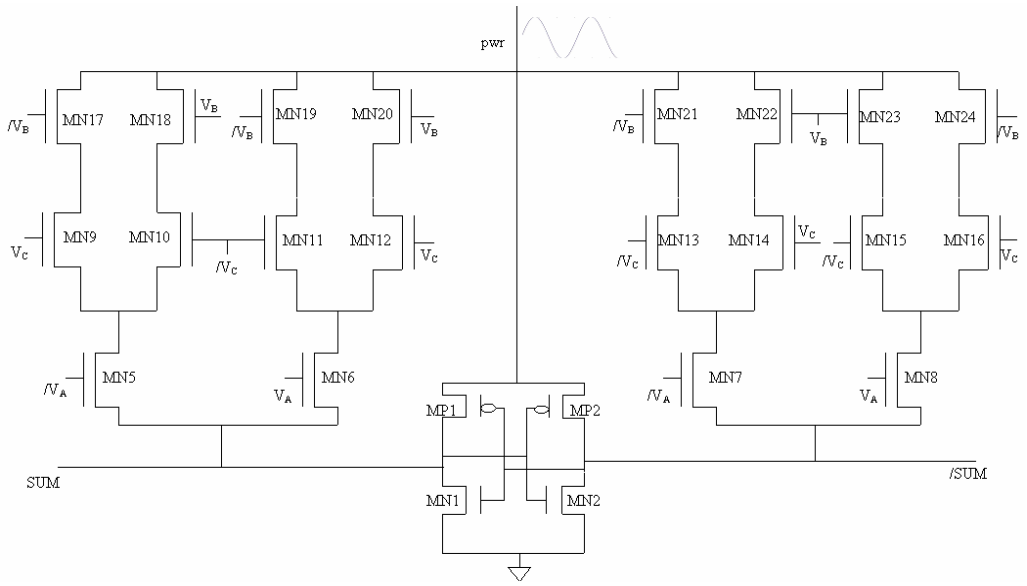


Figure 5.23. The Basic Structure of an Adiabatic PFAL Full-Adder (SUM).

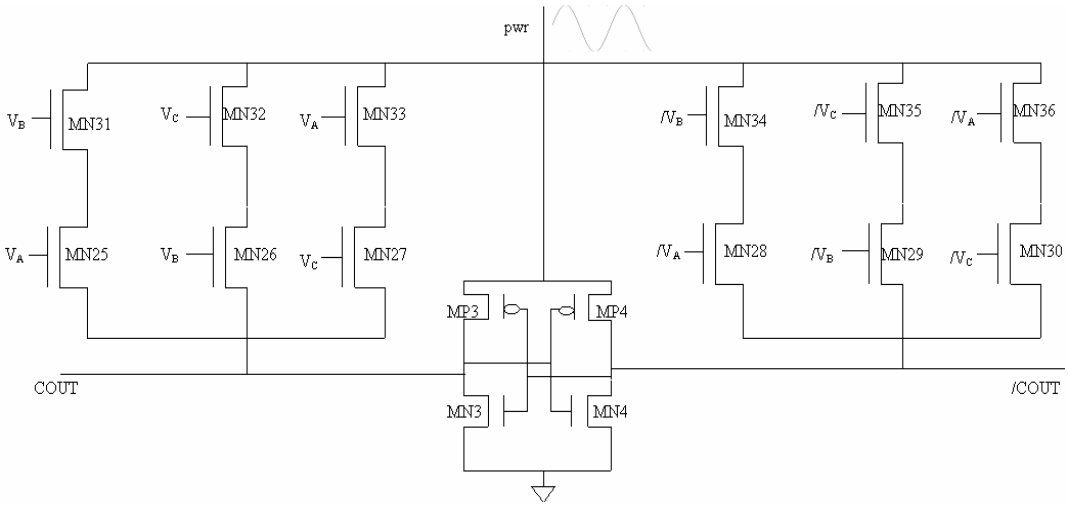


Figure 5.24. The Basic Structure of an Adiabatic PFAL Full-Adder (OUTPUT CARRY).

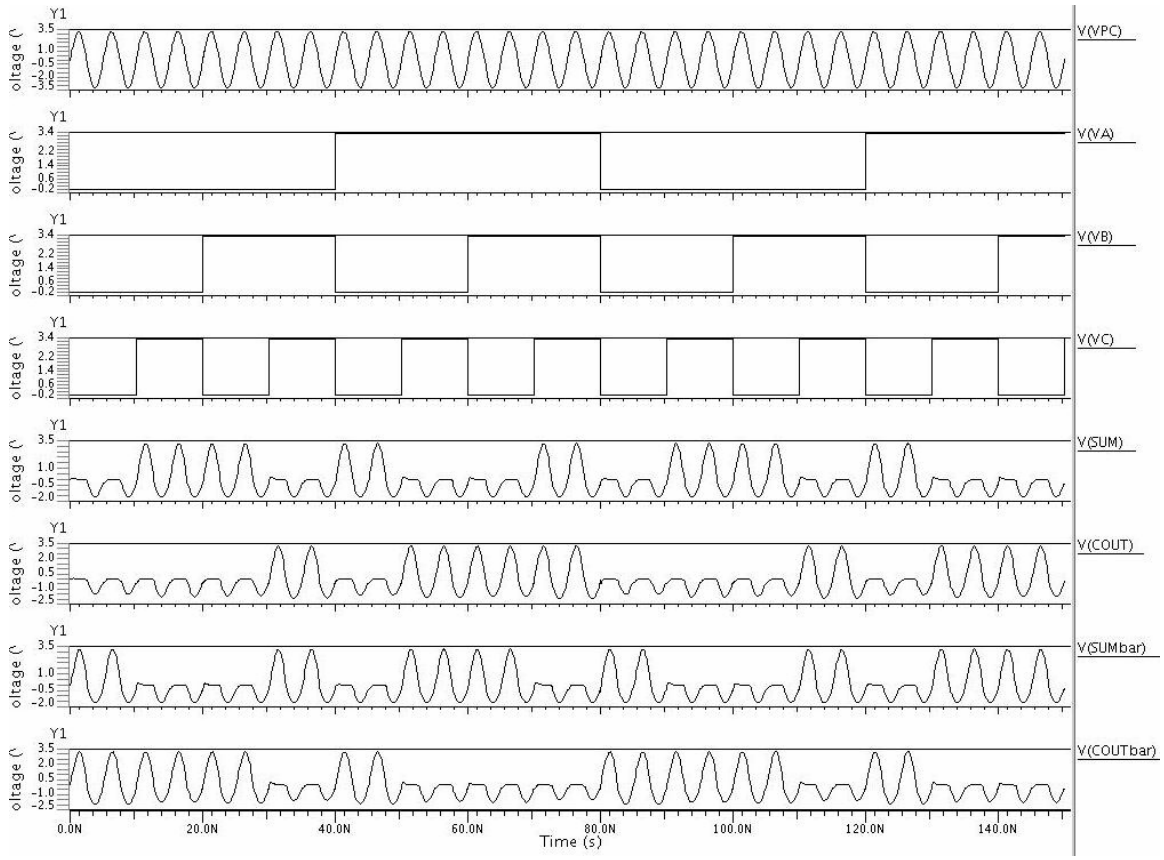


Figure 5.25. Simulation Results of an Adiabatic PFAL 2:1 Multiplexer:
(a) Power Clock Signal (VPC), (b) Input Signal (VA),
(c) Input Signal (VB), (d) Input Signal (VC_{in}),
(e) Voltage Waveform of Output Signal (SUM),
(f) Voltage Waveform of an Output Signal (C_{out}),
(g) Voltage Waveform of Output Signal (/SUM),
(h) Voltage Waveform of Output Signal (/C_{out}).

5.13 POWER DISSIPATION ANALYSIS

5.13.1 VARIATION OF POWER DISSIPATION WITH FREQUENCY

This section deals with the comparison of the full complementary CMOS logic style with the ultra low-power adiabatic logic style in terms of the average dynamic power dissipation, expressed in micro-Watts.

TABLE 5.1

AVERAGE DYNAMIC POWER DISSIPATED BY STATIC CMOS FAMILY AND ADIABATIC PFAL FAMILY FOR AN INVERTER FOR DIFFERENT POWER CLOCK FREQUENCIES

Frequency (MHz)	Static CMOS (µW)	Adiabatic (PFAL) Logic (µW)
25 M	1.4752 µ	0.1249 µ
50 M	2.9497 µ	0.2820 µ
100 M	5.8979 µ	1.3681 µ
125 M	7.2918 µ	1.7383 µ
150 M	8.8989 µ	3.2294 µ
200 M	11.7937 µ	8.3552 µ
250 M	14.5424 µ	12.5624 µ

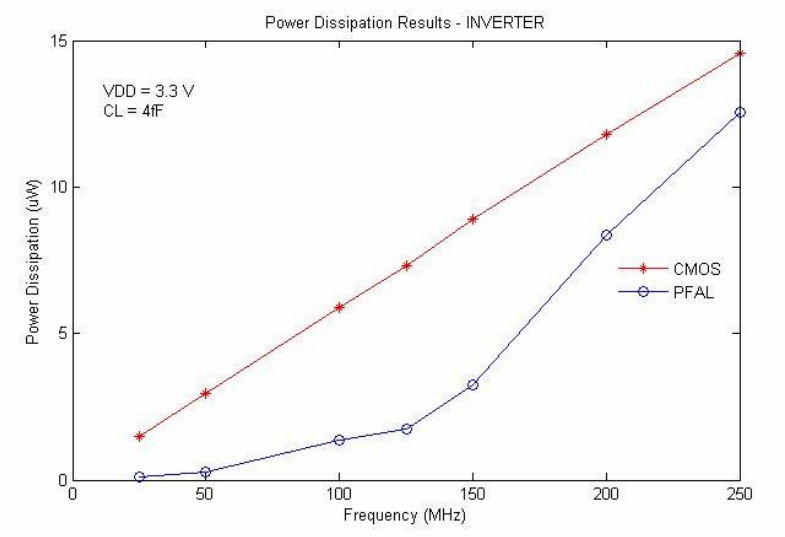


Figure 5.26. Power Dissipation Results for an INVERTER.

TABLE 5.2

AVERAGE DYNAMIC POWER DISSIPATED BY STATIC CMOS FAMILY AND ADIABATIC PFAL FAMILY FOR TWO - INPUT NAND GATE FOR DIFFERENT POWER CLOCK FREQUENCIES

Frequency (MHz)	Static CMOS (µW)	Adiabatic (PFAL) Logic (µW)
25 M	1.9138 µ	1.1655 µ
50 M	3.8275 µ	1.4141 µ
100 M	7.6543 µ	1.4532 µ
125 M	9.4858 µ	1.6039 µ
150 M	11.3425 µ	2.0066 µ
200 M	15.2922 µ	2.1748 µ
250 M	18.9735 µ	2.6338 µ

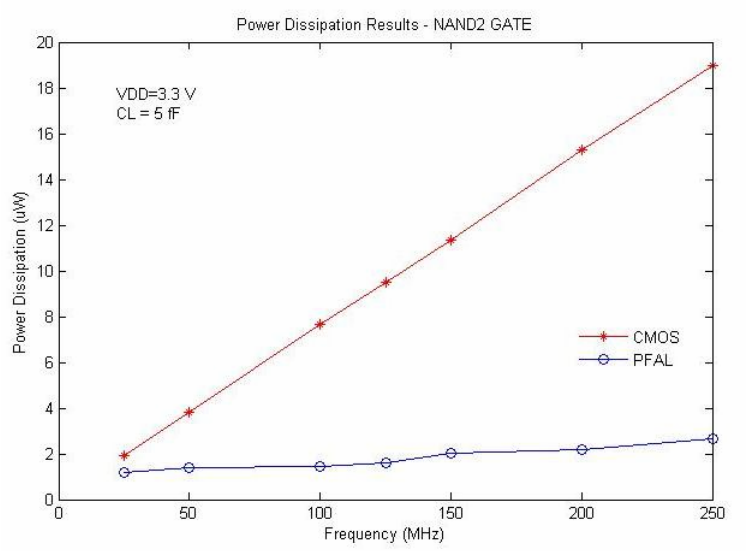


Figure 5.27. Power Dissipation Results for Two-Input NAND Gate.

TABLE 5.3

AVERAGE DYNAMIC POWER DISSIPATED BY STATIC CMOS FAMILY AND ADIABATIC PFAL FAMILY FOR TWO - INPUT NOR GATE FOR DIFFERENT POWER CLOCK FREQUENCIES

Frequency (MHz)	Static CMOS (µW)	Adiabatic (PFAL) Logic (µW)
25 M	5.5229 µ	0.1032 µ
50 M	11.0486 µ	0.1897 µ
100 M	21.9064 µ	0.3575 µ
125 M	27.3754 µ	0.4432 µ
150 M	33.0029 µ	0.4857 µ
200 M	43.9415 µ	0.8198 µ
250 M	54.8195 µ	1.8702 µ

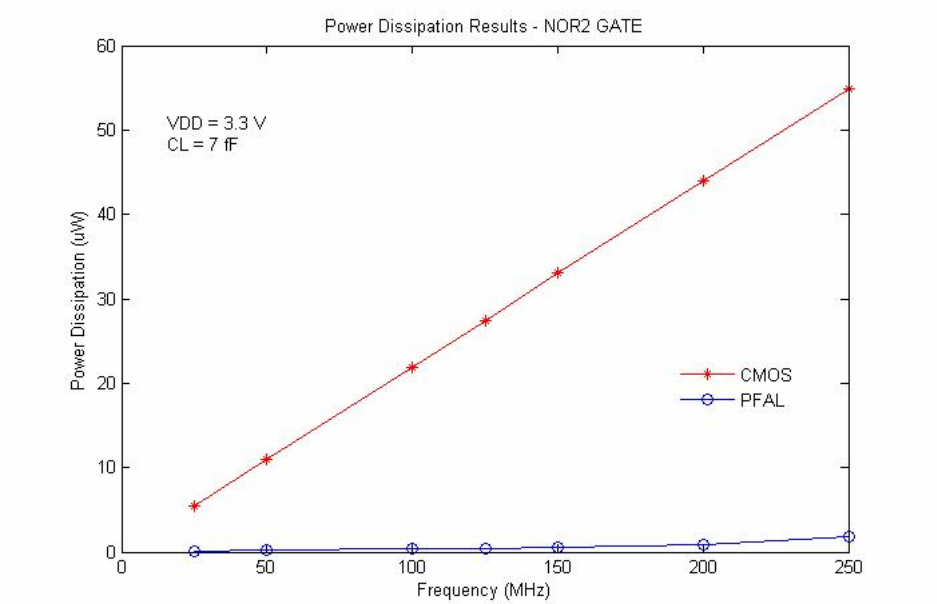


Figure 5.28. Power Dissipation Results for Two-Input NOR Gate.

TABLE 5.4

AVERAGE DYNAMIC POWER DISSIPATED BY STATIC CMOS FAMILY AND ADIABATIC PFAL FAMILY FOR TWO- TO- ONE MULTIPLEXER FOR DIFFERENT POWER CLOCK FREQUENCIES

Frequency (MHz)	Static CMOS (µW)	Adiabatic (PFAL) Logic (µW)
25 M	1.08180 µ	0.37638 µ
50 M	2.16193 µ	0.39386 µ
100 M	4.32028 µ	1.11854 µ
125 M	5.38708 µ	1.53608 µ
150 M	6.56028 µ	2.02470 µ
200 M	8.63974 µ	3.24876 µ

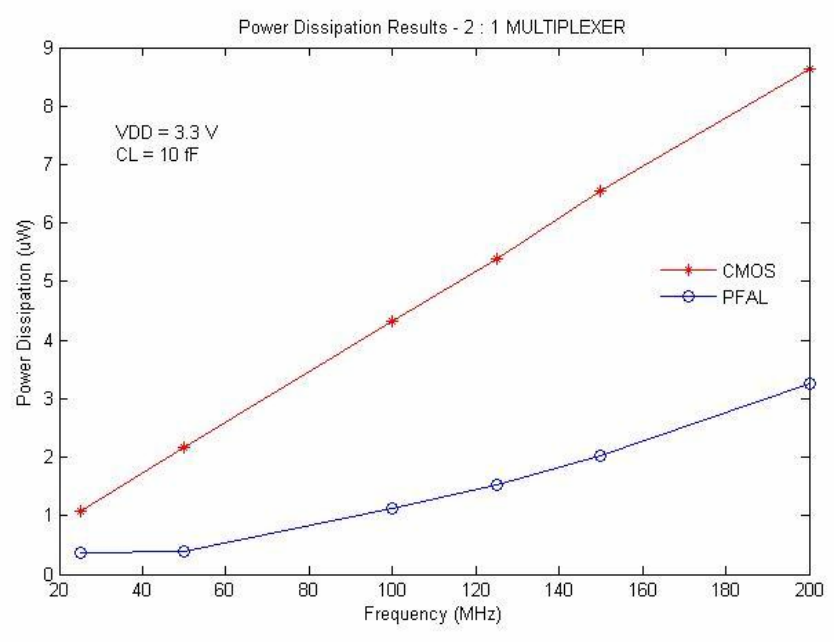


Figure 5.29. Power Dissipation Results for 2:1 MULTIPLEXER.

TABLE 5.5

AVERAGE DYNAMIC POWER DISSIPATED BY STATIC CMOS FAMILY AND ADIABATIC PFAL FAMILY FOR TWO – INPUT XOR GATE FOR DIFFERENT POWER CLOCK FREQUENCIES

Frequency (MHz)	Static CMOS (µW)	Adiabatic (PFAL) Logic (µW)
25 M	1.11672 µ	0.10736 µ
50 M	2.24789 µ	0.52175 µ
100 M	4.49252 µ	0.97935 µ
125 M	5.77343 µ	1.36315 µ
150 M	6.81817 µ	2.17462 µ
200 M	9.01582 µ	3.85372 µ
250 M	11.55732µ	5.95289 µ

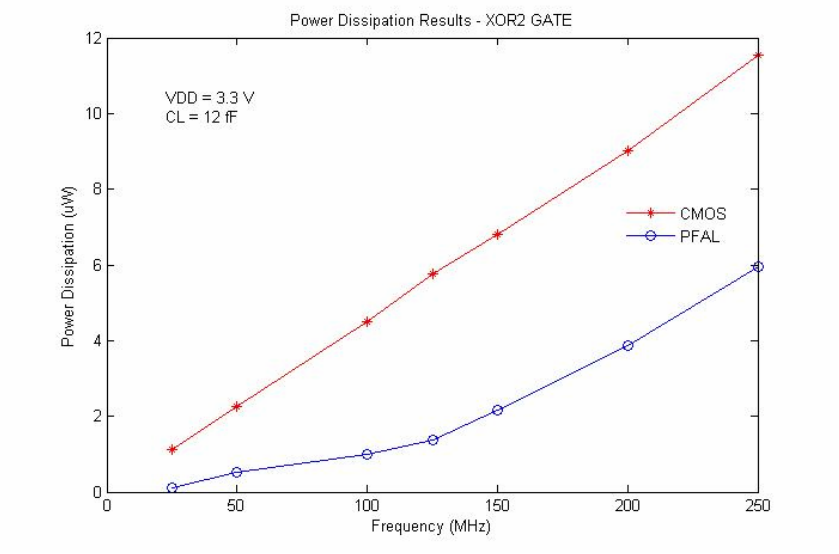


Figure 5.30. Power Dissipation Results for a Two-Input XOR Gate.

TABLE 5.6

AVERAGE DYNAMIC POWER DISSIPATED BY STATIC CMOS FAMILY AND ADIABATIC PFAL FAMILY FOR AN 1 – BIT FULL ADDER FOR DIFFERENT POWER CLOCK FREQUENCIES

Frequency (MHz)	Static CMOS (µW)	Adiabatic (PFAL) Logic (µW)
25 M	3.09117 µ	0.06525 µ
50 M	6.17664 µ	0.07495 µ
100 M	12.34536 µ	0.58937 µ
125 M	15.26948 µ	1.43600 µ
150 M	18.22525 µ	2.43514 µ
200 M	24.68954 µ	6.65162 µ
250 M	30.49156 µ	9.94327 µ

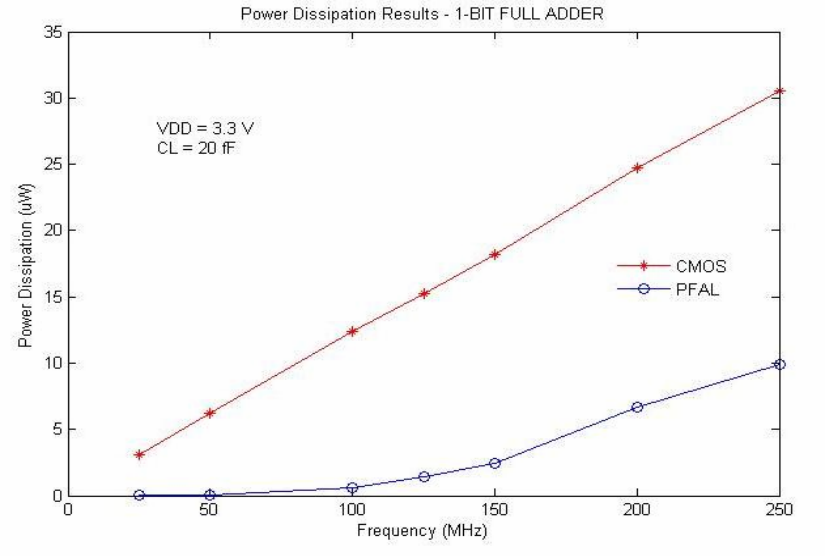


Figure 5.31. Power Dissipation Results for a 1-Bit FULL ADDER.

5.13.2 VARIATION OF POWER DISSIPATION WITH THE LOAD CAPACITANCE

This section discusses the power dissipation analysis of the various design units implemented in standard TSMC 0.35 micron technology. The variation of the power dissipation with the varying load capacitance is shown as in the following figures below. It is inferred from the following figures that with the increase in the load capacitance, there is an increase in the power dissipation of the circuit structure or, the digital system under consideration.

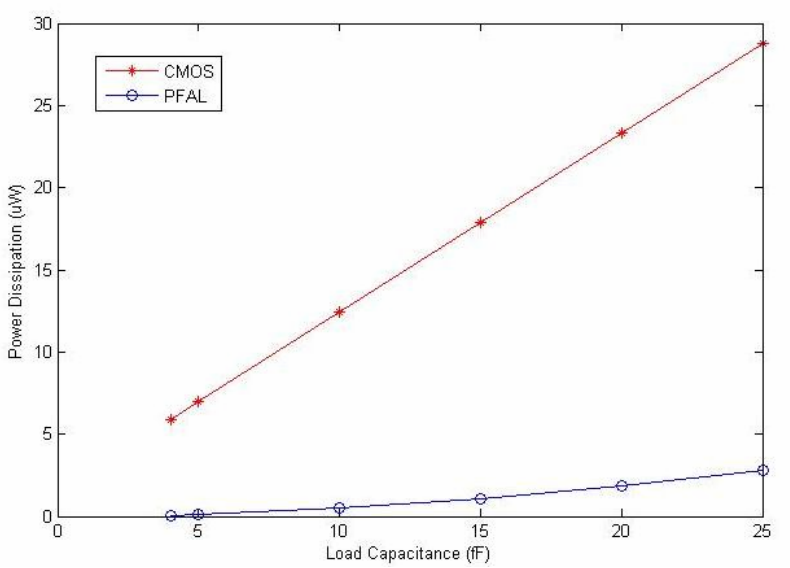


Figure 5.32. Variation of Power Dissipation with the Load Capacitance for an INVERTER operating @ f = 100 MHz and V_{DD} = 3.3 V.

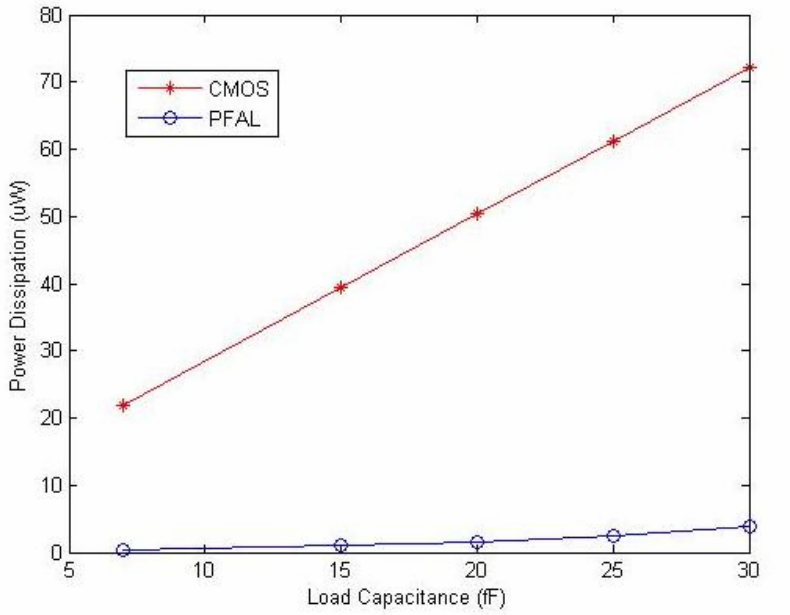


Figure 5.33. Variation of Power Dissipation with the Load Capacitance for Two-Input NOR Gate operating @ f = 100 MHz and V_{DD} = 3.3 V.

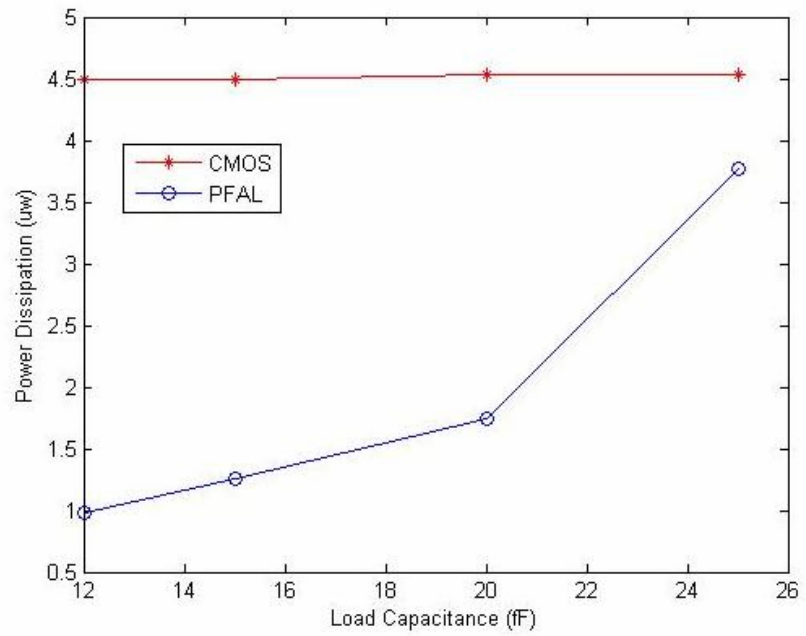


Figure 5.34. Variation of Power Dissipation with the Load Capacitance for Two-Input XOR Gate operating @ *f* = 100 MHz and V_{DD} = 3.3 V.

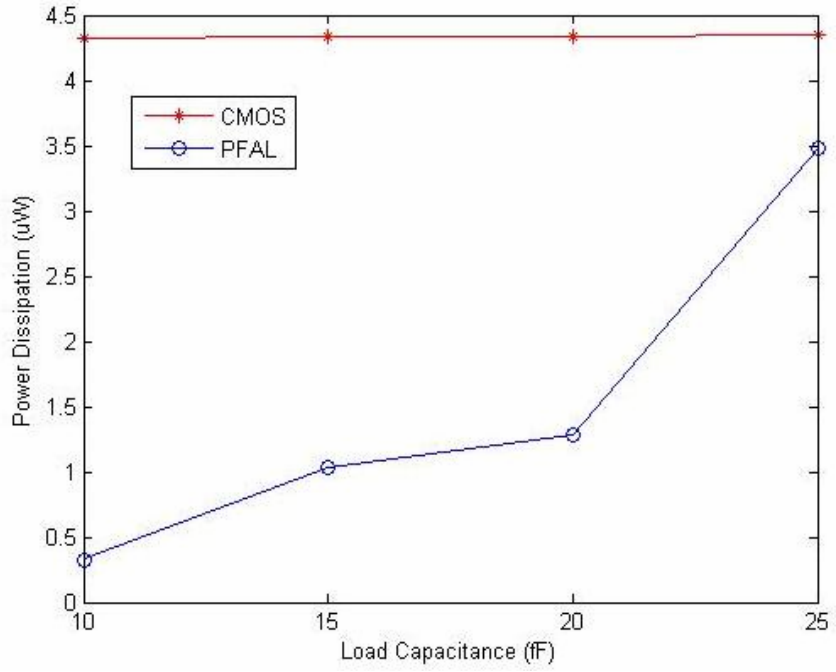


Figure 5.35. Variation of Power Dissipation with the Load Capacitance for 2:1 MULTLIPEXER operating @ *f* = 100 MHz and V_{DD} = 3.3 V.

CHAPTER 6 PHYSICAL LAYOUT DESIGN AND POST-LAYOUT SIMULATIONS

6.1 WHAT IS LAYOUT ?

Integrated Circuit (IC) Layout or mask design is the representation of an integrated circuit in terms of planar geometric shapes which correspond to the patterns of metal, oxide, or semiconductor layers that make up the components of the integrated circuit. In other words, Layout is the process by which a circuit *specification* is converted to a *physical implementation* with enough information to deduce all the relevant physical parameters of the circuit. A layout engineer's job is to place and connect all the components that make up a chip so that they meet all criteria. Typical goals are performance, size, and manufacturability.

6.1.1 THE ROLE OF LAYOUT IN THE DESIGN PROCESS

From a computer scientist's point of view, the layout process seems familiar enough. We are given a piece of *source code*, this time usually in terms of a circuit diagram, and we want to compile it to an *object code*, the physical layout of the circuit.

The layout step is the last major step in the design process before testing and fabrication; it is the step which reveals to the designer all the subtle electrical characteristics of the clean and logical digital systems.

6.1.2 TOLERANCES AND DESIGN RULES

The layout must pass a series of checks in a process known as Verification. The two most common checks in the verification process are Design Rule Checking (DRC), and Layout Versus Schematic (LVS). When all verification is complete, the data is translated into an industry standard format, typically GDSII, and sent to a semiconductor foundry. The process of sending this data to the foundry is called tapeout, due to the fact the data used to be shipped out on a magnetic tape. The foundry converts the data into another format and uses it to generate the photo masks used in a photolithographic process of semiconductor device fabrication.

6.1.3. DESIGN RULE CHECKING

Design Rule Checking of Check(s) (DRC) is the area of Electronic Design Automation that determines whether a particular chip layout satisfies a series of recommended parameters called Design Rules. Design Rule Checking is a major step during Physical Verification of the design, which also involves LVS (Layout Versus Schematic) Check, XOR Checks, ERC (Electrical Rule Check) and Antenna Checks.

Design rules are a set of parameters provided by the semiconductor manufacturer that enable the designer to verify the correctness of the mask set. Design rules are specific to a particular semiconductor manufacturing process. A design rule set specifies a minimum size or spacing requirements between the layers of the same type or of different types.

This provides a safety margin for various process variations, to ensure that the design will still have reasonable performance after the circuit is fabricated. There is a limit to how small features the photolithographic process can generate. Generally, this *feature size* is the width of a single minimum-width polysilicon wire used as a transistor gate (since this is the most important physical circuit dimension in determining circuit speed).

6.1.4 DESIGN RULE CHECKING (DRC) SOFTWARE

The main objective of design rule checking (DRC) is to achieve a high overall yield and reliability for the design. If the design rules are violated the design may not be functional. While design rule checks do not validate that the design will operate correctly, they are constructed to verify that the structure meets the process constraints for a given design type and process technology.

DRC software usually takes as input a layout in the GDSII standard format and a list of rules specific to the semiconductor process chosen for fabrication. From these it produces a report of design rule violations that the designer may or may not choose to correct.

DRC products define rules in a language to describe the operations needed to e performed in DRC. For example, Mentor Graphics uses Standard Verification Rule Format (SVRF) language in their DRC rules files.

Some example of DRC's in IC design includes:
Active to active spacing,
Well to well spacing,
Minimum channel length of the transistor,
Minimum metal width,
Metal to metal spacing,
ESD and I/O rules.

6.1.5 SCMOS DESIGN RULES

Basic Design Rules are

(1) Size Rules.

(2) Separation Rules.

(3) Overlap Rules.

A listing of the design rules is available in the following file:

~cad / Mentor_tools / ASIC_Design_Kit/adk3_1 / technology /ic / process / tsmc035.calibre.rules

The most important design rules are summarized below (all distances are *minimum*):

Polysilicon Region Width	2λ	Poly - Poly Spacing	2λ
Polysilicon Gate Extension	2λ	Diffusion Region Width	2λ
Diffusion – Diffusion Spacing	3λ	Contact Extension	1λ
Metal 1 width	3λ	Metal 1 spacing	3λ
Metal 2 Width	3λ	Metal 2 spacing	4λ
Via size	4λ		

6.1.6 LAYOUT VERSUS SCHEMATIC (LVS)

The Layout Versus Schematic (LVS) is the class of electronic design automation (EDA) verification software that determines whether a particular integrated circuit layout corresponds to the original schematic of circuit diagram of the design.

A successful Design rule check (DRC) ensures that the layout conforms to the rules designed / required for faultless fabrication. However, it does not guarantee if it really represents the circuit you desire to fabricate. This is where an LVS check is used. LVS

checking software recognizes the drawn shapes of the layout that represent the electrical components of the circuit, as well as the connections between them. The software then compares them with the schematic or circuit diagram. In most cases the layout will not pass LVS the first time requiring the layout engineer to examine the LVS software's reports and make changes to the layout.

6.2 PHYSICAL LAYOUT DESIGN OF DIFFERENT CMOS AND ADIABATIC LOGIC BASED CELL STRUCTURES

The physical layout design of different cells based on fully-complementary CMOS logic and adiabatic switching principle logic has been done in standard TSMC 0.35 μm CMOS technology. For the project work, Mentor Graphics Corporation IC Station was used for the design of different physical layout cell structures and an ELDO Simulator was used for all the validation of the physical layout designs.

This chapter discusses different physical layouts for all the proposed cell structures, and the LVS program was made to run for the comparison of the schematic to the physical layout structures. It will use both the extracted view and the schematic view of the physical layout.

6.2.1 LAYOUT CELL DESIGN OF A CMOS INVERTER

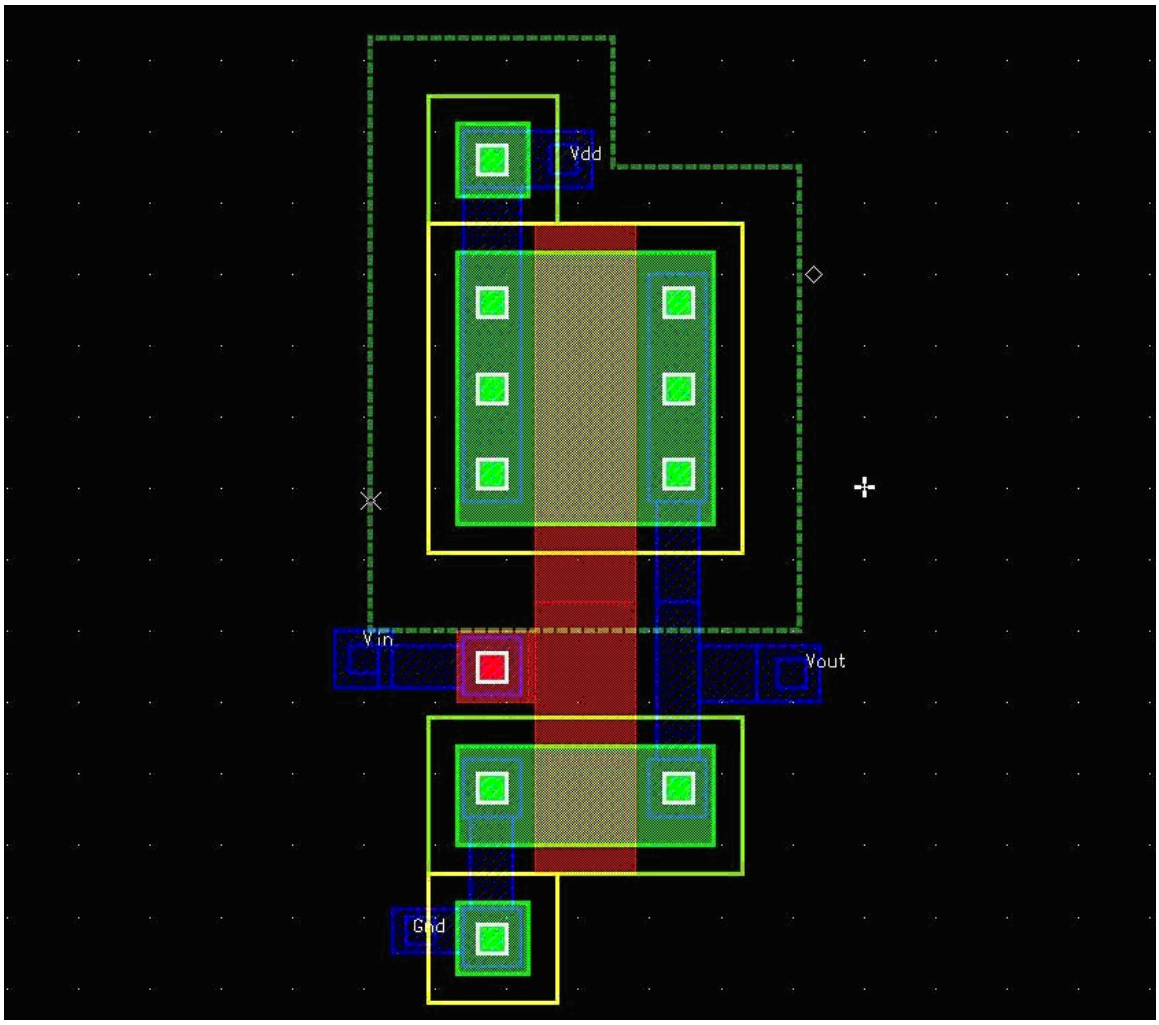


Figure 6.1. Layout of CMOS Inverter.

6.2.2 LAYOUT CELL DESIGN OF A TWO-INPUT CMOS NAND GATE

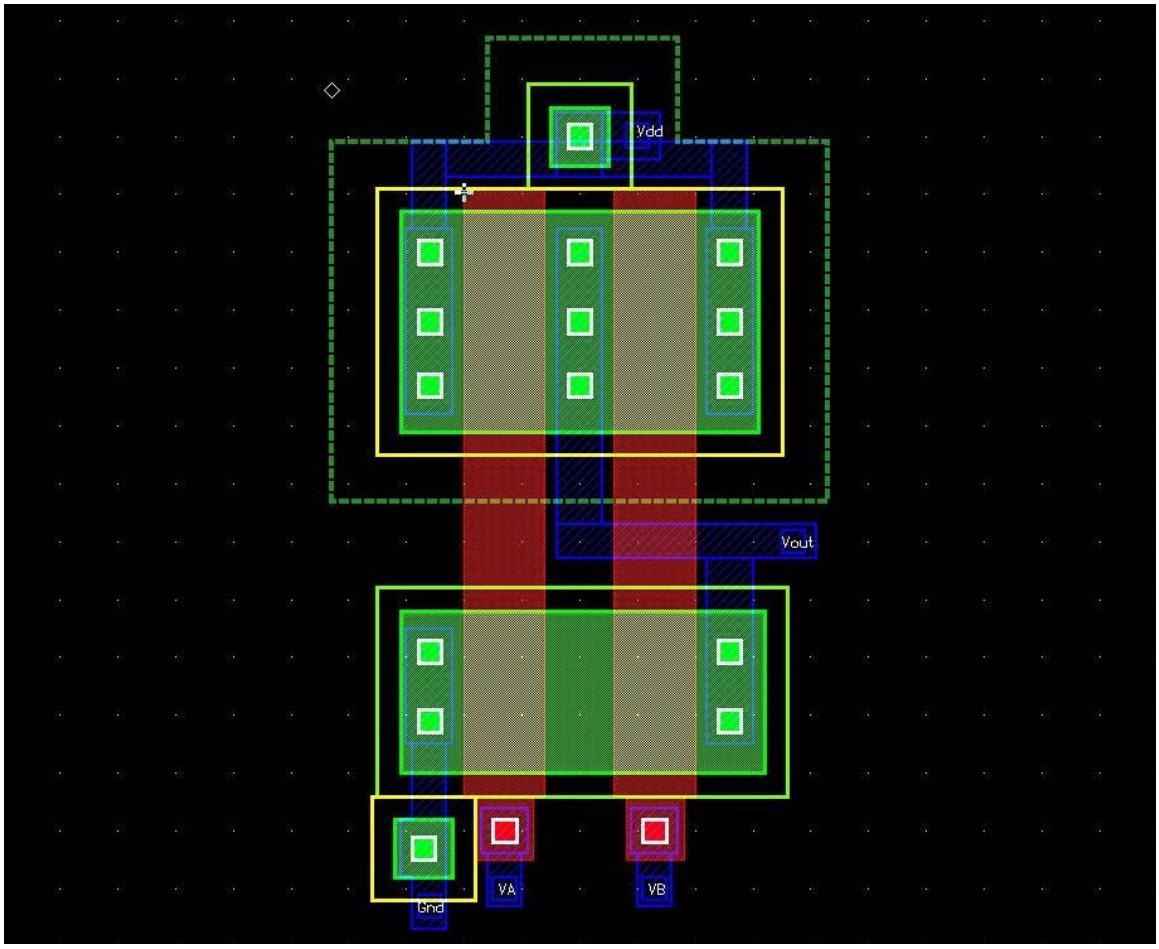


Figure 6.2. Layout of Two- Input CMOS NAND Gate.

6.2.3 LAYOUT CELL DESIGN OF A TWO-INPUT CMOS NOR GATE

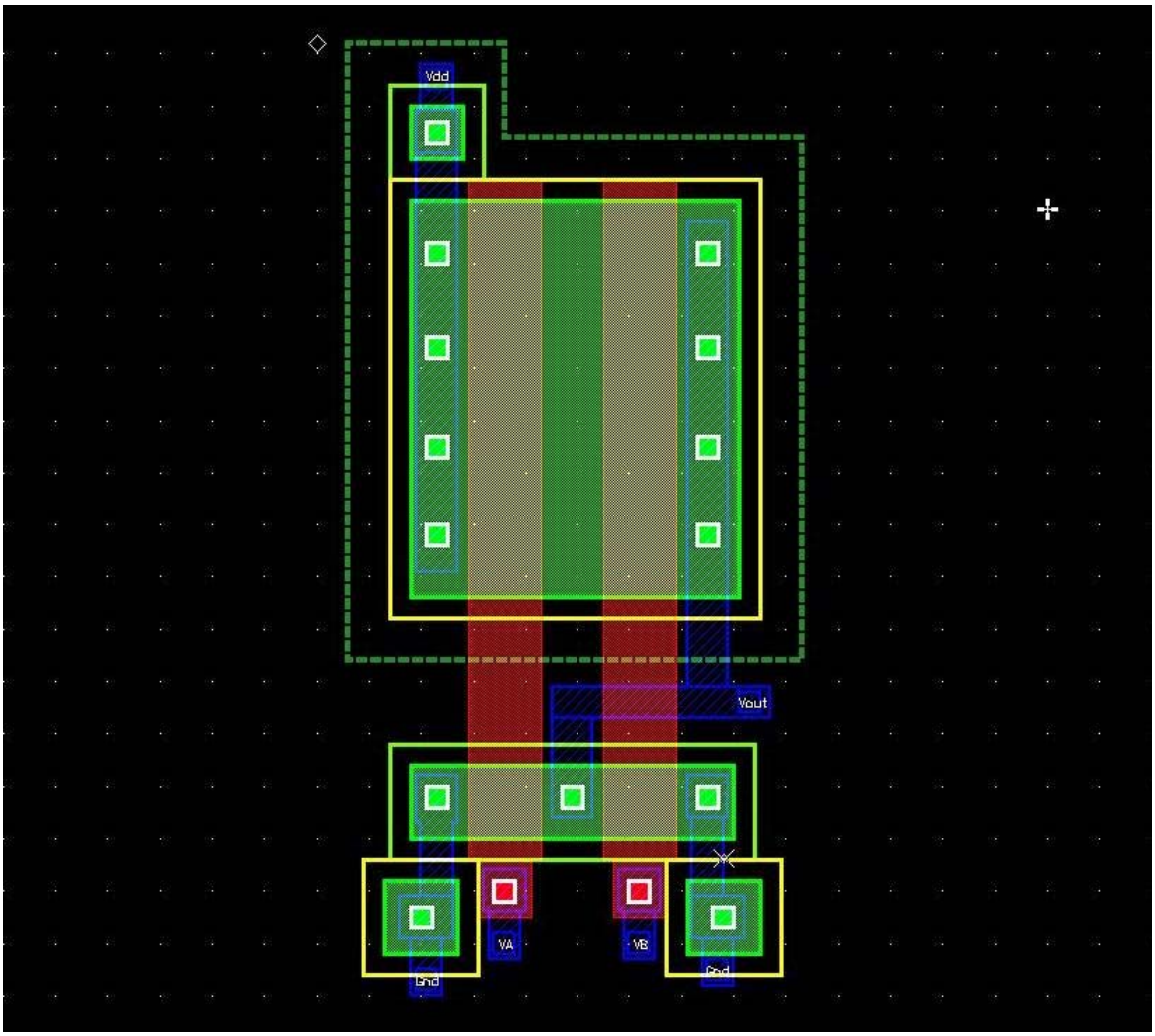


Figure 6.3. Layout of Two-Input CMOS NOR Gate.

6.2.4 LAYOUT CELL DESIGN FOR A ONE-BIT CMOS FULL ADDER

The minimum-sized one-bit CMOS Full Adder is implemented as shown below in Figure 6.4. Here, the regular layout style is used in order to simplify the overall geometry and the signal routing. Note that in this initial adder cell layout, all the NMOS and PMOS transistors are placed in two parallel rows, between the horizontal power supply and the ground lines (metal).

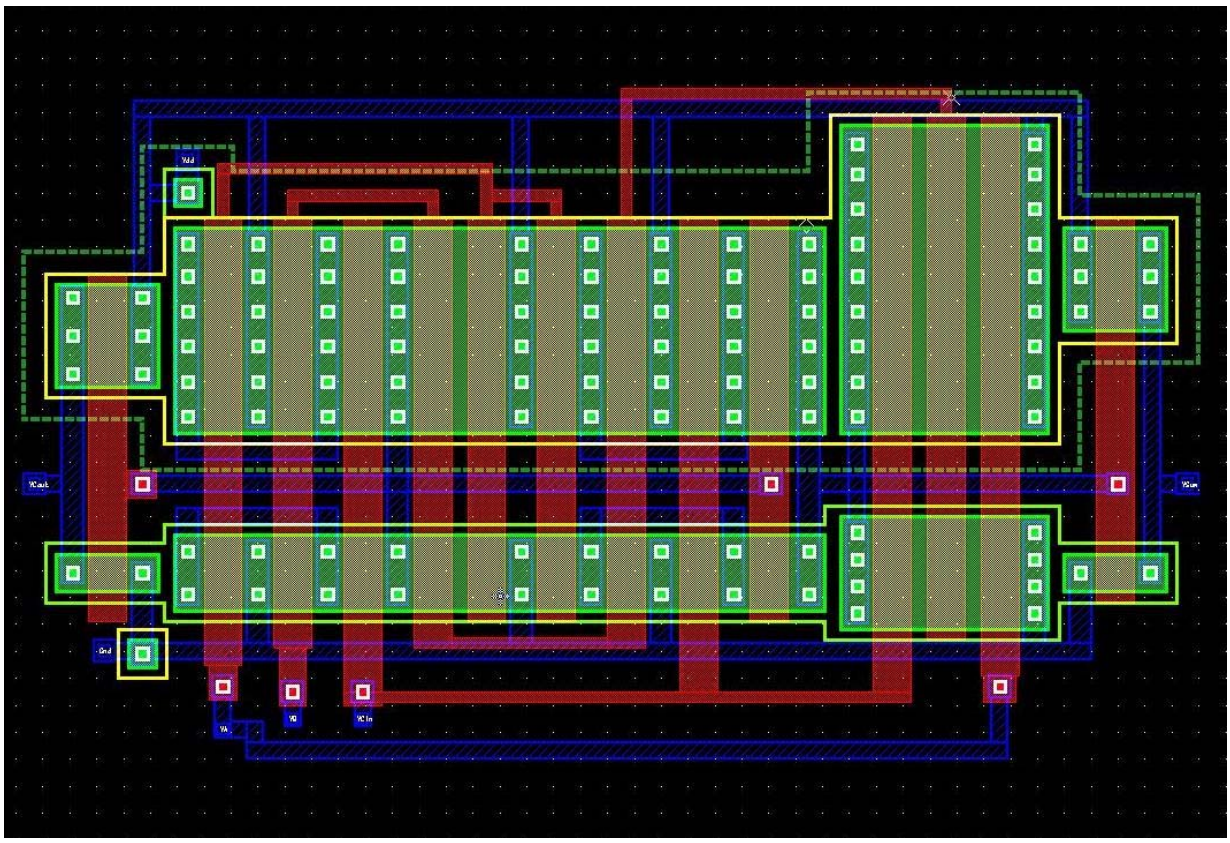


Figure 6.4. Layout of ONE-BIT CMOS FULL ADDER.

All the polysilicon lines are laid out vertically. The area between the n-type and p-type diffusion regions is used for running local metal interconnections (routing). The diffusion regions of the neighboring transistors have been merged as much as possible, in order to save the chip area.

6.2.5 LAYOUT CELL DESIGN FOR AN ADIABATIC PFAL BUFFER / INVERTER

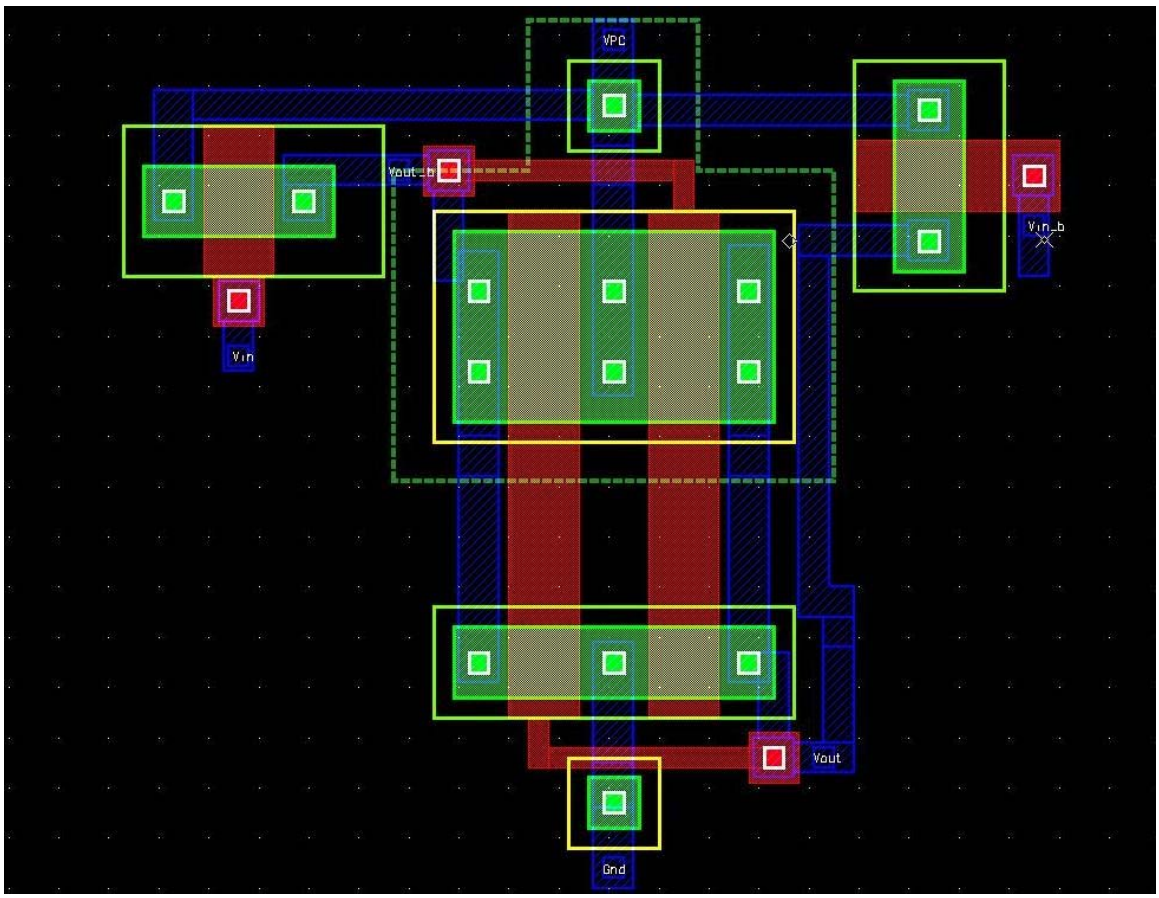


Figure 6.5. Layout of an Adiabatic PFAL Inverter.

6.2.6 LAYOUT CELL DESIGN FOR AN ADIABATIC PFAL AND / NAND GATE

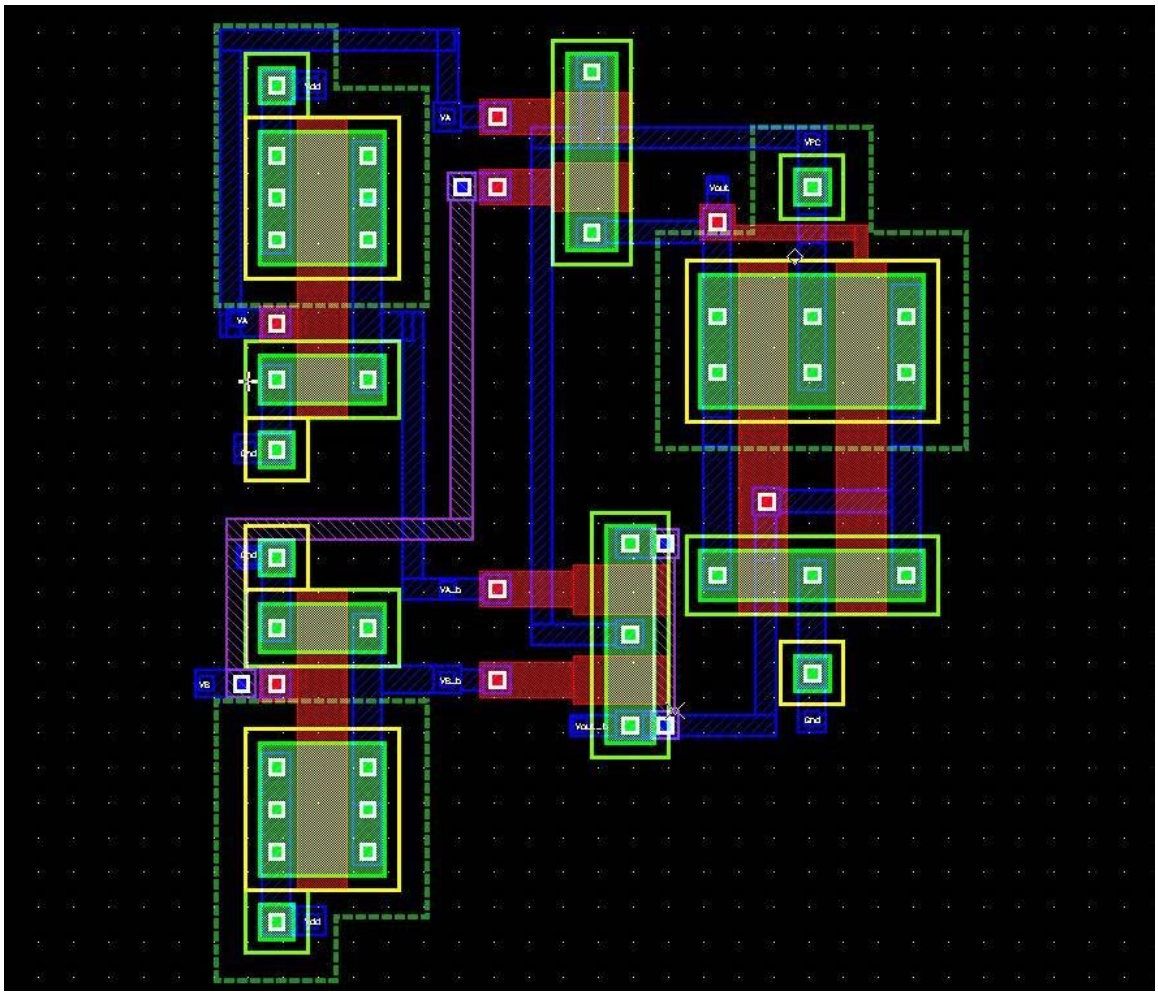


Figure 6.6. Layout of an Adiabatic PFAL Two-Input AND / NAND Gate.

6.2.7 LAYOUT CELL DESIGN FOR AN ADIABATIC PFAL OR / NOR GATE

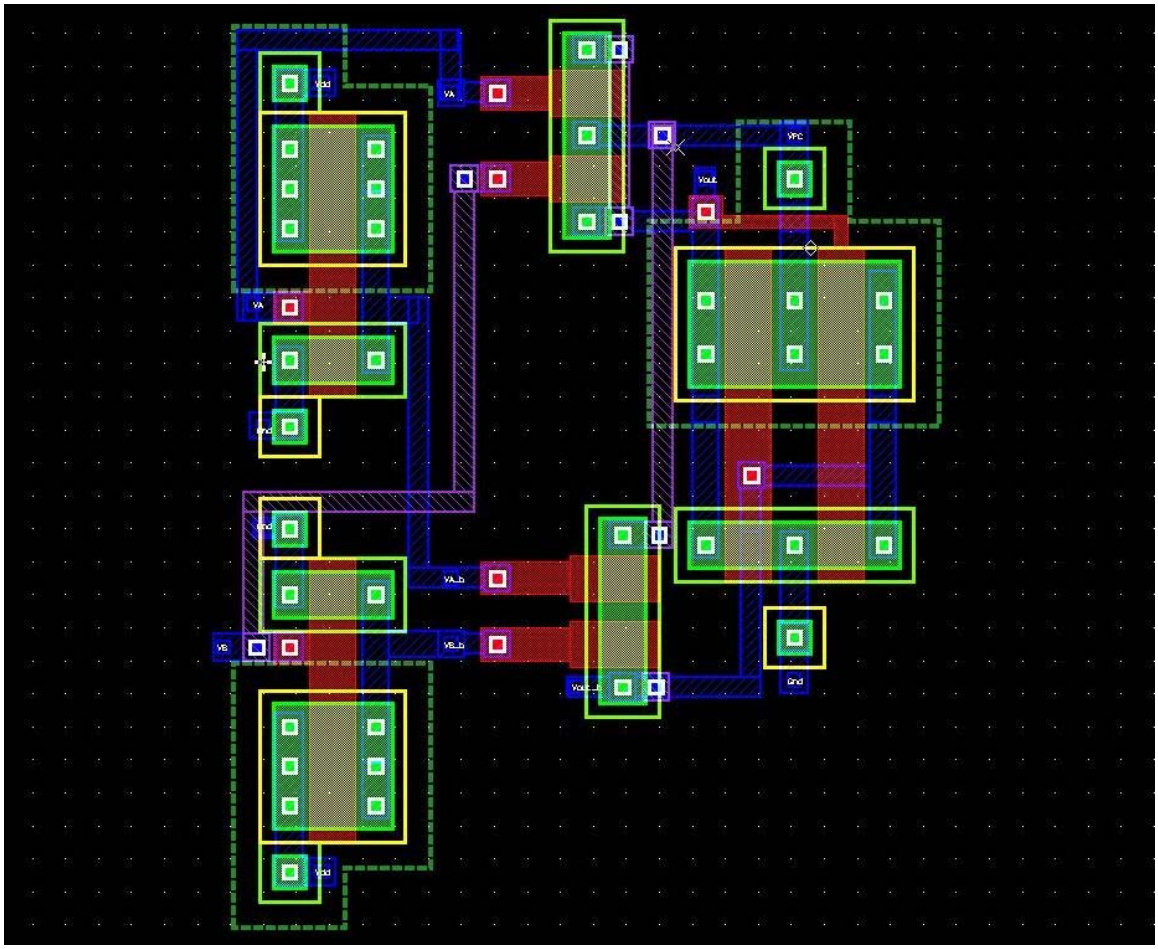


Figure 6.7. Layout of an Adiabatic PFAL Two-Input OR / NOR Gate.

6.2.8 LAYOUT CELL DESIGN FOR AN ADIABATIC PFAL ONE-BIT FULL ADDER

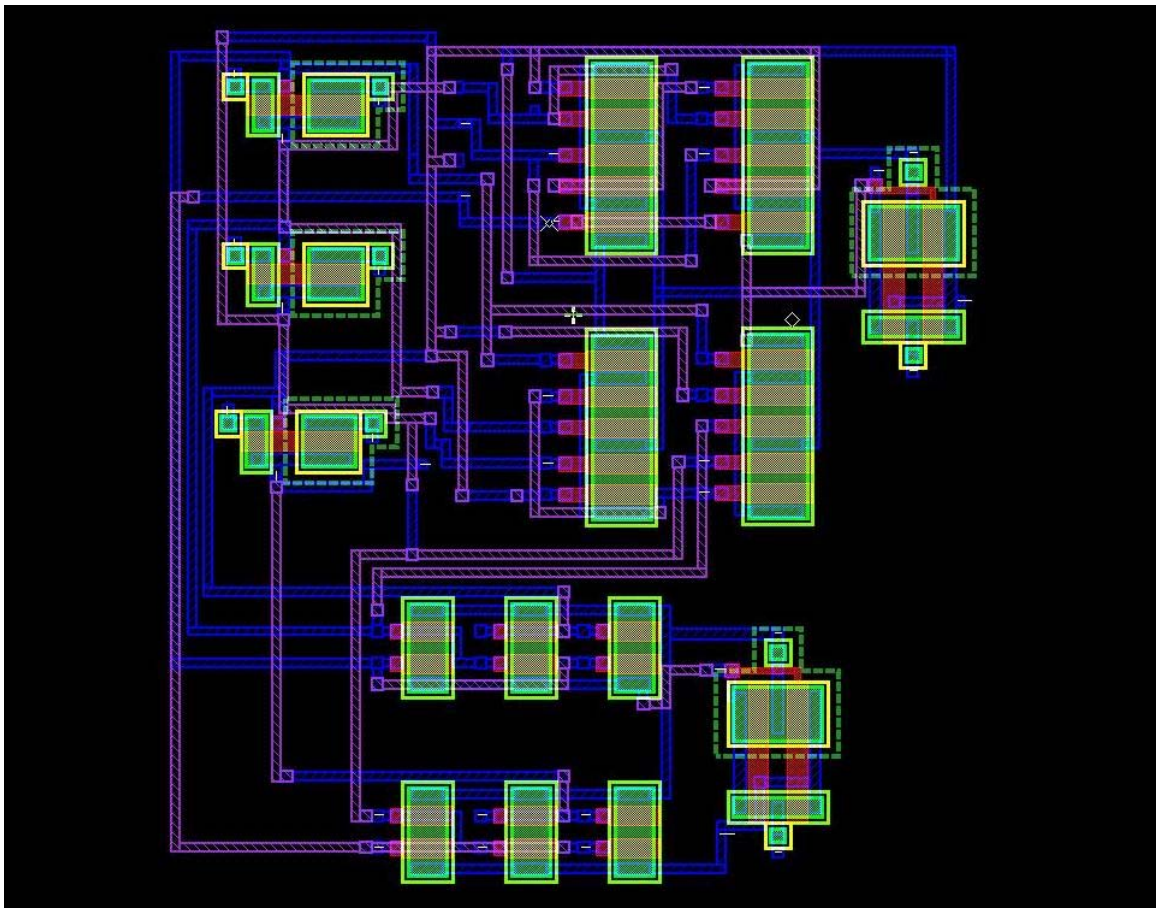


Figure 6.8. Layout of an Adiabatic PFAL One-Bit FULL ADDER.

6.3 POST - LAYOUT SIMULATIONS

After completing the physical layout design of all the cell structures, they are matched with schematic using LVS simulation. With the successful run of LVS, parasitic and layout netlist extraction simulation have been done using PEX. Post Layout simulations have been done on extracted netlist. The simulation results of post layout simulations are as given below.

6.3.1 POST - LAYOUT SIMULATION RESULTS FOR A CMOS INVERTER

Figure 6.9 below shows the post-layout result of the transient analysis for a minimum-sized CMOS Inverter.

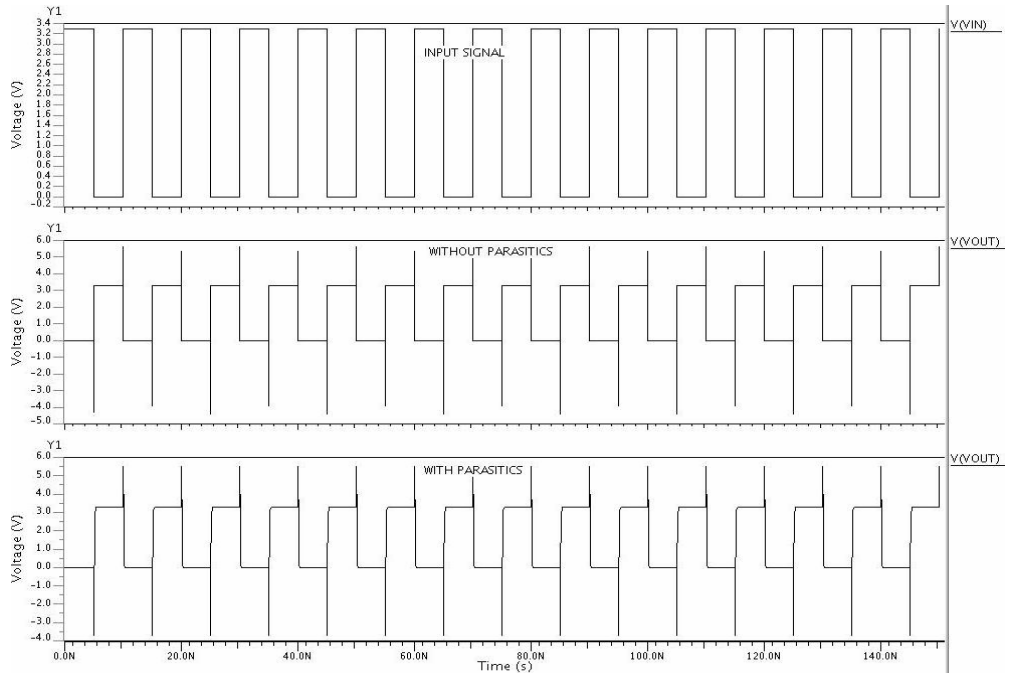


Figure 6.9. Post - Layout Simulation – Transient Analysis for CMOS Inverter.

6.3.2 POST - LAYOUT SIMULATION RESULTS FOR A TWO INPUT CMOS NAND GATE

Figure 6.10 below shows the post-layout result of the transient analysis for a two-input NAND gate.

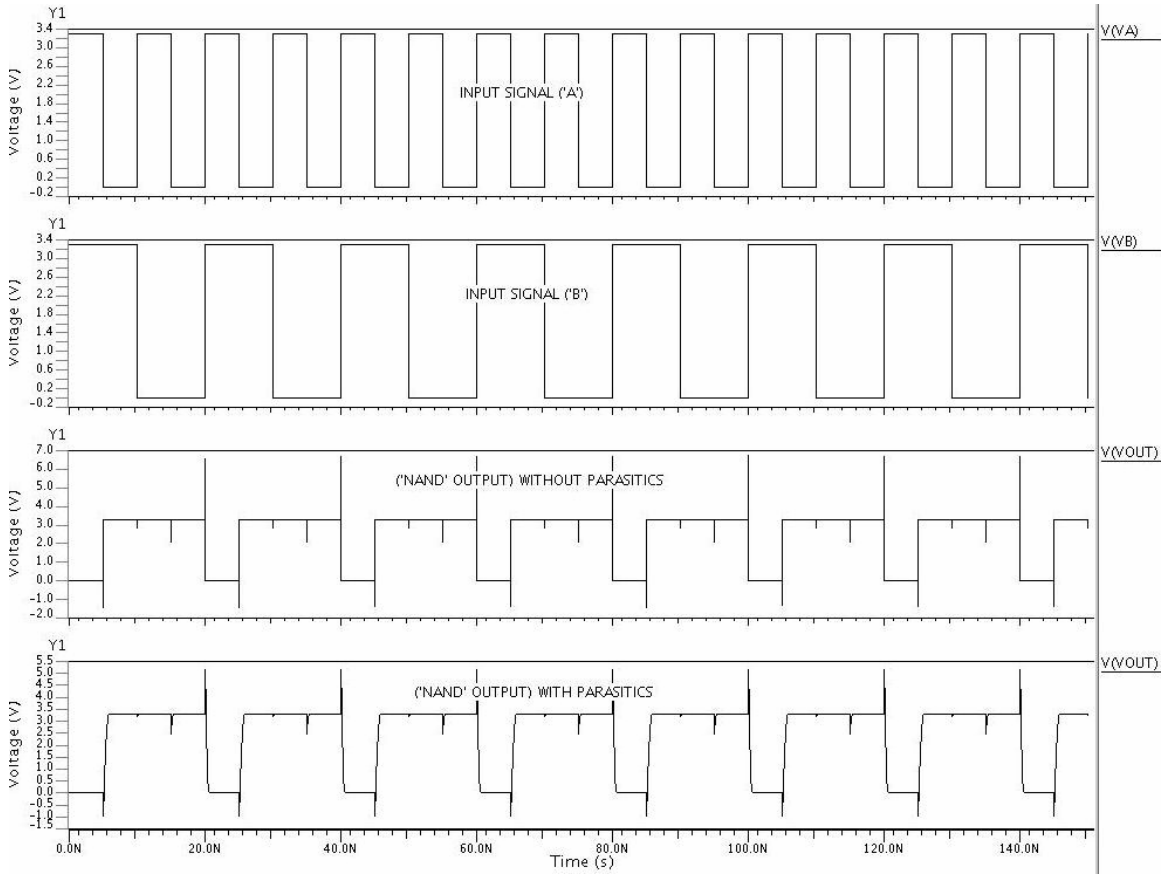


Figure 6.10. Post - Layout Simulation – Transient Analysis for a Two-Input CMOS NAND Gate.

6.3.3 POST - LAYOUT SIMULATION RESULTS FOR A TWO-INPUT CMOS NOR GATE

Figure 6.11 below shows the post-layout result of the transient analysis for a two-input NOR gate.

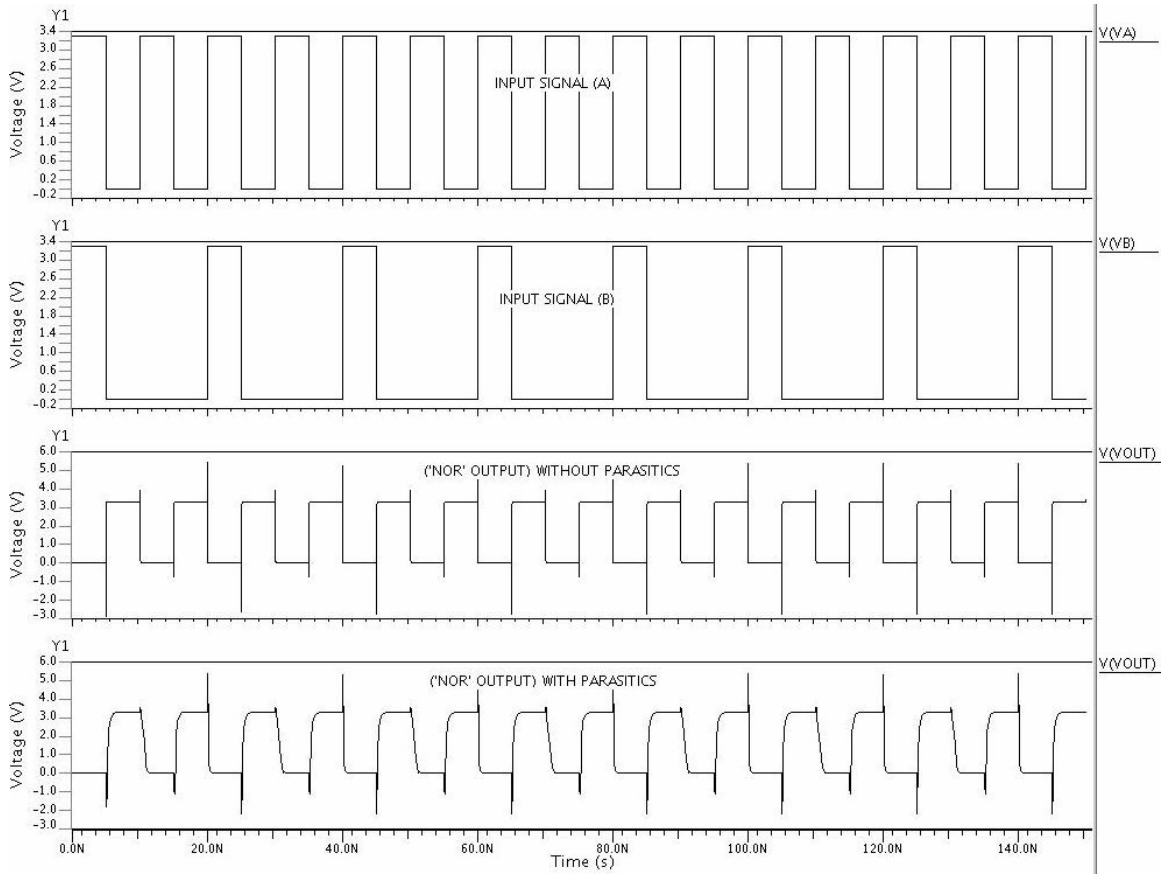


Figure 6.11. Post - Layout Simulation – Transient Analysis for Two-Input CMOS NOR Gate.

6.3.4 POST - LAYOUT SIMULATION RESULTS FOR ONE-BIT CMOS FULL ADDER

Figure 6.12 below shows the post-layout result of the transient analysis for a one-bit CMOS Full Adder.

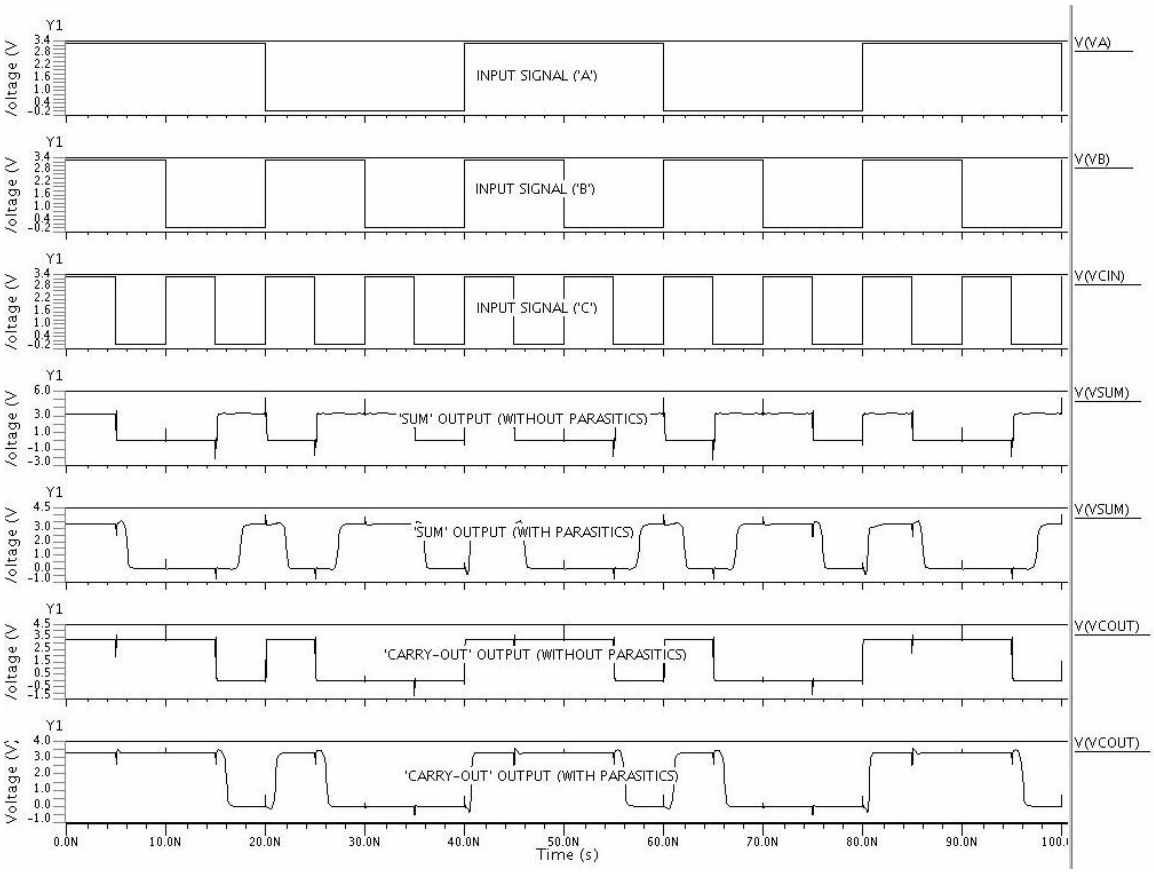


Figure 6.12. Post - Layout Simulation – Transient Analysis for One-Bit CMOS FULL ADDER.

6.3.5 POST - LAYOUT SIMULATION RESULTS FOR AN ADIABATIC PFAL BUFFER / INVERTER

Figure 6.13 below shows the post-layout result of the transient analysis for an Adiabatic PFAL buffer / inverter.

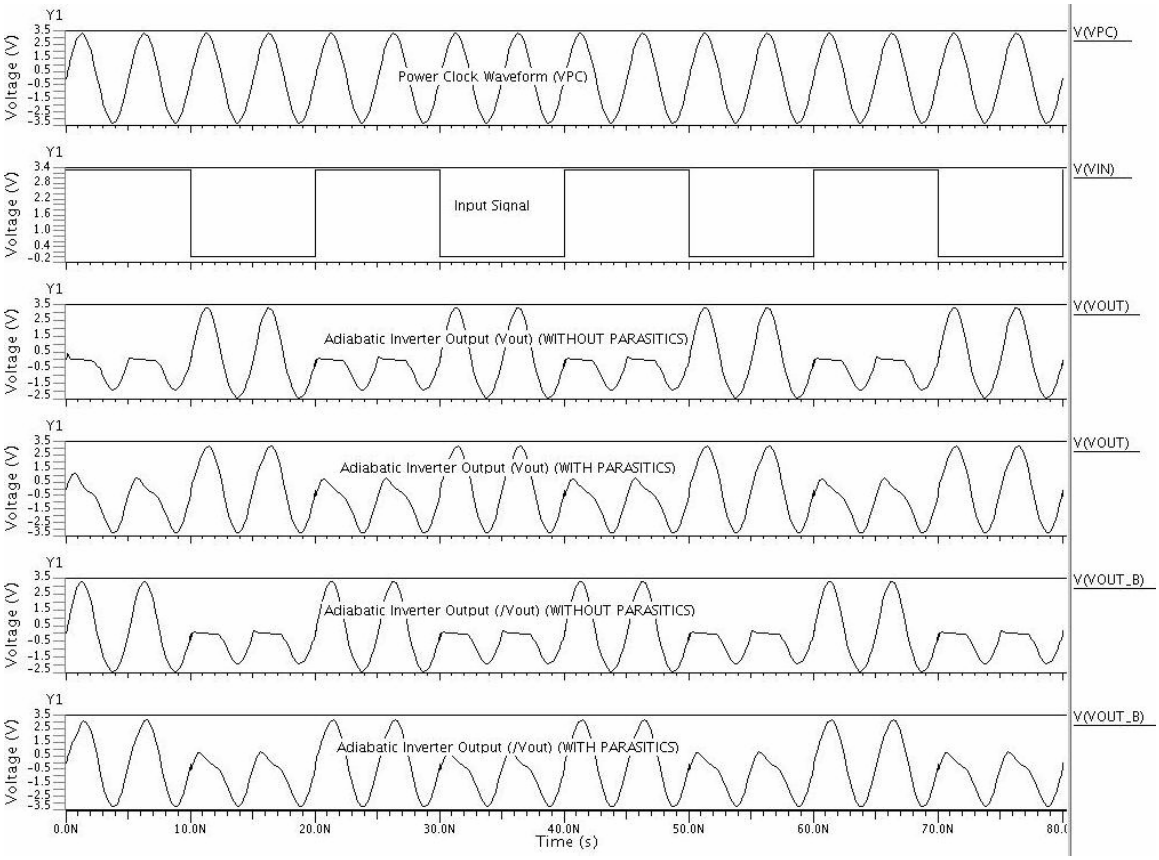


Figure 6.13. Post - Layout Simulation – Transient Analysis for an Adiabatic PFAL Inverter.

6.3.6 POST - LAYOUT SIMULATION RESULTS FOR AN ADIABATIC TWO-INPUT PFAL NAND GATE

Figure 6.14 below shows the post-layout result of the transient analysis for an Adiabatic PFAL two-input NAND gate.

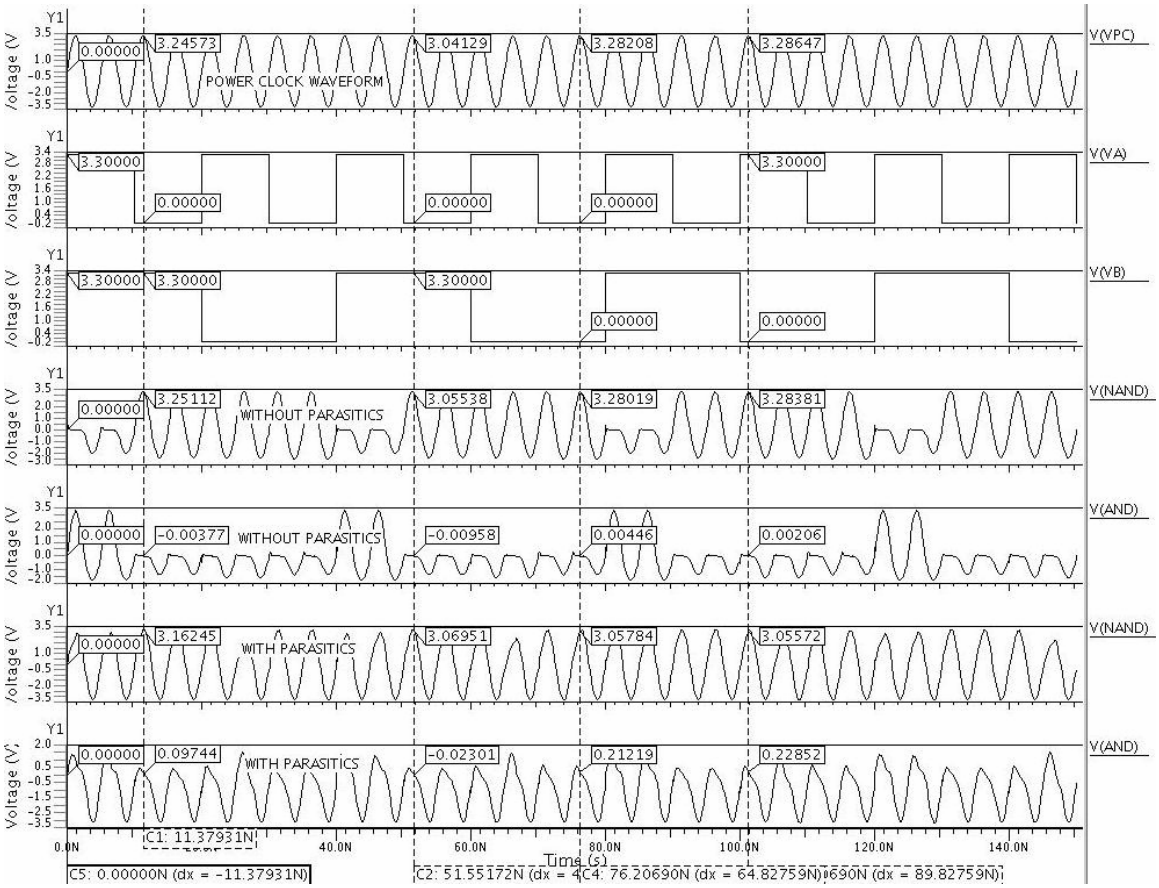


Figure 6.14. Post - Layout Simulation – Transient Analysis for an Adiabatic PFAL Two-Input AND / NAND Gate.

6.3.7 POST - LAYOUT SIMULATION RESULTS FOR AN ADIABATIC TWO-INPUT PFAL NOR GATE

Figure 6.15 below shows the post-layout result of the transient analysis for an Adiabatic PFAL two-input NOR gate.

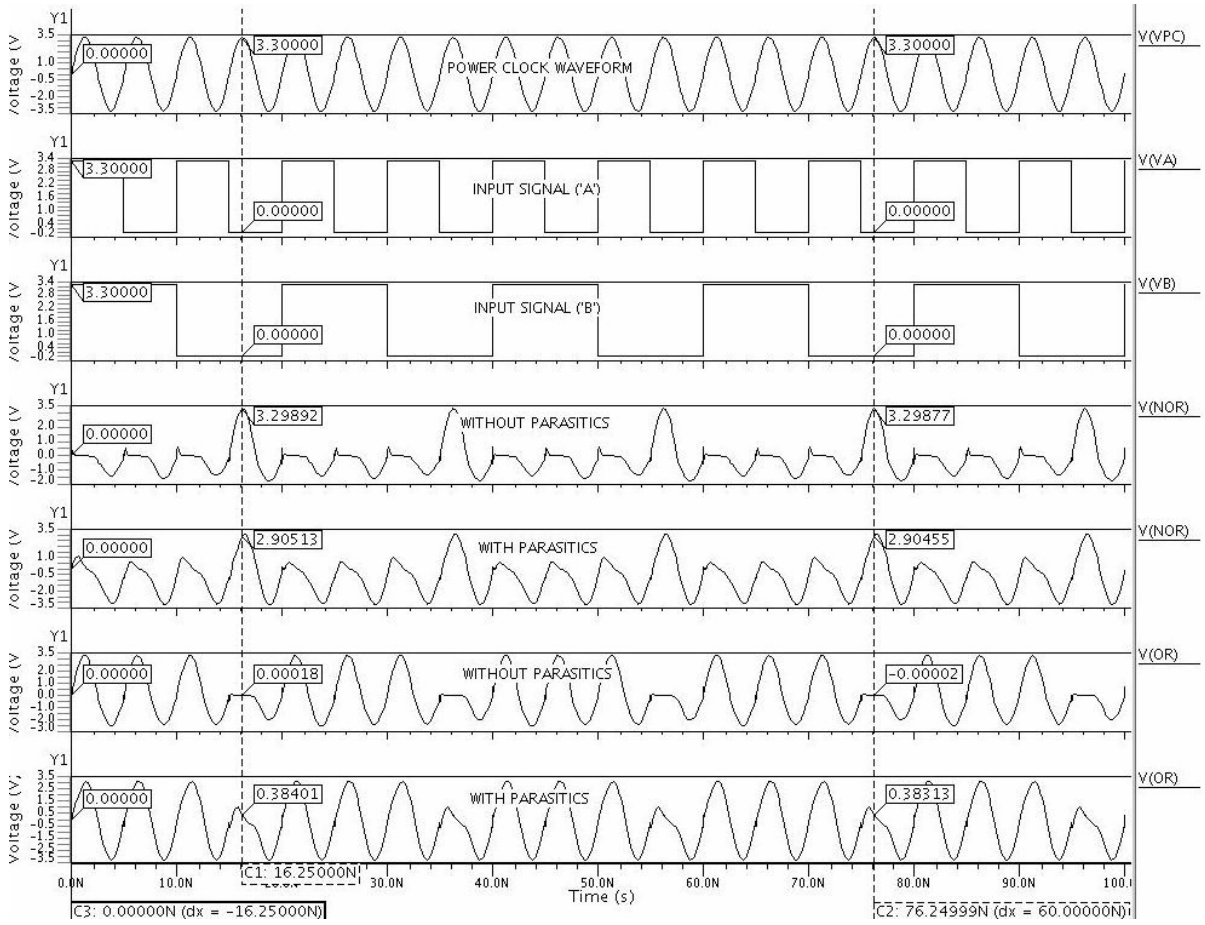


Figure 6.15. Post - Layout Simulation – Transient Analysis for an Adiabatic PFAL Two-Input OR / NOR Gate.

CHAPTER 7

CONCLUSIONS AND FUTURE SCOPE OF WORK

7.1 CONCLUSIONS

The thesis primarily was focused on the design of low power CMOS cell structures, which is the main contribution of this work. The design of low power CMOS cell structures uses fully complementary CMOS logic style and an adiabatic PFAL logic style. The basic principle behind implementing various design units in the two logic styles is to compare them with reference to the average power dissipated by all of them.

A family of full-custom conventional CMOS Logic and an Adiabatic Logic units were designed in Mentor Graphics IC Design Architect using standard TSMC 0.35 μm technology, layout them in Mentor Graphics IC Station and the analysis of the average dynamic power dissipation with respect to the frequency and the load capacitance was done. It was found that the adiabatic PFAL logic style is advantageous in applications where power reduction is of prime importance as in high performance battery-portable digital systems running on batteries such as note-book computers, cellular phones and personal digital assistants.

With the adiabatic switching approach, the circuit energies are conserved rather than dissipated as heat. Depending on the application and the system requirements, this approach can be used to reduce the power dissipation of the digital systems. With the help of adiabatic logic, the energy savings of upto 76 % to 90 % [15] can be reached.

Circuit simulations show that the adiabatic design units can save energy by a factor of 10 at 50 MHz and about 2 at 250 MHz, as compared to logically equivalent conventional CMOS implementation.

7.2 FUTURE SCOPE OF WORK

This section summarizes a few potential future directions for this work.

(a) ADIAMEMS: To perform digital logic in CMOS in a truly adiabatic (asymptotically thermodynamically reversible) fashion requires that the logic transitions be driven by a quasi-trapezoidal (flat-topped) power-clock voltage waveform, which must be generated by a resonant element with very high *Q* (quality factor). Recently, MEMS resonators have attained very high frequencies and *Q* factors and are becoming widely used in communications system-on-chip (SOC) for RF signal filtering, amplification, etc.

(b) APPLICATION OF NANO-TECHNOLOGY: Carbon nano-tubes grown using Chemical Vapor Deposition (CVD) can be selected to conform to a spiraling shape. Thus, a good quality factor *Q* can be achieved. The work left to be done for this design would include a method for causing it to keep its form, since nano-tubes are typically not rigid. Also, putting the tube to use in a circuit would lower the effective *Q* due to the junction discontinuities.

(c) SPACECRAFT: The high cost-per-weight of launching computing-related power supplies, solar panels and cooling systems into orbit imposes a demand for adiabatic power reduction in spacecraft in which these components weigh a significant fraction of total spacecraft weight.

REFERENCES

[1] A. P. CHANDRAKASAN, S. SHENG, AND R. W. BRODERSEN, "Low Power CMOS Digital Design," *IEEE Journal of Solid-state Circuits*, Vol. 27, No. 04, pp. 473-484, April 1999.

[2] H. J. M. VEENDRICK, "Short-circuit Dissipation of Static CMOS Circuitry and its Impact on the Design of Buffer Circuits," *IEEE JSSC*, pp. 468-473, August 1984.

[3] J. M. RABAEY, AND M. PEDRAM, "*Low Power Design Methodologies*," Kluwer Academic Publishers, 2002.

[4] M. HOROWITZ, T. INDENNAUR, AND R. GONZALEZ, "Low Power Digital Design, "*Technical Digest IEEE Symposium Low Power Electronics*, San Diego, pp. 08-11, October 1994.

[5] T. SAKURAI AND A. R. NEWTON, "Alpha-Power Law MOSET Model and its Applications to CMOS Inverter Delay and other Formulas," *IEEE JSSC*, vol. 25, no. 02, pp. 584- 594, October 1990.

[6] A. P. CHANDRAKASAN AND R. W. BRODERSEN, *Low-power CMOS digital design*, Kluwer Academic, Norwell, Ma, 1995.

[7] SUNG-MO KANG AND YUSUF LEBLEBICI, *CMOS Digital Integrated Circuits - Analysis and Design*, McGraw-Hill, 2003.

[8] J. S. DENKER, "A Review of Adiabatic Computing," *Technical Digest IEEE Symposium Low Power Electronics*, San Diego, pp. 94-97, October 1994.

[9] T. GABARA, "Pulsed Power Supply CMOS," *Technical Digest IEEE Symposium Low Power Electronics*, San Diego, pp. 98- 99, October 1994.

[10] B. VOSS AND M. GLESNER, "A Low Power Sinusoidal Clock," *In Proc. of the International Symposium on Circuits and Systems*, ISCAS 2001.

[11] W. C. ATHAS, J. G. KOLLER, L. SVENSSON, "An Energy- Efficient CMOS Line Driver using Adiabatic Switching," *Fourth Great Lakes symposium on VLSI*, California, March 2005.

[12] T. INDERMAUER AND M. HOROWITZ, "Evaluation of Charge Recovery Circuits and Adiabatic Switching for Low Power Design," *Technical Digest IEEE Symposium Low Power Electronics*, San Diego, pp. 102-103, October 2002.

[13] Y. MOON AND D. K. JEONG, "An Efficient Charge Recovery Logic Circuit," *IEEE JSSC*, Vol. 31, No. 04, pp. 514-522, April 1996.

[14] A. KAMER, J. S. DENKER, B. FLOWER, *et al*., "2N2D-order Adiabatic Computation with 2N-2P and 2N-2N2P Logic Circuits," *In Proc. of the International Symposium on Low Power design*, Dana Point, pp. 191-196, 1995.

[15] A. BLOTTI AND R. SALETTI, "Ultralow- Power Adiabatic Circuit Semi-Custom Design," *IEEE Transactions on VLSI Systems*, vol. 12, no. 11, pp. 1248-1253, November 2004.

[16] S. YOUNIS, T. KNIGHT, "Asymptotically Zero Energy Split-Level Charge Recovery Logic. *Proceedings Workshop Low Power Design*, Napa Valley, California 1994, pp. 177- 182.

[17] DRAGAN MAKSIMOVIC´, G. VOJIN, OKLOBDŽIJA, BORIVOJE NIKOLIC´ AND K. WAYNE CURRENT, "Clocked CMOS Adiabatic Logic with Integrated Single-Phase Power-Clock Supply," *IEEE Transactions on VLSI Systems*, Vol. 08, No. 04, pp. 460-463, August 2000.

[18] A. BLOTTI, S. PASCOLI, AND R. SALETTI, "Sample Model for Positive Feedback Adiabatic Logic Power Consumption Estimation," *Electronics Letters*, Vol. 36, No. 2, pp. 116-118, Jan. 2000.

[19] C. HU, "Future CMOS Scaling and Reliability," *Proceedings IEEE*, Vol. 81, No. 05, pp. 682-689, February 2004.

[20] W. C. ATHAS, L. SVENSSON, J. KOLLER, N. TZARTZANIS, AND Y. CHOU, "Low Power Digital Systems based on Adiabatic Switching Principles," *IEEE Trans. on VLSI Systems*, Vol. 2, No. 4, pp. 398-406, Dec. 1994.

[21] SAED G. YOUNIS, "Asymptotically Zero Energy Computing Using Split-Level Charge Recovery Logic," PhD thesis, 1994.

[22] MICHAEL P. FRANK AND MARCO OTTAVI, "Energy Transfer and Recovery Efficiencies for Adiabatic Charging with various driving waveforms," Research Memo, 2006.

[23] KAUSHIK ROY, SHARAT C. PRASAD, *Low-Power CMOS VLSI Circuit Design*, John Wiley & Sons, Inc, 2000.

[24] KAUSHIK ROY, YIBIN YE, *Ultra Low Energy Computing using Adiabatic Switching Principle*, ECE Technical Reports, Purdue University, Indiana, March, 1995.

[25] MOSIS: MOS Integration Service. Available online: www.mosis.org

APPENDIX A

MOSIS SPICE LEVEL – 53 MOS MODEL PARAMETERS FOR A STANDARD N-WELL CMOS TECHNOLOGY

This appendix includes the SPICE BSIM3v3 Version 3.1 MOS model parameters for TSMC 0.35 μm CMOS Technology process from MOSIS [23].

(A) MODEL PARAMETERS FOR N-MOS TRANSISTORS.

+VERSION = 3.1	TNOM = 27	TOX = 7.8E-9
+XJ = 1E-7	NCH = 2.2E17	VTH0 = 0.5490813
+K1 = 0.5749179	K2 = 0.0163016	K3 = 86.4438467
+K3B = -2.4838433	W0 = 2.749916E-5	U0 = 421.3862314
+ UA = -1.41643E-10	UB = 1.752303E-18	UC = 3.989584E-11
+ VSAT = 1.583891E5	A0 = 1.2236736	A1 = 0
+ A2 = 0.4476846	B0 = 1.038291E-6	B1 = 5E-6
+ KETA = 5.546028E-3	CDSC = 2.4E-4	CDSCD = 0
+DELTA = 0.01	CGDO = 2.91E-10	CGSO = 2.91E-10
+CGBO = 1E-12	CJ = 1.003925E-3	PB = 0.8
+MJ = 0.3422887	CJSW = 3.505428E-10	PBSW = 0.8
+MJSW = 0.1352212	CJSWG = 1.82E-10	PBSWG = 0.8
+MJSWG = 0.1352212	WKETA = -5.618765E-3	LKETA = -2.160521E-3

(B) MODEL PARAMETERS FOR P-MOS TRANSISTORS.

+VERSION = 3.1	TNOM = 27	TOX = 7.8E-9
+XJ = 1E-7	NCH = 8.52E16	VTH0 = -0.6807607
+K1 = 0.4403339	K2 = -0.0138626	K3 = 54.9133679
+K3B = -5	W0 = 5.301139E-6	U0 = 155.5194682
+ UA = 1E-10	UB = 1.979139E-18	UC = -1.38347E-11
+ VSAT = 1.789066E5	A0 = 1.103255	A1 = 5.697551E-4
+ A2 = 0.3	B0 = 2.551996E-6	B1 = 5E-6
+ KETA = -7.333027E-3	CDSC = 2.4E-4	CDSCD = 0
+DELTA = 0.01	CGDO = 2.49E-10	CGSO = 2.49E-10
+CGBO = 1E-12	CJ = 1.433541E-3	PB = 0.99
+MJ = 0.5527511	CJSW = 4.291576E-10	PBSW = 0.99
+MJSW = 0.3523334	CJSWG = 4.42E-11	PBSWG = 0.99
+ MJSWG = 0.3523334	WKETA = 3.20553E-3	LKETA = -1.413928E-4

BIOGRAPHICAL SKETCH

Sanjay Kumar was born in Dehradun, Uttaranchal, India in October 1981. He received his Bachelor of Engineering (B.E.) degree with Honors in Electronics and Communication Engineering from Dehradun Institute of Technology, Dehradun, India in June 2003. Thereafter he worked for one year as a Faculty Member in the Department of Electronics and Communication Engineering at Dehradun Institute of Technology, Dehradun. He joined the graduate program in VLSI Design and CAD at Thapar University, Patiala, India in August 2004. His focus has been on VLSI Circuit Design and Low Power VLSI Design of Digital Systems. In January 2006, he started his professional and research career in Indian Space Research Organization (ISRO), Bangalore, India as a Scientist 'C' working towards the India's First Moon Mission 'Chandrayaan'. While working towards his Master's degree, he worked on his thesis under the guidance of Mrs. Alpana Agarwal, Assistant Professor, Thapar University, Patiala, India. He plans to continue his graduate studies towards earning the doctorate degree. His research interests include Low Power Design of VLSI Circuits and Systems, Nanoscale Device Design, Modeling and Characterization. He is also interested in emerging, silicon and non-silicon based nanotechnologies, Carbon-based Electronics, Organic Electronics. Currently he is a Faculty Member in the Department of Electronics and Communication Engineering, Thapar University, Patiala, India. He can be reached via his email address, er.sanjaykumar@gmail.com, sanjaykumar0810@yahoo.co.in.