DESIGN AND ANALYSIS
OF
CURRENT DIFFERENCING TRANSCONDUCTANCE AMPLIFIER

A Thesis Submitted in Partial Fulfilment of the Requirement for the Award of the Degree of

MASTER OF TECHNOLOGY

In

VLSI Design

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JULY, 2018

DECLARATION

I, Raviraj Kour hereby declare that the work presented in this thesis entitled **"Design and Analysis of Current Differencing Transconductance Amplifier"** in partial fulfilment of the requirement for the award of degree of Master of Technology in VLSI Design submitted at Electronics and Communication Engineering Department, Thapar Institute of Engineering & Technology (Deemed to be University), Patiala is an authentic record of work carried out under supervision of **Dr. Rishikesh Pandey**, Assistant Professor, ECED, Thapar Institute of Engineering & Technology (Deemed to be University), from 2017 to 2018. The matter presented in this has not been submitted either in part or full to any other university or institute for the award of any other degree.

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ACKNOWLEDGEMENT

This report has only been possible with the constant guidance and expertise of Dr. Rishiskesh Pandey, Assistant Professor, Electronics and Communication Engineering Department, Thapar Institute of Engineering & Technology (A Deemed To Be University), Patiala and I would like to take this opportunity to express my sincere gratitude to him.

I am also thankful to Dr. Alpana Agarwal, Head of ECE Department, for providing us the adequate infrastructure for carrying out the work.

I am also thankful to Dr. Hem Dutt Joshi, PG Coordinator as well as Dr. Anil Arora, Program Coordinator and the entire faculty and staff of Electronics and Communication Engineering Department for the motivation and inspiration that triggered me for the work.

I am also thankful to Dr. Shireesh Kumar Rai, Assistant Professor, Electronics and Communication Engineering Department, Thapar Institute of Engineering & Technology (A Deemed To Be University), Patiala for his constant guidance throughout my work.

I would also like to thank my friends who always motivated me and have more or less contributed to the preparation of this report. I will be always indebted to them.

Last but not the least, I would like to thank my parents for their years of unyielding love and encouragement. They have always wanted the best for me and I admire their determination and sacrifice.

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ABSTRACT

The current-mode devices play a vital role in the designing of the analog signal processing applications. Since the introduction of these devices, the continuous improvement in the performance parameters has been the most important aspect of research. As current differencing transconductance amplifier (CDTA) is used as a versatile circuit for designing different applications of analog signal processing like filters, oscillators, Schmitt triggers, monostable multivibrators etc., hence there has been a need of enhancing the performance of conventional CDTA. If all the performance parameters of the CDTA, the transconductance plays the most important role in deciding the performance of the designed applications and thus the enhancement of transconductance of CDTA is required while keeping in mind the other parameters.

Thus, this research works includes the techniques to boost the transconductance of the conventional current differencing transconductance amplifier. Four different circuits to enhance the transconductance are proposed. All these circuits use a common source amplifier and merged it with some of the techniques to boost the transconductance. The different techniques applied are the use of parallel n-MOSFETs in the differential pair and a pair of cross-coupled n-MOSFETs across the differential pair. All the circuits are operated at the supply voltages of ±0.9 V. The comparison between all the proposed circuits is also done on the basis of transconductance and dynamic power and the best circuit was chosen as PCCDTACS. The maximum transconductance of 6.75 mS was achieved for PCCDTACS at a bias current of 200μA with the dynamic power of 3.44 mW. The proposed circuits have been designed and simulated in Cadence Virtuoso Analog Design Environment using BSIM3V3 180 nm CMOS technology. The comparison of the proposed PCCDTACS circuits with circuits available in literature shows that the proposed PCCDTACS circuit can be extensively used in the designing of analog signal processing applications.

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LIST OF ACRONYMS

OTA	Operational Transconductance Amplifier
CCII	Second generation Current Conveyors
CDBA	Current Differencing Buffered Amplifier
CDTA	Current Differencing Transconductance Amplifier
CDU	Current Differencing Unit
FVF	Flipped Voltage Follower
MCDCTA	Multifunction Current Differencing Cascaded Transconductance Amplifier
DCCCS	Differential Current Controlled Current Source
MOCDTA	Multi Output Current Differencing Transconductance Amplifier
TBCDTA	Transconductance Boosted Current Differencing Transconductance Amplifier
DC	Direct Current
AC	Alternating Current
CDTACS	Current Differencing Transconductance Amplifier with Common Source amplifier
CS	Common Source
KHN	Kerwin-Huelsman-Newcomb
HP	High-Pass
LP	Low-Pass
BP	Band-Pass
PCDTACS	Current Differencing Transconductance Amplifier with Common Source amplifier and Parallel n-MOSFETs
CCDTACS	Current Differencing Transconductance Amplifier with Common Source amplifier and Cross-coupled n-MOSFETs
PCCDTACS	Current Differencing Transconductance Amplifier with Common Source amplifier, Cross-coupled n-MOSFETs and Parallel n-MOSFETs
CMOS	Complementary Metal-Oxide-Semiconductor

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CHAPTER 1

INTRODUCTION

The voltage-mode devices have dominated the field of the analog signal processing for many years. The performance of these circuit was determined by the voltage levels at the input and output nodes. But these circuits suffer from the disadvantages like no sudden change in the output voltage when the input voltage suddenly changes because of the stray and other parasitic capacitances, low bandwidth due to unity gain bandwidth in the operational amplifier based circuits, dependence of the slew rate on time constants of the circuit, low voltage swings, high voltage supply for better signal-to-noise ratio etc. Thus, voltage-mode devices were not suitable for high frequency applications because a dominant pole is created by the high valued resistance at the low frequency which limits the bandwidth of the circuit. Therefore, the voltage-mode devices are being replaced by the current-mode devices. From the last few decades current-mode devices are being extensively used in this field of analog signal processing because of the advantages they offer over their counterparts. Some of the advantages of the current-mode devices are better linearity, wider bandwidth which is independent of the closed loop gain of the circuit, high slew rate, larger dynamic range of operation, less power consumption, lesser number of passive components to perform a specific function, better feedback mechanism etc. For these reasons, the current-mode devices have dominated the field of analog designing from past few decades. Some of the current-mode active building blocks introduced to meet these properties are operational transconductance amplifier (OTA) [1], current conveyors [2-4] (CCII) [5] and current differencing buffered amplifier [6]. Since the introduction of the current differencing buffered amplifier (CDBA), it has been considered as the most active building block for the designing of analog circuits. It consists of current-mode and voltage-mode unity gain amplifiers. The circuit offered a wide bandwidth and larger dynamic range when compared to the second generation current conveyors but the voltage-mode of operation served as the main disadvantage to the CDBA amplifier. Hence, they were replaced by the current differencing transconductance amplifier. Some of the other problems include the high input impedance and high parasitics in the circuits based on CDBA and OTA. These circuits also suffered from the problem of impedance matching when they were cascaded. To overcome these problems, a new current-mode active building block, namely Current Differencing Transconductance Amplifier (CDTA) has been recently introduced [7] by Biolek. The CDTA is a combination of well-known advantages of current differencing buffered amplifier along with the transconductance amplifier to achieve the implementation of the current-mode filters. It is most versatile and popular current-mode device used in almost all the analog signal processing applications like filters, oscillators, Schmitt trigger, waveform generators etc.

The CDTA is composed of two structures the current differencing unit (CDU) and operational transconductance amplifier (OTA) [1]. The block diagram of conventional CDTA circuit is shown in Figure 1.1. The CDU is a current differencing unit. The currents Ip and In are applied as inputs to the

input terminals of them to pass through a current mirror network. The current is then converted to the voltage at the output terminal of CDU i.e. the Z terminal by connecting a resistance (Rz). The output current of current differencing unit is equal to the difference between the input currents Ip and In. The voltage produced at the output of CDU is then given as input to the operational transconductance amplifier. The OTA comprises of the differential pair and few current mirrors. The output of the CDTA is in the form of two currents Ix+ and Ix- generated at the two output terminals of the OTA.

Thus, the CDTA can be considered as a five terminal device with two input and two output terminals and one intermediate terminal. The CDTA has low input impedance and high output impedance because of this reason it is considered as the most versatile element in the field of analog signal processing applications.

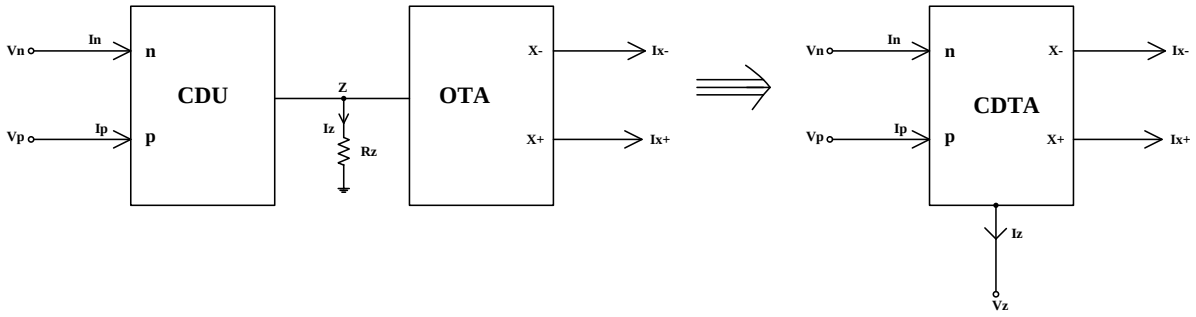


Figure 1.1 Block Diagram of CDTA

1.1 MOTIVATION

Since the introduction of applications based on analog signal processing, the voltage-mode circuits have dominated but as timed passed, there has been a tremendous modifications in the conventional circuits. The voltage-mode circuits suffered from many drawbacks and thus recently, they were replaced by the current-mode circuits as they have noted advantages. Thus, the current-mode circuits have almost replaced their voltage counterparts. Some of the current-mode circuits are the operational transconductance amplifier, current conveyors and current differencing buffered amplifier.

All these voltage mode circuits suffered from the disadvantages like low bandwidth, high signal-to-noise ratio, low frequency of operation etc. so, they were replaced by a new active current-mode element known as CDTA. From the past few decades, the CDTA has been considered as the most commonly used current-mode active element in the field of analog signal processing. The modifications in the basic structures of the CDTA to enhance the performance parameters of the circuit such as input impedance, bandwidth, linearity, output impedance, low power consumption, electrical tuning capability, transconductance etc. has been a topic of research from the past few years.

To improve the bandwidth and input impedance of the circuit, a flipped voltage follower circuit [8-10] has been used in the CDU unit of conventional CDTA. Although, the circuit offered the noted advantages but also lead to the disadvantages of larger MOSFET sizes and DC offset. A differential

current controlled current source [11] had the better linearity but the disadvantages were limited transconductance and less tunability. Some other circuits to enhance the output impedance and the tuning capability of the circuit were the Z copy CDTA [12, 13], Modified CDTA [14], Multifunction cascaded CDTA [15] etc. Although, all these circuits helped in improvement of the conventional circuit of the CDTA but some of the disadvantages included complex design circuitry, no electrical tuning of frequency of oscillator etc. All these circuits improved some of the parameters of the circuits but the boosting of the transconductance has not been a topic of research lately. The conventional methods to enhance the transconductance lead the high power consumption, low voltage swings, lower bandwidth etc. thus there was a need to boost the transconductance of the CDTA as it serves as one of the most important parameter to control the center frequency of the filter and the frequency of the oscillator. But recently, some techniques to boost the transconductance were reported. Some of these are replacement of the differential pair of the OTA with the n-MOSFETs connected in parallel [16, 17], cross-coupled p-MOSFET based CDTA circuit [18] etc. But all these techniques suffered from the drawbacks of limited range of transconductance and higher power dissipation. Thus, the future research in this field can be in the context of boosting the transconductance of the OTA and thus enhancing the performance of the CDTA.

Therefore, the motivation behind the research work recorded in this report was to design a high transconductance based Current Differencing Transconductance Amplifier (CDTA) while keeping in mind the drawbacks of the proposed structures. A comparison of performance parameters of proposed high transconductance Current Differencing Transconductance Amplifier (CDTA) with the conventional ones is also presented. The advantages offered by proposed structure are also mentioned.

1.2 ORGANIZATION OF THE THESIS

Chapter 1 introduces some of the reasons for the use of current-mode devices instead of the conventional voltage-mode devices, few current-mode active elements along with the basic structural description of the conventional CDTA.

Chapter 2 presents a brief description of the research that has been reported in literature for the modification of conventional CDTA circuit and the CDTA based circuits used in the field of analog signal processing.

Chapter 3 describes the proposed Current Differencing Transconductance Amplifier circuits and their applications.

Chapter 4 addresses the simulation results of the proposed circuits. The simulation results have been compared with the similar circuits available in literature.

Chapter 5 concludes the report and also mentions the future possibilities to carry forward the research in this domain.

CHAPTER 2

LITERATURE SURVEY

This chapter aims at discussing the research work carried out on the conventional Current Differencing Transconductance Amplifier (CDTA) by various authors over the years. A number of the modifications have been done on the conventional CDTA to enhance its performance parameters. Different designs of the conventional CDTA have been introduced to modify the parameters of the circuit like input impedance, bandwidth, linearity, output impedance, low power consumption, electrical tuning capability, transconductance [8-21] etc.

A modified CDTA presented in [8] used a flipped voltage follower (FVF) based current-mode circuit in place of conventional current mirrors in the CDU. The FVF is made to work as a current sink. The circuit has a low input impedance because of the feedback provided by FVF. But the design had the disadvantage that the channel lengths of the MOSFETs had to be large to compensate the effects due to the Channel Length Modulation but increasing the size of the MOSFETs resulted in DC offset at the input stage. This in turn reduced the bandwidth of the circuit. One of the solutions to enhance the bandwidth was to use more accurate current mirror circuits but that lead to the high supply voltages, thus altering the configuration of the circuit.

Some of the disadvantages offered by the circuit briefed in [8] were removed by using a FVF structure to obtain the difference of input currents in the CDU region and a multi output OTA, as suggested in [9]. In this circuit, the FVF is used as a current follower circuit. The circuit offers the advantages of very low input impedance, very high output impedance, unity voltage and current gains, high bandwidth, low power consumption, transconductance tuning by using bias current, better dynamic range than the one designed in [8] and high accuracy.

The work presented by Maktoomi *et al.* [10] showed the modified version of the circuit described in [9]. The main difference between these circuits is that a current source and a current sink is used to perform the differencing action of the input currents. The current sink used is same as that used in [9] except the fact that no external voltage supply is applied. The current source consists of a dual flipped voltage follower cell. The complete CDTA circuit composed of three blocks i.e. a FVF which is configured as the current follower or current mirror and works as a current source, the current differencing stage which contains two similar FVF configured current followers, out of which one works as a current source and the difference of the current is taken at the node Z. The current sink is converted to the current source with the help of 'copy and invert' stage. This reduces the number of transistors as there is no need to use extra stage for performing the current differencing action. This results in better frequency response due to the reduction in the number of nodes in the circuit. The circuits offers the advantages of wider bandwidth and use of lesser number of transistors.

A Current Differencing Transconductance Amplifier was introduced by Alaybeyoglu *et al.* in [13]. The circuit consists of two stages i.e. the current differencing unit and dual output transconductance amplifier. CDTA differs in construction from the conventional CDTA by the fact that third generation

current conveyors were used to copy the current at the intermediate Z terminal, instead of the classical current mirrors. The circuit has two input terminals and four output terminals. The input impedances of the circuit are low and output impedances are high. The third generation current conveyor acts as an active floating current sensing element. The operation of current sensing is perfectly achieved with the current conveyors.

A current-mode active element named as the multifunction current differencing cascaded transconductance amplifier (MCDCTA) is reported in [15]. It is an independent and systematic building block which is the combination of current differencing buffered amplifier and the operational transconductance amplifier. MCDCTA greatly improves the flexibility and accuracy of current-mode circuit designs. By cascading two inputs and (n+1) transconductance amplifiers, a MCDCTA can be designed to operate as a lossy integral and a current amplifier. The circuit works on two principle modules i.e. a low input impedance CDU and (n+1) OTA stages. Some of the advantages of the circuit include low input impedance, no parasitic capacitances and wide bandwidth.

A high performance CDTA with qualities such as good linearity, high accuracy, low input resistance, high output resistance, wider bandwidth etc. is suggested in [11]. The circuit also offers a high input/output gain ratio for current transfer. In this circuit, a differential current controlled current source (DCCCS) is used in the CDU which is used for obtaining the difference in current inputs and transforming the difference of currents to the Z terminal. After converting this current to voltage at the Z terminal, a Dual Output OTA (DO-OTA) is used to convert that voltage to the two currents achieved at the two output terminals of the OTA. The resistance connected at the Z terminal of the DCCCS is used to attain the gain of the circuit. The circuit offered a wide bandwidth.

A high performance CMOS implemented CDTA was introduced by Kacar *et. al* [19] with high output impedance and good input/output current tracking. The reported circuit was verified using a transadmittance mode biquad containing two CDTAs, capacitors and resistors.

Xu *et. al.* [20] presented a low voltage high linearity wideband CDTA amplifier. The main design modification presented in the circuit is the use of only n-MOSFETs. The circuit consists of two principle blocks: a CDU and the cross coupled transconductance amplifier circuit. The CDU performs the current differencing action and the OTA offers a high transconductance. The circuit has the advantages such as high linearity, wide frequency bandwidth, low power consumption, high transconductance, low input impedance, high output impedance and tuning of transconductance.

A structure termed as the multi output current controlled CDTA (MOCDTA) was presented in [12]. This structure consisted of two blocks Z copy CDTA and OTA. An extra transconductance amplifier and current mirrors are used in the conventional CDTA circuit to extend the number output ports of the circuit. It has high output impedance and low passive sensitivities even when the non idealities of the circuit were considered. The main difference between the CDTA and MOCDTA lies in the fact that the two blocks of the circuit are relatively independent of each other. The example of the suggested circuit as a current mode quadrature sinusoidal oscillator with high output impedance had

been realized but it has the disadvantage is that the condition of oscillation cannot be electronically adjusted. Another Z-copy CDTA is reported [13] which used third generation current conveyors.

Malcher [14] introduced a modified current differencing transconductance amplifier. The circuit has been modified by making changes in the conventional CDTA circuit such as the addition of an extra terminal in place of the grounded reference node of CDU and the implementation of the OTA as the differential output circuit with the possibility of duplication of the output currents. This circuit had the advantage of providing electrical tuning of input resistance, resistance at the Z terminal and the transconductance at the output stage. Some of the disadvantages of the circuit are the difference in the input impedance of the p and the n terminals of the CDTA, which could be reduced by using the MOSFETs with larger aspect ratios, the tuning range of the bias current is not large enough and the addition of all the structures increase the complexity of the circuit.

Although, a number of structures have been designed to enhance the performance parameters of CDTA circuit but there are only a few available which deal with increasing the transconductance of the OTA and thus improving the transconductance of CDTA. In all the above mentioned circuits, the transconductance was varied by changing the bias current of the circuit but it lead to higher power dissipation and a limited range of transconductance. The second method to vary the value of transconductance was by increasing the aspect ratios of the transistors used to form the differential pair but it had the limitation of low input/output swing and lower bandwidth. The main reason to increase the transconductance of the OTA resides in the fact that in all the applications of analog signal processing, transconductance is used to control different parameters of the circuits such as the center frequency of the filter and the frequency of oscillations of the oscillator circuits. Also, in logarithmic amplifiers and waveform generators a high value of transconductance is required as the output current in these circuits depends on the transconductance. Further, in order to achieve a lager bandwidth of inductance, the grounded capacitors and the floating inductor circuits require a wider range of transconductance values. So, some new techniques were suggested.

2.1 GM BOOSTING TECHNIQUES

The first technique to enhance the transconductance of the CDTA was proposed in [16]. In this technique, the value of bias current was kept constant. The number of MOSFETs in the differential pair were increased by connecting a number of perfectly matched n -MOSFETs in parallel. Thus, two networks of n-parallel MOSFETs were placed in place of the conventional differential pair n-MOSFETs to boost the transconductance of CDTA and hence named as transconductance boosted current differencing transconductance amplifier. The increased number of MOSFETs led to the increase in the current of the circuit as all the MOSFETs were connected to a same gate-to-source voltages. The transconductance of the circuit was increased as the number of MOSFETs were increased in the differential pair. Thus, the output of the TBCDTA will be the summation of currents flowing through

the networks formed in differential pair of the circuit. The circuit offered a high value of transconductance along with the wider range of the transconductance by keeping the power dissipation in the acceptable range as that of a conventional CDTA. The circuit has the disadvantage of using large area but that can be reduced by using an appropriate number of MOSFETs in the design. Another approach with similar concept of parallel n-MOSFETs in differential pair with current copying method is used in [17].

The transconductance of the circuit reported in [18] was boosted without altering bandwidth and input/output swing of the circuit by using a pair of cross-coupled p-MOSFETs across the conventional PMOS active loads. The idea behind the use of cross coupled p-MOSFETs lie in the fact that they formed the positive feedback which resulted in increased gain. The advantage of the circuit were the improved tuning range and input/output swing.

The technique reported in [21] used n-MOSFETs in parallel which were used to form the differential pair and a pair of cross coupled p-MOSFETs along with the active load p-MOSFETs. The cross coupled p-MOSFETs generate a negative resistance by feedback from the output node to enhance the DC gain. By applying the positive feedback technique, achieving a large DC gain becomes partially dependent on matching of parameters of different transistors that are involved in the positive feedback. The circuit offers the advantage of increased transconductance.

Another technique is CDTA based on this technique used a source degenerated differential pair with constant biasing current. The main advantages of the circuit was enhanced transconductance, high linearity and improved tuning range.

Apart from all these structures and available techniques to modify the conventional CDTA structures, a large number of applications based on the CDTA in the field of analog signal processing have been proposed over the years of time. The various applications developed by CDTA from its inception are monostable multivibrators [22], semi Gaussian shaper [23], Schmitt trigger [24-26], comparator [27], multipliers [28-30], power detector [31], current limiters [15], oscillators [32, 33], rectifiers [33, 34], square rooter [35], tunable phase shifter [36], filters [37, 38], logarithmic amplifier [39], modulators [40], Wein bridge oscillator [41], Wheatstone bridge [42] etc.

CHAPTER 3

PROPOSED CDTA AND ITS APPLICATIONS

In this chapter, four current differencing transconductance amplifier (CDTA) structures such as CDTACS, PCDTACS, CCDTACS and PCCDTACS are proposed. The main objective of these circuits is to show the increased transconductance along with keeping the power dissipation to the optimum levels. The KHN filters are used the applications to show the effectiveness of the proposed structures. In the section 3.1, the operation of conventional CDTA is explained. Section 3.2 describes the structure of CDTACS and the advantages of connecting a common source (CS) amplifier in the OTA of proposed CDTACS. Section 3.3 addresses PCDTACS in which the advantage of connecting a number of n-MOSFETs in the differential pair is discussed. A CCDTACS is proposed in Section 3.4, in which the OTA is modified by connecting a pair of cross coupled n-MOSFETs in the differential pair. In the last section 3.5, a proposed PCCDTACS is designed by using a CS amplifier, two networks of parallel n-MOSFETs and the cross-coupled n-MOSFETs in the OTA.

3.1. CONVENTIONAL CDTA

Figure 3.1 shows the circuit diagram of a conventional CDTA. It consists of the two units namely Current Differencing Unit (CDU) [8] and the Operational Transconductance Amplifier (OTA) [3]. The CDU acts as a differencing unit of two input currents. The difference of input currents is calculated at the output terminal of the CDU. This current is then converted to a voltage across the connected resistance. This voltage then acts as an input to the differential pair in the OTA and the output is generated in the form of two currents.

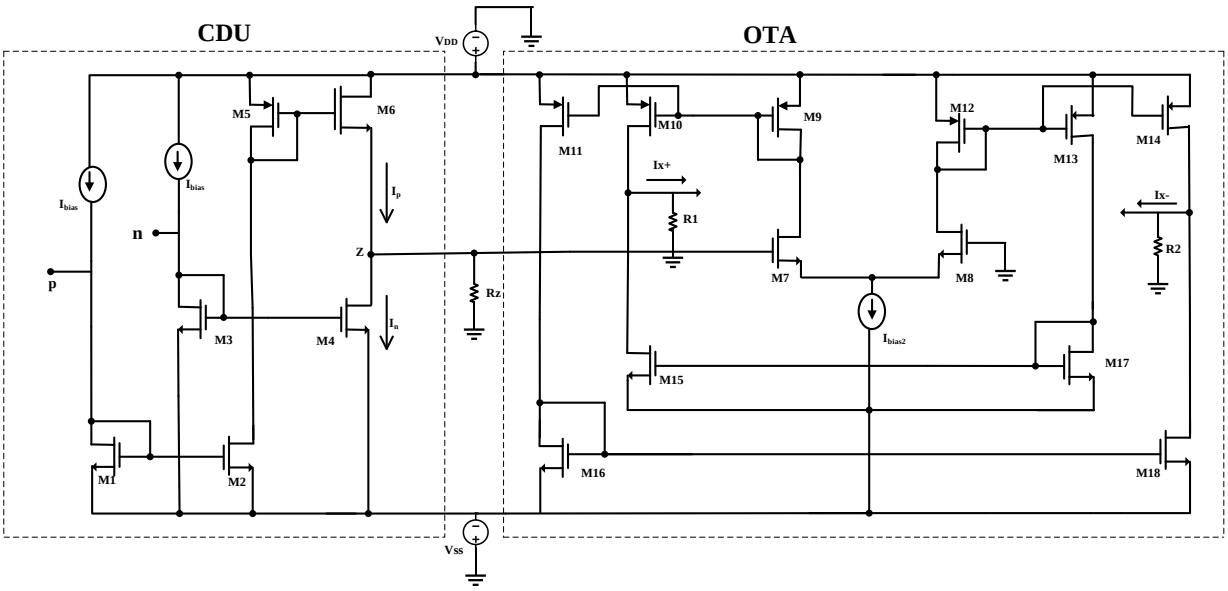


Figure 3.1 Conventional CDTA

The CDU consists of MOSFETs M1-M6 which are in the form of three current mirrors. The input currents are applied to the drain terminal of M1 & M3 and the difference of currents is generated at the Z terminal with the help of current mirrors. This current is then converted to a voltage by connecting a resistance at the Z terminal. All the MOSFETs in the circuit operate in the saturation region. The OTA is composed of the MOSFETs M7-M18. The voltage produced at Z terminal is given as the input to MOSFET M7 of the differential pair. This voltage is again converted to the current via the network of current mirrors formed by MOSFETs M9-M14. The output of CDTA is generated at the drain terminals of M18 and M15.

3.2. PROPOSED CDTA WITH COMMON SOURCE AMPLIFIER (CDTACS)

The operation of both the conventional CDTA and the proposed CDTACS is same except from the fact that the transconductance of the proposed circuit has been boosted. The proposed CDTACS has been developed from the conventional CDTA and a Common Source (CS) Amplifier. The common source amplifier has been used to boost the transconductance of the conventional CDTA as the CS amplifier produces an out-of-phase voltage at the output terminal which is given to the source of one of the MOSFETs in the differential pair thus increasing the overall gate-to-source voltage of the MOSFET.

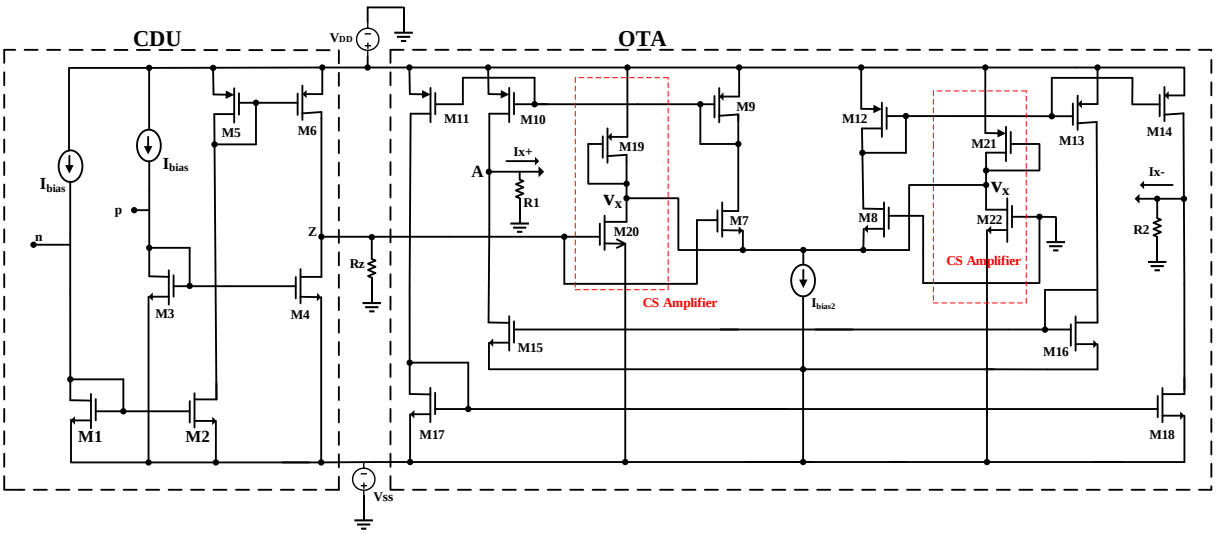


Figure 3.2 Proposed CDTA with Common Source (CDTACS)

Figure 3.2 shows the proposed CDTACS circuit. The proposed CDTACS consists of two units i.e. the CDU and the OTA with CS amplifier. The CDU consists of six MOSFETs M1-M6. These MOSFETs form three current mirror networks. The MOSFETs M1 & M2, M3 & M4 and M5 & M6 are perfectly matched. All the MOSFETs operate in the saturation region. The two currents Ip and In are given as inputs to the drain terminals of the MOSFETs M1 and M3, respectively. This current is then passed through the current mirror circuits and the difference of current is created at the Z terminal of the CDU unit. The value of the resistor connected at the Z terminal is chosen so as to provide a proper operating

range to the OTA. The OTA consists of MOSFETs M7-M22. These MOSFETs are also made to operate in saturation region. The p-MOSFET i.e. M9-M14 and n-MOSFETs M15-M17 form current mirrors. The CS amplifiers are designed by using MOSSFETs M19-M20 and M21-M22. These are connected on both the sides of OTA to make the circuit symmetrical. The CS amplifier is connected across gate and source terminals of the MOSFET M7 of the differential pair. Same input voltage is applied at the gate terminals of MOSFETs M20 and M7. The output of CS amplifier is given to the source terminals of the MOSFETs M7 and M8 of the differential pair. This in turn, increases the gate-to-source voltage of the MOSFETs of the differential pair. The output of the OTA is in the form of two currents named as Ix+ and Ix-. These two currents are taken from the drain terminals of the MOSFETs M15 and M18.

A small signal model of CDTACS as shown in Figure 3.3.

Applying KCL at the node A:

$$i_{x+} = -gm_{10}.vgs_{10} - gm_{15}.vgs_{15} \tag{3.1}$$

where, i_{x+} represents the output current, gm_{10} and gm_{15} are the transconductances of MOSFETs M10 & M15 and vgs_{10} & vgs_{15} are the gate-to-source voltages of M10 & M15.

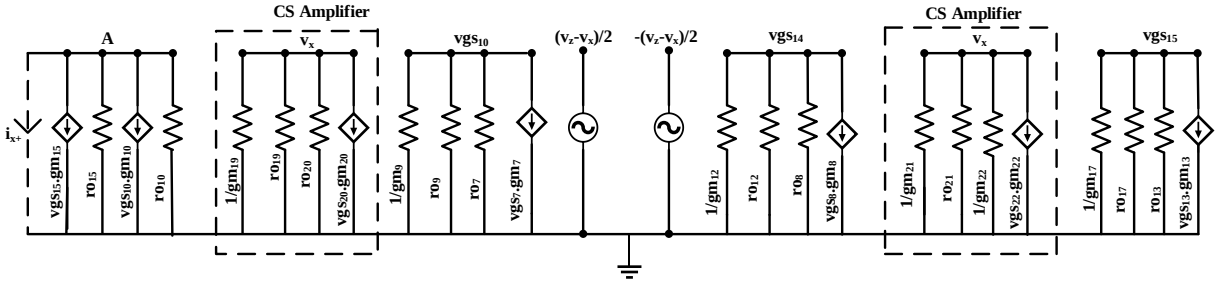


Figure 3.3 Small signal model of CDTACS

Applying KCL at the node v_x to calculate the output voltage produced by the CS Amplifier. The output voltage v_x is given as:

$$v_x = -gm_{20}.vgs_{20}\left(\frac{1}{gm_{19}} \text{ ll } ro_{19} \text{ ll } ro_{20}\right) \tag{3.2}$$

where, gm_{19} and gm_{20} represent the transconductances of MOSFETs M19 & M20, ro_{19} & ro_{20} are the output impedances of M19 & M20 and vgs_{20} is the gate-to-source voltage of M20. The value of $1/gm_{19}$ is smaller than the ro_{19} and ro_{20}. So, the parallel combination of $1/gm_{19}$, ro_{19} and ro_{20} reduces to $1/gm_{19}$. Therefore, v_x equals to:

$$v_x = -\frac{gm_{20}}{gm_{19}}.\left(\frac{v_z}{2}\right) \tag{3.3}$$

where $v_z = 2.vgs_{20}$ is because of the half symmetry of the circuit.

The gate-to-source voltage of the MOSFET M10 i.e. vgs_{10} in terms of v_z.

$$vgs_{10} = -gm_7.vgs_7.\left(\frac{1}{gm_9} \text{ ll } ro_9 \text{ ll } ro_7\right) \tag{3.4}$$

where, gm_7 and gm_9 represent the transconductances of M7 & M9, ro_7 and ro_9 are the output impedances and vgs_7 is the gate-to-source voltage. The value of $1/gm_9$ is smaller than the ro_9 and ro_7. So, the parallel combination of $1/gm_9$, ro_9 and ro_7 yeilds to $1/gm_9$. Therefore, vgs_{10} is equal to:

$$vgs_{10} = -\frac{gm_7}{gm_9}.\, vgs_7 \tag{3.5}$$

$$= -\frac{gm_7}{gm_9}.\left(\frac{v_z}{2} - \frac{v_x}{2}\right) \tag{3.6}$$

$$= -\frac{gm_7}{gm_9}.\left(\frac{v_z}{2} + \frac{gm_{20}}{gm_{19}}.\frac{v_z}{2}\right) \tag{3.7}$$

$$= -\frac{gm_7}{gm_9}.\left(1 + \frac{gm_{20}}{gm_{19}}\right).\frac{v_z}{2} \tag{3.8}$$

The gate-to-source voltage of the MOSFET M13 i.e. vgs_{13} in terms of v_z is given as:

$$vgs_{13} = -gm_8\,.vgs_8.\left(\frac{1}{gm_{12}} \text{ ll } ro_{12} \text{ ll } ro_8\right) \tag{3.9}$$

where, gm_8 and gm_{12} represent the transconductances of M8 & M12, ro_{12} and ro_8 are the output impedances and vgs_8 is the gate-to-source voltage of M8. The value of $1/gm_{12}$ is smaller than the ro_8 and ro_{12}. So, the parallel combination of $1/gm_{12}$, ro_8 and ro_{12} yeilds to $1/gm_{12}$. Therefore, vgs_{13} is equal to:

$$vgs_{13} = -\frac{gm_8}{gm_{12}}.\, vgs_8 \tag{3.10}$$

$$= -\frac{gm_8}{gm_{12}}.\left(-\frac{v_z}{2} + \frac{v_x}{2}\right) \tag{3.11}$$

$$= \frac{gm_8}{gm_{12}}.\left(\frac{v_z}{2} + \frac{gm_{20}}{gm_{19}}.\frac{v_z}{2}\right) \tag{3.12}$$

$$= \frac{gm_8}{gm_{12}}.\left(1 + \frac{gm_{20}}{gm_{19}}\right).\frac{v_z}{2} \tag{3.13}$$

The gate-to-source voltage of the MOSFET M15 vgs_{15} in terms of vgs_{13} is given as:

$$vgs_{15} = -gm_{13}\,.vgs_{13}.\left(\frac{1}{gm_{17}} \text{ ll } ro_{17} \text{ ll } ro_{13}\right) \tag{3.14}$$

where, gm_{13} and gm_{17} represent the transconductances of M13 & M17, ro_{17} and ro_{13} are the output impedances of M13 & M17 and vgs_{13} is the gate-to-source voltage of M13. The value of $1/gm_{17}$ is smaller than the ro_{17} and ro_{13}. So, the parallel combination of $1/gm_{17}$, ro_{17} and ro_{13} yeilds to $1/gm_{17}$. Therefore, vgs_{15} equals to:

$$vgs_{15} = -\frac{gm_{13}}{gm_{17}}.\, vgs_{13} \tag{3.15}$$

Substituting the value of vgs_{13} in Equation (3.15).

$$vgs_{15} = \frac{gm_{13}}{gm_{17}}.\frac{gm_8}{gm_{12}}.\left(1 + \frac{gm_{20}}{gm_{19}}\right).\frac{v_z}{2} \tag{3.16}$$

The MOSFETs M13 and M12 are perfectly matched. Thus, $gm_{13} = gm_{12}$.
Therefore,

$$vgs_{15} = \frac{gm_8}{gm_{17}}.\left(1 + \frac{gm_{20}}{gm_{19}}\right).\frac{v_z}{2} \tag{3.17}$$

Substituting Equation (3.8) and (3.17) in Equation (3.1).
Therefore,

$$i_{x+} = gm_{10}\frac{gm_7}{gm_9}.\left(1 + \frac{gm_{20}}{gm_{19}}\right).\frac{v_z}{2} + gm_{15}\frac{gm_8}{gm_{17}}.\left(1 + \frac{gm_{20}}{gm_{19}}\right).\frac{v_z}{2} \tag{3.18}$$

The MOSFETs M7 & M8, M9 and M10, M15 and M17 are perfectly matched. Thus, their respective transconductance are also equal i.e. $gm_7 = gm_8 = gm$, $gm_9 = gm_{10}$ and $gm_{15} = gm_{17}$. Therefore, the current i_{x+} can be represented as shown in equation 3.12.

$$i_{x+} = gm_7.\left(1 + \frac{gm_{20}}{gm_{19}}\right).\frac{v_z}{2} + gm_8.\left(1 + \frac{gm_{20}}{gm_{19}}\right).\frac{v_z}{2} \tag{3.19}$$

$$i_{x+} = gm.\left(1 + \frac{gm_{20}}{gm_{19}}\right).v_z \tag{3.20}$$

The value can be $\left(\frac{gm_{20}}{gm_{19}}\right)$ can be denoted by a constant A. Thus,

$$i_{x+} = gm.(1 + A).v_z = gm_{CDTACS}.v_z \tag{3.21}$$

Similarly, the i_{x-} can be shown as:

$$i_{x-} = -gm.(1 + A).v_z = -gm_{CDTACS}.v_z \tag{3.22}$$

The gm_{CDTACS} represents the new transconductance of the proposed CDTACS in which the transconductance of the conventional CDTA is boosted by a factor of (1+ A).

3.2.1 KHN Filter based on proposed CDTACS

A Kerwin-Huelsman-Newcomb (KHN) filter designed using the proposed CDTACS is shown in Figure 3.4. The KHN filter is constructed by cascading of two proposed CDTACS circuits with passive elements to obtain the frequency response of High Pass (HP), Low Pass (LP) and Band Pass (BP) filters. The center frequency of the KHN filter (fo) is given as:

$$fo = \frac{1}{2\pi}.\sqrt{\frac{gm_{CDTACS1}.gm_{CDTACS2}}{C_1 . C_2}} \tag{3.23}$$

where, $gm_{CDTACS1} = gm_{CDTACS2} = gm_{CDTACS}$ are the transconductances of the proposed CDTACS, C_1 and C_2 are the two equal value grounded capacitances connected across the terminals of the KHN filter.

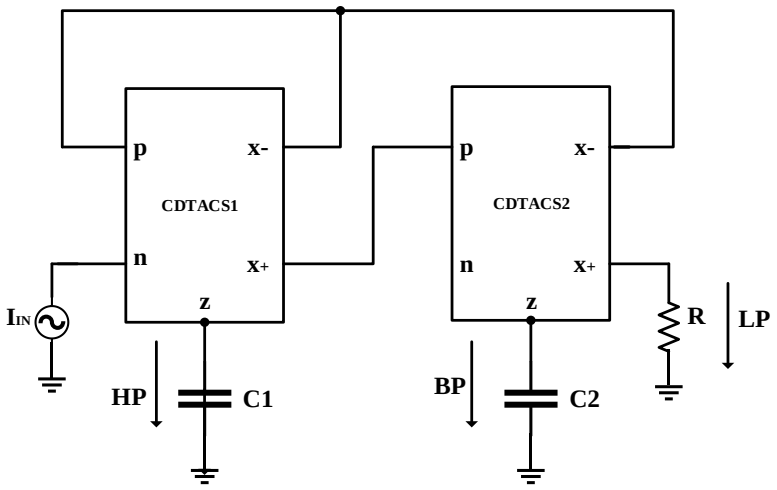


Figure 3.4 KHN Filter using proposed CDTACS

3.3. PROPOSED CDTA WITH CS AMPLIFIER AND PARALLEL N- MOSFETS (PCDTACS)

The proposed PCDTACS is a modification of the proposed CDTACS circuit. In this circuit, the basic structure of the CDTA remains the same except that in place of a single n-MOSFET in differential pair, a number of n-MOSFETs are connected in parallel to enhance the transconductance of the CDTA. In the proposed PCDTACS, five n-MOSFETs are connected in parallel to form two symmetrical networks i.e. N1 and N2 on each sides of the OTA. These networks N1 and N2 of MOSFETs increases the total current in OTA as the total drawn by the current will be the summation of all the individual currents drawn by the MOSFETs and thus increasing the transconductance of circuit.

The PCDTACS is shown in the Figure 3.5. The proposed PDTACS consists of two units i.e. the CDU and the OTA with CS amplifier. The CDU consists of six MOSFETs M1-M6. These MOSFETs form three current mirror networks. The MOSFETs M1 & M2, M3 & M4 and M5 & M6 are perfectly matched. All the MOSFETs operate in the saturation region. The two currents Ip and In are given as inputs to the drain terminals of the MOSFETs M1 and M3, respectively. This current is then passed through the current mirror circuits and the difference of current is created at the Z terminal of the CDU. The value of the resistor connected at the Z terminal is chosen so as to provide a proper operating range to the OTA. The OTA consists of MOSFETs $M7_N$-M22. These MOSFETs are also made to operate in saturation region. The p-MOSFET i.e. M9-M14 and n-MOSFETs M15-M17 form current mirrors. The CS amplifiers are designed by using MOSSFETs M19-M20 and M21-M22. The CS amplifier is connected across gate and source terminal of the MOSFET M7 of the differential pair. The network of parallel n-MOSFETS N_1 and N_2 is used to improve the transconductance of the PCDTACS. These are connected on both the sides of OTA to make the circuit symmetrical. Same input gate voltage is applied to the MOSFETs M20 and $M7_N$. The output of CS amplifier is given to the source terminals of the MOSFETs $M7_N$ and $M8_N$ of the differential pair.

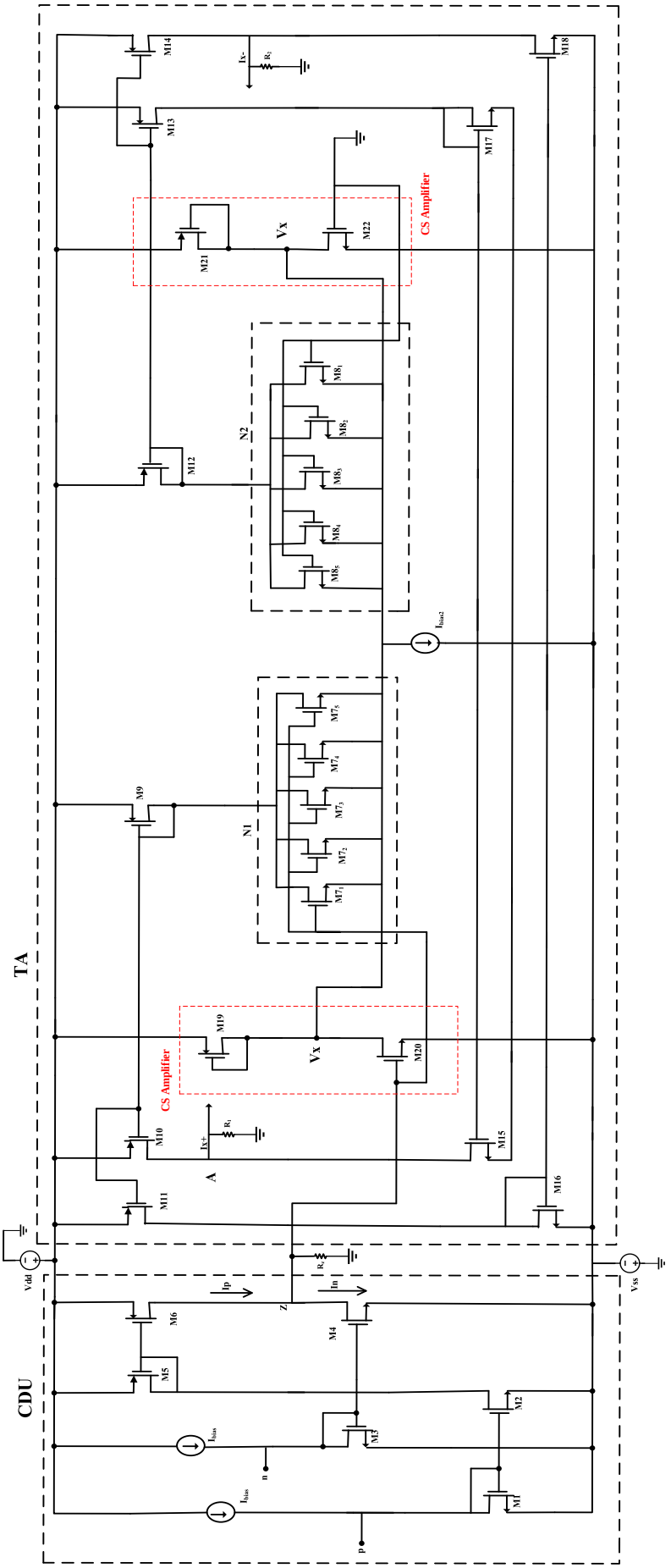


Figure 3.5 Proposed PCDTACS

This in turn, increases the gate-to-source voltage of the MOSFETs of the differential pair. The output of the OTA is in the form of two. These two currents are taken from the drain terminals of the MOSFETs M15 and M18.

A small signal model of PCDTACS as shown in Figure 3.6.

The gain of the CDTACS can be calculated by applying the KCL on the different nodes.

Applying KCL at the node A:

$$i_{x+} = -gm_{10}.vgs_{10} - gm_{15}.vgs_{15} \tag{3.24}$$

where, i_{x+} represents the output current, gm_{10} and gm_{15} are the transconductances of MOSFETs M10 & M15 and vgs_{10} & vgs_{15} are the gate-to-source voltages of M10 & M15.

Applying KCL at the node v_x to calculate the output voltage produced by the CS Amplifier. The output voltage v_x is given as:

$$v_x = -gm_{20}.vgs_{20}\left(\frac{1}{gm_{19}} \text{ ll } ro_{19} \text{ ll } ro_{20}\right) \tag{3.25}$$

where, gm_{19} and gm_{20} represent the transconductances of MOSFETs M19 & M20, ro_{19} & ro_{20} are the output impedances of M19 & M20 and vgs_{20} is the gate-to-source voltage of M20. The value of $1/gm_{19}$ is smaller than the ro_{19} and ro_{20}. So, the parallel combination of $1/gm_{19}$, ro_{19} and ro_{20} reduces to $1/gm_{19}$. Therefore, v_x equals to:

$$v_x = -\frac{gm_{20}}{gm_{19}}.\left(\frac{v_z}{2}\right) \tag{3.26}$$

where, $v_z = 2.vgs_{20}$ is because of the half symmetry of the circuit.

The gate-to-source voltage of the MOSFET M10 i.e. vgs_{10} in terms of v_z.

$$vgs_{10} = -gm_{7N}.vgs_{7N}.\left(\frac{1}{gm_9} \text{ ll } ro_9 \text{ ll } ro_{7N}\right) \tag{3.27}$$

where, gm_{7N} is summation of transconductances of network N_1 i.e. $gm_{7N} = gm_{7,1} + gm_{7,2} + gm_{7,3} + gm_{7,4} + gm_{7,5}$, gm_9 represent the transconductances of M9, ro_{7N} is the parallel combination of output impedances of MOSFETs $M7_{1\text{-}5}$, ro_9 are the output impedances of M9 and vgs_{7N} is the gate-to-source voltage applied to the gate terminals of the MOSFETs $M7_{1\text{-}5}$. The value of $1/gm_9$ is smaller than the ro_9 and ro_{7N}. So, the parallel combination of $1/gm_9$, ro_9 and ro_{7N} yeilds to $1/gm_9$. Therefore, vgs_{10} equals:

$$vgs_{10} = -\frac{gm_{7N}}{gm_9}.vgs_{7N} \tag{3.28}$$

$$= -\frac{gm_{7N}}{gm_9}.\left(\frac{v_z}{2} - \frac{v_x}{2}\right) \tag{3.29}$$

$$= -\frac{gm_{7N}}{gm_9}.\left(\frac{v_z}{2} + \frac{gm_{20}}{gm_{19}}.\frac{v_z}{2}\right) \tag{3.30}$$

$$= -\frac{gm_{7N}}{gm_9}.\left(1 + \frac{gm_{20}}{gm_{19}}\right).\frac{v_z}{2} \tag{3.31}$$

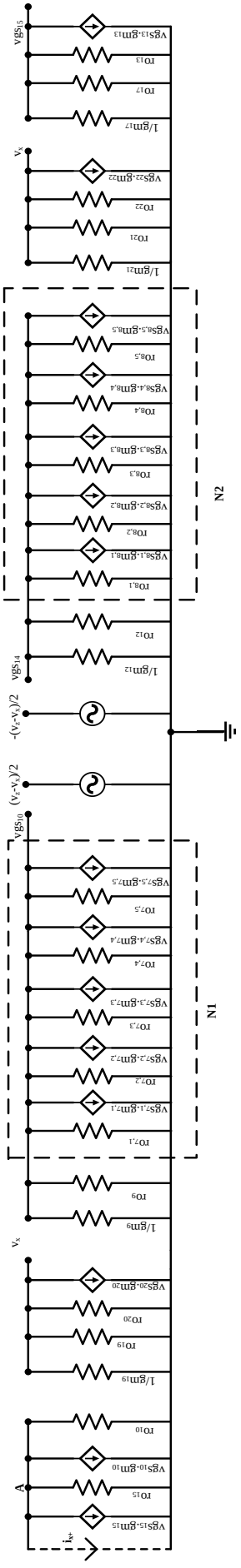


Figure 3.6 Small signal model of PCDTACS

The gate-to-source voltage of the MOSFET M13 i.e. vgs_{13} in terms of v_z is given as:

$$vgs_{13} = -gm_{8N} \cdot vgs_{8N} \cdot \left(\frac{1}{gm_{12}} \text{ ll } ro_{12} \text{ ll } ro_{8N}\right) \tag{3.32}$$

where, gm_{8N} is summation of transconductances of network N_2 i.e. $gm_{8N} = gm_{8,1} + gm_{8,2} + gm_{8,3} + gm_{8,4} + gm_{8,5}$, gm_{12} represent the transconductances of M12, ro_{8N} is the parallel combination of output impedances of MOSFETs $M8_{1\text{-}5}$, ro_{12} are the output impedances of M12 and vgs_{8N} is the gate-to-source voltage applied to the gate terminals of the MOSFETs $M8_{1\text{-}5}$ The value of $1/gm_{12}$ is smaller than the ro_8 and ro_{12}. So, the parallel combination of $1/gm_{12}$, ro_{8N} and ro_{12} yeilds to $1/gm_{12}$. Therefore, vgs_{13} is equal to:

$$vgs_{13} = -\frac{gm_{8N}}{gm_{12}} \cdot vgs_{8N} \tag{3.33}$$

$$= -\frac{gm_{8N}}{gm_{12}} \cdot \left(-\frac{v_z}{2} + \frac{v_x}{2}\right) \tag{3.34}$$

$$= \frac{gm_{8N}}{gm_{12}} \cdot \left(\frac{v_z}{2} + \frac{gm_{20}}{gm_{19}} \cdot \frac{v_z}{2}\right) \tag{3.35}$$

$$= \frac{gm_{8N}}{gm_{12}} \cdot \left(1 + \frac{gm_{20}}{gm_{19}}\right) \cdot \frac{v_z}{2} \tag{3.36}$$

The gate-to-source voltage of the MOSFET M15 vgs_{15} in terms of vgs_{13} is given as:

$$vgs_{15} = -gm_{13} \cdot vgs_{13} \cdot \left(\frac{1}{gm_{17}} \text{ ll } ro_{17} \text{ ll } ro_{13}\right) \tag{3.37}$$

where, gm_{13} and gm_{17} represent the transconductances of M13 & M17, ro_{17} and ro_{13} are the output impedances of M13 & M17 and vgs_{13} is the gate-to-source voltage of M13. The value of $1/gm_{17}$ is smaller than the ro_{17} and ro_{13}. So, the parallel combination of $1/gm_{17}$, ro_{17} and ro_{13} yeilds to $1/gm_{17}$. Therefore, vgs_{15} equals to:

$$vgs_{15} = -\frac{gm_{13}}{gm_{17}} \cdot vgs_{13} \tag{3.38}$$

Substituting the value of vgs_{13} in Equation (3.38).

$$vgs_{15} = \frac{gm_{13}}{gm_{17}} \cdot \frac{gm_{8N}}{gm_{12}} \cdot \left(1 + \frac{gm_{20}}{gm_{19}}\right) \cdot \frac{v_z}{2} \tag{3.39}$$

The MOSFETs M13 and M12 are perfectly matched. Thus, $gm_{13} = gm_{12}$.

Therefore,

$$vgs_{15} = \frac{gm_{8N}}{gm_{17}} \cdot \left(1 + \frac{gm_{20}}{gm_{19}}\right) \cdot \frac{v_z}{2} \tag{3.40}$$

Substituting Equation (3.31) and (3.40) in Equation (3.24).

Therefore,

$$i_{x+} = gm_{10} \frac{gm_{7N}}{gm_9} \cdot \left(1 + \frac{gm_{20}}{gm_{19}}\right) \cdot \frac{v_z}{2} + gm_{15} \frac{gm_{8N}}{gm_{17}} \cdot \left(1 + \frac{gm_{20}}{gm_{19}}\right) \cdot \frac{v_z}{2} \tag{3.41}$$

The MOSFETs $M7_N$ & $M8_N$, M9 and M10, M15 and M17 are perfectly matched. Thus, their respective transconductance are also equal i.e. $gm_{7N} = gm_{8N} = gm_N$, $gm_9 = gm_{10}$ and $gm_{15} = gm_{17}$. Therefore, the current i_{x+} as:

$$i_{x+} = gm_{7N}.\left(1 + \frac{gm_{20}}{gm_{19}}\right).\frac{v_z}{2} + gm_{8N}.\left(1 + \frac{gm_{20}}{gm_{19}}\right).\frac{v_z}{2} \quad (3.42)$$

$$i_{x+} = gm_N.\left(1 + \frac{gm_{20}}{gm_{19}}\right).v_z \quad (3.43)$$

The value can be $\left(\frac{gm_{20}}{gm_{19}}\right)$ can be denoted by a constant A. Thus,

$$i_{x+} = gm_N.(1 + A).v_z = gm_{PCDTACS}.v_z \quad (3.44)$$

Similarly, the i_{x-} can be shown as:

$$i_{x-} = -gm_N.(1 + A).v_z = -gm_{PCDTACS}.v_z \quad (3.45)$$

where, the $gm_{PCDTACS}$ represents the transconductance of the proposed PCDTACS in which the transconductance of the CDTACS is boosted by a factor of gm_N.

3.3.1 KHN Filter based on proposed PCDTACS

A Kerwin-Huelsman-Newcomb (KHN) filter designed using the proposed PCDTACS is shown in Figure 3.7. The KHN filter is constructed by cascading of two proposed PCDTACS circuits with passive elements to obtain the frequency response of High Pass (HP), Low Pass (LP) and Band Pass (BP) filters.

The center frequency of the KHN filter (fo) is given as:

$$fo = \frac{1}{2\pi}.\sqrt{\frac{gm_{PCDTACS1}.gm_{PCDTACS2}}{C_1 . C_2}} \quad (3.46)$$

where, $gm_{PCDTACS1} = gm_{PCDTACS2} = gm_{PCDTACS}$ are the transconductances of the proposed PCDTACS, C_1 and C_2 are the two equal value grounded capacitances connected across the terminals of the KHN filter.

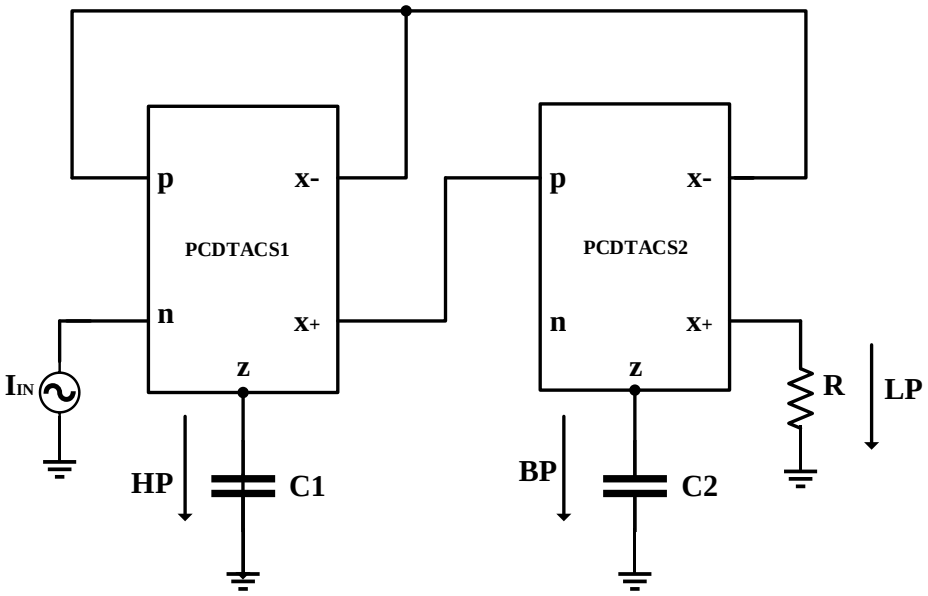


Figure 3.7 KHN Filter using proposed PCDTACS

3.4. PROPOSED CDTA WITH CS AMPLIFIER AND CROSS COUPLED N-MOSFETS (CCDTACS)

The proposed CCDTACS is a modification of the proposed CDTACS circuit. In this circuit, the basic structure of the CDTA remains the same except from the fact that in CCDTACS, a pair of n-MOSFETs is connected in cross coupled configuration across the differential pair of OTA. These cross coupled MOSFETs form a positive feedback in the circuit which leads to the improved transconductance of the circuit. Thus, the overall transconductance of the OTA becomes dependent on the cross-coupled MOSFETs and by selecting their suitable ratios, a high gain can be achieved.

The CCDTACS is shown in the Figure 3.8. The proposed CCDTACS consists of two units i.e. the CDU and OTA with CS amplifier and cross-coupled MOSFETs M9 and M10. The CDU consists of six MOSFETs M1-M6. These MOSFETs form three current mirror networks. The MOSFETs M1and M2, M3 and M4, M5 and M6 are perfectly matched. All the MOSFETs operate in the saturation region. The two currents Ip and In are given as inputs to the drain terminals of the MOSFET M1 and M3, respectively. This current is then passed through the current mirror circuits and the difference of current is created at the Z terminal of the CDU. The value of resistor connected at the Z terminal is chosen so as to provide a proper operating rate to the OTA.

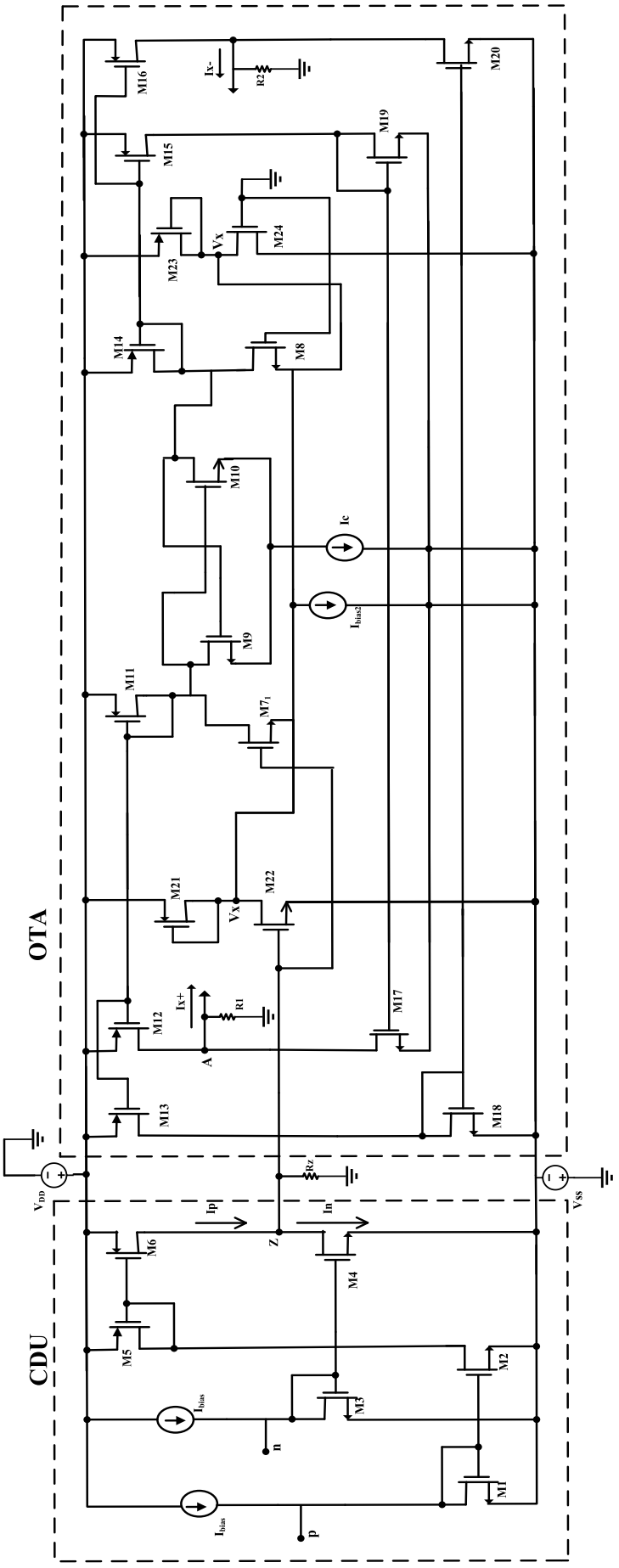


Figure 3.8 Circuit diagram of proposed CCDTACS

The OTA consists of MOSFETs M7-M24. These MOSFETs are also made to operate in saturation region. The p-MOSFETs M11-M16 and n-MOSFETs M17-M20 form current mirrors. The CS amplifiers are designed by using MOSSFETs M21-M22 and M23-M24. The CS amplifiers are connected on both sides of the OTA to make the circuit symmetrical. The CS amplifier is connected across gate and source terminal of the MOSFET M7 and the drain terminal of M7 is connected to the drain of MOSFET M9 to form a cross-coupled pair on one side of OTA. Similarly, on the order side drain of MOSFETs M8 and M10 are connected together. Same input gate voltage is applied to both the MOSFETs, M22 and M7. The output of CS amplifier is given as to the source terminals of the MOSFETs M7 and M8 of the differential pair. This in turn, increases the gate-to-source voltage of the MOSFETs of the differential pair. The cross coupled MOSFETs M9 and M10 are connected to a third current source. These MOSFETs also operate in saturation region. The output of the OTA is in the form two currents and is taken from the drain terminals of the MOSFETs M17 and M20.

The small signal model of the proposed CCDTACS is shown in Figure 3.9.

Applying KCL at the node A:

$$i_{x+} = -\mathrm{gm}_{12}.\mathrm{vgs}_{12} - \mathrm{gm}_{17}.\mathrm{vgs}_{17} \tag{3.47}$$

where, i_{x+} is the output current of the CCDTACS, gm_{12} and gm_{17} are the transconductances of MOSFETs M12 and M17 and vgs_{12} and vgs_{17} are their respective gate-to-source voltages.

Applying KCL at the node v_x to calculate the output voltage of CS Amplifier. The output voltage $v_x$is equal to:

$$v_x = -\mathrm{gm}_{22}.\mathrm{vgs}_{22}\left(\frac{1}{\mathrm{gm}_{21}} \text{ ll } \mathrm{ro}_{21} \text{ ll } \mathrm{ro}_{22}\right) \tag{3.48}$$

where, v_{x+} is the output voltage of the CS amplifier, gm_{21} and gm_{22} are the transconductances of MOSFETs M21 and M22, vgs_{22} is the gate-to-source voltage of MOSFET M22 and $\mathrm{ro}_{21}$and ro_{22} are the output impedances of MOSFETs M21 and M22. The value of $1/\mathrm{gm}_{22}$ is smaller than the ro_{21} and ro_{22}. So, the parallel combination of $1/\mathrm{gm}_{21}$, ro_{22} and ro_{21} yeilds to $1/\mathrm{gm}_{22}$.

Therefore, v_x reduces to:

$$v_x = -\frac{\mathrm{gm}_{22}}{\mathrm{gm}_{21}}.\left(\frac{v_z}{2}\right) \tag{3.49}$$

where, $v_z = 2.\mathrm{vgs}_{22}$ is because of the half symmetry of the circuit. The v_z is the gate voltage of the MOSFETs M7 and M22.

The gate-to-source voltage of the MOSFET M12 i.e. vgs_{12} in terms of v_z.

$$\mathrm{vgs}_{12} = -\mathrm{gm}_7.\mathrm{vgs}_7.\left(\frac{1}{\mathrm{gm}_{11}} \text{ ll } \mathrm{ro}_{11} \text{ ll } \mathrm{ro}_7 \; ll \; \left(-\frac{1}{gm_9}\right)\right) \tag{3.50}$$

where, v_{gs12} is the gate-to-source voltage of M12, gm_{11} and gm_9 are the transconductances of MOSFETs M11 and M9, vgs_7 is the gate-to-source voltage of MOSFET M7 and $\mathrm{ro}_{11}$and ro_7 are the output impedances of MOSFETs M11 and M7 respectively. The value of $\left(\frac{1}{gm_{11}}\right) and \left(-\frac{1}{gm_9}\right)$ is

smaller than the ro_{11} and ro_7. So, the parallel combination of $\left(\frac{1}{gm_{11}}\right), \left(-\frac{1}{gm_9}\right)$, ro_{11} and ro_7 yeilds to $\left(\frac{1}{gm_{11}-gm_9}\right)$.

Therefore, vgs_{12} equals to:

$$vgs_{12} = -\frac{gm_7}{gm_{11}-gm_9}.\ vgs_7 \tag{3.51}$$

$$= -\frac{gm_7}{gm_{11}-gm_9}.\left(\frac{v_z}{2}-\frac{v_x}{2}\right) \tag{3.52}$$

$$= -\frac{gm_7}{gm_{11}-gm_9}.\left(\frac{v_z}{2}+\frac{gm_{22}}{gm_{21}}.\frac{v_z}{2}\right) \tag{3.53}$$

$$= -\frac{gm_7}{gm_{11}-gm_9}.\left(1+\frac{gm_{22}}{gm_{21}}\right).\frac{v_z}{2} \tag{3.54}$$

The gate-to-source voltage of the MOSFET M15 i.e. vgs_{15} in terms of v_z.

$$vgs_{15} = -gm_8.vgs_8.\left(\frac{1}{gm_{14}}\ ll\ ro_{14}\ ll\ ro_8\ ll\ (-\frac{1}{gm_{10}})\right) \tag{3.55}$$

where, v_{gs15} is the gate-to-source voltage of M15, gm_8 and gm_{14} are the transconductances of MOSFETs M8 and M14, vgs_8 is the gate-to-source voltage of MOSFET M8 and ro_8 and ro_{14} are the output impedances of MOSFETs M8 and M14 respectively. The value of $\left(\frac{1}{gm_{14}}\right) and\ (-\frac{1}{gm_{10}})$ is smaller than the ro_8 and ro_{14}. So, the parallel combination of $\left(\frac{1}{gm_{14}}\right), (-\frac{1}{gm_{10}})$, ro_8 and ro_{12} yeilds to $(\frac{1}{gm_{14}-gm_{10}})$. Therefore, vgs_{15} reduces to:

$$vgs_{15} = -\frac{gm_8}{gm_{14}-gm_{10}}.\ vgs_{8N} \tag{3.56}$$

$$= -\frac{gm_8}{gm_8-gm_{10}}.\left(-\frac{v_z}{2}+\frac{v_x}{2}\right) \tag{3.57}$$

$$= \frac{gm_8}{gm_{14}-gm_{10}}.\left(\frac{v_z}{2}+\frac{gm_{22}}{gm_{21}}.\frac{v_z}{2}\right) \tag{3.58}$$

$$= \frac{gm_8}{gm_{14}-gm_{10}}.\left(1+\frac{gm_{22}}{gm_{21}}\right).\frac{v_z}{2} \tag{3.59}$$

The gate-to-source voltage of the MOSFET M17 i.e. vgs_{17} in terms of vgs_{15}.

$$vgs_{17} = -gm_{15}.Vgs_{15}.\left(\frac{1}{gm_{19}}\ ll\ ro_{19}\ ll\ ro_{15}\right) \tag{3.60}$$

where, v_{gs15} is the gate-to-source voltage of M15, gm_{15} and gm_{19} are the transconductances of MOSFETs M15 and M19 M7 and ro_{15} and ro_{19} are the output impedances of MOSFETs M15 and M19 respectively. The value of $1/gm_{19}$ is smaller than the ro_{19} and ro_{15}. So, the parallel combination of $1/gm_{19}$, ro_{19} and ro_{15} yeilds to $1/gm_{19}$. Therefore, vgs_{17} is:

$$vgs_{17} = -\frac{gm_{15}}{gm_{19}}.\ vgs_{15} \tag{3.61}$$

Substituting the value of vgs_{15} in Equation (3.61).

$$vgs_{17} = -\frac{gm_{15}}{gm_{19}}.\frac{gm_8}{gm_{14} - gm_{10}}.\left(1 + \frac{gm_{22}}{gm_{21}}\right).\frac{v_z}{2} \tag{3.62}$$

Substituting Equation (3.54) and (3.62) in Equation (3.47).

Therefore,

$$i_{x+} = gm_{12}.\frac{gm_7}{gm_{11} - gm_9}.\left(1 + \frac{gm_{22}}{gm_{21}}\right).\frac{v_z}{2} + gm_{17}.\frac{gm_{15}}{gm_{19}}.\frac{gm_8}{gm_{14} - gm_{10}}.\left(1 + \frac{gm_{22}}{gm_{21}}\right).\frac{v_z}{2} \tag{3.63}$$

The MOSFETs M17 and M19 are symmetrical. Thus, their respective transconductance are also equal i.e. $gm_{17} = gm_{19}$ and they will be cancelled. Hence, the current i_{x+}can be represented:

$$i_{x+} = gm_{12}.\frac{gm_7}{gm_{11} - gm_9}.\left(1 + \frac{gm_{22}}{gm_{21}}\right).\frac{v_z}{2} + gm_{15}.\frac{gm_8}{gm_{14} - gm_{10}}.\left(1 + \frac{gm_{22}}{gm_{21}}\right).\frac{v_z}{2} \tag{3.64}$$

$$= \left(\frac{gm_{12}.gm_7}{gm_{11} - gm_9} + \frac{gm_{15}.gm_8}{gm_{14} - gm_{10}}\right).\left(1 + \frac{gm_{22}}{gm_{21}}\right).\frac{v_z}{2} \tag{3.65}$$

The terms $\frac{gm_{12}.gm_7}{gm_{11} - gm_9}$ and $\frac{gm_{15}.gm_8}{gm_{14} - gm_{10}}$ are equal as the OTA is symmetrical. So, we can write:

$$\frac{gm_{12}.gm_7}{gm_{11} - gm_9} = \frac{gm_{15}.gm_8}{gm_{14} - gm_{10}} = gm_{CCDTACS} \tag{3.66}$$

Simplifying further,

$$gm_{CCDTACS} = \frac{gm_{12}.gm_7}{gm_{11} - gm_9} \tag{3.67}$$

The MOSFETs M11 and M12 are symmetrical, thus $gm_{12} = gm_{11}$

Therefore,

$$gm_{CCDTACS} = \frac{gm_7}{1 - \frac{gm_9}{gm_{11}}} = \frac{gm_8}{1 - \frac{gm_{10}}{gm_{14}}} \tag{3.68}$$

The factor $\frac{gm_9}{gm_{11}}$ is due to the cross coupled n-MOSFETs. As the positive feedback makes the circuit unstable but by choosing the appropriate values of MOSFETs M9 and M14, the overall transconductance of the CCDTACS can be improved without effecting the stability of the circuit. Also, the value $\left(\frac{gm_{22}}{gm_{21}}\right)$ can be denoted by a constant A. Thus,

$$i_{x+} = gm_{CCDTACS}.(1 + A).v_z \tag{3.69}$$

Similarly, i_{x-} can be represented as shown:

$$i_{x-} = -gm_{CCDTACS}.(1 + A).v_z \tag{3.70}$$

The $gm_{CCDTACS}$ represents the new transconductance of the proposed CCDTACS in which the transconductance of the proposed PCDTACS is boosted by the ratio $\frac{gm_9}{gm_{11}}$ or $\frac{gm_{10}}{gm_{14}}$.

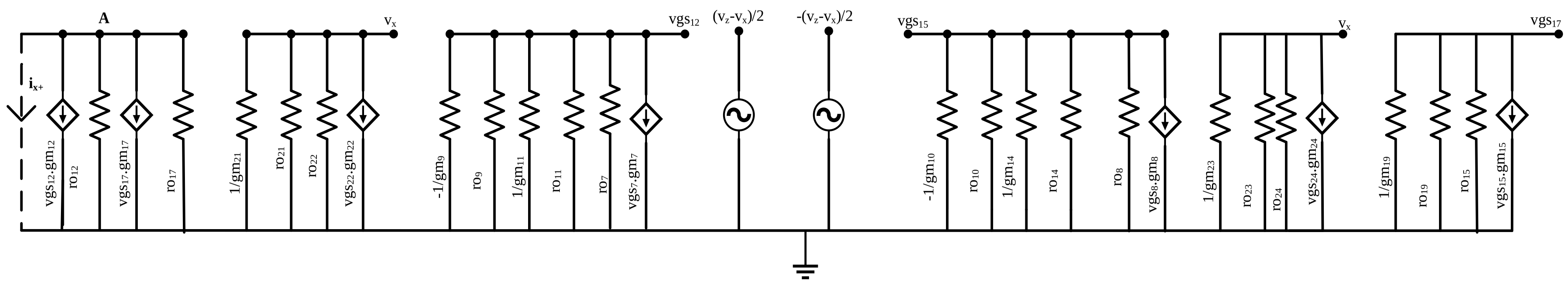


Figure 3.9 Small signal model of CCDTACS

3.4.1 KHN Filter based on proposed CCDTACS

A Kerwin-Huelsman-Newcomb (KHN) filter designed using the proposed CCDTACS is shown in Figure 3.10. The KHN filter is constructed by cascading of two proposed CCDTACS circuits with passive elements to obtain the frequency response of High Pass (HP), Low Pass (LP) and Band Pass (BP) filters. The center frequency of the KHN filter (fo) is given as: The center frequency of the KHN filter (fo) is given by:

$$fo = \frac{1}{2\pi} \cdot \sqrt{\frac{gm_{CCDTACS1} \cdot gm_{CCDTACS2}}{C_1 \cdot C_2}} \tag{3.71}$$

where, $gm_{CCDTACS1} = gm_{CCDTACS2} = gm_{CCDTACS}$ are the transconductances of the proposed CCDTACS, C_1 and C_2 are the two equal value grounded capacitances connected across the terminals of the KHN filter.

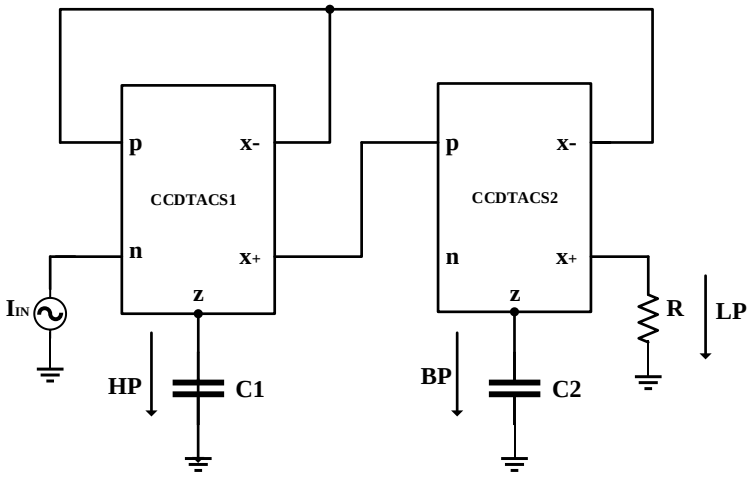


Figure 3.10 KHN Filter using proposed CCDTACS

3.5. PROPOSED CDTA WITH CS AMPLIFIER, CROSS COUPLED N-MOSFET AND PARALLEL N-MOSFETS (PCCDTACS)

The proposed PCCDTACS circuit is a combination of all above three proposed CDTA circuits i.e. OTA of this proposed circuit consists of a CS amplifier, a pair of cross-coupled n-MOSFETs and two networks N1 and N2 consisting of five parallel equal sized n-MOSFETs. The constructional difference between CCDTACS and PCCDTACS is that in place of a single differential pair, a network of MOSFETs is connected on both sides of OTA. This enhances the overall current in the circuit. The cross coupled MOSFETs generates a positive feedback which further leads to the improved transconductance of the circuit because the overall transconductance of the OTA becomes dependent on the cross coupled MOSFETs and the summation of transconductances of the parallel MOSFETs.

The Figure 3.11 shows the circuit diagram of PCCDTACS.

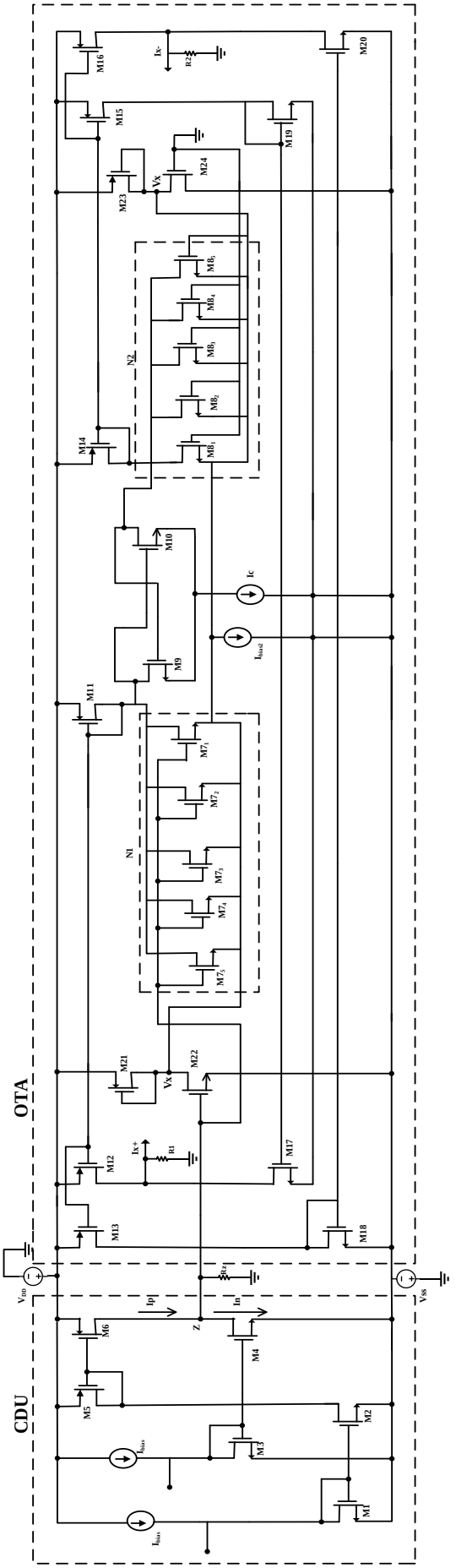


Figure 3.11 Proposed circuit diagram of PCCDTACS

The proposed PCCDTACS consists of two units, the CDU and OTA with CS amplifier and cross coupled MOSFETs M9 and M10. The CDU consists of six MOSFETs M1-M6. These MOSFETs form three current mirror networks. The MOSFETs M1 & M2, M3 & M4 and M5 & M6 are perfectly matched. All the MOSFETs operate in the saturation region. The two currents Ip and In are given as inputs to the drain terminals of the MOSFETs M1 and M3, respectively. This current is then passed through the current mirror and the difference of current is created at the Z terminal of the CDU. The value of resistor connected at the Z terminal is chosen so as to provide a proper operating range to the OTA. The OTA consists of MOSFETs M7-M24. These MOSFETs also operate in saturation region. The p-MOSFETs M11-M16 and n-MOSFETs M17-M20 form current mirror networks. The CS amplifiers are designed by using two MOSSFETs M21-M22 and M23-M24. The CS amplifiers are connected on both sides of OTA to make the circuit symmetrical. Also, drain terminal of these MOSFETs is connected to the drain of MOSFET M9 and MOSFET M10 to form two cross-coupled pairs. The $M7_N$ and $M8_N$ represent the number of MOSFETs connected in the differential pair of OTA to further boost the transconductance of the circuit. Same gate voltage is applied to both the MOSFETs M22 and $M7_N$. The output of CS amplifiers is connected to the source terminal of the MOSFETs present in network N1 and N2. This in turn, increases the gate-to-source voltage of the MOSFETs in the differential pair. The cross coupled MOSFETs M9 and M10 are connected to a third current source, Ic. These MOSFETs operate in saturation region. The output of the OTA is in the form of two currents. These two currents are taken from the drain terminals of the MOSFETs M17 and M20.

The small signal model of PCCDTACS is shown in Figure 3.12.

Applying KCL at the node A:

$$i_{x+} = -\mathrm{gm}_{12}.\mathrm{vgs}_{12} - \mathrm{gm}_{17}.\mathrm{vgs}_{17} \tag{3.71}$$

where, i_{x+} is the output current of the CCDTACS, gm_{12} and gm_{17} are the transconductances of MOSFETs M12 and M17 and vgs_{12} and vgs_{17} are their respective gate-to-source voltages.

Applying KCL at the node v_x to calculate the output voltage of CS Amplifier. The output voltage $v_x$is equal to:

$$v_x = -\mathrm{gm}_{22}.\mathrm{vgs}_{22}\left(\frac{1}{\mathrm{gm}_{21}} \text{ ll } \mathrm{ro}_{21} \text{ ll } \mathrm{ro}_{22}\right) \tag{3.72}$$

where, v_{x+} is the output voltage of the CS amplifier, gm_{21} and gm_{22} are the transconductances of MOSFETs M21 and M22, vgs_{22} is the gate-to-source voltage of MOSFET M22 and $\mathrm{ro}_{21}$and ro_{22} are the output impedances of MOSFETs M21 and M22. The value of $1/\mathrm{gm}_{22}$ is smaller than the ro_{21} and ro_{22}. So, the parallel combination of $1/\mathrm{gm}_{21}$, ro_{22} and ro_{21} yeilds to $1/\mathrm{gm}_{22}$.

Therefore, v_x reduces to

$$v_x = -\frac{\mathrm{gm}_{22}}{\mathrm{gm}_{21}}.\left(\frac{v_z}{2}\right) \tag{3.73}$$

where, $v_z = \mathrm{vgs}_{22}$ due to half symmetry of the circuit.

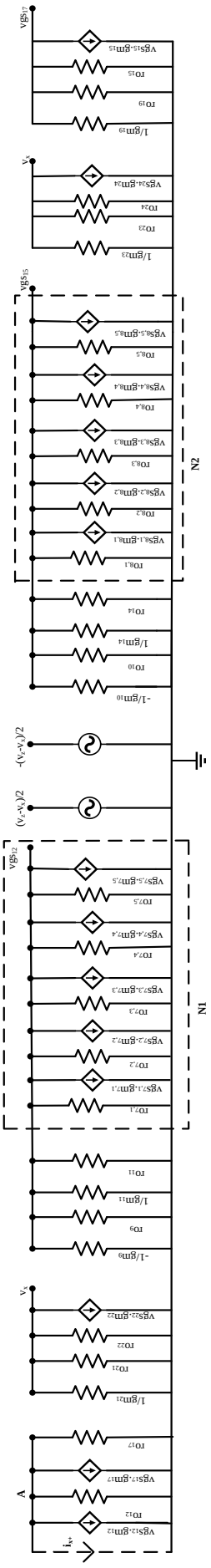


Figure 3.12 Small signal model of PCCDTACS

The gate-to-source voltage of the MOSFET M12 i.e. vgs_{12} in terms of v_z.

$$vgs_{12} = -gm_{7N}.vgs_{7N}.\left(\frac{1}{gm_{11}} \text{ ll } ro_{11} \text{ ll } ro_{7N} \; ll \; (-\frac{1}{gm_9})\right)$$

where, v_{gs12} is the gate-to-source voltage of M12, gm_{11} and gm_9 are the transconductances of MOSFETs M11 and M9, vgs_{7N} is the gate-to-source voltage of all the MOSFET connected in network N1, ro_{11} are the output impedances of MOSFETs M11, ro_{7N} is the output impedance of the parallel combination of all MOSFETs connected in N1 and gm_{7N} is the summation of transconductances of all the MOSFETs in N1 ie. $gm_{7N} = gm_{7,1} + gm_{7,2} + gm_{73} + gm_{7,4} + gm_{7,5}$. The value of $\left(\frac{1}{gm_{11}}\right) and \; (-\frac{1}{gm_9})$ is smaller than the ro_{11} and ro_{7N}. So, the parallel combination of $\left(\frac{1}{gm_{11}}\right), \left(-\frac{1}{gm_9}\right), ro_{11}$ and ro_{7N} yeilds to $(\frac{1}{gm_{11}-gm_9})$. Therefore, vgs_{12} equals:

$$vgs_{12} = -\frac{gm_7}{gm_{11} - gm_9}.\, vgs_{7N} \tag{3.74}$$

$$= -\frac{gm_{7N}}{gm_{11} - gm_9}.\left(\frac{v_z}{2} - \frac{v_x}{2}\right) \tag{3.75}$$

$$= -\frac{gm_{7N}}{gm_{11} - gm_9}.\left(\frac{v_z}{2} + \frac{gm_{22}}{gm_{21}}.\frac{v_z}{2}\right) \tag{3.76}$$

$$= -\frac{gm_7}{gm_{11} - gm_9}.\left(1 + \frac{gm_{22}}{gm_{21}}\right).\frac{v_z}{2} \tag{3.77}$$

The gate-to-source voltage of the MOSFET M15 i.e. vgs_{15} in terms of v_z.

$$vgs_{15} = -gm_{8N}.vgs_{8N}.\left(\frac{1}{gm_{14}} \text{ ll } ro_{14} \text{ ll } ro_{8N} \; ll \; (-\frac{1}{gm_{10}})\right)$$

where, gm_{14} and gm_{10} are the transconductances of MOSFETs M14 and M10 respectively, vgs_{8N} is the gate-to-source voltage of all the MOSFET connected in network N2, ro_{14} are the output impedances of MOSFETs M14, ro_{8N} is the output impedance of the parallel combination of all MOSFETs connected in N2 and gm_{8N} is the summation of transconductances of all the MOSFETs in N2 ie. $gm_{8N} = gm_{8,1} + gm_{8,2} + gm_{8,3} + gm_{8,4} + gm_{8,5}$ .The value of $\left(\frac{1}{gm_{14}}\right) and \; (-\frac{1}{gm_{10}})$ is smaller than the ro_{8N} and ro_{14}. So, the parallel combination of $\left(\frac{1}{gm_{14}}\right), (-\frac{1}{gm_{10}}), ro_8$ and ro_{12} yeilds to $(\frac{1}{gm_{14}-gm_{10}})$. Therefore, vgs_{15} reduces to:

$$vgs_{15} = -\frac{gm_{8N}}{gm_{14} - gm_{10}}.\, vgs_{8N} \tag{3.78}$$

$$= -\frac{gm_{8N}}{gm_8 - gm_{10}}.\left(-\frac{v_z}{2} + \frac{v_x}{2}\right) \tag{3.79}$$

$$= \frac{gm_{8N}}{gm_{14} - gm_{10}}.\left(\frac{v_z}{2} + \frac{gm_{22}}{gm_{21}}.\frac{v_z}{2}\right) \tag{3.80}$$

$$= \frac{gm_{8N}}{gm_{14} - gm_{10}}.\left(1 + \frac{gm_{22}}{gm_{21}}\right).\frac{v_z}{2} \tag{3.81}$$

The gate-to-source voltage of the MOSFET M17 i.e. vgs_{17} in terms of vgs_{15}.

$$vgs_{17} = -gm_{15}.Vgs_{15}.\left(\frac{1}{gm_{19}} \text{ ll } ro_{19} \text{ ll } ro_{15}\right) \tag{3.82}$$

where, v_{gs15} is the gate-to-source voltage of M15, gm_{15} and gm_{19} are the transconductances of MOSFETs M15 and M19 M7 and ro_{15} and ro_{19} are the output impedances of MOSFETs M15 and M19 respectively. The value of $1/gm_{19}$ is smaller than the ro_{19} and ro_{15}. So, the parallel combination of $1/gm_{19}$, ro_{19} and ro_{15} yeilds to $1/gm_{19}$. Therefore, vgs_{17} is:

$$vgs_{17} = -\frac{gm_{15}}{gm_{19}}.\ vgs_{15} \tag{3.83}$$

Substituting the value of Vgs_{15} in Equation (3.83).

$$vgs_{17} = -\frac{gm_{15}}{gm_{19}}.\frac{gm_{8N}}{gm_{14} - gm_{10}}.\left(1 + \frac{gm_{22}}{gm_{21}}\right).\frac{v_z}{2} \tag{3.84}$$

Substituting Equation (3.77) and (3.84) in Equation (3.71).

Therefore,

$$i_{x+} = gm_{12}.\frac{gm_{7N}}{gm_{11} - gm_9}.\left(1 + \frac{gm_{22}}{gm_{21}}\right).\frac{v_z}{2} + gm_{17}.\frac{gm_{15}}{gm_{19}}.\frac{gm_{8N}}{gm_{14} - gm_{10}}.\left(1 + \frac{gm_{22}}{gm_{21}}\right).\frac{v_z}{2} \tag{3.85}$$

The MOSFETs M17 and M19 are symmetrical. Thus, their respective transconductance are also equal i.e. $gm_{17} = gm_{19}$ and they will be cancelled. Hence, the current i_{x+}can be represented:

$$i_{x+} = gm_{12}.\frac{gm_{7N}}{gm_{11} - gm_9}.\left(1 + \frac{gm_{22}}{gm_{21}}\right).\frac{v_z}{2} + gm_{15}.\frac{gm_{8N}}{gm_{14} - gm_{10}}.\left(1 + \frac{gm_{22}}{gm_{21}}\right).\frac{v_z}{2} \tag{3.86}$$

$$= \left(\frac{gm_{12}.gm_{7N}}{gm_{11} - gm_9} + \frac{gm_{15}.gm_{8N}}{gm_{14} - gm_{10}}\right).\left(1 + \frac{gm_{22}}{gm_{21}}\right).\frac{v_z}{2} \tag{3.87}$$

The terms $\frac{gm_{12}.gm_{7N}}{gm_{11} - gm_9}$ and $\frac{gm_{15}.gm_{8N}}{gm_{14} - gm_{10}}$ are equal as the OTA is symmetrical So, we can write:

$$\frac{gm_{12}.gm_{7N}}{gm_{11} - gm_9} = \frac{gm_{15}.gm_{8N}}{gm_{14} - gm_{10}} = gm_{PCCDTACS} \tag{3.88}$$

Simplifying further,

$$gm_{PCCDTACS} = \frac{gm_{12}.gm_{7N}}{gm_{11} - gm_9} \tag{3.89}$$

The MOSFETs M11 and M12 are symmetric, thus $gm_{12} = gm_{11}$

Therefore,

$$gm_{PCCDTACS} = \frac{gm_{7N}}{1 - \frac{gm_9}{gm_{11}}} = \frac{gm_{8N}}{1 - \frac{gm_{10}}{gm_{14}}} \tag{3.90}$$

The factor $\frac{gm_9}{gm_{11}}$ is due to the cross coupled n-MOSFETs. As the positive feedback makes the circuit unstable but by choosing the appropriate values of MOSFETs M9 and M14, the overall

transconductance of the CCDTACS can be improved without effecting the stability of the circuit. Also, the value $\left(\frac{gm_{22}}{gm_{21}}\right)$ can be denoted by a constant A. Thus,

$$i_{x+} = gm_{PCCDTACS}.(1 + A).v_z \tag{3.91}$$

Similarly, i_{x-} can be represented as shown:

$$i_{x-} = -gm_{CCDTACS}.(1 + A).v_z \tag{3.92}$$

The $gm_{PCCDTACS}$ represents the new transconductance of the proposed PCCDTACS in which the transconductance of the proposed CCDTACS is boosted by the ratio of $\frac{gm_9}{gm_{11}}$ or $\frac{gm_{10}}{gm_{14}}$.

3.5.1 KHN filter based on proposed PCCDTACS

A Kerwin-Huelsman-Newcomb (KHN) filter designed using the proposed PCCDTACS is shown in Figure 3.13. The KHN filter is constructed by cascading of two proposed PCCDTACS circuits with passive elements to obtain the frequency response of High Pass (HP), Low Pass (LP) and Band Pass (BP) filters.

The center frequency of the KHN filter (fo) is given as:

$$fo = \frac{1}{2\pi} . \sqrt{\frac{gm_{PCCDTACS1}.gm_{PCCDTACS2}}{C_1 . C_2}} \tag{3.93}$$

where, $gm_{PCCDTACS1} = gm_{PCCDTACS2} = gm_{PCCDTACS}$ are the transconductances of the proposed PCCDTACS, C_1 and C_2 are the two equal value grounded capacitances connected across the terminals of the KHN filter.

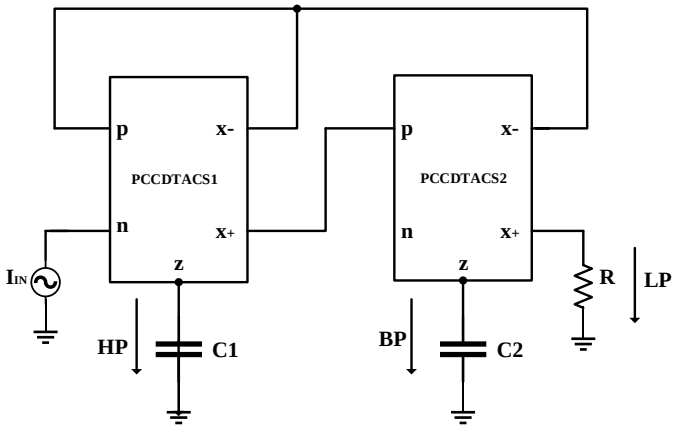


Figure 3.13 KHN Filter using proposed PCCDTACS

CHAPTER 4

SIMULATION RESULTS

This chapter describes the simulation results of all the proposed CDTA circuits. The proposed circuits are designed and simulated in Cadence Virtuoso Analog Design Environment using BSIM3V3 180nm CMOS technology. The Section 4.1 describes the simulation results of proposed current differencing transconductance amplifier with common source amplifier (CDTACS). A KHN filter based on proposed CDTACS is also presented. The simulation results of proposed CDTA with parallel n-MOSFETs (PCDTACS) along with a KHN filter as an application are presented in Section 4.2. Section 4.3 addresses the simulation results of proposed CDTA with cross-coupled n-MOSFETs (CCDTACS). The simulation results of a KHN filter based on CCDTACS for different values of capacitances are also addressed. The simulation results of proposed CDTA with CS amplifier, Cross-coupled n-MOSFETs and parallel n-MOSFETs (PCCDTACS) are discussed in section 4.4. The chapter concludes with Section 4.5, which presents the comparison of different CDTA structures available in literature with the proposed CDTA circuits.

4.1 SIMULATION RESULTS OF PROPOSED CDTACS

The bias currents of the proposed CDTACS circuit are chosen as I_{bias} = 30µA and I_{bias_2} = 200 µA. The supply voltages are selected as V_{DD} = -V_{SS} = 0.9V. The aspect ratios of the MOSFETs used to design CDTACS is given in the Table 4.1.

Table 4.1 Aspect ratios of MOSFETs

S.No.	MOSFETs	Aspect ratio (µm/µm)
1.	M1 - M4	32/2
2.	M5, M6	42.5/0.36
3.	M7, M8	50/036
4.	M9 – M14	20/0.36
5.	M15 – M18	10/0.36
6.	M19, M21	5/0.36
7.	M20, M22	6/0.36

For AC analysis, two input sinusoidal currents Ip and In are applied to the CDTACS. The AC magnitudes of the input currents are 40µA and 30µA with a DC offset of 100mV. The current transfer characteristics are plotted over a range of frequency from 1 Hz to 10GHz. These plots show the variation of the currents at output ports with respect to the input ports. The graphs are plotted for different current ratios such as Ix+/Ip, Ix+/In, Iz/Ip and Iz/In are shown in Figures 4.1, 4.2, 4.3 and 4.4 respectively. The -3dB bandwidth of the circuit for these different current gains is also observed. Figure 4.1 shows the variation of the Ix+/Ip and the -3dB bandwidth is observed as 48.91MHz.

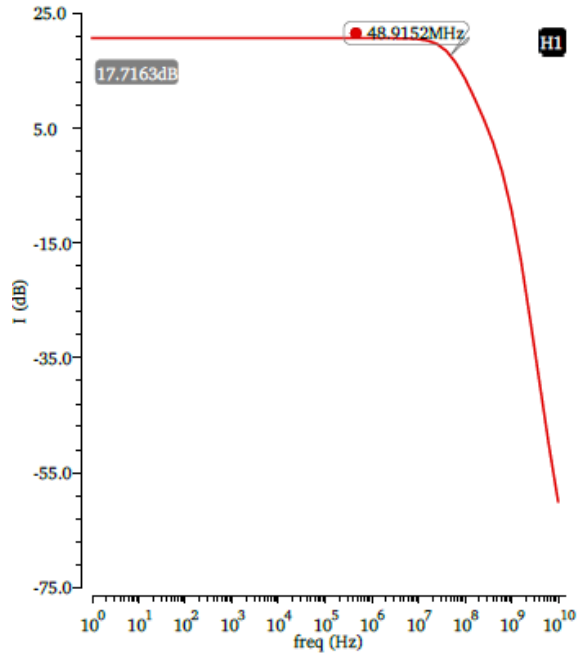


Figure 4.1 Variation of Ix+/Ip at bias current of 200µA

Figure 4.2 shows the frequency response of the CDTACS for the Ix+/In current gain. The -3dB bandwidth is observed to be 48.91 MHz.

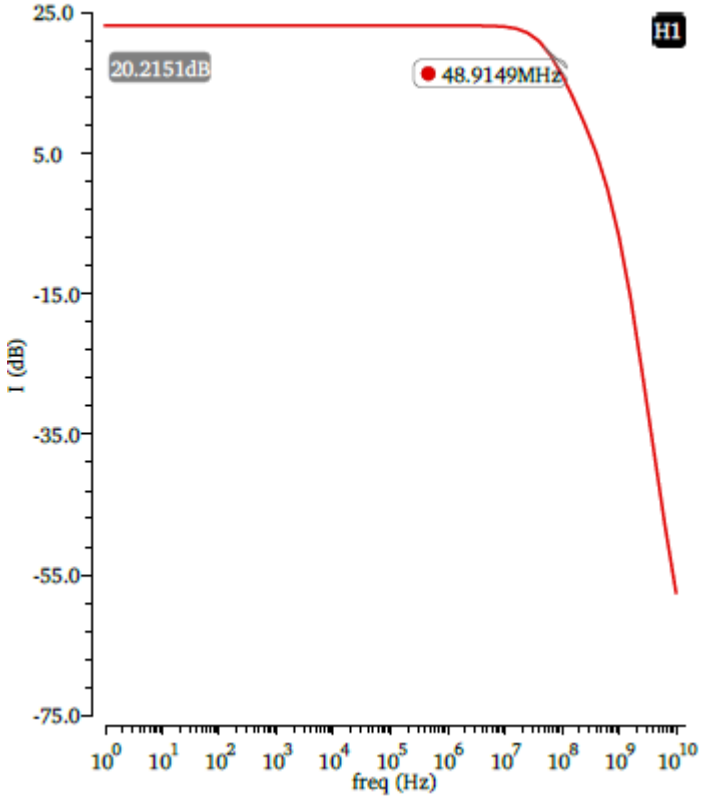


Figure 4.2 Variation of Ix+/In at bias current of 200µA

Figures 4.3 and 4.4 show the variations of the current at the Z terminal to the input currents over a range of frequency from 1 Hz to 10 GHz. The biasing current I_{bias_2} is kept constant at a value of 200µA. The -3dB bandwidth of the circuits for these current gains are observed as 49.16 MHz each.

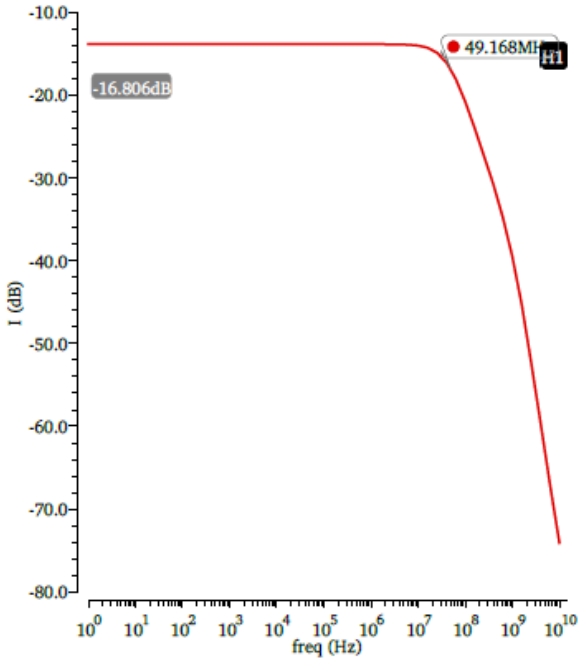


Figure 4.3 Iz/Ip versus frequency

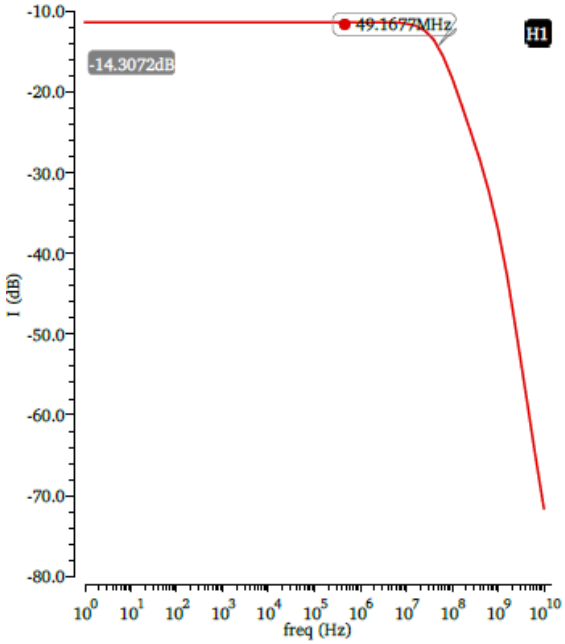


Figure 4.4 Iz/In versus frequency

Figure 4.5 shows the plot between the transconductance (in dB) of the CDTACS over a frequency range of 1 Hz to 10 GHz for constant $Ibias_2$ of 200µA. The -3dB bandwidth of the CDTACS is found to be 637MHz.

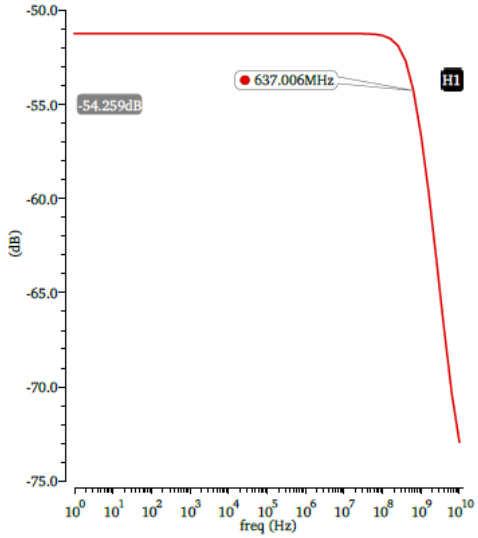


Figure 4.5 Gain vs frequency plot of CDTACS

The -3dB bandwidth of the CDTACS can be observed from the Figures 4.1, 4.2, 4.3, 4.4 and 4.5. The different values of bandwidth are 48.91 MHz, 48.91 MHz, 49.16 MHz, 49.16 MHz and 637 MHz. Thus, the bandwidth of the CDTACS is the minimum of the mentioned values i.e. 48.91 MHz.

Figure 4.6 shows the range of transconductance for different values of bias current ($Ibias_2$). The bias current is varied from 1µA to 200µA with selected values of 1 µA, 2 µA, 3 µA, 4 µA, 5 µA, 10 µA, 20 µA, 30 µA, 40 µA, 50 µA, 60 µA, 70 µA, 80 µA, 90 µA, 100 µA, 150 µA and 200 µA. From the Figure the maximum value of transconductance of the CDTACS is 2.74mS for 200µA of bias current.

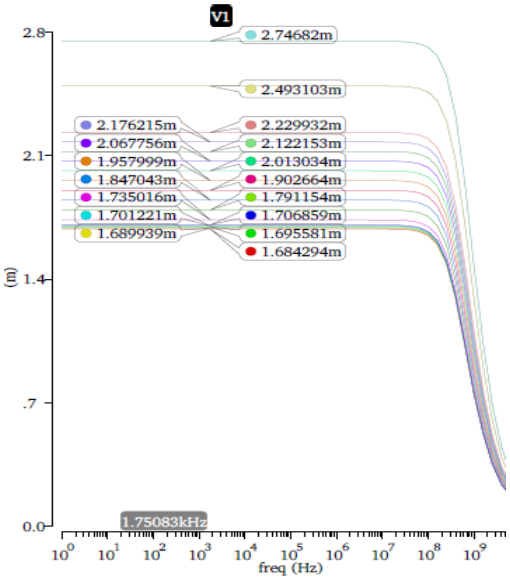


Figure 4.6 Transconductance of CDTACS

The transient analysis of the circuit is performed by applying two square input current pulses at the nodes ‘p’ and ‘n’. The currents Ip and In are chosen as 40µA and 20µA peak-to-peak, respectively with time period of 1µs and the pulse width of 0.5µS. Figure 4.7 shows the transient response of the proposed CDTACS circuit. The transient analysis concludes that the two output currents are out-of-phase with each other and amplified. The peak-to-peak magnitude of the output currents Ix+ and Ix- are found out to be 120mA and 120mA.

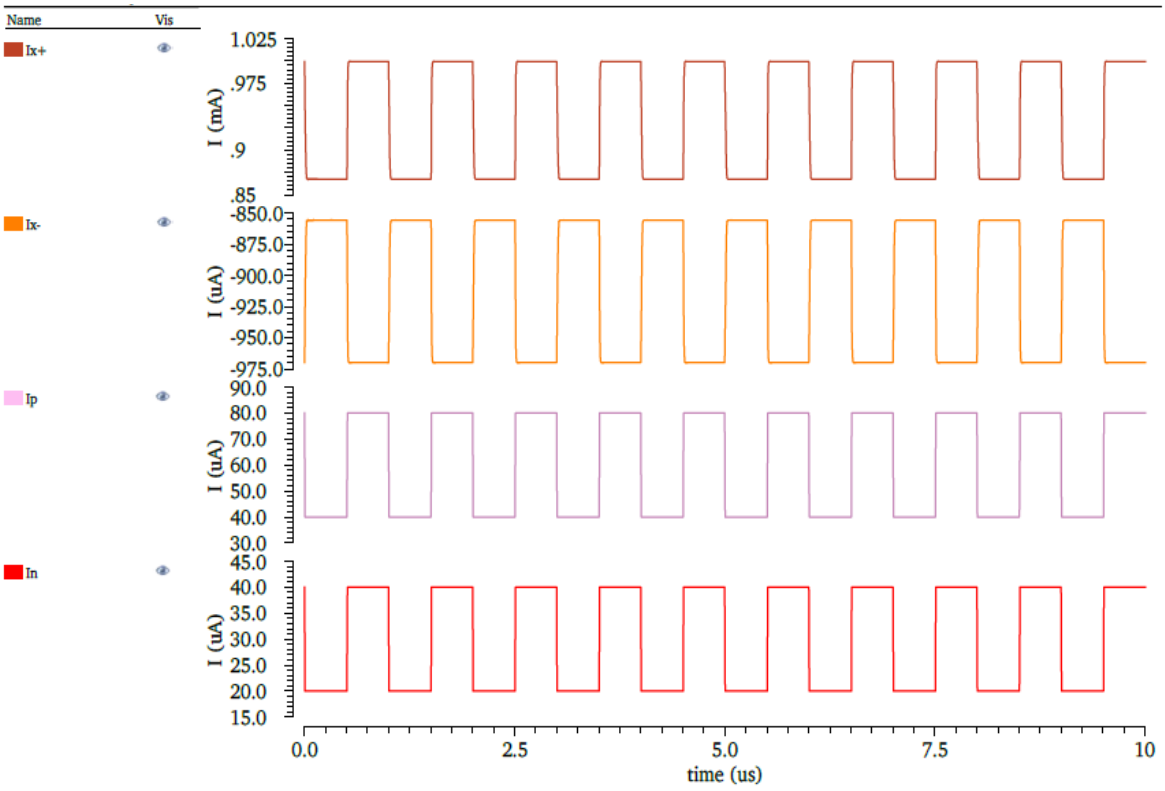


Figure 4.7 Transient response of CDTACS

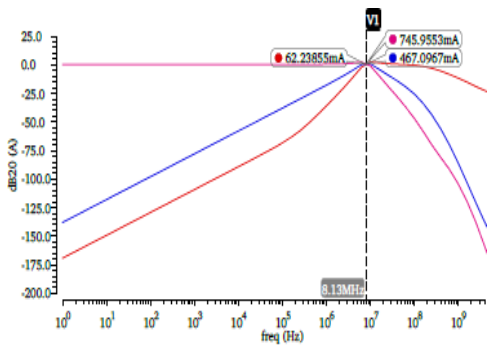
The Table 4.2 shows the comparison between the conventional CDTA and the proposed CDTACS on the basis of transconductance and dynamic power. From the table, it is observed that the dynamic power of CDTACS remains in close proximity to the dynamic power of conventional CDTA but the transconductance (gm) is increased by 2 times. Thus, the proposed CDTACS offers better transconductance than the conventional CDTA.

Table 4.2 Comparison between conventional CDTA and proposed CDTACS

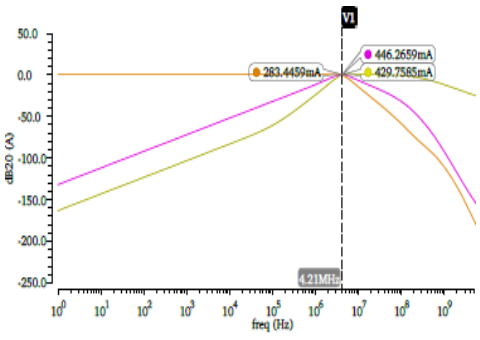
$Ibias_2$ (µA)	Conventional CDTA		Proposed CDTACS	
	Transconductance (µS)	Dynamic Power (mW)	Transconductance (mS)	Dynamic Power (mW)
1	10.68	2.06	1.684	2.03
2	20.19	2.07	1.69	2.04
3	29.15	2.073	1.696	2.044
4	37.73	2.076	1.7	2.048
5	46.02	2.079	1.708	2.05
10	84.71	2.09	1.73	2.07
20	154.66	2.12	1.79	2.11
30	219.44	2.16	1.84	2.15
40	281.07	2.19	1.9	2.19
50	340.39	2.22	1.95	2.23
60	397.86	2.25	2.01	2.27
70	453.77	2.28	2.06	2.31
80	508.3	2.31	2.12	2.35
90	561.57	2.35	2.17	2.39
100	613.71	2.38	2.23	2.43
150	859.51	2.54	2.49	2.64
200	1080	2.74	2.74	2.85

4.1.1 Simulation results of KHN Filter using proposed CDTACS

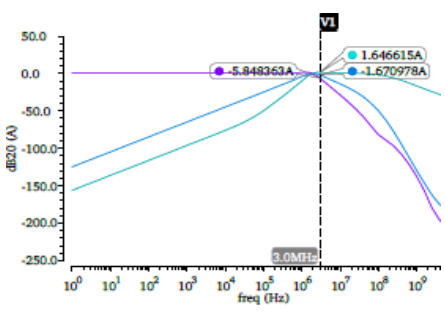
The KHN Filter has been simulated using four different values of capacitances selected as 50pF, 100pF, 150pF and 200pF with a low valued resistance of 1Ω. The values of transconductances of CDTACS are chosen as $gm_{CDTACS1} = gm_{CDTACS2} = 2.74$mS by keeping the bias current at 200µA. The frequencies of KHN filter for different values of capacitances are shown in Figure 4.8 (a), (b), (c) and (d).



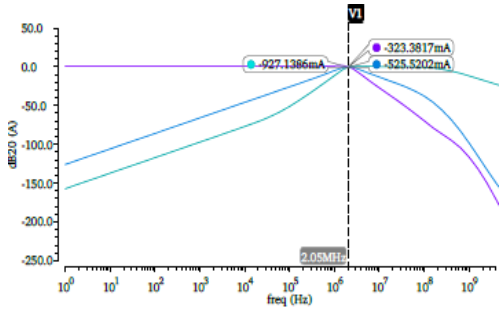
(a) C1 = C2 = 50pF



(b) C1 = C2 = 100pF



(c) C1 = C2 = 150pF



(d) C1 = C2 = 200pF

Figure 4.8 Frequency response of KHN filter with R=1Ω

Table 4.3 Center frequency at different values of capacitances

S. No.	Capacitance (pF)	Theoretical value of center frequency (fo) (MHz)	Actual value of center frequency (fo) (MHz)
1.	50	8.72	8.13
2.	100	4.36	4.21
3.	150	3.12	3.0
4.	200	2.18	2.05

From Figures 4.8 (a), (b), (c) and (d), the obtained center frequencies are listed in Table 4.3 which compares the actual value of center frequency to the theoretical value for different values of the capacitances. The dynamic power of the proposed KHN filter based on proposed CDTACS is 15.2mW which is less than that of the conventional CDTA (19.31mW).

4.2 SIMULATION RESULTS OF PROPOSED PCDTACS

The bias currents of the proposed PCDTACS circuit are selected I_{bias} = 30µA each and I_{bias_2} = 200 µA. The supply voltages are chosen as V_{DD} = -V_{SS} = 0.9V. The aspect ratios of the MOSFETs used to design PCDTACS is given in the Table 4.4.

Table 4.4 Aspect ratios of MOSFETs

S.No.	MOSFETs	Aspect ratio (µm/µm)
1.	M1 - M4	32/2
2.	M5, M6	42.5/0.36
3.	$M7_{1\text{-}N}$, $M8_{1\text{-}N}$	50/036
4.	M9 – M14	20/0.36
5.	M15 – M18	10/0.36
6.	M19, M21	5/0.36
7.	M20, M22	6/0.36

For AC analysis, two input sinusoidal currents Ip and In are applied to the PCDTACS. The AC magnitudes of the input currents are 40µA and 30µA with a DC offset of 100mV. The current transfer characteristics are plotted over a range of frequency from 1 Hz to 10GHz. These plots show the variation

of the currents at output ports with respect to the input ports. The graphs are plotted for different current ratios such as Ix+/Ip, Ix+/In, Iz/Ip and Iz/In are shown in Figures 4.9, 4.10, 4.11 and 4.12 respectively. The -3dB bandwidth of the circuit for these different current gains is also observed. Figure 4.9 shows the variation of the Ix+/Ip and the -3dB bandwidth is observed as 33.42MHz.

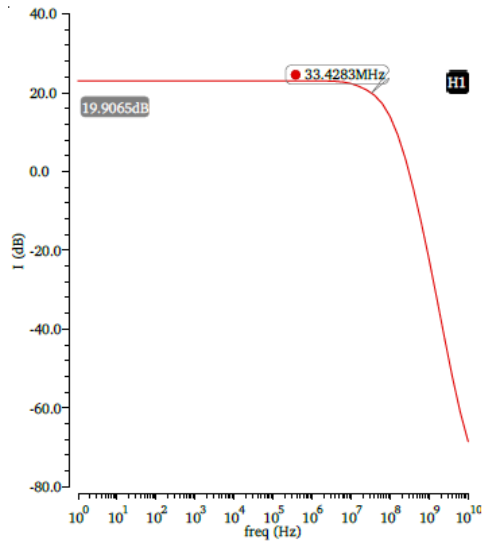


Figure 4.9 Frequency response of Ix+/Ip at bias current of 200µA

Figure 4.12 shows the frequency response of the PCDTACS for the Ix+/In current gain. The -3dB bandwidth is observed to be 34.32MHz.

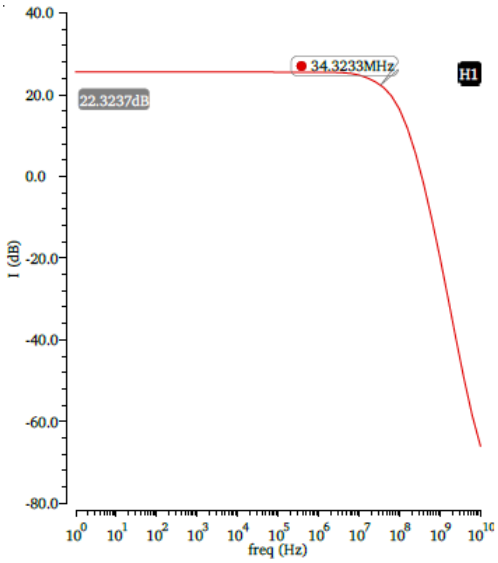


Figure 4.10 Frequency response of Ix+/In for bias current of 200µA

Figures 4.11 and 4.12 show the variations of the current at the Z terminal to the input currents over a range of frequency from 1 Hz to 10 GHz. The biasing current I_{bias_2} is kept constant at a value of 200µA. The -3dB bandwidth of the circuits for these current gains are observed as 36.44 MHz and 36.78 MHz.

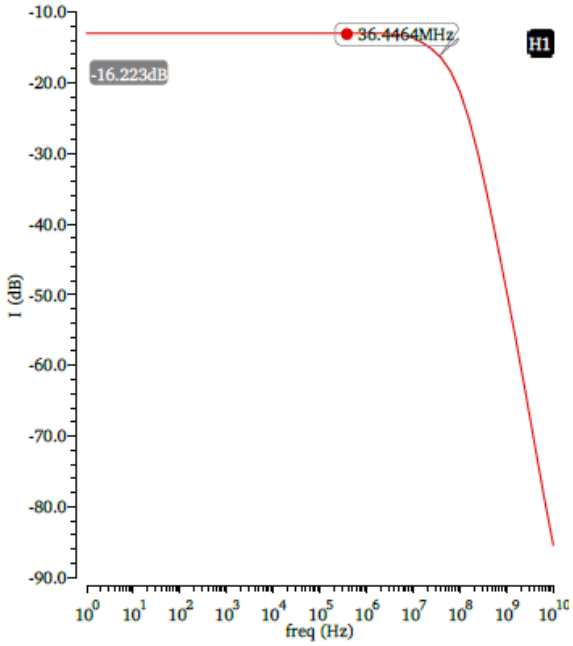


Figure 4.11 Variation of Iz/Ip at bias current of 200µA

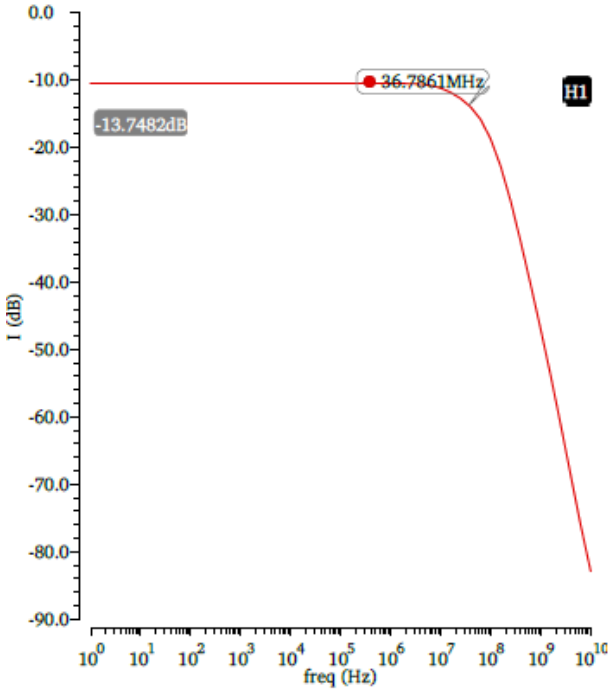


Figure 4.12 Iz/In versus frequency at bias current of 200µA

Figure 4.13 shows the plot between the transconductance (in dB) of the PCDTACS over a frequency range of 1 Hz to 10 GHz for constant I_{bias_2} of 200µA. The -3dB bandwidth of the PCDTACS is found to be 295.99MHz.

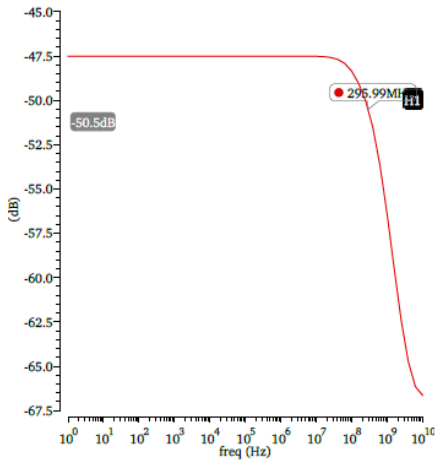


Figure 4.13 Gain vs frequency plot of PCDTACS

The -3dB bandwidth of the PCDTACS can be observed from the Figures 4.9, 4.10, 4.11, 4.12 and 4.13. The different values of bandwidth are 33.42 MHz, 34.32 MHz, 36.44 MHz, 36.78 MHz and 295.99 MHz. The bandwidth of the PCDTACS is the minimum of all these values i.e. 33.42 MHz.

Figure 4.14 shows the range of transconductance for different values of bias current ($Ibias_2$). The bias current is varied from 1µA to 200µA with selected values of 1 µA, 2 µA, 3 µA, 4 µA, 5 µA, 10 µA, 20 µA, 30 µA, 40 µA, 50 µA, 60 µA, 70 µA, 80 µA, 90 µA, 100 µA, 150 µA and 200 µA. From the Figure the maximum value of transconductance of the PCDTACS is found out to be 4.21mS for 200µA of bias current.

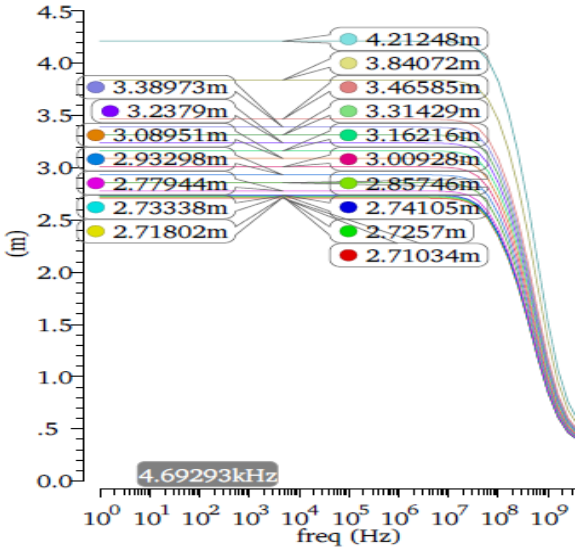


Figure 4.14 Transconductance of PCDTACS

The transient analysis of the circuit is performed by applying two square input current pulses at the nodes ‘p’ and ‘n’. The currents Ip and In are chosen as 20µA peak-to-peak, respectively with time period of 1µs and the pulse width of 0.5µS. Figure 4.15 shows the transient response of the proposed CDTACS circuit. The transient analysis concludes that the two output currents are out-of-phase with

each other and amplified. The peak-to-peak magnitude of the output currents Ix+ and Ix- are found out to be 750mA and 750mA.

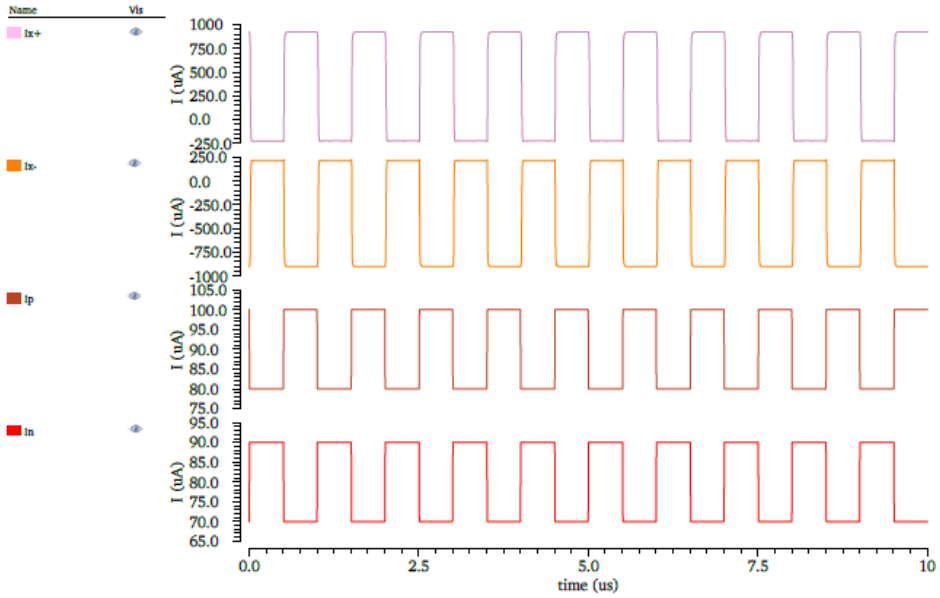


Figure 4.15 Transient response of PCDTACS

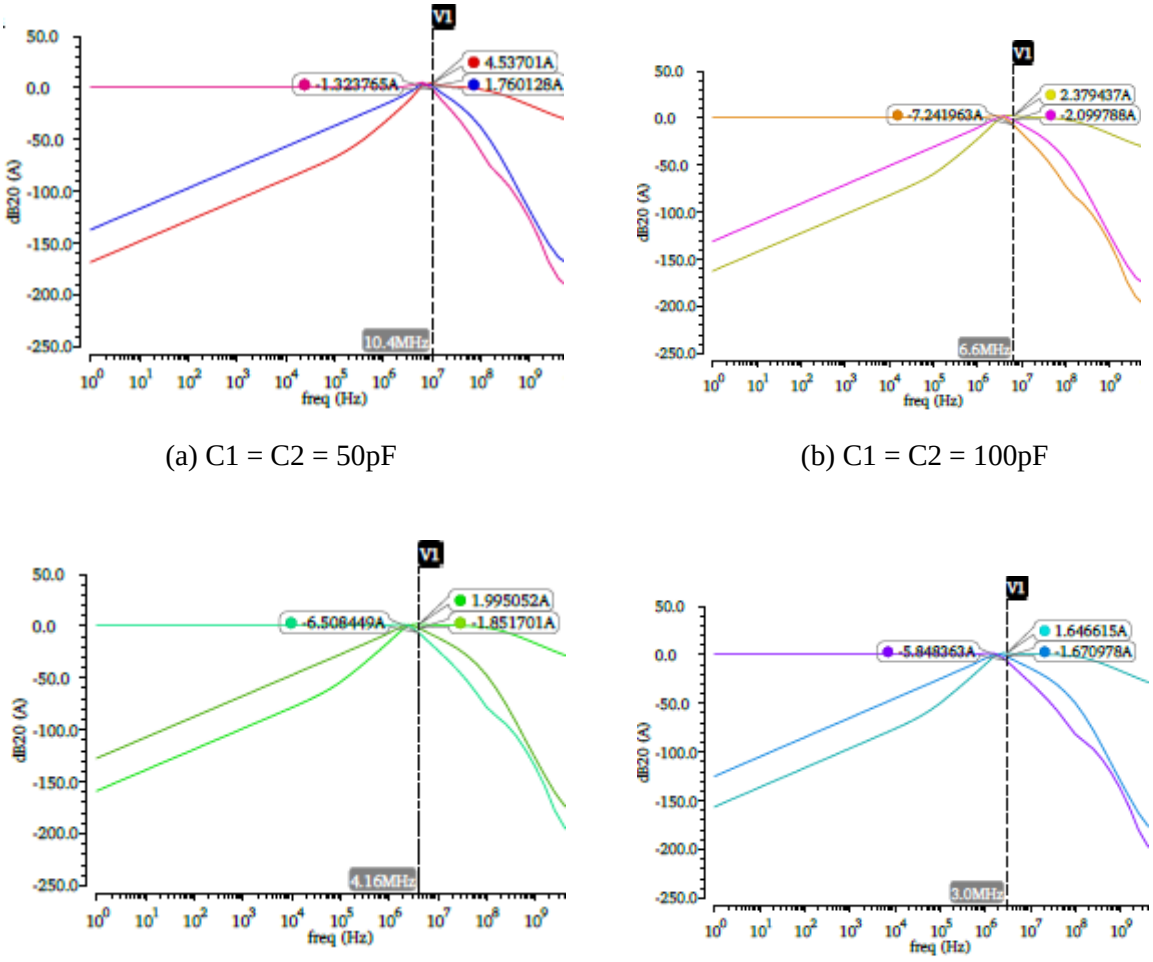
Table 4.5 shows the comparison between the proposed CDTACS and the proposed PCDTACS on the basis of transconductance and dynamic power. From the table, it is observed that the dynamic power of CDTACS remains in close proximity to the dynamic power of proposed PCDTACS but the transconductance (gm) is increased by 1.5 times. Thus, the proposed PCDTACS offers better transconductance than the CDTACS.

Table 4.5 Comparison between proposed CDTACS and proposed PCDTACS

$Ibias_2$ (µA)	**Proposed CDTACS**		**Proposed PCDTACS**	
	Transconductance (mS)	**Dynamic Power (mW)**	**Transconductance (mS)**	**Dynamic Power (mW)**
1	1.684	2.71	2.32	2.03
2	1.69	2.718	2.334	2.04
3	1.696	2.72	2.338	2.044
4	1.7	2.73	2.342	2.048
5	1.708	2.74	2.346	2.05
10	1.73	2.77	2.36	2.07
20	1.79	2.85	2.41	2.11
30	1.84	2.93	2.45	2.15
40	1.9	3.0	2.49	2.19
50	1.95	3.09	2.54	2.23
60	2.01	3.16	2.58	2.27
70	2.06	3.23	2.62	2.31
80	2.12	3.31	2.67	2.35
90	2.17	3.39	2.71	2.39
100	2.23	3.46	2.75	2.43
150	2.49	3.84	2.97	2.64
200	2.74	4.21	3.2	2.85

4.2.1 Simulation results of KHN Filter using proposed PCDTACS

The KHN Filter has been simulated using four different values of capacitances selected as 50pF, 100pF, 150pF and 200pF with a low valued resistance of 1Ω. The values of transconductances of PCDTACS are chosen as $gm_{PCDTACS1} = gm_{PCDTACS2} = 4.21mS$ by keeping the bias current at 200µA. The frequencies of KHN filter for different values of capacitances are shown in Figure 4.16 (a), (b), (c) and (d).



(a) C1 = C2 = 50pF

(b) C1 = C2 = 100pF

(c) C1 = C2 = 150pF

(d) C1 = C2 = 200pF

Figure 4.16 Frequency response of KHN filter with R=1Ω

Table 4.6 Center frequency at different values of capacitances

S. No.	Capacitance (pF)	Theoretical value of center frequency (fo) (MHz)	Actual value of center frequency (fo) (MHz)
1.	50	13.4	10.4
2.	100	6.7	6.6
3.	150	4.46	4.16
4.	200	3.16	3.0

From Figures 4.18 (a), (b), (c) and (d), the obtained center frequencies are listed in Table 4.6 which compares the actual value of center frequency to the theoretical value for different values of the capacitances. The dynamic power of the proposed KHN filter using PCDTACS is 5mW which is less than that of the proposed CDTACS (15.2mW).

4.3 SIMULATION RESULTS OF PROPOSED CCDTACS

The bias currents of the proposed CDTACS circuit are selected as Ibias = 30µA each and I_{bias_2} = 200 µA. The supply voltages are chosen as V_{DD} = -V_{SS} = 0.9V. The aspect ratios of the MOSFETs used to design CDTACS is given in the Table 4.7.

Table 4.7 Aspect ratios of MOSFETs

S.No.	MOSFETs	Aspect ratio (µm/µm)
1.	M1 - M4	32/2
2.	M5, M6	42.5/0.36
3.	M7, M8	50/036
4.	M9 – M10	15/0.36
5.	M11 – M16	20/0.36
6.	M17 – M20	10/0.36
7.	M21, M23	5/0.36
8.	M22, M24	6/0.36

For AC analysis, two input sinusoidal currents Ip and In are applied to the CCDTACS. The AC magnitudes of the input currents are 40µA and 30µA with a DC offset of 100mV. The current transfer characteristics are plotted over a range of frequency from 1 Hz to 10GHz. These plots show the variation of the currents at output ports with respect to the input ports. The graphs are plotted for different current ratios such as Ix+/Ip, Ix+/In, Iz/Ip and Iz/In are shown in Figures 4.17, 4.18, 4.19 and 4.20 respectively. The -3dB bandwidth of the circuit for these different current gains is also observed. Figure 4.17 shows the variation of the Ix+/Ip and the -3dB bandwidth is observed 49.11MHz.

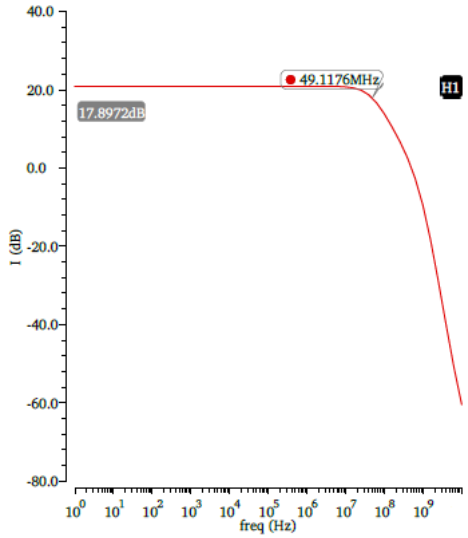


Figure 4.17 Plot of Ix+/Ip versus frequency at I_{bias_2} = 200µA

Figure 4.18 shows the frequency response of the CCDTACS for the Ix+/In current gain. The -3dB bandwidth is observed to be 50.11 MHz.

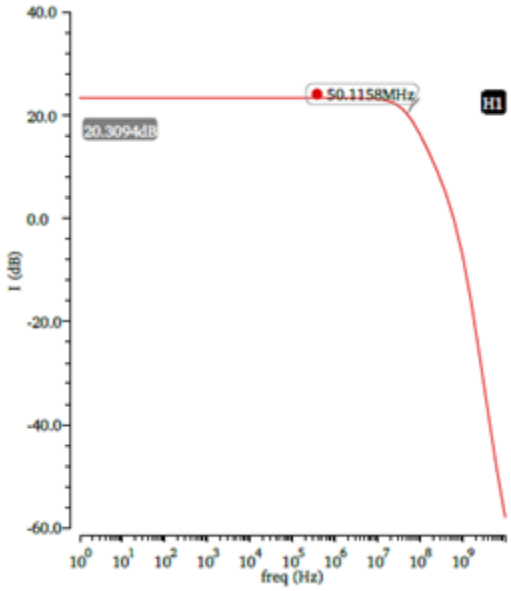


Figure 4.18 Variation of Ix+/In at at I_{bias_2} = 200µA

Figures 4.19 and 4.20 show the variations of the current at the Z terminal to the input currents over a range of frequency from 1 Hz to 10 GHz. The biasing current I_{bias_2} is kept constant at a value of 200µA. The -3dB bandwidth of the circuits for these current gains are observed as 55.11 MHz and 49.41 MHz.

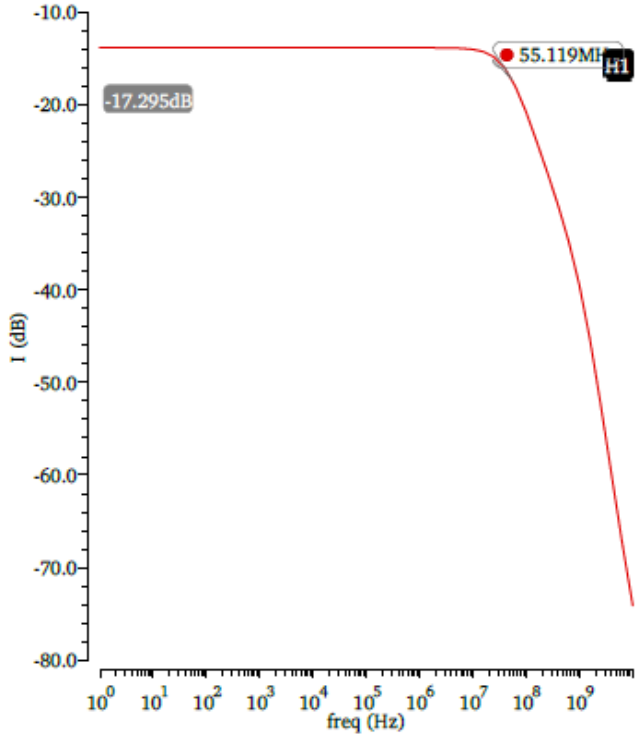


Figure 4.19 Current transfer characteristics of Iz/Ip at biasing current of 200µA

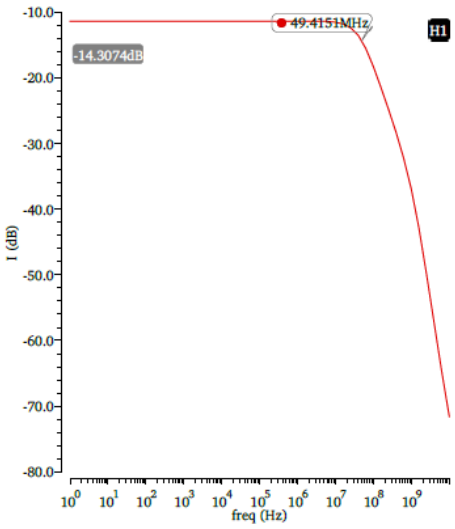


Figure 4.20 Iz/In versus frequency at biasing current of 200µA

Figure 4.21 shows the plot between the transconductance (in dB) of the CCDTACS over a frequency range of 1 Hz to 10 GHz for constant $Ibias_2$ of 200µA. The -3dB bandwidth of the CDTACS is found to be 309.32 MHz.

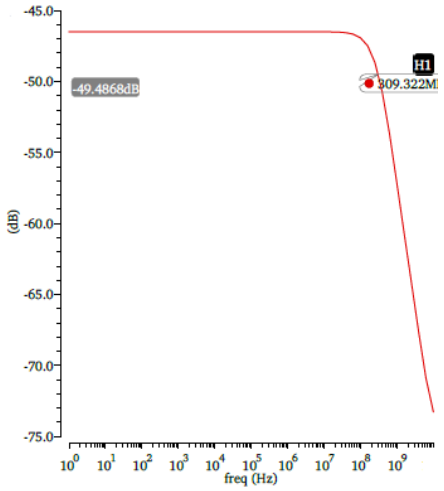


Figure 4.21 Frequency response of CCDTACS at $Ibias_2$ = 200µA

The -3dB bandwidth of the CCDTACS can be observed from the Figures 4.17, 4.18, 4.19, 4.20 and 4.21. The different values of bandwidth are 49.11 MHz, 50.11 MHz, 55.11 MHz, 49.41 MHz and 309.322 MHz. The bandwidth of the CCDTACS is the minimum of the mentioned values i.e. 49.11 MHz.

Figure 4.22 shows the range of transconductance for different values of bias current ($Ibias_2$). The bias current is varied from 1µA to 200µA with selected values of 1 µA, 2 µA, 3 µA, 4 µA, 5 µA, 10 µA, 20 µA, 30 µA, 40 µA, 50 µA, 60 µA, 70 µA, 80 µA, 90 µA, 100 µA, 150 µA and 200 µA. From the Figure the maximum value of transconductance of the CCDTACS is found out to be 4.73mS for 200µA of bias current.

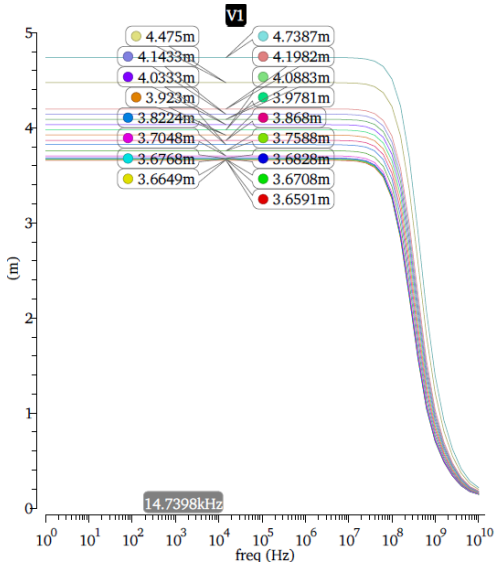


Figure 4.22 Transconductance versus frequency plot of CCDTACS

The transient analysis of the circuit is performed by applying two square input current pulses at the nodes ‘p’ and ‘n’. The currents Ip and In are chosen as 40µA and 20µA peak-to-peak, respectively with time period of 1µs and the pulse width of 0.5µS. Figure 4.23 shows the transient response of the proposed CCDTACS circuit. The transient analysis concludes that the two output currents are out-of-phase with each other and amplified. The peak-to-peak magnitude of the output currents Ix+ and Ix- are found out to be 700mA and 700mA.

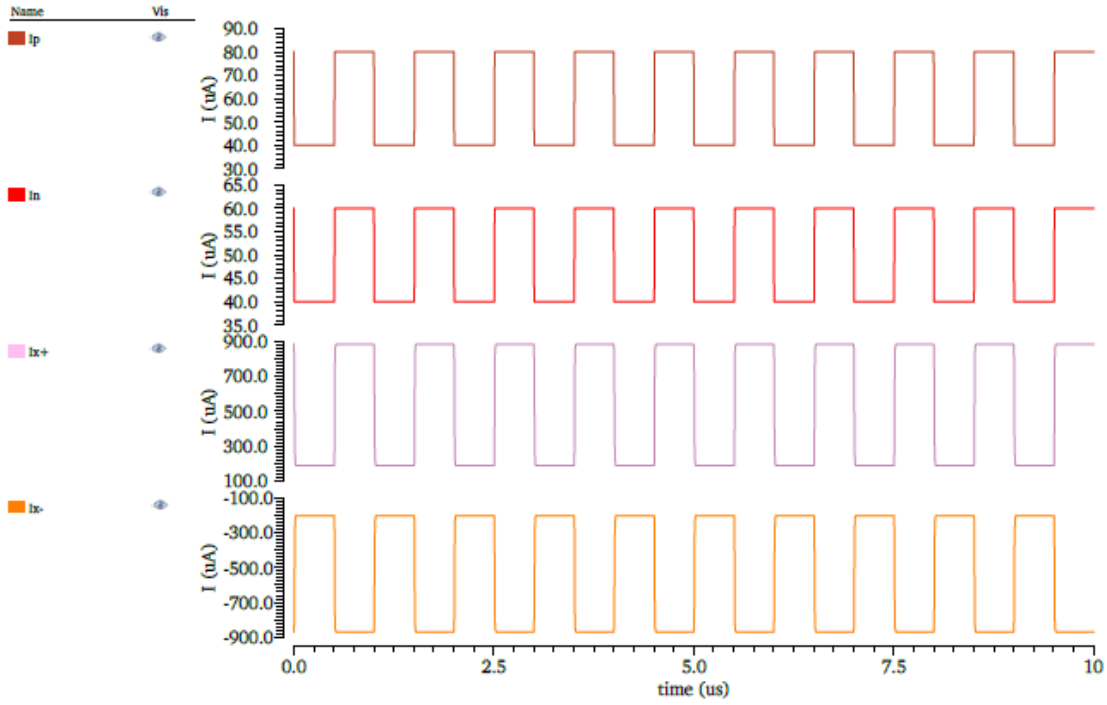


Figure 4.23 Transient response of CCDTACS

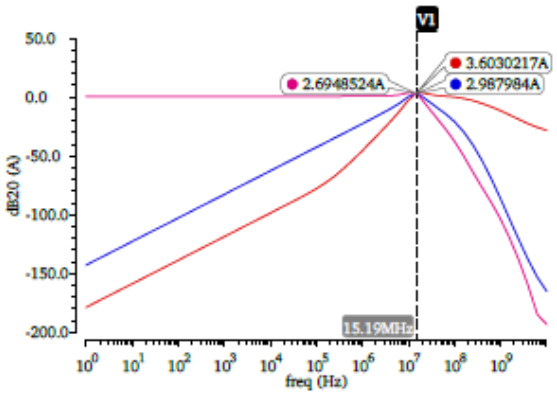
Table 4.8 shows the comparison between the PCDTACS and the proposed CCDTACS on the basis of transconductance and dynamic power. From the table, it is observed that the dynamic power of CCDTACS is less than that of proposed PCDTACS but the transconductance (gm) is increased by 1.14 times. Thus, the proposed CCDTACS offers better transconductance and has less dynamic power than the proposed PCDTACS.

Table 4.8 Comparison between proposed PCDTACS and proposed CCDTACS

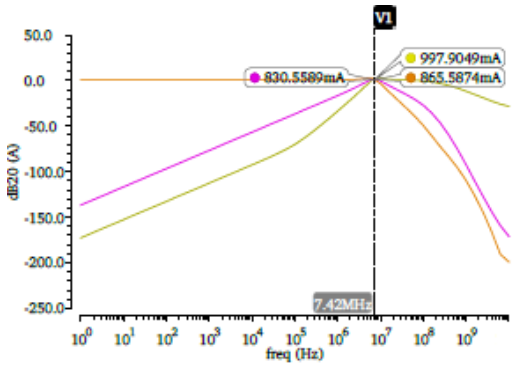
`	**Proposed PCDTACS**		**Proposed CCDTACS**	
	Transconductance (mS)	**Dynamic Range (mW)**	**Transconductance (mS)**	**Dynamic Power (mW)**
1	2.71	2.32	3.65	2.27
2	2.718	2.334	3.66	2.281
3	2.72	2.338	3.65	2.285
4	2.73	2.342	3.65	2.289
5	2.74	2.346	3.65	2.29
10	2.77	2.36	3.65	2.31
20	2.85	2.41	3.65	2.35
30	2.93	2.45	3.65	2.39
40	3.0	2.49	3.65	2.43
50	3.09	2.54	3.65	2.47
60	3.16	2.58	3.65	2.51
70	3.23	2.62	3.65	2.55
80	3.31	2.67	3.65	2.59
90	3.39	2.71	3.65	2.63
100	3.46	2.75	4.19	2.67
150	3.84	2.97	4.47	2.88
200	4.21	3.2	4.73	3.0

4.3.1 Simulation results of KHN Filter using proposed CCDTACS

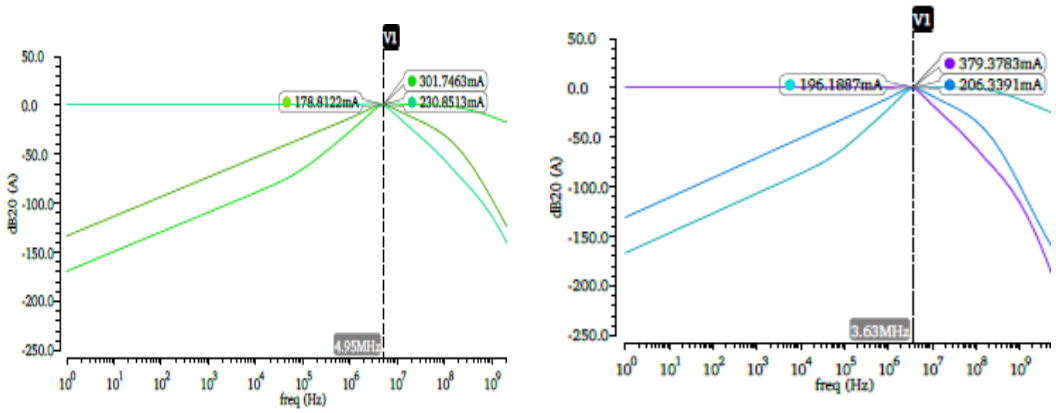
The KHN Filter has been simulated using four different values of capacitances selected as 50pF, 100pF, 150pF and 200pF with a low valued resistance of 1Ω. The values of transconductances of CDTACS are chosen as $gm_{CCDTACS1} = gm_{CCDTACS2} = 4.73$ mS by keeping the bias current at 200µA. The frequencies of KHN filter for different values of capacitances are shown in Figure 4.24 (a), (b), (c) and (d).



(a) C1 = C2 = 50pF



(b) C1 = C2 = 100pF



(c) C1 = C2 = 150pF (d) C1 = C2 = 200pF

Figure 4.24 Frequency response of KHN Filter with R=1Ω

Table 4.9 Center frequency with different capacitances

S. No.	Capacitance (pF)	Theoretical value of center frequency (fo) (MHz)	Actual value of center frequency (fo) (MHz)
1.	50	15.05	15.19
2.	100	7.52	7.42
3.	150	5.01	4.95
4.	200	3.76	3.63

From Figures 4.26 (a), (b), (c) and (d), the obtained center frequencies are listed in Table 4.9 which compares the actual value of center frequency to the theoretical value for different values of the capacitances. The dynamic power of the proposed KHN filter using CCDTACS is 6mW which is in close range to that of proposed PCDTACS (5mW).

4.4 SIMULATION RESULTS OF PROPOSED PCCDTACS

The bias currents of the proposed CDTACS circuit are chosen as I_{bias} = 30µA each and I_{bias_2} = 200 µA. The supply voltages are selected as V_{DD} = -V_{SS} = 0.9V. The aspect ratios of the MOSFETs used to design PCCDTACS is given in the Table 4.10.

Table 4.10 Aspect ratios of MOSFETs

S.No.	MOSFETs	Aspect ratio (µm/µm)
1.	M1 - M4	32/2
2.	M5, M6	42.5/0.36
3.	$M7_N$, $M8_N$	50/036
4.	M9 – M14	20/0.36
5.	M15 – M18	10/0.36
6.	M19, M21	5/0.36
7.	M20, M22	6/0.36

For AC analysis, two input sinusoidal currents Ip and In are applied to the PCCDTACS. The AC magnitudes of the input currents are 40µA and 30µA with a DC offset of 100mV. The current transfer characteristics are plotted over a range of frequency from 1 Hz to 10GHz. These plots show the variation of the currents at output ports with respect to the input ports. The graphs are plotted for different current ratios such as Ix+/Ip, Ix+/In, Iz/Ip and Iz/In are shown in Figures 4.25, 4.26, 4.27 and 4.28 respectively. The -3dB bandwidth of the circuit for these different current gains is also observed. Figure 4.25 shows the variation of the Ix+/Ip and the -3dB bandwidth is observed as 20.511 MHz.

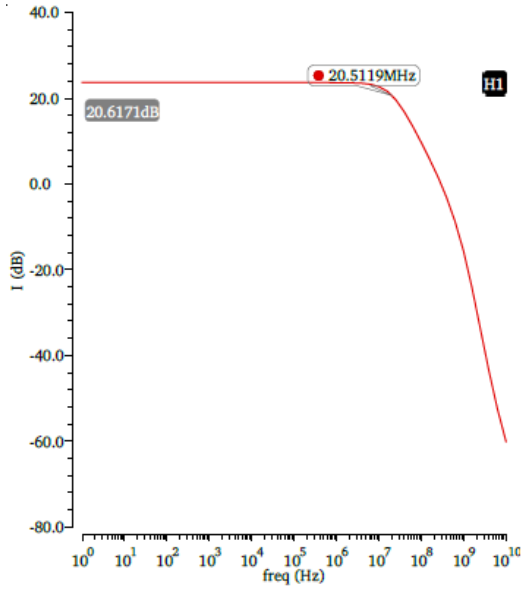


Figure 4.25 Variation of Ix+/Ip at bias current of 200µA

Figure 4.26 shows the frequency response of the PCCDTACS for the Ix+/In current gain. The -3dB bandwidth is observed to be 20.02 MHz.

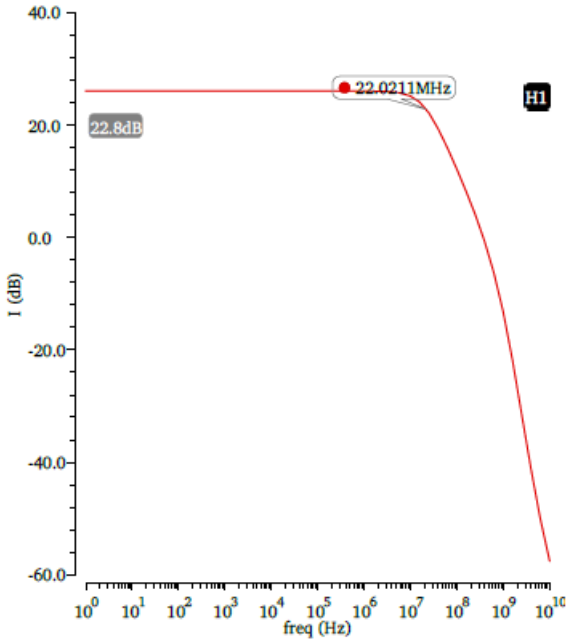


Figure 4.26 Ix+/In versus frequency at bias current of 200µA

Figures 4.27 and 4.28 show the variations of the current at the Z terminal to the input currents over a range of frequency from 1 Hz to 10 GHz. The biasing current I_{bias_2} is kept constant at a value of 200µA. The -3dB bandwidth of the circuits for these current gains are observed as 21.51 MHz and 21.07 MHz.

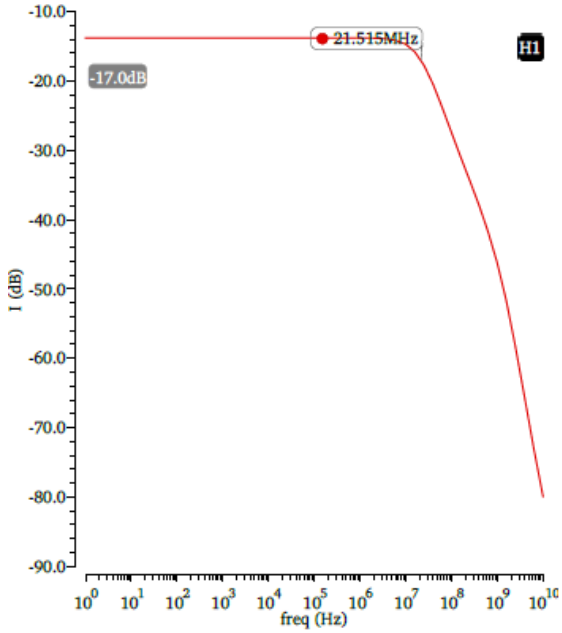


Figure 4.27 Variation of Iz/Ip with frequency for I_{bias_2} = 200µA

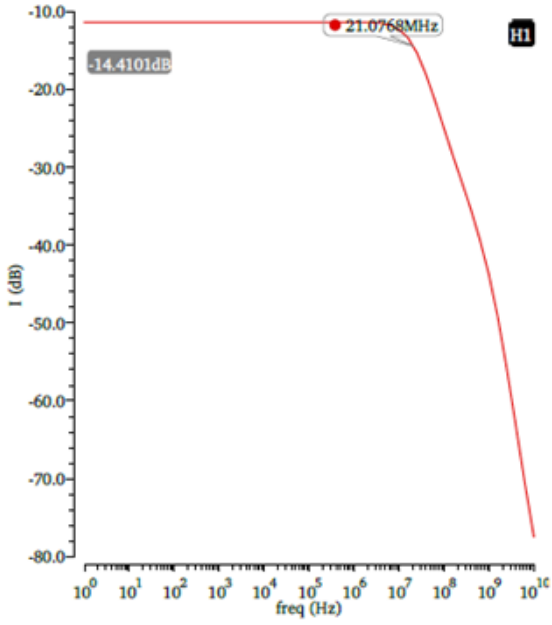


Figure 4.28 Iz/In versus frequency at constant bias current of 200µA

The Figure 4.29 shows the plot between the transconductance of the PCCDTACS over a frequency range of 1 to 10 GHz for constant I_{bias_2} of 200µA. The -3dB bandwidth of the PCCDTACS is found to be 208.93 MHz.

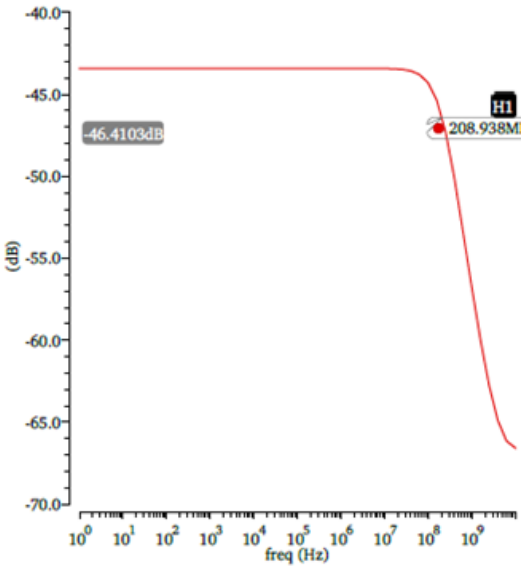


Figure 4.29 Frequency response of PCCDTACS at $Ibias_2$ = 200µA

The -3dB bandwidth of the PCCDTACS can be observed from the Figures 4.25, 4.26, 4.27, 4.28 and 4.29. The different values of bandwidth are 20.51 MHz, 22.02 MHz, 21.51 MHz, 21.07 MHz and 208.93 MHz. The bandwidth of the PCCDTACS is the minimum all the values of bandwidths, mentioned i.e. 20.51 MHz.

Figure 4.30 shows the range of transconductance for different values of bias current ($Ibias_2$). The bias current is varied from 1µA to 200µA with selected values of 1 µA, 2 µA, 3 µA, 4 µA, 5 µA, 10 µA, 20 µA, 30 µA, 40 µA, 50 µA, 60 µA, 70 µA, 80 µA, 90 µA, 100 µA, 150 µA and 200 µA. From the Figure the maximum value of transconductance of the PCCDTACS is found out to be 6.75mS for 200µA of bias current.

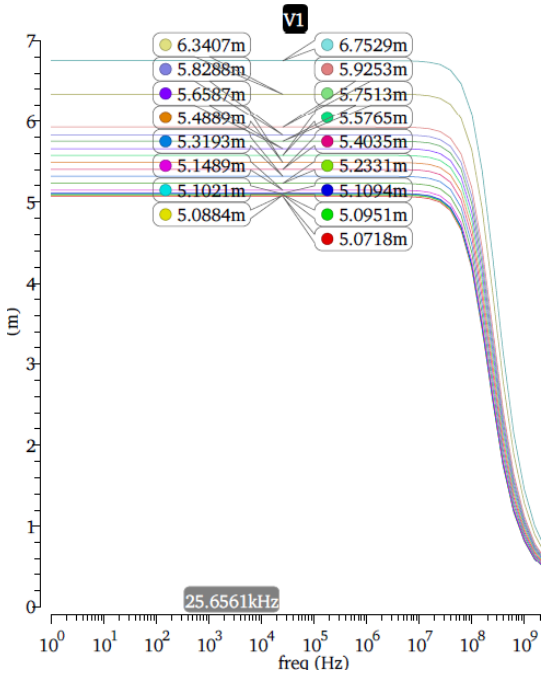


Figure 4.30 Transconductance of PCCDTACS

The transient analysis of the circuit is performed by applying two square input current pulses at the nodes ‘p’ and ‘n’. The currents Ip and In are chosen as 40µA and 20µA peak-to-peak, respectively with time period of 1µs and the pulse width of 0.5µS.

Figure 4.31 shows the transient response of the proposed CDTACS circuit. The transient analysis concludes that the two output currents are out-of-phase with each other and amplified. The peak-to-peak magnitude of the output currents Ix+ and Ix- are found out to be 500mA each.

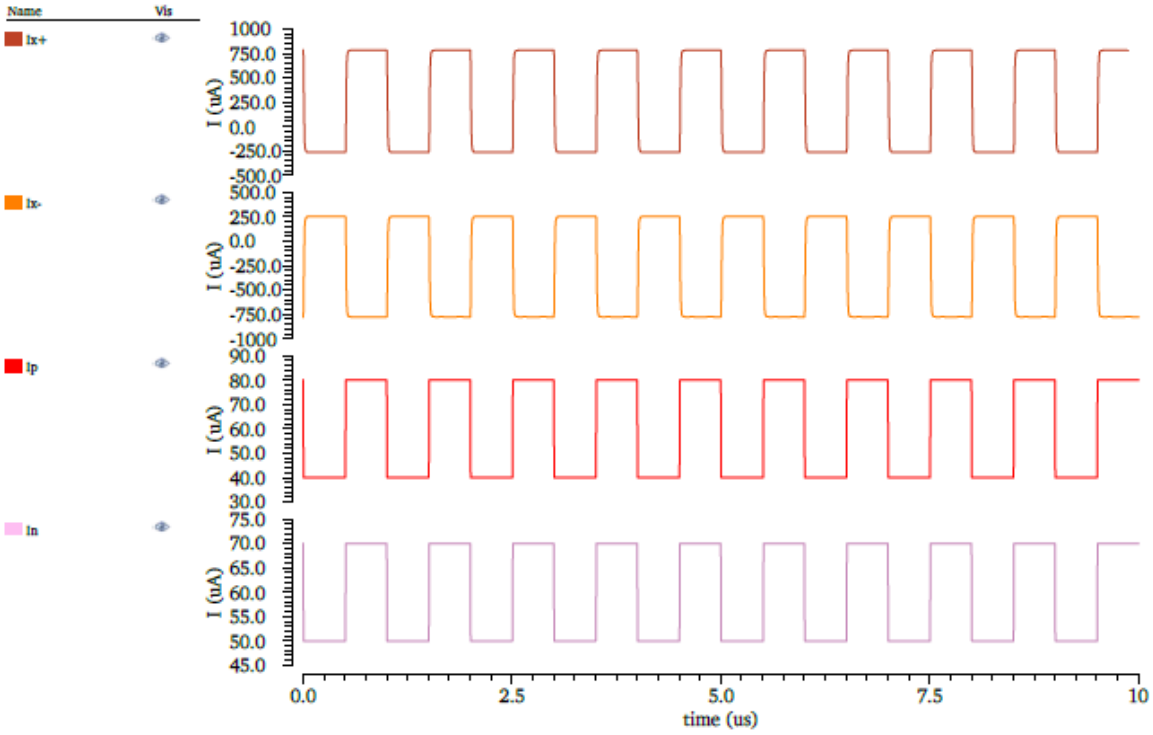


Figure 4.31 Transient response of PCCDTACS

Table 4.11 shows the comparison between proposed CCDTACS and proposed PCCDTACS on the basis of transconductance and dynamic power. From the table, it is observed that the dynamic power of PCCDTACS remains in close proximity to the dynamic power of CCDTACS but the transconductance (gm) is increased by 1.6 times.

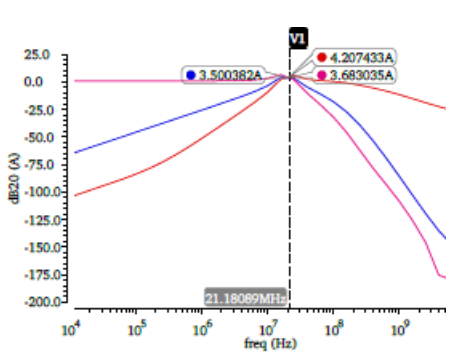
Thus, the proposed PCCDTACS offers better transconductance than the CCDTACS.

Table 4.11 Comparison between proposed CCDTACS and proposed PCCDTACS

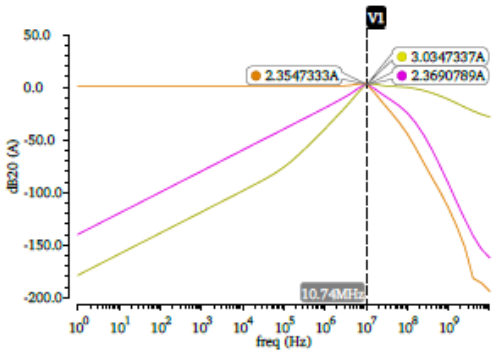
Ibias (µA)	Proposed CCDTACS		Proposed PCCDTACS	
	Transconductance (mS)	Dynamic Power (mW)	Transconductance (mS)	Dynamic Power (mW)
1	3.65	2.27	5.07	2.572
2	3.66	2.281	5.08	2.576
3	3.65	2.285	5.09	2.581
4	3.65	2.289	5.1	2.585
5	3.65	2.29	5.109	2.589
10	3.65	2.31	5.14	2.61
20	3.65	2.35	5.23	2.65
30	3.65	2.39	5.31	2.69
40	3.65	2.43	5.4	2.74
50	3.65	2.47	5.48	2.78
60	3.65	2.51	5.57	2.82
70	3.65	2.55	5.65	2.87
80	3.65	2.59	5.75	2.91
90	3.65	2.63	5.82	2.95
100	4.19	2.67	5.92	3.0
150	4.47	2.88	6.37	3.22
200	4.73	3.0	6.75	3.44

4.4.1 Simulation results of KHN Filter using proposed PCCDTACS

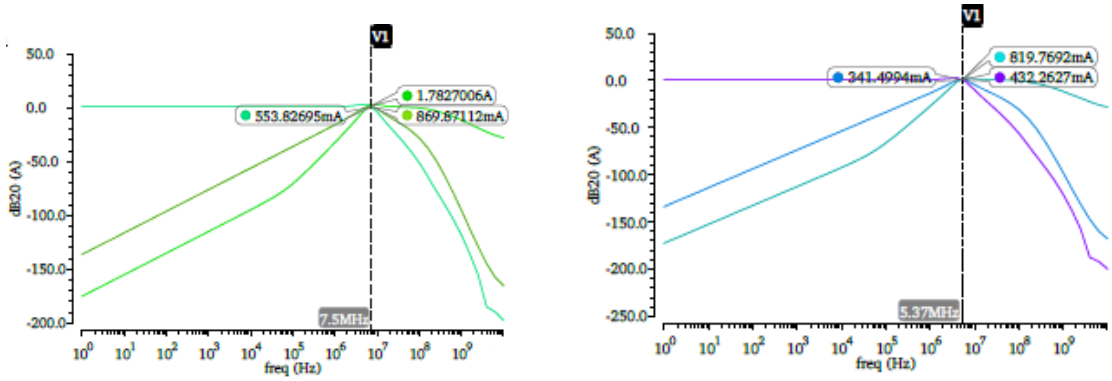
The KHN Filter has been simulated using four different values of capacitances selected as 50pF, 100pF, 150pF and 200pF with a low valued resistance of 1Ω. The values of transconductances of CDTACS are chosen as $gm_{PCCDTACS1} = gm_{PCCDTACS2} = 6.75$ mS by keeping the bias current at 200µA. The frequencies of KHN filter for different values of capacitances are shown in Figure 4.32 (a), (b), (c) and (d).



(a) C1=C2= 50pF



(b) C1=C2= 100pF



(c) C1=C2= 150pF (d) C1=C2= 200pF

Figure 4.32 Frequency response of KHN Filter for R=1ohm

Table 4.12 Center Frequency with different values of capacitances

S. No.	Capacitance (pF)	Theoretical value of center frequency (fo) (MHz)	Actual value of center frequency (fo) (MHz)
1.	50	20.7	21.48
2.	100	10.13	10.74
3.	150	7.16	7.5
4.	200	5.21	5.37

From Figures 4.32 (a), (b), (c) and (d), the obtained center frequencies are listed in Table 4.12 which compares the actual value of center frequency to the theoretical value for different values of the capacitances. The dynamic power of the proposed KHN filter based on PCCDTACS is 6mW which is equal to that of proposed CCDTACS (6mW) but the corner frequency of the KHN filter using proposed PCCDTACS is 1.4 times for C1 = C2 = 50pF than that of proposed CCDTACS.

4.5 COMPARISON

In this section, a comparative study of PCCDTACS with those mentioned in literature is discussed. Table 4.13 shows the comparison on the basis of performance parameters such as transconductance, dynamic power, bandwidth at the bias current of 200µA etc.

Table 4.13 Comparison between proposed PCCDTACS and reported CDTA circuits

Parameters	**Conventional CDTA [7]**	**Low Voltage CDTA [9]**	**A CMOS CDTA [19]**	**TBCDTA [16]**	**CDTA with gm boosting technique [18]**	**Proposed PCCDTACS**
Supply Voltage	±2.5	±0.75	±1.5	±2	±2	±0.9
Bias current (µA)	85	54	100	85	85	30
Maximum Transconductance at bias current of 200µA	1.08mS	210µS	833 µS	7.88mS	3.85mS	6.75mS
Dynamic power (mW)	2.7	0.37	4.96	8.75	4.85	3.4
Bandwidth at 200µA bias current	110	-	-	26	221	208.93
Center frequency of KHN filter (MHz)	1.48	-	1.08 with C1=C2 =0.1pF	24.98 with C1=C2 =100pF	8 with C1=C2 =100pF	20.7 with C1=C2 =50pF
Dynamic power of KHN filter (mW)	21.48	-	-	19.49	24.14	6

From the Table 4.13, it can be seen that the proposed PCCDTACS offers a high value of transconductance with lesser power dissipation as compared to the other CDTA structures available in literature. Although, the CDTA structure presented in [17] has larger transconductance than the proposed PCCDTACS but with higher dynamic power. The circuit reported in [9] has low dynamic power but offers a very low transconductance. Also, it can be concluded that the KHN filter using proposed PCCDTACS offers a center frequency (fo) of 20.7MHz which is 14 times more than that of the conventional CDTA.

CHAPTER 5
CONCLUDING REMARKS AND FUTURE SCOPE

5.1 CONCLUSION

The research work in the thesis presents four transconductance boosted circuits namely CDTACS, PCDTACS, CCDTACS and PCCDTACS. All the proposed circuits offers high transconductance because of the use of a common source (CS) amplifier as the main component in the OTA unit. The dynamic power was kept in close range to that of conventional CDTA. The KHN filters based on all the proposed circuits are also presented. The proposed circuits are simulated in Cadence Virtuoso Analog Design Environment using BSIM3V3 180 nm CMOS technology. Based on the comparison with the CDTA circuits available in literature, it is concluded that the proposed PCCDTACS circuit has higher transconductance and acceptable dynamic power. A higher value of the center frequency, approximately 14 times, than that of the conventional CDTA is achieved by the KHN filter using PCCDTACS circuit.

5.2 FUTURE SCOPE

The research work in the thesis concludes that PCCDTACS circuit can be used as an analog basic building block in the designing of various analog circuits such as filters, oscillators, multivibrators etc. The future work of research will include improvement of linearity, reduction in power supply and power consumption because the low voltage/low-power circuits are used as an integral part of the design for any modern electronic device.

REFERENCES

[1] Fidler JK, Deliyannis T and Sun Y. *Continuous-time active filter design*. CRC press, 1998.

[2] Huijsing H. and De Korte J (1977). Monolithic nullor – a universal active network element. *IEEE Journal of Solid State Circuits*, 12, 59-64.

[3] Wilson B (1989). Universal conveyor instrumentation amplifier. *Electronics Letters*, 25(7), 470-471.

[4] Toumazou C and Lidgey FJ (1989). Novel current mode instrumentation amplifier. *Electronics Letters*, 25(3), 228-230.

[5] Liu SI, Tsao HW and Wu J (1991). CCII-based continuous time filters with reduced gain-bandwidth sensitivity. *IEE proceedings of circuits, devices and systems*, 138(2), 210-216.

[6] Acar C, Ozoguz S (1999). A new versatile building block: current differencing buffered amplifier suitable for analog signal processing filters. *Microelectronics Journal*, 30(2), 157–160.

[7] Biolek D (2003). CDTA- building block for current-mode analog signal processing, *In proceedings of the European conference on circuit theory and design*, [Czech Republic: 2003], pp. 397-400.

[8] Uygur A and Kuntman H (2006). Low-voltage current differencing transconductance amplifier in a novel all pass configuration, *IEEE electrotechnical conference* [Malaga, Spain: 2006], pp. 23-26.

[9] Somdunyakanok M, Siripruchyanun M and Prommee P (2009). CMOS multiple-output CDTA and its applications, *In proceedings of the 1st international conference on technical education* [1st: Bangkok, Thailand: 2009], pp. 184-187.

[10] M. Maktoomi M, Siddiqi M and Pyari MP (2012). FVF based CDTA and its application, *2012 International conference on communication, information, and computing technology (ICCICT)*, [Mumbai, India: 2012], pp. 1-4.

[11] Liu SI, Tsao HW and Wu J (1991). CCII-based continuous time filters with reduced gain-bandwidth sensitivity. *IEE proceedings of circuits, devices and systems*, 138(2), 210-216.

[12] Biolek D, Keskin AU and Biolkova V (2010). Grounded capacitor current mode single - resistance controlled oscillator using single modified current differencing transconductance amplifier. *IET circuits, devices and systems*, 4(6), 496-502.

[13] Alaybeyoglu, E. and Kunman, H. (2013). A new CMOS ZC-CDTA realization and its filter applications. *Journal of electrical engineering and computer sciences*, 24(3), 746-761. (in *Turkish*)

[14] Malcher A (2012). Modified current differencing transconductance amplifier new versatile active element. *Bulletin of the Polish Academy of Sciences, Technical Sciences*, 60(4), 739-750.

[15] Jin J (2016). Multifunction current differencing cascaded transconductance amplifier (MCDTA) and its application to current mode multiphase sinusoidal oscillator. *Wireless personal communications*, 86(2), 367-383.

[16] Rai SK and Gupta M (2015). A transconductance boosted CMOS current differencing transconductance amplifier (TBCDTA) and its application. *Analog Integrated Circuits Signal Processing*, 84(1), 75-88.

[17] Rai SK, Gupta SK (2016). Performance enhancement of current differencing transconductance amplifier (CDTA) by using a new approach of gm boosting and its application. *Optik-International Journal for Light and Electron Optics,* 127(15), 6103–6114.

[18] Rai SK and Gupta M (2016). Current differencing transconductance amplifier (CDTA) with enhanced performance and its application. *Analog Integrated Circuits Signal Processing,* 86(2), 307–319.

[19] Kacar F and Kuntman H (2009). A New CMOS Current Differencing Transconductance Amplifier (Cdta) and Its Biquad Filter Application, *IEEE EUROCON* [St.-Petersburg, Russia: 2009], pp. 189-196.

[20] Xu J *et al.* (2014). Low-voltage high-linearity wideband current differencing transconductance amplifier and its application on current-mode active filter. *Radioengineering*, 23(1), 512-522.

[21] Rai SK and Gupta M (2016). Current differencing transconductance amplifier (CDTA) with high transconductance and its application in filter and oscillator. *Optik-International Journal for Light and Electron Optics,* 127(6), 3388–3396.

[22] Gautam S, Jain N and Sharma AK (2013). Implementation of monostable multivibrator using low voltage current differencing transconductance amplifier. *International journal of innovations in engineering and technology*, 2(3), 289-296.

[23] Pandey N, Sayal A and Pandey R .CDTA based semi Gaussian shapers for detector readout front ends, *International conference on circuits, power and computing technologies (ICCPCT)* [Nagercoil, India: 2013], pp. 703-708.

[24] Silapan P and Siripruchyanun M (2011). Fully and electronically controllable current mode schmitt triggers employing only single MO-CCCDTA and their applications. *Analog integrated circuits and signal processing*, 68(1), 111-128.

[25] Soni GS and Ansari MS (2014). Current mode electronically tunable Schmitt trigger using single 65 nm ± 0.75 V CMOS CDTA. *IEEE international conference on signal propagation and computer technology (ICSPCT),* [Ajmer, India: 2014], pp. 137-141.

[26] Biolek D and Biolkova V (2006). Current-mode CDTA-based comparators, *In the 13th international conference on electronic devices and systems* [13: Brno University of Technology, Czech Republic: 2006], pp. 6-10.

[27] Jaikla W and Siripruchyanun S (2007). A novel current mode multiplier/divider employing only single dual-output current controlled CDTA. *International symposium on communications and information technologies,* [Sydney, NSW, Australia: 2007], pp. 106-109.

[28] M. Dehran, I.P. Singh and K. Singh K, "A current mode multiplier employing single current differencing transconductance amplifier".

[29] Petrovic PB (2015). A new high precision power detector of complex voltage signal. *Measurement science review*, 15(4), 184-195.

[30] Biolek D, Gubek T and Biolkova V (2004). Optimization of CDTA-based circuits simulating ladder structures. *WSEAS transactions on mathematics*, 3(4), 783-788.

[31] Biolek D and Biolkova V (2003). Universal biquads using CDTA elements for cascade filter design. *Circuits, Systems, Communications and Computers*, [Czech Republic: 2003], pp. 232-236.

[32] Lahiri A (2009). Novel voltage/current mode quadrature oscillator using current differencing transconductance amplifier. *Analog integrated circuits and signal processing*, 61(2), 199-203.

[33] Khateb F, Vavra J and Biolek D (2010). A novel current mode full wave rectifier based on one CDTA and two diodes. *Radioengineering*, 19(3), 437-445.

[34] Koton J *et al.* (2011). Precision full wave current mode rectifier using current differencing transconductance amplifier, *3rd international conference on communication software and networks (ICCSN)*, [Xi'an, China: 2011] pp. 460-463.

[35] Lahiri A and Chowdhury A (2009). Current mode square rooting circuit using CCCDTA. *International journal of recent trends in engineering*. 1(3), 280-282.

[36] Marungreang N et al. (2009). Electronically tunable phase shifter using CDTAs. *Asia pacific signal and information processing association*, [Sapporo, Japan: 2009], pp. 311-314.

[37] Shah NA, Quadri M and Iqbal SZ. CDTA based universal transadmittance filter. *Analog integrated circuits and signal processing*, 52(1-2), 2007.

[38] Uygur A and H. Kuntman H (2007). Seventh-order elliptic video filter with 0.1 dB pass band ripple employing CMOS CDTAs. *International journal of electronics and communications*, 61(5), 320-328.

[39] Maktoomi M *et al.* (2012). CDTA based logarithmic amplifier. *2012 IEEE international conference on signal processing, computing and control (ISPCC)*, [Waknaghat Solan, India: 2012], pp. 1-4.

[40] Biolek D, Biolkova V and Kolka Z (2008). Single CDTA (Current differencing transconductance amplifier) current mode biquad revisited. *WSEAS transactions on electronics*, 5(6), 250-256.

[41] Li Y. *Three current mode Wein Bridge oscillators using single modified current controlled current differencing transconductance amplifier*. Mechatronics and Automatic Control Systems. pp 693-700, 2014.

[42] Tanaphatsiri C, Jaikla W and Siripruchyanun M (2008). A current mode wheatstone bridge employing only single DO-CDTA. *IEEE Asia pacific conference (APCCAS)*, [Macao, China: 2008], pp. 1494-1497.