Design and Verification of Dual Port RAM using System Verilog Methodology

A Thesis submitted in partial fulfillment of the requirement for the Award of the Degree of

MASTER OF ENGINEERING TECHNOLOGY

in VLSI Design

Submitted By

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DECLARATION

I, **Nikhil Singh** hereby declare that the work presented in this thesis entitled "**Design and Verification of Dual Port RAM using System Verilog Methodology**" in partial fulfilment of the requirement for the award of degree of **Master of Technology (VLSI Design)** submitted at **Electronics and Communication Engineering Department** , Thapar Institute of Engineering & Technology (Deemed to be University), Patiala is an authentic record of work carried out under supervision of **Dr. Sanjay Kumar (Associate Professor, ECED, Thapar Institute of Engineering & Technology, Patiala)** from June 2023 to July 2024. The matter presented in this has not been submitted either in part or full to any other university or institute for the award of any other degree.

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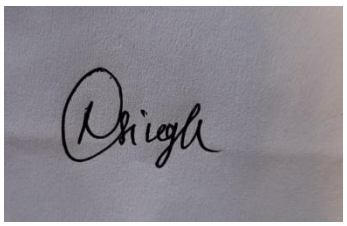

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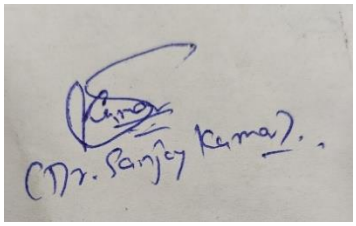

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This is to certify that Nikhil Singh worked as an Interim Engineering Intern at Qualcomm from Aug 21st 2024 to April 30th 2025.

Nikhil's performance, behavior, and conduct remains good during the internship.

We wish him all the best for his future endeavors.

April 29th 2025

Date

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ABSTRACT

This thesis presents the **design and verification of a Dual-Port RAM (DPRAM)** using **System Verilog**, an industry-standard language for hardware design and verification. The primary objective is to ensure the **functional correctness** of the DPRAM design under diverse operational scenarios through an efficient and reusable **testbench environment**.

The research begins with a detailed analysis of DPRAM architecture, covering memory organization, control logic, and data integrity mechanisms. The RTL is developed in **Verilog HDL**, maintaining modularity and adherence to design standards.

To verify the functionality of the design, a **System Verilog-based testbench** is implemented. Simulation results demonstrate successful functional verification, with high coverage metrics reflecting design stability and correctness.

Waveform analysis provides insights into protocol compliance and performance evaluation. This work underscores the effectiveness of **System Verilog-based verification environments** in memory IP validation and proposes optimization techniques to enhance the verification methodology for Dual-Port RAM.

Keywords: Dual-Port RAM, System Verilog, Functional Coverage, Memory Verification, Assertion-Based Verification, DPRAM Testbench

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CHAPTER 1

INTRODUCTION

1.1 Introduction

As semiconductor technology continues to advance toward smaller feature sizes, the complexity of integrated circuits increases, bringing with it a greater likelihood of manufacturing defects. Among various components, memory arrays have become a critical benchmark for evaluating semiconductor manufacturing and process technology. The growing demand for embedded memories is pushing their footprint to nearly 90% of the total die area in modern chips. However, this increased memory density comes at the cost of higher vulnerability to fabrication faults. Compared to logic circuits, memory structures exhibit a greater probability of defects, largely due to the compact arrangement of transistors within memory cells.

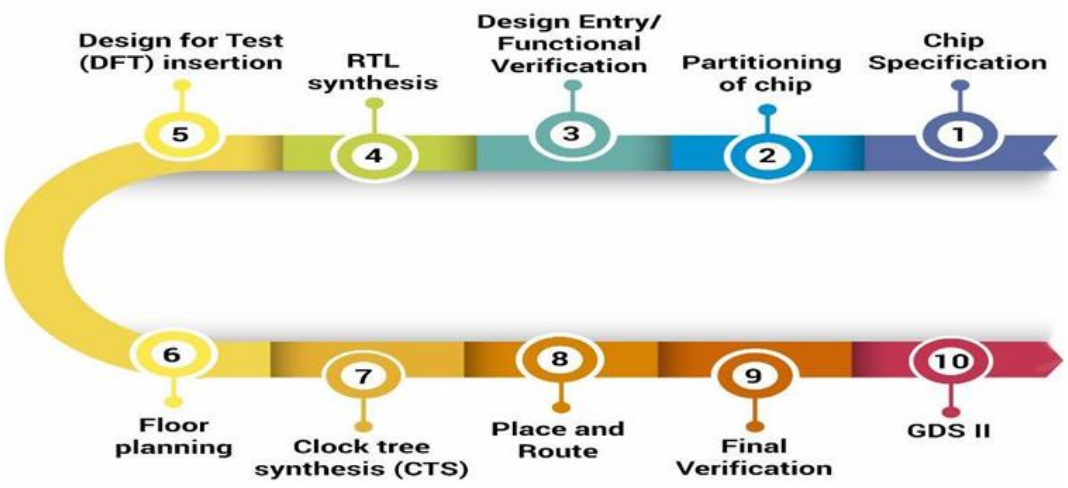

Figure 1.1: Design Cycle of an IC

In modern digital design workflows, verification has become one of the most time-consuming and resource-intensive stages, accounting for over 70% of the total development cycle. A significant difference exists between the languages used by RTL design engineers and those preferred by verification engineers, largely due to differing synthesis and simulation requirements. While RTL designers typically rely on hardware description languages such as Verilog and VHDL for their synthesis capabilities, verification engineers often use simulation-friendly languages like Sugar OVA, VERA, and Specman. To bridge this gap,

System Verilog (SV) was introduced as an extension to the IEEE 1364 Verilog standard. It combines design and verification features into a unified language, offering object-oriented programming constructs, assertions, and coverage tools to strengthen the verification process.

To support reuse and automation in verification, structured methodologies have been adopted widely across the semiconductor industry. These approaches help in building layered testbenches where different verification components operate independently. Though this layered structure may initially increase development time, it significantly improves the maintainability, scalability, and overall efficiency of the verification process.

In this project, a standard industrial Dual-Port RAM (DPRAM) is selected as the Design Under Test (DUT). The design is verified using a SystemVerilog-based testbench, where individual transactors are created for each of the two ports. The testbench is modular in nature and includes a monitor, scoreboard, driver and reference model which has been integrated in System Verilog testbench. Associative arrays are used within the scoreboard to model memory behaviour effectively. Constrained-random stimulus is generated independently for each port, allowing diverse functional scenarios to be exercised. The simulation continues until all pre-defined coverage points are met, ensuring thorough verification of the memory module under a wide range of operating conditions.

1.2 Research Goals

The primary objective of this project is to design and implement a structured System Verilog-based verification environment for a Dual-Port RAM (DPRAM). The project involves both the development of the DPRAM RTL design and the creation of a modular and reusable System Verilog testbench to thoroughly verify its functional correctness.

The DPRAM supports concurrent read and write operations through two separate ports, requiring verification of multiple parallel access patterns. This makes it essential to ensure proper memory access synchronization, data integrity, and arbitration logic between ports.

The testbench is developed using object-oriented SystemVerilog constructs, where constrained-random stimulus is generated independently for each port, allowing diverse functional scenarios to be exercised effectively.

Assertions and functional coverage models are integrated within the environment to verify critical behaviors and track simulation completeness. Waveform analysis and debugging are performed using Xcelium and SimVision, which provide a lightweight and accessible platform for observing signal-level activities during simulation.

The simulation process is executed iteratively until all pre-defined coverage goals are satisfied. This structured approach ensures exhaustive verification of the memory module across a range of operating conditions, contributing to the development of a reliable, scalable, and reusable verification solution aligned with industry standards.

1.3 Overview of Memory Architectures Conclusion

Memory is a crucial component of any digital system, serving as a storage medium for data and instructions required during the execution of operations. As digital systems become more complex and demand higher performance, memory architectures have evolved to support faster data access, increased bandwidth, better scalability, and power efficiency. This chapter provides an overview of memory architectures with a specific focus on Random Access Memory (RAM), leading into the core topic of this thesis—Dual Port RAM.

Digital memory can broadly be classified into primary memory, secondary memory, cache memory, and register memory. Primary memory includes both volatile (RAM) and non-volatile (ROM) types and is directly accessible by the CPU. Secondary memory refers to long-term storage devices like hard drives and solid-state drives, which are not directly accessed by the processor during computations. Cache memory acts as a high-speed intermediary between the CPU and main memory, significantly reducing access latency. Register memory, located inside the CPU, is the fastest and most limited in capacity.

Among different types of RAM, two major categories are Static RAM (SRAM) and Dynamic RAM (DRAM). SRAM uses flip-flops to store data, offering fast access times and better performance, but it is more expensive and consumes more area. DRAM, on the other hand, stores data using capacitors and needs periodic refreshing. While slower than SRAM, DRAM offers higher density and is more cost-effective, making it the preferred choice for main system memory.

Memory can also be categorized based on the number of access ports. Single-port RAM allows either a read or a write operation at any given time, making it simpler in design but less suitable for systems requiring high throughput. In contrast, Dual Port RAM enables simultaneous access from two ports, allowing concurrent read and write operations. This architecture is especially valuable in high-performance applications such as real-time image processing, networking, and systems with multiple data producers or consumers.

The architecture of Dual Port RAM typically includes independent address, data, and control signals for each port. Depending on the design, the ports can operate synchronously or asynchronously, and mechanisms are implemented to handle address conflicts when both ports access the same location. This parallel access capability makes dual-port memories ideal for use in shared-memory systems, inter-processor communication, and pipelined architectures.

In modern digital design, memory is organized hierarchically to balance speed, cost, and capacity. At the top are CPU registers, followed by multiple levels of cache, then main memory (RAM), and finally secondary storage. Each level introduces a trade-off: faster memories are more expensive and offer lower storage capacity, while slower ones provide larger storage at reduced cost

Feature	Single-Port RAM	Dual-Port RAM	General RAM (e.g., DRAM, SRAM)
Access Ports	1 port (shared for read/write)	2 ports (can be independent or symmetric)	Typically 1 port; varies by architecture
Simultaneous Access	No (read or write, not both at once)	Yes (read/write or read/read simultaneously)	Depends on type (e.g., DRAM is single-access)
Clock Domains	Single	Can be single or dual	Usually single
Complexity	Simple to design and simulate	More complex (conflict resolution, timing)	Varies (DRAM needs refresh logic, SRAM is simpler)
Area & Power	Low	Higher (due to duplicated logic and routing)	DRAM: low area, high density; SRAM: higher area, faster
Use Cases	Register files, small buffers	FIFOs, dual-access buffers, inter-processor communication	Main memory (DRAM), cache (SRAM), embedded memory
Volatility	Volatile	Volatile	Volatile (DRAM, SRAM); non-volatile types exist (e.g., MRAM)

Feature	Single-Port RAM	Dual-Port RAM	General RAM (e.g., DRAM, SRAM)
Technology	Often SRAM-based	Often SRAM-based	DRAM (main memory), SRAM (cache)

Table 1.3: Comparison of RAM Types

Recent advancements in memory architecture focus on achieving higher performance while minimizing power consumption. Technologies like low-power SRAM for mobile devices, 3D-stacked memory for high-bandwidth access, and hybrid systems combining volatile and non-volatile memories are becoming increasingly popular. Dual Port RAM is frequently implemented in FPGAs and ASICs for real-time, on-chip data sharing due to its efficiency and speed.

In summary, understanding memory architecture is essential for designing optimized digital systems. Dual Port RAM, with its ability to perform simultaneous operations, addresses many of the performance bottlenecks faced by single-port memory systems. This chapter lays the groundwork for the subsequent discussion on the design and verification of a Dual Port RAM using System Verilog, which forms the core of this thesis.

1.4 Motivation for Using Dual Port RAM

In modern digital systems, achieving high performance and efficient data handling is a critical design objective. Traditional single-port RAM architectures, which support only one memory access at a time, often lead to data access conflicts and reduced throughput, particularly in systems requiring concurrent operations. Dual Port RAM addresses these limitations by allowing two independent memory accesses simultaneously—enabling read/write, read/read, or write/write operations depending on the implementation. This capability makes Dual Port RAM highly suitable for applications such as real-time image processing, communication systems, and multi-core processor architectures, where parallel data access is essential.

Moreover, Dual Port RAM proves beneficial in environments involving multiple clock domains, facilitating asynchronous data transfer between different modules without compromising performance or reliability. It is also widely used in verification environments, where it enables the design under test (DUT) and the testbench to interact with the memory independently, improving simulation control and flexibility. These practical advantages

highlight the growing importance of Dual Port RAM in both design and verification workflows. This thesis focuses on the implementation and verification of a Dual Port RAM using System Verilog, motivated by its relevance in modern high-performance digital systems.

CHAPTER 2

LITERATURE REVIEW

2.1 Previous Work and Research Gaps

1) **Existing Research on Memory Architectures**
   - Numerous studies have focused on designing RAM structures, especially single-port and dual-port RAM.
   - Most implementations use traditional HDLs like Verilog or VHDL.
   - Research efforts primarily emphasize optimizing speed, area, and power consumption.
2) **Design Approaches in Prior Work**
   - Dual Port RAMs are often implemented and validated on FPGA platforms.
   - The focus is largely on functional correctness rather than on thorough verification.
   - Designs are usually validated using simple testbenches without structured verification techniques.
3) **Lack of Modern Verification Techniques**
   - Few projects incorporate System Verilog-based verification, which is standard in industry today.
   - Commonly missing elements in previous work include:
     - Constrained-random stimulus generation.
     - Functional coverage metrics for completeness.
4) **Gaps in Reusability and Scalability**
   - Testbenches used in earlier studies are often tightly coupled to specific designs.
   - Lack of modularity makes them unsuitable for integration into larger SoC verification environments.

2.2 Importance of Verification in VLSI Design

Verification plays a critical role in the VLSI design flow, ensuring that a digital system behaves as intended before it is fabrication. As VLSI designs grow increasingly complex, the likelihood of functional bugs and design errors rises significantly, making verification one of the most time-consuming yet essential phases in the development process. A design that functions correctly in simulation but fails in silicon can lead to costly re-spins and significant time-to-market delays. Therefore, early and thorough verification helps detect and correct issues at the functional level, reducing both financial risk and development time.

Modern verification involves various techniques such as simulation, formal verification, assertion-based verification, and coverage-driven methodologies. Among these, simulation remains the most widely used method, often employing languages like System Verilog for creating testbenches and stimulus environments. SystemVerilog provides powerful constructs for constrained-random verification, functional coverage, and assertions, making it a preferred choice in industry-standard verification flows. It present, verification bridges the gap between design specification and physical realization, ensuring that the implemented logic adheres strictly to the intended functionality. This makes verification not just a supporting activity but a cornerstone of reliable and successful VLSI design.

2.3 Problem Statement

As digital systems become increasingly complex and performance-driven, the demand for faster and more efficient memory architectures continues to grow.

Traditional single-port memory structures often limit system throughput due to their inability to handle concurrent data access operations. In applications that require parallel read and write functionality, such as communication systems, signal processing, and multi-core processors, these limitations become a significant bottleneck. Dual Port RAM offers a viable solution by enabling simultaneous access through two independent ports, thereby enhancing system performance. However, designing and verifying such memory modules requires a robust methodology that ensures correctness, efficiency, and reusability. Despite its importance, many academic and industrial projects overlook comprehensive verification, which leads to functional bugs that surface late in the design cycle. Therefore, there is a need to design a Dual Port RAM with a strong focus on functional verification using industry-standard techniques and tools. This project aims to address this gap by implementing a Dual Port RAM architecture and thoroughly verifying it using System Verilog-based methodologies, ensuring it meets functional correctness and performance expectations.

2.4 Verification Design Flow

As Verification is not a one-step task but a structured process comprising multiple stages, each of which contributes to ensuring the correctness of the digital design before fabrication. The verification design flow followed in this project is outlined in Figure 2.2 and explained below:

1) Specification

This is the starting point of the verification process. At this stage, the design functionality, features, and constraints are clearly defined. The verification engineer studies the specifications to understand what the design is intended to do. This helps identify what needs to be tested and what the expected behavior is under various input conditions.

2) Test Plan

Once the specification is understood, the next step is to develop a **test plan**. The test plan serves as a blueprint for the entire verification effort. It includes:

- List of test scenarios to be verified
- Interface and signal definitions
- Coverage goals (functional and code)
- Pass/fail criteria

A well-written test plan ensures that the verification process is systematic, traceable, and aligned with the design requirements.

3) Testbench Development

In this phase, the verification environment is coded using SystemVerilog. It includes modules like:

- **Driver**: Applies stimulus to the DUT.
- **Monitor**: Observes and captures signal activity.
- **Scoreboard**: Compares DUT output with expected output.
- **Generator**: Produces random or directed stimulus.
- **Reference Model**: Predicts expected output based on inputs.

These components are built around a **virtual interface** that connects the DUT to the testbench. Assertions and coverage models can also be implemented in this stage.

4) Regression

Once the testbench is complete and the initial tests pass, the project enters the **regression testing phase**. This involves running a large set of test cases (both directed and random) in batch mode to ensure the DUT behaves correctly across all scenarios. Bugs discovered during this phase are fixed, and tests are rerun until stability is achieved. Functional and code coverage are measured during regression to track verification completeness.

5) Design Under Test (DUT)

The **DUT**, or Design Under Test, is the actual RTL implementation of the hardware being verified. In this project, it refers to the **Dual Port RAM**. The DUT is integrated into the verification environment and stimulated using various inputs to verify its functional correctness.

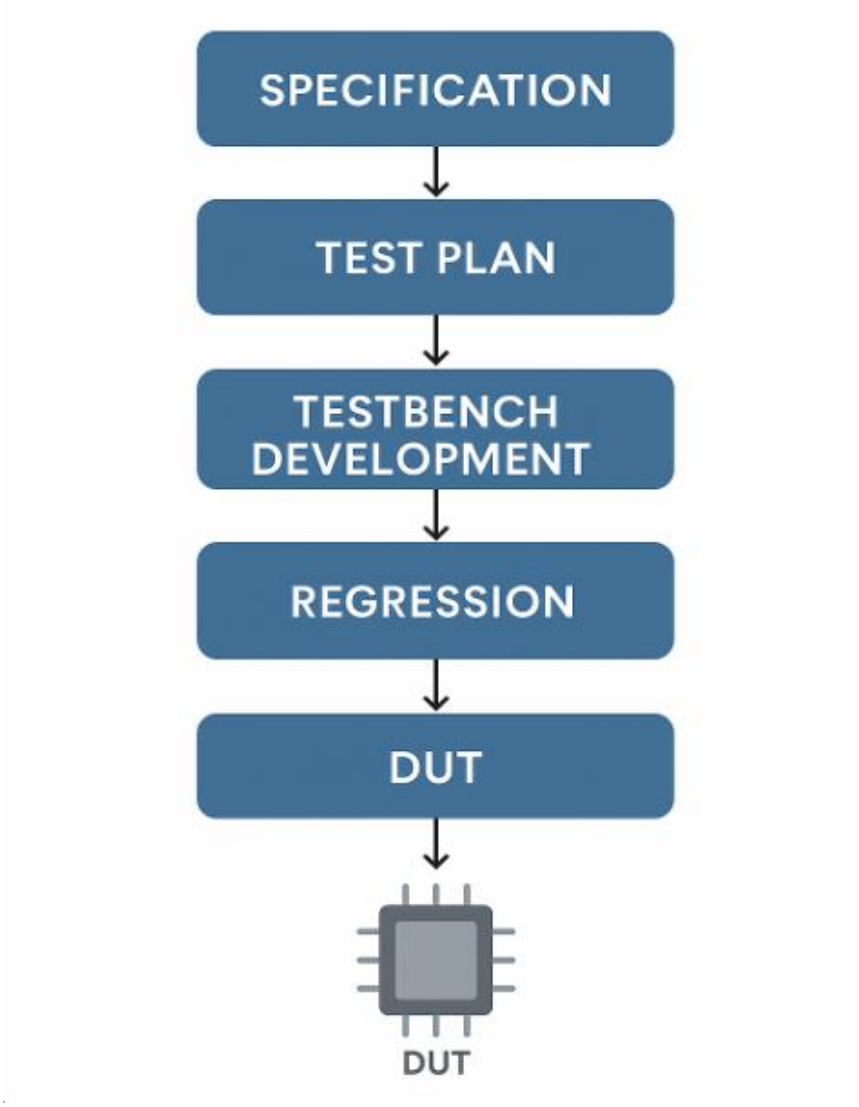

Figure 2.4: VLSI Verification Flow

2.5 Objectives of the Project

The primary objective of this project is to design and verify a Dual Port RAM using a structured System Verilog-based methodology. The project aims to develop a memory module capable of read and write operations parallelly through two independent ports, thereby enhancing data throughput and enabling parallel access. Another key objective is to ensure that the design is functionally correct, efficient for real-world applications such as digital signal processing, processor-memory interfacing, and communication systems. To

achieve this, a comprehensive verification environment will be developed using System Verilog constructs, incorporating features such as constrained-random stimulus generation, and functional coverage. This project also aims to demonstrate the practical application of modern verification techniques and best practices in ensuring design reliability. By fulfilling these objectives, this project contributes toward building a robust foundation in both memory design and functional verification, aligned with industry standards.

2.6 Scope of the Work

The scope of this project encompasses the design and verification of a Dual Port RAM module using System Verilog. The design part includes defining the memory architecture, specifying port configurations, implementing concurrent read/write operations, and ensuring compatibility. The verification scope involves creating a testbench using System Verilog, developing functional and directed test scenarios, and ensuring thorough coverage of all functional aspects of the memory. This project focuses on RTL-level modelling and simulation-based verification, adhering to standard digital design flows. It does not include post-silicon validation, power optimization, or physical layout implementation. However, the developed RTL and verification environment can be extended or integrated into larger VLSI systems and is scalable for further enhancements such as error correction or multi-port extensions.

CHAPTER 3

RAM ARCHITECTURES

3.1 Overview of Existing RAM Architectures

Random Access Memory (RAM) is a fundamental component of digital systems, providing temporary data storage that allows for fast read and write operations. Over the years, various RAM architectures have been developed to meet the evolving demands of speed, density, power efficiency, and parallelism. The two most commonly used types of RAM are **Static RAM (SRAM)** and **Dynamic RAM (DRAM)**, each with distinct characteristics and applications.

SRAM is built using bistable flip-flop circuits and retains data as long as power is supplied. It offers faster access times and is more reliable compared to DRAM. Due to its speed and stability, SRAM is primarily used in cache memory and high-speed registers. However, SRAM requires more transistors per bit, making it less dense and more expensive, which limits its use in large-scale memory arrays.

DRAM, in contrast, stores each bit of data in a capacitor-transistor pair and requires periodic refreshing to maintain its contents. Although slower than SRAM, DRAM offers higher storage density and lower cost per bit, making it suitable for main memory applications in computers and embedded systems. Innovations in DRAM architecture, such as Synchronous DRAM (SDRAM) and Double Data Rate (DDR) SDRAM, have significantly enhanced its performance and bandwidth capabilities.

Beyond the basic architectures, advanced RAM types have emerged to address specialized requirements. **Single-Port RAM** is the simplest form, allowing either read or write access at a given time through one port. **Dual Port RAM** enhances performance by enabling simultaneous access through two independent ports, making it ideal for systems requiring concurrent data operations. Some systems even employ **Multi-Port RAM** to support more than two accesses at once, although this comes at the cost of increased design complexity and area.In addition, modern FPGA and ASIC designs frequently incorporate on-chip RAM blocks such as **Block RAM (BRAM)** and **Distributed RAM**, optimized for specific applications. These memories are designed to integrate seamlessly within programmable logic environments and offer configuration flexibility to match system requirements.

Overall, the evolution of RAM architectures reflects the growing need for memory systems that can support higher speeds, parallelism, and energy efficiency. Understanding these existing architectures is crucial for selecting or designing memory modules tailored to specific application domains. The focus of this thesis is on Dual Port RAM, which strikes an effective balance between complexity and performance, and is particularly suitable for high-throughput and parallel-processing environments.

3.2 Single Port vs Dual Port RAM

Single Port and Dual Port RAM differ primarily in the number of access ports available and how data operations are handled. **Single Port RAM** allows either a read or a write operation to be performed at a given time through a single set of address, data, and control lines. This simplicity results in reduced area and power consumption, making it suitable for applications where memory access is infrequent or occurs in a sequential manner. However, in systems requiring high data throughput or simultaneous access by multiple components, single-port memory can become a bottleneck, as concurrent read and write operations are not possible.

Dual Port RAM, on the other hand, provides two independent access ports, each with its own set of address, data, and control signals. This architecture enables **read and write** operations, significantly improving memory access efficiency and overall system performance. Dual Port RAM is particularly beneficial in applications such as digital signal processing, image processing, communication buffers, and processor-memory interfaces where parallel access is essential. It also allows safe data exchange between modules operating in different clock domains when designed as asynchronous dual-port memory. While Dual Port RAM increases the complexity of design and consumes more area compared to Single Port RAM, its advantages in terms of speed and parallelism make it a preferred choice in high-performance systems.

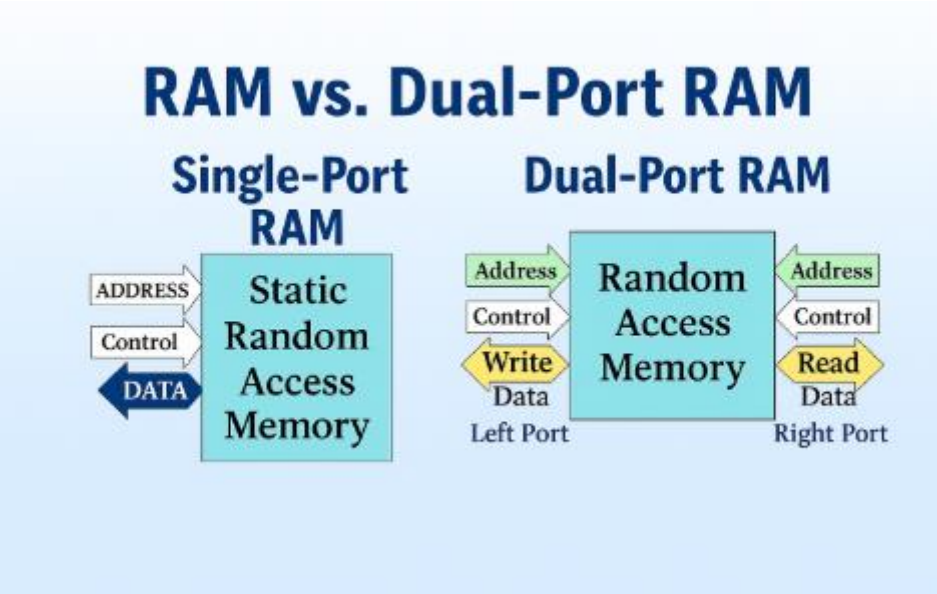

Figure 3.2: Single-Port Ram vs Dual-Port Ram

3.3 Memory Design Methodologies

Memory design methodologies refer to the systematic approaches used to create reliable, efficient, and synthesizable memory architectures within digital systems. These methodologies encompass both the functional design and the physical implementation of memory components. At the RTL (Register Transfer Level), memory design typically begins with the specification of key parameters such as word size, address width, number of ports, and access type (read/write behaviour). The design is modelled using hardware description languages like Verilog or System Verilog, enabling simulation and early-stage verification. Common techniques include behavioural modelling for high-level simulation.

Synchronous memory design, where operations are triggered by a clock signal, is preferred in modern VLSI due to its predictability and ease of timing analysis. Asynchronous designs, while offering greater flexibility, are more complex and susceptible to timing hazards. Memory modules may also be implemented using standard-cell based design or inferred from HDL code for synthesis into on-chip RAM blocks in FPGAs or ASICs.

In high-performance applications, designers often adopt pipelining and register buffering techniques to enhance throughput and minimize latency. Additionally, design reuse through parameterized modules and IP (Intellectual Property) cores is becoming increasingly popular, allowing for scalable and configurable memory blocks. Once the functional design is complete, the memory is verified through simulation and then synthesized, followed by place-and-route and physical verification stages for ASICs or mapped onto logic fabric in FPGAs. Effective memory design methodologies aim to achieve an optimal balance between

speed, area, and power while ensuring functional correctness and integration compatibility with the overall system.

3.4 Basics of System Verilog for Design & Verification

System Verilog is a powerful hardware description and verification language that extends the capabilities of traditional Verilog by introducing advanced features for both design and verification. It is standardized under IEEE 1800 and has become the industry-preferred language for modern digital system development due to its rich set of constructs that support abstraction, reusability, and scalability. For design purposes, System Verilog enhances Verilog by adding support for two-dimensional arrays, enumerated types, user-defined types (typedef), interfaces, and enhanced control structures such as foreach and unique case statements. These features help in writing more concise and maintainable RTL code while also improving readability and modularity.

On the verification side, System Verilog introduces an object-oriented programming model, allowing the creation of reusable and modular testbenches. It supports classes, inheritance, polymorphism, and encapsulation, enabling the development of scalable and reusable verification components. Additionally, System Verilog includes powerful verification constructs such as **constrained-random stimulus generation** and **functional coverage**. These features facilitate exhaustive and automated verification processes that improve confidence in design correctness.

The language also defines standardized verification methodologies such as UVM (Universal Verification Methodology), which promotes a structured and reusable environment for testbench creation. By combining RTL design capabilities with advanced verification features, System Verilog bridges the gap between design and verification, making it highly suitable for complex projects like Dual Port RAM, where functional correctness and verification efficiency are both critical.

Understanding the basic syntax and semantics of System Verilog is essential for successfully implementing and validating hardware modules in contemporary VLSI design flows.

CHAPTER 4

RTL DESIGN OF DUAL PORT RAM

4.1 Functional Requirements of DPRAM

A Dual Port RAM is expected to support independent access from two different ports at the same time. This means both ports should be able to operate without waiting on each other, and each should have its own set of control signals like read, write, address, and data lines. One of the key things is that the memory has to allow read and write operations to happen in parallel - especially when both ports are working on different memory addresses. But if both ports end up trying to access the same location, the system needs a way to handle that situation without causing errors, like giving one port priority or using internal checks. Usually, the RAM works in sync with a clock, so it's important that both ports respond properly on the clock edge. The design might use a single clock for both ports, or even different clocks for each, depending on whether it's synchronous or asynchronous.

The RAM also needs to be able to correctly handle when it should read data or write data, based on control signals. For a read, the right data should come out, and for a write, the data has to be stored in the correct location. Address decoding is another important part - every address coming in must go to the correct memory cell, without any overlap or errors. A good DPRAM design should be flexible, meaning you should be able to change things like memory depth or data width without starting the whole design from scratch. Another thing to make sure of is that no data should get corrupted, even when both ports are accessing the memory at the same time. Lastly, when the system is reset, the memory should either go to all zeroes or some default state, depending on how it's being used. Overall, these are the core features that make a dual port RAM design reliable and usable in real-world applications.

4.2 Design Specifications of Dual Port RAM

The design of Dual Port RAM requires careful specification of various parameters to ensure correct functionality, performance, and compatibility with digital systems. The following are the key design specifications considered for implementing the memory module in this project.

1. **Data Width**
    - Each memory location holds a fixed number of bits.
    - For this design, each word is **8 bits** wide (1 byte).
2. **Address Width**

- The number of address lines determines how many locations the RAM can access.
- Here, the address width is **5 bits**, allowing access to **16 different memory locations** ($2^5 = 32$).

3. **Memory Depth**
   - Total number of memory locations available.
   - With 5-bit address lines, the memory depth is **16 words**.
4. **Number of Ports**
   - This is a **Dual Port RAM**, so it has two independent ports for **read and write** operation
   - Each port has its own set of address, data, and control signals.
5. **Read/Write Control Signals**
   - Each port has a **read enable** and **write enable** signal to control memory operations.
6. **Clock Signal**
   - The memory is **synchronous**, operating on a clock edge.
   - Both ports can share the same clock or have separate clocks (if designed to support asynchronous mode).
7. **Reset Signal**
   - A **reset input** is used to bring the memory or control logic to a known state.
   - This ensures the memory starts cleanly after power-up or during reinitialization.
8. **Data Input and Output Buses**
   - Each port has its own **data input** and **data output** lines for independent operation.

4.3 Architecture of Dual Port RAM

The architecture of Dual Port RAM is designed to allow two independent ports—for read and write operation—to access the memory simultaneously. Each port is equipped with its own set of address lines, data input/output buses, read and write control signals, and sometimes even separate clock signals.

This separation enables both ports to perform read or write operations at the same time, either on different memory locations or, in some cases, the same location. Internally, the memory array is shared, but access is managed in such a way that data integrity is maintained, even during simultaneous operations. A control logic block is used to monitor and coordinate activities when both ports target the same address, typically using conflict resolution strategies like prioritizing one port or disabling one operation. The architecture is usually synchronous, meaning all actions occur on clock edges, but it can also be adapted to asynchronous modes for cross-clock domain applications. Overall, the dual port memory structure enhances data throughput and allows for efficient parallel processing, making it ideal for systems that require high-speed data exchange between multiple modules.

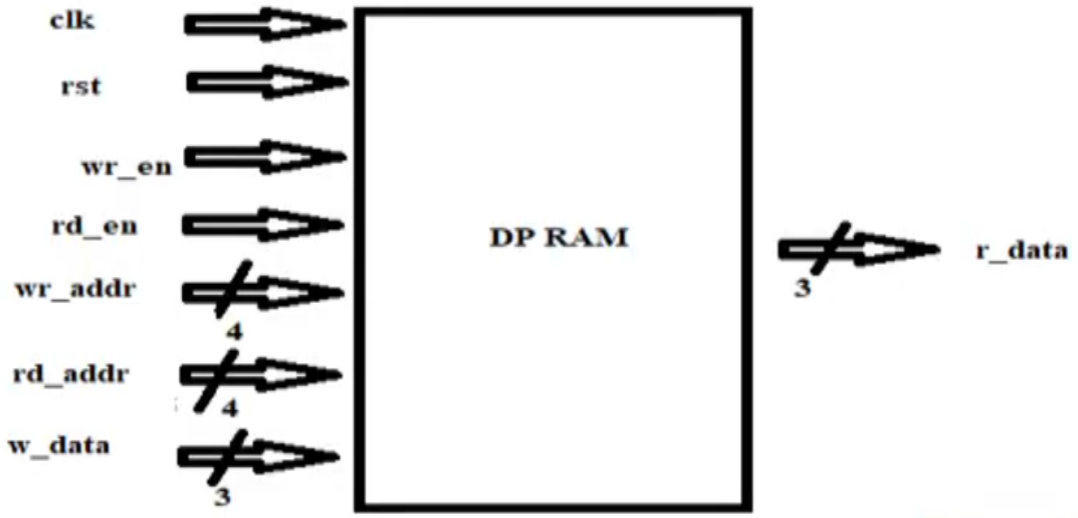

Figure 4.3: DPRam Architecture

4.4 RTL Coding in System Verilog

Register Transfer Level (RTL) coding refers to the design of digital systems using a hardware description language that describes how data flows between registers under the control of a clock. In this project, System Verilog is used for implementing the RTL model of Dual Port RAM due to its strong support for both design and verification.

The RTL code describes the internal structure of the memory, including how it stores and retrieves data, manages two ports, and handles control signals like read, write, clock, and reset. The design is written using synchronous logic, where memory operations are triggered by clock edges to ensure predictable behaviour. Each port in the code is assigned its own address, data, and control lines, allowing fully independent operation. System Verilog's support for logic data types, 2D arrays for memory modelling, and structured control flow

makes the code more readable and maintainable. Parameterization can also be implemented in the RTL code, allowing easy modification of data width and memory depth without rewriting the design. The goal of the RTL implementation is to ensure correct functionality, synthesis compatibility, and smooth integration with the verification environment.

4.5 **Simulation Strategy**

Simulation is a critical part of verifying the correct behaviour of the RTL design before hardware realization. The objective is to test the Dual Port RAM under different input conditions, including normal operation and edge cases, using a controlled and automated test environment.

Simulation Strategy Steps:

1. **Testbench Development**
    - A dedicated testbench was created using System Verilog.
    - It includes clock generation, reset logic, input stimulus, and output checking.
2. **Clock and Reset Generation**
    - A periodic clock signal was used to drive synchronous operations.
    - Active-low reset was applied at the beginning to initialize memory contents.
3. **Stimulus Creation**
    - Test cases were created for different operations like write-only, read-only, and combined read/write.
    - Both ports were tested individually and together to ensure independent functionality.
4. **Same Address Access Testing**
    - Cases where both ports access the same memory location were simulated.
    - These tests check for proper conflict handling and data consistency.
5. **Boundary Address Testing**
    - Read and write operations were tested at the lowest (0) and highest (2^n - 1) memory addresses.
    - This ensures correct address decoding across the full memory range.
6. **Functional Coverage Goals**
    - All valid operation combinations (read, write) were included in the tests.

- The aim was to cover typical usage scenarios and possible corner cases.

7. **Simulation Environment**
    - All simulations were run using **Xcelium**, a cloud-based HDL simulation platform.
    - Waveforms were analysed using **SimVision** for visual inspection of signal transitions and memory behaviour.
8. **Debugging and Analysis**
    - Errors and unexpected behaviour were identified using waveform data.
    - Debugging was done by tracing signal changes and matching them with expected behaviour.

CHAPTER 5

VERIFICATION USING SYSTEM VERILOG TESTBENCH RAM

5.1 Introduction to Functional Verification

Functional verification is the process of checking whether a digital design behaves as it is supposed to under various input conditions. It focuses on making sure that the implemented RTL code matches the original specification and performs all expected operations correctly. In modern VLSI design, functional verification has become one of the most time-consuming yet essential steps because a small logic error can lead to major issues in real hardware. Instead of physically building the circuit and testing it, simulation-based verification is used to try out different scenarios virtually. This helps catch bugs early and reduces the cost of corrections later. Verification involves creating a testbench, applying test cases, and observing the outputs to ensure that they match the expected behaviour. Tools like assertions, coverage analysis, and constrained-random testing are often used to make the process more thorough. In this project, functional verification was used to confirm that the Dual Port RAM performs correct read and write operations, even when both ports are active at the same time.

5.2 Verification Methodology Adopted

To verify the functionality of the Dual Port RAM, a simulation-based verification methodology was adopted. This approach focuses on validating whether the RTL design performs as expected under a wide range of operational conditions. The entire verification process was built using System Verilog and executed on **Xcelium**, with waveform analysis performed using **SimVision**.

The first step in the verification methodology was to define a clear set of functional requirements and test objectives. These included checking individuals read and write operations, testing both ports simultaneously, handling corner cases like accessing the same address from both ports at once, and verifying correct operation under reset conditions. These requirements formed the basis for designing the test scenarios.
A modular testbench architecture was developed to ensure that the verification environment was reusable, organized, and easy to extend.

The architecture included standard components like a **generator**, **driver**, **interface**, **monitors**, **reference model**, and **scoreboard**, each serving a specific role. The **generator** was responsible for producing test transactions, which were structured using a defined **packet**

format. These packets encapsulated all necessary information for a memory operation, such as address, data, and control signals.

The **driver** converted these transactions into actual pin-level activity by applying stimulus to the DUT through a virtual interface. The **interface** acted as a shared signal bridge between the testbench and the DUT, simplifying communication. Two **monitors** were used: one to capture input stimulus sent to the DUT and another to observe the outputs produced by the DUT. This dual-monitor setup allowed both input tracking and output checking in parallel.
To check the correctness of the DUT's behaviour, a **reference model** was implemented. This model processed the same inputs captured by the monitor and generated the expected outputs based on ideal RAM behaviour. These expected results were then compared with the DUT's actual output using the **scoreboard**. Any mismatches were logged and highlighted for debugging.

The methodology also included **reset testing** at the beginning of every test sequence to bring the DUT into a known state. Different types of test cases were written, including directed tests to target specific scenarios and random tests to increase functional coverage. In each test case, memory content was tracked and verified to ensure consistency and correctness.
Although assertions were not used in this setup, the layered methodology made debugging simpler. Whenever an output mismatch occurred, waveform traces from SimVision helped in identifying whether the issue was in stimulus generation, data handling inside the DUT, or timing misalignments.
In summary, the verification methodology followed a structured and layered approach that ensured every functional aspect of the Dual Port RAM was exercised and validated. The use of Xcelium for simulation and SimVision for waveform analysis made the process both accessible and effective for catching functional bugs.

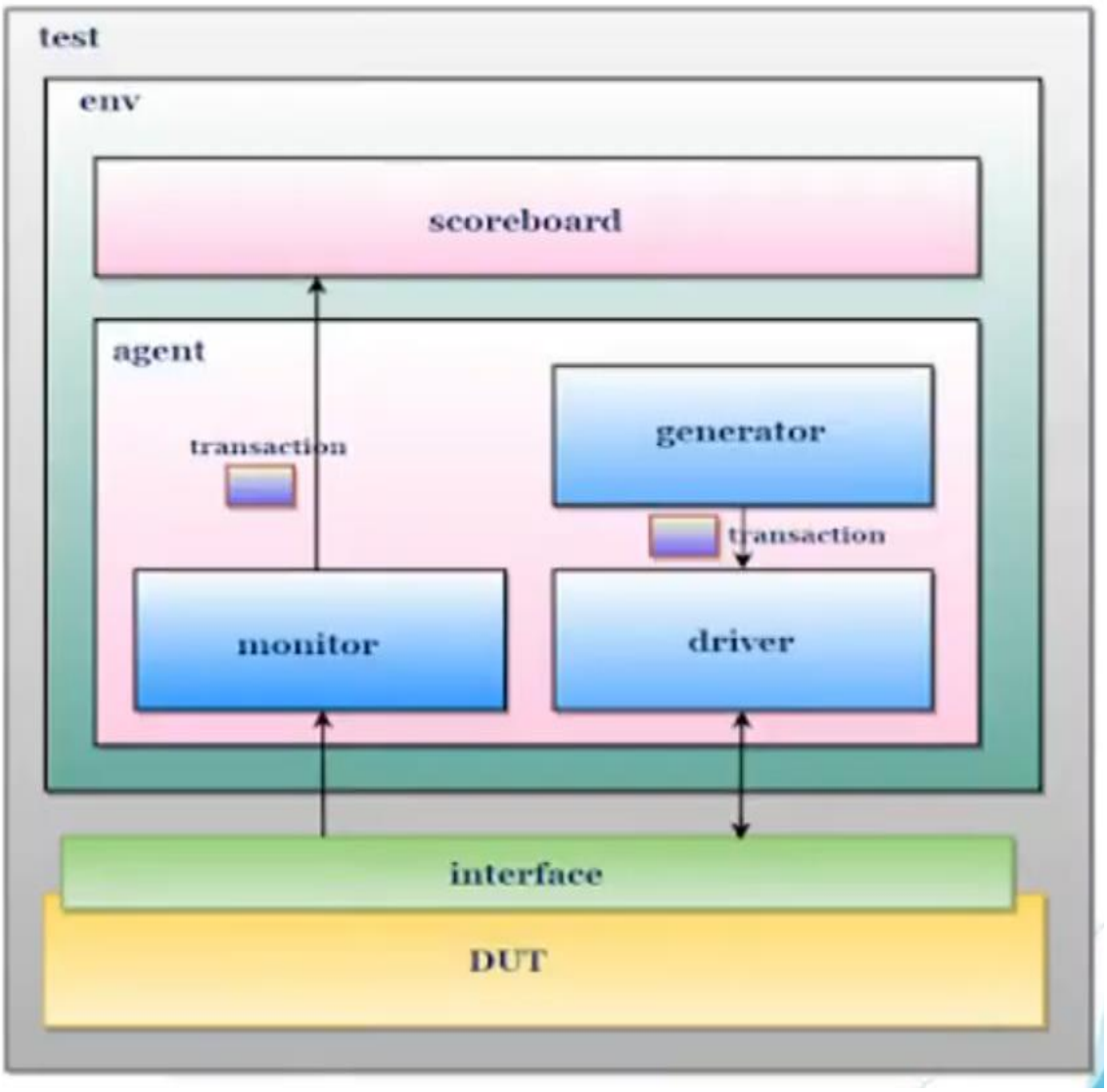

Figure 5.2: Testbench Architecture

5.3 Testbench Architecture

The verification environment for the Dual Port RAM was built using a structured testbench architecture, where each block plays a distinct role in the overall simulation and checking process. This modular approach provides clear separation between stimulus generation, DUT interaction, signal observation, and result validation, making the testbench easy to manage and extend.

1) Transaction

This is the fundamental unit of the testbench, which defines the format of a memory transaction. It typically includes fields like address, data, operation type (read,write,read & write), and any required control bits. Transaction are passed across various testbench components to ensure uniformity in how test cases are described and applied.

2) Generator

The generator creates a series of transaction either with random values for stress testing or directed values to cover specific scenarios. These transactions are used to test various operations like single-port writes, reads, and simultaneous dual-port access. Once created, packets are sent to the driver using a mailbox for synchronization.

3) Driver

The driver receives transaction from the generator and translates them into actual signal-level activity. It applies the inputs to the DUT by driving address, data, read/write enables, and other control signals through a virtual interface. The driver ensures that high-level test instructions are properly executed on the DUT.

4) Interface

The interface acts as a shared connection point between the DUT and the rest of the testbench. It groups all signals such as data, address, control, clock, and reset into a unified structure, making it easier for the driver and monitors to interact with the DUT using a virtual handle.

5) DUT (Design Under Test)

This block represents the RTL implementation of the Dual Port RAM. It receives signal-level inputs from the driver and processes them according to the internal logic. The DUT performs read or write operations based on the control signals and generates appropriate output data.

6) Monitor_1

Monitor_1 passively observes the inputs applied to the DUT. It uses a virtual interface to capture input transactions without interfering with signal flow. These observed transactions are sent to the reference model to generate expected outputs for validation.

7) Reference Model

The reference model simulates ideal behaviour of the memory. Based on the inputs from Monitor_1, it produces expected outputs that the DUT should ideally generate. These are used as a baseline to compare against the DUT's actual responses.

8) Monitor_2

This monitor listens to the DUT's output signals. It captures the actual results produced during the simulation and forwards them to the scoreboard. Monitor_2 plays a critical role in determining the final correctness of each test case.

9) Scoreboard

The scoreboard receives both expected outputs from the reference model and actual outputs from Monitor_2. It performs a comparison and flags mismatches if any discrepancies occur. This component helps identify logical errors in the DUT and logs mismatches for review.This architecture ensures a well-organized, robust simulation environment for verifying the Dual Port RAM. Its modular nature allows easier debugging and reuse, making it ideal for both current design validation and future design upgrades.

5.4 Constrained Random Stimulus Generation

Constrained random stimulus generation is a key technique used in modern verification environments to thoroughly test a digital design under a wide range of scenarios. Instead of manually writing each test case, the testbench is programmed to generate input values randomly—but within defined rules or "constraints."

This allows for automatic generation of diverse and unpredictable inputs, while still ensuring that the generated data is valid and meaningful for the design under test (DUT).In the context of verifying the Dual Port RAM, this approach helps simulate a variety of real-world memory access conditions without the need to write individual tests for every possible combination. For example, the generator may randomly select read or write operations, choose address values within a valid range, and assign data values that follow certain patterns. Constraints are applied to make sure, for instance, that invalid addresses are not chosen, or that simultaneous write operations to the same location by both ports are handled carefully.

This technique is especially useful for catching bugs that may not appear during regular directed testing. Since constrained random generation can produce sequences that a human might not think of, it increases the likelihood of exposing corner-case issues or timing-related bugs. Furthermore, coverage metrics can be used alongside this method to ensure that the design is being tested across all its functional states.

In this project, the **Generator** module was designed to support constrained random stimulus.

It creates memory transactions by randomly selecting fields such as address, data, and control signals, while keeping within legal boundaries using user-defined constraints. These transactions are then sent to the **Driver**, which applies them to the DUT.

Overall, constrained random stimulus generation adds flexibility, depth, and efficiency to the verification process, making it more likely to find hidden design issues early in the development cycle.

5.5 Debugging Techniques and Challenges

Constrained random stimulus generation is a key technique used in modern verification environments to thoroughly test a digital design under a wide range of scenarios. Instead of manually writing each test case, the testbench is programmed to generate input values randomly—but within defined rules or "constraints." This allows for automatic generation of diverse and unpredictable inputs, while still ensuring that the generated data is valid and meaningful for the design under test (DUT).

Debugging is a crucial step in the verification process, aimed at identifying and resolving issues that arise during simulation or functional testing. It ensures that the Design Under Test (DUT) behaves correctly under all defined conditions. However, as designs become more complex, debugging also becomes more time-consuming and technically demanding.

Common Debugging Techniques

1. **Waveform Analysis Using SimVision -** One of the most commonly used methods is visual waveform inspection using tools like **EPWave** (integrated in Xcelium). Engineers observe signal transitions and timing relationships to pinpoint errors in logic, timing, or sequencing.
2. **Assertions (When Used)** - System Verilog assertions (SVAs) help detect violations of design expectations. If an assertion fails during simulation, it flags the error immediately and provides the exact condition that was violated.
3. **Print Statements and Logs** -Inserting $display or $monitor statements allows the verification engineer to track variable values or control flow during simulation. Though basic, this method remains effective for small-scale designs.

4. **Scoreboard and Reference Model Comparison** - By comparing DUT outputs with a predicted result from a reference model, mismatches can be quickly detected. The **scoreboard** flags discrepancies, helping isolate bugs in the data path or control logic.

5. **Transaction Logging** - Capturing high-level transactions (from generator to driver, monitor, and scoreboard) provides insight into where failures occur and in what context, making root-cause analysis easier.

Common Challenges in Debugging

- **Signal Complexity and Volume** - Large numbers of signals and clock domains can make it difficult to trace the exact sequence of operations leading to an error.
- **Concurrency Issues** - In dual-port memory, simultaneous read/write operations can lead to conflicts or race conditions that are difficult to detect unless specific checks are in place.
- **Random Stimulus Behaviour** - Constrained-random stimulus generation improves coverage but can make bugs harder to reproduce without storing the random seed.
- **Poor Observability** - If internal signals are not exposed or monitored, it becomes difficult to know what went wrong inside the DUT.
- **Tool Limitations** - Online tools like Xcelium and SimVision are limited in terms of speed and scope compared to full-fledged commercial tools, which can sometimes delay debugging.

CHAPTER 6

RESULTS, CONCLUSION, AND FUTURE WORK

6.1 Summary of Design and Verification Results

The design of the Dual Port RAM was successfully implemented using System Verilog, meeting all specified functional and architectural requirements. The module supported simultaneous read and write operations across two independent ports, with correct handling of control signals, address decoding, and data path operations. Key design parameters such as 8-bit data width and 5-bit address width (allowing 16 memory locations) were verified to function as expected under various scenarios.

The verification environment was built using a modular testbench structure on Xcelium, with SimVision used for waveform inspection. Multiple test scenarios were developed, including single-port operations, dual-port accesses, simultaneous read/write, and corner cases involving access conflicts. Functional coverage was achieved through a mix of directed and constrained-random test generation.

All test cases passed successfully, and the DUT's outputs matched those predicted by the reference model. No mismatches were found in the scoreboard, confirming the correctness of both individual operations and multi-cycle behaviors. The testbench also demonstrated the design's robustness under reset conditions and when subjected to edge-case inputs.

In conclusion, the results confirmed that the Dual Port RAM design operated reliably across all tested scenarios, validating the effectiveness of both the RTL implementation and the adopted verification methodology.

1) Write Operation

```
# KERNEL: ------GENERATOR writing------0
# KERNEL: wr=1, rd=0, w_addr=0x02, w_data=0xAB, r_addr=--, r_data=--, enb=1
# KERNEL: ------DRIVER WITH OUTPUT------1
# KERNEL: wr=1, rd=0, w_addr=0x02, w_data=0xAB, r_addr=--, r_data=--, enb=1
# KERNEL: ------COLLECTED IN MONITOR_1------3
# KERNEL: wr=1, rd=0, w_addr=0x02, w_data=0xAB, r_addr=--, r_data=--, enb=1
```

2) Read Operation

```
# KERNEL: ------GENERATOR reading------10
# KERNEL: wr=0, rd=1, w_addr=--, w_data=--, r_addr=0x02, r_data=0xAB, enb=1
# KERNEL: ------DRIVER WITH OUTPUT------11
# KERNEL: wr=0, rd=1, w_addr=--, w_data=--, r_addr=0x02, r_data=0xAB, enb=1
# KERNEL: ------COLLECTED IN MONITOR_2------13
# KERNEL: wr=0, rd=1, w_addr=--, w_data=--, r_addr=0x02, r_data=0xAB, enb=1
```

3) Simultaneous Read + Write Operation

```
# KERNEL: ------GENERATOR read+write------20
# KERNEL: wr=1, rd=1, w_addr=0x05, w_data=0x66, r_addr=0x02, r_data=0xAB, enb=1
# KERNEL: ------DRIVER WITH OUTPUT------21
# KERNEL: wr=1, rd=1, w_addr=0x05, w_data=0x66, r_addr=0x02, r_data=0xAB, enb=1
# KERNEL: ------COLLECTED IN MONITOR_1------22
# KERNEL: wr=1, rd=1, w_addr=0x05, w_data=0x66, r_addr=0x02, r_data=0xAB, enb=1
# KERNEL: ------COLLECTED IN MONITOR_2------23
# KERNEL: wr=1, rd=1, w_addr=0x05, w_data=0x66, r_addr=0x02, r_data=0xAB, enb=1
```

Figure 6.1: Output Log

6.2 Output Snapshots and Waveforms

To validate the functional correctness of the Dual Port RAM design, simulation waveforms were generated and analyzed using **EPWave**, the waveform viewer available on **Xcelium**. These waveforms visually confirm that the memory behaved as expected under a variety of test conditions.

The output snapshots include key scenarios such as:

- **Write Operation**: When the write enable (wr) signal is high and valid address and data are provided, the waveform shows data being written correctly to the targeted memory location.

- **Read Operation**: For cases where the read enable (rd) is asserted, the output data line (data_out) reflects the stored value from the specified address after the appropriate clock cycle delay.
- **Simultaneous Read/Write**: A critical snapshot captures the behaviour when both ports are active simultaneously, performing a read on one port and a write on the other. The design maintains correct data flow, showing no interference or corruption.
- **Reset Behaviour**: The waveforms confirm that when the reset signal (rst_n) is asserted (low), the memory contents are cleared or initialized, and the output data lines return to a known state.

Each waveform view was inspected closely to confirm signal integrity, timing correctness, and data consistency. No glitches or unexpected transitions were observed during testing. These visual outputs provided additional confirmation alongside scoreboard-based checks, proving the Dual Port RAM's correctness across normal and edge-case operations. Waveform analysis played a crucial role in debugging and validating the design and helped identify and resolve minor issues during early testbench development.

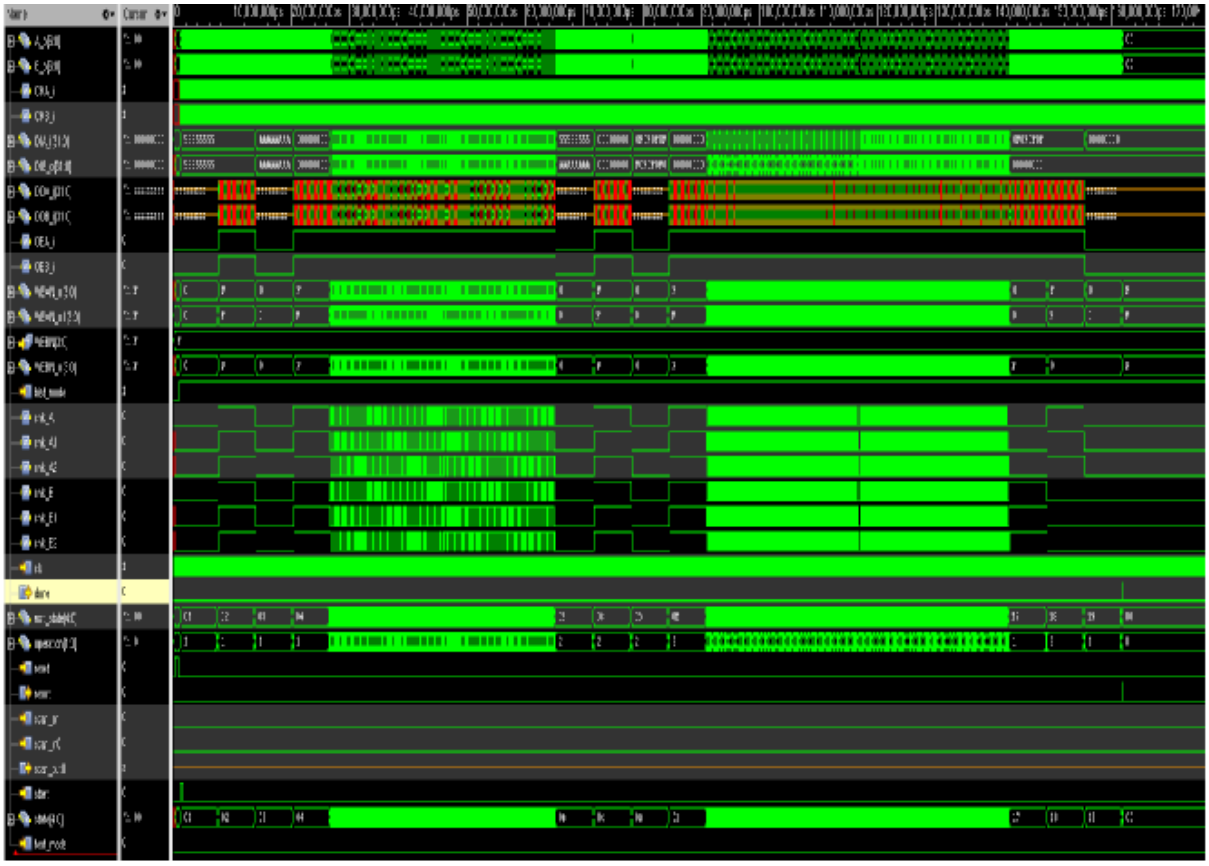

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Figure 6.2: Output Waveform

6.3 Architecture of Dual Port RAM

During the verification of the Dual Port RAM, test completeness and reliability were evaluated using basic System Verilog testbench. While formal coverage tools were not used in this project, the testbench was designed to cover all primary use cases manually. Test scenarios included single-port operations (read/write), simultaneous dual-port access with different addresses, both ports accessing the same location, and reset conditions. These conditions ensured that all control paths, address ranges, and data variations were exercised at least once during simulation.

Each test case was associated with expected output values, which were compared against the actual DUT responses by the **scoreboard**. In this project, all executed test cases passed successfully, indicating that the RTL design met its functional requirements.

Though formal code coverage metrics like line, toggle, or branch coverage were not recorded, the use of **constrained-random stimulus**, combined with directed tests, helped increase confidence in verification completeness.

Additionally, waveform inspection through SimVision confirmed that signals transitioned as expected across various scenarios. Overall, the results demonstrated that the verification effort was thorough enough to validate the reliability and correctness of the Dual Port RAM design.

6.4 Limitations of Current Work

While the design and verification of the Dual Port RAM were successfully completed, there are certain limitations in the current work that can be addressed in future improvements. First, the testbench used for verification was built manually without using industry-standard verification frameworks like UVM. As a result, scalability and reusability are limited, especially for more complex memory systems. Additionally, formal coverage metrics such as code coverage, functional coverage, or assertion-based coverage were not collected or analysed, which may leave some areas of the design unverified at a deeper level. The memory depth and data width were kept relatively small (16 locations with 8-bit width) to keep simulation simple and readable, but this may not reflect real-world requirements. Moreover, the current design assumes synchronous operation with a shared clock;

asynchronous dual-port scenarios or multi-clock domain behavior were not tested. Finally, although basic conflict handling was considered, advanced arbitration logic for simultaneous writes to the same address was not implemented, which could be essential in more complex applications.

6.5 Conclusion

The objective of this project was to design and verify a Dual Port RAM module using System Verilog, with a focus on both functionality and verification efficiency. Through systematic development of the RTL design, the memory was built to support simultaneous operations on two independent ports, enabling parallel read and write transactions. The design adhered to defined parameters such as address width, data width, and synchronous clocking, ensuring proper functionality across all valid memory access scenarios.

A modular and reusable verification environment was developed entirely in System Verilog and implemented on Xcelium. The testbench included transaction-level components like generator, driver, monitors, reference model, and scoreboard to create a comprehensive simulation setup. Both directed and constrained-random test cases were used to evaluate a wide range of use cases, including corner conditions. Waveform inspection using SimVision further confirmed the signal-level behaviour of the design under test.

All test cases passed successfully, and the output data matched the expected values predicted by the reference model. The scoreboard reported no mismatches, confirming the correctness of the DUT across tested conditions. The verification strategy proved effective in exposing and resolving functional issues early in the process.

In conclusion, the design met its intended objectives, and the adopted verification methodology provided reliable assurance of its correctness. Although the project has a few limitations—such as the absence of formal coverage metrics and multi-clock testing—the overall framework lays a strong foundation for future enhancement, scalability, and potential integration into larger digital systems.

6.6 Scope for Future Enhancements

While the current design and verification of the Dual Port RAM meet basic functional requirements, several enhancements can be explored to extend its capabilities and make it more suitable for real-world applications:

1. **Error Correction Code (ECC) Integration**

To improve data reliability in safety-critical or noise-prone environments, the RAM can be extended with ECC mechanisms such as Hamming Code. This would enable automatic detection and correction of single-bit errors, making the memory more robust for industrial or communication systems.

2. **Migrate to UVM-Based Verification**

   Although the current testbench was built using a custom System Verilog environment, migrating to the **Universal Verification Methodology (UVM)** would allow for better scalability, reuse, and integration with industry-standard IP verification flows. UVM also offers built-in support for constrained-random generation, functional coverage, and advanced reporting mechanisms.

3. **Pipelined DPRAM Architecture**

   To increase performance, the Dual Port RAM design can be enhanced with **pipelining techniques**. This would allow read and write operations to be broken down into multiple clock-cycle stages, improving throughput and timing closure for high-speed designs, especially in FPGA and ASIC implementations.

4. **Support for Asynchronous Operation**

   The current version assumes synchronous operation for both ports using a shared clock. Future versions can include support for **asynchronous ports**, where each port operates on a separate clock domain. This is particularly useful in multi-core processors and SoCs where modules operate at different frequencies.

5. **Configurable Design Parameters**

   Making data width, address depth, and number of ports configurable at compile time or runtime (via generics or parameters) would increase flexibility. This could enable easier reuse of the memory design in different systems with varying requirements.

6. **Power-Aware Design Techniques**

   Power gating, clock gating, and low-power mode support can be introduced in future versions to make the RAM more suitable for battery-powered or energy-efficient systems.

7. Integrating into SoC or CPU Subsystems

The design can be embedded into a larger **System-on-Chip (SoC)** or used as a tightly coupled memory for a **custom processor core**. This would test its real-world compatibility and performance in an integrated digital system.

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APPENDIX

Dual Port RAM RTL

```
module dual_port_ram (
   input  logic       clk,
   input  logic       rst,
   input  logic       wr,
   input  logic       rd,
   input  logic [3:0]  w_addr,   // Write address
   input  logic [3:0]  r_addr,   // Read address
   input  logic [7:0]  w_data,   // Write data
   output logic [7:0]  r_data    // Read data
);

   // Define memory array
   logic [7:0] mem [15:0];

   always_ff @(posedge clk or posedge rst) begin
      if (rst) begin
         r_data <= 8'b0; // Reset read data
      end
      else begin
         if (wr && !rd) begin
            mem[w_addr] <= w_data;  // Write operation
         end
         else if (!wr && rd) begin
            r_data <= mem[r_addr];  // Read operation
         end
         else if (wr && rd) begin
            mem[w_addr] <= w_data;
            r_data <= mem[r_addr];  // Simultaneous read & write
         end
         else begin
            for (int i = 0; i < 16; i++) begin
               mem[i] <= mem[i]; // Maintain stored values
            end
         end
      end
   end
endmodule
```

Transaction

```
class transaction;

   // Data members
   rand logic [7:0]  w_data;     // Randomized write data
        logic        enb = 1;    // Enable signal
        logic        wr;         // Write control
        logic        rd;         // Read control
   rand logic [4:0]  w_addr;     // Randomized write address
        logic [4:0]  r_addr;     // Read address
        logic [7:0]  r_data;     // Read data received from DUT

   // Constraint on address range
   constraint W_addr1 { w_addr <= 16'h000F; }

   // -------------------------
   // Display function for debug
   // -------------------------
```

```
    function void display(string name);
        $display("------%s------%0t", name, $time);
        $display("wr=%0h, rd=%0h, w_addr=%0h, w_data=%0h, r_addr=%0h, r_data=%0h, enb=%0b",
                 wr, rd, w_addr, w_data, r_addr, r_data, enb);
    endfunction

endclass
```

Generator

```
class generator;

    transaction tx;
    mailbox gen2drv;
    logic [4:0] w_addr;

    // Constructor: Bind mailbox
    function new(mailbox gen2drv);
        this.gen2drv = gen2drv;
    endfunction

    // ------------------------------
    // Task for Write Operation
    // ------------------------------
    task write();
        repeat (1) begin
            tx = new();
            tx.randomize();
            tx.wr   = 1;
            tx.rd   = 0;
            tx.enb  = 1;
            tx.w_addr = tx.w_addr;      // Randomized address
            tx.w_data = 8'hAB;          // Example write data
            gen2drv.put(tx);
            tx.display("GENERATOR writing");
        end
    endtask

    // ------------------------------
    // Task for Read Operation
    // ------------------------------
    task read();
        repeat (1) begin
            tx = new();
            tx.wr   = 0;
            tx.rd   = 1;
            tx.enb  = 1;
            tx.r_addr = 5'h0B;          // Example read address
            gen2drv.put(tx);
            tx.display("GENERATOR reading");
        end
    endtask

    // ------------------------------------------------
    // Task for Simultaneous Read and Write Operation
    // ------------------------------------------------
    task read_write();
        repeat (1) begin
            tx = new();
            tx.wr   = 1;
            tx.rd   = 1;
            tx.enb  = 1;
            tx.w_addr = 5'h0D;          // Write to different address
```

```
            tx.w_data = 8'h66;          // Example write data
            tx.r_addr = 5'h0B;          // Read from earlier written address
            gen2drv.put(tx);
            tx.display("GENERATOR read+write");
        end
    endtask

endclass
```

Driver

```
class driver;

    transaction tx;
    mailbox gen2drv;
    virtual intf vif;   // Virtual interface handle

    // Constructor: bind mailbox and interface
    function new(mailbox gen2drv, virtual intf vif);
        this.gen2drv = gen2drv;
        this.vif     = vif;
    endfunction

    // ------------------------------
    // Task: Drive transaction to DUT
    // ------------------------------
    task run();
        repeat (1) begin
            gen2drv.get(tx);            // Get transaction from generator

            // Apply signals to DUT via interface
            vif.enb     <= tx.enb;
            vif.wr      <= tx.wr;
            vif.rd      <= tx.rd;
            vif.w_addr  <= tx.w_addr[4:0];
            vif.r_addr  <= tx.r_addr[4:0];
            vif.w_data  <= tx.w_data[7:0];

            #1;  // Wait for signals to settle (if needed)

            tx.display("DRIVER WITH OUTPUT");
        end
    endtask

endclass
```

Scoreboard

```
class scoreboard;
  transaction tx, tx_ref;
  mailbox mbx;

  function new(mailbox mon2scb);
    mbx = mon2scb;
  endfunction

  task run();
    forever begin
      mbx.get(tx);
      $display("Scoreboard received transaction");

      // Create a reference copy
```

```
      tx_ref = new();
      tx_ref.enb     = tx.enb;
      tx_ref.wr      = tx.wr;
      tx_ref.rd      = tx.rd;
      tx_ref.w_addr  = tx.w_addr;
      tx_ref.r_addr  = tx.r_addr;
      tx_ref.w_data  = tx.w_data;

      // Wait for 1 time unit or simulation cycle
      #1;

      // Scoreboard comparison logic
      if (tx.r_data == tx_ref.r_data) begin
        $display("------------ TEST PASS ------------");
        $display("Actual Data   : %0h", tx.r_data);
        $display("Expected Data : %0h", tx_ref.r_data);
      end else begin
        $display("------------ TEST FAIL ------------");
        $display("Actual Data   : %0h", tx.r_data);
        $display("Expected Data : %0h", tx_ref.r_data);
      end
    end
  endtask

endclass
```

Interface

```
interface intf (input logic clk);

    // Control and data signals
    logic rst;
    logic enb;
    logic wr;
    logic rd;

    logic [4:0] w_addr;     // Write address
    logic [7:0] w_data;     // Write data

    logic [4:0] r_addr;     // Read address
    logic [7:0] r_data;     // Read data

    // Clocking block (optional)
    // Useful for synchronizing in advanced testbenches
    // clocking cb @(posedge clk);
    //     output wr, rd, enb, w_addr, w_data, r_addr;
    //     input r_data;
    // endclocking

endinterface
```

Enviornment

```
class environment;

  // Component handles
  generator  gen;
  driver     drv;
  monitor    mon;
  scoreboard scb;
```

```
  // Mailboxes for inter-component communication
  mailbox gen2drv = new();
  mailbox mon2scb = new();

  // Virtual interface handle
  virtual intf vif;

  // Constructor
  function new(virtual intf vif);
    this.vif = vif;

    // Create and connect components
    gen = new(gen2drv);
    drv = new(gen2drv, vif);
    mon = new(mon2scb, vif);
    scb = new(mon2scb);
  endfunction

  // Run method to start parallel execution of components
  task run();
    fork
      gen.write();
      drv.run();
      mon.run();
      scb.run();
    join
  endtask

endclass
```

QuillBot

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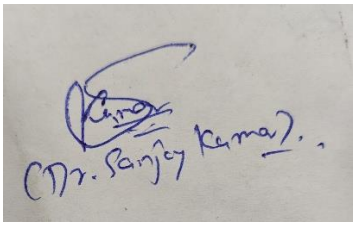

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