DESIGN OF LOW POWER CMOS CELL STRUCTURES BASED ON SUBTHRESHOLD CONDUCTION PRINCIPLE

Thesis submitted towards the partial fulfillment of the requirements for the award of the degree of

Master of Technology (VLSI Design & CAD)

Submitted by

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CERTIFICATE

I hereby certify that the work which is being presented in the thesis entitled "**DESIGN OF LOW POWER CMOS CELL STRUCTURES BASED ON SUBTHRESHOLD CONDUCTION PRINCIPLE**", in the partial fulfillment of the requirements for the award of degree of **Master of Technology in VLSI Design & CAD** at **Thapar University, Patiala,** is an authentic record of my own work carried out under the supervision of **Mr. Sanjay Kumar,** Assistant Professor, Department of Electronics and Communication Engineering and refers other researcher's work which are duly listed in the reference section.

The matter embodied in this thesis has not been submitted for the award of any other degree of this or any other university.

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This is to certify that the above statement made by the candidate is correct and true to the best of my knowledge.

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ABSTRACT

While performance and area remain to be two major design goals, power consumption has become a critical concern in today's VLSI system design. Also the battery operated devices demand to reduce the power to increase the life of devices. Digital circuits operating in the subthreshold region of the transistor are being used as an ideal option for ultra low power complementary metal oxide semiconductor (CMOS) design. But in subthreshold circuit design the performance of the circuit degrades significantly. Hence the use of subthreshold circuit designing in fast and energy efficient circuits is always needed, in electronics industry especially in DSP, image processing and arithmetic units in microprocessors, where the low power is the primary concern and the delay can be tolerated.

The main aim of this thesis work is to understand the viability of subthreshold circuit designing to design low power circuits in VLSI. So different CMOS cell structures are designed operating in subthreshold conduction region and also a methodology to identify the minimum energy point, frequency range and operating voltage for CMOS standard cells is defined. The similar CMOS cell structures are also designed operating in superthreshold conduction region. Power of these structures are then compared to understand the usefulness of subthreshold circuit designing for low power VLSI design. All these circuits were designed in Mentor Graphics IC Design Architect using standard TSMC 0.18 μm technology, laid out in Mentor Graphics IC Station.

All the circuit simulations has been done using various schematics of the structures and post-layout simulations are also being done after they all have been laid-out by considering all the basic design rules and by running the LVS program. Finally, the analysis of the average dynamic power dissipation with respect to the frequency and the supply voltage was done to show the amount of power dissipated by the circuits operating in subthreshold conduction region and superthreshold conduction region.

By the analysis, it was seen that the power dissipation in the circuits operating in subthreshold conduction region was in the range of picowatt while the power dissipation in the circuits operating in subthreshold conduction region was in the range of microwatt.

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α	Switching Activity [dimensionless]
C_L	Load Capacitance [Farads]
C_{ox}	Oxide Capacitance [Farads/ μm^2]
E	Energy [Jouls]
$E_{dynamic}$	Dynamic Energy [Jouls]
E_{static}	Static Energy [Jouls]
f	Frequency of Operation [Hz]
L_{DP}	Depth of Critical Path [dimensionless]
I_{static}	Static Current [Amperes]
I_D	Drain Current [Amperes]
I_{on-sub}	Subthreshold Current [Amperes]
I_0	Drain Current for V_{gs}= V_{th} [Amperes]
P	Power [Watts]
μ_{eff}	Effective Mobility of majority carriers [Cm^2/V Sec]
n	Subthreshold Slope Factor [dimensionless]
$\frac{W}{L}$	Aspect Ratio [μm/ μm]
t_d	Propagation Delay of an Inverter [Seconds]
T_D	Total Delay of a circuit [Seconds]
V_{dd}	Supply Voltage [Volts]
V_{th}	Threshold Voltage of MOSFET [Volts]
V_T	Thermal Voltage [Volts]
V_s	Voltage Swing [Volts]

CHAPTER 1 INTRODUCTION

1.1 MOTIVATION

As the scale of integration keeps growing, more and more sophisticated signal processing systems are being implemented on a VLSI chip. These signal processing applications not only demand great computation capacity but also consume considerable amounts of energy. While performance and area remain to be two major design goals, power consumption has become a critical concern in today's VLSI system design [1]. The need for low-power VLSI systems arises from two main forces. First, with the steady growth of processing capacity per chip, large current has to be delivered and the heat due to large power consumption must be removed by proper cooling techniques. Second, battery life in portable electronic devices is limited. Low power design directly leads to prolonged operation time in these portable devices.

Also, with shrinking technology sizes, energy efficiency has become a critical aspect of designing digital circuits. Traditionally, voltage scaling, a mechanism in which the supply voltage is varying and the threshold voltage is constant, has been an effective solution in meeting stringent energy requirements. However, voltage scaling does come at a cost of reduction in performance. The limits of voltage scaling, and therefore energy minimization, can be explored by operating a circuit at subthreshold [2]. In subthreshold circuits, the supply voltage is reduced well below the threshold voltage of a transistor. Due to the quadratic reduction in power with respect to the supply voltage, subthreshold circuits are classified as *ultra low power circuits*.

Specifically in application areas where performance can be sacrificed for low power, subthreshold circuits are an ideal fit. Some of the applications include devices such as digital wrist watches [3], radio frequency identification (RFID), sensor nodes, pacemakers and battery operated devices such as, cellular phones.

1.2 WHY TO MINIMIZE THE POWER

Even when power is available in nonportable applications, the issue of low power design is becoming critical. Up until now, this power consumption has not been of great concern, since large packages and other cooling techniques have been capable of dissipating the generated heat. However, as the density and size of the chips and systems continue to increase, the difficulty in providing adequate cooling might either add significant cost to the system or provide a limit on the amount of functionality that can be provided [4].

While the power dissipation increases linearly as the years go by, the power density increases exponentially, because of the ever-shrinking size of the integrated circuits. If this exponential rise in the power density were to increase continuously, a microprocessor designed a few years later, would have the same power as that of the nuclear reactor. Such high power density introduces reliability concerns such as, electromigration, thermal stresses and hot carrier induced device degradation, resulting in the loss of performance. Thus, it is evident that the methodologies for the design of low power digital systems are needed.

Another factor that fuels the need for low power chips is the increased market demand for portable consumer electronics powered by batteries. The craving for smaller, lighter and more durable electronic products indirectly translates to low power requirements. Battery life is becoming a product differentiator in many portable systems. Being the heaviest and biggest component in many portable systems, batteries have not experienced the similar rapid density growth compared to the electronic circuits. The main source of power dissipation in these high performance battery-portable digital systems running on batteries such as, laptops, cellular phones and personal digital assistants (PDAs) are gaining prominence. For these systems, low power consumption is a prime concern, because it directly affects the performance by having effects on battery longevity. In this situation,

low power VLSI design has assumed great importance as an active and rapidly developing field.

Hence, motivated by emerging battery operated applications that demand intensive computation in portable environments such as, laptops, PDAs, digital wrist watches, pacemakers and cellular phones etc, techniques are investigated which reduce power consumption in CMOS digital circuits, by operating the devices at low currents and low voltages. It is known that MOS devices and circuits especially CMOS circuits consume relatively low power. But there seems to be a need to reduce this power further to prolong the life of battery [5].

1.3 OPERATING REGION FOR POWER MINIMIZATION

Due to their extreme low power consumption, subthreshold design approaches are appealing for a widening class of applications which demand low power consumption and can tolerate larger circuit delays [6]. Over the last 10 years, digital subthreshold logic circuits have been developed for applications in the ultra low power design domain, where performance is not the priority [5].

Subthreshold logic circuits operate with power supply V_{dd} less than transistors threshold voltage V_{th} . This is done to ensure that all the transistors are indeed operating in the subthreshold region [7,8].

Subthreshold (leakage or cut-off) currents are a necessary evil in traditional VLSI design methodologies. These currents increase exponentially as threshold voltage scales, creating a serious problem for traditional design approaches. Our approach is based on the exclusive use of subthreshold conduction currents to perform circuit operations, turning this problem into an opportunity. This yields a dramatic improvement in power consumption compared to traditional circuit design approaches. This reduction makes it feasible to design extreme low power circuits with such an approach.

The magnitude of subthreshold currents are significantly smaller than linear or saturation currents since I_{D0} is extremely small. In traditional digital VLSI design, the subthreshold region of operation is avoided. Circuit operation is based purely on linear or saturation

mode currents, and subthreshold currents are viewed as an attendant evil, since they contribute towards leakage power consumption when the device is in stand-by. As the minimum feature size of processes continues to shrink with each successive process generation (along with the value of supply voltage and therefore V_{dd}), leakage currents increase exponentially. On the one hand this would suggest the choice of larger V_{th} values, but this in turn leads to slower circuits since the device (operating in linear or saturation region) has a slower turn-on when V_{th} is increased. Choosing a lower V_{th} results in lower delays but increased leakage power dissipation. Leakage power already comprises about 50% of the total power dissipation of modern designs, so this option is not desirable.

We exclusively utilize subthreshold leakage currents to implement circuits. This is achieved by actually setting the circuit power supply V_{dd} to a value less than or equal to V_{th}. This choice results in dramatically smaller conduction currents and power, but also larger circuit delays as well [5].

1.4 THESIS ORGANIZATION

The primary goal of this thesis is to demonstrate a circuit level design approach, for use in designs which demand ultra low power dissipation.

This thesis is organized as follows:

CHAPTER 1: INTRODUCTION. In this chapter, the power consumption issues in the area of VLSI have been introduced. This chapter also explains why we need low power design in the today's era of continuously scaling down of technologies.

CHAPTER 2: SUBTHRESHOLD CONDUCTION FOR LOW POWER VLSI DESIGN. This chapter begins with an introduction to different conduction regions of the circuits and after that, explains the behavior of a transistor in the subthreshold region of operation. This chapter also discusses about the total power and energy of a circuit.

CHAPTER 3: MATHEMATICAL ANALYSIS OF SUBTHRESHOLD CMOS INVERTER. This chapter explains how to find the optimal value of supply voltage V_{dd} by using graphical method and after that this chapter also explains the mathematical

method to find the optimal value of V_{dd}. In this chapter, other components of leakage current except subthreshold leakage current have also been discussed.

CHAPTER 4: DESIGN AND SIMULATION RESULTS OF DIFFERENT CMOS CIRCUITS. This chapter gives a detailed description of the various design and their simulation results used in the development of low power CMOS circuits. The simulation results of various CMOS circuits operating in superthreshold conduction region and subthreshold conduction region are presented. The power dissipation analysis is done with the variations of both the supply voltage V_{dd} and power clock frequencies.

CHAPTER 5: LAYOUT DESIGN AND POST-LAYOUT SIMULATION RESULT. This chapter discusses the designs of different layouts for all the proposed structures, which are designed in Mentor Graphics IC Station TSMC 0.18 μm Technology and the Layout versus Schematic (LVS) program was executed to perform a comparison of the schematic to the physical layout.

CHAPTER 6: CONCLUSIONS AND FUTURE SCOPE OF WORK. This chapter summarizes all the work of this thesis and present the scope for the future related to this thesis work.

CHAPTER 2 SUBTHRESHOLD CONDUCTION FOR LOW POWER VLSI DESIGN

Rapid development of such portable systems as laptops, PDAs, digital wrist watches, pacemakers and cell phones require low power consumption and high density integrated circuits. So, the designing of digital circuits for achieving ultra low power is done by running the digital circuits in subthreshold conduction region. The incentive of operating is able to exploit the subthreshold leakage current as the operating drive current. The subthreshold current is exponentially related to gate voltage. This exponential relationship is expected to give an exponential reduction in power consumption, but also an exponential increase in delay [5]. So, we use the circuits operating in subthreshold conduction region where the power is main concern and large delay can be tolerated.

Hence, this chapter begins with an introduction to conduction regions of the circuits. It then explains the behavior of a transistor in the subthreshold region of operation. After that energy and power will be discussed.

2.1 CONDUCTION REGIONS OF A MOS TRANSISTOR

The conduction region of a transistor depends on the supply voltage at which it operates. As the supply voltage is reduced, the region of operation shifts from strong inversion to moderate inversion and finally to weak inversion. The strong inversion region, also known as the superthreshold regime, is characterized by large current drives and a supply voltage substantially above V_{th}, the threshold voltage of the transistor. The moderate inversion has lower current drives as compared to the superthreshold regime and an

operating voltage near to the V_{th}. The weak inversion region, also known as the subthreshold region, is characterized by small current drives and a supply voltage below V_{th} [9].

To understand the conduction in CMOS, a minimum sized NMOS transistor with a constant drain voltage V_{ds} of 1.8 V was simulated using Mentor Graphics IC Design Architect using standard TSMC 0.18 μm technology with ELDO simulator for different values of V_{gs} (Figure 2.1). Each of the CMOS I_d operation regions are labeled in the Figure 2.1. The current I_d has linear dependency in the strong inversion region while in the moderate inversion region it shows quadratic dependency. The current in the subthreshold region does not drop abruptly below $V_{gs} = V_{th}$, but actually decays exponentially, similar to BJT operation.

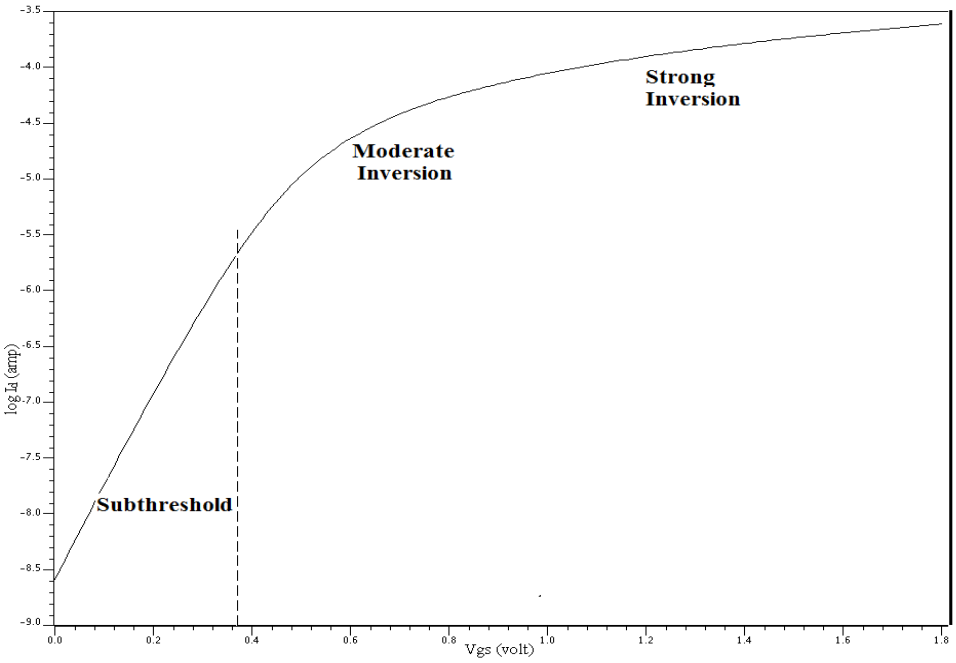

Figure 2.1: CMOS conduction regions for an NMOS with V_{ds} = 1.8 V and V_{gs} varying from 0 V to 1.8 V.

The effect of CMOS transistors conducting below the threshold voltage V_{th} is called subthreshold conduction. Unlike moderate and strong inversion, in which the drift component of current dominates, subthreshold conduction is dominated by diffusion current [9].

2.2 MODELLING SUBTHRESHOLD CURRENT

Subthreshold conduction current can be expressed by the following basic equation:

$$I_{on-sub} = I_0 \, exp\left(\frac{V_{gs}-V_{th}}{nV_T}\right) \tag{2.1}$$

Where I_0 is the drain current when V_{gs}= V_{th} given below:

$$I_0 = \mu_{eff} C_{ox} \frac{W}{L_{eff}} (n-1) V_T^2 \tag{2.2}$$

where W is the width of the transistor, L_{eff} is the effective length, μ_{eff} is the effective mobility, C_{ox} is the oxide capacitance, n is the subthreshold slope factor $\left(n = 1 + \frac{C_d}{C_{ox}}\right)$, V_{th} is the transistor threshold voltage and V_T is the thermal voltage,V_T =*(kT/q).*

As expected for diffusion current, equation (2.1) shows that I_{on-sub} depends exponentially on V_{gs} [10].

As it is clear that the transistor current I_{on-sub} in the subthreshold region is exponentially dependent on V_{th} and supply voltage V_{dd} due to which power, delay and current matching between two transistors is also exponentially dependent on V_{th} and V_{dd}. This exponential dependence is a key challenge in designing circuits in subthreshold. Some of the parameters that are affected by this challenge are process variations, noise margins, soft errors and output voltage swings. Therefore, when designing energy optimal subthreshold circuits, these parameters play an important role .

The current in the subthreshold region, also known as leakage current, is considered to be undesirable when operating the transistor in the superthreshold region. However, this current is quintessential as far as subthreshold operation is concerned. Leakage current is utilized by subthreshold circuits as their conduction current [11].

2.3 ADVANTAGES AND DRAWBACKS OF SUBTHRESHOLD OPERATION

The **advantages** of a circuit design approach that utilizes subthreshold conduction are [6]:

- Power is significantly lower [12].
- Device transconductance is an exponential function of V_{gs}, resulting in a high ratio of *on* to *off* current in a device stack. As a consequence, circuit noise margins are high.
- Delay gets worse, but the overall PDP (Power-Delay Product) improves [12]. It has been shown [17] that we can obtain an improvement in the Energy-Delay product as well, by operating the circuit in the near-subthreshold region.

The **disadvantages** of a sub-threshold design methodology are:

- I_D exhibits an exponential dependence on temperature, requiring circuitry to compensate for this effect.
- I_D is highly dependent on process variations. For example, small changes in V_{th} result in large changes in I_D due to the exponential dependence of I_D on V_{th} . We therefore require circuitry to compensate for this effect as well.

Techniques to dynamically compensate for the process, voltage and temperature dependence of the sub-threshold delay have been proposed [6].

2.4 POWER AND ENERGY IN DIGITAL CIRCUITS

Power refers to the number of Joules dissipated over a certain amount of time whereas energy is a measure of the total number of Joules dissipated by a circuit. Strictly speaking, low-power design is a different goal from low-energy design although they are related. Power is a problem primarily when cooling is a concern while energy is a problem when the bettery lifetime is to be maximized.

In other words, the energy (E) required for a given operation is the integral of the power (P) consumed over the operation time (T_D), hence,

$$E = \int_0^{T_D} P(t)\, dt \tag{2.3}$$

Here, the power of digital CMOS circuit is given by,

$$P = C_L\, V_{dd}\, V_s\, f \tag{2.4}$$

where, C_L is the capacitance being charged during a transition, V_{dd} is the supply voltage, V_s is the voltage swing of the signal, and *f* is the clock frequency. If it is assumed that an operation requires α clock cycles, T_D can be expressed as α / f. Hence, Equation (2.3) can be rewritten as:

$$E = \alpha\, C_L\, V_{dd}\, V_s \tag{2.5}$$

It is important to note that the energy per operation is independent of the clock frequency. Reducing the frequency will lower the power consumption but will not change the energy required to perform a given operation [4].

2.4.1 OVERVIEW OF TOTAL POWER CONSUMPTION

The total power in a CMOS circuit is given by Equation (2.6):

$$P_{Total} = P_{dynamic} + P_{static} = \frac{1}{2} C_L\, V_{dd}^2\, \alpha f + I_{SC}\, V_{dd} + I_{static}\, V_{dd} \tag{2.6}$$

where C_L is the load capacitance, *f* is the frequency of operation, I_{SC} is the short circuit current and α is the activity factor. As can be seen from Equation (2.6) the total power consists of two major components: dynamic power and leakage power. Both these components reduce in magnitude as the supply voltage reduces.

The dynamic power consumption is due to the charging and discharging of the load capacitance and the short circuit current. A short circuit current flows when the pull up and pull down networks in a CMOS circuit are simultaneously on and a direct path exists between the supply line and ground. Dynamic power is directly proportional to the square of the supply voltage. Therefore, dynamic power reduces in a quadratic manner when the supply voltage is reduced. Leakage power is dependent on the leakage current flowing in the CMOS circuit.

At superthreshold, the charging (or discharging) current is greater than the leakage current. Hence, dynamic power dominates over leakage power in superthreshold. At subthreshold, supply voltage is lower than the threshold voltage of the transistor. Due to its quadratic relation with supply voltage, dynamic power reduces drastically in subthreshold. Also, leakage current is regarded as the conduction current in subthreshold.

Therefore, leakage power dominates than dynamic power in the subthreshold region of operation [2].

2.4.2 TOTAL ENERGY DISSIPATION

Energy is one of the important design metrics in digital circuits. The energy estimation in these circuits is given by Equation (2.7):

$$E_{Total} = E_{dynamic} + E_{static} = \frac{1}{2} C_L V_{dd}^2 \alpha + I_{static} V_{dd} T_D \quad (2.7)$$

where C_L is the load capacitance, T_D is the circuit delay and α is the activity factor.

The important observation in Equation (2.7) is the dependence of leakage energy on delay T_D. Since T_D is high in subthreshold, the leakage energy is greater than the dynamic energy. As the supply voltage is increased, the delay and hence the leakage energy, reduces. Therefore, at superthreshold the dynamic energy is the more dominant of the two. Short circuit energy is negligible at subthreshold and can be ignored [2].

To understand the variation in power and frequency characteristics in superthreshold and subthreshold regions, simulations of a seven-stage ring oscillator using an inverter chain were performed in IBM 65 nm technology node [11]. The power and frequency characteristics of the ring oscillator are shown in Figure 2.2 and Figure 2.3, respectively.

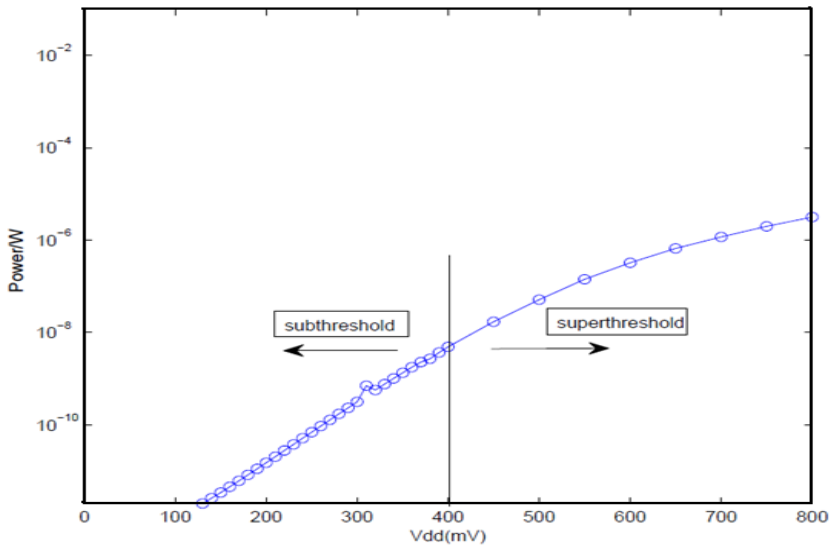

Figure 2.2: Ring oscillator power characteristics [11].

As can be observed from the graphs, both, power and frequency increase exponentially with supply voltage. With an increase in supply voltage from 200 mV to 700 mV, a 7000x increase in power and a 700x increase in frequency are observed. Thus, the advantage of low power in the subthreshold region comes at a cost of reduced speed of operation [11].

2.5 ENERGY POINT MINIMIZATION

Since energy minimization is the enabling factor for subthreshold design, identifying the operating voltage range for the optimal energy forms the design basis. Two commonly used terms in subthreshold design are V_{min} , the voltage at which the energy of the circuit is minimum and $V_{dd,limit}$, the lowest supply voltage at which the circuit can be operated. In most cases the V_{min} is greater than $V_{dd,limit}$. V_{min} denotes the ideal supply voltage at which the circuit should be operated. Stacking of transistors raises the $V_{dd,limit}$

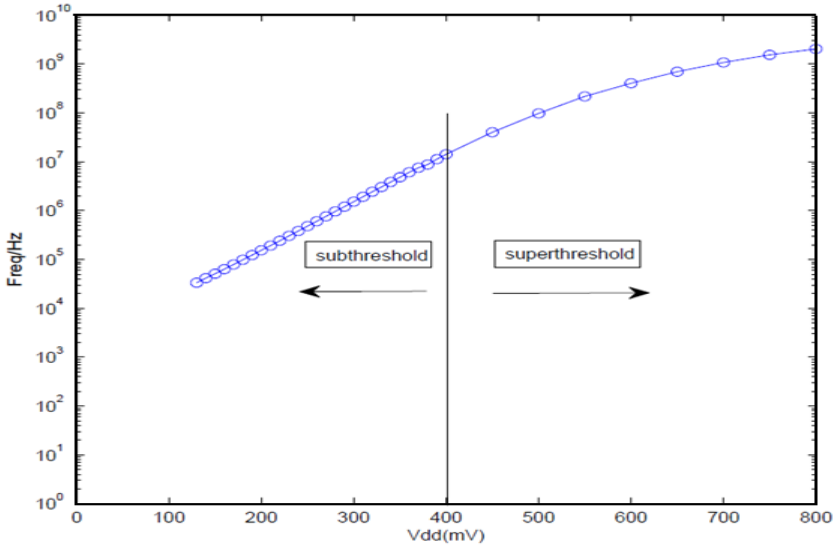

Figure 2.3: Ring oscillator frequency characteristics [11].

of a circuit well above that of a simple inverter. The location of the energy minimum of any circuit is a compromise between the dynamic and leakage energies. The point of intersection of the dynamic and leakage energy curves is defined as the minimum energy point of the circuit. The activity factor α, V_{th}, L_{eff} , subthreshold slope and I_{on} are interdependent and should be considered for determining the minimum energy point of any design [11].

2.6 DESIGNING OF DIFFERENT BASIC LOGIC GATES

This section describes the design of various digital logic gates in subthreshold. One of the primary reasons to design these logic gates is to use these gates as basic building blocks for larger circuits.

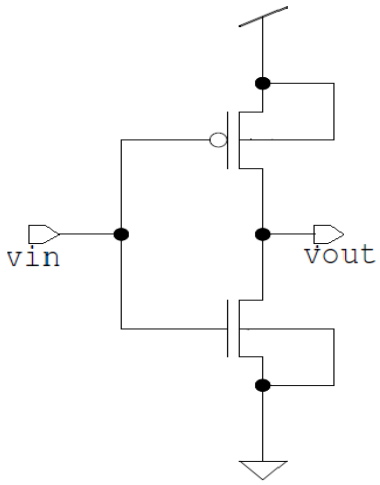

Figure 2.4: Basic CMOS Inverter.

First, the basic CMOS inverter, shown in Figure 2.4, is analyzed in detail and then, based on this analysis, the NAND and the NOR gates are designed and after that, other larger circuits can also be designed by calculating the values of *W/L* with the help of these *W/L* values of inverter which has been designed for symmetric output and equal charging and discharging current.

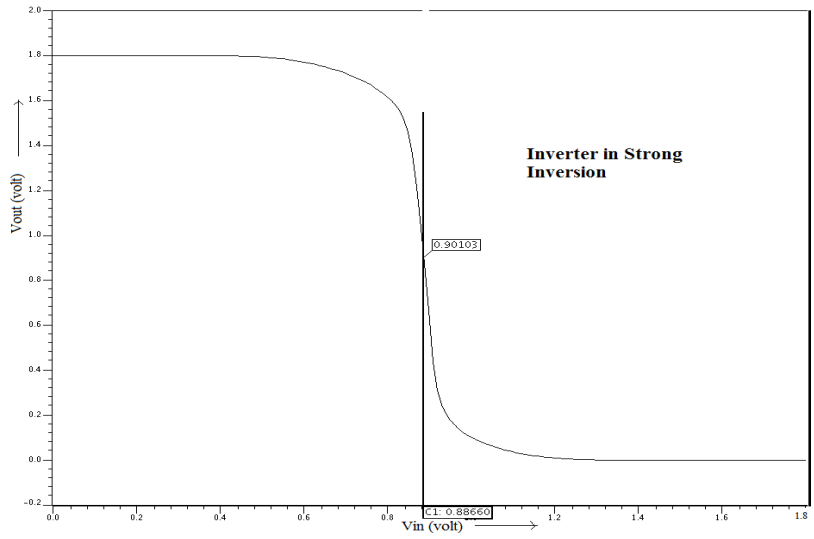

Figure 2.5: VTC curve of Inverter operating in strong inversion region.

By simulating this CMOS Inverter using Mentor Graphics IC Design Architect using standard TSMC 0.18 μm technology with ELDO simulator, the Inverter's value of *W/L* for PMOS = (1.2 μm/0.18 μm) and *W/L* for NMOS = (0.27 μm /0.18 μm) was obtained for strong inversion operation. While the Inverter's value of *W/L* for PMOS = (3.0 μm/0.18 μm) and *W/L* for NMOS = (0.27 μm /0.18 μm) was obtained for subthreshold operation.

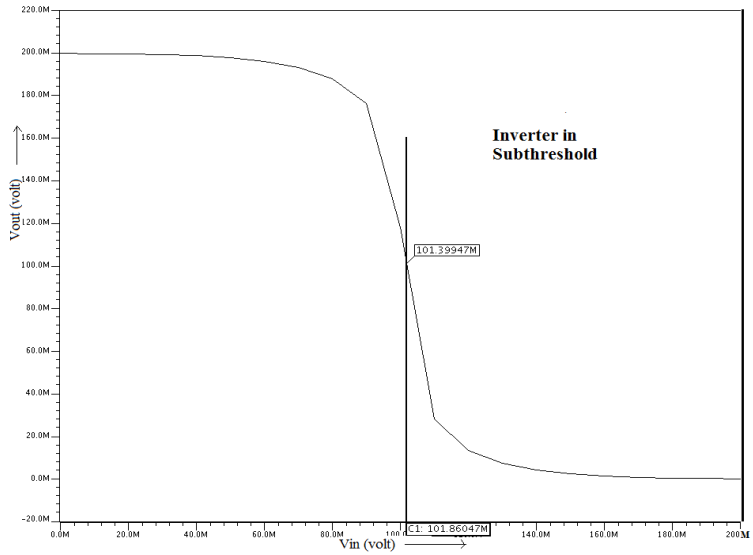

Figure 2.6: VTC curve of Inverter operating in Subthreshold region.

By using these values of *W/L* of basic Inverter, the larger circuits were designed having the equivalent *W/L* values equal to that of a basic Inverter.

CHAPTER 3 MATHEMATICAL ANALYSIS OF SUBTHRESHOLD CMOS INVERTER

In this chapter, we will discuss how to find the optimal value of supply voltage V_{dd} and also we will discuss the value to be applied at the input of a standard cell (CMOS Inverter) for minimum power consumption. So, first we discuss about the graphical method to find the optimal value of V_{dd}, after that we will discuss about the mathematical method to find the optimal value of V_{dd} [10].

3.1 ENERGY-PERFORMANCE CONTOURS FOR OPTIMAL V_{dd} & V_{th}

By examining the energy and delay contours for a simple circuit over supply voltage V_{dd} and threshold voltage V_{th} we show that minimum energy operation occurs in the subthreshold operation region. This optimum point changes with different activity factors and with threshold variation [10].

3.1.1 VARIABLE ACTIVITY FACTOR CIRCUIT

Simulations of a variable activity factor ring oscillator circuit demonstrate the optimal V_{dd} and V_{th} for CMOS circuits. The circuit consists of an 11-stage 2-input NAND ring oscillator (RO) (Figure 3.1). We define the performance as the simulated ring oscillator's frequency.

A variable activity factor is achieved by placing 9 additional delay chains in parallel which are driven by the ring oscillator and run at the same frequency. This circuit enables variable activity factor by changing the proportion of gates switching. The Select inputs to the delay chains can be used to "activate/deactivate" different delay chains. When all Select inputs are "high", the activity factor 1, (i.e. all nodes in the ring oscillator are switching during the clock period). However, in typical logic gates, the activity factor is rarely equal to 1. By setting one Select input to "low", then the corresponding, for example, by selecting Select0-Select4 "high" and Select5-Select9 "low", half of the gates are switching, while the other half is idle, and the activity factor is 1/2.

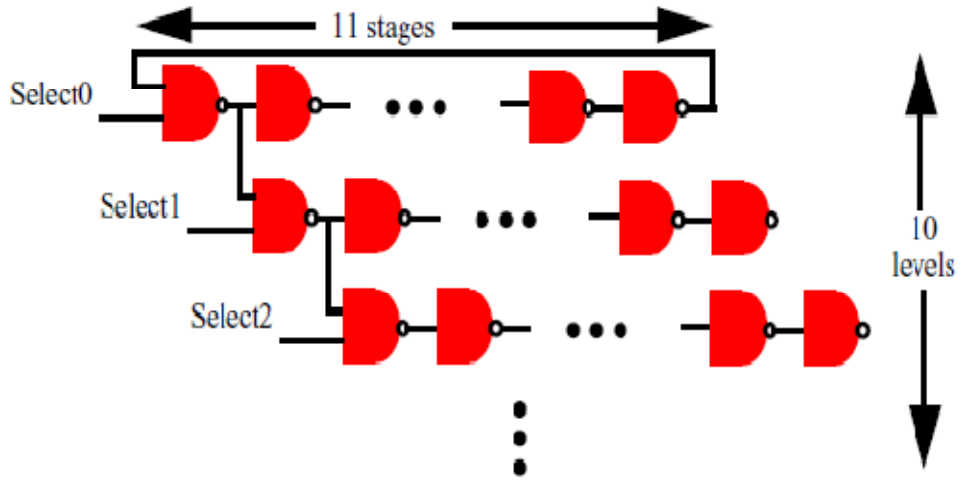

Figure 3.1: Circuit to show Energy and Performance in subthreshold region for variable activity factor [13].

As activity factor decreases, the switching energy also decreases, and total energy is dominated by leakage energy [13].

3.1.2 ENERGY AND PERFORMANCE CONTOURS

Simulations of the energy and performance variable activity factor ring oscillator circuit in Figure 3.1 are performed using BSIM3 models of a 0.18 μm process [14].

Simulations of the energy-performance variable activity factor ring oscillator circuit in a 0.18 μm process are shown in Figure 3.2. This shows constant normalized performance and energy curves for α = 1 (constant activity factor). The performance varies between

10 kHz and 100 MHz. In these simulations, V_{dd} varies from 0.1 V to 0.6 V, and the threshold voltage for both NMOS and PMOS varies from 0 V to 0.6 V. The combination

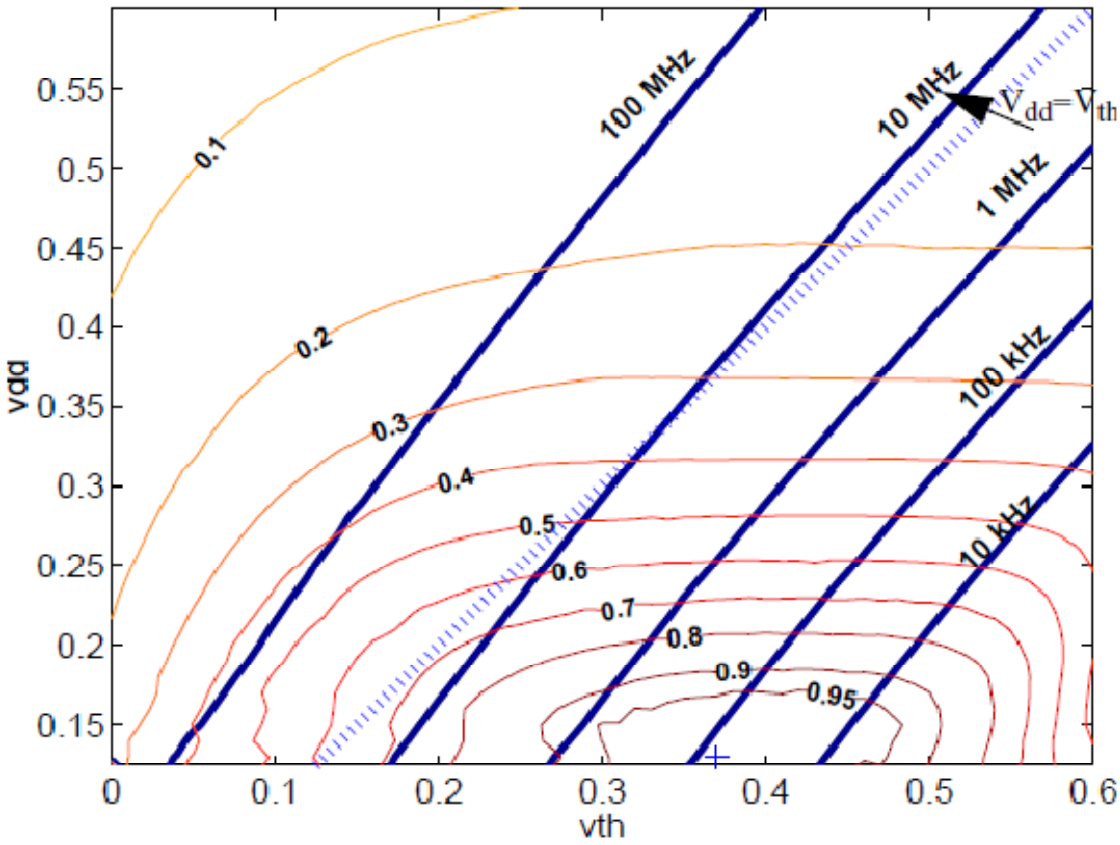

Figure 3.2: Minimum energy point and constant energy and performance contours of the variable activity factor circuit with α = 1 [13].

of V_{dd} and V_{th} for which the circuit consumes the least amount of energy is shown by the '+' mark in figure and occurs at $V_{dd,opt}$ = 130 mV and $V_{th,opt}$ = 370 mV. The straight thick lines are contours of constant performance. Also, the simulations show that at the line of "at-threshold" or V_{dd} = V_{th} (diagonal dotted line), the highest achievable performance is only 10 MHz. For applications which require clock frequencies lower than 10 MHz, operation in the subthreshold regime is suggested for minimal energy dissipation. The contours around the minimum energy point are constant normalized energy contours which is defined as:

$$\text{Normalized Energy} = (\text{min. Energy})/\text{Energy} \tag{3.1}$$

which is the inverse of energy normalized by the minimum energy point. For example, the line labeled 0.5, indicates the constant energy contour which is twice the minimum energy point.

The optimal V_{dd}-V_{th} operating points can be extracted from these curves, which is useful for circuit design. The optimal operating point is the V_{dd}-V_{th} which gives the minimum energy dissipated for a desired clock frequency. This point is where the performance curve is tangent to one of the energy curves [13].

The occurrence of a minimum energy point is due to the relationship between energy and latency at the given V_{dd} and V_{th}. At strong inversion supply voltages, switching energy dominates the total power. As V_{dd} is lowered from 1 V to 100 mV, a dramatic reduction of switching energy occurs because switching energy scales quadratically with supply voltage:

$$E_{dynamic} = \alpha\, C_L\, V_{dd}^2 \tag{3.2}$$

However, as the supply is reduced to sub-threshold voltage levels, the propagation delay increases exponentially. This leads to a corresponding exponential increase in leakage energy since the leakage current is accumulated over a longer period of time.

Mathematically, the minimum energy point occurs where the slopes of the leakage energy and active energy are equal in magnitude and opposite in sign [10].

3.2 MATHEMATICAL MODELLING FOR MINIMUM ENERGY CONSUMPTION

Although the energy contours provide good insight related to minimum energy operation, still a specific analysis of the minimum energy point is needed. This section describes an analytical model that supplies such an analysis. First, this section introduces a model of the MOSFET drain current in the subthreshold region. The current model serves as a basis for the minimum energy point analysis. The model that we develop for the minimum energy point allows quick estimation of important trends and the impact of key parameters on the system energy.

3.2.1 SUBTHRESHOLD LEAKAGE CURRENT MODELS

In subthreshold operation, the channel of the transistors is not inverted and current flows by diffusion. Equation (3.3) is a basic equation for modeling sub-threshold current and total off current.

$$I_{on-sub} = I_0 \, exp\left(\frac{V_{gs}-V_{th}}{nV_T}\right) \tag{3.3}$$

Equation (3.4) shows the same basic equation with low V_{ds} roll-off:

$$I_{on-sub} = I_0 \, exp\left(\frac{V_{gs}-V_{th}}{nV_T}\right)\left(1 - exp\left(\frac{-V_{ds}}{V_T}\right)\right) \tag{3.4}$$

Where I_0 is the drain current when V_{gs}= V_{th} given below:

$$I_0 = \mu_{eff} C_{ox} \frac{W}{L_{eff}} (n-1) V_T^2 \tag{3.5}$$

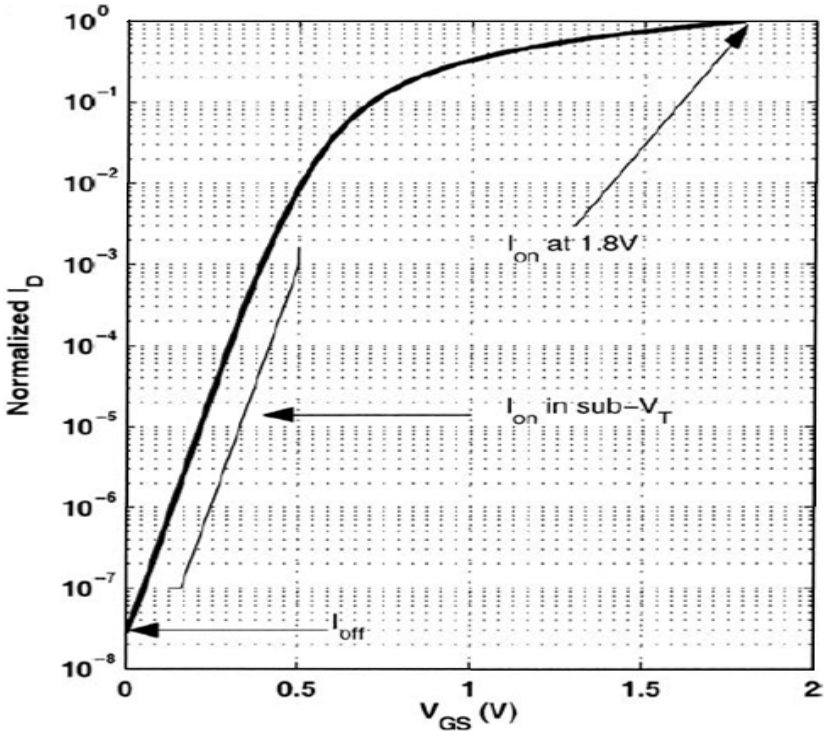

Figure 3.3: MOSFET I_D versus V_{gs} in 0.18 μm with V_{dd} = 1.8 V [10].

As expected for diffusion current, Equation (3.4) shows that I_{on-sub} depends exponentially on V_{gs}. Here, V_{th} is the transistor threshold voltage, n is the sub-threshold slope factor $\left(n = 1 + \frac{C_d}{C_{ox}}\right)$ and V_T is the thermal voltage, V_T =*(kT/q).* The parenthetical

term on the right models the roll-off in current that occurs when V_{ds} drops to within a few times V_T.

Figure 3.3 shows the drain current of a MOSFET versus its gate to source voltage V_{gs}, across the full range from 0 V to 1.8 V, which is V_{dd} for this 0.18 μm technology. At low values of V_{gs} in the subthreshold region, I_D varies exponentially with V_{gs} as expected. We define the threshold voltage V_{th}, by the point on the I_D versus V_{gs} plot where I_D ceases to depend exponentially on V_{gs}. This point occurs at around half a volt for the transistor in the Figure 3.3 .

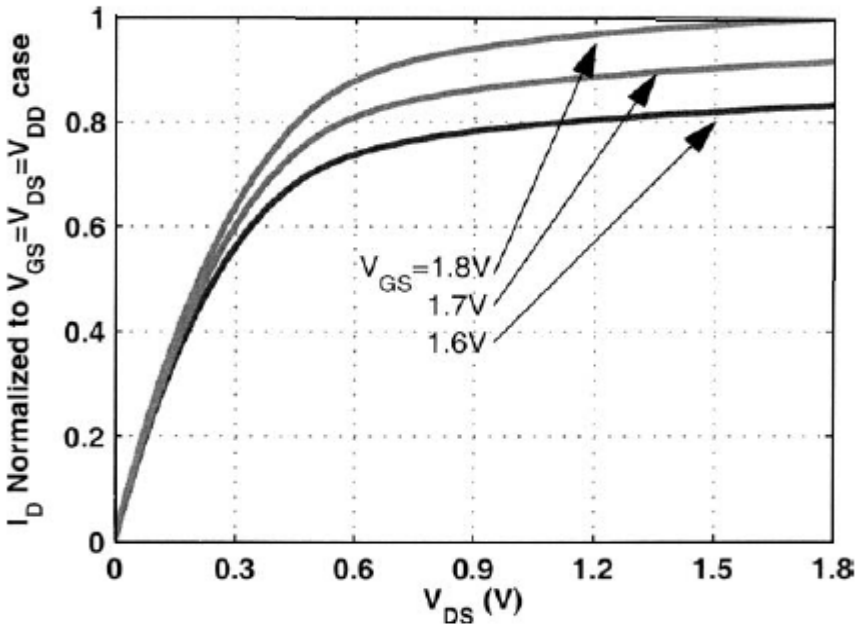

Figure 3.4: I_D versus V_{ds} curves of an Inverter for three values of V_{gs} in a 0.18 μm process with V_{dd} = 1.8 V [10].

Figure 3.4 shows standard I_D versus V_{ds} curves for strong inversion. The current in this plot clearly demonstrates the linear region and the velocity saturation region (not saturation, because I_D changes linearly with V_{gs} instead of quadratically). Figure 3.5 shows the same curves in subthreshold. The curves show the exponential dependence on V_{gs}, but they otherwise appear quite similar to the strong inversion curves in their shape. The 'quasi-linear' region comes from the roll-off of current at low V_{ds}, as seen in (3.4). Unlike strong inversion, the onset of this roll-off depends only on V_{ds} and not on V_{gs}. In strong inversion, the V_{ds} dependence in the velocity saturation region results from

channel length modulation and is commonly modeled with the Early voltage. In subthreshold, the V_{ds} dependence in the 'quasi-saturation' region results from DIBL and can be modeled with the DIBL coefficient as in equation given below [10]:

$$I_{on-sub} = I_0 \exp\left(\frac{V_{gs}-V_{th}+\eta V_{ds}}{nV_T}\right)\left(1-\exp\left(\frac{-V_{ds}}{V_T}\right)\right) \tag{3.6}$$

where, $\eta =$ drain induced barrier lowering (DIBL) coefficient.

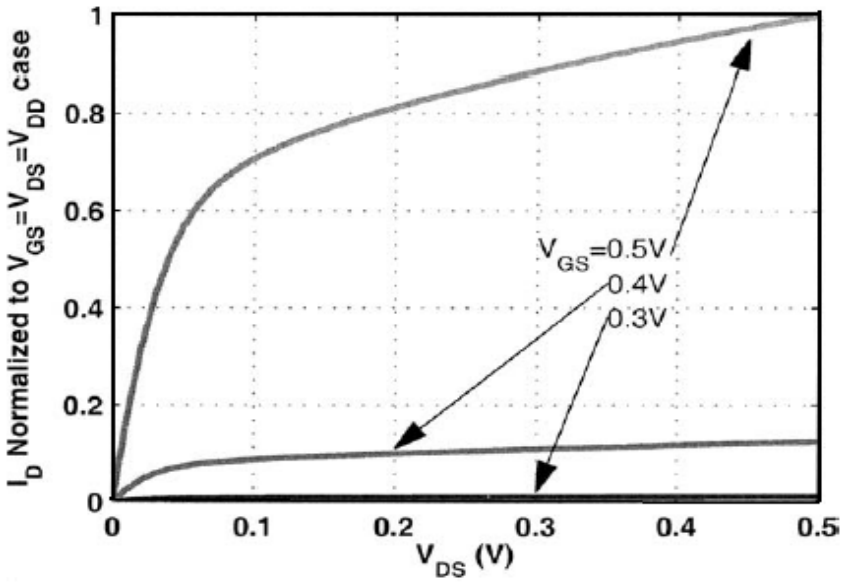

Figure 3.5: $I_D$versus V_{ds} curves for three values of V_{gs} in a 0.18 μm process, but V_{dd}= 500 mV, so the Inverter is in subthreshold region [10].

3.2.2 OTHER COMPONENTS OF LEAKAGE CURRENT

Subthreshold current is not the only type of leakage current that affects deep sub-micron transistors. This section briefly describes other types of leakage current and other subthreshold current effects and discusses their impact in the subthreshold region.

As technologies scale, the gate oxide gets progressively thinner. The higher resulting electrical field across the oxide enables carriers to tunnel through the oxide [9]. For subthreshold analysis, though, it is reasonable to ignore gate leakage because Gate tunneling current has a very strong dependence on the voltage across the gate, so it decreases with supply voltage much more quickly than does subthreshold current. As a

result, gate leakage becomes negligible in the subthreshold region except in rare cases[10].

Gate-Induced Drain Leakage (GIDL) is a leakage current that is generated at the edge of the drain and terminates in the body of the transistor. GIDL current appears for high V_{ds} values in combination with low V_{gs} [9]. On a semilog plot of I_D versus V_{gs}, GIDL appears as a "tail" where the current begins to increase when V_{gs} approaches 0 and continues to increase for negative V_{gs} . For subthreshold operation, the lower V_{ds} reduces the electric field across the drain such that GIDL becomes negligible.

DIBL occurs in short channel transistors because the depletion regions around the source and drain actually overlap slightly, lowering the source potential barrier increasing current [9]. As V_{ds} increases, the depletion region at the drain grows, further lowering the barrier due to larger overlap with the source depletion region and increasing current. The DIBL effect still impacts current in subthreshold, but the lower V_{ds} means that the impact is less than at strong inversion voltages.

Reverse biased diode leakage from the source and drain to the bulk also contributes to overall leakage current. This junction leakage results from a combination of minority carrier diffusion and drift at the depletion region edge and electron-hole pair generation inside the depletion region [9]. Process technologies generally are designed to make this PN-junction leakage small relative to subthreshold current. Since the junction leakage scales with V_{dd} and temperature in a similar fashion to subthreshold current, it is negligible across the full range of supply voltage.

Although these other components of current can be quite significant for normal strong inversion operation, they tend to be negligible in the subthreshold region. This allows us to equate total current in the subthreshold region to subthreshold current [10].

3.2.3 MINIMUM ENERGY POINT MODEL

In this section, we drive a closed form solution for the optimum V_{dd} and V_{th} for a given frequency and technology operating in the subthreshold region means ($V_{dd} < V_{th}$).

The equation given below shows the well known form of the delay of an inverter in (above threshold) strong inversion region :

$$t_d = \frac{K\, C_g\, V_{dd}}{(V_{dd} - V_{th})^2} \tag{3.7}$$

The denominator of this equation is the on current of the inverter in strong inversion i.e.

$$t_d = \frac{K\, C_g\, V_{dd}}{I_{on}} \tag{3.8}$$

We adopt the form of (3.8) for modeling the inverter in subthreshold. This equation shows the propagation delay of an inverter with output capacitance C_g in subthreshold:

$$t_d = \frac{K\, C_g\, V_{dd}}{I_{on-sub}} \tag{3.9}$$

In more detailed form, we can write this equation as :

$$t_d = \frac{K\, C_g\, V_{dd}}{I_0\, exp\left(\frac{V_{dd}-V_{th}}{nV_T}\right)\left(1-exp\,(\frac{-V_{ds}}{V_T})\right)} \tag{3.10}$$

Where I_0 is the drain current when V_{gs}= V_{th} given below:

$$I_0 = \mu_{eff} C_{ox} \frac{W}{L_{eff}} (n-1) V_T^2 \tag{3.11}$$

V_{th} = the transistor threshold voltage,

n = the sub-threshold slope factor $\left(n = 1 + \frac{C_d}{C_{ox}}\right)$,

V_T = the thermal voltage.

As with (3.7), K is a delay fitting parameter.

The exponential dependence of current on V_T and temperature results in large variations in delay across process and temperature corners. Although this large variation is a problem for certain types of systems, it is not the focus of this chapter.

Operational frequency is simply given by :

$$f = \frac{1}{t_d\, L_{DP}} \tag{3.12}$$

where L_{DP} is the depth of the critical path in characteristic inverter delays.

Thus, the total delay along the critical path of a circuit is :

$$T_D = \frac{1}{f} = t_d \, L_{DP} \tag{3.13}$$

Now, understanding the effects of CMOS in the subthreshold region in the previous sections is important since the minimum energy per operation point (MEP) of CMOS occurs in the subthreshold region. The total energy per operation of a digital circuit consists of two components: switching and leakage energy. The switching energy assuming rail-to-rail swing is:

$$E_{SW} = C_{eff} \, V_{dd}^2 \tag{3.14}$$

where C_{eff} is the average effective switched capacitance per operation.
The leakage energy is given by :

$$\begin{aligned} E_L &= I_{leak} \, V_{dd} T_D \\ &= W_{eff} I_0 \, exp\left(\frac{-V_{th}}{nV_T}\right) V_{dd} t_d L_{DP} \\ &= W_{eff} K C_g \, L_{DP} V_{dd}^2 exp\left(\frac{-V_{dd}}{nV_T}\right) \end{aligned} \tag{3.15}$$

The total energy per operation is then expressed as :

$$\begin{aligned} E_{Total} &= E_{SW} + E_L \\ &= V_{dd}^2 \left(C_{eff} + W_{eff} K C_g \, L_{DP} exp\left(\frac{-V_{dd}}{nV_T}\right) \right) \end{aligned} \tag{3.16}$$

Solving this set of above equations provides a good estimate of the optimum point and shows how the optimum point depends on the major parameters.

To define the V_{dd} at which the *minimum energy point* should occur, the derivative of (3.16) is taken with respect to V_{dd}, setting it equal to zero, and applying a number of rearrangements, we find :

$$\left(2 - \frac{V_{dd}}{nV_T}\right) exp(2 - \frac{V_{dd}}{nV_T}) = \frac{-2C_{eff}}{W_{eff}KC_g L_{DP}} exp(2) \quad (3.17)$$

Now according to Lambert function [15],

If $y = x . e^x$, then x = lambert W(y)

So, the analytical solution for $V_{dd,opt}$ from Equation (3.17) is given as:

$$V_{dd,opt} = nV_T \left(2 - \text{lambert W} \left(\frac{-2C_{eff}}{W_{eff}KC_g L_{DP}} exp\,(2)\right)\right) \quad (3.18)$$

Now, we know that,

$$f = \frac{1}{t_d L_{DP}}$$

By putting the value of $t_d$with $V_{dd} = V_{dd,opt}$ and then solving it, we find the optimum value of $V_{th} = V_{th,opt}$ for a given frequency f:

$$V_{th,opt} = V_{dd,opt} - nV_T \, log_e \left(\frac{fKC_g L_{DP} V_{dd,opt}}{I_0}\right) \quad (3.19)$$

If the argument to the natural log in (3.19) exceeds 1, then the assumption of subthreshold operation no longer holds because $V_{th,opt} < V_{dd,opt}$. This constraint shows that there is a maximum achievable frequency for a given circuit in the subthreshold region. Equations (3.18) and (3.19) give the optimum supply voltage and threshold voltage for subthreshold circuits consuming the minimum energy for a given frequency [10].

Assuming a standard technology where V_{th} is fixed, the problem becomes finding the optimum V_{dd} and frequency to minimize energy for a given design. The optimum V_{dd} for minimizing energy per cycle in this scenario still is given by (3.18), and the optimum frequency is given by (3.12) at $V_{dd} = V_{dd,opt}$ [10].

Swanson and Meindl devised a charge based model for the inverter to account for static or "off " current and used this model to analyze the Voltage Transfer Characteristic (VTC) of the inverter and showed that the inverter operation could be simulated down to 100 mV [16]. The VTC curve for different supply voltages are shown in Figure (3.6). To

find the minimum voltage, Swanson equated the *off* current of NMOS and PMOS and calculated the inverter gain in subthreshold. Since an inverter must have sufficient gain at $V_{dd}/2$, the minimum voltage which can be used was estimated to be 8*(kT/q)* or 0.2 V [16].

Hence, the designing for all the circuits in this thesis will be done for the supply voltage equal to 0.2 V.

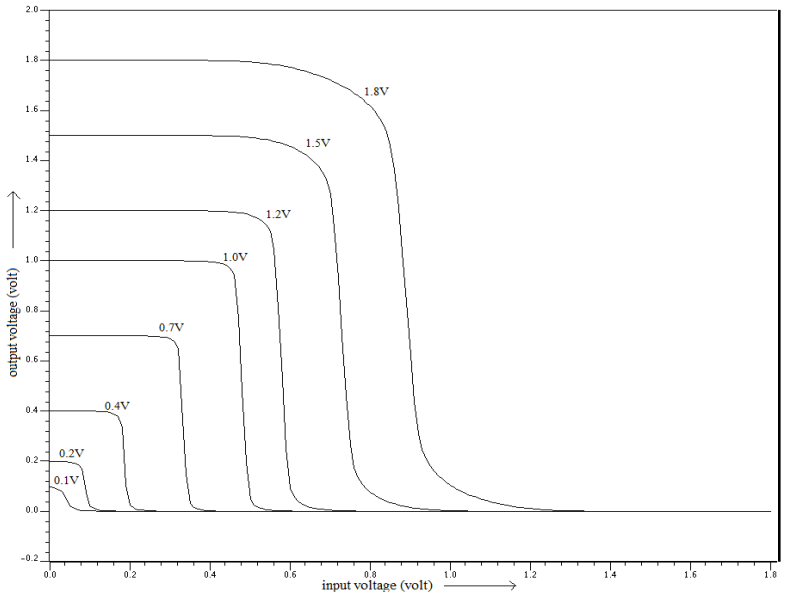

Figure 3.6: Inverter VTC showing operation down to 100 mV in a 0.18 μm process.

CHAPTER 4 DESIGN AND SIMULATION RESULTS OF DIFFERENT CMOS CIRCUITS

All the designs are implemented using standard TSMC 0.18 μm CMOS technology and simulated with ELDO simulator at an operating temperature of 27^{o} C. Mentor Graphics Corporation based tool known as IC Design Architect have been used for all the design and analysis. 1.8 V supply voltage was used for circuits operating in superthreshold conduction region while 0.2 V supply voltage was used for circuits operating in subthreshold conduction region. Different basic cells, for example, Inverter, Two-Input NAND Gate, Two-Input NOR Gate, Two-Input AND Gate, Two-Input XOR Gate, Three-Input AND Gate, Three-Input OR Gate, 2:1 MUX, Half Adder, One-Bit Full Adder are designed and analyzed after that a Two-Bit Multiplier is designed.

4.1 DESIGN AND SIMULATION RESULT FOR A CMOS INVERTER

The CMOS Inverter is the basic building block for any circuit implementation in VLSI designing. So, this chapter also starts with the designing of the basic CMOS Inverter of minimum transistor size. The standard TSMC 0.18 μm CMOS technology has been used for this design. Here, both Inverters, designed for superthreshold conduction region and subthreshold conduction will be discussed. The basic structure of a CMOS Inverter is shown in Figure 4.1.

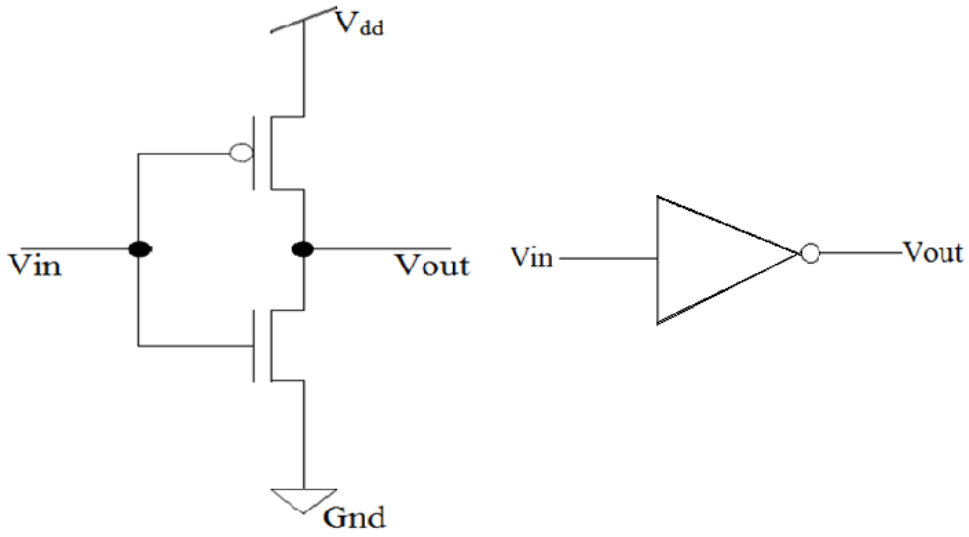

Figure 4.1: The Basic Structure of CMOS Inverter.

4.1.1 CMOS INVERTER OPERATING IN SUPERTHRESHOLD CONDUCTION REGION

The supply voltage used for this Inverter is 1.8 V and load capacitance is 5 *fF*. The simulation is done by use of ELDO Simulator of Mentor Graphics Corporation. The V_{gs}-I_d curve for this inverter is shown in Fugure 4.2.

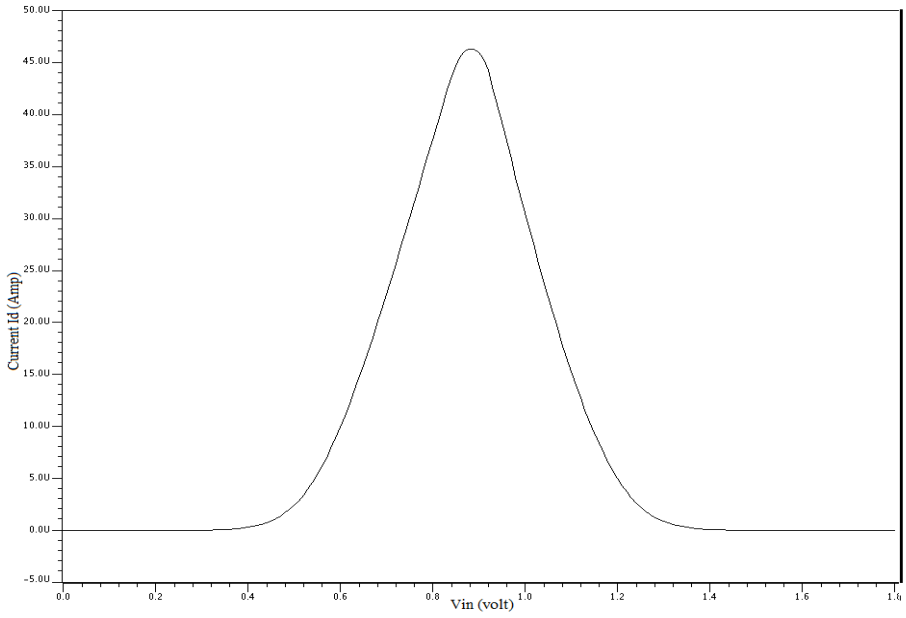

Figure 4.2: Current variation with input voltage in superthreshold conduction region.

The simulation result of transient analysis is shown in Figure 4.3.

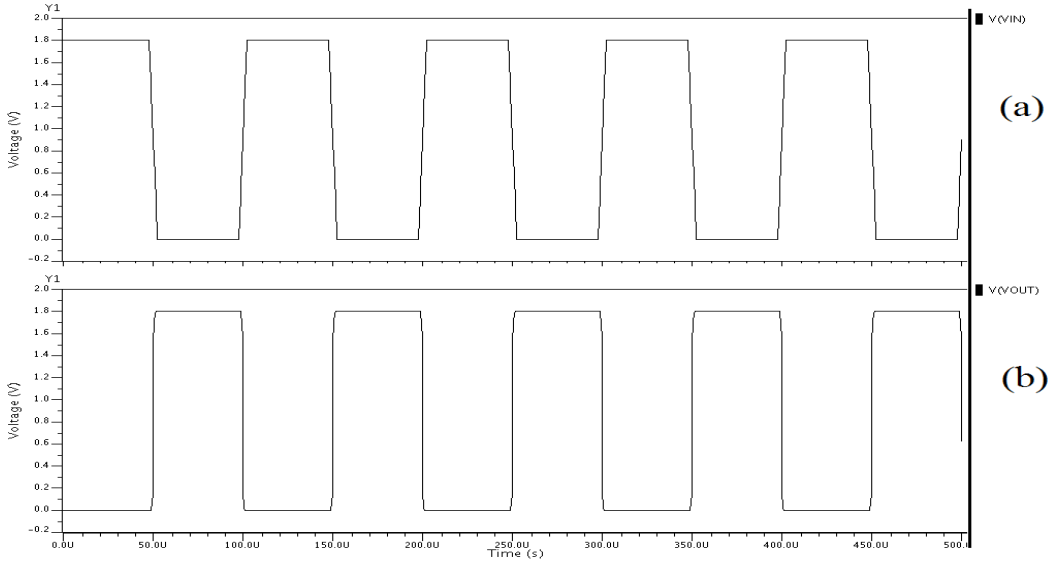

Figure 4.3: Simulation result of transient analysis for CMOS Inverter in superthreshold conduction region:
(a) Input Signal,
(b) Voltage Waveform of Output Signal.

4.1.2 CMOS INVERTER OPERATING IN SUBTHRESHOLD CONDUCTION REGION

The supply voltage used for this Inverter is 0.2 V and load capacitance is 11 fF. The V_{gs}-I_d curve for this inverter is shown in Fugure 4.4.

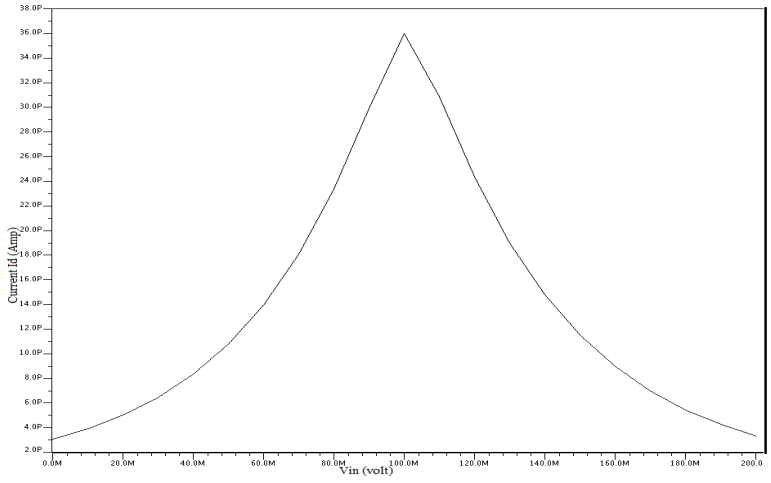

Figure 4.4: Current variation with input voltage in subthreshold conduction region.

The simulation result of transient analysis is shown in Figure 4.5.

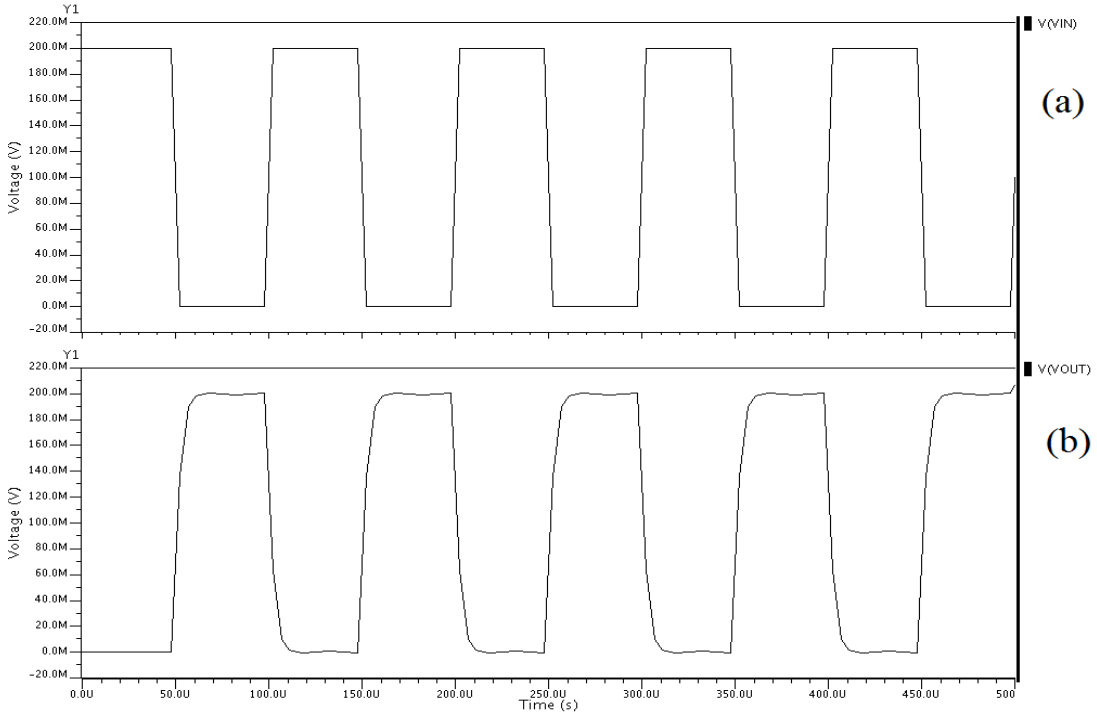

Figure 4.5: Simulation result of transient analysis for CMOS Inverter in subthreshold conduction region:
(a) Input Signal,
(b) Voltage Waveform of Output Signal.

4.2 DESIGN AND SIMULATION RESULT FOR A TWO-INPUT CMOS NAND GATE

Two-Input CMOS NAND Gate can also be designed having the minimum size as the equivalent *W/L* of this NAND Gate is the same as that of the Inverter. This has been designed and simulated in standard TSMC 0.18 μm CMOS technology. The basic structure of a Two-Input NAND Gate is shown in Figure 4.6.

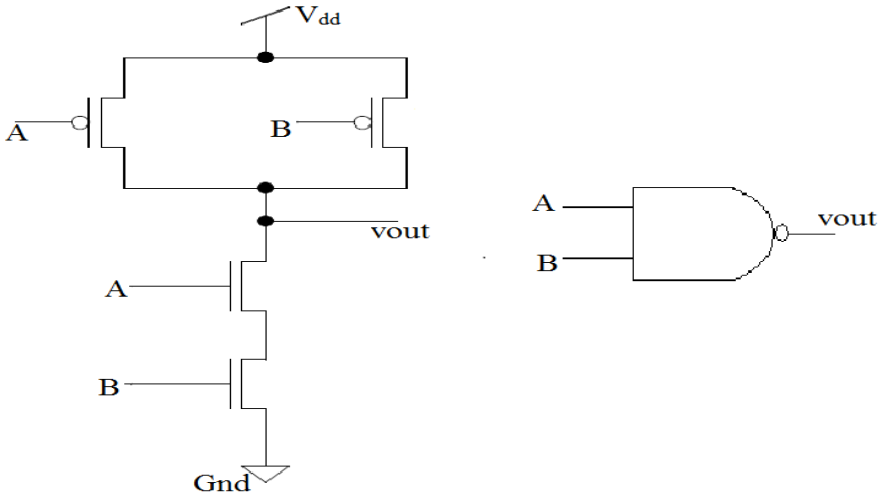

Figure 4.6: Basic Structure of a Two-Input CMOS NAND Gate.

4.2.1 TWO-INPUT CMOS NAND GATE OPERATING IN SUPERTHRESHOLD CONDUCTION REGION

The supply voltage used for this Two-Input CMOS NAND Gate is 1.8 V and load capacitance is 10 *fF*. The simulation result of transient analysis is shown in Figure 4.7.

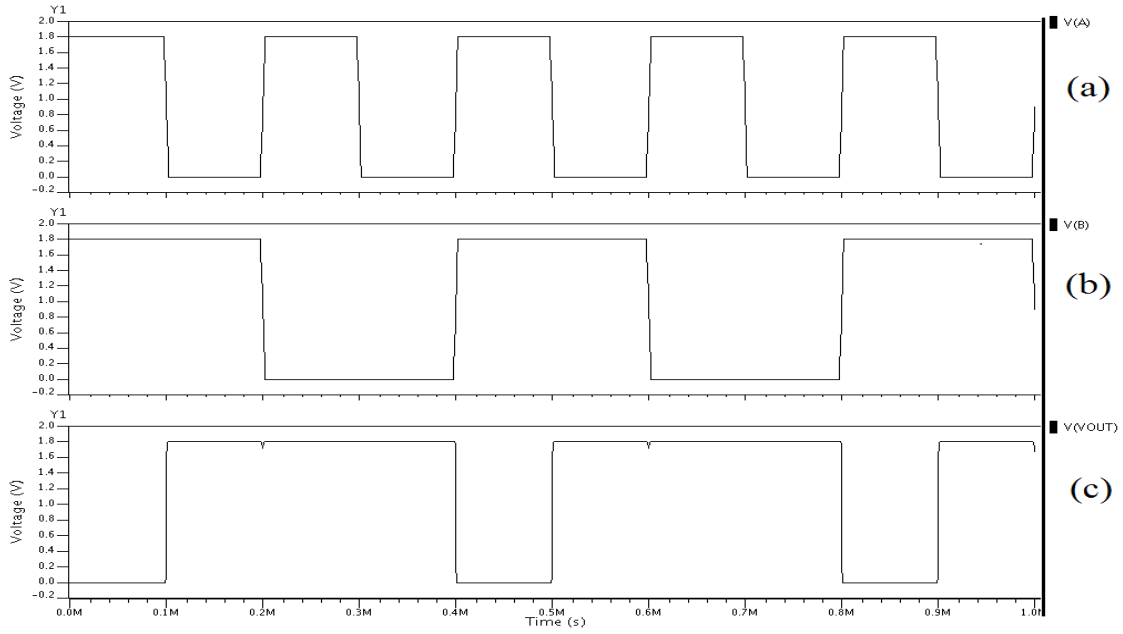

Figure 4.7: Simulation result of Two-Input CMOS NAND Gate in superthreshold conduction region:
(a) Input Signal (A), (b) Input Signal (B),
(c) Voltage Waveform of Output Signal (VOUT).

4.2.2 TWO-INPUT CMOS NAND GATE OPERATING IN SUBTHRESHOLD CONDUCTION REGION

The supply voltage used for this Two-Input CMOS NAND Gate is 0.2 V and load capacitance is 18 *fF*. The simulation result of transient analysis is shown in Figure 4.8.

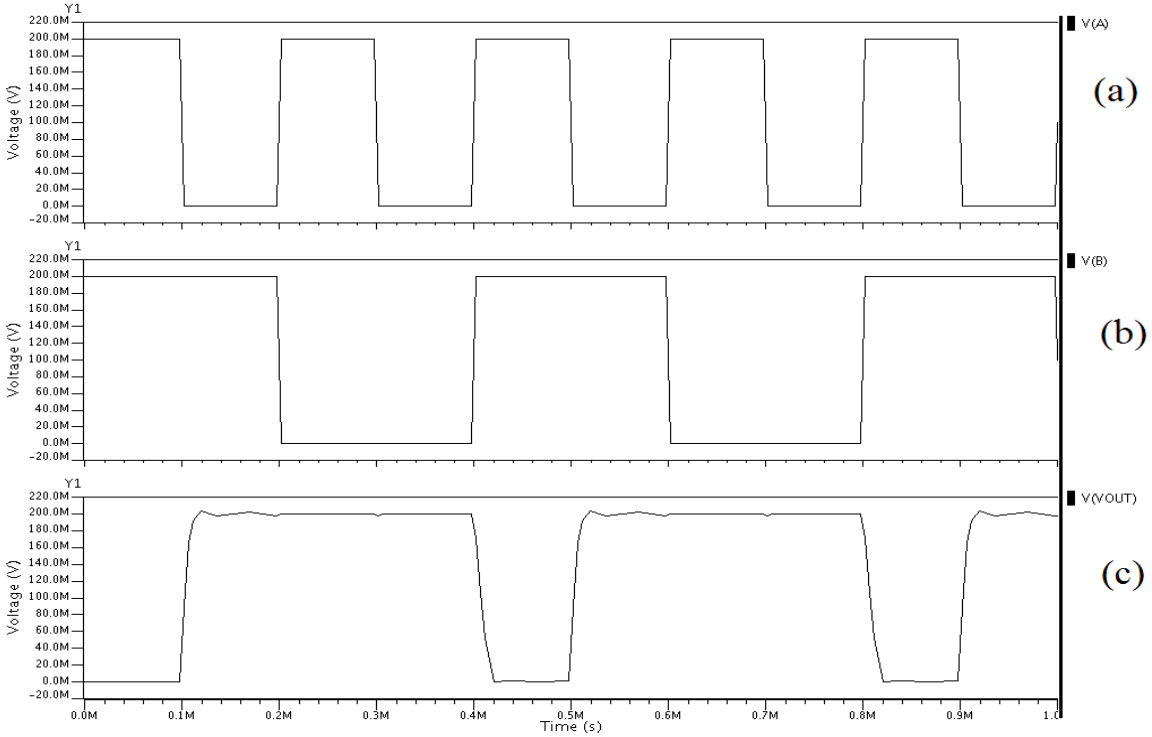

Figure 4.8: Simulation result of Two-Input CMOS NAND Gate in subthreshold conduction region:
(a) Input Signal (A), (b) Input Signal (B),
(c) Voltage Waveform of Output Signal (VOUT).

4.3 DESIGN AND SIMULATION RESULT FOR A TWO-INPUT CMOS NOR GATE

Two-Input CMOS NOR Gate can also be designed having the minimum size as, the equivalent *W/L* of this NOR Gate is the same as that of the Inverter. This has been designed and simulated in standard TSMC 0.18 μm CMOS technology. The basic structure of a Two-Input NOR Gate is shown in Figure 4.9.

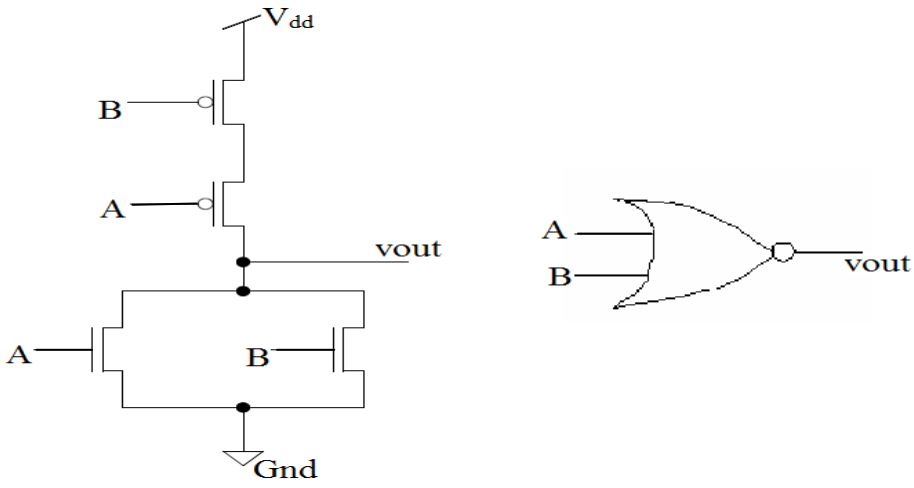

Figure 4.9: Basic Structure of a Two-Input CMOS NOR Gate.

4.3.1 TWO-INPUT CMOS NOR GATE OPERATING IN SUPERTHRESHOLD CONDUCTION REGION

The supply voltage used for this Two-Input CMOS NOR Gate is 1.8 V and load capacitance is 12 *fF*. The simulation result of transient analysis is shown in Figure 4.10.

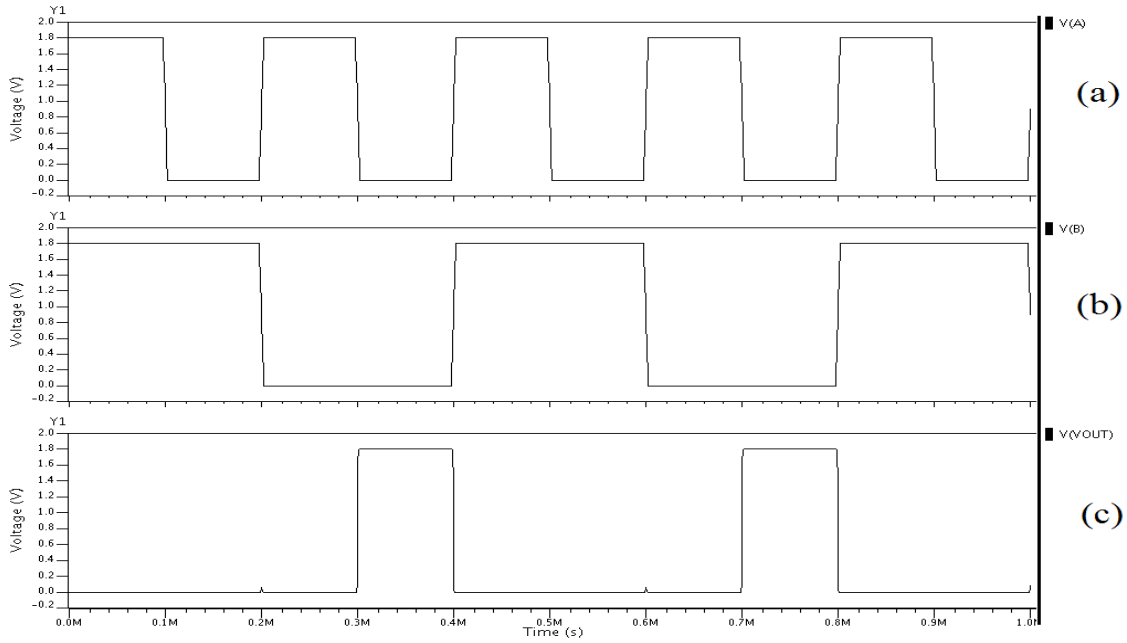

Figure 4.10: Simulation result of Two-Input CMOS NOR Gate in superthreshold conduction region:
(a) Input Signal (A), (b) Input Signal (B),
(c) Voltage Waveform of Output Signal (VOUT).

4.3.2 TWO-INPUT CMOS NOR GATE OPERATING IN SUBTHRESHOLD CONDUCTION REGION

The supply voltage used for this Two-Input CMOS NOR Gate is 0.2 V and load capacitance is 30 *fF*. The simulation result of transient analysis is shown in Figure 4.11.

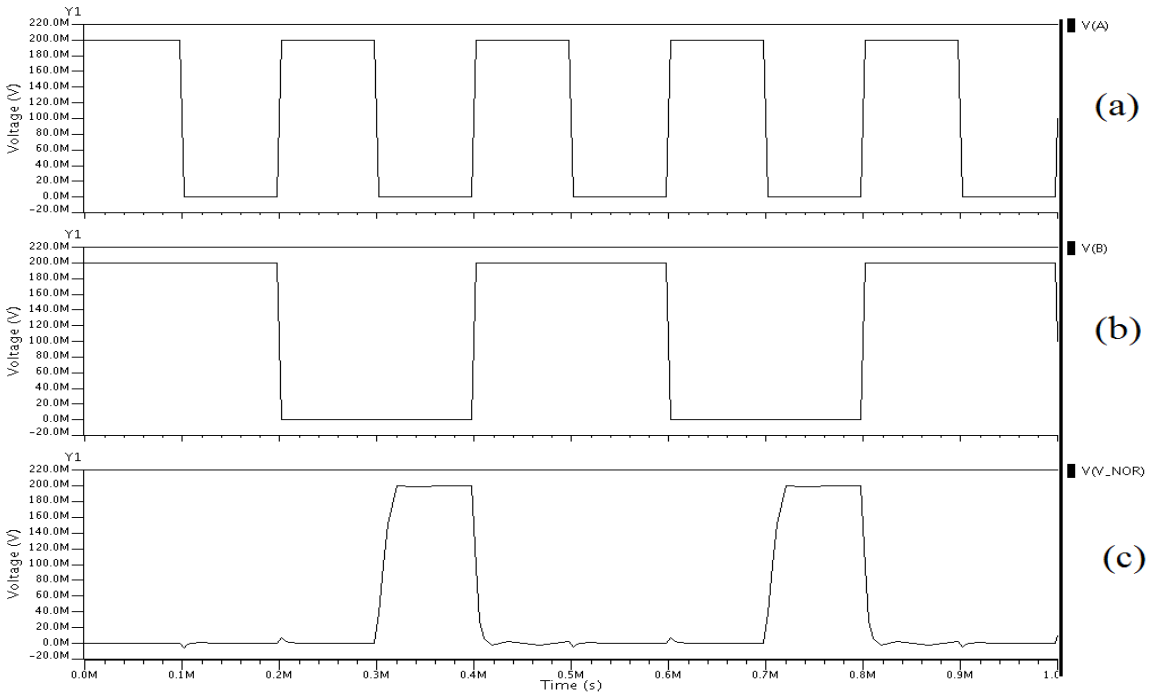

Figure 4.11: Simulation result of Two-Input CMOS NOR Gate in subthreshold conduction region:
(a) Input Signal (A), (b) Input Signal (B),
(c) Voltage Waveform of Output Signal (V_NOR).

4.4 DESIGN AND SIMULATION RESULT FOR A TWO-INPUT CMOS AND GATE

The basic structure of minimum sized Two-Input CMOS AND Gate is shown below in Figure 4.12 which has been designed using standard TSMC 0.18 μm CMOS technology and simulated using ELDO simulator.

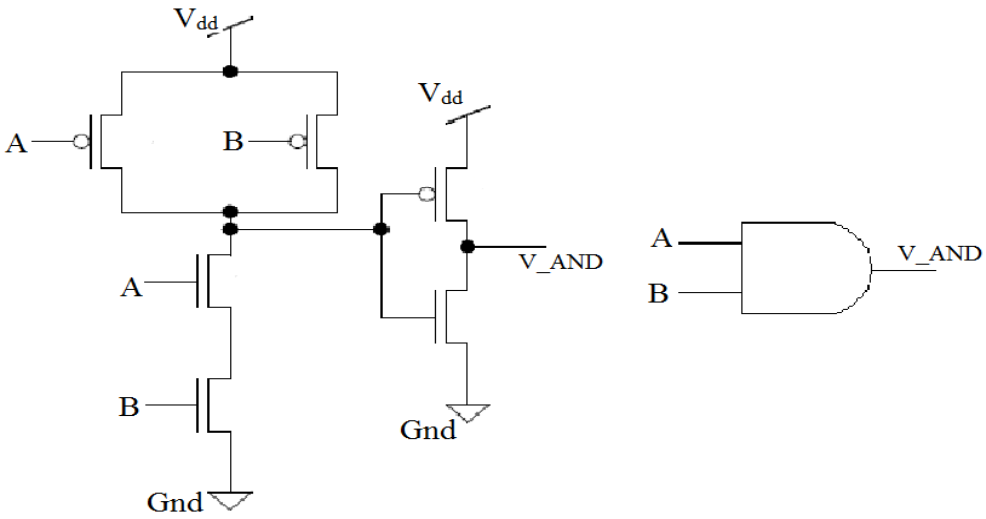

Figure 4.12: Basic Structure of a Two-Input CMOS AND Gate.

4.4.1 TWO-INPUT CMOS AND GATE OPERATING IN SUPERTHRESHOLD CONDUCTION REGION

The supply voltage used for this Two-Input CMOS AND Gate is 1.8 V and load capacitance is 5 *fF*. The simulation result of transient analysis is shown in Figure 4.13.

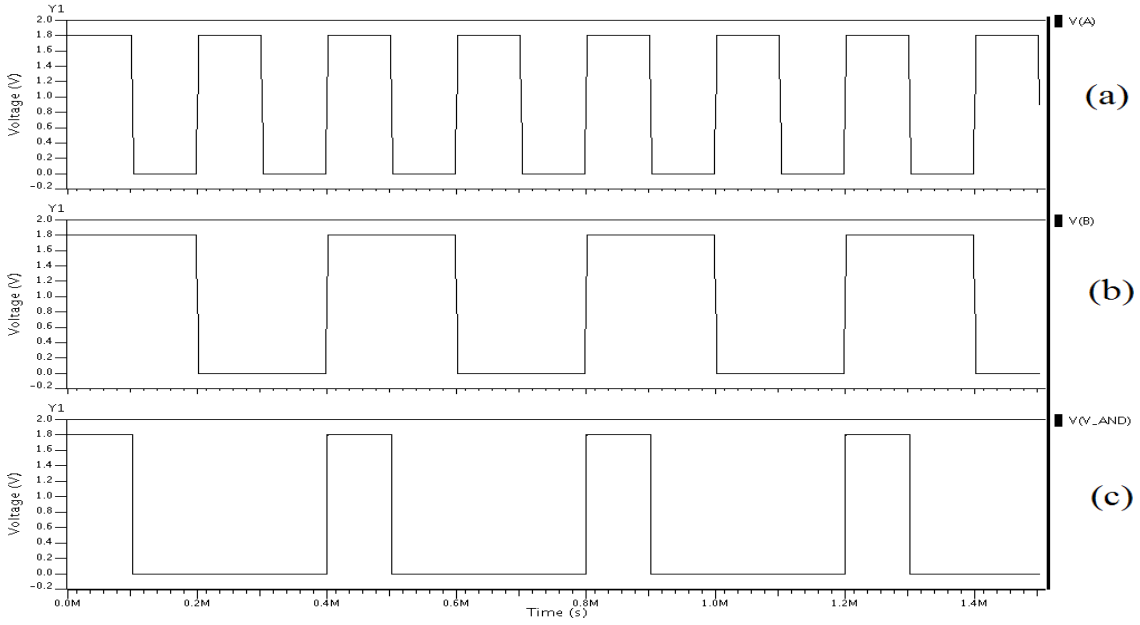

Figure 4.13: Simulation result of Two-Input CMOS AND Gate in superthreshold conduction region:
(a) Input Signal (A), (b) Input Signal (B),
(c) Voltage Waveform of Output Signal (V_AND).

4.4.2 TWO-INPUT CMOS AND GATE OPERATING IN SUBTHRESHOLD CONDUCTION REGION

The supply voltage used for this Two-Input CMOS AND Gate is 0.2 V and load capacitance is 11 *fF*. The simulation result of transient analysis is shown in Figure 4.14.

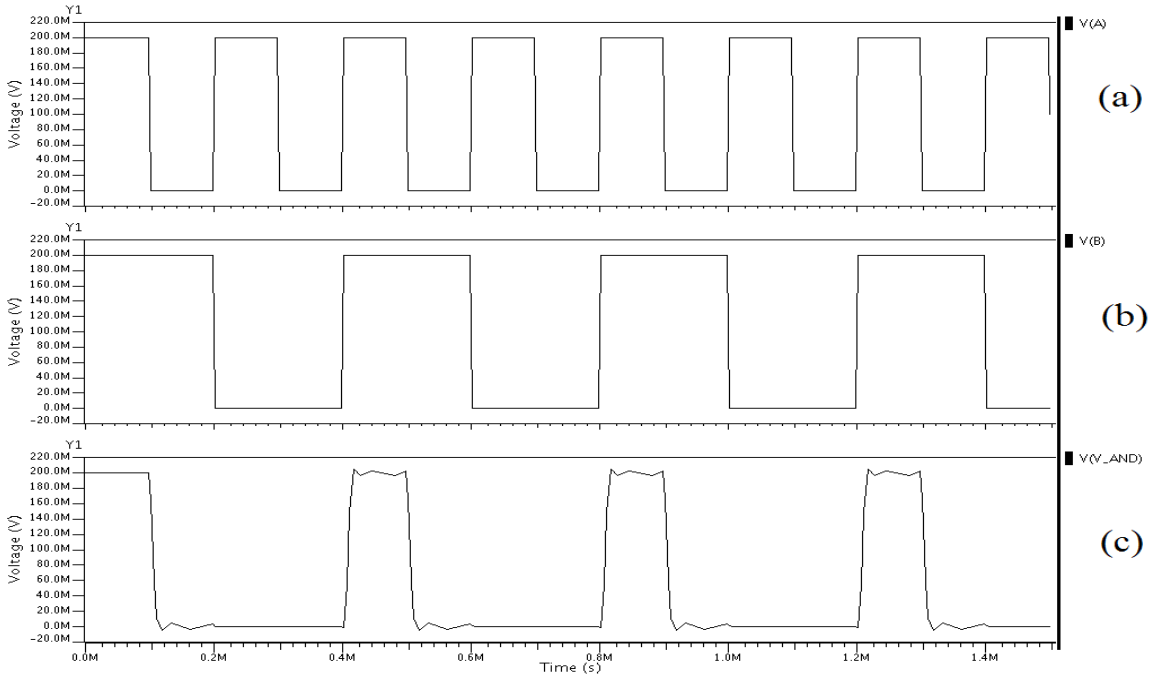

Figure 4.14: Simulation result of Two-Input CMOS AND Gate in subthreshold conduction region:
(a) Input Signal (A), (b) Input Signal (B),
(c) Voltage Waveform of Output Signal (V_AND).

4.5 DESIGN AND SIMULATION RESULT FOR A TWO-INPUT CMOS XOR GATE

The basic structure of minimum sized Two-Input CMOS XOR Gate is shown below in Figure 4.15 which has been designed using standard TSMC 0.18 μm CMOS technology and simulated using ELDO simulator.

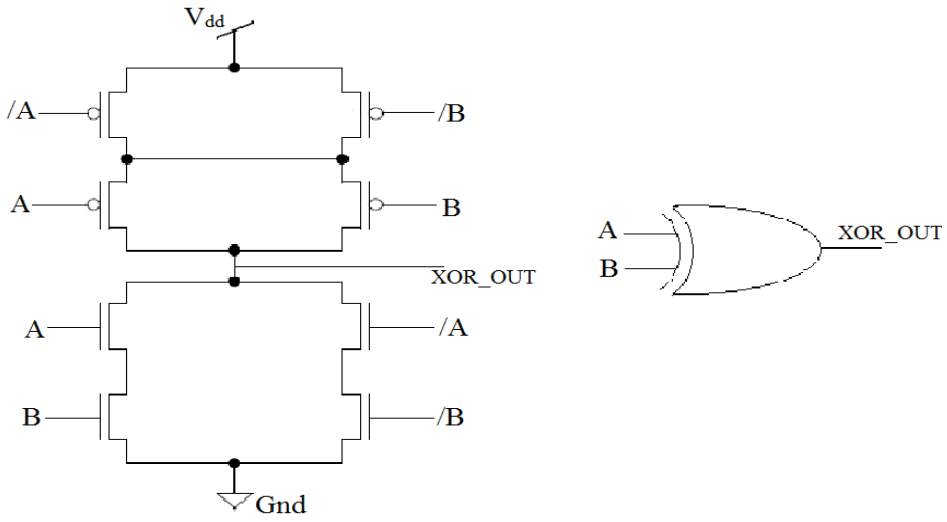

Figure 4.15: Basic Structure of a Two-Input CMOS XOR Gate.

4.5.1 TWO-INPUT CMOS XOR GATE OPERATING IN SUPERTHRESHOLD CONDUCTION REGION

The supply voltage used for this Two-Input CMOS XOR Gate is 1.8 V and load capacitance is 12 *fF*. The simulation result of transient analysis is shown in Figure 4.16.

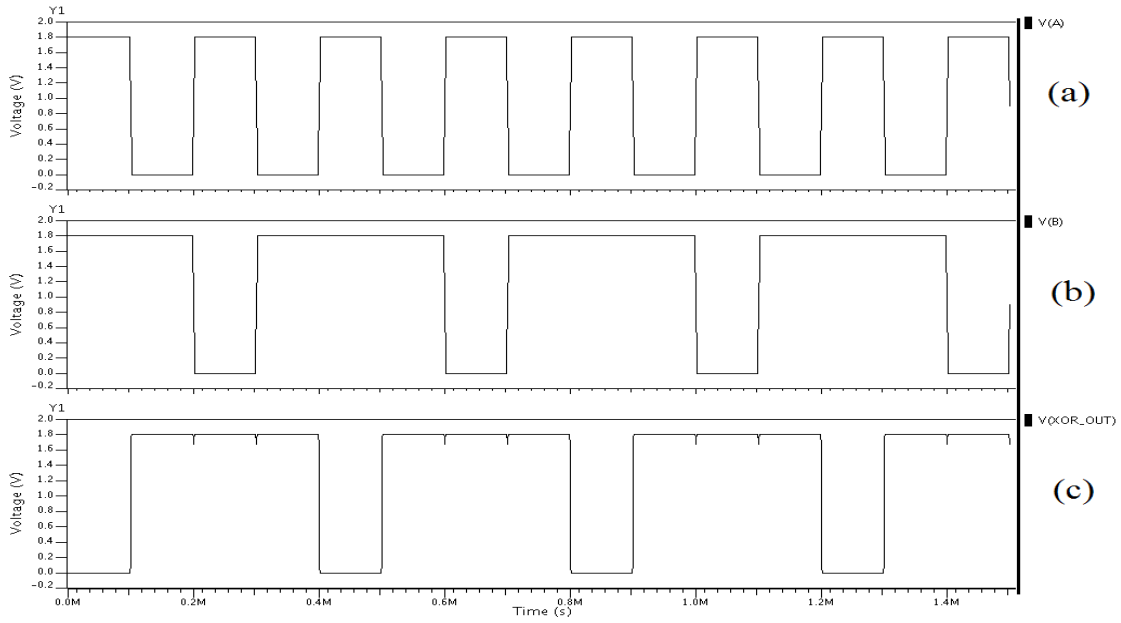

Figure 4.16: Simulation result of Two-Input CMOS XOR Gate in superthreshold conduction region:
(a) Input Signal (A), (b) Input Signal (B),
(c) Voltage Waveform of Output Signal (XOR_OUT).

4.5.2 TWO-INPUT CMOS XOR GATE OPERATING IN SUBTHRESHOLD CONDUCTION REGION

The supply voltage used for this Two-Input CMOS XOR Gate is 0.2 V and load capacitance is 25 *fF*. The simulation result of transient analysis is shown in Figure 4.17.

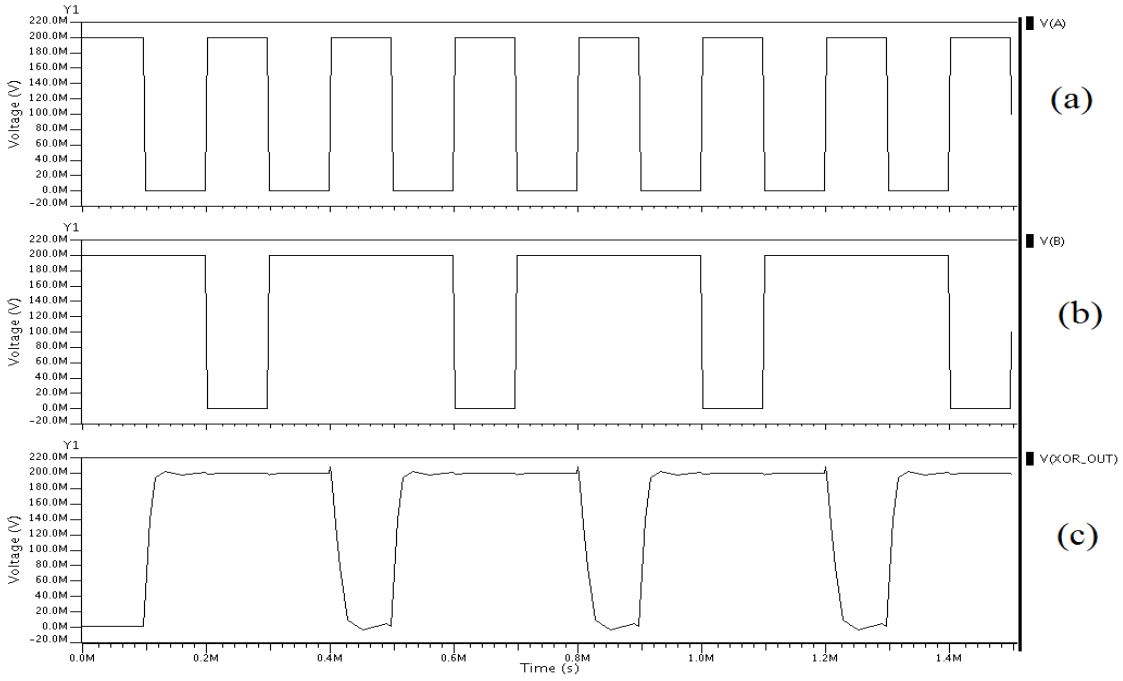

Figure 4.17: Simulation result of Two-Input CMOS XOR Gate in subthreshold conduction region:
(a) Input Signal (A), (b) Input Signal (B),
(c) Voltage Waveform of Output Signal (XOR_OUT).

4.6 DESIGN AND SIMULATION RESULT FOR A THREE-INPUT CMOS AND GATE

The minimum sized Three-Input CMOS AND Gate, designed using standard TSMC 0.18 μm CMOS technology is shown in Figure 4.18. This has been simulated using ELDO simulator.

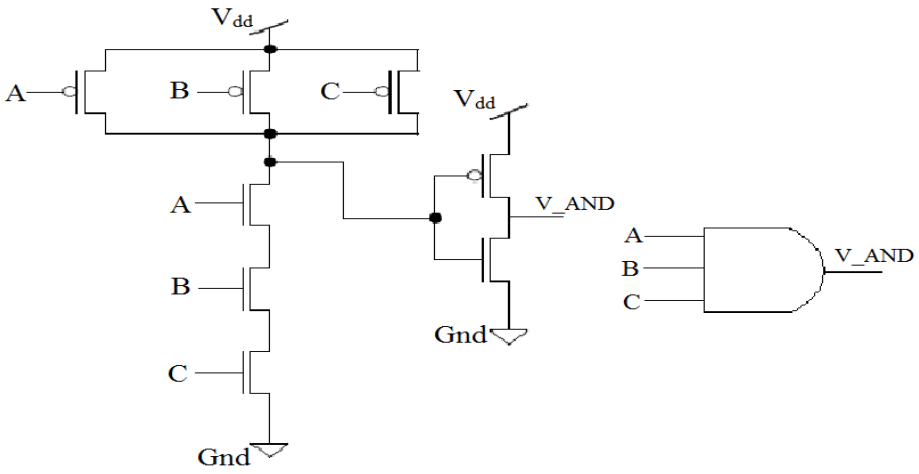

Figure 4.18: Basic Structure of a Three-Input CMOS AND Gate.

4.6.1 THREE-INPUT CMOS AND GATE OPERATING IN SUPERTHRESHOLD CONDUCTION REGION

The supply voltage used for this Three-Input CMOS AND Gate is 1.8 V and load capacitance is 5 *fF*. The simulation result of transient analysis is shown in Figure 4.19.

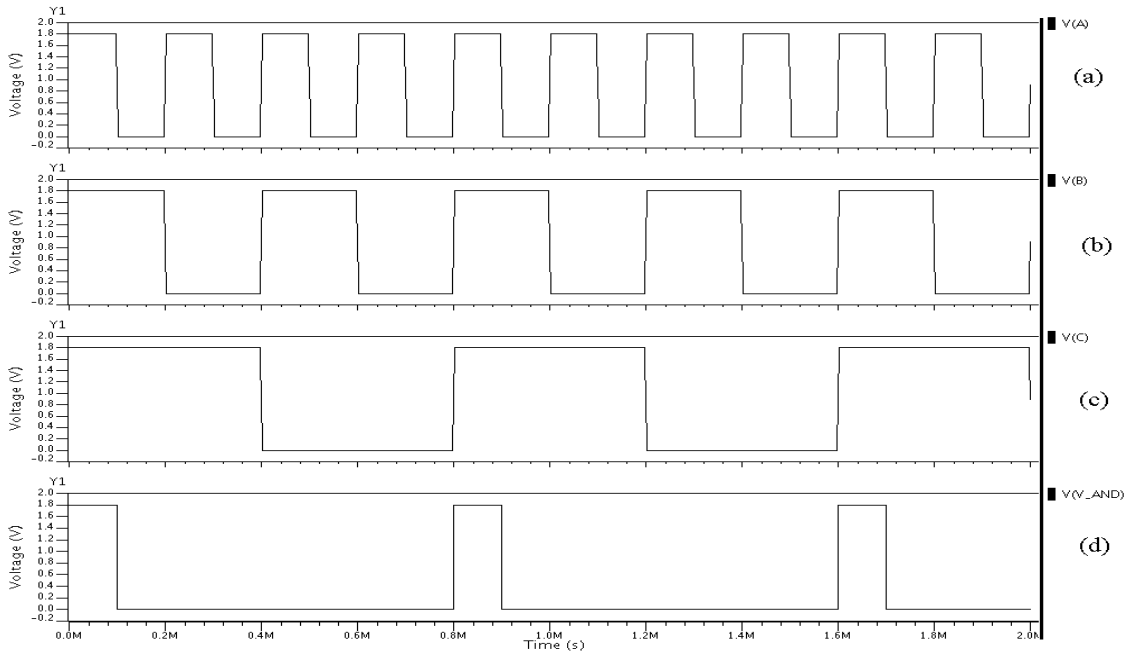

Figure 4.19: Simulation result of Three-Input CMOS AND Gate in superthreshold conduction region:
(a) Input Signal (A), (b) Input Signal (B), (c) Input Signal (C), (d) Voltage Waveform of Output Signal (V_AND).

4.6.2 THREE-INPUT CMOS AND GATE OPERATING IN SUBTHRESHOLD CONDUCTION REGION

The supply voltage used for this Three-Input CMOS AND Gate is 0.2 V and load capacitance is 11 *fF*. The simulation result of transient analysis is shown in Figure 4.20.

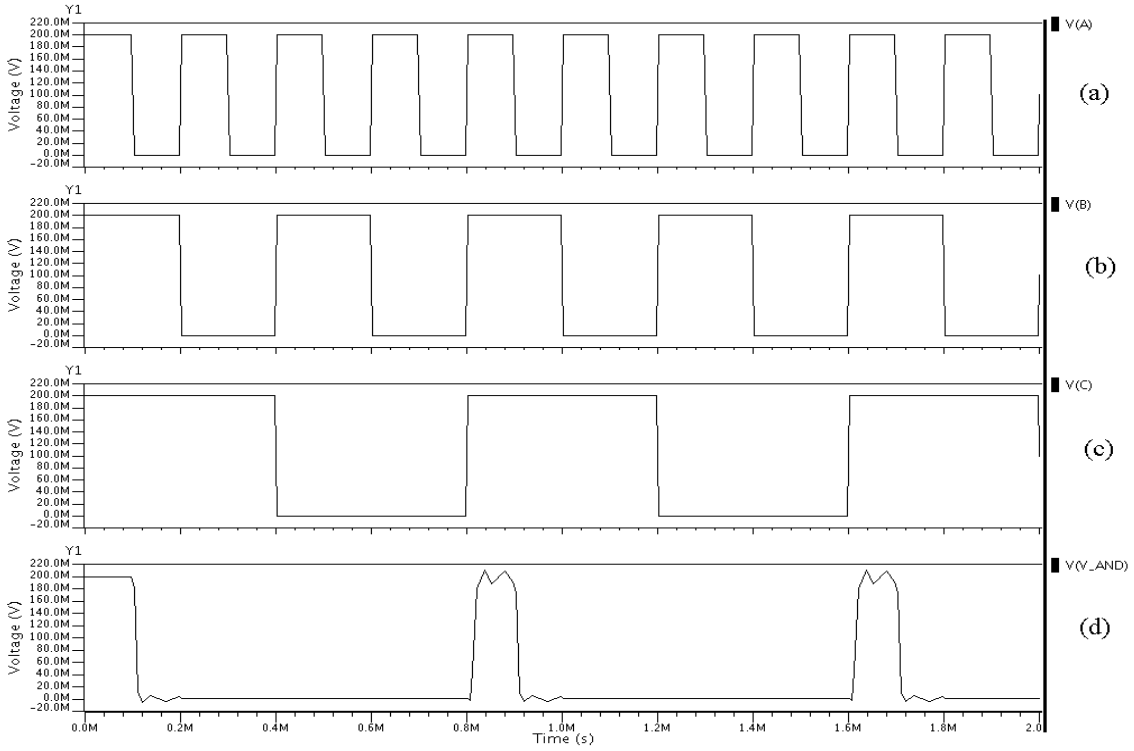

Figure 4.20: Simulation result of Three-Input CMOS AND Gate in subthreshold conduction region:
(a) Input Signal (A), (b) Input Signal (B), (c) Input Signal (C), (d) Voltage Waveform of Output Signal (V_AND).

4.7 DESIGN AND SIMULATION RESULT FOR A THREE-INPUT CMOS OR GATE

The minimum sized Three-Input CMOS OR Gate, designed using standard TSMC 0.18 μm CMOS technology is shown in Figure 4.21. This has been simulated using ELDO simulator.

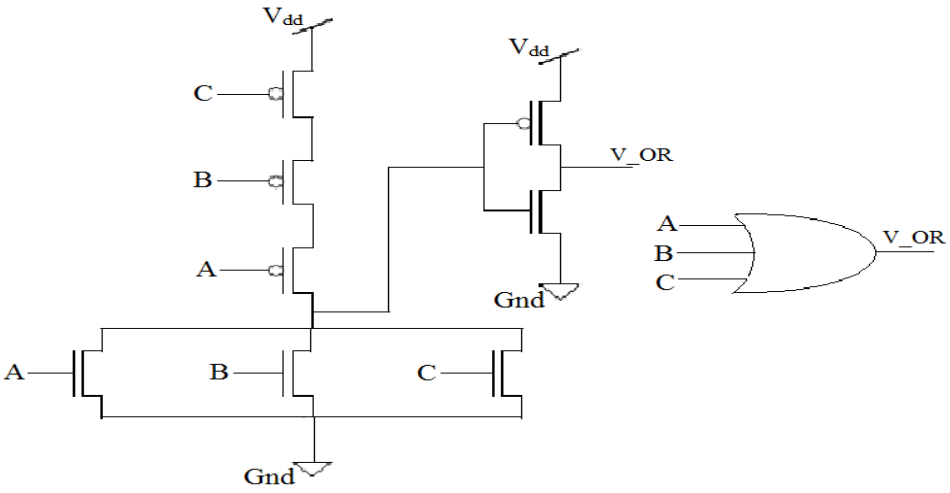

Figure 4.21: Basic Structure of a Three-Input CMOS OR Gate.

4.7.1 THREE-INPUT CMOS OR GATE OPERATING IN SUPERTHRESHOLD CONDUCTION REGION

The supply voltage used for this Three-Input CMOS OR Gate is 1.8 V and load capacitance is 5 *fF*. The simulation result of transient analysis is shown in Figure 4.22.

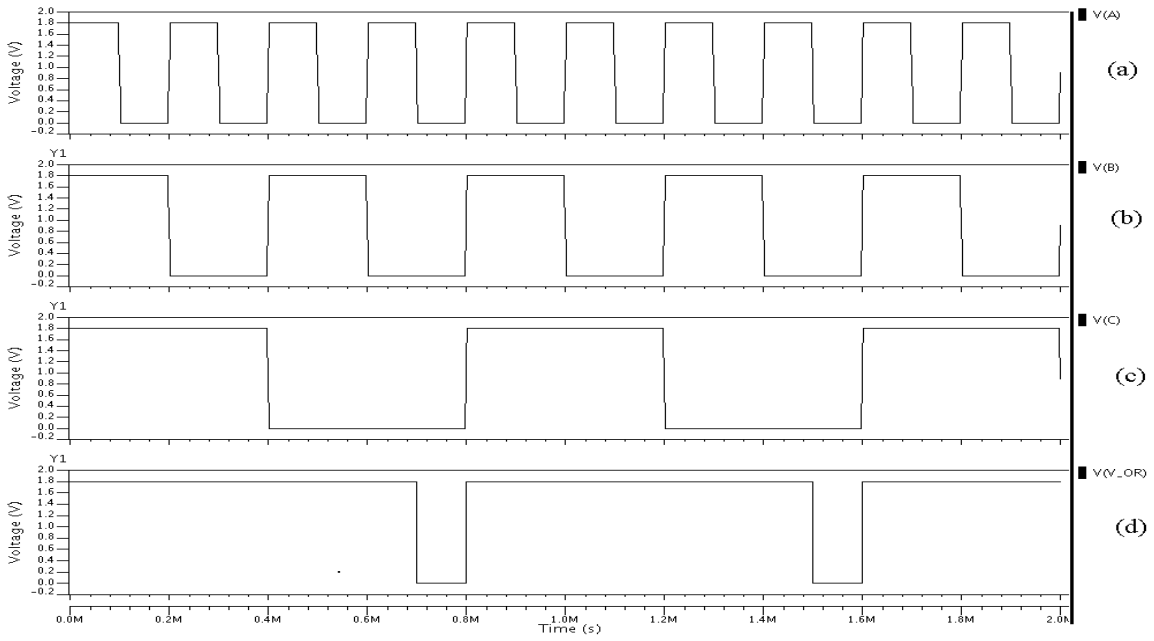

Figure 4.22: Simulation result of Three-Input CMOS OR Gate in superthreshold conduction region:
(a) Input Signal (A), (b) Input Signal (B), (c) Input Signal (C), (d) Voltage Waveform of Output Signal (V_OR).

4.7.2 THREE-INPUT CMOS OR GATE OPERATING IN SUBTHRESHOLD CONDUCTION REGION

The supply voltage used for this Three-Input CMOS OR Gate is 0.2 V and load capacitance is 11 *fF*. The simulation result of transient analysis is shown in Figure 4.23.

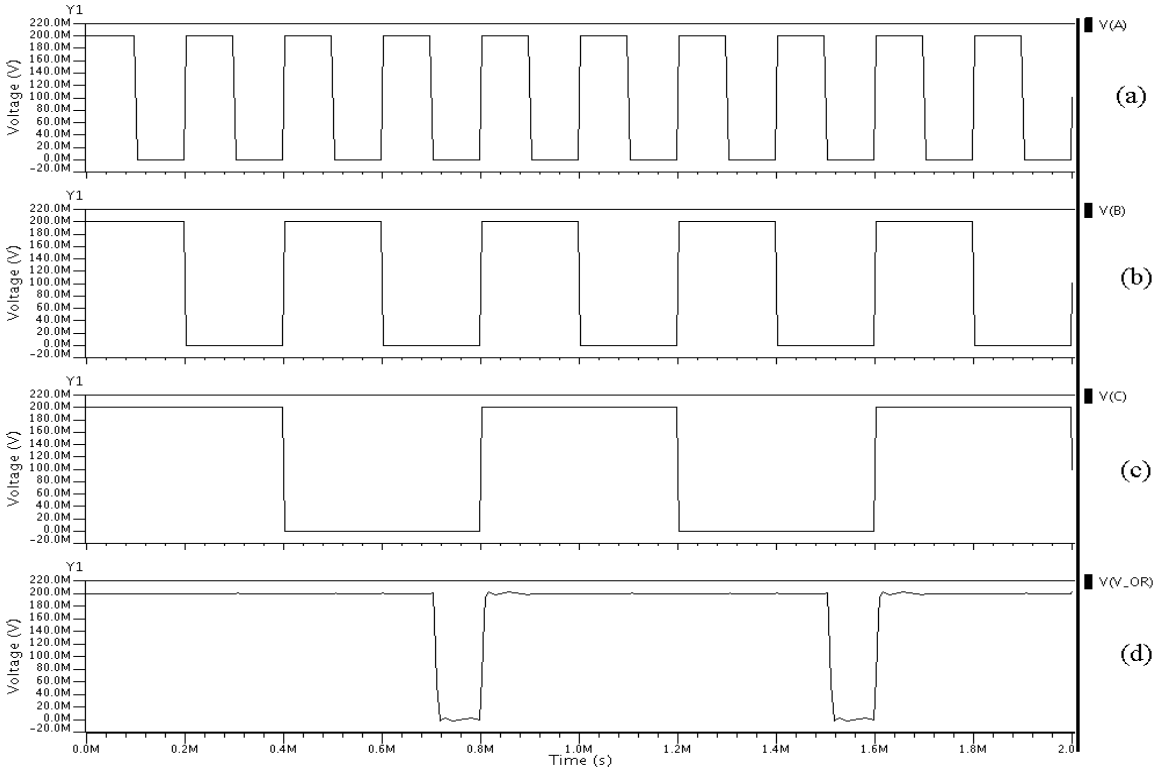

Figure 4.23: Simulation result of Three-Input CMOS OR Gate in subthreshold conduction region:
(a) Input Signal (A), (b) Input Signal (B), (c) Input Signal (C), (d) Voltage Waveform of Output Signal (V_OR).

4.8 DESIGN AND SIMULATION RESULT FOR A 2-TO-1 CMOS MULTIPLEXER

The CMOS based Two-to-One Multiplexer designed in Mentor Graphics IC Design Architect in Standard TSMC 0.18 *μm* CMOS Technology was simulated in ELDO Simulator. The basic structure of this Two-to-One Multiplexer is shown in Figure 4.24.

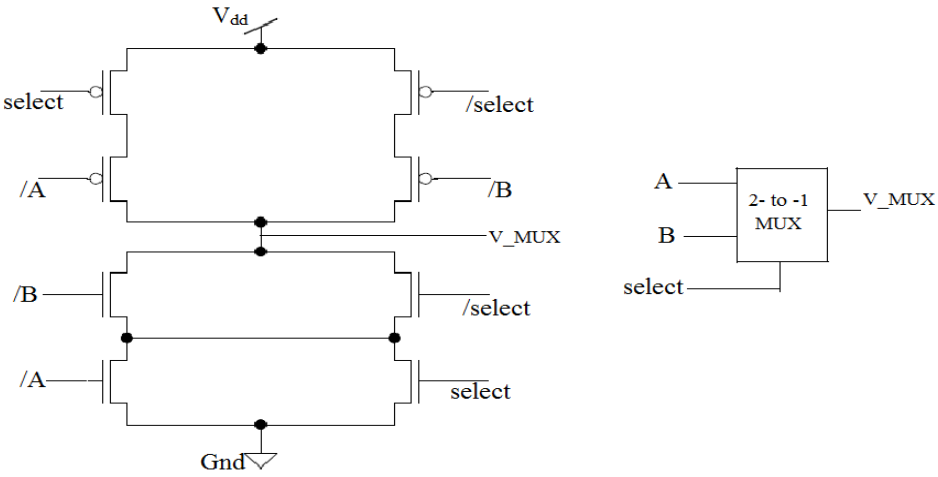

Figure 4.24: Basic Structure of a Two-to-One CMOS Multiplexer.

4.8.1 2-TO-1 CMOS MULTIPLEXER OPERATING IN SUPERTHRESHOLD CONDUCTION REGION

The supply voltage used for this Two-to-One CMOS Multiplexer is 1.8 V and load capacitance is 13 *fF*. The simulation result of transient analysis is shown in Figure 4.25.

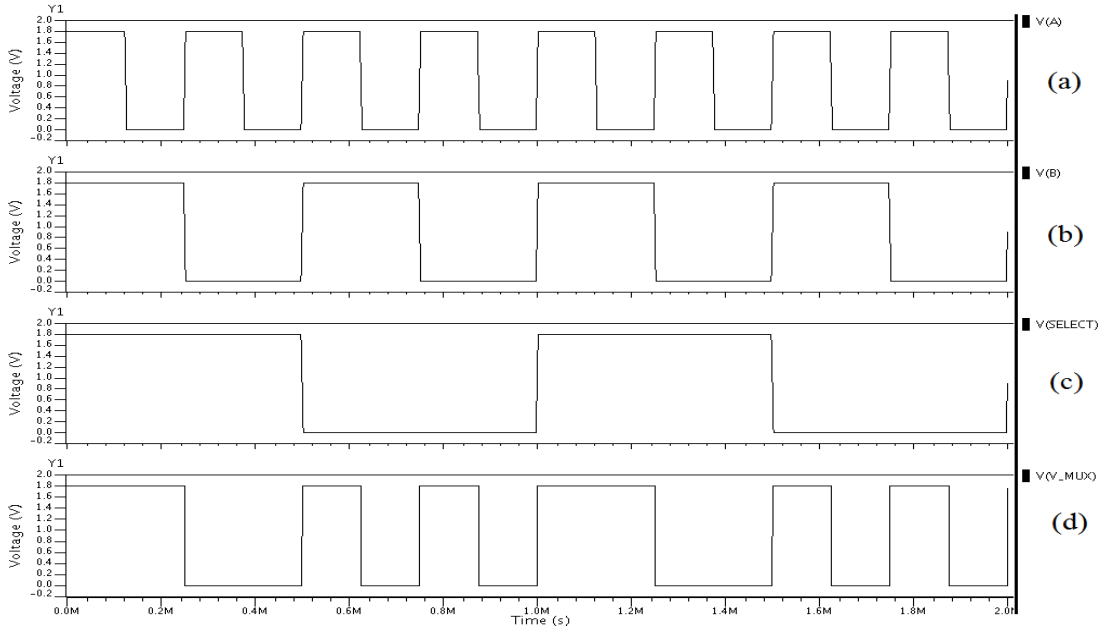

Figure 4.25: Simulation result of Two-to-One CMOS Multiplexer in superthreshold conduction region:
(a) Input Signal (A), (b) Input Signal (B),
(c) Input Signal (SELECT),
(d) Voltage Waveform of Output Signal (V_MUX).

4.8.2 2-TO-1 CMOS MULTIPLEXER OPERATING IN SUBTHRESHOLD CONDUCTION REGION

The supply voltage used for this Two-to-One CMOS Multiplexer is 0.2 V and load capacitance is 30 *fF*. The simulation result of transient analysis is shown in Figure 4.26.

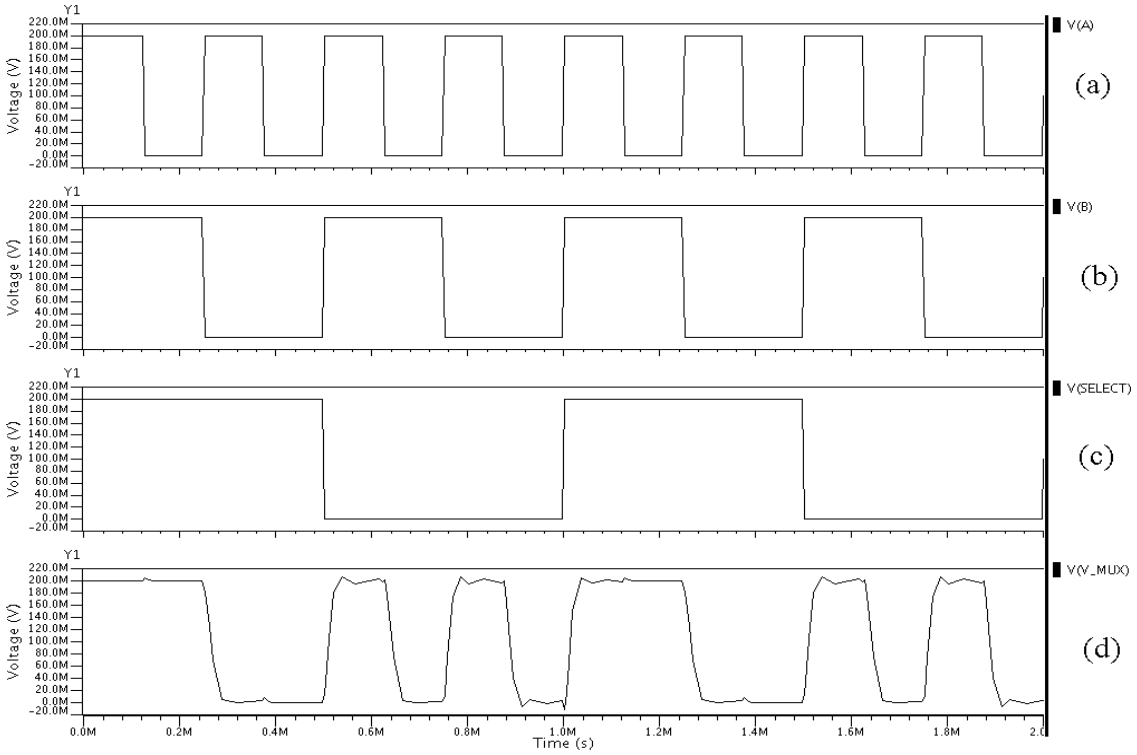

Figure 4.26: Simulation result of Two-to-One CMOS Multiplexer in subthreshold conduction region:
(a) Input Signal (A), (b) Input Signal (B),
(c) Input Signal (select),
(d) Voltage Waveform of Output Signal (V_MUX).

4.9 DESIGN AND SIMULATION RESULT FOR A CMOS HALF ADDER

The basic structure of a minimum sized CMOS Half Adder is shown below in Figure 4.27 which has been designed using standard TSMC 0.18 μm CMOS technology and simulated using ELDO simulator.

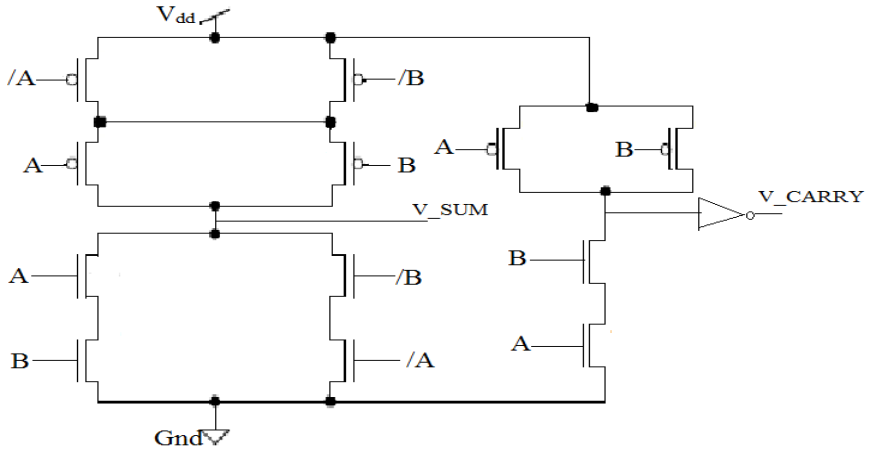

Figure 4.27: Basic Structure of a CMOS Half Adder.

4.9.1 CMOS HALF ADDER OPERATING IN SUPERTHRESHOLD CONDUCTION REGION

The supply voltage used for this CMOS Half Adder is 1.8 V and load capacitance for carry is 5 *fF* while load capacitance for sum is 12 *fF*. The simulation result of transient analysis is shown in Figure 4.28.

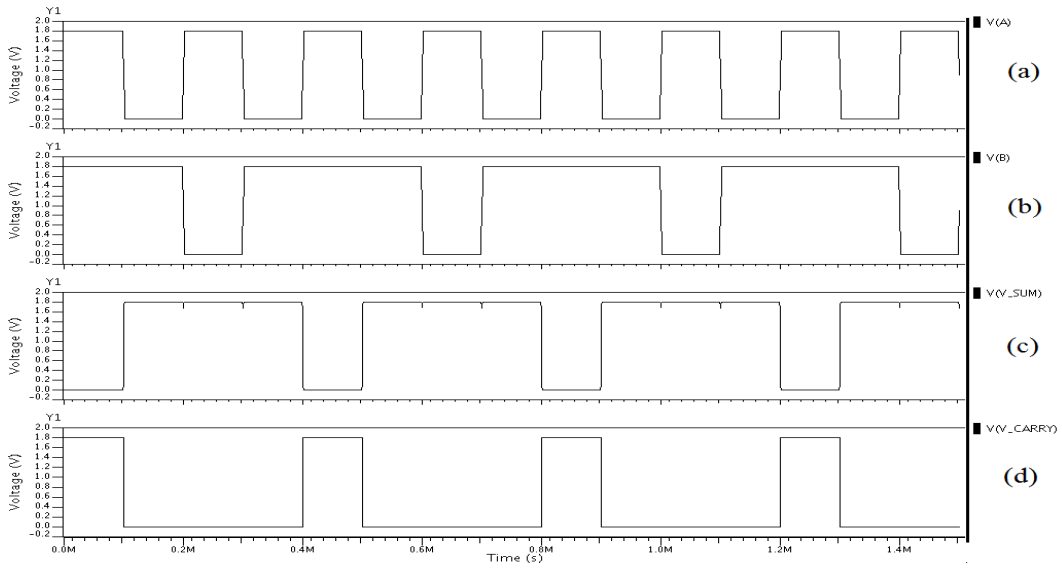

Figure 4.28: Simulation result of CMOS Half Adder in superthreshold conduction region:
(a) Input Signal (A), (b) Input Signal (B),
(c) Voltage Waveform of Output Signal (V_SUM),
(d) Voltage Waveform of Output Signal (V_CARRY).

4.9.2 CMOS HALF ADDER OPERATING IN SUBTHRESHOLD CONDUCTION REGION

The supply voltage used for this CMOS Half Adder is 0.2 V and load capacitance for carry is 11 *fF* while load capacitance for sum is 25 *fF*. The simulation result of transient analysis is shown in Figure 4.29.

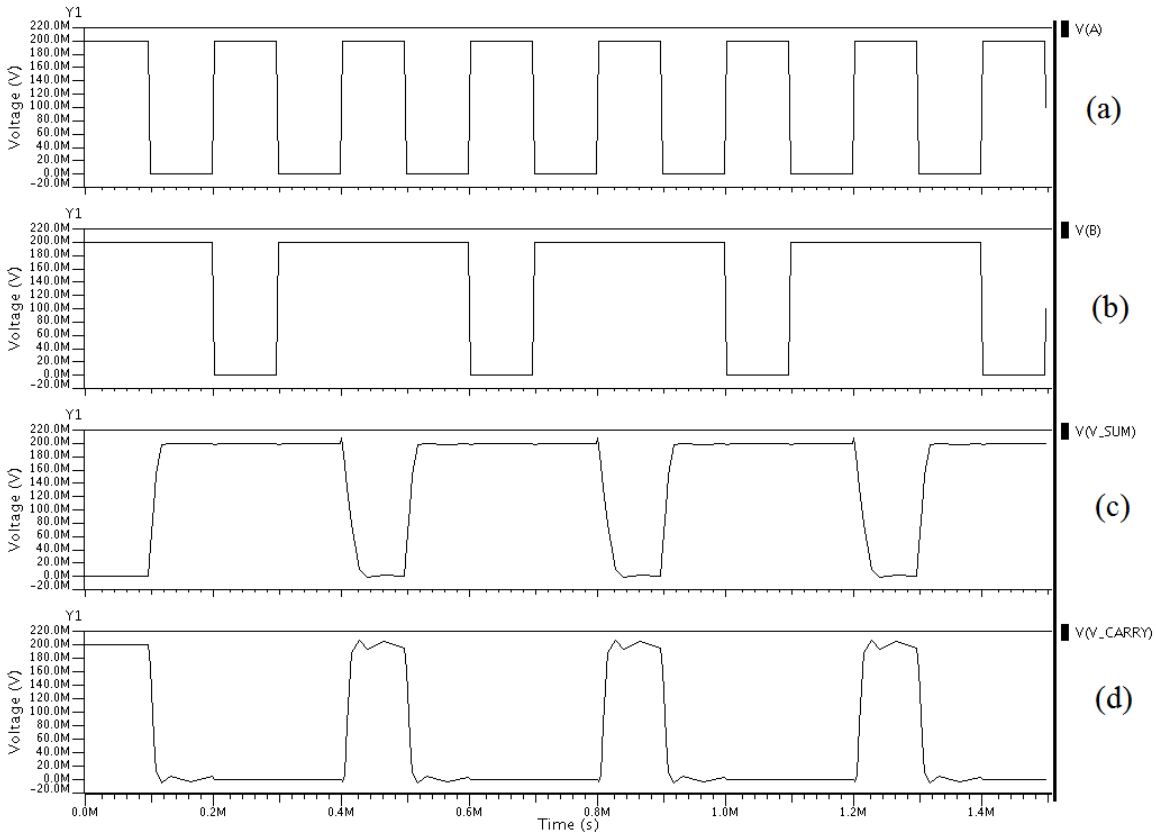

Figure 4.29: Simulation result of CMOS Half Adder in subthreshold conduction region:
(a) Input Signal (A), (b) Input Signal (B),
(c) Voltage Waveform of Output Signal (V_SUM),
(d) Voltage Waveform of Output Signal (V_CARRY).

4.10 DESIGN AND SIMULATION RESULT FOR A ONE-BIT CMOS FULL ADDER

The Full Adder is the basic structure for any arithmetic circuit, so the design of a Full Adder is also necessary. The CMOS based One-Bit Full Adder designed in Mentor Graphics IC Design Architect in Standard TSMC 0.18 μm CMOS Technology was simulated in ELDO Simulator. The basic structure of this One-Bit Full Adder is shown in Figure 4.30.

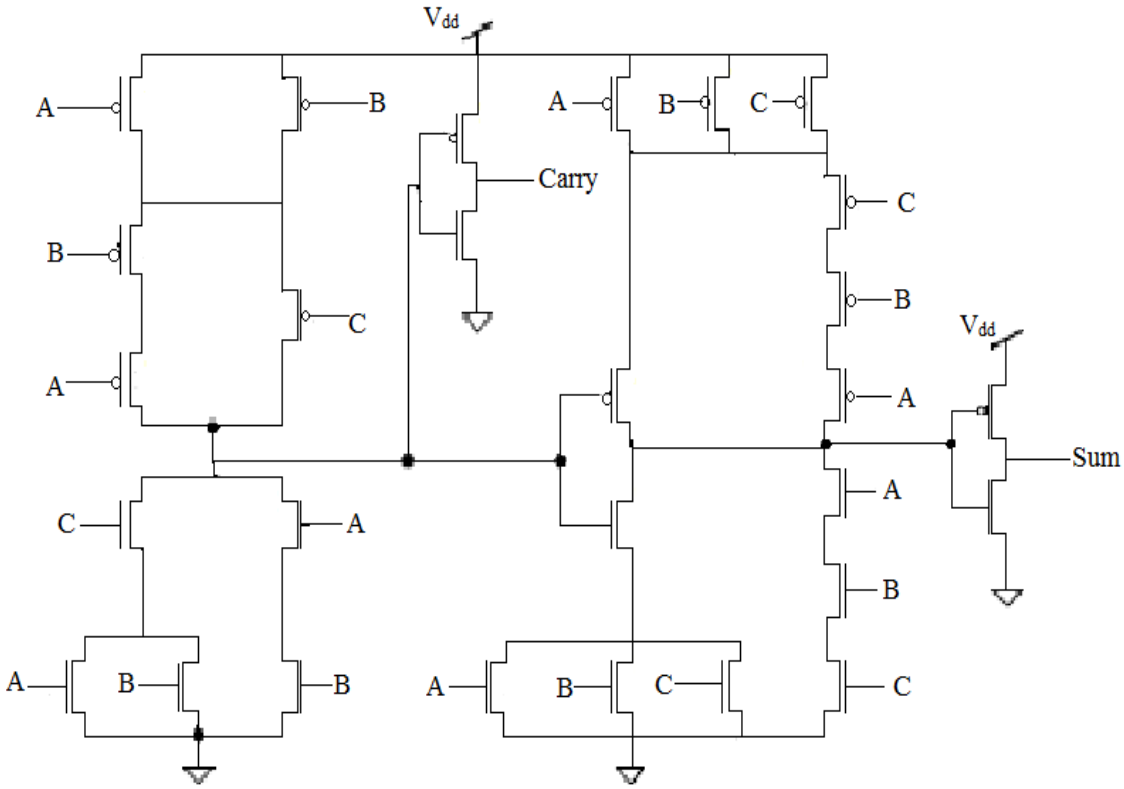

Figure 4.30: Basic Structure of a One-Bit CMOS Full Adder.

4.10.1 ONE-BIT CMOS FULL ADDER OPERATING IN SUPERTHRESHOLD CONDUCTION REGION

The supply voltage used for this One-Bit CMOS Full Adder is 1.8 V and load capacitance for carry is 5 *fF* while load capacitance for sum is also 5 *fF*. The simulation result of transient analysis is shown in Figure 4.31.

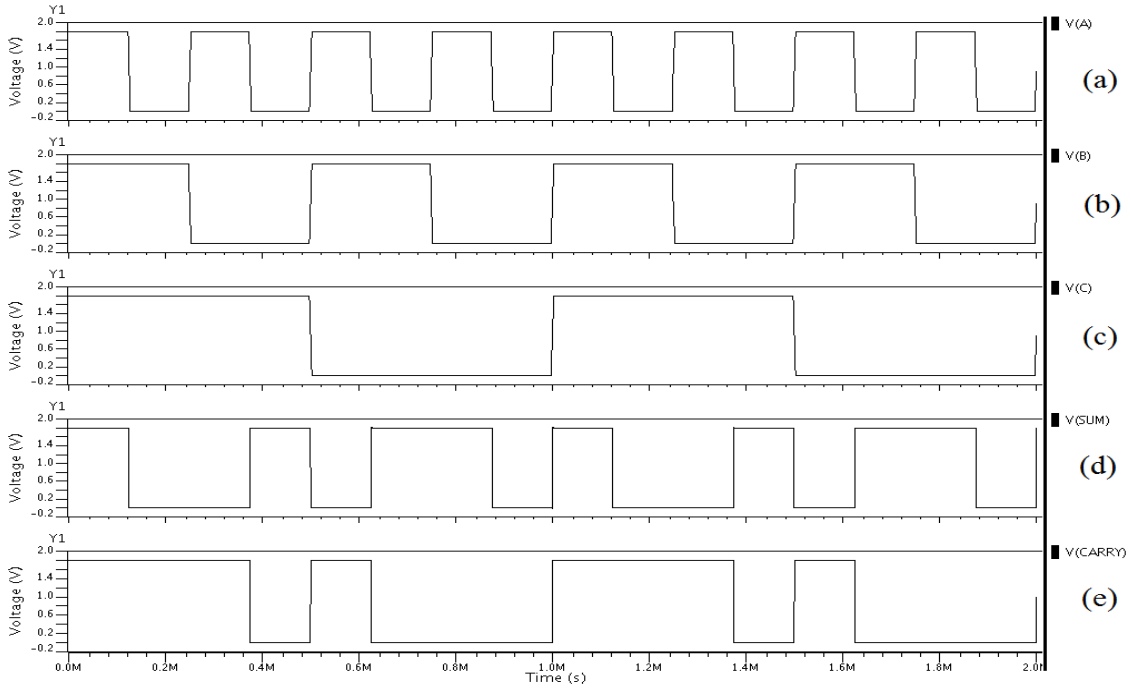

Figure 4.31: Simulation result of One-Bit CMOS Full Adder in superthreshold conduction region:
(a) Input Signal (A), (b) Input Signal (B),
(c) Input Carry Signal (C),
(d) Voltage Waveform of Output (SUM) Signal,
(e) Voltage Waveform of Output (CARRY) Signal.

4.10.2 ONE-BIT CMOS FULL ADDER OPERATING IN SUBTHRESHOLD CONDUCTION REGION

The supply voltage used for this One-Bit CMOS Full Adder is 0.2 V and load capacitance for carry is 8 *fF* while load capacitance for sum is also 8 *fF*. The simulation result of transient analysis is shown in Figure 4.32.

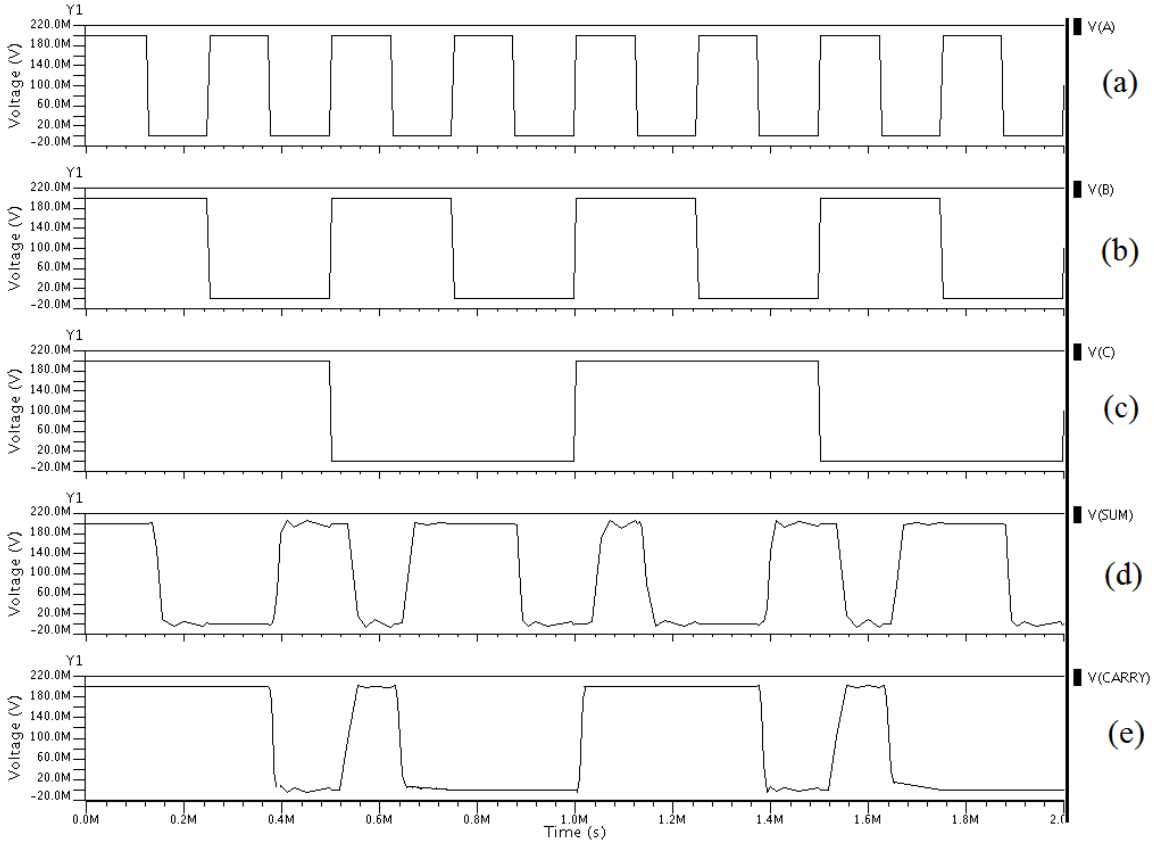

Figure 4.32: Simulation result of One-Bit CMOS Full Adder in subthreshold conduction region:
(a) Input Signal (A), (b) Input Signal (B),
(c) Input Carry Signal (C),
(d) Voltage Waveform of Output (SUM) Signal,
(e) Voltage Waveform of Output (CARRY) Signal.

4.11 DESIGN AND SIMULATION RESULT FOR A TWO-BIT MULTIPLIER

The Multiplier is an important kernel of digital signal processors (DSP) because it typically determines the performance of the chips. Furthermore, because of high circuit complexity, the power consumption and the layout area are another two design considerations of the Multiplier [18].

Also, nowadays, many digital signal processing systems are targeted at portable, battery operated systems, so power dissipation is one of the primary design constraints. Since,

Multipliers are rather complex circuits and typically must operate at a high system clock rate, reducing the power dissipation of multipliers is a key to satisfying the overall power budget [19]. Digital CMOS circuits consume relatively less power and static CMOS logic is widely used because of its robustness, and its suitability for design automation [20].

The CMOS based Two-Bit Multiplier designed in Mentor Graphics IC Design Architect in Standard TSMC 0.18 μm CMOS Technology was simulated in ELDO Simulator. The basic structure of this Two-Bit Multiplier is shown in Figure 4.33.

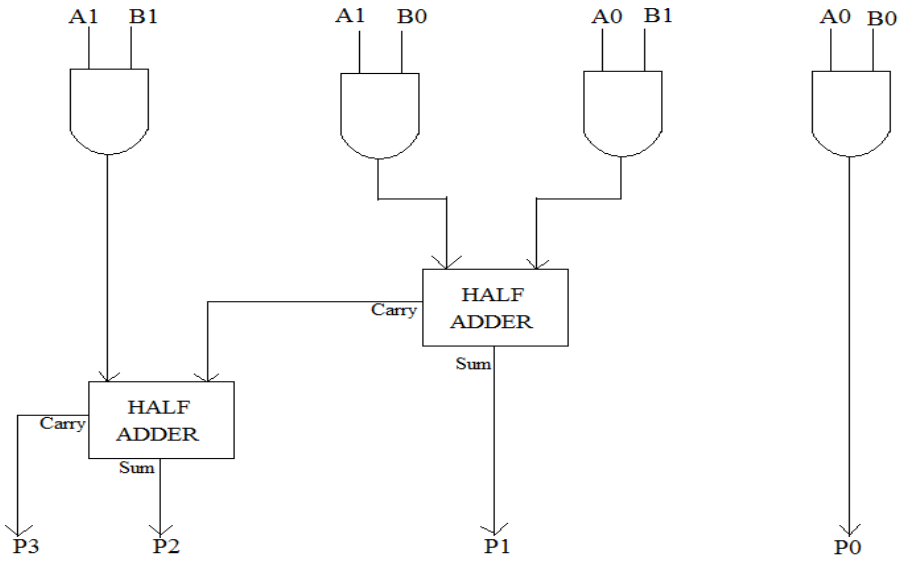

Figure 4.33: Basic Structure of a Two-Bit Multiplier.

The circuit shown in Figure 4.33 provide the multiplication of two 2-Bit digital numbers (A1 A0) and (B1 B0) in the following way:

$$
\begin{array}{cccc}
 & & B1 & B0 \\
 & & A1 & A0 \\
\hline
 & & A0B1 & A0B0 \\
 & A1B1 & A1B0 & \\
\hline
P3 & P2 & P1 & P0 \\
\hline
\end{array}
$$

4.11.1 TWO-BIT MULTIPLIER OPERATING IN SUPERTHRESHOLD CONDUCTION REGION

The supply voltage used for this Two-Bit Multiplier is 1.8 V and load capacitance for output nodes, P0 and P3 is 5 *fF* each, while load capacitance for output nodes, P1 and P2 is 12 *fF* each. The simulation result of transient analysis is shown in Figure 4.34.

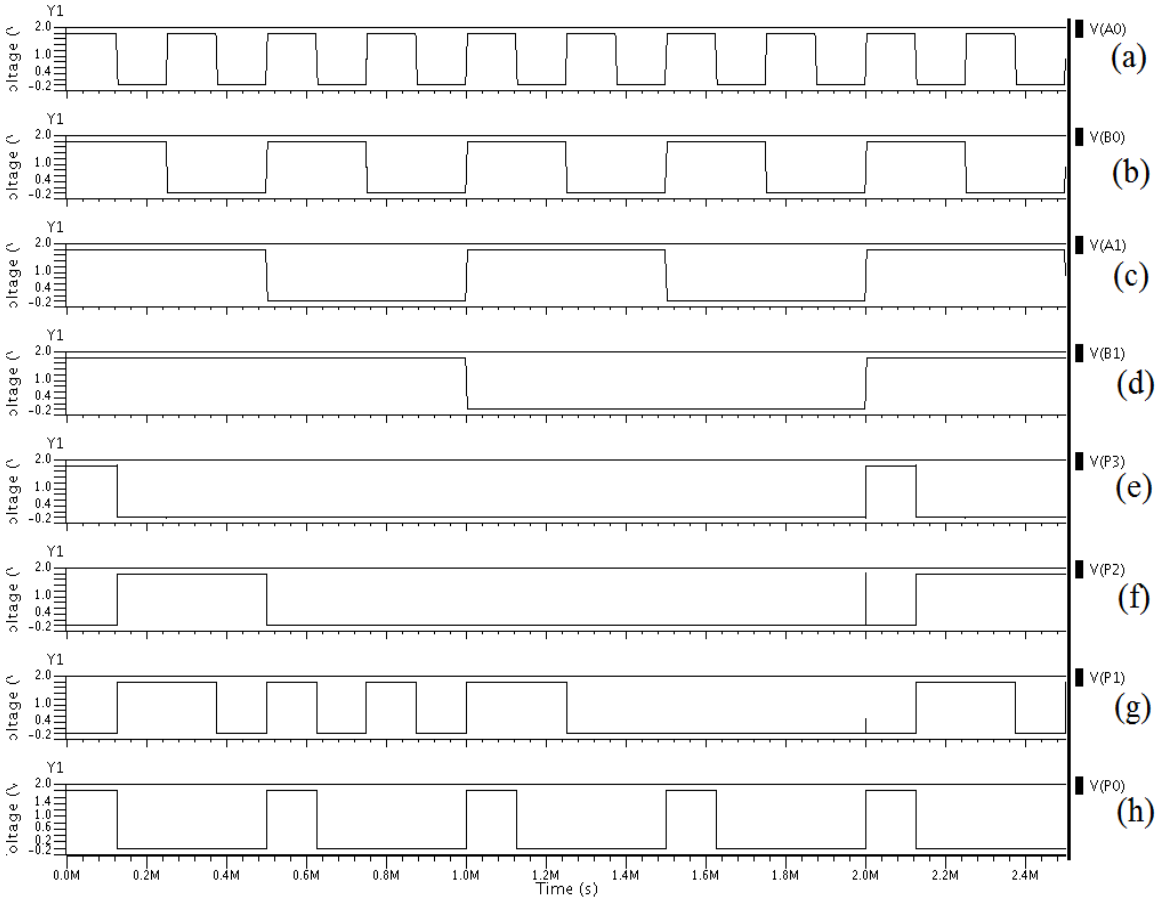

Figure 4.34: Simulation result of Two-Bit Multiplier in superthreshold conduction region:

(a) Input Signal (A0), (b) Input Signal (B0),

(c) Input Signal (A1), (d) Input Signal (B1),

(e) Voltage Waveform of Output Signal (P3),

(f) Voltage Waveform of Output Signal (P2),

(g) Voltage Waveform of Output Signal (P1),

(h) Voltage Waveform of Output Signal (P0).

4.11.2 TWO-BIT MULTIPLIER OPERATING IN SUBTHRESHOLD CONDUCTION REGION

The supply voltage used for this Two-Bit Multiplier is 0.2 V and load capacitance for output nodes, P0 and P3 is 11 *fF* each, while load capacitance for output nodes, P1 and P2 is 25 *fF* each. The simulation result of transient analysis is shown in Figure 4.35.

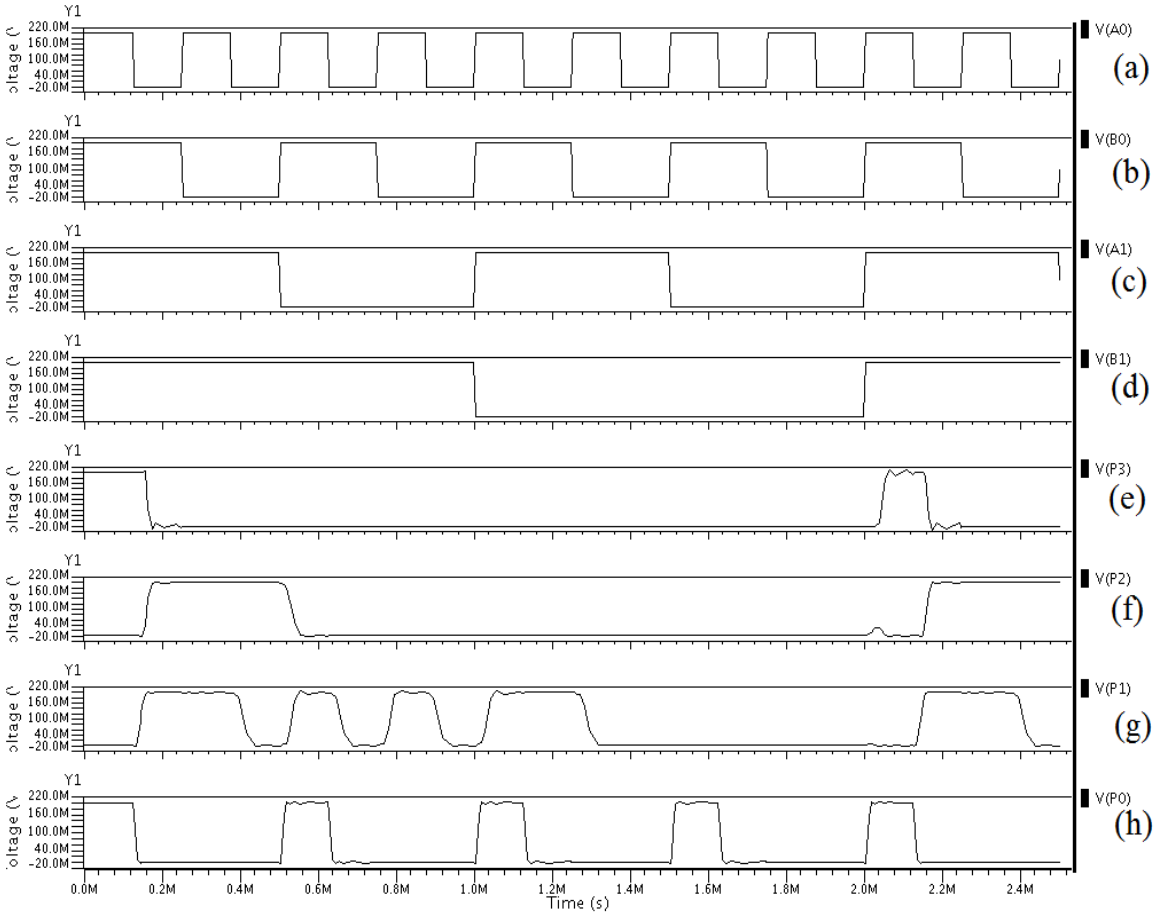

Figure 4.35: Simulation result of Two-Bit Multiplier in subthreshold conduction region:

(a) Input Signal (A0), (b) Input Signal (B0),

(c) Input Signal (A1), (d) Input Signal (B1),

(e) Voltage Waveform of Output Signal (P3),

(f) Voltage Waveform of Output Signal (P2),

(g) Voltage Waveform of Output Signal (P1),

(h) Voltage Waveform of Output Signal (P0).

4.12 POWER DISSIPATION ANALYSIS

4.12.1 VARIATION OF POWER DISSIPATION WITH SUPPLY VOLTAGE

This section deals with the comparison of the CMOS Inverter operating in superthreshold conduction region with the CMOS Inverter operating in subthreshold conduction region in terms of the average dynamic power dissipation varying with supply voltage. The variation of the power dissipation with the varying supply voltage is shown in figures given below.

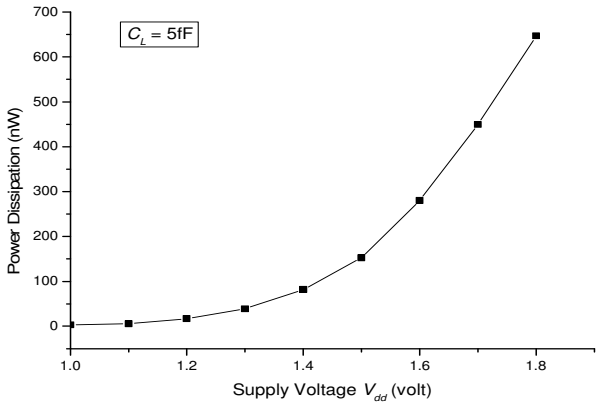

Figure 4.36: Variation of Power Dissipation with the Supply Voltage for an Inverter in superthreshold conduction region operating @ f = 5 KHz.

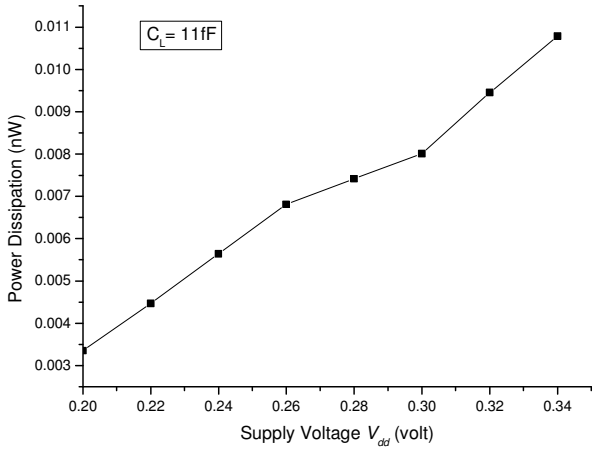

Figure 4.37: Variation of Power Dissipation with the Supply Voltage for an Inverter in subthreshold conduction region operating @ f = 5 KHz.

4.12.2 VARIATION OF POWER DISSIPATION WITH FREQUENCY

This section deals with the comparison of CMOS Digital Circuits operating in superthreshold conduction region with CMOS Digital Circuits operating in subthreshold conduction region in terms of the average dynamic power dissipation varying with frequency.

TABLE 4.1

AVERAGE DYNAMIC POWER DISSIPATED BY AN INVERTER OPERATING IN SUPERTHRESHOLD CONDUCTION REGION AND SUBTHRESHOLD CONDUCTION REGION FOR DIFFERENT CLOCK FREQUENCIES

Frequency (KHz)	Power (nW)	
	Superthreshold Conduction Region	Subthreshold Conduction Region
2 K	275.87 n	0.001557 n
4 K	389.54 n	0.002107 n
5 K	486.93 n	0.002576 n
7 K	646.99 n	0.003356 n
10 K	973.84 n	0.004899 n
20 K	1947.67 n	0.009639 n

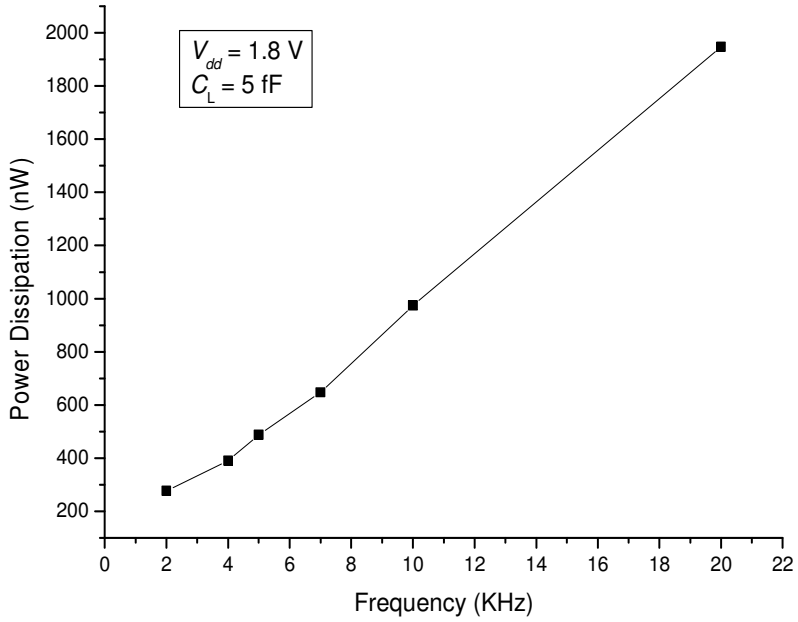

Figure 4.38: Power Dissipation Results for an Inverter operating in superthreshold conduction region.

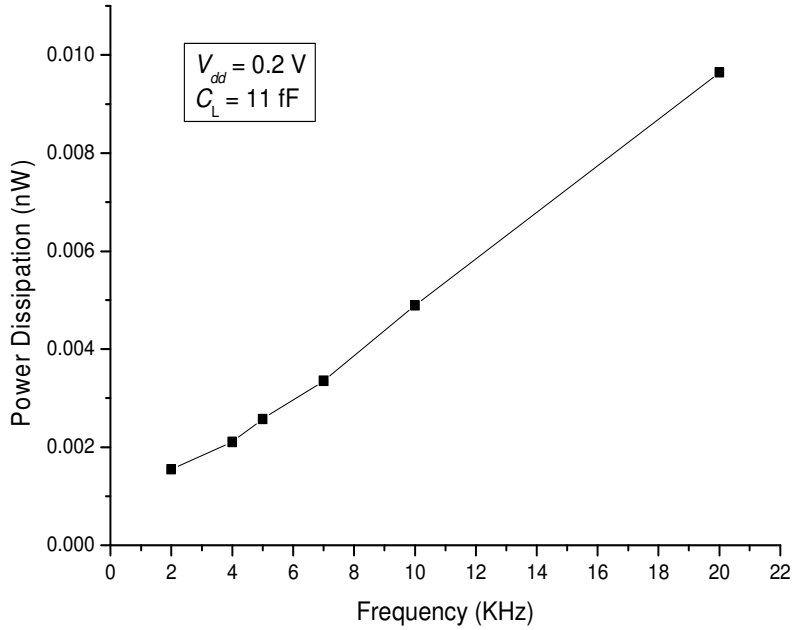

Figure 4.39: Power Dissipation Results for an Inverter operating in subthreshold conduction region.

TABLE 4.2

AVERAGE DYNAMIC POWER DISSIPATED BY A TWO-INPUT NAND GATE OPERATING IN SUPERTHRESHOLD CONDUCTION REGION AND SUBTHRESHOLD CONDUCTION REGION FOR DIFFERENT CLOCK FREQUENCIES

Frequency (KHz)	Power (nW)	
	Superthreshold Conduction Region	Subthreshold Conduction Region
2 K	189.39 n	0.001874 n
3 K	275.36 n	0.002218 n
4 K	366.56 n	0.002732 n
5 K	442.54 n	0.003382 n
7 K	697.60 n	0.004513 n
10 K	1131.33 n	0.006288 n

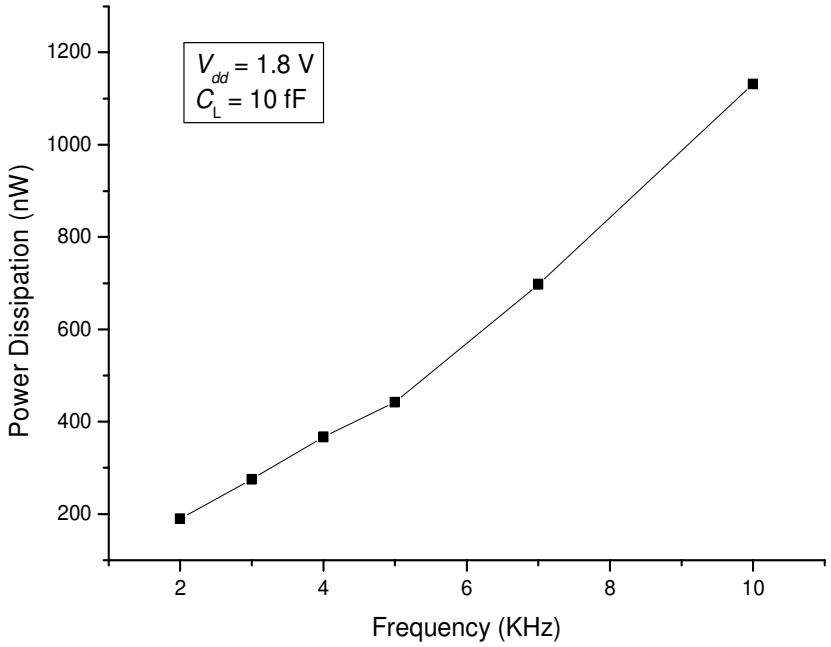

Figure 4.40: Power Dissipation Results for a Two-Input NAND Gate operating in superthreshold conduction region.

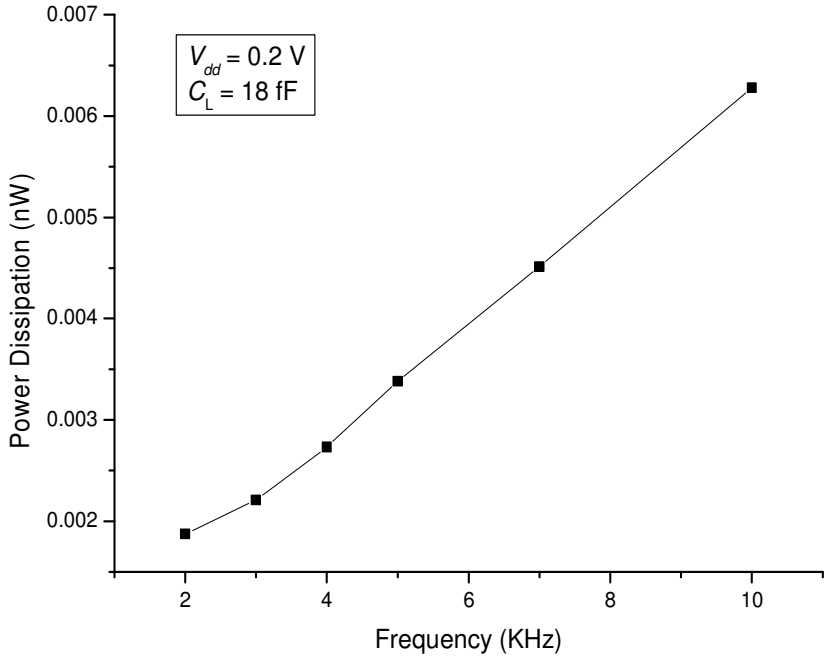

Figure 4.41: Power Dissipation Results for a Two-Input NAND Gate operating in subthreshold conduction region.

TABLE 4.3

AVERAGE DYNAMIC POWER DISSIPATED BY A TWO-INPUT NOR GATE OPERATING IN SUPERTHRESHOLD CONDUCTION REGION AND SUBTHRESHOLD CONDUCTION REGION FOR DIFFERENT CLOCK FREQUENCIES

Frequency (KHz)	Power (nW)	
	Superthreshold Conduction Region	Subthreshold Conduction Region
2 K	2.28 n	0.00000739 n
3 K	3.11 n	0.00001008 n
4 K	3.92 n	0.00001240 n
5 K	4.66 n	0.00001513 n
7 K	6.41 n	0.00002073 n
10 K	9.32 n	0.00002914 n

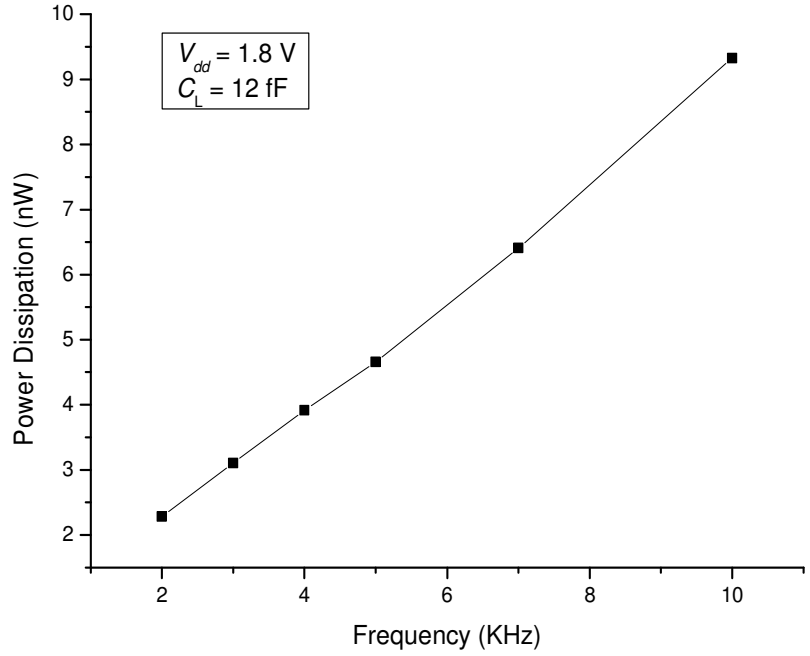

Figure 4.42: Power Dissipation Results for a Two-Input NOR Gate operating in superthreshold conduction region.

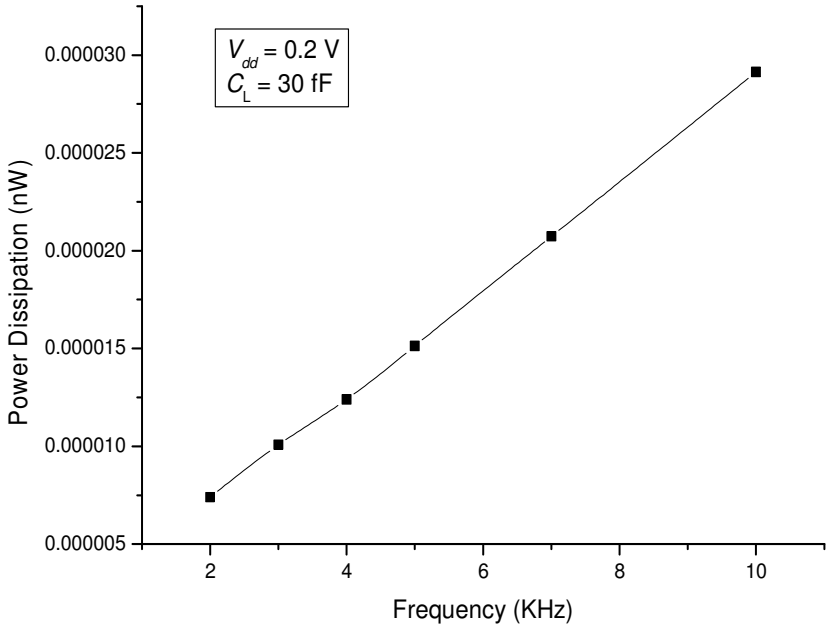

Figure 4.43: Power Dissipation Results for a Two-Input NOR Gate operating in subthreshold conduction region.

TABLE 4.4

AVERAGE DYNAMIC POWER DISSIPATED BY A TWO-INPUT AND GATE OPERATING IN SUPERTHRESHOLD CONDUCTION REGION AND SUBTHRESHOLD CONDUCTION REGION FOR DIFFERENT CLOCK FREQUENCIES

Frequency (KHz)	Power (nW)	
	Superthreshold Conduction Region	Subthreshold Conduction Region
1 K	174.89 n	0.001974 n
2 K	325.48 n	0.002577 n
3 K	484.73 n	0.003125 n
4 K	632.82 n	0.003641 n
5 K	786.57 n	0.004158 n
7 K	1098.23 n	0.005357 n

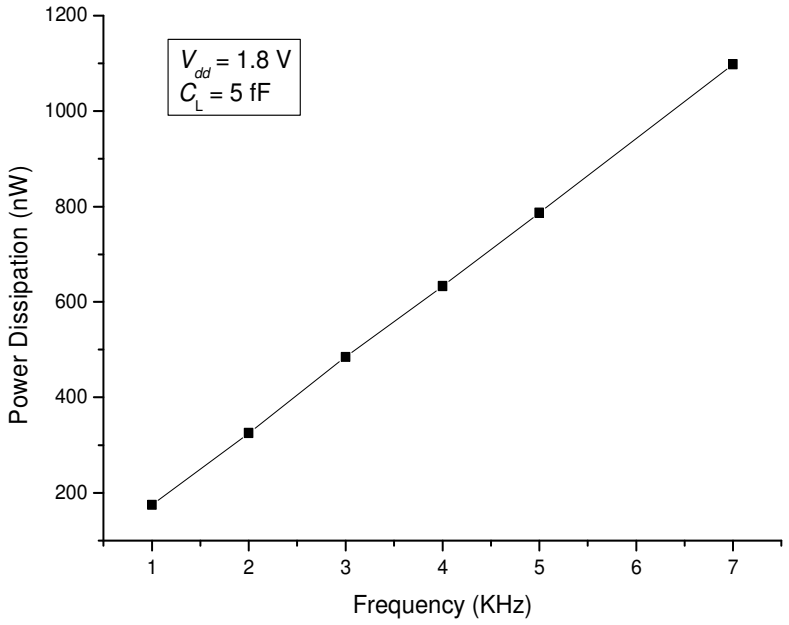

Figure 4.44: Power Dissipation Results for a Two-Input AND Gate operating in superthreshold conduction region.

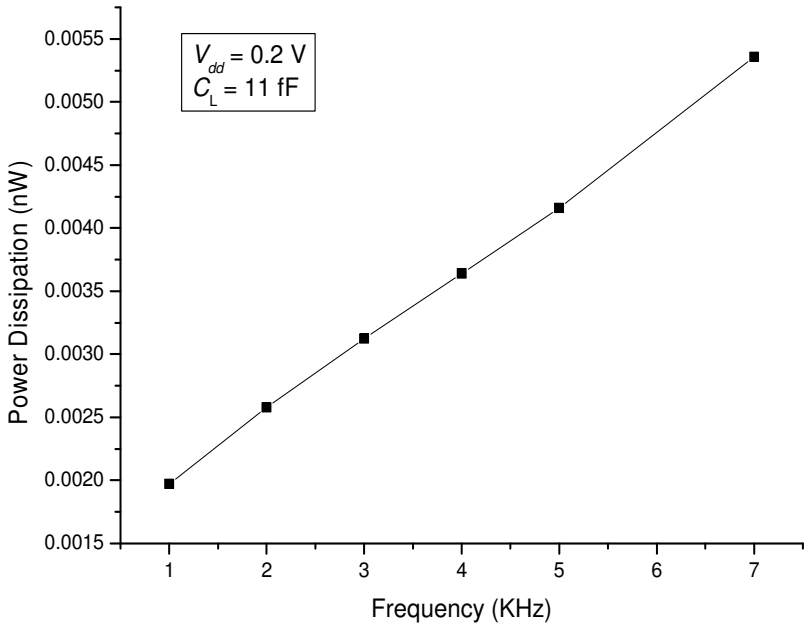

Figure 4.45: Power Dissipation Results for a Two-Input AND Gate operating in subthreshold conduction region.

TABLE 4.5

AVERAGE DYNAMIC POWER DISSIPATED BY A TWO-INPUT XOR GATE OPERATING IN SUPERTHRESHOLD CONDUCTION REGION AND SUBTHRESHOLD CONDUCTION REGION FOR DIFFERENT CLOCK FREQUENCIES

Frequency (KHz)	Power (nW)	
	Superthreshold Conduction Region	Subthreshold Conduction Region
1 K	261.71 n	0.002220 n
2 K	488.53 n	0.003162 n
3 K	748.24 n	0.004012 n
4 K	968.30 n	0.004931 n
5 K	1218.58 n	0.005844 n
7 K	1758.2 n	0.007550 n

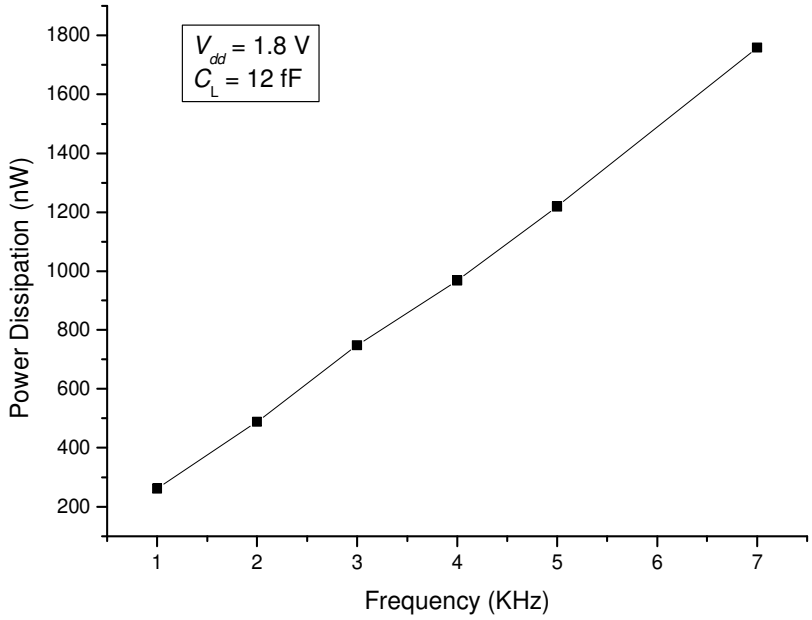

Figure 4.46: Power Dissipation Results for a Two-Input XOR Gate operating in superthreshold conduction region.

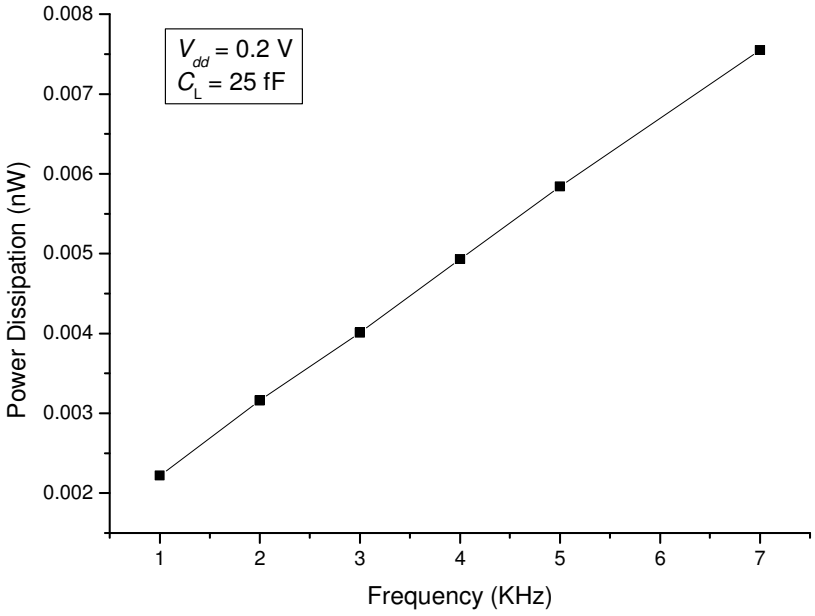

Figure 4.47: Power Dissipation Results for a Two-Input XOR Gate operating in subthreshold conduction region.

TABLE 4.6

AVERAGE DYNAMIC POWER DISSIPATED BY A THREE-INPUT AND GATE OPERATING IN SUPERTHRESHOLD CONDUCTION REGION AND SUBTHRESHOLD CONDUCTION REGION FOR DIFFERENT CLOCK FREQUENCIES

Frequency (KHz)	Power (nW)	
	Superthreshold Conduction Region	Subthreshold Conduction Region
1 K	84.57 n	0.001748 n
2 K	138.63 n	0.002173 n
3 K	198.58 n	0.002634 n
4 K	257.01 n	0.003058 n
5 K	321.24 n	0.003508 n

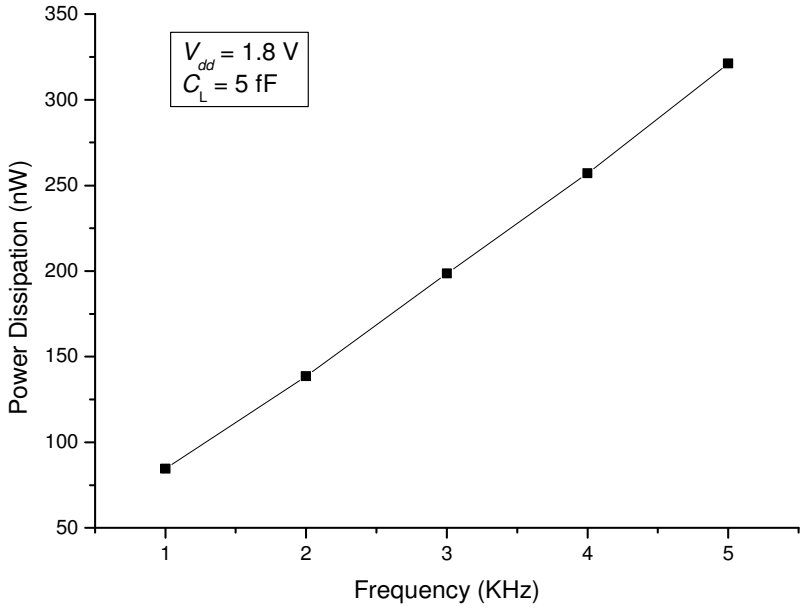

Figure 4.48: Power Dissipation Results for a Three-Input AND Gate operating in superthreshold conduction region.

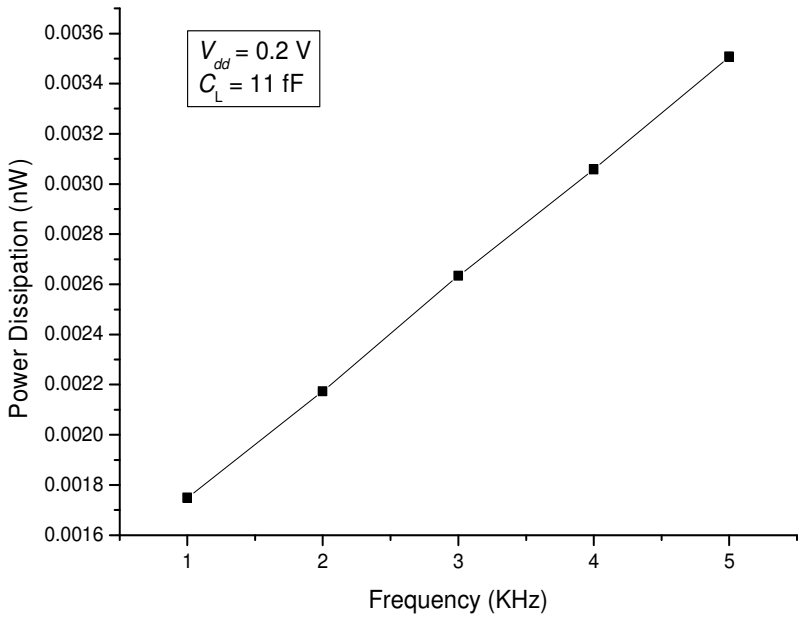

Figure 4.49: Power Dissipation Results for a Three-Input AND Gate operating in subthreshold conduction region.

TABLE 4.7

AVERAGE DYNAMIC POWER DISSIPATED BY A THREE-INPUT OR GATE OPERATING IN SUPERTHRESHOLD CONDUCTION REGION AND SUBTHRESHOLD CONDUCTION REGION FOR DIFFERENT CLOCK FREQUENCIES

Frequency (KHz)	Power (nW)	
	Superthreshold Conduction Region	Subthreshold Conduction Region
1 K	42.05 n	0.002267 n
2 K	85.91 n	0.002796 n
3 K	131.61 n	0.003369 n
4 K	169.70 n	0.003890 n
5 K	211.87 n	0.004429 n

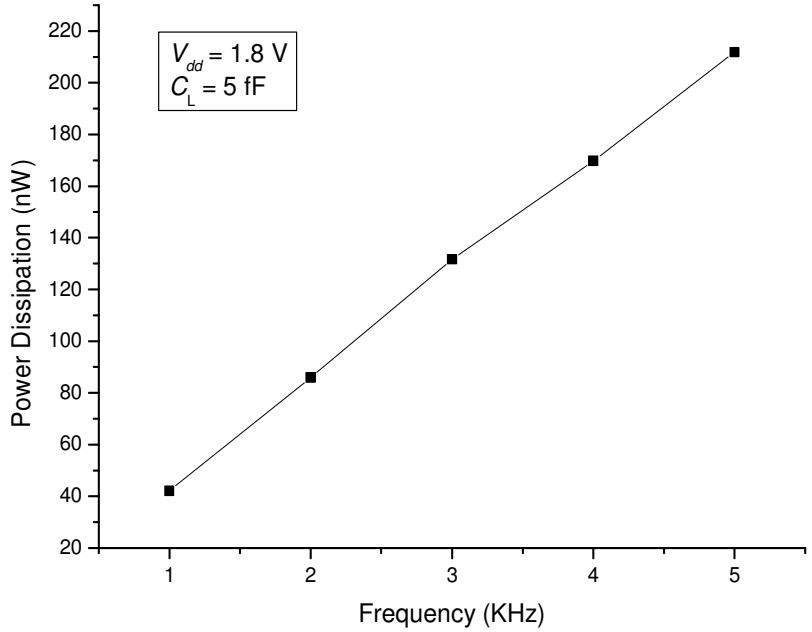

Figure 4.50: Power Dissipation Results for a Three-Input OR Gate operating in superthreshold conduction region.

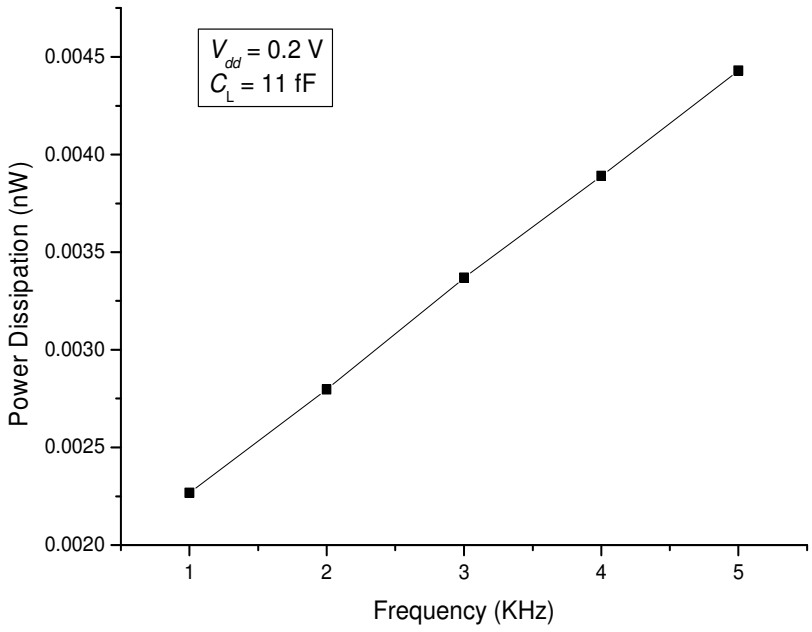

Figure 4.51: Power Dissipation Results for a Three-Input OR Gate operating in subthreshold conduction region.

TABLE 4.8

AVERAGE DYNAMIC POWER DISSIPATED BY A TWO-TO-ONE MULTIPLEXER OPERATING IN SUPERTHRESHOLD CONDUCTION REGION AND SUBTHRESHOLD CONDUCTION REGION FOR DIFFERENT CLOCK FREQUENCIES

Frequency (KHz)	Power (nW)	
	Superthreshold Conduction Region	Subthreshold Conduction Region
1 K	351.33 n	0.003732 n
2 K	468.51 n	0.004125 n
3 K	651.41 n	0.004565 n
4 K	869.55 n	0.004995 n
5 K	1038.58 n	0.005414 n

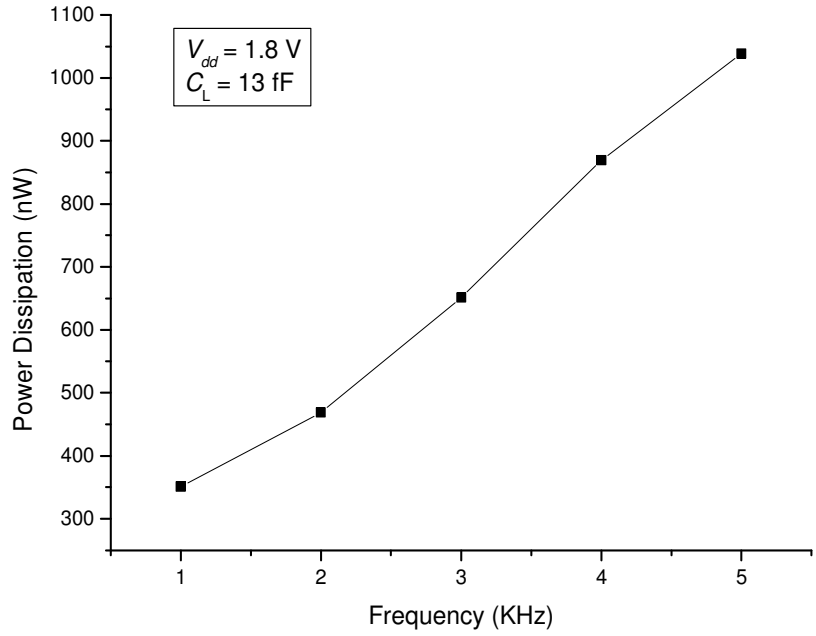

Figure 4.52: Power Dissipation Results for a 2:1 Multiplexer operating in superthreshold conduction region.

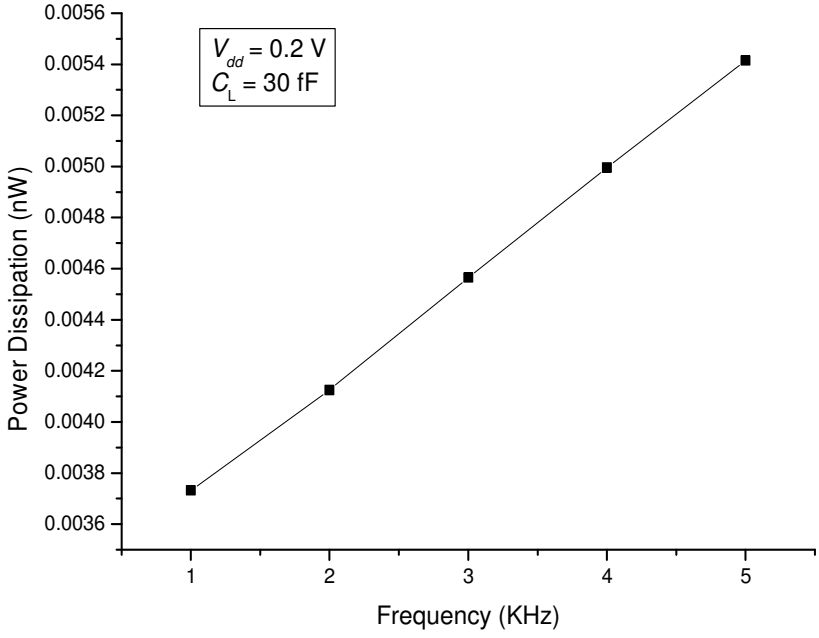

Figure 4.53: Power Dissipation Results for a 2:1 Multiplexer operating in subthreshold conduction region.

TABLE 4.9

AVERAGE DYNAMIC POWER DISSIPATED BY A HALF ADDER OPERATING IN SUPERTHRESHOLD CONDUCTION REGION AND SUBTHRESHOLD CONDUCTION REGION FOR DIFFERENT CLOCK FREQUENCIES

Frequency (KHz)	Power (nW)	
	Superthreshold Conduction Region	Subthreshold Conduction Region
1 K	612.57 n	0.007568 n
2 K	1123.05 n	0.009754 n
3 K	1659.57 n	0.012159 n
4 K	2197.10 n	0.014498 n
5 K	2720.06 n	0.016933 n

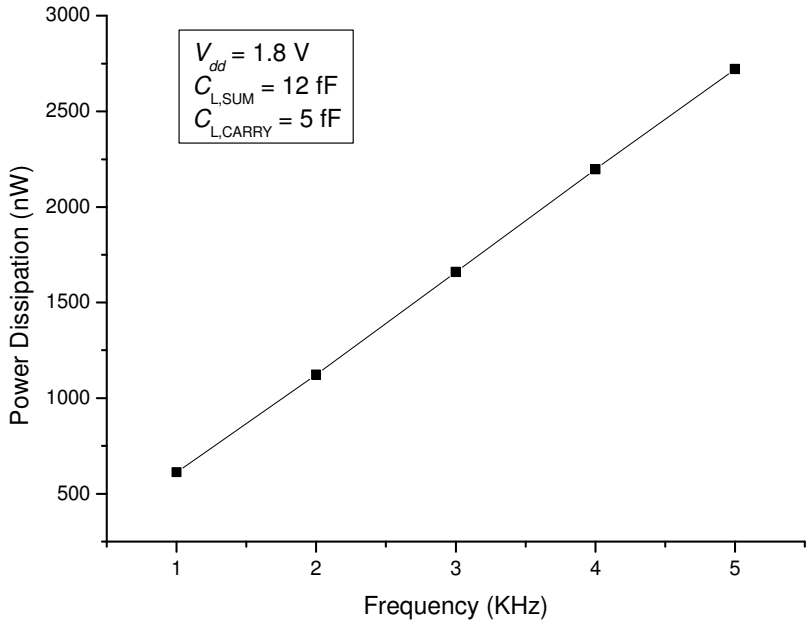

Figure 4.54: Power Dissipation Results for a Half Adder operating in superthreshold conduction region.

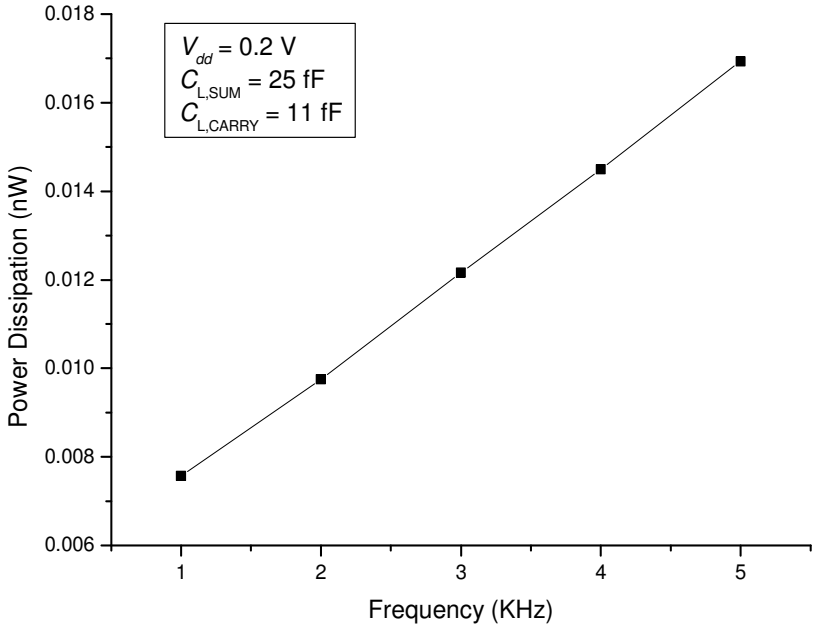

Figure 4.55: Power Dissipation Results for a Half Adder operating in subthreshold conduction region.

TABLE 4.10

AVERAGE DYNAMIC POWER DISSIPATED BY A 1-BIT FULL ADDER OPERATING IN SUPERTHRESHOLD CONDUCTION REGION AND SUBTHRESHOLD CONDUCTION REGION FOR DIFFERENT CLOCK FREQUENCIES

Frequency (KHz)	Power (nW)	
	Superthreshold Conduction Region	Subthreshold Conduction Region
1 K	315.97 n	0.012832 n
2 K	535.54 n	0.016520 n
3 K	766.75 n	0.020892 n
4 K	971.15 n	0.024413 n
5 K	1100.94 n	0.027932 n

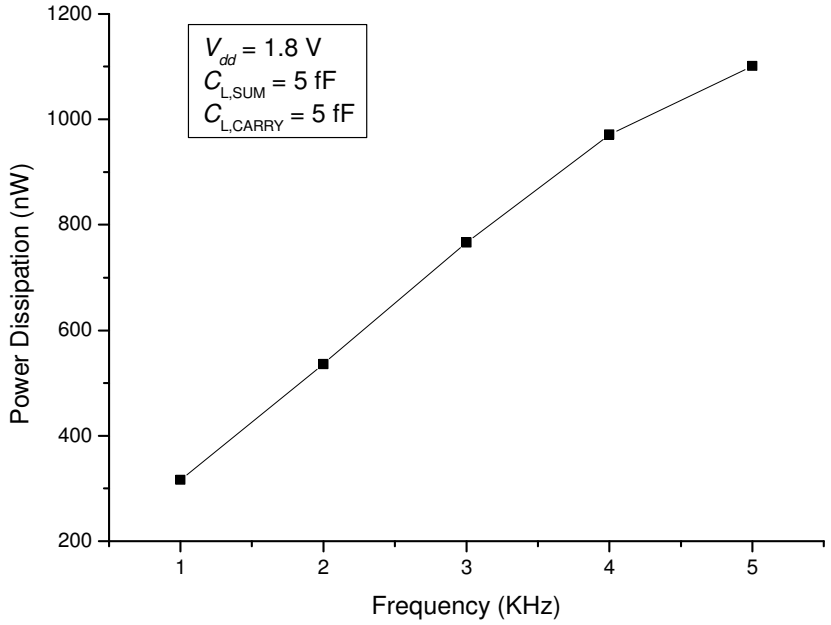

Figure 4.56: Power Dissipation Results for a 1-Bit Full Adder operating in superthreshold conduction region.

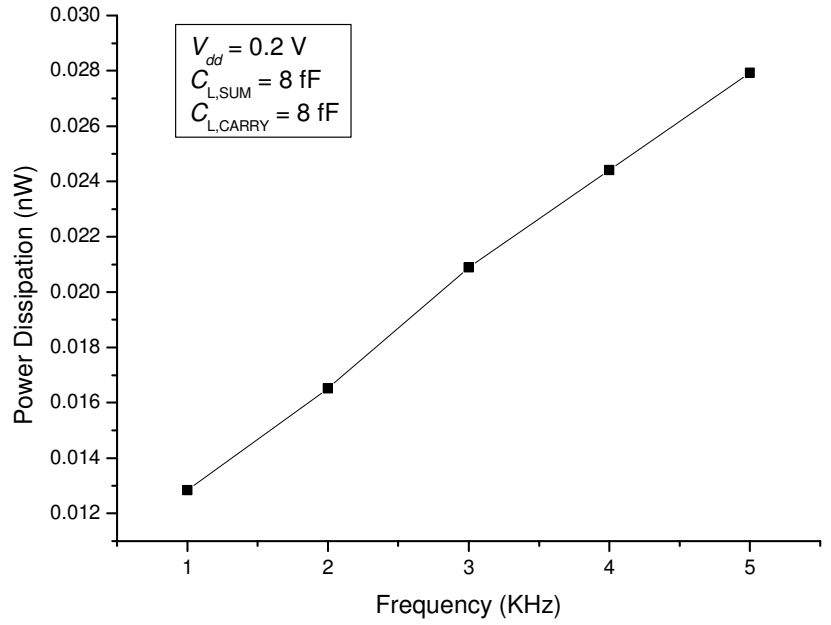

Figure 4.57: Power Dissipation Results for a 1-Bit Full Adder operating in subthreshold conduction region.

TABLE 4.11

AVERAGE DYNAMIC POWER DISSIPATED BY A 2-BIT MULTIPLIER OPERATING IN SUPERTHRESHOLD CONDUCTION REGION AND SUBTHRESHOLD CONDUCTION REGION FOR DIFFERENT CLOCK FREQUENCIES

Frequency (KHz)	Power (nW)	
	Superthreshold Conduction Region	Subthreshold Conduction Region
1 K	437.75 n	0.019279 n
2 K	842.20 n	0.023806 n
3 K	1241.10 n	0.028139 n
4 K	1639.26 n	0.032217 n
5 K	2048.98 n	0.036459 n

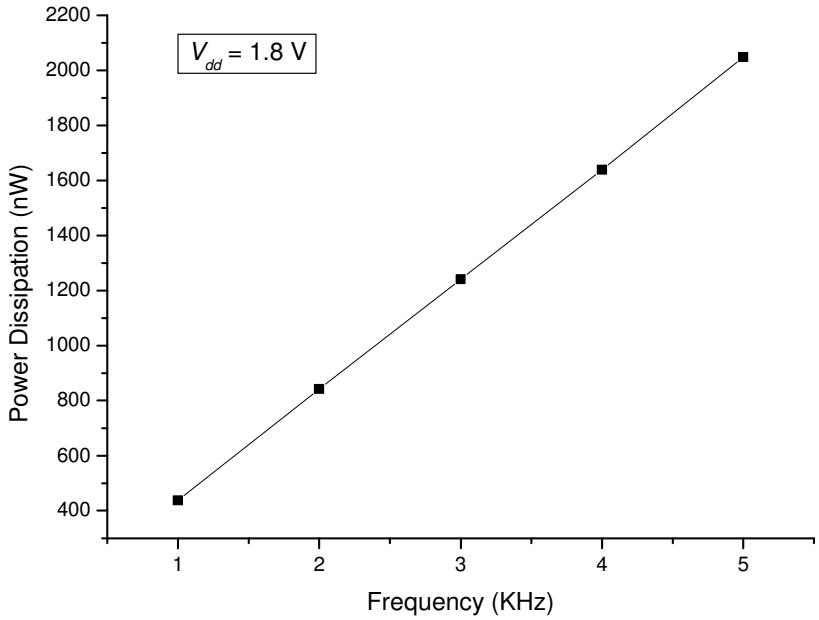

Figure 4.58: Power Dissipation Results for a 2-Bit Multiplier operating in superthreshold conduction region.

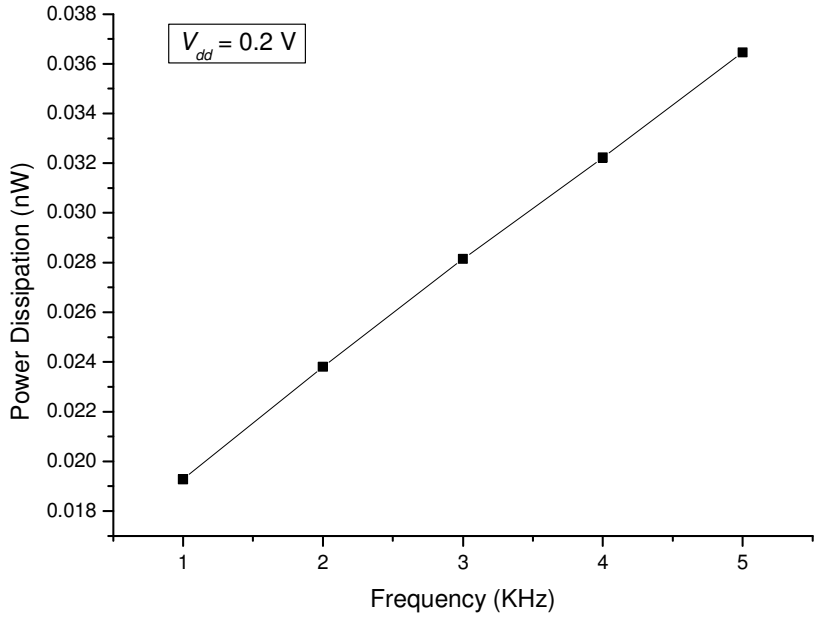

Figure 4.59: Power Dissipation Results for a 2-Bit Multiplier operating in subthreshold conduction region.

CHAPTER 5 LAYOUT DESIGN AND POST-LAYOUT SIMULATION RESULTS

5.1 WHAT IS LAYOUT DESIGN ?

Integrated Circuit (IC) Layout or mask design is the representation of an integrated circuit in terms of planar geometric shapes which correspond to the patterns of metal, oxide, or semiconductor layers that make up the components of the integrated circuit. In other words, Layout is the process by which a circuit *specification* is converted to a *physical implementation* with enough information to deduce all the relevant physical parameters of the circuit. A layout engineer's job is to place and connect all the components that make up a chip so that they meet all criteria.

The layout must pass a series of checks in a process, known as Verification, for its correctness. The two most common checks in the verification process are Design Rule Checking (DRC), and Layout Versus Schematic (LVS).

5.1.1 DESIGN RULE CHECKING

Design Rule Checking (DRC) is the area of Electronic Design Automation that determines whether a particular chip layout satisfies a series of recommended parameters called Design Rules. Design Rule Checking is a major step during Physical Verification of the design, which also involves LVS (Layout Versus Schematic) Check and ERC (Electrical Rule Check).

Design rules are a set of parameters provided by the semiconductor manufacturer that enable the designer to verify the correctness of the mask set. Design rules are specific to a particular semiconductor manufacturing process. A design rule set specifies a minimum size or spacing requirements between the layers of the same type or of different types. This provides a safety margin for various process variations, to ensure that the design will still have reasonable performance after the circuit is fabricated.

The main objective of design rule checking (DRC) is to achieve a high overall yield and reliability for the design. If the design rules are violated the design may not be functional. While design rule checks do not validate that the design will operate correctly, they are constructed to verify that the structure meets the process constraints for a given design type and process technology.

Mentor Graphics uses Standard Verification Rule Format (SVRF) language in their DRC rules files.

5.1.2 CMOS DESIGN RULES

Basic Design Rules are :

(1) Size Rules
(2) Separation Rules
(3) Overlap Rules

A listing of the design rules is available in the following file:
cad/Mentor_tools/ASIC_Design_Kit/adk3_1/technology/ic/process/tsmc018.calibre.rules

The most important design rules are summarized below (all distances are *minimum*):

Polysilicon Region Width	2λ	Poly - Poly Spacing	2λ
Polysilicon Gate Extension	2λ	Diffusion Region Width	2λ
Diffusion - Diffusion Spacing	3λ	Contact Extension	1λ
Metal 1 width	3λ	Metal 1 spacing	3λ
Metal 2 Width	3λ	Metal 2 spacing	4λ

5.1.3 LAYOUT VERSUS SCHEMATIC (LVS)

The Layout Versus Schematic (LVS) is the class of Electronic Design Automation (EDA) verification software that determines whether a particular integrated circuit layout corresponds to the original schematic of circuit diagram of the design.

A successful Design rule check (DRC) ensures that the layout conforms to the rules designed/required for faultless fabrication. However, it does not guarantee if it really represents the circuit you desire to fabricate. This is where an LVS check is used. LVS checking software recognizes the drawn shapes of the layout that represent the electrical components of the circuit, as well as the connections between them. The software then compares them with the schematic or circuit diagram.

5.2 PHYSICAL LAYOUT DESIGN OF DIFFERENT CMOS CIRCUITS

The physical layout design of different CMOS circuits has been done in standard TSMC 0.18 μm CMOS technology. For the project work, Mentor Graphics Corporation IC Station was used for the design of different physical layouts and an ELDO Simulator was used for all the validation of the physical layout designs.

This chapter discusses different physical layouts for all the proposed CMOS circuits, and LVS program was made to run for the comparison of the schematic to the physical layout structures.

5.2.1 LAYOUT DESIGN OF CMOS INVERTER OPERATING IN SUPERTHRESHOLD CONDUCTION REGION

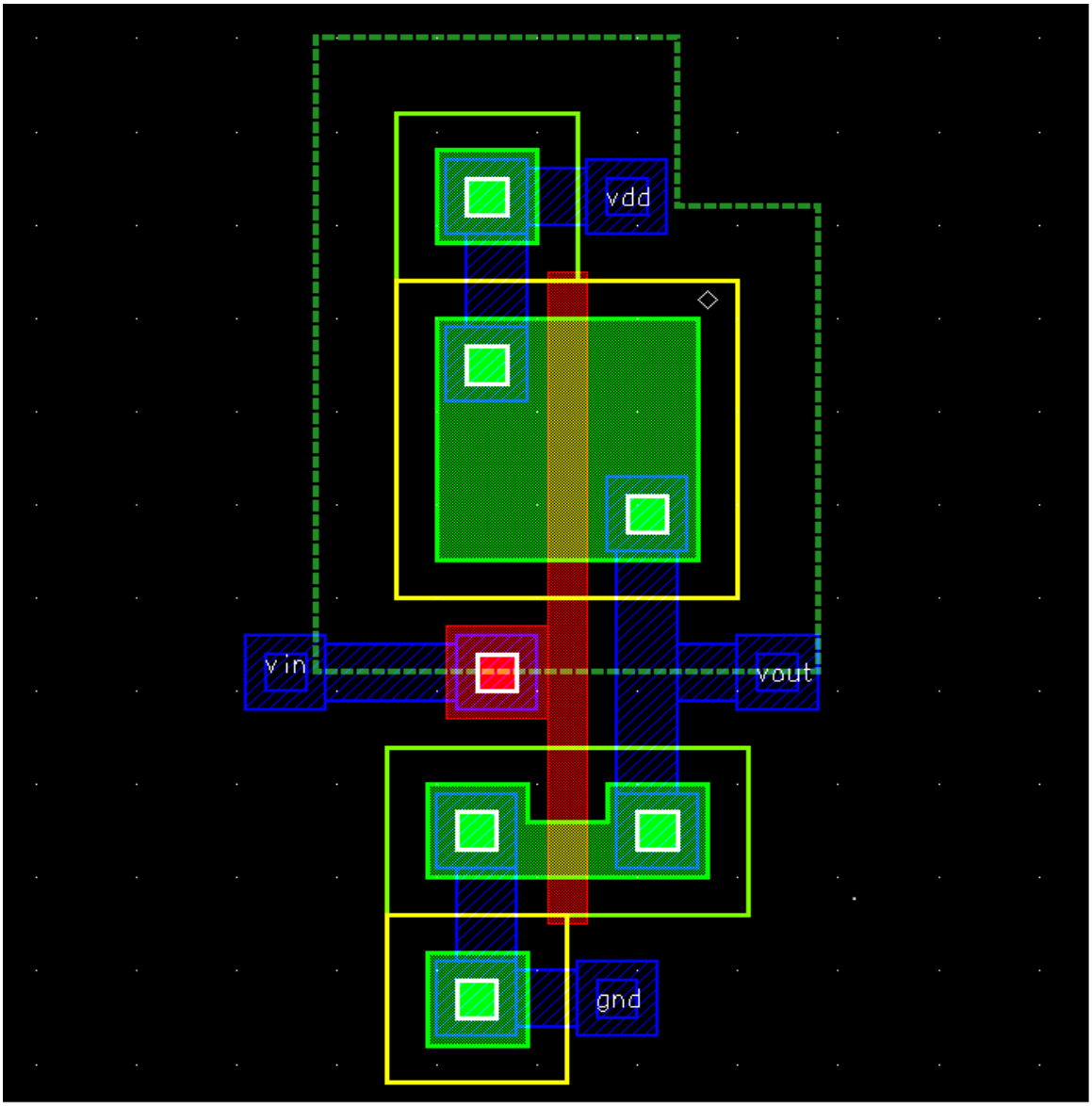

Figure 5.1: Layout of CMOS Inverter operating in superthreshold conduction region.

5.2.2 LAYOUT DESIGN OF CMOS INVERTER OPERATING IN SUBTHRESHOLD CONDUCTION REGION

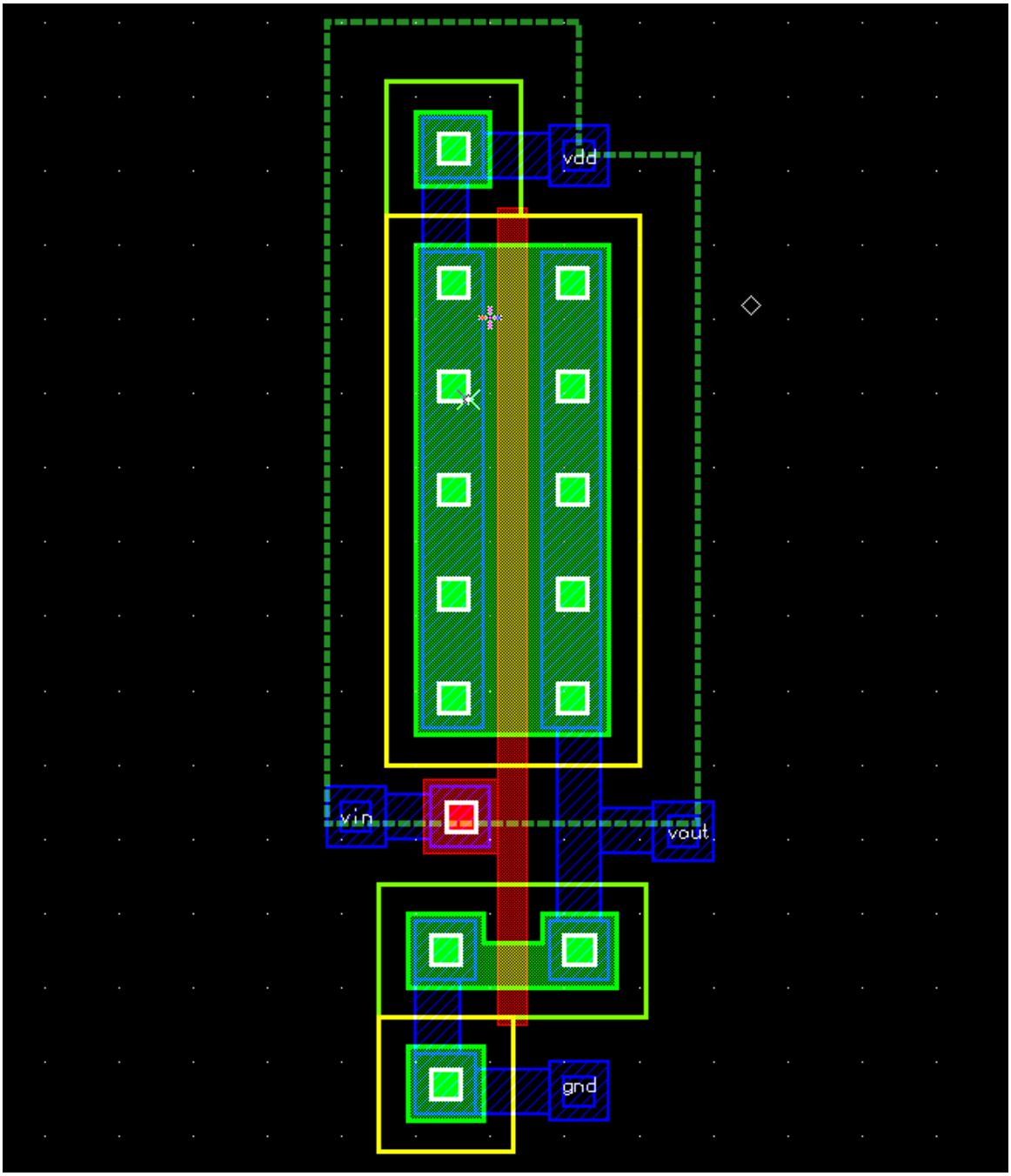

Figure 5.2: Layout of CMOS Inverter operating in Subthreshold conduction region.

5.2.3 LAYOUT DESIGN OF TWO-INPUT CMOS NAND GATE OPERATING IN SUPERTHRESHOLD CONDUCTION REGION

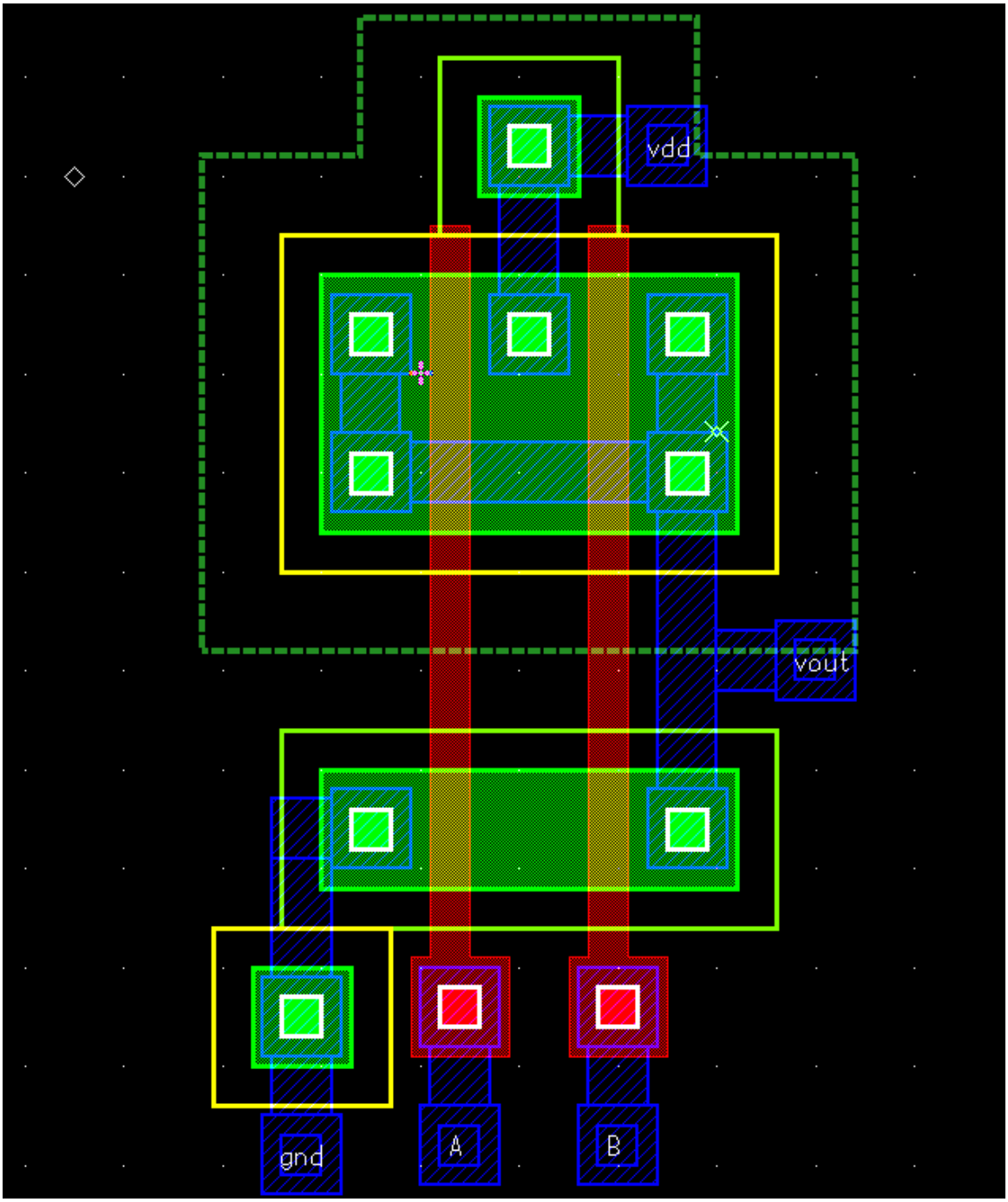

Figure 5.3: **Layout of Two-Input CMOS NAND Gate operating in superthreshold conduction region.**

5.2.4 LAYOUT DESIGN OF TWO-INPUT CMOS NAND GATE OPERATING IN SUBTHRESHOLD CONDUCTION REGION

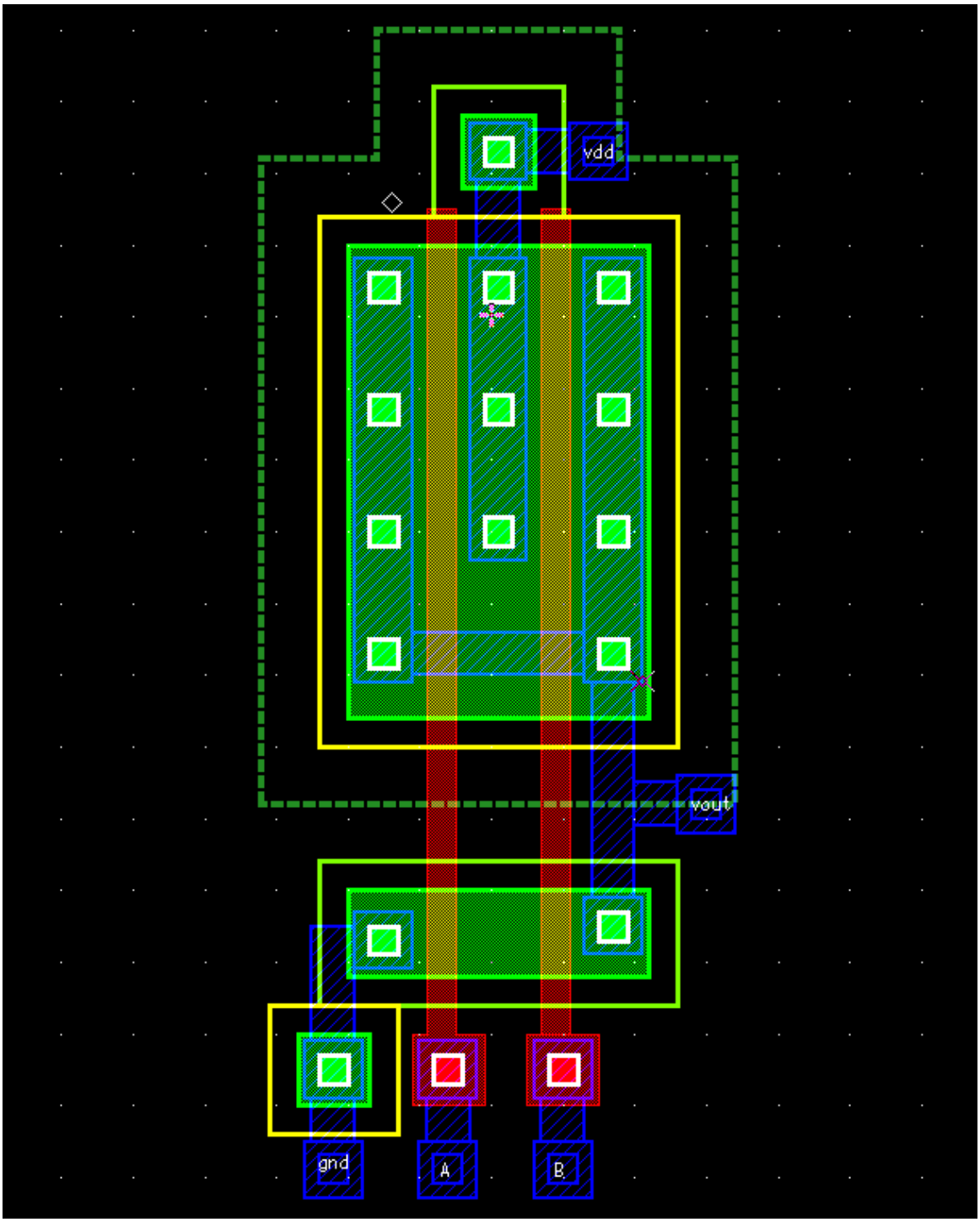

Figure 5.4: **Layout of Two-Input CMOS NAND Gate operating in subthreshold conduction region.**

5.2.5 LAYOUT DESIGN OF TWO-INPUT CMOS NOR GATE OPERATING IN SUPERTHRESHOLD CONDUCTION REGION

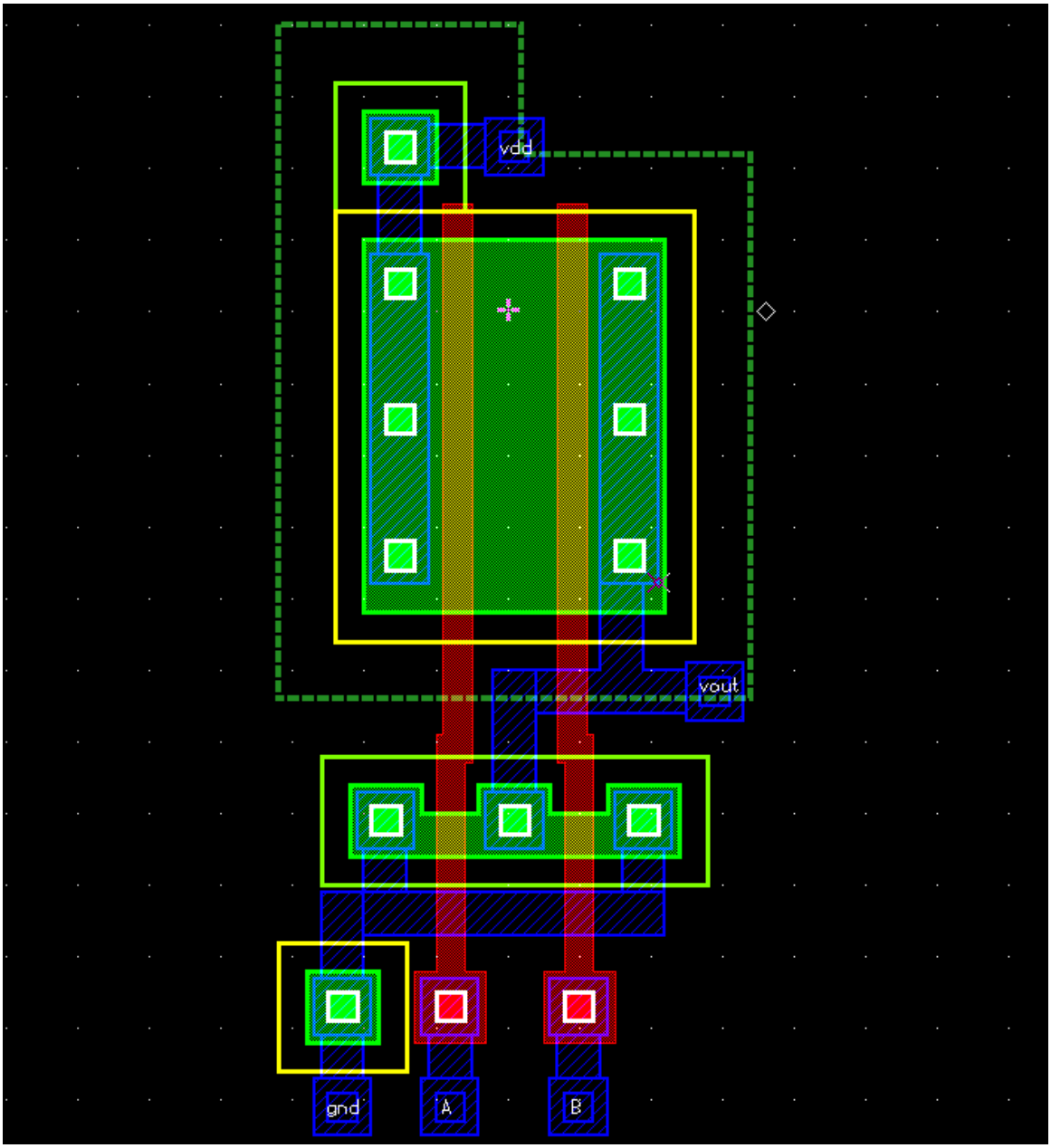

Figure 5.5: **Layout of Two-Input CMOS NOR Gate operating in superthreshold conduction region.**

5.2.6 LAYOUT DESIGN OF TWO-INPUT CMOS NOR GATE OPERATING IN SUBTHRESHOLD CONDUCTION REGION

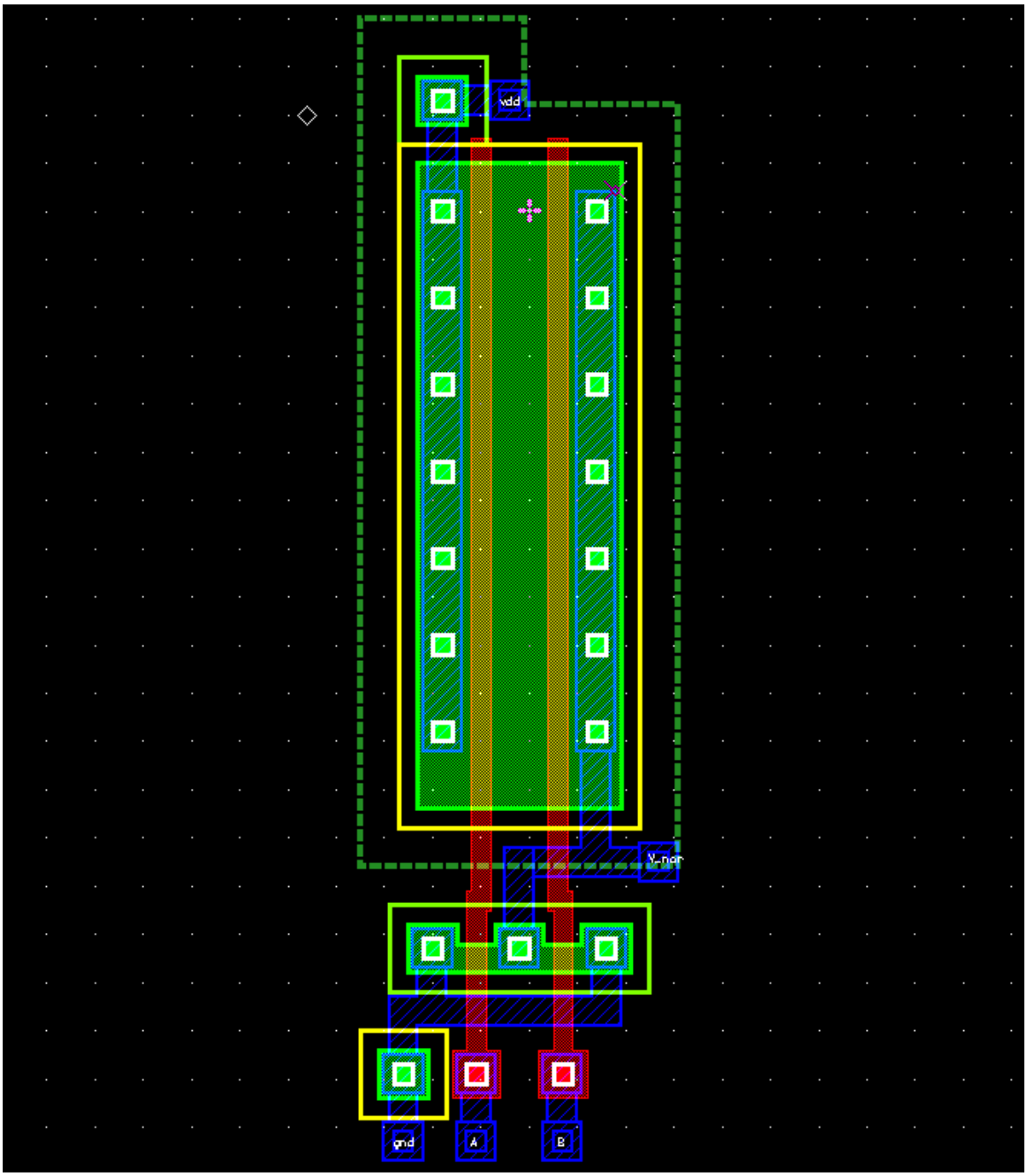

Figure 5.6: **Layout of Two-Input CMOS NOR Gate operating in subthreshold conduction region.**

5.2.7 LAYOUT DESIGN OF TWO-INPUT CMOS AND GATE OPERATING IN SUPERTHRESHOLD CONDUCTION REGION

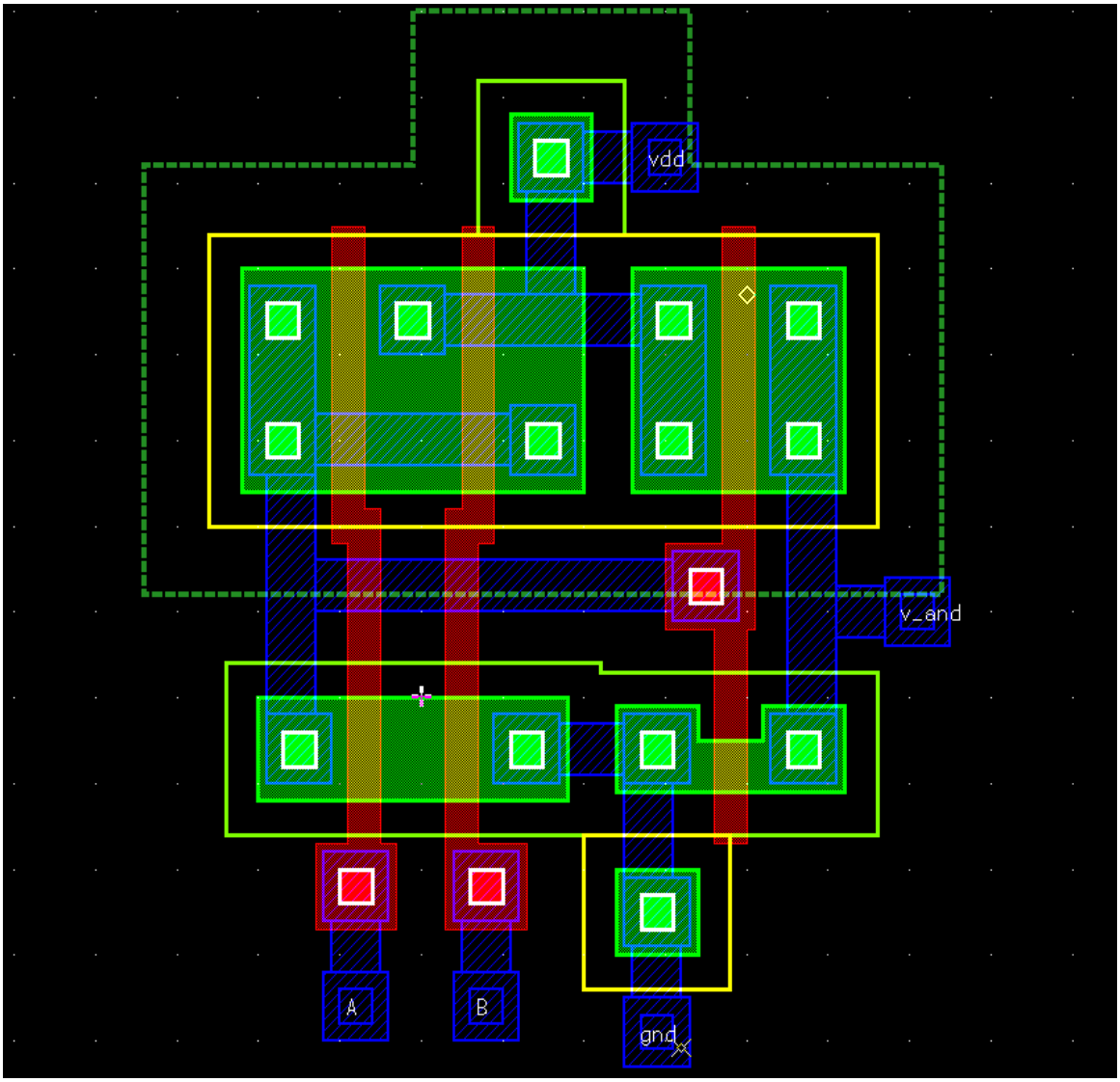

Figure 5.7: Layout of Two-Input CMOS AND Gate operating in superthreshold conduction region.

5.2.8 LAYOUT DESIGN OF TWO-INPUT CMOS AND GATE OPERATING IN SUBTHRESHOLD CONDUCTION REGION

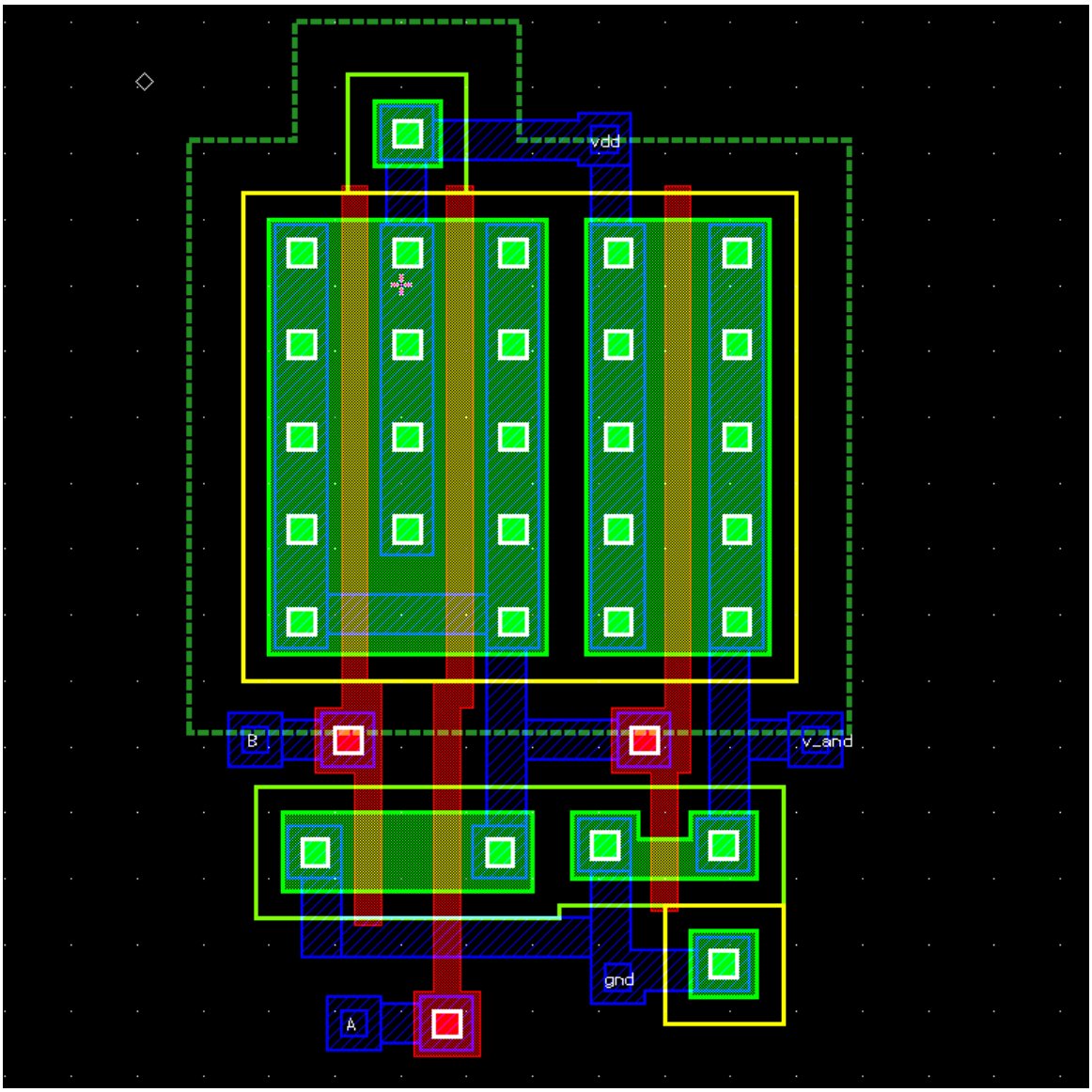

Figure 5.8: Layout of Two-Input CMOS AND Gate operating in subthreshold conduction region.

5.2.9 LAYOUT DESIGN OF TWO-INPUT CMOS XOR GATE OPERATING IN SUPERTHRESHOLD CONDUCTION REGION

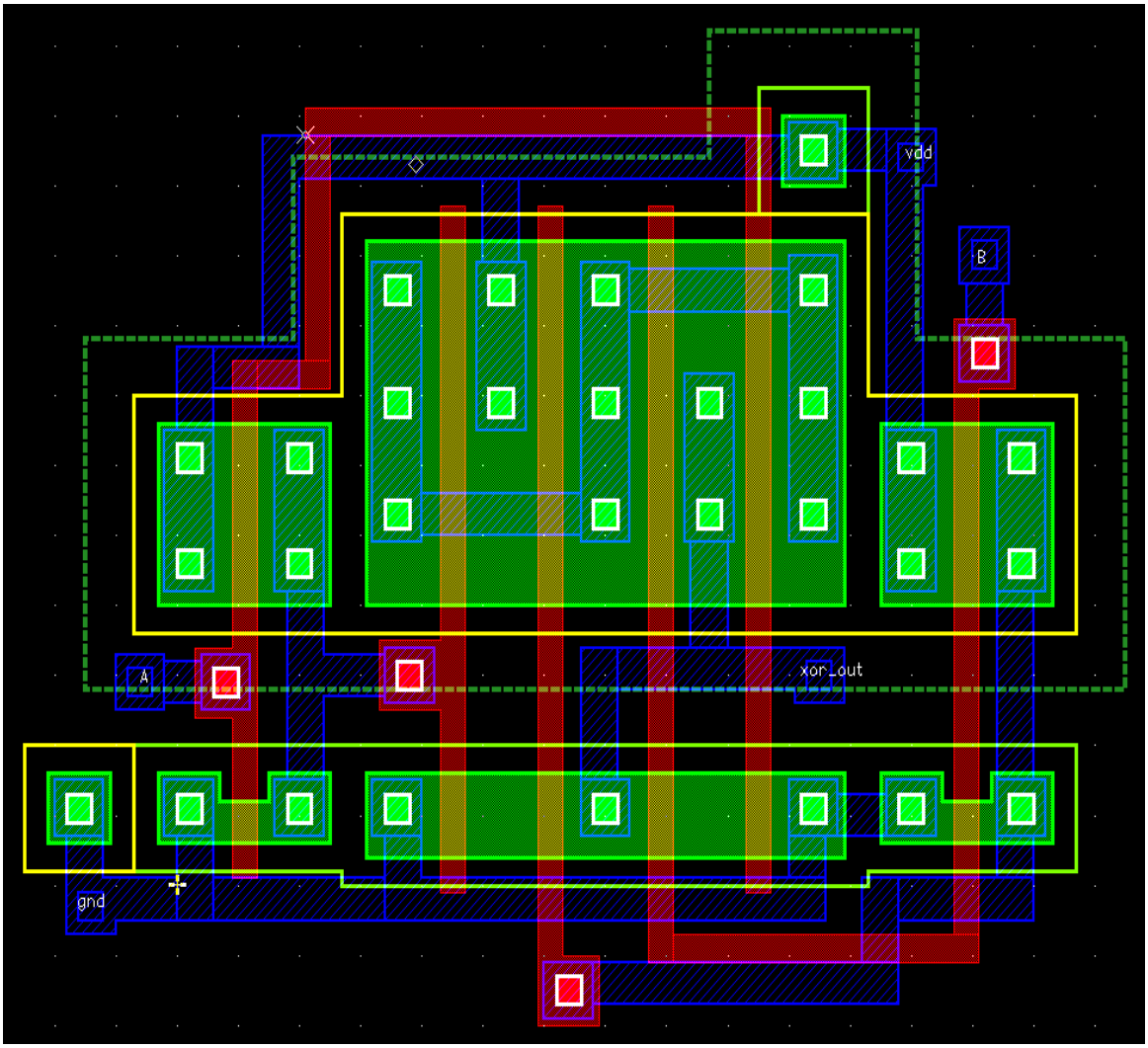

Figure 5.9: **Layout of Two-Input CMOS XOR Gate operating in superthreshold conduction region.**

5.2.10 LAYOUT DESIGN OF TWO-INPUT CMOS XOR GATE OPERATING IN SUBTHRESHOLD CONDUCTION REGION

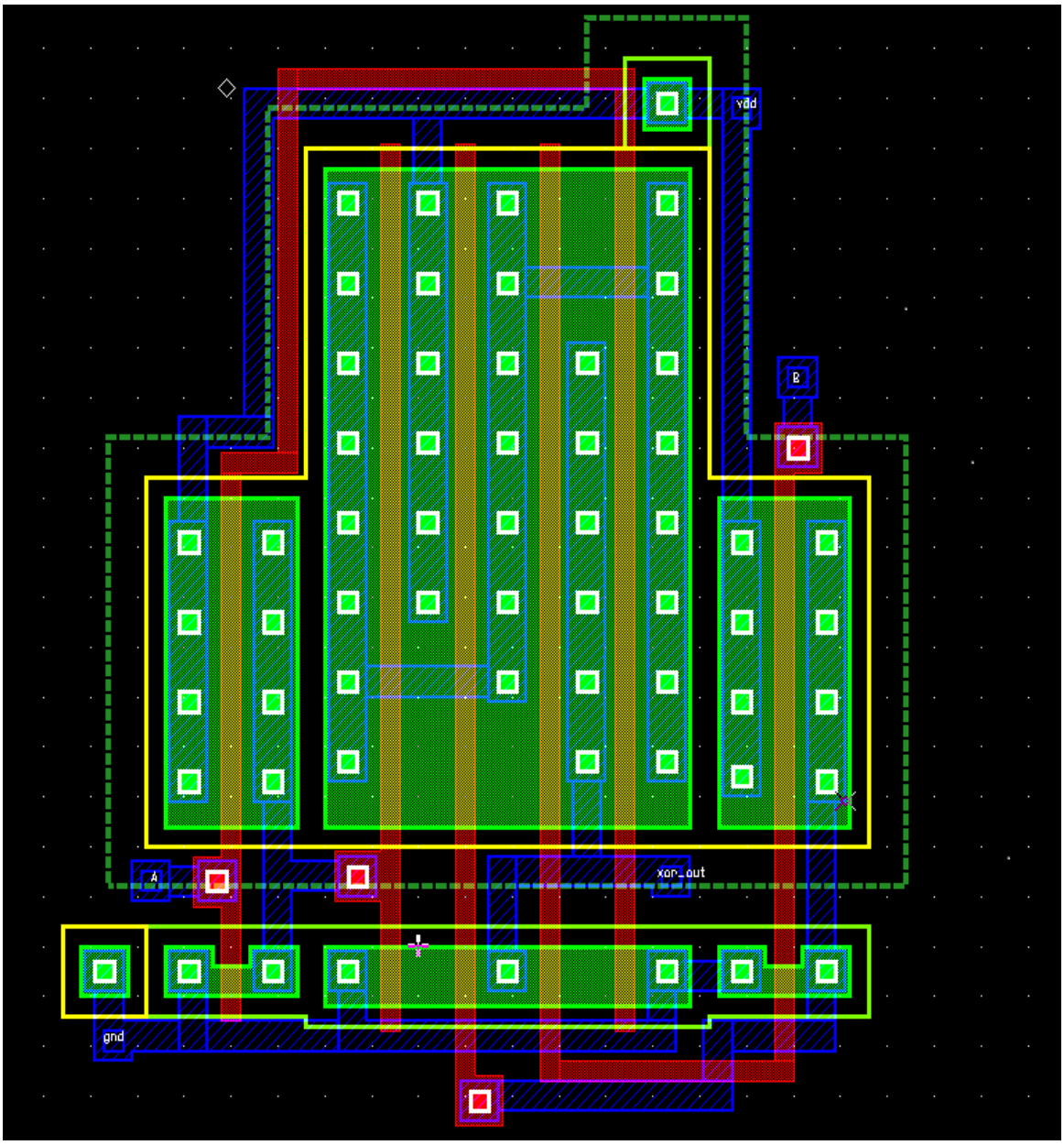

Figure 5.10: Layout of Two-Input CMOS XOR Gate operating in subthreshold conduction region.

5.2.11 LAYOUT DESIGN OF THREE-INPUT CMOS AND GATE OPERATING IN SUPERTHRESHOLD CONDUCTION REGION

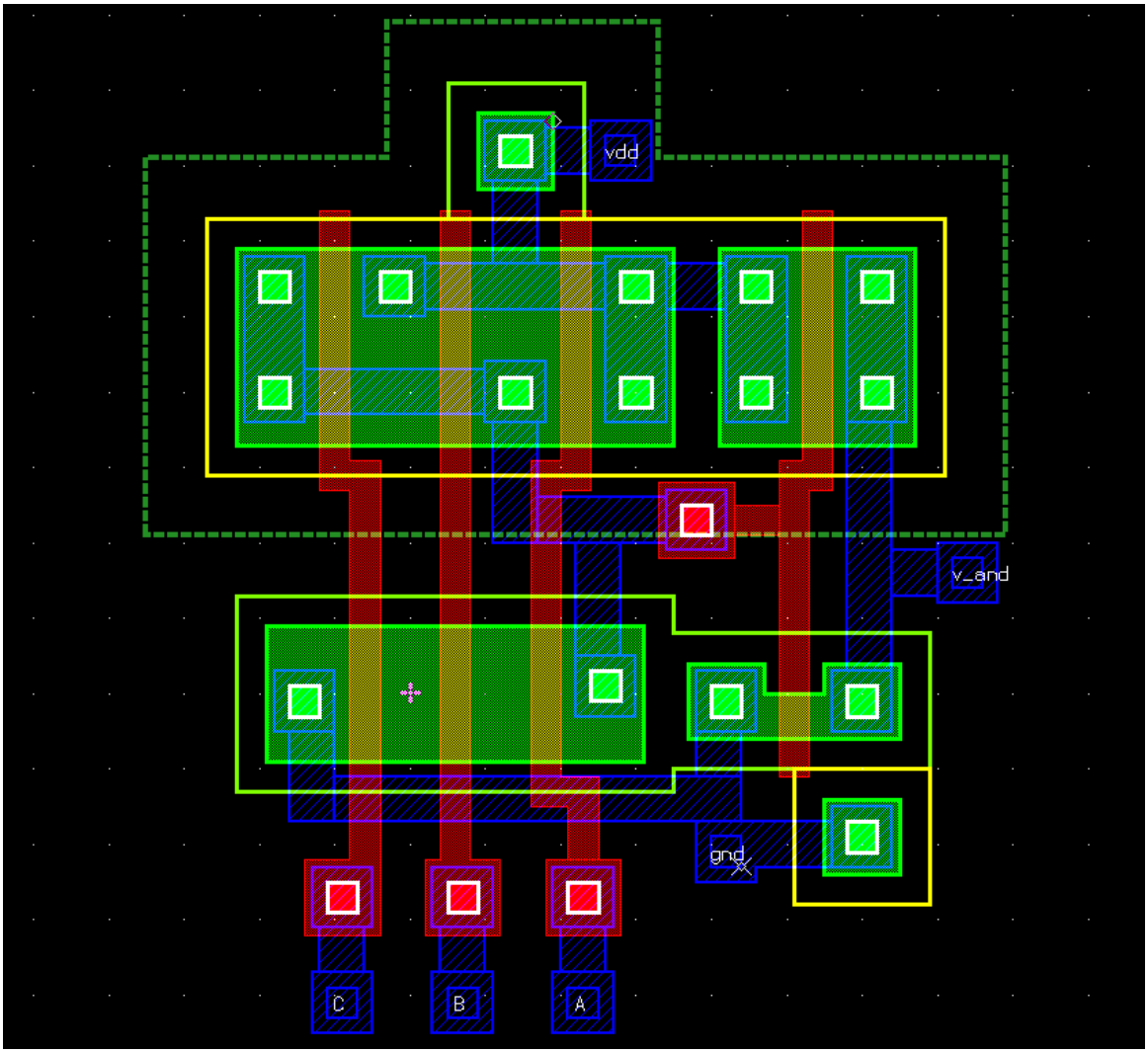

Figure 5.11: Layout of Three-Input CMOS AND Gate operating in superthreshold conduction region.

5.2.12 LAYOUT DESIGN OF THREE-INPUT CMOS AND GATE OPERATING IN SUBTHRESHOLD CONDUCTION REGION

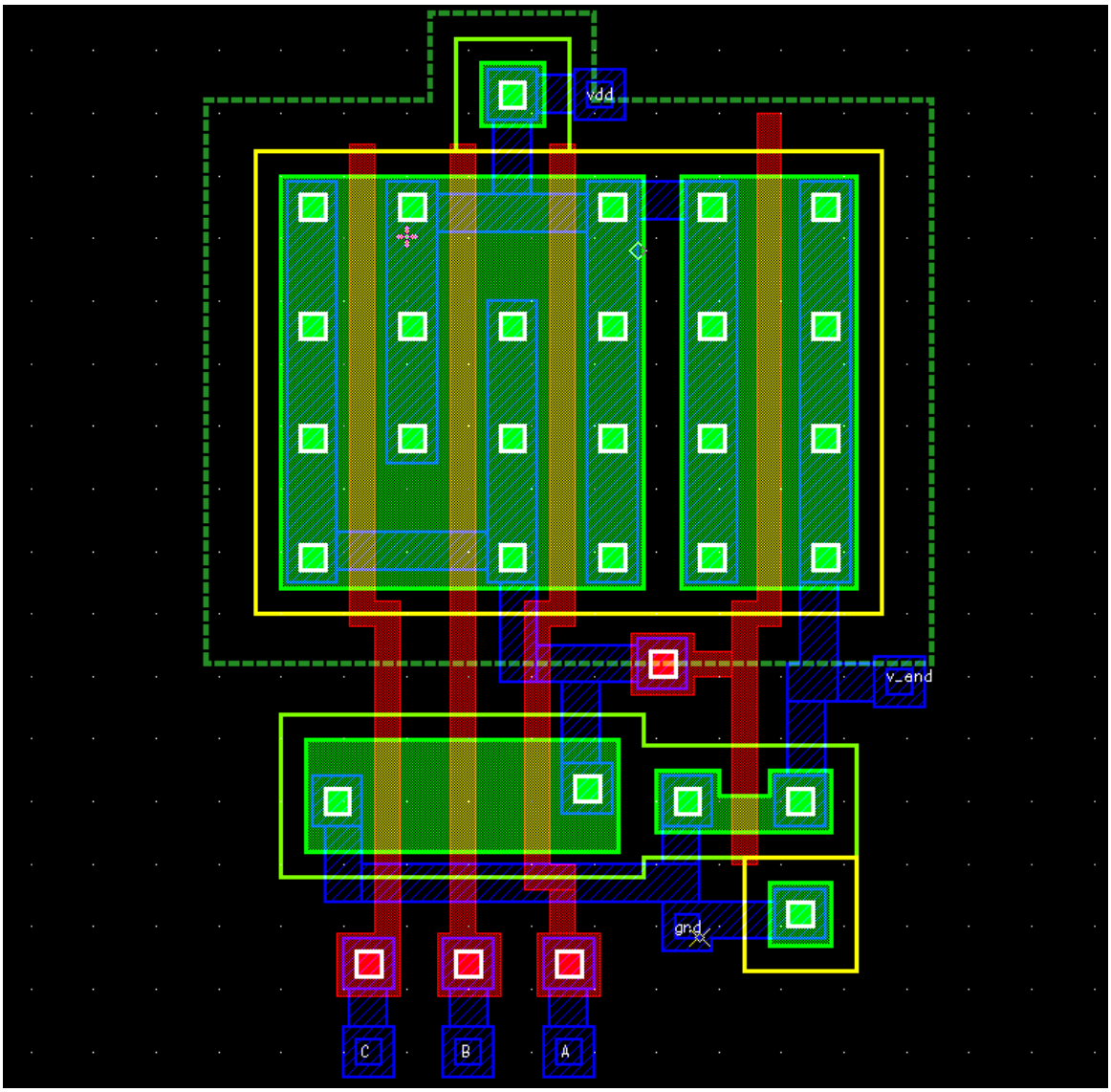

Figure 5.12: Layout of Three-Input CMOS AND Gate operating in subthreshold conduction region.

5.2.13 LAYOUT DESIGN OF THREE-INPUT CMOS OR GATE OPERATING IN SUPERTHRESHOLD CONDUCTION REGION

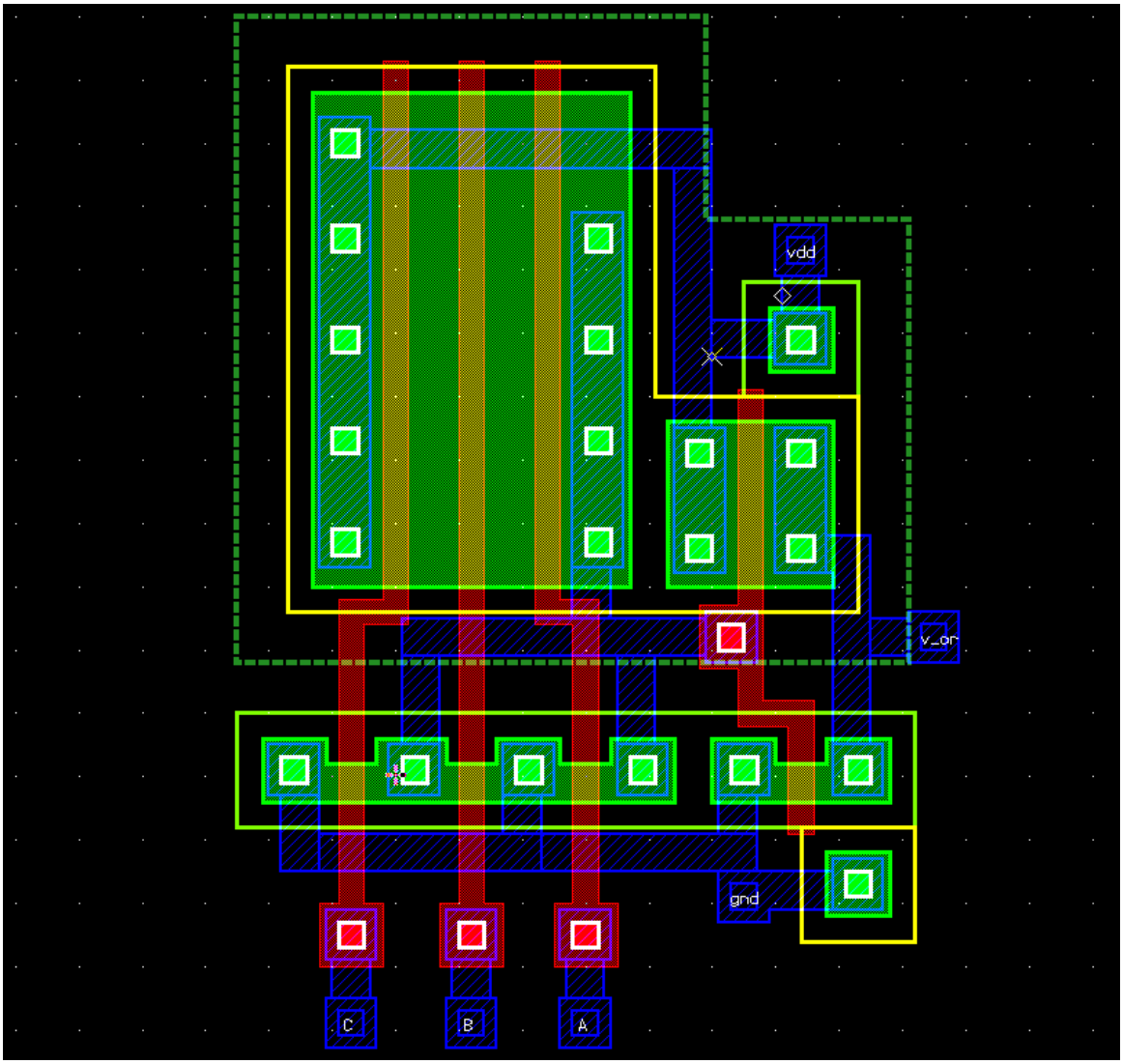

Figure 5.13: Layout of Three-Input CMOS OR Gate operating in superthreshold conduction region.

5.2.14 LAYOUT DESIGN OF THREE-INPUT CMOS OR GATE OPERATING IN SUBTHRESHOLD CONDUCTION REGION

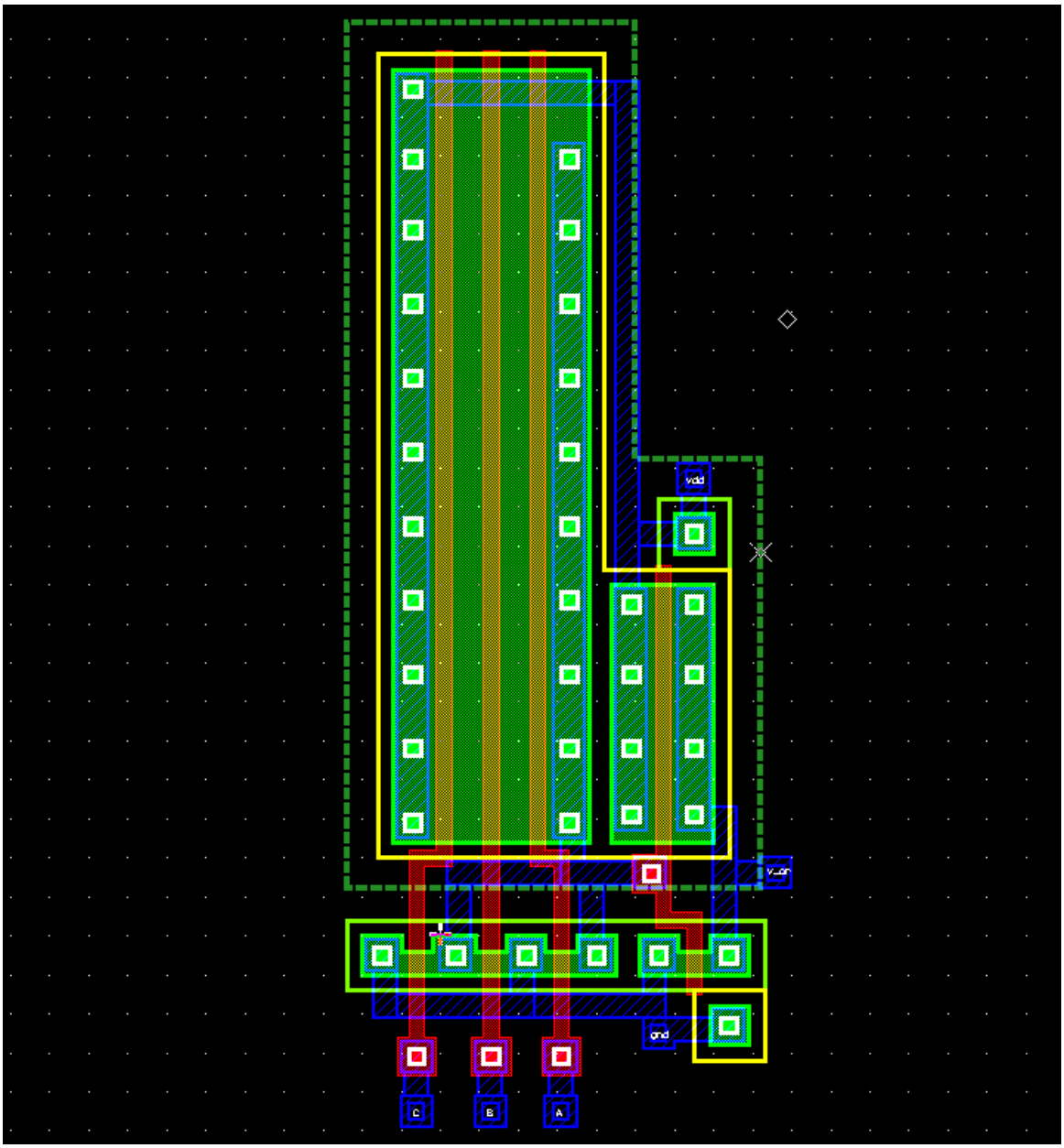

Figure 5.14: Layout of Three-Input CMOS OR Gate operating in subthreshold conduction region.

5.2.15 LAYOUT DESIGN OF 2-TO-1 CMOS MULTIPLEXER OPERATING IN SUPERTHRESHOLD CONDUCTION REGION

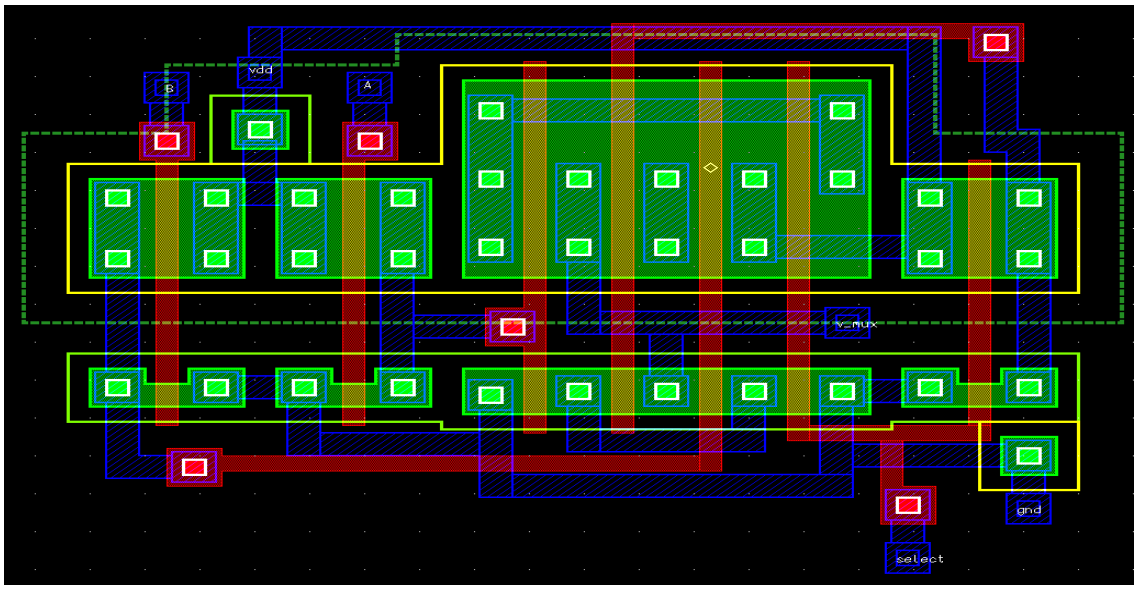

Figure 5.15: Layout of 2-to-1 CMOS Multiplexer operating in superthreshold conduction region.

5.2.16 LAYOUT DESIGN OF 2-TO-1 CMOS MULTIPLEXER OPERATING IN SUBTHRESHOLD CONDUCTION REGION

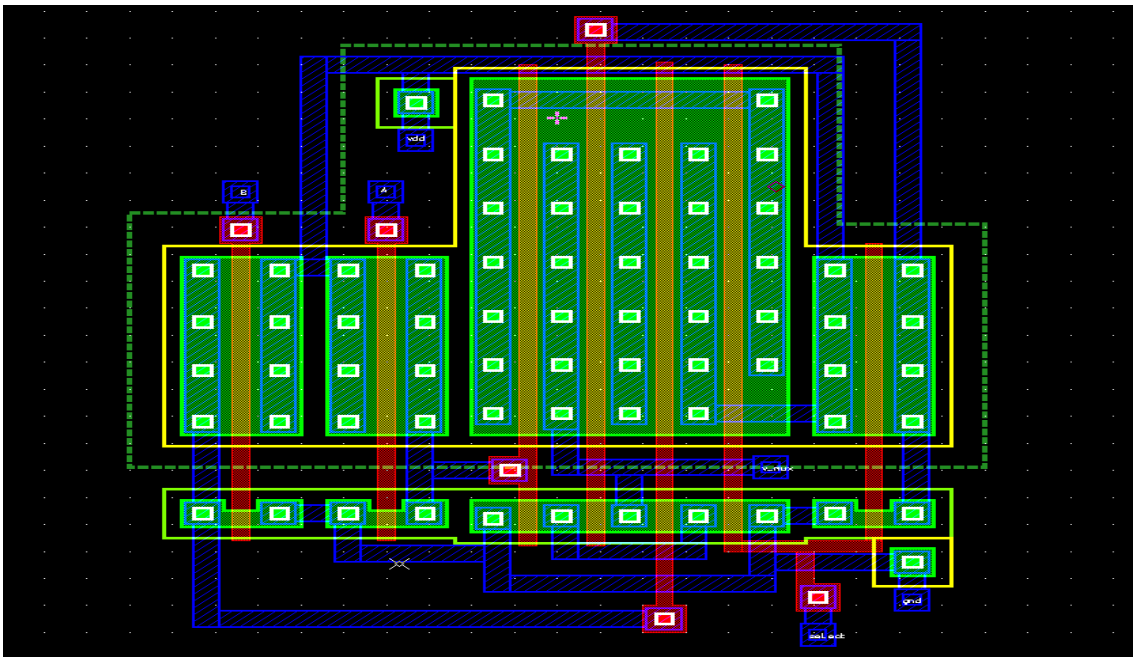

Figure 5.16: Layout of 2-to-1 CMOS Multiplexer operating in subthreshold conduction region.

5.2.17 LAYOUT DESIGN OF CMOS HALF ADDER OPERATING IN SUPERTHRESHOLD CONDUCTION REGION

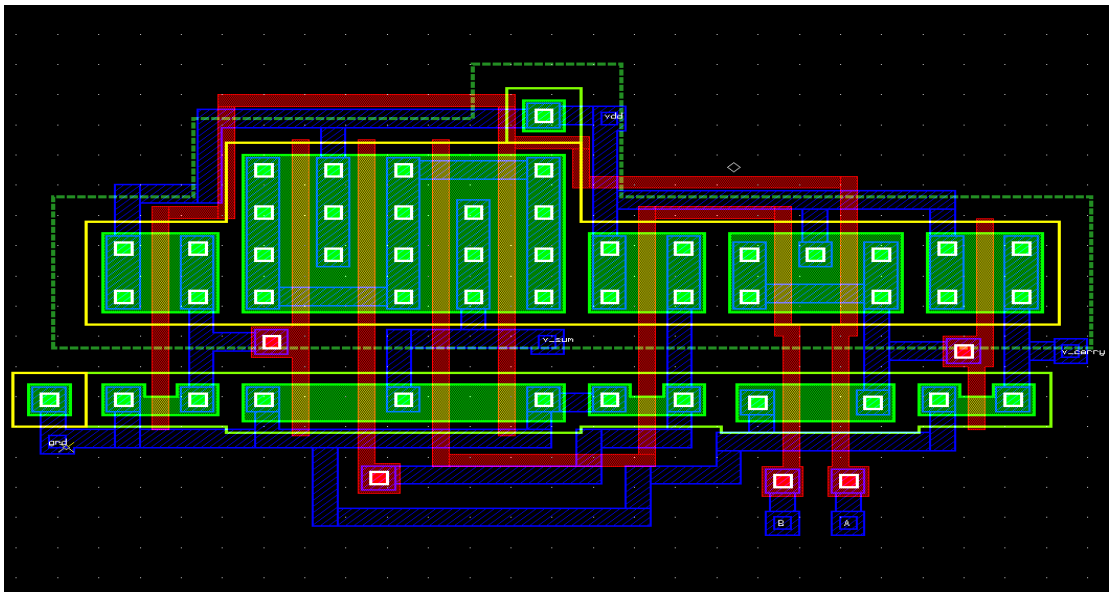

Figure 5.17: Layout of CMOS Half Adder operating in superthreshold conduction region.

5.2.18 LAYOUT DESIGN OF CMOS HALF ADDER OPERATING IN SUBTHRESHOLD CONDUCTION REGION

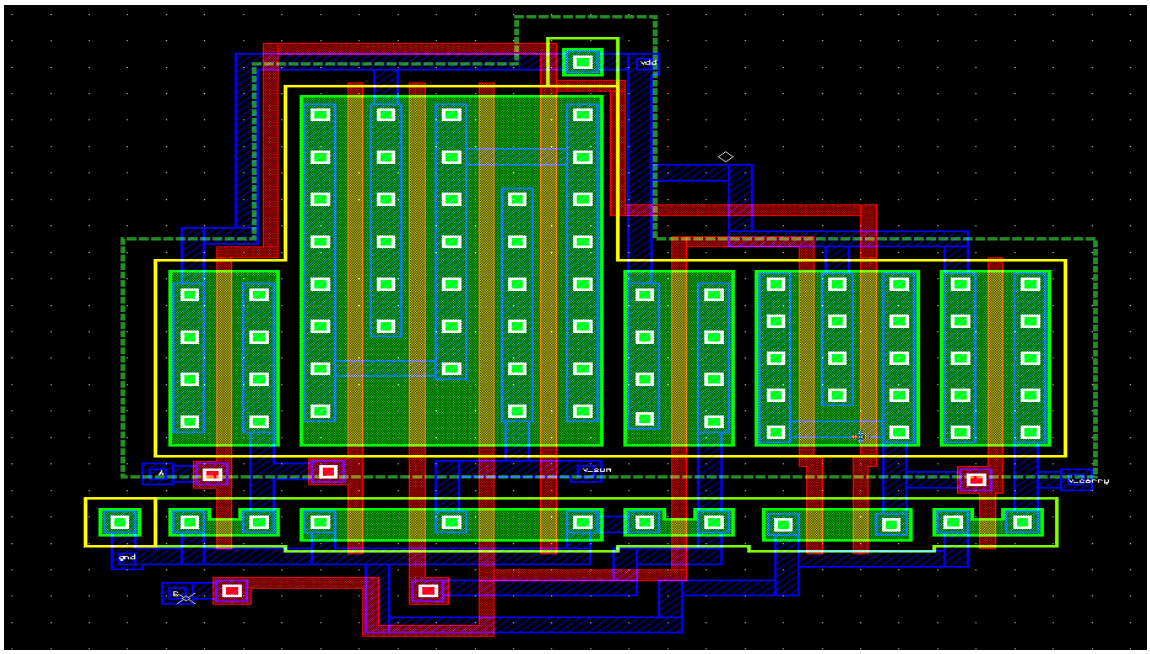

Figure 5.18: Layout of CMOS Half Adder operating in subthreshold conduction region.

5.2.19 LAYOUT DESIGN OF ONE-BIT CMOS FULL ADDER OPERATING IN SUPERTHRESHOLD CONDUCTION REGION

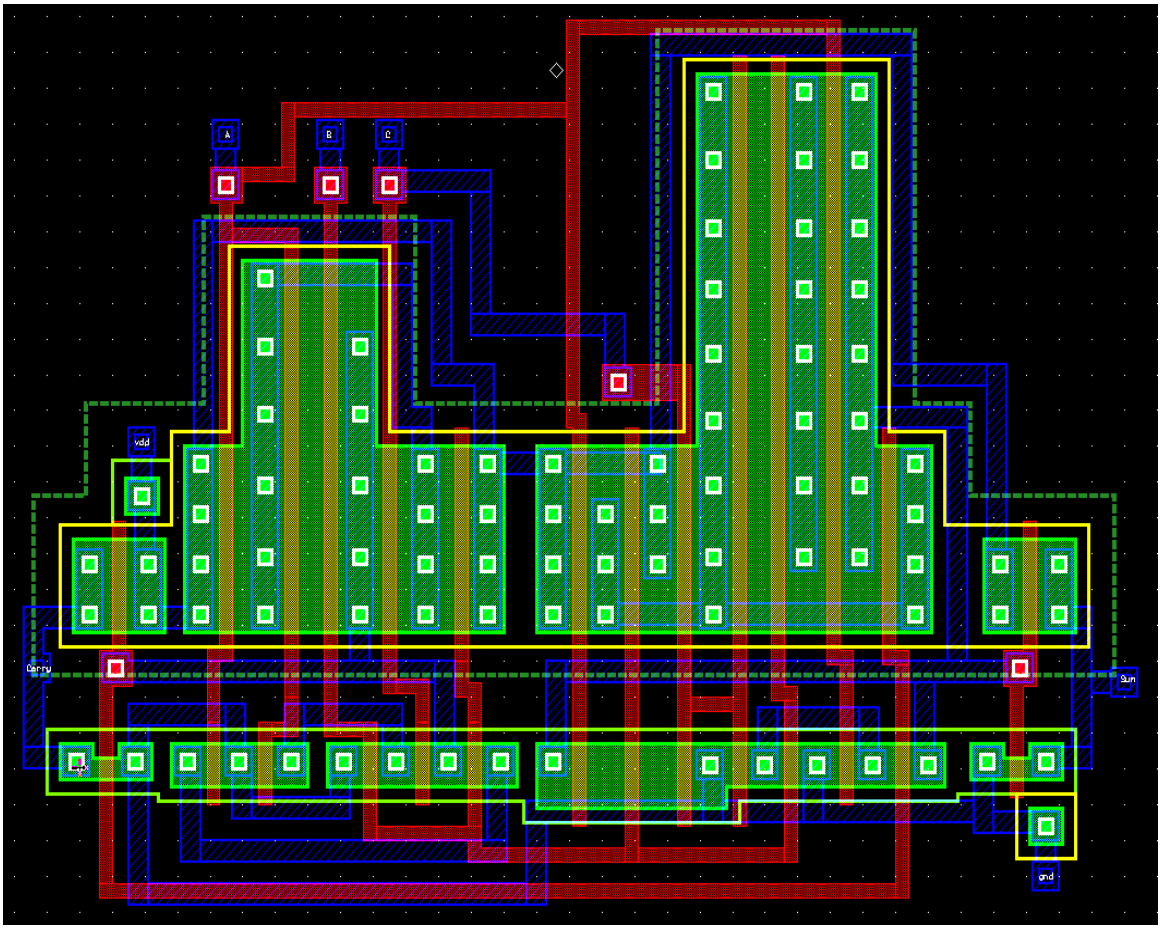

Figure 5.19: Layout of One-Bit CMOS Full Adder operating in superthreshold conduction region.

5.2.20 LAYOUT DESIGN OF ONE-BIT CMOS FULL ADDER OPERATING IN SUBTHRESHOLD CONDUCTION REGION

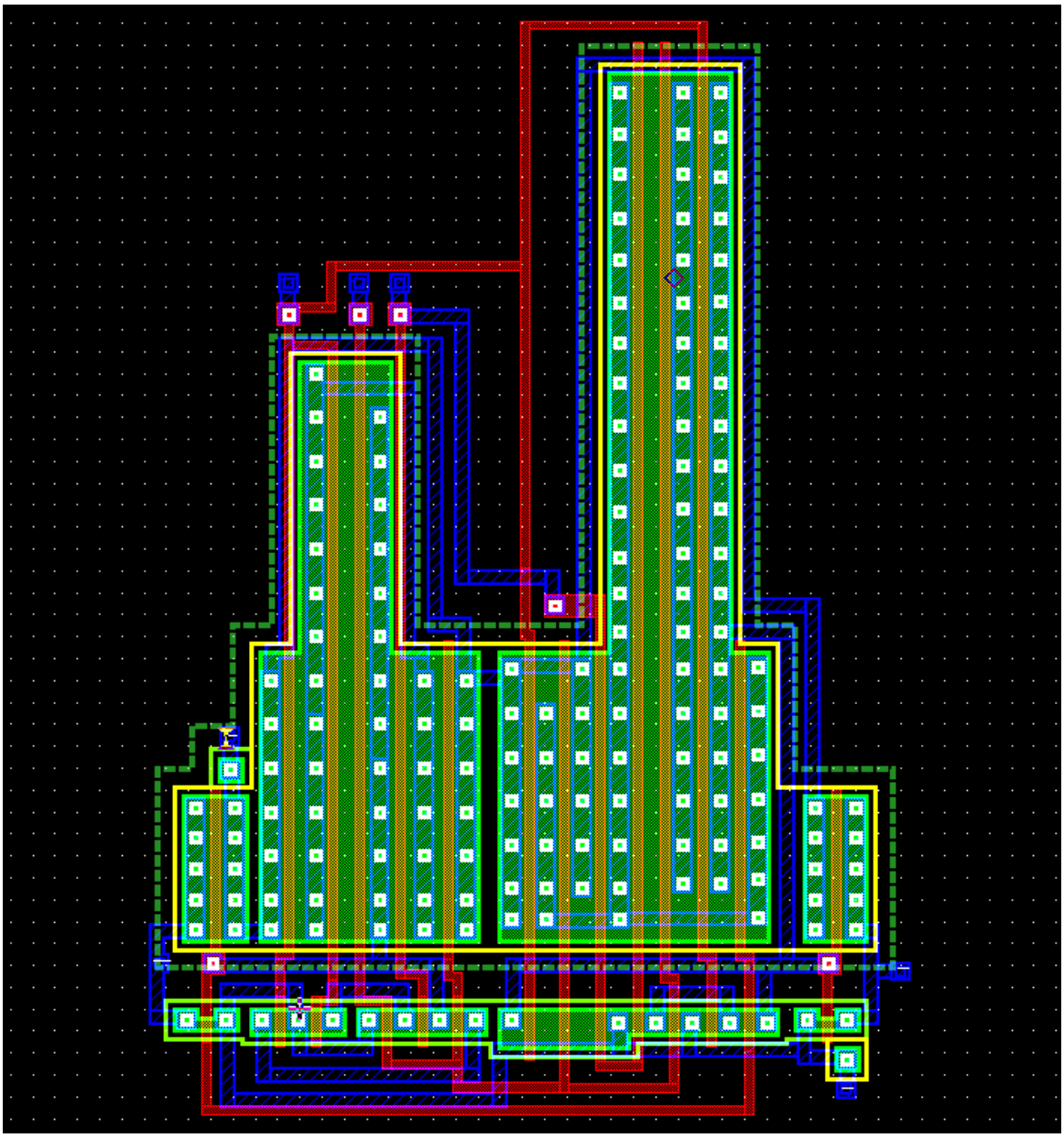

Figure 5.20: Layout of One-Bit CMOS Full Adder operating in subthreshold conduction region.

5.2.21 LAYOUT DESIGN OF TWO-BIT MULTIPLIER OPERATING IN SUPERTHRESHOLD CONDUCTION REGION

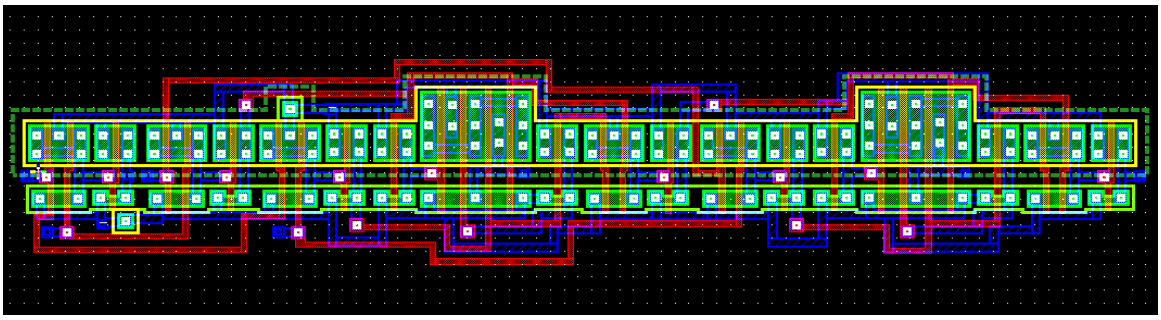

Figure 5.21: Layout of Two-Bit Multiplier operating in superthreshold conduction region.

5.2.22 LAYOUT DESIGN OF TWO-BIT MULTIPLIER OPERATING IN SUBTHRESHOLD CONDUCTION REGION

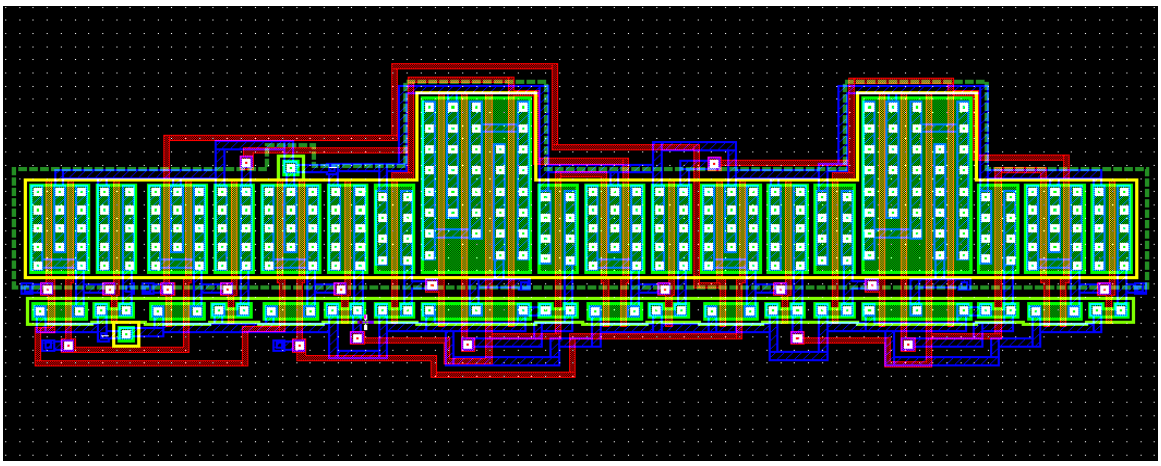

Figure 5.22: Layout of Two-Bit Multiplier operating in subthreshold conduction region.

5.3 POST - LAYOUT SIMULATIONS

After completing the physical layout design of all the structures, they are matched with schematic using LVS simulation. With the successful run of LVS, parasitic and layout netlist extraction simulation have been done using PEX. Post Layout simulations have been done on extracted netlist. The simulation results of post layout simulations are as given below.

5.3.1 POST - LAYOUT SIMULATION RESULTS FOR CMOS INVERTER

Figure 5.23 and Figure 5.24 show the post-layout results of the DC analysis for a minimum sized CMOS Inverter.

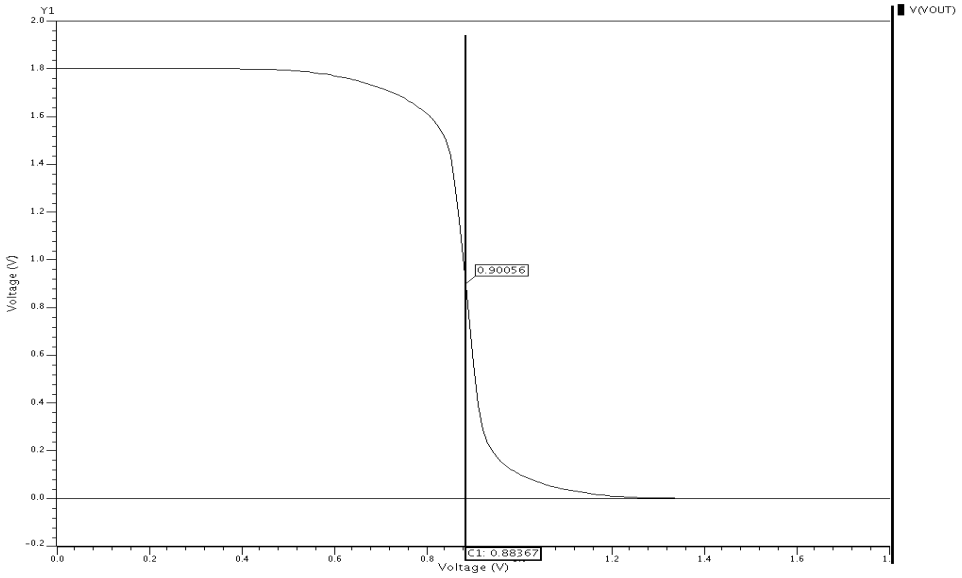

Figure 5.23: Post-Layout Simulation – DC analysis for CMOS Inverter operating in superthreshold conduction region.

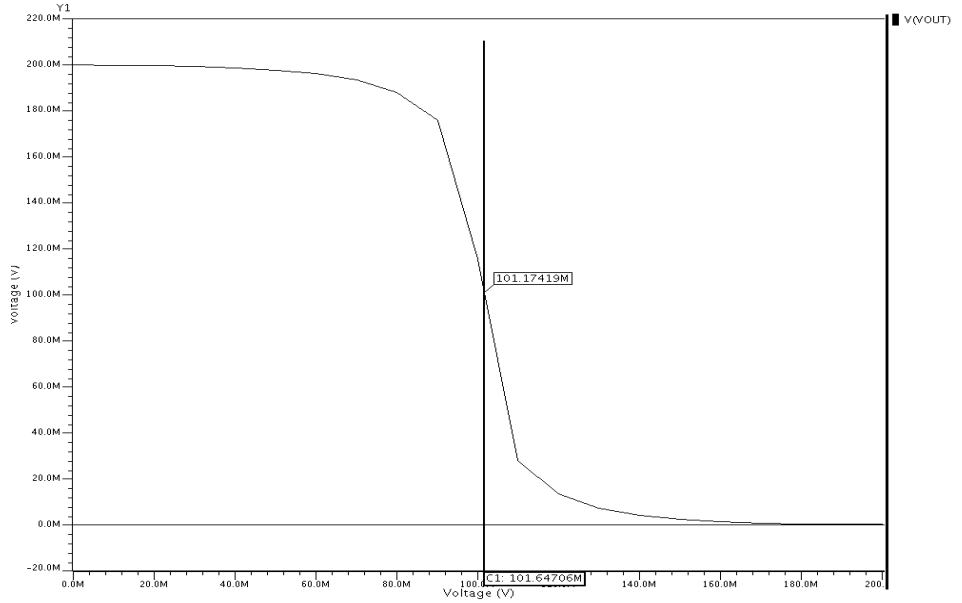

Figure 5.24: Post-Layout Simulation – DC analysis for CMOS Inverter operating in subthreshold conduction region.

Figure 5.25 and Figure 5.26 show the post-layout results of the transient analysis for a minimum sized CMOS Inverter.

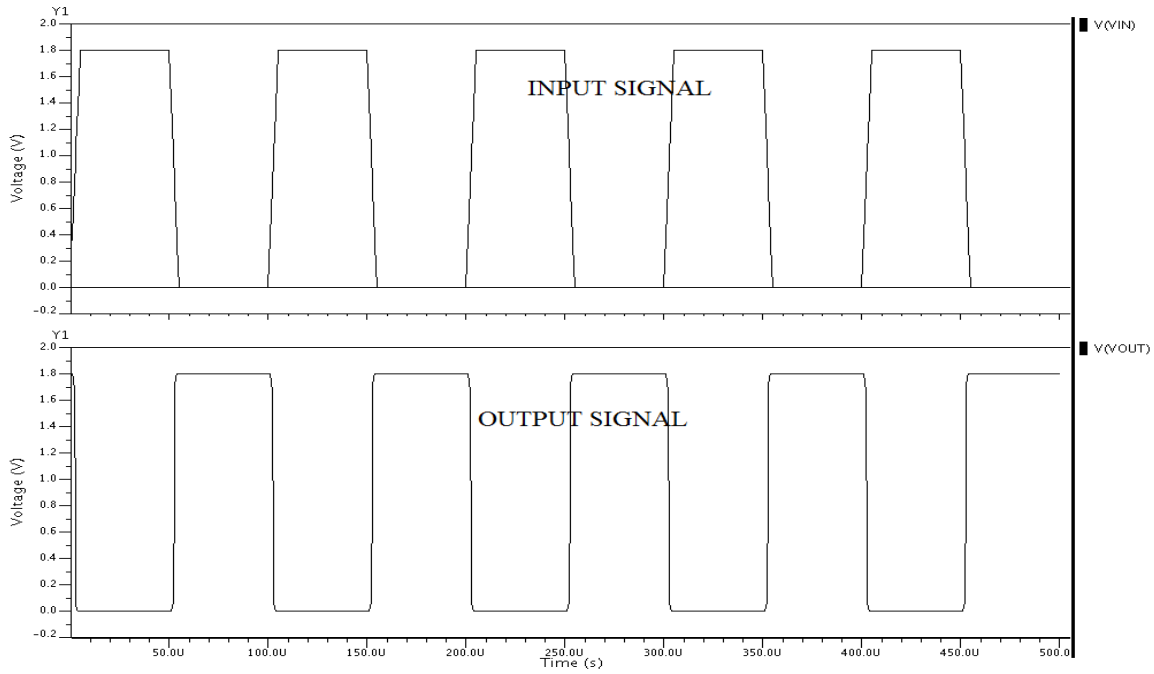

Figure 5.25: Post-Layout Simulation – Transient analysis for CMOS Inverter operating in superthreshold conduction region.

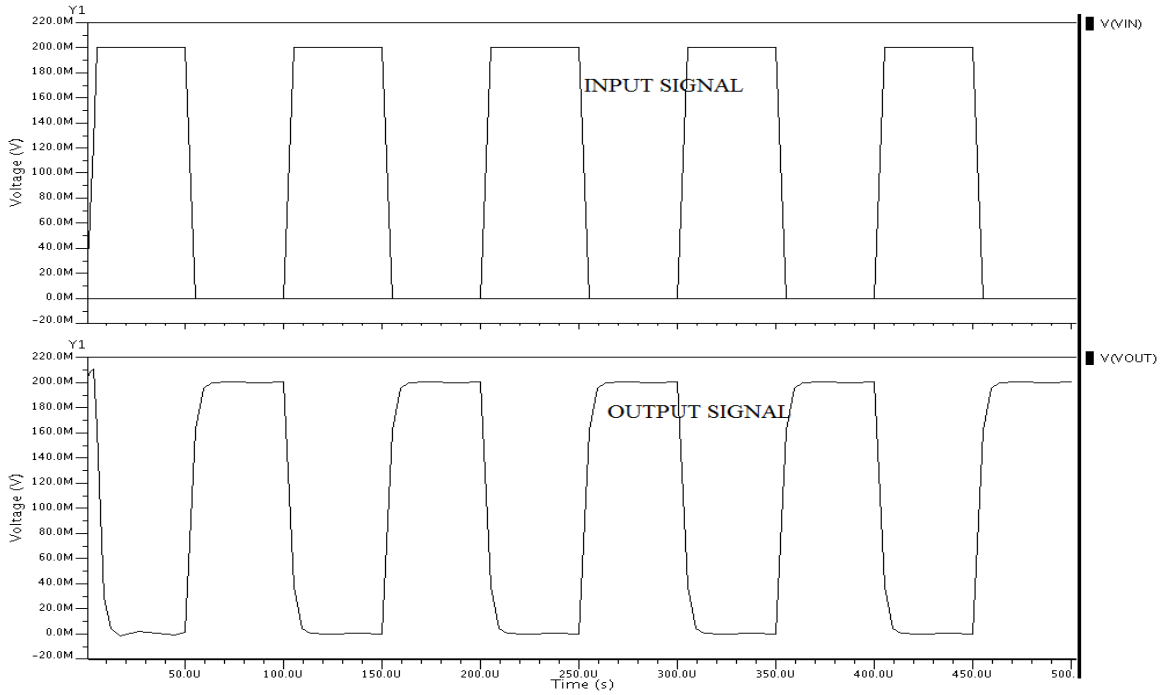

Figure 5.26: Post-Layout Simulation – Transient analysis for CMOS Inverter operating in subthreshold conduction region.

5.3.2 POST - LAYOUT SIMULATION RESULTS FOR TWO-INPUT CMOS NAND GATE

Figure 5.27 and Figure 5.28 show the post-layout results of the transient analysis for a minimum sized Two-Input CMOS NAND Gate.

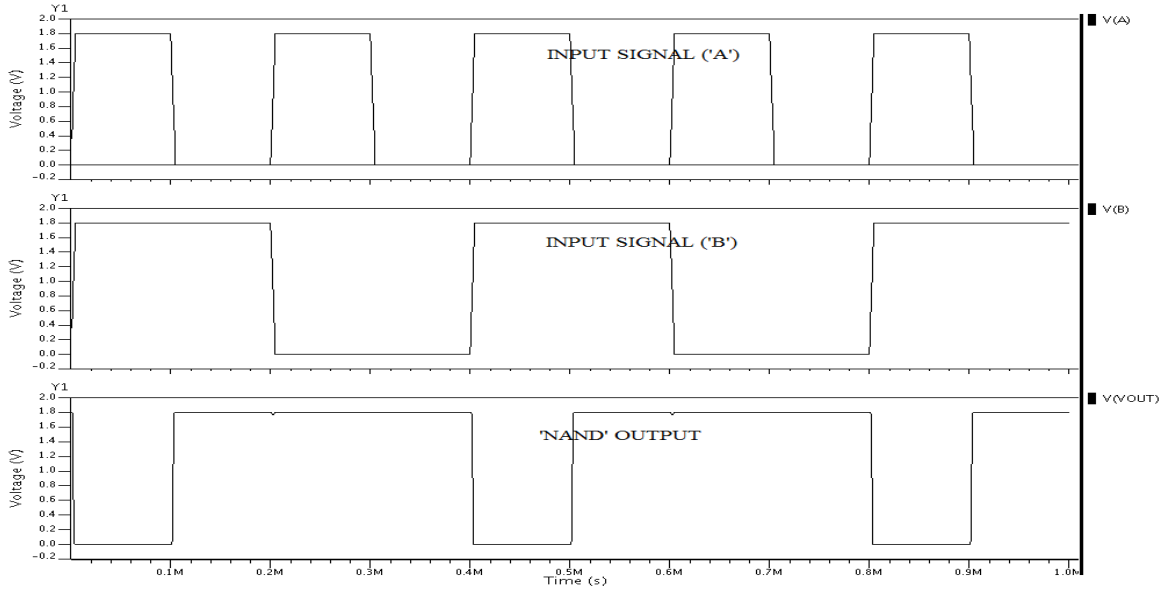

Figure 5.27: Post-Layout Simulation – Transient analysis for Two-Input CMOS NAND Gate operating in superthreshold conduction region.

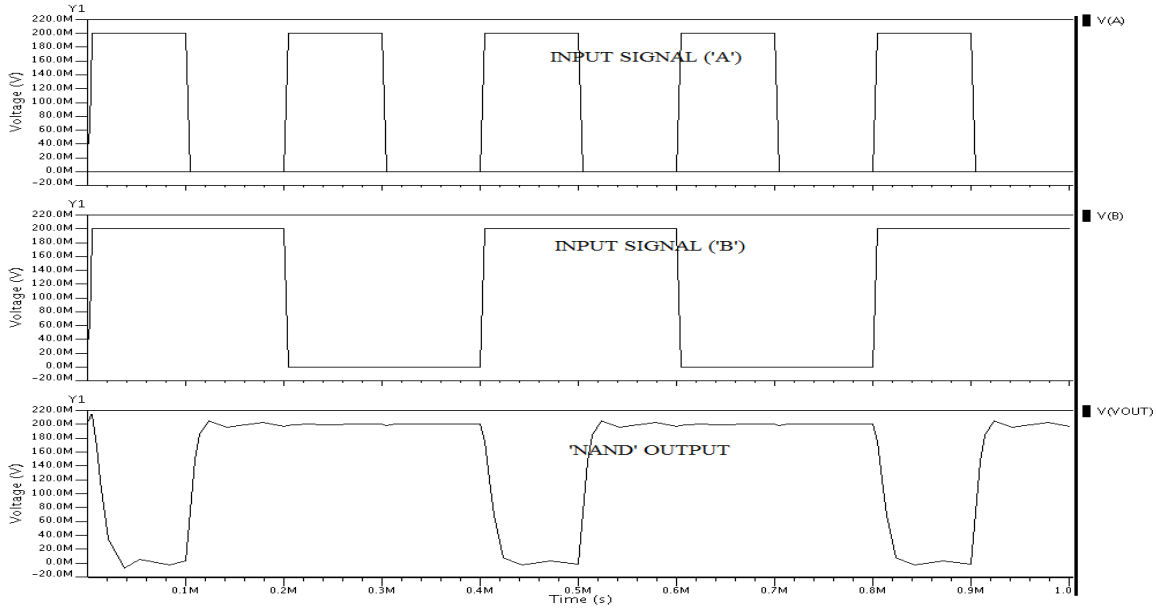

Figure 5.28: Post-Layout Simulation – Transient analysis for Two-Input CMOS NAND Gate operating in subthreshold conduction region.

5.3.3 POST - LAYOUT SIMULATION RESULTS FOR TWO-INPUT CMOS NOR GATE

Figure 5.29 and Figure 5.30 show the post-layout results of the transient analysis for a minimum sized Two-Input CMOS NOR Gate.

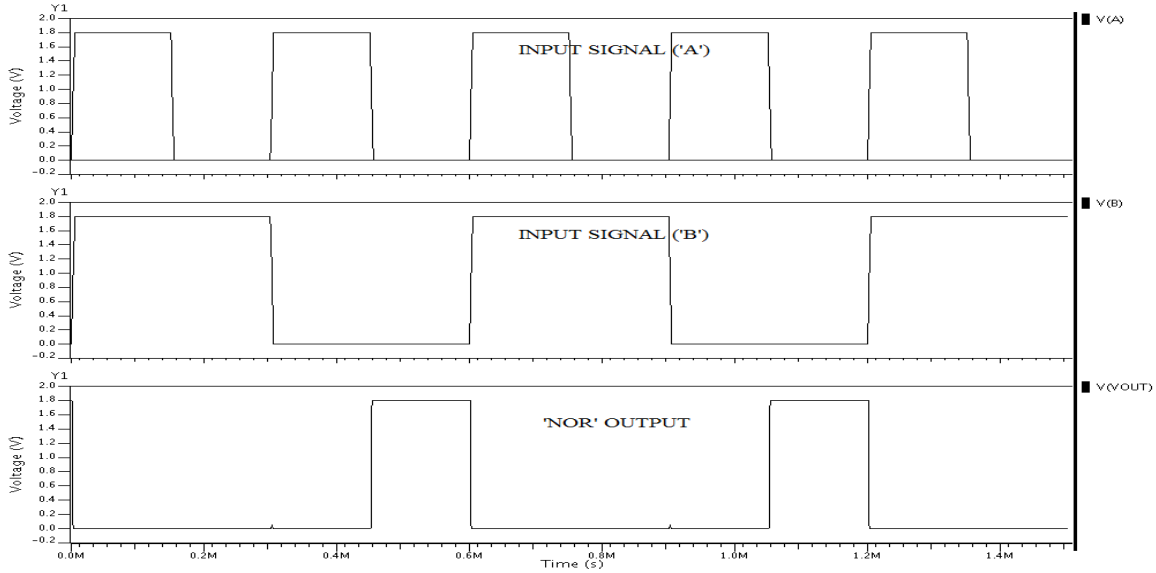

Figure 5.29: Post-Layout Simulation – Transient analysis for Two-Input CMOS NOR Gate operating in superthreshold conduction region.

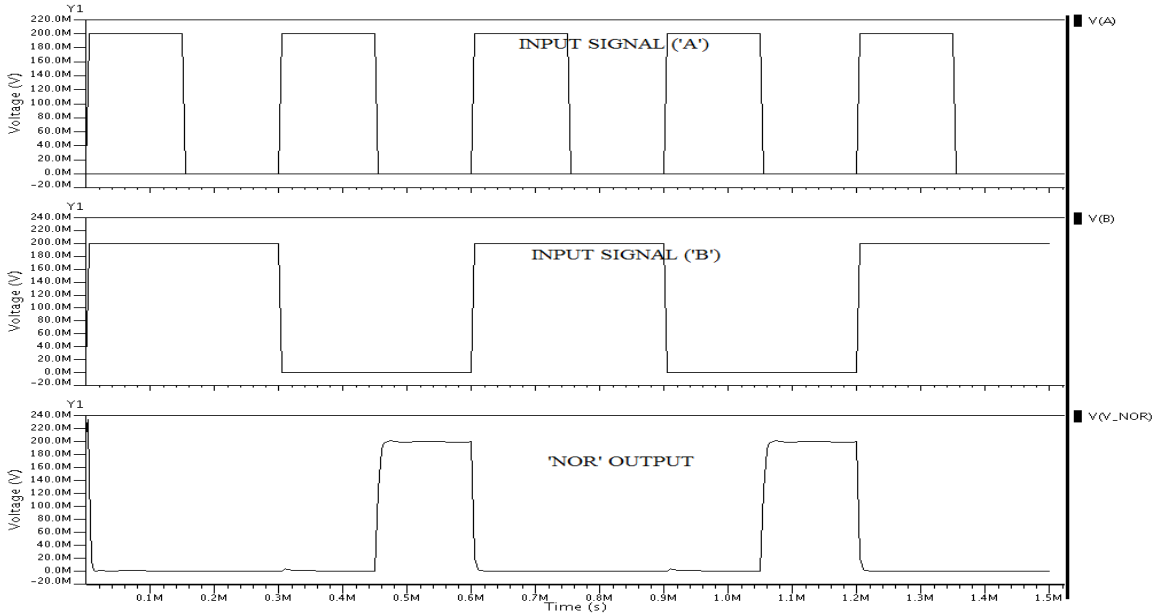

Figure 5.30: Post-Layout Simulation – Transient analysis for Two-Input CMOS NOR Gate operating in subthreshold conduction region.

5.3.4 POST - LAYOUT SIMULATION RESULTS FOR TWO-INPUT CMOS XOR GATE

Figure 5.31 and Figure 5.32 show the post-layout results of the transient analysis for a minimum sized Two-Input CMOS XOR Gate.

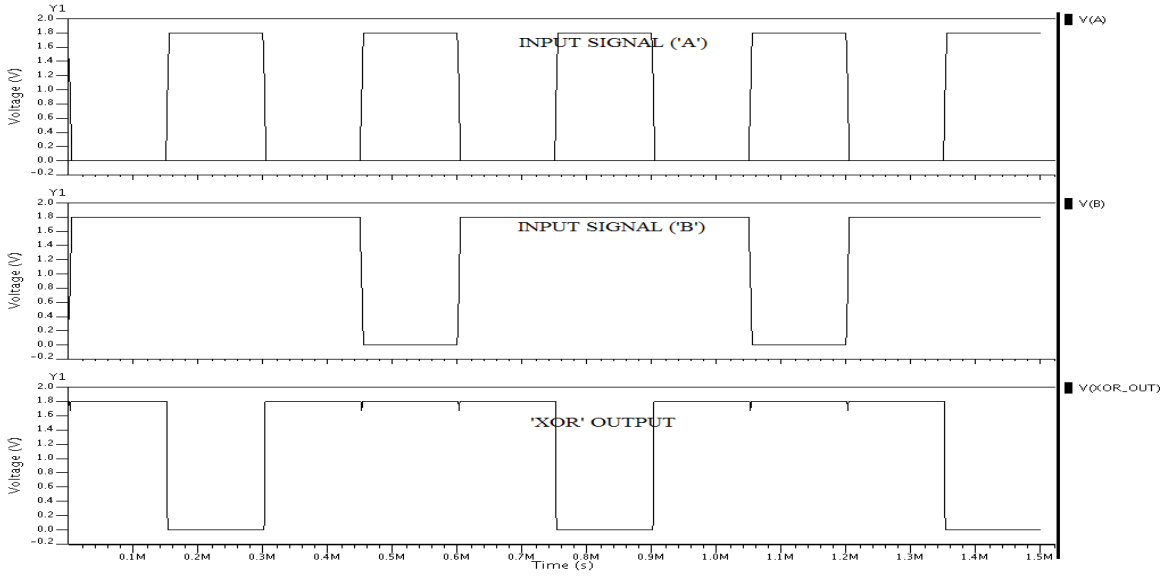

Figure 5.31: Post-Layout Simulation – Transient analysis for Two-Input CMOS XOR Gate operating in superthreshold conduction region.

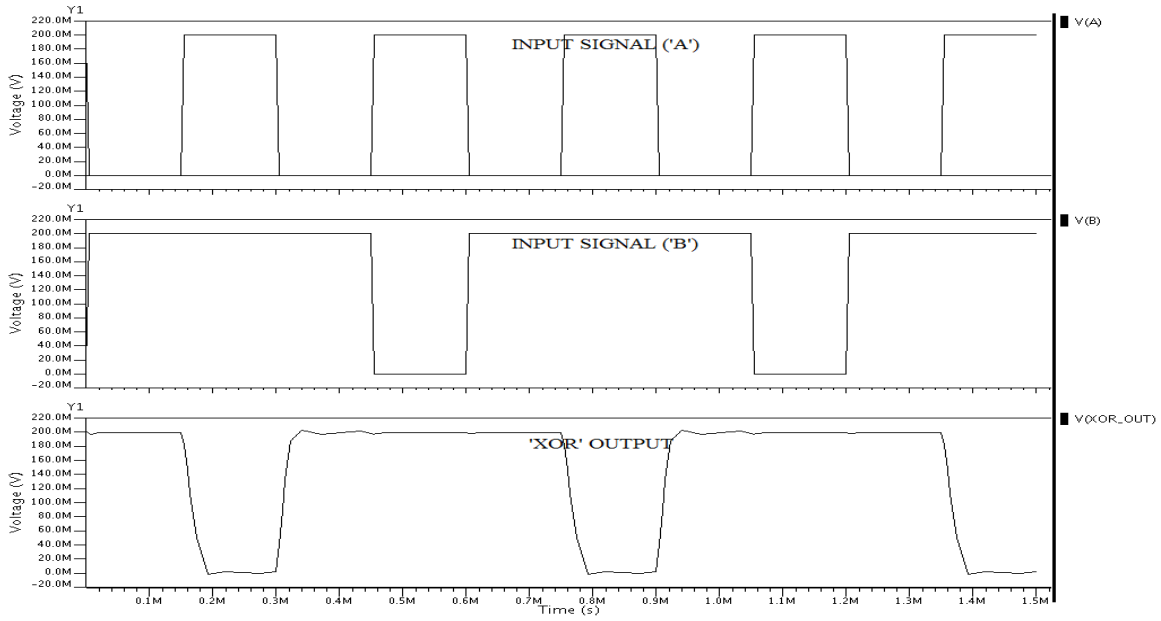

Figure 5.32: Post-Layout Simulation – Transient analysis for Two-Input CMOS XOR Gate operating in subthreshold conduction region.

5.3.5 POST - LAYOUT SIMULATION RESULTS FOR 2-TO-1 CMOS MULTIPLEXER

Figure 5.33 and Figure 5.34 show the post-layout results of the transient analysis for a minimum sized 2-to-1 CMOS Multiplexer.

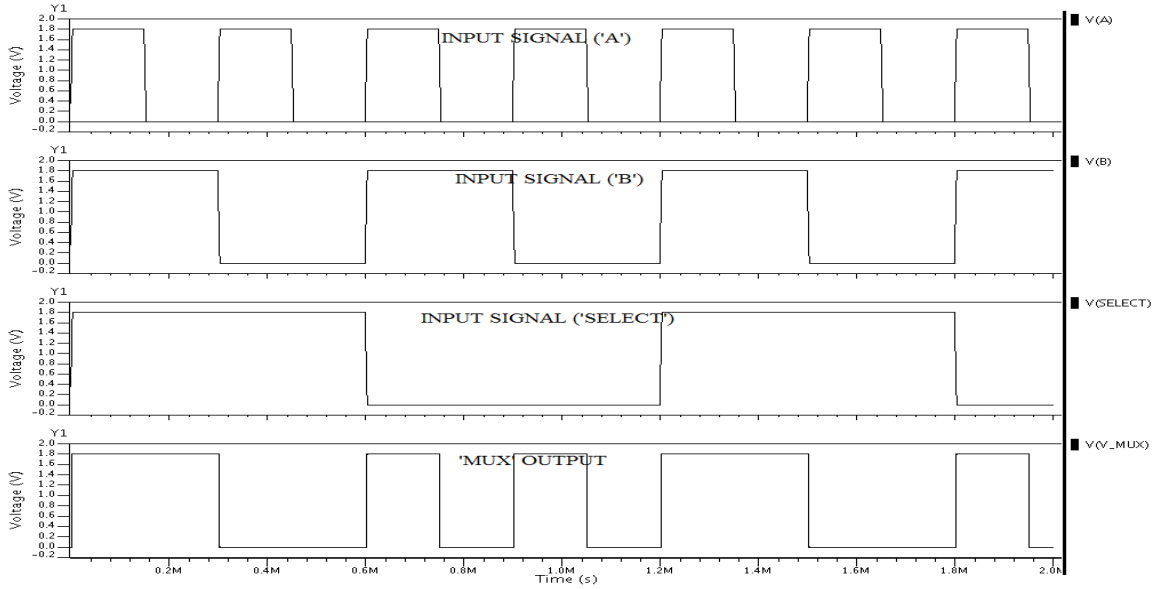

Figure 5.33: Post-Layout Simulation – Transient analysis for Two-to-One CMOS Multiplexer operating in superthreshold conduction region.

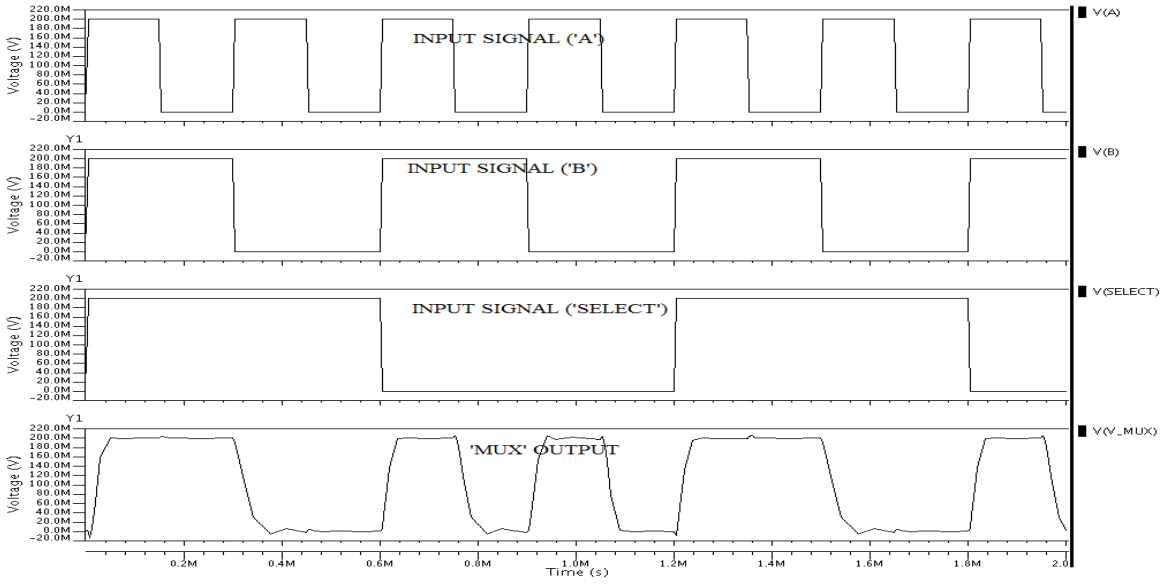

Figure 5.34: Post-Layout Simulation – Transient analysis for Two-to-One CMOS Multiplexer operating in subthreshold conduction region.

5.3.6 POST - LAYOUT SIMULATION RESULTS FOR CMOS HALF ADDER

Figure 5.35 and Figure 5.36 show the post-layout results of the transient analysis for a minimum sized CMOS Half Adder.

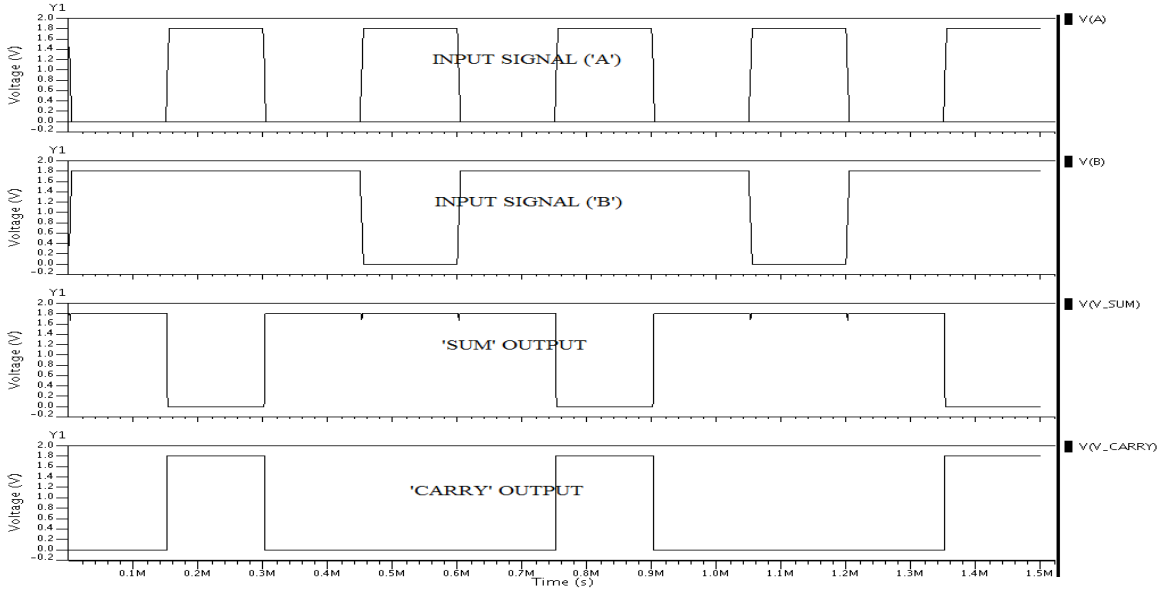

Figure 5.35: Post-Layout Simulation – Transient analysis for CMOS Half Adder operating in superthreshold conduction region.

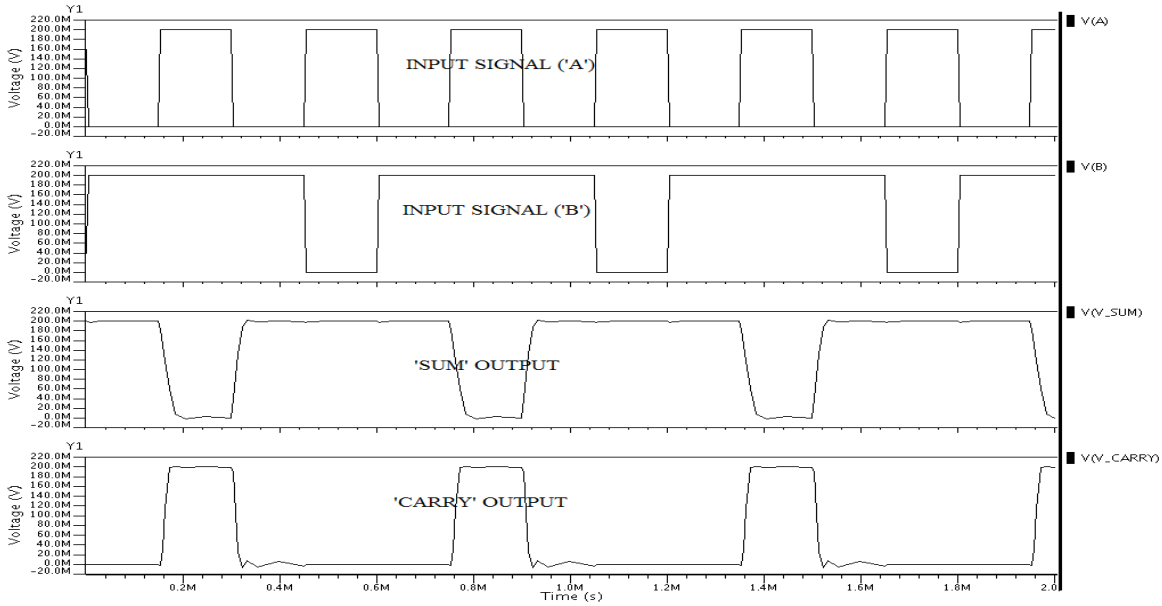

Figure 5.36: Post-Layout Simulation – Transient analysis for CMOS Half Adder operating in subthreshold conduction region.

5.3.7 POST - LAYOUT SIMULATION RESULTS FOR ONE-BIT CMOS FULL ADDER

Figure 5.37 and Figure 5.38 show the post-layout results of the transient analysis for a One-Bit CMOS Full Adder.

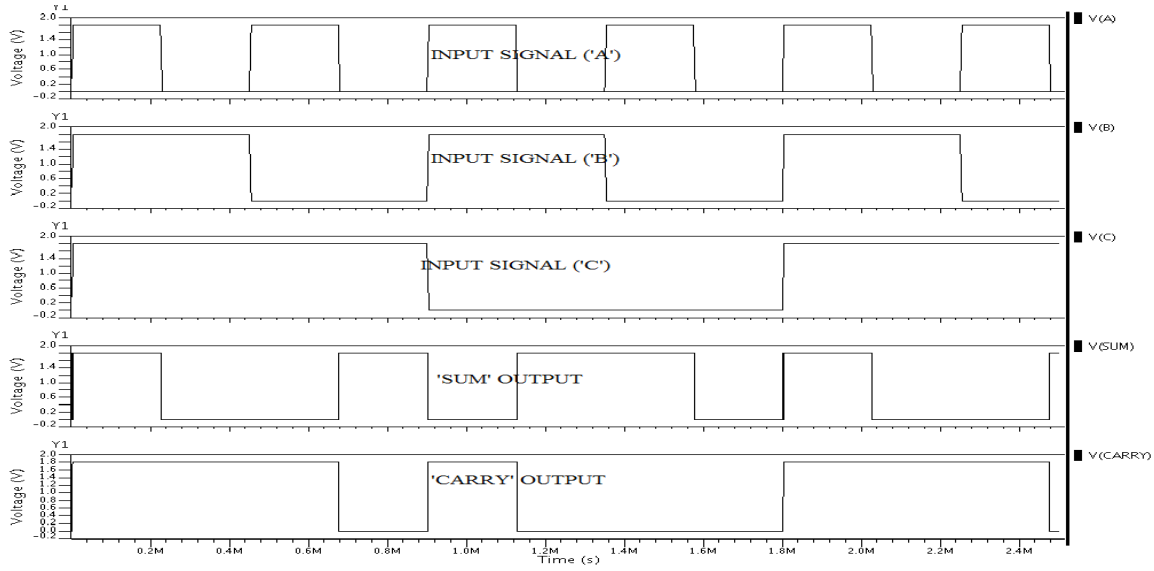

Figure 5.37: Post-Layout Simulation – Transient analysis for One-Bit CMOS Full Adder operating in superthreshold conduction region.

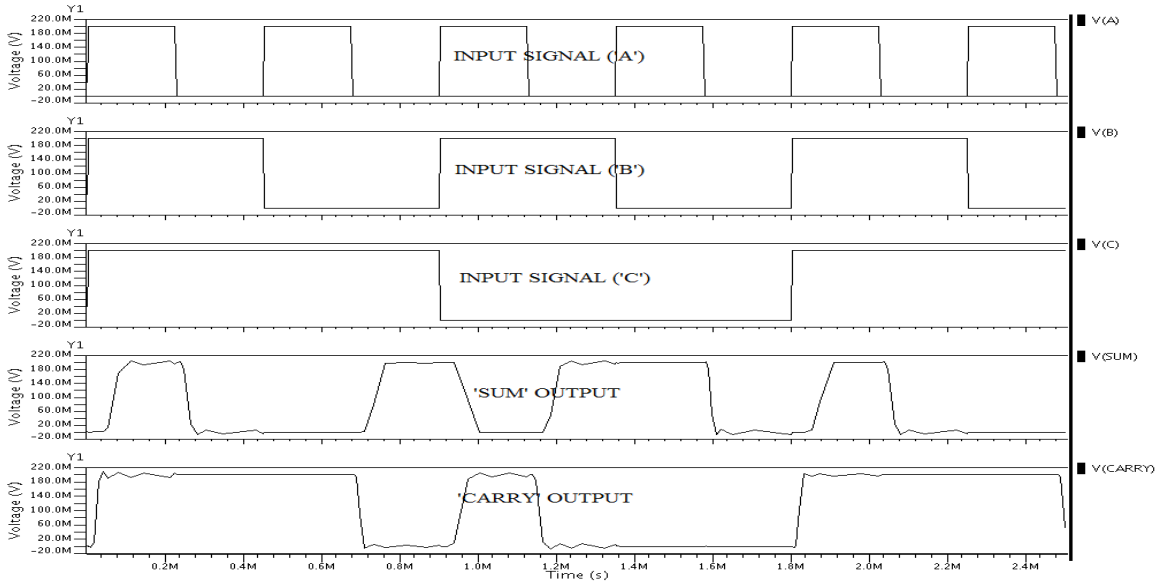

Figure 5.38: Post-Layout Simulation – Transient analysis for One-Bit CMOS Full Adder operating in subthreshold conduction region.

5.3.8 POST - LAYOUT SIMULATION RESULTS FOR TWO-BIT MULTIPLIER

Figure 5.39 and Figure 5.40 show the post-layout results of the transient analysis for a Two-Bit Multiplier.

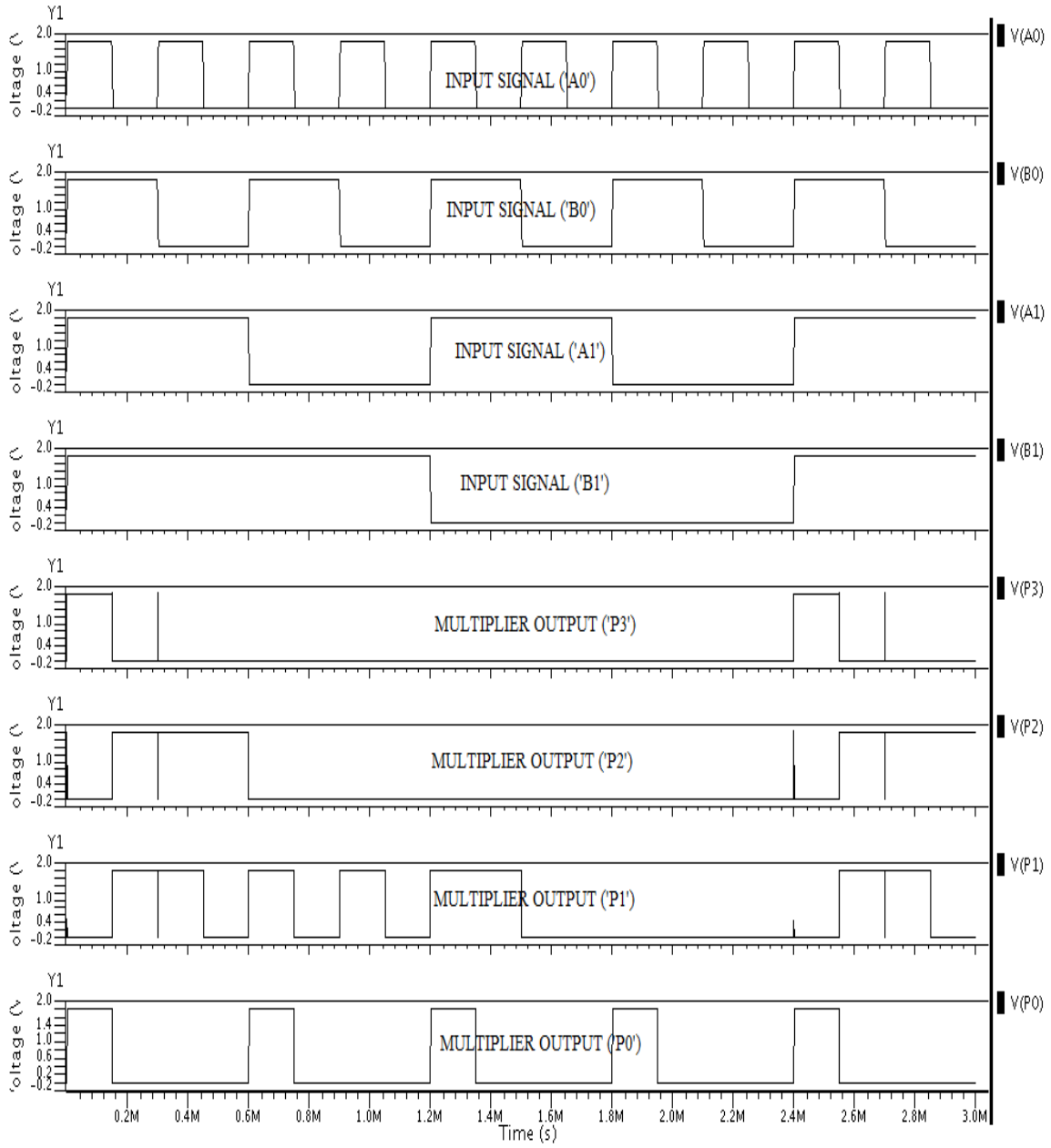

Figure 5.39: Post-Layout Simulation – Transient analysis for Two-Bit Multiplier operating in superthreshold conduction region.

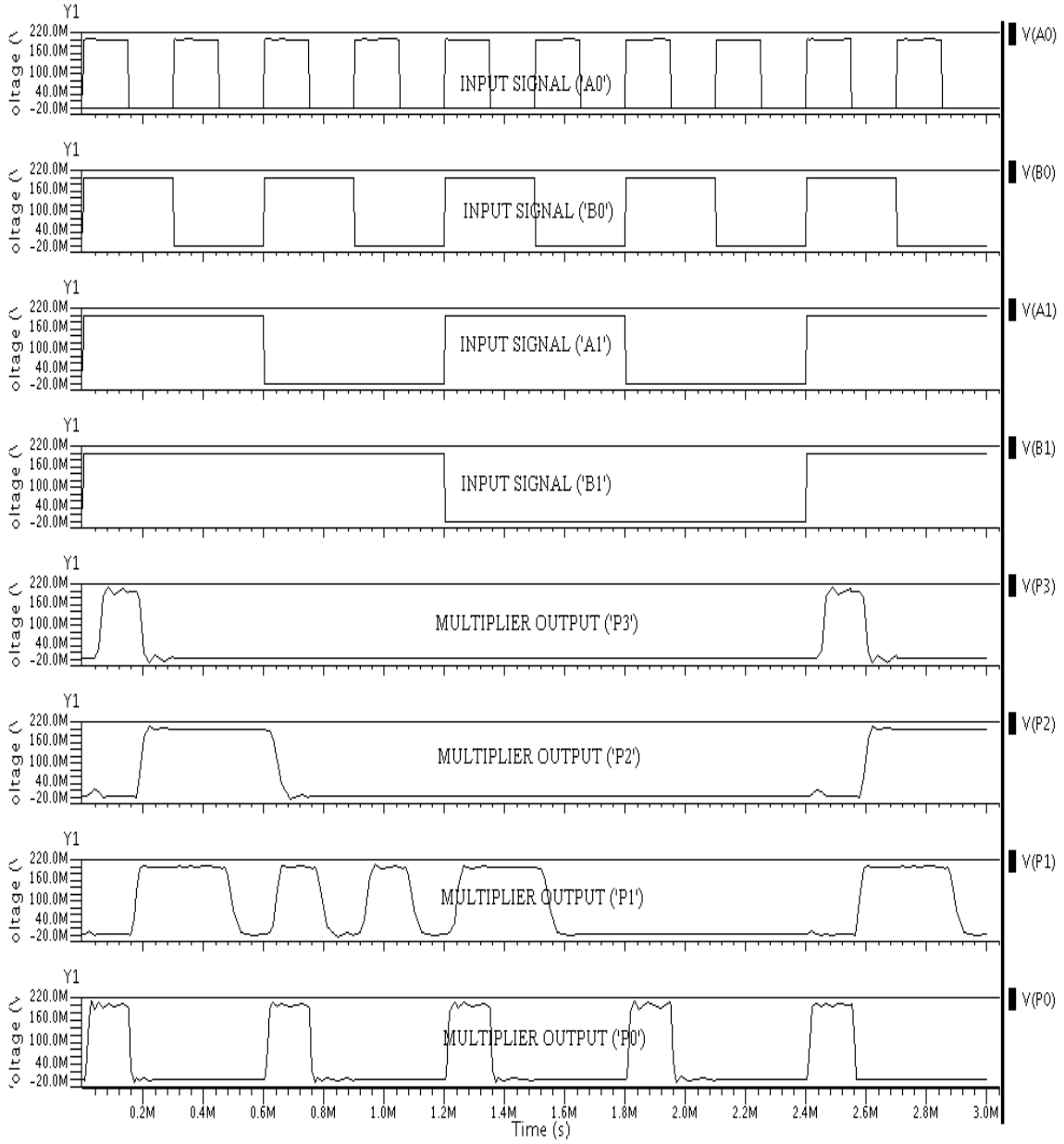

Figure 5.40: Post-Layout Simulation – Transient analysis for Two-Bit Multiplier operating in subthreshold conduction region.

CHAPTER 6 CONCLUSIONS AND FUTURE SCOPE OF WORK

6.1 CONCLUSIONS

The main concern of the work is to design low power VLSI circuits that can play an important role in VLSI domain. So the main concern in the project is to design different basic logic gates at the circuit level. The basic logic gates designed are Inverter, Two-Input NAND Gate, Two-Input NOR Gate, Two-Input AND Gate, Two-Input XOR Gate, Three-Input AND Gate, Three-Input OR Gate, Two-to-One Multiplexer, Half Adder and Full Adder. Also an attempt has been done to design the circuit of Two-Bit Multiplier. The designing of all these circuits were done in fully complementary CMOS logic style. All the circuits were designed operating in subthreshold conduction region and in superthreshold conduction region. Then, the power dissipation analysis has been carried out and it is found that the circuits operating in subthreshold conduction region provide the significant power reduction than the superthreshold conduction region.

The CMOS digital circuits operating in superthreshold conduction region and subthreshold region were designed in Mentor Graphics IC Design Architect using standard TSMC 0.18 μm Technology, layout them in Mentor Graphics IC Station and the analysis of the average dynamic power dissipation with respect to the supply voltage and frequency was done. In superthreshold conduction region, the circuits operate at a supply voltage of 1.8 V and in subthreshold conduction region, the circuits operate at a supply voltage of 0.2 V. It was found that subthreshold conduction region is advantageous in

applications where power is the main concern and the performance can be sacrificed to achieve the low power because the speed of a circuit operating in subthreshold conduction region becomes significantly slow. Hence subthreshold conduction can be used to design low power circuits such as digital wrist watches, radio frequency identification (RFID), sensor nodes, pacemakers and battery operated devices such as, cellular phones etc.

6.2 FUTURE SCOPE OF WORK

The potential for minimizing energy at the cost of speed degradation defines the following set of applications for which subthreshold circuits are well suited.

(a) Energy-constrained applications such as wireless sensor nodes, RFID tags, medical equipments such as hearing aids and pace-maker, wearable computing or implants, personal digital assistants (PDAs), and laptops, which are dominated primarily by the need to minimize energy consumption and increase battery life time, speed is a secondary consideration for this class of applications, so subthreshold circuits offer a good solution.

(b) Many burst mode applications, requiring high performance for very short duration between extended periods of low performance operation, subthreshold circuits can minimize energy for computations executed during the low performance slots. This type of applications appears almost in every design, including the high-performance microprocessors and cell phones.

(c) Non-Performance constrained (NPC) DSP systems have a very tight energy budget and have little to no performance requirements. With NPC systems, often performance can be sacrificed in order to reduce power. So, the subthreshold conduction can be a good solution to reduce the power for such DSP applications.

REFERENCES

[1] *International Technology Roadmap for Semiconductors*, 2001 Edition.

[2] S. Hanson, B. Zhai, K. Bernstein, D. Blaauw, A. Bryant, L. Chang, K. K. Das, W. Haensch, E. J. Nowak and D. Sylvester, "Ultralow-voltage, minimum-energy CMOS," *IBM Journal of Research and Development*, vol. 50, no. 4-5, pp. 469–490, 2006.

[3] J. E. Franca and Y.P. Tsividis, *Design of Analog-Digital VLSI Circuits for telecommunication and Signal Processing*, Prentice-Hall, 1994.

[4] A. P. Chandrakasan, S. Sheng and R. W. Brodersen, "Low Power CMOS Digital Design," *IEEE Journal of Solid-state Circuits*, vol. 27, no. 4, pp. 473-484, April 1999.

[5] K. Ragini and B. K. Madhavi, "Ultra Low Power Digital Logic Circuits in Subthreshold for Biomedical Applications," *Journal of Theoretical and Applied Information Technology,* 2005.

[6] N. Jayakumar, R. Garg, B. Gamache and S. P. Khatri, "A PLA based Asynchronous Micropipelining Approach for Subthreshold Circuit Design," *San Francisco, California, USA,* July 2006.

[7] H. Soeleman, K. Roy and B. C. Paul, "Robust Subthreshold Logic for Ultra Low power operation," in *IEEE transactions On VLSI systems,* vol. 9, no. 1, pp. 90-99, 2001.

[8] H. Soeleman, K. Roy, and B. C. Paul, "Robust ultra low power subthreshold DTMOS logic," in *IEEE International Symposium on low power electronics*, pp. 94- 96, 2000.

[9] K. Roy, S. Mukhopadhyay, and H. Mahmoodi-Meimand, "Leakage current mechanisms and leakage reduction techniques in deep-submicrometer cmos circuits," in *Proceedings of IEEE*, vol. 91, no. 2, pp. 305-327, 2003.

[10] A. Wang, B. H. Calhoun and A. P. Chandrakasan, *Subthreshold Design For Ultra Low-Power Systems,* Springer, USA, 2006.

[11] H. Kanitkar, "Subthreshold circuits: Design, Implementation and Application," *A thesis in Kate Gleason College of Engineering Rochester Institute of Technology Rochester, New York,* February 2009.

[12] N. Jayakumar and S. Khatri, "A variation-tolerant Subthreshold Design Approach," in *Proceedings, Design Automation Conference*, pp. 716-719, June 2005.

[13] A. Wang and A. P. Chandrakasan, "Optimal Supply and Threshold Scaling for Subthreshold CMOS Circuits," in *proceedings of IEEE Computer Society Annual Symposium on VLSI,* 2002.

[14] P. Ko, J. Huang, Z. Liu and C. Hu, "BSIM3 for Analog and Digital Circuit Simulation," in *Proceedings of IEEE Symposium on VLSI Technology CAD,* pp. 400-429, January 1993.

[15] R. Corless, G. Gonnet, D. Hare, D. Jeffrey and D. Knuth, "On the Lambert W function," *Advance in Computational Mathematics,* vol. 5, pp. 329-359, 1996.

[16] R. M. Swanson and J. D. Meindl, "Ion-Implanted Complementary MOS Transistors in Low-Voltage Circuits," *IEEE Journal of Solid-State Circuits,* vol. *7*, no. 2, pp. 146-153, April. 1972.

[17] N. Jayakumar and S. P. Khatri, "Minimum energy near-threshold network of PLA based design," in *Proceedings of IEEE International Conference on Computer Design*.

[18] J. S. Wang, C. N. Kuo, T. H. Yang, "Low Power Fixed Width Array Multipliers," in *Proceedings of IEEE Symposium on Low Power Electronics and Design,* pp. 307–312, August 2004.

[19] M. Ito, D. C. and K. Keutzer, "Low Power Multiplication Algorithm for Switching Activity Reduction through Operand Decomposition," in *Proceedings of the 21st International Conference on Computer Design,* August 2003.

[20] J. M. Rabaey, A. Chandrakasan and B. Nikolic, *Digital Integrated Circuits*, Prentice Hall, 2003.

[21] K. Roy and S. C. Prasad, *Low-Power, CMOS VLSI Circuit Design*, John Wiley & Sons Inc., 2000.

APPENDIX A

MOSIS SPICE LEVEL – 53 MOS MODEL PARAMETERS FOR A STANDARD N-WELL CMOS TECHNOLOGY

This appendix includes the SPICE BSIM3v3 Version 3.1 MOS model parameters for TSMC 0.18 μm CMOS process.

(A) MODEL PARAMETERS FOR N-MOS TRANSISTORS.

+VERSION = 3.1	TNOM = 27	TOX = 4.1E-9
+XJ = 1E-7	NCH = 2.3549E17	VTH0 = 0.3725327
+K1 = 0.5933684	K2 = 2.050755E-3	K3 = 1E-3
+K3B = 4.5116437	W0 = 1E-7	NLX = 1.870758E-7
+DVT0W = 0	DVT1W = 0	DVT2W = 0
+DVT0 = 1.3621338	DVT1 = 0.3845146	DVT2 = 0.0577255
+U0 = 259.5304169	UA = -1.413292E-9	UB = 2.229959E-18
+UC = 4.525942E-11	VSAT = 9.411671E4	A0 = 1.7572867
+AGS = 0.3740333	B0 = -7.087476E-9	B1 = -1E-7
+KETA = -4.331915E-3	A1 = 0	A2 = 1
+RDSW = 111.886044	PRWG = 0.5	PRWB = -0.2
+WR = 1	WINT = 0	LINT = 1.701524E-8
+XL = 0	XW = -1E-8	DWG = -1.365589E-8
+DWB = 1.045599E-8	VOFF = -0.0927546	NFACTOR=2.449429
+CIT = 0	CDSC = 2.4E-4	CDSCD = 0
+CDSCB = 0	ETA0 = 3.175457E-3	ETAB = 3.494694E-5
+DSUB = 0.0175288	PCLM = 0.7273497	PDIBLC1=0.1886574
+PDIBLC2 = 2.617136E-3	PDIBLCB = -0.1	DROUT = 0.7779462

+PSCBE1 = 3.488238E10	PSCBE2 = 6.841553E-10	PVAG = 0.0162206
+DELTA = 0.01	RSH = 6.5	MOBMOD = 1
+PRT = 0	UTE = -1.5	KT1 = -0.11
+KT1L = 0	KT2 = 0.022	UA1 = 4.31E-9
+UB1 = -7.61E-18	UC1 = -5.6E-11	AT = 3.3E4
+WL = 0	WLN = 1	WW = 0
+WWN = 1	WWL = 0	LL = 0
+LLN = 1	LW = 0	LWN = 1
+LWL = 0	CAPMOD = 2	XPART = 0.5
+CGDO = 8.53E-10	CGSO = 8.53E-10	CGBO = 1E-12
+CJ = 9.513993E-4	PB = 0.8	MJ = 0.3773625
+CJSW = 2.600853E-10	PBSW = 0.8157101	MJSW = 0.1004233
+CJSWG = 3.3E-10	PBSWG = 0.8157101	MJSWG = 0.1004233
+CF = 0	PVTH0 = -8.863347E-4	PRDSW = -3.6877287
+PK2 = 3.730349E-4	WKETA = 6.284186E-3	LKETA = -0.0106193
+PU0 = 16.6114107	PUA = 6.572846E-11	PUB = 0
+PVSAT = 1.112243E3	PETA0 = 1.002968E-4	PKETA=-2.90604E-3

(B) MODEL PARAMETERS FOR P-MOS TRANSISTORS.

+VERSION = 3.1	TNOM = 27	TOX = 4.1E-9
+XJ = 1E-7	NCH = 4.1589E17	VTH0 = -0.3948389
+K1 = 0.5763529	K2 = 0.0289236	K3 = 0
+K3B = 13.8420955	W0 = 1E-6	NLX = 1.337719E-7
+DVT0W = 0	DVT1W = 0	DVT2W = 0
+DVT0 = 0.5281977	DVT1 = 0.2185978	DVT2 = 0.1
+U0 = 109.9762536	UA = 1.325075E-9	UB = 1.577494E-21
+UC = -1E-10	VSAT = 1.910164E5	A0 = 1.7233027
+AGS = 0.3631032	B0 = 2.336565E-7	B1 = 5.517259E-7
+KETA = 0.0217218	A1 = 0.3935816	A2 = 0.401311
+RDSW = 252.7123939	PRWG = 0.5	PRWB = 0.0158894
+WR = 1	WINT = 0	LINT = 2.718137E-8
+XL = 0	XW = -1E-8	DWG = -4.363993E-8
+DWB = 8.876273E-10	VOFF = -0.0942201	NFACTOR = 2

+CIT = 0	CDSC = 2.4E-4	CDSCD = 0
+CDSCB = 0	ETA0 = 0.2091053	ETAB = -0.1097233
+DSUB = 1.2513945	PCLM = 2.1999615	PDIBLC1=1.2381E-3
+PDIBLC2 = 0.0402861	PDIBLCB = -1E-3	DROUT = 0
+PSCBE1 = 1.034924E10	PSCBE2 = 2.991339E-9	PVAG = 15
+DELTA = 0.01	RSH = 7.5	MOBMOD = 1
+PRT = 0	UTE = -1.5	KT1 = -0.11
+KT1L = 0	KT2 = 0.022	UA1 = 4.31E-9
+UB1 = -7.61E-18	UC1 = -5.6E-11	AT = 3.3E4
+WL = 0	WLN = 1	WW = 0
+WWN = 1	WWL = 0	LL = 0
+LLN = 1	LW = 0	LWN = 1
+LWL = 0	CAPMOD = 2	XPART = 0.5
+CGDO = 6.28E-10	CGSO = 6.28E-10	CGBO = 1E-12
+CJ = 1.160855E-3	PB = 0.8484374	MJ = 0.4079216
+CJSW = 2.306564E-10	PBSW = 0.842712	MJSW = 0.3673317
+CJSWG = 4.22E-10	PBSWG = 0.842712	MJSWG = 0.3673317
+CF = 0	PVTH0 = 2.619929E-3	PRDSW = 1.0634509
+PK2 = 1.940657E-3	WKETA = 0.0355444	LKETA=-3.03702E-3
+PU0 = -1.0227548	PUA = -4.36707E-11	PUB = 1E-21
+PVSAT = -50	PETA0 = 1E-4	PKETA=-5.16729E-3