Surface Potential Based Drain Current Modeling of Junctionless Double-Gate MOSFET

A Dissertation Submitted in Partial Fulfillment of the Requirement for the Award of the Degree of

MASTER OF TECHNOLOGY

in

VLSI DESIGN

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JULY, 2017

DECLARATION

I, **Abhilash Garg** hereby declare that the work presented in this thesis entitled "**Surface Potential Based Drain Current Modeling of Junctionless Double-Gate MOSFET**" in partial fulfillment of the requirement for the award of degree of Master of Technology submitted at Electronics and Communication Engineering Department, Thapar University, Patiala is an authentic record of work carried out under supervision of **Mr. Arun Kumar Chatterjee** (Assistant Professor, ECED, Thapar University, Patiala). The matter presented in this has not been submitted either in part or full to any other university or institute for the award of any other degree.

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It is certified that the above statement made by the candidate is correct to the best of my knowledge and belief.

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My greatest thanks is to all who wished me success especially my family and friends. Above all I render my gratitude to the Almighty who bestowed ability and strength in me to complete this work.

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ABSTRACT

The Junctionless transistor is a device with uniform doping concentration in the channel and source/drain regions. This change in device structure poses many advantages like simplified fabrication process, nearly ideal subthreshold slope, high on to off current ratio, lower DIBL effect etc. In this dissertation, a surface potential based drain current model has been developed for long channel junctionless double gate MOSFET. The threshold voltage model has also been developed. For each region of operation of the device i.e. depletion, partial depletion and accumulation, a different model has been developed and then merged for the entire range of gate voltage. Effect of various geometrical parameters like channel length, silicon thickness, oxide thickness and doping concentration on surface potential and drain current has been studied. Effect of drain voltage on the threshold voltage has exclusively been studied. Surface potential has been calculated in terms of the Lambert W function for subthreshold region. Surface potential model has been used further to calculate mobile charge density in the channel region and Pao-Sah integral has been used to calculate drain current of the device. Simulation of the device has been performed using Silvaco ATLAS tool. Developed model has been compared with the published and simulation results, and they are in good agreement with each other.

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LIST OF ABBREVIATIONS

IC	Integrated Circuit
MOSFET	Metal-Oxide-Semiconductor Field Effect Transistor
CMOS	Complementary Metal-Oxide-Semiconductor
ITRS	International Technology Roadmap for Semiconductors
SCE	Short Channel Effect
SOI	Silicon-On-Insulator
FET	Field Effect Transistor
BJT	Bipolar Junction Transistor
DIBL	Drain-Induced Barrier Lowering
GIDL	Gate Induced Drain Leakage
SS	Subthreshold Slope
PD-SOI	Partially Depleted SOI
FD-SOI	Fully Depleted SOI
DG JL MOSFET	Double Gate Junctionless MOSFET
DG MOSFET	Double Gate MOSFET

CHAPTER 1
INTRODUCTION

1.1 EVOLUTION HISTORY OF SEMICONDUCTOR DEVICES [1]

Point-Contact Rectifiers

German physicist Ferdinand Braun was the first to study the electrical characteristics of electrolytes and crystals at Wurzburg University in 1874. He found the rectification effect at the interface point between metals and certain crystals. This device found no useful practical application until the invention of radio. Firstly, this device was used as a signal receiver in a crystal radio set in 1901. J. C. Bose then obtained a patent for PbS point-contact rectifiers in 1904. After that many point contact rectifiers were developed using different materials to improve the rectification property. Devices which perform rectification are known as diodes, therefore this device is popularly known as point contact diode.

The p-n Junction

Russel Ohl was trying to fix the problems with the radio detection. He found that the problem with the cat's whisker detector is due to the bad quality of semiconductor. He performed an experiment by melting silicon in quartz tubes and accidentally found the presence of impurities which in turn created the p-n junction.

Bipolar Transistor

Discovery of Bipolar transistors revolutionized the electronics, telecommunication industry completely. Earlier vacuum tubes were the prominent device used in electronic appliances but main disadvantage of a vacuum tube is that those were very bulky. 1st transistor introduced was point contact diode but that was having unstable electrical characteristics. Grown junction transistors were the successor of point contact transistors with improved electrical characteristics. The Main disadvantage of junction transistors was its fabrication complexity due to complicated doping procedure. After that alloyed junction transistors came into existence which provided simpler fabrication and less wastage of silicon material. Base width obtained at that time was 10um which can operate up to few MHz only. This was further improved using the Ge diffused transistors. At the time BJT's were invented, not much of the characteristics of this device were known but later on continuous research has been carried out in this domain.

Integrated Circuit

Integrated circuit was first demonstrated by Jack Kilby in 1958. He fabricated several devices on a single silicon substrate and connected them with the help of wires. Utilization of wires for bonding was a major concern that Kilby proposed because it makes the IC very bulky. Later Kilby proposed the formation of these interconnects using deposition of the aluminium layer on SiO_2. Jack Kilby received the Noble Prize in physics for his discoveries in 2000.

Tunnel Diode

Tunnel diode was first proposed by Leo Esaki. He made the doping in the base junctions very high. He was aware of the fact that at high doping and narrow width tunneling could happen. He proposed the tunnel diodes with both silicon and germanium material. The Main advantage of tunnel diode was its high switching speed. He was awarded the Noble Prize in physics in 1973 for his contribution in tunneling.

Metal Oxide Semiconductor Field Effect Transistor (MOSFET)

MOSFET was actually invented before BJT, but inventors were not able to justify its conduction mechanism at that time therefore it got no response from the reviewers. But later it became a popular device. It consists of a SiO_2 layer at the top, which in turn produces fields down the bulk. MOSFET is basically a four terminal device i.e. gate, source, drain, bulk. Early MOSFETs were having the aluminium gate but later poly-Si gate came into existence which in turn provides better fabrication stability and lesser gate overlap parasitic capacitance. Poly-Si were having very high resistance therefore later they were replaced by silicide of some refractory metal. Further with the reduction in device dimensions many complexities came into picture which revolutionized the research in Semiconductor devices field. The Main disadvantage of device scaling was the emergence of short channel effects (SCE's). SCE's can be reduced considerably by reducing the gate oxide thickness. But reduced gate oxide thickness results in increased gate leakage currents, which in turn increases power consumption in the chip which is completely undesirable. Therefore various other fabrication techniques are employed to overcome these SCEs which includes SOI, FDSOI, and FD UTB SOI fabrication techniques.

The Invention of a transistor is the biggest revolution of the present century. One can't suppose present day life without computers, mobiles, the internet etc. The Backbone of all these technologies is transistors. A continuous research had been carried out in the field of semiconductor devices since the evolution of semiconductor industry to optimize the

performance and obtain required performance results. This research is still in progress in the present time.

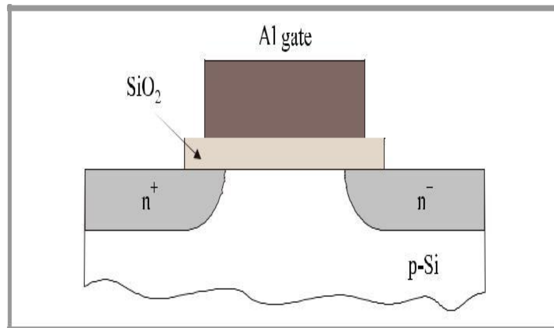

Figure 1.1: A cross-section of a MOSFET [1]

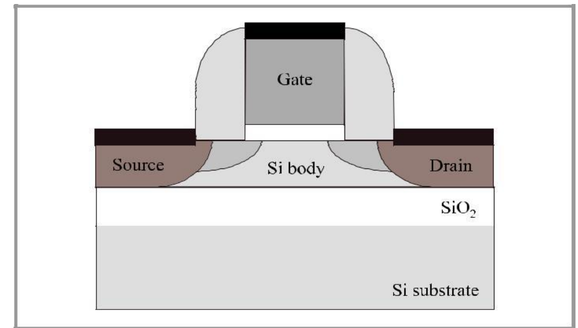

Figure 1.2: SOI MOSFET [1]

Number of transistors in an IC are increasing exponentially since the very beginning of silicon microelectronics. This trend was first predicted by Gordon Moore and hence named as Moore's law. This trend keeps on continuing until the starting of this decade but fails disasterably after that.

1.2 THE SCALING OF MOSFET [2]

The microelectronics industry had gained a lot since last three decades due to the miniaturization of the MOSFET dimensions. Main advantages of transistor scaling are the low cost of manufacturing, the increased speed of data transfer, the increased ability to perform multiple tasks simultaneously.

1.2.1 Moore's law

Gordon Moore in 1965 predicted the number of transistors that can be placed on a single chip for the next ten years only, but his prediction keeps on following until the coming three decades. Moore's law is basically an empirical formula which observes the rate of growth of semiconductor technology. In 1965 when G. Moore made his statement then a number of transistors on a microprocessor was approximately 32 and now they have reached up to half a billion [2]. The Most accepted statement about Moore's law is that number of transistor on a chip doubles every 18 months.

This scaling of device dimensions ultimately led to various short channel effects within the device. These SCEs are discussed in detail in the following section. Other than these short channel effects, quantum effects are also present in the devices which also affect device behavior.

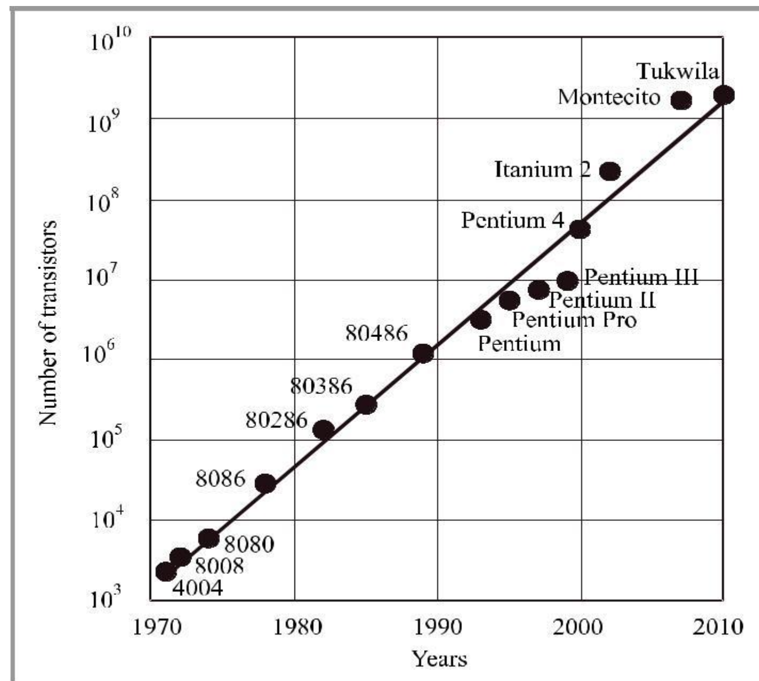

Figure 1.3: Increased Transistor count with time.

1.2.2 Implications of Moore's law [4] [5]

Moore's law had widely affected the microelectronics manufacturing industry since last three decades. With every new generation of integrated circuit, increased performance, reduced cost, improved functionality has been achieved. Various implications are

1. ITRS defines functionality as the no. of logic transistors on the given chip. Improved functionality results in minimized delay of operation due to the isolation of different functions on separate ICs. Enhanced functionality also results in improved packaging density of integrated circuits [4].
2. 2nd important factor associated with Moore's law is chip cost. With the increased transistor count on a chip and reduced area per transistor, cost per function also reduced. ITRS [3] had observed that cost per function reduces by 50% in almost every two years.
3. The Third implication is performance. Performance generally associated with the speed of operation of typical microprocessors. In general, the frequency of operation measures the speed of chip. Frequency is inversely proportional to the delay time of the inverter [6].

$$\tau_{inv} = R_{sw}(C_{in} + C_{out})$$

Where τ_{inv} is the delay of the inverter, R_{sw} is the switching resistance, C_{in} is the input capacitance of inverter and C_{out} is the output capacitance of inverter. This delay time is inversely proportional to the scaling factor (k).

1.2.3 Types of scaling

Scaling may be classified into following categories

1. Constant field scaling.
2. Generalized scaling.

Constant field scaling

Dennard et al proposed the concept of scaling where there is a linear reduction in length and supply voltage of the transistor and increase in doping concentration in order to enhance the performance and functionality of the device such that electric field within the device remains constant [7][8]. Therefore it is known as constant field scaling. All the design parameters are changed by a factor called scaling factor.

Generalized scaling

At Submicrometer regimes sometimes electric field doesn't remain constant due to dominance of short channel effects. Electric Field keeps on changing significantly as the device dimensions keep on reducing therefore gradual field approximation fails. This challenge to above scaling technique was addressed by Brews et al. [9].They proposed a minimum channel length which can be maintained after scaling to maintain the same subthreshold characteristics.

$$L_{min} = A\left[x_j t_{ox}(W_s + W_d)^2\right]^{1/3}$$

Where L_{min} denotes the minimum channel length, W_s and W_d is the depletion widths of source and drain regions, x_j is the junction depth, t_{ox} is oxide thickness, A is proportionality constant.

This scaling approach has many advantages over the constant field scaling [10]. The Major advantage is that all the parameters need not be scaled down by the same factor. Brews only suggested three parameter dependence of scaling but later it is found that MOSFET scaling includes five parameters i.e. $L_g, t_{ox,} V_{dd}, N_a, x_j$. Device behavior under short channel effects (SCE) and DIBL depends on all these five device parameters.

Here L_g is the channel length of the device, $t_{ox,}$ represents oxide thickness, V_{dd} represents voltage applied to the drain terminal of the device, N_a is the doping concentration of the bulk in the device and x_j is the junction depth of the device.

Table 1: Technology Scaling Rules.

Physical Parameter	Constant Electric Field Scaling Factor	Generalized Scaling Factor	Generalized Selective Scaling Factor
Channel Length, Insulator Thickness	1/β	1/β	$1/\alpha_d$
Channel Width, Wiring Width	1/β	1/β	$1/\alpha_w$
Electric Field	1	Ε	ε
Voltage	1/β	ε/β	ε/α_d
ON Current per Device	1/β	ε/β	ε/α_w
Doping	Β	Εβ	$\varepsilon\alpha_d$
Area	$1/\beta^2$	$1/\beta^2$	$1/\alpha_w^2$
Capacitance	1/β	1/β	$1/\alpha_w$
Gate Delay	1/β	1/β	$1/\alpha_d$
Power Dissipation	$1/\beta^2$	ε^2/β^2	$\varepsilon^2/\alpha_w\alpha_d$
Power Density	1	ε^2	$\varepsilon^2/\alpha_w\alpha_d$

1.2.4 Challenges imposed to Scaling

With the advancements in the scaling of devices in microelectronics industry, many technological challenges had been imposed. As ITRS 2015 has announced latest technological nodes between 10-20 nm, scaling becomes really crucial in that scenario. Major effects which prohibits the scaling in conventional MOSFET are discussed below [11].

High Electric field

Due to the reduction in channel length, width, oxide thickness and comparatively larger biasing voltage applied, the electric field becomes large which in turn gives rise to a surge in electrical currents ultimately causing breakdown of device. This effect is more prominent in the case of devices made with bulk silicon.

Heat dissipation

With the scaling of device dimensions at nanoscale, leakage currents within the device increases which gives rise to increased heat dissipation. Due to Larger chip density, this increase in heat dissipation becomes more severe and can result in heat up of devices and degraded performance.

Power Supply and Threshold voltage

During scaling supply voltage also needs to be scaled down in order to maintain a constant electric field in the device. Threshold voltage can’t be scaled down much due

to the involvement of leakage components of current. If we try to do so, leakages within the device increases and results in enhanced active power consumption.

Parasitic resistances and capacitances

Scaling introduces more parasitic components (resistances and capacitances) in the device which greatly effects on-current characteristics of the device.

PN junction leakage currents

Generally, source and drain to well junctions are reverse biased. Due to its reverse biasing there is always a reverse bias current which comprises of two components: one is minority carrier current due to drift/diffusion and other is current due to recombination of charges in depletion region in pn junction. pn junction leakage current depends mainly on junction area and doping in that region. If doping concentration of pn junction is made to be very high (halo doping implant) then band to band tunneling current dominates over reverse bias current.

There are other short channel effects which arise due to the scaling of device dimensions, and are discussed below.

Drain Induced Barrier Lowering and punch through

As the drain voltage applied to the MOSFET increases, drain and bulk regions forming PN junction got more and more reverse biased. Ultimately causing overlapping of two depletion regions formed due to reverse biasing of junctions. This overlapping results in punch through of channel. Punch through can be avoided using high doping within the channel, using thinner oxides and shallower junctions.

Current flows in the conventional MOSFET through an inversion layer which is formed by applying a gate voltage (V_{gs}) greater than the threshold voltage. If the gate voltage is lesser than the threshold voltage it will provide a potential barrier to the flow of charge carriers and hence device will be said to operate in the subthreshold region. In small geometry MOSFETs, this flow of charges in inversion layer is controlled by both gate and drain voltage. At higher drain voltages this barrier height got reduced and carriers can move from source to drain even at the low gate voltage (less than the threshold voltage) thus maintaining a flow of current which is known as subthreshold current. This phenomenon of reduction in barrier height due to increase in drain voltage is referred to as drain induced barrier lowering (DIBL).

Hot electrons

Hot electrons are caused by the high electric field in the device. Electrons from the substrate sometimes gain sufficiently high kinetic energy to overcome the potential barrier and enters into the oxide region. They start accumulating there resulting in the rise of the threshold voltage. It greatly affects the reliability of the solid state devices. This effect is more prominent in the case of n channel devices than that of p channel because electrons are having more mobility than that of holes. Hot electrons cause leakage currents within the device and hence resulting in larger power dissipation.

Impact Ionization

This effect is also caused by sub micro meter gate lengths due to high longitudinal electric field. High electric field results in scattering of carriers in the valence band which in turn transfers energy to the valence electrons and giving rise to electron-hole pair. This carrier pair generation gives rise to the extra peak of currents.

Velocity Saturation

The Velocity of charge carriers in the device is directly proportional to the electric field applied.

$$V_d = \mu E \qquad \text{Eq. (1.1)}$$

Where V_d represents drift velocity of carriers, μ is the mobility and E is the electric field applied.

As the electric field is increased by increasing the applied gate voltage, drift velocity also increases [12]. But after a certain value of electric field (nearly 104 V/cm) velocity starts saturating. This effect is more pronounced at small dimensions.

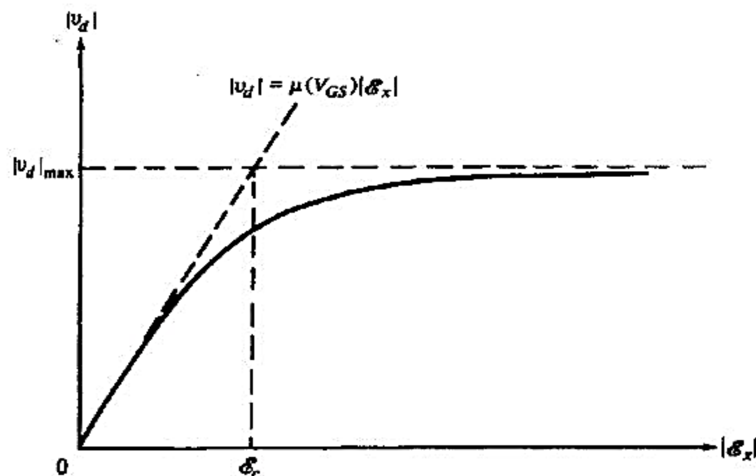

Figure 1.4: Carrier Velocity saturation with increasing electric field [12]

Surface Scattering

As the device dimensions reduces, longitudinal electric field increases within the device. Due to this carrier mobility becomes field dependent. Carrier transport within the device is fully confined within the inversion layer. Increased electric field causes more no. of charge carriers to accumulate near the surface (interface between channel and oxide) resulting in scattering of charges and ultimately causing reduction of mobility and current.

Oxide Leakages

These are caused by the device through the gate to the substrate due to reduced gate oxide thickness. If oxide thickness is reduced upto 2nm then this effect is more prominent. Electrons start tunneling through the gate to the substrate. Oxide leakages result in higher power dissipation in the device. These leakages can be reduced by using high k dielectric material for gate terminal.

Gate Induced Drain Leakage (GIDL)

With the scaling and increased voltages, the electric field at the gate-drain overlap becomes extremely high [13]. This increased electric field results in depletion of carriers into drain overlap region as shown below in the figure 1.5. From the figure it is clear that valence band of gate and conduction band of drain region overlaps. This overlapping results in band to band tunneling of electrons from gate to drain.

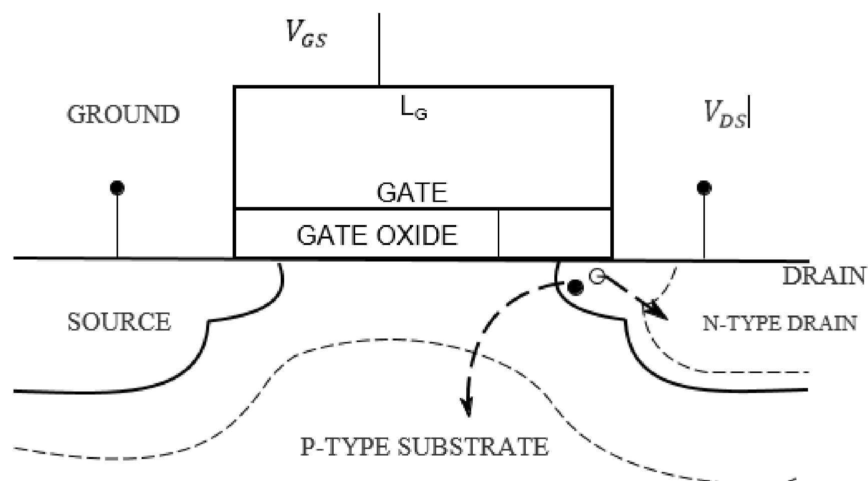

Figure 1.5: GIDL Illustration using schematic view [13].

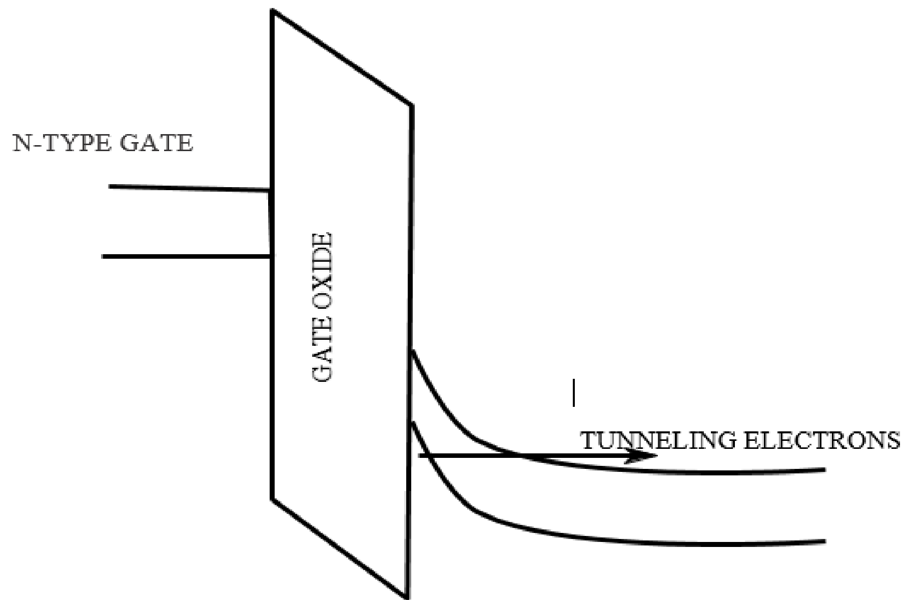

Figure 1.6: Band to Band Tunneling due to GIDL [13].

1.3 TECHNOLOGIES TO OVERCOME CHALLENGES IMPOSED DUE TO SCALING

We can overcome above challenges by two ways. Either we can change the material used within the device or we can make some technological advancements used to fabricate the device. All the possible methods are discussed below.

1.3.1 SOI Technology [14]

SOI (Silicon on Insulator) is a technology which uses layered silicon-insulator-silicon substrate rather than using single silicon substrate. The main motto behind using this technique is to reduce parasitic capacitances within the device. Insulator material used is either silicon dioxide or sapphire. If using sapphire as an insulator then this technology is known as SOS (Silicon on Sapphire). This reduction in junction capacitances reduces power consumption within the device.

In the conventional CMOS technology, a p-type body of NMOS transistor is grounded and while N-type substrate of the transistor is held at supply voltage by means of interconnection. On the other hand in case of SOI technology source, drain, body regions are insulated from the substrate. In SOI technology body of the device remains unconnected and hence cause charging and discharging due to external disturbances and switching. This floating node causes many problems with the device stability. Area consumed in the fabrication of MOSFET's using SOI

Technology is lesser than in the case of conventional bulk technology due to the no need of metal contacts with the well.

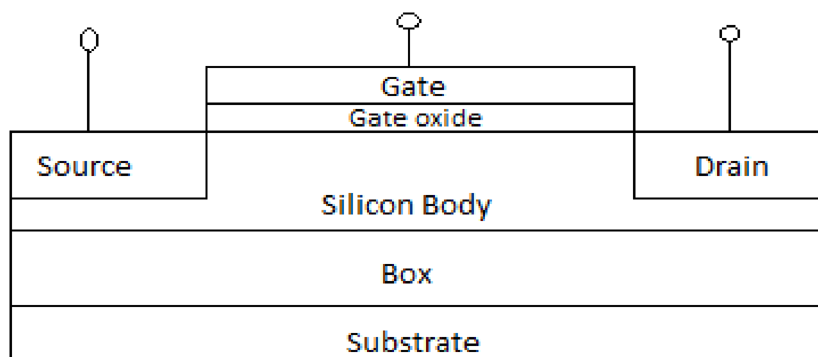

Figure 1.7: SOI MOSFET structure.

1.3.1.1 Types of SOI

Type of SOI depends on the thickness of the insulating layer used. Depending on that thickness there are 2 types of operation of SOI MOSFET's [15].

1. Fully Depleted.
2. Partially Depleted.

Fully Depleted SOI (FDSOI) [15]

Considering the case of NMOS transistor, by applying a positive voltage to the gate terminal produces an inversion layer below the gate by depleting the P-type substrate. In FDSOI MOSFET, the Insulating layer is very thin and hence by applying sufficient gate voltage this layer gets fully depleted easily and extends upto the body. This technology enables the low power devices when a body is lightly doped.

Partially Depleted SOI [15]

SOI MOSFET operates in the partially depleted mode when the insulating layer thickness made to be thicker. Even after applying the sufficient gate voltage inversion layer formed couldn't extend itself to the body of the device and hence substrate remains partially depleted therefore it is known to be a partially depleted mode of operation of SOI MOSFET. Here body voltage does affect the conduction in the channel. At smaller applied voltages, inversion layer formed is thinner and hence results in lower conductivity and slower switching. Whereas at higher voltages, inversion layer

formed is thick enough to provide high conductivity and faster switching. PDSOI MOSFET is formed when silicon width is at least twice as that of maximum depletion width xdmax.

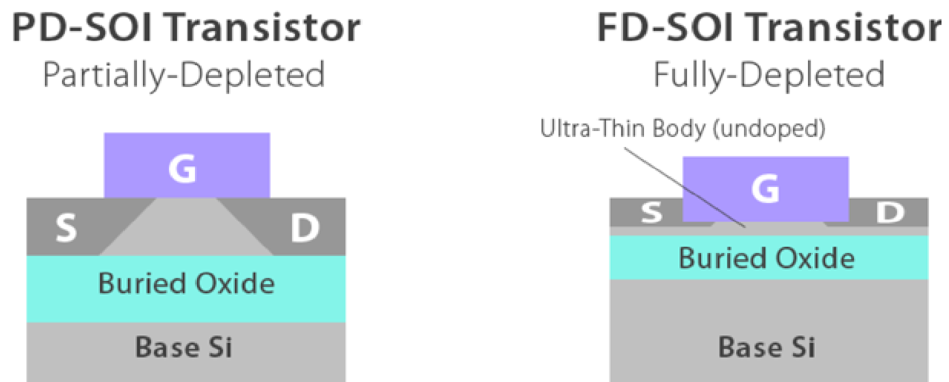

Figure 1.8: Types of SOI MOSFETs.

Another method to overcome short channel effects within the device is to make changes in the device materials. P-type polysilicon and N-type polysilicon as a gate material can be exchanged with the silicide of some metal to provide low series resistance of the gate.

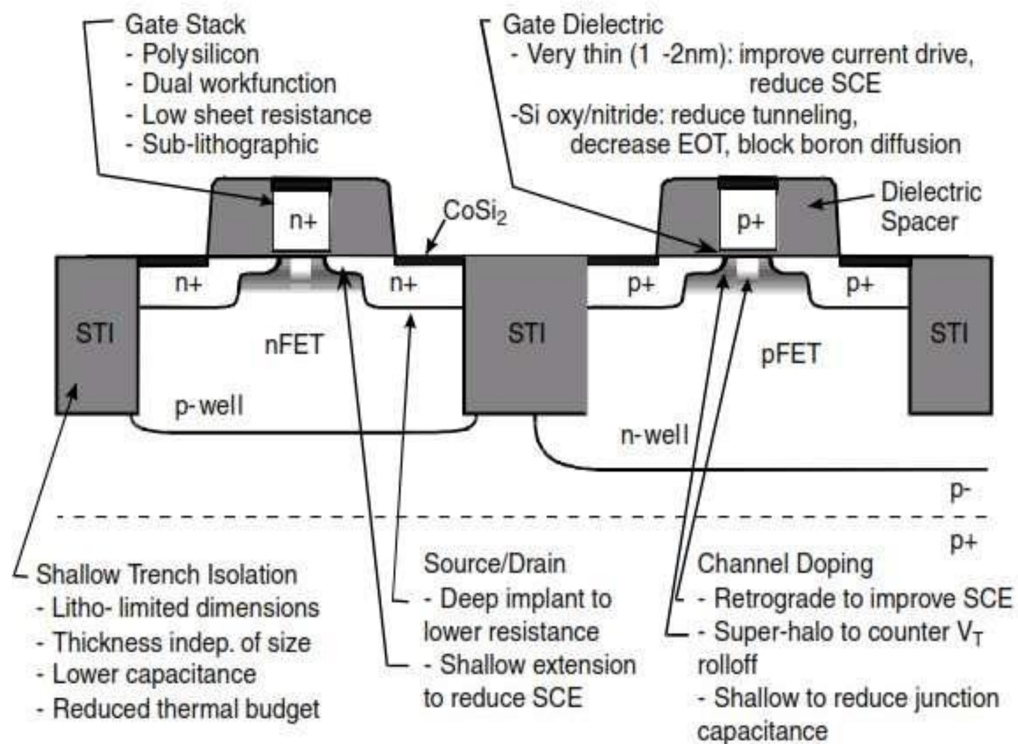

Figure 1.9: Conventional CMOS technology cross section [14].

To improve the performance of the device, thickness of insulating layer need to be reduced but this gives rise to another drawback of tunneling which in turn increases leakages and hence power consumption of the device.

Shallow trench isolation technique is used to separate two FET's such that parasitic can be minimized, but this usually resulted in higher circuit density. To make further improvements in the short channel characteristics of the device a combination of shallow and deep implants are perfectly matched together.

Another aspect to improve the performance of the device is by using double gate FET structure. The extra gate used is to improve the field of the drain and body. 2nd gate makes the drain current double. Double gate MOSFET provides better flexibility towards scaling of channel length than that of conventional bulk MOSFET because later can't be made with thinner oxide layers but earlier can be.

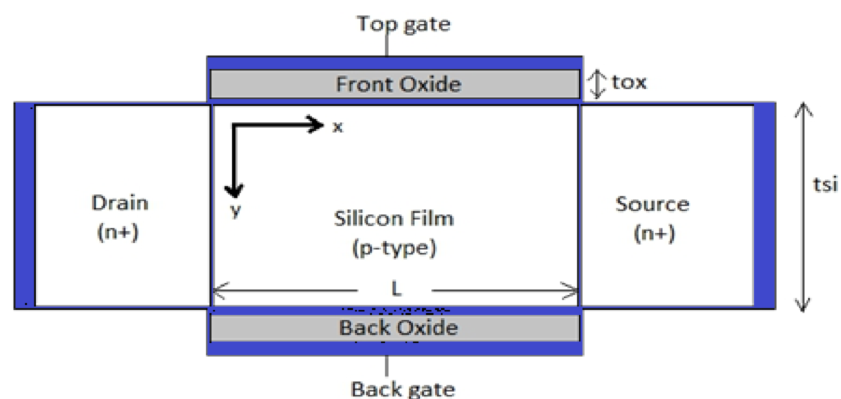

Figure 1.10: Double Gate MOSFET structure [14].

1.4 BASIC INTRODUCTION TO DEVICE MODELING

Last two decades has led to the rapid development of semiconductor industry, especially in the field of device modeling. Always there is a need to understand the operation and optimization of semiconductor integrated circuits for better performance. Device modeling provides a better understanding about the behavior of semiconductor devices and how that can be utilized further to improve the system performance on the larger scale. As the consequences of scaling are increasing, device behavior starts departing from the actual one. Therefore modeling plays a crucial role in that case to better understand and formulate that changed behavior of the device. Modeling also helps in predicting the characteristics of any new device prior to its fabrication such that involved cost of research can be reduced.

Device models basically have been characterized into two types, one is a physical model and other is equivalent circuit model. Device model incorporate the physics of operation of the device whereas circuit model is based on the electrical characteristics of the device.

Physical models include numerical techniques which are generally implemented on computers using specific algorithms. Physical models are solved using either bulk carrier transport equations or Boltzmann transport equations. Most popular among these two in classical physics is bulk transport equation. Later semi-classical and quantum models are also incorporated. Table 1.2 illustrates the various advantages and disadvantages of various semi-classical and quantum transport device models.

Table 1.2: Illustration of Various modeling techniques.

Approach (Approximate → Exact)	**Model**	**Improvements** (Easy → Difficult)
Semi Classical Approach	Compact models	Appropriate for circuit design
	Drift-Diffusion Equation	Good for devices down to 0.5μm, includes μ(E)
	Hydrodynamic Equations	Velocity overshot effect can be Treated properly
	Boltzmann Transport Equation Monte Carlo Methods	Accurate up to the classical Limits
Quantum Approach	Quantum Hydrodynamics	Keep all classical Hydrodynamics features + quantum corrections
	Quantum Monte Carlo Methods	Keep all classical features + quantum corrections
	Quantum kinetic equation	Accurate up to single particle description
	Green's Functions methods	Includes corrections in both space and time domain
	Direction solution of the n-body Schrodinger equation	Can be solved only for small number of particles

1.4.1 Standard Compact Models

Industry has standardized some techniques for compact modeling of devices, these models include charge based model, surface potential based model and conductance based models. Out of these all, surface potential based models are most popular due to its correctness.

1.4.1.1 Charge Based Model

This modeling approach is a traditional way of modeling devices. In this approach, inversion charges present in the channel are calculated using terminal voltages i.e. drain and source voltages and thereafter overall drain current has been calculated. This model describes the working of the device in each region of operation separately. The prominent charge based models are level 1, level 2, and level 3, BSIM 1, HSPICE level 28, BSIM 2, BSIM 3, BSIM 4, and BSIM 5. BSIM 5 is the latest entry in the stack and further BSIM 6 is in the development stage. These models take into consideration the effect of SCE's like DIBL, velocity saturation, mobility degradation etc.

1.4.1.2 Surface Potential Based Model

This is most accurate approach of modeling a semiconductor device. This approach is based on the calculation of potential in the channel of a MOSFET and then calculating current-voltage characteristics. This model is even applicable to the sub-nanometre device nodes. Numerous efforts are being put in to consider the effect of strained silicon in the modeling using this approach.

1.4.1.3 Conductance Based Model

This approach is the most suitable when it comes to short channel devices with low power consumption. This model is used for analog applications. This was first developed by the Swiss Federal Institute of Technology, Switzerland. In other modeling approaches, we always consider Source/ Drain as the reference but here we consider substrate as the reference. This is not commonly used due to its complexity.

Out of all the three methods discussed, no one is accurate. Therefore there is always need for the empirical model which can better describe the physics of the device.

1.5 ORGANIZATION OF THE THESIS WORK:

Chapter2-Literature Survey

This chapter deals with the motivation behind the evolution of Junctionless transistors and how double gate Junctionless transistors can be a strong candidate for future technology nodes.

Chapter3- Surface Potential Based Drain Current Model for Long-Channel Junctionless Double-Gate MOSFET

In this chapter, we deal with the potential distribution using 2-D Poisson's equation and then establishes a relationship between gate voltage and potential in the device for different region of operation of double gate Junctionless transistor. This potential equation is further utilized to find the current dependencies of the device, a drain current model has been obtained.

Chapter4-Results and Discussion

This chapter explains the results obtained from the TCAD simulations of the device and that obtained from the Matlab execution of the derived model.

Chapter5-Conclusion and Future Scope

Here we have explained the impact of various results on the overall performance of the device and how we can further improve it using the previous results.

Chapter 2

Literature Survey

2.1 MOTIVATION

In the conventional CMOS technology, two FET's are separated by the depletion layer formed between them. This depletion layer is formed due to the PN junction formation and gives rise to leakage currents in the device. These leakage currents are highly temperature dependent and increases exponentially with the temperature. These leakages creates many reliability issues with the performance of the device. These currents badly affects the circuit operation at micro levels and degrades the performance by increasing power consumption of the complete circuit. Sometimes n-p-n and p-n-p transistor formation within the tubs disturbs the latch-up phenomenon to be occurring in the CMOS technology.

In the recent years good performance and speed are achieved by using improved design, using some other high quality material, and by scaling device dimensions. But these improvements further produces some technological limitations in the form of short channel effects. In small dimension devices, reduction in threshold voltage at high drain voltages and hot electrons giving rise to surface scattering and DIBL dominates. Junction leakages are of utmost concern while improving the performance of the device at sub-nanometre regime. These junction leakages can be controlled by using ultra-sharp doping profiles of source/drain regions with the channel. But achieving this ultra-sharp doping is a very typical task to perform creating fabrication disadvantages. To overcome these limitations of fabrication industry one need to develop some other technology which can be implemented and fabricated quite easily. This can be done by fabricating the device using a technology where no junctions are formed in the device i.e. by maintaining a constant doping profile. This idea was 1st implemented by J.P.Collinge at Tyndall National institute and resulted in a device called Junctionless transistors (JLFET) [19].

Junctionless transistors are having very small leakage currents and less fabrication complexity due to the uniform doping concentration of source/drain and the channel region. Silicon layer in Junctionless transistors is having very high doping concentration. This high doping degrades the mobility of carriers in that particular region and hence affects the conductivity of the device. This results in poor drive current and transconductance as compared to conventional devices.

2.2 JUNCTIONLESS TRANSISTOR (JLT)

To overcome above challenges imposed due to scaling, a new device called Junctionless transistor is introduced. This device consists of terminals as that of conventional MOSFET i.e. source, drain, gate and channel. But unlike conventional MOSFET this device have a uniform concentration of carriers throughout the channel, source and drain regions. Initially, when no gate voltage is applied, the channel is completely depleted and hence the device is said to be in off state [19]. To make the device conducting, the gate voltage is increased to a considerable value such that depletion diminished within the channel and accumulation of carriers start. In this device to reduce leakages, gate material with a high work function difference is used. This device operates in bulk conduction mode unlike others which operates in surface conduction, hence they provide better on to off current ratio. To improve the conductance of the device doping of silicon bar needs to be very high. Due to high doping, depletion width normally is very small which in turn gives rise to a very small width of silicon layer such that device can be completely off (complete depletion).

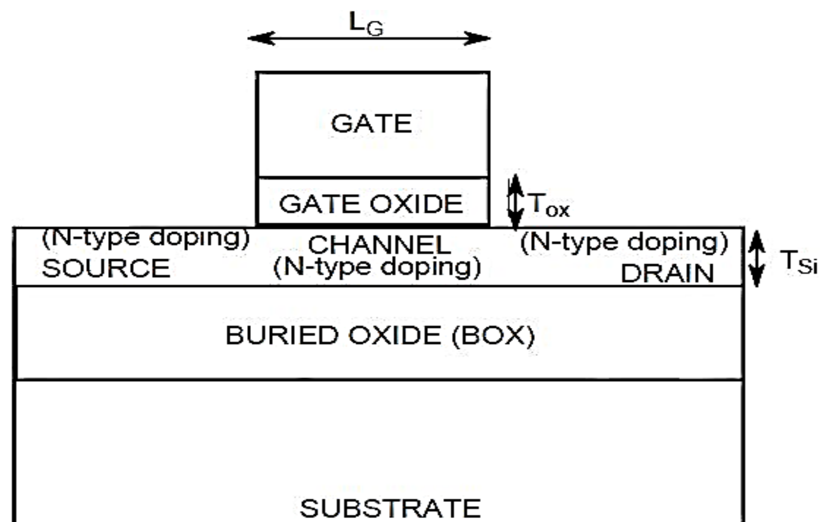

Figure 2.1: Thin Film SOI Junctionless transistor.

Figure 2.1 shows the schematic diagram of Junctionless transistor. Here doping of the pentavalent impurity is added in a high proportion (upto the order of 1e18 or 1e19). Since doping is pentavalent this forms the NFET. Silicon thickness (T_{si}) made to be very small as compared to the channel length. Gate material used can be n-type polysilicon or p-type polysilicon, generally material with high workfunction difference with the body of the device is used. Therefore p-type polysilicon is preferred [22] over others since it is having workfunction of nearly 5.1ev and produces a workfunction difference of approx. 1ev. With no

voltage applied at the gate, the silicon layer is fully depleted. As gate voltage is further increased, depletion width starts diminishing and when gate voltage applied exceeds the flat band voltage then device starts operating in accumulation mode and bulk conduction starts within the device. Off current in the device will be zero until depletion width will be larger than that of silicon thickness otherwise current will still flow from source to drain due to applied drain to source biasing voltage called leakage current.

2.3 DOUBLE GATE JUNCTIONLESS TRANSISTOR (DGJLMOSFET)

The scaling of channel length and other dimensions causes vital operational drawbacks in the device which includes lack of gate control on the device current. Therefore to improve this gate control over the device double gate and multi-gate concept has been introduced [24]. Larger will be the no. of gates in the device better will be the control of gate on channel formation. In multi-gate FET (MuGFET) [16], the gate is formed all around the silicon nanowire such that applied voltage appears all around the gate and hence helps in control of depletion region in the silicon layer [16].

Recently double gate Junctionless transistor has been proposed as a promising candidate for the future generation silicon microelectronics. It is similar to the conventional double gate FET except the fact that channel region is having high and uniform doping concentration throughout the channel in the DGJLFET. The Junctionless transistor is basically a resistor with uniform doping concentration in the silicon body [17].

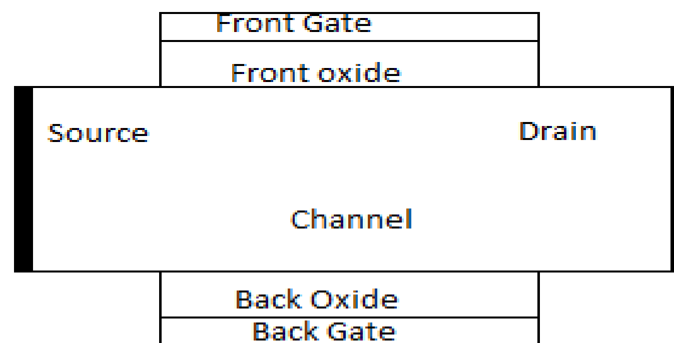

Figure 2.2: Schematic of Double Gate Junctionless FET.

This device performs bulk conduction rather than surface conduction, which is the case of conventional MOSFET [24]. Figure 2.2 shows the structure of double gate Junctionless transistor. Here Source/Drain/Channel region is having uniform doping without the formation of the junction.

Considering the operation of n-channel Junctionless double gate FET, it is evident that it is quite different than that of conventional bulk devices. In JLT's initially due to higher workfunction difference and smaller thickness of silicon layer, device operates in full depletion and complete channel below the gate is having depleted positive charges. Electric field at this point of time is maximum in the channel region due to the presence of depleted charges. Further increasing applied gate voltage brings the device out of depletion slowly and thereby reducing the electric field in the device [20]. At gate voltage equals to the flatband voltage, channel becomes completely neutral. Again increasing gate voltage above flatband voltage generates negative charges in the channel and channel is said to be volume accumulated. Now after accumulation, surface conduction starts in the channel. This surface conduction starts when gate voltage is much higher than that of threshold voltage. Device current here is contributed by both surface conduction and bulk conduction, but bulk conduction is dominating factor here.

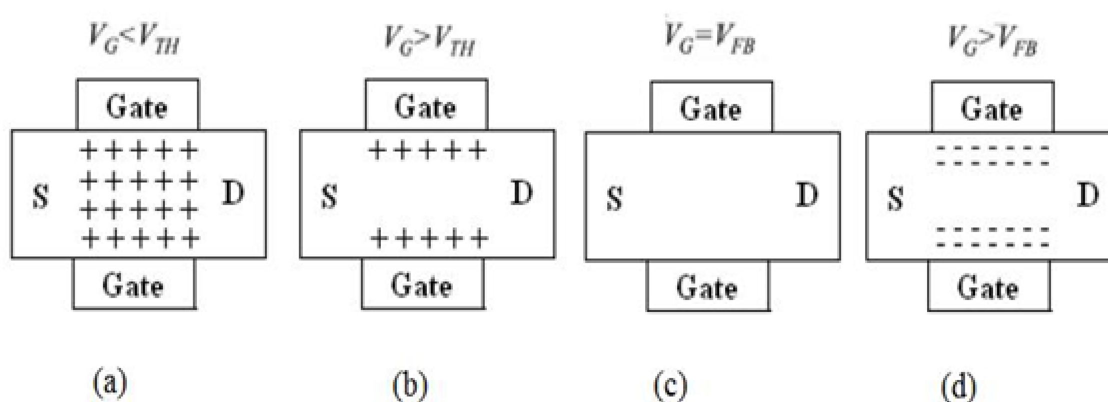

Figure 2.3: Various modes of operation of DGJLMOSFET. a) Full depletion mode. b) Partial depletion mode. c) Flat band condition. d) Accumulation mode [19]

Figure 2.3 completely describes the operation of double gate Junctionless MOSFET. When applied gate voltage is less than threshold voltage then device operates in full depletion mode. When applied voltage exceeds the threshold voltage then device enters into semi depleted or partial depletion mode [19]. Further increasing gate voltage upto flatband voltage, device enters into flatband mode of operation. When gate voltage becomes way greater than flatband voltage then device operates in accumulation mode. To turn off the device, channel needs to be fully depleted which is a typical task due to the high doping of channel. Therefore to achieve this task silicon layer thickness needs to be maintained very thin (comparable to the length of the channel).

2.4 JUNCTIONLESS TRANSISTORS: A REVIEW

It became extremely challenging now a days to implement the junctions beyond 32 nm for the conventional MOSFETs due to the need of ultra-sharp doping profiles which aren't easy to obtain [25]. However, devices with the 14nm node are present in the market recently but that requires a high degree of precision and fabrication complexity resulting in enhanced prices for products. To overcome these challenges, recently a new idea of device fabrication based on the Lilienfeld's first transistor architecture [26] was developed at Tyndall National institute by J.P. Colinge. This device doesn't have any metallurgical junctions and was successfully fabricated on silicon [25] [29] [30]. New designs which are proposed, include nanowire gate all around (GAA) architectures [27] [29] [31], vertically stacked devices [32], tri-gated nanowire architectures with silicon on insulator (SOI) [25] and bulk substrates [33]. To further simplify fabrication process planar architectures on bulk substrates were also developed [28] in recent years. The Junctionless transistor is the device which is having an ultra-thin layer of a highly doped semiconductor as a bar which is volume depleted in the OFF state (at zero gate bias) due to its workfunction difference with that of the gate material. This device results in extremely low leakage current [25]. By applying a positive gate voltage, depletion layer start diminishing and bands starts entering into flat band condition. Further increasing gate bias forces the device into accumulation which in turn increases drain current [29]. The gate terminal of Junctionless transistor helps in modulating the resistance of the heavily doped semiconductor; hence, the device can be seen as a gated resistor [25] [34]. Trigate Junctionless transistors (JLTs) with the channel length of 1 µm were demonstrated on silicon-on-insulator (SOI) substrates [25]. Recently 50nm [29] and 26 nm [35] gate length JLT's performance have been reported. P-channel JLTs on Germanium-on-insulator (GeOI) substrates [36] and N-channel JLT's with poly-Si nanowire channels have also been reported [30]. Junctionless transistors can be widely used in many applications where performance is of utmost concern. It has been observed that JLT can be a promising candidate for flash memory application, because of which this concept was applied to NAND flash and 3D integrated flash memories like vertical stacked-array-transistor memory for solid state drives [37] and bit cost scalable memories. This device was also shown as a suitable candidate for dynamic and static random access memory [26] applications. Recent studies also include temperature dependence of electrical characteristics, effects of strain on JLT performance, its ballistic nature at shorter channel lengths, and radio frequency (RF) performance analysis. This device also offers nearly ideal subthreshold slope due to which it is a promising candidate for analog applications. Devices mentioned above offers several advantages over the conventional bulk MOSFETs which are as follows:

1. Reduced fabrication process complexity [28][39]
2. Better scalability [38]
3. High mobility [41].
4. ON state of the device offers Low electric field. [28]
5. High ON/OFF current ratio [19].
6. Nearly ideal sub-threshold slope [40]

We here discuss the milestones during the evolution of JLTs. Starting phases of the evolution of the device include the gate all around Junctionless transistor architecture, known as a nanowire pinch-off FET [27] and Vertical Slit FET (VeSFET) [32]. The schematics of nanowire pinch-off FET and VeSFET are shown in Figure 2.4. The VeSFET is a double gated Junctionless transistor wherein the two gates can be operated independently. Independent gate architecture allows the designer to realize logic functions such as AND, OR etc. Its vertical assembly makes the VeSFET an attractive device for 3D integration [32].

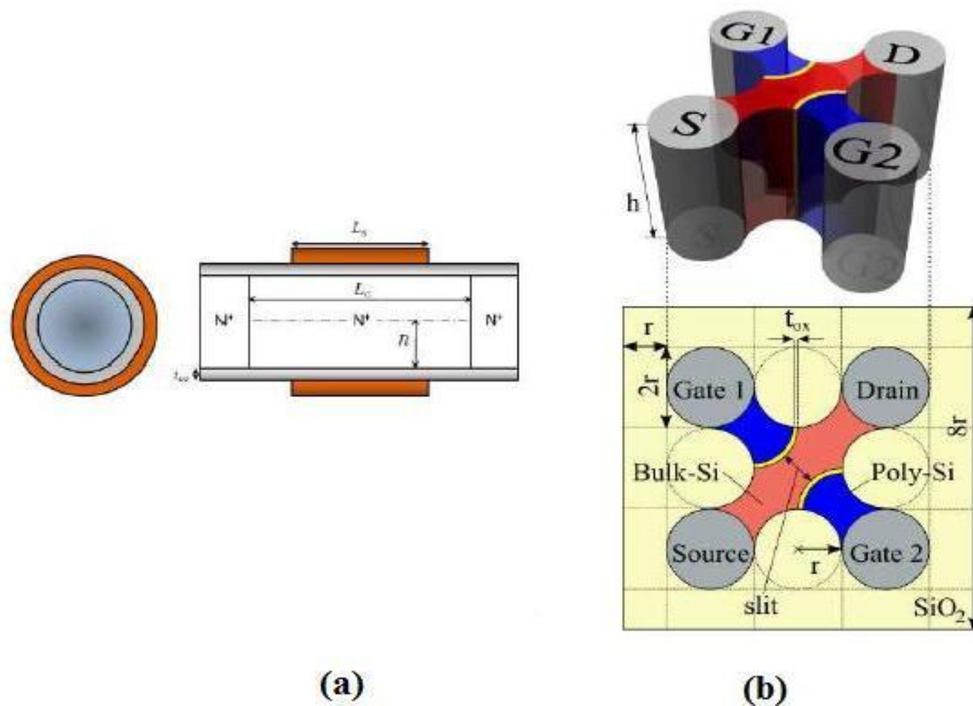

Figure 2.4: Schematic representation of (a) nanowire pinch-off FET [31] (b) Vertical Slit FET (VeSFET) [32]

However, channel length scaling to the ultra-short regime would be difficult due to the circular nature of the gate. The first Junctionless transistor was fabricated by Collinge et al, at Tyndall National institute in 2010. They illustrated the JLTs as a potential device alternative to the

conventional MOSFETs. The ON current demonstrated at 1μm channel length is on par with the conventional MOSFET [25]. They have demonstrated a device with negligible DIBL, near-ideal subthreshold slope etc. Even in the recent short channel (& 50nm) Junctionless transistor fabricated by Colling et al., they show that the electrostatic integrity is intact [40]. Later, it was shown by Choi et al., [29], that a short channel length (& 50nm) GAA Junctionless FET has an unacceptable variability with nanowire width variations. A large shift (& 3V) in threshold voltage is observed just by doubling the width of nanowire. An inversion mode transistor fabricated with a similar process flow does not have such variability. Very recently, Rios et al. [35], have a contradicting version of results shown by [25] and [40]. They show that for a given OFF current JLTs have lower ON current with an increased short channel effects. In view of the above-mentioned shortcomings of Junctionless transistors, there is a tremendous need for reducing the short channel effects to make the device an attractive alternative for low standby power applications.

2.5 SUMMARY

As the scaling of device dimensions becoming very crucial in conventional CMOS devices now a days, therefore, numerous researches have been carried out now a days to improve the functionality and performance of the device and to find out an alternative to this very dominant technology. But this task has to be done by keeping in mind that Moore’s law can be justified further. The Most popular alternative adopted for this is use of double gate devices which provides better stability and performance. However, with the reduction in integrated node technology short channel effects (SCEs) are becoming very crucial in delivering the performance of the devices. SCEs loosen the control of the gate voltage on drain current. This control is lost due to increased charge-sharing from the drain/source regions, which leads to the degradation of the subthreshold slope and the increase in drain off-current. Numerous efforts had been put by researchers to eliminate the undesirable effects caused by SCEs in the last decade. Various Engineering techniques have been employed to improve controlled channel doping profile but this task seems to be very tedious in case of extremely thin-film components which imply problems in yield and reliability of the device. Therefore, it is challenging to fabricate a device at small dimensions which is having low power and better speed of operation. There is always a trade-off between speed and power, therefore, an optimized solution has to be found out. On the other hand, buried oxides thinner than 100 nm is needed to avoid coupling, which trades-off with junction capacitance considerations. Multiple gate SOIs offer a better immunity against SCE but they are difficult to integrate into the current CMOS fabrication technology. Recently developed Junctionless MOSFETs, an alternative solution in suppressing SCEs better than conventional inversion-mode devices is discussed. Therefore, a systematic analysis of the effect of Junctionless MOSFETs is required to aid in understanding its efficiency in suppressing SCE in deep sub-micron CMOS devices.

CHAPTER 3

MODELING OF JUNCTIONLESS DOUBLE-GATE MOSFET

3.1 INTRODUCTION

The Junctionless transistor is a prominent candidate for future technology nodes. This device is fabricated using high impurity concentrations throughout the channel which results in the formation of no junctions. This Junctionless device poses many advantages like easier fabrication technology, high current swing (ON/OFF current ratio), nearly ideal subthreshold slope, low DIBL, low source/drain resistances.

DG JLFET is having excellent electrostatic behavior therefore it becomes necessary to develop an accurate model to describe the correct functionality of this device. There are many approaches to develop the model of a device, but out of these surface potential model is very popular because of its accuracy in compact modeling. This model uses various approximations. As first of all we are considering a long channel device therefore lateral component of the electric field can be neglected and only perpendicular component originating due to applied gate voltage will contribute towards the potential in the channel thereby making the calculations limited to one dimensional only and simplifying calculations. Gradual channel approximation technique is used to calculate the potential within this region. This analysis will fail if we will consider short channel devices because here electric field will be having two-dimensional behavior, therefore 2-D Poisson equation will be solved for this purpose.

The Model has been developed using 2-D Poisson equation for the symmetrical Junctionless double gate MOSFET structure by considering only the mobile charges. Surface potential has been calculated for each region of operation of device i.e. deep depletion, partial depletion and accumulation regions. Further by using a pao-sah integral approximation, full range drain current has been calculated separately for each region of operation. The Lambert-W function is used to determine surface potential in sub-threshold region due to its accuracy.

3.2 STRUCTURE AND OPERATION OF JUNCTIONLESS DG MOSFET

This device is having a silicon bulk which is doped with high concentration of impurity. Let doping concentration of silicon layer is N_{si}. This doping is uniform throughout the channel and source/drain. Let t_{si} be the silicon thickness and t_{ox} be the oxide thickness. Oxide thickness at both the interfaces i.e. front oxide and back oxide are same. Channel length has denoted by L. Polysilicon has been used as gate material for both the gates. The Structure described above is

shown in the figure 3.1 below.

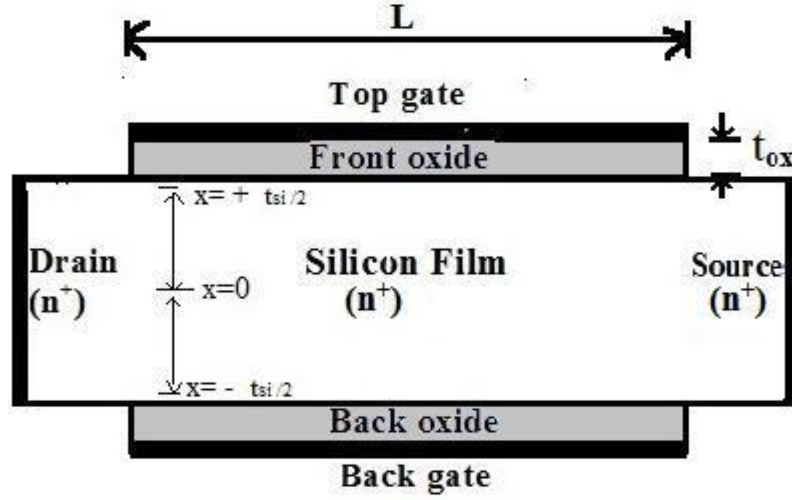

Figure 3.1: Schematic of Junctionless DG MOSFET.

Considering the case of n-channel Junctionless DGFET, its operating principle is quite different than that of the inversion mode FET. At negative gate voltages, majority carriers are pushed back such that it will result in deep depletion and hence no current will flow ideally. As gate voltage increases, depletion starts vanishing and steadily bulk conduction starts in the device. When gate voltage becomes equals to flatband voltage then maximum bulk current will flow in the device. When gate voltage has been further increased above flatband voltage then surface conduction starts in the device and increases further with the increase in gate voltage.

3.3 SURFACE POTENTIAL MODEL

According to classical physics, Poisson's equation which relates surface potential with the charge density in the silicon body can be written as

$$\frac{d^2\psi}{dx^2} = \frac{q}{\varepsilon_{si}} N_D \left[exp\left(\frac{\psi - V}{v_t}\right) - 1\right] \qquad Eq\ (3.3.1)$$

Here ε_{si} represents the permittivity of silicon material, v_t represents thermal voltage, V is quasi-fermi potential of the silicon body, q is the positive electronic charge and ψ(x) represents surface potential distribution along the width of the silicon layer. Boundary conditions for the validity of surface potential in JL DGFET shown above in figure 3.1 are given below as [42]

$$\frac{d\psi}{dx}(x = 0) = 0 \ \ , \psi\left(\pm\frac{t_{si}}{2}\right) = \psi_s$$

$$\frac{d\psi}{dx}\left(x = \pm\frac{t_{si}}{2}\right) = \frac{C_{ox}}{\varepsilon_{si}}\left(V_G - V_{fb} - \psi(\pm\frac{t_{si}}{2})\right) \qquad Eq\ (3.3.2)$$

$$Q_{SC} = -2\varepsilon_{si}\frac{d\psi}{dx}\left(x = \pm\frac{t_{si}}{2}\right) = -2C_{ox}\left(V_G - V_{fb} - \psi_s\right) \qquad Eq\ (3.3.3)$$

$$E_s^2 = \frac{2qN_D v_T}{\varepsilon_{si}}\left[exp\left(\frac{\psi_s - V}{v_T}\right) - exp\left(\frac{\psi_0 - V}{v_T}\right) - \left(\frac{\psi_s - \psi_0}{v_T}\right)\right] \qquad Eq\ (3.3.4)$$

Q_{SC} represents the space charge density per unit area, C_{ox} represents oxide capacitance per unit area, V_{fb} is flat band voltage and E_s represents electric field density in the device. Simplifying terms by using Taylor series expansion as shown below

$$exp\left(\frac{\psi_0 - V}{v_T}\right) = 1 + \frac{\psi_0 - V}{v_T}$$

Therefore

$$E_s^2 = \frac{2qN_D v_T}{\varepsilon_{si}}\left[exp\left(\frac{\psi_s - V}{v_T}\right) - 1\right] \qquad Eq\ (3.3.5)$$

Further substituting equation (3.3.5) in equation (3.3.4)

$$\left(V_G - V_{fb} - \psi_s\right)^2 = \beta v_T\left[exp\left(\frac{\psi_s - V}{v_T}\right) - 1\right] \qquad Eq\ (3.3.6)$$

Here β is an intermediate parameter which can be described as $\beta = \frac{2qN_D\varepsilon_{si}}{C_{ox}^2}$.

Above equation (3.3.6) is valid for finding surface potential in the channel in accumulation region of operation.

Now to calculate surface potential in a partly depleted mode we have used depletion approximation. This will give a relationship between ψ_s & V.

$$\Psi(x) = \psi_0 - \frac{qN_D}{2\varepsilon_{si}}\left[x - \left(\frac{t_{si}}{2} - x_d\right)\right]^2 \qquad Eq\ (3.3.7)$$

at $x_d \le \frac{t_{si}}{2}$, replacing ψ_0 with V.

$$\psi_s = V - \frac{qN_D}{2\varepsilon_{si}}{x_d}^2 \qquad Eq\ (3.3.8)$$

Space charge density in this limit is given by

$$Q_{SC} = 2qN_D x_d = -2C_{ox}\left(V_G - V_{fb} - \psi_s\right) \qquad Eq\ (3.3.9)$$

Depletion width in partly depleted mode hence can be calculated as

$$x_d = -\frac{C_{ox}(V_G - V_{fb} - \psi_s)}{qN_D} \qquad Eq\ (3.3.10)$$

Further substituting the value of x_d in equation (3.3.8), we obtain the surface potential dependencies in partly depleted mode as below

$$\psi_s = V - \frac{1}{\beta}(V_G - V_{fb} - \psi_s)^2 \qquad Eq\ (3.3.11)$$

Above expression for surface potential is valid only when the device operates in partly depleted mode.

We know that applied gate voltage appears across surface potential, oxide interface and to overcome work function difference and make the bands flat.

$$V_{G=} V_{fb} + \psi_S + \psi_{ox}$$

Also

$$\psi_{ox} = -\frac{Q_{SC}}{C_{ox}} = -\frac{qN_D x_d t_{ox}}{\varepsilon_{ox}}$$

If $x_d = \frac{t_{si}}{2}$ then $V_{G=} V_{th}$

Therefore equation for the threshold voltage can be written as below

$$V_{th} = V_{fb} - \frac{qN_D t_{si}^2}{8\varepsilon_{si}} - \frac{qN_D t_{si}}{2C_{ox}} \qquad Eq\ (3.3.12)$$

Above equation of threshold voltage doesn't consider the effect of drain bias. Here only vertical electric field of device has been taken into consideration. We may also write threshold voltage as

$$V_{th} = V_{fb} - \frac{qN_D t_{si}}{2C_{eff}}$$

Where

$$\frac{1}{C_{eff}} = \frac{1}{4C_{si}} + \frac{1}{C_{ox}}$$

Further solving to obtain surface potential in subthreshold regime we combine equations (3.3.3) & (3.3.4)

$$\frac{C_{ox}}{\varepsilon_{si}}\left(V_G - V_{fb} - \psi_s\right) = \sqrt{\frac{2qN_D v_T}{\varepsilon_{si}}\left[exp\left(\frac{\psi_s - V}{v_T}\right) - exp\left(\frac{\psi_0 - V}{v_T}\right) - \left(\frac{\psi_s - \psi_0}{v_T}\right)\right]}$$

Let

$$\frac{\psi_0 - \psi_s}{v_T} = \gamma$$

$$\left(V_G - V_{fb} - \psi_s\right) = \sqrt{\frac{2qN_D V_T \varepsilon_{si}}{C_{ox}^2}\left[\gamma + \exp\left(\frac{\psi_s - V}{v_T}\right) - \left(\frac{\psi_0 - V}{v_T}\right)\right]} \qquad Eq\ (3.3.13)$$

After solving further

$$\left(V_G - V_{fb} - \psi_s\right) = -\sqrt{\frac{2qN_D V_T \varepsilon_{si}\gamma}{C_{ox}^2}\left[1 - \left(\frac{1 - e^{-\gamma}}{\gamma}\right)\exp\left(\frac{\psi_0 - V}{v_T}\right)\right]} \qquad Eq\ (3.3.14)$$

Now applying binomial expansion to the terms in square root and exponential term

$$\left(V_G - V_{fb} - \psi_s\right) = -\sqrt{\frac{2qN_D V_T \varepsilon_{si}\gamma}{C_{ox}^2}\left[1 - \exp\left(\frac{\psi_0 - V}{v_T}\right)\right]}$$

$$\left(V_G - V_{fb} - \psi_s\right) = -\sqrt{\frac{2qN_D V_T \varepsilon_{si}\gamma}{C_{ox}^2}\left[1 - \frac{1}{2}\exp\left(\frac{\psi_0 - V}{v_T}\right)\right]}$$

Putting value of γ in above equation

$$\left(V_G - V_{fb} - \psi_s\right) = -\sqrt{\frac{2qN_D \varepsilon_{si}}{C_{ox}^2}\left(\psi_0 - \psi_s\right)\left[1 - \frac{1}{2}\exp\left(\frac{\psi_0 - V}{v_T}\right)\right]}$$

We know

$$\psi_0 - \psi_s = \frac{qN_D t_{si}^2}{8\varepsilon_{si}} \qquad Eq\ (3.3.15)$$

Putting this value of $\psi_0 - \psi_s$ in above equation, we get

$$\left(V_G - V_{fb} - \psi_s\right) = -\frac{qN_D t_{si}}{2C_{ox}}\left[1 - \frac{1}{2}\exp\left(\frac{\psi_0 - V}{v_T}\right)\right] \qquad Eq\ (3.3.16)$$

Also

$$V_{fb} = V_{th} + \frac{qN_D t_{si}}{2C_{ox}} + \frac{qN_D t_{si}}{8C_{si}} \qquad Eq\ (3.3.17)$$

Now putting this value of V_{fb} in the above equation and solving this by using Lambert function as a promising function we get the expression for surface potential in the subthreshold region.

$$\Psi_s = V_G - V_{th} - \frac{qN_D t_{si}}{8C_{si}} - v_T W[m] \qquad Eq\ (3.3.18)$$

Where W[m] is Lambert function with its variable as m and Lambert function may be described as the inverse function of $y=xe^x$. Here

$$m = \frac{qN_D t_{si}}{4C_{ox} v_t} exp\left(\frac{V_G - V - V_{th}}{v_t}\right)$$

3.4 DRAIN CURRENT MODEL

Drain current in the device can be calculated by finding mobile charges density which is given as

$$Q_m = Q_{sc} - Q_d \qquad Eq\ (3.4.1)$$

Also

$$Q_d = qN_D t_{si}$$

Current continuity equation expresses current as

$$I_{ds} = \mu W_d Q_m \frac{dv}{dy} \qquad Eq\ (3.4.2)$$

Here μ represents the mobility of majority charge carriers and W_d represents the width of the device. Now by making use of gradual channel approximation and integrating $I_{ds}dy$ using pao-sah model for current calculation we may write it as

$$I_{ds} = -\mu \frac{W_d}{L} \int_0^{V_{ds}} Q_m dv \qquad Eq\ (3.4.3)$$

$$I_{ds} = \mu \frac{W_d}{L} \int_0^{V_{ds}} \left[2C_{ox}\left(V_G - V_{fb} - \psi_s\right) + Q_d \right] dv \qquad Eq\ (3.4.4)$$

Now here we have assumed that voltage applied at source terminal is zero and some voltage V_{ds} has been applied at drain terminal. Based on the applied gate voltage device will operate in different regions of operation i.e. accumulation, partial depletion and subthreshold.

Consider $V_G \geq V_{fb} + V_{ds}$ then device will operate in accumulation region and to find out current, let's first expand exponential term in equation 3.3.6 using binomial expansion we obtain

$$\left(V_G - V_{fb} - \psi_s\right)^2 = \beta[\psi_s - V] \qquad Eq\ (3.4.5)$$

Now differentiating equation 3.3.6 w.r.t. ψ_s.

$$exp\left(\frac{\psi_s - V}{v_t}\right) = -2 \frac{\left(V_G - V_{fb} - \psi_s\right)}{\beta\left[1 - \frac{dv}{d\psi_s}\right]} \qquad Eq\ (3.4.6)$$

Also after rearranging equation 3.3.6, it may be written as

$$exp\left(\frac{\psi_s - V}{v_t}\right) = 1 + \frac{(V_G - V_{fb} - \psi_s)^2}{\beta v_t} \qquad Eq\ (3.4.7)$$

On comparing equations (3.4.6) and (3.4.7), finally we get the expression

$$\frac{dv}{d\psi_s} = 1 + \frac{2v_t\left(V_G - V_{fb} - \psi_s\right)}{\beta v_t + (V_G - V_{fb} - \psi_s)^2} \qquad Eq\ (3.4.8)$$

Now rewriting and splitting the equation (3.4.4) into two parts

$$I_{ds} = \underbrace{\mu \frac{W_d Q_d}{L} dv \Big|_S^D}_{C1} + \underbrace{\mu \frac{W_d}{L} \int 2C_{ox}\left(V_G - V_{fb} - \psi_s\right) \frac{dv}{d\psi_s}\, d\psi_s}_{C2} \qquad Eq\ (3.4.9)$$

Now 1st solving integral present in the C2 part of above equation (3.4.9)

$$C1 = \mu \frac{W_d}{L} \int 2C_{ox}\left(V_G - V_{fb} - \psi_s\right)\left(1 + \frac{2v_t\left(V_G - V_{fb} - \psi_s\right)}{\beta v_t + (V_G - V_{fb} - \psi_s)^2}\right) d\psi_s$$

$$C1 = \mu \frac{W_d}{L} \int [2C_{ox}\left(V_G - V_{fb} - \psi_s\right) + \frac{4C_{ox}v_t\left(V_G - V_{fb} - \psi_s\right)^2}{\beta v_t + (V_G - V_{fb} - \psi_s)^2}] d\psi_s$$

$$C1 = \underbrace{-\mu \frac{W_d C_{ox}(V_G - V_{fb} - \psi_s)^2}{L}\Bigg|_S^D}_{C3} + \underbrace{\mu \frac{W_d}{L}\int \frac{4C_{ox}v_t(V_G - V_{fb} - \psi_s)^2}{\beta v_t + (V_G - V_{fb} - \psi_s)^2} d\psi_s}_{C4} \quad Eq\ (3.4.10)$$

Now considering only C4 term from above equation and solving further

$$C4 = \mu \frac{W_d}{L}\int \frac{4C_{ox}v_t(V_G - V_{fb} - \psi_s)^2}{\beta v_t + (V_G - V_{fb} - \psi_s)^2} d\psi_s$$

$$C4 = \frac{4C_{ox}}{\beta}\mu \frac{W_d}{L}\int \frac{(V_G - V_{fb} - \psi_s)^2}{\left(\frac{V_G - V_{fb} - \psi_s}{\sqrt{\beta v_t}}\right)^2 + 1} d\psi_s$$

$$C4 = 4C_{ox}v_t\,\mu \frac{W_d}{L}\int \frac{\left(\frac{V_G - V_{fb} - \psi_s}{\sqrt{\beta v_t}}\right)^2}{\left(\frac{V_G - V_{fb} - \psi_s}{\sqrt{\beta v_t}}\right)^2 + 1} d\psi_s$$

Solving above expression will result in arctan formulation of above integral as shown below

$$C4 = 4C_{ox}v_t\,\mu \frac{W_d}{L}\left[\left(\frac{V_G - V_{fb} - \psi_s}{\sqrt{\beta v_t}}\right) - arctan\left(\frac{V_G - V_{fb} - \psi_s}{\sqrt{\beta v_t}}\right)\right] \quad Eq\ (3.4.11)$$

Further solving and combining equations (3.4.9), (3.4.10), (3.4.11) we get

$$I_{ds} = \mu \frac{W_d}{L}\Bigg[Q_d V - C_{ox}(V_G - V_{fb} - \psi_s)^2 - 4C_{ox}v_t(V_G - V_{fb} - \psi_s) + 4C_{ox}v_t\sqrt{\beta v_t}\,arctan\left(\frac{V_G - V_{fb} - \psi_s}{\sqrt{\beta v_t}}\right)\Bigg]\Bigg|_S^D \quad Eq\ (3.4.12)$$

This equation of drain current is valid when Junctionless DG MOSFET will operate in accumulation region only. Surface potential is been calculated from source to drain terminal i.e. x=0 to x=L.

Now consider the case where our device operates in partially depleted mode ($V_{th} < V_G < V_{fb}$)

From equation (3.3.11)

$$\psi_s = V - \frac{1}{\beta}(V_G - V_{fb} - \psi_s)^2$$

Differentiating this equation w.r.t. ψ_s

$$\frac{dv}{d\psi_s} = 1 - \frac{2}{\beta}\left(V_G - V_{fb} - \psi_s\right) \qquad Eq\ (3.4.13)$$

Now current in partially depleted mode can be written as

$$I_{ds} = \mu \frac{W_d}{L} \int_0^{V_{ds}} \left[2C_{ox}\left(V_G - V_{fb} - \psi_s\right) + Q_d\right] \frac{dv}{d\psi_s}\, d\psi_s$$

$$I_{ds} = \mu \frac{W_d Q_d}{L} dv\Big|_S^D + \mu \frac{W_d}{L} \int 2C_{ox}\left(V_G - V_{fb} - \psi_s\right) 1 - \frac{2}{\beta}\left(V_G - V_{fb} - \psi_s\right) d\psi_s \quad (3.4.14)$$

On integrating above equation

$$I_{ds} = \mu \frac{W_d}{L}\left[Q_d V - C_{ox}\left(V_G - V_{fb} - \psi_s\right)^2 + \frac{4C_{ox}}{3\beta}\left(V_G - V_{fb} - \psi_s\right)^3\right]\Big|_S^D \qquad Eq\ (3.4.15)$$

This is the model equation for the amount of current when our device is operating in partially depleted mode. When applied gate voltage is less than the threshold voltage of the device then device operates in deep depletion mode or subthreshold mode. Here negligible current flows in the device. Current flowing in the subthreshold mode of operation is also known as off current of the device. Now to find out this current consider the equation (3.3.18)

$$\psi_s = V_G - V_{th} - \frac{qN_D t_{si}}{8C_{si}} - v_T W[m]$$

Where W[m] is Lambert function with its variable as m.

$$m = \frac{qN_D t_{si}}{4C_{ox} v_t} exp\left(\frac{V_G - V - V_{th}}{v_t}\right)$$

Also we know that

$$I_{ds} = \mu \frac{W_d}{L} \int_0^{V_{ds}} \left[2C_{ox}\left(V_G - V_{fb} - \psi_s\right) + Q_d\right] dv$$

Now differentiating equation (3.3.18) w.r.t ψ_s, we obtain

$$\frac{dv}{d\psi_s} = \left[\frac{1 + W[m]}{W[m]}\right] \qquad Eq\ (3.4.16)$$

Solving (3.4.16) and (3.4.4)

$$I_{ds} = \mu \frac{W_d}{L} 2C_{ox} v_t \int_{\psi_0}^{\psi_s} (1 + W[m]) d\psi_s \qquad Eq\ (3.4.17)$$

Where ψ_0 and ψ_s being the surface potential at x=0 and x=L respectively.

Final equation of drain current in subthreshold region is obtained by solving above equation

$$I_{ds} = \mu \frac{W_d}{L} v_t^2 (1 + p)(s - q) \qquad Eq\ (3.4.18)$$

Where p = $W\left[\frac{qN_D t_{si}}{4C_{ox} v_t} exp\left(\frac{V_G - V_{th}}{v_t}\right)\right]$ and q = $W\left[\frac{qN_D t_{si}}{4C_{ox} v_t} exp\left(\frac{V_G - V_D - V_{th}}{v_t}\right)\right]$

Now drain current equations for all the regions of operation has been derived. Therefore we can easily find out full range drain current for the entire range of gate voltages by merging them.

CHAPTER 4

RESULTS AND DISCUSSION

The results obtained from the above modeling of Junctionless double gate MOSFET are being validated with the numerical simulation of the same device using Silvaco TCAD ATLAS tool. Since here we have developed a long channel model therefore Lombardi mobility model has been used to better understand the dependence on the impurity concentration and take into consideration the effect of traverse as well as the longitudinal electric field. SRH (Shockley-Read-Hall) recombination model and CVT model has also been used throughout the numerical simulations. Channel length has been considered to be 1um to avoid short and narrow width effects. To avoid parasitic effects within the source and drain edges, source/drain length has been considered to be 10nm. Gate workfunction has been considered to be 5.2 eV. Uniform doping concentration of silicon bar has been maintained at 10^{19} /cm^3. Effective mobility of the carriers has been considered to be 100 cm^2/V. The thickness of silicon bar (t_{si}) and oxide (t_{ox}) has been considered to be 10 nm and 8 nm respectively. After making all these parametric considerations, various analysis has been performed like calculation of surface potential, output characteristics and transfer characteristics by considering various other scenarios of parametric variations. Temperature for the complete set of simulations has been considered to be 300 K.

4.1 SURFACE POTENTIAL VS GATE VOLTAGE ANALYSIS

4.1.1 Device Structure (Channel Length=1um)

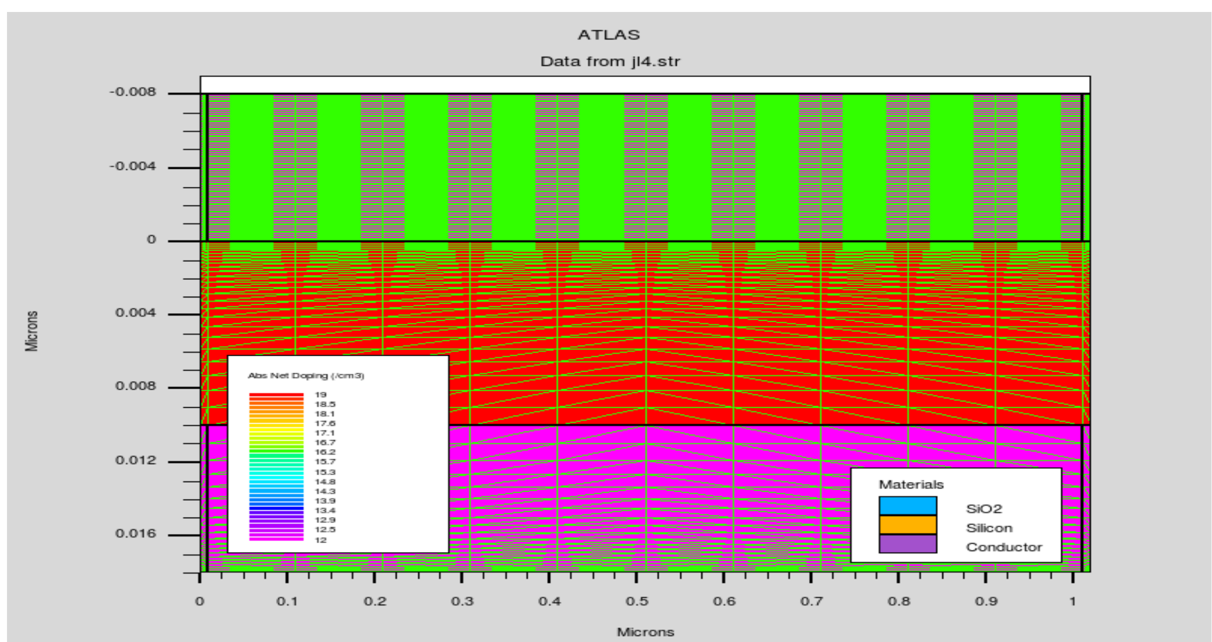

Figure 4.1: Device Structure of JL DG MOSFET at a channel length of 1um.

4.1.2 With the Variation in the doping concentration of Silicon Bar

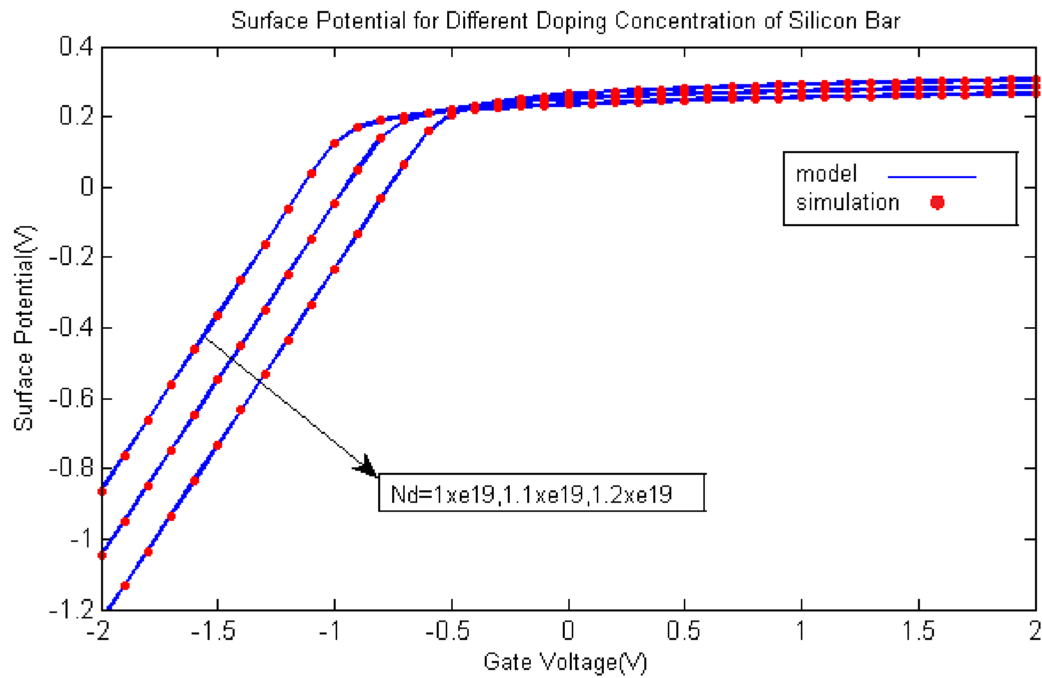

Figure 4.2: Surface Potential variation of JL DG MOSFET with change in the Doping concentration of channel and Source/Drain.

Here doping concentration in the silicon bar has been varied as shown above in figure 4.2. A gate voltage sweep from -2V to 2V with step size of 0.5V has been obtained to better understand the behavior of the device. Quasi-fermi potential for the device has been maintained to be zero (V=0). When substrate doping has been increased then surface potential tend to become more negative for the lower range of gate voltages.

4.1.3 With the Variation in Oxide Thickness

As the oxide thickness of device has been varied, it starts offering more accumulated distribution of potentials in the channel region with the change in gate voltage. Figure 4.3 shows this distribution of surface potential at V=0.

4.1.4 With the Variation in Silicon Thickness (t_{si})

Silicon thickness plays a vital role in defining characteristics of the device. More will be the bar thickness more will be the carriers that can accumulate in the device and hence contributes more towards drain current and potential in the device. The surface potential curve for this scenario is shown below in figure 4.4.

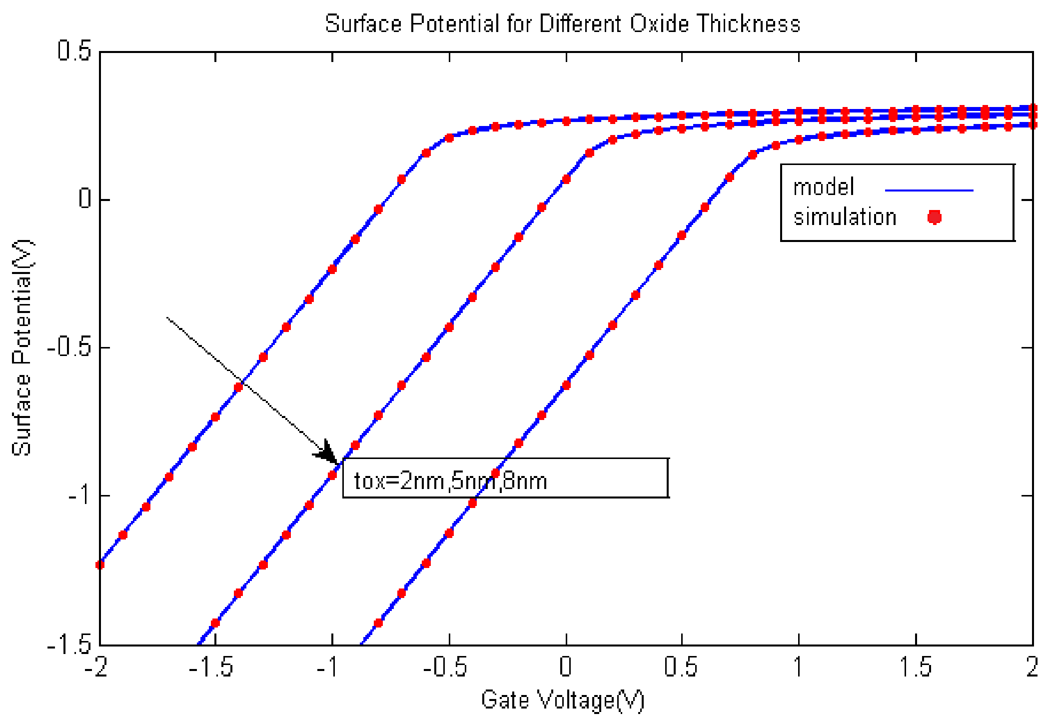

Figure 4.3: Surface Potential variation of JL DG MOSFET with change in oxide thickness.

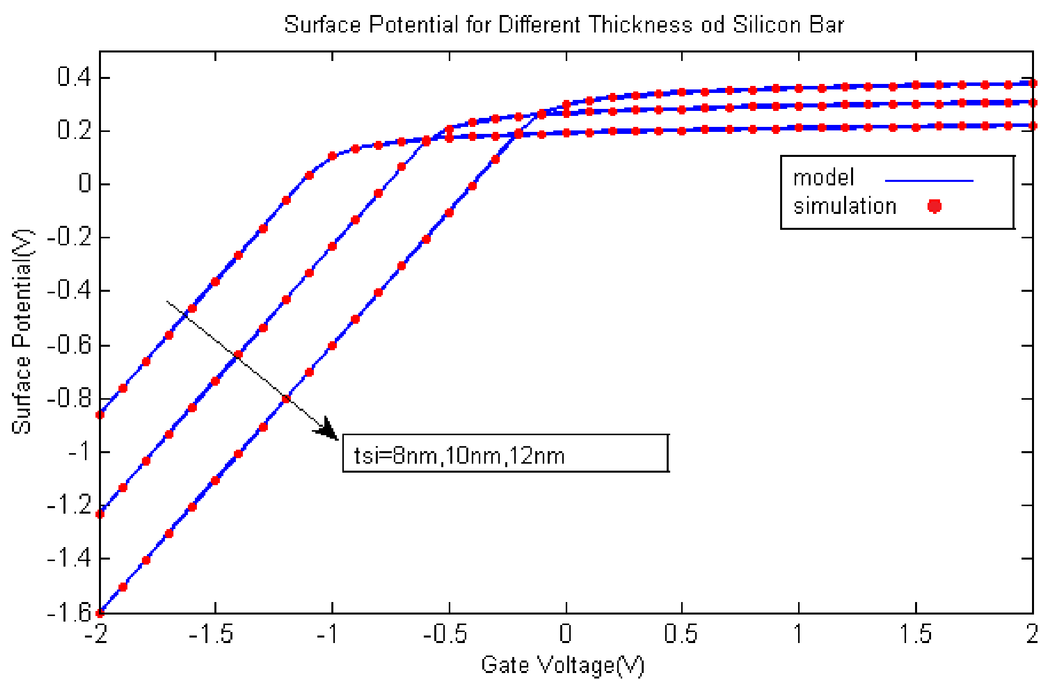

Figure 4.4: Surface potential variation with change in silicon bar thickness in JL DG MOSFET.

4.2 THRESHOLD VOLTAGE ANALYSIS

The threshold voltage is an important parameter in the device, it describes the current behavior of the device. It may be defined as the minimum voltage that has to be applied to the gate terminal such that device starts conducting. For better conduction in the device, threshold voltage should be as small as possible.

For this analysis, some preliminary considerations have been made. Channel length has been considered to be 50nm. The length of source and drain regions are considered to be 10nm each to avoid parasitic effects. Silicon bar thickness is 10nm and oxide thickness has been maintained to be 1.5 nm. The doping concentration in the channel and Source/Drain have been maintained to be 10^{18} /cm^3. A constant voltage of 1V has been applied at drain terminal. Some parametric variations has been performed to obtain the above analysis. These include the change of gate material and workfunction, change of silicon thickness, change of doping in the channel. Results obtained for this analysis are tabulated as shown below. These results are obtained from numerical simulation of the device using Silvaco TCAD Atlas tool.

Table 4.1 Threshold Voltage calculation for Different Gate Materials of JL DGFET.

S.NO.	***Gate Material Used***	***Threshold Voltage (V_{th})***
1.	Aluminium(Al)	-0.483495 V
2.	n^+ polysilicon	-0.413493 V
3.	Molybdenum (Mo)	-0.0535928 V
4.	$MoSiO_2$	0.216505 V
5.	p^+ polysilicon	0.66646 V

Table 4.1 shows that threshold voltage of the device is highly dependent on the Gate material used. It can vary in the large range of scale (from negative values to positive values) only by changing gate material used and keeping other parameters as it is. By changing the gate material used, we are changing the workfunction of the gate material and hence the flat band voltage of the device. As it is evident from equation (3.3.12), greater will be the flat band voltage higher will be threshold voltage and vice versa.

Table 4.2 shows the threshold voltage values obtained by changing the thickness of silicon bar used in our device. Here we have considered n^+ polysilicon as the gate material. From equation (3.3.12) it is evident that with the increase in silicon thickness threshold voltage of the device decreases and same behavior has been obtained here. Therefore simulation and model results are in good agreement and showing the same behavior.

Table 4.2: Threshold Voltage calculation with the change in Silicon Thickness of JL DGFET.

S.NO.	***Silicon Thickness (t_{si})***	***Threshold Voltage (V_{th})***
1.	5 nm	-0.372179 V
2.	8 nm	-0.399408 V
3.	10 nm	-0.413493 V
4.	12 nm	-0.440859 V
5.	15 nm	-0.518933 V

Now considering the effect of channel doping in silicon bar, again from equation (3.3.12) it is clear that with the increase in channel doping threshold voltage of the device decreases and vice-versa. Table 4.3 shows the same behavior which is obtained from numerical simulation of the device, hence model is in good agreement with the simulation results.

Table 4.3: Threshold Voltage calculation with the change in Channel Doping Concentration in JL DGFET.

S.NO.	***Doping Concentration of Channel(N_D)($1/cm^3$)***	***Threshold Voltage (V_{th})***
1.	$1x10^{18}$	-0.413493 V
2.	$5x10^{18}$	-0.457078 V
3.	$1x10^{19}$	-0.59641 V

4.2.1 Threshold Voltage Variation with change in Drain Voltage

In equation (3.3.12) we haven't considered the effect of drain biasing on the threshold voltage of the device. Now we will write an expression, which will consider this effect also [43]. Further many new parameters will come into the picture.

$$V_{th} = V_{fb} - \frac{qN_D t_{si}^2}{8\varepsilon_{si}} - \frac{qN_D t_{si}}{2C_{ox}} - \frac{1}{2}\left[V_{ds} - \frac{\pi t_{si}}{4L_g^2}\left(\frac{\varepsilon_{si} t_{ox}}{\varepsilon_{ox}} + \frac{t_{si}}{4}\right)\left(\frac{V_{ds}}{2} + V_{ref}\right)\right] \qquad Eq\ (4.2.1.1)$$

Above equation is modified form of equation (3.3.12). This equation also takes into account the effect of drain voltage applied, channel length.

Here V_{ref} is the electrostatic potential of the source region relative to the cathode of a power supply.

Certain considerations have been made for the TCAD simulation of the device. Oxide thickness has been kept at 2nm, silicon layer thickness has been maintained at 10nm. Doping of the silicon layer has been kept uniform at $1\text{x}10^{19}$ /cm^3. Values has been calculated for each value of channel length (10 nm, 30 nm, 50 nm). V_{ref} has been maintained to be 0.548 V.

Figure 4.5 illustrates the variation of threshold voltage with that of drain voltage for different values of channel length. At shorter channel lengths, it is showing different behavior than that at longer lengths. With the increase in drain voltage, threshold voltage tends to decrease due to DIBL effect. From equation (4.2.1.1) it is clear that drain voltage is having the adverse effect on the threshold voltage of the device. With the reduction in threshold voltage, subthreshold leakages in the device increases. These leakages add up to the power consumption in the device and makes our device unsuitable for stand by power applications. The threshold voltage of our device decreases with increase in silicon thickness, oxide thickness and doping concentration of silicon bar.

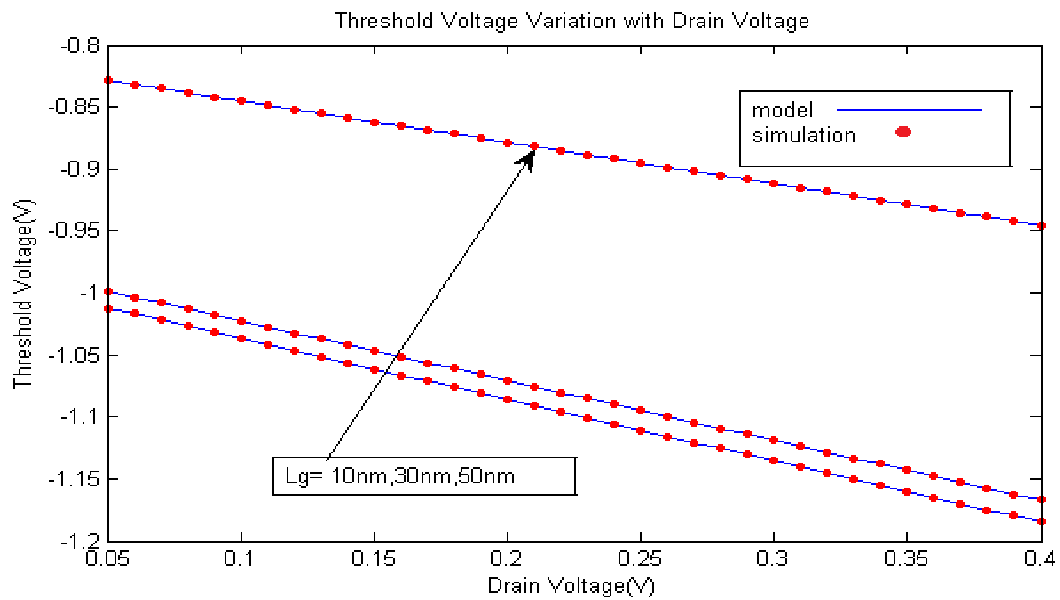

Figure 4.5: Threshold Voltage variation with the change in drain voltage for different values of channel length.

4.3 DRAIN CURRENT ANALYSIS

Drain current analysis of JL DGFET includes two type of characteristics i.e. transfer characteristics and output characteristics. Here we have done both the analysis for different conditions of parameters viz. channel length, silicon thickness, oxide thickness etc. Drain current has been obtained for different regions of operation (subthreshold, partial depletion and accumulation) and then has been combined for a complete range of gate voltage.

4.3.1 Transfer Characteristics

Figure 4.5 represents the transfer characteristics of JL DG MOSFET for different values of drain bias applied. Silicon bar doping for this analysis has been maintained to be $1x10^{19}$ /cm^3. Silicon bar thickness has been taken to be 10nm. Channel length has been fixed at 1um such that a long channel device model can be observed. Oxide thickness has been taken to be 8nm to avoid tunneling of charges from gate to bulk. All the simulations have been carried out using Silvaco ATLAS tool and model has been plotted using MATLAB. From figure 4.5 it is clear that model and simulation results are in good agreement though there are some variations but those can assumed to be negligible. All the analysis discussed here are done by considering biasing w.r.t source terminal. Channel length of the device has been taken to be 1um, silicon thickness is 10nm, and oxide thickness is 8nm. Both gate terminals are shorted to obtain the analysis.

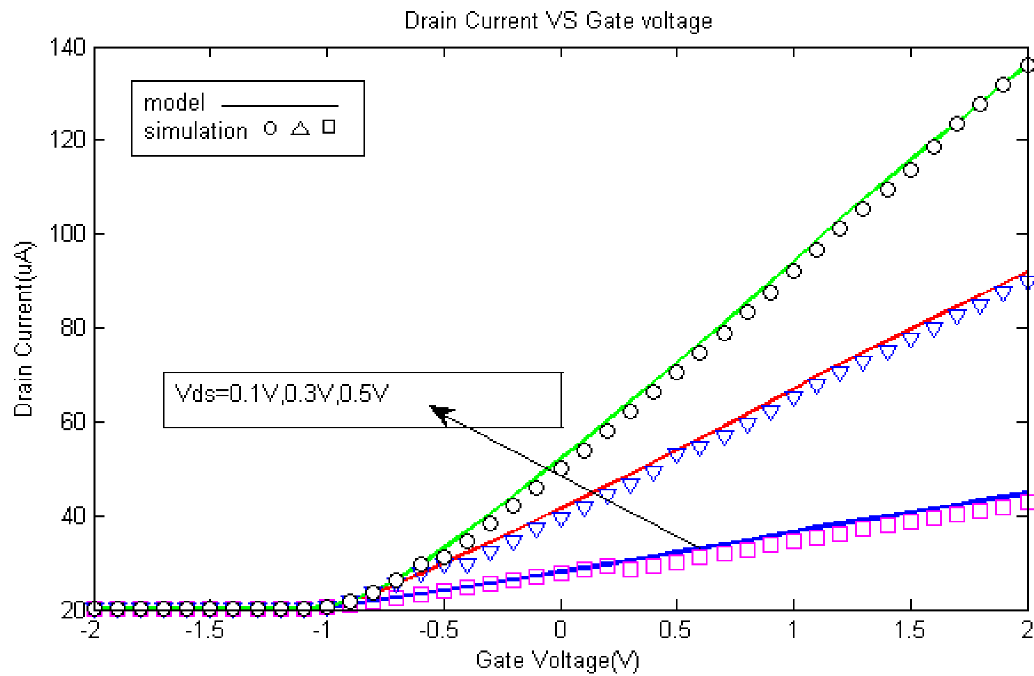

Figure 4.6: Transfer curve for JL DG MOSFET at a channel length of 1um for different Drain Voltage.

Above figure also illustrates the effect of drain voltage on the transfer characteristics of the device. As drain voltage value has been increased, transfer curve starts shifting upwards means more current will start flowing in the device. Figure 4.5 shows three different curves each for different drain bias i.e. 0.1V, 0.3V, and 0.5V. It is evident from above curve that accumulation region drain current is smoother in comparison to that of other regions because with the increase in drain voltage threshold voltage of the device shifts to some other value.

4.3.2 Output Characteristics

Figure 4.6 describes the output characteristics of JL DG MOSFET for different values of applied Gate voltages. Output characteristics of any device explain the drain current behavior of the device with that of drain voltage. All the analysis has been performed by considering biasing w.r.t. source terminal. At lower drain voltage values, drain current is increasing but at larger values, it starts saturating. This trend seems to be quite similar to that of conventional MOSFET. We have plotted output characteristics for different values of applied gate voltages. At smaller gate voltages, drain current is not that high but at larger values of gate voltage high drain current flows within the device. Applied Gate voltage helps in deciding the region of operation of the device. Drain current largely depends upon the operational region of the device. Drain current is smaller when operating in depletion or partial depletion but it is large when device starts operating in accumulation. Figure 4.6 shows the simulation results versus model results for output characteristics of the device. Both the results are in good agreement with some avoidable range of error.

These characteristics are obtained at a channel length of 1um, oxide thickness is 8nm and silicon thickness is 10nm. Analysis has been performed by applying same biasing at both the gate terminals.

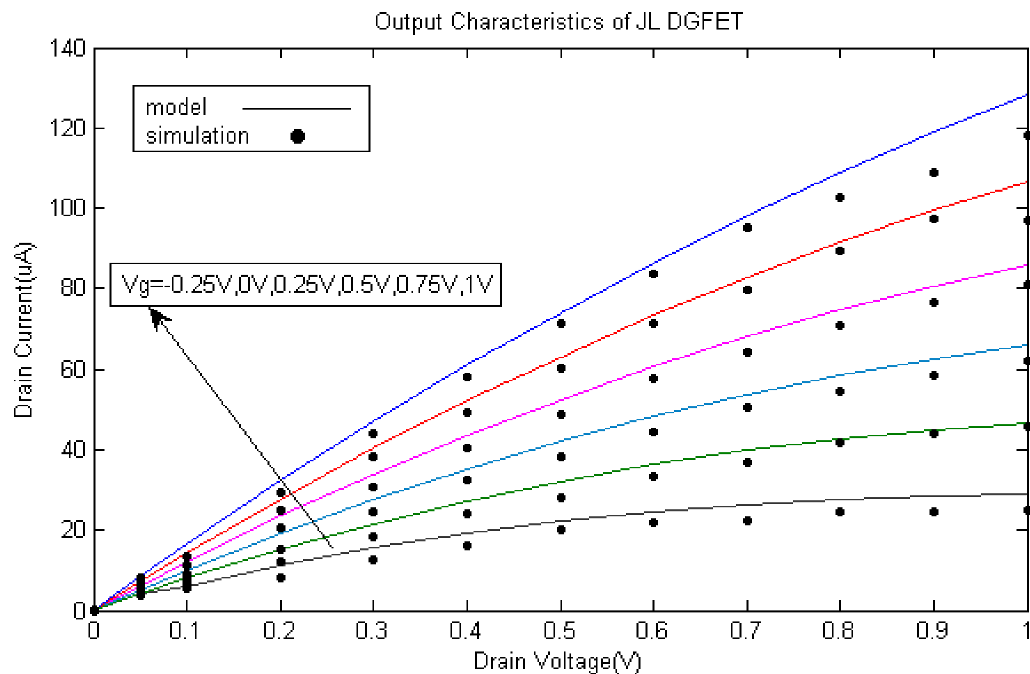

Figure 4.7: Drain Current VS Drain Voltage analysis for JL DG MOSFET.

CHAPTER 5

CONCLUSION AND FUTURE WORK

5.1 CONCLUSION

In this work, an analytical model for a symmetrical JL DGFET has been proposed. This model helps in calculating surface potential, drain current and threshold voltage of the device. Various assumptions have been made to find the characteristics under depletion, partial depletion and accumulation regions of operation. These assumptions were necessary due to the non-availability of closed form solution for Poisson equation. Developed model does not consider the effect of any short channel effect or any other phenomenon (quantum effects or tunneling). Developed model is in good agreement with that of simulation results at the long channel lengths but fails certainly at shorter channel lengths. Developed model is showing high drain current values (high ON-OFF current ratio) which are a good result for the feasibility of this device. Other than the performance advantages, this device offers simplified fabrication and cost effectiveness.

5.2 SCOPE FOR FUTURE WORK

Work presented here represents a primary work only, it could have many possible extensions. This extension of work may include following aspects.

1. Developed model does not consider the effect of any Short channel or Narrow channel effects. These effects can be included further to obtain the more accurate and practical model of the device.
2. Developed model can be included with the quantum effects such as quantum confinement.
3. Due to a high doping concentration of silicon channel, constant carrier mobility was assumed. This can further be investigated by taking into account mobility degradation for better results.
4. The threshold voltage of our device is highly dependent on the structural parameters. Threshold voltage gets shifted with these parameters. Therefore some structural optimization can be achieved to obtain better stability of threshold voltage.
5. The model developed here follows the classical drift-diffusion approach, further models can be developed using semi-classical modeling approaches.

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