Design of Fully Differential Operational Amplifier with High Gain, Large Bandwidth and Large Dynamic Range

A Thesis Submitted in partial fulfillment of the requirements for the award of degree of

Master of Technology

in

VLSI Design & CAD

Submitted by

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July- 2009

CERTIFICATE

I hereby certify that the work which is being presented in this thesis entitled, "**Design of Fully Differential Operational Amplifier with High Gain, Large Bandwidth and Large Dynamic Range,**" submitted in partial fulfillment of the requirements for the award of degree of **Master of Technology** in **VLSI Design and CAD** at **Thapar University, Patiala,** is an authentic record of my own work carried out under the supervision of **Ms. Alpana Agarwal, Assistant Professor, ECED** and refers other researcher's work which are duly listed in reference section.

The matter embodied in this thesis has not been submitted for the award of any other degree of this or any other university.

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This is to certify that the above statement made by the candidate is correct and true to best of my knowledge.

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ACKNOWLEDGEMENT

With a deep sense of gratitude, I wish to express my sincere thanks to my supervisor, **Ms. Alpana Agarwal,** for her immense help in planning and executing the work in time. The confidence and dynamism with which she guided the work requires no elaboration. Her company and assurance at the time of crisis would be remembered lifelong. Her valuable suggestions as final words during the course of work are greatly acknowledged. What I know today about the process of research, I learned from **Ms Alpana Agarwal.**

My sincere thanks are due to **Prof. A. K. CHATTERJEE,** head of the department, for providing me constant encouragement. I specially thank **Mr. Mohd Iliyas SMDP VLSI Project Faculty, ECED** for the help extended to me when I approached him and the valuable discussion that I had with him during the course of thesis.

Special thanks are due to **Mr. Sanjay Kumar and Mr. B. K. Hemant** for extending timely help in carrying out my important pieces work. The cooperation I received from other faculty members of this department is gratefully acknowledged. I will be failing in my duty if I do not mention the laboratory staff and administrative staff of this department for their timely help.

I acknowledge the Hardware & Software support provided by *Department of Information Technology (Govt. of India)* through project ***"Special Manpower Development Program for VLSI Design & Related Software (Phase - II)"***.

I also want to thank my friends and parents, who taught me the value of hard work by their own example. I would like to share this moment of happiness with my father, mother, brother and sister. They rendered me enormous support during the whole tenure of my thesis work.

Finally, I would like to thank all whose direct and indirect support helped me completing my thesis in time.

Date: **MANISH KUMAR**

(60761010)

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LIST OF ABBREVIATIONS AND SYMBOLS

Symbol	Quantity	Units
μ	Charge carrier mobility	cm^2/V_S
A_o	DC open-loop gain	dB
Av	Closed loop voltage gain	dB
B	Bandwidth	Hz
C_{gs}	Gate-source capacitance	f
CMRR	Common-Mode Rejection Ratio	dB
C_L	Load capacitor	f
C_{OX}	Normalized oxide capacitance	f/m^2
DR	Dynamic Range	dB
DM	Differential mode signal	
F	Frequency	Hz
GBW	Unity gain bandwidth	Hz
g_m	Trans-conductance	Ω^{-1}
$g_{m,n}$	Trans-conductance of n-transistor	Ω^{-1}
$g_{m,p}$	Trans-conductance of p-transistor	Ω^{-1}
$g_{m,T}$	Total trans-conductance	Ω^{-1}
ICMR	Input Common Mode Range	dB
I_d	Drains current	A
K	Boltzmann's constant	J/K
K_p	PMOS process trans-conductance parameter	A/V^2
K_n	NMOS process trans-conductance parameter	A/V^2
L	Channel length	μm
W	Channel width	μm
LVS	Layout Vs Schematic	
PSRR	Power Supply Rejection Ratio	dB
$P_{peak\text{-}signal}$	Peak to peak signal power	V^2/Hz

P_{noise}	Output noise power	V^2
SNR	Signal-to-Noise Ratio	dB
SR	Slew rate	V/μs
UGB	Unity gain bandwidth	Hz
V_{CM}	Common-mode input voltage	V
V_{DD}	Positive supply	V
$V_{o,swing}$	Output voltage swing	V
V_{DS}	Drain-source voltage	V
$V_{d,sat}$	Saturation voltage	V
V_{GS}	Gate-source voltage	V
V_{on}	Output noise voltage	V
GND	Ground	
V_{th}	Thermal voltage	V
V_{tn}	Threshold voltage	V
V_{tn0}	Threshold voltage at V_{sb}=0V	V
S-S	Slow-Slow	
S-F	Slow-Fast	
F-S	Fast-Slow	
F-F	Fast-Fast	
Z	Impedance	Ω

ABSTRACT

This thesis work presents the full custom design of a two-stage fully differential CMOS amplifier with outstanding characteristics of high unity-gain bandwidth and large dynamic range at output. The circuit has been designed. The simulation results in TSMC 0.35μm CMOS process from a 3.3V voltage-supply demonstrate that the designed operational amplifier has satisfied state-of-the-art design specifications with a dedicated optimization technique. This fully differential op-amp can be used in a pipeline ADC stage. The amplifier consists of four parts, a telescopic differential amplifier that provides most of the open loop gain, second stage common source amplifier that provide the output swing, a common mode feedback circuit to maintain the constant output voltage and a compensation circuitry for achieving desired phase margin with high unity gain bandwidth.

The amplifier exhibit large output swing of 3.1 V peak-to-peak, a fast settling time 2.8 ns to the accuracy of 1%. While the open loop amplifier have the considerable gain as high as 86.02 dB, the differential AC loop unity gain bandwidth reaches 270 MHz and the dynamic range at the output gets 85.15dB with phase margin of 50°. The present work also demonstrate how to efficiently design and further optimize the circuit topology and parameters in order to meet some strict specifications given in advance for a specific engineering project.

CHAPTER 1

INTRODUCTION

This chapter discusses the background and motivation behind the fully differential operational amplifier and ideal requirements of fully differential operational amplifier for input stage. It also discusses various applications of fully differential operational amplifier.

1.1 Background

Constraints imposed by advanced IC process technologies, modern electronic system requirements, and the economics of circuit integration have created new challenges in analog circuit design. With the advancement of CMOS process technologies and the increasing popularity of battery-powered mobile electronic systems comes the demand for lower-voltage analog circuit designs. In addition, the drive to reduce system costs is forcing the integration of both analog and digital circuitry onto a single die. Both of these changes have a detrimental impact on analog circuit performance. With a reduction in power supply voltage comes a decrease in both the peak SNR and the dynamic range of an analog circuit. Integrating analog circuitry and noisy digital circuitry on the same die further degrades analog performance due to noise injection through a common power supply and/or power distribution network, the die substrate, and/or capacitive coupling between conductors.

Many analog design techniques and methodologies have been devised to enable high performance analog signal processing in today's environment. Fully differential analog signal processing is one technique that has become widespread because it reduces the problems associated with both reduced signal swings and noise coupling. Using a differential design technique effectively doubles the maximum signal swing in the circuit. Also, all external noise sources that influence both signal paths of a balanced differential system in the same way, to a first order approximation, will be rejected. This is due to the fact that, in a differential system, the signal of interest is the difference between the signals in the two signal paths. Thus any noise common to both signal paths will be subtracted away. For the same reason, the total harmonic distortion of the circuit due to non-linear elements can be reduced. Each distortion component at a frequency that is an

even harmonics of the fundamental signal frequency will be subtracted away from the differential signal because it is a common in both signal paths [1].

Operational amplifiers are the backbone for many analog circuit designs. It is a fundamental building block for many circuit designs that utilize its high gain, high input impedance, low output impedance, high bandwidth and fast settling time. Operational amplifier (Op-Amp) is one of the basic and important circuits which have a wide application in several analog circuits such as switched-capacitor filters, algorithmic, pipelined and sigma-delta A/D converters, sample-and hold amplifiers etc. The speed and accuracy of these circuits depend on the bandwidth and DC gain of the Op-amp. Larger the bandwidth and gain, higher the speed and accuracy of the amplifier[2]. Operational amplifiers are a critical element in analog sampled-data circuits, such as SC filters, modulators. Higher and higher clock frequency requirement for these circuits translates directly to higher frequency requirement for the Op-amp. A high gain bandwidth (GBW) is essential for accurate dynamic charge transfer in an switch-capacitor (SC) circuit in a short sampling period. Applications of the high speed opamp range from video amplifiers to sampling circuits. Many fiber optic applications also require analog drivers and receivers operating in the megahertz range wide-band op amps are necessary.

In recent years, CMOS analog-digital converters (ADC) are expected to achieve a high gain and unity gain frequency, and a fast settling time. However, the problem is that high speed and high open-loop gain are two contradictory demands [3].

An integrated, fully-differential amplifier is very similar in architecture to a standard, voltage feedback operational amplifier. Fully differential amplifiers have differential outputs, while a standard operational amplifier's output is single-ended. There is typically one feedback path from the output to the negative input in a standard operational amplifier. A fully-differential amplifier has multiple feedback paths.

1.2 Need of Fully Differential Amplifier

1 *Increase noise immunity,* invariably, when signals are routed from one place to another, noise is coupled into the wiring. In a differential system, keeping the transport wires as close as possible to one another makes the noise coupled into the conductors appear as a common-mode voltage. Noise that is common to the power supplies also appears as a common-mode voltage. Since the differential amplifier rejects common-mode voltages, the system is more immune to external noise.

2. *Increased output voltage swing,* due to the change in phase between the differential outputs, the output voltage swing increases by a factor of 2 over a single-ended output with the same voltage swing. This makes them ideal for low voltage applications.
3. *Reduced even order harmonics*, expanding the transfer functions of circuits into a power series is a typical way to quantify the distortion products.

   Taking generic expansion of outputs and assuming matched amplifiers, we get

$$V_{out+} = K_1 V_{in} + K_2 V_{in}^2 + K_3 V_{in}^3 + \ldots\ldots\ldots\ldots \text{ and} \quad (1.1)$$

$$V_{out-} = K_1(-V_{in}) + K_2(-V)_{in}^2 + K_3(-V)_{in}^3 + \ldots. \quad (1.2)$$

   taking the differential output

$$V_{od} = 2K_1 V_{in} + 2K_3(-V)_{in}^3 + \ldots\ldots \text{ where } K_1, K_2 \ldots \text{ are constants.} \quad (1.3)$$

   The quadratic terms gives rise to second-order harmonic distortion, the cubic terms gives rise to third-order harmonic distortion, and so on. In a fully-differential amplifier, the odd-order terms retain their polarity, while the even-order terms are always positive. When the differential is taken, the even order terms cancel.
4. *Fully differential amplifier had large output dynamic range*, due to its noise immune property.
5. *The differential pair provides a built-in level shif*t that allows for all-NMOS devices in the signal path. This would allow for a rough 2X increase in speed for the same power, or a decrease in power for the same speed.
6. *Fully differential telescopic op-amp consume much less power* than their counter folded cascode fully differential op-amp.

1.3 Applications of Fully Differential Operational Amplifier

- Digitally programmable voltage gain amplifier.
- Fully differential amplifier can be used as pipeline ADC stage.
- Telescopic fully differential op-amp is employed as main stage of CMOS ADC.
- Switched- capacitor filter.
- RF modulator and audio systems.
- Fully differential op-amp use in Delta Sigma modulator.

1.4 MOTIVATION

The design of high-accuracy analogue circuits is becoming a difficult task with the scaling down of supply voltages and transistor channel lengths of the current mixed-signal integrated circuits. Most of this kind of circuits requires the use of the highest performance active cell: the operational amplifier (op amp). Designers are continuously working toward trades off solutions between gain, input/output swings, speed, power dissipation and noise. Basically, the principal topologies of op amps are based on the telescopic cascode, folded cascode, two-stage or gain boosting schemes. Op-amp with active cascode circuits achieve to increase the open-loop gain without adding cascade stage and cascode devices. In this way, high speed circuits with low headroom can be obtained.

1.5 Organisation of Thesis

Introduction to fully differential operational amplifier its benefits over single ended opamp and applications of fully differential opamps.

Chapter two starts with basic parameters of opamp. Discussing the various property opamp and design procedure of two stage opamp. Comparative study of various topologies of fully differential amplifier has been given. The idea of common mode feedback technique has been present. How to use various compensation techniques for high performance and high stable op-amp are also discuss.

Chapter three starts with the choice of topology for input stage of the fully differential op-amp. Design of fully differential telescopic op-amp for targets specifications with using common mode feedback and compensation techniques.

Chapter four presents the simulations results for schematic of fully differential amplifier. It also discusses the results of post layout, process corner and Monte Carlo simulations.

Chapter five concludes the present work and some scope of further improvements, have been suggested.

CHAPTER 2

LITERATURE SURVEY

This chapter examines a number of various input stage topologies for the fully differential op-amp and explains how the input stage design is shaped by the constraints from specifications. The related constraints are common-mode rejection ratio, DC open loop gain, input offset voltage, settling time, slew rate, dynamic range and unity gain bandwidth are the discussed in this context.

Input Common Mode Range:

One of the primary specifications of the op amp in design is to have the input common mode range that includes ground for the single supply operation as well as mid supply voltage for dual-supply operation.

DC Open Loop Gain

The ultimate settling accuracy is limited by the finite opamp DC gain. The exact settling error is depends not only on the gain but also on the feedback factor in the circuit utilizing the op-amp. Typically, the DC gain requirement is from 60 dB up to 100 dB. In some circuits, such as a front-end S/H circuit, insufficient opamp DC gain results only in a gain error which is usually tolerable. The DC gain, however, has to be constant over the op-amp output voltage range in order to avoid harmonic distortion [3].

Settling Time

It takes a finite time for a signal to propagate through the internal circuitry of an op amp. Therefore, it takes a certain period of time for the output to react to a step change in the input.

The settling time consists of 30% of slewing time and 70% of linear settling time. The settling time constant τ is given by [3]:

$$\tau = \frac{C_L}{g_m} \tag{2.1}$$

The number of settling time constants to obtain the required accuracy is given by Williams *et al* [3]:

$$n_\tau = \frac{T_s}{2\tau} \tag{2.2}$$

If the system has no slew rate limiting then the number of time constants can be less than five, *i.e* $\tau < 5$[3].

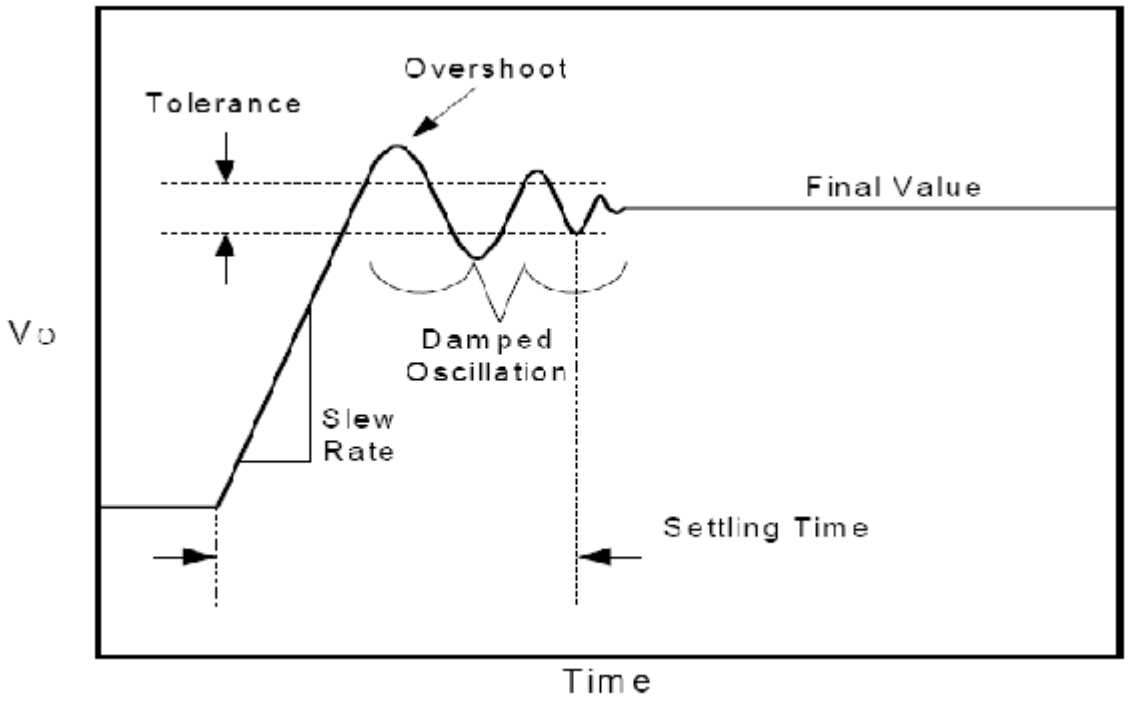

Figure 2.1: Settling time

Slew Rate

The Slew rate (SR) is the current available to drive the capacitance present at the output of the amplifier**.** Slew rate is defined as in [4]

$$SR = \frac{I_{bais}}{C_L} \tag{2.3}$$

Where, I_{bais} is the bias current and C_L is the output load capacitance. SR can also be expressed as:

$$SR = \frac{V_{ov}}{2} UGB \tag{2.4}$$

Where, *Vov* is the overdrive voltage and UGB is the unity gain bandwidth. If the unity gain bandwidth is kept constant, the slew rate is improved by increasing the overdrive voltage. SR can be further improved by using larger lengths or decreasing the transconductance by keeping the current and gain bandwidth constant. It is recommended that the SR should be five times the sampling frequency of the system [3].

Unity Gain Bandwidth

Unity gain bandwidth (UGB) and gain bandwidth product (GBW) are similar and specifies as the frequency at which differential DC gain of opamp is unity. GBW specifies the gain-bandwidth product of the op amp in an open loop configuration and the output loaded:

GBW= A_D*f, where A_D is differential DC gain and f is unity gain frequency (2.5)

Dynamic Range

Dynamic range is defined as:

$$DR = 10\log\left(\frac{P_{peaksignal}}{P_{noise}}\right) \quad (2.6)$$

The peak signal power is the power of the maximum differential sinusoidal signal that does not overload the amplifier. The noise power is the total noise at the amplifier output integrated from 1Hz to infinity [5].

2.1 Fundamentals of Ideal Fully Differential Op-Amp

The differential op-amp has two input signals, V_{i1} and V_{i2}, and two output signals, V_{O1} and V_{O2} as shown in figure 2.2. However, the input and output signals of interest in this system is the difference between the two input terminals and the two output terminals, respectively. The difference between these signals is called the differential mode input and differential-mode output, or V_{iDM} and V_{ODM}. If this is a balanced system with balanced inputs, the input and output signals can be referenced to a common mode, or average voltage, V_{ICM} and V_{OCM}, respectively as shown in figure 2.3. If the common-mode voltage is set to analog ground, as is usually the case, then the following relation holds: $V_1 = -V_2$

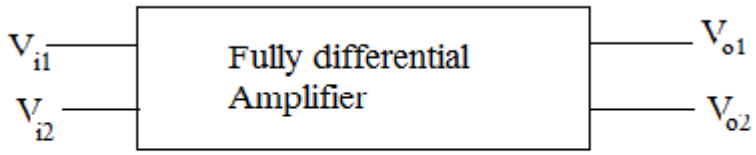

Figure 2.2: Input/ Output of fully differential op-amp

There are 4 gain parameters of interest. Gain A_{DD} relates the differential output signal, Vo_{DM}, and the differential input signal, Vi_{DM}.

$$V_{i1} = Vicm + \frac{1}{2}Vidm \qquad V_{i2} = Vicm - \frac{1}{2}Vidm \tag{2.7}$$

$$V_{o1} = Vocm + \frac{1}{2}Vodm \qquad V_{o2} = Vocm - \frac{1}{2}Vodm \tag{2.8}$$

$$Vidm = V_{i1} - V_{i2} \qquad Vicm = \frac{1}{2}[V_{i1} - V_{i2}] \tag{2.9}$$

$$Vodm = V_{O1} - V_{O2} \qquad Vocm = \frac{1}{2}[V_{O1} - V_{O2}] \tag{2.10}$$

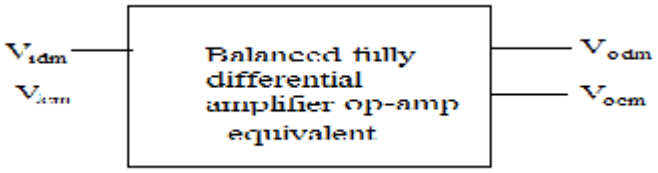

Figure 2.3 Input/ Output of balanced fully differential op-amp

This is the most important gain parameter for a differential op-amp and ideally it approaches infinity. This high differential gain parameter is what creates a differential-mode virtual short between the Vi1 and Vi2 terminals when the op-amp is used in a negative feedback configuration. Gain A_{CD} relates the differential output signal, V_{ODM}, and the common-mode input signal, V_{iCM}. Ideally, V_{ODM} is not related to V_{iCM}, so A_{CM} approaches 0. The ratio of A_{DD} to A_{CM} is called the common-mode rejection ratio, or CMRR of the op-amp. The higher the CMRR is better, and ideally it approaches infinity. Gain A_{DC} relates V_{OCM} and V_{iDM}. Ideally, the output common mode signal has no relation to the input differential signal, so A_{DC} approaches 0. Gain A_{CC} relates V_{OCM} and V_{iCM}. There should not be a relation between the common-mode output and common-mode input, so ideally A_{CC} approaches zero.

So input/output signal relationship for fully differential op-amp is [6]:

$$\begin{bmatrix} V_{ODM} \\ V_{OCM} \end{bmatrix} = \begin{bmatrix} A_{DD} & A_{CD} \\ A_{DC} & A_{CC} \end{bmatrix} \times \begin{bmatrix} V_{IDM} \\ V_{iCM} \end{bmatrix} \tag{2.11}$$

2.2 Need of Differential Output Op-Amp

This section discussed about the need fully differential opamp. The basic necessity of fully differential operational amplifier are followings:

- Increased signal swing as shown in figure 2.4.
- Cancellation of common mode signals including clock feed through as shown in figure 2.6.
- Cancellation of even-order harmonics
- Common mode output voltage stabilisation. If the common mode gain not small, it may cause the common mode output voltage to be poorly defined.

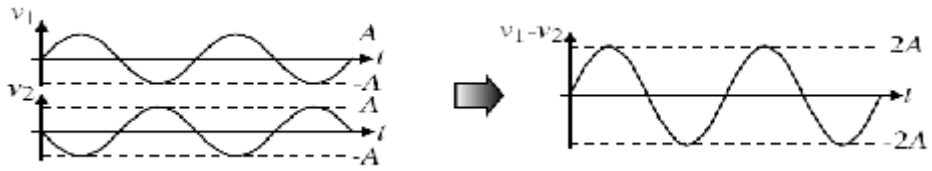

Figure 2.4 Difference Signal and differential output[7]

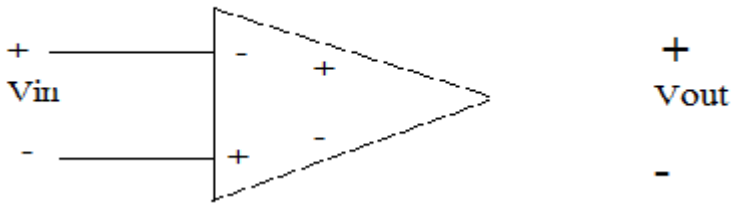

Figure 2.5 Symbol of fully differential op-amp

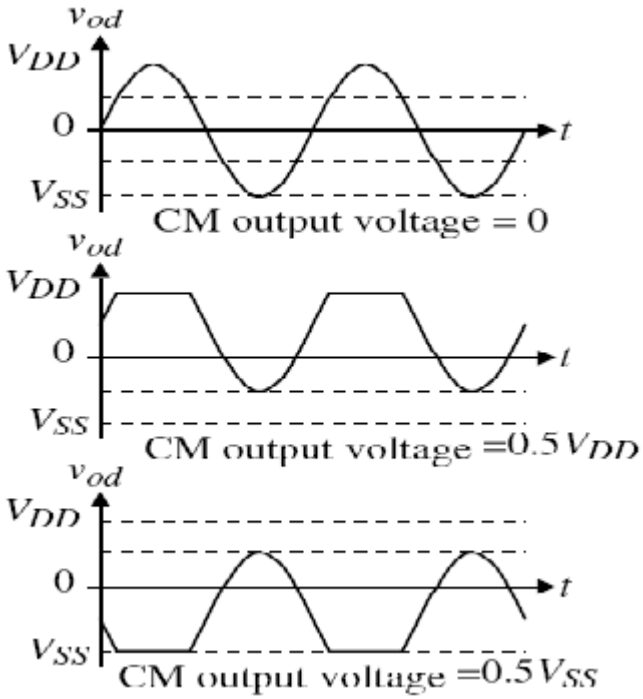

Figure 2.6 Illustration of output common mode [7]

2.3 Design Procedure of Two Stage Opamp

This section presents a basic two-stage CMOS opamp design procedure that provides the circuit designer with a means to strike a balance between two important characteristics in electronic circuit design, namely noise performance and power consumption.

CMOS opamps are ubiquitous integral parts in various analog and mixed-signal circuits and systems. The two-stage CMOS opamp is widely used because of its simple structure and robustness. In designing an opamp, numerous electrical characteristics, *e.g.*, gain-bandwidth, slew rate, common-mode range, output swing, offset, all have to be taken into consideration. Furthermore, since opamps are designed to be operated with negative-feedback connection, frequency compensation is necessary for closed-loop stability. Unfortunately, in order to achieve the required degree of stability, generally indicated by phase margin, other performance parameters are usually compromised. As a result, designing an opamp that meets all specifications needs a good compensation strategy and design methodology.

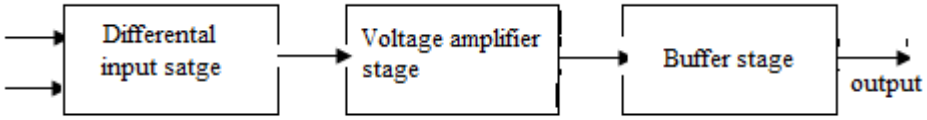

Figure 2.7 Block diagram of basic op-amp [1]

A classic op-amp architecture is made up of three stages as shown in figure 2.7, even though it is often referred to as a ”two-stage” op-amp, ignoring the buffer stage. The first stage usually consists of a high-gain, differential amplifier. This stage has the most dominant pole of the system. A common source amplifier usually meets the specifications of the second stage, having a moderate gain. The third stage is most commonly implemented as a unity gain source follower with a high frequency and negligible pole [2].

A typical CMOS differential amplifier stage is given in figure 2.8. Differential amplifiers are often desired as the first stage in an op-amp due to their differential input to single ended output conversion and their high gain.

The high gain requirement indicates that either a very high-gain single stage or two modest gain stages are needed. The main disadvantage of the single stage implementation is the low output range [7].

One of the biggest benefits of the two-stage approach is that the net open loop gain can be achieved with two distinct stages, thereby eliminating much of the complexity involved in

designing a single gain stage and leaving the distribution of gain in each stage up to the designer's discretion. The first-stage does not have to drive the large capacitive load at the output of the second stage. The most logical approach would be to have a large gain in the first stage and a small gain and high swing in the second; the rationale being that low second stage gain would not greatly amply first stage noise and high swing would give better dynamic range [8].

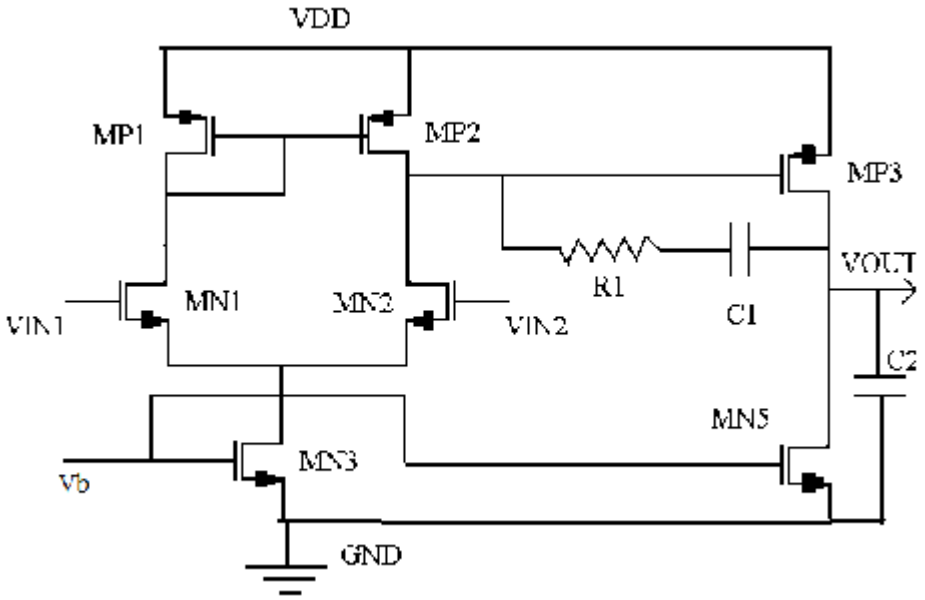

Figure 2.8 CMOS differential input stage amplifier [5]

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There are several benefits of a two-stage topology compared to that of a single stage amplifier. First and foremost is that the net amplifier gain required can be realized in two stages, thus de-coupling gain and headroom considerations. Typically, the majority of the gain is realized in the first stage. Secondly, the second stage or output stage can be designed to simultaneously source large currents and have a large output swing since its gain requirements are significantly reduced by the two-stage topology. Also, the noise in a two-stage amplifier is comparable to that of a single stage amplifier. This is because very little input referred noise is contributed by the second stage due to the typically large gain in the first stage. Consequently, the total output noise is primarily due to only the first stage of the amplifier.

The major drawback of a two-stage design is that of speed. This is due to the additional non-dominant pole added by cascading the two stages. However, a compensation capacitor can be used to offset this issue. Thus the two-stage design with compensation capacitor was chosen over the single stage. However, the two-stage design is more

flexible than that of a single stage design. This suggests that the slowness of the two-stage design can be compensated for without having to trade off significantly in terms of gain, and dynamic range. Upon comparison of the single stage to two-stage topologies, we found that the advantages of the two -stage topology outweighed its disadvantages. Consequently, we opted for a two-stage design over single stage design.

The two-stage operational transconductance amplifier (OTA) in figure 2.9 is a widely used analog building block. Indeed, it identifies a very simple and robust topology which provides good values for most of its electrical parameters such as dc gain, output swing, linearity, CMRR, *etc*. Although the term OTA was originally conceived for operational transconductance amplifiers with linear transconductance.

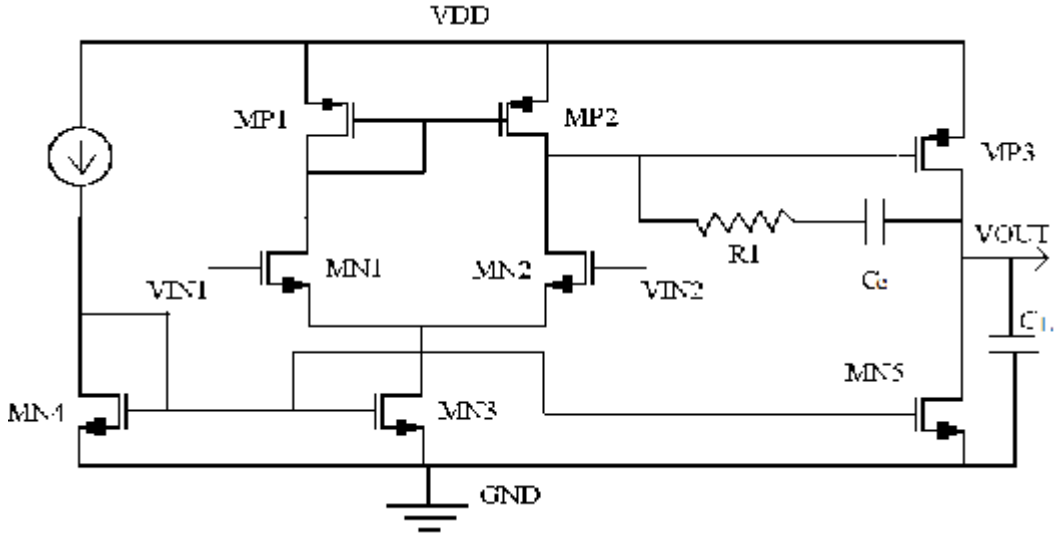

Figure 2.9 Schematic of two stage OTA

The design procedure is based on the following main parameters: noise, phase margin *(*M_Φ*)*, gain-bandwidth product *(f_{GBW})*, load capacitance *(C_L)*, slew rate (*SR*), input common mode range (*CMR*), output swing (*OS*), and input offset voltage (due to systematic errors).

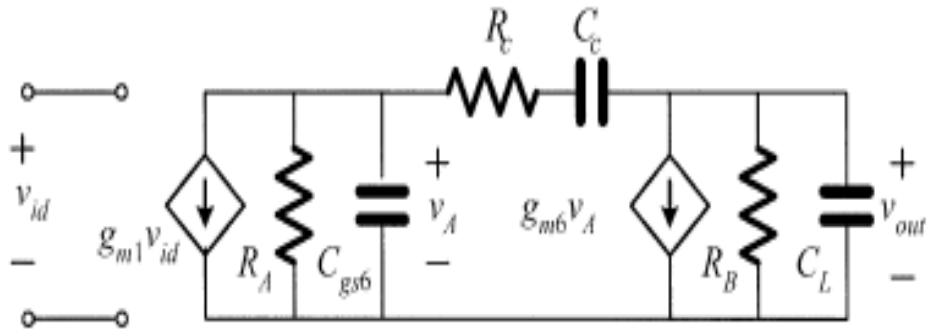

Figure 2.10 Small signal equivalent of two stage OTA [7]

The equations for determining the various opamp characteristics can be shown as follows:

(a) Gain and Bandwidth

According to the equivalent circuit shown in Figure 2.10 under typical conditions $g_{m6}R_B >> C_{gs6}/C_C$, $g_{m6}R_A >> C_L/C_C$ and $R_C << R_A, R_B$.

The dc gain of opamp is given by

$$A_{v0}=g_{m1}g_{m6}R_AR_B \tag{2.12}$$

The op-amp's dominant pole frequency and unity-gain bandwidth, also commonly known as gain-bandwidth, can be found to be

$$\omega_{P1}=\frac{1}{g_{m6}R_AR_BC_C} \quad \text{and} \quad \omega_U=\frac{g_{m1}}{C_C}=A_{V0}=g_{m1}\omega_{P1} \tag{2.13}$$

Where ω_{P1} and ω_U are dominant pole and unity gain bandwidth respectively. The transfer function of two stage OTA is given by [7]:

$$\frac{V_{OUT}}{V_{ID}}=A_{V0}\frac{1-sC_C\left(\frac{1}{g_{m6}}-R_C\right)}{1+g_{m6}R_AR_BC_Cs+R_AR_B\left(C_{g6}C_L+C_{g6}C_C+C_LC_C\right)s^2+R_AR_BR_CC_{g6}C_LC_Cs^3} \tag{2.14}$$

(b) Output Swing

By defining V_{HR}^{OUT} as the voltage head room voltage at output, *i.e*

$V_{HR}^{OUT+} = V_{DD} - V_{out}(max)$ and $V_{HR}^{OUT-} = V_{out}(min) - V_{SS}$

(c) Common Mode range

If we define V_{CM} as the opamp input common mode range i.e

$V_{CM}^{+} = V_{DD} - V_{CM}(max)$ and $V_{CM}^{-} = V_{CM}(min) - V_{SS}$

According to Figure 2.8, it can be shown that

$V_{CM}^{+} = V_{eff3} - V_{tn}$ and $V_{CM}^{-} = V_{eff5} + V_{eff1,2} + V_{tn}$

(d) Internal Slew Rate

The slew rate associated with C_C is found to be

$$SR=\frac{I_{D5}}{C_C} \tag{2.15}$$

The slew rate associated with C_L is found to be

$$SR=\frac{I_{D7}-I_{D5}}{C_L} \tag{2.16}$$

Combining both (2.15) and (2.16) we obtain

$$I_{D7}=SR(C_C+C_L) \tag{2.17}$$

2.4 Topologies for Input Stage Fully Differential Amplifier

This section discusses various topologies for the input differential amplifier for fully differential amplifier.

There are many different topologies that can be considered for this design. Four of the most relevant methods are compared in Table 2.1 [2, 9].

Table 2.1 Performance of four different topologies [2]

Topology	Gain	Output swing	Speed	Power Consumption
Telescopic Cascode	Medium	Medium	Highest	Lowest
Folded Cascode	Medium	Medium	High	Medium
Two Stage	High	Highest	Low	Medium
Regulated Cascode	High	Medium	Medium	High

From the above table it is clearly visible that telescopic and folded cascode opamp are best suited for high speed application although the gain provided by them is medium. As in this thesis work high speed opamp is being desired so folded cascade and telescopic opamp are studied in detail.

2.4.1 Folded Cascode Fully Differential [10-13]

A fully-differential folded-cascode op-amp is shown in figure. 2.11. Four current sources are needed to drive the amplifier. The current sources are implemented using the cascode technique. A folded topology enables the amplifier to have a high output voltage swing at the cost of having a common-mode level sensitive to device mismatches. The folded cascode op amp has a push pull output stage which can sink or source current from the load. The exact match of the currents in the differential amplifier is not demanded by the folded cascode op amp since extra current can flow in or out of the current mirrors. While the bias current of the conventional cascode delivers the current to both the input devices and the cascode devices since they are stacked together, the bias current I_{SS} of the folded cascode supplies only the input devices. Additional bias currents are required to add necessary bias current. In general, the folded cascode connection dissipates more power. The gain of a folded cascode op amp is normally lower than that of a corresponding conventional cascode op amp due to the lower impedance of the devices in parallel. A

folded cascode op amp has a pole at the folding connection which is lower compared to that node pole of the conventional cascode op-amp.

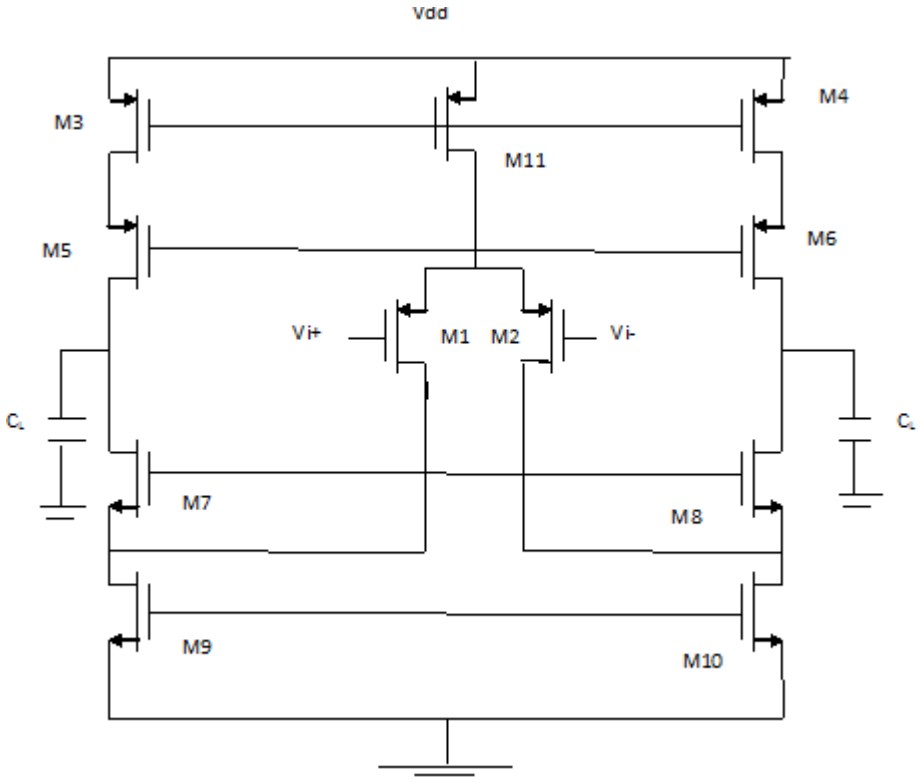

Figure 2.11 Fully differential folded cascode amplifier

This is due to the larger parasitic capacitance of extra and possibly wider devices in the folded structure. Sometimes this low folding pole can self-compensate a folded cascode if the phase margin is good enough.

By applying good approximations, the voltage gain of the Op-Amp is given by:

$$A_V = G_m R_O \tag{2.18}$$

where $R_O = \left(g_{m7} r_{O7} \left(r_{O1} \parallel r_{O9}\right)\right) \| \left(g_{m5} r_{O5} r_{O3}\right)$

There are two dominant poles and a zero are considered in the studying of the frequency response:

1. First dominant pole is given by the high output resistance(R_O) occurs at output node [11]:

$$\omega_{P1} = -1 \Big/ R_O C_O \tag{2.19}$$

$$C_O = C_L + C_{D5} + C_{D7} \tag{2.20}$$

2. The second pole which have frequency much greater than dominant pole frequency and is given by

$$w_{P2} = -1/R_{CASC}C_{CASC} \tag{2.21}$$

$$C_{CASC} = C_{D1} + C_{S7} + C_{D9} \tag{2.22}$$

$$R_{CASC} \approx \left(1/g_{m7}\right) \| r_{O1} \| r_{O7} \| r_{O9} \tag{2.23}$$

3. Due to the existing a second signal path through C_{gd1}, a right half plane zero is introduced in transfer function is calculated as

$$\omega_{Z1} = g_{m1}/C_{gd1} \tag{2.24}$$

There is pole at folding point *i.e* the source of M7 & M8 is quite closer to the origin that associated with the sources of cascode devices.

The maximum output voltage swing of the folded cascode with proper choice of bias voltages, the lower end of the swing is given by V_{OD3}+V_{OD5} and the upper end by $V_{DD} - \left(|V_{OD7}| + |V_{OD9}|\right)$. Thus, the peak-to-peak swing on each side is equal to $V_{DD} - (V_{OD3} + V_{OD5} + |V_{OD7}| + |V_{OD9}|)$.

Thus, voltage swing of folded casode amplifier is slightly higher than that of telescopic configuration. This advantage comes at the cost of higher power dissipation, lower voltage gain, lower pole frequencies and higher noise [12, 14].

2.4.2. Telescopic OP-AMP

Cascode configurations may be used to increase the voltage gain of CMOS transistor amplifier stages. This structure has been called a 'telescopic-cascode' opamp because the cascodes are connected between the power supplies in series with the transistors in the differential pair, resulting in a structure in which the transistors in each branch are connected along a straight line. The main potential advantage of telescopic cascode op-amps is that they can be designed so that the signal variations are entirely handled by the fastest-polarity transistors in a given process [15, 16]. In the first stage, we were simply looking for a configuration that allowed for high gain, low noise and minimal current since output swing is less critical. The folded cascode and the telescopic configurations were considered since we required at least one cascoded stage for a gain on the order of $\left(g_m r_o\right)^2$. A high swing configuration still needs to be used to insure that all the devices in this stage are in saturation. In comparing the two topologies, the folded cascode has more

current legs and more devices in the signal path. This leads to larger static current and more noise contributors [17]. On the other hand, the telescopic configuration has half as many current legs and fewer devices.

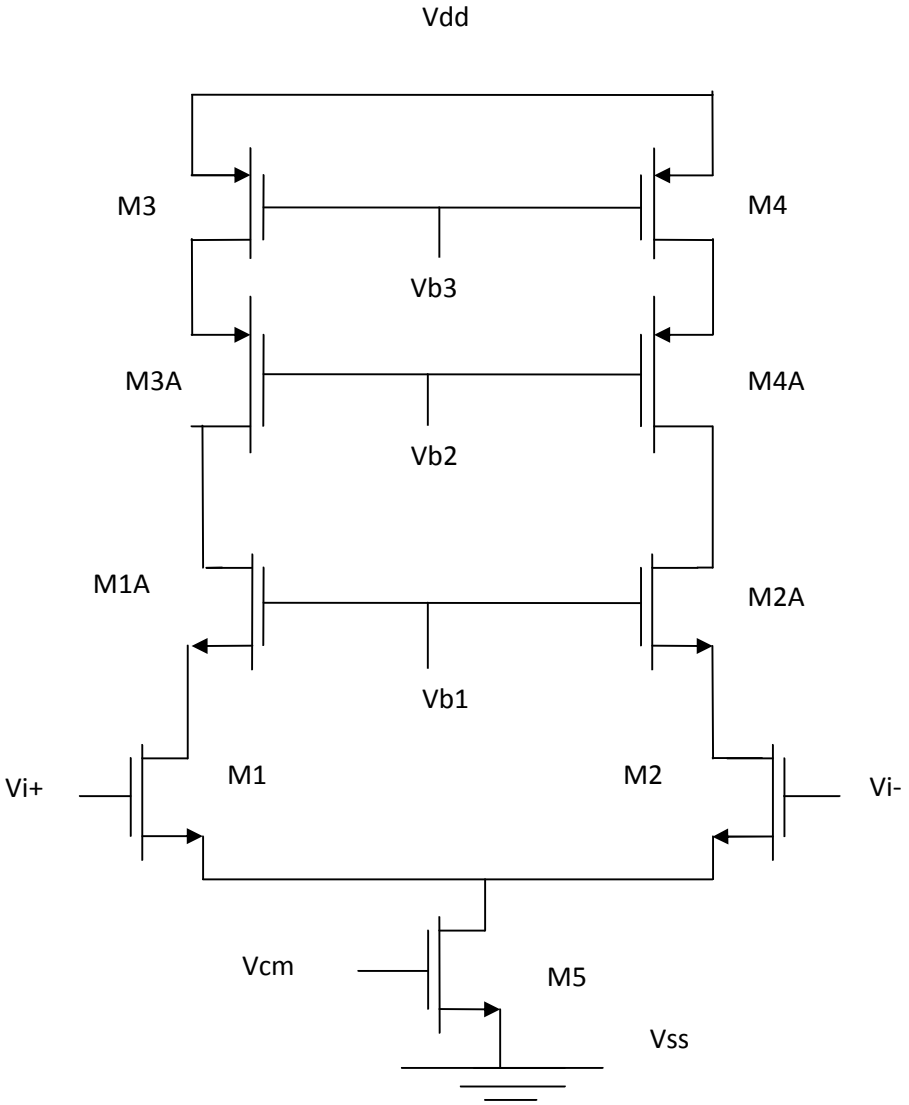

Figure 2.12 Fully Differential Telescopic Single Stage op-amp

A telescopic cascode op-amp, as shown in figure 2.12, typically has higher frequency capability and consumes less power than other topologies. Its high-frequency response stems from the fact that its second pole corresponding to the source of the n-channel cascode devices is determined by the transconductance of n-channel devices as opposed to p- channel devices, as in the case of a folded cascode. Also the parasitic capacitance at this node arises from only two transistors instead of three, as in the latter. The single stage architecture naturally suggests low power consumption.

The disadvantage of a telescopic op-amp is severely limited output swing. It is smaller than that of the folded cascode because the tail transistor directly cuts into the output swing from both sides of the output. In the telescopic op-amp shown in figure 2.12, all transistors are biased in the saturation region. Transistors M1–M2, M7–M8, and the tail current source M9 must have at least V_{DSAT} to offer good common-mode rejection, frequency response, and gain [18].

The maximum output voltage depends on the common-mode input. However, this limitation as well as the limitation on the common-mode input range can be overcome in switched-capacitor circuits. Such circuits allow the op-amp common-mode input voltage to be set to a level that is independent of all other common-mode voltages on the same integrated circuit [19].

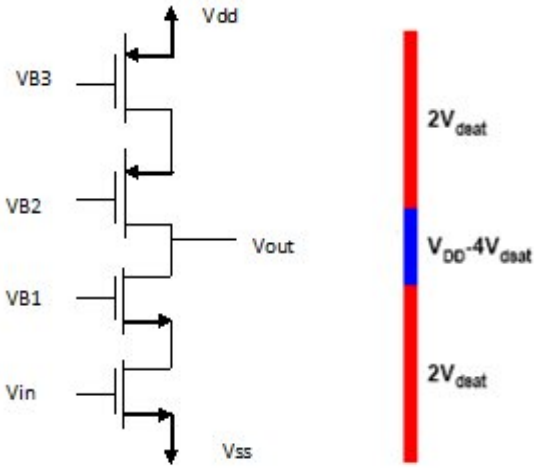

Figure 2.13 Voltage swing of cascode amplifier [20]

The voltage swing of cascode amplifier is being shown in figure 2.13.

This property holds because the only coupling of signals to the op-amp inputs is through capacitors, which conduct zero dc current even with a nonzero dc voltage drop.

$$V_{OmaX} = V_{DD} - 2|V_{OV}| \tag{2.25}$$

This equation (2.25) shows that the maximum output voltage of a telescopic op amp that consists of the first stage with optimum common-mode input biasing is three overdrives

less than the positive supply. This result stems from the observation that three transistors are connected between V_{DD} and the output.

$$V_{OMIN} = V_{SS} + 3V_{OV} \tag{2.26}$$

To determine the minimum required supply voltage difference, we will subtract (2.25)

from (2.26), this gives

$$V_{O1(MAX)} - V_{O1(MIN)} = V_{DD} - (V_{SS}) - 5|V_{OV}| \tag{2.27}$$

Assuming that the magnitudes of all the overdrives are all equals. Rearranging this equation gives

$$V_{DD} - V_{SS} = V_{O1(MAX)} - (V_{O1(MIN)}) + 5|V_{OV}| \tag{2.28}$$

This equation shows that the minimum difference between the supply voltages in a telescopic cascode op amp must be at least equal to the peak-to-peak output signal swing plus five overdrive voltages to operate all transistors in the active region. For example, with a peak-to-peak output swing of 1 V and V_{OV} = 100 mV for each transistor, the minimum difference between the supply voltages is 1.5 V. To avoid this problem, transistors in practical op amps are usually biased so that the magnitude of the drain-source voltage of each transistor is more than the corresponding overdrive by a margin of typically at least one hundred milli volts. The margin allowed for each transistor directly adds to the minimum required supply voltage difference.

The extra three overdrive terms stem from the two cascode devices and the tail current source. The overdrives from the cascodes should be viewed as the cost of using cascodes. A fully differential cascode op amp is shown in Figure 2.12. Compared to its single-ended counterpart; the main difference is that diode connections are removed from transistors M_3 and M_{3A}. Also, the gates of cascode transistors M_{1A}-M_{4A} are connected to bias voltages here. The op-amp outputs are taken from the drains of M_{IA} and M_{2A} .The resulting circuit is symmetric with each output loaded by a cascoded current source [2]. An advantage of the topology in figure.2.12 is that the DM signal path consists only of PMOS transistors. That is, only the PMOS transistors conduct time-varying currents. The NMOS transistors conduct constant currents. Such a configuration maximizes the op-amp speed because n-channel transistors have higher mobility and f_t than their NMOS counterparts.

The telescopic-cascode topology, although has extremely high gain on the order of $(g_m r_O)^3$ can provide enough gain and minimize power due to the fact that we have current flowing through only one branch [21].

To minimize differential noise, it is vital to keep a large V_{eff} in all current sources in differential branches. So if we reduce V_{eff} in those transistors in hopes of increasing the dynamic range, we risk increasing its effective noise factors thus nullifying any potential dynamic range increase [8].

The second stage differential amplifier can provide a large output swing thus relaxing the output noise allowed. Meanwhile, while most of the gain will be generated in the first telescopic stage, it will not be driving the large capacitive load and can be optimized for gain and range. This division of roles allows a large degree of flexibility in its design. Meanwhile, while most of the gain will be generated in the first telescopic stage, it will not be driving the large capacitive load and can be optimized for gain and range. This division of roles allows a large degree of flexibility in its design. However, in any two-stage amplifier design, a potential compensation capacitance must be placed between the two stages to adjust its phase margin for settling requirements. The second stage may be replaced with a common-source amplifier where the increased output swing would be at the cost of decreased CMRR.

2.5 Common Mode Feedback

For proper operation of a fully differential amplifier, common mode feedback (CMFB) is required to fix the voltages at high impedance nodes in the circuit to their desired values.

Because we employ a two stage design with two inversions, the CMFB also must be inverting. This is accomplished by a switched-capacitor circuit and PMOS differential pair which adjusts the common mode level of the first stage by either injecting current into or bleeding current from the input legs as needed. The common mode output of the first stage is set to the point which minimizes the quiescent current in the second stage. The common mode voltage of the second stage is also dynamically adjusted using the transistors M1 and M2. These transistors help to correct the inherent imbalance in pulling between NMOS in PMOS in a class AB stage during switching. In order not to degrade the overall speed of the amplifier, the unity gain bandwidth of the CMFB circuits must be greater than that of the main amplifier.

2.5.1 Primary Reason for Common Mode Feedback

Since each of input transistors carries a current of $I_{SS}/2$, the CM level depends on how close I_{D3} and I_{D4} are to this value. In practice, as expemilfied by figure 2.14, mismatches in the PMOS and NMOS current mirrors defining I_{SS} and $I_{D3,4}$ create a finite error between $I_{D3,4}$ and I_{SS}. For high gain amplifiers, we wish a p-type current source to balance an n-type current source. As illustrated in figure 2.14, the difference between I_P and I_N must flow through intrinsic output impedance of the amplifier, creating an output voltage change of $(I_P - I_N)(R_P \| R_N)$. Since the current error depends on mismatches and $R_P \| R_N$ is quite high, the voltage error may be large, thus driving p-type and n-type current sources into triode region. As a general rule, if the output CM level cannot be determined by visual inspection and requires calculation based on device properties. Thus we emphasize that differential feedback cannot define the CM level.

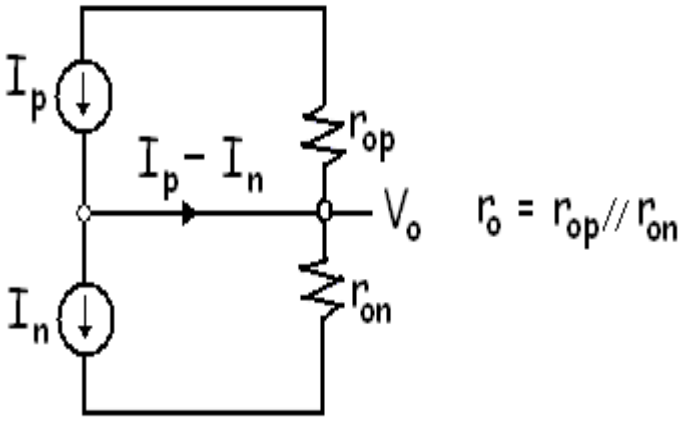

Figure 2.14 Current mismatch problem

The sensing method suffers from an important drawbacks, it limits the differential output swings. Since the common-mode loop gain is not large enough to keep the common-mode voltages steady we must add an external circuit to implement a high-gain Common-Mode Feedback (CMFB) loop. A block diagram of a fully-differential op-amp with CMFB is shown below in figure 2.15 the gain parameters A_{DD}, A_{CD}, A_{DC}. The gain parameters A_{DD}, A_{CD}, A_{DC}, and A_{CC} are the same as shown in figure 2.15. The new gain parameters A_{SD}, A_{SD}, A_{DS}, and A_{CS} model how the CMFB circuit will effects the op-amps behaviour.

The gain parameters A_{SD} and A_{SC} model how the CM control signal Vs effects both V_{ODM} and V_{OCM}. Ideally, the CMFB circuit should keep V_{CM} stable without influencing V_{ODM}. Thus, A_{SC} should be large and ideally approach infinity and A_{SD} should be small and ideally approach 0. The gain parameters A_{DS} and A_{CS} relate the CM control voltage Vs to V_{ODM} and V_{OCM}, respectively. We want the CM sense circuit to generate a control voltage

Vs which is dependant only on the output CM voltage and reject the differential mode (DM) output voltage. Thus, we want A_{DS} to be small and ideally approach 0, and A_{CS} to be large and ideally approach infinity. Given this the following approximations hold: $V_{OCM} \approx A_{SC}*V_S$ and $V_S \approx A_{CS} * V_{OCM}$. From this we can get one of the most important performance parameters of the CMFB loop, namely the CMFB loop gain which is equal to $A_{CML}=(A_{SC}*A_{CS})$.

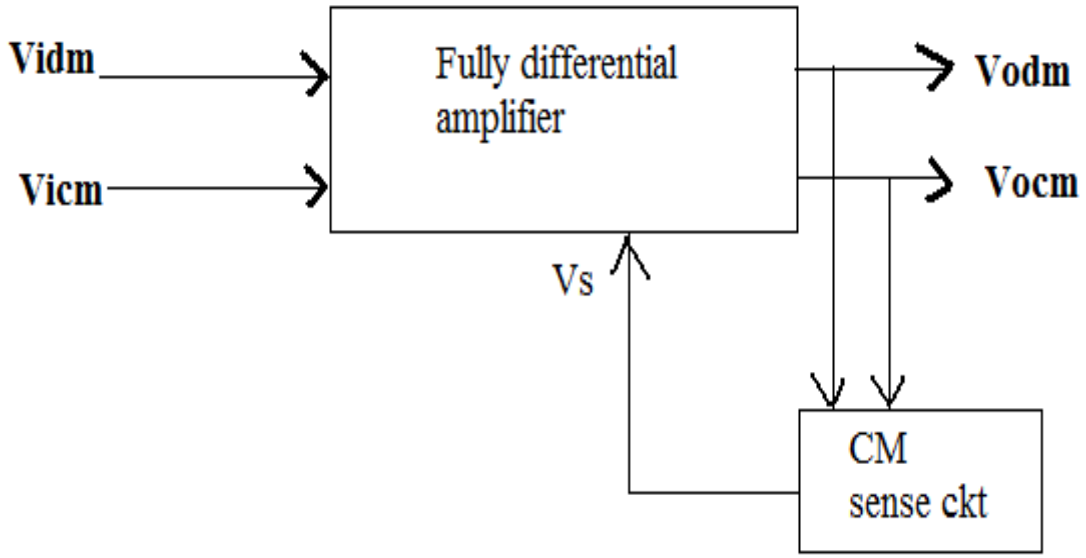

Figure 2.15 Fully differential amplifier with CMFB

To minimize the offset in V_{OCM}, A_{CML} should be designed to be as large as possible, and ideally it approaches infinity. Since in a real world implementation the magnitude of A_{SC} and A_{CS} will be a function of frequency, we want a large magnitude for A_{CML} with a bandwidth as large as the bandwidth of the differential mode bandwidth of the op-amp. A CMFB circuit averages both differential output voltages to produce a common mode voltage V_{CM}. Voltage V_{CM} is then compared to a desired reference common-mode voltage, V_{CM}, usually equal to the average of the two power supplies, or analog ground. The difference between V_{CM} and V_{CMS} is amplified and this error voltage is used to change the common-mode bias current of the op-amp to force V_{CM} and V_{CMS} to be equal. Figure 2.16 shows the connectivity between a current-mirror differential amplifier and its CMFB circuitry.

Notice that the CMFB control voltage Vs changes the common-mode bias current of the op-amp by controlling the gate to source voltage of M3 and M5. As Vs increases, the bias current being sunk into the drain of M3 and M5 also increases which causes an equal reduction in the voltage of nodes Vo+ and Vo-, thereby decreasing Vcm. As Vs

decreases, the bias current sunk into the drain of M3 and M5 decreases thereby increasing Vcm.

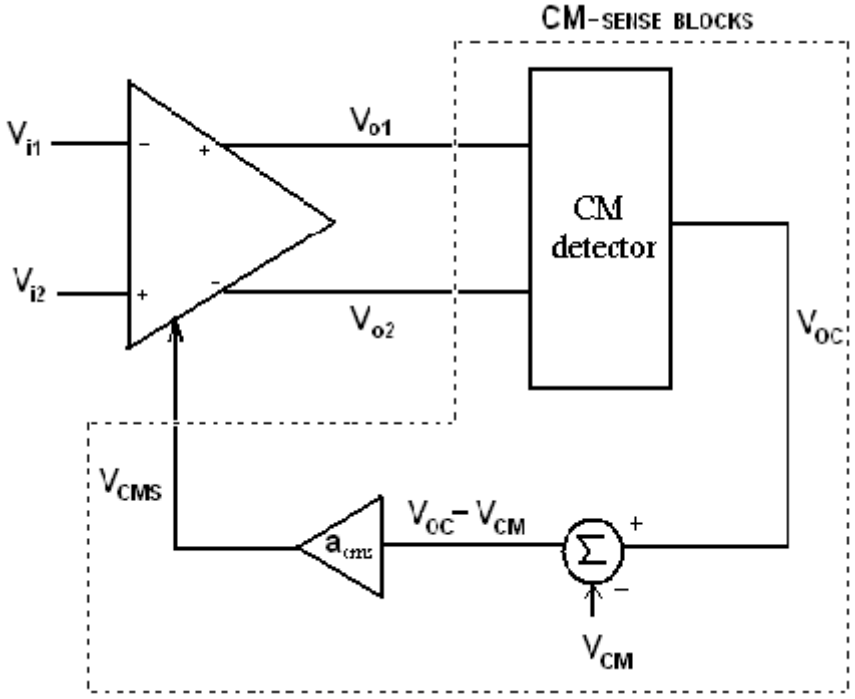

Figure 2.16 Conceptual block diagram of CMFB loop [24]

The I/O signal relationships for fully differential Op-amp with CMFB [24]

$$\begin{bmatrix} V_{ODM} \\ V_{OCM} \end{bmatrix} = \begin{bmatrix} A_{DD} & A_{CD} & A_{SD} \\ A_{DC} & A_{CC} & A_{SC} \end{bmatrix} \times \begin{bmatrix} V_{iDM} \\ V_{iCM} \\ V_S \end{bmatrix} \tag{2.28}$$

$$\begin{bmatrix} V_S \end{bmatrix} = \begin{bmatrix} A_{DS} & A_{CS} \end{bmatrix} \times \begin{bmatrix} V_{ODM} \\ V_{OCM} \end{bmatrix} \tag{2.29}$$

The current in the CMFB circuit does not need to be large as long as the currents through the top and bottom of the OTA are fairly well balanced. Since the common mode feedback circuit only adds to the bias current in the bottom of the circuit, it is expected that the bias currents in top half will be slightly lower.

Most CMFB circuits can be divided into three general categories: Switched-Capacitor (SC) CMFB circuits, differential difference amplifier (DDA) CMFB circuits or resistor-averaged CMFB circuits. The major distinction between these three categories is the technique used to average the differential output voltages to produce the common mode voltage V_{CM}.

2.6 Frequency Compensation Techniques

The single stage amplifier typically has good frequency response and could achieve a phase margin of 90° assuming the gain bandwidth is ten times higher than the single pole. However, the dc gain of the single amplifier is generally not high enough and is even less for submicron CMOS transistors. In general, op amps require at least two gain stages. As a result, op amp circuits have multiple poles. The poles contribute to the negative phase shift and may cause phase angle -180°, before the unity gain frequency. The circuit will then oscillate due to the negative phase margin. It leads to the necessity of altering the amplifier circuit to increase the phase margin and stabilize the closed loop circuit. This process is called "compensation".

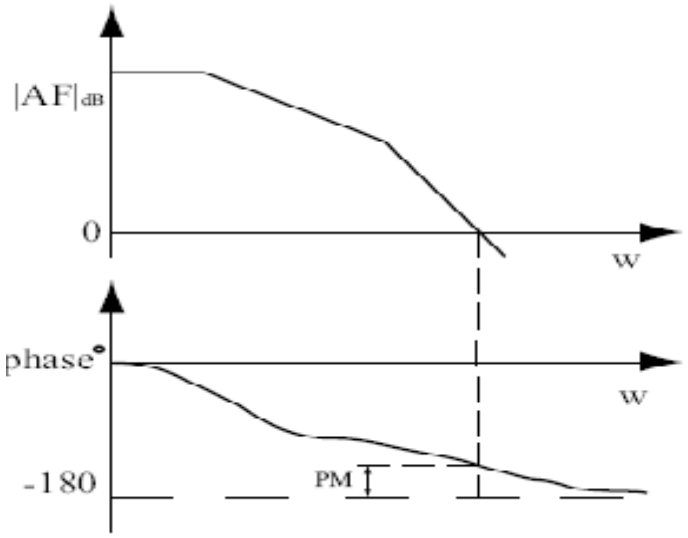

Figure 2.17 Phase Margin Plot

The most straightforward way is to make the gain drop faster in order for the phase shift to be less than −180° at the unity gain frequency. This method achieves stability by reducing the bandwidth of the amplifier. The most popular pole splitting method uses this procedure. Another compensation method pushes the phase crossover frequency out by decreasing the total phase shift. In this case, the number of the poles of the op amp needs to be minimized while still providing enough gain. Pushing the phase crossover frequency out is the basic idea of approaches like introducing zeros to cancel the poles or using feed forward paths to improve the phase margin without narrow-banding the bandwidth as much as the pole splitting method does. The feed forward method modifies the open loop transfer function or the closed loop transfer function to increase the phase margin [23]. The frequency response of the multistage amplifier is not as good as that of the single

stage and this amplifier has a higher probability of oscillation in feedback circuits. One popular way to predict the closed loop stability is by measuring the phase margin of the open loop gain response. PM must be greater than 0^{o} for no oscillation to occur. A good performing amplifier will need a PM of about 45° to 60°. Otherwise, the amplifier may exhibit ringing in the time domain and peaking in the frequency domain.

2.6.1 PARALLEL COMPENSATION

Parallel compensation is a classical way to compensate the op amp. A capacitor is connected in parallel to the output resistance of a gain stage of the operational amplifier to modify the pole. It is not commonly used in the integrated circuit due to the large capacitance value required to compensate the op amp, which costs considerable die area.

2.6.2 POLE SPILITTING –SINGLE MILLER COMPENSATION (SMC)

By putting a compensation capacitor between the input and output nodes of the second inverting stage of the op amp, the dominant pole is created due to Miller feedback. This method maintains a high midband gain for the op amp since the capacitor does not affect the dc response of the amplifier.

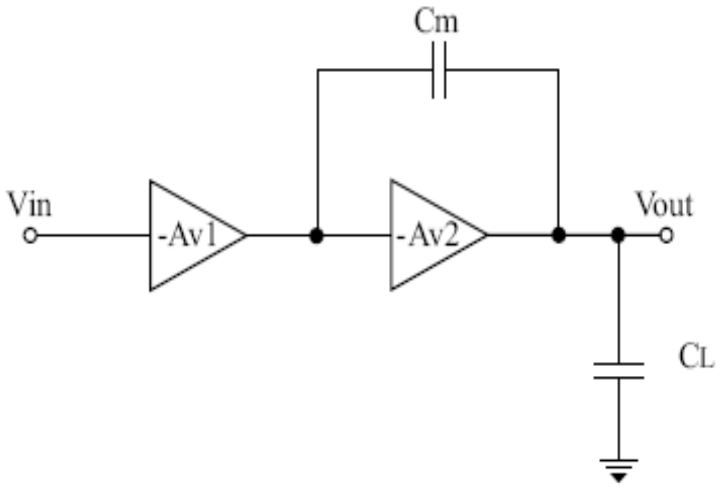

Figure 2.18 Single Miller Compensation (SMC)

Figure 2.18 shows standard SMC topology. As the transistor gain of the second stage increases, the dominant pole decreases and the non-dominant pole increases. In this way the two poles are being split apart and stabilize the feedback amplifiers by greatly narrowing the bandwidth. This simple pole splitting method also introduces a right half plane zero which causes negative phase shift, as a result, the stability is made a little poorer. The zero comes from the direct feed through of the input to the output through the

Miller capacitor. To eliminate the RHP zero due to the feed through and increase the phase margin of the op amp, lead compensation which adds a nulling resistor in series with the compensation capacitor (SMCNR) to increase the impedance of the feed through path is reported.

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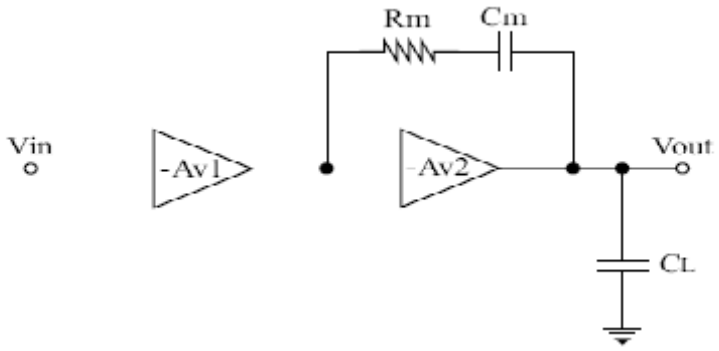

Figure 2.19 Single Miller Capacitor Nulling Resistor (SMCNR)

The effect of the nulling resistor to the positions of the poles as well as that of the zero and pointed out the pole splitting would break down if the resistor becomes too big. When the resistor gets very large, there is no pole splitting since the compensation capacitor is actually open circuit. Single Miller capacitor nulling resistor (SMCNR) configuration is shown in figure 2.19.

2.6.3 SINGLE MILLER FEEDFORWARD COMPENSATION (SMFFC)

Many compensation techniques mentioned above are not suitable for large load capacitors. The demand for lower power consumption, lower chip integration area, capability for driving large capacitive loads and stable high gain bandwidth of amplifiers calls for improved frequency compensation patterns. The topologies using a single Miller capacitor in three stage amplifiers could greatly reduce the needed sizes of the compensation capacitors compared to NMC related schemes and result in amplifiers with smaller chip area. The presented SMFFC and the modified SMC with the additional feed forward path from the output of the first stage to the output load stage.

The topology of the SMFFC op amp is represented in figure. 2.20. Instead of using pole zero cancellation, SMC with one forward path adopts the separate pole approach for compensation in the situation of large capacitive loads. SMFFC employs two forward

paths and provide a LHP zero to compensate the first non dominant pole to alleviate the bandwidth reduction and improve the phase margin.

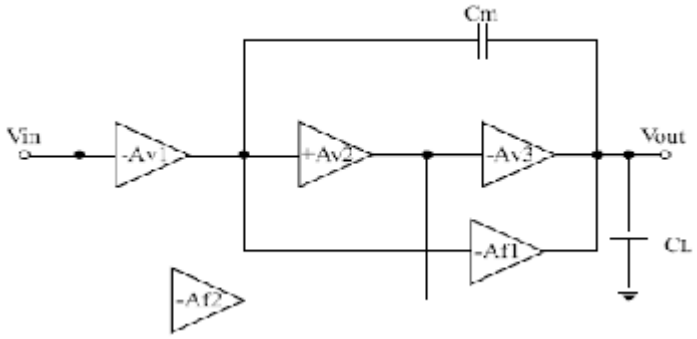

Figure 2.20 Single Miller Feed Forward Compensation (SMFFC)

The second and third poles of the amplifier would be placed at higher frequencies that lead to a coarse single pole system for an easier frequency compensation strategy. The appropriate selection of the moderate gain of the second stage will then decrease the compensation capacitor size. Unfortunately, this method does not truly resolve the compressed gain bandwidth issue due to the super high gain of the first stage and the nature of the pole separation. Gain enhanced feed forward path compensation.

2.6.4 NEGATIVE MILLER CAPACITANCE COMPENSATION (NMCC)

The negative Miller capacitance compensates high speed CMOS op amp, that consists of an operational transconductance amplifier (OTA) and a buffer. The buffer with a dc gain of A_V is used to detach the OTA from the load. The OTA is compensated with a capacitor Cc connected between the input and output of the buffer. Assuming the op amp drives a load with a parallel combination of a resistor R_L and a capacitor C_L, the effective capacitance seen at the input of the buffer is $C_{in} = C_C(1 - A_V)$ and $C_{out} = C_L + C_C\left(1 - \frac{1}{A_V}\right)$ at the output of buffer. Since the gain of the buffer is positive and smaller than one, the reflected Miller capacitor $C_C\left(1 - \frac{1}{A_V}\right)$ at the output will be negative. The total effective output capacitance is reduced to be smaller than the original load capacitance due to the negative Miller capacitance. NMCC can be applied to drive a large capacitive load. The experimental results show that the NMCC design shifts the first non dominant pole to a higher frequency while keeping the position of the dominant pole almost the same, could increase both the bandwidth and phase margin.

CHAPTER 3
DESIGN OF TWO STAGE FULLY DIFFERENTIAL OPERATIONAL AMPLIFIER

3.1 Topology Selection

For high speed and high accuracy circuits, op amps with high open loop DC gain for the settling accuracy of 1% in less than 30ns, high output swing due to large output dynamic range specification of 85dB, high unity-gain bandwidth are required. This indicates that the chosen topology must have large output swing as well as minimal noise. Our target is to design an amplifier with 300MHz unity-gain bandwidth and a DC-gain higher than 80dB, with a 5pF load. This op amp is intended to work in a switched-capacitor integrator in the first stage of a delta-sigma modulator and CMOS ADC.

The first, and probably the most important, step of the design is to select an amplifier topology that possesses the ability to meet all the specifications using the least amount of power. Due to the high close-loop gain and the extremely small allowable settling error of 0.01%, a quick calculation reveals that the amplifier must be able to deliver an open-loop gain of 80dB, which is on the order of $(g_m r_O)^3 \sim (g_m r_O)^4$. Gain boosting is very attractive because boosters can multiply up the gain of the main amplifier while consuming minimal power. An important concern when utilizing gain boosters is the pole-zero doublet, which must be placed at a high enough frequency to prevent it from slowing the settling but not so high that it causes significant ringing around the local gain-booster loop.

Topologies that will certainly satisfy this magnitude of DC gain include a two stage amplifier with either a telescopic or folded cascode first stage, a gain-boosted amplifier or a folded triple cascode. To avoid much complexity in the design process a two-stage topology is chosen.

The 85dB dynamic range specification calls for a careful comparison between single-stage and two stage topologies. In a two-stage implementation, the second stage can be designed to provide a larger output swing of 3V, thereby reducing the capacitance driven by the input transistors and consequently lowering the required current in the first stage. However, the second stage generally needs to flow at least the same amount of current as the first stage to allow for slewing during amplifier operation. The total currents required

for the two-stage topology would therefore be at least double that of the first stage. Hence, if a single stage amplifier can achieve output swing higher than 2.3V (3.3 divided by $\sqrt{2}$), it would dissipate lower power than a two-stage amplifier. In terms of circuit topology, telescopic is the necessary choice over folded-cascode in order to realize this benefit in decreased power since a telescopic amplifier consumes only half as much power and produces less noise at the expense of a slightly tighter output swing. For the a fore mentioned reasons, telescopic single-stage with gain boosting is chosen as the topology of our amplifier. Output swing of at least 2V zero-to-peak is set as an additional design specification, which leaves 1V for 5 stacking transistors. This, combined with a large tail current stemming from the stringent settling accuracy requirement, requires us to pursue a design with large transistors. To prevent the large input parasitic capacitance from lowering the feedback factor, C_f and C_s would have to be increased accordingly, leading to huge on-chip area consumption if we were to layout the amplifier. Fortunately, area is not a specification or an objective to be optimized in this project. NMOS is selected to be the input transistors over PMOS because smaller area is needed to realize the same trans-conductance. Another shortcoming of this design is a poor CMRR because we are forced not to cascode the tail current source due to limited voltage headroom.

Designing a one stage gain-boosted amplifier to have a high output swing, low noise, and high gain at the same time is obviously not an easy task. Although two-stage design seems to be less power efficient (four main current legs), it gives us more degrees of freedom in the design. Our basic calculations indicates that by combining the high-output swing and relatively low noise properties, two-stages amplifier tends to consume less power than the gain-boosted one stage amplifier for reaching the given specifications. So we select the two stage topology for our design. Noting that using two stages allows one to separates the gain stage from the stage that determines the output swing, we further looked into the two-stage design. We liked the fact that the main gain stage would not have to drive the large capacitive load. Additionally the two-stage topology would give us more degrees of freedom to optimize our design, at the cost of complexity. We made our decision after verifying that a two-stage topology would not cause problems meeting the speed requirements. We decided on the telescopic design over folded cascode for our first stage because it has fewer current legs, consumes less power, and adds less noise to the signal path. A large signal swing was not required of the first stage, which also is in favour of the telescopic design. the telescopic amplifier has only four transistors in the signal path contributing significant noise power, whereas the folded cascode has six

transistors. Because it consumes less power and has less noise, the telescopic amplifier was chosen for the first stage.

Telescopic cascode op-amp as shown in figure 3.1, typically has higher frequency capability and consumes less power than other topologies. Its high-frequency response stems from the fact that its second pole corresponding to the source nodes of the n-channel cascode devices is determined by the transconductance of n-channel devices as opposed to p-channel devices, as in the case of a folded cascode. Also the parasitic capacitance at this node arises from only two transistors instead of three, as in the latter. The single stage architecture naturally suggests low power consumption.

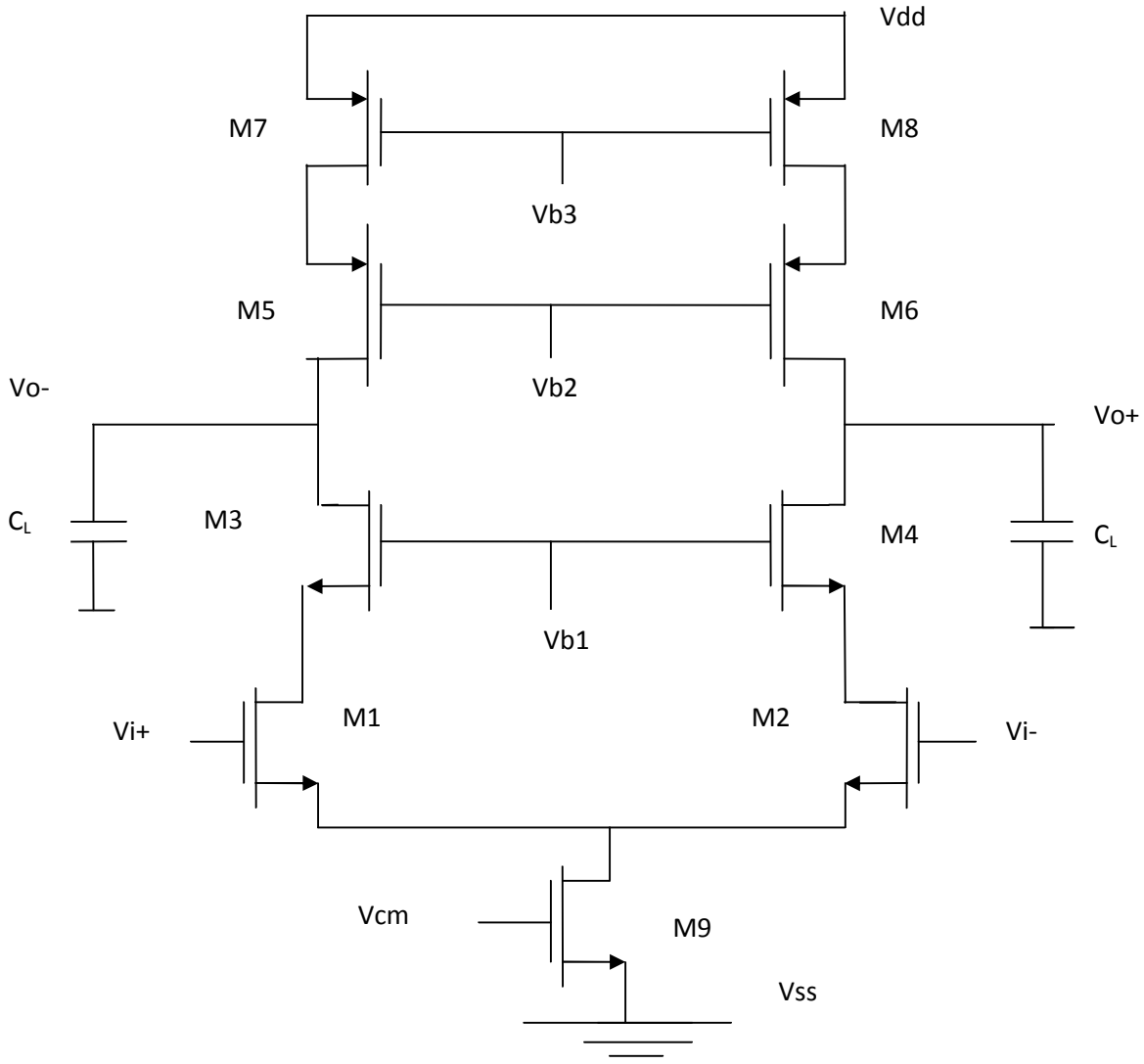

Figure 3.1 Telescopic differential amplifier

3.2. Design Specifications

The target specifications of the design are given in the Table 3.1.

Table 3.1 Target Specifications of Design

Specification	Target Value
DC open loop gain	≥ 80 dB
Unity gain bandwidth	300 MHz
Phase margin	≥50°
f_{-3dB} frequency	≥ 5KHz
Output dynamic range	≥85 dB
CMRR	≥ 85 dB
Output voltage swing	≥ 3V (peak to peak)
Power dissipation	Minimize (≤ 5mW)
Slew rate	≥ 20 V/μS
Settling time	≤ 30 nS
Load capacitance	5pF
Supply voltage	3.3V

3.3. Design of Two Stage Telescopic Fully Differential OTA

In this section we discuss various steps to follows in the designing of the fully differential with having target specification as given in Table 3.1.

The first step of any two stage design is the design of input differential stage amplifier, which is telescopic differential amplifier in our case. The input transistors of the telescopic cascode stage are NMOS devices to maximize gm/Id.

For the second/output stage, a common source amplifier for each differential output was utilized as typically done. Differential amplifiers as output stage would be more complicated due to the design of another common mode feedback circuit. In addition, the tail current transistor for the differential amp will only consume voltage headroom, thus lowering the output swing. To ensure stability of the amplifiers, miller compensation is used despite the cascode compensation's better high frequency performance. Miller compensation however, can be easily designed and will introduce non-negligible noise depending on how the circuit is compensated.

3.3.1 Design of First Stage Telescopic Amplifier

Telescopic differential amplifier as shown in figure 3.1, all transistors must be in saturation region of operation. Since schematic is of balance in nature so we adopt half circuit method to find its dc gain.

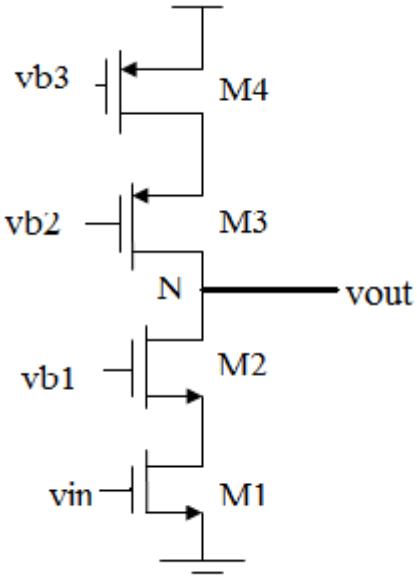

Figure 3.2 Half circuit of telescopic cascode

Let us now consider the small signal characteristics of a cascode stage, assuming all transistors operates in saturation. The voltage gain is equal to that of common source stage because the drain current produced by input device must flow through the cascode device. An important property of the cascode structure is its high output impedance. The output impedance (R_{OUT}) of the schematic as shown in figure 3.2 is calculated as;

$$R_{OUT} = \{(1+(g_{m2}+g_{mb2})r_{O2})r_{O1}+r_{O2}\} \| \{(1+(g_{m3}+g_{mb3})r_{O3})r_{O4}+r_{O4}\} \quad (3.1)$$

We calculated the gain as

$$A_V \approx -G_m R_{OUT} \text{ and } G_m \approx g_{m1} \quad (3.2)$$

Where, g_{m1} is the trans-conductance of input transistor M1.

The transconductance g_m of MOS transistor is defined as

$$g_m = \frac{\delta I_D}{\delta V_{GS}} \text{ at constant } V_{DS} \quad (3.3)$$

$$g_m = \mu_n C_{OX} \frac{W}{L}(V_{GS} - V_{th}) \quad (3.3(a))$$

$$= \sqrt{2\mu_n C_{OX} \frac{W}{L} I_D} \tag{3.3(b)}$$

$$= \frac{2I_D}{V_{GS} - V_{th}} \tag{3.3(c)}$$

The total gain of the cascode structure is give by;

$$A_V \approx g_{m1}\{(1+(g_{m2}+g_{mb2})r_{O2})r_{O1}+r_{O2}\} \| \{(1+(g_{m3}+g_{mb3})r_{O3})r_{O4}+r_{O4}\} \tag{3.4}$$

$$A_V \approx g_{m1}(g_{m2}r_{O1}r_{O2}) \| (g_{m3}r_{O3}r_{O4}) \tag{3.5}$$

Therefore, cascading of transistors increases the differential gain substantially but at the cost of consuming more voltage headroom.

The power dissipation of two stage operational amplifier is given by;

$P_d=V_{DD}$ (I_{TAIL} + I_{SECOND}), where I_{TAIL} is input tail current of first stage and I_{SECOND} is total sum of output branch current which is twice of individual output branch current.

Since input differential amplifier is gain stage of our design, the telescopic cascode amplifier is of gain of the order of $(g_m r_O)^2$. Since the total gain of operation amplifier is ≥ 80 dB, therefore we divide this much of gain as 55db for first stage and rest 30 db for second stage which is a common source stage with appropriate phase margin.

To achieve the power dissipation (<5mW) and gain parameter. We distributed the current as the current in second stage must be at least 4-5 times of the input stage current, so that there is no overlapping of non-dominant pole with dominant pole for getting good phase margin and proper high bandwidth. Let input tail transistor draw 100μA of current, i.e. I_{SS}=100μA=2I_D.

$$I_{DP} = \frac{1}{2}\mu_P C_{OX}(V_{SG} - |V_{tp})^2 \tag{3.6(a)}$$

$$I_{Dn} = \frac{1}{2}\mu_n C_{OX}(V_{GS} - V_{tn})^2 \tag{3.6(b)}$$

The technology parameters used in calculations are:

$\mu_n C_{OX} = 132.5\times10^{-6}$ A/V^2 $\quad$ λ_n=0.02 V^{-1} $\quad$ $V_{tn} = 0.549V$

$\mu_p C_{OX} = 50.12\times10^{-6}$ A/V^2 $\quad$ λ_p=|0.04| V^{-1} $\quad$ $V_{tp} = -0.68V$

And $r_O \approx \frac{1}{\lambda I_D}$

In figure 3.1, the input common mode (CM) level and the bias voltages V_{b1} and V_{b2} must be chosen so as to allow maximum output swings. The maximum allowable input CM

level equals $V_{GS1}+V_{OD9}=V_{th1}+V_{OD1}+V_{OD9}$. The minimum value of V_{B1} is given by $V_{GS3}+_{OD1}+V_{OD9}$. Similarly, $V_{B2,\max} = V_{DD}-(|V_{GS5}|+V|_{OD7}|)$. In practise, some margin must be included in the value of V_{B1} and V_{B2} to allow the process variation.

The telescopic cascode design starts with the sizing of the main differential input pair of transistors M1 and M2 as shown in figure 3.2, using the desired phase margin and gain bandwidth specifications. As these are the two factors that affect the input pair transistors they are first designed to meet the required specifications. Care has to be taken not to make the input pair too big to affect the bandwidth and at the same time making them big enough to provide enough transconductance and hence the gain. The NMOS Ml and M2 cascode transistors are then sized to act as a buffer between the input pair and the output. These transistors are sized such as not to load the output nodes with huge parasitic capacitances so as to affect the bandwidth of the amplifier.

The PMOS cascode load transistors are designed to steer the required amount of current through both the legs. Here again the PMOS cascode transistors are sized so as not to load the output with huge parasitic capacitances. The overall gain is in general increased by approximately the gain of the gain-boost amplifiers; the gain specifications of the gain-boost amplifiers were thereby known. The unity gain frequency of the gain-boost amplifiers should be large enough so that they do not significantly affect the frequency behaviour of the overall amplifier. They will reduce the unity gain frequency of the overall amplifier since by adding the gain-boost amplifiers to the output side, extra capacitance and thereby some extra poles are added.

The gain had increased, but both the unity gain frequency as well as the phase margin was degraded too much. The bias currents of the main amplifier were then increased and some of the bias voltages were altered. Since the output DC-level of the gain boost amplifiers can be chosen from a wider range than the bias voltages, this was another benefit of using gain boosting. In a way they give both increased gain and voltage level shift although at the cost of added complexity.

Let the gain for first stage is of 55 dB and tail current of 100µA

$I_D=I_{SS}/2=50\mu A$

Hence $r_{O1} \approx \frac{1}{\lambda_n I_D} = 1M\Omega \approx r_{O2}$ and

$$r_{O3} \approx \frac{1}{\lambda_p I_D} = 0.5M\Omega \approx r_{O4}$$

Keeping V_{incm}=1.65V for getting maximum output swing. For biasing all the stack transistors in saturation, we satisfy the condition of saturation of MOSFET $(V_{GS} - V_t) < V_{DS}$ for each transistor of cascode stage.

V_{incm}=1.65V and V_{tail}= 0.6V for current source tail transistor and also assuming the output DC level at 1.65V for better response. By applying all conditions we gets biasing voltage condition as follows as shown in half circuit figure 3.2.

$$V_{b1} \leq 2.65V \; ; \; V_{b2} \leq 2.35V \text{ and } V_{b3} > 2.15V \tag{3.7}$$

First before starting actual design it is important to fix length of the device. Length of the device is normally kept three or four times of the minimum feature size of the selected technology. Thus length selected for the design is L = 1.4μm (four times of feature size).

After employing above all conditions equation 3.1- 3.7 and using some iteration on tool, we design first stage of telescopic differential amplifier with following aspect ratio as for figure 3.1.

Table 3.2 Aspect ratio of input stage transistors

Transistor	M1,M2	M3,M4	M5,M6	M7,M8	M9
Aspect ratio	18.9/1.4	14/1.4	56/1.4	112/1.4	694.75/1.4

Now consider the fully differential telescopic cascode, in addition various useful properties of differential operation, this topology avoids the mirror pole, thereby exhibiting stable behaviour for a greater bandwidth. In fact, we identify one dominant pole at each output node and one nondominant pole arising from output node. This suggests the fully differential telescopic cascode circuits are quite stable.

The capacitance at node N in figure 3.2.

$$C_N = C_{GS5} + C_{SB5} + C_{GD7} + C_{DB7} \tag{3.8}$$

The C_N shunts the output resistance of M7 at high frequencies, thereby dropping the output impedance of the cascode. The Z_{out} of the single stage fully differential op-amp is;

$$Z_{out} = (1 + g_{m5} r_{O5}) Z_N + r_{O5} \tag{3.9}$$

where body effect is neglected and $Z_N = r_{O7} \,||\, (C_N s)^{-1}$ (3.10)

We have,

$$Z_{out} \approx (1 + g_{m5} r_{O5}) \frac{r_{O7}}{r_{O7} C_N s + 1} \tag{3.11}$$

Now, we take the output load capacitance into account;

$$Z_{out} \| \frac{1}{C_L s} = \frac{(1+g_{m5}r_{O5})\dfrac{r_{O7}}{1+r_{O7}C_N s} \bullet \dfrac{1}{C_L s}}{(1+g_{m5}r_{O5})\dfrac{r_{O7}}{1+r_{O7}C_N s} + \dfrac{1}{C_L s}} \tag{3.12}$$

$$= - \frac{(1+g_{m5}r_{O5})r_{O7}}{[(1+g_{m5}r_{O5})r_{O7}C_L + r_{O7}C_N]s+1} \tag{3.13}$$

Thus, the parallel combination of Z_{out} and load capacitance (C_L) still contains a single pole corresponding to a time constant $(1+g_{m5}r_{O5})r_{O7}C_L + r_{O7}C_N$.

3.4 Compensation of Two Stage Op-Amp

The two stage topologies may prove inevitable if the output swing voltage swing must be maximized. Thus, the stability and compensation of such op-amps is of interest. The circuit shown in figure 3.3, we identify three poles: pole at X (or Y), another at E (or F) and third at A (or B). From our foregoing discussion, we know that the pole at X lies at relatively high frequencies.

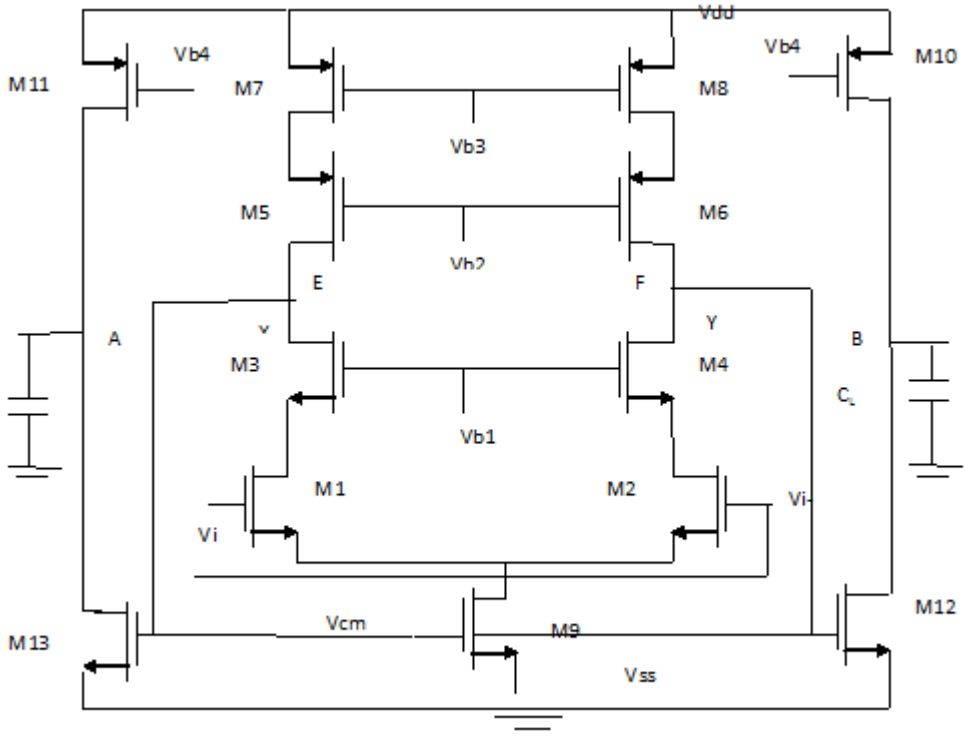

Figure 3.3 Two Stage telescopic Op-Amp

The small signal resistance seen at E in figure 3.4 is quite high, even the capacitance of M3, M5 and M9 create a pole relatively close to the origin. At node A, the small signal resistance is lower but the value of C_L may be quite high. Consequently, we say that the circuit exhibit two dominant poles. One of the dominant poles must move toward the origin so as to place the gain crossover well below the phase crossover. However, the unity gain bandwidth after compensation cannot exceed the frequency of the second pole of the open loop system. Thus, if the magnitude of $\omega_{P,E}$ is to reduced, the available bandwidth is limited to approximately $\omega_{P,A,}$, a low value. Furthermore, the very small magnitude of the required dominant pole translates to a very large compensation capacitor.

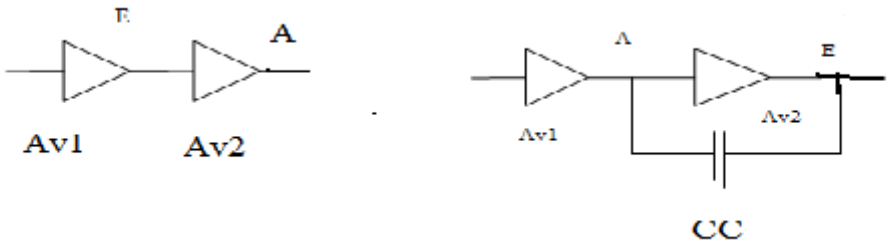

Figure 3.4 Miller compensation of two stage op-amp

The circuit as shown in figure 3.3 with Miller capacitances gives two poles as follows:

$$\omega_{P1} \approx \frac{1}{R_S\left[\left(1+g_{m9}R_L\right)\left(C_C+C_{GD9}\right)+C_E\right]+R_L\left(C_C+C_{GD9}+C_L\right)} \tag{3.14}$$

$$\omega_{P2} \approx \frac{R_S\left[\left(1+g_{m9}R_L\right)\left(C_C+C_{GD9}\right)+C_E\right]+R_L\left(C_C+C_{GD9}+C_L\right)}{R_S R_L\left[\left(C_C+C_{GD9}\right)C_E+\left(C_C+C_{GD9}\right)C_L+C_E C_L\right]} \tag{3.15}$$

where, R_S denotes output resistance of the first stage and $R_L = r_{O10} \| r_{O12}$.

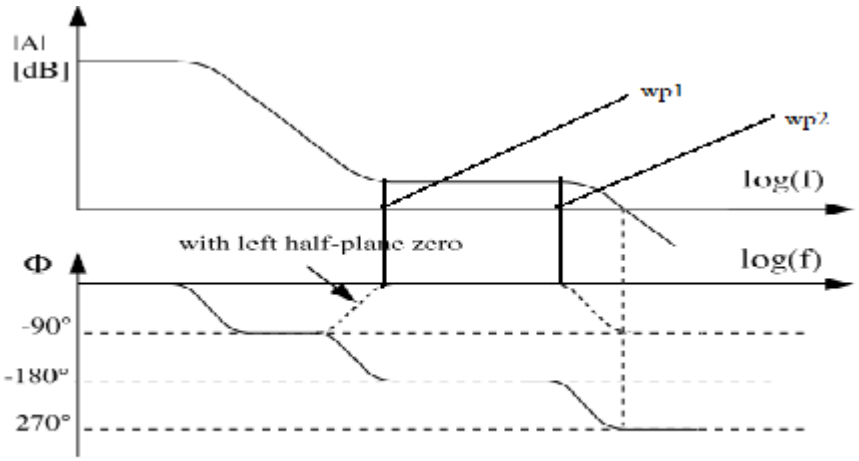

Figure 3.5 Bode plots of loop gain of two stage op-amp

These expressions are based on the assumption $|\omega_{P1}| << |\omega_{P2}|$.Before compensation, ω_{P1} and ω_{P2} are of the same order of magnitude. For large C_L the magnitude of output pole approximated as $\omega_{P2} \approx 1/(R_L C_L)$ and after compensation, $\omega_{P2} \approx g_{m9}/(C_E + C_L)$.

In cascode topologies, the zeros are quite far from the origin, in two stage op-amps incorporating Miller compensation, a nearby zero appears in the circuit. The right half plane zero at $\omega_Z = g_{m9}/(C_C + C_{GD9})$. This is because $C_C + C_{GD9}$ forms a 'parasitic' signal path from input to output. The presence of right half zero degrades the stability considerably. The right half plane zero in two-stage CMOS op amps, given by $g_m/(C_c + C_{GD})$, is a serious issue because g_m is relatively small and C_C is chosen large enough to position the dominant pole properly.

For moving or eliminating zero, there are many method have been develop, one approach is to place a resistor in series with compensation capacitor, thereby modifying the zero frequency. The zero frequency is given by:

$$\omega_Z \approx \frac{1}{C_C\left(g_{m9}^{-1} - R_Z\right)} \tag{3.16}$$

In practise we may even move the zero well into the left half plane so as to cancel the first nondominant pole. This occurs if

$$\frac{1}{C_C\left(g_{m9}^{-1} - R_Z\right)} = \frac{-g_{m9}}{C_L + C_E}, \tag{3.17}$$

that is,

$$R_Z = \frac{C_L + C_C + C_E}{g_{m9} C_C} \tag{3.18}$$

$$\approx \frac{C_L + C_C}{g_{m9} C_C} \tag{3.19}$$

because, C_E is typically much less than C_L+C_C.

The above followed compensation technique is known as nulling resistor compensation technique. The zero position is pushed away with a resistance in series with *Cc*.

$$\frac{V_O}{V_{in}} \approx A_O \frac{1 + s\left(R_Z - 1/g_{m2}\right)C_C}{\left(1 + \frac{s}{P_1}\right)\left(1 + \frac{s}{P_2}\right)} \tag{3.20}$$

3.5 COMMON MODE FEEDBACK CIRCUIT

The high differential gain of a fully differential amplifier stabilizes the differential-mode signals within the amplifier, but the common-mode signals can float. Extra circuitry, called a Common-Mode Feedback (CMFB) circuit, is required to increase the common-mode loop gain of the amplifier so that the common-mode signals are stabilized. This CMFB circuit implements a negative feedback loop that must be compensated properly to minimize the loop settling time and maintain stability. The design of the CMFB circuit is more challenging than the actual op-amp design due to the difficulty of properly compensating it. The differential amplifier stabilizes the common mode signal by common mode feedback.

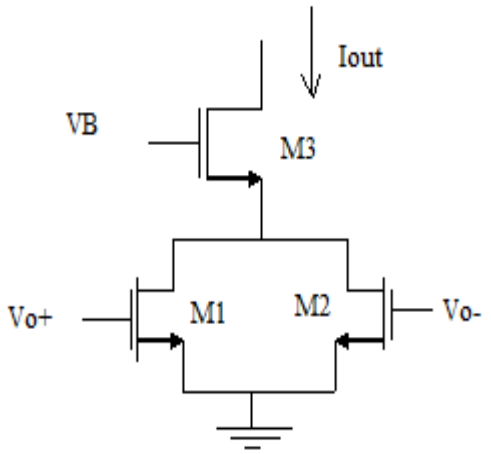

Figure 3.6 Common mode feedback schematic

The voltage VB is chosen such that M1 and M2 are in linear region. The $(W/L)_1$ and $(W/L)_2$, M1 and M2 are like parallel of two voltage dependent resistances.

$$I_1 = \mu_n C_{OX}\left(\frac{W}{L}\right)_1 \{(V_{o+} - V_t)V_{DS} - \frac{1}{2}V_{DS}{}^2\} \tag{3.21}$$

$$I_{2=}\mu_n C_{OX}\left(\frac{W}{L}\right)_2 \{(V_{o-} V_t)V_{DS} - \frac{1}{2}V_{DS}^2\} \tag{3.22}$$

$$I_{OUT} = I_1 + I_2 = \frac{1}{2}\ \mu_n C_{OX}\left(\frac{W}{L}\right)_3 (V_B - V_{DS} - V_t)^2 \tag{3.23}$$

With common mode signal: if positive, I_{OUT} increases.

With common mode signal: if negative, I_{OUT} decreases.

Common mode feedback circuits were used to regulate the common mode outputs for the first and second stages. The dual differential pair sense amp configuration was used, with a diode connected NMOS tail supplying the common mode control voltage to the bottom NMOS transistors on the telescopic cascode amplifier.

3.6 OUTPUT STAGE DESIGN

Analog circuits are often required to drive large loads with wide signal swing. This creates a need for output stages with wide signal swing capability and sufficient transconductance relative to the load capacitance to meet bandwidth requirements. Output stages, especially at low supply voltages, are limited to a single n-channel and p-channel transistor as shown in figure 3.8 to maximise the signal swing.

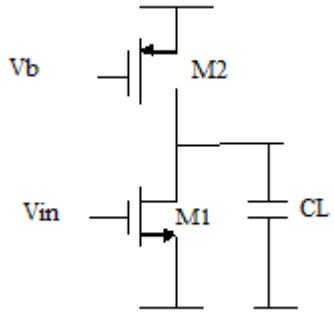

Figure 3.7 Schematic of class A output stage

This allows the output range from V_{dsat} to V_{SUPPLY} - V_{dsat}. Class A output stages as shown in figure 3.8, are simple to design and have low distortion.

The gain of output stage is given by

$$A_{V2} \approx g_{m1}\left(r_{O1} \| r_{O2}\right) \tag{3.24}$$

The current in the output stage is atleast three times to that of input differential stage for proper stability and bandwidth.

The output stage transconductance is largely determined by transistor sizing since biasing variations are limited by headroom at low supply voltages.

The two-stage design was supposed to be good when its first stage gain is much larger than that of second stage. That was noise could be approximated by the first stage alone since the gain of the second stage should be negligible. The major setback with that trade-off is that by decreasing the gain ratio of the first stage to second stage is that the noise

from the first stage will be amplified significantly. As a result, due to the large amplification of the telescopic noise, the measured dynamic range is now reduced. This assumption is further proved by measuring the output noise of the first stage as compared to the output noise of the second stage.

3.7 Schematic of Two Stage Fully Differential Op-Amp

The complete schematic of the fully differential telescopic operational amplifier which meets the target specifications is shown in figure 3.9.

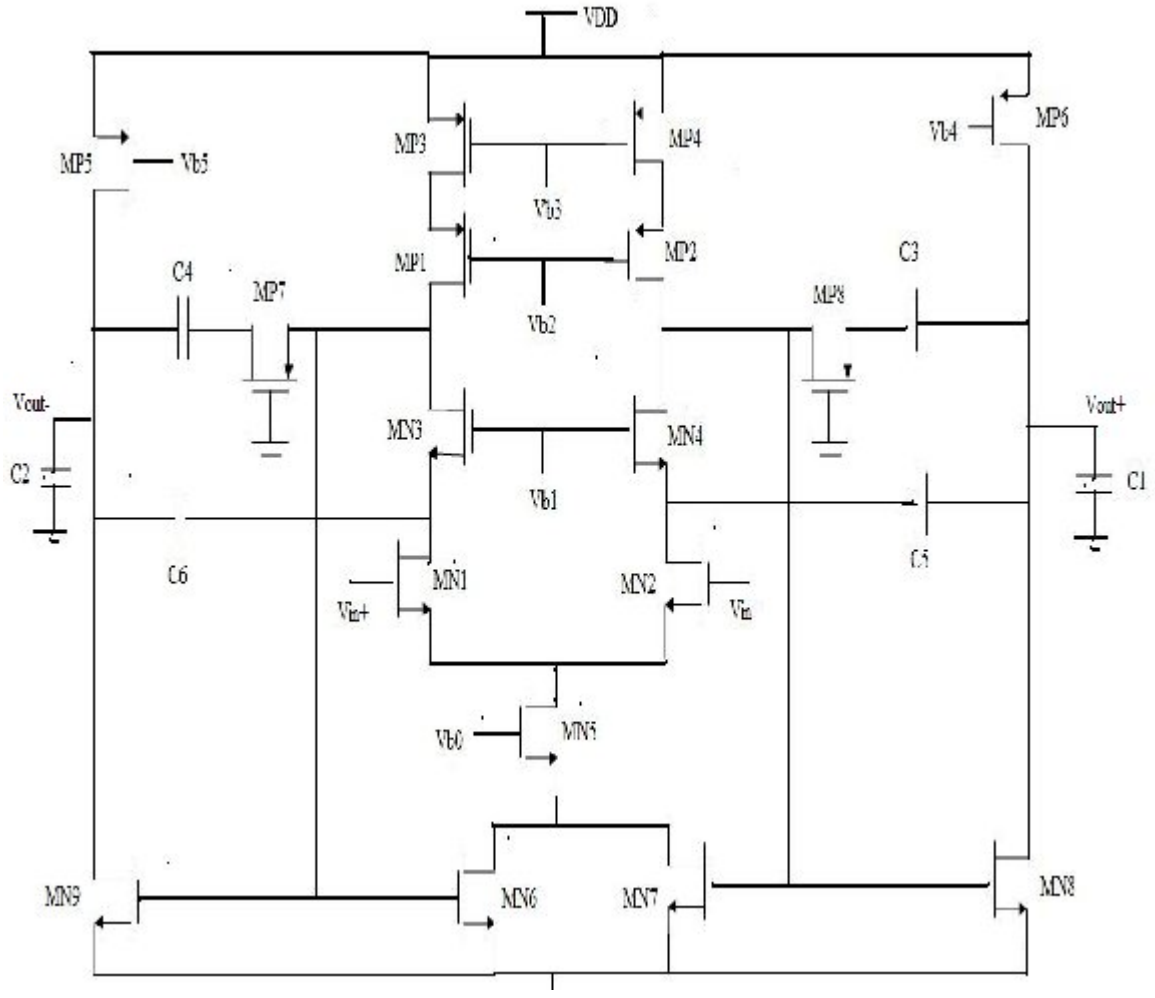

Figure 3.8 Schematic of two stage fully differential op-amp

The aspect ratio of each transistor in circuit design with their function in circuit is given in Table 3.3. The values of capacitances and bias voltages of circuit are given in Table 3.4 and Table 3.5 respectively.

Table 3.3 Aspect ratio of transistors and their functions in op-amp

Transistors	Aspect ratio	Function	Region of operation
MN1& MN2	18.9µm/1.4µm	Input drivers	Saturation
MN3 & MN4	14µm/1.4µm	Cascode load	Saturation
MN5	694.75µ/1.4µm	Bias current source	Saturation
MN6 & MN7	7.7µm/1.4µm	Common mode feedback	Linear
MN8 & MN9	5.95µm/1.4µm	Second stage driver	Saturation
MP1 & MP2	56µm/1.4µm	Cascode load	Saturation
MP3 & MP4	112µm/1.4µm	Cascode load	Saturation
MP5 & MP6	287µm/1.4µm	Second stage load	Saturation
MP7 & MP8	210 µm/13.3 µm	Nulling resistor	Linear

Table 3.4 Capacitance value

Capacitors	Capacitors value	function
C1 & C2	5 pf	Load capacitances
C3 & C4	5 pf	Miller compensation capacitances
C5 & C6	0.05 pf	Feed forward capacitances

Table 3.5 Biasing voltages

Voltage Port	Voltage value(Volt)
V_{incm}	1.65
Vb0	0.7
Vb1	2.25
Vb2	2.05
Vb3 , Vb4 & Vb5	2.45

The primary trade off for this circuit is given in Table 3.6.

Table 3.6 Primary design trade's off for our topology.

Parameter to improve	Method to improve	Potential tradeoffs/draw backs
DC gain	Increase L, maintain W/L	Feedback factor degraded
	Increase g_m, same L same I_{ds}	Reduce V_{dsat}
	Reduce I_{ds} at same g_m	Slew rate degrades
Dynamic range	Increase C_C	Worse slewing, much more current, lower UGB
	Increase C_L	Reduce phase marin
	Increase g_{m1}	Reduce V_{dsat}
	Decrease g_{m3}	Increase first stage swing
Unity gain bandwidth	Reduced C_C	More noise, lower dynamic range
	Increase C_C	Reduced UGB

3.8 Layout of Op-Amp

Analog layout demand many more layout precautions so as to minimize effects such as crosstalk, mismatches, noise etc. The main problems of layout for analog ICs are device matching and unwanted parasitic reduction. Sometimes chip area may also be a concern. For matching, the techniques are common-centroid and interdigital, which can be used separately or in combination, as well as dummy devices and device unitization. If there are no parasitic, then there is no noise coupling. The parasitics reduction techniques include, shield, guard ring, long distance between noisy digital circuitry etc.

3.8.1 Issues in analog layout

1. Matching of devices

Device mismatch is too often treated as part of the black art of analog design. Random device mismatch plays an important role in the design of accurate analog circuits. The device mismatch is due to number factors like local process variation, global lithographic

variations, local lithographic variations and process gradients. These factors affect all devices transistors, resistor, capacitors, and therefore similar techniques can be used to match all elements.

Matching improves with increasing device area. And accuracy requirements impose a minimal device area. Use of transistor fingering for large and critical transistors is always beneficial. In fingering the transistor is "fingered" into multiple transistors that are connected in parallel. The folded transistors reduce the source/ Drain junction area and the gate resistance. The gate resistance can be reduced by decomposing the transistor into more parallel fingers. There is an advantage with an even number of fingers; the active capacitance is less, because the drain region is surrounded with gate poly instead of field.

The large transistors are breaks in number of small transistors in parallel. This also decreases the physical size of the device, and thus can provide a more compact layout. Minimum size will usually provide a minimum in terms of parasitic capacitance, but still, this may not provide the optimal device for a given application. For example, an application that is more sensitive to gate resistance may warrant a non-optimal device size, in terms of parasitic capacitance. Lower gate resistance is obtained by smaller finger width. This increases the overall number of fingers and therefore increases the junction capacitances C_{sb} and C_{db}.

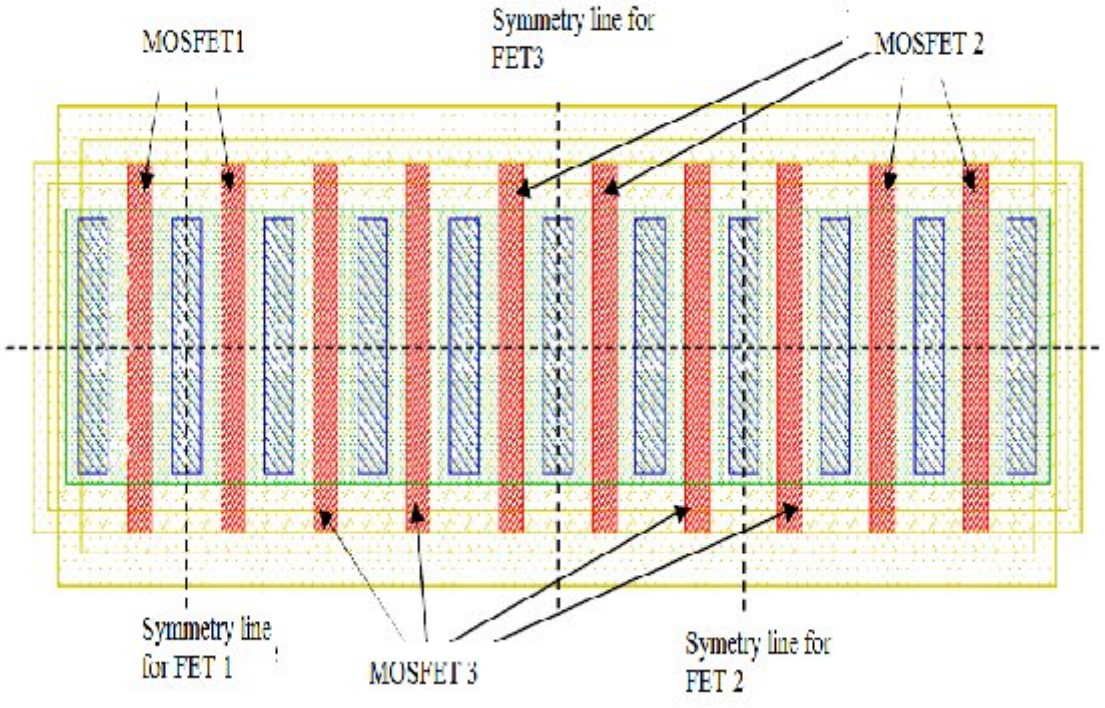

Figure 3.9 Interdigitated MOSFET's [27]

Since MOSFET's allow device folding, many devices with the same finger width can be, "interdigitated" with one another. The only requirement for interdigitating devices is that these devices share source terminals, drain terminals, or source and drain terminals. These compact, interdigitated devices provide better matching for both process and thermal gradients. When matched signals or currents are needed, precision device matching is required. For example, current mirrors and differential pairs. In many cases, these structures can provide symmetry along two separate axes, completely alleviating the affects of linear gradients as shown in figure 3.9.

An interdigitation pattern that will minimize source/drain parasitics by placing two same devices gates back-to-back.

It should also be pointed out that, although the compound device is repetitive, the end devices do not match the inner devices and therefore device mismatch can exist due to processing gradients. In order to alleviate this problem, dummy devices should be added to the structure.

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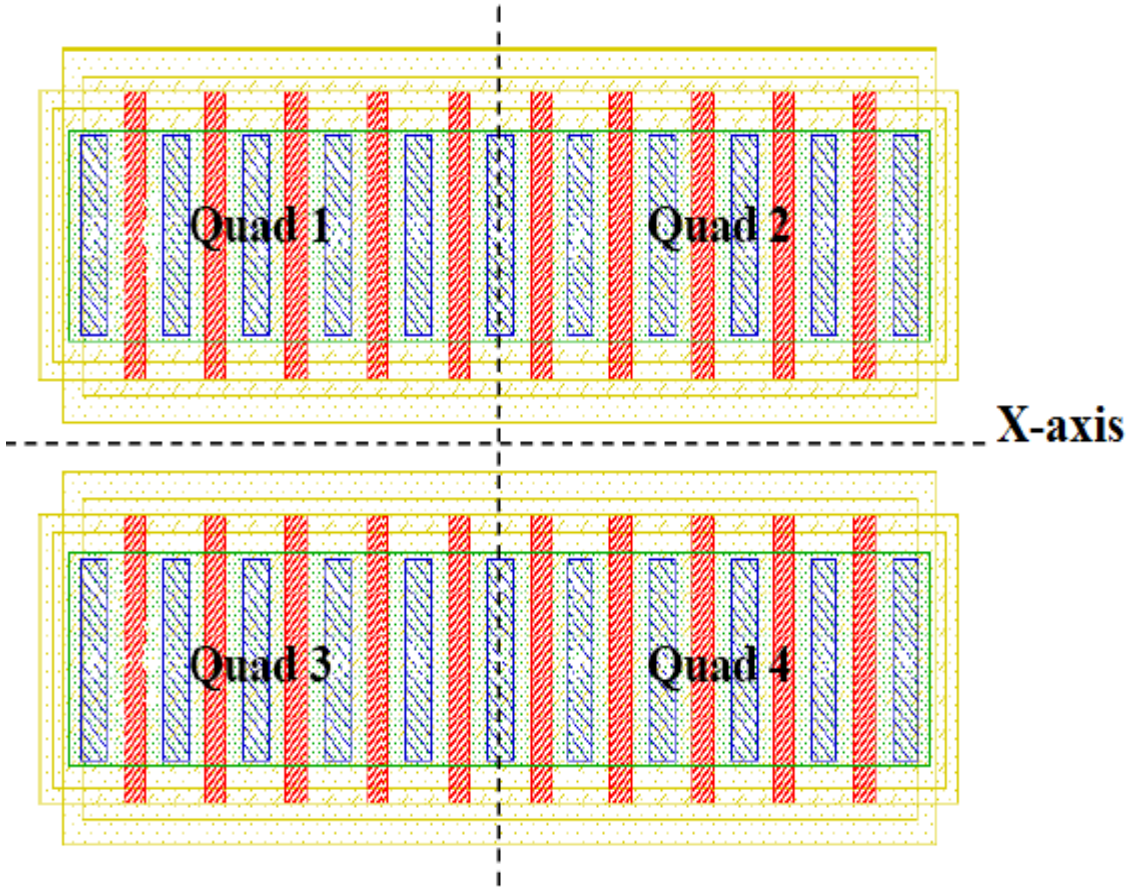


Figure 3.10 Basic structure of common centroid layout[27]

While on the subject of matching, it should also be mentioned that metal routing over transistors might affect device matching. Such routing can cause threshold voltage mismatch as well as transconductance mismatch. Therefore, it is recommended that routing over transistors be avoided. If such routing cannot be avoided, the routing over symmetric devices should be made symmetric as well, and if possible, higher metal layers should be used.

In order to consistently provide symmetry along two axes, a layout technique called a, "common-centroid" can be used. Figure 3.10 shows how such a layout provides two axes of symmetry. Typically, this form of layout is used for precise matching of only two devices. The method can be extended to more devices; however, the routing for such a compound device becomes very cumbersome some golden rules for device matching are

- Use of the same W and L and vary M (takes out ΔW and ΔL effects, M is number of fingers)
- Use M's that are even.
- Use Common-Centroid, or nearly Common-Centroid, layout.
- Use dummy transistors at the ends of the row (takes out poly etch loading and mask misalignment effects)
- Use plenty of substrate and well taps.
- Route currents a long way, not voltages - IR drops can cause big mismatches.

2. Noise: Noise is important in all analog circuits because it limits dynamic range. In general there are two types of noise, random noise and environmental noise. Random noise refers to noise generated by resistors and active devices in an integrated circuit; environmental noise refers to unwanted signals that are generated by humans. Two common examples of environmental noise are switching of digital circuits and 60 Hz 'hum'. In general, random noise is dealt with at the circuit design level. However they are some layout techniques which can help to reduce random noise. Multi-gate finger layout reduces the gate resistance of the poly-silicon and the neutral body region, which are both random noise sources. Generous use of Substrate plugs will help to reduce the resistance of the neutral body region, and thus will minimize the noise contributed by this resistance. Environmental noise is also dealt with at the circuit level. One common design technique used to minimize the effects of environmental noise is to employ a 'fully-differential' circuit design, since environmental noise generally appears as a common-mode signal. However Substrate plugs is also very useful for reducing substrate noise,

which is a particularly troublesome form of environmental noise encountered in highly integrated mixed-signal systems and Systems-On-a-Chip (SOC). Substrate noise occurs when large amount digital circuits are present on a chip. The switching of a large number of circuits discharges large dynamic currents to the substrate, which cause the substrate voltage to 'bounce'. The modulation of the substrate voltage can then couple into analog circuits via the body effect or parasitic capacitances. Substrate plugs minimizes substrate noise because it provides a low impedance path to ground for the noise current.

Issues that are important in digital circuits are still important in analog layout. Foremost among these is parasitic aware layout. It is important to minimize series resistance in digital circuits because it slows switching speed. Series resistance also slows analog circuits, plus it introduces unwanted noise. Parasitic capacitance is avoided in digital circuits because it slows switching speed and/or increases dynamic power dissipation. Stray capacitance has the same effect in analog circuits (bias current must be increased to maintain bandwidth and/or slew rate when extra load capacitance is present) plus it can lead to instability in high gain feedback systems.

3.9 Complete layout of Op-Amp

From figure 3.9 and table 3.2, the transistors are divided into fingers as given in table 3.7.

Table 3.7 Transistors with aspect ratio and number of finger

Transistor	**Aspect ratio (in schematic)**	**Number of finger**	**Aspect ratio (of each finger)**
M1 & M2	18.9µm/1.4µm	6	3.2µm/1.4µm
M3 & M4	14µm/1.4µm	4	3.5µm/1.4µm
MN6 & MN7	7.7µm/1.4µm	2	3.9µm/1.4µm
MN8 & MN9	5.95µm/1.4µm	2	3µm/1.4µm
MP1 & MP2	56µm/1.4µm	8	7µm/1.4µm
MP3 & MP4	112µm/1.4µm	8	14µm/1.4µm
MP5 & MP6	287µm/1.4µm	10	28.7µm/1.4 µm
MP7 & MP8	210µm/13.3µm	6	35µm/13.3 µm

Since MN5 have aspect ratio of 694.75µm /1.4µm is very big transistor, the number of calculated finger is 70, which is too large to make on single level and also consume large layout area and make routing complex. That's why we use here stacking of transistor *i.e* one above the other. For number of fingers=70, we use 5 stacks of 10 fingers and each

finger of aspect ratio of 14µm/1.4µm. As, 694.75µm/1.4µm ≈ 5stack * 10 finger * 14µm/1.4 µm. Stack layout is shown in figure 3.11.

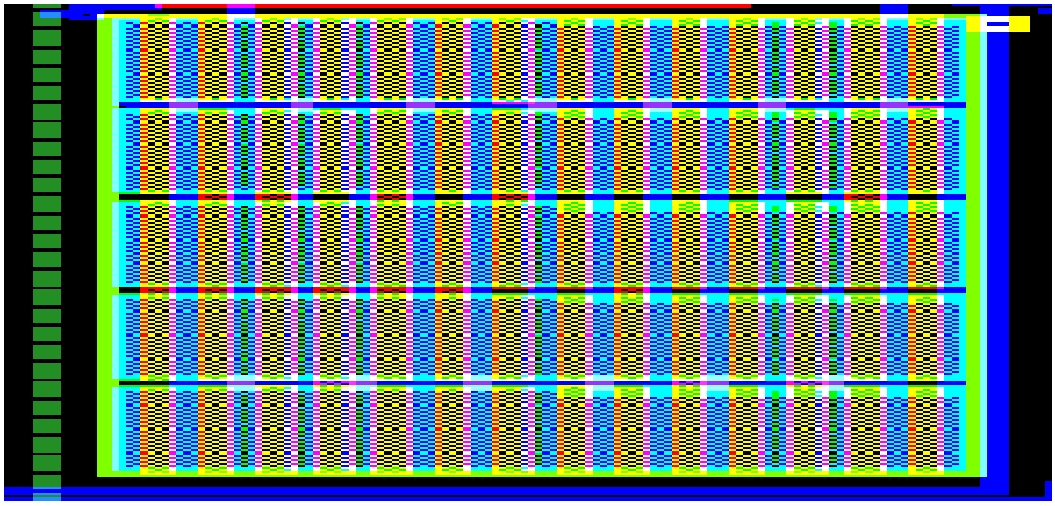


Figure 3.11 Stack layout design of MN5

The complete layout of the op-amp design is shown in figure 3.12

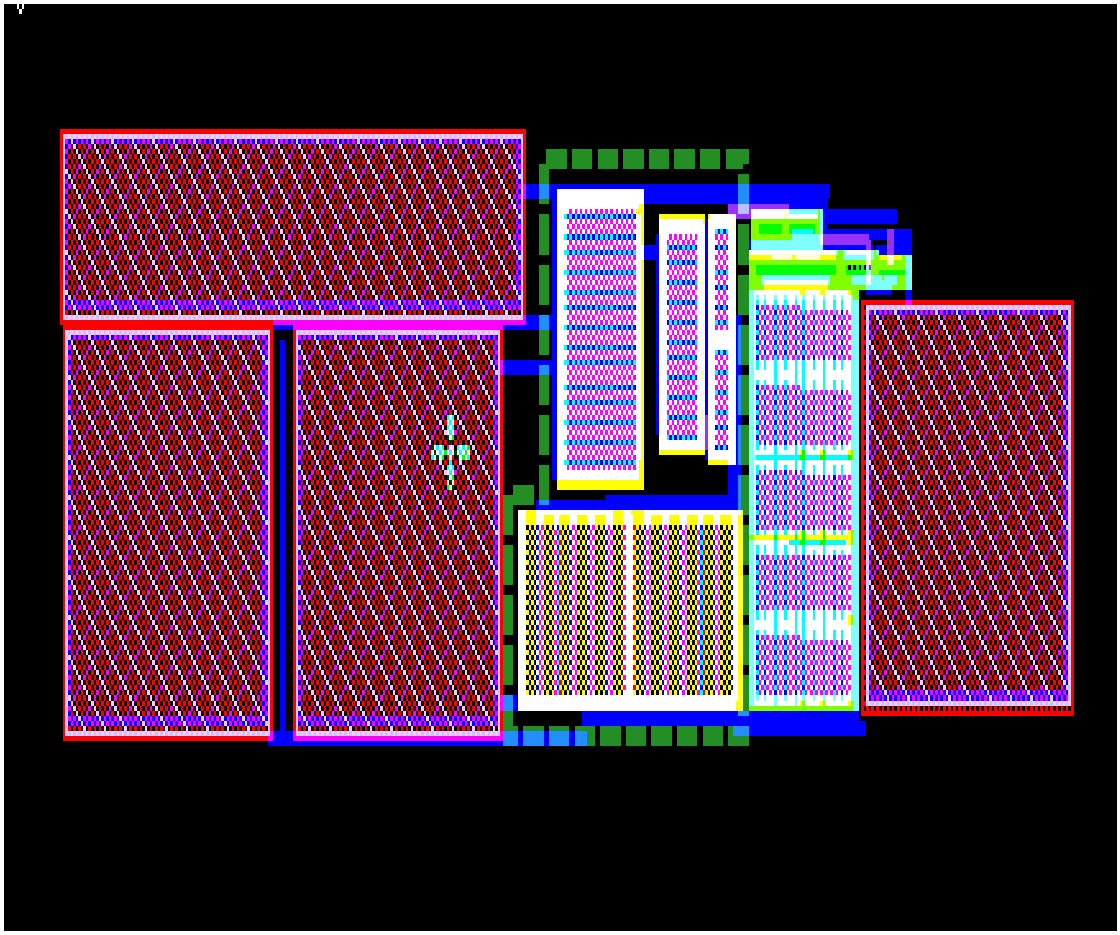


Figure 3.12 Complete layout of fully differential op-amp

LVS Report

This design is DRC clean, and layout of the circuit is matched with schematic, both DRC and LVS are verified by the Calibre.

Figure 3.13 shows there is LVS matching.

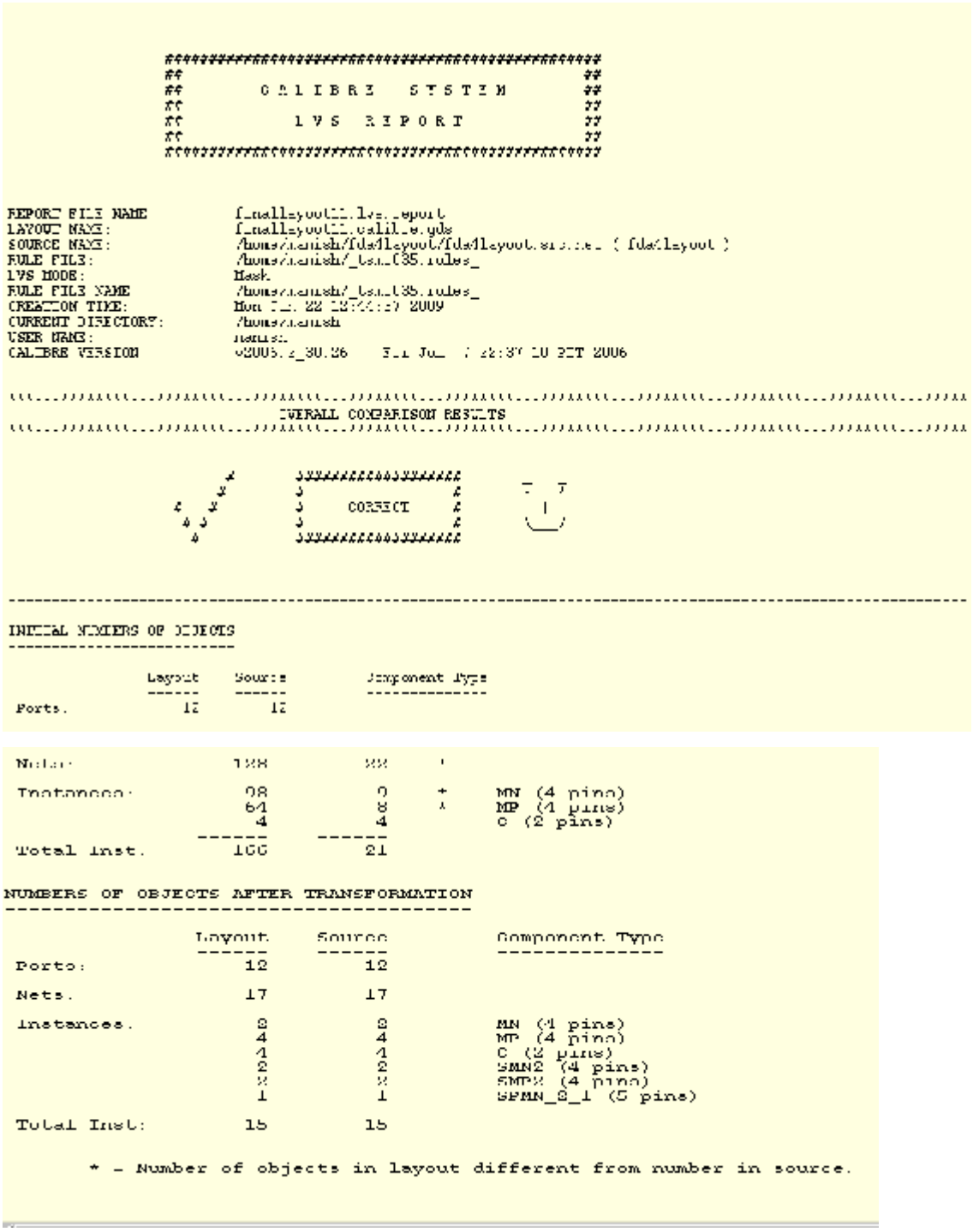


Figure 3.13 Complete LVS Report

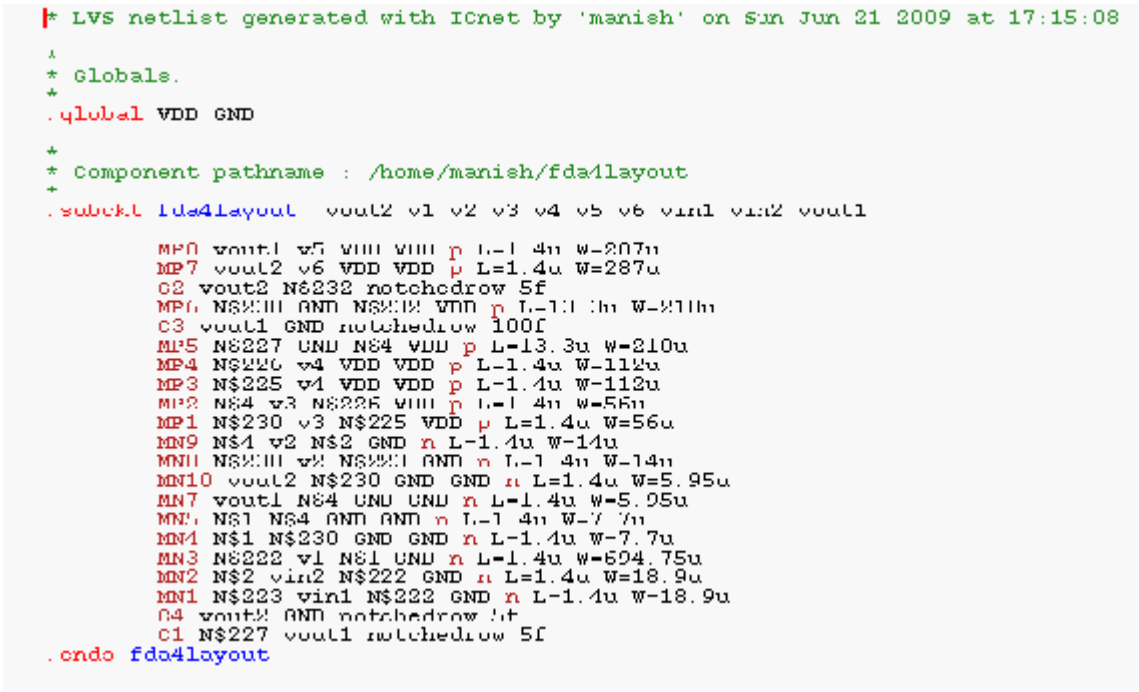


Figure 3.14 LVS netlist report

CHAPTER 4

SIMULATION RESULTS

In this chapter the schematic of the circuit has been tested for various parameters of operational amplifier. The amplifier is powered by supply voltage of 3.3V. The fully differential CMOS Op-Amp has been designed and simulated on tsmc 0.35µm technology.

This chapter dived in four sections:

- Schematic simulations
- Post layout simulations
- Process corner simulations
- Monte Carlo simulations

4.1 Schematic Simulations

4.1.1 AC Response

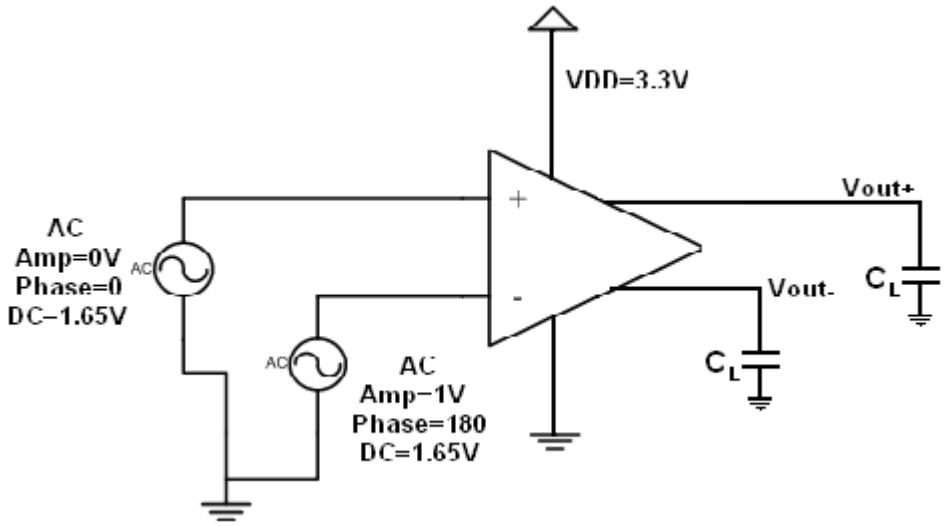


Figure. 4.1: Test setup for AC response of the op-amp

In figure 4.2, a Bode and phase plot for 3.3V, 27°C and C_L= 5pf is shown. As can be seen, the open loop gain is 86.0217dB, and a phase margin is 50.018°. The unity gain bandwidth is 270.455 MHz and f_{-3db} bandwidth is 6.105 KHz.

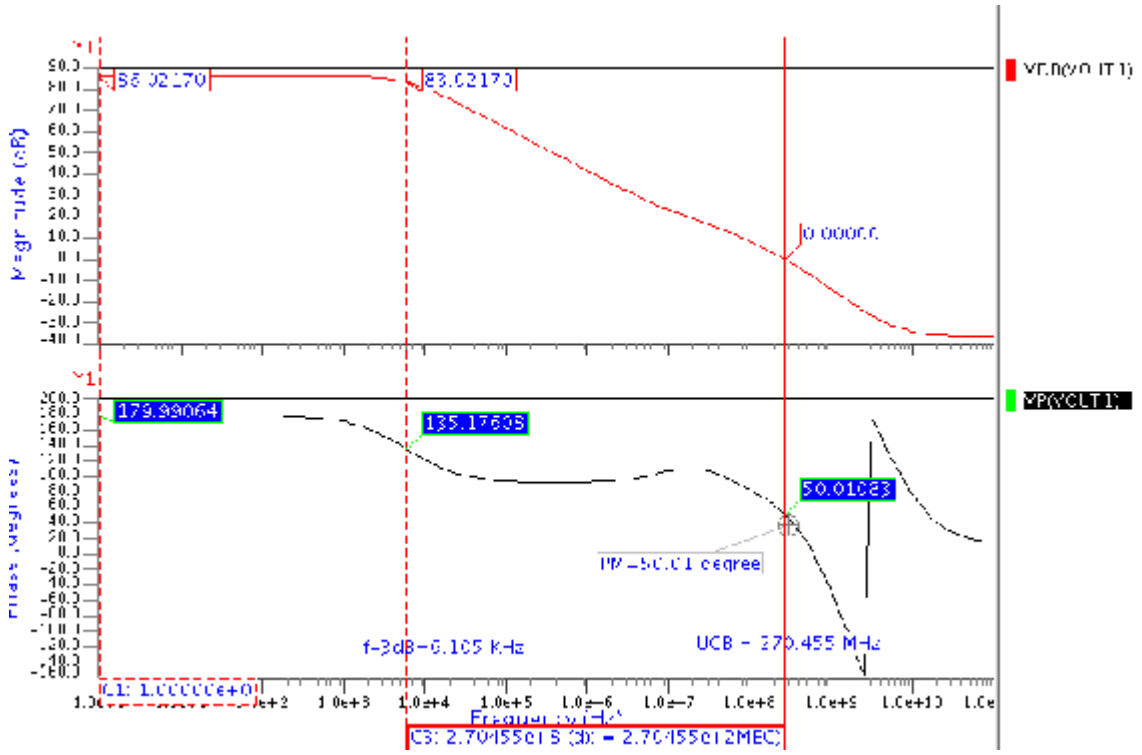


Figure 4.2(a) Frequency response plot with C_L=5pf

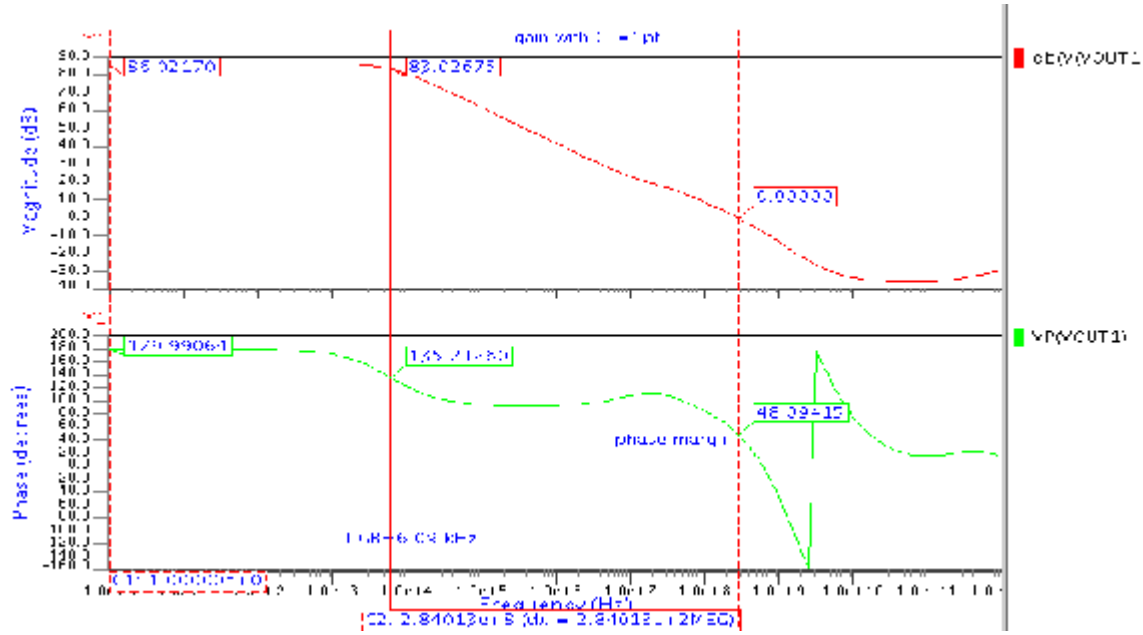


Figure 4.2(b) Frequency response plot with C_L=1pf

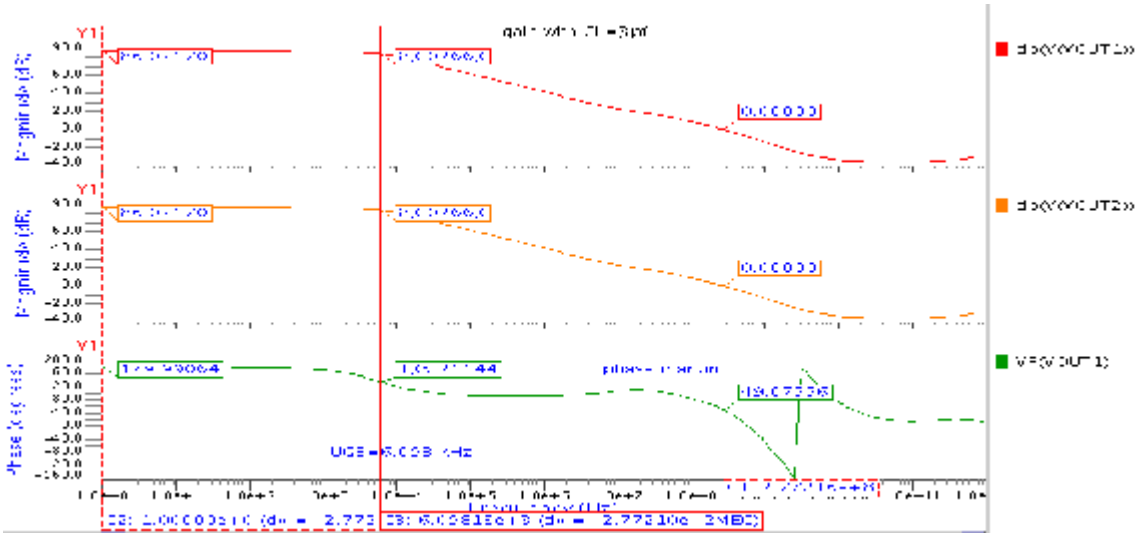


Figure 4.2(c) Frequency response plot with C_L=3pf

Table 4.1 shows the effect of load variation on AC response.

Table 4.1 AC result due to load capacitance variation

Capacitor (pF)	DC gain(dB)	UGB(MHz)	f_{-3dB}(KHz)	Phase margin
1	86.02	284.013	6.09	48.09°
3	86.02	277.21	6.098	49.07°
5	86.02	270.455	6.105	50.01°

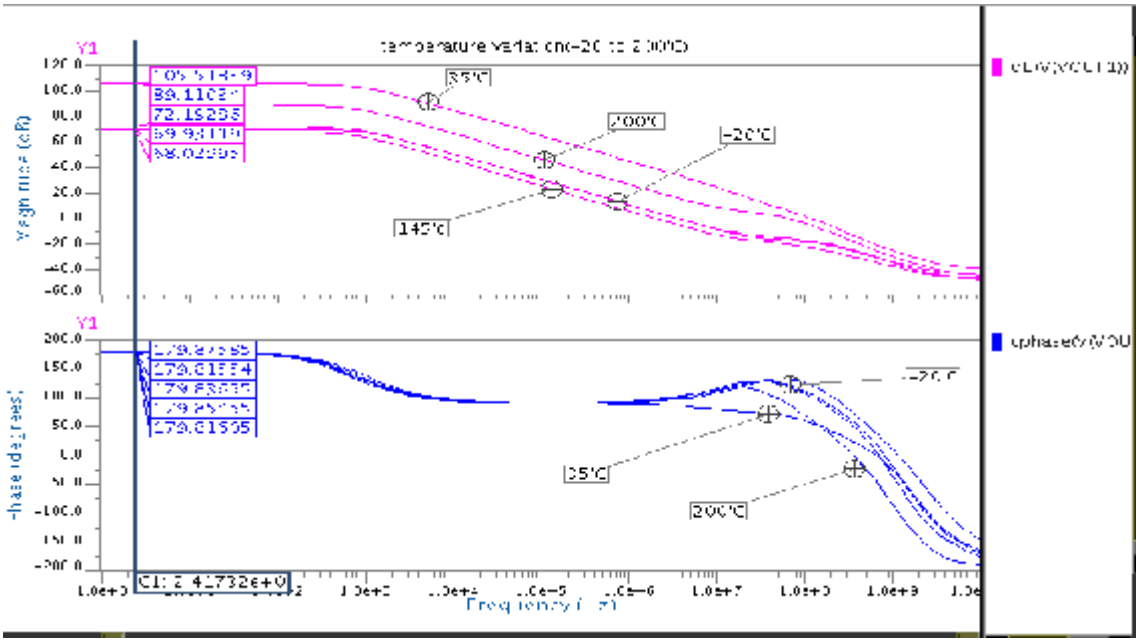


Figure 4.3 Frequency responses with temperature variation

The temperature has been varied from -20deg to +200deg centegrade. Increasing temperatures tend to reduce the gain of the circuit. The increasing temperature also reduces the UGB of the opamp.

4.1.2 Common Mode Rejection Ratio

In order to know the CMRR of the opamp we need to know the differential gain as well as the common mode gain of the opamp and the CMRR is obtained by A_d(dB)-A_c(dB). The resulting CMRR response is shown in the figure 4.5.

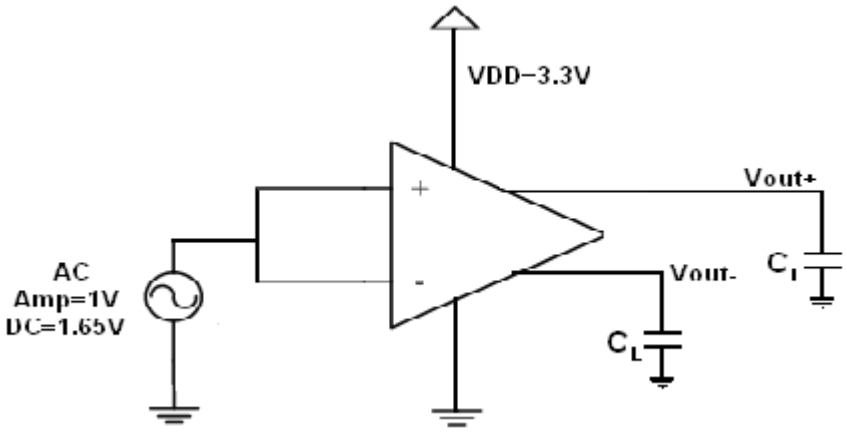


Figure 4.4 Test setup for Common Mode response

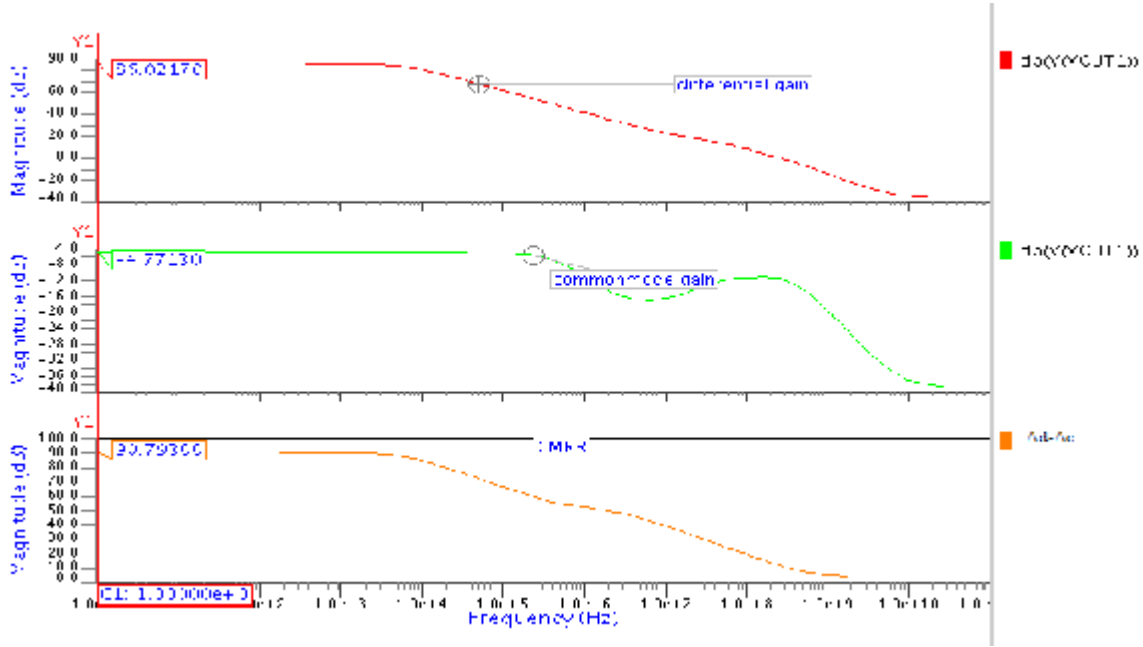


Figure 4.5 CMRR at 27°C with C_L=5pf

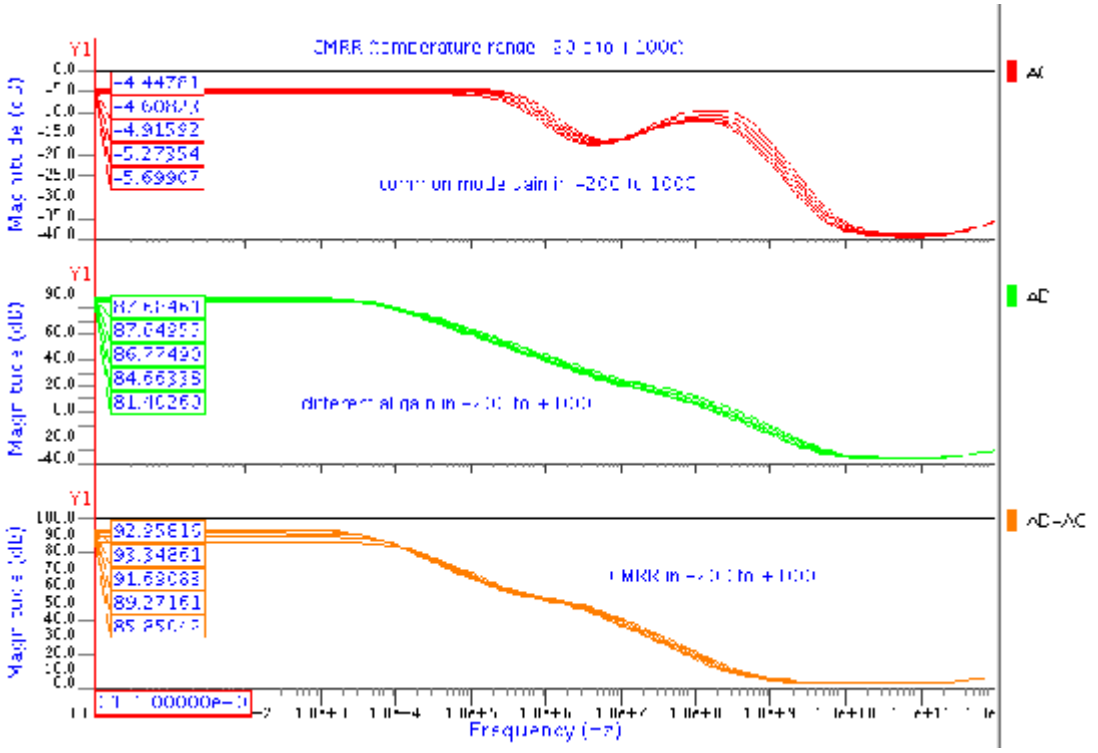


Figure 4.6 CMRR with temperature variation

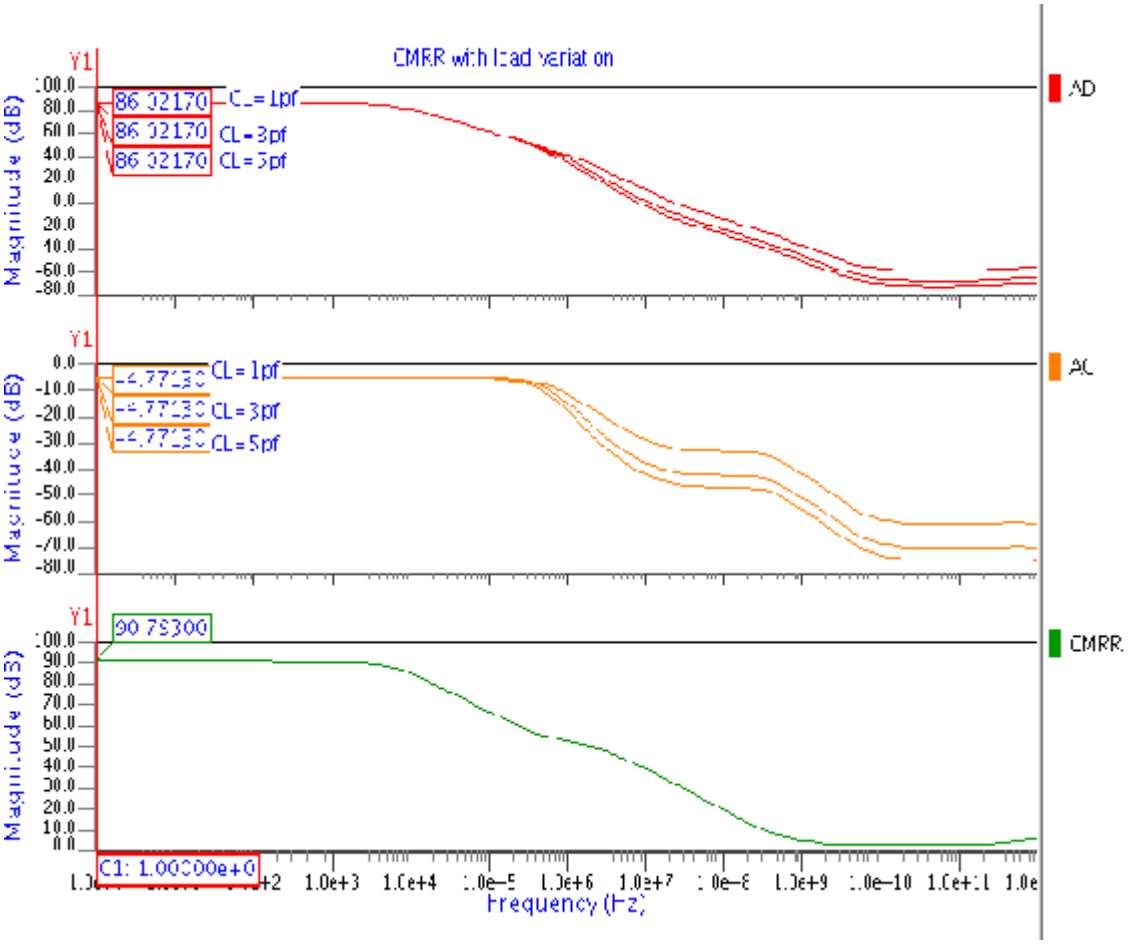


Figure 4.7 CMRR with load capacitance variation

Table 4.2 CMRR with load capacitance variation

Capacitor(pf)	CMRR(dB)
1	90.793
3	90.793
5	90.793

The CMRR with load variation is given in Table 4.2. It concludes that CMRR is independent of load variations.

4.1.3 Power Supply Rejection Ratio

PSRR was measured by placing a 1V AC signal on the power supply. PSRR is equal to the ratio of the AC signal at the output node to the AC signal on V_{DD}.

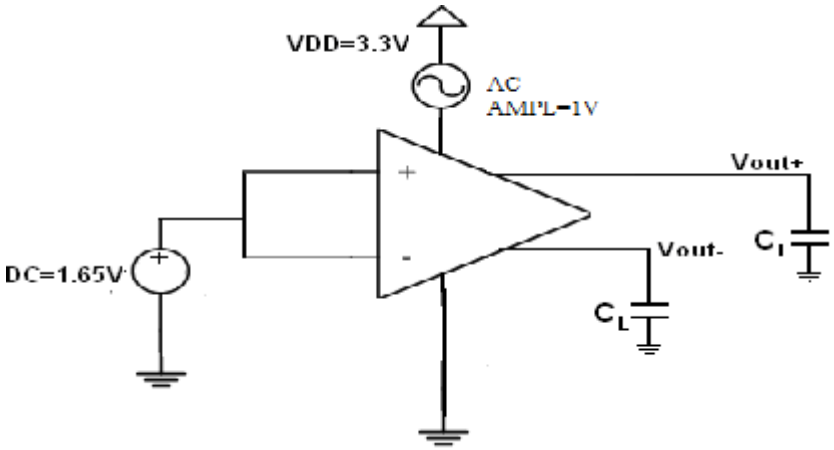


Figure 4.8 Test setup for PSRR

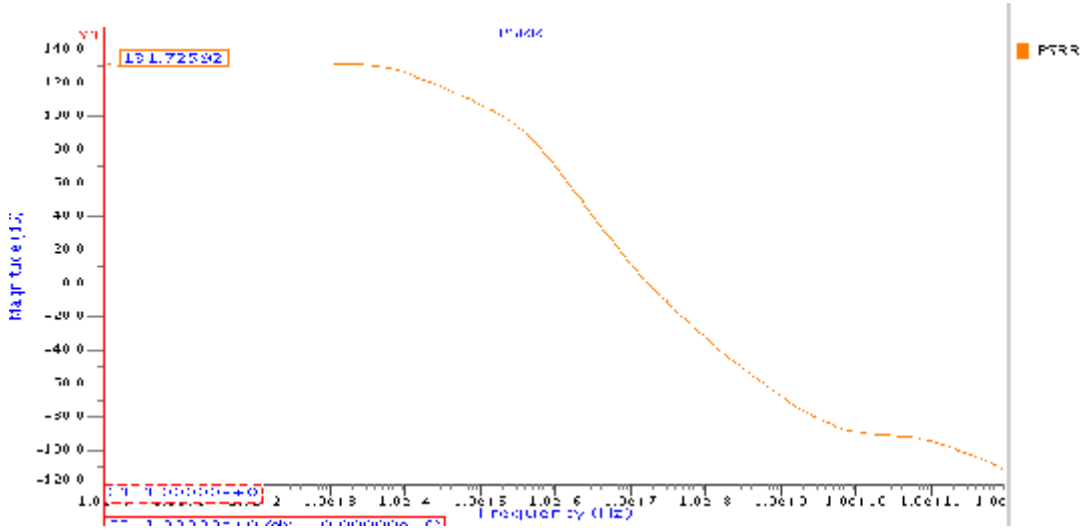


Figure 4.9 PSRR of op-amp

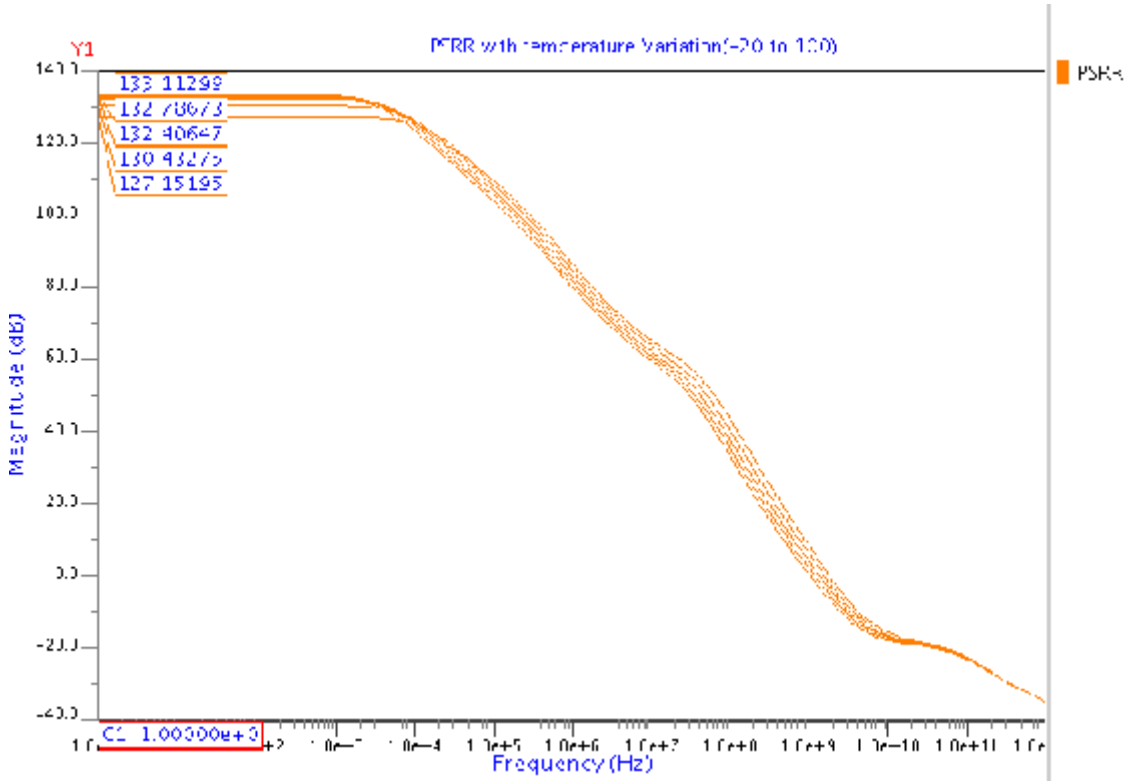


Figure 4.10 PSRR with temperature variation

The PSRR of the fully differential op-amp is 132.725 dB. The effect of temperature on PSRR is given in figure 4.10. It shows that there is a very little variation in PSRR due to variation in temperature. As temperature increases PSRR decrease.

4.1.4. Input Common Mode Range (ICMR)

This test is per formed to test the offset voltage and the input common mode range of the opamp that is the range of opamp for which there is a linear relationship between input and the output.

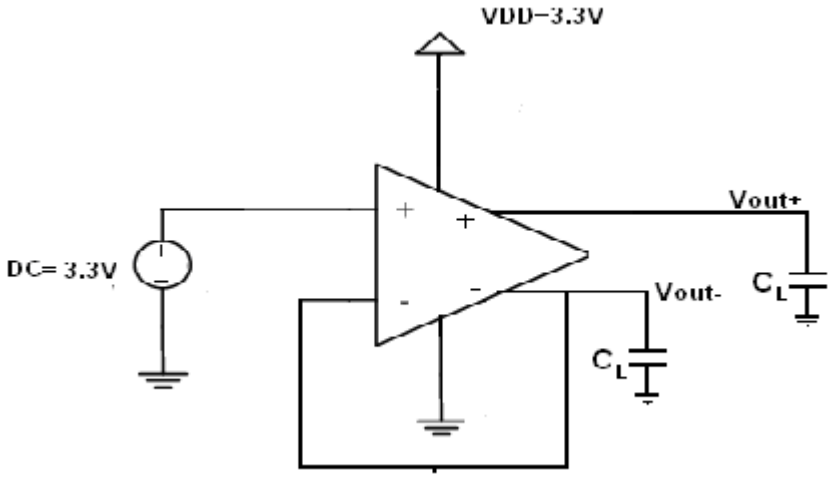


Figure 4.11 Test setup for ICMR

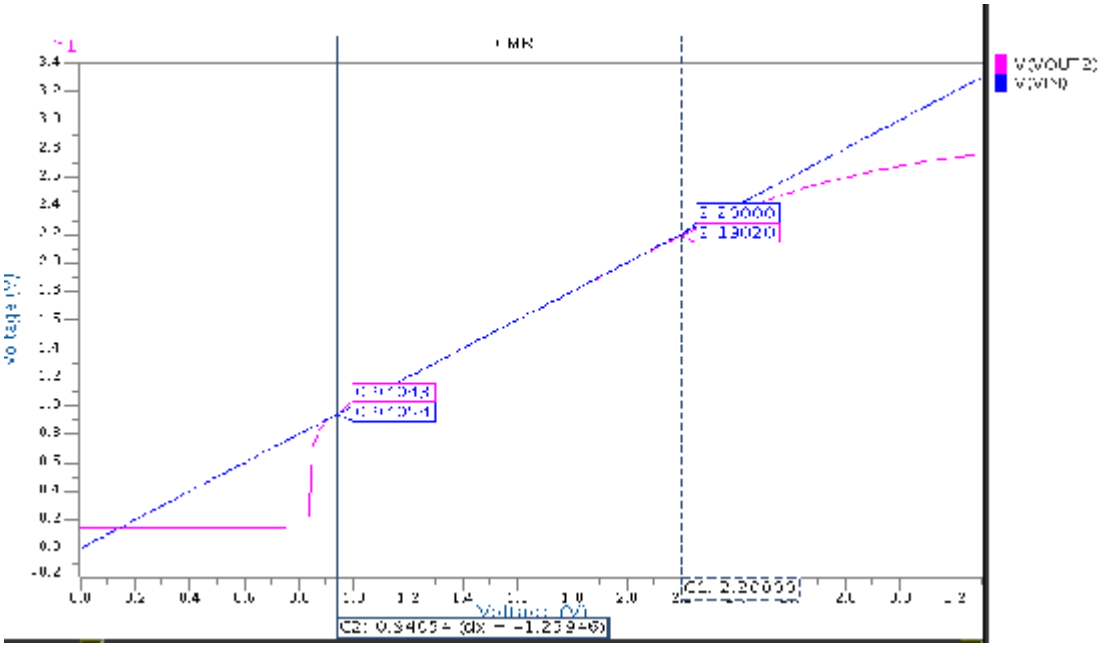


Figure 4.12 ICMR of op-amp

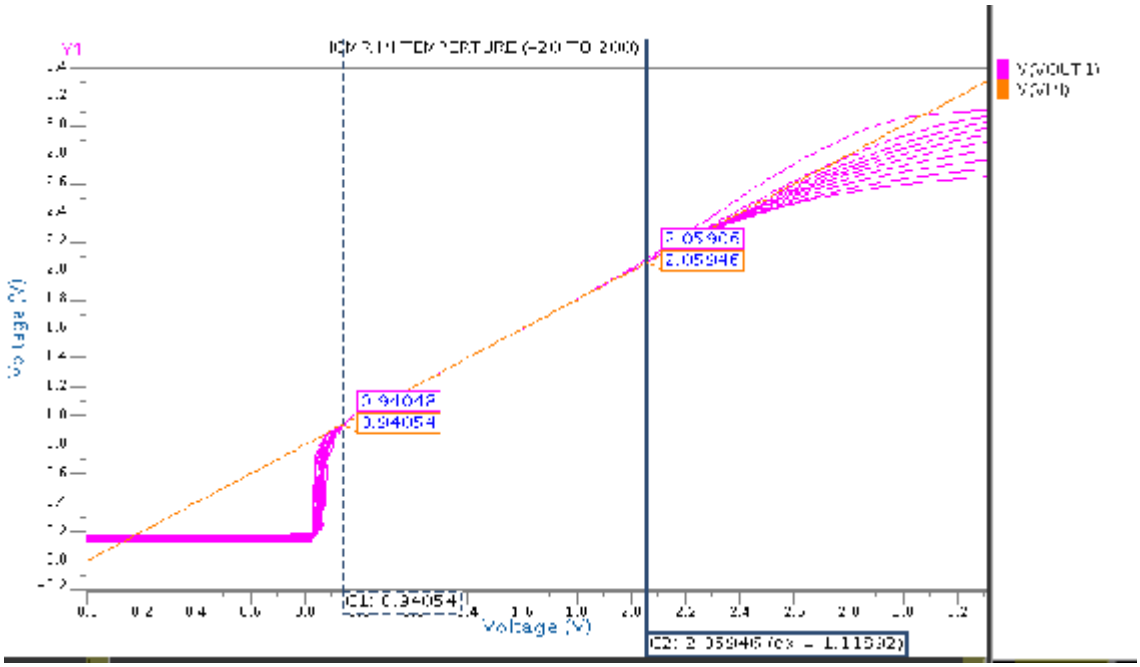


Figure 4.13 ICMR with temperature variation

From ICMR we also find the offset voltage i.e the output voltage of op-amp when input is zero. In our case offset is 0.17V.

The output voltage varies linearly with input voltage for a voltage range of 0.94V to 2.2V so this is called the ICMR range of the op amp.

ICMR with temperature variation is shown in figure 4.13. With rise of temperature ICMR reduces.

4.1.5 Transient Response

For observing the transient sinusoidal response of the op-amp the test setup of figure 4.14 is used. In this setup sinusoidal signals are applied to the two inputs and the effective value of input signal is the difference of the voltage at the two terminals. DC potential is also applied along with the sinusoidal signal in order to provide the bias voltage to the input transistors. The output is taken differentially from the two complementary outputs.

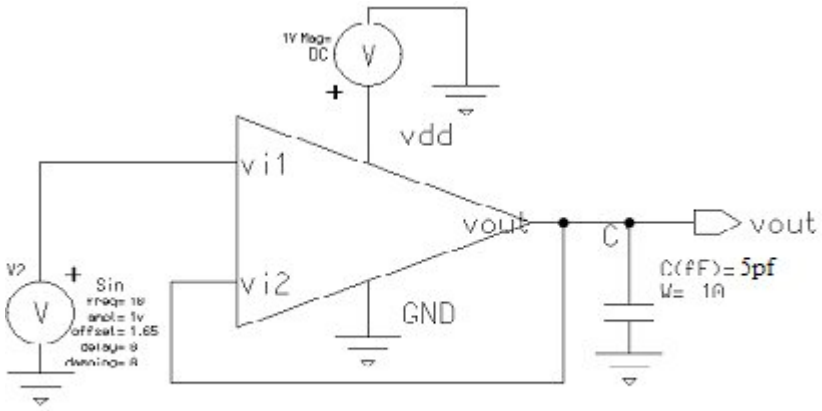


Figure 4.14 Schematic for the sinusoidal transient response

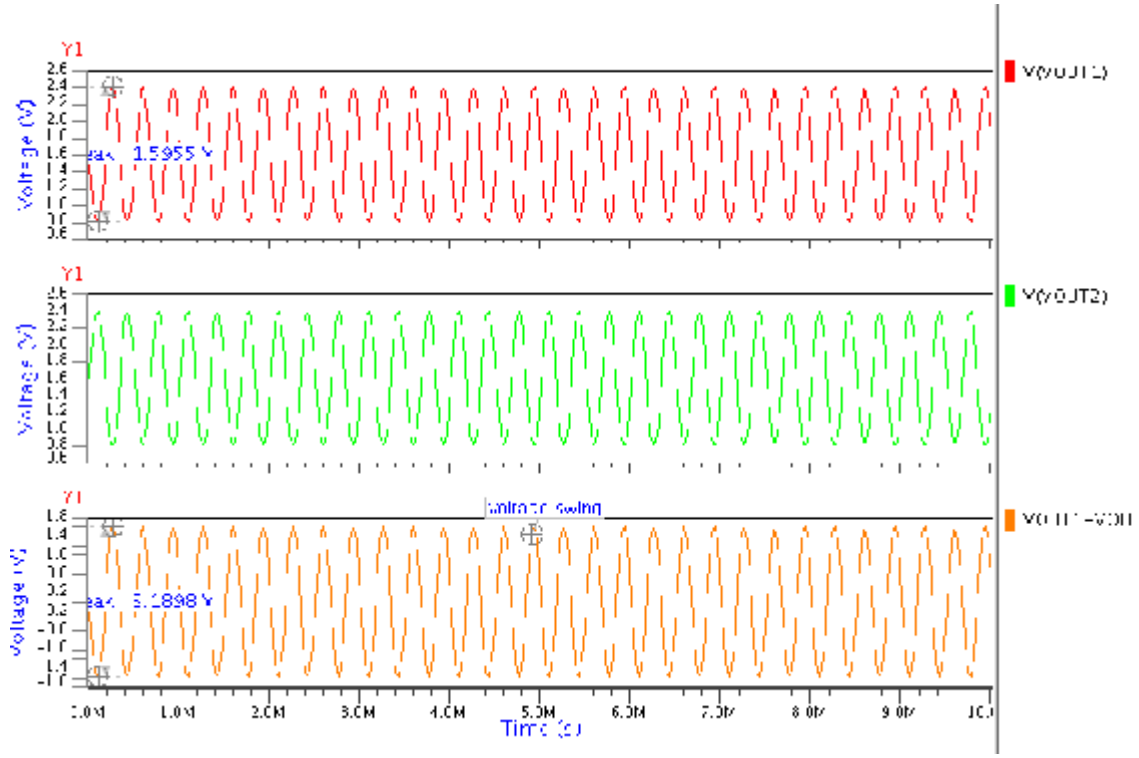


Figure 4.15 Sinusoidal transient differential outputs

From figure 4.15, it is measure that the complete voltage swing (peak-to-peak) is 3.1898V.

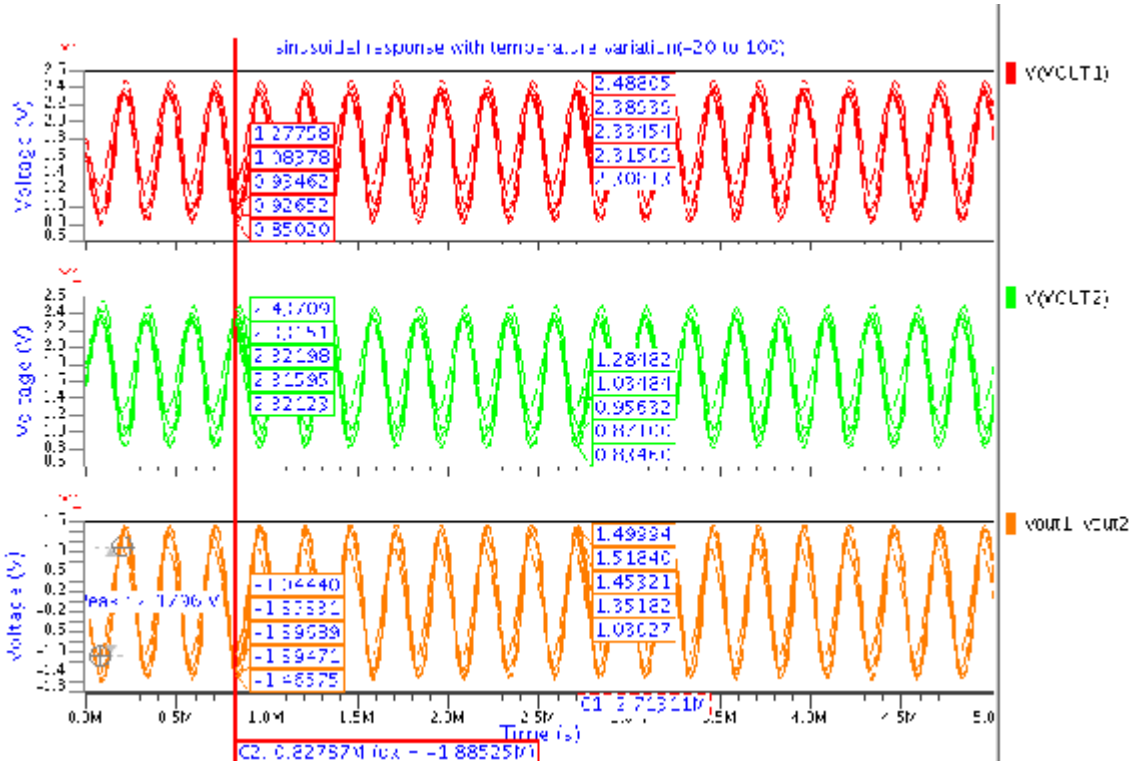


Figure 4.16 Sinusoidal transient differential outputs with temperature variations

4.1.6 Transient Step Response

In Figure 4.17, a step from ground to V_{DD} is applied at the input with unity feedback configuration.

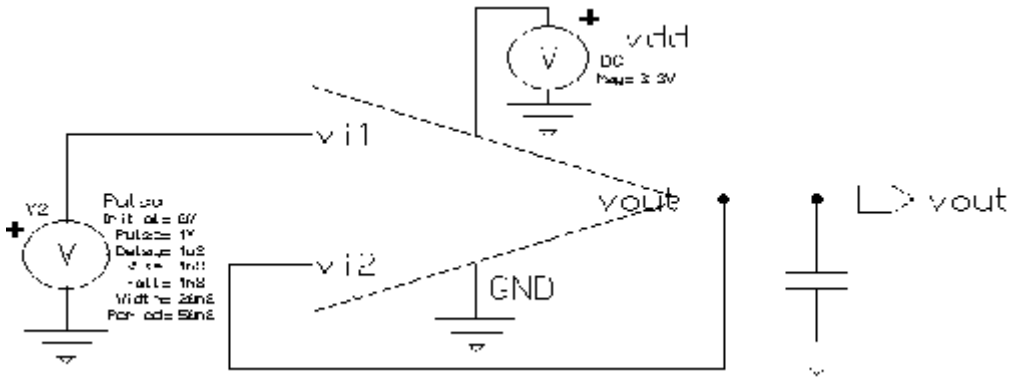


Figure 4.17 Schematic for the simulation and measurement of the slew rate

The slew rate of op-amp is 40.585V/µS for rising edge of pulse and 19.406V/ µS for falling edge of the pulse.

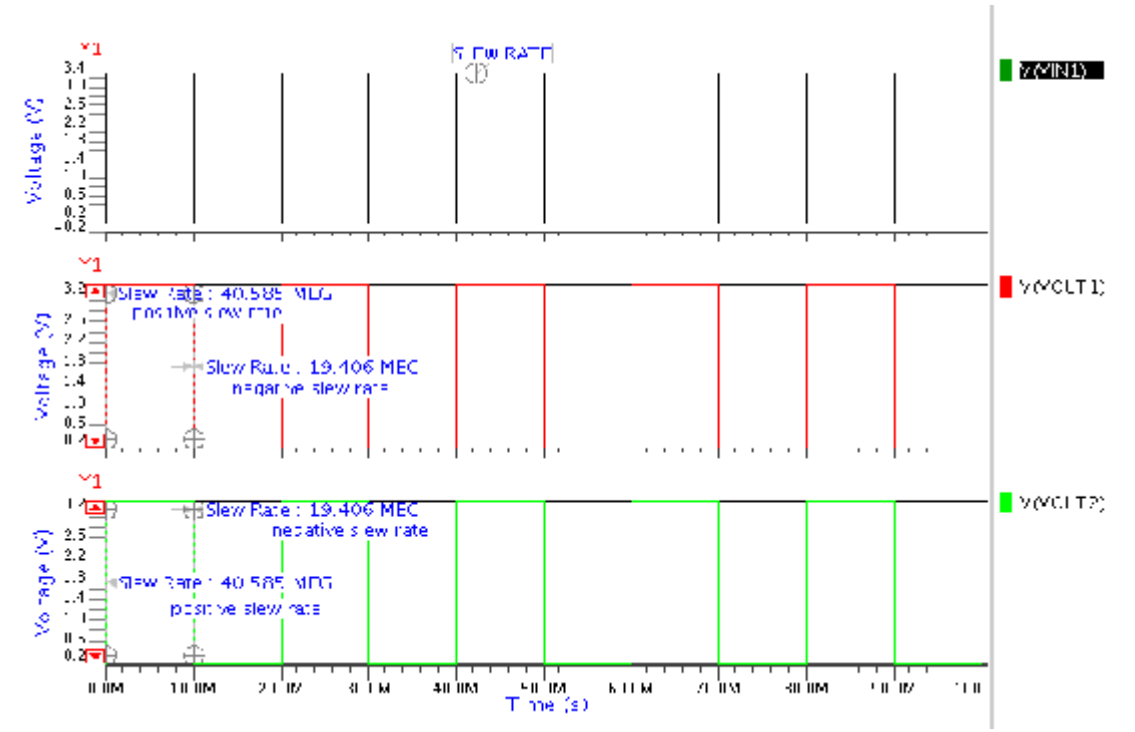


Figure 4.18 Transient pulse response of op-amp for slew rate measurement

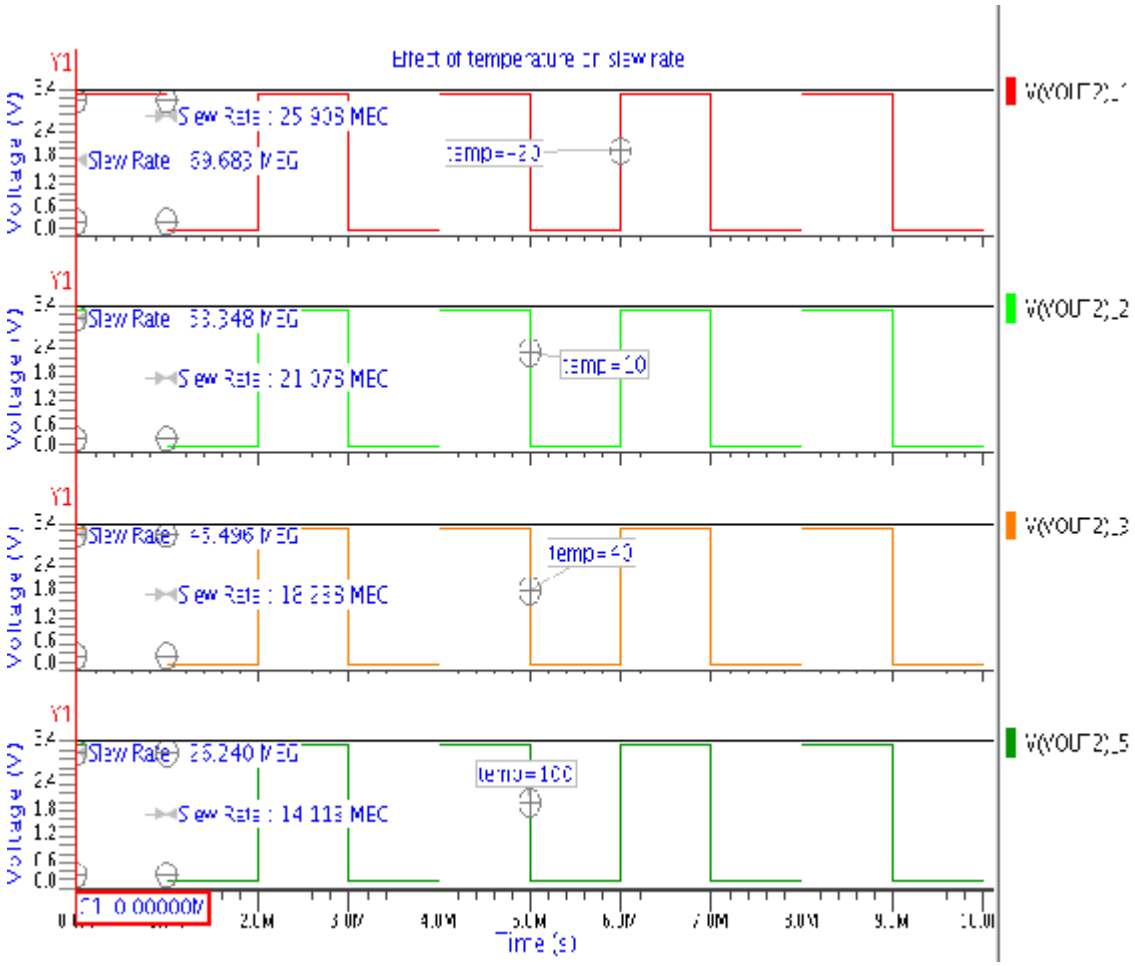


Figure 4.19 Effect of temperature on slew rate

Table 4.3 Show the effect of temperature on slew rate

Temperature (°C)	Slew rate(V/µS) (+ve)
-20	69.683
10	53.348
27	40.585
40	45.496
100	26.240

4.1.7 Settling Time

Settling time is length of the time in which the response of the step input get settle within certain tolerance of its final value.

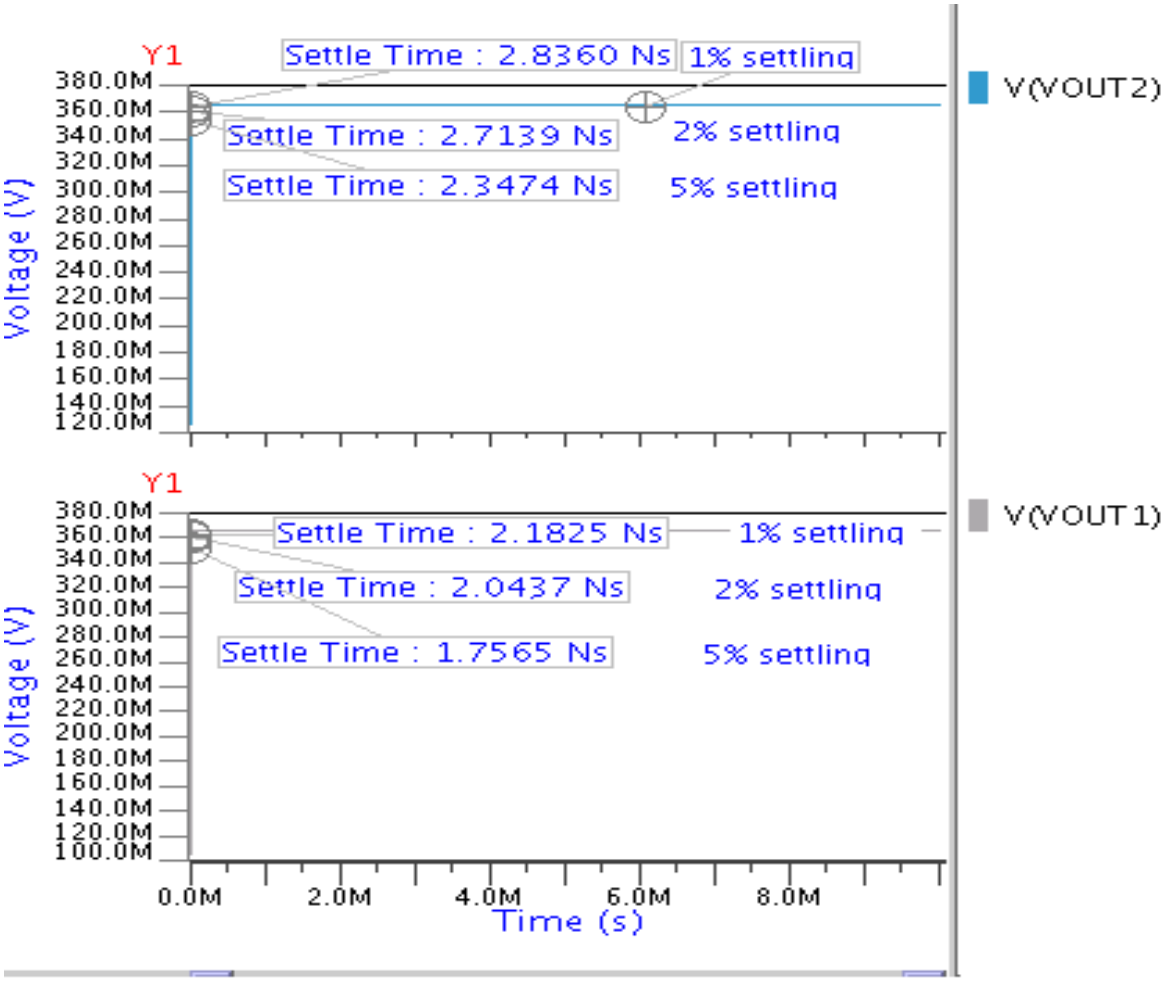


Figure 4.20 Settle time at various tolerances level of differential output

Table 4.4 Settling time of differential outputs

Tolerance %	Vout1	Vout2
1%	2.185 Ns	2.836 Ns
2%	2.0437 Ns	2.7139 Ns
5%	1.7565 Ns	2.3474 Ns

Table 4.3 shows the settling time of differential outputs at various tolerance levels.

4.1.8 Output Dynamic Range of Op-Amp

The dynamic range is a measure of the signal to noise ratio. It requires high swing and low noise.

First we determined the maximum total output noise we could tolerate for a given output swing. This translates directly into determining the size of the compensation capacitor and feedback capacitor to give the desired dynamic range. We initially assumed that we would have a single-ended output swing of 1.65V (VDD -2V_{DSAT} ≈ 1.65V), which corresponds to a differential swing of 3.3V peak-to-peak.

The maximum voltage swing essentially voltage rail minus the minimum voltage drop across series FET's.

The output dynamic range is specified as

$$DR = 10\log\frac{P_{Peak-signal}}{P_{noise}} \tag{4.1}$$

$$\text{Thus, } \frac{P_{Peak-signal}}{p_{noise}} = \frac{V_{o,swing}^2}{V_{on}^2} \tag{4.2}$$

where $P_{Peak-signal}$ is signal power (peak-peak) and

P_{noise} is output noise power.

The noise output voltages of op-amp at different frequencies are given in figure 4.21 and the output swing at corresponding frequencies are given in figure 4.22.

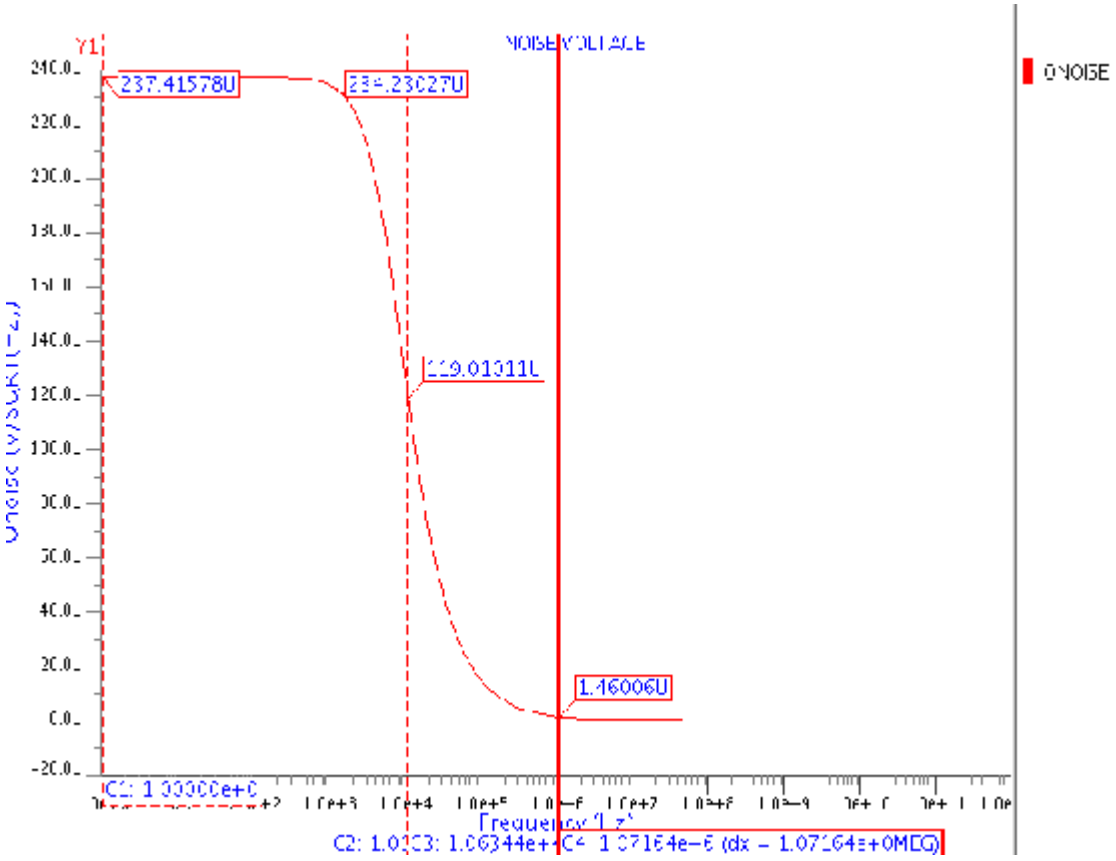
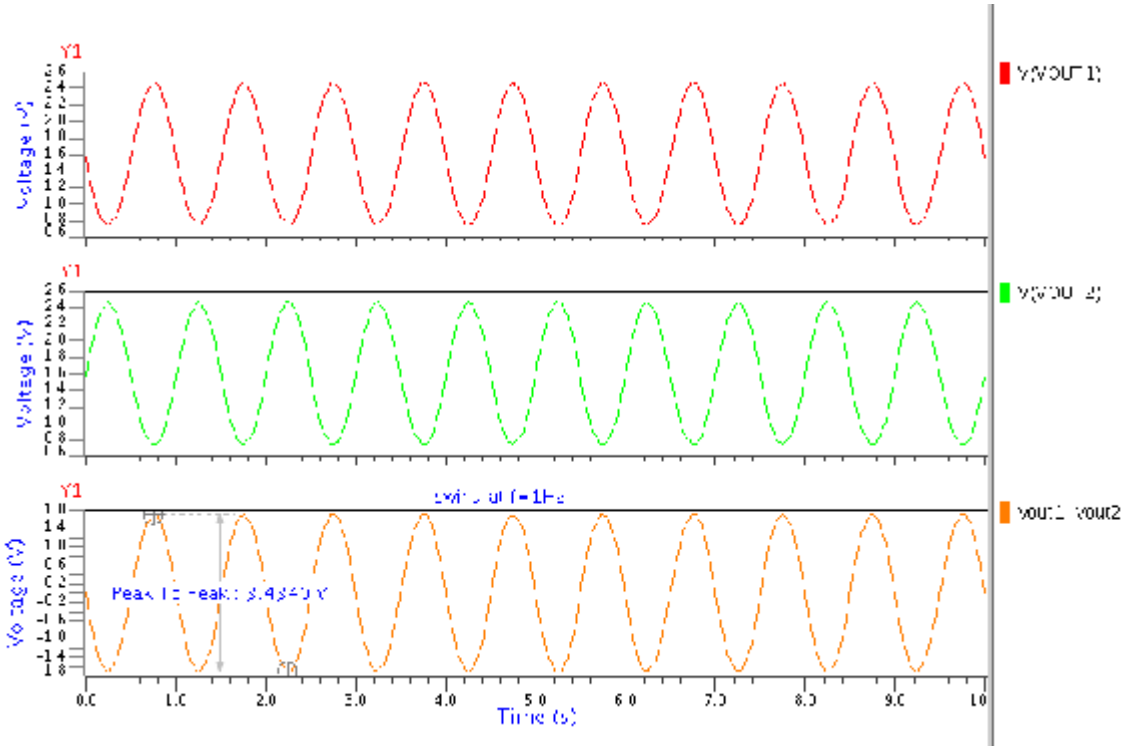


Figure 4.21 Output noise voltages



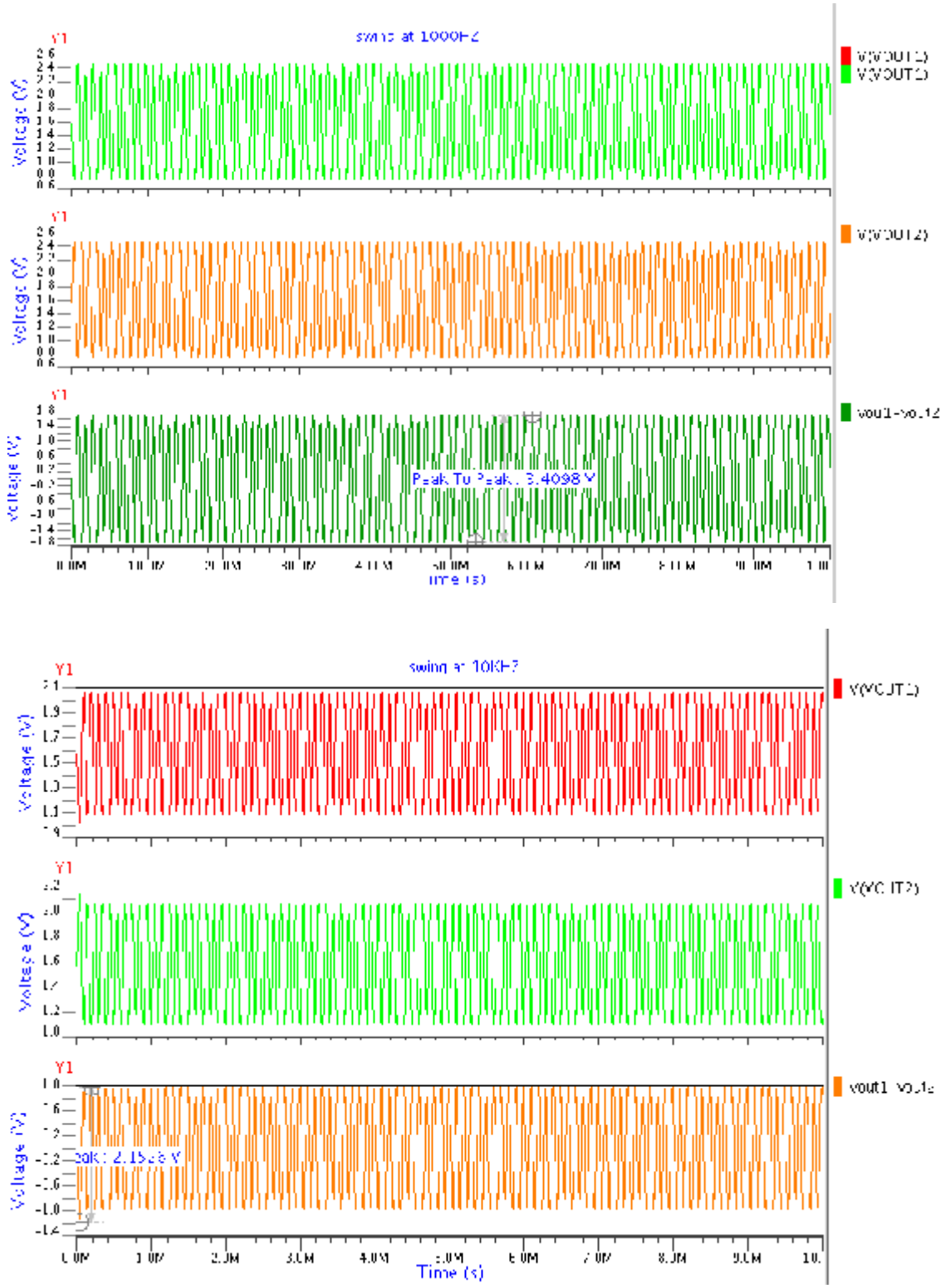


Figure 4.22 Output swing at differential output at various frequencies

The dynamic range with frequency variation is shown in Table 4.4. It concluded that as the frequency increases output dynamic range also increase for fully differential operational amplifier

Table 4.5 Dynamic Range of op-amp at various frequencies

Frequency	Output noise voltage	Output swing	Output dynamic range
1Hz	237.4157μV	3.43V	83.19 dB
1KHz	234.23027μV	3.4098V	83.26 dB
10KHz	119.0101μV	2.1526V	85.15 db

.

At the end of this section, all simulated results of opamp characterization are tabulated in Table 4.5 with target specification and specification of the opamp designed by conventional way.

Table 4.6 Simulation Results of fully differential Op-Amp

	Target specification	Simulation results
DC gain (dB)	≥80	86.02
Unity gain bandwidth(MHz)	300	270.45
Phase margin	≥50°	50.01°
f_{-3dB} frequency(KHz)	≥5	6.105
Output dynamic range (dB)	≥85	85.15
CMRR (dB)	≥85	90.795
PSRR (dB)	-	131.725
ICMR (V)	-	0.9 to 2.2
Output voltage swing(p-p)(V)	≥3V	3.1898
Settling time (nS)	≤30	2.836
Slew rate (V/μS)	≥20	40.585
Power dissipation	Minimize (≤ 5mW)	1.4446 m W
Load capacitance (pf)	5	5
Supply voltage (V)	3.3	3.3

4.2 Post Layout Simulations

After completing the layout of the opamp, it is matched with schematic using LVS simulation. With the successful run of LVS, parasitic and layout netlist extraction simulation have been done using PEX. Post layout simulations have been done on extracted netlist. The simulation results of post layout simulation are given below.

AC Response

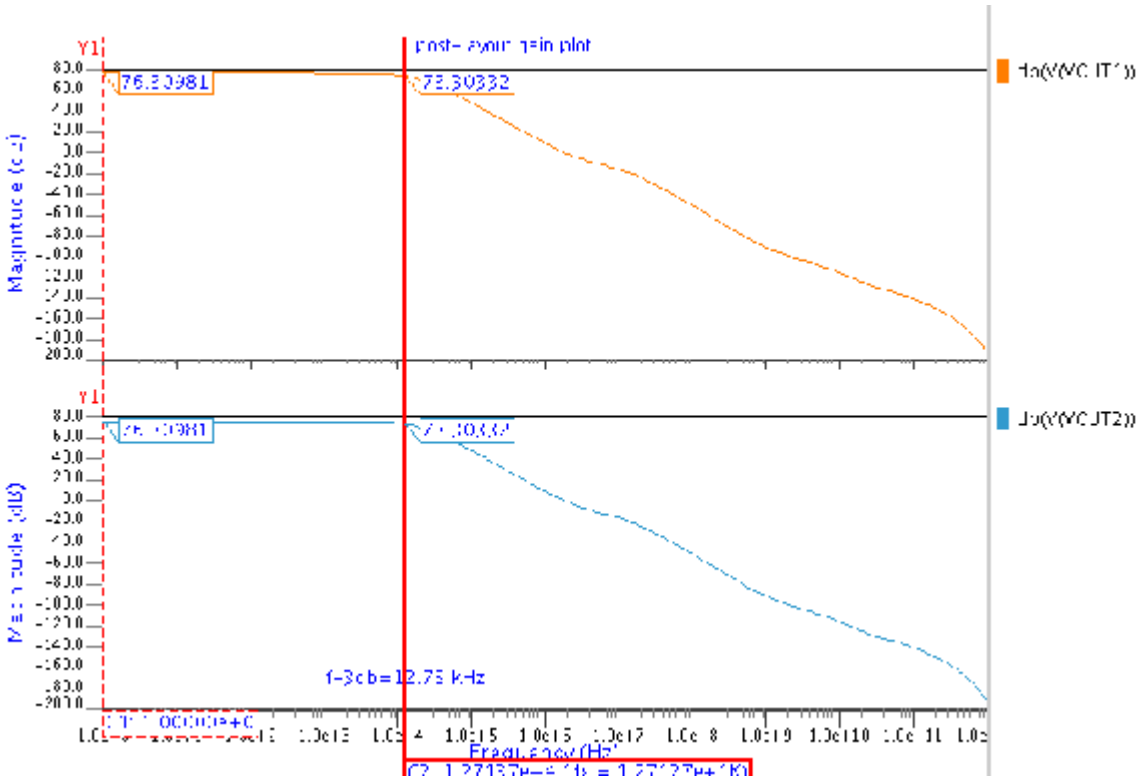


Figure 4.23 Post layout gain-phase plot

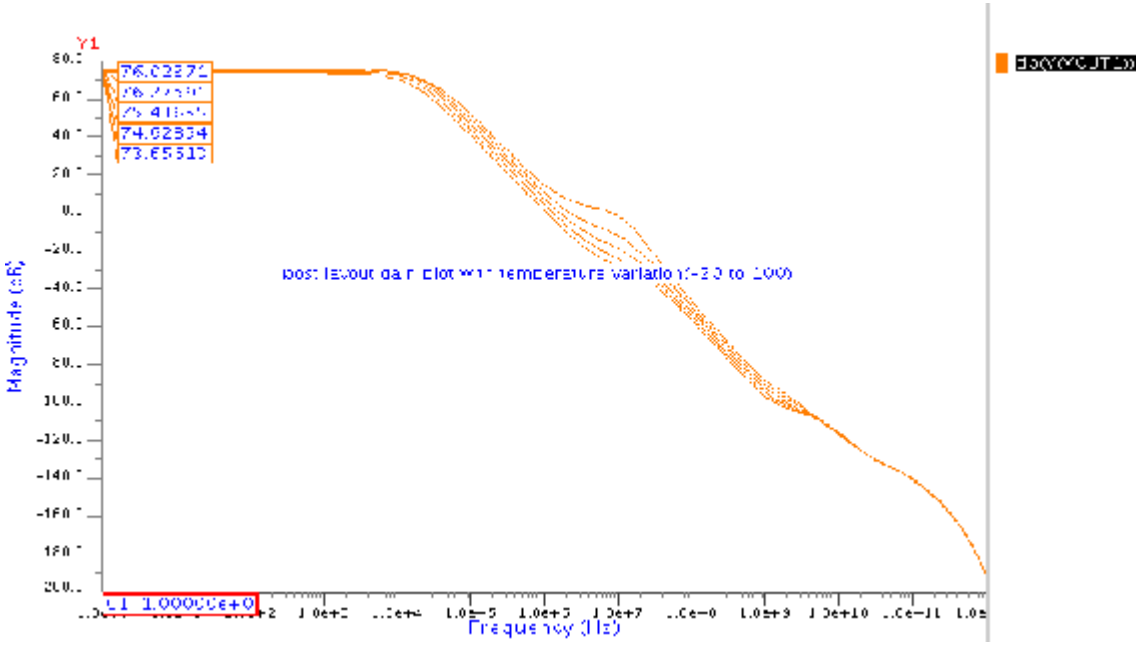


Figure 4.24 Post layout gain-phase plot with temperature variation

CMRR

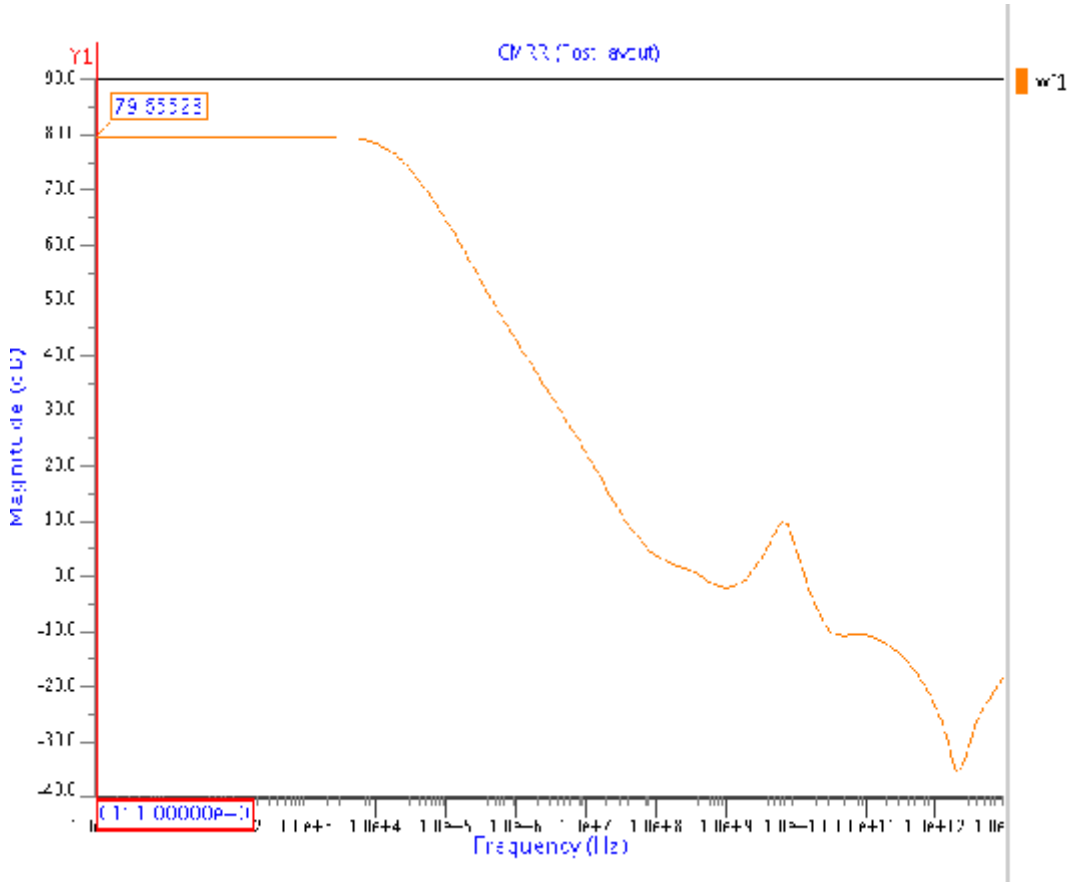


Figure 4.25 CMRR of post layout

Results of post layout simulation are in table 4.7.

Table 4.7 Post layout simulation results

Specifications	**Schematic results**	**Post layout results**
DC gain(dB)	86.02	76.309
f_{-3dB} frequency (KHz)	6.105	12.73
CMRR (dB)	90.795	79.655

4.3 Process Corner Simulation

In this section, Process corner simulation has been done on extracted netlist from layout. The netlist extracted from layout also includes two more netlist, one is distributed RC network netlist, which contains distributed RC network formed by considering resistances and parasitic capacitances of different devices and routing in layout. Another netlist included is the netlist of coupling capacitors in adjacent layers. These parasitic effects can make a big problem if any process parameter varies during fabrication process.

Thus it is necessary to check the circuit performance at every expected corner of the process variation. The simulation done considering all probabilities of process parameter variation is called as process corner simulation.

Here in this simulation process parameter like oxide thickness, mobility and electrical parameter threshold voltage are considered with variations of 10% in each

SS (Slow-Slow)

1) Transient analysis of process corner SS (slow-slow) result shown below;

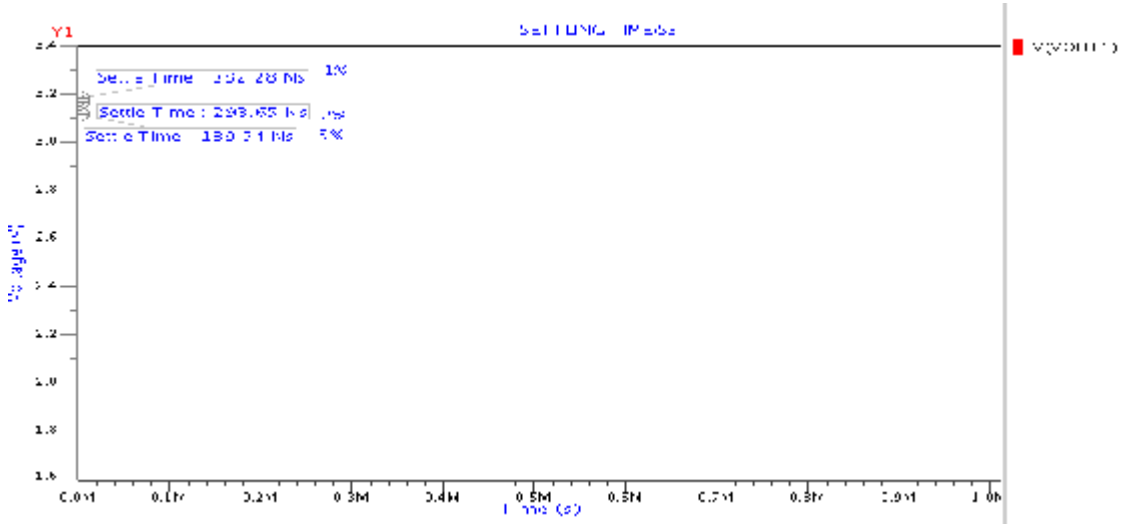


Figure 4.26 Settling time for SS corner

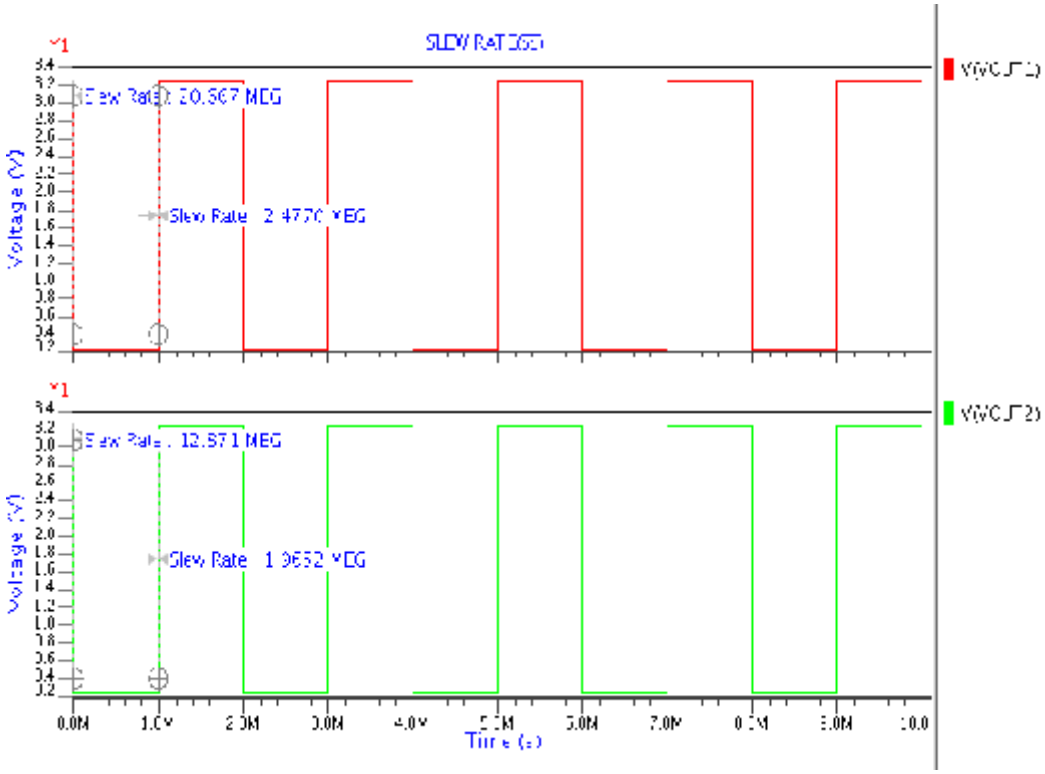


Figure 4.27 Slew rate for SS corner

2) **AC Analysis for SS**

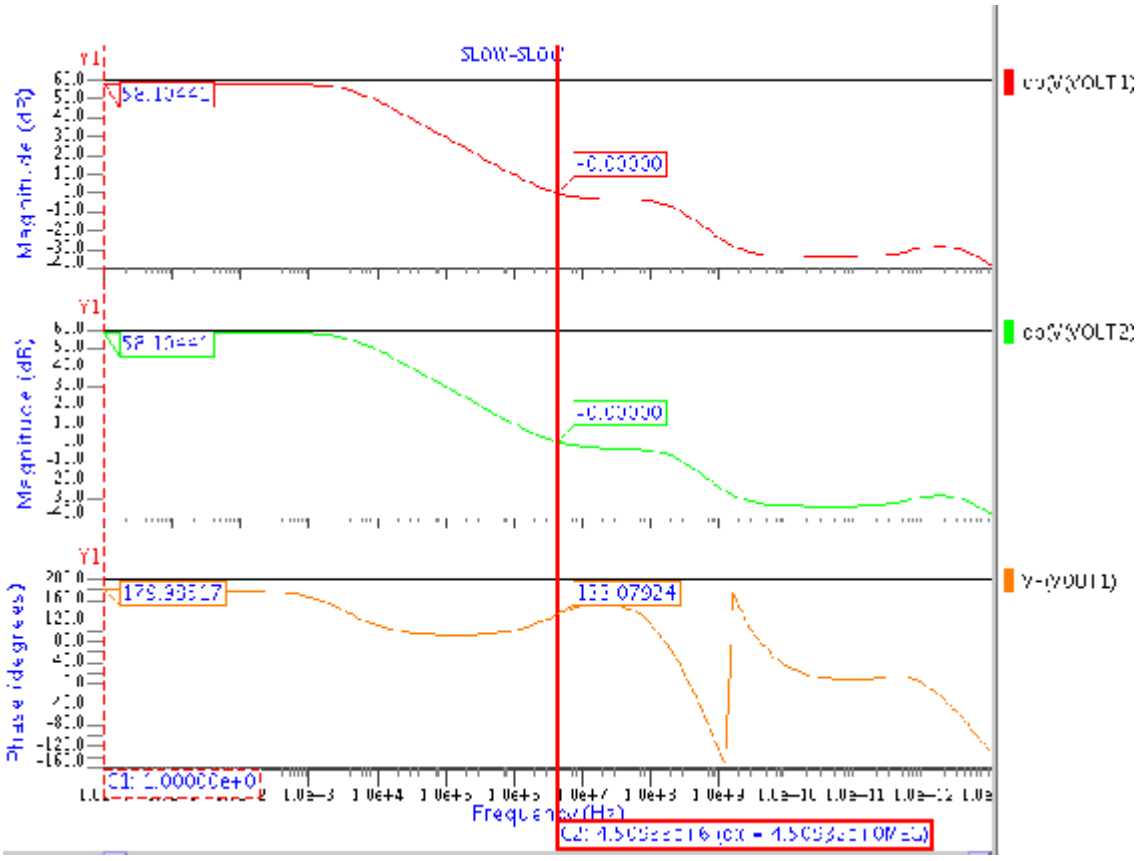


Figure 4.28 Gain- phase plots for SS

SF (Slow-Fast)

1) Transient Analysis

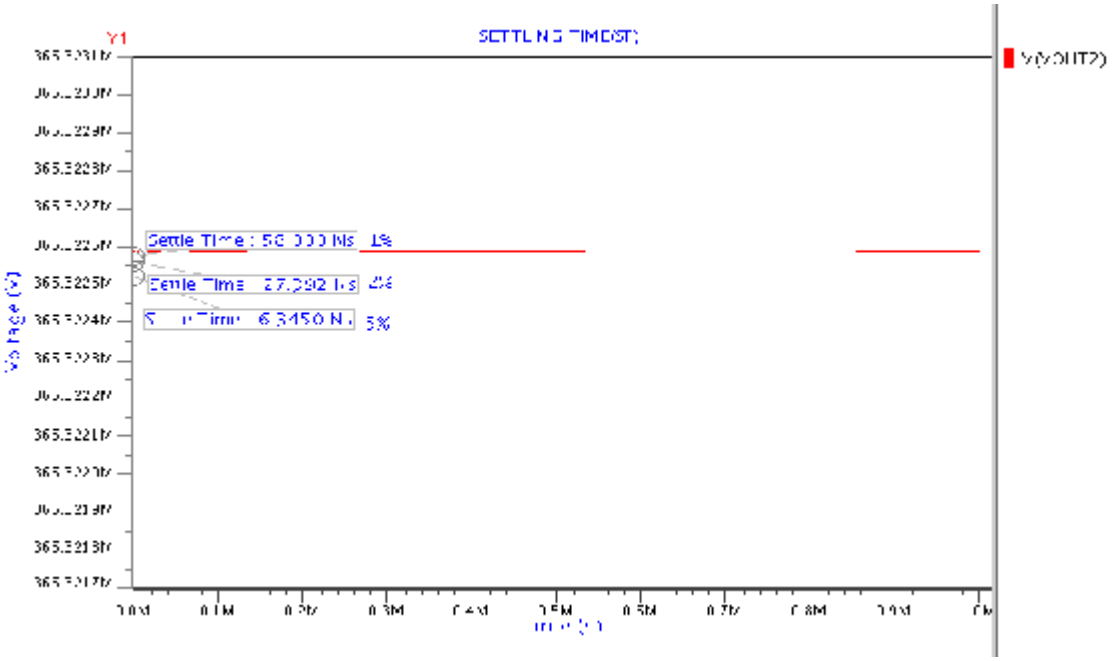


Figure 4.29 Settling time for SF corner

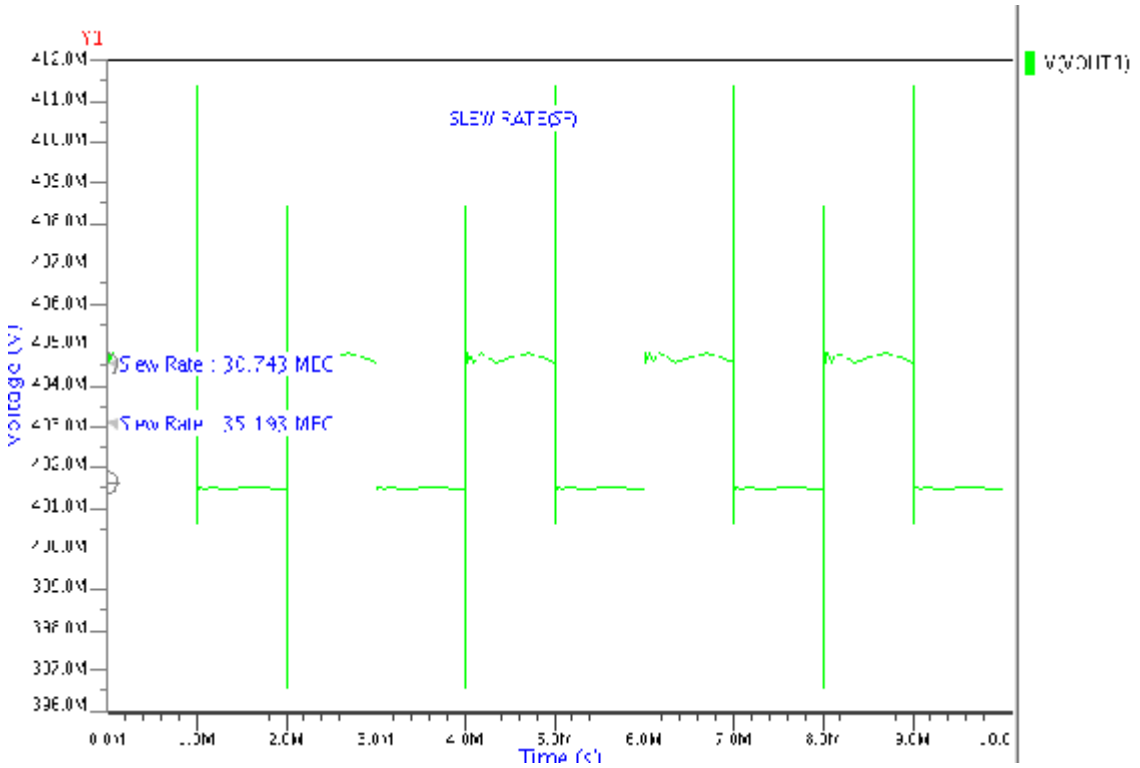


Figure 4.30 Slew rate for SF Corner

2) Ac Analysis for SF

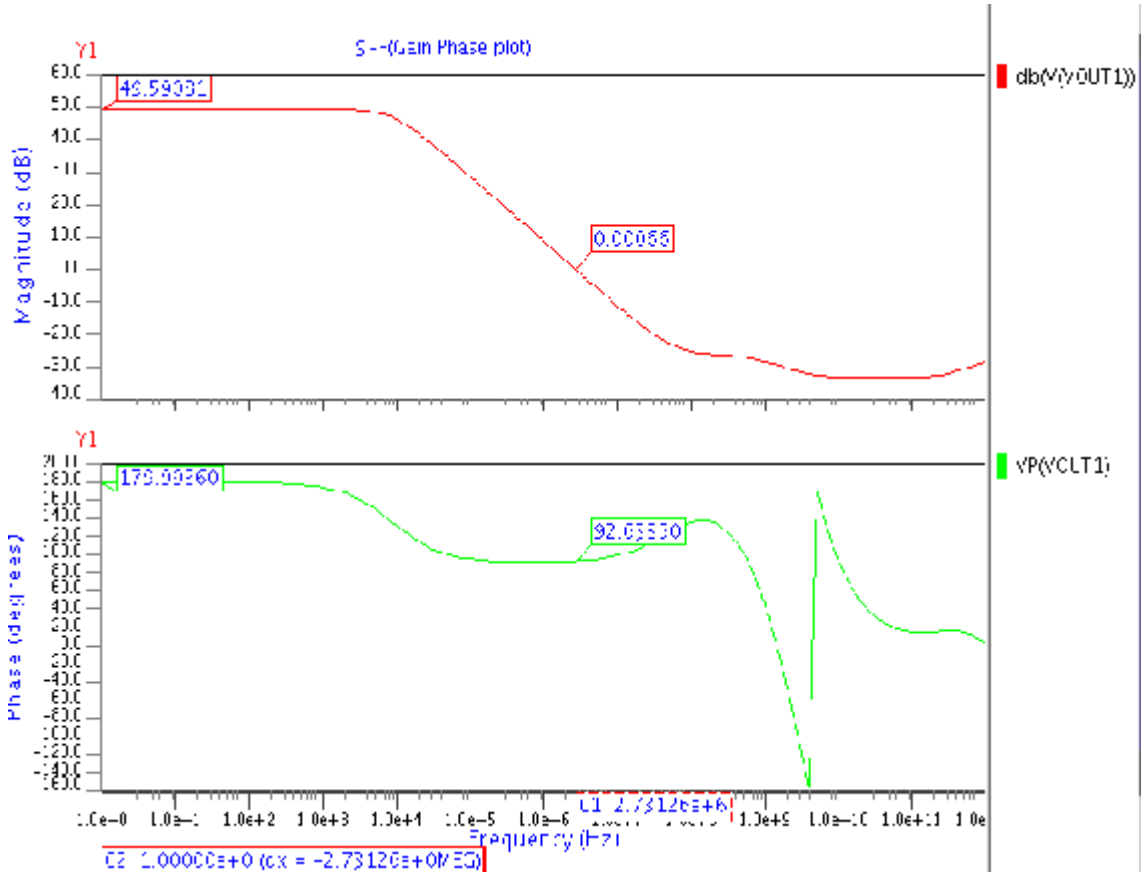


Figure 4.31 Gain-phase plots for SF corner

FS (Fast-Slow)

1) **Transient Analysis**

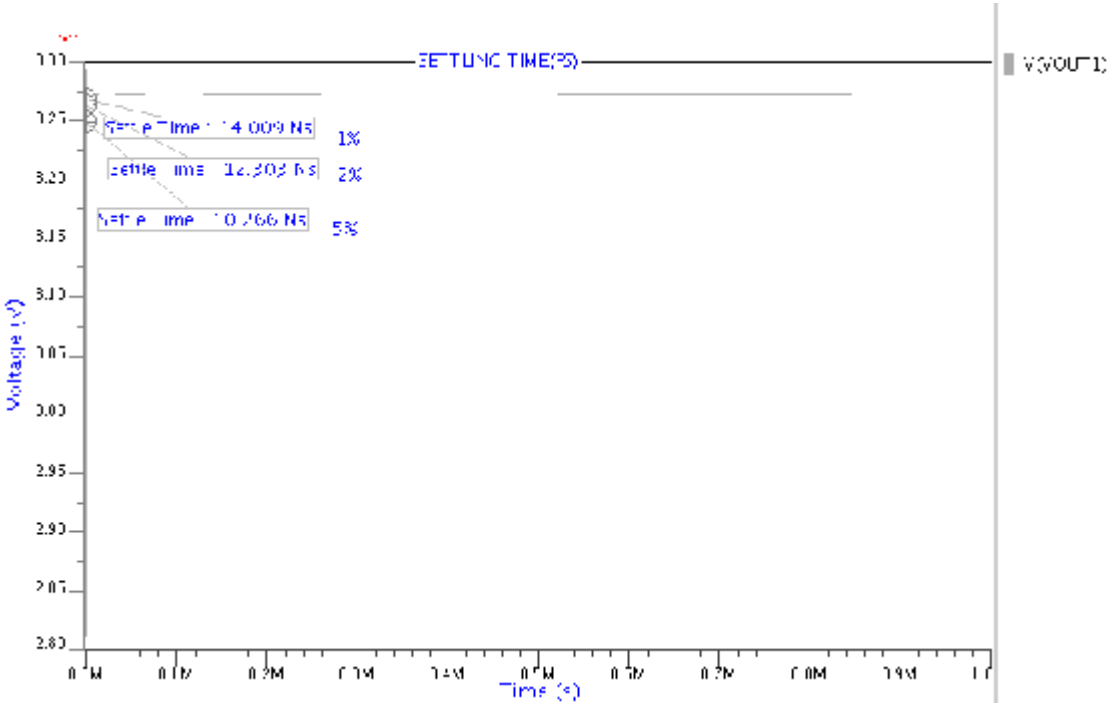


Figure 4.32 Settling time plots for FS corner

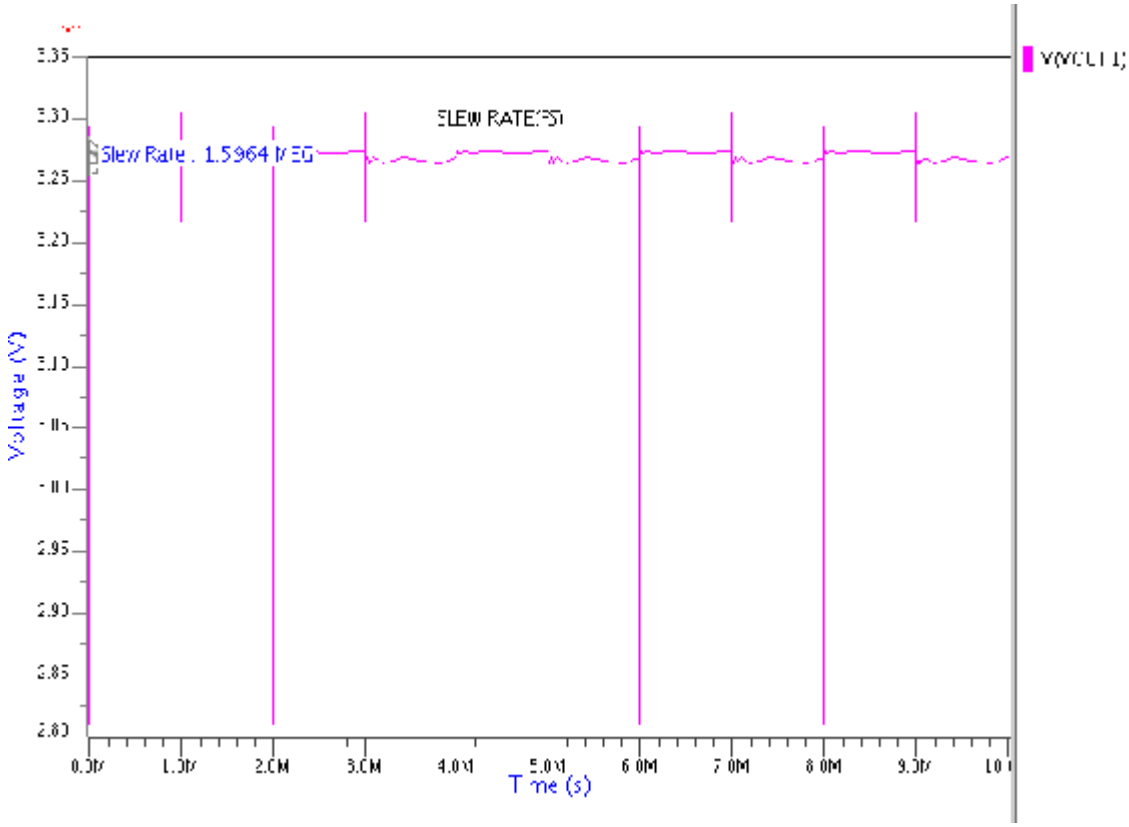


Figure 4.33 Slew rate for FS corner

2) **Ac Analysis for FS**

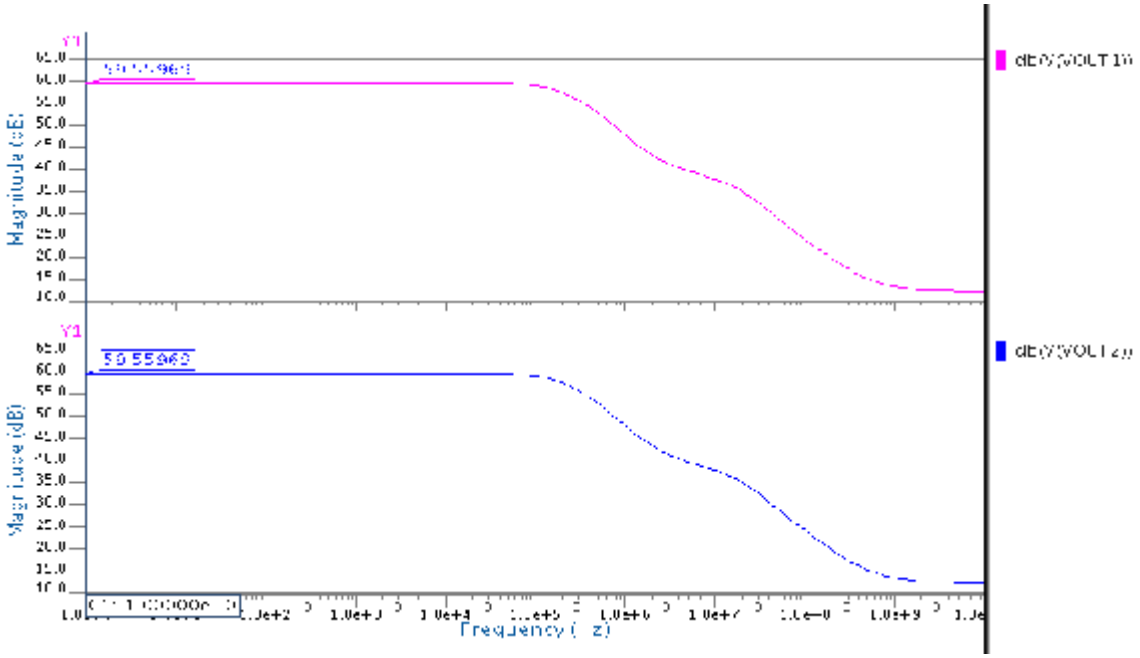


Figure 4.34 Gain plot for FS corner

FF (Fast-Fast)

1) **Transient Analysis**

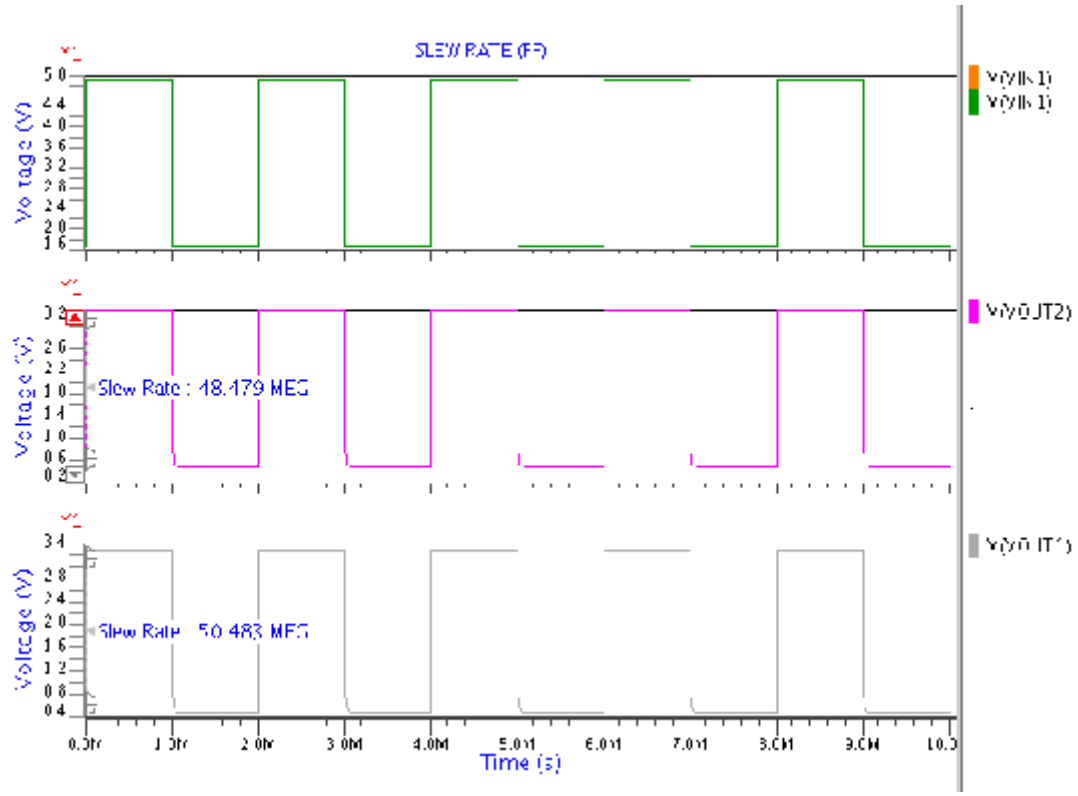


Figure 4.35 Slew rate for FF corner

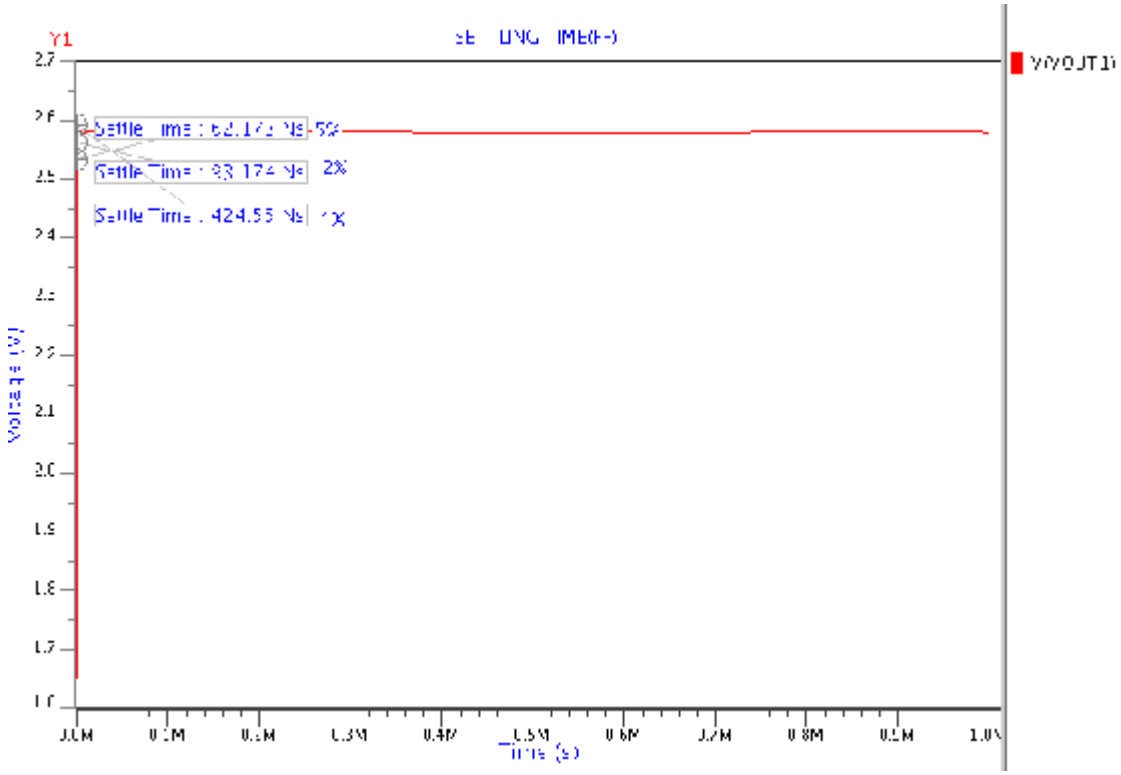


Figure 4.36 Settling time for FF corner

2) AC Analysis

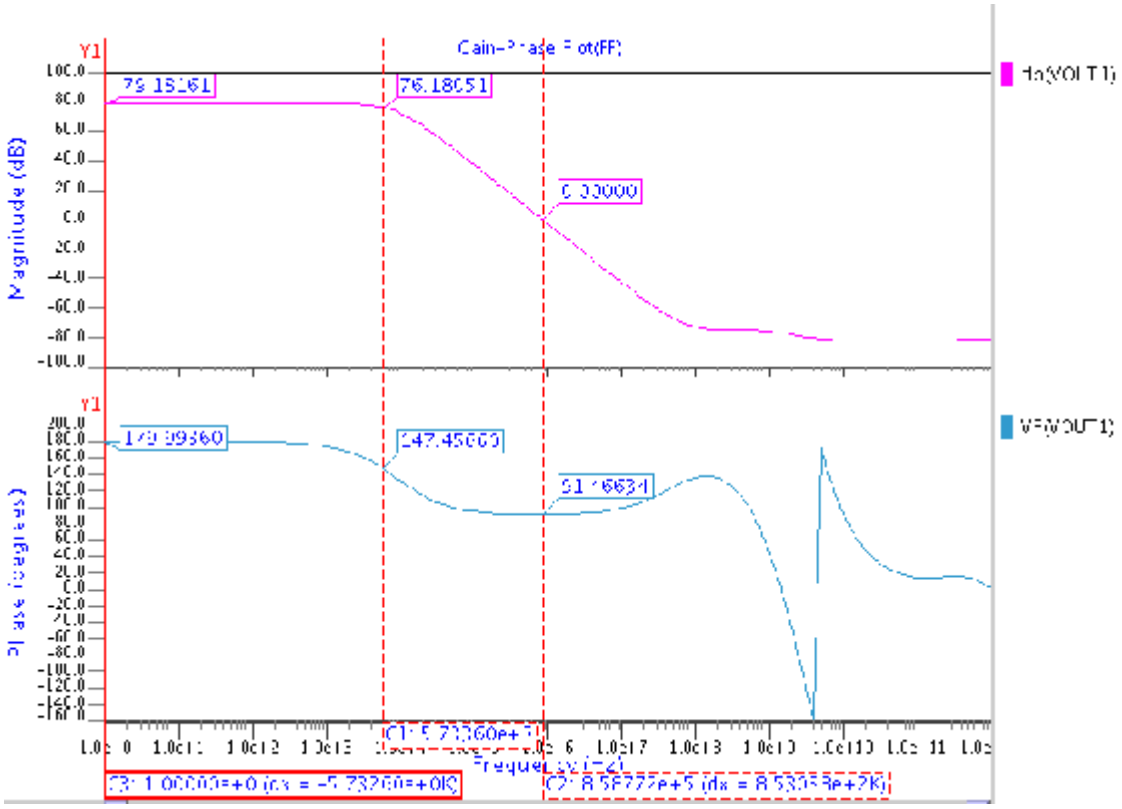


Figure 4.37 Gain –Phase plots for FF corner

Results of process corner simulations are given in table 4.8.

Table 4.8 Results of process corner simulations

Specifications	SS	SF	FS	FF
DC gain (dB)	58.104	49.5	59.55	79.18
Settling time(1% tolerance)(nS)	382.28	58	14.009	424.55
Slew rate (V/µS)	20.667	35.193	15.964	50.483

4.4 Monte Carlo Simulations

The Monte Carlo technique provides the greatest flexibility for studying the results of process variations. All process parameters can be varied either simultaneously or individually. It is the only technique in which a distribution is obtained, not just a trend or a small set of individual points. The resultant distribution is more useful than worst-case analysis since the probability of an occurrence as well as its value is available. This allows process and device engineers to make realistic tradeoffs in setting process tolerances.

The Monte Carlo technique is a method of solving problems by simulating original data with a random number generator. There are two basic requirements for doing a Monte Carlo analysis. A reasonable model for the parameters of interest must exist and a mechanism to simulate the model is needed.

The Monte Carlo simulation results are shown in figure 4.38, for 10 run per individual simulation.

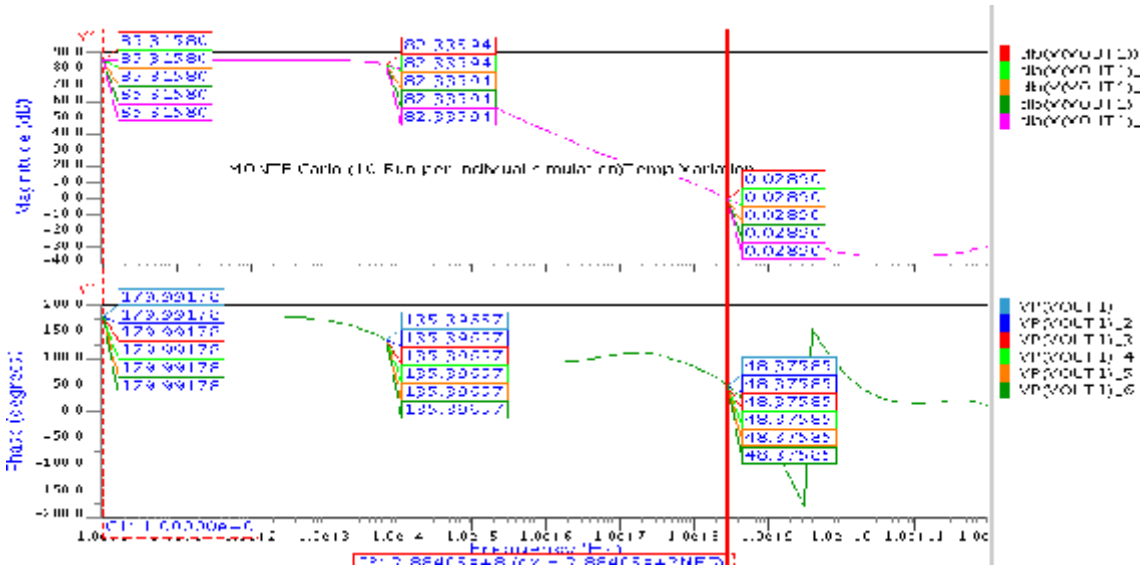


Figure 4.38 (a) Gain phase plots with temperature variation

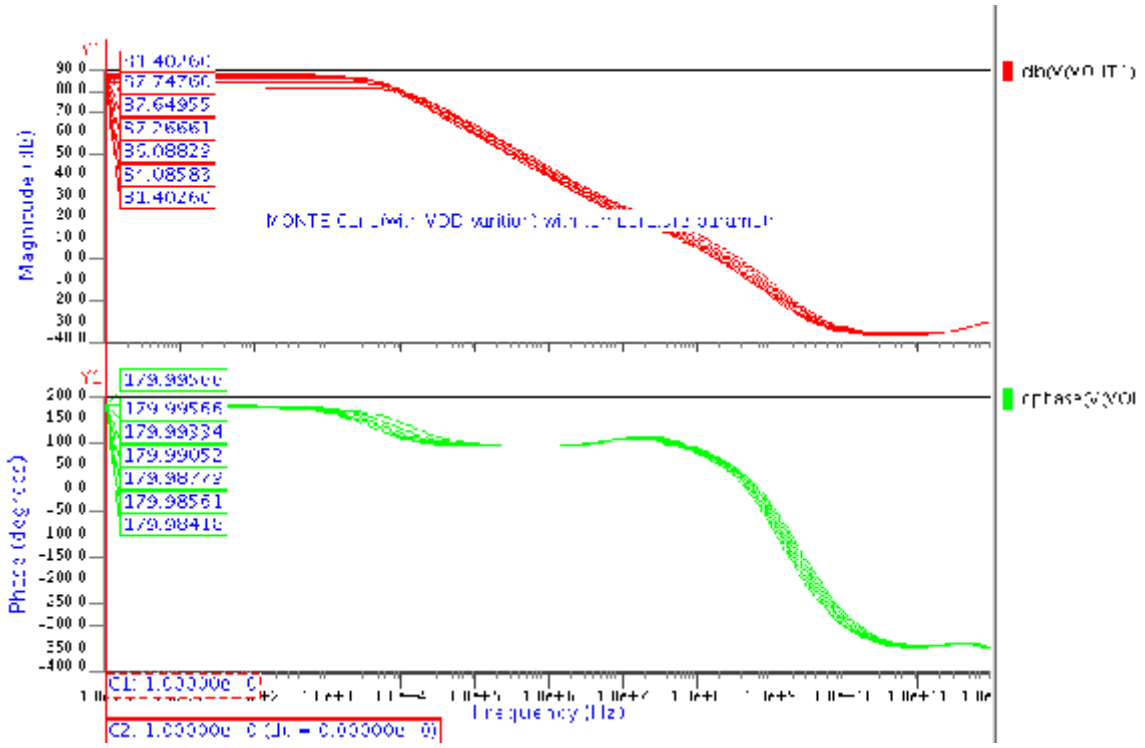


Figure 4.38 (b) Gain phase plots with VDD variation

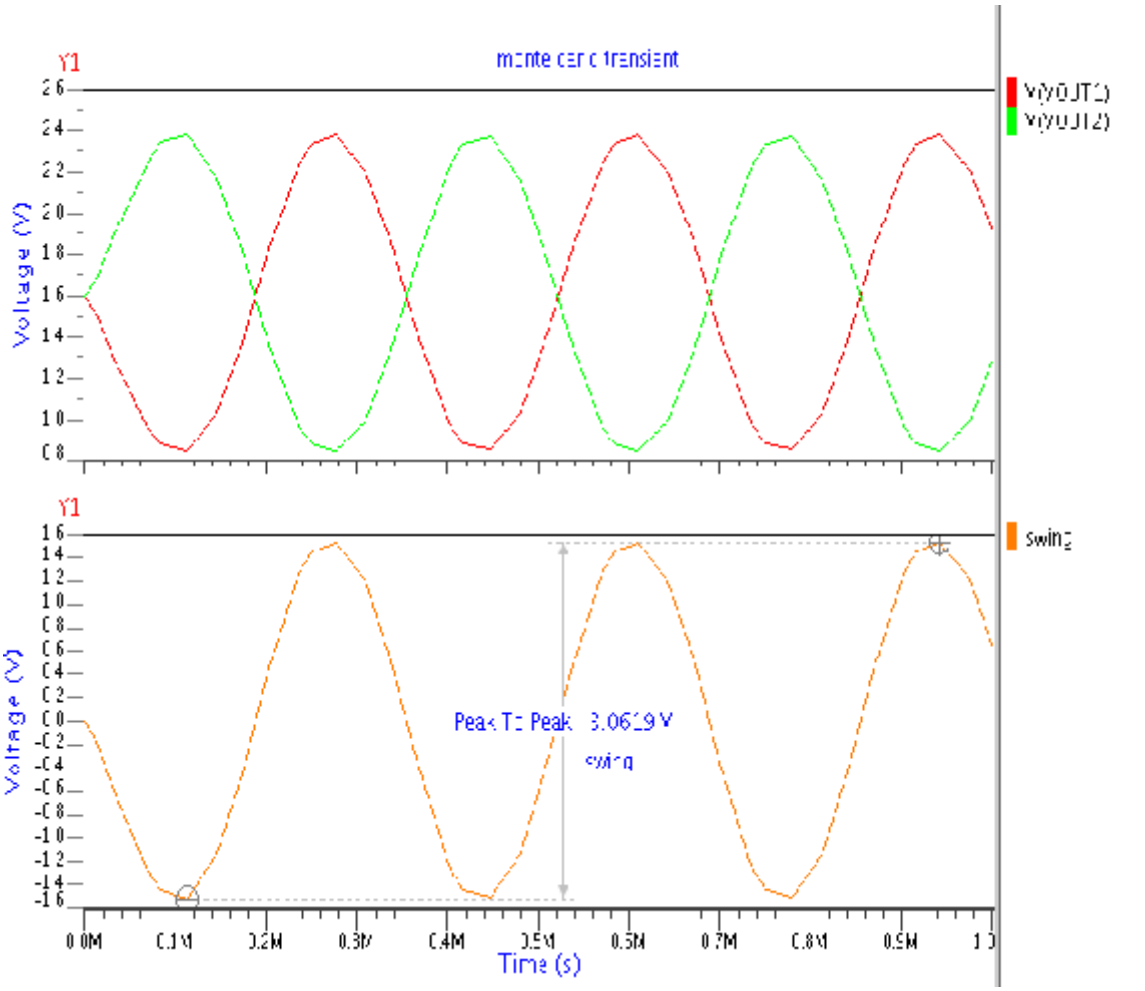
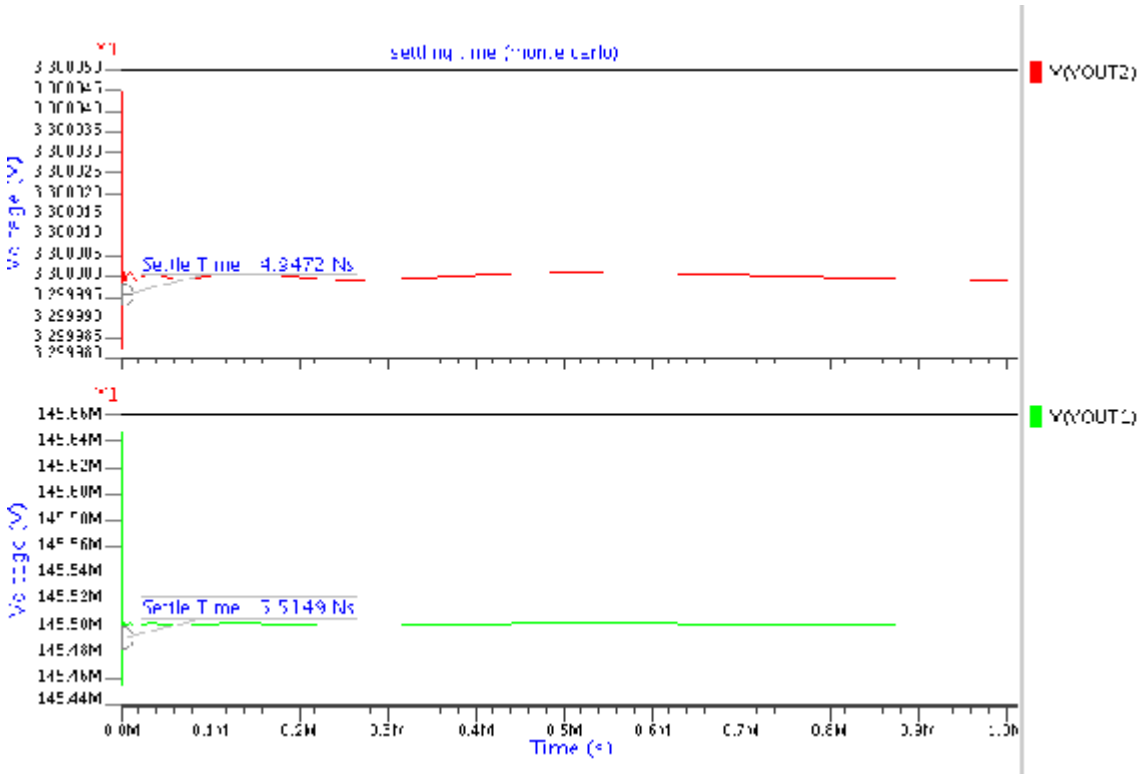


Figure 4.38 (c) Output swing



(d) Settling time

Figure 4.8 Monte Carlo simulation results

Table 4.9 Results of Monte Carlo simulation

Specification	Schematic result	Monte Carlo result
DC gain (dB)	86.02	85.315
f_{-3dB} frequency(KHz)	6.105	5.88
Unity gain bandwidth(MHz)	270.45	288
Settling time(nS)	2.836	5.5149
Output swing (p-p)(V)	3.1898	3.0619
Power dissipation	1.4446mW	2.654mW

Table 4.9 show the Monte Carlo results of the circuit design. It shows that the results of Monte carlo simulation have quite variation from that of schematic simulation results.

CHAPTER 5

CONCLUSION AND FUTURE PROSPECTS

5.1 Conclusion

The fully differential OTA is designed in this thesis work is based on telescopic cascode topology is chosen over its folded cascode counter parts due its less consumptions of power, which is in this design is 1.44mW much less than typical fully differential amplifier. The OTA provide DC gain of 86.02 dB, unity gain of 270 MHz with f_{-3dB} of 6.1 KHz. The low value of settling time of 2.836Ns shows the speed of OTA is quite good at nominal process. The high unity gain bandwidth is achieved by using nulling resistor capacitor compensation technique with feed forward capacitors at both ends.

There is some variation in performance of op-amp is found at two process corners (SF & FS) of design.

Monte carlo simulation gives result much nearer to that obtained in schematic simulation in nominal conditions.

5.2 Future Scope

Applications such as ADC requires high gain as well as large bandwidth and noise rejection capability is found in this design. In addition of all mention parameters, there is scope to improve phase margins for good transient operation. Also there is improvement is require in power dissipation which can we further minimize (<1mW) by using power reduction techniques.

This topology may use subthereshold current for low power & low voltage operation with gain boosting techniques.

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