Study and Analysis of Reliability of Chip with Latest Technology

A Thesis Submitted in Partial Fulfilment of the Requirement for the Award of the Degree of

MASTER OF TECHNOLOGY

in VLSI Design

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CERTIFICATE

This is to certify that **Divya** (Regn. No. 601662005), student of M.Tech.(VLSI Design), **Thapar Institute of Engineering and Technology, Patiala** is doing one year (August 2017 – till now) internship programme in Intel Technology India pvt. ltd. Her title of dissertation is "Study and Analysis of Reliability of chip with latest technology".

During the period of her internship programme, she was punctual and hardworking.

I wish her every success in life.

Biswajit Patra
Principal Engineer
HPG group

DECLARATION

I, Divya, hereby declare that the work presented in this thesis report entitled “Study and Analysis of Reliability of Chip with latest technology” in fulfillment of the requirement for the award of degree of Master of Technology (VLSI Design) submitted at Department of Electronics and Communication, Thapar Institute of Engineering and Technology (Deemed to be university), Patiala is an authentic record of work carried out under supervision of Dr. Alpana Agarwal (Associate Professor, Electronics and Communication Engineering Department, Thapar Institute of Engineering and Technology, Patiala) from August 2017 to June 2018. The matter presented in this has not been submitted either in part or full to any other university of institute for the award of any other degree.

Date: 14 June 2018

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It is Certified that the above statement made by the student is correct to the best of my knowledge and belief.

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ABSTRACT

With the growing technology, various challenges are coming to picture at SOC level with respect to functionality of the design, timing and power perspective. Reliability of a chip includes IR drop (or voltage drop) and Electromigration (or EM) observed in the chip. The IR drop further includes Static IR Drop and Dynamic IR Drop. The current flowing in the metal grid, having some resistance will result in Static IR Drop. The maximum limit of Static IR drop that will not affect the circuit or design is 10%. In the design, 15% Static IR Drop was coming due to weak metal grid. Grid weakness is defined in terms of the current carrying capacity of the metal grid. More current flowing in the design requires more metal paths. Thus, by making grid more robust, Static IR drop was brought down to 9%.

Dynamic IR Drop is high toggling cells in the design. The higher the toggle rate of the cells, the higher is the peak current in the design, resulting in higher IR Drop. The reason for Dynamic IR in this design was cluster of high toggling cells sitting near to each other. Due to this Dynamic IR was observed as 35% but the limit for Dynamic IR to occur in the chip is taken as 30%. By declustering all the high toggling cells, the Dynamic IR was brought down to 28%.

More is the EM percentage in the design higher will be the localized temperature, which may heat up the nearby metals also. Similar to Static IR and Dynamic IR, criteria for EM percentage that will not increase the localized temperature is taken as 400%. The percentage of EM observed in this design is 550% due to high output load capacitance. To meet the EM criteria, load splitting is the optimal solution in this case, which brought down the EM percentage to 380%.

TABLE OF CONTENTS

Sr. No **Chapter Title** **Page number**

LIST OF TABLES

LIST OF FIGURES

LIST OF ACRONYMS

SOC	System On Chip
EM	Electromigration
HIP	Hard Intellectual Property
ECO	Engineering Change Order
P/G	Power/Ground
DSM	Deep Sub Micron
FIT	Failure In Time
DRC	Design Rule Check
Decap	Decoupling Capacitor
DEF	Design Exchange Format
LEF	Library Exchange Format
LIB	Library Exchange Format
GSR	Global Specification Requirement
SPEF	Standard Parasitic Exchange Format
PNR	Place and Route
ITRS	International Technology Roadmap for Semiconductor

CHAPTER 1

INTRODUCTION

1.1 GROWTH IN CHIP DESIGNING

SOC stands for system on chip. Growth of SOC depends upon device, design and application. It has become more popular in the last 17-18 years. According to Gordon Moore, a later founder of Intel Corporation describes in his statement that components on the chip will continue to double every year. For several years the fact was true and hence people started calling this law as Moore's law. At this time, this law has been modified with the statement that components on the chip will continue to double but in every 18 months.

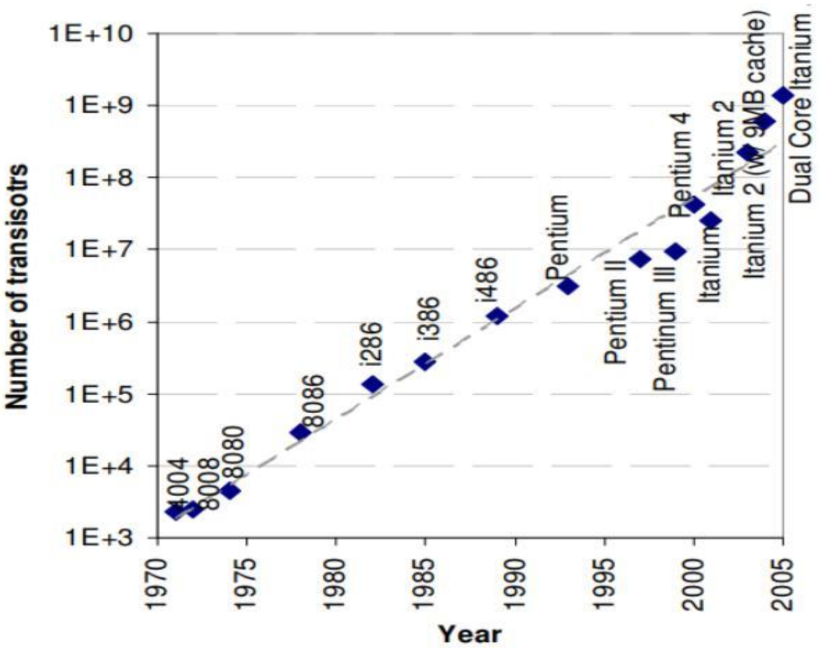


Figure 1.1 Number of transistors vs year

Figure 1.1 shows the trend of growth of number of transistors on a chip. This growth follows moore's law. With the growth of technology nodes, according to moore's law, number of transistors that can be incorporated in a chip are not involved in the process because of other reasons that might lead to degrade in the functionality of the chip.

In the growth of SOC, from the device point of view, we can say that according to moore's law, number of transistors that can be incorporated in a chip have increased. From, the application point of view, we can say that number of different applications are involved in a chip such that user is free to go for more than one application at one time. Last, by the design point of view, we can say that design integration has become more complex because of more complexity in application and device integration. Because of this, Moore’s law is now partially applicable with the advancement in technology node.

1.2 MOTIVATION

In practical cases a die or a chip is placed inside a package. The die is responsible for all the functionality for which the chip is designed and also when power is supplied to the chip through external source like switch, then there is a huge possibility of the voltage drop because metal grid inside the chip will have some finite resistance. For better functionality of the chip, this drop should be less and also reliability of the chip can be made more longer by controlling the rise in the local temperature. The trend of static IR drop, dynamic IR drop and electromigration is not constant for all the technology nodes. These issues will not reduce definitely with the newer technology nodes because of reduction in area. Therefore, it is better to converge the design based on technology node by adopting new ways of doing the same.

1.3 THEORITICAL BACKGROUND

As per the power distribution within a chip is concerned, various things play vital role, which can be found as below :

1.3.1 Metal Grid

Metal acts as a good conductor of heat of electricity. Thus, stack of metal act as a current carrying path, through via from power source to standard cells. Via acts as a current divider. In short we can say that the standard cells will get supply voltage through this grid only. Generally, Copper and aluminum both are used to create metal grid in vlsi designs. We know that silver, copper and aluminum are best conductors of electricity arranged in the order of conductivity ranging from best to good. Out of these three metals, silver is the best conductor of electricity means flow of electrons will be fast than copper and aluminium. But silver is expensive than copper and aluminium, so it is not possible to use silver at commercial level. So, we use copper and aluminum to make power/ground grid. Despite of all this, copper is used for upper metal power-ground grid while aluminium is used for lower metal power/ground grid.

Metal grids can be of any type depending on the design. But generally, we prefer stacks of metals as shown in the above figure. Again, the cost criteria is area. It is always preferred to reduce the area. Horizontal-Vertical-Horizontal .. type metal stacking is the optimal solution to reduce the reduce the area. Generally, lower metal layers are kept more resistive than top metal layers.

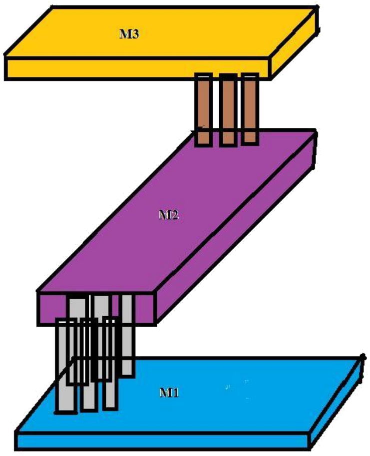


Figure 1.2 Metal Grid

In the above figure, horizontal-vertical-horizontal-… metal grid is shown. Pitch of a metal layer is defined as the distance between the two similar but near placed metal layers. This can be shown in the figure below Figure 1.3. We know that resistance is directly proportional to length and inversely proportional to area. For metal layer, area is nothing but product of length and width. So, we can conclude here that the lower metal layers will be of smaller width than top metal layers. Again, pitch of metal layers depends on technology used and design of the project.

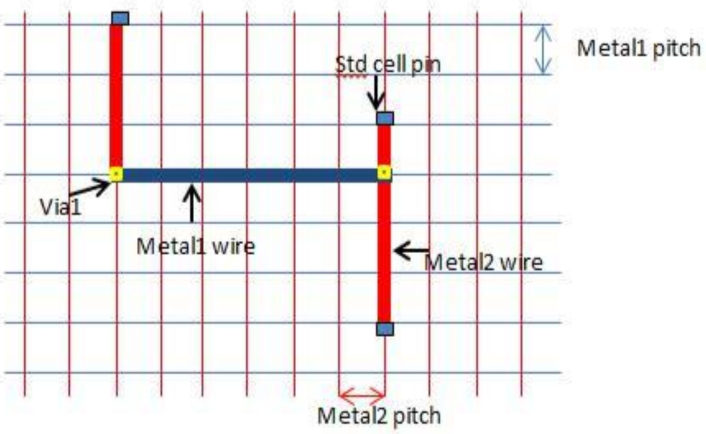


Figure 1.3 Current Distribution to Standard cells through metal grid

In the figure Figure 1.3, we can also see that how metal layers are making a grid like structure and are behaving as current carrying path for the standard cells by making a connection to the standard cell pins.

1.3.2 Standard Cells

Standard cells contain all the logic of the design. To verify the functionality of the logic inside the standard cells various checks are done at different level. Based on the functionality of the chip, number of standard cells in the design may vary. To implement standard cells in the design, various libraries are required which means we are reusing certain designs in implementing one logic in the design. Standard cells are always incorporated into the design before the metal grid insertion. This is done to provide the proper power and ground connections to the standard cells.

Standard cells are of three types :

1. Normal standard cells

2. Double height standard cells

3. Single row standard cells

Length and pitch of the standard cell is fixed. This criteria is used to fix the distance between supply voltage and ground. Also, based on the functionality, height of the standard cell might be double as compared to normal standard cell. These standard cells are called double height standard cells. The only difference lies between normal standard cell and double height standard cell is that double height standard cells are carrying more number of logics, which are required for the design. With the advancement of the technology, single row standard cells are also introduced. The cost parameter of the standard cells in the design is area. So, single row standard cells in the design are good to fulfill the cost parameter of the design. To power these standard cells, metal grid is used. To reduce the wastage of power in the form of heat, grid should be robust enough. Based on the functionality, standard cells can be of three types :

1. High Vt cells: Vt stands for threshold voltage. These types of standard cells are required for reducing the leakage voltage. For Setup violations coming in the design, High Vt cells can be dangerous as they will introduce more delay in the path. So, we can use high Vt cells in the path, which are not timing critical paths. But to save leakage power, we use high vt cells.

2. Low Vt cells: These cells are required for reducing the delay. Generally for timing perspective, generally Setup violations, we use these cells. But for power perspective, these cells are not good.

3. Nominal Vt cells: Nominal Vt cells are also called Standard Vt cells. Delay and power dissipation is average in nominal Vt cells as compared to High and Low Vt cells. So, for timing critical paths and path where we don’t want to increase the power dissipation beyond a point, there we use these nominal Vt cells.

Both power and timing issues are related to each other. So, if we have any power related issue, it is to be taken care that timing of that path is not affected and vice-versa. This is done by using these types of cells.

1.3.3 Multi VDD

Different standard cells in the design might operate at different voltage. Every stage in making chip comes with some cost function. Here, the cost function is voltage drop or power dissipation. If a standard cell is operating is V1 voltage and we are providing V2 voltage, such that (V2 > V1). In this case (V2-V1) voltage is waste, resulting in unwanted dissipation of heat or it might burn the circuitry of the standard cell. So, we provide different voltages to different standard cells.

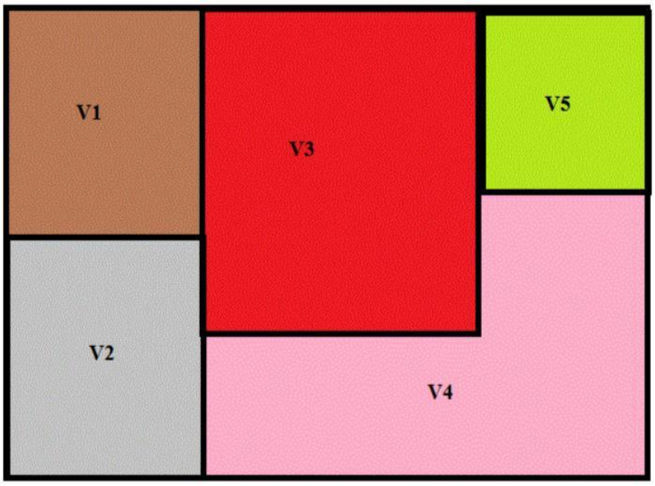


Figure 1.4 Different voltage domains in a design

Multi VDD power domains are created under UPF (unified power format). After there formation, Standard cells are placed in the design according to the type of supply required by them. For instance, some Standard cells are placed in the always on domain and some are placed in the gated domain. The Motivation for this type of voltage domains in that Standard cells placed in the gated region will come to picture only when they are required, while Standard cells in the always on domain will be used always in the design.

Steps to create these domains and use them for different blocks in a chip are as under:

Step 1: create_power_domain

This step helps in creating different power domains within the block or partition. For example, if in a circuit, you want to create two power domains and one ground domain then, we can create power domains like,

```
create_power_domain <domain1_power>

create_power_domain <domain2_power>
```

let us assume domain1_power is operating is higher voltage than domain2_power.

Step 2: create_supply_ports

Once we are done with creating different power domains, it is required to create ports, so that we can connect the main circuitary to the power supply. Again, this is done using following steps :

```
create_supply_ports <low_to_high>

create_supply_ports <high_to_low>

create_supply_port VSS
```

For creating ground in the circuit, we need not to separately create power domain because ground will be common throughout the circuit.

Step 3: create_supply_net

This step is done to connect the ports to the cells in the circuit or design. This is also done in a similar way, but only difference is that there we need to write reuse because we are again creating supply net and connecting it to the standard cells or HIP’s (Hard IP’s) in the design. Example of creating and connecting net is :

```
create_supply_net <domain1_power> -reuse

create_supply_net <domain2_power> -reuse

create_supply_net VSS
```

1.3.4 Static IR drop and Dynamic IR Drop

When power is applied to the die, then current starts flowing through the metal and reach till standard cells. If the voltage applied is not equal to the voltage we are getting at the standard cell, then it is called IR Drop. IR drop is very critical and important aspect of the power analysis because it will impact the functionality of the standard cells and hence, complete circuit will be affected. The Standard cells require minimum voltage to operate. If the voltage reaching at the standard cells is not enough to make the standard cells turn on, then the required output won’t be achieved and functionality of the circuit is circuit is affected adversely.

Static IR drop comes on the chip when constant current flows through the chip. In that case, metal is also having some resistivity and current is also flowing through the die, hence both contribute to the Static IR drop.

If the toggling of the Standard cells is also added to the scenario, then the current flowing through the device will be peak current. In that case, the drop coming on the metal is different from the previous case. This is called dynamic IR drop. In short, we can say that Static IR drop is the leakage current flowing the CMOS circuitry and dynamic IR drop is due to internal power and switching power of the CMOS circuitry.

1.4 OBJECTIVE

The Objectives of this Thesis are :

- To Analyze the Reliability of the Design
- To Provide Optimal Solution for any Violation
- To Generate the Engineering change order (ECO) for better performance of the design.

1.5 THESIS ORGANIZATION

CHAPTER 2: This Chapter is Literature Review and will describe all the previous work done on these topics.

CHAPTER 3: This Chapter describes all the problems encountered while reducing IR drop and improving the reliability of the chip.

CHAPTER 4: This Chapter contains inputs required, outputs generated, Real Scenarios related to IR and EM coming in the design.

CHAPTER 5: This Chapter contains all the Results with Explanations.

CHAPTER 6: This Chapter contains about the future scope of IR and EM violations seen in the design, followed by conclusion of the work done.

CHAPTER 2

LITERATURE REVIEW

This section highlights the literature review done to study and reduce the effect of IR drop and improve the reliability in the chip designing.

Amir H. Ajami [1], describes in his paper the requirement of reducing the static IR and dynamic IR drop. Also, the effect of power/ground (P/G) network is shown with the advancement in the technology. IR drop might introduce the significant amount of skew in the design, which might lead to timing issues. In this paper, the author describes various fixes how the Static IR drop can be reduced by reducing the power supply glitches and ground bounce. Similarly, the effect of Dynamic IR on a circuit can be reduced by adopting various fixes. The task here is that the cells in the design should not toggle simultaneously. If they are toggling at the same time, grid robustness will decrease.

The metal grid is used to carry current from power pads to the standard cells. If IR drop is coming on a metal layer, it means the amount of voltage required by the standard cell to operate will not reach there, so the cell will not work thus it will disturb the complete logic of the circuit, thus the chip will not function properly, so we can say the power distribution is very important in the chip design. In this paper, the author has referred the power grid planning criteria in order to reduce the IR drop.

Yen Kuang Chen and S.Y. Kung [2], discussed in their paper the emerging issues in SOC design. Various challenges are coming as the technology is changing. In this paper, the author described various strategies to deal with and overcome the challenges coming on the way as power consumption, memory, bandwidth, latency, transistor variability, thermal management, multi-processor SOC, reconfigurable logic, etc. In this paper, the author has described the concept of 2D and 3D interconnects. Growing use of 3D interconnects can resolve bandwidth issues but power or thermal issues can grow at faster rate than ever. So, there is a trade-off between the two or more properties or factors , so, we need to make a balance between them.

Theo A.C.M. Claasen [3], in his paper described about the future and current state of work going on in industry. According to author, the system-in-package is going to take place of System-on-Chip, as moore’s law is now not incorporated fully in industry. As per as moore’s law, we are still lagging behind by many times. To provide the solution, in terms of wafer processing, the industry can look at the 65 nm and 45 nm on 300-mm wafers. Major area of concern is 32-nm CMOS technology node. According to author the technology node which will be pushed into major challenges in the designing and power or thermal trade-off is 32 nm and all the smaller technologies to it

Year of Production	2004	2007	2010	2013	2016
Technology Node (hp = half-pitch)	hp90	hp65	hp45	hp32	hp22
DRAM ½ Pitch (nm)	90	65	45	32	22
MPU/ASIC Metal 1 (M1) ½ Pitch (nm)	107	76	54	38	27
MPU/ASIC ½ Pitch (nm) (Un-contacted Poly)	90	65	45	32	22
MPU Printed Gate Length (nm)	53	35	25	18	13
MPU Physical Gate Length (nm)	37	25	18	13	9
ASIC/Low Operating Power Printed Gate Length (nm)	75	45	32	22	16
ASIC/Low Operating Power Physical Gate Length (nm)	53	32	22	16	11

Figure 2.1 ITRS Data

The author has described various technology nodes as shown in the Figure 2.1 and there parameter variation. The data is fetched from ITRS (International Roadmap for Semiconductors) by the author to explain various factors affecting design with smaller technology nodes.

Shih Hung Weng *et al.* [4], discussed in this paper about the worst IR drop seen when the timing analysis is done. Traditionally, gates involved in the design having worst IR drop are considered for timing analysis. The author has tried to implement the same thing using power gate circuit. The author has implemented some algorithms to do so. The algorithm is done considering the effect of decaps for power-gating designs. These algorithms were efficient to reduce the delay coming on it by about 83%.

Jeffrey P. Gambino *et al.* [5], presented in there paper about the reliability issues with advanced copper interconnects. Copper is preferred than aluminium for interconnects because of better resistivity and reliability. But because of low dielectric constant, many issues are coming to picture as technology is growing. In this paper, author has shown the experimental results with few technology nodes, which is shown in Table 2.1.

Table 2.1 Issues coming with advanced interconnects

Node	Dielectric	K	Module	Thermal cond.	Porosity
180 nm	SiO2	4.0	60 GPa	1.0 W/m-K	0%
130 nm	FSG	3.6	60 GPa	1.0 W/m-K	0%
90 nm	SiCOH	3.0	15 GPa	0.6 W/m-K	0%
65 nm	SiCOH	2.8	9.2 GPa	0.35 W/m-K	0%
45 nm	p-SiCOH	2.4	4.6 GPa	0.2 W/m-K	22%
32 nm	p-SiCOH	2.2	2.7 GPa	0.15 W/m-K	31%

In the Table 2.1, it can be observed that with better technologies coming to the picture, how different parameters are varying. With Deep-Sub-Micron (DSM) technology, the length of the interconnect is decreasing, thus, void formation will occur in shorter time, which is thus, impacting the reliability of the chip or circuit. Thus, dielectric breakdown is a more challenging task with newer technology nodes. As the technology is shrinking, in new designs, metal capping is a prime solution. One more solution is there, alloying of cu metal, which we are using for interconnects, but the effectiveness of this process depends on the design.

G. Jerke and J. Lienig [6], proposed in there paper algorithms for easy analysis of Electromigration at the early stages itself. Generally after the design comes to stability, then we go for Electromigration analysis and fixes. But in these cases, it becomes too late for analysis. Sometimes in modern IC’s because of various issues or challenges coming to picture, it becomes difficult to fix them at later stages when design is about to close so it is always better to go for early analysis. For this purpose, the author has described algorithm that will work at the early stage only. The algorithm divides the nets into critical nets and non-critical nets by doing all the analysis on the design. So, based on these analysis, the electromigration issues coming at the peak of the project can be reduced. Not only for time perspective, but also for the design changes, this algorithm is good. In short, at early stages only, metal and location can be taken care in the design from the beginning itself.

Nithin S K *et al.* [7], describes in the paper various challenges and issues in fixing dynamic IR drop. In this paper, the author has described the difference between Static IR and Dynamic IR drop. Dynamic IR drop is due to peak current flowing the metal grid but in Static IR drop estimation, average power dissipation is considered due to average current flowing through the device.

The author has also described how power and timing issues are related to each other. The design complexity lies in the fact that while fixing dynamic IR issues, timing issues might come and vice versa. Thus to balance both of them, we need to find out a way such that we satisfy both the issues. In this paper, the author has described a way by which using we can resolve both the dynamic IR and timing issues.

The author has described various frequency goals by which we can reduce the voltage drop and improve the timing slack as shown in Table 2.2.

Table 2.2 Slack vs Voltage drop failing

Design	Worst Slack (ps)	Failing End Points
IP1	-251	370
IP2	-347	95
IP3	-30	8
IP4	-37	2

Slack should be either zero or some positive value. But here, the slack is negative, so we can improve the dynamic IR drop by fixing these timing issues on priority.

Selcuk Kose and Eby G. Friedman [8], suggested in the paper an algorithm that can be effective in calculating the IR Drop in a fast manner. The author has proposed four algorithms based on different voltage and current scenarios. This method is much faster than the traditional methods followed in estimating and minimizing IR drop. These algorithms are based on principle of locality. The error in these algorithms is less than 0.3%.

Jens Lienig [9], describes in his paper about the electromigration effect in chip fabrication. When the current density in a metal piece is more than the limit that it can resist, then it causes the electromigration effect. The effect of electromigration can also cause voids or hillocks in the metal junction. If it will continue then then it might break the metal junction. EM critical nets depend upon various factors like frequency and load capacitance. In this paper, the author has described various ways to reduce the electromigration.

Vasantha Kumar B.V.P *et al.* [10], proposed in his paper a new technique named glitch compensation technique to reduce the dynamic IR issue. When a glitch in CMOS circuit, then it causes more delay than the expected delay. This increases the total delay in the circuit, which further causes large amount of switching at a same time, thus resulting in more power dissipation. Power dissipated in the form of heat cause change in functionality of the chip and hence the chip will not be that much reliable as per the expectation. The Results shown by the author are as follow :

Table 2.3 Proposed vs Traditional Trends in IR Drop

MAC Layout Quality of Results (QOR)	**Original Place and Routed MAC layout (1301 Cells)**	**After Inserting Proposed Glitch Compensation Circuit to Reduce Dynamic IR Drop (57 Cells)**	**After Inserting Decoupling Capacitance (Decap) Cells to Reduce Dynamic IR Drop**		
			Trail-1 (1953 Cells)	Trail- 2 (68 Cells)	Trail- 3 (31 Cells)
Glitch power (W)	4.85E-05	4.25E-05	5.19E-05	5.23E-05	5.23E-05
Peak Power (W)	3.94E-2	3.85E-2	3.98E-2	3.94E-2	3.94E-2
Switching Power (mW)	6.632E-1	6.59446E-1	6.86207E-1	6.86195E-1	6.86202E-1
Short Ckt Power (mW)	2.44752	2.37256	2.44648	2.44682	2.44682
Internal Power (mW)	8.02345E-1	7.44282E-1	8.03834E-1	8.03645E-1	8.03646E-1
Leakage Power (mW)	1.83135E-1	1.81372E-1	2.17156E-1	1.8432E-1	1.83675E-1
Total Power (mW)	4.0962	3.95766	4.15367	4.12098	4.12035
Total Core Cap (in F)	6.55E-02	6.88E-02	3.87E+03	134.707	61.447
Worst Slack (ns)	2.2926	1.5515	2.292	2.2917	2.2916

In the Table 2.3, we can clearly see the difference in following traditional method and following this new technique glitch reduction technique. In traditional methods, we add decoupling capacitors on-chip. But, in this method, the author has experimentally shown 12% to 50% reduction in Dynamic IR by reducing the top 10 peak transient IR drop numbers. The only thing which makes this method less effective is that in addition to reducing the glitch power reduction, it will add 5% capacitance in the overall capacitance of the circuit. But as the technology node continues to rise, this method will be more effective. More we can reduce the IR drop in a circuit by making more robust power grids.

Minghui Han [11], describes in paper the study of how increase in resistance in a specific part of the supply grid can lead to the increase in the Static IR drop in that region. If the circuit components start toggling at the same time, it leads to Dynamic IR drop. The Aim of reducing the IR drop either Static IR drop or Dynamic IR drop is to make the grid more resistive and robust enough. Designer might come across different challenges while reducing the Static IR drop or Dynamic IR drop, optimization can be done for these issues by finding a way such that we can make a trade-off between the two.

The author describes how we can reduce their drop at different levels. Reducing IR drop is also related to reducing the impedance at the package level. In short, we can say that different factors are there at different levels to reduce the drop.

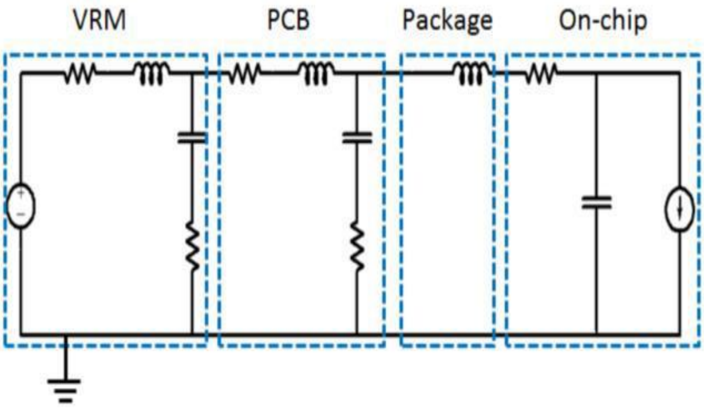


Figure 2.2 Network behind SOC

At the chip or block level, the factor is resistance i.e. making the grid robust enough by reducing the resistance. At the package level, there comes impedance. Again at the PCB level, different factors like resistance, inductance plays a significant role as shown in Figure 2.2.

Tsu-wei Tseng *et al.* [12], explained in his paper about the IR drop coming after routing stage. After floorplanning and placement stage, few routing area will be left in the design. It becomes a challenging task to reduce the IR drop. Because of the lack of routing area, ECO (engineering change orders) are a crutial part of the designing. It might require to re-synthesis the whole design. Thus, it will result in a long process again. The author has suggested few methods by which we can solve our problem and implement the fixes in the design. The author has suggested a technique named greedy-Pareto-optimal (GPO), in which we can reduce the ir drop of the chip with less routing area also. By using this technique, the author has reduced the IR Drop at the post-routing stage from 9.34% to 3.84%. This reduction is almost 58.9%. This is how the IR Drop is improved in the design without affecting the routing congestion.

Valeriy Sukharev *et al.* [13], explained in their paper the voltage drop is increasing beyond the threshold value then it causes the voltage drop to increase beyond the limit that the p/g (power/ground) grid can sustain. This also causes EM violations to occur. The author has described a technique to calculate the stress distribution inside the multi-branch interconnect tree i.e. the stack of metal layers. Lowermost metal layer will be having the highest resistance while topmost layer will be having the lowest resistance. The author has described about time-to-failure (TTF) and various factors affecting the Electromigration phenomenon occurring in the chip. The method suggested by the author accounts for the redundancy of the power grids, assuming that the circuit will definitely fail if it will not function properly.

Zheng Qin and Zhi Wang *et al.* [14], explained the phenomenon of self-heat and leakage as per the reliability of the chip/device is concerned. With every new technology, the demand is high speed and more integration of functional elements on the chip. To fulfill every demand coming with the new technology, one thing to be taken care is package reliability. Change in temperature causes leakage power dissipation in the form of heating or self-heating. In this paper, author has used two layer high density FCBGA (Full chip ball grid array) package in the design. According to estimations shown in this paper, with and without considering the self-heat coming on package makes approximate difference of 16.1 %. Thus, it becomes mandatory to check the reliability of package as well as die.

Govind Saraswat *et al.* [15], presented in paper about estimating the reliability in terms of FIT (Failure-in-time) rate. The author has described the FIT rate calculation by defining all the parameters involved in this process. 1 FIT means 1 failure in 1 billion devices. In this below figure, it can be seen that how we can how high current density in a metal piece can lead to creation of voids or hillocks

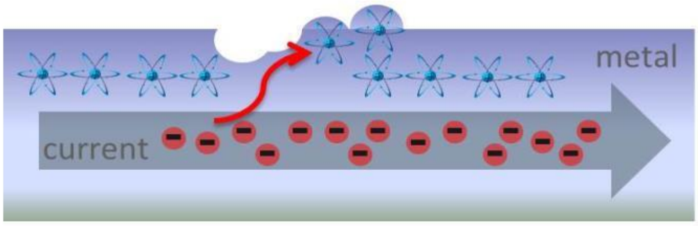


Figure 2.3 Voids and Hillocks

. Electromigration or EM can be defined as :

$$EM = J/Jmax \tag{2.1}$$

Where, J is the actual current flowing in that area whereas,

Jmax is the maximum amount of current allowed to flow in that area.

In this paper, the author has described ways to calculate the Jmax. FIT Rate is used to calculate the failure rate. This information is used to abstract the current limit on every metal segment. This is how EM is calculated.

M.M. Mohammed Imran and N. Shylashree [16], explained in the paper the complete details of the reliability in chip designing . This paper explains the importance of automation in the design and fixing almost all the violations. The author has described has also described various factors on which reliability of the chip depends like load capacitance and frequency. One reliability factor can also cause other reliability issue to occur because anyhow the factors affecting them are same. The fixes of the almost every reliability issues are also explained in this paper. The author has implemented the reliability issues using PARADE tool. This paper also describes various scenarios where reliability issues can come. The implementation of these reliability issues might sometimes not possible because of various reasons, then in that case, we go with the statement that whether it is good to fix or must to fix kind of situation.

CHAPTER 3

PROBLEM STATEMENT

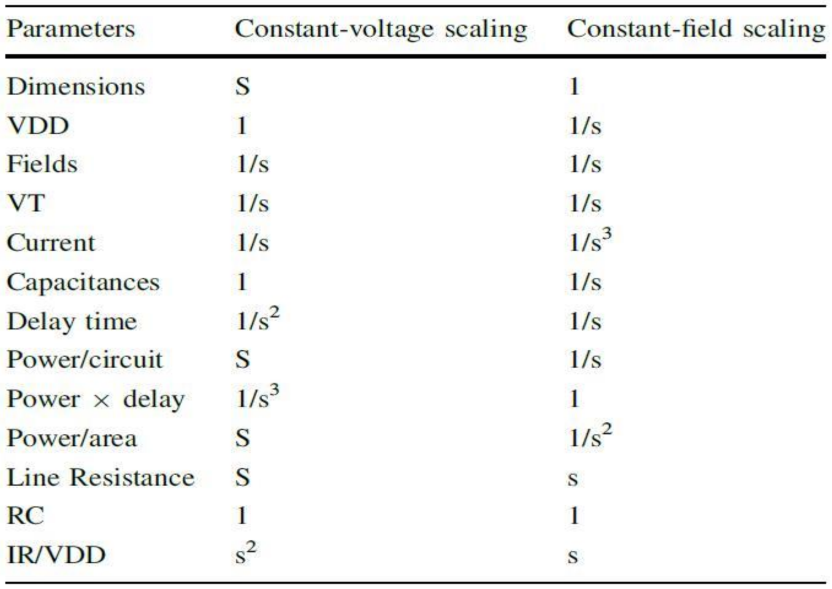
3.1 PROBLEM STATEMENT

Power delivery network in chip fabrication deals with current density, temperature and voltage drop in the chip. Till now with this advancement of technology, the IR drop reduction and reduction of electromigration (EM) effect is a challenging task because of reduction in various parameters of a chip. If resistance is more, it will increase the drop and power dissipation will be more. Also, the reliability of the chip will decrease with increase in EM violations. Thus, lifetime of the chip will decrease.

3.2 PROBLEM EXPLANATION

As the technology is growing, more challenges are coming on the way. The main reason behind this is scaling down of various parameters of the device.

Table 3.1 Constant-Field Scaling and Constant Voltage Scaling



Parameters	Constant-voltage scaling	Constant-field scaling
Dimensions	S	1
VDD	1	1/s
Fields	1/s	1/s
VT	1/s	1/s
Current	1/s	$1/s^3$
Capacitances	1	1/s
Delay time	$1/s^2$	1/s
Power/circuit	S	1/s
Power × delay	$1/s^3$	1
Power/area	S	$1/s^2$
Line Resistance	S	s
RC	1	1
IR/VDD	s^2	s

The Table 3.1 explains about the scaling of the various parameters. As we move from one technology to other, the decrease in the area is the main concern. Power/area is scaled up means that power dissipation will increase, which will cause IR drop and Electromigration effect. Thus, moving ahead will newer technologies is a challenging task even if the circuit functionality is same. Also, number of features in a die can be increased.

According to ohm's law, V = IR. Voltage drop is further of two types: Static and Dynamic. Static voltage drop means that we consider that on an average how much the current flowing in the device multiplied by the resistance of the metal grid.

$$V= IR \tag{3.1}$$

Average current flowing in the circuit depends upon the requirement of the circuit based on the functionality of the circuit. Power bumps are used to provide current to the standard cells. If more power bumps are there, then more current will flow through the metal interconnection. So, average current will increase. This is called glitch in the power supply. But, while calculating Static IR drop, ground bounce is also considered. It also plays a vital role in static IR drop.

For different circuits, the criteria for the static IR drop may vary. The least percentage of the Static IR drop we can achieve is always best for the circuit. But again as we move towards more advanced technology, various challenges and issues are coming on the way to achieve this.

Dynamic IR drop due to high toggling of the cells. If the toggle rate of the cell is more, then the peak current will be more and hence, Dynamic IR drop will be more. Similar to Static IR drop, the calculation of the Dynamic IR drop is same. The difference here lies in the fact that in this case, different types of cells will have different ideal voltages. As we are considering toggling of the cells, the ideal voltages of the cells is considered while calculating Dynamic IR.

Unlike Static IR drop calculation, we check the peak current coming on that net. Based on that, we can calculate the percentage of dynamic IR drop occurring in the chip or block.

Another problem or challenges we face are to control the Electromigration effect. Cu metal are used to carry current from power pad to standard cells. If the current injection is more, then, it might cause voids or hillocks.

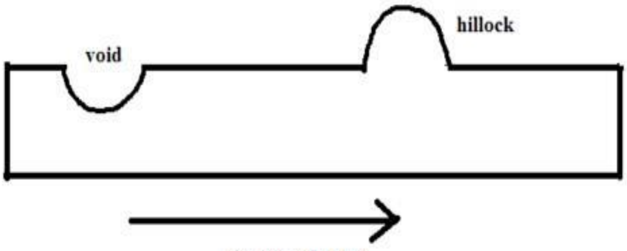


Figure 3.1 Excess Flow of electrons causing EM issues

If more and more current will continue to flow, then it might increase the local temperature of the metal, which might further cause more and more deep voids or hillocks and ultimately the metal will break. Hence, no current will flow in the device. The complete chip will not work.

$$EM = (Irms/Ilimit) \tag{3.2}$$

Irms is the amount of current flowing the conductive path and Ilimit is the limit of current allowed to pass through the metal path based on several experiments, depending upon the length and width of metal. Different metal layers have different dimensions, so the limit of current it can resist without causing any damage to the device (Ilimit), will also vary.

In the market, more reliable devices are costly. Also, with the new technology, meeting the EM reliability is very difficult. Because the area is reducing impacting more and more heat dissipation, causing rise in the local temperature, again impacting the electromigration (EM) effect.

Other reasons for electromigration are long nets, bigger driver size of the driver cell, high frequency of the cell and higher fanout of the driver cell.

We know that the resistance value is directly proportional to the length of the route made to connect the driver cell to the load. If we increase the length, resistance will increase, which further results in increasing the local temperature. Thus, EM will definitely increase.

If one driver is driver couple of cells, then the current requirement of the cell will be more, this high current dissipates more heat (as per joule’s law). This heat is enough to increase the temperature and causing metal atoms to displace, causing voids or hillocks.

Higher the frequency, faster will be the transition of the data. This is the requirement of the high speed circuits to improve the performance. But, it will cause the movement of electrons fast and thus, they will collide with each other, causing further increase in the temperature, causing Irms to increase beyond the limit.

If in a design, we are using bigger driver cell, then it can allow large amount of current to flow, which again causes higher Irms. This will further increase the electromigration effect.

CHAPTER 4

ANALYSIS OF DESIGN RELIABILITY

4.1. IR DROP

Power to the chip is supplied by some external sources like battery or switches. The current start flowing through metal interconnects. As metal is also having some resistance, thus voltage difference starts increasing, this is called IR Drop. IR analysis is divided into two types: Static IR and Dynamic IR.

4.1.1. Static IR analysis

Metal grid has some finite resistance, used to distribute current to the standard cells. According to ohm’s law, V=I.R , thus some drop will occur, called as Static IR drop.

4.1.1.1 The inputs required and outputs generated to perform Static IR analysis :

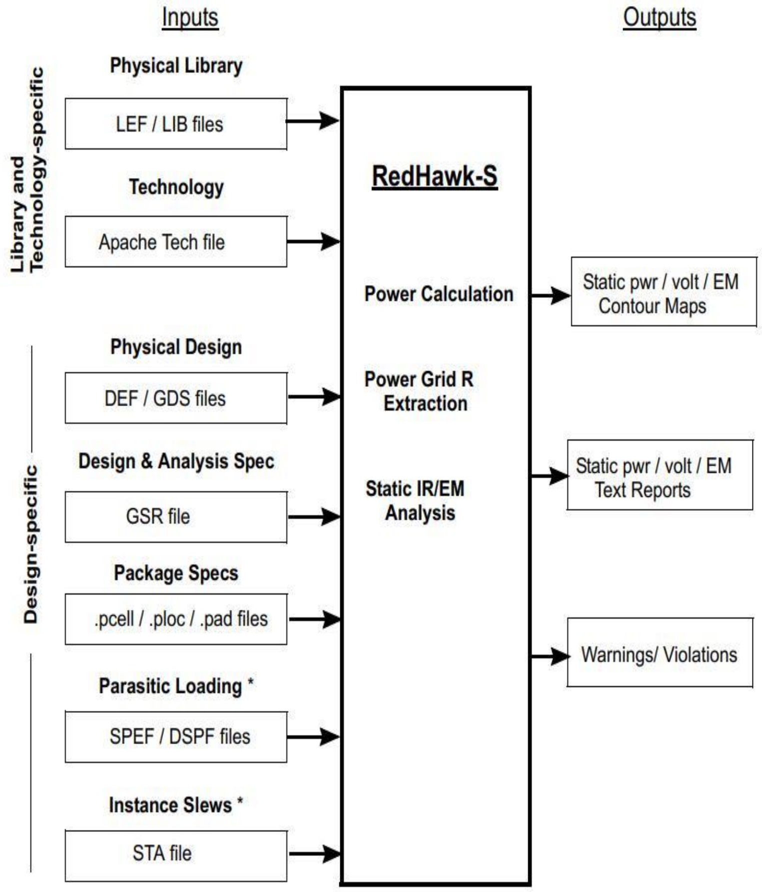


Figure 4.1 Flowchart for Inputs and outputs for Static IR drop

The above flowchart describes the inputs required to perform the static IR analysis and also describes the outputs generated from these analysis. The inputs which are shown with asterisk sign are optional for performing the static IR analysis. The description of various inputs are as :

(a). DEF (Design Exchange Format) : This is a standard format file used to read the design. This file contains the information about the design like physical description of instances, power and ground network, and other circuit elements. If in a design, we have multiple def files then we need to specify every def files with extension “top” at partition level. DEF file is created by PNR (Place and Route) tool like icc or icc2 from synopsys and encounter from cadence.

(b). LEF (Library Exchange Format) : LEF files contain the physical information about the library cells like Layer, Type, Width and Routing. LEF file is also a standard format file used to run the simulations.

These two files are used to read the design. By default, the tool will be able to read all these files in zipped format.

(c). GSR (Global Specification Requirement) is a file which is created by the tool, which acts an input file for the simulation. It contains all the files required by the tool. In short, we can say that the tool will take this file as input file. This file contains DEF file, LEF file and all other files required by the tool.

4.1.1.2. Steps involved in calculation of Static IR drop :

The following are the key steps in the static IR drop :

(a). Prepare design data files.

(b). Import design data using the automated setup script or the GSR file.

(c). Perform power calculation.

(d). Perform power grid extraction for R network.

(e). Evaluate power/ground grid weakness.

(f). Define pad and package constraints.

(g). Perform static IR drop voltage drop and EM analysis .

(h). Perform static IR/EM summary reports and evaluate what other information is needed from the analysis.

(i). Explore solutions to reduce excessive static IR drop with the Redhawk power grid Fixing and optimization tool.

4.1.1.3. Necessity of Static IR drop Estimation

Static IR drop is the due to the average current flowing through the device. The figure below describes the I-V characteristics curve of the device.

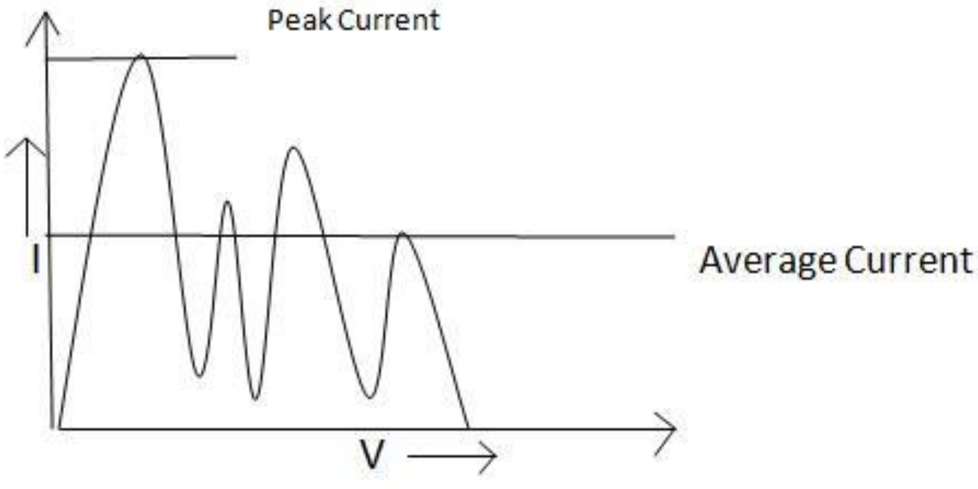


Figure 4.2 I-V Characteristic Curve

Static voltage drop means that we consider that on an average how much the current is flowing the device multiplied by the resistance value. According to Equation (2.1),

$$V = I R$$

Average current flowing in the circuit depends upon the requirement of the circuit based on the functionality of the circuit. Power bumps are used to provide current to the standard cells. If more power bumps are there, then more current will flow through the metal interconnection. So, average current will increase. This is called glitch in the power supply. But, while calculating Static IR drop, ground bounce is also considered. It also plays a vital role in Static IR drop.

4.1.1.4. Calculation of Static IR Drop :

Static IR drop estimation is not a difficult task. It depends on Ideal voltage, Glitch in power supply and ground bounce.

Glitch in the power supply: It is defined as the voltage drop occurring due to current flowing through the parasitic inductance associated with the package wire bonding due to sudden charge and discharge of capacitance with respect to VDD. It can be defined the change in the supply voltage assumed to reach in the standard cell and the voltage actually reaching there.

Glitch in supply voltage = (ideal voltage assumed to reach standard cell) – (actual voltage reaching there) 4.1

Ground bounce: It is defined as the difference between the ground voltage i.e. 0V and the actual ground voltage reaching there. It is actually supposed to go to ground level but it bounces and creates some spikes.

Static IR can be calculated as:

$$\text{Static IR drop \%} = \frac{(\quad h\ h \quad + \quad)}{} \text{ X 100 \%} \tag{4.2}$$

Ideal voltage is the operating voltage of the standard cells. For different blocks or circuits, the criteria for the static IR drop may vary. The least percentage of the static IR drop we can achieve is always best for the circuit.

4.1.1.5. Finding the Minimum Resistive Path

Static IR drop is due to average current flowing in the metal grid. As the grid is made up of copper, it has some resistance value. Therefore, when power is applied to the grid through some I/O peripherals, then due to resistance of the metal, voltage drop occurs. We can’t do anything with metal resistance, which is the default value. But we can reduce the effective resistance of the instances in the design and thus, tool can decide the minimum resistive path of the way current can flow through it.

In all previous work, people have explained different ways in which they can reduce the drop. But practically, it becomes tough to fix these issues with the growing technology node. In Deep-sub-micron technology, fixing one IR issue might cause other disturbance in the circuit, like DRC (Design Rule Check), timing issue, etc. Sometimes, due to routing congestion also, reduction of normalized resistance becomes difficult.

The normalized resistance can be calculated as:

$$\text{Rnorm} = (\text{Rinst} - \text{Rmin})/(\text{Rmax} - \text{Rmin}) * 100 \tag{4.3}$$

Where, Rinst is the effective resistance of the Power/Ground arc with some max value and min value.

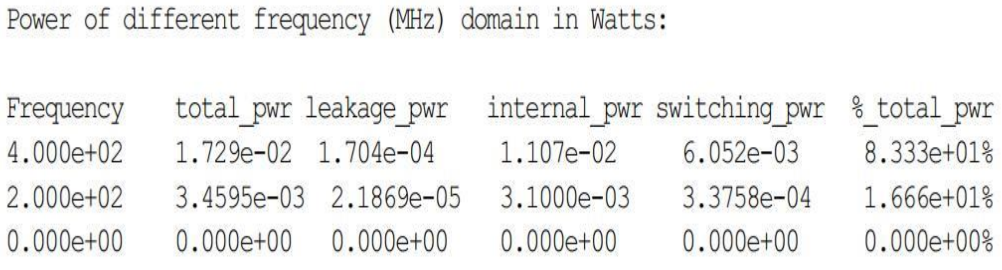
Rmin is the minimum value of the Rinst and Rmax is the maximum value of Rinst.

Static IR drop can also occur due to weakly connected instances to the power/Ground mesh. Via on a metal layer act a current divider. Therefore, more via’s on a metal means it divides the current in more paths. More current paths, lead to smaller length of the segment having current flowing through it, thus, reduces resistance, and hence voltage drop reduces. Because of via-to-via DRC issue, again, we can’t add more via’s on the metal. Thus, increase in the resistance of minimum resistive path, the Static IR drop will also increase.

4.1.1.6. POWER SUMMARY

Different types of cells are present in a design. Every cell in a design is not intended to operate at same frequency, so different cells in a design must be having different frequencies, again based on these frequency values, leakage power, internal power, switching power and total power will vary.

Power has components – Static component and Dynamic component. As the name suggests that the static component is defined by the leakage current in the design, and Dynamic IR component is defined by the internal power and switching power of the design. More is the value of these components, more will be the power dissipation. For least Static IR drop, leakage power should be less and for least Dynamic IR drop, internal and switching power should be less.

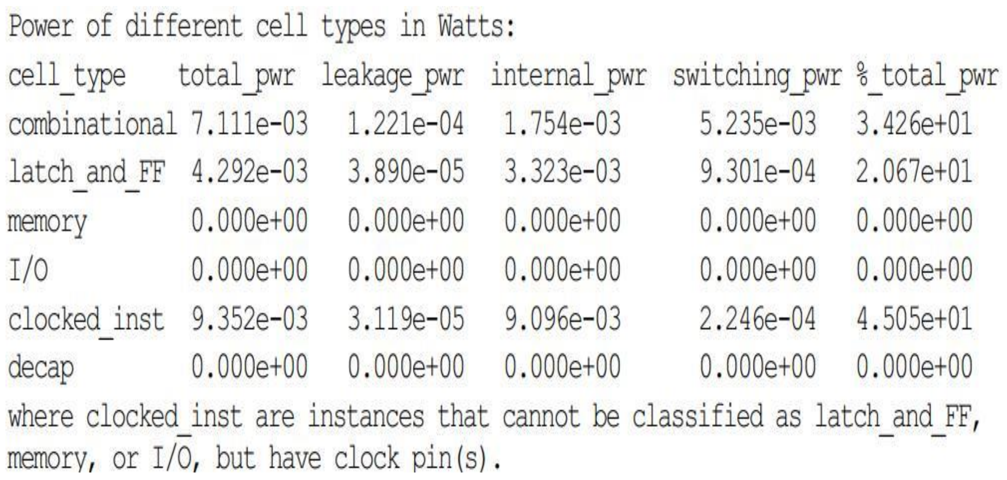


```
Power of different frequency (MHz) domain in Watts:

Frequency     total_pwr leakage_pwr   internal_pwr switching_pwr  %_total_pwr
4.000e+02     1.729e-02  1.704e-04     1.107e-02     6.052e-03      8.333e+01%
2.000e+02     3.4595e-03  2.1869e-05   3.1000e-03    3.3758e-04     1.666e+01%
0.000e+00     0.000e+00   0.000e+00    0.000e+00     0.000e+00      0.000e+00%
```

Figure 4.3 Report 1 for different powers in a design

Report 1 gives the internal power, leakage power and switching power in the design based on frequencies used in the design. Power dissipation in the design based on type of circuits used in the design like, combinational, clock, memories, etc. This is described in the Figure 4.4. Memories are more complex than Standard cells in the design. Although, designing process and adding memories and standard cells in a design is same, but difference lies in the logic functions of the chip. More the logic functions are there in a design, it will dissipate more power. Therefore, on a whole at SOC level or block level, it should be taken care that the memories in the design should dissipate less power. That is, the drop across them should be less in order to make design more robust to IR drop.



```
Power of different cell types in Watts:
cell_type     total_pwr  leakage_pwr  internal_pwr  switching_pwr %_total_pwr
combinational 7.111e-03   1.221e-04    1.754e-03     5.235e-03     3.426e+01
latch_and_FF  4.292e-03   3.890e-05    3.323e-03     9.301e-04     2.067e+01
memory        0.000e+00   0.000e+00    0.000e+00     0.000e+00     0.000e+00
I/O           0.000e+00   0.000e+00    0.000e+00     0.000e+00     0.000e+00
clocked_inst  9.352e-03   3.119e-05    9.096e-03     2.246e-04     4.505e+01
decap         0.000e+00   0.000e+00    0.000e+00     0.000e+00     0.000e+00
where clocked_inst are instances that cannot be classified as latch_and_FF,
memory, or I/O, but have clock pin(s).
```

Figure 4.4 Report 2 for different types of cells in a design and power associated with them

4.1.1.7. Types of Issues Faced

Case 1: Weak Grid

In the case of higher current flowing through the metal, due to resistivity of metal involved, will cause more IR drop. The best solution to avoid this type of issue is providing more paths for the current to flow. Thus, it will reduce the current flowing through the device, then it will definitely cause the IR drop to reduce.

Case 2: High Impedance of the Path

The increased impedance of path is something unpredictable type of issue. During placement and routing, it can be predicted that the value of impedance of the path will be more. So, after analyzing this scenario, we will have to think of a solution that the value of the impedance is reduced down to some other value that can be accepted for the design. This issue can be resolved in various ways depending on the maximum resistance difference occurring on a metal and pin. This can be resolved by adding vias or providing more path as more number of parallel wires will be resulting in reduced resistance.

Case 3: High Package Parasitics

Package Parasitics is also a critical part of analysis. It includes all the power locations in the design. If more than required power is coming in the design, it will definitely cause voltage drop. Also, there might be some power hungry devices in the design, which may require more power. So, sufficient amount of power locations are required. Both count of power pads and location of power pads plays important role in Static IR analysis.

4.1.2. Dynamic IR Drop

The Reason for the Dynamic IR Drop is the fast toggling of the standard cells. When these fast toggling cells are sitting near, then it will increase the peak current flowing through the device. This peak current gets multiplied to the resistance of the metal grid, causing higher Dynamic IR Drop. The Reason for Dynamic IR is that the grid is not robust enough to carry the current caused by the high toggling cells in the design. Sometimes cluster of high toggling cells results in Dynamic IR but single high toggling cell in the design can also result in Dynamic IR Drop.

4.1.2.1 Inputs required for the Dynamic IR drop and Outputs generated

The inputs required and various outputs generated to perform the Dynamic IR drop are shown in Figure 4.5

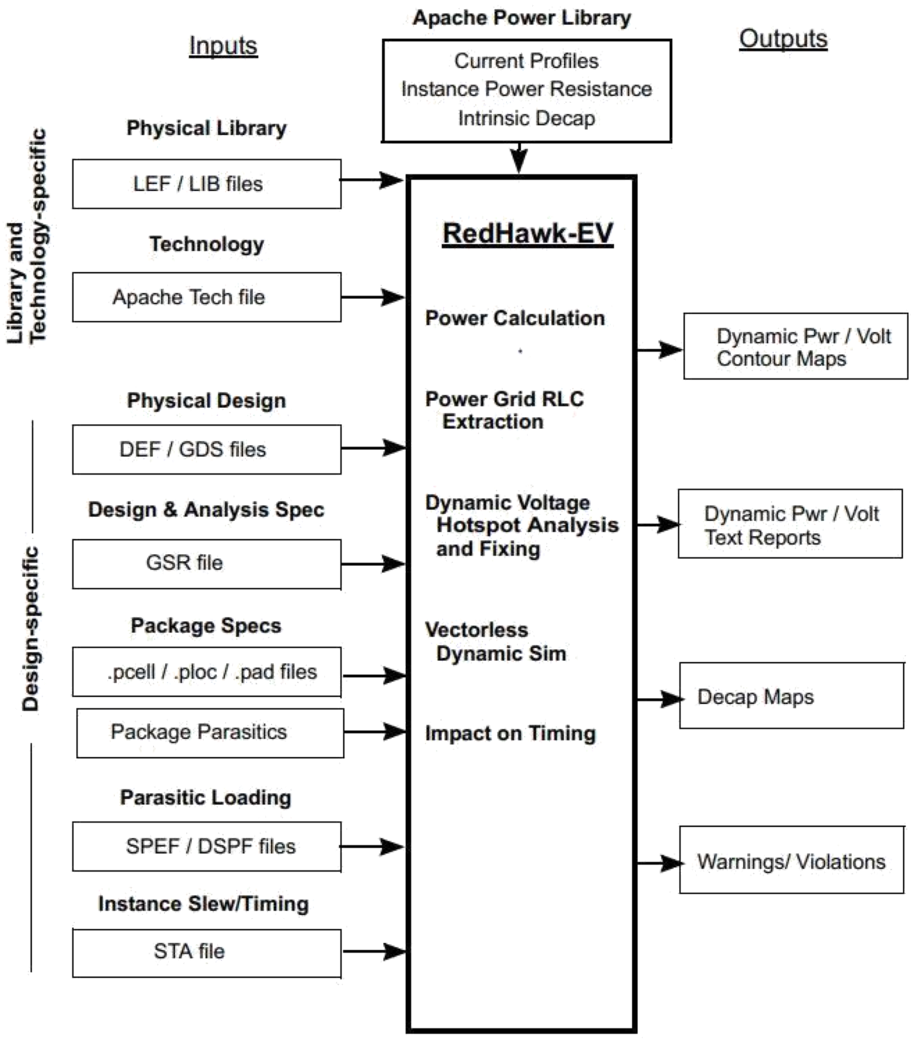


Figure 4.5 Inputs required and output generated to perform Dynamic IR drop

1. DEF (Design Exchange Format): This file is required for performing all the analysis, no matter it is Static IR analysis or Dynamic IR analysis. Because it will give the complete design related information. If in a design, we have multiple def files then we need to specify every def files with extension "top" at partition level.

2. LEF (Library Exchange Format): LEF file is used for both Static IR and Dynamic IR analysis. This file or input is again a standard file format, required for getting coordinates of all the design related things.

3. SPEF (Standard Parasitic Extend Format): This input file will contain all the parasitic values like R and C values of the design. This file is required for the Dynamic IR analysis, else actual values of load capacitance or higher effective resistance will not be covered in the analysis, else it would have picked default values from the flow.

4. Timing Information File (or STA file)

(a).Timing window files are required by the tool to perform Dynamic IR analysis, irrespective of Voltagestorm from Cadence or Redhawk from Ansys. This file contains all the information of instance wise minimum and maximum transition times and defines the clock network of the data.

(b). The Timing file is required for the Dynamic analysis. If this file is not present than the tool, by default will consider that the power of all instances is zero. Dynamic IR Analysis is based on the toggling of the cells. If all the cells with maximum transition time will toggle at the same rate then the Dynamic IR will be more.

(c). The file or input is required to get the switching activity report of all the standard cells in the design. If the standard cells are toggling fast, then more chances of getting dynamic IR. This input is required not only for standard cells. Other types of cells in the design will not contribute in the dynamic IR. Because only functional cells in the design are standard cells, rest other cells in the design are not contributing in the functionality of the design, but are required for some other purposes.

(d). Based on the corner conditions, like minimum and maximum corner conditions, we can perform analysis more accurately. For Dynamic IR, we need the max corner information, because it will provide the max. toggle rate and other parameters of the design. To deal with worst case-scenarios, max corners are required.

4.1.2.2 Factors on which Dynamic IR depends :

Dynamic IR depends on three factors, which are described below.

1. Toggle Rate,

2. Frequency,

3. Load capacitance

1. Toggle Rate: Dynamic IR drop is mainly depending upon the toggle rate. More cells are placed near to each other in a cluster having more toggle rate will cause more Dynamic IR drop. This is because, if cells are toggling at higher rate, then the peak current will be more. Hence, more drop will be observed.

As, we can see that from the graph as shown in Figure 4.6, the I-V characteristics curve, that when the toggle rate of a cell is high, then peak current will be high because of high rise time and high fall time.

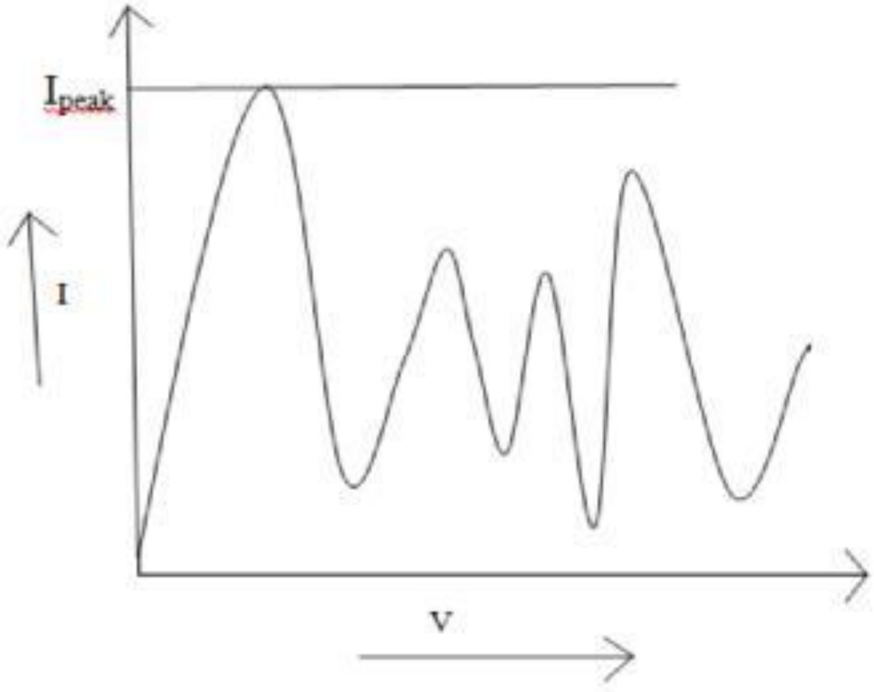


Figure 4.6 Peak current

The other alternative is to add Decap cells in the design because of their functionality. Decap cell is nothing but decoupling capacitor, which will not allow DC to flow. Decap cells act as a capacitor which will get charged when more current is flowing through the device is more and will get discharged when the current is not sufficient in the design.

2. Frequency: In the design, if the frequency of the standard cells is higher, then it means that the time period to charge and discharge the load capacitance related is small. As current and frequency are directly proportional to each other, thus it will result in more drop and hence higher power dissipation.

3. Load Capacitance: The load capacitance also plays an important role in dynamic IR calculation. If the load capacitance is more, then the rise time and fall time will be steep, hence, the peak current will be more. This will result in dynamic IR drop. Also, more is the load capacitance, current requirement will be more through that cell, which will ultimately result in higher drop.

4.1.2.3. Requirement of Dynamic IR Analysis

There are three types of power dissipation in CMOS design – leakage power dissipation, short-circuit power dissipation and Dynamic power dissipation. Leakage power dissipation and short-circuit power dissipation depends on the fact that how we fabricate them. While dynamic power dissipation is due to charging and discharging of the load capacitance. If the current charges and discharges immediately, then the peak current will be high. If peak current is more, then the dynamic IR drop will be more. Average power dissipation due to charging and discharging is shown in Equation 7.

$$\text{dynamic} =^{2} \qquad \frac{\Sigma \ =0}{{}_{2}} \tag{4.4}$$

Where, Pdynamic is the dynamic power dissipation,

Vdd is the operating voltage of the design,

K is the total number of nodes,

is the toggle rate of the ith node ,

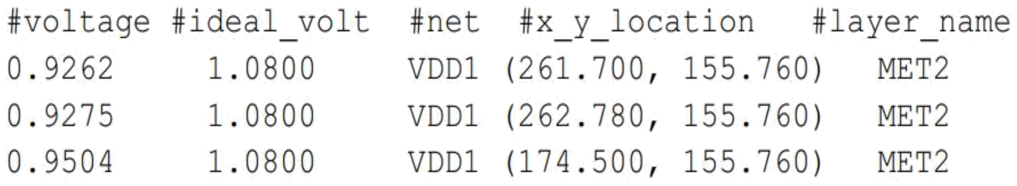
is the load capacitance of the ith node ,

is the time taken by the clock period.

Power dissipation at the circuit level depends upon toggle rate only. This is because out of other factors, few will be either constant depends on designing or fabrication. Toggle rate will result in higher peak current. If the Metal grid is not robust enough to carry that current then Standard cells might not work if they are not able to get the sufficient operating voltage. Thus, design will not work properly and hence, IR Drop is of more concern.

4.1.2.4. Reports Generated

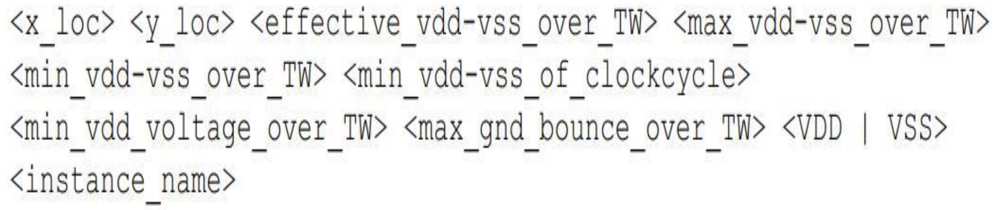
Dynamic IR is reported in the form of text file, which contains all the information related to the Dynamic IR drop occurring in the design. Reports are generated as shown in the Figure 4.7



```
#voltage #ideal_volt  #net  #x_y_location    #layer_name
0.9262     1.0800     VDD1 (261.700, 155.760)   MET2
0.9275     1.0800     VDD1 (262.780, 155.760)   MET2
0.9504     1.0800     VDD1 (174.500, 155.760)   MET2
```

Figure 4.7 Report 1 for Dynamic IR

In the Figure 4.7, information related to layer, location of Dynamic IR drop on the (x,y) location is given. It also contains the information related to net on which it is occurring. The figure below reports the difference in vdd-vss coming from the timing window.



```
<x_loc> <y_loc> <effective_vdd-vss_over_TW> <max_vdd-vss_over_TW>
<min_vdd-vss_over_TW> <min_vdd-vss_of_clockcycle>
<min_vdd_voltage_over_TW> <max_gnd_bounce_over_TW> <VDD | VSS>
<instance_name>
```

Figure 4.8 Report 2 for Dynamic IR

In the Figure 4.8, report is shown and is used to calculate the Dynamic IR drop. Here only attributes are defined but when we run Dynamic IR on the design, this file will contain data. The amount of drop coming in the design can be calculated using the Dynamic IR formula as described and the required information can be gathered from this report. The percentage of dynamic IR that is coming in the design, can be accepted or not depends on the design itself. More than the desired drop coming in the design needs to be fixed.

4.1.2.5 Real Cases in Dynamic IR Drop Reduction

Case 1: Weak Grid

In case of weak grid, the metal resistance is constant but the current flowing through that path will be more, thus it will cause more drop. In order to overcome with this problem, grid should be robust enough to carry current through it. The robustness of the grid is important to all the power related issues. More robust the power/ground grid will be, more current will be divided and hence drop will be less.

Case 2: Cluster of High Toggling Cells

Due to simultaneous toggling of cells will result in high peak current. Thus dynamic IR drop will be more. In order to tackle such a situation, we need to decluster all the cells. When we decluster these high toggling cells, then it will reduce peak current flowing in that area, thus it will reduce the dynamic IR drop over that area.

Case 3: Single cell sitting at one side of the design with high toggle Rate

This is a very typical scenario if the grid of the cell is fine and the still the peak current is high. In this case, the only option left is that we need to add decap cell, such that it will be get charged if the current flowing in the grid is high and the decap cell will get discharged if the current flowing in the grid is very less. Thus, the decap cell will act as a reservoir of charge storage.

4.1.3. Relationship between timing and IR drop analysis

IR drop and Timing issues are closely related to each other. By Timing issue, we mean here Setup and Hold Violations. Any Circuit in VLSI has two types of path in the circuit, which is clock path and Signal path. High IR drop on clock path causes Hold violations whereas High IR drop on signal path causes setup violations. Out of setup and hold violations, hold violation is bad for chip designing. Fixing hold violations is more critical because hold violations are coming because of High IR drop on clock path. Timing issues can be resolved by adding buffer in between the timing critical path. Again, addition of buffer in the long route will not reduce the current the amount of current flowing through the circuit but it will reduce the current flowing in that area. This, it will reduce the IR drop coming on that particular net.

4.2 ELECTROMIGRATION (EM)

Electromigration is a very critical part in VLSI design. It is the property of metals on which lifetime of a chip depends. It we meet our criteria then only we can make the chip to work for that particular time period. Electromigration or EM is the property of metals that helps in finding the temperature effect in metal. So, we can say that in order to meet the electromigration criteria's, we need to have knowledge of current per unit area (or current density) in that metal.

Till date, we have so many hand-held devices in our homes, work-places and public-places, etc. we have seen that in small hand-held devices, the major issue is heating up of the device. This is because of small area of the devices. Small area of the chip means if there is a large current injection in a place, then current per unit area will increase, which may lead to increase in local temperature, which may further lead to electromigration effect. This increase may lead to increase in electromigration in other metal straps also. So, we can conclude that there are two types of nets while calculating the electromigration:

1. Aggressor: As the name specifies, the net which will cause the more current to flow through a particular unit area is called Aggressor. This net will result in increase in local temperature.
2. Victim: The other nets which are affected by the increase in the local temperature of the aggressor net causing them to increase the local temperature, are called Victim nets. It is always mandatory to fix Aggressor nets, but the Victim nets will depend upon the change in temperature.

4.2.1. Inputs Required for Electromigration

Different inputs required for Electromigration analysis are:

1. DEF (Design Exchange Format): This input file contains all the design related information. This file is a standard file format followed everywhere to get the design information. For all the IR/RV related information and analysis, this input is required. For multiple DEF files in the design, we need to specify every def files with extension "top" at partition level.
2. LEF (Library Exchange Format): This input file format is again a standard file format, which is required to perform all the analysis for IR and RV. If LEF file is not present then the tool will not be able to understand various things. Thus, it will provide some error and we will not be to perform analysis.
3. Timing window file – (with max corners): Timing Window plays a critical role in the EM calculation. Timing Window contains all the information of the design related slew information, toggling information, frequency of the design. Max corner information is required for performing the EM analysis because of performing pessimistic analysis. If timing window is not present then the tool will put default power of the design as zero. So, performance and analysis will be based on the false criteria's.
4. SPEF – (with max corners): This input file is required to get all the R and C values. Again for optimistic approach, we go for max corner. If we are going for max corners, it means we are assuming maximum values of R and C, in this way, we are excluding the fact in worst case how the chip will behave or taking care of all the possible cases under which the chip failure can be caused.

These files are mandatory for the electromigration analysis, rest input files depends on the methodology followed for the analysis and debug.

4.2.2. Factors affecting EM

Electromigration depends on many factors, which are as follow:

1. Rise in Temperature:

The temperature of the metal is counted as the main factor in electromigration. The metal has some temperature due to flow of electrons. If more current starts flowing in the metal, then the temperature of the metal will increase. If this change is more, then the aggressor and victim nets also need to resolve. Thus increase in local temperature will result in increase in electromigration effect. This increase in temperature, can be mathematically explained as:

$$\Delta = T2 - T1 \tag{4.4}$$

In this above Equation, T1 is the actual temperature of the net,

T2 is the temperature of the net after the aggressor net come into picture.

and, Δ is the change in the temperature.

Thus, we can conclude that for better reliability of the chip, Δ should be less. The reason is that the rise in temperature of the one net may rise the global temperature of that area, thus it may increase the temperature of nearby nets.

2. Frequency

Frequency is nothing but a way to measure how fast our device or chip is responding. Lesser the slew, more fast the device will work. With more functionalities incorporated in a chip, requirement of zero or positive slew is increasing. Thus, with this scenario, the toggling rate of the cells should be more, which will further impact frequency of the chip. By default, the toggle rate (in percentage) of the signal coming on the net should be 100% and toggle rate (in percentage) coming on the signal should be 200%. It means, data will toggle only once in a clock period and as clock frequency is half than the signal frequency, so it will toggle twice. If any signal or clock toggle rate is coming more than this value, then it is called as Violation. Thus, the Frequency issue is very critical issue in the design.

3. Load Capacitance

Load capacitance is one of the key factor responsible for electromigration (EM), if a cell or instance is placed somewhere such that the load capacitance is high, then those load capacitances or those cells will try to draw more and more current from the driver cell, such that it will not be able to supply them with sufficient amount of current, so it will try to provide current to the load cells, which will cause increase in current density, thus will cause electromigration. For better reliability of the chip, it is good choice that number of loads which driver cell will drive should be made according to the capacity of the driver cells. For more loads to carry, more strong the driver cell needs to be. Thus, upsizing the driver size or splitting the load is the optimal solution if the load capacitance is higher for a particular standard cell.

4.2.3. Mathematical calculations of Electromigration:

Electromigration or EM is nothing but the factor of current flowing through the metal and current limit allowed to flow through the device. Depends on the chip, we can set the value to some random number, then, according to that, we can decide the violation.

Mathematically EM is calculated as:

$$\mathrm{EM} = \frac{\mathrm{Irms}}{\mathrm{Ilimit}} \tag{4.5}$$

Where Irms is the current flowing in actual in the metal and Ilimit is the max amount of current which is allowed to flow in that metal. For different chips, based on different logics and functions, this ratio will vary. In order to calculate EM in percentage, we simply need to multiply this ratio with 100. Then we will get % EM. Again Irms can be defined as:

$$\mathrm{Irms} = \surd\!\int \ (\ )^{2} \quad / \tag{4.6}$$

Where, Irms is the RMS current flowing through the metal,

$\int \ (\ )^{2}$ is the total current flowing the device,

dt is the change in the time period between two peak currents

tp is the input time period of the peak current spike between its 50% rise time and 50% fall time.

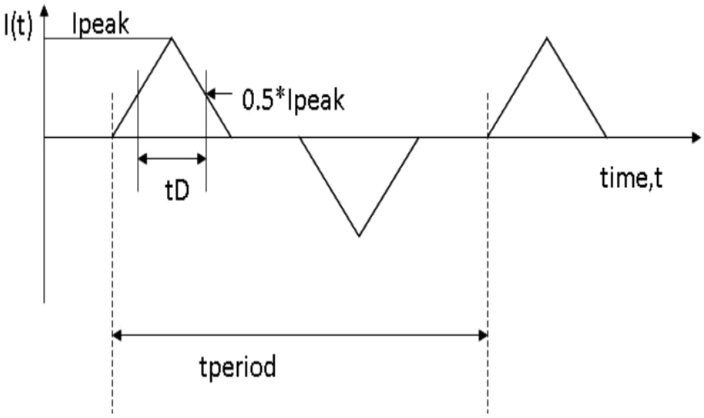


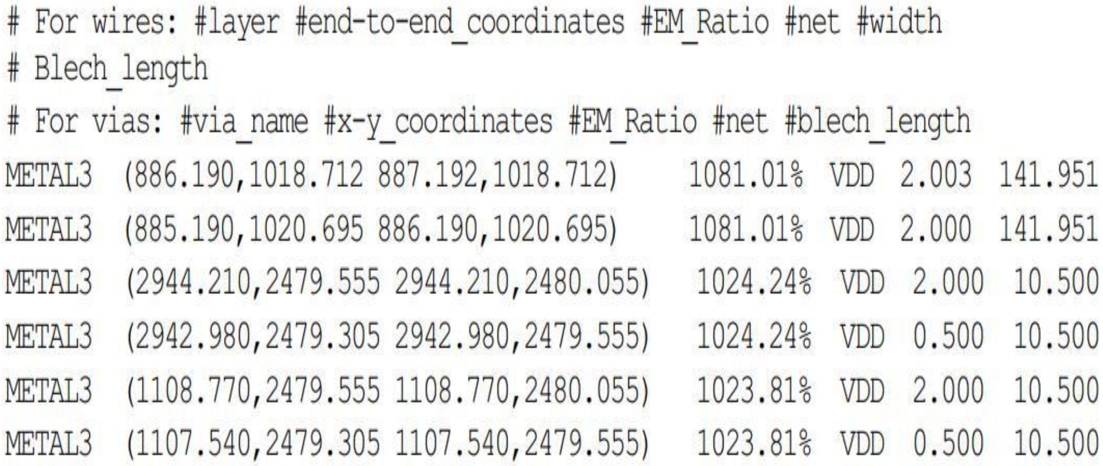
Figure 4.9 Variation of current with time period

In the Figure 4.9, the I(t) characteristics are shown. This graph is incorporating current flowing per unit time in all the metal layers.

In Real Scenarios, it is always difficult to fix the electromigration (EM) coming on a net or metal. To design is deprived of Electromigration issue with newer technology nodes. It’s always a challenge to fix them. Different criteria’s are followed by different people to fix them.

4.2.4. Report generated for Electromigration

The amount of Electromigration in the design can be reported in the form of text file. Based on this, we can decide the EM critical nets in the design. Report generated is as follow:



```
# For wires: #layer #end-to-end_coordinates #EM_Ratio #net #width
# Blech_length
# For vias: #via_name #x-y_coordinates #EM_Ratio #net #blech_length
METAL3  (886.190,1018.712 887.192,1018.712)     1081.01% VDD 2.003  141.951
METAL3  (885.190,1020.695 886.190,1020.695)     1081.01% VDD 2.000  141.951
METAL3  (2944.210,2479.555 2944.210,2480.055)   1024.24%  VDD  2.000  10.500
METAL3  (2942.980,2479.305 2942.980,2479.555)   1024.24%  VDD  0.500  10.500
METAL3  (1108.770,2479.555 1108.770,2480.055)   1023.81%  VDD  2.000  10.500
METAL3  (1107.540,2479.305 1107.540,2479.555)   1023.81%  VDD  0.500  10.500
```

Figure 4.10 Report for Calculation of Electromigration

In the Figure 4.10, the EM report is shown. It contains all the data required to get the information regarding the EM occurrence on a design like on which metal layer EM is coming and on which type of net (either power/ground net or signal net) EM is coming, including the percentage of EM coming on that particular metal layer. Fixing of EM depends on the design and other technology-factors.

4.2.5. Real Scenarios Based on EM

Case 1: Long Route

In a design, if a cell is deriving another cell, is not an issue. Because, in that case, output load is not high. So, it will not create any kind of EM issue. But, if the route between the two cells is long, then the current flowing per unit area (i.e. current density) will increase. Thus, EM % will increase. To reduce this we can apply some technique such that which can divide the current flowing through the metal. For this we can add buffer somewhere in the route.

Case 2: High Load at the output

If a cell or driver is driving so many cells, then the load capacitance of the cell will be high. The EM basically depends on the input transition and output capacitance. If the output capacitance is more, then the driver cell will have to provide more current in order to support the functionality of the load cells. But, as we know that capacitance and current are both directly proportional to each other. Thus, more is the output capacitance, more will be the current flowing per unit area, this will result in the rise in default temperature of the net in the form of power dissipation in the form of heat. To avoid this, we can split the load. This will reduce the output capacitance.

Case 3: High frequency of the standard cell

More is the frequency, more will be the current flowing through the metal, hence, current density will increase. This will again increase the EM % coming on the net. In order to deal with high frequency, will need to check few criterias like length of route, load capacitance, addition of parallel path, via laddering, etc. If this is a real issue, then addition of parallel path or addition of via ladder will be of greater help if load capacitance is fine and also the length of the route is not much long.

CHAPTER 5

SIMULATION RESULTS

5.1 Simulation Results for Static IR, Dynamic IR and EM related issues

5.1.1 Static IR Results :

In the below figure 5.1(a), Red colour in the IR drop map depicts the area with higher percentage of Static IR drop in the design. The limit of Static IR drop (in percentage) in this design is taken as 10 %.

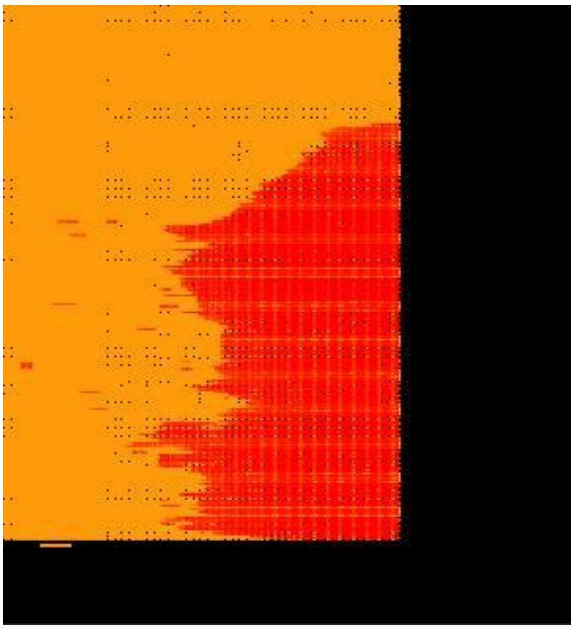


Figure 5.1 (a) Static IR Drop Map Before Fixing

In the Figure 5.1 (a), the Static IR observed is 15%. The reason for this Static IR drop is weak metal grid. Weak Metal Grid in this design means the power and ground connections are there for that particular domain cells, but the tappings or paths are less, such that the more current is flowing in that area, resulting in more Static IR Drop.

In the Figure 5.1 (b), it can be seen that no red spots are there indicating no Static IR violation above 10%.

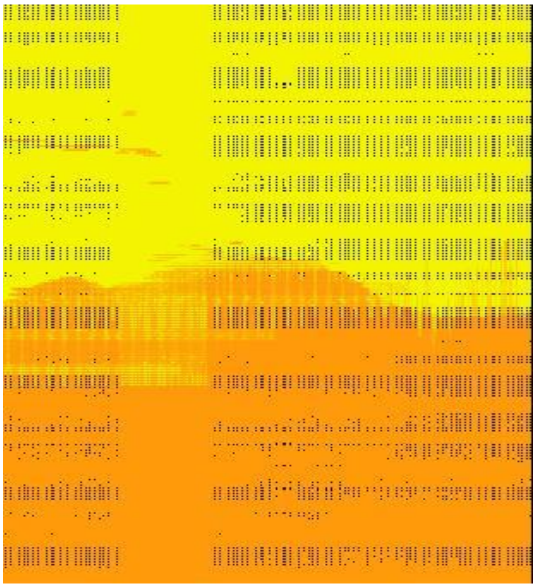


Figure 5.1 (b) Static IR Drop Map After Fixes

The Static IR violation is reduced down to 9% by adding more parallel paths. In this way, current is divided in many paths as current follows low resistance paths. Thus, the Static IR got reduced.

5.1.2 Dynamic IR Results

In Figure 5.2 (a), three red spots can be seen easily indicating the Dynamic IR violation above 30%. The Reason for 35% Dynamic IR Drop coming in this design is clustering of High toggling cells are placed close to each other, which causes increase in peak current in that area.

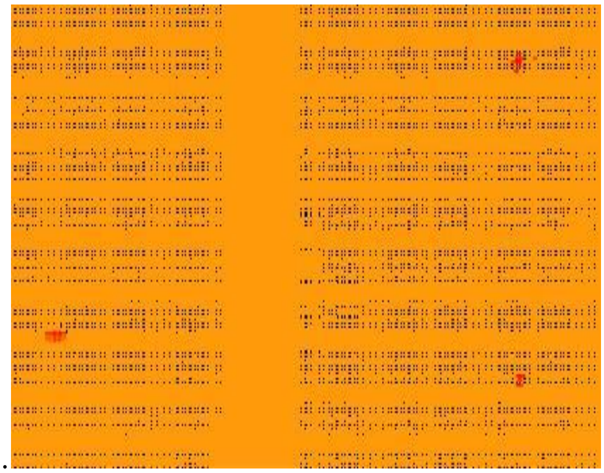


Figure 5.2 (a) Dynamic IR drop contour map without fixes

In the Figure 5.2(b), the Dynamic IR Drop observed is 28%, which is less than the Dynamic IR limit which will not affect the design.

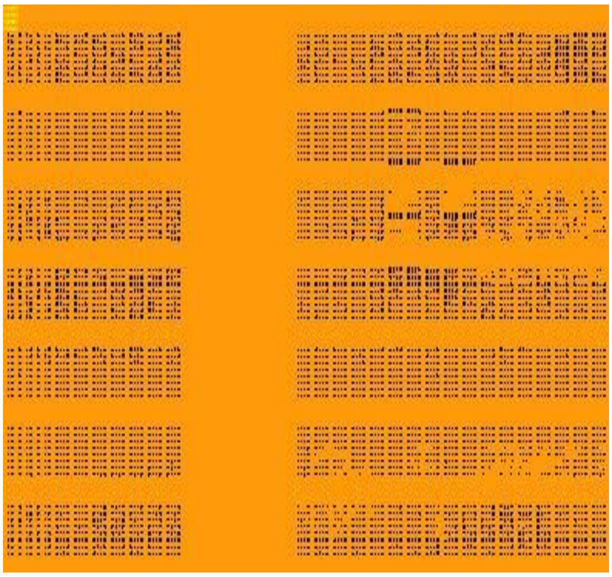


Figure 5.2 (b) Dynamic IR Drop Map with fixes

The Dynamic IR Drop got removed by declustering the high toggling cells. By declustering the high toggling cells, the grid is robust enough to carry the current. Thus, peak current will not cause any kind of Dynamic IR issue.

5.1.3 Electromigration

The EM percentage that will not cause any issues in the design is 400%. By calculating the EM percentage from the Equation 9, the EM percentage seen in the design is 550%. The reason for the Electromigration is high output load capacitance. Due to high load capacitance, the current density is high, which is leading to higher percentage of electromigration. This might increase the local temperature by as shown in Equation 8 in metal grid, if not fixed, and may also cause other nets to violate and will show higher percentage of EM.

Figure 5.3 Electromigration

The EM issues observed in the design are brought down to 380% by splitting the load, which will reduce the current density by reducing the current carrying capacity of the driver cell.

CHAPTER 6

CONCLUSION AND FUTURE WORK

The chip designing has becoming a challenging task with the advancement in the technology. Reliability of the chip includes IR Drop and EM. As far as power is concerned with the design, it is needed to minimize the drop as much as possible. When it comes to design a chip (in real scenarios) when any consumer buy any electronic device like mobile phones, laptops or any other device, the main ask is about the battery backup. As a consumer, no one prefers to buy a phone which will radiate heat like a microwave oven. So, it is designers, duty to meet the Static IR and Dynamic IR drop limits of the chip along with the resolving the Electromigration related issues.

But, the challenging task here is that with advancement in the technology, various factors will have to be taken care while meeting all the IR Drop related issues EM related issues. Fixing one thing might affect the other factors in the design, not necessary that those factors will be related to power only. These issues might cause timing violations or DRC’s in the design. So, with the upcoming technologies, more accuracy need to be maintained. With the advancement of the technology, cost parameters are area, power and performance. If area is reduced, performance is enhanced, what if the power dissipation is more? The answer is no one will buy that product. In this way, Power is one of the critical aspects of the design. Moreover Routes are becoming smaller and congested, which makes the process of fixing IR drop and EM a bit challenging task with latest technology nodes.

Table 6.1 Variation in IR drop and EM with different technologies

Technology Node	Static IR Drop	Dynamic IR Drop	Electromigration
45 nm	Low	Low	More
32 nm	Low	Low	More
28 nm	Medium	Low	More
22 nm	Medium	Medium	More
14 nm	More	Medium	Less
10 nm	More	More	Less
7 nm	More	More	Less

From the Table 6.1, it can be observed that with the advanced technology, one need to be more accurate about the IR drop and EM related issues in the chip. For this purpose, the design should be robust at the initial phase of implementing the design. In future, in order to increase the speed and improve the performance of the chip, it is recommended to Route at the higher metal layers.

Memories or other IP’s (intellectual property), which are used in the design, the drop across them should not be higher than the limit. This can be achieved by taking the IP from other vendors and modifying according the requirement of the design. Thus in future, it can be make sure that our design is more compact and reliable by improving the grid, load capacitance, frequency of the design. Every HIP and route of the circuit is needed to taken care more vigilantly, so that one can acquire more accuracy in the chip in terms of Static IR drop Dynamic IR Drop and EM such that they will not affect the performance of the design.

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