Analysis of Depletion Region Width and Breakdown Voltages of 6H-SiC DIMOSFET Using Linearly Graded Profile in the Drift Region

A Thesis submitted towards the partial fulfillment of the requirements for the award of the degree of

Master of Technology
in
VLSI Design & CAD

Submitted by
Indra Mani Sharma
Regn. No. 601061031

Under the supervision of
Dr. A. K. Chatterjee
Professor and Head, ECED, Thapar University

DEPARTMENT OF ELECTRONICS & COMMUNICATION ENGINEERING
THAPAR UNIVERSITY
PATIALA – 147004, PUNJAB, INDIA

JULY 2011

CERTIFICATE

I, Indra Mani Sharma hereby certify that the work which is being presented in this thesis entitled "**Analysis of depletion region width and breakdown voltages of 6H-SiC DIMOSFET using linearly graded profile in the drift region**" by me in partial fulfillment of requirements for the award of degree of **Master of Technology in VLSI Design and CAD** from **Thapar University, Patiala** is an authentic record of my own work carried under the supervision and guidance **of Dr. A.K. Chatterjee**, Professor and Head, Electronics and Communication Engineering Department, Thapar University, Patiala.

The matter presented in this thesis has not been presented in any other University or Institute for the award of any other degree.

INDRA MANI SHARMA

Regn. No. 601061031

This is certified that the above statement made by the candidate is correct to the best of my knowledge and belief.

Date 26.7.11.

Dr. A.K. CHATTERJEE
Supervisor
Professor and Head ECED,
Thapar University
Patiala-147004

26.7.11.

Dr. A.K. CHATTERJEE
Professor and Head ECED
Thapar University
Patiala-147004

Dr. S.K. MOHAPATRA
Dean of Academic Affairs
Thapar University
Patiala-147004

ACKNOWLEDGEMENT

First of all, with a deep sense of gratitude, I wish to express my sincere thanks to my supervisor, **Dr. A. K.Chatterjee** (Professor & Head), ECED, Thapar University, Patiala, for his patient guidance and support throughout this work. I am truly very fortunate to have the opportunity to work under him as a student. It was both an honor and a privilege to work with him. He also provides help in technical writing and I found this guidance to be extremely valuable.

I take this opportunity to express my gratitude and sincere thanks to **Dr. Alpana Agarwal, Associate Professor,** Electronics & Communication Engineering Department, all the staff members of Electronics & Communication Engineering Department for providing me all the facilities required for the completion of this work.

I wish to thank all my classmates for their time to time suggestions and cooperation. Also I would like to thank **Mr. Arun Kr. Chatterjee,** Assistant Professor, ECED, for their suggestions and encouragement during thesis work. I thank and owe my deepest regards to all of them and all others who have helped me directly or indirectly.

Finally it is the support, encouragement and good wishes of my parents and other family members without which I would not have been able to complete my thesis.

My acknowledgements would not be complete without expressing my gratitude towards God. I feel very fortunate to come to know Him during my post-graduate years at Thapar University and have continually been blessed by His endless love ever since. He is the true shepherd of my life.

INDRA MANI SHARMA

Regn. No. 601061031

ABSTRACT

The thesis work carried out here on 6H-Silicon Carbide Double Implanted Power MOSFET has been an attempt to understand the analysis of the depletion region width and breakdown voltages for various types of doping profiles in the drift region of the device. The doping profiles used are primarily uniformly doped and linearly graded doping profile in the drift region.

The ultimate aim for making this study is to provide a graded profile in the drift region of the MOSFET with lower doping at the top of the device near the source to a higher doping near the drain. This type of profile will help in increasing the breakdown voltage. Breakdown voltages selected for the purpose of analysis ranges from 1kV to 20 kV. It has been established that the linearly graded device can be used easily to obtain much higher values of critical electric field than uniformly doped device. For linearly graded devices with precalculated device heights, it was found that Punch through and Avalanche breakdown voltages were almost equal for all values of gradients and N_{eff} for linearly graded DIMOSFETs. This can be verified from Table 5.6. However this type of tally is not seen in the case of uniformly doped devices as shown in Table 4.4. Here breakdown voltages V_{bpt} and V_{bav} are found to be nearly equal only in the case of doping level of 10^{15} /cc for V_{bpt} of 5kV, 10kV and doping level of 10^{16} /cc for V_{bpt} of 1kV. Equivalence of these two breakdown voltages have not been established for other doping levels and breakdown voltages.

It has been shown that at the expense of an increase in the depletion region width of uniformly doped drift region devices of 6H-SiC DIMOSFET, the magnitude of critical field E_c and V_{bpt} and V_{bav} can be significantly increased by decreasing the magnitude of the concentration gradient in the drift region.

TABLE OF CONTENTS

LIST OF ACRONYMS

SMPC	Switched mode power conversion
PE	Power electronics
kHz	Kilohertz
MOS	Metal oxide semiconductor
MOSFET	Metal oxide semiconductor field effect transistors
Si	Silicon
BJTs	Bipolar junction transistors
IGBTs	Insulated-gate bipolar transistors
GTOs	Gate turn-off thyristors
SiC	Silicon carbide
GaN	Gallium nitride
Cu	Copper
WBG	Wide Band Gap Semiconductor
DRAM	Dynamic Random Access Memory
GaAs	Gallium Arsenide
SOI	Silicon-On-Insulator
SBD	Schottky barrier diode
JFET	Junction field-effect transistor
Ti	Titanium
Ni	Nickel
IMPATT	Impact- ionization Avalanche Transit-Time
CCD	Charge Coupled Devices
CMOS	Complementary MOS
LDMOSFET	Lateral doubled diffused MOSFET
SiO_2	Silicon Dioxide
RIE	Reactive Ion Etching
Fig.	Figure

NOTATION

Symbol	**Description**
E_g	Band Gap energy
χ	Electron affinity
E_v	9˚°˚ı˝˘#¸˚ı˛#˘ı˘ßÆÊ#
E_c	Conduction Band Energy
eV	Electron Volt
H	Hexagonal
C	Cubic
R	Rhombohedral
R_{on}	On-state Resistance
R_{dson}	On state drain resistance
CO	Carbon Monoxide
IC	Integrated Circuit
μ	Mobility
v_{sat}	Saturation Velocity
λ	Thermal conductivity
KV	Kilo-Volt
$R_{on\text{-}sp}$	Specific on-resistance
V_B	Breakdown voltage
N_d	Doping level or doping concentration at breakdown
ε_{SiC}	Permittivity of Silicon Carbide
ε_o	Permittivity of free space
μ_n	Electron mobility
E_c	Critical electric field
Wu	Depletion region width of abrupt P^+-N junction for uniformly doped Profile.

NOTATION Contd...

Symbol	Description
V_{bpt}	Punch through Breakdown Voltage
V_{BAV}	Avalanche Breakdown Voltage
W_g	Depletion Region Width of Linearly Graded Junction
G	Gradient of profile
N(x)	Desired doping density
N (0)	Lowest doping density, used as reference doping level for calculating the Gradient at different desired doping density.
h	Device height (calculated using uniform doping profile)
e	Electronic charge ($1.6*10^{-19}$ coulombs)
V_g	Gradient voltage
N_{eff}	Effective doping concentration

LIST OF FIGURES

LIST OF TABLES

CHAPTER 1

INTRODUCTION

1.1 BACKGROUND

Power semiconductor devices are a key component of all power electronic systems. Large number of electric appliances and large amount of electricity are used in our daily life. The conservation of the global environment have been demanding the ecological appliances which are small, light, and also consume very little electricity. The switched-mode power-conversion (SMPC) circuits such as converters and inverters have been widely applied to power electronics (PE) applications, such as motor-control systems and home appliances, because of their high conversion efficiency. Carrier frequencies of typical SMPC circuits for home appliances are ranging from 1 kHz to 100 kHz [1]. The semiconductor switches and diodes are the key devices for the SMPC circuits. It is estimated that at least 50 percent of the electricity used in the world is controlled by power devices. With the wide spread use of electronics in the consumer, industrial, medical, and transportation sectors, power devices have a major impact on the economy because they determine the cost and efficiency of systems [2]. Modern society is increasingly dependent upon electrical appliances for comfort, transportation, and healthcare, motivating great advances in power generation, power distribution and power management technologies. These advancements owe their allegiance to enhancements in the performance of power devices that regulate the flow of electricity.

The power devices, which are based on Silicon, have long dominated the power electronics and power systems applications. Devices such as bipolar, unipolar, controlled, uncontrolled, and metal oxide semiconductor (MOS) - gated Si devices that are widely used by power electronics and power systems designers. Examples of such devices are diodes (p-i-n and Schottky rectifiers), bipolar junction transistors (BJTs), insulated-gate bipolar transistors (IGBTs) ,thyristors, gate turn-off thyristors (GTOs), and power metal–oxide–semiconductor field-effect transistors (MOSFETs). Large-area devices that are capable of handling thousands of amperes and kilovolts such as IGBTs are now able to handle voltages

up to 6 kV and currents up to 1200 A [3]. IGBTs are being widely used for motor drives, resonant converters, and power supplies. GTOs and thyristors are still widely used for very high power applications, such as power systems conditioning equipment, dynamic voltage regulators, transfer switches, and large direct-current rectifiers [4]–[7].

Silicon offers multiple advantages to power circuit designers, but at the same time suffers from limitations that are inherent to silicon material properties, such as low bandgap energy, low thermal conductivity, and switching frequency limitations. Wide bandgap semiconductors, such as silicon carbide (SiC) and gallium nitride (GaN), provide larger band gaps, higher breakdown electric field, and higher thermal conductivity. Power semiconductor devices made with SiC and GaN are capable of higher blocking voltages, higher switching frequencies, and higher junction temperatures than silicon devices. SiC is by far the most advanced material and, hence, is the subject of attention from power electronics and systems designers. Silicon Carbide is fast becoming a material of reckoning for manufacturing of high temperature high power integrated circuits. In addition to a large bandgap, high thermal conductivity and a very high breakdown field, the main characteristic that sets SiC apart from other wide bandgap materials, is its ability to grow a natural oxide. Like silicon, it is possible to grow silicon dioxide on a silicon carbide substrate. This characteristic of SiC makes it easy to manufacture SiC MOSFETs and other devices which have been traditionally made using silicon. Through the years since the first integrated circuit, silicon based devices have been able to meet the need for smaller, faster, cheaper, more reliable, and more diverse electronic circuits. But all silicon based ICs have faced limitations in terms of operating temperatures ($<150^{o}C$) and usable power. SiC based devices and integrated circuits will work at much higher temperatures, and much higher power, as compared to Si based devices.

Among all power-device structures, the metal–oxide–semiconductor (MOS)-controlled devices are favorable due to their high input impedance and low switching losses, which make power electronic circuits more controllable with higher efficiency [8]. MOSFETs have high conduction losses due to their high on-state resistance, R_{dson}. As the blocking voltage increases, so does their on-state resistance R_{dson}, hence, making MOSFETs less attractive for high-voltage applications (beyond 600 V). Recent enhancements in power MOSFET technology such as the CoolMOS allow for substantial reduction of the conduction losses [9].

Silicon carbide MOSFETs are more efficient than silicon MOSFETs because devices can have smaller area and thus smaller capacitance due to the higher doping densities and higher current density of the SiC material.

1.2 MOTIVATION

The high electrical breakdown field strength and the indirect band gap make it possible to design high voltage devices with low power losses. SiC based devices can operate at higher temperatures than Si devices due to the wide band gap and the high thermal stability. Heat produced by power losses is efficiently dissipated since the thermal conductivity of SiC is high, better than Cu. The high saturation drift velocity makes SiC attractive for high frequencies devices. In addition, SiC is chemically inert which allowing the device to operate in very harsh environments [10]. It is an ideal semiconductor material for implementation of devices used in high power switching and high power microwave applications. Devices used in these applications require high inversion layer electron mobility, low on-resistance and high breakdown voltage. Inversion layer nobilities obtained in 6H-SiC MOSFETS were about 10-50 cm^2 per V-sec, even lower in the case of 4H-SiC MOSFETs.

Dc-dc converters and ac drives are extensively used in power electronics, power systems, traction drives, and hybrid electric vehicle (HEV) applications, where diodes and MOSFETs are used as switching devices. These devices have to carry large currents during the ‘on’ state and have to sustain large blocking voltages during the ‘off’ state. The performance of the silicon- (Si)-based switches is approaching the theoretical limits in high power applications due to its intrinsic material properties. SiC is an alternate material that can be used to overcome the limitations of the Si-based switching devices. In case of SiC UMOS-based devices severe enhancement in high-field stressing in the gate oxides at the bottom of the etched trench, poor inversion channel mobility and low blocking voltage capability has seen.

Vertical structure is chosen because there was no problem of oxide breakdown at etched trenches and channel length of the vertical MOS transistor is not defined by lithography. This means no requirements for post-optical lithography techniques such as

x-ray, extreme ultra-violet, electron projection lithography, ion projection lithography or direct write e-beam which are possibly prohibitively expensive.

Vertical MOS transistors are easily made with both front gate and back gate which doubles the channel width per transistor area. This leads to an increase of packing density of at least a factor of four as compared to horizontal transistors. Vertical MOSFET prevents short channel effects from dominating the transistor by adding processes that are not easily realized in horizontal transistors, such as a polysilicon source to reduce parasitic bipolar effects or a dielectric pocket to reduce drain induced barrier lowering (dibl).

1.3 THESIS ORGANISATION

In the Chapter 1 applications and requirements of power devices has been introduced and requirements of Silicon Carbide has been discussed. This chapter also describes motivation behind this thesis.

Chapter 2 focused on the study of literature surveys of Silicon carbide and power semiconductor devices. In this chapter need of wide band gap semiconductor, need of silicon carbide as power semiconductor device material, crystal structure of Silicon carbide, transport properties, comparison of electronic properties of different semiconductor. A brief description about different poly types of silicon carbide, applications and benefits of SiC electronics has been presented.

In chapter 3 introductions of different silicon carbide devices has been nicely given. This chapter also reviews need of silicon carbide Power MOSFETS, types of SiC MOSFETS and their device structures has been given.

In Chapter 4 a brief description of 6H DIMOSFET has been discussed. Structure of 6H DIMOSFET, device theory, interface physics, breakdown voltage, model of Vertical DIMOSFET, device equations to calculate breakdown voltage and depletion region width using uniform doping profile, calculations, tables and related graphs for uniform doping profile has been presented.

In chapter 5 device equations to calculate gradients, depletion region width, electric field, breakdown voltage, effective doping for linearly graded profile has been given. Calculations have been made by varying drift region doping density (low doping density at source side and higher towards drain side). Also tables and related graphs for linearly graded profile have been presented.

Chapter 6 presents general conclusions and scope of future work of this thesis.

CHAPTER 2

LITERATURE SURVEY

Power semiconductor devices made from materials with bandgap energies larger than in Si have been touted for many decades. The potential advantages of these wide bandgap devices include higher achievable junction temperatures and thinner drift regions (because of the associated higher critical electric field values) that can result in much lower on-resistance than is possible in Si [11].

2.1 WIDE BAND GAP SEMICONDUCTOR

Some semiconductors are classified as "wide-bandgap" semiconductors because of their wider bandgap. Silicon has a bandgap of 1.12 eV and is not considered a wide-bandgap semiconductor. The bandgaps of WBG semiconductors are about three times or more that of Si as can be seen in Table 2.1. Generally, a wide band gap (WBG) semiconductor is a semiconductor with an energy band gap wider than about 2 eV. Fig 2.1 shows the energy band diagram of a semiconductor. Examples of WBG semiconductors are Aluminum Nitride (AlN, E_g = 6.2 eV), Gallium Nitride (GaN, E_g = 3.4 eV), and Silicon Carbide (SiC, E_g between 2.2 eV to 3.25 eV depending on polytype). Polytype mean 3C, 4H, 6H, 15R – Silicon Carbide [12].

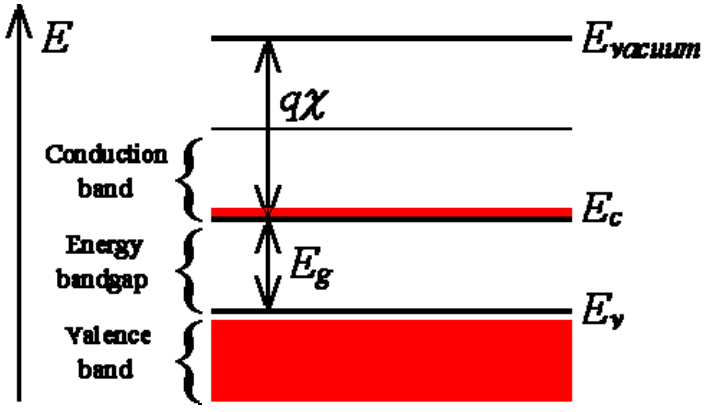

Fig.2.1 Energy band diagram where the energy band gap, E_g, valence band edge, E_v, and the conduction band edge, E_c The vacuum level, E_{vacuum}, and the electron affinity, χ [12]

2.1.1 ADVANTAGES OF WBG

It is already proven that even the first WBG semiconductor-based (SiC-based) power devices surpass Silicon's theoretical limits. WBG semiconductor power devices, with their superior characteristics, offer great performance improvements and can work in harsh environments where Si power devices cannot function. Some of the advantages compared with Si based power devices are as follows [13]:

- WBG semiconductor-based unipolar devices are thinner and have lower on-resistances. Lower R_{on} also means lower conduction losses; therefore, higher overall converter efficiency is attainable.

- WBG semiconductor-based power devices have higher breakdown voltages because of their higher electric breakdown field; thus, while Si Schottky diodes are commercially available typically at voltages lower than 300 V, the first commercial SiC Schottky diodes are already rated at 600 V.

- WBG devices have a higher thermal conductivity (4.9 W/cm-K for SiC and 22 W/cm-K for diamond, as opposed to 1.5 W/cm-K for Si). Therefore, WBG-based power devices have a lower junction-to case thermal resistance, Rth-jc . This means heat is more easily transferred out of the device, and thus the device temperature increase is slower. GaN is an exception in this case.

- WBG semiconductor-based power devices can operate at high temperatures. The literature notes operation of SiC devices up to 600°C. Si devices, on the other hand, can operate at a maximum junction temperature of only 150°C.

- Forward and reverse characteristics of WBG semiconductor-based power devices vary only slightly with temperature and time; therefore, they are more reliable.

- WBG semiconductor-based bipolar devices have excellent reverse recovery characteristics. With less reverse recovery current, switching losses and

electromagnetic interference (EMI) are reduced, and there is less or no need for snubbers. As a result, there is no need to use soft-switching techniques to reduce switching losses.

- Because of low switching losses, WBG semiconductor-based devices can operate at higher Frequencies (>20 kHz) not possible with Si-based devices in power levels of more than a few tens of kilowatts.

Since the electronic properties of a semiconductor are dominated by the highest partially empty band and the lowest partially filled band, it is often sufficient to only consider those bands. This leads to a simplified energy band diagram for semiconductors.

2.2 THEORY OF SILICON CARBIDE

Silicon carbide is older than our solar system, having wandered through the Milky Way for billions of years as generated in the atmospheres of Carbon rich red giant stars and by supernova remnants [14]. SiC never attracted a special fascination on man, as, for example, diamond did, due to the nearly total absence of its crystals in nature .Silicon Carbide is, however, better suited than diamond for electronic purposes. Silicon Carbide (SiC) was discovered in 1824 by the Swedish scientist Jons Jacob Berzelius [15], Silicon carbide (SiC) is a very promising material for use in high performance semiconductor devices. SiC is a wide band gap semiconductor with an energy gap wider than 2 eV and possesses extremely high power, high voltage switching characteristics and high thermal, chemical and mechanical stability. It is so thermally stable that dopant impurities cannot be diffused at any reasonable temperature; so chemically stable that it is impervious to any known chemical etchant; and so mechanically stable that it is used as a coating for drill bits and saw blades. **S**ilicon Carbide is rapidly maturing as a semiconductor material system since the commercial availability of single crystal substrates of 6H- and 4H-SiC poly types. Considerable progress has been reported in wafer size, epitaxy, and in discrete device and integrated circuit technologies for silicon carbide [16]. The wide bandgap of silicon carbide (3.0 eV for 6H-SiC and 3.25 eV for 4HSiC), its high avalanche breakdown field (2–3 MV/cm), and high

thermal conductivity (4.9 W/cm K) make it especially attractive for high-voltage, high-power, and high-temperature applications.

Silicon carbide is the only stable binary compound of silicon and carbon existing in a solid phase. It crystallizes in three bravais lattices

- Close packed cubic (zinc blende structure)
- Hexagonal (wurtzite structure)
- Rhombohedral

Single-crystal SiC forms in the hexagonal lattice, with alternating hexagonal planes of silicon and carbon atoms, as shown in Fig.2.2.

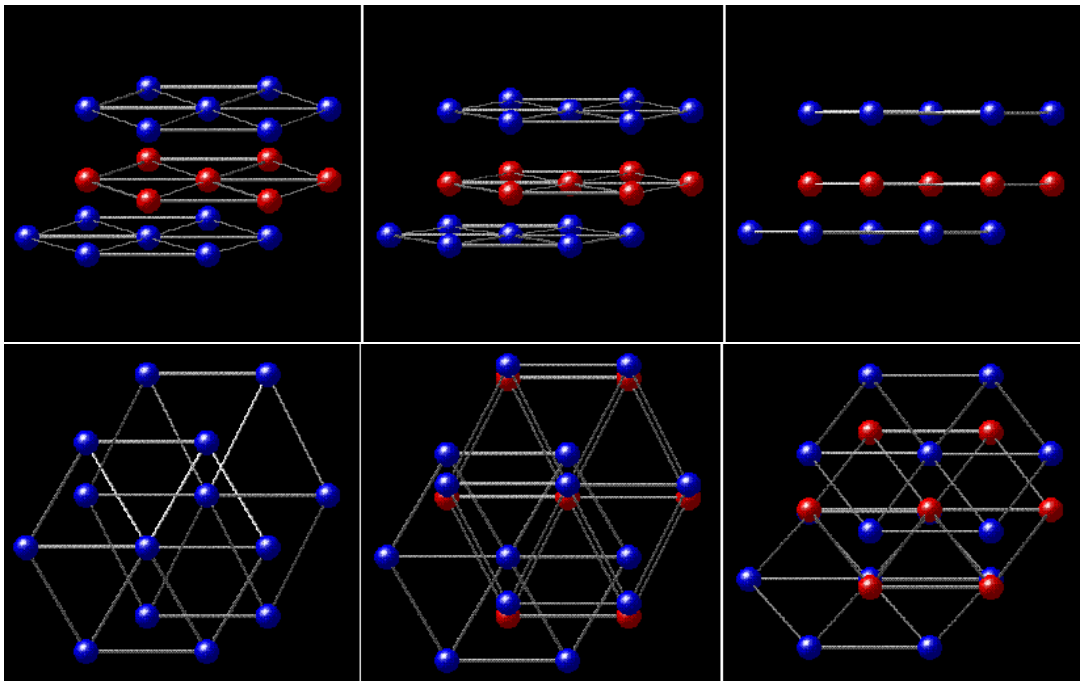

Fig. 2.2 Primitive crystal structure of SiC [12]

Each silicon atom bonds to four nearest-neighbor carbon atoms, and each carbon atom bonds to four nearest-neighbor silicon atoms (bonds are not shown). Note that the atoms in the second silicon plane are offset with respect to the atoms in the first silicon plane. As successive planes are added, each plane must be offset with respect to the plane below. This stacking sequence leads to different flavors, or polytypes, of the basic SiC crystal. There are a large number of possible polytypes, but the most important are 3C, 4H, and 6H. The

polytypes differ in band gap energy, carrier mobility, and breakdown field. For example, the E_g = 2.2, 3.25, and 3.0 eV for 3C, 4H, and 6H-SiC respectively [12].

Silicon atoms (blue) and carbon atoms (red) form alternating hexagonal planes. The sticks in this rendering are intended to emphasize the hexagonal lattice arrangement, and do not represent bonds. Each carbon atom bonds to three silicon atoms in the plane below and to one silicon atom in the plane above (bonds not shown). Note that the silicon atoms in the top plane are offset with respect to the silicon atoms in the bottom plane.

2.2.1 NEED OF SILICON CARBIDE

Silicon carbide is the only Wide Band Gap semiconductor that possesses a high-quality native oxide suitable for use as an MOS insulator in electronic devices. Thermal oxidation of Silicon Carbide produces a layer of SiO_2 (silicon dioxide) on the surface, while the carbon atoms from the Silicon Carbide form CO, which escapes as a gas. Therefore it is possible to make all the devices found in silicon IC technology in Silicon Carbide, including high quality, stable MOS transistors and MOS integrated circuits. The breakdown field in Silicon Carbide is about 8 times higher than in silicon. This is important for high-voltage power switching transistors. For example, a device of a given size in Silicon Carbide will have a blocking voltage 8 times higher than the same device in silicon. Important thing is that, the on-resistance of the SiC device will be about 100 times lower than the silicon device [12].

Thermal generation of electron-hole pairs is many orders of magnitude lower at any given temperature due to the wider band gap of silicon carbide than silicon, This makes it possible to build "dynamic" memories (DRAMs) in Silicon carbide that only need to be refreshed about once every 100 years at room temperature. This also makes it possible to operate Silicon carbide devices at temperatures as high as 650°C without degradation in electrical performance.

2.2.2 TRANSPORT PROPERTIES

In general the transport parameters give silicon carbide devices better performance than comparable silicon devices. Among the most important transport parameters for electronic

devices are the mobility (μ), saturation velocity (v_{sat}), breakdown electric field (*Ecrit*), and thermal conductivity (λ). The mobility describes the mean velocity that the electrons and holes travel with when an electric field is applied. At low electric fields the velocity increases proportional to the field. At higher fields the proportionality is lost and the velocity is saturated at *vsat*. When the electric fields exceed *Ecrit,* the impact ionization becomes large, rapidly increasing the current, which destroys the material if the current is not limited [17]. The thermal conductivity does not directly affect the performance, but with a good thermal conductivity it is easier to conduct the heat away from the chip to a heat sink. As the mobility and saturation velocity are reduced at high temperatures, a high thermal conductivity indirectly gives better performance for power devices. The advantages of SiC over Si are the twofold increase in saturation velocity, tenfold increase in breakdown fields, and the more than doubling of thermal conductivity. The carrier mobility in silicon carbide is somewhat lower than in silicon, but in general the transport parameters give silicon carbide devices better performance than comparable silicon devices.

2.2.2.1 MOBILITY

The mobility defines that how easily the electrons and holes can be moved in an electric field. Due to random scattering within the crystal, the velocity does not increase with constant acceleration as in a vacuum. The electron velocity rather quickly reaches an equilibrium mean-velocity proportional to the mobility and the electric field. The mobility in SiC is somewhat lower than for silicon and much lower than in high mobility materials, such as GaAs. The low mobility in SiC devices is compensated by operation at larger electric fields taking advantage of the higher carrier velocity. To some extent the mobility can be described using the same models as those used for silicon. The parameters for the mobility models are collected from measurements for a temperature dependent mobility model [18].

2.2.2.2 SATURATION VELOCITY

At high electric fields the velocity ceases to be proportional to the electric field, due to increased scattering. The velocity saturates at *vsat*, which for SiC is approximately twice the value for silicon. A high saturation velocity allows faster devices with shorter switching times.

2.2.2.3 BAND GAP

The band gap is a forbidden zone in the energy spectra for a crystal. Without a band-gap the crystal is a metal, and with a large band-gap the crystal is an insulator. A semiconductor has a band-gap up to a few eV. For some traditional semiconductors the band gaps are: 1.11 eV for Si, 0.7 eV for Ge, and 1.4 eV for GaAs. Many of the favorable transport parameters in SiC are related to the large band-gap, which is of the order of 3 eV. For such a large band gap the intrinsic carrier concentration is negligible at temperatures up to 600 degrees Celsius. The intrinsic carrier concentration is responsible for the thermal noise, and also partly responsible for the leakage current, which are both very small in large band-gap materials. The minimum energy required to create an electron-hole pair is equal to the band-gap that in SiC falls within the 3 eV range corresponding to a photon with wavelength close to 400 nm. SiC devices are thus also insensitive to the main part of the visible spectrum, making SiC suitable as a detector material for UV radiation with minimal noise from the visible background

2.2.2.4 CRITICAL ELECTRIC FIELD

For high electric fields the carrier energy is increasing, and, as the energy exceeds the band-gap, the probability of an impact ionization event increases. In an impact-ionization event the carrier knocks out one electron from the valence-band, creating an electron-hole pair (EHP). As the energy must be conserved, the energy for the incident carrier is reduced by the band-gap energy plus the initial energy for the created electron and hole. The critical electric field is related to the impact ionization rate, which increases as the carrier energy exceeds the band-gap. Due to the large bandgap the critical electric field is thus about 10 times higher in SiC than for small band-gap materials, such as Si and GaAs. With high *Ecrit* devices can be much smaller for the same voltage, alternatively operate at much higher voltages.

2.2.3 THERMAL CONDUCTIVITY

The thermal conductivity for SiC is close to that for copper, a quality that is very important in power semiconductor devices in order to transport the heat from the power

dissipated in the device. For high power devices the thermal effects constitute one of the main limiting factor of the performance. One of SiC´s competitors is gallium nitride (GaN), which is a material with similar properties to those of SiC but which are less mature.

2.2.4 SURFACE MOBILITY

The surface mobility describes the transport in the inversion layer of a MOSFET device and is critical for device performance. Pioneering experiments have given very poor values for the surface mobility in SiC devices in the range of 10 cm^2/Vs [17]. The low mobility is related to the high defect density in the oxide-semiconductor interface.

2.2.5 COMPARISION OF ELECTRONIC PROPERTIES OF Si, SiC & GaAs

Silicon Carbide (SiC) has superior properties for power devices as compared to silicon. Silicon carbide (SiC) device development is increasing due to the need for electronic devices capable of operation at high power levels and high temperature. The main strength of silicon carbide is that it can resist high field strengths, it offers better heat-conducting capacity than copper at room temperature and it has a large energy band gap, which means that electrical components continue functioning even when the mercury starts climbing. With very high thermal conductivity (~5.0 W/cm), high saturated electron drift velocity (~2.7 x 10^7 cm/s) and high breakdown electric field strength (~3 MV/cm), SiC is a material of choice for high temperature, high voltage, high frequency and high power applications. Table 2.1 lists electrical properties of the common SiC polytypes in comparison to that of Si and GaAs [19].

The most important SiC property of all is the large bandgap, which is nearly three times larger than that of silicon. The large S-C bonding energy makes SiC resistant to chemical attack and radiation. Silicon carbide belongs to a class of semiconductors commonly known as wide band gap semiconductors, where conventional semiconductors like Si and GaAs cannot adequately perform under extreme conditions. The wider band gap of SiC also enables one to design smaller, higher density devices that will withstand high voltages. The high thermal conductivity of SiC decreases the need for special packaging and system cooling for device operation [19].

Properties	Si	GaAs	6H-SiC	4H-SiC	3C-SiC
Energy Bandgap (eV)	1.1	1.42	3.0	3.2	2.3
Breakdown Field @10^{17} (MV/cm)	0.6	0.6	3.2	3.0	>1.5
Electron Mobility @ 10^{16} (cm^2/V-s)	1100	6000	370	800	750
Saturated Electron Drift Velocity (cm/s)	10^7	10^7	2 x 10^7	2 x 10^7	2.5 x 10^7
Thermal Conductivity (W/cm-K)	1.5	0.5	4.9	4.9	5.0
Hole Mobility @ 10^{16} (cm^2/V-s)	420	320	90	115	40

Table 2.1 Comparison of properties of SiC with Si and GaAs at room temperature [19]

2.2.6 SILICON CARBIDE POLYTYPES

Silicon carbide exists in hundreds of different polytypes, the most common being 3C-, 4H- and 6H-SiC. Furthermore, islands of 15R can be found on 4H and 6H wafers, and small crystals of 2H-SiC have been grown. The digit in the name is the number of double layers (one Si and one C layer) in the primitive lattice cell; and the character gives the type of crystal symmetry. H stands for hexagonal, C for cubic and R for rhombohedral.

Depending on the stacking sequence (steps to the right and to the left), a lone cubic polytype denoted 3C- or β-SiC, a great number of hexagonal polytypes denoted 2H-, 4H-, 6H-SiC etc., and a great number of rhombohedral polytypes denoted 15R-, 21R-, 27R-SiC etc. are obtained (see Fig. 2.3). Altogether more than 200 different SiC polytypes are identified by Laue patterns. The hexagonal and rhombohedral polytypes are collectively referred to as α-SiC. Depending on the particular polytype, a different number of non-equivalent lattice sites exists either with cubic (see hatched areas in Fig. 2.3) or with hexagonal (see cross-hatched areas in Fig.2.1) environment (3C: one cubic site (k), 4H: one cubic site (k) and one hexa-gonal site (h), 6H: two cubic sites (k1, k2) and one hexagonal site (h).

The stacking sequence is shown in Fig 2.3 for the three most common polytypes 3C, 4H and 6H-Silicon carbide. Silicon carbide cubic, hexagonal and rohombohedral crystal

structures are shown in Fig.2.3. If we designate a Si-C atom pair in an A-plane in a close packed lattice as A, and in the B-plane as B, and in the C-plane as C, then we can generate a series of lattice unit cells by variation of SiC plane stacking sequence along the principal crystal axis [19].

The ABCABC... stacking, will generate the 3C-SiC zinc-blende or cubic lattice, and ABAB... stacking, will generate the 2H-SiC wurtzite lattice. Other stacking sequences, such as ABACABAC….. will generate 4H-SiC; and ABCACB..... Will generate 6H-SiC. The number of atoms per unit cell varies from polytype to polytype, significantly affecting the number of electronic energy bands and vibrational branches possible for a given polytype. This diversity in electronic and vibrational band structures profoundly affects the physical properties of the different polytypes.

2.2.6.1 6H-SiC

6H-SiC has a large anisotropy due to the long repetition length in the crystallographic lattice. Compared with Si the mobility in 6H-SiC is about 25% in the direction perpendicular to the c-axis, and 7% in the direction parallel to it. The saturation velocity for 6H-SiC is $2*10^7$cm/s in the direction perpendicular to the c-axis, but only $0.6*10^7$ cm/s in the direction parallel to it.

2.2.6.2 4H-SiC

The low-field mobility for 4H-SiC is about half that of silicon with a small anisotropy. The anisotropy in 4H-SiC depends on the electric field, and at high electric fields the saturation velocity is 20% lower in the c-axis direction. 4H-SiC and 6H-SiC are the most mature polytypes and they are the ones which have been characterized most thoroughly.

2.2.6.3 3C-SiC

3C-SiC has an advantage as it is able to be grown on silicon substrates, however at the moment with reduced quality. This allows for the possibility in the future of integration of 3C-SiC devices with silicon technology on the same chip. Another advantage is that 3C-SiC does not suffer from stacking faults growth, as these tend to grow towards 3C-SiC. 3C-

SiC has larger electron mobility than for 4H-SiC but has reduced hole mobility. The main disadvantages when compared to other polytypes are the lower band-gap and breakdown field and the advantage of replacing existing silicon devices is strongly reduced.

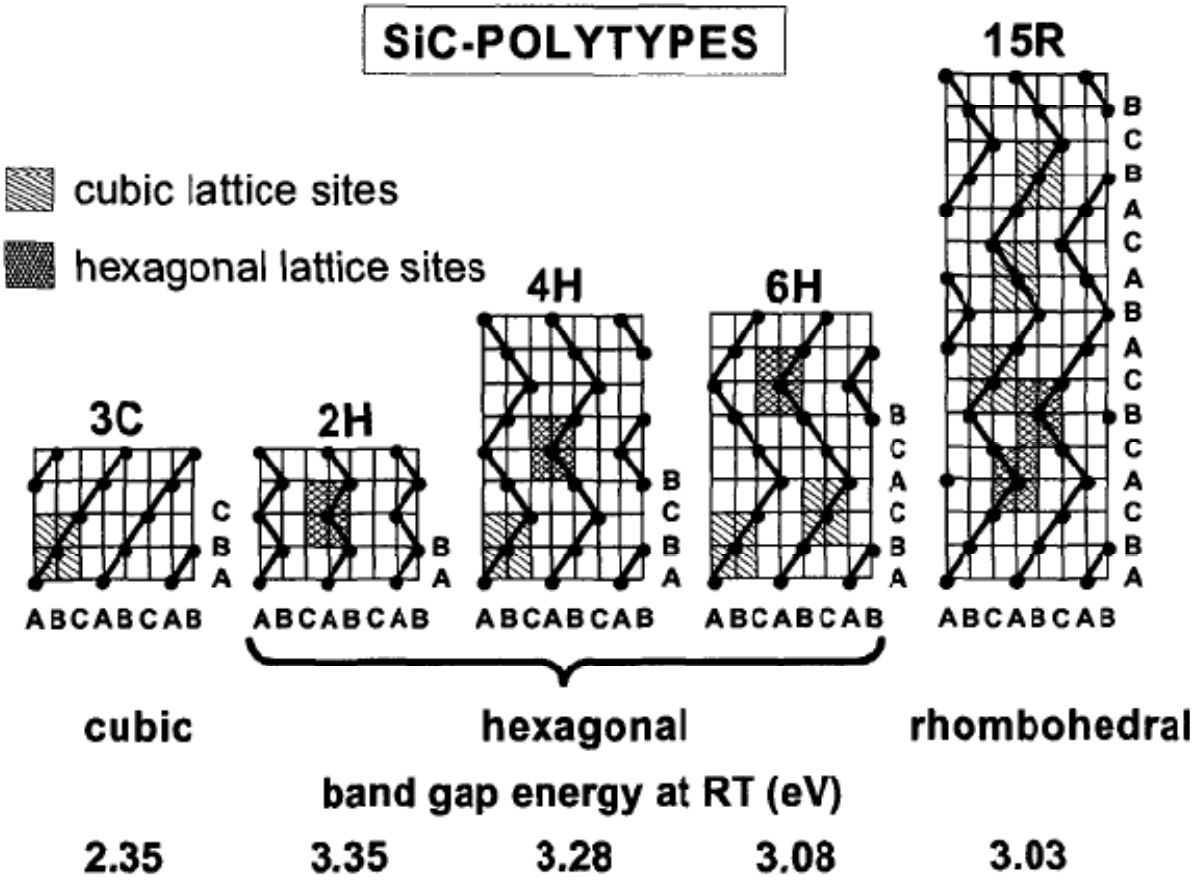

Fig. 2.3 SiC polytypes; the non-equivalent lattice sites are schematically indicated by the hatched (k) and cross-hatched (h) areas [20].

2.2.6.4 15R-SiC

15R-SiC is very complex, namely 15 atomic layers ordered in a rhombohedral structure. A few years ago, much attention was focused on 15R-SiC, owing to improved experimental MOSFET performance when compared to the other polytypes. These devices have been manufactured on 4H- or 6H-SiC, where pieces of 15R-SiC were found. Mono-crystalline 15RSiC wafers are however not a reality in the near future.

2.2.6.5 2H-SiC

2H-SiC is not a commercially available substrate, but small mono-crystalline pieces have been grown. Monte Carlo simulations predict that the performance perpendicular to the c-axis direction is similar to 4H-SiC, but the mobility is better in the parallel to the c axis direction (similar to silicon) [17].

2.3 APPLICATIONS AND BENEFITS OF SiC ELECTRONICS

Two most beneficial advantages that SiC-based electronics offer are in the areas of high temperature device operation and high-power device operation. The specific SiC device physics that enables high temperature and high power capabilities will be examined first, followed by several examples of revolutionary system-level performance improvements these enhanced capabilities enable.

2.3.1 HIGH TEMPERATURE DEVICE OPERATION

There are a number of factors both inside and outside the semiconductor that limit the high-temperature operation of semiconductor electronic devices and circuits. Proper understanding of these factors is crucial in determining which high-temperature applications can be met with mature technologies like silicon and silicon-on-insulator (SOI) versus which applications will be met with wide bandgap semiconductors. This section will briefly examine the main device physics limits of operating semiconductor devices at high temperature, with a particular emphasis placed on the most fundamental limits of silicon that wide bandgap semiconductors could be used to overcome [21].

The wide band gap energy and low intrinsic carrier concentration of SiC allows maintaining semiconductor behavior at much higher temperatures than silicon, which in turn permits SiC semiconductor device functionality at much higher temperatures than silicon. The temperature dependence of intrinsic carrier concentration for silicon, 6H-SiC, and 2H-GaN is given in Fig 2.4. Semiconductor electronic devices function in the temperature range where intrinsic carriers are negligible so that conductivity is controlled by intentionally introduced dopant impurities.

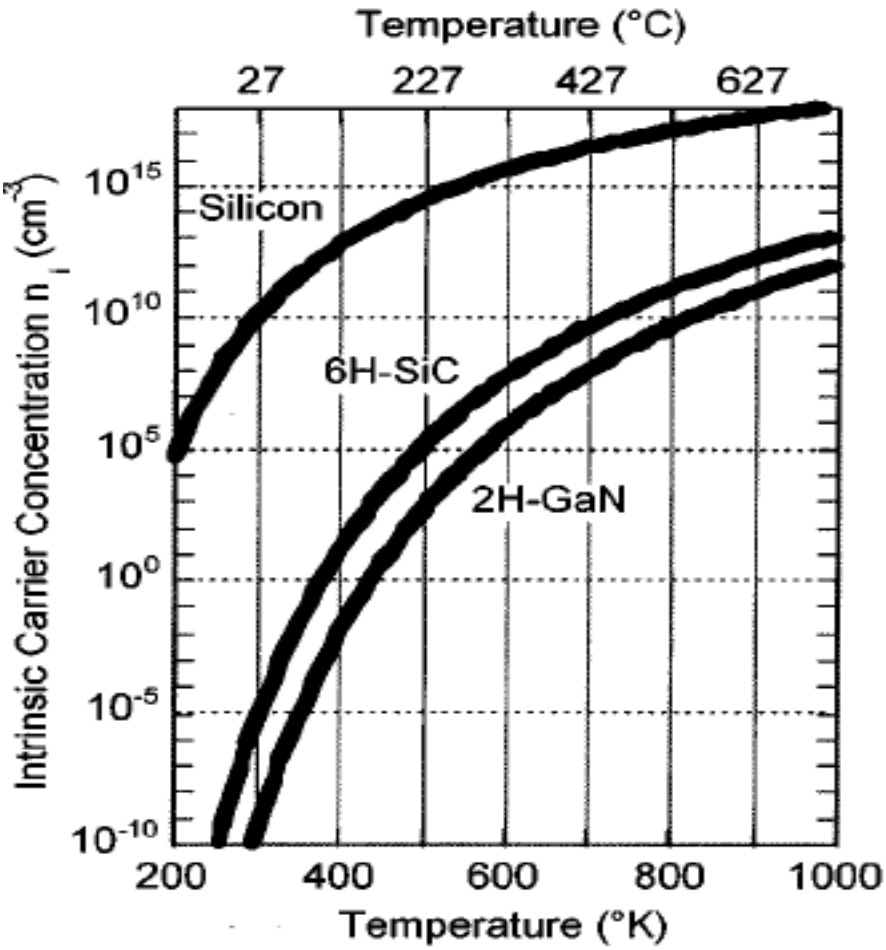

Fig.2.4 Semiconductor intrinsic carrier concentration (n_i) versus temperature for silicon, 6H-SiC, and 2H-GaN [21].

Furthermore, the intrinsic carrier concentration n_i is a fundamental prefactor to well-known equations governing undesired junction reverse bias leakage currents. As temperature increases, intrinsic carriers increase exponentially so that undesired leakage currents grow unacceptably large, and eventually at still higher temperatures, the semiconductor device operation is overcome by uncontrolled conductivity as intrinsic carriers exceed intentional device doping [22,23]. Depending upon specific device design, the intrinsic carrier concentration of silicon generally confines silicon device operation to junction temperatures less than 300^{0}C. SiC's much smaller intrinsic carrier concentration theoretically permits device operation at junction temperatures exceeding 800^{0}C, and 600^{0}C SiC device operation has been experimentally demonstrated on a variety of SiC devices [24].

2.3.2 HIGH POWER DEVICE OPERATION

The high breakdown field and high thermal conductivity of SiC coupled with high operational junction temperatures theoretically permit extremely high power densities and efficiencies to be realized in SiC devices. Figures 2.5 and 2.6 demonstrate the theoretical advantage of SiC's high breakdown field compared to silicon in shrinking the drift-region and associated parasitic on-state resistance of a 3000 V rated unipolar power MOSFET device [23]. The high breakdown field of SiC relative to silicon enables the blocking voltage region to be roughly 10X thinner and 10X heavier-doped, permitting a roughly 100-fold decrease in the dominant blocking region (N-Drift Region) resistance R_D of Figure 2.5 for the SiC device relative to an identically rated 3000 V silicon power MOSFET.

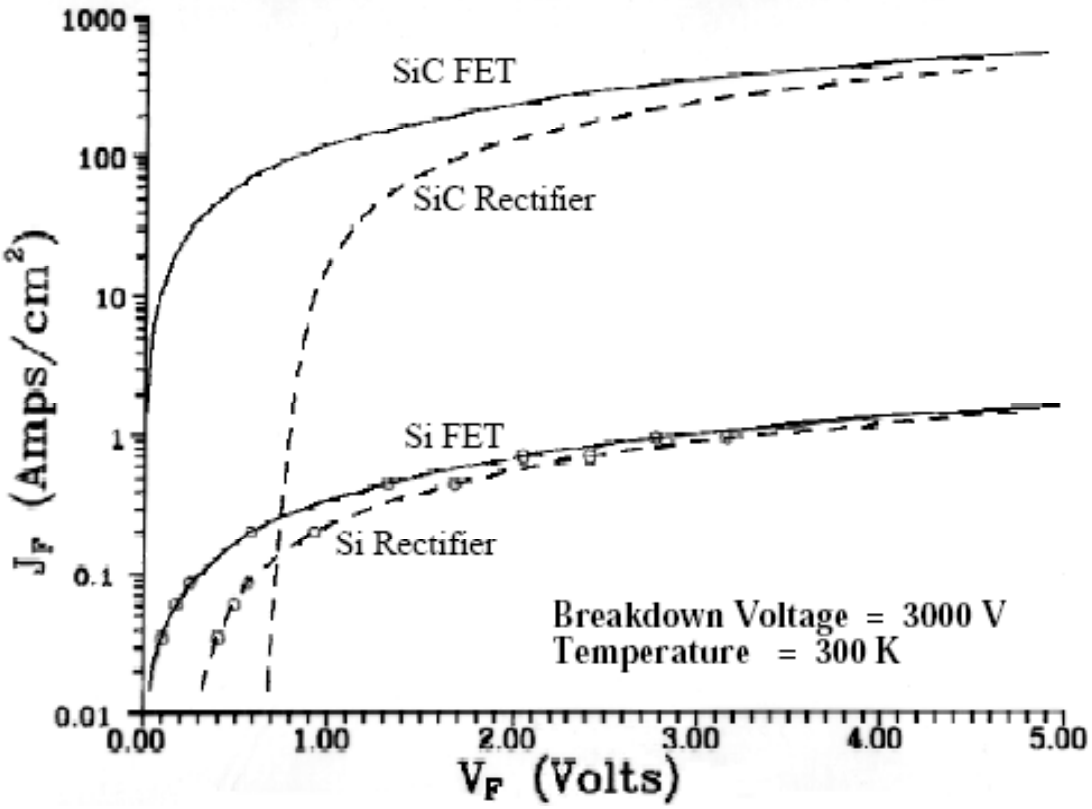

Fig: 2.5 Forward conduction characteristics of ideal Si and 6H-SiC power MOSFET's and Schottky rectifiers at room temperature with a breakdown voltage of 3000 V [23]

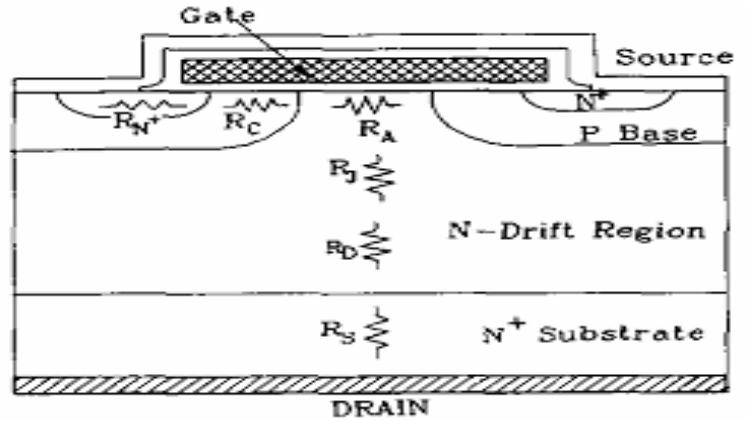

Fig: 2.6 Cross section of a power DMOSFET showing various internal resistances Associated with it [Ref.23].

Significant energy losses in many silicon high-power system circuits, particularly hard switching motor drive and power conversion circuits, arises from semiconductor switching energy loss. Switching energy loss is often a function of the turn-off time of the semiconductor switching device, generally defined as the time lapse between when a turn-off bias is applied to the time that the device actually cuts off most current flow. The faster a device turns off, the smaller its energy loss in a switched power conversion circuit. For device-topology reasons, SiC's high breakdown field and wide energy bandgap enable much faster power switching than is possible in comparably volt-amp rated silicon power-switching devices. Therefore, SiC-based power converters could operate at higher switching frequencies with much greater efficiency (i.e. less switching energy loss). Higher switching frequency in power converters is highly desirable because it permits use of proportionally smaller capacitors, inductors, and transformers, which in turn can greatly reduce overall system size and weight.

While SiC's smaller on-resistance and faster switching helps minimize energy loss and heat generation, SiC's higher thermal conductivity enables more efficient removal of waste heat energy from the active device. Because heat energy radiation efficiency increases greatly with increasing temperature difference between the device and the cooling ambient, SiC's ability to operate at high junction temperatures permits much more efficient cooling to take place, so that heat sinks and other device-cooling hardware (i.e., fan cooling, liquid

cooling, air conditioning, etc.) typically needed to keep high-power devices from overheating can be made much smaller or even eliminated.

2.4 POWER MOSFETS

The breakdown electric field of SiC is approximately 8 times higher than silicon. This makes it possible to design power switching devices having correspondingly higher blocking voltages than their silicon counterparts. More importantly, the specific on resistance (i.e. resistance-area product) of a power device scales inversely as the cube of the breakdown field, so the on-resistance of SiC power MOSFETs are 100-200 times lower than comparable devices in silicon [12].

2.5 BREAKDOWN VOLTAGE

The most unique feature of power semiconductor devices is their ability to withstand high voltages. In transistors designed for microprocessors and semiconductor memories, the pressure to reduce their size to integrate more devices on a monolithic chip has resulted in a reduction in their operating voltage. The desire to control larger power levels in motor drive and power distribution systems has encouraged the development of power devices with larger breakdown voltages. Depending upon the application, the breakdown voltage of devices can range from 20 to 30 V for voltage regulator modules (power supplies) used to deliver power to microprocessors in personal computers and servers to over 5,000 V for devices used in power transmission networks.

In a semiconductor, the ability to support high voltages without the onset of significant current flow is limited by the avalanche breakdown phenomenon, which is dependent on the electric field distribution within the structure. High electric fields can be created within the interior of power devices as well as at their edges. The design optimization of power devices must be performed to meet the breakdown voltage requirements for the application while minimizing the on-state voltage drop, so that the power dissipation is reduced.

2.5.1 AVALANCHE BREAKDOWN

The maximum voltage that can be supported by a power device before the onset of significant current flow is limited by the avalanche breakdown phenomenon. In power devices, the voltage is supported across depletion regions. Mobile carriers are accelerated in the presence of a high electric field until they gain sufficient energy to create hole–electron pairs upon collision with the lattice atoms. This impact ionization process determines the current flowing through the depletion region in the presence of a large electric field. An impact ionization coefficient was defined as the number of electron–hole pairs created by a mobile carrier traversing 1 cm through the depletion region along the direction of the electric field. The impact ionization coefficients for electrons and holes are a strong function of the magnitude of the electric field.

2.5.2 PUNCH-THROUGH BREAKDOWN

It occurs in devices with relatively short channels when the drain voltage is increased to the point that the depletion region surrounding the drain region extends through the channel to the source. The drain current then increases rapidly. Normally, punch-through does not result in permanent damage to the device. Punch-through occurs when the depletion region on the Source side of the body-drift p-n junctions reaches the source region at drain voltages below the rated avalanche voltage of the device. Trade-offs for this phenomenon involves the following: 1) on-resistance requiring shorter channel lengths and 2) punch-through avoidance requiring longer channel lengths.

CHAPTER 3

AN INTRODUCTION TO SILICON CARBIDE DEVICES

SiC electronic devices can be broadly classified into two categories: Semi-conducting- and semi-insulating-based devices. The semi-conducting SiC power devices can also be categorized into power rectifiers and power switches, while semi-insulating-based devices comprise high power high frequency application devices.

It should be noted that many types of SiC power devices are still in the prototype demonstration phase while others have demonstrated performance measures far superior to silicon. These include the PiN (positive-intrinsic-negative) diodes, the Schottky barrier diode (SBD), the merged PiN Schottky diode (MPS) operate with blocking voltages above 12 kV , the metal-oxide semiconductor field-effect transistor (MOSFET) , the junction field-effect transistor (JFET), the bipolar junction transistor (BJT) with performance figures 100 times higher than in silicon, the gate turn-off thyristor (GTO) blocking over 3 kV and switching over 60 kW , the metal-semiconductor field-effect transistor (MESFET) and the static induction transistor (SIT) which show ultrahigh frequency, power density and an associated power added efficiency (PAE) of 78%[25] .Silicon carbide has several unique properties (higher breakdown field, wider band gap, lower thermal generation rate and lower intrinsic carrier concentration) to enhance performance in devices. Some of devices will be described in detail In following sections.

3.1 SCHOTTKY BARRIER DIODES

Schottky barrier diodes (SBDs) have many benefits compared to other rectifying devices, such as fast switching speeds and relatively easy fabrication. Couple this with the large amount of data that can be extracted through measurements and SBDs provide a great research platform. The formation of an ideal Schottky contact depends on the work functions of the two materials being brought into intimate contact with each other. When a metal and a semiconductor are brought together two outcomes are possible: either a Schottky contact or

an ohmic contact can form. Both types of contacts are extremely important to solid state research.

However, due to the difficulty in the formation of well-controlled metal/SiC interface, the Reverse leakage current of Schottky barrier diodes can be significantly increased prior to junction breakdown [26]. An increase in reverse leakage current of SBDs leads to higher power loss and premature breakdown. It is therefore important to reduce reverse leakage current of Schottky barrier diodes.

Schottky barrier diodes (SBD) are unipolar devices, i.e. they do not inject minority carriers into a neutral region as do PN diodes. Since there is no minority charge storage, the turn of event is fast and the transient reverse current is small. As a result, the switching energy dissipated during turn-off is minimal. Hence, Schottky diodes eliminate the switching losses. SiC Schottky barrier diodes are attractive because the breakdown field of SiC is 8 to 10 times higher than for silicon. Hence, these are capable of operation at much higher temperatures than silicon devices.

Schottky barrier diodes (SBD's) are used as high voltage rectifiers in many power switching applications. Whenever current is switched to an inductive load such as an electric motor, high-voltage transients are induced on the lines. To suppress these transients, diodes are placed across each switching transistor to clamp the voltage excursions.PN junction diodes could be used for this application, but they store minority carriers when forward biased, and extraction of these carriers allows a large transient reverse current during switching. Schottky Barrier Diodes are rectifying metal-semiconductor junctions, and their forward current consists of majority carriers injected from the semiconductor into the metal. Consequently, SBD's do not store minority carriers when forward biased, and the reverse current transient is negligible. This means the SBD can be turned off faster than a PN diode, and dissipates negligible power during switching.

SiC Schottky Barrier Diodes are especially attractive because the breakdown field of SiC is about 8x higher than in silicon. In addition, because of the wideband gap, SiC SBD's should be capable of much higher temperature operation than silicon devices. They have

fabricated SBD's on 4H SiC using both Ni and Ti as Schottky metals. The cross-sections of the experimental device is shown in Fig.3.1

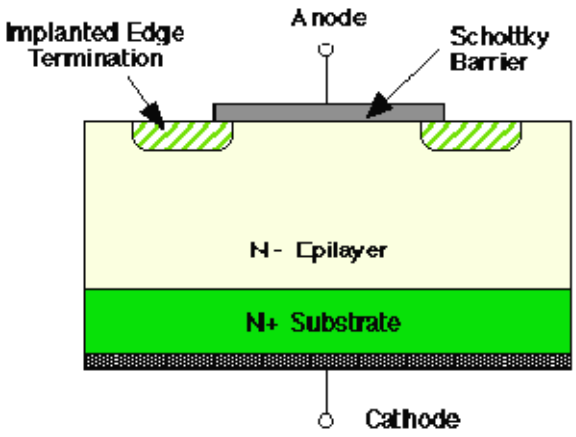

Fig. 3.1 Cross-section of an implant-edge-terminated Schottky barrier diode in SiC [12]

Forward and reverse I-V characteristics for the Ti and Ni SBD's are shown in Fig. 3.2. The barrier heights for Ti and Ni on 4H-SiC at room temperature are 0.8 and 1.3 V, respectively. The lower barrier height Ti gives lower forward voltage drop but higher reverse leakage current as compared to the Ni barrier. The reverse blocking voltages are 1480 and 1720 V, respectively. The blocking voltage of the Ni SBD is the highest yet reported for any SBD on SiC.

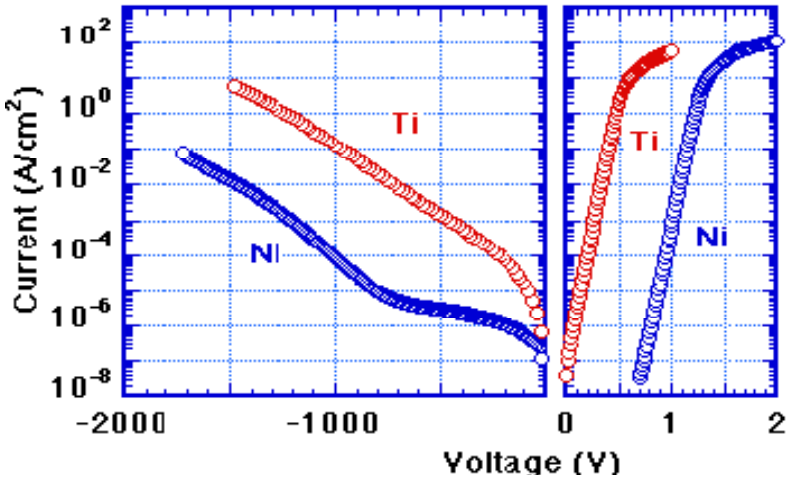

Fig 3.2 Forward and reverse current-voltage characteristics for Ti and Ni Schottky barrier diodes on 4H-SiC at room temperature [12].

Ni Schottky diodes recently fabricated on a 50 μm epilayer of 4H-SiC [27]. These diodes exhibited blocking voltages as high as 4.9 kV, the highest yet reported for a SiC Schottky diode. Figure 3.3 shows forward and reverse current-voltage characteristics of a 425 μm diameter diode at room temperature SiC Schottky diodes for in-circuit testing are also fabricated on large-area. These diodes were packaged at Cree Research and shipped to Harris Semiconductor, Mountaintop, PA, where they replaced silicon PiN diodes in an IGBT-driven inductive switching circuit. Tests by Harris indicated that the switching energy of the IGBT circuit is reduced by a factor of four compared to the case with silicon PiN diodes [28].

3.2 SIC IMPATT DIODE

SiC is used for the fabrication of high-power microwave devices due to its most important properties that is high breakdown field. Due to its high breakdown field the SiC can be considered as the ideal material for the fabrication of high-power microwave devices. One device, in particular, that benefits from the high breakdown field of SiC is the Impact-ionization Avalanche Transit-Time (IMPATT) diode oscillator. IMPATT diodes deliver the highest RF power of any semiconductor microwave oscillator, and are used to produce carrier signals for microwave transmission systems, particularly airborne and ground-based radar.¦Depending upon the design, IMPATT diodes can operate from a few GHz to a few hundred GHz. The power-frequency product (p f2) of an IMPATT diode scales as the square of the critical field for avalanche breakdown times the electron saturation drift velocity. In SiC, the critical field is about 10x higher than in silicon or GaAs, and the saturation drift velocity is about 2x higher. Thus, the power-frequency product (in the electronic limit) is theoretically expected to be about 400x higher for SiC IMPATT diodes than for diodes in silicon or GaAs. A typical cross section of a Read-type (Hi-Lo) IMPATT diode is shown in Fig. 3.3[29].

The diode is operated in reverse bias near breakdown, and both the N and N-regions are completely depleted. The internal electric field is shown at the bottom of the figure. Because of the difference in doping between the "drift region" and "avalanche region", the electric field is highly peaked in the avalanche region and nearly flat in the drift region. In operation, avalanche breakdown occurs at the point of highest electric field, and this

generates a large number of hole-electron pairs by impact ionization. The holes are swept into the cathode, but the electrons travel across the drift region toward the anode. As they drift, they induce image charges on the anode, giving rise to a displacement current in the external circuit that is 180° out of phase with the nearly sinusoidal voltage waveform.

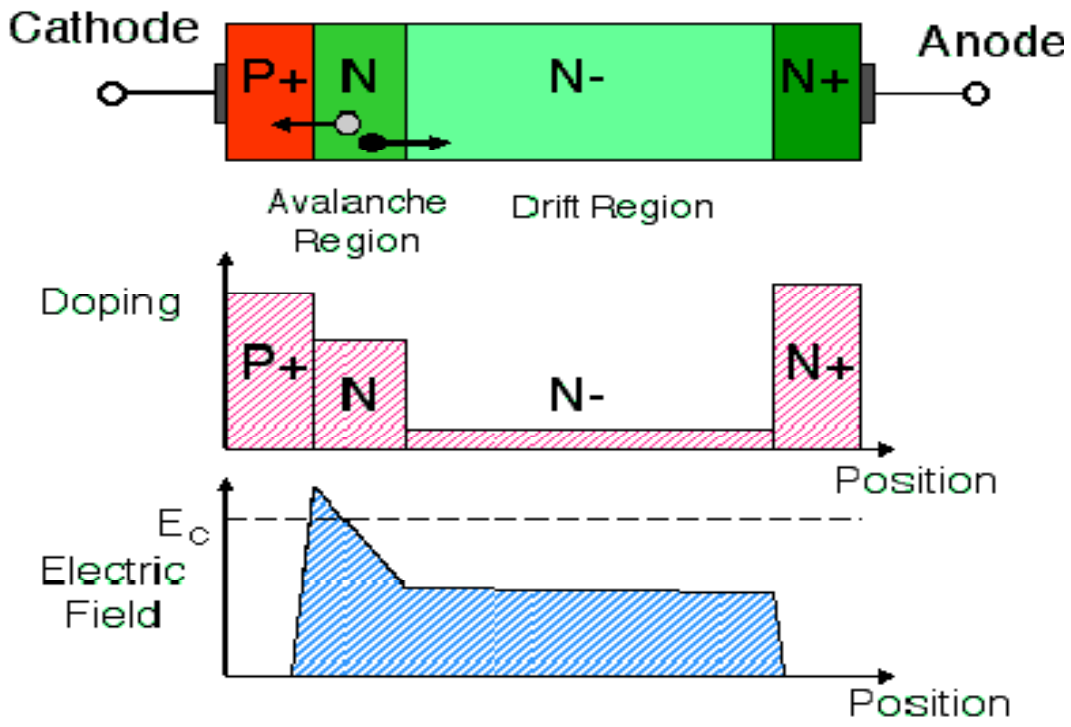

Fig 3.3 Cross section of a SiC IMPATT diode. Hole-electron pairs are created at the point of highest electric field (the "Avalanche Region"). Holes are swept into the cathode, but electrons drift toward the anode, inducing a displacement current in the external circuit as they drift [29].

Figure 3.4 shows the buildup of microwave oscillations in the diode current and voltage when the diode is embedded in a resonant cavity and biased at breakdown. Figure 3.4 shows a close-up of the current and voltage waveforms after oscillations have stabilized. It is clear from Fig. 3.4 that the current is 180° out of phase with the voltage. This represents a negative ac resistance, and corresponds to the net generation of microwave power by the diode

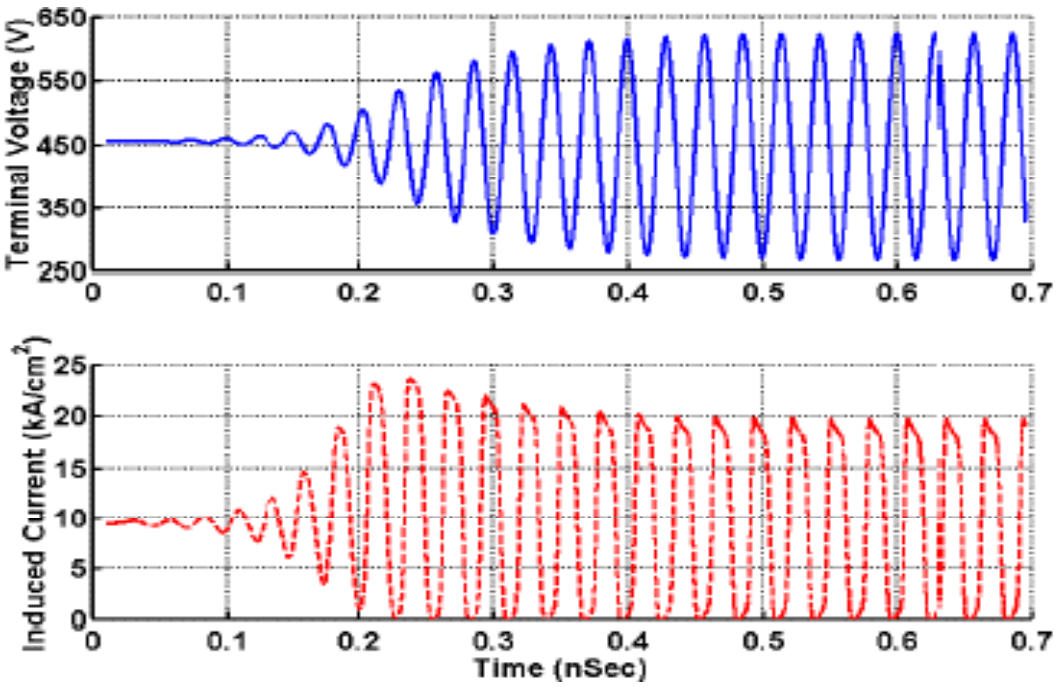

Fig. 3.4 Buildup and stabilization of microwave oscillations, as predicted by a two dimensional transient device simulator [29].

3.3 CHARGE COUPLED DEVICES

In the charge-coupled structure, the voltage blocking capability is enhanced by the extension of depletion layers in two-dimensions. This effect is created by the formation of a horizontal Schottky contact on the top surface as illustrated in Fig. 3.5, which promotes the extension of a depletion region along the vertical or *y*-direction. Concurrently, the presence of the vertical P–N junction created by the alternate N- and P-type regions promotes the extension of a depletion region along the horizontal or *x*-direction. These depletion regions conspire to produce a two dimensional charge coupling in the N-drift region, which alters the electric field profile. The optimization of the charge-coupled structure requires proper choice of the doping concentration and thickness of the N- and P-type regions. It has been found that the highest BV occurs when the charge in these regions is given by equation 3.1

$$Q_{optimum} = 2qN_dW_N = \varepsilon_s Ec \qquad (3.1)$$

Where q = Charge of an electron (1.6 × 10−19 C).

N_d = Doping concentration of the N-type drift region.

W_N = Half the width of the N-type drift region as shown in Fig. 3.5

ε_s = Dielectric constant of the semiconductor.

And E_C = Critical electric field for breakdown in the semiconductor.

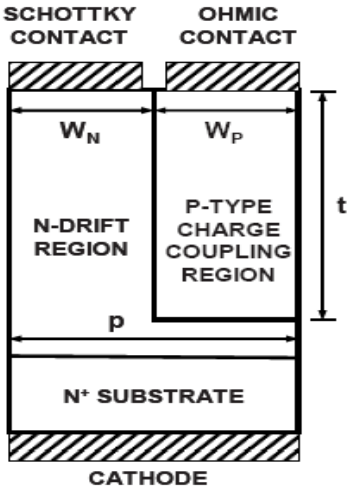

Fig. 3.5 Basic charge coupled Schottky diode structure using P-N junctions [2]

In designing the drift region for charge-coupled structures, it is important to recognize that, unlike in the conventional one-dimensional case, the doping concentration of the drift region is dictated by the cell pitch and not the BV. The BV in the charge-coupled structure is determined solely by the depth of the trench used to provide the charge coupling effect and is independent of the doping concentration of the N-drift region.

Silicon CCDs are widely used as image sensors, particularly in digital still cameras and hand-held video cameras. SiC is of interest as a specialized image sensor because its wide bandgap makes it transparent to visible light, resulting in an ultraviolet (UV) sensor which is virtually blind to solar radiation. Such a sensor has applications in aerospace research, UV astronomy and in military systems. In this structure, the source and drain junctions and the buried n-type channel are formed by nitrogen ion implantation and the implants are activated by high temperature annealing. The gate oxide is thermally grown using the optimized conditions identified in MOS investigations. Then deposit a layer of polysilicon for the first-level gates and dope the poly with phosphorus. The polysilicon is

patterned by reactive ion etching and oxidized to form a passivation layer. A second layer of polysilicon is then deposited and doped to form the second-level gates.

3.4 CMOS DIGITAL INTEGRATED CIRCUITS

Development of CMOS technology in SiC is expected to provide low power, high temperature circuits as well as reliable control circuitry for smart power integrated circuits. CMOS technology is attractive for digital logic because it offers low power consumption, full rail-to-rail output swing, and greater noise margins than NMOS circuits. CMOS also provides active current sources for linear applications. CMOS Process utilized an implanted n-well and deposited oxides, but due to other processing problems the PMOSFETs exhibited a very high threshold voltage. Implanted p-well and thermally grown oxide is used to fabricate this device. A typical Cross section of a CMOS inverter in the implanted p-well process is shown in fig3.6

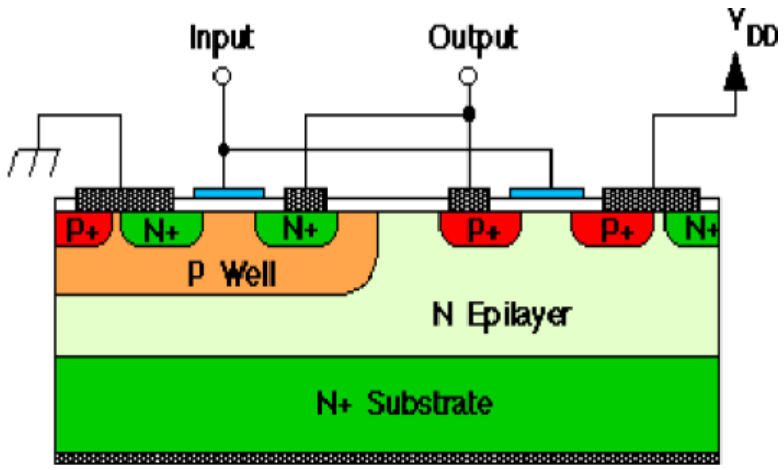

Fig. 3.6 Cross section of a CMOS inverter in the implanted p-well process. The p-well , P+ source regions, and N+ source regions are all formed by ion implantation. Both transistors have a polysilicon gate over a thermally grown oxide [12].

3.5 NONVOLATILE MEMORIES

The thermal generation rate in semiconductors is proportional to the intrinsic carrier concentration n_i, and n_i decreases exponentially with band gap energy. Wide band gap semiconductors have dramatically lower thermal generation, with the thermal generation rate of 6H-SiC being about 16 order-of-magnitude lower than silicon. This makes it possible to construct on-transistor memory cells in SiC which retain information for many years without power. 6H silicon carbide is a single-crystal semi conducting material with a band gap of 3.0 eV. Since thermal generation scales directly with the intrinsic carrier concentration, leakage currents in SiC are negligible[30].

3.6 SILICON CARBIDE POWER MOSFETS

Power switches can be considered as the heart of all power electronic systems [31]. The major types of power switching devices for low and medium power applications are BJTs, MESFETs, JFETs and MOSFETs. The BJT is attractive for high power applications because conductivity modulation in the collector layer may lead to a significantly reduced specific on-resistance. However, low current gain delays the progress of the development of power BJTs. Since the BJT is fundamentally a current controlled device, it requires the complex and expensive gate drive circuits to deal with the low current gain. Moremore, at the operation of relatively high current density, the high level injection in the base region causes the further fall-off in current gain. Although the current gain can be improved by using the Darlington pair configuration, the disadvantage of this structure is a considerable increase in the on-state voltage drop.

The increased power capabilities, ease of control, and reduced costs of power switches have made power electronic systems affordable in a large number of applications. The first power switches were thyristors and bipolar transistors which have been developed in 1950's. Thyristors were used in higher power systems because their ratings were scaled at a faster pace than bipolar transistors. Bipolar transistors were favored for low and medium power applications because of their faster switching capability. Power MOSFETs differ from bipolar transistors in operating principles, specifications and performance. In fact, the performance characteristics of MOSFETs are generally superior to those of bipolar

transistors with significantly faster switching time, simpler driver circuitry, the absence of or reduction of the second breakdown failure mechanism, the ability to be paralleled and stable gain and response time over a wide temperature range.

By the virtue of electrically-isolated gate, a MOSFET is described as a high-input impedance, voltage-controlled device, whereas a bipolar transistor is low-input impedance, current controlled device. As a majority carrier semiconductor, a MOSFET stores no charge and so can switch faster than a bipolar switch. Majority carrier semiconductors also tend to slow down as temperature increases. This effect, brought about by the carrier mobility (where mobility is a term that defines the average velocity of carrier in terms of the electrical field imposed on it) makes a MOSFET more resistive at elevated temperatures and much more immune to thermal-runaway problem as experienced by bipolar devices.

The rating of these devices grew steadily until the late 1970s, the year in which the first power MOSFET was introduced. Since the introduction of the first power MOSFET, Si power MOSFET have been immensely improved and has become the dominant device technology since 1980s for many applications, due to following reasons:

1. MOSFET has a very high input impedance due to its MOS gate structure. Hence, it provides the simplest gate drive requirements. The creation of either inversion layers or accumulation layers under the MOS channel can be controlled using integrated circuits because of the small gate current that is required to charge and discharge the high input gate capacitance.

2. The MOSFET is a majority carrier device hence there is no minority charge storage involved in its operation. This results in faster switching operation.

3. Compared to the bipolar transistors the MOSFETs have superior ruggedness and forward biased safe operating area which allows the elimination of snubber circuits for protection of the switch during operation in typical hard-switching applications.

4. As the majority carriers in silicon exhibit increasing resistivity with temperature, the thermal run away behavior is avoided in MOSFETs. MOSFET devices are formed as

parallel combination of many thousands of individual MOSFET cells to take advantage of the thermal behaviour. Any device carrying excess current will heat up and become more resistive, diverting current into parallel paths. Excessive loss still produces thermal failure in MOSFET, but there is no unstable runaway effect if the parasitic BJT does not act. Due to these excellent characteristics, it would be desirable to utilize power MOSFETs for high voltage/power electronic applications.

However, the blocking voltage capability of the MOSFET is based upon the ratings of the reverse body diode of the drift region. This blocking voltage is determined in part by the distance from source to drain. High blocking voltage capability implies high resistance because of geometry, so there is a trade-off between low drift region resistance and diode voltage capability.

3.6.1 TYPES OF POWER MOSFETS

Power MOSFET can be classified under the following categories:

1) DMOS or Double implanted MOSFET or DIMOSFET
2) UMOS or UMOSFET
3) Lateral or LDMOSFET

3.6.1.1 DMOS

Basically DMOS or Double implanted MOSFET or DIMOSFET and UMOS or UMOSFET are vertical type MOSFET. The DMOS, or "Double-implanted MOS", power MOSFET is shown in Fig.3.7. This device is analogous to the silicon "DMOS", or "double-Diffused MOS", power MOSFET except that the P base and N^+ source regions are produced by ion implantation instead of thermal diffusion (diffusion is not practical in SiC because of the very low diffusion coefficients in the material).

The first SiC DIMOS power transistors were developed in June 1996 [16,32].These devices exhibited blocking voltages in excess of 760 V, approximately 3 times higher than the best SiC MOSFETs up to that time. Specific on-resistance was 125 $m\Omega\text{-}cm^2$ for the 760 V

devices and 66 mΩ-cm^2 for 2 µm channel length devices on the 500 V wafer. In June 1997 Lateral DIMOS (LDMOS) power transistors in SiC were introduced [16,33**]**.

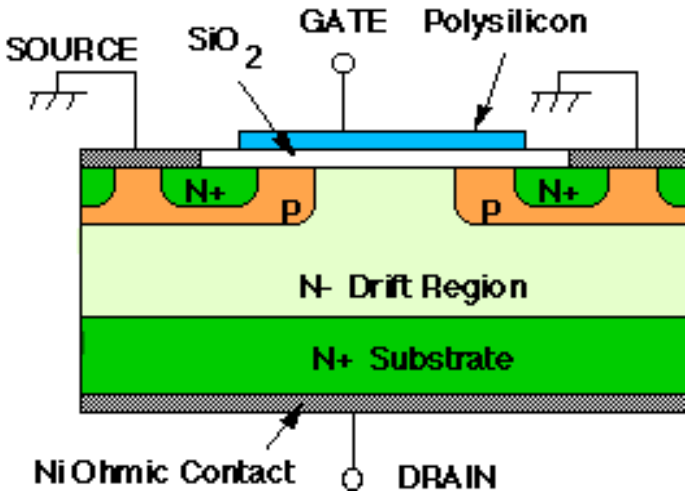

Fig. 3.7 Cross section of a SiC ion-implanted "DIMOSFET" power transistor [12].

These devices exhibited a blocking voltage of 2.6 kV, which is still the highest blocking voltage for any SiC power switching device. In DIMOS device, a positive bias on the poly silicon gate creates a surface inversion layer at the interface between the SiO2 and the P-type SiC. Electrons flow from the N^+ source along the inversion layer to the N-drift region. Upon reaching the drift region, electrons flow vertically to the N^+ drain at the bottom. The thick, lightly doped N-drift region is needed for large drain voltage when the device is in the off state (gate at ground).

3.6.1.2 UMOSFET

Most of the previous work in SiC power transistors has been devoted to the trench-gate or "UMOS" power transistor, shown in Fig.3.8.The electric fields in the blocking state (transistor OFF) are shown at the right. Looking at the blue (right-hand) plot, we note that the electric field in the oxide at the bottom of the trench is 2.5 times higher than the peak field in the semiconductor. Such a high electric field will lead to catastrophic breakdown of the oxide. The field at the corner of the trench is even higher due to two-dimensional effects.

This oxide breakdown problem represents a major limitation to the UMOSFET structure in SiC.

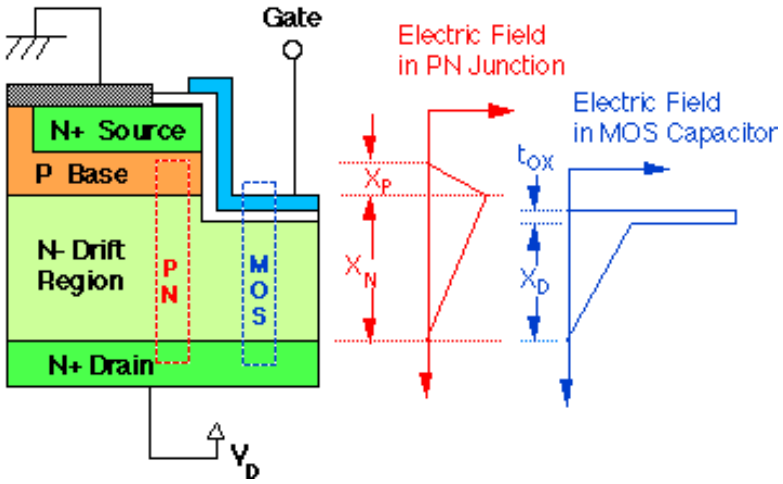

Fig 3.8 Cross section of a UMOS power transistor in silicon carbide. The electric field is illustrated on the right side for two regions within the device, the pn junction region and the MOS capacitor region. The field in the oxide at the base of the trench is 2.5 times higher than the peak field in the semiconductor because of the discontinuity in dielectric constants at the interface [12].

A novel UMOS structure, with Integral Oxide Protection (IOP) as shown in Fig 3.9, that limits the electric field in the trench oxide while simultaneously reducing on-resistance. This structure is shown in Fig.3.9, along with the electric fields in the blocking state. The new P-type region in the bottom of the trench reduces the electric field at the oxide/semiconductor interface to zero, thereby protecting the oxide from high electric fields in the blocking state. The new N-type epilayer beneath the P-base prevents pinch-off of the conducting channel in the on-state and facilitates lateral current spreading into the drift region. The device in Fig.3.9 also includes a lightly-doped N-type epilayer grown on the sidewalls of the trench. This layer converts the device into an accumulation-layer MOSFET, or "ACCUFET", increasing the MOSFET mobility and further reducing on-resistance.

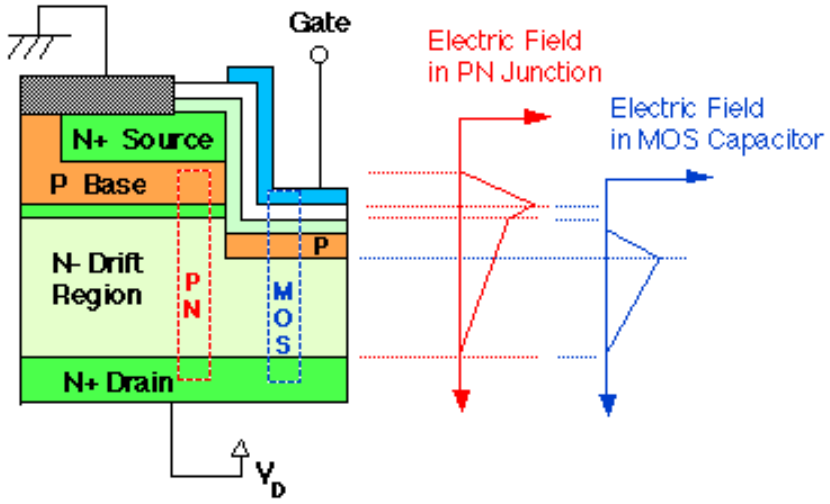

Figure 3.9 Cross section of the recently-introduced IOP-UMOS power transistor. The electric field is illustrated on the right side for two regions within the device. The P-type region under the trench reduces the field in the oxide at the base of the trench to zero [12].

3.6.1.3 LATERAL OR LDMOSFET

MOSFETs and thyristors had been fabricated as vertical structures with the substrate acting as an anode, before the advent of power devices of SiC. In the off state, the voltage was blocked by a reverse-biased pn junction. In order to achieve high blocking voltage, the drift region should be lightly doped and thick. For a given device thickness, there was a maximum possible blocking voltage regardless of doping. For SiC lateral MOSFETs with a 10 μm drift region, the maximum possible voltage is 1600V. To overcome the limitations of vertical-type MOSFETs we use the lateral type MOSFET. The structure of lateral DMOSFET is as shown in Figure 3.10.

The principal difference between this structure and the conventional inversion-layer structure is the presence of a thin n-channel region (accumulation-layer) below the gate oxide using a buried p-well region formed by the ion-implantation. The thickness, length, and n-doping of this accumulation-layer is carefully chosen so that it is completely depleted by the built-in potential of the p-n junction. This causes a potential barrier between the n+ source and the n-drift regions, resulting in a normally off device with the entire drain voltage supported by the p/n-drift region.

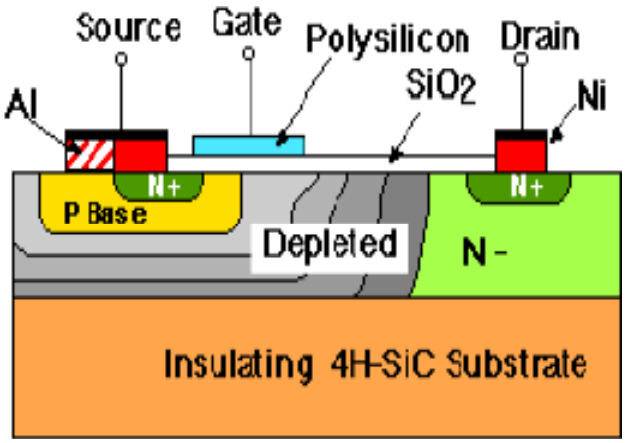

Fig 3.10 Cross section of Lateral MOSFET [12]

Thus it can support high forward blocking voltages at zero gate bias with low leakage currents. When a positive gate bias is applied, an accumulation channel of electrons at the SiO_2-SiC interface is created and hence, a low resistance path for the electron current flow from the source to the drain can he achieved. This structure utilizes the buried p-well region as a shield to the influence of a high SiC bulk electric filed on the gate oxide [34]. The structure also offers the possibility of moving the channel away from the oxide interface, thereby removing the effect of interface quality on the channel mobility.

CHAPTER 4

6H-SiC DIMOSFET USING UNIFORM DOPING PROFILE

4.1 BRIEF INTRODUCTION TO 6H DIMOSFET

The Double Implanted Metal-Oxide Semiconductor (DIMOS) field effect transistor has been frequently used in high voltage power electronics applications. Power switching devices are reaching the upper limits imposed by low breakdown field of silicon, and high breakdown voltage can be achieved only by using a semiconductor with a higher breakdown field. SiC is unique among compound semiconductors since its native oxide is SiO_2, the same oxide as of silicon. This means that power devices used in silicon can all be fabricated in SiC. DIMOS transistors are common in silicon power device technology where the p-base and n+ source regions are formed by diffusion of impurities through a common mask opening.

MOSFET's have a high input impedance which makes the gate drive circuitry very simple. Because of very high switching speeds, power MOSFET's have several advantages over power bipolar transistors for high-frequency applications where switching power losses are dominant. Additionally, compared with power bipolar transistors they show an excellent safe operating area and better output characteristics for paralleling. These characteristics of power MOSFET's are useful for many high-frequency applications such as inverters and switch-mode power supplies.

However, these advantages are offset by the high specific on-resistance $R_{on,sp}$ associated with Si power MOSFET's for high breakdown voltages. Consequently, the use of Si power MOSFET's has been limited to breakdown voltages below 1000 V. This evaluation is in terms of the reduction in the on-resistance and consequent improvement in current-handling capability of SiC power MOSFET's at higher breakdown voltages. The improvement in the current-handling capability of the SiC MOSFET's over the Si MOSFET's is quite significant at higher breakdown voltages where it could show approximately a twenty-fold improvement in specific on-resistance $R_{on,sp}$ for the same junction temperature

and device packaging. This would allow a considerable increase in the power rating or a decrease in the chip size, for the SiC devices as compared with Si devices.

The first MOSFETs in SiC were reported in late 1980s and the first power MOSFETs in 1994. The power devices were the vertical trench MOSFETs or UMOSFETs. UMOSFETs are attractive because the base and source regions are formed epitaxially without the need for ion implantation and associated high temperature annealing. In UMOSFETs, the MOS channel is formed on the sidewalls of trenches created by RIE. However, SiC UMOSFETs have been reported to have two serious problems. The problems are as given below.

(i) A high electric field occurs in the gate oxide caused by higher electric fields in the SiC drift region. This problem occurs at the trench corners leading to catastrophic failure of the gate oxide at higher drain voltages, thus restricting the maximum operating voltage to less than 40% of ideal breakdown voltage,

(ii) The low inversion layer mobility along the trench sidewalls results in high specific on-resistance, which nullifies the advantage of low drift region in SiC. By 1995, UMOSFETs fabricated on the carbon face of SiC had achieved the breakdown voltage of about 260V.

A way to avoid the problem with oxide breakdown at the trench corners is to eliminate the trenches. This was accomplished in 1996 with the introduction of planar implanted DIMOSFETs [32]. This is the main reason why we have switched to fabrication of DIMOSFETs to meet our requirements. Since impurity diffusion is impractical in SiC, the base and source regions are formed by selective ion implantation using aluminum or boron for the p-type base and nitrogen for n+ source. Because p-type implants are conducted at temperatures between 1600 ^{o}C and 1700 ^{o}C, self-aligned implant process using polysilicon gates are not practical in SiC and realignment tolerances must be allowed between the base, the source and the gate features. Due to these disadvantages, the elimination of the trench corners resulted in a threefold improvement in device blocking voltage to 760 V. This blocking voltage was achieved using 6H-SiC [16]. Also 10 kV SiC powers MOSFET have been reported in recent years [35].

4.1.1 6H DIMOSFET STRUCTURE

The DIMOS structure is fabricated by using planar diffusion technology with a refractory gate such as poly-silicon. Cross sectional structure of Sic 6H-DIMOS is shown in figure 4.1. In these devices, the P-base and N^+-source regions are diffused through a common window defined by the edge of the poly silicon gate. The surface channel region is defined by the difference in the lateral diffusion between the P-base and N^+-source region.

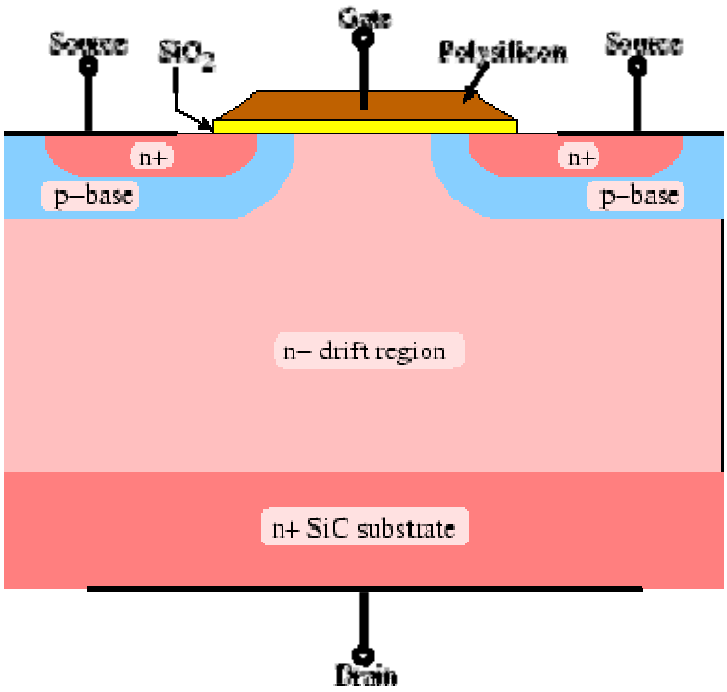

Fig. 4.1 Cross section of DIMOS power transistor in SiC [25]

The forward blocking capability is achieved by the PN-junction between the P-base region and the N-drift region. During device operation, a fixed potential to the P-base region is established by connecting it to the source metal by a break in the N^+-source region. By short-circuiting the gate to the source and applying a positive bias to the drain, the P-base/N-drift region junction becomes reverse-biased and this junction supports the drain voltage by the extension of a depletion layer on both sides. However, due to the higher doping level of the P-base layer, the depletion layer extends primarily into the N-drift region. On applying a positive bias to the gate electrode, a conductive

path extending between the N^+-source region and the N-drift region is formed. The application of positive drain voltage results in a current flow between drain and source through the n-drift region and conductive channel.

4.1.2 THEORY OF 6H DIMOSFET DEVICES

To understand the flow of the current in the power DIMOS it is essential to analyze physics of the MOS device structure. It controls the characteristics of the channel region, which is responsible for output characteristics of the device. Physics of the power DIMOS have only majority carrier i.e. unipolar device. The power MOSFET structure contains two back-to-back junctions created between the N+ source, P-base, and N-type drain regions.

4.1.2.1 MOS INTERFACE PHYSICS

The conductivity of the channel in the power MOSFET structure depends upon the density of free carriers and their mobility. The charge density in the channel is governed by the gate bias. The transport mobility for these free carriers is reduced when compared with transport in the bulk of the semiconductor due to the additional surface scattering. To obtain the charge density in the semiconductor, a one-dimensional MOS structure will be first considered with an ideal dielectric layer. The ideal dielectric layer is assumed to prevent the transport of charge between the gate and the semiconductor and contains no charge within it. When a P-type semiconductor region is assumed, then the analysis of current transport in the n-channel power MOS will be applicable. In this analysis, the oxide layer is assumed to be a perfect insulator that doesn't allow any charge carrier between gate and semiconductor. The energy-band diagrams for an ideal MOS structure is with a P-type semiconductor for different bias potential at metal is shown in Fig.4.2. Here the ideal MOSFET has the following conditions,

- the insulator has infinite resistivity,
- charge can exist only in semiconductor and on the metal electrode,
- there is no energy difference between the work function of the metal and the semiconductor.

The change in the inversion region plays a key role for determination of current transport in MOSFET devices.

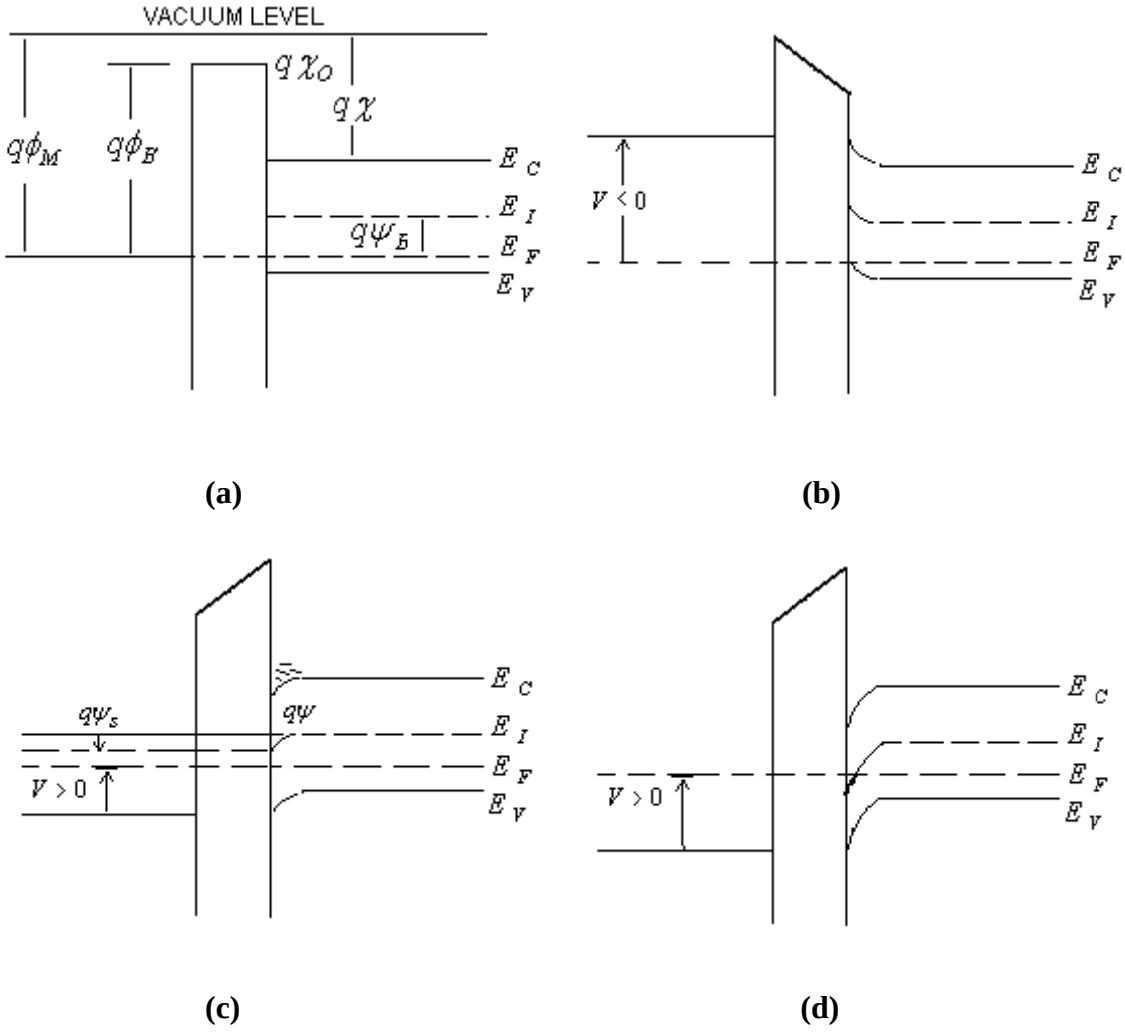

Figure 4.2 MOS structure with P-type semiconductor under different region (a) Flat-band energy band diagram (zero gate voltage), (b) accumulation (negative gate voltage), (c) depletion (positive gate voltage), (d) inversion (positive gate voltage).

4.1.2.2 SPECIFIC ON RESISTANCE OF DIMOSFET

The performance of power MOSFETs is restricted by the internal resistance. It is useful to ascertain the minimum value for the internal resistance for a power MOSFET structure that is capable of supporting a desired blocking voltage. The current flow in the power DIMOSFET during forward conduction is achieved by the applying positive gate bias voltage for N-channel device to create the conductive path. This flow is limited by the total

resistance between source and drain. This consists of several components as shown below in Fig. 4.3.

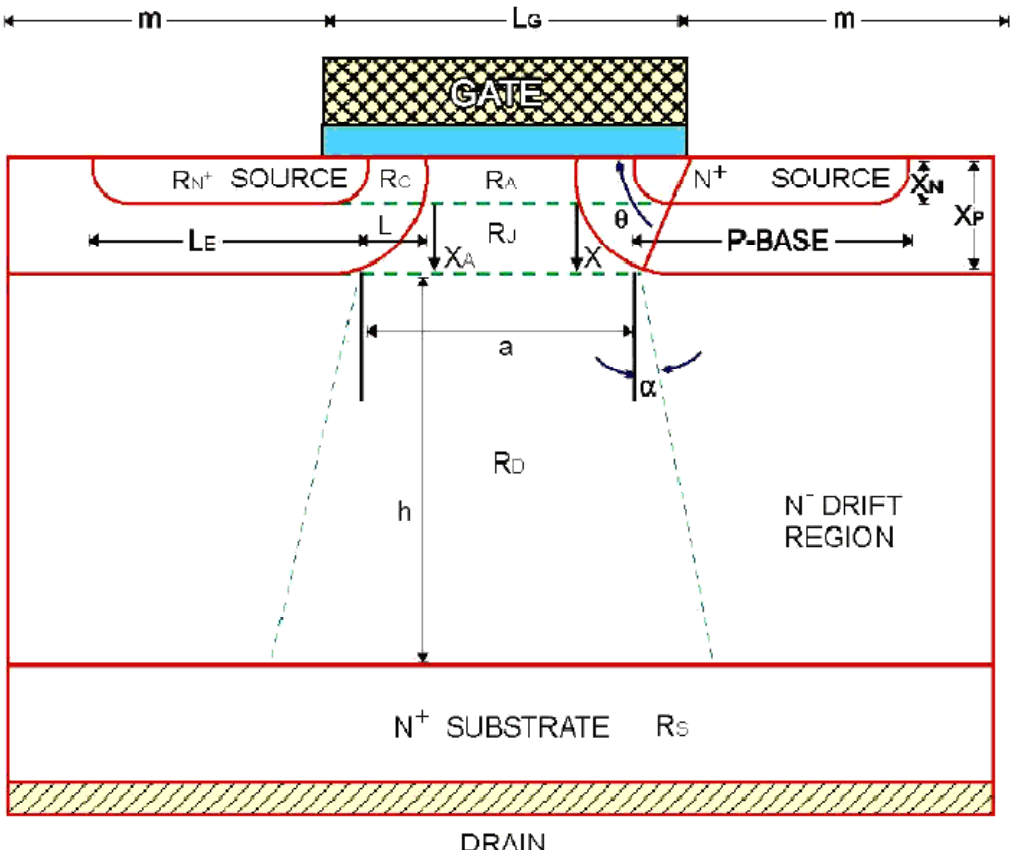

Fig. 4.3 Various specific on resistance components of DIMOSFET [4.2]

The on resistance of a power MOSFET is the total resistance between the source and drain terminals during the on-state [36]. It is the important device parameter because it determines the maximum current rating. The cell structure with each component of the specific on-resistance ($R_{on,sp}$) is shown in the Fig.4.3. The application of a positive drain voltage results in a current flow between drain and source through the N-drift region and conductive channel. The conductivity of the channel is modulated by the gate bias voltage and the current flow is determined by the resistance of various resistive components shown in Fig.4.3.

The total specific on-resistance ($R_{on,sp}$) is determined as,

$$R_{on,sp} = R_{N^+} + R_C + R_A + R_J + R_D + R_S \quad (4.1)$$

Where, R_{N^+} is the contribution from the n+ sources diffusion region

R_C is the channel resistance,

R_A is the accumulation layer resistance,

R_J is the resistance of the JFET pinch-off region,

R_D is the drift region resistance and,

R_S is the substrate resistance.

In a power MOSFET, the blocking voltage is supported across the drift layer, and thus the drift region resistance is considered to be the minimum possible theoretical limit for the on-resistance of a MOSFET. For an ideal DIMOSFET, the resistances associated with the n+ source, the n-channel, the accumulation region and the n+ substrate are assumed to be negligible and the specific on-resistance of the power MOSFET is determined by the drift region only. This assumption is not accurate at lower breakdown voltages where the drift region resistance R_D is comparable to the other resistive components and these resistances should be included in calculating Ron-sp. However, at higher breakdown voltages, R_D is significantly higher than other resistances and Ron-sp can be approximated by R_D.

4.1.2.3 BREAKDOWN VOLTAGE IN 6H DIMOSFET USING UNIFORM DOPING

The power MOSFET structure is capable of supporting a high voltage in the first quadrant of operation when the drain bias voltage is positive. During operation in the blocking mode, the gate electrode is shorted to the source electrode by the external gate bias circuit. The application of a positive drain bias voltage produces a reverse bias across junction J_1 between the P-base region and the N-drift region. Most of the applied voltage is supported across the N-drift region. The doping concentration of donors in the N-epitaxial drift region and its thickness is chosen to attain the desired breakdown voltage. In devices designed to support low voltages (<50 V), the doping concentration of the P-base region is comparable with the doping concentration of the N-drift region leading to a

graded junction profile. Consequently, a fraction of the applied drain voltage is supported across a depletion region formed in the P-base region. It is preferable to make the depth of the P-base region smaller to reduce the channel length in the power MOSFET structure. However, the design of the P-base region must take into account reduction of the breakdown voltage due to the depletion region in the P-base region reaching through to the N+ source region.

4.2 VERTICAL DIMOSFET MODEL USING UNIFORM DOPING PROFILE

There are large numbers of material and electronic properties which make SiC a promising material for high power devices, such as wide band gap (~ 3eV), high breakdown field of 3MV/cm and good thermal conductivity (3W per cm K). This section analyzes the device structure of 6H-SiC vertical DIMOSFET using uniformly doped profiles. The performance of the device is limited by the quasi-saturation behavior in its characteristics. It is shown that such effect is due to the carrier velocity saturation because of the high electric field, low impurity concentration in drift layer, and narrow p-body spacing. The detail of DIMOS structure identifying different regions of operation is shown in Fig.4.4. Since the diffusion process in 6H-SiC is ineffective, ion implantation is the only way to form p-body and n+ region for the vertical structure and double diffusion is not suitable for the 6H-SiCdevice fabrications.

From the figure 4.4

h drift-region height of the device (cm, depends on V_b and doping profile),
W width of the device (cm),
W_j height of the p-body (cm),
W_t total vertical height (cm),
W_d depletion width (cm),
L channel length formed under the gate and inside the p-body (cm),
L_p length of p-body (cm),
L_{diff} separation of p-bodies (cm),
Z total length of the device (cm),
t_{ox} oxide thickness(cm),

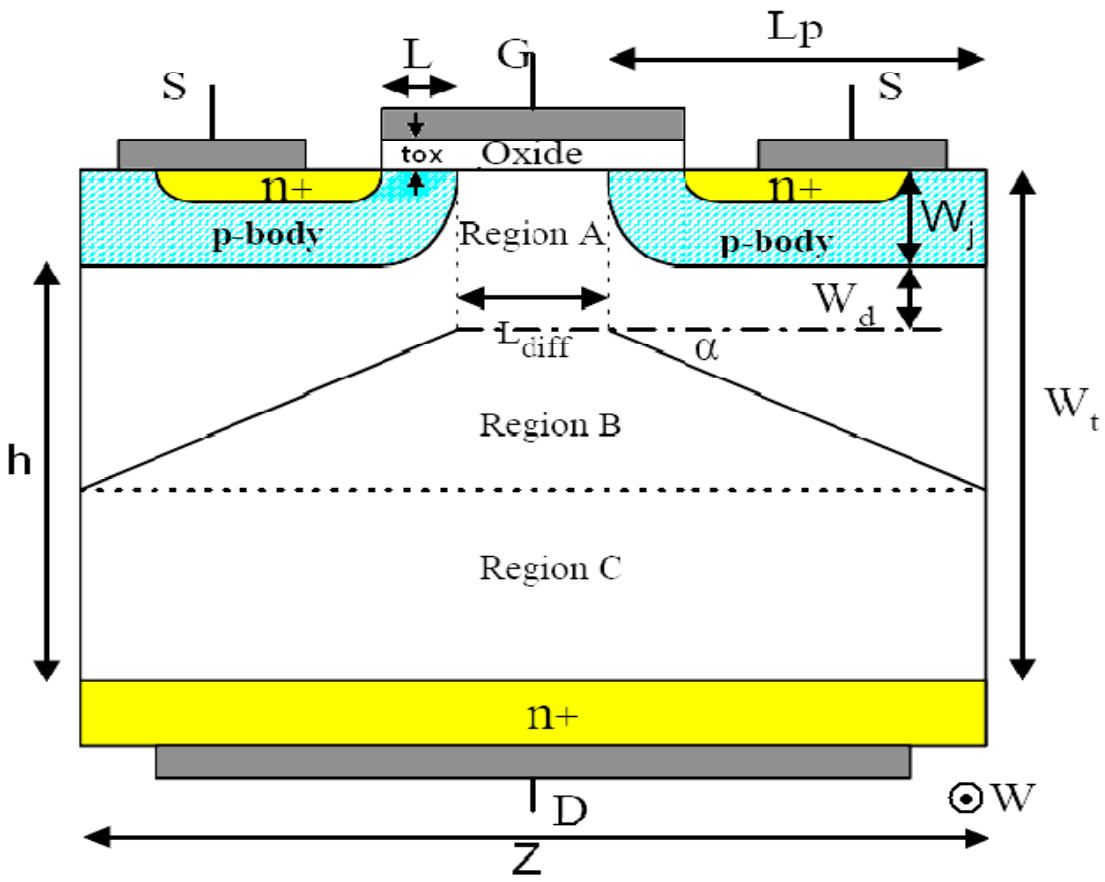

Fig. 4.4 Structure of Double Implanted Metal-Oxide Semiconductor (DIMOS) [38]

α Angle of slope of the drift region narrowing(degree)

ε_o Permittivity constant in free space (F/cm)

ε_{ox} Oxide permittivity (F/cm)

ε_{SiC} Silicon carbide permittivity (F/cm)

4.3 DEVICE EQUATIONS

Consider the depletion region between the P-base and N-drift region as a one dimensional abrupt P-N junction. It can be shown that the doping level $N_d\,(cm^{-3})$ that can support a given breakdown voltage V_B and the depletion width W (cm) at breakdown can be given as [36].

$$N_d = \varepsilon \cdot E_C^2 / (2 \cdot q \cdot V_B) \qquad (cm^{-3}) \qquad (4.2)$$

$$W = 2V_B / E_C \qquad \text{(cm)} \tag{4.3}$$

The specific on-resistance, $R_{on,sp}\ (\Omega \cdot cm^2)$ of the drift layer to support V_B is

$$R_{on,sp} = W/(q \cdot N_d \cdot \mu_n) \quad (\Omega \cdot cm^2) \tag{4.4}$$

$$= 4V_B^2/(\varepsilon_s \cdot E_C^3 \cdot \mu_n) \tag{4.5}$$

Where, ε_s is the permittivity of semiconductor (F/cm),

E_C is the critical field of breakdown (V/ cm), and

μ_n is the electron mobility $\left(cm^2/V \cdot \sec\right)$.

The equation connecting the breakdown electric field strength E_C on the doping level N_d for a P^+-N diode of 6H-SiC has been given [36]. Based on these results the relationship between E_C and N_B was obtained

$$E_C^{6H-SiC} = 1.95 \times 10^4 N_B^{0.131} \qquad (V/cm) \tag{4.6}$$

The depletion region width at breakdown can be estimated by first estimating the depletion region width for punch through breakdown voltage, V_{bpt} and is obtained using the equation [37]

$$W_u = \sqrt{\frac{2\varepsilon_s(V_{bpt}+V_{bi})}{eN_d}} \approx W_u = \sqrt{\frac{2\varepsilon_s V_{bpt}}{eN_d}} \qquad \text{(cm)} \tag{4.7}$$

Where V_{bi} = Built in potential for uniformly doped case as $V_{bi} \ll V_{bpt}$.

Wu=Depletion region width of abrupt P^+-n junction for uniformly doped profile.

ε_S = Permittivity of semiconductor used.

N_d=Doping concentration or doping level (/cc)

For the case of a uniformly doped drift region, the breakdown voltage for avalanche breakdown V_{bav} is obtained by calculating the depletion width Wu from eq. (4.7) and using the equation (4.6) as given below.

$$V_{bav} = \tfrac{1}{2} E_C W_u \qquad \text{(Volt)} \tag{4.8}$$

4.4 CALCULATIONS FOR UNIFORM DOPING PROFILE

By using the equations presented in section 4.3 the values of critical electric field, depletion region width and after that avalanche breakdown voltage has been calculated. Parameters and their values which have been used for calculation are given below

$\varepsilon_{SiC} = 9.7 * \varepsilon_0$

ε_0=8.85*10^{-14} F/cm, it is the permittivity of free space

For the calculation of breakdown voltage in this analysis, uniform doping level ranges has been considered from 10^{14} donor atoms /cc to 10^{20} donor atoms /cc.

Set of equations (4.6) to (4.8) have been used to calculate the critical electric field ,depletion region width at punch through breakdown voltage $V_{bpt,}$ and corresponding avalanche breakdown voltage $V_{bav.}$

The calculated values are given in tables from 4.1 to table 4.4, and their related graphs are given in figures from 4.5 to 4.8.

4.5 TABLES AND GRAPHS FOR UNIFORM DOPING PROFILE

Table 4.1 Values of depletion region width W_u at different value of doping level for different value of Punch through Breakdown voltage (V_{bpt})

Doping N_d (/cc)	Depletion region width Wu (µm)				
	V_{bpt}=1kV	V_{bpt}=5kV	V_{bpt}=10kV	V_{bpt}=15kV	Vbpt=20kV
10^{15}	32.758	73.248	103.588	126.869	146.496
10^{16}	10.358	13.163	32.757	40.119	46.326
10^{17}	03.275	07.324	10.358	12.686	14.649
10^{18}	01.035	02.316	03.275	04.011	04.632
10^{19}	00.327	00.732	01.035	01.268	01.464
10^{20}	00.103	00.231	00.327	00.401	00.463

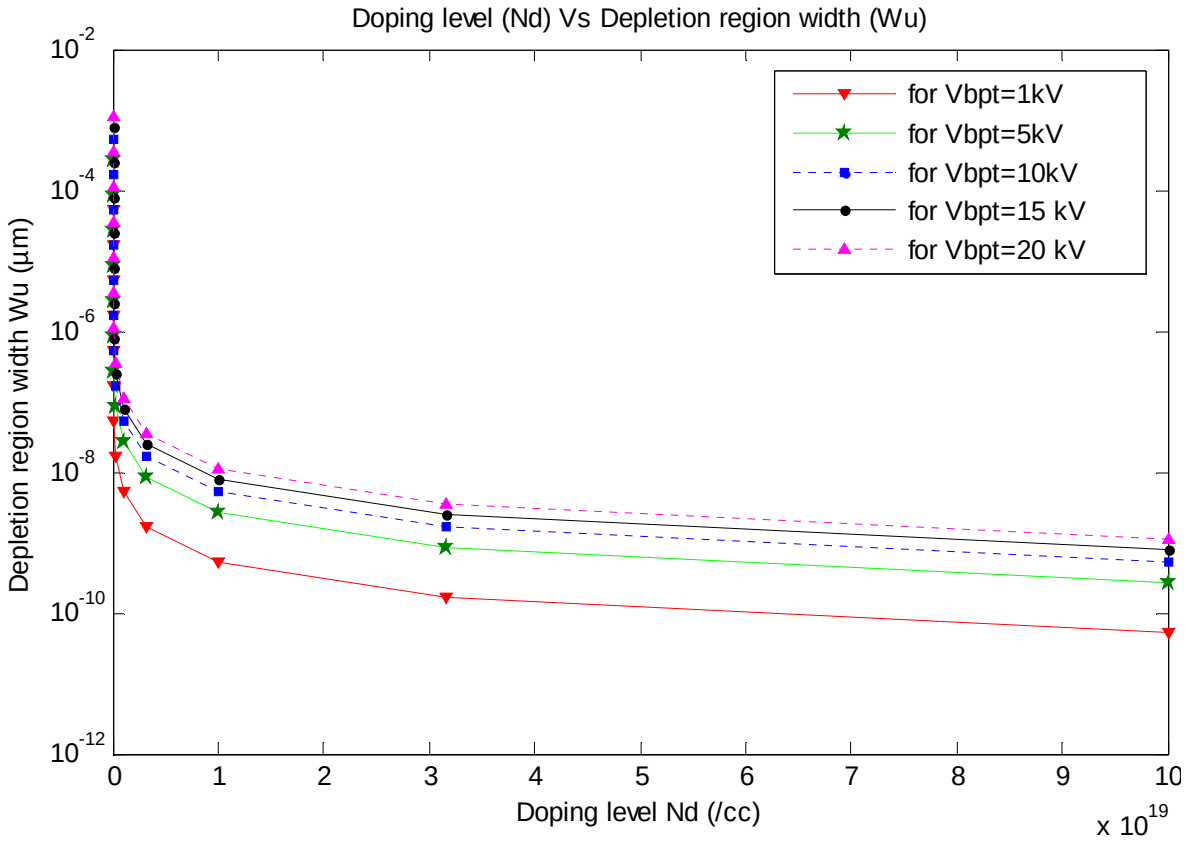

Fig. 4.5 Plot of depletion region width against doping level for different value of Punch through Breakdown voltage.

Table 4.2 Values of Depletion region width Wu (µm) at different values of Punch through Breakdown voltage (V_{bpt}) for different value of doping level N_d (/cc) using uniform doping profile.

V_{bpt} (kV)	Depletion region width Wu (µm)					
	$N_d=10^{15}$ (/cc)	$N_d=10^{16}$ (/cc)	$N_d=10^{17}$ (/cc)	$N_d=10^{18}$ (/cc)	$N_d=10^{19}$ (/cc)	$N_d=10^{20}$ (/cc)
1	32.758	10.358	03.275	01.035	00.327	00.103
5	73.248	13.163	07.324	02.316	00.732	00.231
10	103.588	32.757	10.358	3.275	1.035	0.327
15	126.869	40.119	12.686	4.011	1.268	0.401
20	146.496	46.326	14.649	4.632	1.464	0.463

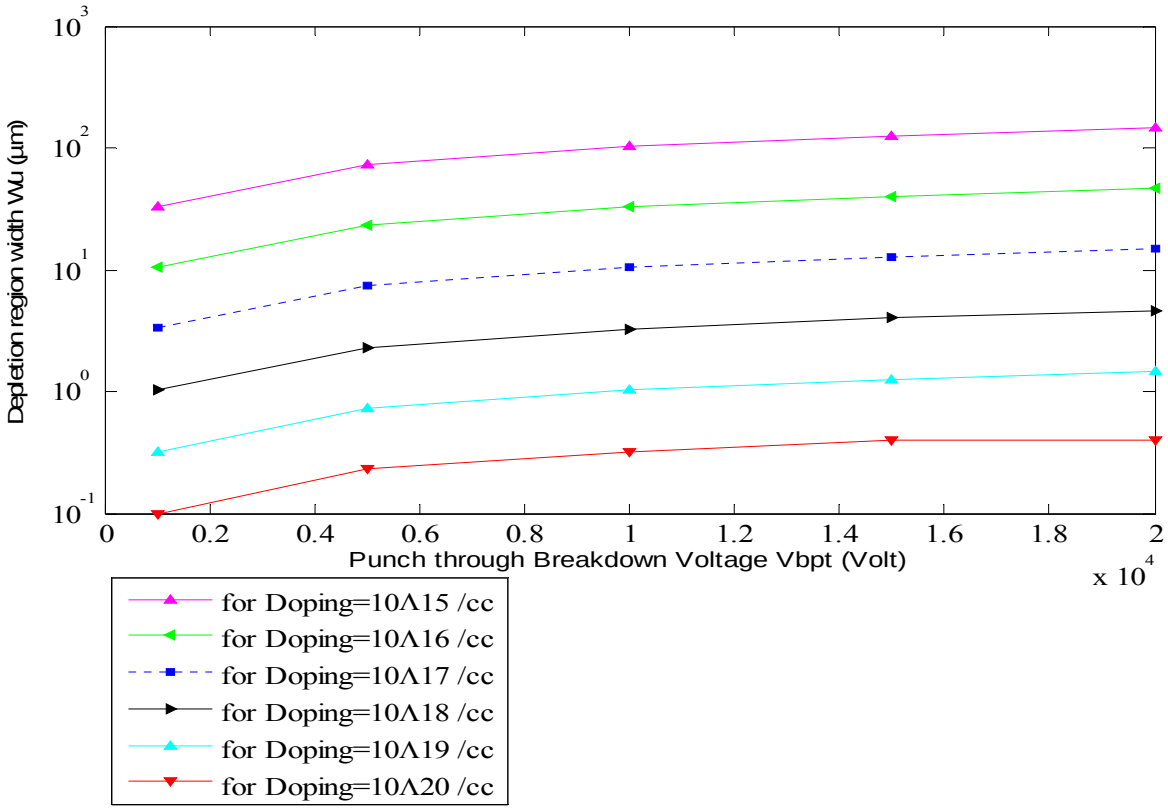

Fig 4.6: Plot of Depletion region width (W_u) against Punch through Breakdown voltage (V_{bpt}) for different value of doping

Table 4.3 Values of critical electric field at different doping levels using uniform doping profile.

Doping level N_d (/cc)	Critical electric field E_c (V/cm)
10^{15}	1.799 x 10^6
10^{16}	2.432 x 10^6
10^{17}	3.288 x 10^6
10^{18}	4.446 x 10^6
10^{19}	6.012 x 10^6
10^{20}	8.128 x 10^6

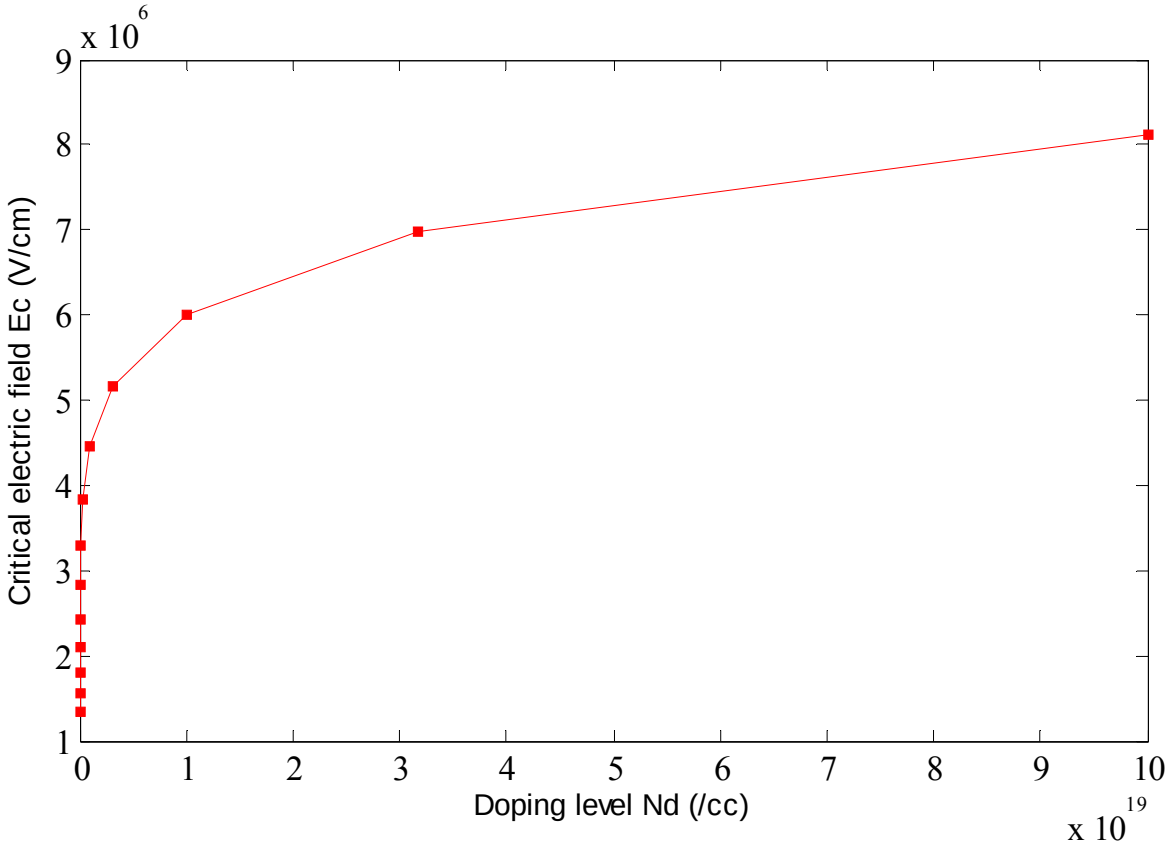

Fig 4.7 Plot of critical electric field against different value of doping levels

Table 4.4 Values of Avalanche Breakdown voltage at different values of doping for different value of Punch through breakdown voltage.

Doping level N_d /cc	Avalanche breakdown voltage V_{bav} (kV)				
	V_{bpt}=1 kV	V_{bpt}=5 kV	V_{bpt}=10 kV	V_{bpt}=15 kV	V_{bpt}=20 kV
10^{15}	2.946	6.555	9.317	11.412	13.177
10^{16}	1.259	2.817	3.983	4.879	5.634
10^{17}	0.538	1.204	1.703	2.086	2.408
10^{18}	0.460	0.514	0.728	0.891	1.029
10^{19}	0.098	0.220	0.311	0.381	0.440
10^{20}	0.042	0.094	0.133	0.163	0.188

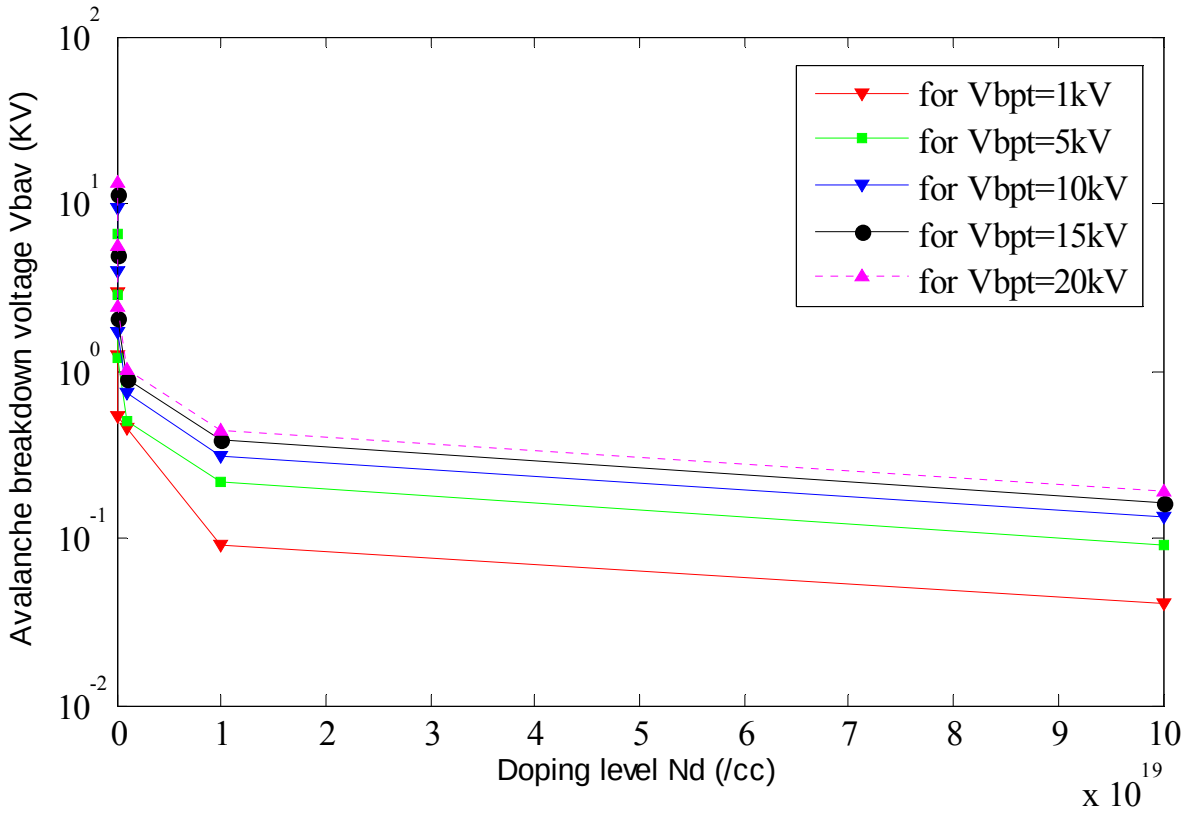

Fig 4.8 Plot of Avalanche Breakdown voltage (V_{bav}) against different value of Doping level.

CHAPTER 5

6H-SiC DIMOSFET USING LINEARLY GRADED PROFILE

In the present chapter an analysis of depletion region width and breakdown voltage of the 6H-SiC DIMOSFET using linearly graded doping profile in drift region has been described. Model of 6H-SiC DIMOSFET has been utilized from previous chapter 4 (From fig: 4.4).

5.1 DEVICE EQUATIONS USED IN LINEARLY GRADED PROFILE

Gradient of the profile can be obtained by dividing the doping density by device height and can be given by formula as given under [39]

$$G = \frac{N(x) - N(0)}{h} \qquad (\text{cm}^{-4}) \qquad (5.1)$$

Where G = Gradient of profile

N(x) = Desired doping density

N(0) = Lowest doping density, used as reference doping level for calculating the gradient at different desired doping density.

h = Device height

Values of depletion region width at Punch through Breakdown voltage for linearly graded profile can be obtained from Equation as given below [40].

$$W_g = \sqrt[3]{\frac{12\varepsilon_{SiC}(V_{bpt}+V_g)}{eG}} \approx \sqrt[3]{\frac{12\varepsilon_{SiC}V_{bpt}}{eG}} \qquad (\text{cm}) \qquad (5.2)$$

Where W_g = Depletion region width of linearly graded junction

V_{bpt} = Punch through Breakdown voltage

e = Electronic charge ($1.6*10^{-19}$ coulombs)

V_g = Gradient voltage

N_{eff} = effective doping concentration

And $V_g << V_{bpt,}$

Effective doping can be given by following relations [40]

$$Neff = \frac{Gh}{\ln(1+\frac{Gh}{N_0})} \quad (/cc) \tag{5.3}$$

Where G= Gradient of the profile

h= Device height

Value of critical electric field can be obtained as

$$E_C = \frac{eG}{8\varepsilon_{SiC}}(W_g)^2 \quad (V/cm) \tag{5.4}$$

And avalanche breakdown voltage (V_{bav}) can be calculated as given under

$$V_{bav} = \frac{2}{3}E_C W_g \quad (Volt) \tag{5.5}$$

5.2 CALCULATIONS FOR LINEARLY GRADED PROFILES

By using set of equations from (5.1) to (5.5) value of gradient, depletion region width, critical electric field, and avalanche breakdown voltage can be calculated.

For calculation of gradient, device heights for different Punch through Breakdown voltage ($V_{bpt)}$ has been taken from table 5.1 as given below, and these heights have been calculated using uniform doping level 10^{14} /cc.

Table 5.1 Values of device height at different values of Punch through Breakdown voltage (V_{bpt}).

Punch through Breakdown voltage V_{bpt} (kV)	Device height (h) (µm)
1	103.588
5	231.631
10	327.567
1 5	401.197
20	463.264

5.3 TABLES AND GRAPHS FOR LINEARLY GRADED PROFILE

Table 5.2 Values of depletion region width (W_g) at different values of gradient (G) for different value of Punch through Breakdown voltage (V_{bpt}).

V_{bpt}=1kV		V_{bpt}=5kV		V_{bpt}=10kV		V_{bpt}=15kV		V_{bpt}=20kV	
G (cm^{-4})	W_g (µm)	G (cm^{-4})	W_g (µm)	G (cm^{-4})	W_g (µm)	G (cm^{-4})	W_g (µm)	G (cm^{-4})	W_g (µm)
8.69 x10^{16}	90.493	3.86 x10^{16}	202.348	2.75 x10^{16}	286.164	2.24 x10^{16}	350.778	1.94 x10^{16}	404.697
9.56 x10^{17}	40.689	4.27 x10^{17}	90.098	3.02 x10^{17}	128.672	2.45 x10^{17}	157.590	2.13 x10^{17}	181.970
9.64 x10^{18}	18.829	4.31 x10^{18}	42.104	3.04 x10^{18}	59.544	2.49 x10^{18}	72.926	2.15 x10^{18}	84.208
9.65 x10^{19}	8.737	4.32 x10^{19}	19.537	3.05 x10^{19}	27.629	2.49 x10^{19}	33.839	2.16 x10^{19}	39.074
9.65 x10^{20}	4.055	4.32 x10^{20}	9.068	3.05 x10^{20}	12.824	2.49 x10^{20}	15.706	2.15 x10^{20}	18.136
9.65 x10^{21}	1.882	4.32 x10^{21}	4.209	3.05 x10^{21}	5.952	2.49 x10^{21}	7.290	2.15 x10^{21}	8.418

Table 5.3 Values of critical electric field Ec (V/cm) at different values of gradient G(cm^{-4}) for different values of Punch through Breakdown voltage V_{bpt} (kV).

V_{bpt}=1kV		V_{bpt}=5kV		V_{bpt}=10kV		V_{bpt}=15kV		V_{bpt}=20kV	
G (cm^{-4})	Ec (V/cm)	G (cm^{-4})	Ec (V/cm)	G (cm^{-4})	Ec (V/cm)	G (cm^{-4})	Ec (V/cm)	G (cm^{-4})	Ec (V/cm)
8.69 $x10^{16}$	0.165 $x10^{6}$	3.86 $x10^{16}$	0.371 $x10^{6}$	2.75 $x10^{16}$	0.524 $x10^{6}$	2.24 $x10^{16}$	0.642 $x10^{6}$	1.94 $x10^{16}$	0.741 $x10^{6}$
9.56 $x10^{17}$	0.369 $x10^{6}$	4.27 $x10^{17}$	0.808 $x10^{6}$	3.02 $x10^{17}$	1.164 $x10^{6}$	2.45 $x10^{17}$	1.428 $x10^{6}$	2.13 $x10^{17}$	2.648 $x10^{6}$
9.64 $x10^{18}$	0.797 $x10^{6}$	4.31 $x10^{18}$	1.781 $x10^{6}$	3.04 $x10^{18}$	2.519 $x10^{6}$	2.49 $x10^{18}$	3.085 $x10^{6}$	2.15 $x10^{18}$	3.562 $x10^{6}$
9.65 $x10^{19}$	1.717 $x10^{6}$	4.32 $x10^{19}$	3.838 $x10^{6}$	3.05 $x10^{19}$	5.429 $x10^{6}$	2.49 $x10^{19}$	6.649 $x10^{6}$	2.16 $x10^{19}$	7.678 $x10^{6}$
9.65 $x10^{20}$	3.698 $x10^{6}$	4.32 $x10^{20}$	8.271 $x10^{6}$	3.05 $x10^{20}$	11.697 $x10^{6}$	2.49 $x10^{20}$	14.325 $x10^{6}$	2.15 $x10^{20}$	16.542 $x10^{6}$
9.65 $x10^{21}$	7.968 $x10^{6}$	4.32 $x10^{21}$	17.889x 10^{6}	3.05 $x10^{21}$	25.199 $x10^{6}$	2.49 $x10^{21}$	30.861 $x10^{6}$	2.15 $x10^{21}$	35.638 $x10^{6}$

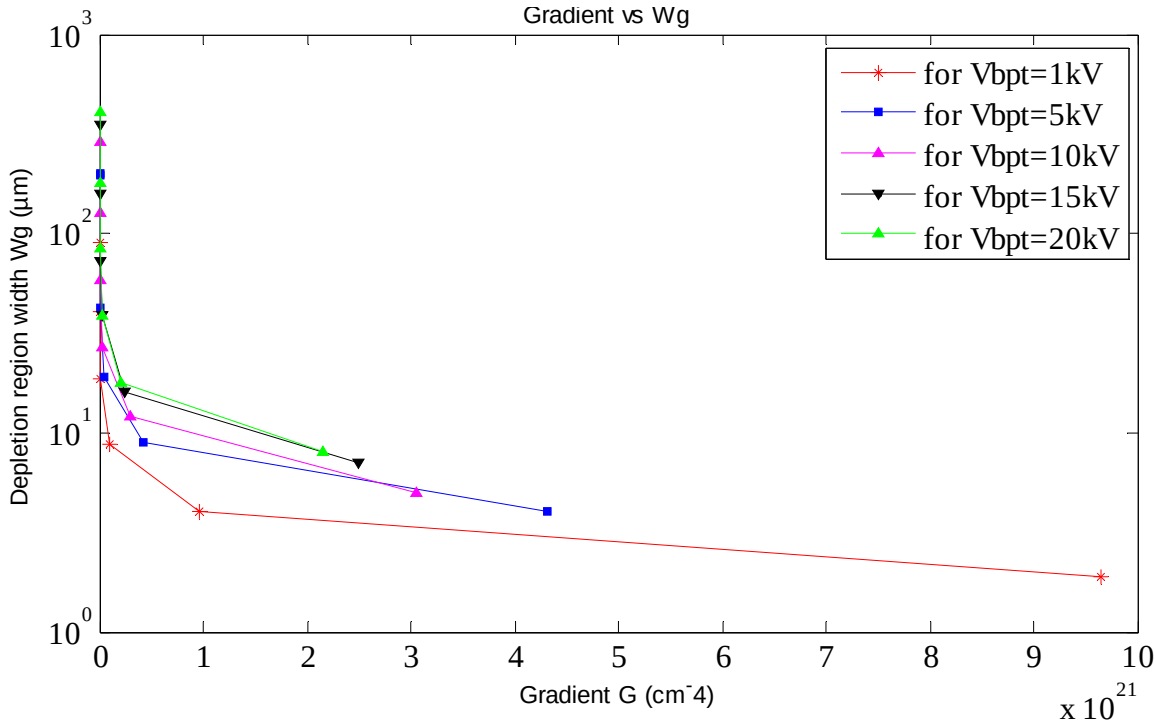

Fig. 5.1 Plot of depletion region width (W_g) against different value of Gradient (G) for different value of Punch through Breakdown voltage (V_{bpt}).

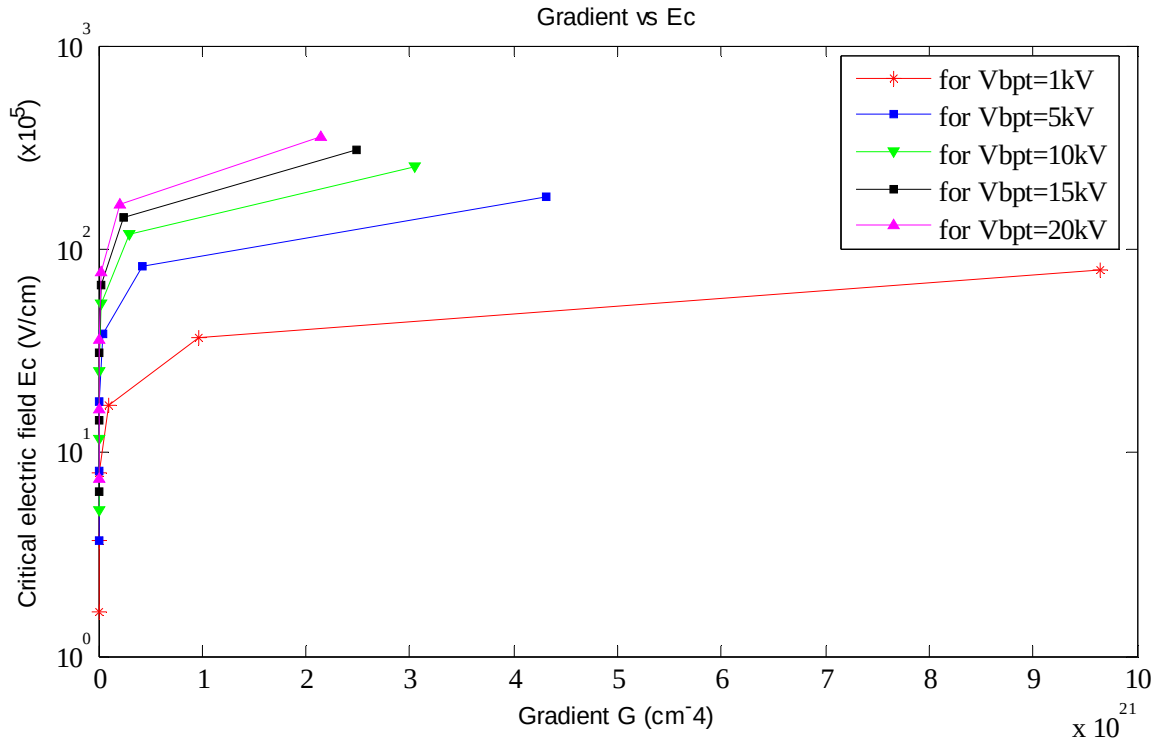

Fig 5.2 Plot of critical electric field E_c against different values of gradient (G) for different values of Punch-through Breakdown voltage (V_{bpt}).

Table 5.4 Values of depletion region width W_g (µm) at different value of Punch through Breakdown voltage (V_{bpt}) for different values of effective doping N_{eff} (/cc).

V_{bpt} (kV)	Depletion region width W_g for different value of effective doping (µm)					
	N_{eff} (/cc) $3.90x10^{14}$	N_{eff} (/cc) $2.15x10^{15}$	N_{eff} (/cc) $1.45x10^{16}$	N_{eff} (/cc) $1.08x10^{17}$	N_{eff} (/cc) $0.87x10^{18}$	N_{eff} (/cc) $0.72x10^{19}$
1	90.493	40.689	18.829	8.737	4.055	1.882
5	202.348	90.098	42.104	19.537	9.068	4.209
10	286.164	128.672	59.544	27.629	12.824	5.952
15	350.778	157.590	72.926	33.839	15.706	7.290
20	404.697	181.970	84.208	39.074	18.136	8.418

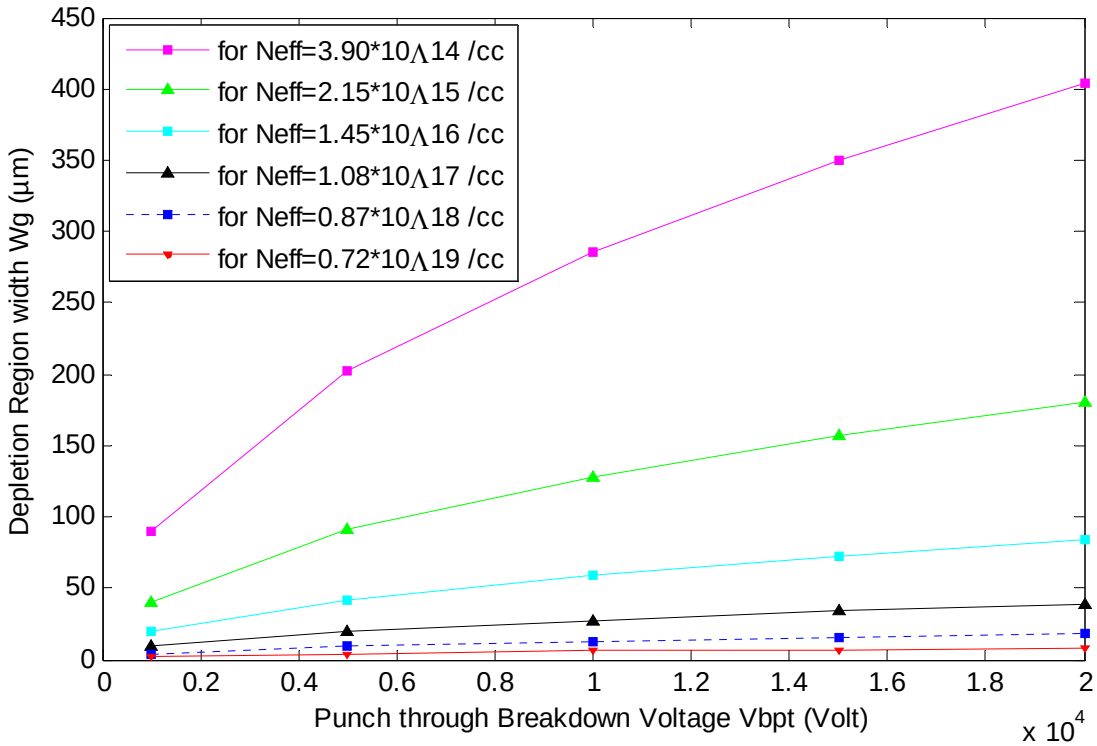

Fig. 5.3 Plot of depletion region width W_g (µm) against Punch through Breakdown voltage V_{bpt} (kV) for different value of effective doping N_{eff} (/cc).

Table 5.5 Values of critical electric field E_c (V/cm) at different values of Punch through Breakdown voltage (V_{bpt}) for different values of effective doping.

V_{bpt} (kV)	Critical electric field E_c (V/cm)					
	N_{eff} (/cc) $3.90x10^{14}$	N_{eff} (/cc) $2.15x10^{15}$	N_{eff} (/cc) $1.45x10^{16}$	N_{eff} (/cc) $1.08x10^{17}$	N_{eff} (/cc) $0.87x10^{18}$	N_{eff} (/cc) $0.72x10^{19}$
1	$0.165\ x10^6$	$0.369x10^6$	$0.797x10^6$	$1.717x10^6$	$3.698x10^6$	$7.968x10^6$
5	$0.371x10^6$	$0.808x10^6$	$1.781x10^6$	$3.838x10^6$	$8.271x10^6$	$17.88x10^6$
10	$0.524x10^6$	$1.164x10^6$	$2.519x10^6$	$5.429x10^6$	$11.697x10^6$	$25.199x10^6$
15	$0.642x10^6$	$1.428x10^6$	$3.085x10^6$	$6.649x10^6$	$14.325x10^6$	$30.861x10^6$
20	$0.741x10^6$	$2.648x10^6$	$3.562x10^6$	$7.678x10^6$	$16.542x10^6$	$35.638x10^6$

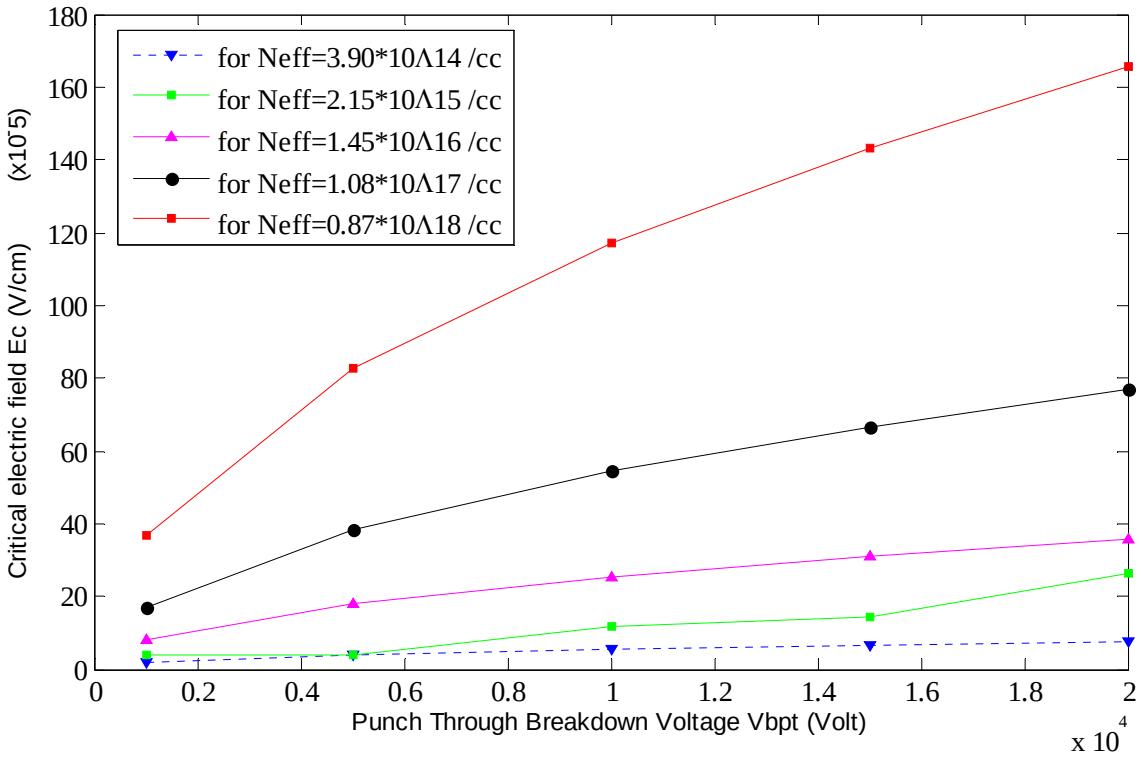

Fig. 5.4 Plot of Critical Electric field against different values of Punch through Breakdown voltage (V_{bpt}) for different values of effective doping.

Table 5.6 Values of avalanche breakdown voltage V_{bav} at different values of effective doping N_{eff} (/cc) and different value of gradient for different value of punch through breakdown voltage.

N_{eff} (/cc)	Avalanche breakdown voltage V_{bav} (kV)									
	V_{bpt}=1 kV		V_{bpt}=5 kV		V_{bpt}=10 kV		V_{bpt}=15 kV		V_{bpt}=20 kV	
	G (cm^{-4})	V_{bav} (kV)	G (cm^{-4})	V_{bav} (kV)	G (cm^{-4})	V_{bav} (kV)	G (cm^{-4})	V_{bav} (kV)	G (cm^{-4})	V_{bav} (kV)
$3.90x10^{14}$	$8.69 x10^{16}$	0.99	$3.86 x10^{16}$	4.99	$2.75 x10^{16}$	9.99	$2.24 x10^{16}$	14.99	$1.94 x10^{16}$	19.99
$2.15x10^{15}$	$9.56 x10^{17}$	0.99	$4.27 x10^{17}$	4.85	$3.02 x10^{17}$	9.96	$2.45 x10^{17}$	14.99	$2.13 x10^{17}$	19.95
$1.45x10^{16}$	$9.64 x10^{18}$	1.00	$4.31 x10^{18}$	4.95	$3.04 x10^{18}$	9.99	$2.49 x10^{18}$	14.99	$2.15 x10^{18}$	19.99
$1.08x10^{17}$	$9.65 x10^{19}$	1.00	$4.32 x10^{19}$	4.99	$3.05 x10^{19}$	9.75	$2.49 x10^{19}$	15.00	$2.16 x10^{19}$	19.75
$0.87x10^{18}$	$9.65 x10^{20}$	1.00	$4.32 x10^{20}$	4.99	$3.05 x10^{20}$	9.99	$2.49 x10^{20}$	14.99	$2.15 x10^{20}$	19.68
$0.72x10^{19}$	$9.65 x10^{21}$	0.99	$4.32 x10^{21}$	4.99	$3.05 x10^{21}$	9.85	$2.49 x10^{21}$	14.99	$2.15 x10^{21}$	19.99

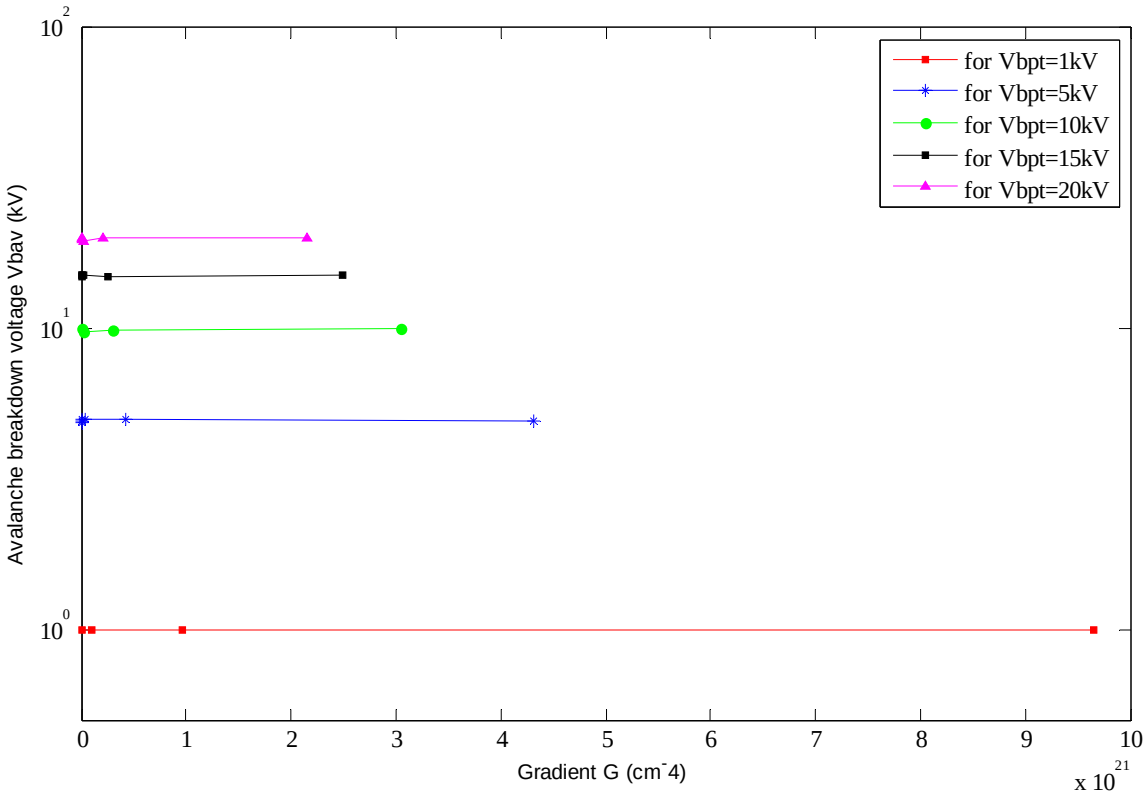

Fig. 5.5 Plot of Avalanche Breakdown voltage V_{bav} at different values of effective doping and different value of gradient for different value of Punch through Breakdown voltage.

CHAPTER 6

CONCLUSIONS AND SCOPE OF FUTURE WORK

The work presented in this thesis is an analysis of the variation of depletion region width and breakdown voltage namely punch through and avalanche breakdown voltage for various gradients in the drift region of 6H-SiC DIMOSFET. The drift region has been considered to have a linearly graded profile with the doping level of 10^{14} /cc near the source and increasing linearly to values of 10^{15}, 10^{16}……..10^{20} (/cc) near the drain over the finite pre-calculated device height.

The results of the linearly graded device have been compared with those of a 6H-SiC DIMOSFET with uniformly doped drift region. The range of voltages selected were from 1 kV to 20 kV with increments of 5 kV for successive punch-through breakdown voltages. The results for the two devices have been compared with each other in terms of the doping level on the basis of uniformly doped drift region device with results of nearly same effective concentration for linearly graded drift region devices. It was found that for a punch through voltage (V_{bpt}) of 1 kV the depletion region width varies from 32.758 μm for a uniform doping of 10^{15} /cc to 0.013 μm for a doping of 10^{20}/cc .

At a doping level of 10^{17}/cc the depletion region width for V_{bpt} of 1 kV the depletion width was 3.725 μm and it increase to 8.737 μm for a gradient of $9.65x10^{19}$ (cm^{-4}) with corresponding N_{eff} of 1.45 $x10^{17}$ /cc. This can be verified from Table 4.1, 5.3 and 5.5. The same range of variation is observed for V_{bpt} of upto 20 kV from the same set of tables.

The critical electric field for a uniformly doped device at a doping level of 10^{15}/cc was 1.799 $x10^{6}$ (V/cm) increasing to $8.128x10^{16}$ (V/cm) at a doping level of 10^{20} /cc and is shown in Table 4.3. However at a V_{bpt} of 1 kV N_{eff} values of $3.9x10^{14}$ /cc at a gradient of $8.69x10^{16}$ cm^{-4} the critical field was $0.165x10^{6}$ V/cm increasing to $0.741x10^{6}$ V/cm at a gradient of $1.94x10^{16}$ cm^{-4} at V_{bpt} of 20 kV in linearly graded profile. Increasing gradients of upto $9.65x10^{21}$ cm^{-4} give a higher critical electric field (E_c) of 7.968 $x10^{6}$ V/cm for V_{bpt} of 1 kV. The corresponding E_c values for V_{bpt} of 20 kV for gradients from $1.94x10^{16}$ cm^{-4} to

$2.15x10^{21}$ cm^{-4} give E_c values ranging from $0.74x10^6$ V/cm to $35.68x10^6$ V/cm. this can be seen from table 5.3.

In comparison with uniformly doped device from Table 4.3 it can be seen that the linearly graded device can be used easily to obtain much higher values of E_c than uniformly doped device. For linearly graded devices with precalculated device heights, it was found that punch through and avalanche breakdown voltages were almost equal for all values of gradients and N_{eff} for linearly graded DIMOSFETS. This can be verified from Table 5.6. However this type of tally is not seen in the case of uniformly doped devices as shown in Table 4.4. Here break down voltages V_{bpt} and V_{bav} are found to be nearly equal only in the case of doping level of 10^{15} for V_{bpt} of 5 kV, 10 kV and doping level of 10^{16} for V_{bpt} of 1 kV. Equivalence of these two breakdown voltages have not been established for other doping levels and breakdown voltages.

Thus it can be seen that at the expense of an increase in the depletion region width of uniformly doped drift region devices of 6H-SiC DIMOSFET, the magnitude of critical field E_c, V_{bpt} and V_{bav} can be significantly increased by decreasing the magnitude of the concentration gradient in the drift region.

In the end, it can be said that other non-linear profiles like the Gaussian or complementary error function profile can be used in the drift region of 6H-SiC DIMOSFETS which may possibly help to develop still better devices with smaller device heights and higher breakdown voltages.

REFERENCES

[1] M. Kitabatake, S.Kazama, C.Kudou, Advanced Devices Development Center, Panasonic Corporation, Yagumo-naka-machi, Moriguchi, Osaka 570-8501, Japan. M. Imai, A. Fujita, S. Sumiyoshi, H. Omori ,Core Technology Development Center, Corporate Engineering Division, Home Appliances Company, Panasonic Corporation, Noji-higashi, Kusatsu City, Shiga, Japan,"4H-SiC-DIMOSFET power device for home appliances", 978-1-4244-5393-1/10©2010 IEEE.

[2] B. J.Baliga, Silicon Carbide Power Devices, page vii Copyright © 2005 by World Scientific Publishing Co. Pte. Ltd.

[3] S. Bernet, "Recent developments of high power converters for industry and traction applications," IEEE Trans. Power Electron., vol. 15, pp. 1102–1117, Nov. 2000.

[4] N. Hingorani, "Introducing custom power," IEEE Spectrum, vol.32, pp. 41–48, 1995.

[5] "Flexible ac transmission," IEEE Spectrum, vol. 30, pp. 40–45, Apr. 1993.

[6] F. Nozari and H. S. Patel, "Power electronics in electric utilities: HVDC Power Transmission Systems," Proc. IEEE, vol. 76, pp. 495–506, Apr. 1988.

[7] L. Gyugyi, "Power electronics in electric utilities: Static Var Compensators," in Proc. IEEE, vol. 76, Apr. 1988, pp. 483–494.

[8] Liangchun C. Yu, Greg T. Dunne, Kevin S. Matocha, Member, IEEE, Kin P. Cheung, John S. Suehle, and Kuang Sheng, Senior Member, IEEE" Reliability Issues of SiC MOSFETs : A Technology for High-Temperature Environments" *IEEE Transactions On Device And Materials Reliability,* Vol. 10, No. 4, December 2010.

[9] AHMED ELASSER, MEMBER, IEEE, AND T. PAUL CHOW, *senior member*, IEEE, "Silicon Carbide Benefits and Advantages for Power Electronics Circuits and Systems*", proceedings of the IEEE, VOL. 90, NO. 6, June 2002.*

[10] C. Codreanu, M. Avram, E. -Carbunescu, E. Iliescu, "Comparison of 3C-SiC, 6H-SiC and 4H SiC MESFETs performances", Materials Science in Semiconductor Processing, p. 137-142, 2000.

[11] Jerry L. Hudgins, Senior Member, IEEE, Grigory S. Simin, Member, IEEE, Enrico Santi, Senior Member, IEEE,and M. Asif Khan, Member, IEEE" An Assessment of Wide Bandgap Semiconductors for Power Devices" IEEE transactions on Power electronics, vol. 18, no. 3, may 2003

[12] www.ecn.purdue.edu/WBG/SiC Data Bank, Introduction, Basic Studies, Device Research: From the Purdue's Wide Band Gap Semiconductor Device Research in Electrical and Computer Department, America.

[13] B. Ozpineci L. M. Tolbert, "Comparison of Wide-Bandgap Semiconductors for Power Electronics Applications", December 12, 2003, OAK RIDGE NATIONAL LABORATORY Oak Ridge, Tennessee 37831, ORNL/TM-2003/257.

[14] G. Brezeanu, "Silicon Carbide (SiC): A short history: An analytical Approach for SiC Power device design", University "POLITEHNICA" Bucharest, Romania 0-7803-9214-© 2005 IEEE.

[15] J.J. Berzelius, Ann. Phys. Lpz., 1 (1824) 169-230.

[16] Jayarama N. Shenoy, Student Member, IEEE, James A. Cooper, Jr., Fellow, IEEE, and Michael R. Melloch, Senior Member, IEEE, High-Voltage Double-Implanted Power MOSFET's in 6H-SiC IEEE electron device letters,VOL. 18, NO. 3, march 1997.

[17] Kent Bertilsson,"Simulation and Optimization of SiC Field Effect Transistors" Doctoral Thesis, Laboratory of Solid State Devices (SSD) Department of Microelectronics and Information Technology (IMIT) Royal Institute of technology (KTH) Stockholm 2004.

[18] M. Roschke, F. Schwiertz, "Electron mobility Models for 4H, 6H, and 3C SiC", IEEE trans. Elec. Dev. Vol. 48, No. 7, 2001, pp1442-1447.

[19] http://www.grc.nasa.gov/WWW/SiC/SiCReview.html: Philip G. Neudeck, NASA Lewis research Center, M.S. 77-1, 21000, Brook Park road, Cleveland, OH 441 35.

[20] Gerhard pensl, florin ciobanu, thomas frank, michael krieger, sergey reshanov, frank schmid, ichael weidner Institute of Applied Physics,University of rlangen-Nurnberg,Staudtstrasse7D-91058Erlangen,Germany, International Journal of High Speed Electronics and Systems Vol. 15, No. (2005) 705-745, © World Scientific Publishing Company, SiC material properties.

[21] PHILIP G.NEUDECK, SENIOR MEMBER, IEEE, ROBERT S.OKOJIE, MEMBER, IEEE, AND LIANG-YU CHEN, “High-Temperature Electronics- A Role for Wide Bandgap Semiconductors?”, Proceedings of the IEEE, VOL. 90, NO. 6, JUNE 2002.

[22] Sze S. M., Physics of Semiconductor Devices, 2nd. Edition, Wiley-Interscience, New York.

[23] Baliga, B. J. and Bhatnagar, M.,“Comparison of 6H-SiC, 3C-SiC, and Si” for power devices Proceedings of the IEEE, 82, 1112, 1994. Power Devices, IEEE Transactions on Electron Devices, 40, 645, 1993.

[24] Philip G. Neudeck NASA Lewis Research Center, M.S. 77-1, 21000 Brook park Road, Cleveland, OH 44135 USA “SiC Technology (1998)”.

[25] http://www.iue.tuwien.ac.at/phd/ayalew/node77.html

[26] Crofton, J., Sriram, S.: IEEE Trans. Electron Devices, Vol.43 (1996), p. 2305.

[27] H. M. Mc Glothlin, D. T. Morisette, J. A. Cooper, Jr., and M. R. Melloch, "4 kV Silicon Carbide Schottky Diodes for High-Frequency switching Applications,"IEEE Device Research Conf., Santa Barbara, CA, June 28 - 30, 1999.

[28] G. M. Dolny, D. T. Morisette, P. M. Shenoy, M. Zafrani, J. Gladish, J. M. Woodall, J. A: Cooper, Jr., and M. R. Mellach, "Static and Dynamic Characterization of Large-Area High-Current-Density SiC Scltottky Diodes," IEEE Device Research Conf., Charlottesville, VA, June 22 - 24, 1998.

[29] L. Yuan, M.R. Melloch, J.A. Cooper, and K.J. Webb, " Silicon Carbide IMPATT Oscillators for High-Power Microwave and Millimeter-Wave Generation, " IEEE/ Cornell Conference on Advanced Concepts in High Speed Semiconductor Devices and Circuits, Ithaca, NY, August 7-9, 2000.

[30] W.Xie, J.A.Cooper, Jr., M.R.Melloch, J.W.Palmour and C.H.Carter, Jr.,"A Vertically Integrated Bipolar Storage Cell in 6H Silicon Carbide for Nonvolatile Memory Applications, "IEEE Electron Device Lett., 15,212(1994).

[31] Ashoke K. Chatterjee and Munish Vashishath. Recent trends in silicon carbide device research Mj. Int. J. Sci. Tech. 2008, 2(03), 444-470.

[32] J.N. Shenoy, M.R. Melloch, and J.A. Cooper, Jr., " High-Voltage Double-Implanted MOS Power Transistors in 6H-SiC, " IEEE Device Research Conf., Santa Barbara, CA, June 24-26, 1996.

[33] J. Spitz, M.R. Melloch, and J.A. Cooper, Jr., " 2.6 kV 4H-SiC Power MOSFET", (late news) IEEE Device Researh Conf., Ft.Collins, CO, June 23- 25, 1997.

[34] Tesfaye Ayalew, Jong-Mun Park, Andreas Gehring, Tibor Grasser, and Siegfried Selberherr, ”Silicon Carbide Accumulation-Mode Laterally Diffused MOSFET”. Institute for Microelectronics, TU Vienna, A-1040 Vienna, Austria Ayalew@iue.tuwien.ac.at.

[35] Jun Wang, Student Member, IEEE, Tiefu Zhao, Student Member, IEEE, Jun Li, Alex Q. Huang, Fellow, IEEE, Robert Callanan, Fatima Husna, and Anant Agarwal, Member, IEEE, “Characterization, Modeling, and Application of 10-kV SiC MOSFET”, IEEE Transactions On Electron Devices, Vol. 55, NO. 8, August 2008.

[36] Ashoke Kumar Chatterjee and Munish Vashishath, “Theoretical analysis and design of double implanted MOSFET on 6H silicon carbide wafer for low power dissipation and large breakdown voltage” , Mj. Int. J. Sci. Tech. 2008, 2(02), 308-319.

[37] Sze, S. M., Physics of Semiconductor Devices, 2nd. Edition, Wiley-Interscience, New York.

[38] M.Hasanuzzaman, S.K.Islam, L.M.Tolbert, B.Ozpineci, “Model Simulation and Verification of a Vertical Double Implanted (DIMOS) Transistor In 4H-SiC”, proceedings of the 7th IASTED International Multi-Conference, ece.utk.edu., pp.1,2003.

[39] Rajneesh Talwar and A.K.Chatterjee, “Estimation of power dissipation of a 4H-SiC Schottky barrier diode with a linearly graded doping profile in the drift region”, Maejo International Journal of Science and Technology, vol.03, issue 02, pp. 352- 6, 2009.

[40] Rajneesh Talwar and A.K.Chatterjee, “Analytical Estimation of Breakdown Voltage and Power Dissipation of Double Implanted MOSFET on 6H Silicon Carbide Wafer with Linearly Graded Profile”, Journal of Electron Devices, Vol. 7, 2010, pp. 214-224 © JED [ISSN: 1682 -3427].