

DESIGN AND ANALYSIS OF MEMRISTOR EMULATORS USING OPERATIONAL TRANSCONDUCTANCE AMPLIFIER

*A Thesis submitted in partial fulfillment of the requirement for the Award of the
Degree of*

MASTER OF TECHNOLOGY

in VLSI Design

Submitted By

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DECLARATION

I, **Suchitra Gupta** hereby declare that the work presented in this thesis entitled "**Design and analysis of memristor emulators using operational transconductance amplifier**" in partial fulfillment of the requirement for the award of degree of **Master of Technology (VLSI Design)** submitted at **Electronics and Communication**, Thapar Institute of Engineering & Technology (Deemed to be University), Patiala is an authentic record of work carried out under supervision of **Dr. Shireesh Kumar Rai (Assistant Professor, ECED, Thapar Institute of Engineering and Technology)** from **01/01/2019 to 15/07/2019**. The matter presented in this has not been submitted either in part or full to any other university or institute for the award of any other degree.

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I would like to express our deep gratitude and thanks to all those who helped me directly and indirectly to make my effort a success.

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ABSTRACT

There are three basic elements which are generally required to form any electrical circuit. Each element is defined by one of the relations among current i , voltage v , charge q and flux Φ . The relation between voltage and current defines a resistor, the relation between charge and voltage defines a capacitor, the relation between flux and current defines an inductor. Among these, one relation between charge and flux is missing. This missing element was predicted by Leon Chua in 1971. After Chua's prediction not many people started working towards memristor due to lack of understanding and available resources. After three decades, people have started working over this topic and thus there is a huge scope of research available in this direction. In May 2008, researchers at HP Labs published a paper announcing a model for the physical realization of the memristor. This paper has drawn significant attention of researchers and made this topic alive. A new era in electronics has come due to the advantages offered by memristors in various applications. Now, memristor is expected to be used in numerous applications of analog signal processing, digital signal processing and in memory industry. But, memristor is still not easily available in device form due to complexity in fabrication, higher cost that restricts its use in real time applications. Therefore, the researchers and engineers got motivated to design the memristor emulator circuits which mimic the properties of memristor. Various emulator circuits are being reported by using various active building blocks such as current conveyers (CC), voltage differential current conveyor (VDCC), operational transconductance amplifier (OTA), current conveyor transconductance amplifier (CCTA) and differential voltage current conveyor transconductance amplifier (DVCCTA). Among these blocks, OTA is becoming popular due to its availability as off-the-shelf component, simpler in design, electronic tunable and also requires less number of passive components to realize memristor. In the thesis, different configurations of OTA have been designed to realize memristor emulator circuits. These configurations are designed to provide the advantages for memristor emulator circuits such as improvement over range of transconductance, high transconductance gain and linearity. The different structures of OTA have been used in both floating as well as grounded memristor emulator circuits. These

grounded and floating memristor emulator circuits are compared with existing configurations. A new grounded and floating memristor emulator is proposed by using CDTA, OTA and a grounded capacitor. Both incremental and decremental configuration can be formed with a slight change in the circuit. The simulations results are verified by using Mentor Graphics ELDO tool using TSMC 0.18 μ m process parameters.

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ABBREVIATIONS

PLA:	Programmable Logic Array
PAL:	Programmable Array Logic
FPGA:	Field-Programmable Gate Array
CMOS:	Complementary Metal Oxide Semiconductor
SPICE:	Simulation Program with Integrated Circuit Emphasis
TiO ₂ :	Titanium Oxide
HP:	Hewlett Packard
MOS-FET:	Metal-Oxide-Semiconductor Field-Effect Transistor
NMOS:	N – type Metal Oxide Semiconductor
PMOS:	P – type Metal Oxide Semiconductor
TSMC:	Taiwan Semiconductor Manufacturing Company
OTA:	Operational Transconductance Amplifier
VDTA:	Voltage Differential Transconductance Amplifier
CCTA:	Current Conveyer Transconductance Amplifier
CBTA:	Current Backward Transconductance Amplifier

CHAPTER 1

INTRODUCTION

There are three basic elements which are generally required to form any electrical circuit. Each element is defined by one of the relations among current i , voltage v , charge q and flux Φ . The relation between voltage and current defines a resistor ($dv=Rdi$), the relation between charge and voltage defines a capacitor ($dq=Cdv$), the relation between flux and current defines an inductor ($d\Phi=Ldi$), the time derivative of charge defines current ($dq=idt$), the time derivative of flux defines voltage ($d\Phi=vdt$). Among these, one relation between charge and flux is missing [1]. This missing element was predicted by Leon Chua in 1971 and was defined by the relation $d\Phi=Mdq$ where "M" is termed as Memristor as shown in figure 1.1. Initially, memristor has not gained popularity due to lack of knowledge and challenges of resources. After three decades of Chua's prediction, many research groups have started working over memristor and various advantages offered by memristors are now highlighted. The first memristor was fabricated by the team of Hewlett Packard (HP) led by R. Stanley Williamson 2008 [3]. This memristor was fabricated by using a thin-film of titanium oxide but it is still not commercially available in device form due to complexity in fabrication, high cost that restricts its use in real time application. This has motivated the researchers and engineers to go for the design of emulator circuits which mimic the properties of memristor. Later, Chua also defined that there are the two types of memristors which are voltage-controlled and current-controlled. The circuit which is controlled by voltage is a voltage-controlled memristor and vice-versa for current-controlled circuit

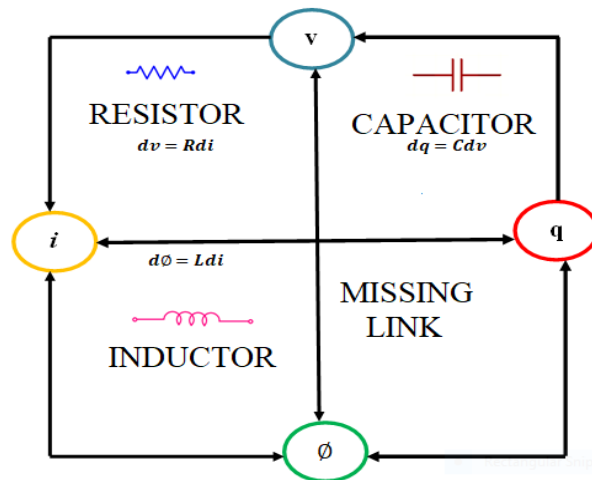


Figure 1.1. The missing link between charge and flux

Chua compared the fourth missing element to Aristotle's theory of matter. With the help of this theory he could connect the different elements and concluded that one element was missing among these. In this theory, he observed that there were four main elements: Earth, water, air and fire. He formed a relation between all the elements like moistness, dryness, coldness a hotness, and compared them to various elements of figure 1.1. Fire was related to hotness, air was related to moistness, water was related to coldness and earth was related to dryness as shown in figure 1.2. He concluded that the fourth element must be present to complete the symmetry of the elements and then gave a relationship between flux and charge which he named memristor.

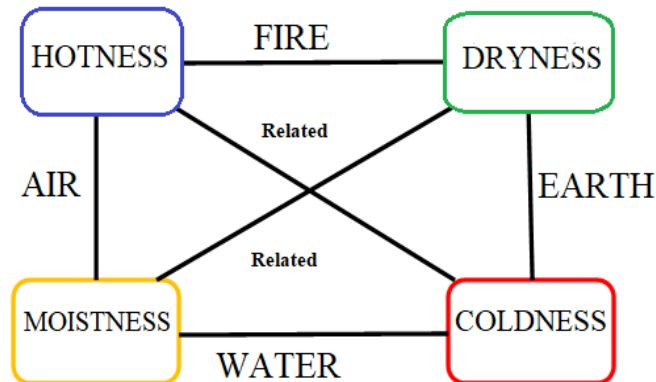


Figure 1.2. The Aristotle's theory

Figure 1.3 shows the fourth element and its relation with all the other element. It can be observed that with memristor the connections are completed which can be used in any basic electronic circuitry.

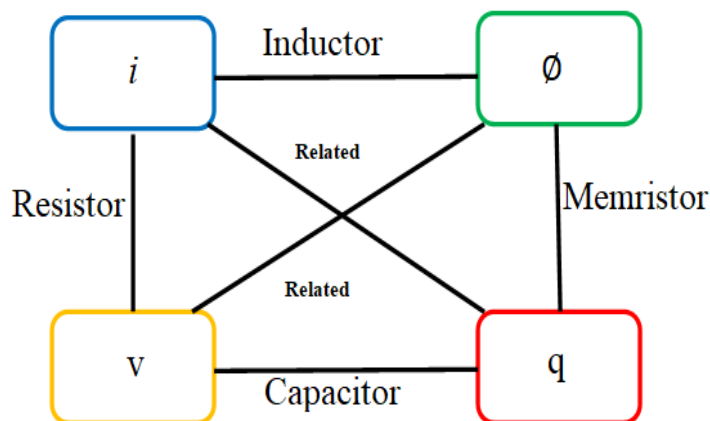


Figure 1.3. Four basic circuit elements

Memristor is the combination of two words, Memory and resistor. It is a passive element that provides resistance as well as memory in data which can be stored. It is defined as a two-terminal device in which flux is the amount of charge that has passed the device. Fig.1.4 shows the symbol of a memristor.

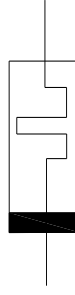


Figure 1.4. Symbol of memristor

1.1 TYPES OF MEMRISTOR

A memristor can be of two types, charge-controlled and flux-controlled. In a charge-controlled memristor, flux and charge are expressed as a function of charge whereas it is said to be flux-controlled if the relationship is expressed as a function of flux.

For a Flux-controlled memristor,

$$q = f(\phi) \quad (1.1)$$

Differentiating equation results in

$$\frac{dq}{dt} = \frac{df(\phi)}{d(\phi)} \frac{d\phi}{dt} \quad (1.2)$$

$$i(t) = w(\phi)v(t) \quad (1.3)$$

where $i(t) = \frac{dq}{dt}$, $W(\phi) = \frac{df(\phi)}{d\phi}$ is called memconductance, and $\frac{d\phi}{dt} = v(t)$.

For a Charge-controlled memristor,

$$\phi = f(q) \quad (1.4)$$

Differentiating equation (1.4) yields,

$$\frac{d\phi}{dt} = \frac{df(q)}{dq} \frac{dq}{dt} \quad (1.5)$$

Equation (1.5) can be expressed as

$$v(t) = M(q)i(t) \quad (1.6)$$

Where $i(t) = \frac{dq}{dt}$, $M(q) = \frac{df(q)}{dq}$ where $M(q)$ is memristance and $\frac{d\phi}{dt} = v(t)$

$$M(q) = \frac{df(q)}{dq} \quad (1.7)$$

In 2011 [5], Chua explained in detail about the fingerprint characteristic of memristor which is known as pinched hysteresis curve. The hysteresis graph is plotted with input current (i) and input voltage (v) meeting at zero crossing for both current-controlled and voltage-controlled memristor. A device or circuit is said to behave as a memristor if it forms the hysteresis loop. The memristor hysteresis loop must shrink with the increase in the frequency. With the increase in the temperature the loops should also shrink. In Figure 1.5, behavior of pinched hysteresis loop is observed at different frequencies and it can be observed that the loop size decreases with the increases in frequency. At a particular frequency, both the loops meet with each other and forms a straight line and therefore, behaving as a resistor. This resistor can further be used in many applications in analog and digital circuits.

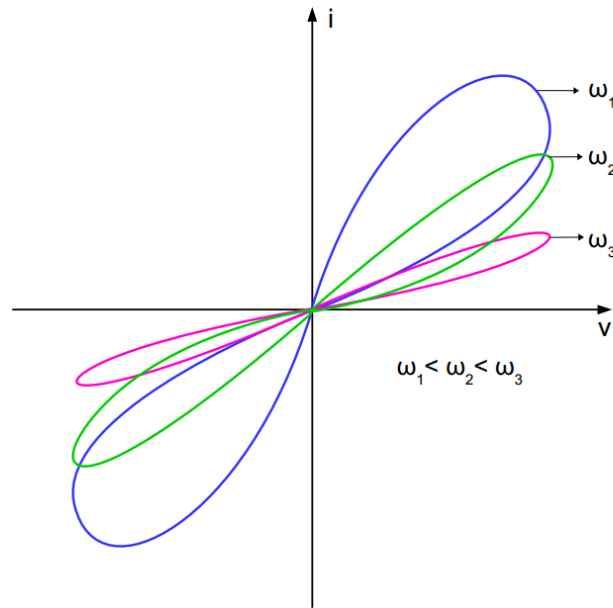


Figure 1.5. The pinched hysteresis loop

1.2 COMPOSITION OF HP MODEL

After 37 years of Chua's prediction, R. Stanley Williams et al. in Hewlett Packard (HP) fabricated a device that exhibited the properties of memristor. A device was fabricated by using a very thin layer of titanium dioxide which has been sandwiched with platinum which is placed in either side of it as shown in Fig. 1.6. A part of titanium dioxide is doped with oxygen vacancies while the other part is undoped.

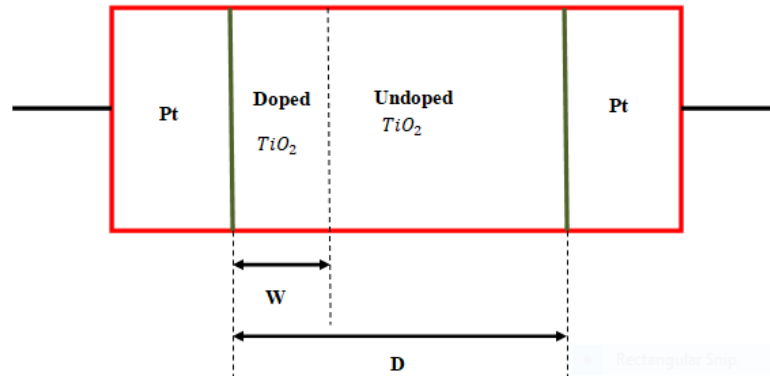


Figure 1.6. Composition of HP model

Since, the vacancies are positively charged a junction is formed where one side is doped and the other side is undoped as shown in figure 1.7. D is referred to as device length, W is referred to as length of doped region. The material property of titanium dioxide is a semiconductor and it is highly resistive in nature as shown in Fig. 1.7(a). When a positive voltage is applied, positive charged valance oxygen gets repelled and move towards the undoped region. Therefore, the boundary is shifted forward as a result the conductivity is increased as shown in Fig. 1.7(b). When a negative charge is applied, the oxygen vacancies move towards titanium dioxide layer and as a result the insulating property of the whole device is increased Fig. 1.7(c). When no voltage is applied the oxygen, vacancies don't move. Therefore, this is the reason that the data stored in memristor even when the power is switched-off and when the power is on it starts from the last point where the data was frozen. The doping material can be changed according to the need of the application.

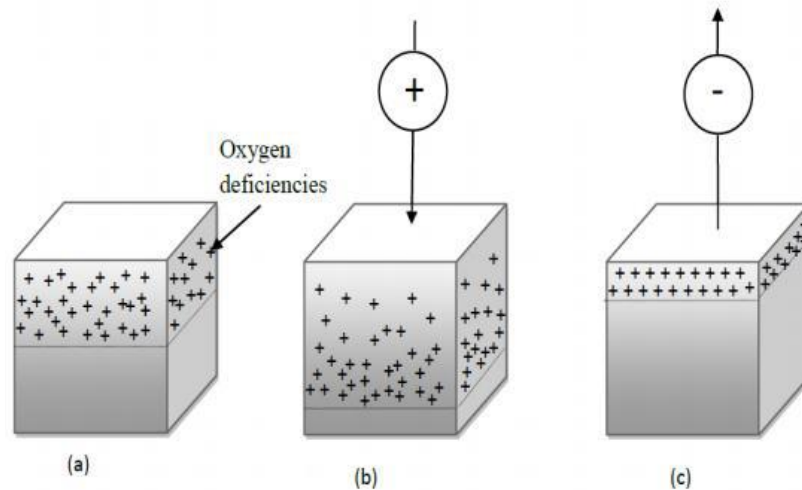


Figure 1.7. Working of HP model

Since, Memristor is not commercially available in device form, as is very costly and is difficult to fabricate. When a device has to be commercially available the cost plays a vital role and therefore, the researchers and engineers got motivated to realize emulator circuits in which various active building blocks are being used to make a circuit which mimic the properties of memristor. The memristor

emulators are realized with different blocks like voltage differential current conveyor (VDCC), operational transconductance amplifier (OTA), current feedback operational amplifier (CFOA), current conveyer transconductance amplifier (CCTA) and differential voltage current conveyor transconductance amplifier (DVCCTA). Among these blocks, OTA is becoming popular due to its availability as off-the-shelf component which is simpler in design, electronic tunable and requires less number of passive components to realize memristor. Researchers are also working on memcapacitance and meminductance, which are also not available in the device form. Memcapacitance and meminductance can also be realized from the circuit of memristor after few modifications in it. They can be further used in replacing capacitance and inductance from circuits. Inductor covers larger space in circuits and therefore, such kind of replacement will be a boom for circuits and systems. There are wide applications of memristor emulators as it provides both memory and resistance and this combination is used in most of the applications. Initially, these circuits were only used in digital circuits such as field-programmable gate array (FPGA), programmable logic array (PLA), RAM, ROM and in multi-level circuits are also embedded with memristor. The application of memristors is increased to a wide range as now it is also used in analog circuitry like filters, oscillators, amplifiers.

1.3 STRUCTURE OF THESIS

The structure of the thesis is as follows. Chapter 2 presents a detailed literature survey of memristor. Figure 1.8 gives an overview of the different chapters that are present in the thesis. In the thesis, different techniques have been applied on OTA to modify its structure. The benefits of these structures are increased linearity and enhanced gain whereas other parameters are not much affected. These advantages are future used in the memristor emulator circuit and the different results are discussed. Both floating and grounded memristor emulator are implemented with the designed OTA and a comparison among all the circuits is explained in detail.

Chapter 3 gives the structure of an existing symmetrical OTA. A detailed small signal analysis of the circuit is also presented. Different analysis like AC, DC and transient are done on the symmetrical OTA. The grounded and floating memristor emulators realized by symmetrical OTA are explained. The floating and grounded memristor emulator requires a tunable OTA and therefore, fixed bias current is replaced by a voltage tunable current mirror circuit. The memristor emulator circuit has been checked for different frequencies and a range of frequency over which the pinched hysteresis loop is not deformed is noticed. The effect of different temperature on pinched hysteresis loop of memristor emulator is also observed.

Chapter 4 presents a structure of symmetrical OTA with degeneration resistances. Detailed small signal model of the structure is also provided. The floating and grounded memristor emulator requires a tunable OTA and therefore, fixed bias current is replaced by a voltage tunable current

mirror circuit. By using source degeneration resistor, the linear range of circuit is increased. The results of OTA and memristor emulator circuits are provided at different frequencies and temperature.

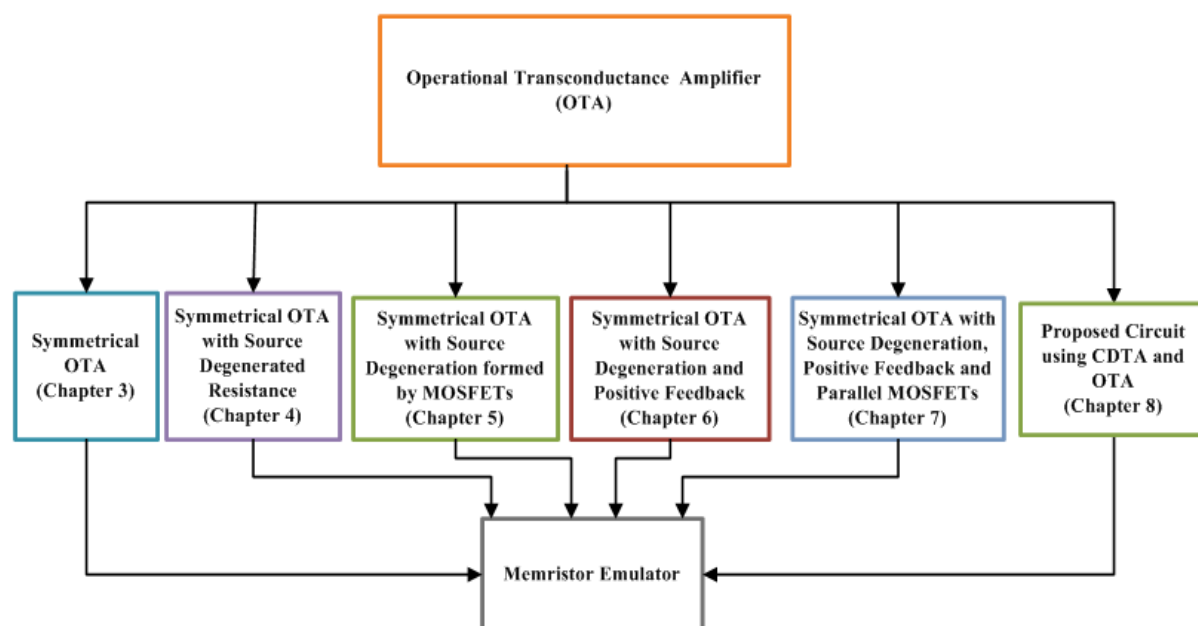


Figure 1.8 Structure of thesis

Chapter 5 gives another technique in which the source degeneration resistor is replaced by MOSFET in the structure of symmetrical OTA. The motivation of replacement is to obtain a wide tunable range for OTA that is required for the design of memristor emulator circuit. In this circuit additional current mirror is not required as the MOSFET can be used for the same. A small signal model of the structure is also explained. This technique provides a wider range of linearity. Results of OTA and memristor emulator circuits are explained in detail.

In chapter 6, both techniques namely source degeneration and positive feedback have been combined in the structure of symmetrical OTA to obtain better results. Small signal analysis has been done and various approximations have been taken to reduce the complex equations. Source degeneration maintains the linear range while the positive feedback provides a higher transconductance. The OTA designed by combining both the techniques have been used to realize memristor emulator circuits and their results are explained in detail.

Chapter 7 is a combination of three techniques which are source degeneration, positive feedback and parallel MOSFETs. These techniques provide a trade-off between transconductance gain, linearity and power dissipation. The parameters must be kept such that it should provide higher gain without affecting the other parameters of the circuit. A higher value as well as wide range of transconductance is achieved by using these techniques. The small signal model of the circuit is also explained in detail. Results of OTA and memristor emulator circuits are explained in detail.

A comparison table is provided which discusses the various results obtained in different chapters of thesis.

Chapter 8 proposes a new circuit of grounded and floating memristor emulator using CDTA and OTA. Incremental and decremental memristor emulators are also designed for both grounded and floating memristors. Pinched hysteresis loop for grounded and floating memristor are presented for frequency range of 600KHz to 2MHz. Effect of different temperatures on the pinched hysteresis loop of memristor emulator are also seen.

In Chapter 9, conclusion and future scope of the presented work has been covered.

All the simulations are performed in Mentor Graphics ELDO tool by using the TSMC 0.18um technology parameters.

CHAPTER 2

LITERATURE SURVEY

The concept of memristor (resistor with memory) was reported first by Prof. Leon Chua in 1971 which highlighted the missing element by giving the relationship between flux and charge [1]. He also gave the mathematical description of memristor and various graphs through which memristor can be better understood.

In 1976, Leon Chua and Sung Mo Kang published a paper in which he generalizing the theory of memristors and memristive systems, also giving pinched hysteresis curve characterizing current versus voltage behavior crossing at zero [2].

Buot and Rajgopal published a paper in 1994, entitled as Binary information storage at zero bias in quantum-well diodes. This paper described a similar current-voltage characteristics to the memristor in AlAs/GaAs/AlAs quantum-well diodes [3]. The analysis showed no direct connection to Chua's memristor.

In June 2009, Zdenek Biolková, Dalibor Biolková, Viera Biolková published an article for the SPICE model of the memristor. They have justified the working of the memristor. They have given the various mathematical analysis and working of the doped and undoped area of memristor. The working of the SPICE model was verified by simulation results [4].

Nadine Gergel-Hackett, Behrang Hamadani have fabricated a flexible solution-processed device that exhibits the electrical properties of a memristor [5]. All the electrical behavior like the non-volatile memory can be achieved at a very inexpensive flexible light weighted device. They have not used the expensive method using various techniques to deposit titanium oxide layer on the device whereas they have used process in which the titanium is spinning on a plastic substrate at the room temperature. This device exhibits the electrical behavior with memory storage of a memristor. The phenomena of read and write is also verified in this paper.

In 2010, a paper was published by Bharathwaj Muthuswamy in which the Chua diode was replaced by a memristor [6]. The obtained result was matched with mathematical analysis, he also implemented the circuit on a breadboard with the ICs and the results were verified.

X.Y. Wang, A.L. Fitch, H.H.C. Iu, W.G. Qi published a paper [7] in which they have shown how a memristance circuit can be changed into a memcapacitor circuit. Memcapacitor was realized by a

circuit in which LDR was used. Simulation results and emulator circuit results implemented with the help of LDR were closer to the theoretical concepts.

Changju Yang, Maheshwar Pd. Sah published an article in 2012, which gives an elaborate knowledge about the various application of memristor [8]. They realized a circuit which gives the properties of memristor by using Op-Amp. They further made the same circuit on the breadboard and verified the properties. In the paper they have also shown the various arrangements of the memristor when used in series and parallel.

In October 2012, Hyongsuk Kim, Maheshwar Pd. Sah, made an emulator circuit using off-the-shelf solid-state components. They described the same working as that of titanium oxide memristor and used the emulator circuit in parallel, series and in hybrid with opposite and same polarities [9]. The various arrangements were verified by the mathematical analysis of circuit.

In January 2013, Shahar Kvatinsky, Eby G. Friedman published a paper in which they suggested a new model of memristor known as TEAM (Threshold Adaptive Memristor Model) [10]. They also explained the characteristics of memristor in detail and the model suggested was very flexible and can be used in many applications. A comparison has also been included with previous existing papers.

In 2013, another paper was published in which a memcapacitor emulator was proposed. The emulator circuit was also be used in various basic circuits and the working was verified by using it in R-C frequency selection networks [11].

A. S. Elwakil wrote a paper in August 2013, regarding the double-loop hysteresis behavior of the memristor, also gave a detailed study about the hysteresis loop and mathematically proved the importance of the behavior [12]. Further, he also showed the working of the loop in the incremental/decremental memristor with the help of an emulator circuit.

Another paper was published in which the basic properties of memristors are highlighted. The three required parameters to be fulfilled were ; (1) The circuit must exhibit the " Pinched hysteresis loop" ,(2) The loop should shrink as the frequency is increased and (3) The loop should shrink to a single value when frequency tends to infinity and thereafter the circuit acts as resistance[13]. The author has given a full explanation of the set parameters and how the different frequency affect the hysteresis loop.

In 2013, Ahmed I. Hussein wrote a paper in which an emulator circuit was realized with current-controlled circuit. This was the first paper in which memristor emulator was made by using CCII. After this, numerous papers were published in which CCII was used to realize the memristor

emulator. In this paper, the memristor emulator was also used in an oscillator circuit to verify the application. All the results obtained by simulation were well agreed with mathematical concept [14].

In May 2014, C. Sanchez-Lopez gave a brief introduction about a floating memristor emulator with the use of the CCII. In this paper a floating memristor emulator was realized and described the various applications in which it can be used like sensor, analog circuits, neural networks [15]. The paper also covers the various frequencies in which the memristor emulator can work.

Another paper was published in May 2014, in which a floating flux-controlled meminductor emulator was designed. In this design, the meminductor was realized directly and, it was not converted from a memristor. Since it is a floating device, it has a wide application and can be used in any circuitry [16].

A new memristor emulator was designed using DDCC (differential difference current conveyor). In this paper, the authors have designed a grounded memristor emulator using passive elements like resistor and capacitors [17]. In these arrangements, a multiplier is also required which makes the circuitry more complex and bulkier.

In 2014, Muhammad Taher Abuel maatti wrote a paper in which they realized memristor emulator using a current-feedback operational amplifier and passive elements like resistance. The device can only provide a binary memristance level [18].

In 2014, another paper was published in which CCII to make a memristor emulator circuit. The working of a memristor was verified by both mathematically as well as by simulation results. Further, the circuit was used in the design of relaxation oscillator [19].

In 2014, a meminductor emulator was introduced by the use of off the self-realization. The model was verified mathematically first and then it was simulated to verify the same [20].

There has been a good effort to use the memristor in digital signal processing (DSP) circuits. The applications mainly focus on the realization of better memories and realizing the neural networks. The block used was CFOA and various passive elements were also used [21]. Further, they have shown various applications in which the circuit can be used such as ASK, FSK, and BPSK.

In September 2014, Leon Chua published a paper in which a detailed information about the working of a memristor was given and also described how it can be judged whether the circuit is a memristor or not. He gave all the possible graphs of memristor [22].

In May 2015, another emulator memristor circuit was designed in which second generation of CCII with double output was used. In this circuit, one analog multiplier, one capacitor and two resistors are also used [23]. This circuit was first checked and it showed not only the frequency-dependent hysteresis graph but also the current versus voltage graph which hold up to 16KHz. Various graphs were shown with different frequency of operation.

In 2015, Abdullah G. Alharbi, Zainulabideen J. Khalifa published a paper with the use of two CCII, and forming a memristor emulator circuit. All the fingerprints of a memristor has been verified by this circuit and the circuit was also been made by available ICs to show the same results [24].

In June 2015, a paper was published in which two memristors were placed in different arrangements and their properties was noticed [25]. In the paper, the memristor were placed in series and parallel and their behavior has been verified. The series and parallel arrangements of memristor have also been verified experimentally.

Muhammad Taher Abuelma, Zainulabideed Jamal Khalifa wrote a paper in October 2015, they realized a floating memristor emulator using a current-feedback operational amplifier. In this paper, an analog multiplier was not used and therefore, the complexity of the circuit as compared to other reported work. They have also utilized the circuit in communication applications like FM-to-AM converter [26].

In 2015, another memristor emulator was realized by using an OTA and electronically tunable CCII. The arrangement was done such that it imitated the behavior HP model of memristor [27]. The circuit was simulated and the results were also verified by making it on a breadboard.

In 2016, Rajeev Kumar Ranjan gave another realization of memristor emulator namely current conveyor transconductance amplifier (CCTA) from which memristor emulator was realized. It could be used as floating and grounded memristor emulator by the use of the same circuit. No sub circuits were used like multiplier, ADC or DAC [28]. This circuit was implemented on a breadboard with the use of various ICs and the simulation results were compared with the experimental results. Various applications were implemented by the use of this circuit like amplitude modulation, frequency modulation and demodulation.

Another paper was published in the same year in which two emulator circuits were realized by using an OTA and was utilized in neuron circuit [29]. This circuit generate spiking and bursting firing. Behavior of the firing can only be varied by changing the external biasing voltage. The spiking can be observed at various time period and different results can be verified.

Another paper related to the spiking behavior was published in the same year but this circuit does not require any extra circuit like the analog multiplier. Therefore, the circuitry becomes compact, the paper gave a detailed information of the Spike Timing-Dependent Plasticity (STDP) [30].

In 2016, a paper was published in which a grounded memristor emulator was designed by using the second-generation current conveyor, a four-quadrant multiplier, a capacitor and a resistor. Incremental and decremental memristor can be constructed from this grounded memristor emulator design. This circuit operates from 16Hz to 860KHz. The circuit provides a wide range of frequency variation. The circuit was also realized by available ICs [31].

In 2016, Abdullah G. Alharbi, Zainulabideen J. Khalifa gave another memristor emulator circuit with the use of CCII+ and an exponential amplifier. The paper provided mathematical analysis for the proposed circuit. Simulation results were also verified [32]. This circuit was simple as compared to other memristor emulator. This circuit can be used in various applications like relaxation oscillators and filters.

Another paper related to memristor emulator design was realized by using two CCII and one analog multiplier. It is a voltage-controlled memristor model. This design is experimentally verified by using various IC and the results are observed in CRO [33].

In 2016, Yunus Babacan, Fırat Kacar published a paper in which the MOS are operating in sub threshold region which provide high memristive value. The design consists one OTA, two MOSs and one capacitor. The simulation results show the pinched hysteresis loop. Same configuration is verified in series and parallel combination [34].

Another paper in the same year published by Van Ha Nguyen. Keun Yong Sohn, Hanjung Song gave information about the working of the HP model consisting the titanium oxide. The internal working between the layers was explained in detail [35]. The flux-controlled memristor model was also explained and verified mathematically. They have also made a simple model for memristor emulator using basic analog circuits. The circuit was made on the PCB and the experimental results were compared with the simulation results.

In 2016, another emulator circuit was designed in which four CCII and three OTA were used to form a memristor emulator. This was bulky and complex as compared to previous realization of memristor emulators. Frequency analysis was done for the proposed circuit. The pinched hysteresis loop was verified experimentally by realizing circuit on a breadboard [36].

In 2017, Rajeev Kumar Ranjan, Nishtha Rani, Ratnadeep Pal, Sajal K. Paul, Gaurav Kanyal made memristor emulator by using a new analog block CCTA [37]. Both floating and grounded memristor was designed from the same circuit without any modification. Comparisons are done with the previous existing papers. This circuit was very simple as it uses only one active building block. The circuit was made by various ICs and the experimental results were compared with the simulation results.

Another paper was published in July 2017 in which the memristor emulator was designed by using Differential Voltage Current Conveyor Transconductance Amplifier (DVCCTA), three resistors and one capacitor. All the properties of DVCCTA are explained in the paper and the mathematical analysis of memristor emulator is also given. Both simulation and experimental results are compared for the memristor emulator [38].

In July 2017, Yunus Babacan design a memristor emulator by using OTA and an analog multiplier. The parameters of the memristor emulator could be changed by a small variation in the biasing current of the OTA [39]. Incremental and detrimental memristor can be made from the circuit with same block.

Umut Engin Ayten, Shahram Minaei, Mehmet Sagb as published a paper in August 2017, which they used anew active building block CBTA to make the memristor emulator. In this circuit an additional analog multiplier is required. This configuration only provides a grounded memristor [40].

In 2018, Fatih Gula, Yunus Babacanb, have realized memristor emulator by using OTA but by the use of semiconductor in this paper they have worked with the metal properties and created a film of 300nm of zinc oxide. Further, they have used to create the hysteresis loop [41].

Later in 2018, another paper was published by the use of OTA by Gaurav Kanyal, Pratik Kumar, Sajal K. Paul, Ashok Kumar Dept [42]. The emulator circuit was made by the use of two OTA. They realized both incremental and decremental memristor and also realized grounded as well as floating memristor emulator. The major difference as compared to the other reported work is that they have not used multiplier and therefore, reduced the area of the chip.

In February 2018, Abdullah Yesil published an article in which by the use of only seven MOSFETs the memristor emulator was realized and there by reduces the area of the chip significantly [43]. This paper only realizes grounded memristor emulator.

In March 2018, Predrag B. Petrovic, published an article in which VDTA was used with one multiplier, the whole circuit consists of 32 MOSFETs [44].

In October 2018, Abdullah Yesil, Yunus Babacan, and Firat Kacar, wrote another paper in which memristor emulator was realized by using VDTA and few capacitors [45].

In 2019, Leimin Wang, Tiandu Dong published a paper in which an memristor emulator circuit is realized to implement the MCSs [46]. Then, based on the presented emulator circuit, the model of the Memristor Chaotic system (MCSs) is provided and its finite-time synchronization problem was resolved by the use of this circuit.

In January 2019, Zhijun Li, Chengyi Zhou published a paper in which a memristor chaotic system was proposed by using universal memristor emulator into a state controlled cellular neural network (SC-CNN), in this configuration incremental and decremental memristor can be formed [47]. When the parameters of the system are varied, a series of symmetrical attractors are induced while interchanging the operating configurations used by the emulator in the system.

In February 2019, Herbert Ho-Ching Iu Simin Yu · Fang Yuan published a paper in which a memristor emulator and meminductor emulator circuit was realized. By, using the circuit a chaotic circuit was realized by using memristor, meminductor and capacitor all in parallel. Both the simulation and experimental results are compared [48].

In March 2019, Fatih Gul published a paper in which a memristor emulator circuit was realized without using any active building block. The circuit less complex and is compact in size due the use of less number of MOSFETs. Experimental results were compared with the simulation results [49].

In 2019, John Vista published a paper on a floating memristor emulator circuit in which the metal–oxide–semiconductor field-effect transistor count is minimized [50]. The proposed circuit uses only three NMOS transistor, a single capacitor and constant current source. It offers less design complexity over existing memristor emulator circuits.

CHAPTER 3

DESIGN AND ANALYSIS OF MEMRISTOR EMULATORS USING SYMMETRICAL OTA

3.1 INTRODUCTION

There are so many active building blocks which are widely being used in different applications of analog signal processing. Operational amplifier is the most dominating element among all these blocks but it also suffers from some drawbacks. Due to disadvantages offered by operational amplifier researchers and engineers always try to find out the alternate solutions. The disadvantages of op-amp are limited bandwidth and modest slew rate and it also requires much more passive elements to realize any circuit. In addition, it needs a strict matching between passive components. Operational transconductance amplifier (OTA) is often seen as one of the best alternatives of op-amp due to availability of electronic tunability, simpler in design, and requires less numbers of passive elements to realize intended circuits. It is being used in various applications such as comparator, inductance simulation circuits, analog filters, oscillators and amplifiers, etc. Due to versatile in nature, it is now being used in the design of memristor emulator circuits. In this chapter OTA is designed in view of using it in memristor emulator circuits of the subsequent chapters of the thesis. Figure 3.1 shows the structure of symmetrical OTA. MOSFETs M1 and M2 form the differential pair input. The differential pair is biased by the current I_B . Current mirrors are formed by M3-M, M6-M8, M9- M12.

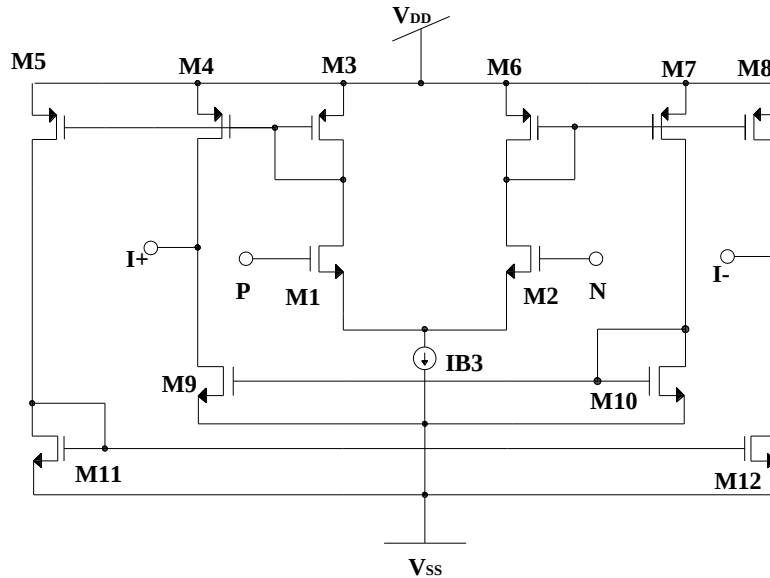


Figure 3.1 CMOS realization of symmetrical OTA

It is a four terminal device out of which two terminals P and N are input voltage terminals. Two current output terminals are I^+ and I^- which are same in amplitude but flows in opposite direction.

Two outputs are often beneficial while realizing different applications because of negative feedback can be formed either by shorting I+ with N terminal or I- with P terminal. The difference of two voltages V_p and V_n are applied to input terminals of OTA as given in equation (3.1) which are converted into two currents I_+ and I_- by transconductance (G_m) as shown by equation (3.2). The transconductance of OTA is varied by changing the bias current I_B as expressed in equation (3.3).

$$V_P - V_N = V_{in} \quad (3.1)$$

$$I_+ = g_m V_{in} \quad (3.2)$$

$$g_m = \sqrt{2\mu_n C_{ox} \frac{W}{L}} \sqrt{I_B} \quad (3.3)$$

Various applications also need voltage tunable OTA in which biasing current I_B is replaced by the structure of current mirror and biasing voltage V_B as shown in Figure 3.2.

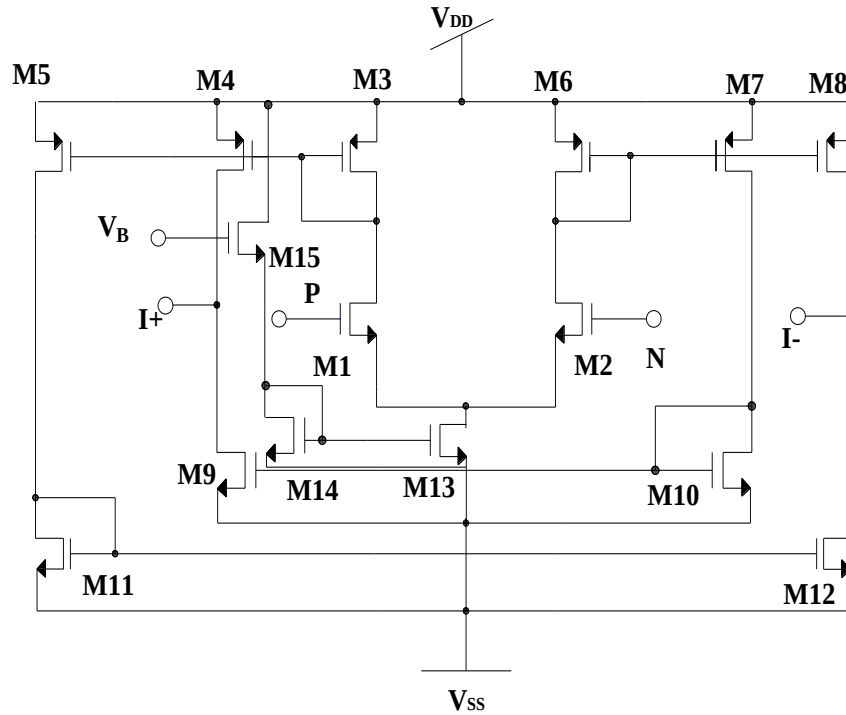


Figure 3.2 CMOS realization of symmetrical OTA with current mirror

The transconductance of voltage tunable OTA shown in figure 3.2 is controlled by varying biasing voltage V_B as given in equation (3.4). The other parameters of equation (3.4) are fixed as dependent on technology parameters as given by equation (3.5)

$$G_m = \frac{k}{\sqrt{2}} (V_B - V_{SS} - 2V_{th}) \quad (3.4)$$

where k is the parameter of MOS defined by

$$k = \mu_n C_{ox} \frac{W}{L} \quad (3.5)$$

The same arrangement of the Figure 3.2 will be utilized in the design of grounded and floating memristor emulators. Grounded and floating memristor emulator circuits are required in most of the applications in the area of analog signal processing. These circuits can also be changed into incremental and decremental memristor emulators after few modifications. In the subsequent section, small signal analysis of OTA is covered in order to provide a foundation for better understanding when it is used in the design of memristor emulator.

3.2 SMALL SIGNAL ANALYSIS OF SYMMETRICAL OTA

The small signal model of Figure 3.1 is shown in Figure 3.3. The value of V_{g4} is calculated from Figure 3.3 and is given in equation (3.6).

$$V_{g4} = -g_{m1} \frac{V_z}{2} \left(\frac{1}{g_{m13}} \parallel r_{01} \parallel r_{03} \right) \quad (3.6)$$

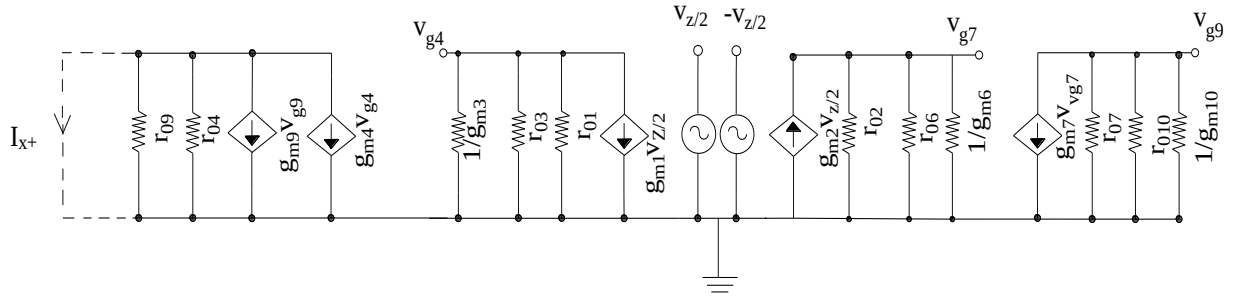


Figure 3.3 Small signal model of OTA

The value of $r_{01} \parallel r_{013}$ are very large when compared with $1/g_{m3}$ thus, the equation can be reduced to

$$V_{g4} = -\left(\frac{g_{m1}}{g_{m3}} \right) \left(\frac{V_z}{2} \right) \quad (3.7)$$

Similarly, the value of V_{g7} can be calculated and is given in equation (3.8)

$$V_{g7} = -g_{m4} \frac{V_z}{2} \left(\frac{1}{g_{m6}} \parallel r_{02} \parallel r_{06} \right) \quad (3.8)$$

The equation (3.8) can be reduced to equation (3.9) as the value of $r_{02} \parallel r_{06}$ are very large when compared with $1/g_{m6}$

$$V_{g7} = -\left(\frac{g_{m4}}{g_{m6}}\right)\left(\frac{V_z}{2}\right) \quad (3.9)$$

The value of v_{g9} can be obtained from Figure 3.3 and is given in equation (3.10).

$$V_{g9} = -g_{m7}V_{g7}\left(\frac{1}{g_{m10}} \parallel r_{07} \parallel r_{10}\right) \quad (3.10)$$

The value of $r_{07} \parallel r_{10}$ are very large as compared to $1/g_{m10}$ thus, the equation can be reduced to (3.11)

$$V_{g9} = -\left(\frac{g_{m7}}{g_{m10}}\right)V_{g7} \quad (3.11)$$

After putting the value of V_{g7} from equation (3.9) into the equation (3.12), we get

$$V_{g9} = -\left(\frac{g_{m7}}{g_{m10}}\right)\left(\frac{g_{m2}}{g_{m6}}\right)\left(\frac{V_z}{2}\right) \quad (3.12)$$

Since the aspect ratios of M1 and M2 are same. Therefore, the equation (3.12) is reduced to equation (3.13) as their transconductance are same i.e $g_{m6} = g_{m7}$

$$V_{g9} = -\left(\frac{g_{m2}}{g_{m10}}\right)\left(\frac{V_z}{2}\right) \quad (3.13)$$

The current I_{X+} is obtained by equation (3.14)

$$I_{X+} = -g_{m4}V_{g4} - g_{m9}V_{g9} \quad (3.14)$$

Substituting the values of V_{g4} and V_{g9} from equations (3.7) and (3.12) into equation (3.14) results in (3.15)

$$I_{X+} = \left(\frac{g_{m1} + g_{m2}}{2}\right)V_z \quad (3.15)$$

Since MOSFETs M1 , M2 are differential pair MOSFETs and are identical in size therefore, equation (3.15) is reduced to equation (3.3).

3.3 RESULTS AND DISSCUSIONS

The circuit of OTA is designed and simulated by Mentor graphics ELDO simulation tool by using 0.18 μ m technology parameters. The bias voltages V_{DD} and $-V_{SS}$ are 0.9 V. The value of bias current I_B is 100 μ A. The aspect ratios of MOSFETs are shown in Table 3.1.

Table 3.1. Aspect ratios of MOSFETs

MOSFETS	W(μ m)	L(μ m)
M1, M2	16	1
M3-M8	6	1
M9-M12	4	1

The Figure 3.4 shows the DC analysis of OTA which gives linear range of -200mV to 200mV. Figure 3.5 depicts the AC analysis of the OTA, in which the bandwidth is found to be 406MHz. Infigure 3.6 gives the variation of transconductance for different biasing current I_B . The value of transconductance is 0.91mA/V for the bias current of 300 μ A. Figure 3.7 shows the transient analysis of OTA and it can be observed that the amplitude of output swing is $\pm 50\mu$ A.

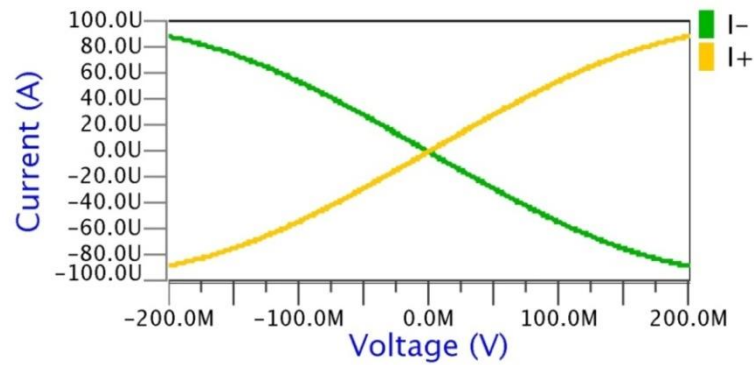


Figure 3.4. DC Analysis of OTA with linear range of ± 200 mV

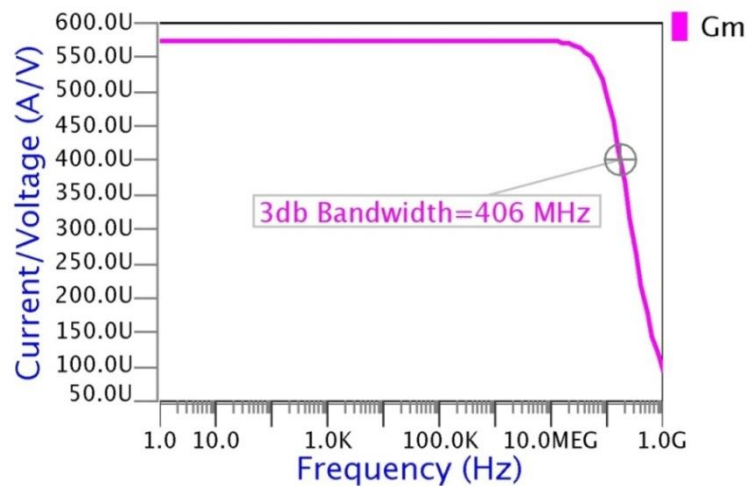


Figure 3.5 AC analysis of OTA with I_B of 100uA

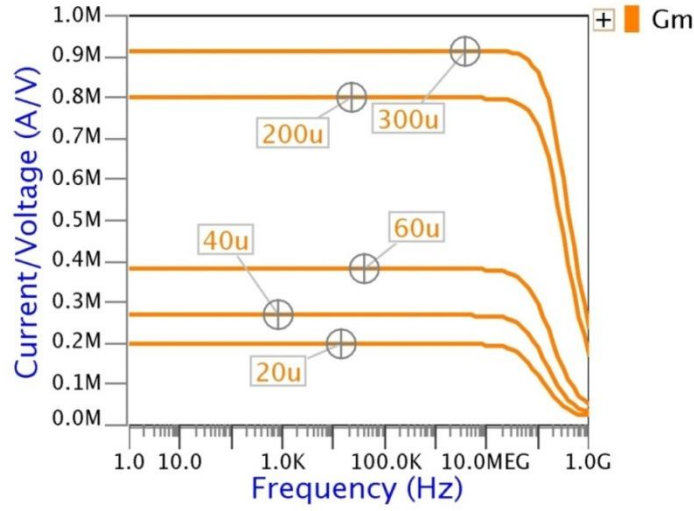


Figure 3.6 Change in transconductance for different biasing currents

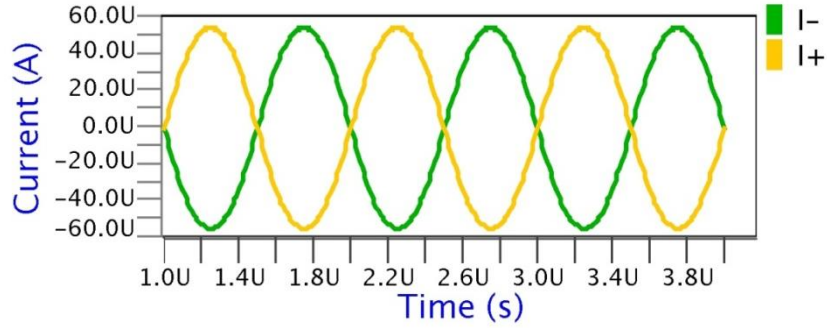


Figure 3.7 Transient analysis of symmetrical OTA

3.4 GROUNDED MEMRISTOR EMULATOR CIRCUIT BY USING OTA

A memristor emulator can be designed by using the proposed OTA as shown in figure 3.2. The grounded memristor emulator circuit can be designed from the proposed circuit as shown in figure 3.8. This configuration is used as a test circuit for all proposed OTA circuits in the subsequent chapters. Incremental and decremental memristor circuits can be formed by switching the configurations between w, x, y and z. For a grounded memristor emulator circuit only single output OTA is required. P and N are the voltage input terminals. Capacitor is the only passive element required for these circuits [42].

The values of input current (I_{in}) and capacitor current (I_c) can be seen from the figure (3.8) and is given in equation (3.16) and (3.17)

$$I_{in}(t) = -I_{o2+} = +G_{m2}V_{in}(t) \quad (3.16)$$

$$I_c(t) = I_{o1+} = +G_{m1}V_{in} \quad (3.17)$$

Biasing voltage (V_{B2}), is given in equation (3.18)

$$V_{B2} = \frac{1}{C} \int I_C(t) dt = \frac{G_{m1}}{C} \int V_{in}(t) dt = \frac{G_{m1} \phi_{in}}{C} \quad (3.18)$$

where the value of flux can be calculated from equation (3.19)

$$\phi_{in} = \int V_{in}(t) dt \quad (3.19)$$

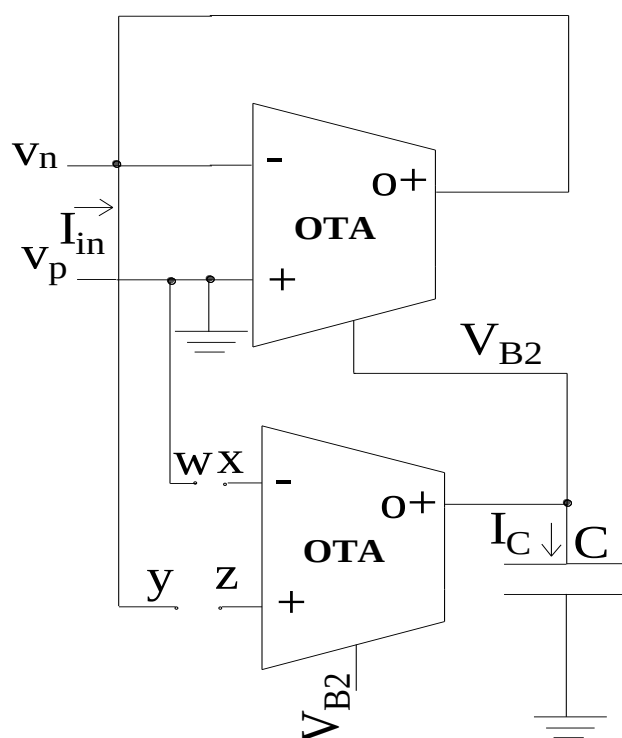


Figure 3.8. Schematic diagram of grounded memristor emulator [42]

Substituting the value of V_{B2} from equation (3.18) into Eq. (3.4), the value of transconductance results in equation (3.20)

$$G_{m2} = \frac{k}{\sqrt{2}}(V_{B2} - V_{SS} - 2V_{th}) = \frac{k}{\sqrt{2}}\left(\frac{G_{m1}\phi_{in}}{C} - V_{SS} - 2V_{th}\right) \quad (3.20)$$

Combining the equations (3.16) and (3.20) we get the input current which is expressed in equation (3.21)

$$I_{in} = \frac{k}{\sqrt{2}} \left(\frac{G_{m1} \phi_{in}}{C} - V_{SS} - 2V_{th} \right) V_{in} \quad (3.21)$$

Substituting the equation (3.18) into equation (3.21) it results in equation (3.22)

$$W(\phi) = \frac{I_{in}}{V_{in}} - \frac{k}{\sqrt{2}}(V_{SS} + 2V_{th}) - \frac{k}{\sqrt{2}} \frac{G_{m1}}{C} \phi_{in} \quad (3.22)$$

It can be concluded that the first part of the equation (3.29) is constant and the second part is a variable, it changes to form an incremental and decremental memristor emulator. Therefore, the working figure 3.8 is justified.

3.5 FLOATING MEMRISTORS EMULATOR CIRCUIT BY USING OTA

The floating memristor emulator circuit can be designed by using the proposed circuit of the OTA in Figure 3.2. An incremental and decremental memristor circuits can be formed by switching the configurations between w, x, y and z. The floating memristor emulator circuit requires one single output OTA and one dual output OTA as shown in figure 3.9. P and N are the voltage input terminals. The difference in the input voltages is applied to the circuit as given in equation (3.24).

The I_a , I_b , I_C of the floating memristor emulator is given in equation (3.23)

$$I_a = I_b = I_{in} \quad (3.23)$$

The current in capacitor I_C can be expressed as given in equation (3.24)

$$I_C = I_{01+} = -G_{m1} V_{in} \quad (3.24)$$

The input voltage can be calculated from equation (3.25)

$$V_{in}(t) = V_A(t) - V_B(t) \quad (3.25)$$

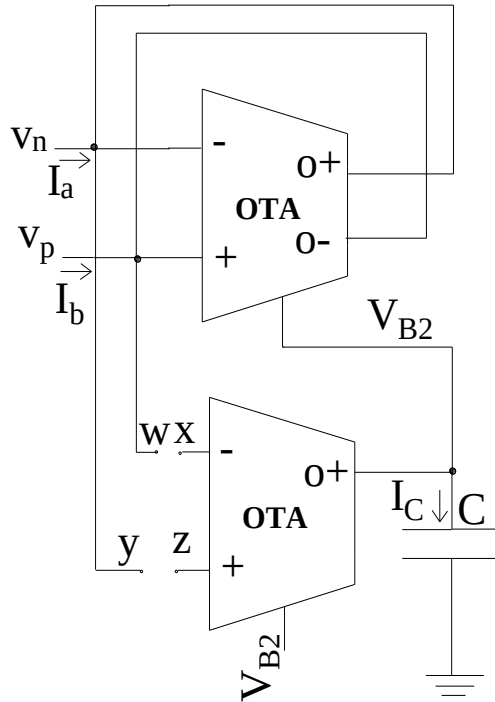


Figure 3.9. Schematic diagram of floating memristor emulator [42]

Biasing voltage (V_{B2}), is given by equation (3.26)

$$V_{B2} = \frac{1}{C} \int I_C(t) dt = \frac{G_{m1}}{C} \int V_{in}(t) dt = \frac{G_{m1} \phi_{in}}{C} \quad (3.26)$$

Substituting the value from the equation (3.26) into equation (3.4) the value of transconductance results in

$$G_{m2} = \frac{k}{\sqrt{2}} (V_{B2} - V_{SS} - 2V_{th}) = \frac{k}{\sqrt{2}} \left(\frac{G_{m1} \phi_{in}}{C} - V_{SS} - 2V_{th} \right) \quad (3.27)$$

For floating memristor emulator, the input current (I_{in}) is given as

$$I_{in} = \frac{k}{\sqrt{2}} (V_{B2} - V_{SS} - 2V_{th}) V_{in} \quad (3.28)$$

The equation (3.26) can be substituted in equation (3.28) which results in equation (3.29)

$$W(\phi) = \frac{I_{in}}{V_{in}} - \frac{k}{\sqrt{2}} (V_{SS} + 2V_{th}) + \frac{k}{\sqrt{2}} \frac{G_{m1}}{C} \phi_{in} \quad (3.29)$$

If sinusoidal input voltage of $V_m \sin \omega t$ is applied to grounded memristor emulator, the Φ_{in} results in

$$\phi_{in} = \frac{V_m}{\omega} \cos\left(\omega t - \frac{\pi}{2}\right) \quad (3.30)$$

Where V_m is the maximum amplitude of the voltage signal and ω is the frequency of applied signal in radian/sec.

$$W(\phi) = \frac{I_{in}}{V_{in}} - \frac{k}{\sqrt{2}} (V_{SS} + 2V_{th}) + \frac{k}{\sqrt{2}} \frac{G_{m1}}{C} \frac{V_m \cos\left(\omega t - \frac{\pi}{2}\right)}{\omega} \quad (3.31)$$

It can be concluded that the first part of the equation (3.31) is constant and the second part is a variable, it changes to form an incremental and decremental memristor emulator. The memconductance is dependent on the amplitude and frequency of the input sinusoidal signal. It also depends on the value of capacitor used in circuit. Therefore, the working of figure 3.9 is justified.

3.6 RESULTS AND DISSCUSIONS

The circuit of memristor emulator is designed and simulated by Mentor graphics ELDO simulation tool by using 0.18 μ m technology parameters. The bias voltages V_{DD} and $-V_{SS}$ are 0.9V. The value of bias voltage V_B is 600mV. The aspect ratios of MOSFETs are shown in Table 3.2

Table 3.2. Aspect ratio of MOSFETs

MOS	W (μ_m)	L (μ_m)
M1, M2	16	1
M3-M8	6	1
M9-M12	4	1
M13, M14	14	0.18
M15	15	0.18

The figure 3.10 shows the transient analysis of memristor emulator with input voltage of 100 mV at 1 MHz frequency. For the grounded memristor emulator circuit the figures 3.11-3.14 shows the current-voltage relationship which is the pinched hysteresis loop at different frequencies of 600KHz, 900KHz, 1MHz and 2MHz .It can be observed that the loop shrinks in size with the increase in frequencies and at higher frequency when both the loops coincide, it will behave as a linear resistor. For the floating memristor emulator, figures 3.15 and 3.16 show the characteristic of pinched hysteresis loop at frequencies 600KHz and 1MHz. The figure 3.17 shows the graph at different temperatures from -40°C to, it can be observed that with the increase in the temperature the loop size shrinks.

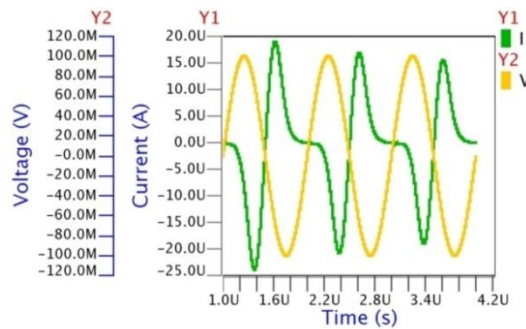


Figure 3.10. Transient analysis of memristor emulator

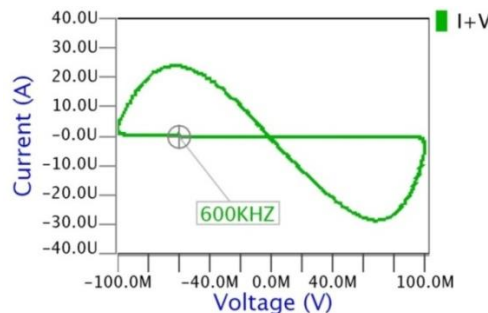


Figure 3.11. Hysteresis loop of grounded memristor emulator at 600KHz frequency

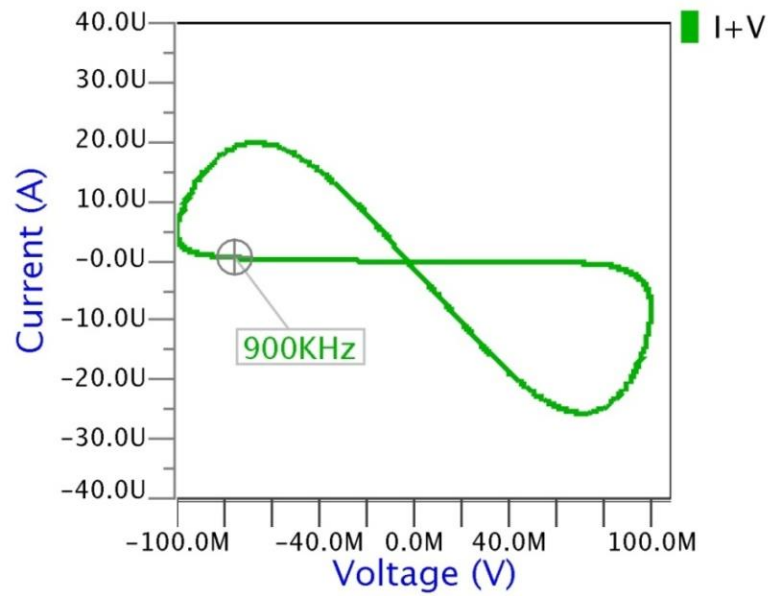


Figure 3.12. Hysteresis loop of grounded memristor emulator at 900KHz frequency

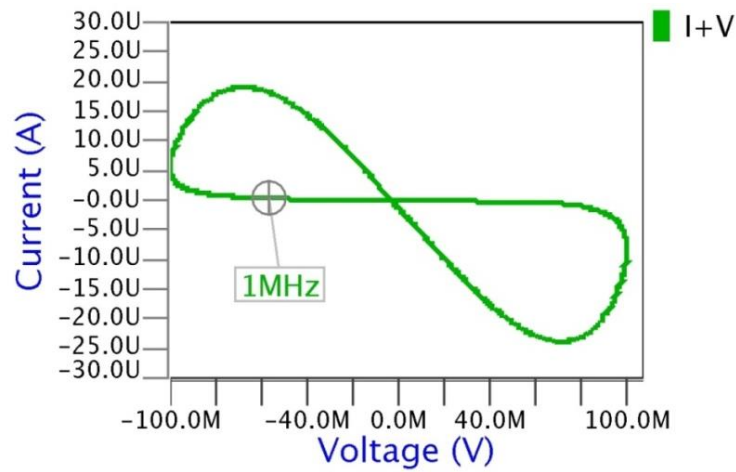


Figure 3.13. Hysteresis loop of grounded memristor emulator at 1MHz frequency

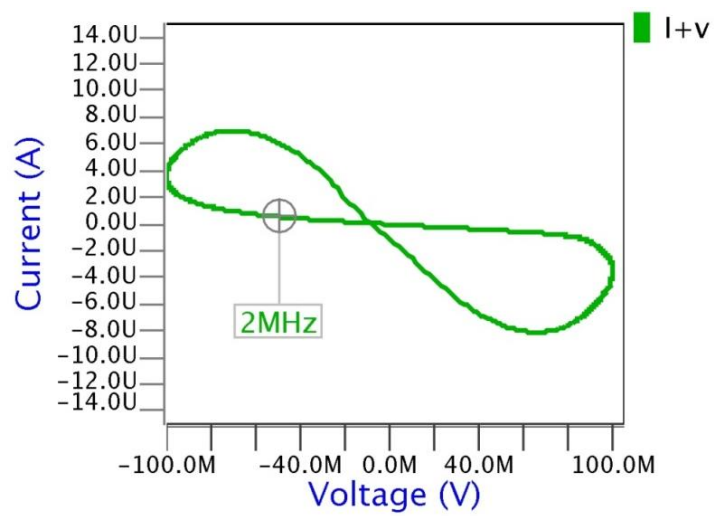


Figure 3.14. Hysteresis loop of grounded memristor emulator at 2MHz frequency

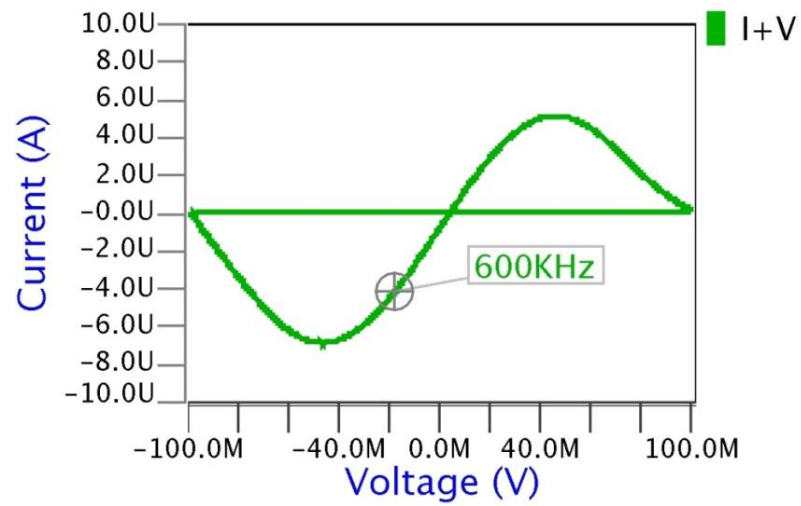


Figure 3.15. Hysteresis loop of floating memristor emulator at 600KHz frequency

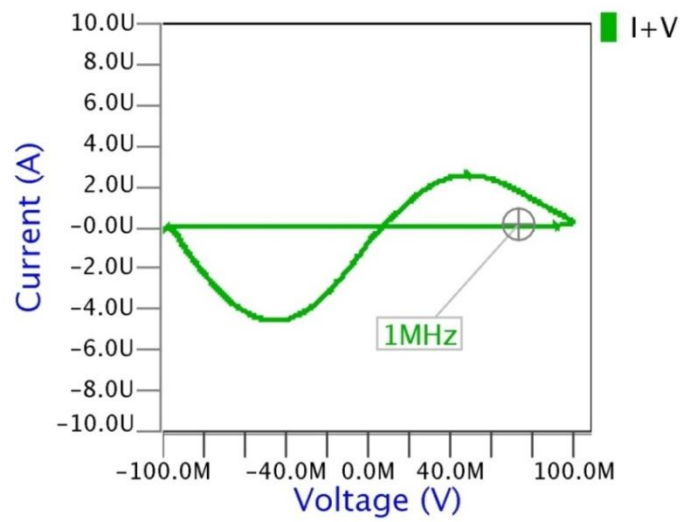


Figure 3.16. Hysteresis loop of floating memristor emulator at 1 MHz frequency

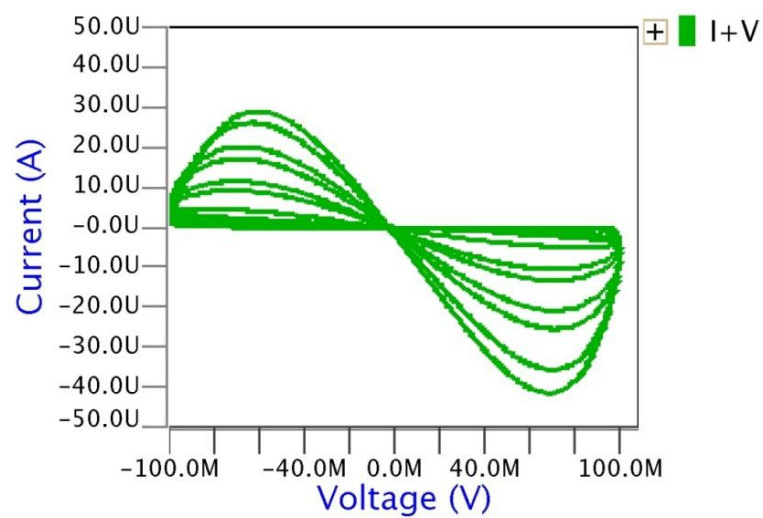


Figure 3.17. Hysteresis loop at different temperatures

3.7 CONCLUSION

It can be concluded, from the chapter that an existing OTA is implemented small signal analysis are explained in detail giving a better understanding of the circuit. Various analysis is performed on the circuit for understanding the parameters of the circuit. The linear range of OTA observed is $\pm 100\text{mV}$. Gain achieved is $580\mu\text{A/V}$. Transient analysis of OTA shows the symmetrical nature of the circuit. Working of floating and grounded memristor are explained in detail and is verified by mathematical analysis. Memristor emulators are implemented by using OTA. Grounded memristor emulator works for range from 600KHz-2MHz frequency and floating memristor emulator works for 600KHz and 1MHz. Pinched hysteresis loop is observed for different temperatures.

DESIGN AND ANALYSIS OF MEMRISTOR EMULATORS USING SYMMETRICAL OTAWITH SOURCE DEGENERATION RESISTANCE

This chapter, presents a source degenerated OTA in which degeneration resistance R_1 and R_2 are connected at the source terminals of the differential pair MOSFETs M_1 and M_2 as shown in figure 4.1. The current source is replaced by a current mirror formed by MOSFETs M_{13} to M_{15} . MOSFET M_{15} has a tunable voltage V_B , which is required for memristor emulator circuits. Source degeneration provides a wider range of linearity. There is a trade-off between transconductance (g_m) gain, linearity and power dissipation of the circuit by using this technique. If the value of resistance is kept high, the transconductance will decrease. The P and N are inputs of the differential pair MOSFET M_1 and M_2 . Since, the differential pair MOSFETs M_1 and M_2 are symmetrical, the transconductance of both the MOSFETs will be same ($g_{m1} = g_{m2}$). MOSFETs M_3 to M_5 and M_6 to M_8 form the current mirrors. Currents I_+ and I_- obtained at X_+ and X_- terminals of the symmetrical OTA are same in magnitude but opposite in phases. These opposite outputs are helpful in the design of different applications.



4.2 SMALL SIGNAL ANALYSIS OF OTA WITH SOURCE DEGENERATION

RESISTANCE

Figure 4.2 shows the small signal model of figure 4.1. The equations formed by applying KCL on node V_x are

$$\frac{g_{m1}V_z}{2} - \frac{V_x}{2} + \frac{V_{g4} - V_x}{r_{o1}} = 0 \quad (4.1)$$

$$V_x = -V_{g4}g_{m3}R \quad (4.2)$$

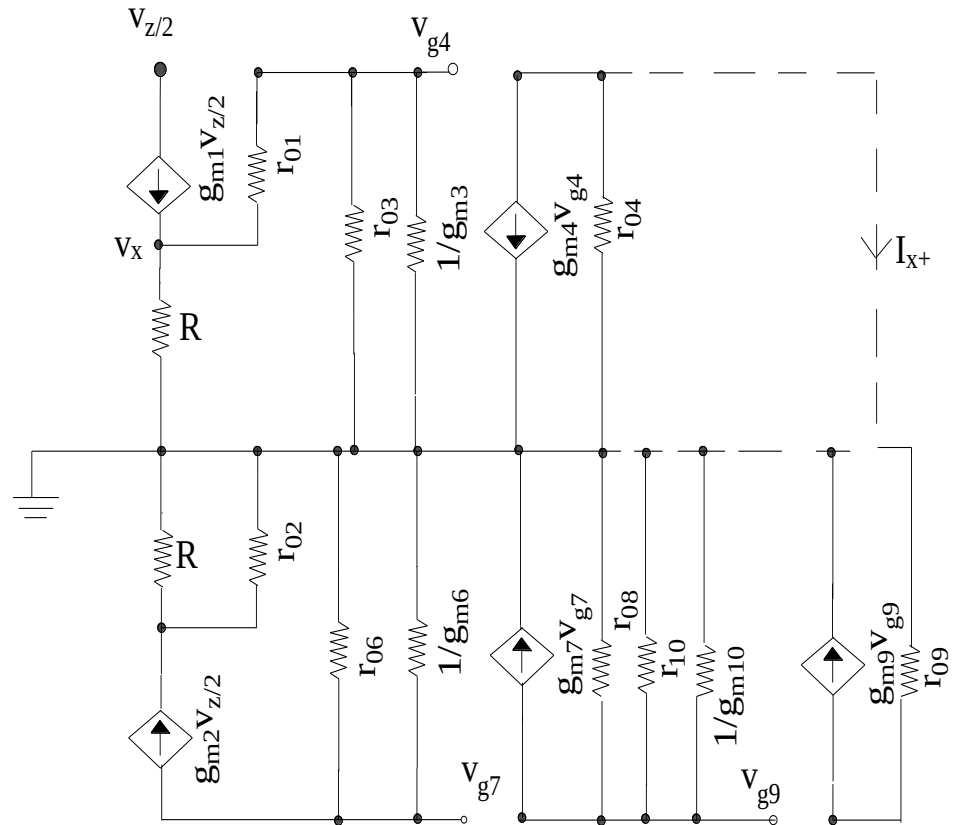


Figure 4.2. Small signal model of OTA with resistance

Substituting the equation (4.2) into equation (4.1), the value of V_{g4} is obtained in equation (4.3)

$$V_{g4} = - \left(\frac{\frac{g_{m1}V_z}{2}}{g_{m3} + \frac{1}{r_{o1}}(1 + g_{m3}R)} \right) \quad (4.3)$$

From Figure 4.2, it can be observed that V_{g4} and V_{g7} are symmetrical. Therefore, the value of V_{g7} is given in equation (4.4)

$$V_{g7} = \left(\frac{\frac{g_{m2}V_z}{2}}{g_{m6} + \frac{1}{r_{o2}}(1 + g_{m6}R)} \right) \quad (4.4)$$

The value of V_{g9} can be obtained from equation (4.5)

$$V_{g9} = - \left[\frac{g_{m7}V_{g7}}{g_{m10}} \left(\frac{\frac{g_{m2}V_z}{2}}{g_{m6} + \frac{1}{r_{o2}}(1 + g_{m6}R)} \right) \right] \quad (4.5)$$

The output current can be expressed in equation (4.6)

$$I_+ = -g_{m4}V_{g4} - g_{m9}V_{g9} \quad (4.6)$$

Substituting the equation (4.3) and (4.5) into equation (4.6)

$$I_+ = \frac{g_m V_z}{g_{m6} + \frac{1}{r_{o2}}(1 + g_{m6}R)} \quad (4.7)$$

Simplifying the equation (4.7) as the value of $1/r_{o2}$ is very small when compared to $g_{m6}R$

$$I_+ = \left[\frac{g_m V_z}{g_{m6} \left(1 + \frac{R}{r_{o2}} \right)} \right] \quad (4.8)$$

Therefore, it can be concluded that the linear range can be increased by choosing the appropriate value of resistance R .

4.3 RESULTS AND DISSCUSSIONS

The circuit of symmetrical OTA with resistance is designed and simulated by Mentor graphics ELDO simulation tool by using 0.18 μ m technology parameters. The bias voltages V_{DD} and $-V_{SS}$ are 0.9 V. The value of bias voltage V_B is 600mV. The values of R_1 and R_2 are 5k Ω . The aspect ratios of MOSFETs are shown in Table 4.1.

Table 4.1 Aspect ratios of MOSFETs

MOS	$W(\mu_m)$	$L(\mu_m)$
M1, M2	16	1
M3-M8	6	1
M9-M12	4	1
M13, M14	14	0.18
M15	15	0.18

The figure 4.3 shows the DC analysis of symmetrical OTA with source degeneration. The linear range of -500mV to 500mV. Figure 4.4 gives the AC analysis of the OTA, and the observed bandwidth is 175MHz. Figure 4.5 shows the time response of the OTA and the swing is observed to be $\pm 6u$.

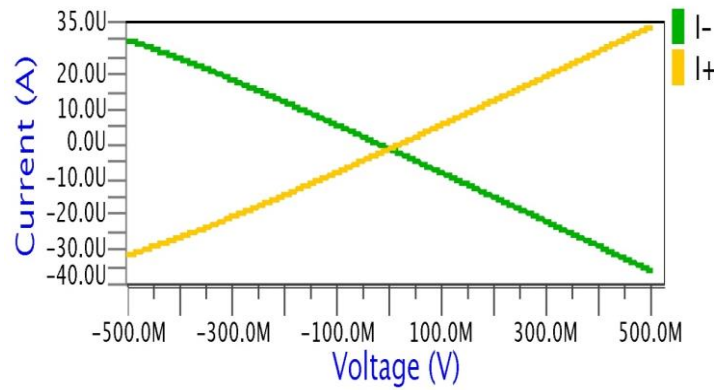


Figure 4.3. DC analysis of OTA with linear range of $\pm 500mV$

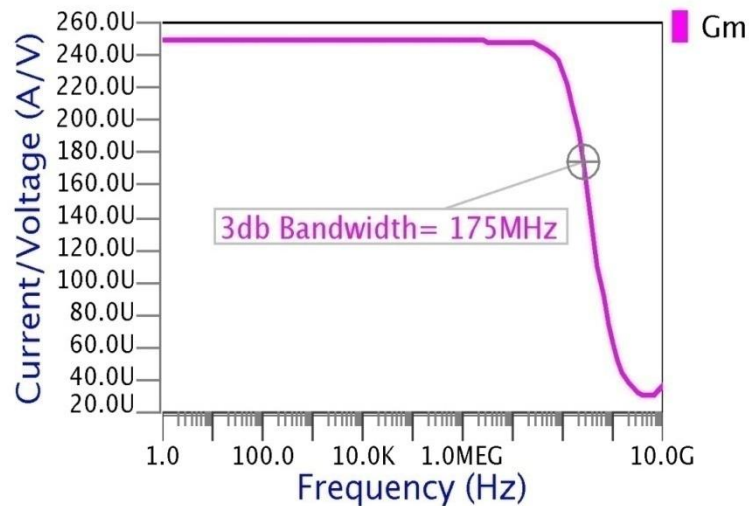


Figure 4.4. AC analysis of OTA with source degeneration resistance

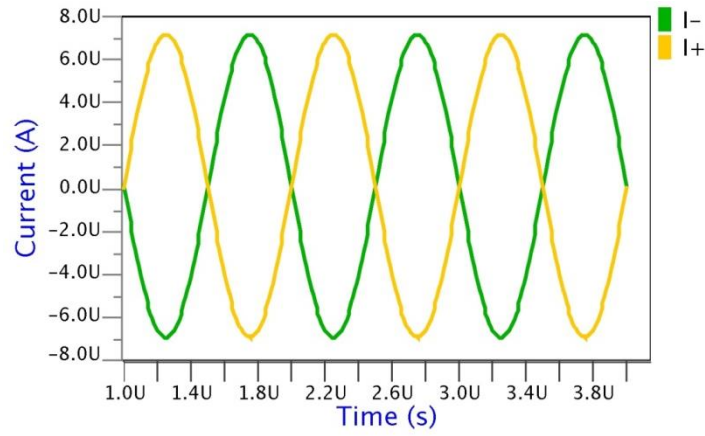


Figure 4.5. Transient analysis of OTA with source degeneration resistance

The figure 4.6 shows the transient analysis of memristor emulator given in Figure 3.9 and designed by using source degenerated OTA at the input voltage of 500mV with 1MHz frequency. The figures 4.7-4.10 shows the characteristics of pinched hysteresis loop for a grounded memristor emulator circuit at different frequencies of 600KHz, 900 KHz, 1MHz and 2 MHz. It can be observed that with the increase in frequency the loop size shrinks and at higher frequency the circuit behave as a linear resistor. The figures 4.11-4.14 shows the pinched hysteresis loop for floating memristor emulator at frequencies 600KHz, 900KHz, 1MHz and 2MHz. The figure 4.15. shows the pinched hysteresis loop at different temperatures from -40°C to 100°C it can be observed, that with the increase in temperature the loop size shrinks and becomes smaller.

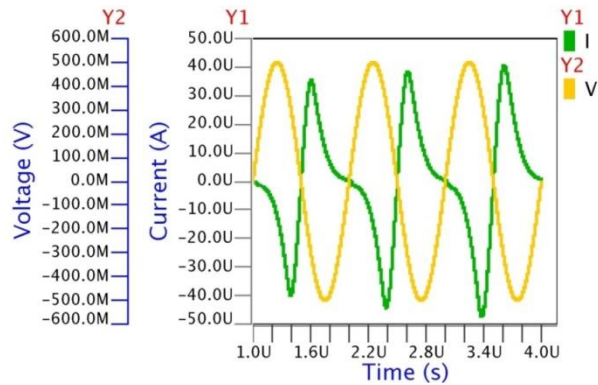


Figure 4.6. Transient analysis of memristor emulator

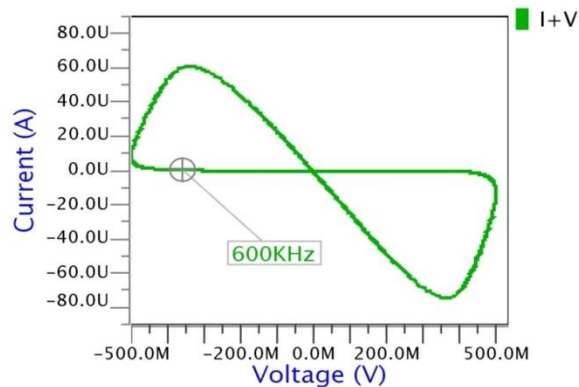


Figure 4.7. Hysteresis loop for grounded memristor at 600KHz frequency

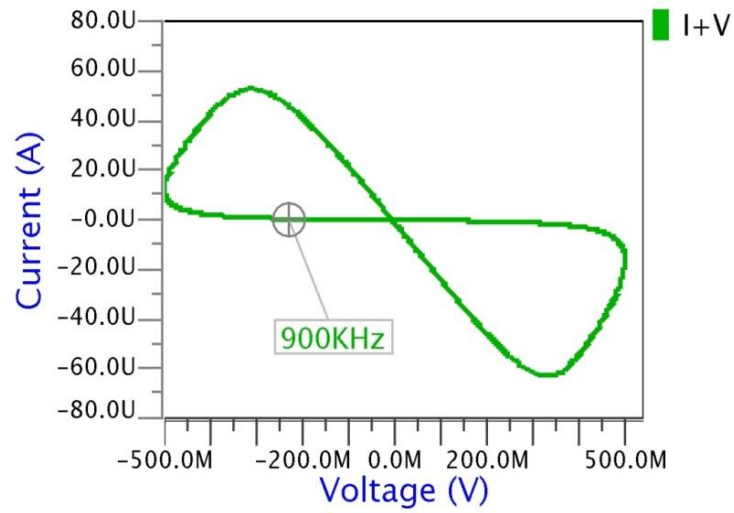


Figure 4.8. Hysteresis loop for grounded memristor at 900KHz frequency

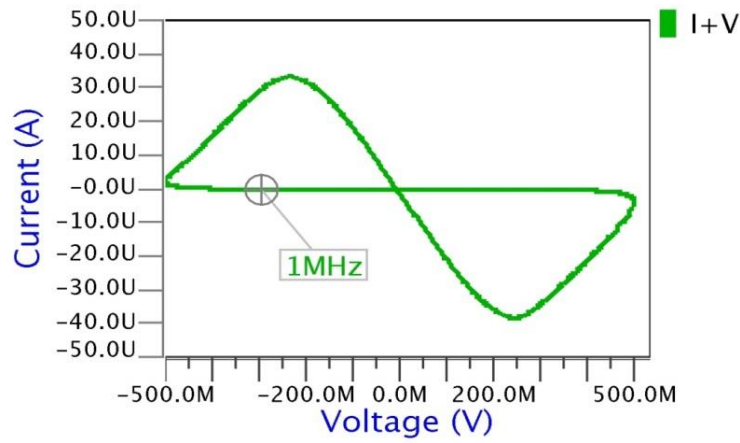


Figure 4.9. Hysteresis loop for grounded memristor at 1MHz frequency

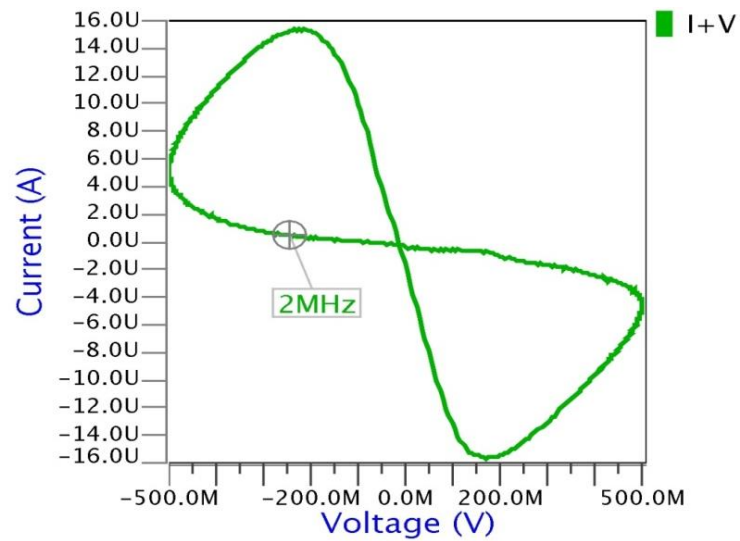


Figure 4.10. Hysteresis loop for grounded memristor at 600KHz frequency

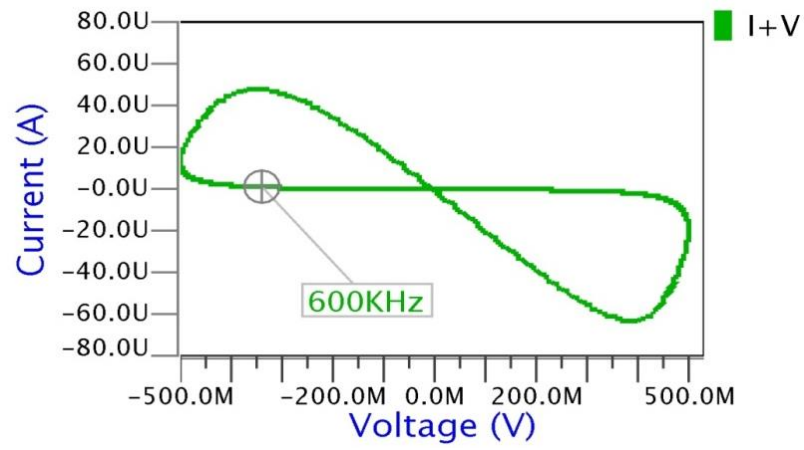


Figure 4.11. Hysteresis loop for floating memristor at 600KHz frequency

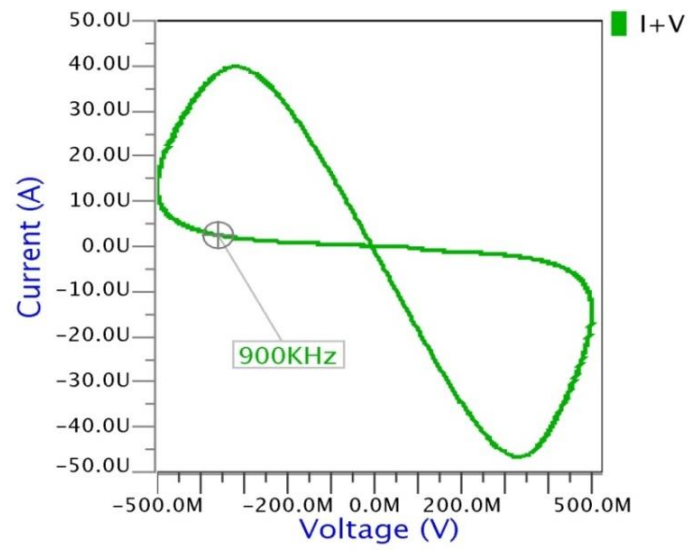


Figure 4.12. Hysteresis loop for floating memristor at 900KHz frequency

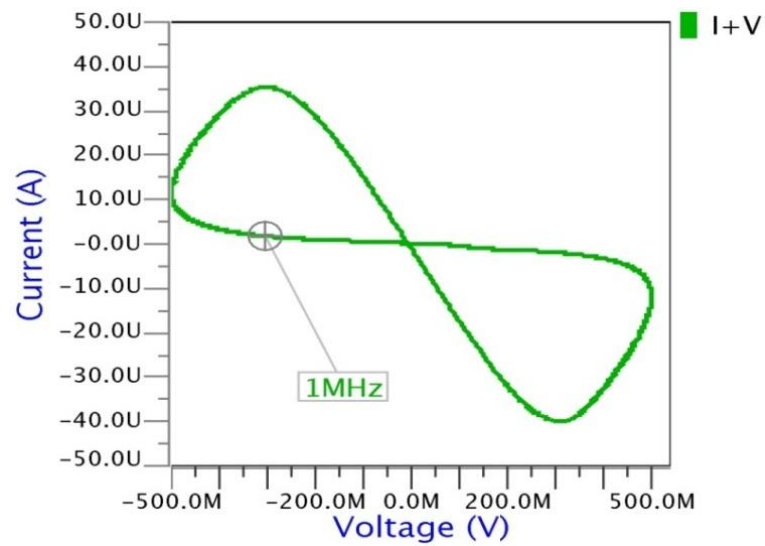


Figure 4.13. Hysteresis loop for floating memristor at 1MHz frequency

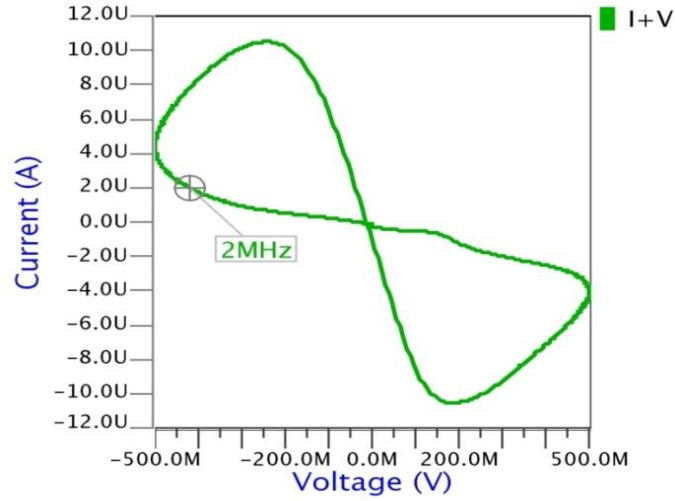


Figure 4.14. Hysteresis loop for floating memristor at 2MHz frequency

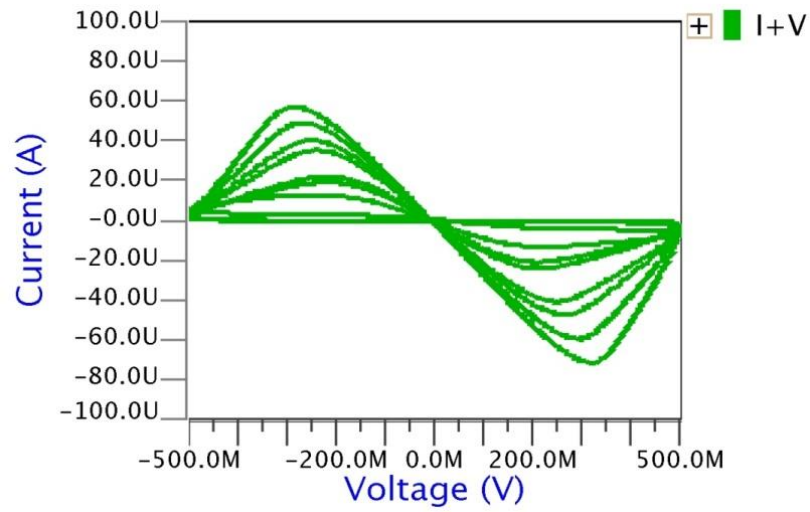


Figure 4.15. Hysteresis loop at different temperature

4.4 CONCLUSION

In this chapter, a symmetrical OTA with source degenerated resistance is implemented. Small signal analysis is presented for the better understanding of the circuit. OTA analysis results show that the linear range is extended up to $\pm 500\text{mV}$ and the transient analysis shows that the circuit is symmetrical. Gain received in this case is $250\mu\text{A/V}$. By using this technique, the linearity increases but the transconductance decreases. Pinched hysteresis loop for memristor emulators are observed with a linear range of $\pm 500\text{mV}$ which is more than the existing OTA. Both floating and grounded memristor emulator works for the frequencies range of 600KHz to 2MHz .

CHAPTER 5

DESIGN AND ANALYSIS OF MEMRISTOR EMULATORS USING SYMMETRICAL OTA WITH SOURCE DEGENERATION FORMED BY MOSFETs

5.1 INTRODUCTION

In this chapter, a source degeneration technique is used by using MOSFET M13 as a source degeneration resistor in the symmetrical OTA circuit as shown in Figure 5.1. The MOSFET M13 has a tunable voltage V_B , which is also required for the memristor emulator circuit. MOSFET M13 is added to the source of the differential pair MOSFETs M1 and M2. This technique provides a wider tunable range, and increases the linearity of the circuit. The number of MOSFETs used for source degeneration technique can be increased depending upon the applications for which it is to be used. These MOSFETs can be added in series as well as in parallel as shown in figure 5.2 Since the differential pair MOSFETs M1 and M2 are symmetrical, the transconductance of both the MOSFETs will be same ($g_{m1} = g_{m2}$). MOSFETs M3 to M5 and M6 to M8 constitute the current mirrors. Therefore, the received output from I- and I+ will be same but different in phase.

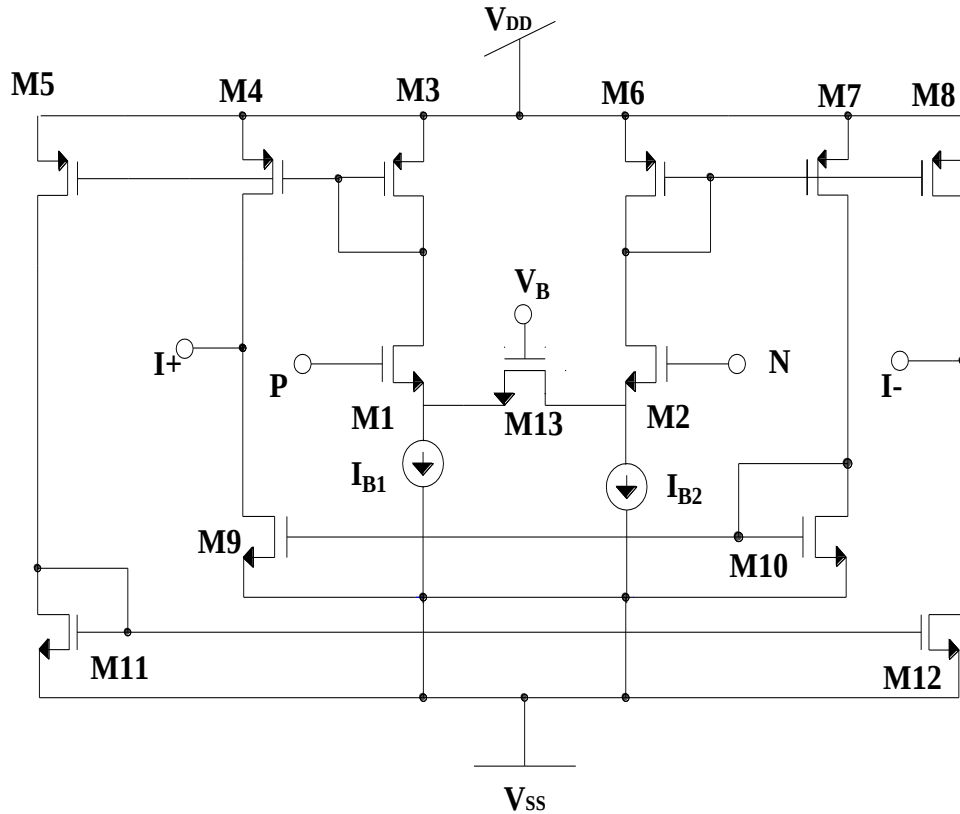


Figure 5.1 CMOS realization of OTA with source degeneration formed by MOSFETs

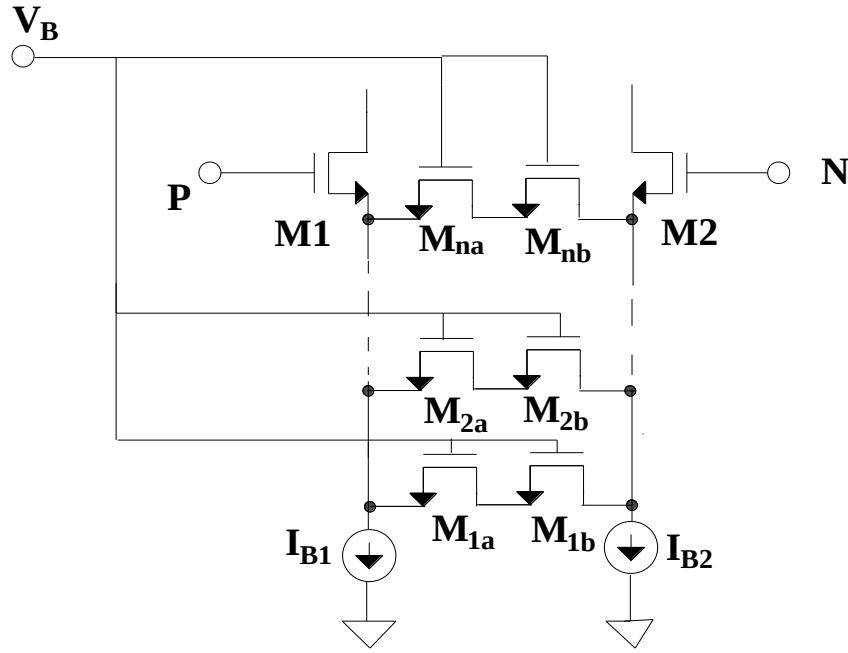


Figure 5.2 Parallel and series arrangement of source degenerated resistor

5.2 SMALL SIGNAL ANALYSIS OF OTA WITH SOURCE DEGENERATION FORMED BY MOSFETs

Figure 5.3 shows the small signal model for the figure 5.1. This small signal analysis is similar to the small signal of Figure 4.1 with a small change in which the resistors are replaced by the MOSFET M13.

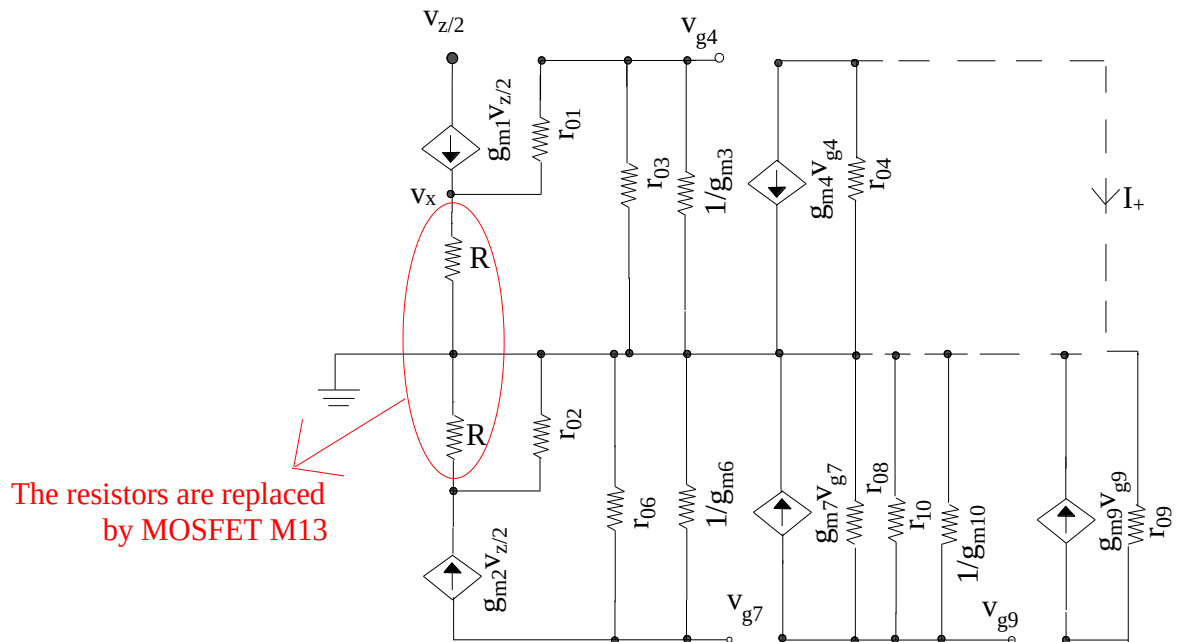


Figure 5.3 Small signal model of OTA with source degeneration formed by MOSFETs

All the calculations will remain same but the value of resistance will change and it can be expressed in equation (5.1)

$$R = \frac{1}{2\mu C_{ox} \frac{W_{13}}{L_{13}} V_{B35}} \quad (5.1)$$

The equation (5.1) can be substituted in equation (5.2) to result in equation of output current

$$I_{+} = \frac{g_m V_z}{g_{m6} \left(1 + \frac{\frac{1}{2\mu C_{ox} \frac{W_{13}}{L_{13}} V_{B35}}}{r_{02}} \right)} \quad (5.2)$$

It can be concluded that with the increase in resistance value the linear range of the OTA increases.

5.3 RESULTS AND DISSCUSIONS

The circuit of OTA with source degeneration is designed and simulated by Mentor Graphics ELDO simulation tool by using 0.18 μ m technology parameters. The bias voltages V_{DD} and $-V_{SS}$ are 0.9 V. The value of bias voltage V_B is 600mV. The biasing current I_{B1} and I_{B2} are 100 μ A. The aspect ratios of MOSFETs are shown in Table 5.1.

Table 5.1. Aspect ratios of MOSFETs

MOS	W (μ_m)	L (μ_m)
M1, M2	16	1
M9-M12	4	1
M13	20	1
M3-M8	6	1

The figure 5.4 shows the DC analysis of symmetrical OTA with source degeneration formed by MOSFETs with a linear range of -200mV to 200mV. Figure 5.5 gives the AC analysis of the OTA, and the observed bandwidth is 350MHz. Figure 5.6 gives the transient analysis where the output current swing is $\pm 80\mu$ A.

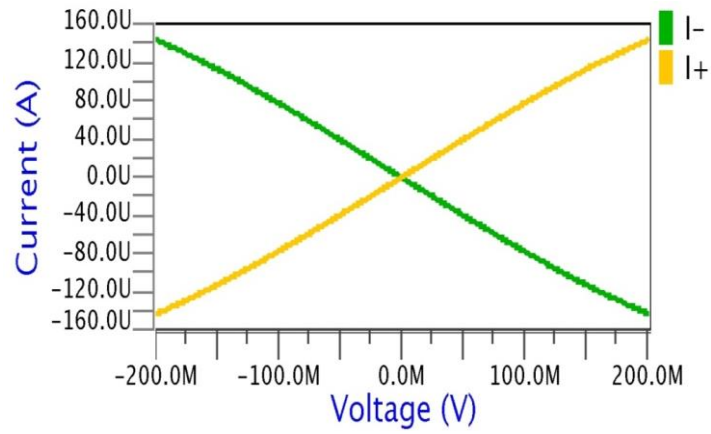


Figure 5.4. DC analysis of OTA with linear range of $\pm 200\text{mV}$

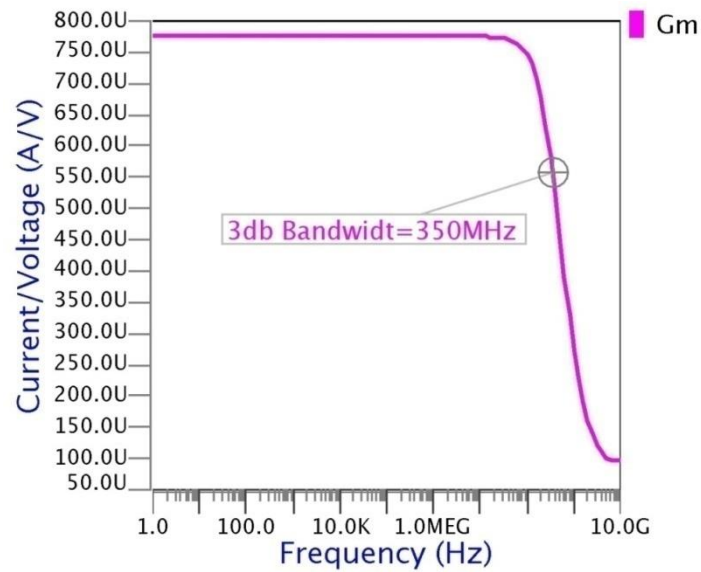


Figure 5.5. AC analysis of OTA with source degeneration where $I_{B1}=I_{B2}=100\mu\text{A}$

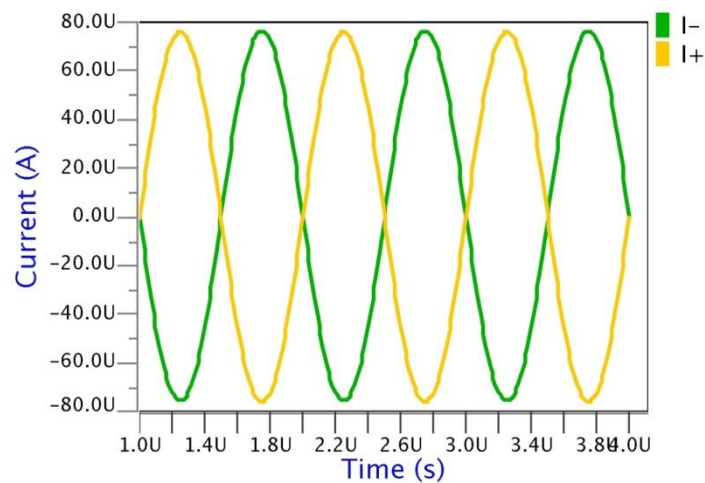


Figure 5.6. Transient analysis of OTA with source degeneration

The figure 5.7 shows the transient analysis when the input voltage of amplitude 200mV with 1MHz frequency is applied. The figures 5.8- 5.11 shows the characteristics of pinched hysteresis loop for a

grounded memristor emulator circuit at different frequencies of 600KHz, 900KHz, 1MHz and 2MHz. It can be observed that with the increase in frequency the loop size shrinks and at higher frequency the circuit behave as a linear resistor. The figures 5.12-5.15 shows the pinched hysteresis loop for floating memristor emulator at frequencies 600KHz, 900KHz, 1MHz and 2MHz. The figure 5.16. shows the pinched hysteresis loop at different temperatures from -40°C to 100°C it can be observed, that with the increase in temperature the loop size shrinks and becomes smaller.

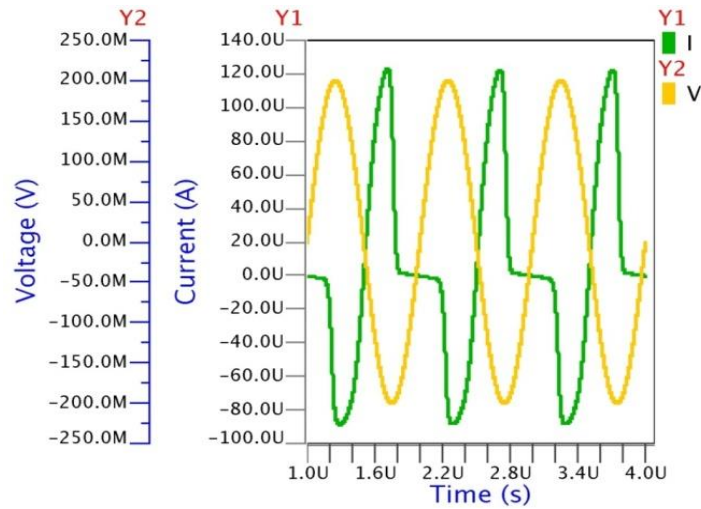


Figure 5.7. Transient analysis of memristor emulator

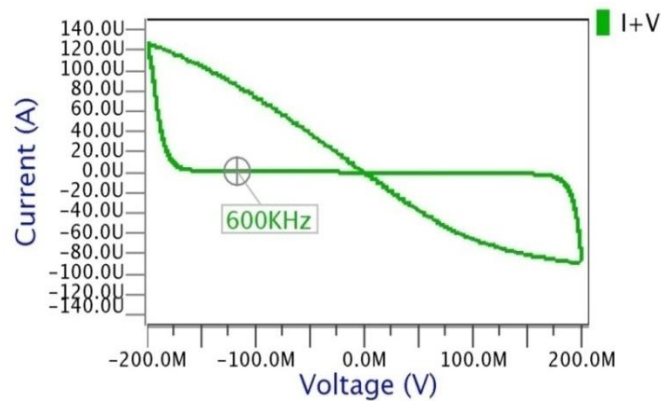


Figure 5.8. Hysteresis loop of grounded memristor emulator at 600KHz frequency

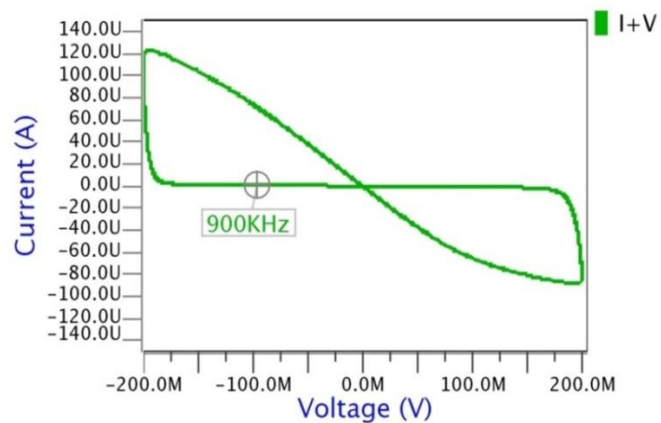


Figure 5.9. Hysteresis loop of grounded memristor emulator at 900KHz frequency

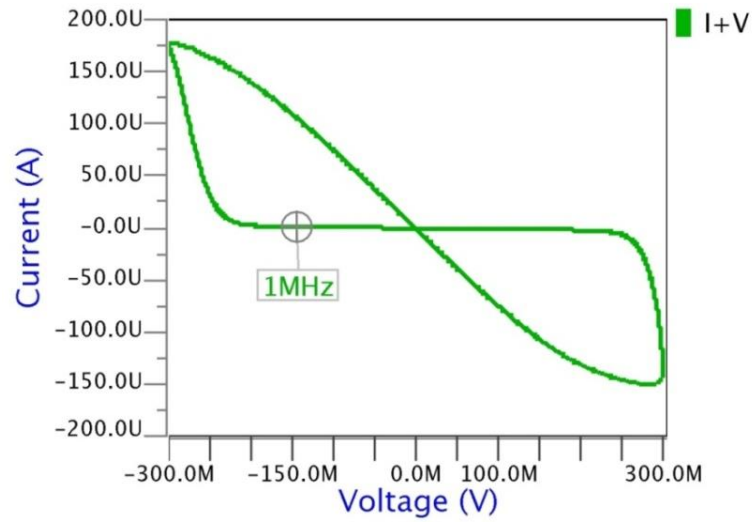


Figure 5.10.Hysteresis loop of grounded memristor emulator at 1MHz frequency

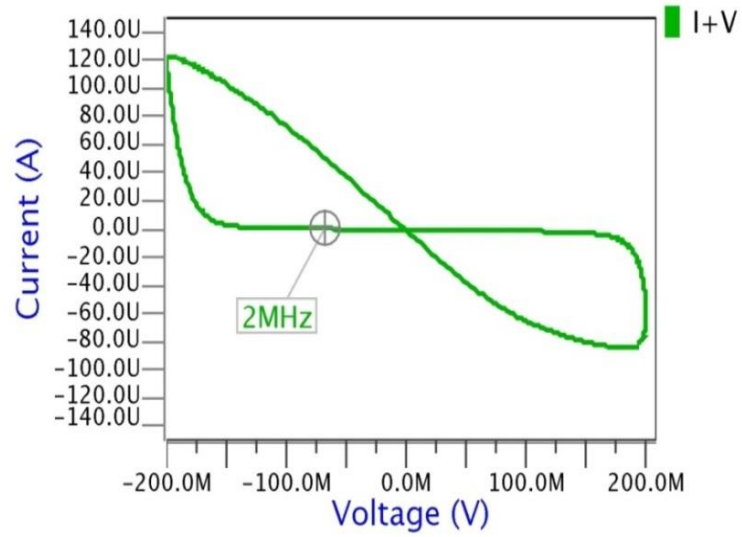


Figure 5.11.Hysteresis loop of grounded memristor emulator at 2MHz frequency

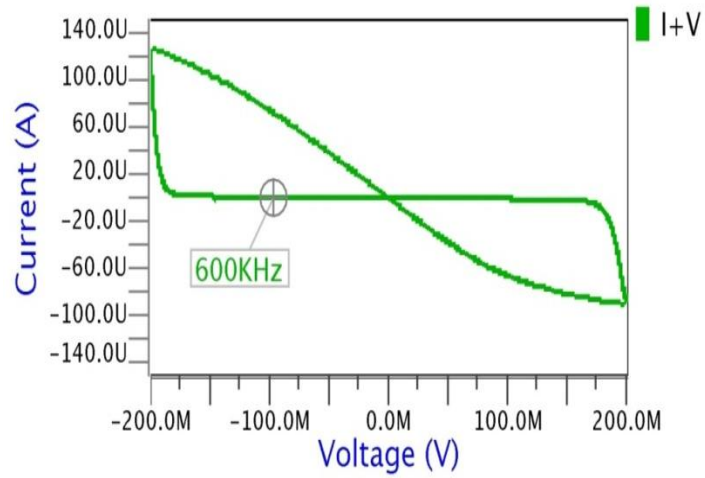


Figure 5.12.Hysteresis loop of floating memristor emulator at 600KHz frequency

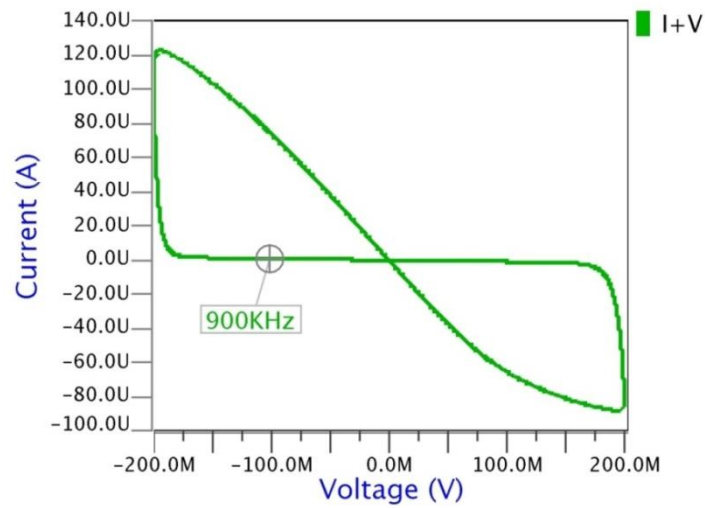


Figure 5.13.Hysteresis loop of floating memristor emulator at 900KHz frequency

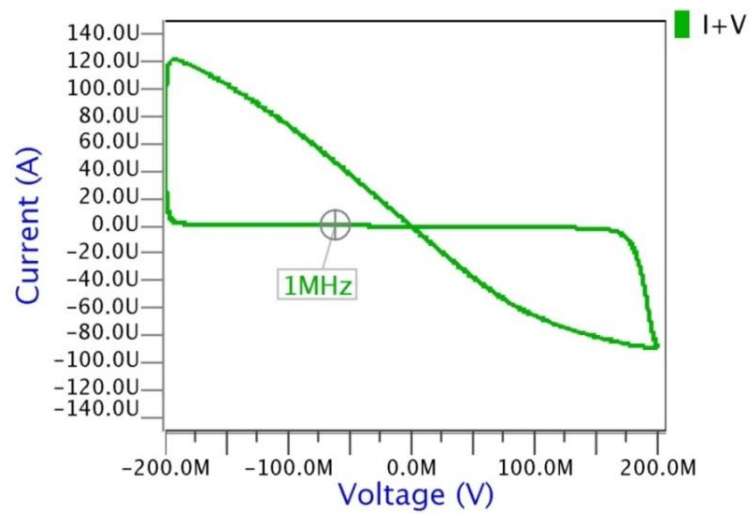


Figure 5.14.Hysteresis loop of floating memristor emulator at 1MHz frequency

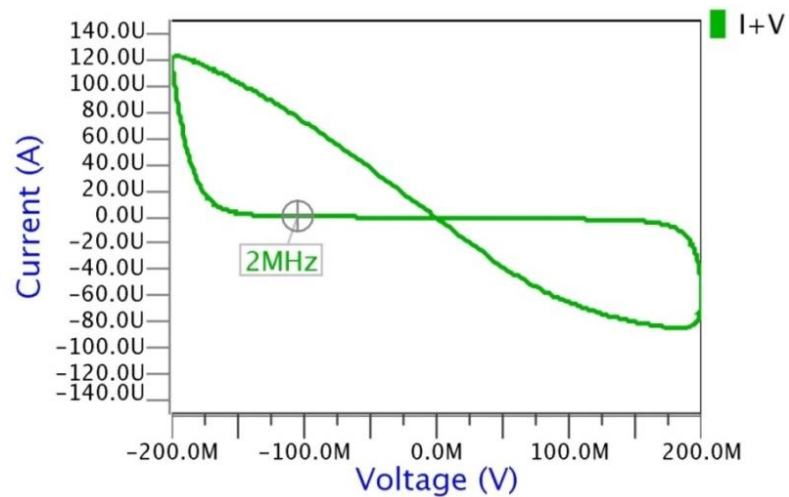


Figure 5.15.Hysteresis loop of floating memristor emulator at 2MHz frequency

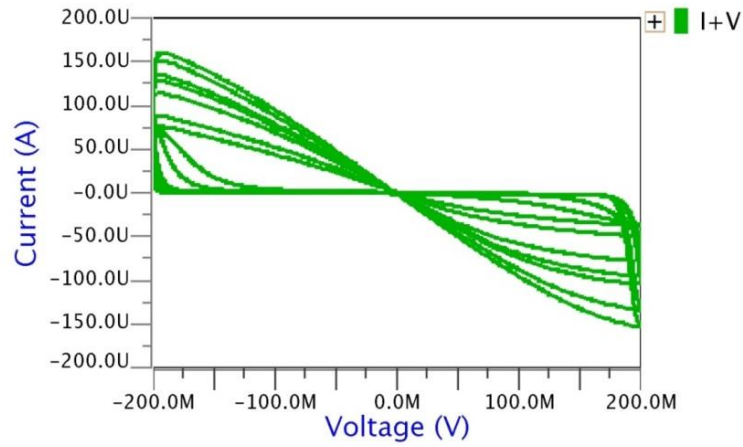


Figure 5.16.Hysteresis loop at different temperatures

5.4 CONCLUSION

In the chapter, source degeneration resistor is formed by using a MOSFET. The MOS M13 is applied at the source of the differential pair M1 and M2. The linear range is increased to $\pm 200\text{mV}$. Gain achieved is $780\mu\text{A/V}$. The transient analysis verifies the symmetry of the circuit. Both floating and grounded memristor emulator works for frequencies range of 600KHz to 2MHz .

CHAPTER 6

DESIGN AND ANALYSIS OF MEMRISTOR EMULATORS USING SYMMETRICAL OTA WITH SOURCE DENERATION AND POSITIVE FEEDBACK

6.1 INTRODUCTION

In this chapter, two techniques have been combined in order to obtain better results. In the first technique, positive feedback is formed by MOSFETs M14 and M15 in the active load (M3 and M6) of differential pair MOSFETs as shown in Figure 6.1. In the second technique, source degeneration technique has been utilized. The drain and gate of both the MOSFETs are connected to the source of MOSFETs M3 and M6 respectively. MOSFET M13, has a tunable voltage V_B , which is required for memristor emulator circuits. Positive feedback provides higher transconductance gain while degeneration technique maintains the linearity of OTA. There is a trade-off between gain and linearity of the circuit by using these techniques. The aspect ratios of MOSFETs M14 and M15 must be kept nearer to unity to provide a better result. The P and N are inputs of the differential pair MOSFET M1 and M2. Since the differential pair MOSFETs M1 and M2 are symmetrical, the transconductance of both the MOSFETs will be same ($g_{m1} = g_{m2}$). MOSFETs M3 to M5 and M6 to M8 form the current mirrors. Terminals I- and I+ are the output for the symmetrical OTA which provide same result but in different phases. These outputs are really useful for different applications. I_{B1} and I_{B2} are the biasing currents required by the OTA circuit.

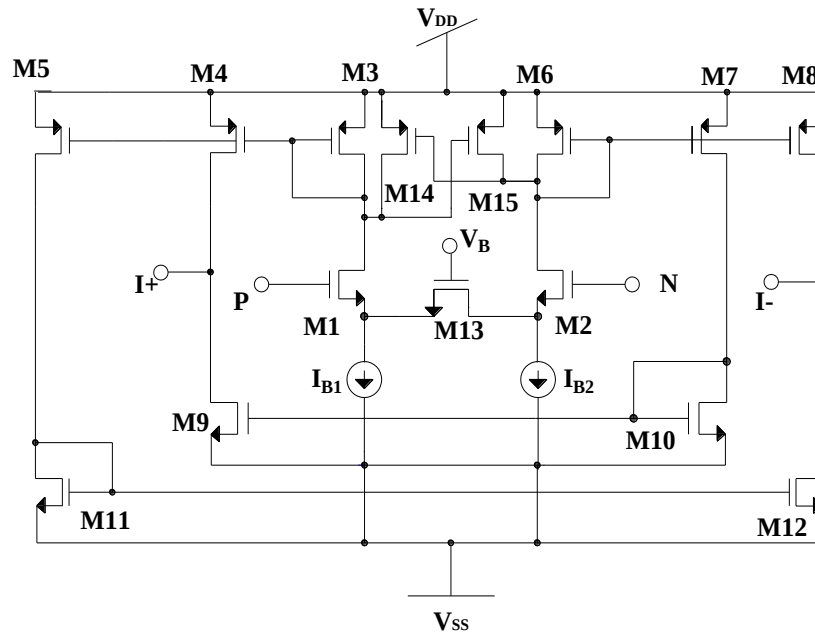


Figure 6.1 CMOS realization for positive feedback and source degeneration symmetrical OTA

6.2 SMALL SIGNAL ANALYSIS OF POSITIVE FEEDBACK AND SOURCE

DEGENERATION OTA

Figure 6.2 shows the small signal model for figure 6.1. By applying the KCL at node V_x , the value of V_{g4} can be expressed in equation (6.1)

$$V_{g4} = - \left(\frac{\frac{g_{m1}V_z}{2}}{(g_{m3} - g_{m14}) + \frac{1}{r_{o1}}(1 + g_{m3}R)} \right) \quad (6.1)$$

From Figure 6.2, it can be observed that V_{g4} and V_{g7} are symmetrical. Therefore, the value of V_{g7} is given in equation (6.2)

$$V_{g7} = \left(\frac{\frac{g_{m2}V_z}{2}}{(g_{m6} - g_{m15}) + \frac{1}{r_{o2}}(1 + g_{m6}R)} \right) \quad (6.2)$$

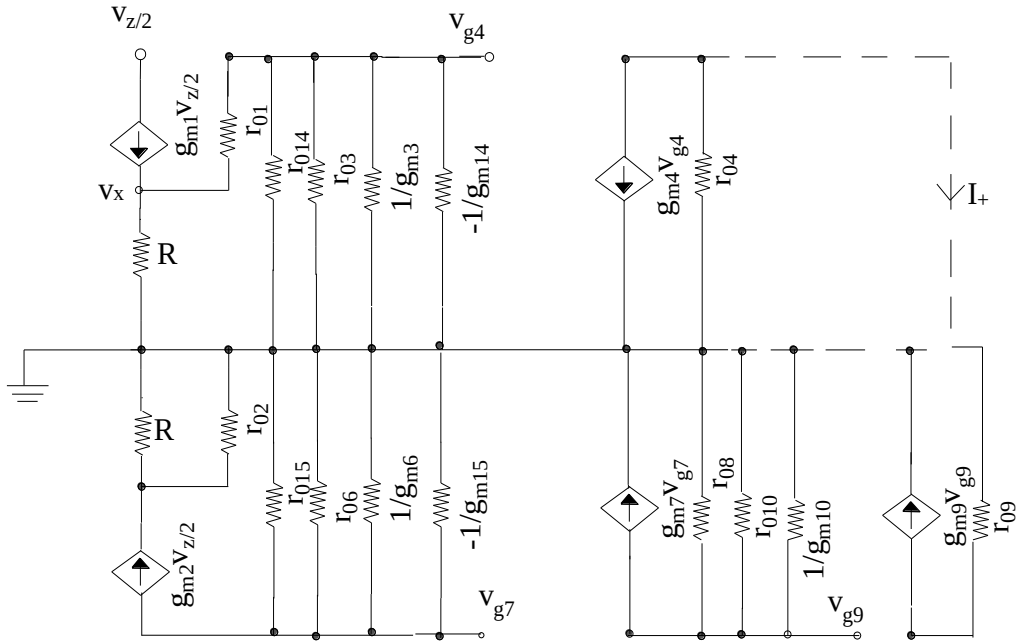


Figure 6.2 Small signal model for positive feedback and source degeneration symmetrical OTA

The value of V_{g9} can be obtained from equation (6.3)

$$V_{g9} = - \left[\frac{g_{m7}V_{g7}}{g_{m10}} \left(\frac{\frac{g_{m2}V_z}{2}}{(g_{m6} - g_{m15}) + \frac{1}{r_{o2}}(1 + g_{m6}R)} \right) \right] \quad (6.3)$$

The output current can be expressed in equation (6.4)

$$I_+ = -g_{m4}V_{g4} - g_{m9}V_{g9} \quad (6.4)$$

Substituting the equation (6.1) and (6.3) into equation (6.5)

$$I_+ = \frac{g_m V_z}{(g_{m6} - g_{m15}) + \frac{1}{r_{o2}}(1 + g_{m6}R)} \quad (6.5)$$

Simplifying the equation (6.5) as the value of $1/r_{o2}$ is very small when compared to $g_{m6}R$

$$I_+ = \left[\frac{g_m V_z}{(g_{m6} - g_{m15}) \left(1 + \frac{R}{r_{o2}} \right)} \right] \quad (6.6)$$

Therefore, it can be concluded that the linear range can be increased by the value of resistance R whereas the transconductance gain is increased by choosing the appropriate value of g_{m6} and M16.

6.3 RESULTS AND DISSCUSIONS

The circuit of OTA with source degeneration and positive feedback is designed and simulated by Mentor graphics ELDO simulation tool by using 0.18 μ m technology parameters. The bias voltages V_{DD} and $-V_{SS}$ are 0.9 V. The value of bias voltage V_B is 600mV. The biasing current I_{B1} and I_{B2} are 100 μ A. The aspect ratios of MOSFETs are shown in Table 6.1

Table 6.1. Aspect ratios of MOSFETs

MOS	W(μm)	L(μm)
M1, M2	16	1
M3-M8	6	1
M9-M12	4	1
M13	20	1
M14, M15	4	1

The figure 6.3 shows the DC analysis of symmetrical OTA with source degeneration and positive feedback with a linear range of -200mV to 200mV. Figure 6.4 gives the AC analysis of the OTA, and the observed bandwidth is 129MHz. Figure 6.5 gives the transient analysis where the swing of output current is $\pm 140\mu\text{A}$.

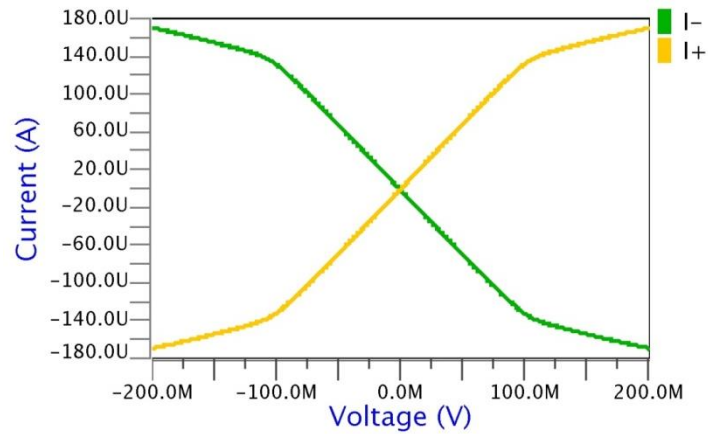


Figure 6.3. DC analysis of OTA with linear range of $\pm 200\text{mV}$

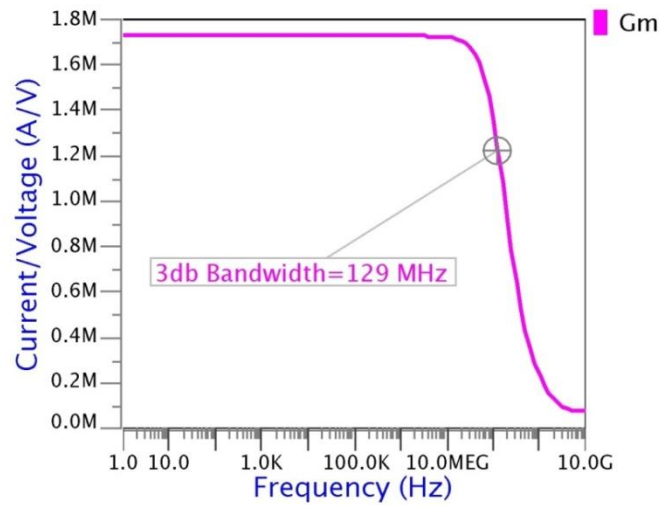


Figure 6.4. AC analysis of OTA where $I_{B1}=I_{B2}=100\mu\text{A}$

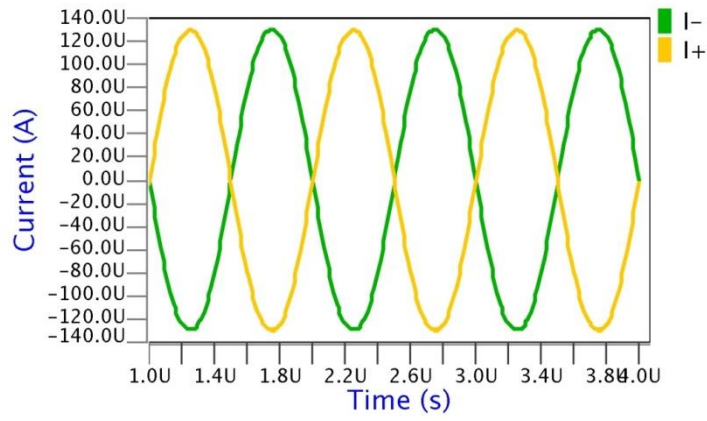


Figure 6.5. Transient analysis of OTA

Figure 6.6 shows the transient analysis after applying the input voltage of amplitude of 100mV with 1MHz frequency. The figures 6.7-6.10 shows the current-voltage graph which are the pinched hysteresis loop for a grounded memristor emulator circuit at different frequencies of 600 KHz, 900 KHz, 1MHz and 2MHz. It can be observed that with the increase in frequency the loop size shrinks and at higher frequency the circuit behave as a linear resistor. The figures 6.11-6.14 shows the pinched hysteresis loop for floating memristor emulator at frequencies 600KHz, 900KHz, 1MHz and 2MHz. The figure 6.15. shows the pinched hysteresis loop at different temperatures from -40°C to 100°C it can be observed, that with the increase in temperature the loop size shrinks and becomes smaller.

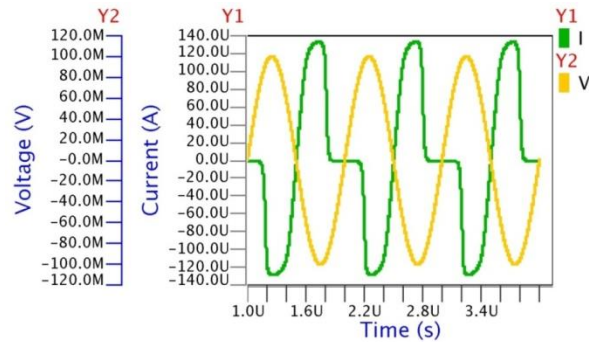


Figure 6.6. Transient analysis of memristor emulator

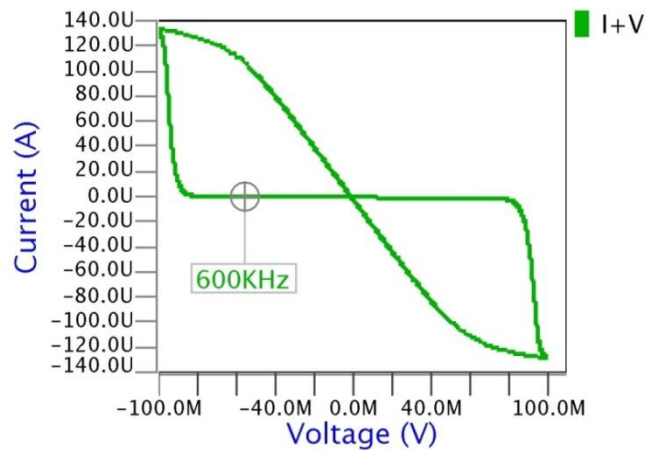


Figure 6.7. Hysteresis loop of grounded memristor emulator at 600 KHz frequency

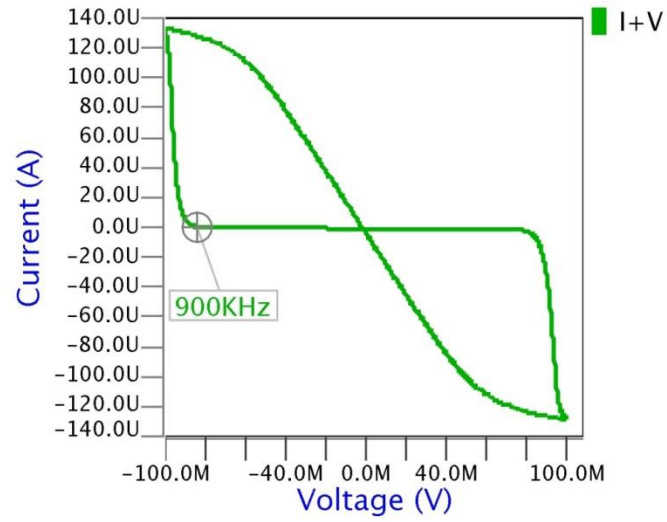


Figure 6.8. Hysteresis loop of grounded memristor emulator at 900KHz frequency

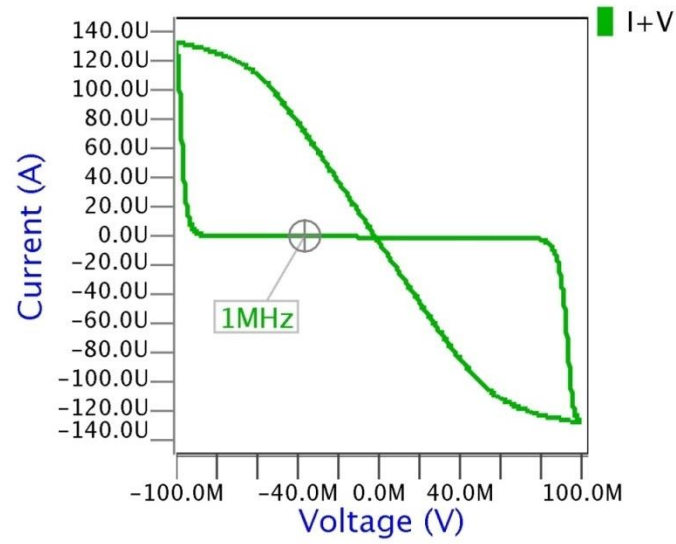


Figure 6.9. Hysteresis loop of grounded memristor emulator at 1MHz frequency

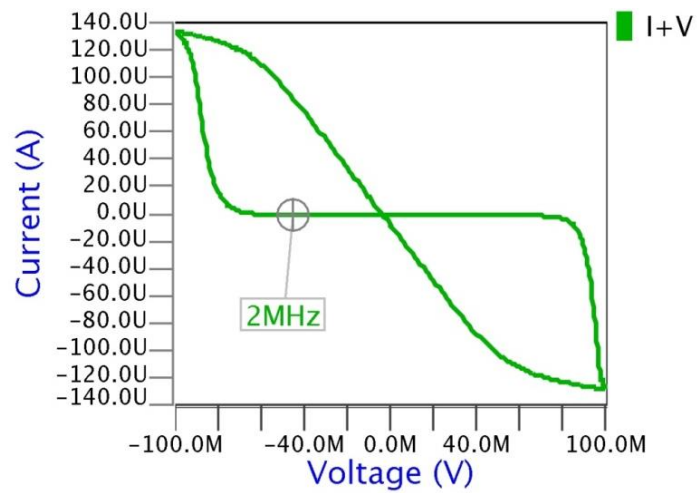


Figure 6.10. Hysteresis loop of grounded memristor emulator at 2MHz frequency

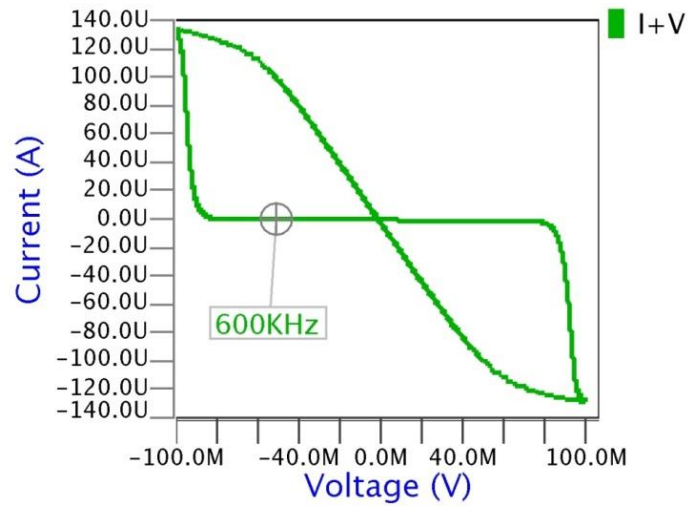


Figure 6.11. Hysteresis loop of floating memristor emulator at 600KHz frequency

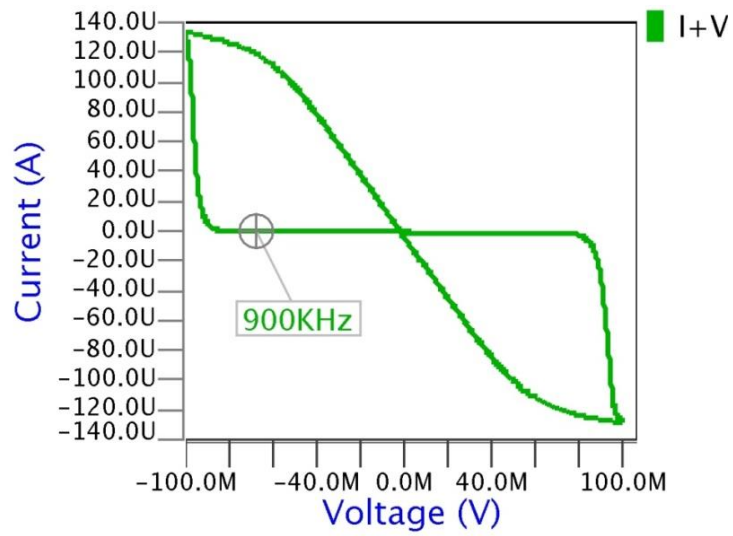


Figure 6.12. Hysteresis loop of floating memristor emulator at 900KHz frequency

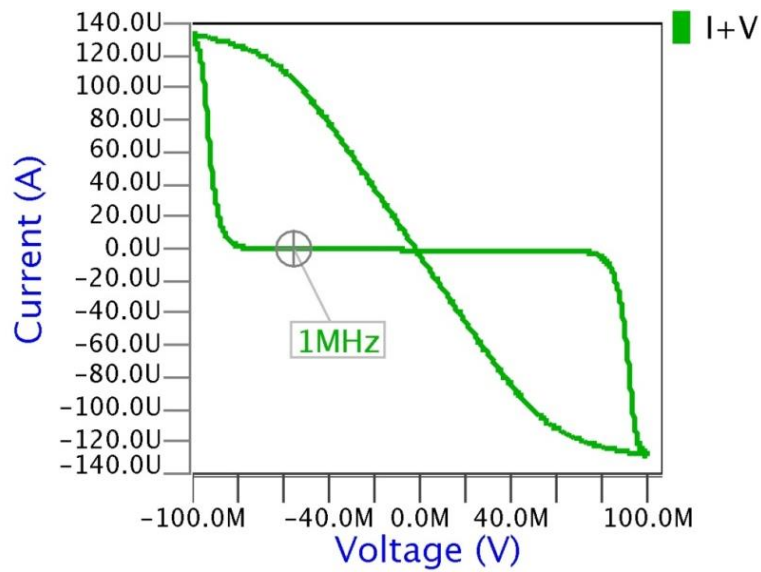


Figure 6.13. Hysteresis loop of floating memristor emulator at 1MHz frequency

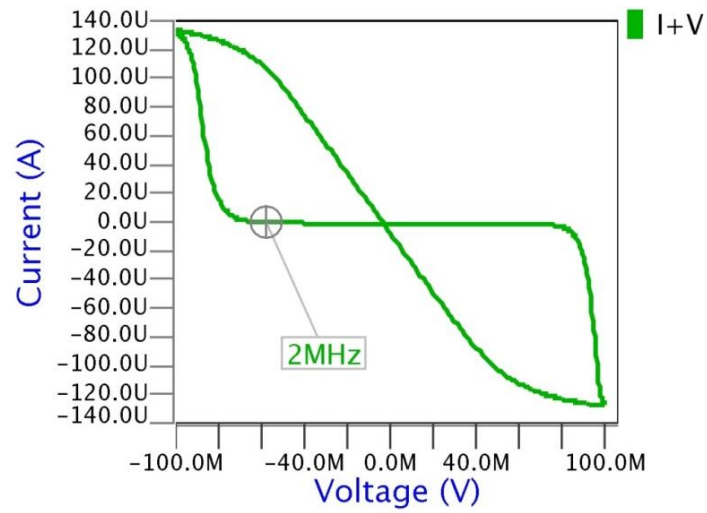


Figure 6.14. Hysteresis loop of floating memristor emulator at 2MHz frequency

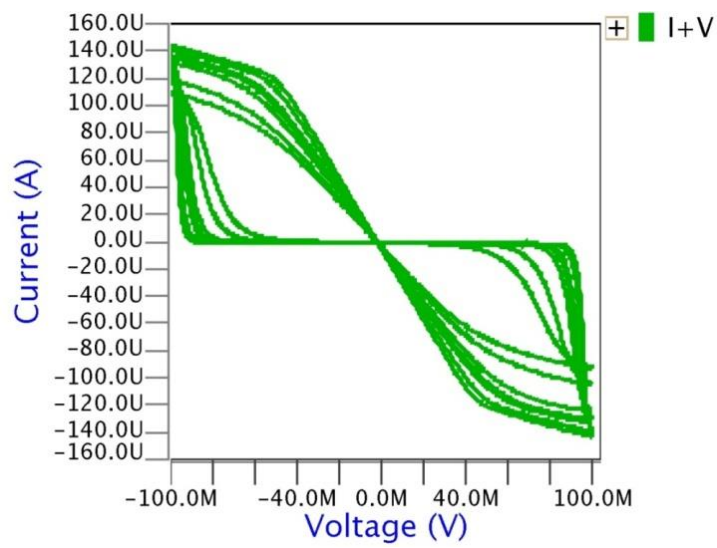


Figure 6.15. Hysteresis loop at different temperatures

6.4 CONCLUSION

In this chapter, two techniques are combined which are source degeneration and positive feedback. By using these two techniques the linearity and transconductance gain are increased. The linear range of the OTA is $\pm 200\text{mV}$ and the gain is 1.75mA/V which is more than all the previous techniques. Transient analysis is performed to verify the symmetry of the circuit. The circuit is used for memristor emulators. Both floating and grounded memristor emulator work for the frequencies range 600KHz to 2MHz .

CHAPTER 7

DESIGN AND ANALYSIS OF MEMRISTOR EMULATORS USING SYMMETRICAL OTAWITH SOURCE DEGENERATION, POSITIVE FEEDBACK AND PARALLEL MOSFETs USED IN DIFFERENTIAL PAIR

7.1 INTRODUCTION

In this chapter, three techniques are combined to get better results for the symmetric OTA. For the first technique, MOSFETs M16 and M17 are applied in parallel to the differential pair MOSFETs M1 and M2. For the second technique, positive feedback is applied at the active load of the differential pair MOSFETs M3 and M6. The third technique is the MOS M13 which is applied for the source degeneration as shown in figure 7.1. The number of parallel MOSFETs can be increased depending upon the application it is used in. The source and drain of the parallel MOSFETs connected to the source and drain of the differential pair MOSFETM1 and M2. M13 MOS, has a tunable voltage V_B , which is needed for memristor emulator circuits. Parallel MOSFETs and positive feedback both offers high transconductance gain while source degeneration maintains the linear range of the circuit. There is a trade-off between transconductance gain, linearity and power dissipation of the circuit by using these techniques. The aspect ratios of MOSFETs M16 and M17 are kept same as that of the differential pair MOSFET. The P and N are inputs of the differential pair MOSFET M1 and M2. Since the differential pair MOSFETs M1 and M2 are symmetrical, the transconductance of both the MOSFETs will be same ($g_{m1} = g_{m2}$). MOSFETs M3 to M5 and M6 to M8 forms the current mirrors. The obtained results (I_- and I_+) at X_+ and X_- terminals are the output for the symmetrical OTA which provide same amplitude but phase is different. I_{B1} and I_{B2} are the biasing currents required by the OTA circuit.

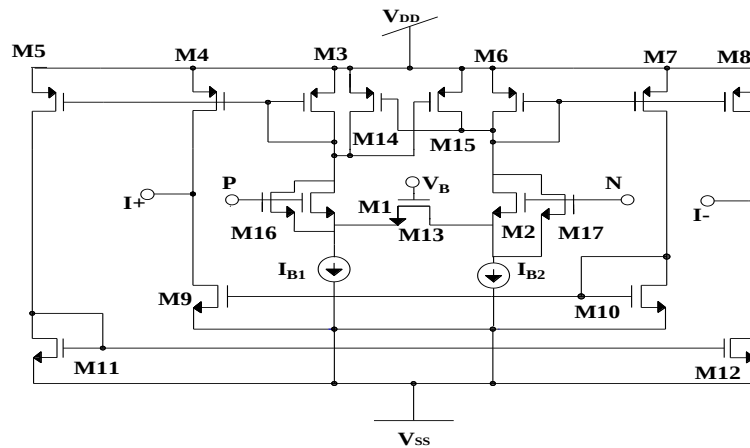


Figure 7.1. CMOS realization of OTA with source degeneration, parallel MOSFETs and positive feedback

7.2 SMALL SIGNAL ANALYSIS OF OTA WITH SOURCE DEGENERATION, POSITIVE FEEDBACK AND PARALLEL MOSFETs

Figure 7.2 shows the small signal model for figure 7.1. By applying the KCL at node V_x , the value of V_{g4} can be expressed in equation (7.1).

$$V_{g4} = - \left(\frac{g_{m1} + \dots + g_{m1(N-1)} + g_{m1N}}{(g_{m3} - g_{m14}) + \frac{1}{r_{o1}}(1 + g_{m3}R)} \right) \frac{V_z}{2} \quad (7.1)$$

From Figure 7.2, it can be observed that V_{g4} and V_{g7} are symmetrical. Therefore, the value of V_{g7} is given in equation (7.2)

$$V_{g7} = \left(\frac{(g_{m2} + \dots + g_{m2(N-1)} + g_{m2N})V_z}{2} \right) \frac{1}{(g_{m6} - g_{m15}) + \frac{1}{r_{o2}}(1 + g_{m6}R)} \quad (7.2)$$

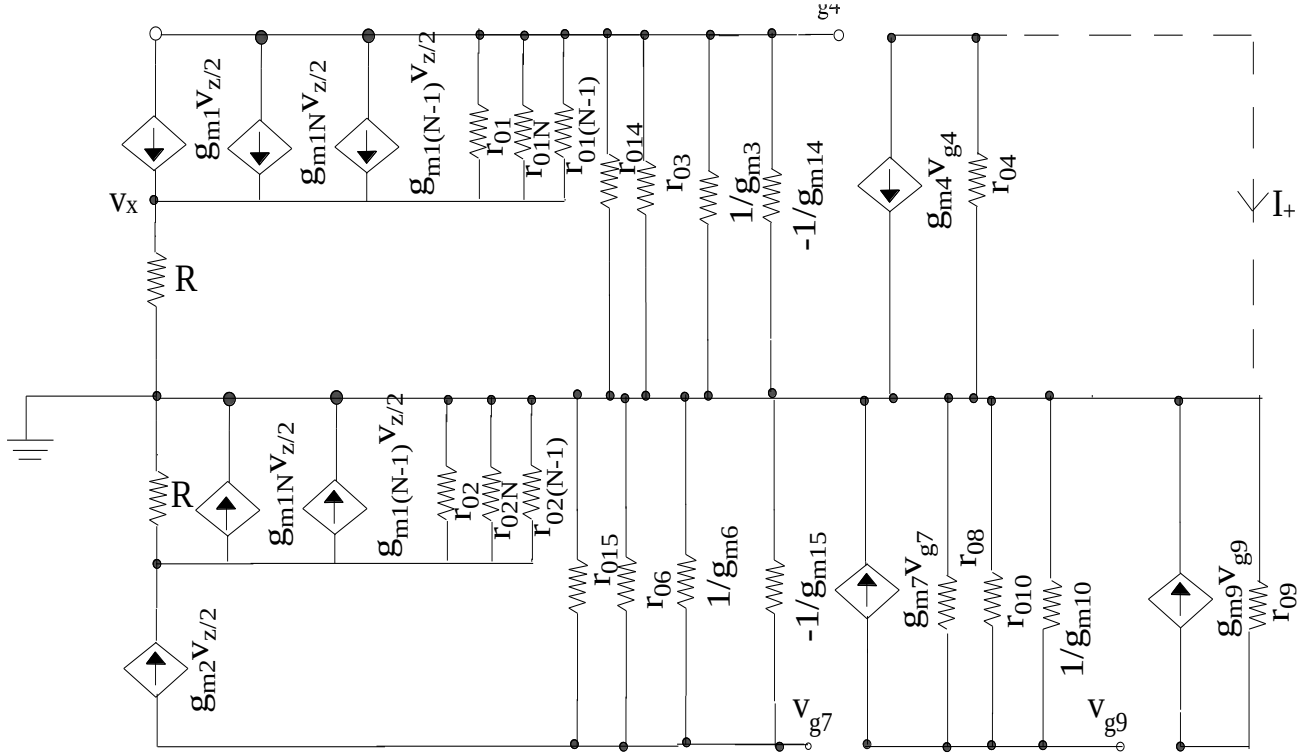


Figure 7.2. Small signal model for parallel MOSFETs, positive feedback and source degeneration symmetrical OTA

The value of V_{g9} can be obtained from equation (7.3)

$$V_{g9} = - \left[\frac{g_{m7} V_{g7}}{g_{m10}} \left(\frac{(g_{m2} + \dots + g_{m2(N-1)} + g_{m2N})}{(g_{m6} - g_{m15}) + \frac{1}{r_{02}} (1 + g_{m6} R)} \right) \frac{V_z}{2} \right] \quad (7.3)$$

The output current can be expressed in equation (7.4)

$$I_+ = -g_{m4} V_{g4} - g_{m9} V_{g9} \quad (7.4)$$

Substituting the equation (7.1) and (7.3) into equation (7.5)

$$I_+ = \frac{(g_{m1} + \dots + g_{m1(N-1)} + g_{m1N}) + (g_{m2} + \dots + g_{m2(N-1)} + g_{m2N}) V_z}{(g_{m6} - g_{m15}) + \frac{1}{r_{02}} (1 + g_{m6} R)} \quad (7.5)$$

Simplifying the equation (7.5) as the value of $1/r_{02}$ is very small when compared to $g_{m6} R$

$$I_+ = \left(\frac{(g_{m1} + \dots + g_{m1(N-1)} + g_{m1N}) V_z}{(g_{m6} - g_{m15}) \left(1 + \frac{R}{r_{02}} \right)} \right) \quad (7.6)$$

Therefore, it can be concluded that the linear range can be increased by the value of resistance R .

7.3 RESULTS AND DISSCUSSIONS

The circuit of symmetrical OTA with source degeneration, positive feedback and parallel MOSFET is designed and simulated by Mentor Graphics ELDO simulation tool by using 0.18 μ m technology parameters. The bias voltages V_{DD} and $-V_{SS}$ are 0.9 V. The value of bias voltage V_B is 600mV. The biasing current I_{B1} and I_{B2} are 100 μ A. The aspect ratios of MOSFETs are shown in Table 7.1

Table 7.1. Aspect ratios of MOSFETs

MOS	W(μ_m)	L(μ_m)
M1, M2, M16, M17	16	1
M3-M8	6	1
M9-M12	4	1
M13	20	1
M14, M15	4	1

The figure 7.3 shows the DC analysis of symmetrical OTA with source degeneration and positive feedback with a linear range of -200mV to 200mV .Figure 7.4 gives the AC analysis of the OTA, and the observed bandwidth is 120MHz. Figure 7.5 gives the transient analysis of the symmetrical OTA with the output current swing of $\pm 150\mu\text{A}$.

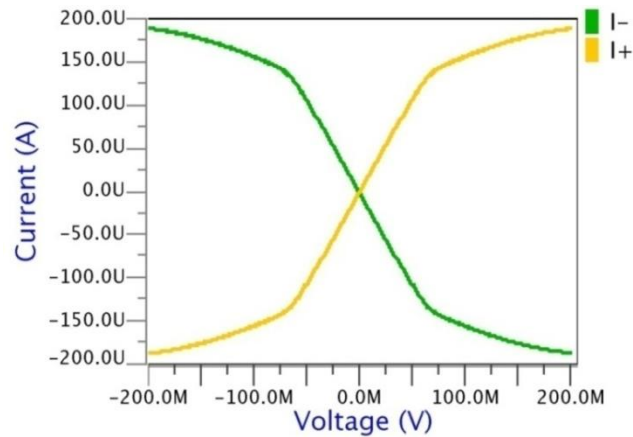


Figure 7.3. DC analysis of OTA at 200mV

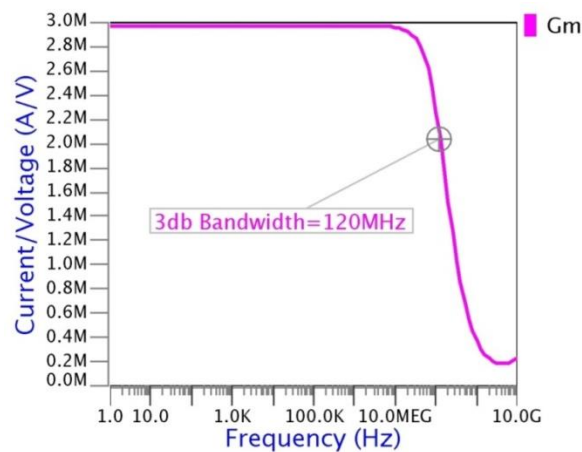


Figure 7.4. AC analysis of OTA where $I_{B1}=I_{B2}=100\mu\text{A}$

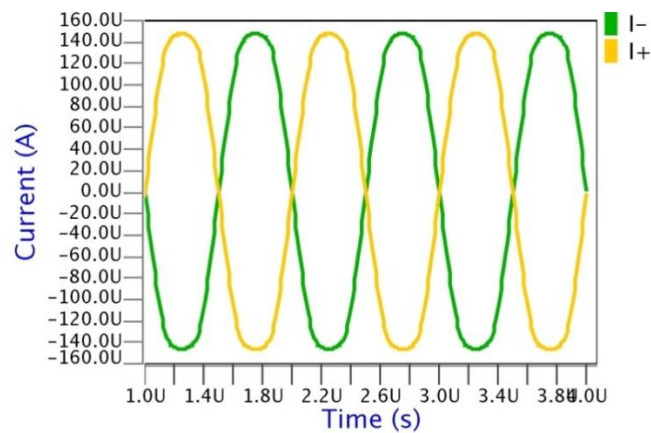


Figure 7.5. Transient analysis of OTA

The figure 7.6 shows the time response at 100mV with frequency 1MHz of memristor emulator circuit with source degeneration and positive feedback. The figures 7.7- 7.9 shows the characteristics of pinched hysteresis loop for a grounded memristor emulator circuit at different frequencies of 600KHz,900KHz and 1MHz. It can be observed that with the increase in frequency the loop size shrinks and at higher frequency the circuit behave as a linear resistor. The figures 7.10-7.12 shows the pinched hysteresis loop for floating memristor emulator at frequencies 600KHz, 900KHz and 1MHz. The figure 7.13 shows the pinched hysteresis loop at different temperatures from -40°C to 100°C it can be observed, that with the increase in temperature the loop size shrinks and becomes smaller.

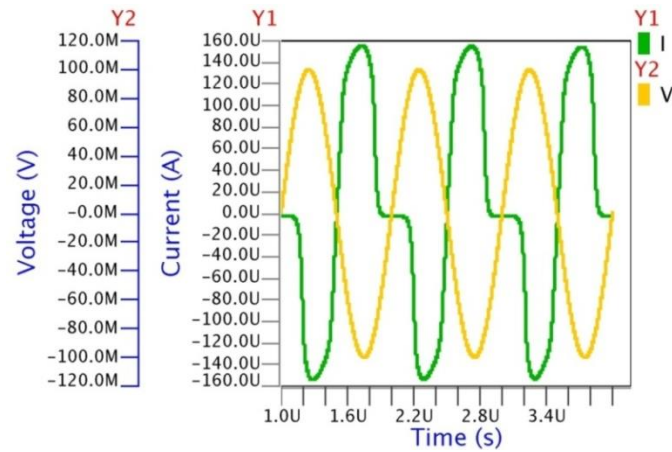


Figure 7.6. Transient analysis of memristor emulator

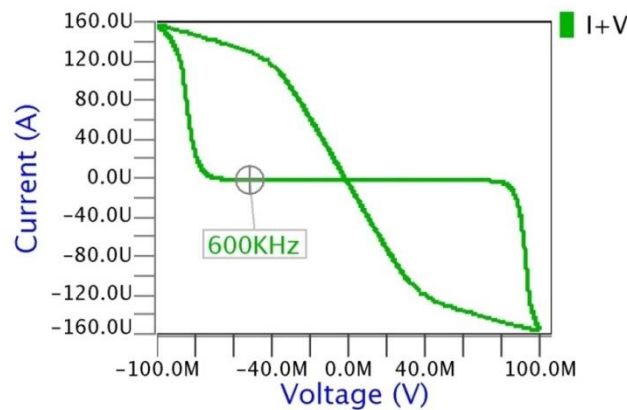


Figure 7.7. Hysteresis loop of grounded memristor at 600KHz frequency

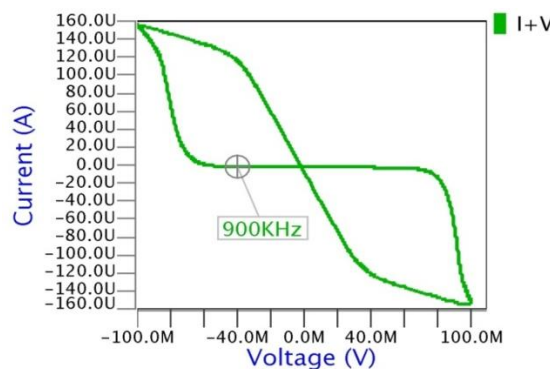


Figure 7.8. Hysteresis loop of grounded memristor at 900KHz frequency

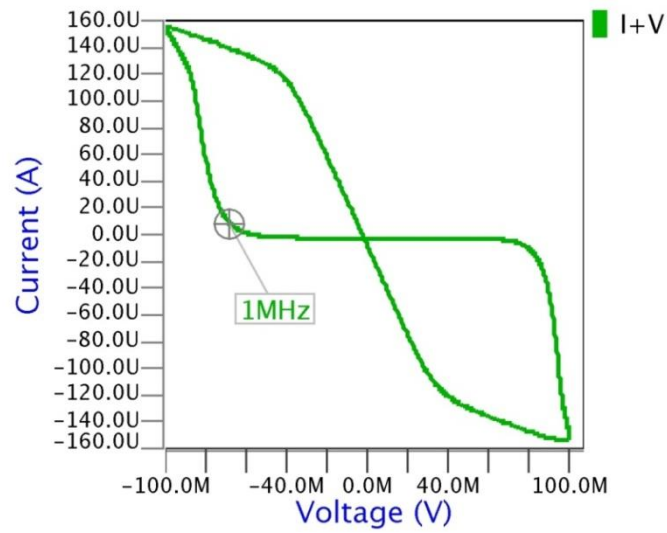


Figure 7.9. Hysteresis loop of grounded memristor at 1MHz frequency

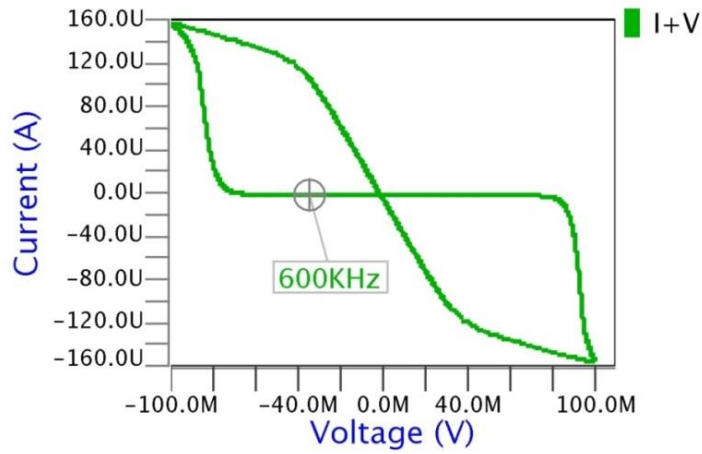


Figure 7.10. Hysteresis loop of floating memristor at 600KHz frequency

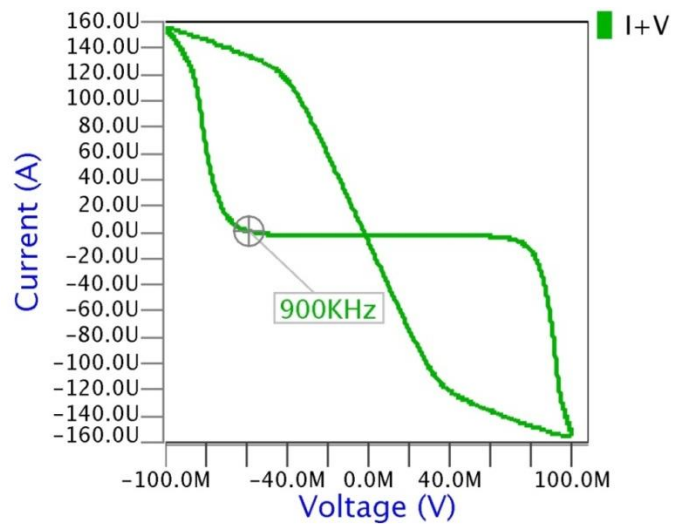


Figure 7.11. Hysteresis loop of floating memristor at 900KHz frequency

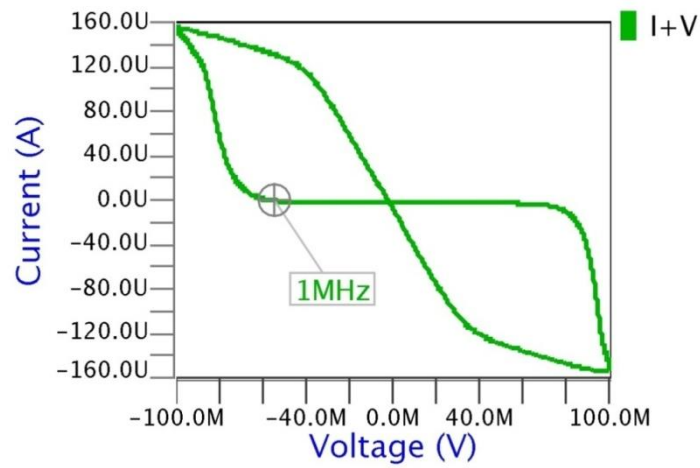


Figure 7.12. Hysteresis loop of floating memristor at 1MHz frequency

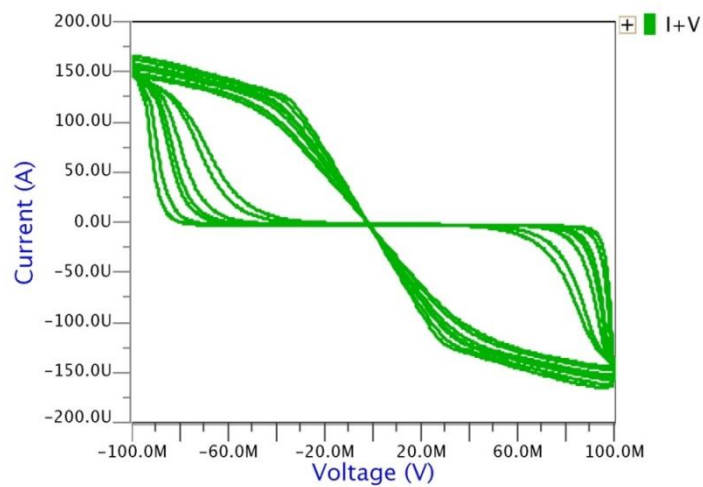


Figure 7.13. Hysteresis loop at different temperatures

The Table7.2 shows the comparisons between the existing OTA and the OTA in which different techniques are applied. Comparisons among different parameters such as linear range, power dissipation and transconductance gain

Table7.2. Comparison between different OTA structures

Characteristics	Existing OTA	OTA with resistance	OTA with source degeneration	OTA with positive feedback +source degeneration	OTA with parallel MOSFETs +positive feedback + source degeneration
Supply voltage	$\pm 0.9V$	$\pm 0.9V$	$\pm 0.9V$	$\pm 0.9V$	$\pm 0.9V$
Technology	TSMC CMOS 0.18 μm	TSMC CMOS 0.18 μm	TSMC CMOS 0.18 μm	TSMC CMOS 0.18 μm	TSMC CMOS 0.18 μm

I₊/I₋ (-3dB) BW	406MHz	175MHz	350MHz	129MHz	120MHz
Biasing current	I _{B1} =100μA	-	I _{B1} =I _{B2} =100μA	I _{B1} =I _{B2} =100μA	I _{B1} =I _{B2} =100μA
Linearity	-100 to 100mV	-500 to 500mV	-200 to 200mV	-200 to 200mV	-200 to 200mV
Power Dissipation	518.3622 μW	2.5183 mW	1.0365 mW	820.2889 μW	809.4486 μW
Gain	580μA/V	250μA/V	750 μA/V	1.75mA/V	2.99mA/V

The advantages offered by different techniques are present in this table. Depending upon the application the technique can be used. It can be observed from the table, that the linear range is maximum for OTA with source degeneration resistance which is $\pm 500\text{mV}$. The transconductance gain is maximum for OTA with source degeneration, positive feedback and parallel MOSFETs which is 2.99 mA/V .

7.4 CONCLUSION

In this chapter, combination of three techniques is applied which are source degeneration, positive feedback and parallel MOSFETs. The observed linear range is $\pm 200\text{mV}$. Gain is 2.99 mA/V which is the highest among all the other OTAs. Transient analysis shows that the OTA is symmetric. Both the grounded and floating memristor emulator works for frequency range of 600KHz to 1MHz . A comparison table for different structures of OTA is also presented in this chapter to summarize the results obtained in different chapters.

CHAPTER 8

PROPOSED GROUNDED AND FLOATING MEMRISTOR EMULATORS

8.1 INTRODUCTION

In this chapter, new grounded and floating memristor emulator are proposed by the use of CDTA and OTA. CDTA (current differential transconductance amplifier) is an active block in which both input and output are currents. This block is a combination of CDU unit and transconductance (TA). The transconductance amplifier uses a biasing current source I_B . The output of CDU is provided to the input of the differential pair. The difference of the input current p and n is transferred to the z terminal as shown in figure 8.1. The transconductance amplifier helps in providing two opposite polarities of outputs. The terminal equations of CDTA are given as

$$V_p = V_n = 0, \quad I_z = I_p - I_n, \quad (8.1)$$

$$V_z = I_z \cdot Z_z, \quad (8.2)$$

$$I_{x+} = g_m V_z, \quad I_{x-} = -g_m V_z. \quad (8.3)$$

$$g_m = \sqrt{2 \cdot \mu_n \cdot C_{ox} \cdot \frac{W}{L}} \cdot \sqrt{I_B} \quad (8.4)$$

The transconductance of OTA can be given by Equation (8.5)

$$G_m = \frac{k}{\sqrt{2}} (V_B - V_{SS} - 2V_{th}) \quad (8.5)$$

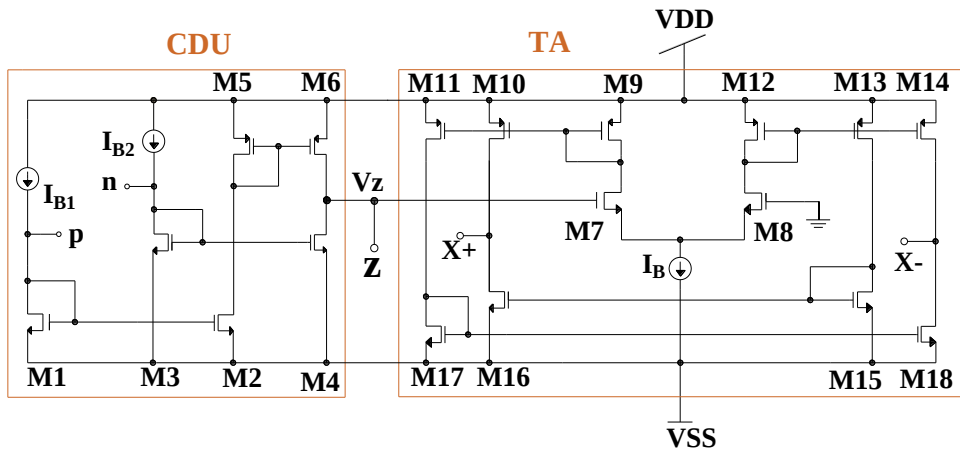


Figure 8.1 CMOS realization of CDTA

8.2 WORKING OF MEMRISTOR EMULATOR CIRCUIT

The proposed grounded and floating memristor emulator circuit is realized by using a CDTA and a OTA as shown in figure 8.2 and figure 8.3 respectively. The OTA used for the circuit is shown in Figure 3.2. The biasing current I_B is replaced by a current mirror. Both incremental and decremental memristor emulator circuits can be made with interchanging the input terminals of OTA.

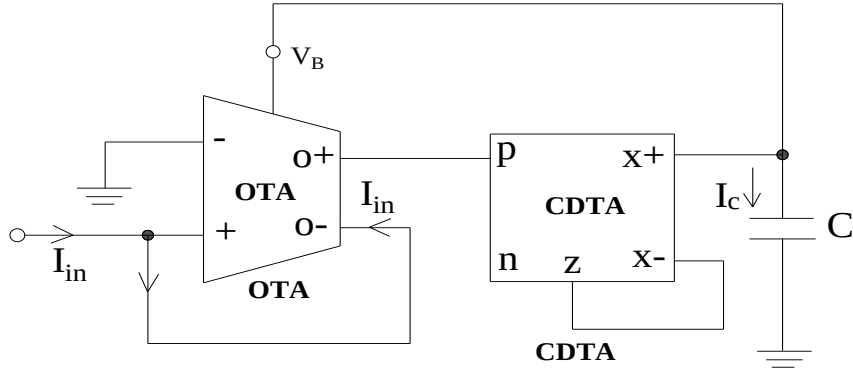


Figure 8.2 Proposed grounded memristor emulator

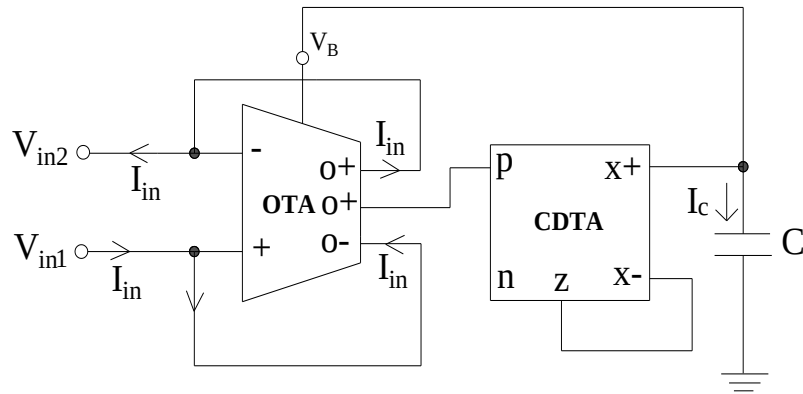


Figure 8.3 Proposed floating memristor emulator

The mathematical analysis of circuit is as follow

The input current can be given in equation (8.6)

$$I_{in} = I_{o-} = G_m V_{in} \quad (8.6)$$

$$I_c(t) = I_{x+} = G_m V_{in} \quad (8.7)$$

The value of capacitor voltage is given in

$$V_c(t) = V_B = \frac{1}{C} \int I_c(t) dt \quad (8.8)$$

Substituting the value of $I_c(t)$ from equation (8.7) into equation (8.8) results in

$$V_c(t) = V_B = \frac{1}{C} \int G_m V_{in}(t) dt = \frac{G_m \phi_{in}}{C} \quad (8.9)$$

Substituting the value of V_B from equation (8.9) into equation (8.5), the obtained transconductance is given

$$G_m = \frac{\frac{k}{\sqrt{2}} (-V_{ss} - 2V_{th})}{1 - \frac{k}{\sqrt{2}} \frac{\phi_{in}}{C}} \quad (8.10)$$

Calculating the value of memristance

$$M(\phi) = \frac{V_{in}}{I_{in}} = \frac{1}{G_m} = - \frac{1}{\frac{k}{\sqrt{2}} (V_{ss} + 2V_{th})} + \frac{\phi_{in}}{C(V_{ss} + 2V_{th})} \quad (8.11)$$

← Fixed part → ← Variable part →

From equation (8.11) it can be observed that the first part of the equation is fixed and the second part is variable which depends upon whether the memristor emulator is incremental and decremental as shown in equation (8.12).

$$M(\phi) = \frac{V_{in}}{I_{in}} = \frac{1}{G_m} = - \frac{1}{\frac{k}{\sqrt{2}} (V_{ss} + 2V_{th})} - \frac{\phi_{in}}{C(V_{ss} + 2V_{th})} \quad (8.12)$$

← Fixed part → ← Variable part →

8.3 RESULTS AND DISCUSSIONS

The proposed memristor emulator is designed and simulated by Mentor Graphics ELDO simulation tool by using 0.18μm technology parameters. The bias voltages V_{DD} and $-V_{SS}$ are 0.9 V. The value of bias current of the transconductance amplifier I_B is 100μA. The aspect ratios of MOSFETs are shown in Table 8.1.

Table.8.1 Aspect ratios of MOSFETs

MOS	W(μ_n)	L(μ_n)
M1-M4	32	2
M5,M6	42.5	0.36
M7,M8	16	1
M9-M14	9	1
M15-M18	4	1

Figure 8.4 shows the transient analysis after applying the input voltage of amplitude of 100mV with 1MHz frequency. The figures 8.5-8.8 shows the current-voltage graph which are the pinched hysteresis loop for a grounded memristor emulator circuit at different frequencies of 600KHz, 800 KHz, 1MHz and 2MHz. It can be observed that with the increase in frequency the loop size shrinks and at higher frequency the circuit behave as a linear resistor. The figures 8.10-8.13 shows the pinched hysteresis loop for floating memristor emulator at frequencies 600KHz, 800KHz, 1MHz and 2MHz. The figure 8.9 and 8.14 shows the pinched hysteresis loop for grounded and floating memristor emulator at different temperatures from -40°C to 40°C it can be observed, that with the increase in temperature the loop size shrinks and becomes smaller.

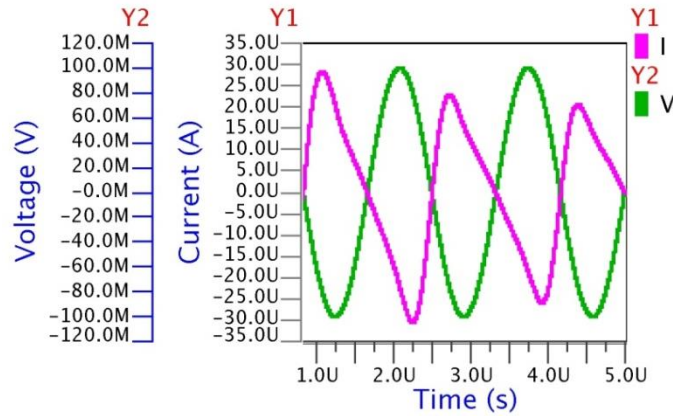


Figure 8.4 Transient analysis of the proposed grounded memristor emulator

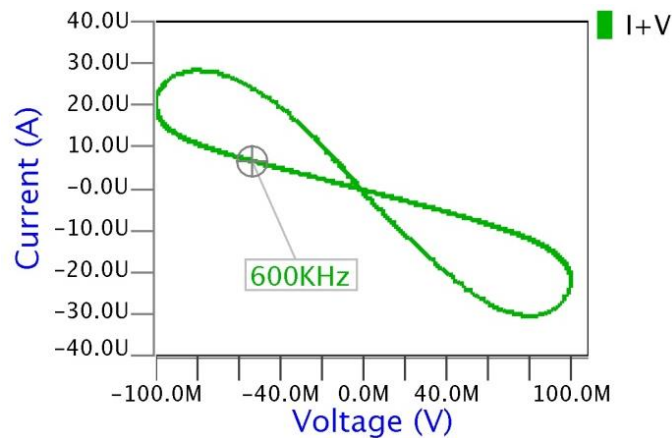


Figure 8.5 Hysteresis loop for grounded memristor emulator at 600KHz frequency

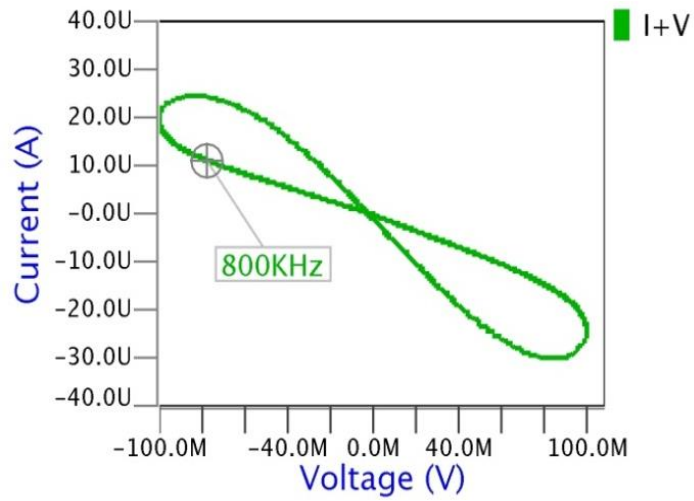


Figure 8.6 Hysteresis loop for grounded memristor emulator at 800KHz frequency

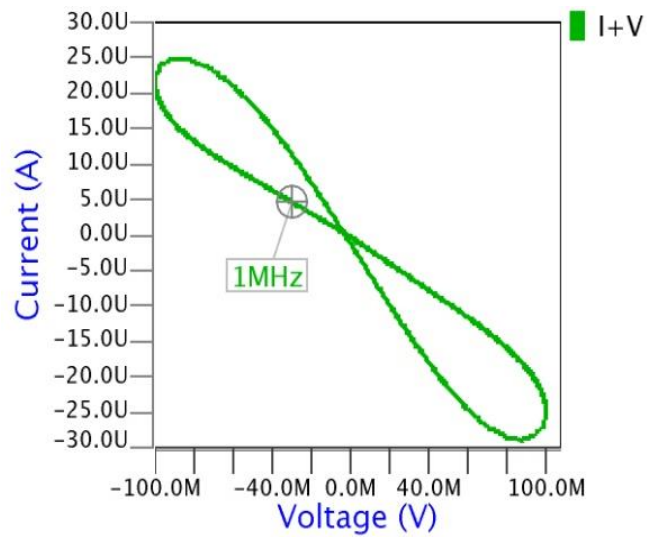


Figure 8.7 Hysteresis loop for grounded memristor emulator at 1MHz frequency

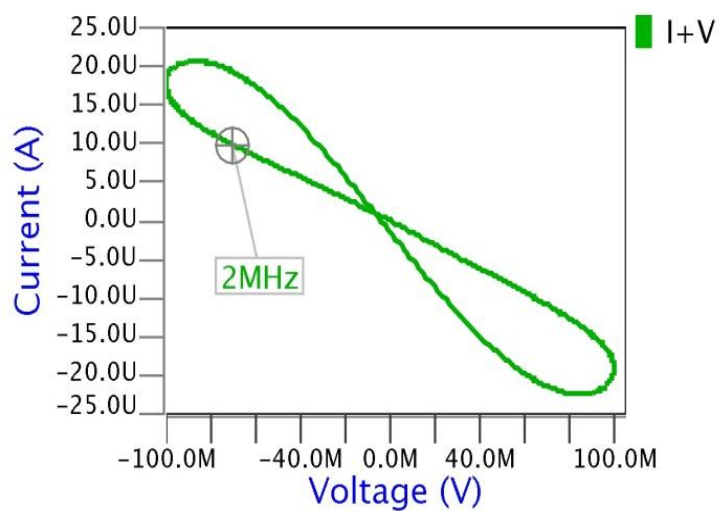


Figure 8.8 Hysteresis loop for grounded memristor emulator at 2MHz frequency

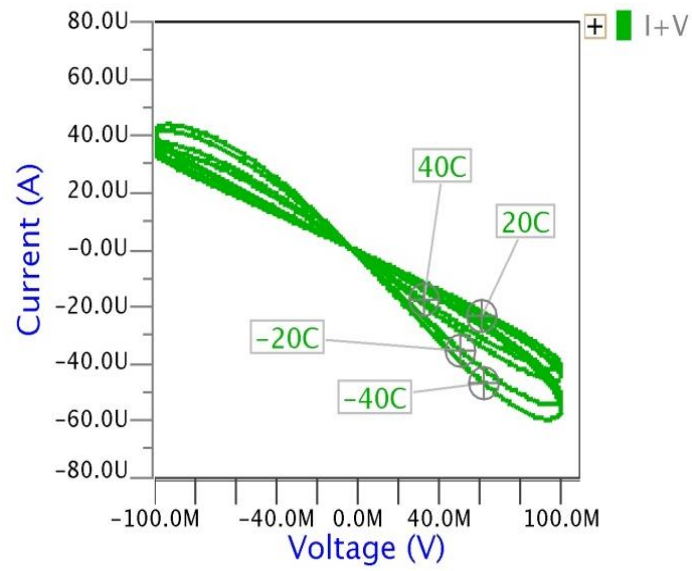


Figure 8.9 Hysteresis loop at different temperature

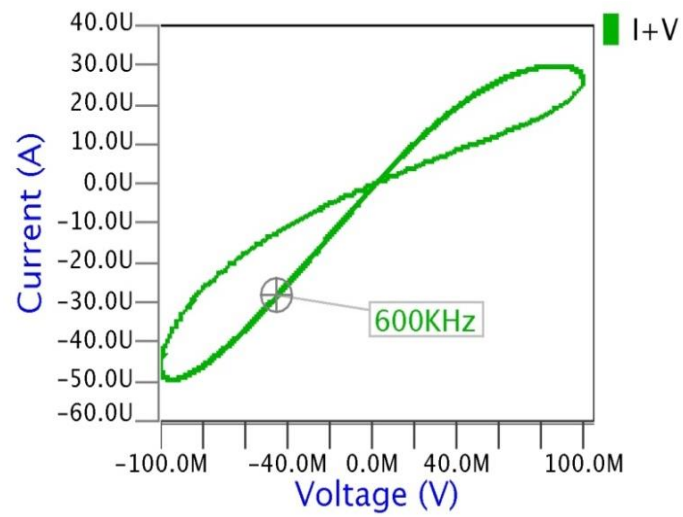


Figure 8.10 Hysteresis loop for floating memristor emulator at 600KHz frequency

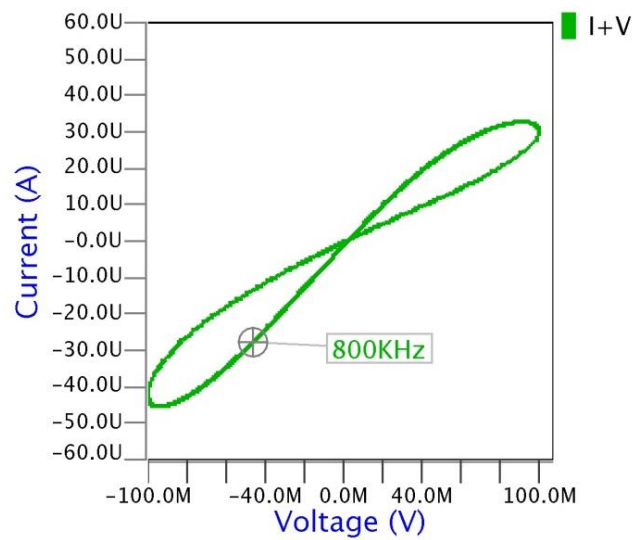


Figure 8.11 Hysteresis loop for floating memristor emulator at 800KHz frequency

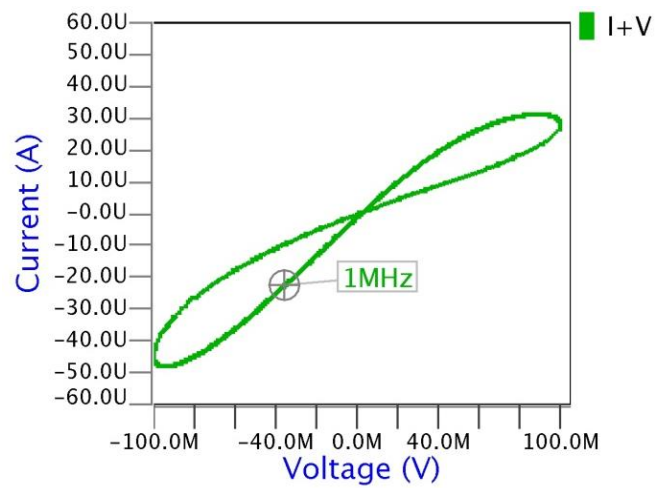


Figure 8.12 Hysteresis loop for floating memristor emulator at 1MHz frequency

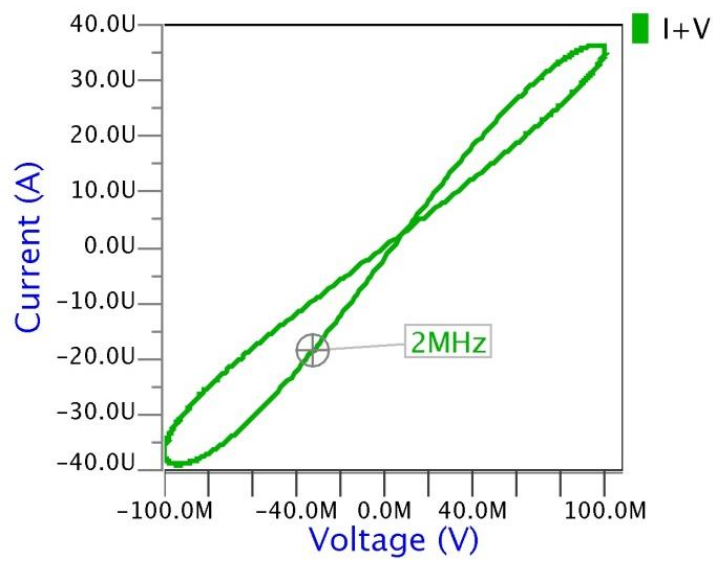


Figure 8.13 Hysteresis loop for floating memristor emulator at 2MHz frequency

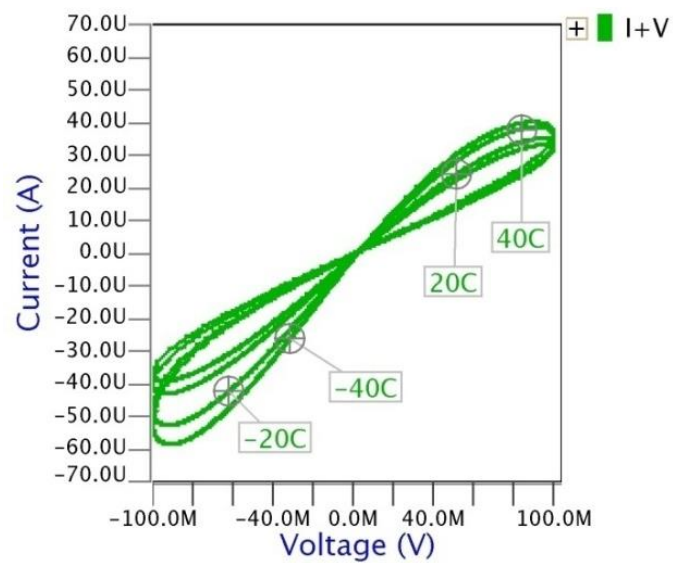


Figure 8.14 Hysteresis loop at different temperatures

8.4 CONCLUSION

A proposed circuit is presented in this chapter, the circuit is realized by using CDTA and OTA. CMOS structure of the circuit is also given. Both grounded and floating memristor emulator is made from the circuit. Incremental and decremental can also be made for floating as well as grounded memristor emulator. Only one passive element capacitor is used in this configuration. Pinched hysteresis loop for grounded and floating memristor emulator is explained in detail with a frequency range of 600KHz to 2MHz. Effect of temperature is also explained in detail with graphs.

CHAPTER 9

CONCLUSION

This thesis presents different structures of OTA and utilize these structures in the design of memristor emulator circuits. Later, a memristor emulator circuit is proposed by using CDTA and OTA. Chapter 3 presents the configuration of an existing symmetrical OTA. Small signal analysis is given which helps in better understanding of the OTA. The circuit for the grounded and floating memristor emulators is explained and this configuration is used as a test circuit for performance verification of all OTAs designed in different chapters of the thesis. The results for OTA and pinched hysteresis loop of memristor emulators is explained in detail. Chapter 4 presents the symmetrical OTA with source degeneration resistances. The source degenerated resistance provides a wider range of linearity. The results of OTA give the linear range of operation and the obtained transconductance. The memristor emulator results provide the working range of circuit at different frequencies. It can be concluded that as the frequency increases the loop size shrinks. The pinched hysteresis loop at different temperature concludes that with the increase in temperature the loop size shrinks. Chapter 5 provides the OTA with source degenerated formed by MOSFETs. The resistances in the above circuit is replaced by MOSFETs. The number MOSFET can be increased in series and parallel. The linear range of the circuit is increased and the transconductance of OTA can be managed with the aspect ratios of the MOSFETs. Results of OTA and memristor emulator are discussed in detail. Chapter 6 is the combination of two techniques which are source degeneration and positive feedback. There is a trade-off between linearity and transconductance of the circuit. Positive feedback provides higher transconductance whereas source degeneration maintains the linearity of the circuit. Results of OTA and memristor emulator are explained in detail. Chapter 7 is the combination of three techniques which are parallel MOSFETs, positive feedback and source degeneration. These provide a higher transconductance and wider range of linearity. Small signal analysis gives the mathematical explanation of the circuit and helps in understanding the circuit better. Results of OTA and memristor emulator circuits are explained in detail. A comparison table is also presented in which all the different techniques applied on OTA are compared, different parameters like transconductance, power dissipation, supply voltage etc. This table helps in choosing the technique according to the application. Chapter 8 presents a proposed circuit of memristor emulator using a CDTA and OTA. Both grounded and floating memristor emulators is designed by using this configuration. With slight change in the circuit the incremental and decremental memristor emulator are also formed. Pinched hysteresis loop for both grounded and floating memristor emulator are shown for the frequency range of 600KHz to 2MHz. Effect of temperature on the loop is also shown.

Since the proposed circuit consist of OTA therefore, in the future scope different techniques can be applied to the proposed circuit to obtain better results in term of linearity, transconductance gain, input/output swing and etc.

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- [50] Vista, J., & Ranjan, A. (2019). A Simple Floating MOS-Memristor for High-Frequency Applications. *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*.

LIST OF PUBLICATIONS

1. Suchitra Gupta, Shireesh Kumar Rai, "New grounded and floating incremental/decremental memristor emulators based on CDTA and its application" Analog integrated circuits and signal processing (Springer) 2019. [under review].

APPENDIX

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21

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