STUDY THE WAVEFORM ANALYSIS OF INTERCONNECT PERFORMANCE FOR FUTURE VLSI DESIGN

Dissertation submitted in the partial fulfillment of requirement for the award of degree of

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VLSI Design

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DECLARATION

I hereby declare that the work which is being presented in the dissertation entitled, **"Study the waveform analysis of interconnect performance for future VLSI design"** in partial fulfillment of the requirement for the award of degree of Master of Technology in VLSI Design, submitted in Electronics and Communication Engineering Department of Thapar University, Patiala, is an authentic record of my own work carried out under the supervision of Mr. Mayank Kumar Rai, Assistant Professor, ECED and refers other researcher's work which are duly listed in the reference section.

The matter presented in this dissertation has not been submitted in any other University/Institute for the award of degree.

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My greatest thanks are to my parents who always wished me success. They have always wanted the best for me and I admire their determination and sacrifice.

Date: Devenderpal Singh

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ABSTRACT

Propagation delay plays an important role in the performance of a chip. But aggressive technology scaling in VLSI field results an increase in resistance of copper interconnect which causes increase in propagation delay. Many researchers show that carbon nanotubes are the best promising candidates for next generation of VLSI interconnect. Carbon nanotubes are preferred over copper interconnect due to their high current carrying capacity and high thermal conductivity.

In this dissertation analytical expression of the output waveform of an SWCNT bundle interconnect and coupled interconnects are presented at 32 nm technology node. Alpha power law model is used to derive current expression for driver transistor and results are compared with existing copper interconnect at same technology node and frequency. A good agreement between analytical model and SPICE simulation model is observed. The effect of various parameters such as interconnect length, driver size and number of repeaters on propagation delay has been analyzed.

The crosstalk induced waveform at victim output has been derived and compared with SPICE simulation results.

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ABBREVIATIONS

CMOS	Complementary Metal Oxide Semiconductor
VLSI	Very Large Scale Integration
CNT	Carbon Nanotube
EDA	Electronic Design Automation
ITRS	International Technology Road Map for Semiconductor
SWCNT	Single Wall Carbon Nanotube
MWCNT	Multi Wall Carbon Nanotube
RLC	Resistance, Inductance and Capacitance
SPICE	Simulation Program with Integrated Circuit Emphasis
PTM	Predictive Technology Model

CHAPTER

1 INTRODUCTION

Introduction:

This chapter involves the basic introduction about VLSI interconnects and previously used interconnect material for VLSI design. A VLSI interconnect is a conducting material that provides electrical connection between two or more nodes of the circuit formed on the silicon chip. Interconnects are multi-conductor lines existing on different physical planes. Interconnect in VLSI circuits is best modeled as a lossy transmission line in high speed integrated circuits [1].

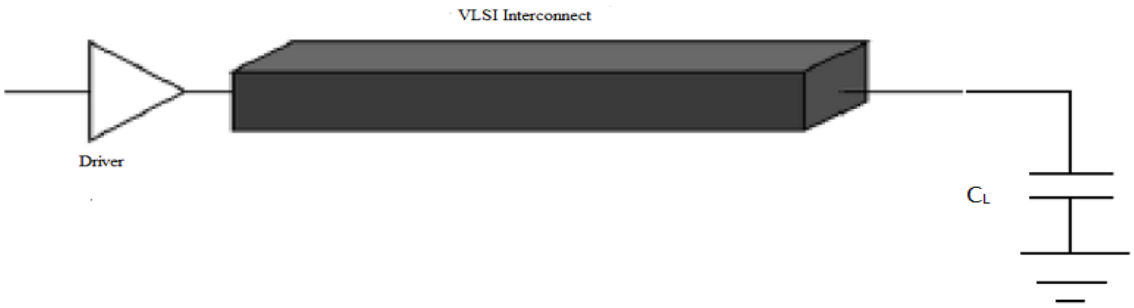

Figure 1.1 VLSI Interconnect [2]

A VLSI interconnect plays an important role in deep submicron technology because in deep submicron technology interconnect can no longer be act as a simple resistor. The associated parasitic such as inductance and capacitance are also need to be considered in deep submicron technologies. These parasitic introduces delay in a propagating signal through interconnects.

1.1 Types of Interconnects

- Local Interconnect
- Semi global Interconnect
- Global Interconnect

Local Interconnect: These are the first, or lowest, level of interconnects. They usually connect gates, sources and drains in MOS technology, and emitters, bases and collectors in bipolar technology. In MOS technology a local interconnect, polycrystalline silicon, also serves as the gate electrode material. Silicided gates and silicided source/drain regions also act as local interconnects [3].

Semi global Interconnects: These are used to connect device within a block.

Global Interconnect: These are used to connect long interconnects between the blocks, including power, ground and clocks. Global interconnects are generally all of the interconnect levels above the local interconnect level. They often travel over large distances, between different devices and different parts of the circuit and therefore are always low resistant metals.

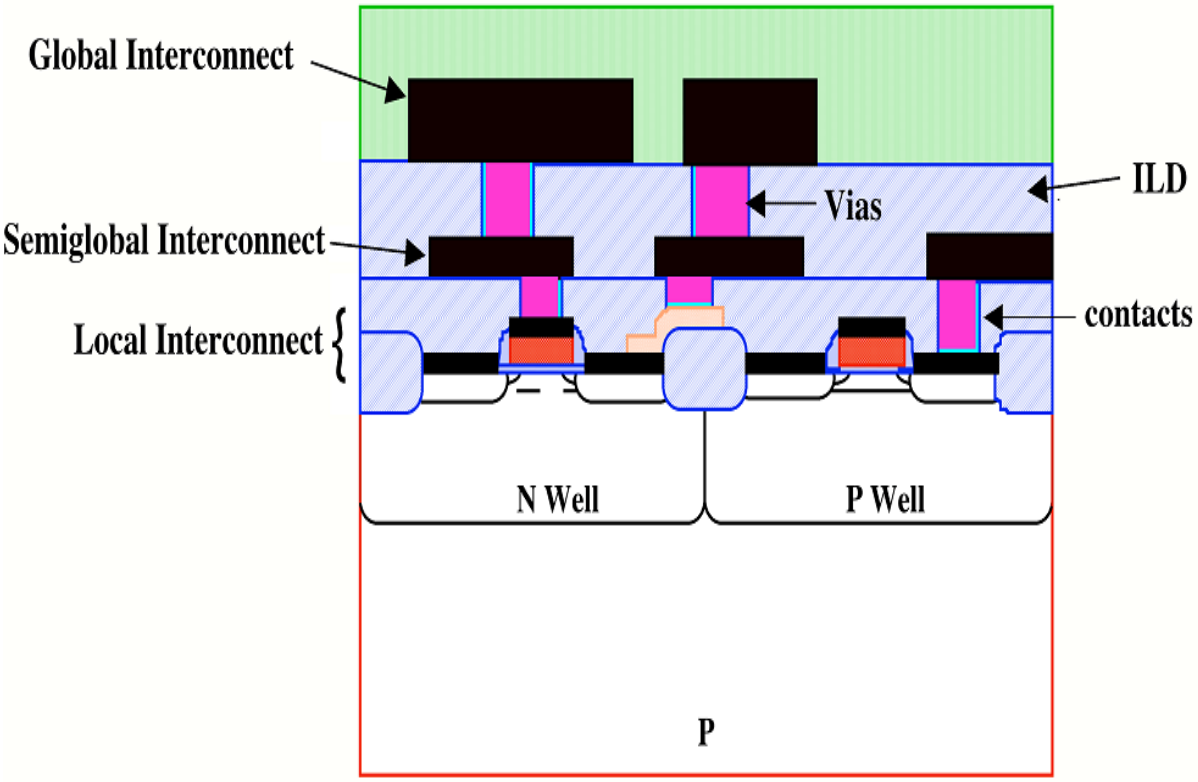

Figure 1.2 Types of Interconnect [3]

Ohmic contacts connect an interconnect with active regions or devices in the silicon substrate. A high resistivity dielectric layer, usually silicon dioxide, separates the active regions from the first level global interconnect, and electrical contact is made between the interconnect and the active regions in the silicon through openings in that dielectric layer. At the same time in the processing, contact can be made between the first level global interconnect and the local interconnects, since they are also separated

by that same dielectric layer. This is shown in Figure. Connections between two levels of global interconnects are usually given a different name: vias.

Separating interconnects from each other and from the active areas and devices are dielectric materials. Those dielectric layers separating one global interconnect level from another are called intermetal dielectrics, or IMD. (Some call these interlevel dielectrics or ILD.) Vias connect interconnects through these layers.

1.2 Scaling of Device and Interconnect Lines

The area occupied by a MOS transistor can be made smaller by shortning its channel width and length. Based on constant field scaling table is suggested (ideal scaling) [4]-

Table 1.1 Scaling of Interconnect

Device/Circuit parameter	Scaling factor
Dimensions w, L	1/S
Voltage	1/S
Field	1
Gate delay	1
Line resistance	S
Line capacitance	1/S

1.3 Previously Used interconnects:

Earlier the most commonly used material was aluminum. The choice was based on its good conductivity. Another useful property of aluminum is that it forms good ohmic contact with silicon. With continuous reduction of feature size there has been a parallel increase in die size. The result is more and more increase in length of some of the on chip interconnects as technology scaling continues. Any increase in interconnect length causes R, L and C to increase [4]. This in turn results in an increase in interconnect signal propagation delay. As device density increased with technology scaling, interconnect current density increased. A disadvantage with aluminum is that at high current densities considerable electro migration takes place. Later copper material was used due to its high conductivity than aluminum. In comparison with aluminum, copper can withstand about five times more current density for IC-applications [5]. Copper has a higher melting point

(1,357 K) than aluminum (933 K). This provides more thermal stability to copper. Because of these advantages copper is the most preferred on chip interconnect material for the present day integrated circuits. Due to the advantages that it offers copper became the preferred interconnect material, especially for submicron and deep submicron high density, high performance chips. With advancement of VLSI technology, the number of on chip interconnects is on the rise. To accommodate more interconnects the cross-sectional dimensions are reduced rapidly resulting in dimensions of the order of mean free path of electrons in copper (~ 40 nm at room temperature). As the dimension approaches electron mean free path grain boundary and surface scattering are enhanced [1, 5]. Consequently, resistivity of interconnect is increased. Another effect of dimension scaling is increase in current density. Thus as technology scales these effects on resistivity together with increase in interconnect resistance with length enhances delay and due to this power dissipation also increases.

1.4 Problems with Existing Interconnect Material:

As technology scales down the interconnect material face many problems which are described as follows:

- **Grain boundary effect**: A grain boundary is the interface between two grains, or crystallites, in a polycrystalline material. Grain boundaries are defects in the crystal structure, and tend to decrease the electrical and thermal conductivity of the material. In copper volume fraction of atoms lying at the grain boundaries are more as compared with conventional coarse-grained polycrystalline materials.
- **Electro migration**: Electro migration is caused by the gradual movement of the ions in a conductor due to the momentum transfer between conducting electrons and diffusing metal atoms. It can cause the eventual loss of connections or failure of a circuit. The electro migration resistivity of copper is high. Due to continuing scaling of very large scale integrated (VLSI) circuits, thin-film metallic conductors or interconnects are subject to increasingly high current densities. Under these conditions, electro migration can lead to the electrical failure of interconnects.

1.5 Carbon Nanotube as Future VLSI interconnect:

Resistivity of copper increases due to effect of electro migration and surface scattering in deep submicron technologies. To overcome these problems various alternative are used, but carbon nanotubes are found to be better alternative than copper interconnect. The CNTs are grown in the form of seamless cylinders with the walls formed by one atomic layer of graphite (graphene). The diameters of these cylinders are of the order of nanometer.

1.5.1 Classification of Carbon Nanotubes:

- **Based on Conductivity:**
  - Metallic
  - Semiconducting
- **Based on layers:**
  - Single-walled Carbon nanotube (SWCNT)
  - Multi-walled Carbon nanotube (MWCNT)

Single walled CNT (SWCNT) and Multiwall CNT (MWCNT). CNTs constituted by only one thin wall of graphene sheet are SWCNTs. There are some CNTs which consist of a multiple of concentric SWCNT like grapheme tubes. These are termed MWCNT. The metallic CNTs are attractive interconnect materials because of their high thermal and mechanical stability [9-10], thermal conductivity as high as 5800W/mK, ability to carry current in excess of 10^{14} A/m^2 current density even at temperatures higher than 200°C. CNTs can be used as building blocks of future integrated circuits due to their outstanding electrical properties. Metallic CNTs have also been suggested as an interconnect material due to their high current carrying capacity and mechanical stability. Due to the variety of extraordinary properties exhibited by carbon nanotubes, a large number of possible applications have been proposed [10].

1.6 Role of Repeaters in interconnect

The Propagation Delay of interconnects is a major factor determining the performance of VLSI circuits, because the RC time constant of interconnects increases very rapidly as chip and interconnect dimensions are scaled aggressively. As the chip dimension increases and the minimum feature size decreases, and propagation delay rises rapidly. To reduce interconnect time delay, properly-scaled multilevel conductors, repeaters,

cascaded drivers, and cascaded drivers as repeaters are presented [7]. Repeater insertion is a technique for reducing the time delay associated with long wire lines in integrated circuits. The technique involves the division of long wire interconnect into smaller sections and inserting a repeater between each new pair of short wire. It can be done by inserting a buffer at the beginning and at the end of the interconnect line to improve the delay and slew rate of the signal [7].

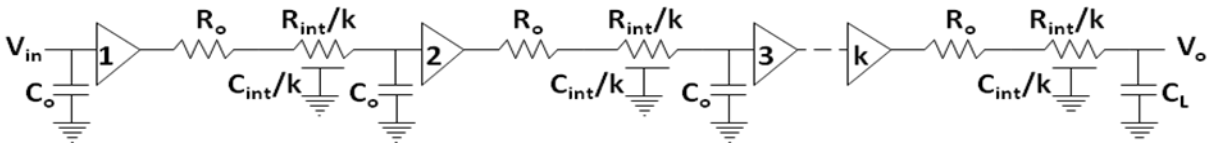

Figure 1.3 Minimum Size Repeaters [7]

When the resistance of the interconnection is comparable to or larger than the on-resistance of the driver, propagation delay increases as the square of the interconnection length because both capacitance and resistance increase linearly with length. The use of repeaters makes time delay linear with length by dividing the interconnection into smaller subsections.

CHAPTER

2 LITERATURE REVIEW

2.1 Interconnect delay models:

H B BAKOGLU, et al. [7] developed a model for interconnection time delay that included the effects of scaling transistor, interconnection and chip dimensions. The delays of aluminum, WSi2, and polysilicon lines were compared. As the chip dimension increases, the minimum feature size decreases, R_{int} becomes important and delay rises rapidly. So, the major challenges were to minimize the capacitances and resistances to reduce the delay. So, two approaches to shortening the delay were investigated. The first was to reduce the interconnection resistance by using only aluminum lines for long-distance communication and by forming multilayers of interconnections with thicker and wider lines in the upper levels. The second was to improve the driver circuit through cascaded drivers that increase in size until the last device was large enough to drive the line and/or by using repeaters that divide the interconnections into smaller subsections.

Yehea I. Ismail, et al. **[17]** developed a model that was based on the alpha power law for deep submicron technology. Two figure of merit were presented that were useful for determining if a section of interconnect should be modeled as either in RC or RLC impedance. The damping factor of a lumped RLC circuit was shown to be useful figure of merit. The second useful figure of merit was the ratio of the rise time of the input signal at the driver of an interconnect line to the time of flight of the signals across the line. A closed form solution of the output response of a CMOS inverter driving an RLC transmission line is presented using the alpha power law for deep sub micrometer technologies. Simple to use figures of merit have been developed that determine the relative accuracy of RC impedance to model on-chip interconnect. At first interconnect was modeled as a lumped RC circuit. To further improve accuracy, the interconnect was modeled as a distributed RC circuit (multiple T and π sections) for those nets requiring more accurate delay models. The range of length of interconnect where a more accurate

transmission line model becomes necessary was shown to be based on the parasitic impedances of the line (R, L, and C) and the rise time of the input signal at the gate driving the line.

Yehea I. Ismail, et al., [18] introduced the effect of inductance on repeater insertion in RLC trees to minimize the maximum path delay. With the continuous scaling of technology and increased die area, the cross-sectional area of interconnects increases due to which resistance of interconnects increases. Meanwhile the gate parasitic impedance decreases due to shrinking of the minimum feature size. So repeater insertion is proposed for driving long resistive interconnects. The interconnects can be subdivided into shorter sections by inserting repeaters to reduce the propagation delay. As inductance affect increases, the area and power consumed by circuit decreases.

Magdy A. et al. [2] proposed an optimum tapered structure for RLC interconnect to minimize the power dissipation. The inductive behavior of the interconnect can no longer be neglected, particularly in long interconnect lines operating at high frequencies. Wire tapering is usually applied to long lines, further increasing the importance of including the line inductance in the optimization process. Wire tapering is an efficient technique to decrease the signal propagation delay in RLC circuit. Wire tapering increases the width of the driver. Tapering an interconnect line can decrease the signal transition time at the load, decreasing the short-circuit current in the load gate circuit. Due to tapering he capacitance of the interconnect line decreases. This decreases in line capacitance reduces both the short-circuit power of the load gate and the dynamic power of the driver, reducing the total power dissipation as compared to uniform sizing. The total power dissipation of an optimally tapered RLC interconnects for minimum power is less than the total power dissipation of a uniformly sized interconnects designed for minimum power. The reduction in power becomes greater as the number of driven gates increases. A reduction in total power dissipation of about 72% is achieved when optimal tapering for minimum power is used rather than uniform sizing with minimum line width.

Devendra Kumar Sharma,et al **[8]** introduced the coupling capacitance (Cc) and mutual inductance (M) among on-chip interconnects. Due to presence of these inductive effects, it is more effective to model the interconnect as distributed RLC transmission line rather than simple RC-one. These parasitic lead to crosstalk noise, propagation delay and power dissipation which affects the signal integrity and degrade the performance of the circuit. Therefore, it is important to investigate the effects of interwire parasitics on crosstalk noise and delay. The effects of mutual inductance and coupling capacitance on delay and

peak overshoot in coupled RLC lines were observed. All results were obtained using SPICE simulation. It was observed that coupling capacitance and mutual inductance had opposite effect on line propagation delay. Furthermore, it was observed that peak overshoot voltage increases with increase in coupling parasitic of line when inputs were switching in same phase. The peak overshoot voltage significantly decreases with the increase in mutual inductance, while it slightly increases with increases in coupling capacitances.

Kaustav Banerjee and Navin Srivastava **[12]** highlighted the thermal problems of Cu interconnects, vias and contacts and examined the advantages as well as the process technology requirements for CNT bundle based vias. ***A. Raychaudhury et al.*****[19]** suggested that CNT interconnect do not offer any performance benefit over copper and hence are not suitable for VLSI.

A. Naeemi **[20]** suggested that CNT bundle interconnects have superior performance over Cu but there were some assumptions. They do not consider the density of nanotubes in CNT bundle nor do they analytically model the equivalent circuit's parameters of CNT bundle interconnects. Realistic drivers/loads are not considered either and the imperfect metal nanotube contact resistance is completely ignored. They also concluded that a flat array of metallic CNT performs better that Cu interconnects.

M.K Rai and S.Sarkar **[1, 10]** reported the effect of tube diameter on delay and power dissipation on CNT bundle interconnect performance and also reveal that the effect of resistance in deep submicron region for both CNT and Copper. It was concluded that resistance of Cu interconnect increases with decrease in technology due to electron migration and grain boundary effect, where as in CNT resistance increases marginally with lower technology.

J.A. Davis, J.D. Meindl **[26-29]** derived the expressions of delay, repeater insertion and peak overshoot for distributed RLC lines, however the CMOS gate was replaced by a single resistor. When an equivalent linear resistor is used in place of CMOS inverter, it leads to inconsistency in results. In the linear region, the transistor can be replaced by a resistor and in the saturation region, the transistor is modeled as a current source with a parallel high resistance.

B K Kaushik et al **[24]** proposed a model consisting of a CMOS gate driving a pi-equivalent circuit and this gate was modeled by an alpha power law model. The analytical expression for output waveform was calculated and compared with SPICE simulation. It was observed that analytical equations and SPICE simulation results closely match each

other for both slow and fast input ramp. The output voltage waveform was calculated for every four regions of operations of transistor.

2.2 Crosstalk Models:

Daniele Rossi et al. **[30]** proposed an RLC equivalent model for CNT bus architecture. The effects of crosstalk on performance are evaluated by simulaton. The result showed that the proposed CNT bus arrangement improves the circuit performance.

D Das and H rahman **[9]** developed an equivalent circuit model to perform the crosstalk analysis. The impact of crosstalk on gate oxide reliability in terms of failure-in-time (FIT) rate was calculated and comparisons were made with copper interconnect. The results showes that the CNT based interconnects are more suitable in VLSI circuits as far as the gate oxide reliability is concerned.

Abinash Roy et al.**[31]** analyzed the effect of capacitive and inductive coupling on interconnect delay and clock skew was analyzed in. The result showed that capacitive coupling and mutual inductance have opposite impact on interconnect delay.

A B Khang aet al **[32]** developed delay model for coupled RC lines and this model was applied along with SPICE simulation to perform various studied related to interconnect delay. It was concluded that delay uncertainty on victim is high for global interconnect as compared to local interconnect.

B K Kaushik and S Sarkar **[33]** proposed a crosstalk model comprising a CMOS gate driving a coupled RLC line that was based on coupled transmission line theory. The output waveform was calculated by using alpha power law model.

D K Sharma et al **[8]** presented the effect of coupling parasitics such as capacitive coupling and mutual inductance on propagation delay and peak overshoot for lox K-dielectric material. The effect of these parasitics was captured by SPICE simulation result. It was observed that capacitive coupling and mutual inductance have opposite impact on interconnect delay.

CHAPTER

3 EQUIVALENT IMPEDANCE PARAMETERS FOR COPPER AND CNT BUNDLE INTERCONNECT

Introduction:

The equivalent impedance parameters of copper and one dimensional CNT bundle as interconnects for VLSI circuit are described in this chapter. The effect of these parameters on interconnect length is analyzed for both copper and CNT bundle interconnect.

3.1 Equivalent Circuit model of Copper interconnect

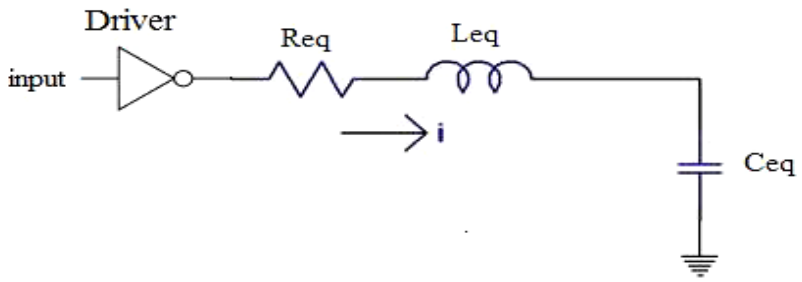

Figure 3.1 Equivalent Circuit model of copper interconnect

According to the model, the thickness of the interconnect is t, the width of interconnect is w, and h is the height of the interconnect above the ground.

3.1.1 Equivalent resistance

Based on this model, the resistance of the copper interconnect of length L is given by following equation-

$$R = \frac{\rho L}{wt}$$

where ρ is the resistivity of copper, w is width and t is thickness.

3.1.2 Equivalent Capacitance

The total effective capacitance of the copper interconnect is given by-

$$C_g = \epsilon\left[\frac{w}{h} + \left\{2.22\left(\frac{s}{s+.7h}\right)^{3.19}\right\} + \left\{1.17\left(\frac{s}{s+1.51h}\right)^{0.76}\left(\frac{t}{t+4.53h}\right)^{0.12}\right\}\right]$$

Where ε is the dielectric permittivity; and ε_r is the relative dielectric permittivity of Copper and is given as-

$\varepsilon = \varepsilon_r \times 8.86 \times 10^{-12}$

Thickness t is determined by t = 3 × W (width of interconnect)

3.1.3 Equivalent Inductance

Inductance associated with copper interconnects is given by the following expression:

$$L_s = \frac{\mu_0 l}{2\pi}\left[\ln\left(\frac{2l}{w+t}\right) + \frac{1}{2} + \frac{.22(w+t)}{l}\right]$$

Where μ_o is the permeability and given as $\mu_o = 4\pi \times 10^{-7}$

3.2 Equivalent Circuit Model for Carbon nanotube

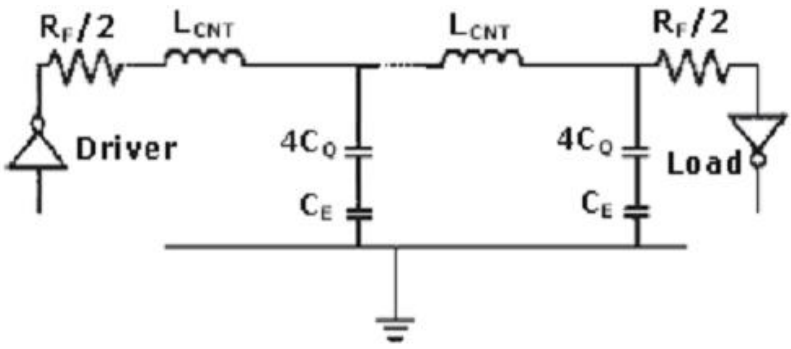

Figure 3.2 Equivalent circuit for an isolated CNT RLC circuit [1, 10]

3.2.1 Resistance of Isolated SWCNT

The resistance of equivalent circuit for length of interconnect (L) is less than mean free of electron (λ_{CNT}) is [1, 8, 9]-

$$Rf = \frac{h}{4e^2}$$

If the length of CNT is greater that mean free path of electron then resistance is given as [1, 8, 9]-

$$R_{CNT} = \frac{h}{4e^2}\frac{L}{L0}$$

The resistance of a CNT has three components: the fundamental resistance R_f, the scattering resistance R_{CNT} and the contact resistance at the two ends of the tube [1, 10].

3.2.2 Capacitance of Isolated SWCNT

CNT has two capacitances of different origins. One is electrostatic capacitance and the other quantum capacitance. The electrostatic capacitance (C_E) is due to charge stored by the CNT- ground plane system and is given by [10]-

$$C_E = \frac{2\pi\epsilon}{ln\,(y/d)}$$

This is per unit length of NanoTube. The quantum capacitance (C_Q) accounts for the quantum electrostatic energy stored in the nanotube when it carries current. It is given as[10]-

$$C_Q = \frac{2e^2}{hv_f}$$

Where v_f is the Fermi velocity. As CNTs have four conducting channels, total effective quantum capacitance resulting from four parallel channels is $4C_Q$. When current flows both C_E and $4C_Q$ carry same charge. Thus the two capacitances appear in series in the isolated SWCNT equivalent circuit.

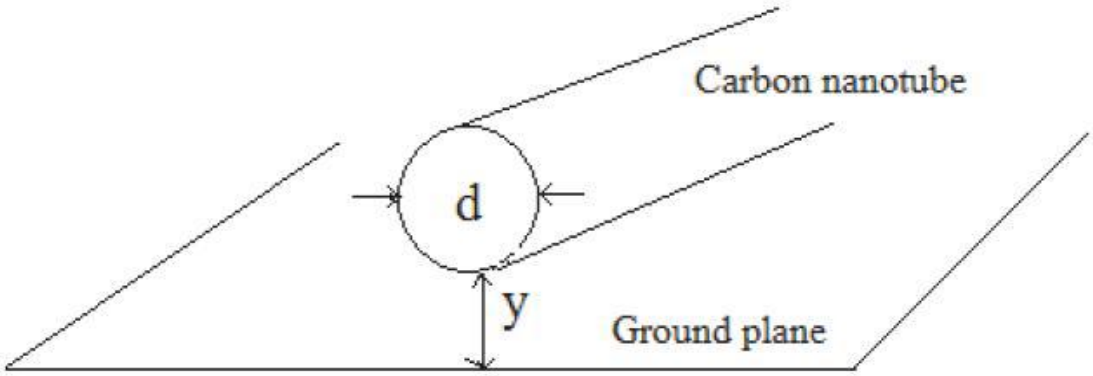

Figure 3.3 Carbon nanotube with diameter‘d’ and, distance ‘y’ below ground [1]

3.2.3 Inductance of an Isolated SWCNT

For a SWCNT, there are two types of inductances termed magnetic inductance and kinetic inductance. Magnetic inductance (L_M) is due to the total magnetic energy resulting from the current flowing in the wire. The kinetic inductance (L_k) arises from kinetic energy stored in each conducting channel of the CNT. The four parallel conducting channels in a CNT results in an effective kinetic inductance of $L_k/4$. The expressions for L_M and L_k are [10] –

$$L_k = \frac{\mu}{2\pi} \ln (y/d)$$

$$L_M = \frac{h}{(v_f)2e^2}$$

3.3 Equivalent Circuit Parameters for a Bundle of SWCNTs

The expressions to calculate the number of CNTs in the bundle are shown in following equations where n_H is the number of "rows" in the interconnect bundle, n_W is the number of "columns" n_{CNT} is the total number of CNTs and denotes the largest integer less than or equal to 'y'.

Number of columns in interconnect bundle is given by[10]-

$$n_W = \left\lfloor \frac{w-d}{s} \right\rfloor$$

Number of rows in interconnect bundle is given by

$$n_H = \left\lfloor \frac{h-d}{\left(\frac{\sqrt{3}}{2}\right)s} \right\rfloor + 1$$

Therefore number of CNT used in the interconnect bundle is given by the following equations [1,10].

If number of rows n_H in the CNT bundle is even, the number of CNT used is given by

$$n_{CNT} = n_W n_H - \frac{n_H}{2}$$

If number of rows n_H in the CNT bundle is odd, the number of CNT used is given by

$$n_{CNT} = n_W n_H - \frac{n_H - 1}{2}$$

3.3.1 Resistance of CNT bundle:

In order to calculate the effective resistance of a CNT bundle, it is assumed that all CNTs packed into the interconnect structure are metallic and conducting. The CNT-bundle resistance is then given by following Equation:

$$R_{CNT}(bundle) = \frac{h}{4e^2}\frac{L}{L_0}/n_{CNT}$$

where n_{CNT} is the total number of CNTs forming the bundle[1,10].

3.3.2 Capacitance of CNT bundle:

CNT bundle is given by-

$$C(bundle) = \frac{C_E^{\ bundle}.C_Q^{\ bundle}}{C_E^{\ bundle} + C_Q^{\ bundle}}$$

Where-

$$C_E^{bundle} = 2C_{En} + \frac{n_W - 2}{2} C_{Ef} + \frac{3(n_H - 2)}{5} C_{En}$$

Where C_{En} and C_{Ef} are the intrinsic plate capacitances calculated for an isolated CNT over a ground plane[1,10].

C_{En} is calculated assuming the ground plane to be at a distance equal to the separation distance ‘s’from the adjacent interconnect [10]-

$$C_{En} = \frac{2\pi\epsilon}{\ln\left(\frac{s}{d}\right)}$$

C_{Ef} is calculated assuming the ground plane to be at a distance equal to the separation distance‘s+w’ from the “far” adjacent interconnect.

$$C_{Ef} = \frac{2\pi\epsilon}{\ln\left(\frac{s+w}{d}\right)}$$

Quantum capacitance of the bundle is given by the following expression:

$$C_Q^{bundle} = C_Q^{CNT}.n_{CNT}$$

3.3.3 Inductance of CNT Bundle

The inductance of a CNT bundle is given by the parallel combination of the inductances corresponding to each CNT forming the bundle.

The inductance of CNT bundle is given by [1, 6, 10]:

$$L(bundle) = \frac{L_M + (L_K/4)}{n_{CNT}}$$

3.4 Impedance analysis of SWCNT bundle interconnect

The effect of impedance parameters (R, L, C) on interconnect length are shown in Fig.3.4.The circuit impedance parameters are calculated from the models available in [10, 12]. Table 3.1, 3.2 and 3.3 show the comparison of impedance parameters for both SWCNT bundle and copper interconnect. Fig. 3.4(a), 3.4(b) and 3.4(c) show that the value of impedance parameters R, L, C increases with increase in interconnect length.

Table 3.1 Comparison of CNT bundle and copper resistance at different length of interconnect.

	Resistance(ohm)	
Length of Interconnect (µm)	CNT	Cu
100	83.56	509.25
400	334.24	2037.04
700	584.92	3564.814
1000	835.601	5092.59

Table 3.2 Comparison of CNT bundle and copper inductance at different length of interconnect.

	Inductance	
Length of Interconnect (µm)	CNT (fH)	Copper(pH)
100	26.4	148.98
400	48.7	706.79
700	85.31	1315.24
1000	121.8	1950.24

Table 3.3 Comparison of CNT bundle and copper capacitance at different length of interconnect.

	Capacitance	
Length of Interconnect (µm)	CNT(pF)	Copper(fF)
100	0.82	1.69
400	1.53	6.79
700	2.67	11.874
1000	3.82	16.96

Table 3.4 Impedance parameters at different length for CNT bundle interconnect

length(um)	R(ohm)	L(f)	C(p)
400	335.6	48.7	1.53
500	417.6	60.94	1.91
600	501.8	73.13	2.29
700	584.3	85.31	2.67
800	668.4	97.54	3.062
900	752.1	109.69	3.44
1000	835.6	121.88	3.85

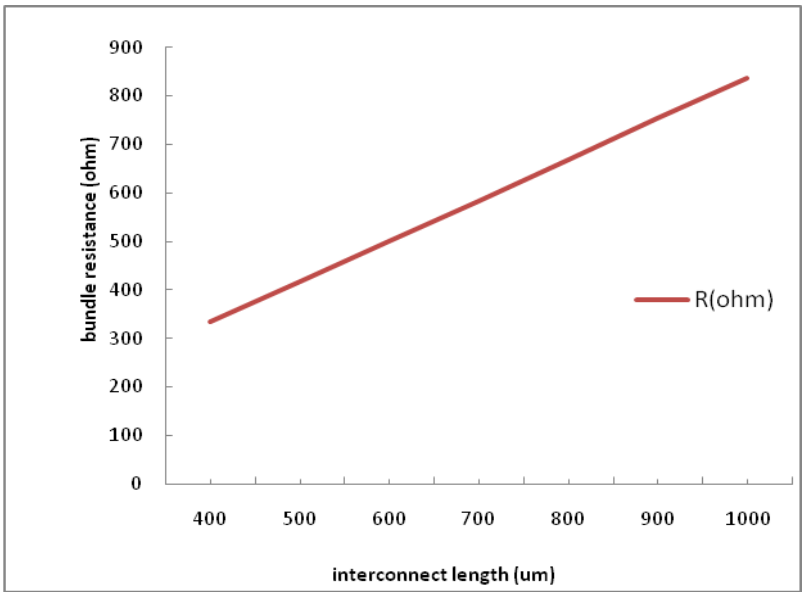

Figure 3.4 (a). Variation of bundle resistance as a function of interconnect length at 32 nm technology node.

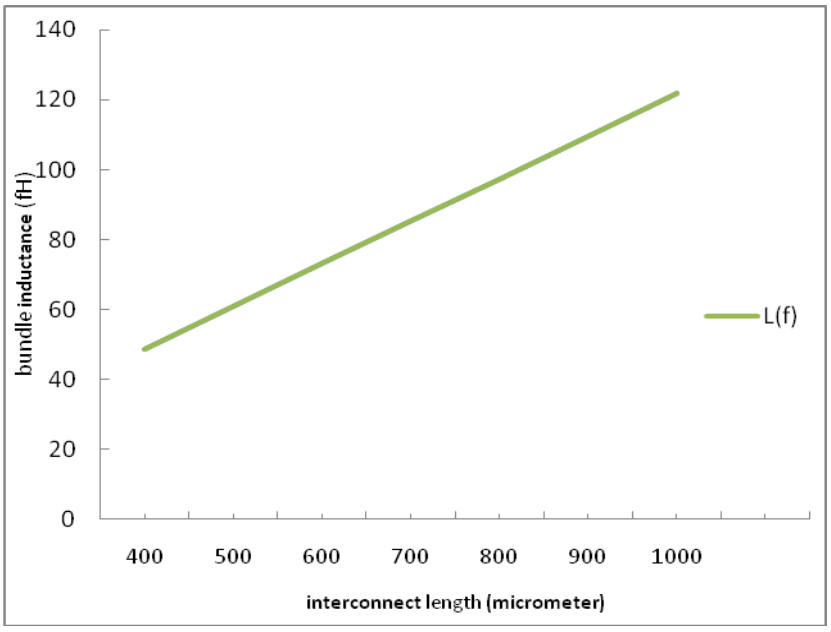

Figure 3.4 (b) Variation of bundle inductance as a function of interconnect length at 32 nm technology node

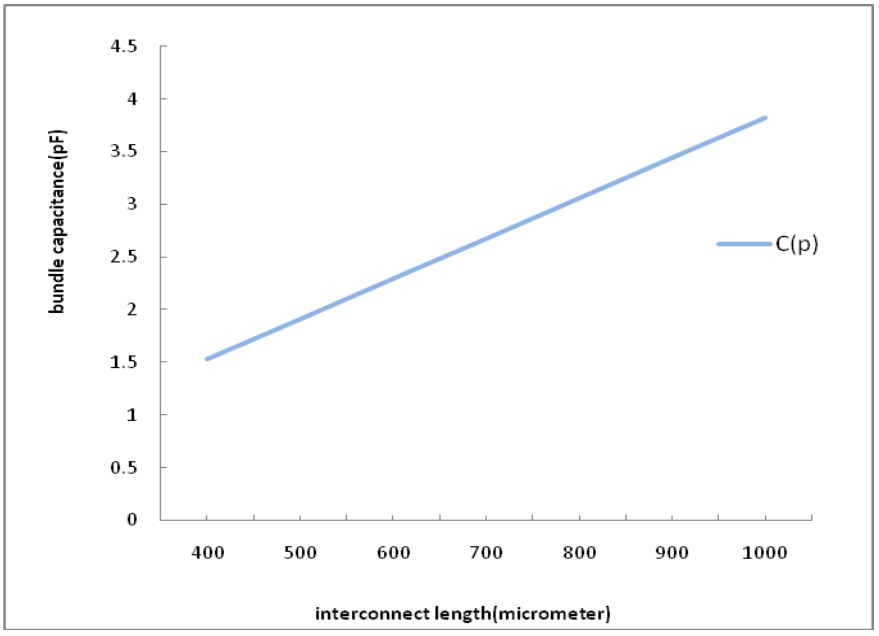

Figure 3.4(c) Variation of bundle capacitance as a function of interconnect length at 32 nm technology node.

CHAPTER

4 ANALYTICAL MODEL OF INTERCONNECT

Introduction:

A model is developed to calculate equivalent circuit parameters for a SWCNT bundle interconnect. Using this model, the performance of SWCNT bundle interconnects at global level is analyzed. For analytical model equivalent resistance, capacitance and inductance are calculated using equations given in previous chapter for SWCNT bundle interconnect. Using these parasitic, the output waveform for an L-segment RLC is derived using alpha power law model. This analytical output waveform is compared with SPICE simulation result for both copper and CNT bundle interconnect.

4.1 Interconnect Models:

4.1.1 The Lumped RC Model

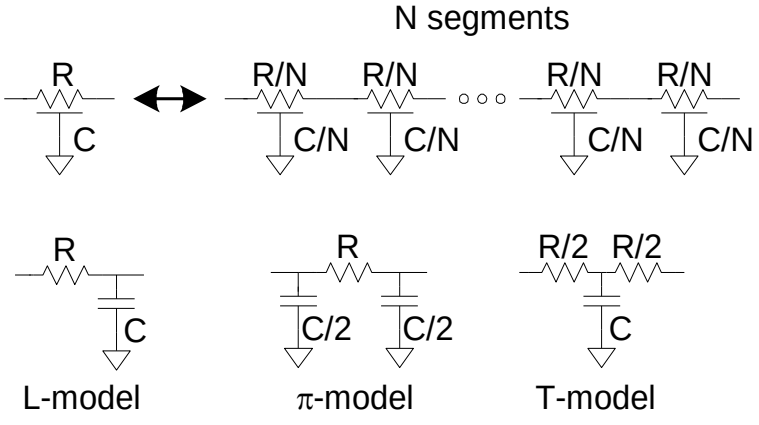

Figure 4.1 Different configuration of RC interconnect models

Figure 4.1 shows the different configuration of RC interconnect models. For making distributed RC model resistance and capacitance can be divided into equal segments.

4.1.2 Distributed RLC model

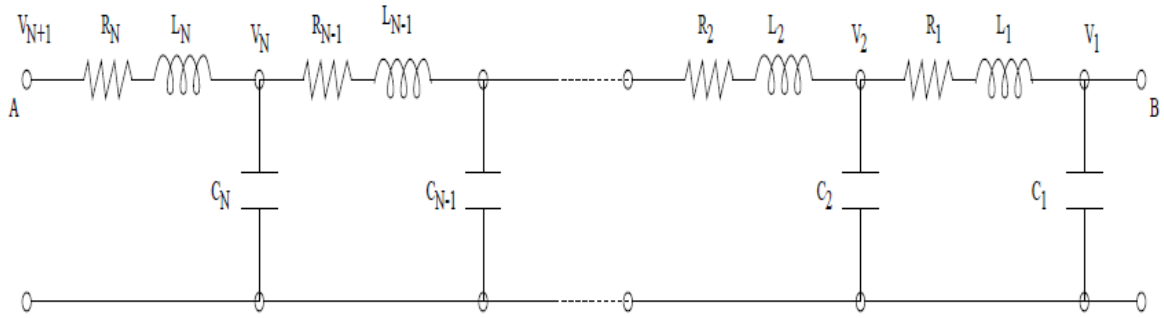

Figure 4.2 Distributed RLC model with N-segments [21]

The distributed RLC line can be approximated by a lumped multi-stage RLC ladder network and individual element is given by-

$$R_N = \frac{R}{N}, \quad L_N = \frac{L}{N}, \; C_N = \frac{C}{N}$$

where R, L and C are the total resistance, inductance and capacitance respectively.

4.1.3 Pi- Model

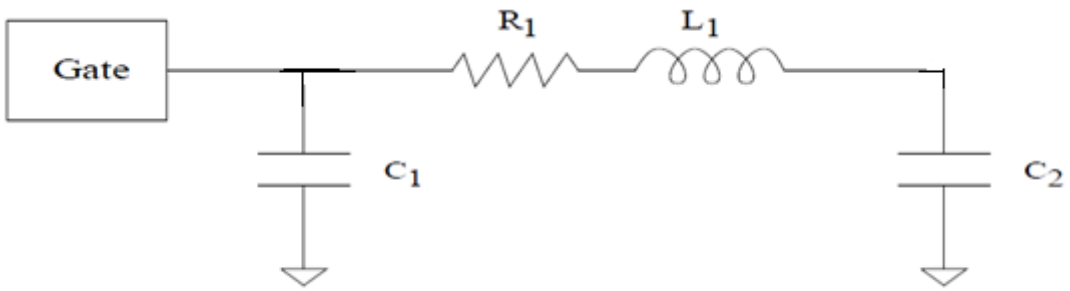

Figure 4.3 Pi model for CNT interconnect [21]

The impedance for above RLC-π model is given as-

$$R_{eq} = \left(R_1 + sL_1 + \frac{1}{sC_2}\right) || \frac{1}{sC_1}$$

So, driving point admittance is given as-

$$Y_{eq} = \frac{1}{R_{eq}}$$

$$Y_{eq} = sC_1 + \frac{sC_2}{1+sC_2(R_1+sL_1)} \quad (1)$$

$$Y_{eq} = sC_1 + sC_2\left(\left(1 + sC_2(R_1 + sL_1)\right)^{-1}\right)$$

By expanding above equation we get-

$$Y_{eq} = s(C_1 + C_2) - s^2R_1C_2^2 + s^3(R_1^2C_2^3 - L_1C_2^2) + \cdots \quad (2)$$

Similar to the driving point admittance approximation for the RLC interconnect tree, we approximate the entire RLC tree with an equivalent open-ended RLC line whose resistance, inductance and capacitance are equal to the total interconnect resistance, inductance and capacitance as shown in fig 4.4. The admittance of an open ended RLC line can be obtained as [21]-

$$Y(s) = \frac{tanh\theta}{Z_0}$$

where propagation constant $\theta = \sqrt{(R_t + sL_t)sC_t}$ and characteristics impedance $Z_0 = \sqrt{\frac{R_t+sL_t}{sC_t}}$

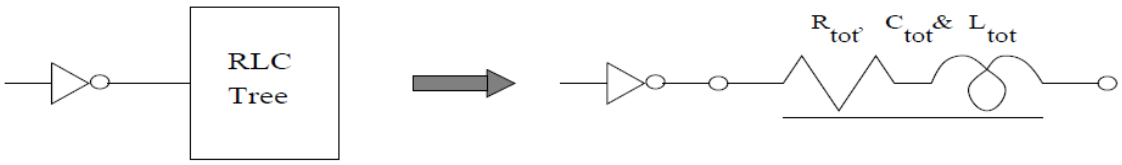

Figure 4.4 An open-ended RLC line to capture RLC interconnect tree [21]

So Y(s) can be written as-

$$Y(s) = sC_{tot} - \frac{s^2R_{tot}C_{tot}^2}{3} + s^3\left(\frac{2R_{tot}^2C_{tot}^3}{15} - \frac{L_{ott}C_{tot}^2}{3}\right) + \cdots \quad (3)$$

The general expression for driving point admittance is given by [20]-

$$Y(s) = \sum_{i=1}^{\infty} A_i s^i$$

$$Y(s) = sA_1 + s^2A_2 + s^3A_{3+} \ldots\ldots \quad (4)$$

By comparing equations (3) and (4)-

$$A_1 = C_{tot},\ A_2 = -\frac{R_{tot}C_{tot}^2}{3},\ A_3 = \frac{2R_{tot}^2C_{tot}^3}{15} \qquad (5)$$

By comparing equations (2) and (4)-

$$A_1 = C_1 + C_2,\ \ A_2 = -R_1C_2^2, A_3 = R_1^2C_2^3 \qquad (6)$$

The inductance parameter of the π-model can be obtained by matching the inductive term in the third moment of the driving point admittance. From equation (6) the values of R_1, C_1 and C_2 can be obtained as-

$$R_1 = -\frac{A_3^2}{A_2^3} \quad C_1 = A_1 - \frac{A_2^2}{A_3} \quad C_2 = \frac{A_2^2}{A_3} \qquad (7)$$

Putting the values of A_1, A_2 and A_3 in equation (7), we can find the values of resistance, inductance and capacitances and these are given below-

$$R_1 = \frac{12}{25}R_{tot},\ L_1 = \frac{12}{25}L_{tot},\ \ C_1 = \frac{1}{6}C_{tot},\ C_2 = \frac{5}{6}C_{tot}$$

The pi-model obtained by these values is shown in figure-

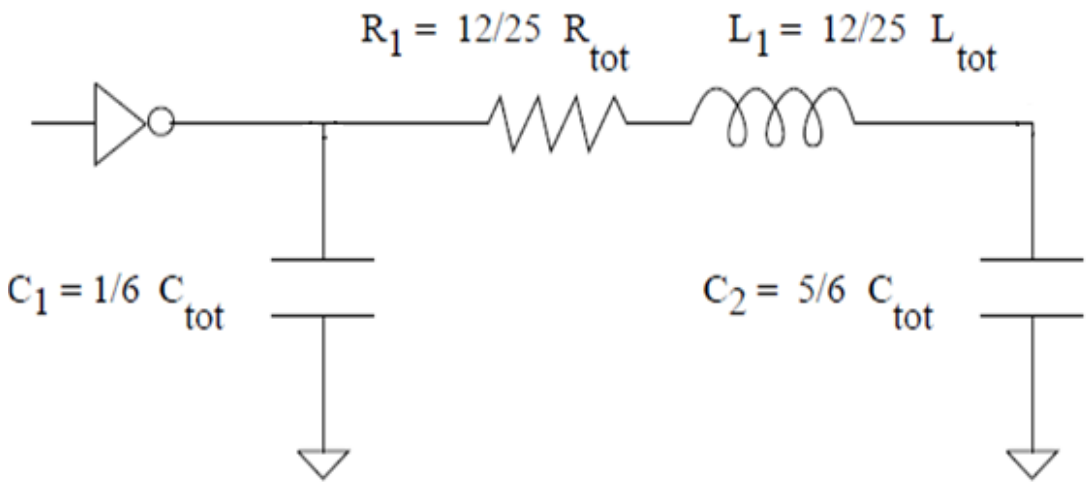

Figure 4.5 An RLC π-model [21]

The resistance, capacitance and inductance reduce in case of π-model that results the decrease in delay. So π -model is better than distributed model of interconnect.

4.2 Piecewise Transient Analysis for L-segment RLC:

A CMOS inverter with L segment RLC circuit of 1mm length of interconnect is shown in fig.4.6. The alpha-power law model [23] is used to represent the transistor current. The drain current is given in following equation for different regions of operations-

$$I_d = \begin{cases} 0; & V_{GS} \le V_{To} : cut-off\ region \\ k_l(V_{GS} - V_{TO})^{\alpha/2} V_{DS}; & V_{DS} < V_{DSAT} : linear\ region \\ k_s(V_{GS} - V_{TO})^{\alpha}; & V_{DS} \ge V_{DSAT} : saturation\ region \end{cases}$$

Here α is called velocity saturation index; k_l, k_s are the transconductance parameters in linear and saturation region of the transistor respectively, V_{DSAT} is drain-saturation voltage and V_{To} is threshold voltage at zero bias.

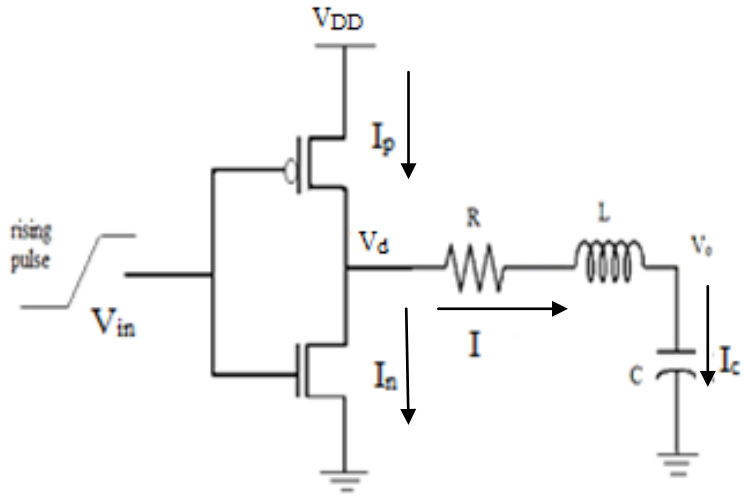

Figure 4.6 An equivalent model of CMOS gate driving L segment RLC circuit of interconnect.

In this case the analytical expression for output voltage is obtained in different four regions of operations of the transistor for fast input ramp [24].

Applying KCL at drain of nmos-

$$I_n + I - I_p = 0 \qquad (1)$$

An analytical expression for output voltage is calculated for rising input ramp. During rising input ramp, output node is discharged that means nmos transistor will be conducting. So during rising transition, the effect of pmos transistor can be neglected due to short circuit current [24] ($I_p = 0$).

So from equation (1)- $I_n + I = 0$ (2)

Region 1 ($0<t<t_1$): The nmos transistor is in cut off during this region. This region extends until time t_1, when $V_{GS} = V_{To}$. So putting $I_n = 0$, equation (2) reduces to-

$$I = 0,\ I_c = 0, C\frac{dV_o}{dt} = 0$$

Here initial condition is- $V_o(0) = V_{DD}$

The output V_o remains V_{DD} upto time t_1.

Region 2 ($t_1<t<\tau$): During this region nmos operates in saturation region. Here τ is the rise time of input pulse. The current through nmos transistor during saturation region is given as-

$$I_n = k_s(V_{GS} - V_{To})^{\alpha}$$

$$I_n = k_s\left(\frac{V_{DD}}{\tau}t - V_{To}\right)^{\alpha}$$

From equation (2)-

$$k_s\left(\frac{V_{DD}}{\tau}t - V_{To}\right)^{\alpha} + I = 0$$

$$k_s\left(\frac{V_{DD}}{\tau}t - V_{To}\right)^{\alpha} + C\frac{dV_o}{dt} = 0 \quad (3)$$

$$here\ k_s = \frac{I_{DO}}{(V_{DD}-V_{TH})^{\alpha}}$$

To solve equation (3), the term including α is solved using second order taylor series expansion at t=τ/2 (here $V_{in}=V_{DD}/2$) as-

$$\frac{k_s\left(\frac{V_{DD}}{\tau}t - V_{To}\right)^{\alpha}}{C} = a_o + a_1 t + a_2 t^2$$

So the solution of differential equation (3) is as -

$$V_o(t) = K - a_o t - \frac{a_1}{2}t^2 - \frac{a_2}{3}t^3$$

Here K is integration constant and value of K is calculated using initial condition $V_o(0)=V_{DD}$

Region 3 ($\tau<t<t_2$): At this region the input ramp has reached its final value and nmos transistor is still operates in saturation region. The current through nmos transistor is given as [23]-

$$I_n = k_s(V_{DD} - V_{To})^{\alpha}$$

Now differential equation becomes-

$$C\frac{dV_o}{dt} + k_s(V_{DD} - V_{To})^{\alpha} = 0 \qquad (4)$$

The solution of above differential equation is-

$$V_o(t) = K_1 - K_2 t$$

Here K_1 is integration constant and

$$K_2 = \frac{k_s}{C}(V_{DD} - V_{To})^{\alpha}$$

The nmos transistor exits saturation at time t_2. Time t_2 is calculated by equating drain-source voltage and drain-saturation voltage of nmos transistor [23].

$$V_d(t_2) = V_{DSAT}$$

$$RI + L\frac{dI}{dt} + V_o = V_{DSAT} \qquad (5)$$

Here $I = C\frac{dV_o}{dt}$ and $V_{DSAT} = \frac{k_s}{k_l}(V_{GS} - V_{TN})^{\alpha/2}$

Region 4 ($t>t_2$): During this region nmos transistor operates in linear region and current through the transistor is given as-

$$I_n = k_l(V_{DD} - V_{To})^{\alpha/2}V_d$$

Now differential equation becomes-

$$C\frac{dV_o}{dt} + k_l(V_{DD} - V_{To})^{\alpha/2}\, V_d = 0 \qquad (6)$$

Here $V_d = RI + L\frac{dI}{dt} + V_o$

k_l is calculated by $I_{DS} - V_{DS}$ characteristics of transistor and is given as [23]-

$$k_l = \frac{I_{Do}}{V_{Do}(V_{DD} - V_{TH})^{\alpha/2}}$$

Equation (6) becomes-

$$\frac{d^2V_o}{dt^2}\left(LCk_l(V_{DD} - V_{To})^{\alpha/2}\right) + \frac{dV_o}{dt}\left(C + RCk_l(V_{DD} - V_{To})^{\alpha/2}\right) + k_l(V_{DD} - V_{To})^{\alpha/2}V_o = 0$$

So the solution of differential equation (6) is-

$$V_o(t) = 0.45 * \frac{\left(-K_2 * \sqrt{M} - K_2^2 + 4 * K_3 * K_1\right)}{-M} e^{-(K_2 - \sqrt{M})t/2 * K_1} + 0.45 * \frac{\left(K_2 * \sqrt{M} - K_2^2 + 4 * K_3 * K_1\right)}{-M} e^{-(K_2 + \sqrt{M})t/2 * K_1}$$

Here

$K_1 = LCk_l(V_{DD} - V_{To})^{\alpha/2}, K_2 = \left(C + RCk_l(V_{DD} - V_{To})^{\alpha/2}\right)$

$K_3 = k_l(V_{DD} - V_{To})^{\alpha/2}$ *And* $M = K_2^2 - 4 * K_3 * K_1$

4.3 Waveform Analysis:

On the basis of parasitic explained with equations in previous chapter the equivalent resistance, capacitance and inductance of copper and CNT bundle is determined. With variation in length and width of interconnect, variation in resistance, capacitance and inductance of global interconnect is observed with the help of graph. In SWCNT, for both distributed and Pi-model 90% delay is calculated from the SPICE simulation result. Simulation is carried out at frequency 0.1GHz.

Table 4.1 ITRS 2005 based parameters for calculation at 32 nm technology [1]

Parameters	CNT	Cu
Vdd	0.9	0.9
Width(w) of global interconnect	48nm	48nm
Aspect ratio (global)	3	3

Thickness(H) of global interconnect	144nm	144nm
Width(w) of local and semi global interconnect	32nm	32nm
Aspect ratio (local)	2	2
Diameter	1nm	1nm
Length(L)	1000um	1000um
ILD thickness	110.4nm	110.4nm
Separation(s) between adjacent bundle of global interconnect	48nm	48nm
Separation(s) between adjacent bundle of local interconnect	32nm	32nm
ε (relative)	2.25	2.25

4.3.1 Comparison of analytical an simulation model

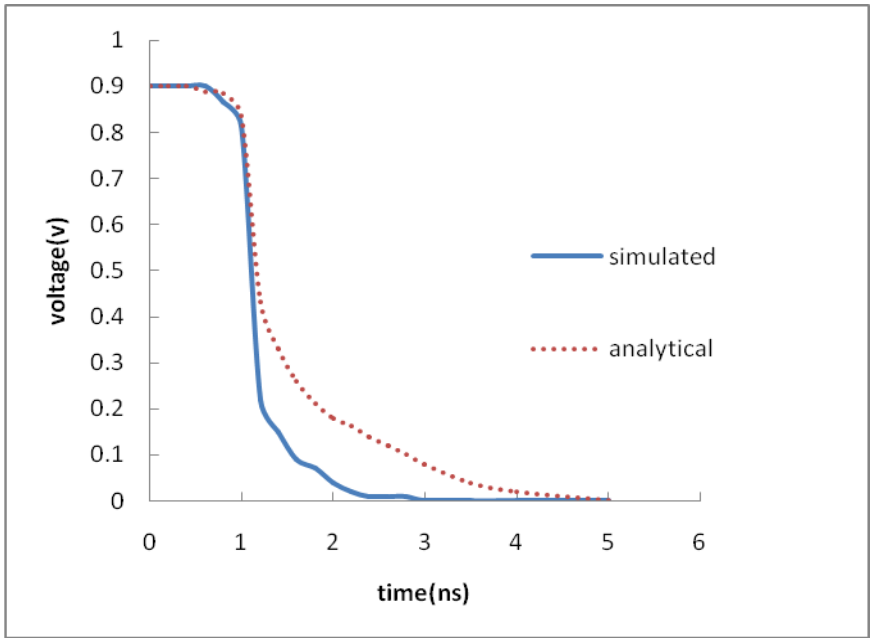

Figure 4.7 Comparison of analytical and simulated result of L segment RLC line for rising input pulse.

Figure 4.7 shows the transient response of CNT bundle for 1mm length of interconnect. The above graph reflect the difference between analytical and simulation result of L segment RLC circuit of 1mm length of interconnect. It is observed that for fast ramp

input signal, analytical result in terms of output voltage accurately matched with simulation in saturation and some deviation is found in linear region.

4.3.2 Delay Analysis

CNT and Copper delay is determined by using the parasitic discussed in previous chapter. The above resistance, inductance and capacitances are used for calculation of delay for different models of interconnects. By performing transient analysis by Tanner EDA tool at 32nm technology at 0.1GHz frequency, delay is determined for bundled CNT and copper interconnect.

a) Delay Analysis of distributed model

i) Delay analysis for different number of repeaters

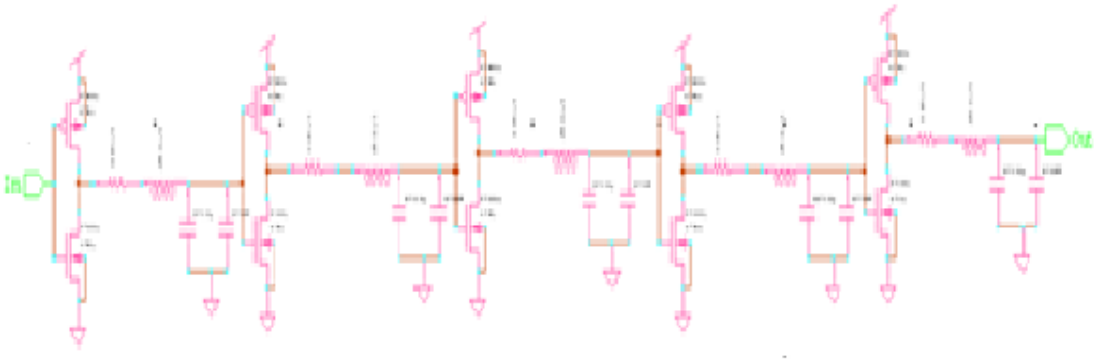

Figure 4.8 Distributed RLC model with 4 repeaters

Table 4.2 Delay of CNT bundle with variation in number of repeaters

Number of repeaters	Delay (ns)
4	1.9
6	1.5
8	1.29
10	1.15

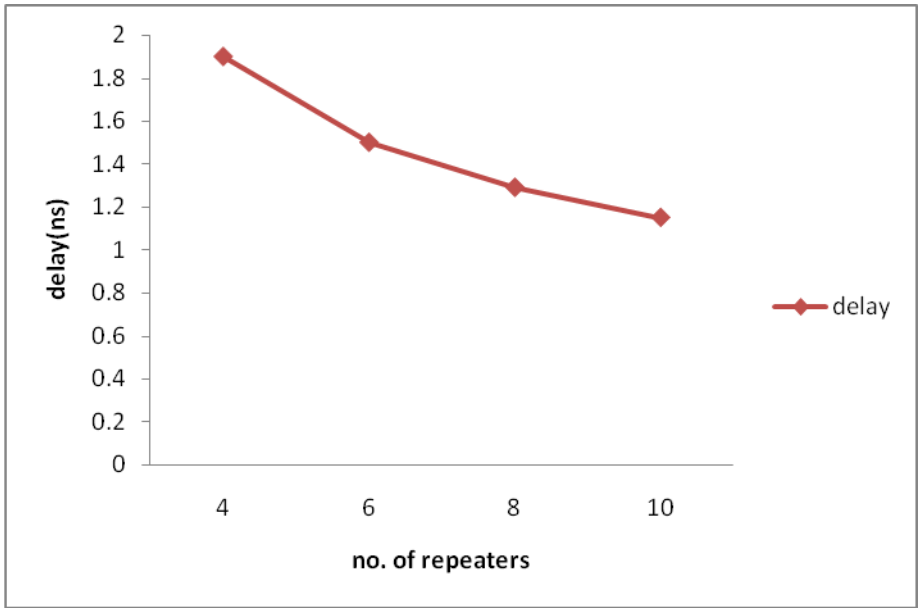

Figure 4.9 Number of repeaters versus delay

Figure 4.9 reveals the delay as function of repeater. This graph shows that delay reduces with increase in number of repeaters. This is because the use of repeaters makes time delay linear with length by dividing the interconnect into smaller subsections, resulting the decrease in RC delay.

ii) Delay analysis of CNT interconnect at different W/L with different number of repeaters

Table 4.3 Delay of CNT bundle with variation in repeaters and size of driver transistor

Size of driver transistor	Delay (ns)			
	Repeater 4	Repeater 6	Repeater 8	Repeater 10
30	2.1	1.82	1.58	1.2
40	1.9	1.6	1.35	1.15
50	1.6	1.34	1.08	1.02
60	1.44	1.1	0.96	0.85
70	1.34	1.015	0.84	0.72
80	1.2	0.95	0.76	0.68

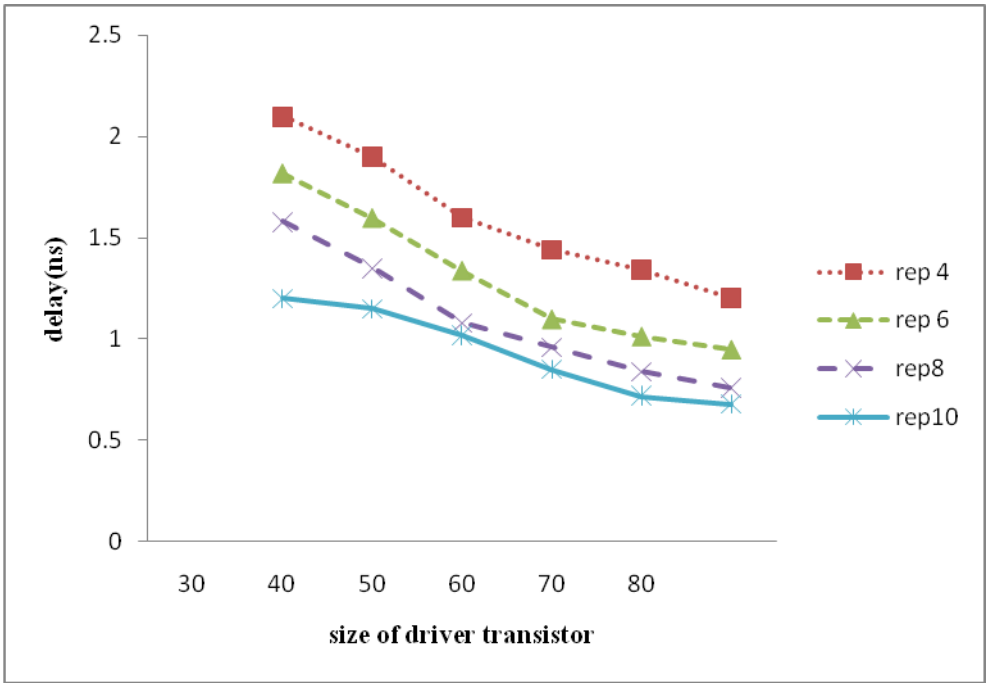

Figure 4.10 Size of driver transistor versus delay at different repeaters

Figure 4.10 shows the delay as a function of driver size for different number of repeaters. It shows that delay can be reduced by increasing the size of driver transistor and also by increasing the number of repeaters. The resistance of the driver transistor decreases with increase in size of driver transistor which results a decrease in propagation delay.

b) Delay Analysis of Pi Model

i) Pi model with different number of repeaters

Table 4.4 Delay with variation in size of driver transistor and number of repeaters

Size of driver transistor	Delay (ns)	
	Repeater 2	Repeater 4
40	1.76	1.58
50	1.5	1.26
60	1.35	1.14
70	1.21	1.03
80	1.15	0.94

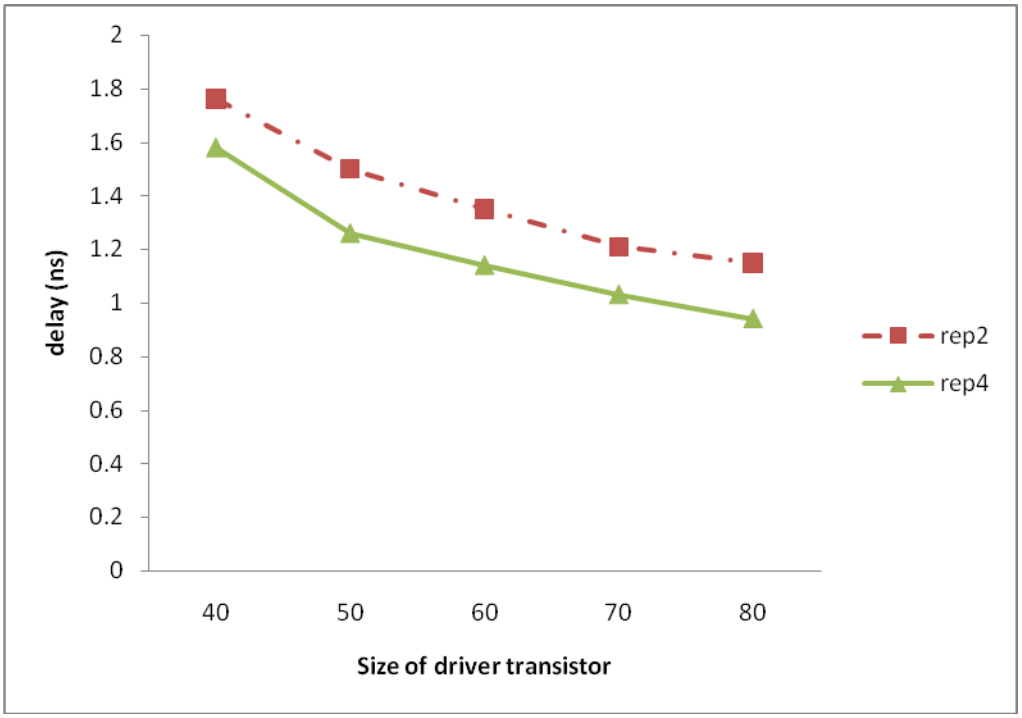

Figure 4.11 Size of transistor versus delay at different repeaters for pi model

Figure 4.11 shows the delay as a function of size of driver transistor at different number of repeaters for Pi-RLC model of interconnect. It reveals that delay can be reduced by both increasing the size of the driver transistor and number of repeaters.

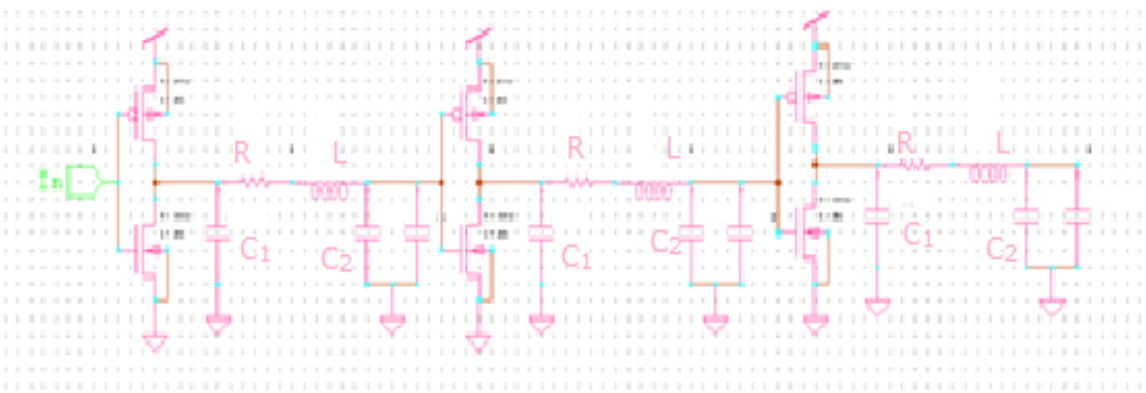

Figure 4.12 RLC-Pi model of Interconnect with 2 repeaters

c) Comparison

i) Comparison of distributed model and Pi-model for CNT

Table 4.5 Comparison of delay of distributed and Pi model at different W/L

Size of driver transistor	Delay (ns)	
	Distributed model	Pi model
30		1.84
40	1.9	1.58
50	1.6	1.26
60	1.44	1.14
70	1.34	1.03
80	1.2	0.94

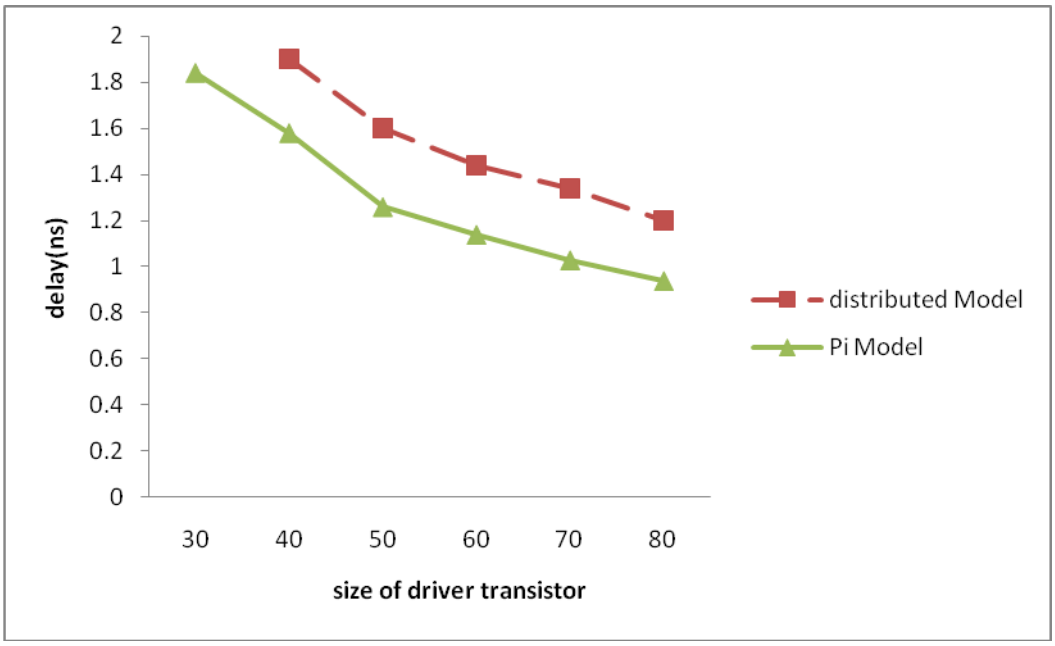

Figure 4.13 Delay comparison of distributed and pi model

Figure 4.13 shows the delay comparison between distributed and Pi model of CNT bundle interconnect. It can be observed that delay in case of Pi-model is much less than the delay in case of distributed model because impedance parameters are decreased in case of Pi model. So it can be concluded that Pi-model of interconnect gives better performance than the distributed model.

ii) Comparison CNT and Copper interconnect

Table 4.6 Comparison of Pi and distributed models of Cu and CNT

Size of driver transistor	Delay (ns)			
	Cu distributed model	Cu pi model	CNT distributed model	CNT pi model
40	2.91	2.1	1.9	1.58
50	2.8	2	1.6	1.26
60	2.75	1.915	1.44	1.14
70	2.74	1.88	1.34	1.03
80	2.72	1.842	1.2	0.94

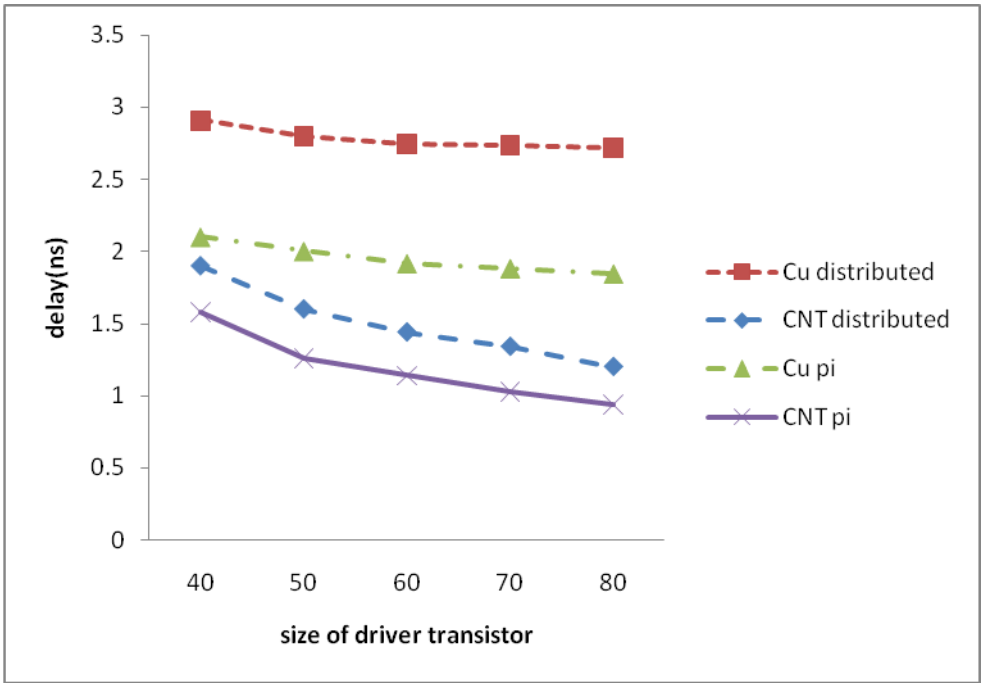

Figure 4.14 Comparison of models of CNT and Cu interconnect

Figure 4.14 shows the comparison of distributed and Pi model of CNT bundle and copper interconnect. The graph tells that delay in case of CNT bundle interconnects is less than copper interconnect for both distributed and Pi-model. So it can be concluded that use of CNT bundle interconnects increase the performance of circuit.

4.3.3 Effect of interconnect length on bundle SWCNT delay

The circuit considered for analysis [5, 10] comprise a CMOS-inverter driving a distributed RLC model of interconnect. A load capacitance of 10fF terminates the interconnect and 0.1Ghz pulse of 1ns rise time provides input to the CMOS inverter. The performance of this setup is studied by SPICE simulation in 32nm technology node with Predictive technology model(PTM)[34] and optimum number of repeaters are used.

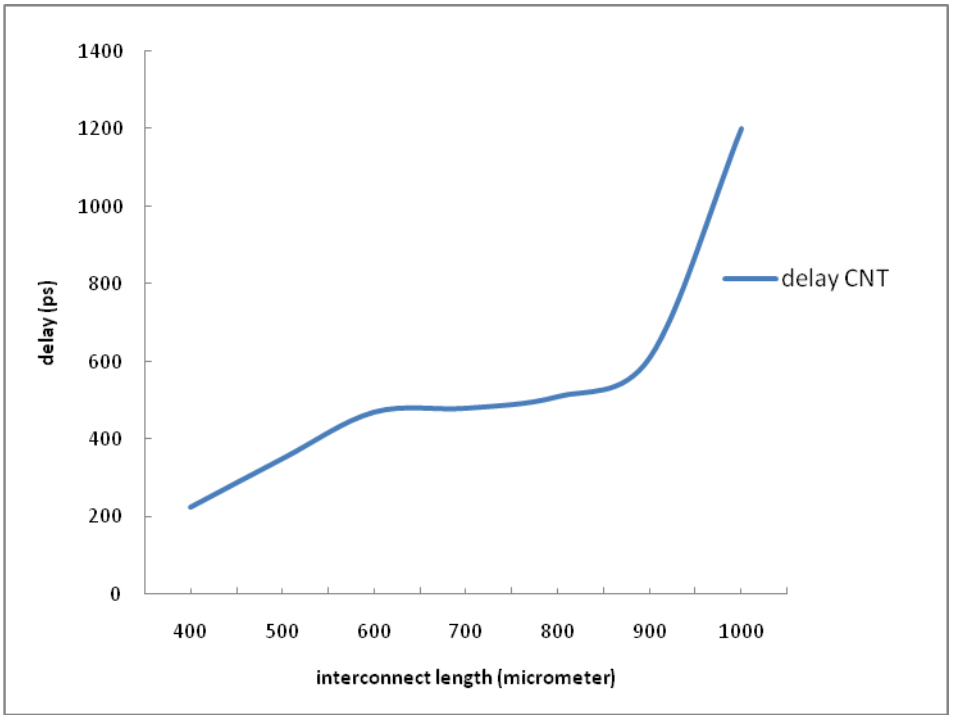

Figure 4.15 Variation of 90% average delay of SWCNT bundle as a function of interconnect length

90% average delay is illustrated in fig.4.15 as a function of interconnect length. Result shows that 90% average delay increases with length of interconnect. The increase of normalized delay indicates dominance of CNT bundle resistance over its capacitance.

CHAPTER 5

CROSSTALK ANALYSIS

Introduction:

Crosstalk is the unwanted noise or unwanted output produced at the output node. Crosstalk is due to capacitive and inductive coupling between adjacent interconnect lines. Crosstalk induce signal delay, overshoot, undershoot and glitches in the victim [8]. Crosstalk harmfully affects the circuit operating at high frequencies (GHz range). Crosstalk induces two types of faults: glitch fault and delay fault. Glitch occurs when the victim line is proposed to be at stable state and a noise pulse occurs on the net.

In this chapter the output waveform for coupled RLC interconnect is derived in which an input pulse is applied at the resistor. The analytical expression for the output waveform is obtained for capacitive coupling and alpha power law model is used to model the transistor.

5.1 Capacitive coupling and mutual inductance:

Capacitive coupling refers to transfer of energy within an electrical network by means of capacitance between two nodes.

$$C_c = \varepsilon \left[1.14 \frac{t}{s} \left(\frac{h}{h+2.06s} \right)^{0.09} + 0.74 \left(\frac{w}{w+1.59s} \right)^{1.14} + 1.16 \left(\frac{w}{w+1.87s} \right)^{0.16} \left(\frac{h}{h+0.98s} \right)^{1.18} \right]$$

Here t is thickness of wire, s is separation, h is distance from ground, w is width of interconnect and ε is dielectric constant.

Inductive coupling between two conductors occur when change in current flow through one wire induces a voltage across the end of other wire. The amount of inductive coupling is measured by mutual inductance.

$$M = \frac{\mu_0 L}{2\pi}\left[ln\left(\frac{2L}{d}\right) - 1 + \frac{d}{L}\right]$$

Here L is interconnect length and d is diameter.

5.2 Crosstalk analysis in RLC interconnect with input pulse:

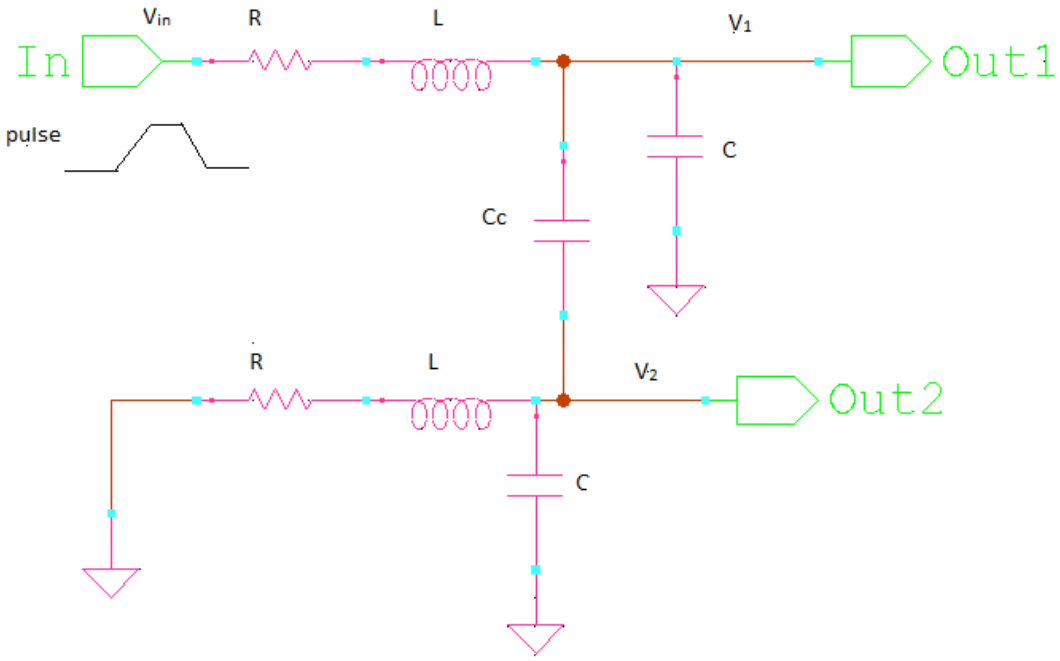

Figure 5.1 Crosstalk RLC model with input pulse

KCL at V_1-

$$\frac{V_1(s) - V_{in}(s)}{R + sL} + \frac{V_1(s)}{X_C} + \frac{V_1(s) - V_2(s)}{X_{Cc}} = 0 \qquad (1)$$

KCL at V_2-

$$\frac{V_2(s)}{R + sL} + \frac{V_2(s)}{X_C} + \frac{V_2(s) - V_1(s)}{X_{Cc}} = 0 \qquad (2)$$

From eqn (1)-

$$V_1(s) = \frac{\frac{V_2(s)}{X_{Cc}} + \frac{V_{in}(s)}{R + sL}}{sC + sC_c + \frac{1}{R + sL}}$$

$$V_1(s) = \frac{V_{in}(s) + sC_c(R+sL)V_2(s)}{1 + s(R+sL)(C+C_c)}$$

Putting the value $V_1(s)$ in equation (2)-

$$V_2(s)\left[sC + sC_c + \frac{1}{R+sL}\right] = sC_c\left[\frac{V_{in}(s) + sC_c(R+sL)V_2(s)}{1 + s(R+sL)(C+C_c)}\right]$$

$$V_2(s)\left[sC + sC_c + \frac{1}{R+sL}\right] = \frac{sC_cV_{in}(s)}{1 + s(R+sL)(C+C_c)} + \frac{s^2C_c^2(R+sL)V_2(s)}{1 + s(R+sL)(C+C_c)}$$

Here R=835.6 ohm

L=121.8f

C=3.85p

C_c=82.1f

$$V_2(s) = V_{in}(s)\left[\frac{0.68 * 10^{-10}s + 0.99 * 10^{-26}s^2}{0.219 * 10^{-48}s^4 + 0.312 * 10^{-32}s^3 + 0.107 * 10^{-16}s^2 + 0.65 * 10^{-8}s + 1}\right]$$

$$V_2(s) = V_{in}(s)\left[\frac{s(s + 0.68 * 10^{16})}{(s + 0.303 * 10^9 - 0.364 * 10^{16}i)(s + 0.65 * 10^{16})(s + 0.72 * 10^{16})(s + 0.303 * 10^9 + 0.364 * 10^{16}i)}\right]$$

$$V_2(t) = L^{-1}(V_2(s))$$

$$V_2(t) = V_{in}(t)[(5.67 * 10^{-17} - 0.300 * 10^{-17}i)e^{(-0.303*10^9 + 0.36*10^{16}i)t} + (-5.019 * 10^{-17} - 3.2710^{-33}i)e^{0.65*10^{16}t} - 6.32 * 10^{-17}e^{-0.72*10^{16}t} + (5.67 * 10^{-17} + 0.300 * 10^{-17}i)e^{(-0.303*10^9 - 0.364*10^{16}i)t}]$$

5.3 Crosstalk Analysis in Pi-Model:

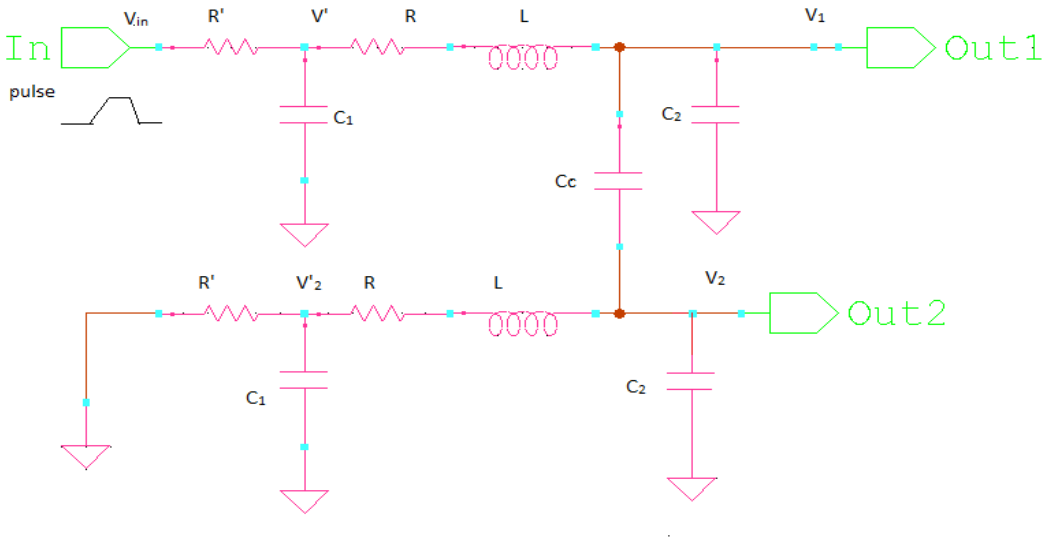

Figure 5.2 Crosstalk model with Pi-RLC segment

Applying KCL at V'-

$$\frac{V'(s)-V_{in}(s)}{R'}+\frac{V'(s)-V_1(s)}{R+X_L}+\frac{V_1(s)}{X_{c1}}=0 \qquad (3)$$

Applying KCL at V_1-

$$\frac{V_1(s)-V'(s)}{R+X_L}+\frac{V_1(s)-V_2(s)}{X_{Cc}}+\frac{V_1(s)}{X_{c2}}=0 \qquad (4)$$

From equation (3) and (4)-

$$V_1(s)\left[\frac{1}{R+X_L}+\frac{1}{X_{c2}}+\frac{1}{X_{Cc}}+\frac{R'}{X_{c2}}+\frac{R'}{X_{Cc}}+\frac{R'}{X_{c1}}\right]=\frac{V_2(s)}{X_{Cc}}+V_{in}(s)+\frac{V_2(s)R'}{X_{Cc}} \qquad (5)$$

Applying KCL at V_2 −

$$\frac{V_2(s)-V_2'(s)}{R+X_L}+\frac{V_2(s)-V_1(s)}{X_{Cc}}+\frac{V_2(s)}{X_{c2}}=0 \qquad (6)$$

Applying KCL at V_2' −

$$\frac{V_2'(s)-V_2(s)}{R+X_L}+\frac{V_2'(s)}{R'}+\frac{V_2'(s)}{X_{c1}}=0 \qquad (7)$$

From equation (6) and (7)-

$$\frac{V_2(s)}{R+X_L}\left[\frac{\frac{1}{R'}+sC_1}{\frac{1}{R'}+sC_1+\frac{1}{R+X_L}}\right]+\frac{V_2(s)}{X_{Cc}}+\frac{V_2(s)-V_1(s)}{X_{Cc}}=0 \qquad (8)$$

From equation (5) the value of V_1 is given as-

$$V_1(s)=\frac{sC_cV_2(s)+V_{in}(s)+sC_cV_2(s)R'}{\frac{1}{R+sL}+sC_2+sC_c+R'sC_2+R'sC_c+R'sC_1}$$

Putting above value in equation (8), we get the value of $V_2(s)$-

$$V_2(s)=V_{in}(s)\left[\frac{As^4+Bs^3+Ds^2+Es}{Xs^5+Ys^4+Zs^3+Ws^2+Us+1}\right]$$

$$V_2(t)=L^{-1}(V_2(s))$$

5.4 Comparison of CNT bundle and Copper interconnect:

Table: 5.1 Comparison of crosstalk noise for L-segment RLC

	Crosstalk noise (mV)	
time(ns)	CNT	Copper
0	0	0
2	3	311.4
4	10	120
6	11.2	-320
8	5	-221.5
10	2.5	-98

Table 5.1 shows the comparison of crosstalk noise for copper and CNT bundle interconnect for L-segment RLC. It reveals that crosstalk noise for the case of CNT bundle interconnect is much less than the copper interconnect which means that CNT bundle introduces less noise than copper interconnect and gives better performance.

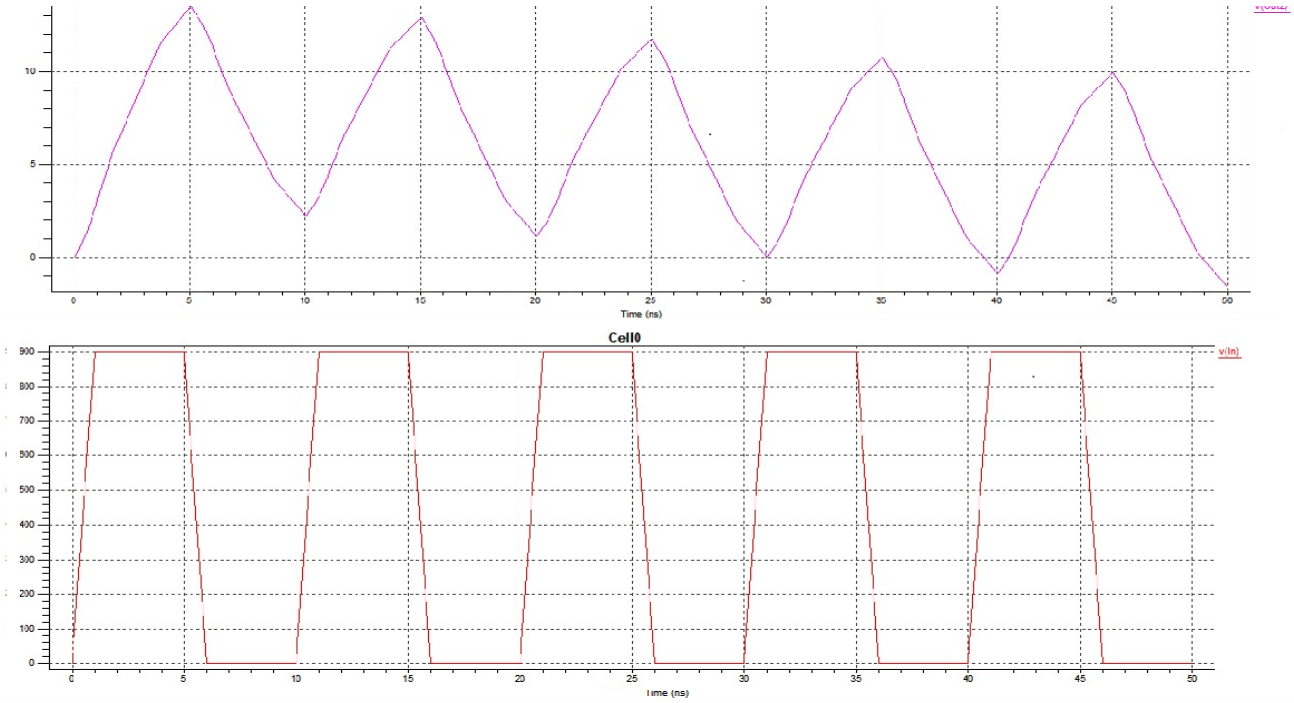

Figure 5.3: Crosstalk noise of L-segment RLC for CNT bundle interconnect

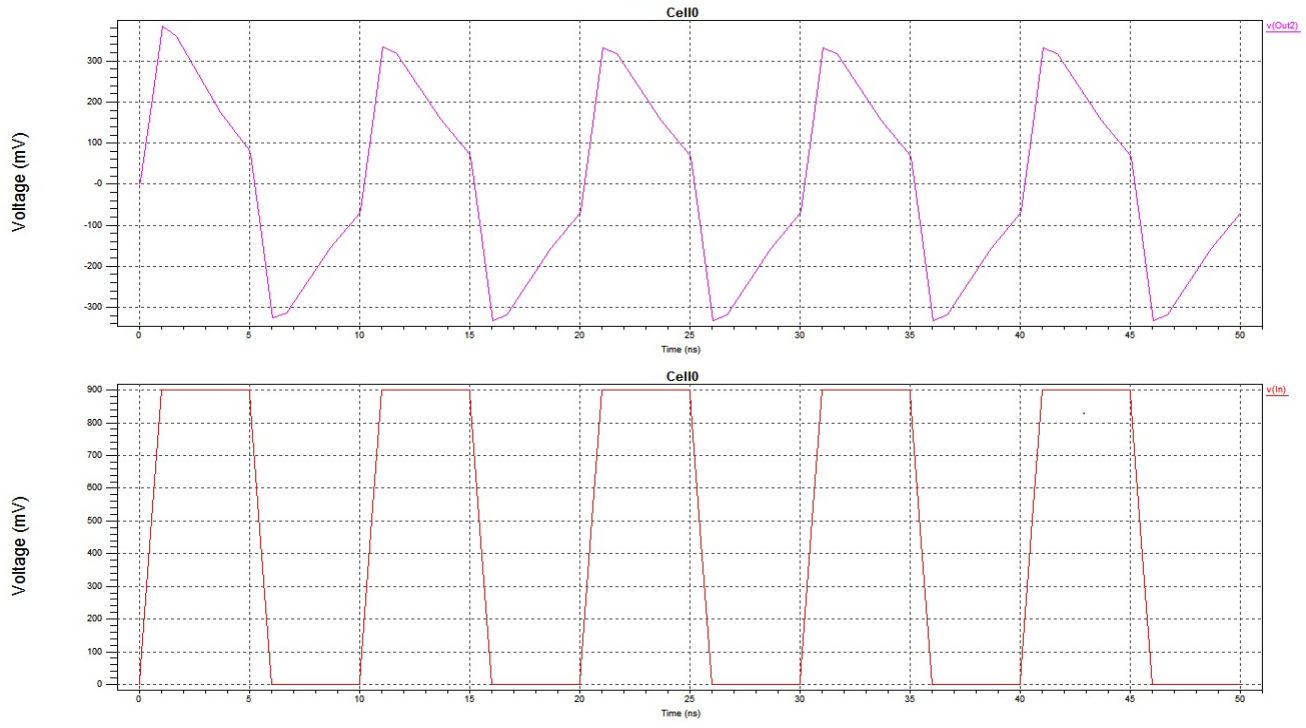

Figure 5.4: Crosstalk noise for L-segment RLC for Copper interconnect

Figure 5.3 and 5.4 shows the change of crosstalk noise (output voltage at victim line) with respect to time for L-segment model of CNT bundle and copper interconnect. An input pulse with rise time and fall time of 1ns is applied at the aggressor net and a output noise is obtained at the victim line.

Table: 5.2 Comparison of crosstalk noise for Pi-RLC circuit

	Crosstalk Noise (mV)	
Time(ns)	CNT	Copper
0	0	0
2	10	300
4	17	85
6	8	-400
8	0	-200
10	-0.1	-60

Table 5.2 shows the comparison of crosstalk noise for copper and CNT bundle interconnect for Pi-RLC. It reveals that crosstalk noise for the case of CNT bundle interconnect is much less than the copper interconnect which means that CNT bundle introduces less noise than copper interconnect and gives better performance.

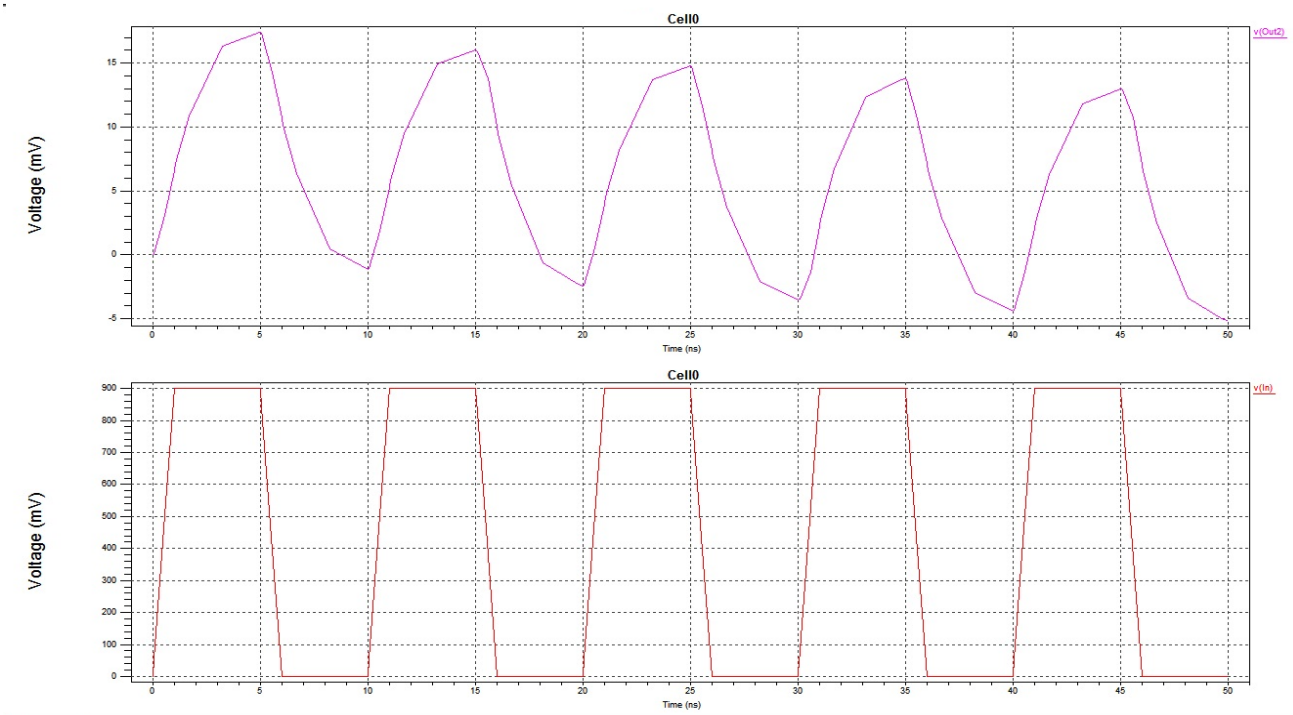

Figure 5.5: Crosstalk noise for Pi-RLC model of CNT bundle interconnect

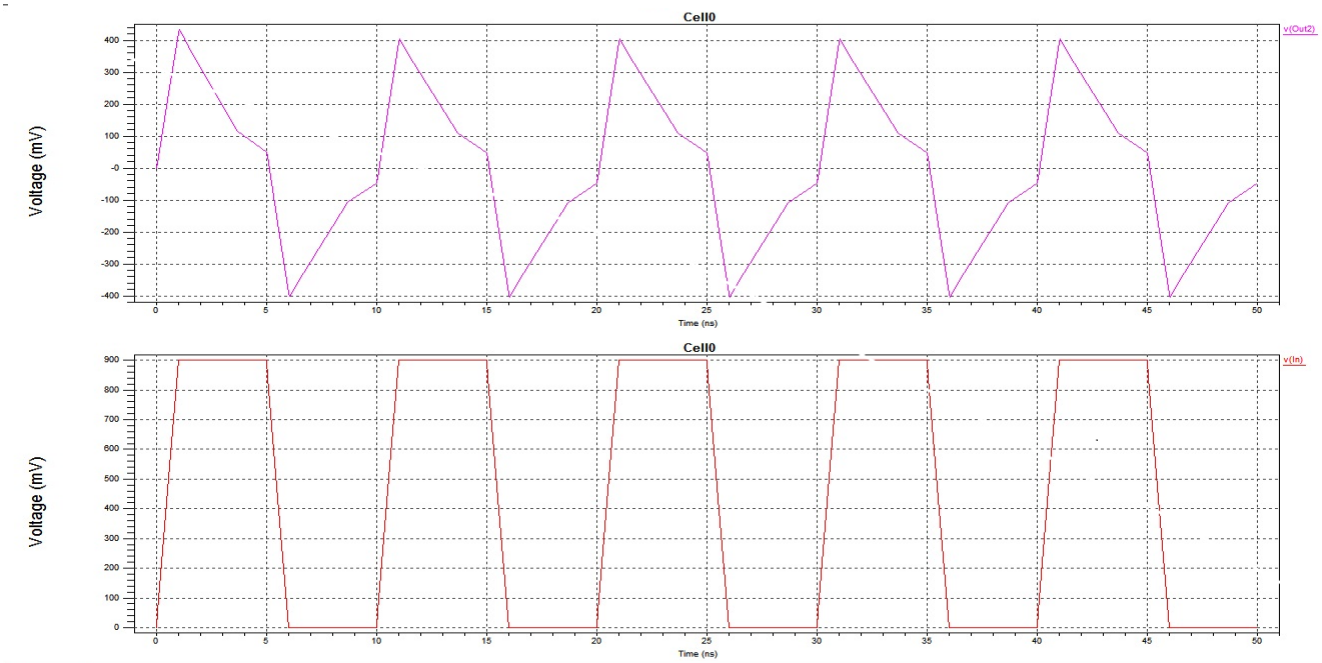

Figure 5.6: Crosstalk noise for Pi-RLC model of Copper Interconnect

Figure 5.5 and 5.6 shows the change of crosstalk noise (output voltage at victim line) with respect to time for Pi-model of CNT bundle and copper interconnect. An input pulse with rise time and fall time of 1ns is applied at the aggressor net and an output noise is obtained at the victim line.

5.5 Effect of various parameters on crosstalk:

The value of impedance parameters at different length is calculated using equations described in [10]. Here resistance of minimum sized transistor is 13.7k.

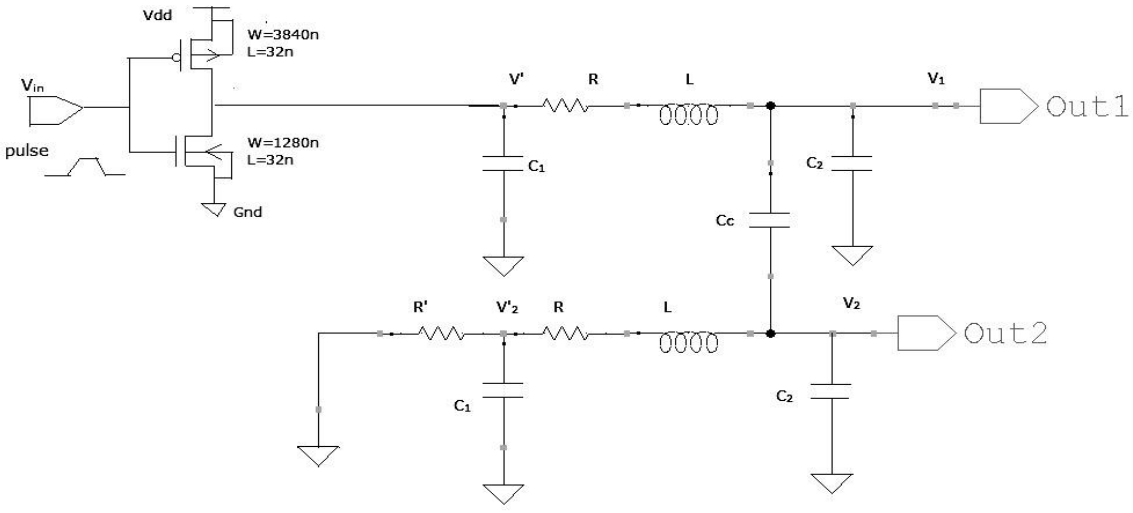

Figure 5.7 Crosstalk Model for Pi-RLC with CMOS inverter

Table 5.3 Impedance parameters at different length of interconnect

Length(um)	R(ohm)	L(fH)	C_1(pF)	C_2(pF)
400	161.08	23.37	0.255	1.275
500	200.44	29.25	0.318	1.59
600	240.86	35.1	0.381	1.9
700	280.46	40.94	0.445	2.225
800	320.83	46.81	0.51	2.55
900	361.008	52.65	0.57	2.86
1000	401.56	58.5	0.641	3.2

The value of impedance parameters at different length of interconnect for Pi-model of RLC is illustrated in table 5.3. These parameters are calculated using equations used in chapter 3. It shows that impedance parameters are increased with increase in interconnect length.

(a) Effect of interconnect length on peak overshoot

Table 5.4 Peak overshoot at different length of interconnect

Length(um)	Peak overshoot(mV)
400	11.32
500	9.95
600	8.69
700	8.08
800	7.56
900	6.53
1000	5.71

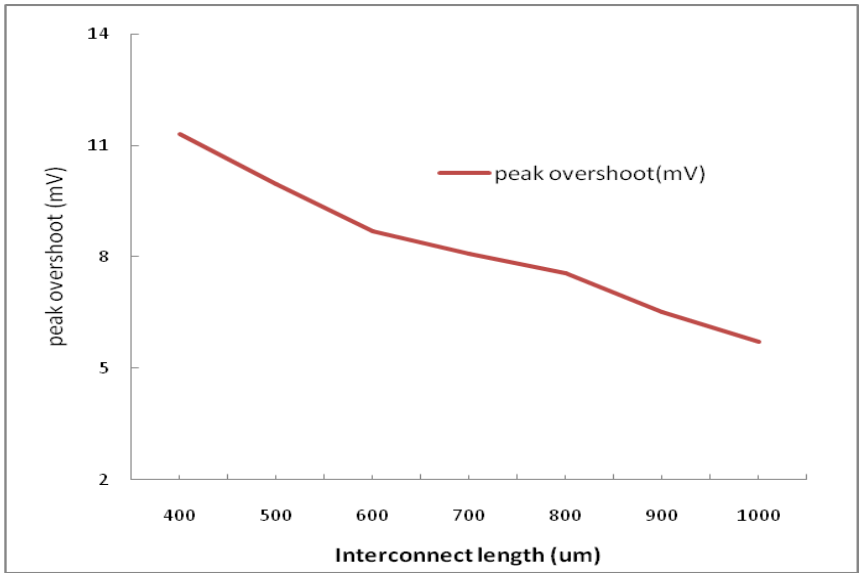

Figure 5.8 Peak overshoot as a function of interconnect length

Figure 5.8 illustrates the dependence of peak overshoot on interconnect length for CNT bundle. It shows that peak overshoot decreases with increase in interconnect length, because increase in length causes increase in impedance parameters (shown in table 5.4) resulting an increase in RC delay which reduces the peak overshoot.

Table 5.5 Peak overshoot as a function of size of driver transistor

Size of driver transistor	Peak overshoot (mV)
40	5.65
80	6.24
120	6.06
160	5.81
200	5.01

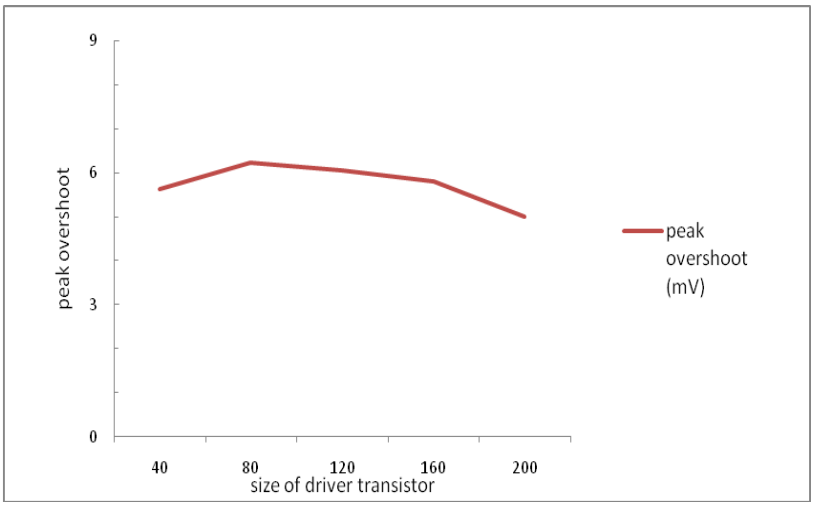

Figure 5.9 Peak overshoot as a function of size of driver transistor

Figure 5.9 shows the peak overshoot as function of driver transistor for Pi-RLC circuit of CNT bundle interconnect. It reveals that peak overshoot decreases with increase in size of driver transistor because with increase in size of driver transistor resistance increases that causes an increase in RC delay.

CHAPTER 6

CONCLUSION

In this dissertation, the analytical output waveform expression for L-segment RLC comprising a CMOS inverter, is calculated and compared with SPICE simulation result. A good agreement is observed between analytical model and SPICE model. Delay performance of CNT bundle interconnect has been compared with copper interconnects by using SPICE simulation at 32nm technology node. It is observed that CNT interconnect can greatly reduce signal delay. The effect of size of driver transistor and repeater insertion on the delay is also shown to optimize the delay performance of interconnects. The effect of interconnect length on impedance parameters of CNT bundle is also analyzed. Result shows that impedance parameters are increases with increase in length of interconnect. The changes in impedance parameters of CNT interconnect also affect the propagation delay.

A comparative study of Pi-model and distributed model of copper interconnect has also been carried out and result is compared with the CNT interconnect. It is concluded that delay can be reduced by using Pi-model than distributed model of interconnects.

An analytical model for crosstalk between two parallel L-segments RLC and Pi-RLC is derived and output noise at the victim line is calculated. The effect of various parameters such as length of interconnect and width of driver transistor on peak overshoot has been analyzed.

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APPENDIX

A.1 PTM level 54 model

This model is used for simulation of equivalent circuit model of CNT.

.model nmos nmos level = 54

+version = 4.0 binunit = 1 paramchk= 1 mobmod = 0

+capmod = 2 igcmod = 1 igbmod = 1 geomod = 1

+diomod = 1 rdsmod = 0 rbodymod= 1 rgatemod= 1

+permod = 1 acnqsmod= 0 trnqsmod= 0

+tnom = 27 toxe = 6.5e-010 toxp = 4e-010 toxm = 6.5e-010

+dtox = 2.5e-010 epsrox = 3.9 wint = 5e-009 lint = 1.35e-009

+ll = 0 wl = 0 lln = 1 wln = 1

+lw = 0 ww = 0 lwn = 1 wwn = 1

+lwl = 0 wwl = 0 xpart = 0 toxref = 6.5e-010 xl = -9e-9

+dlcig = 1.35e-009

+vth0 = 0.3692 k1 = 0.2 k2 = 0 k3 = 0

+k3b = 0 w0 = 2.5e-006 dvt0 = 1 dvt1 = 2

+dvt2 = 0 dvt0w = 0 dvt1w = 0 dvt2w = 0

+dsub = 0.078 minv = 0.05 voffl = 0 dvtp0 = 1e-011

+dvtp1 = 0.1 lpe0 = 0 lpeb = 0 xj = 7.2e-009

+ngate = 1e+023 ndep = 1.2e+019 nsd = 2e+020 phin = 0

+cdsc = 0 cdscb = 0 cdscd = 0 cit = 0

+voff = -0.13 nfactor = 2.3 eta0 = 0.0045 etab = 0

+vfb = -1.058 u0 = 0.0181 ua = -5e-010 ub = 1.7e-018

+uc = 0 vsat = 200000 a0 = 1 ags = 0

+a1 = 0 a2 = 1 b0 = 0 b1 = 0

+keta = 0.04 dwg = 0 dwb = 0 pclm = 0.06

+pdiblc1 = 0.001 pdiblc2 = 0.001 pdiblcb = -0.005 drout = 0.5

+pvag = 1e-020 delta = 0.01 pscbe1 = 2.0e+009 pscbe2 = 1e-007

+fprout = 0.2 pdits = 0.01 pditsd = 0.23 pditsl = 2300000

+rsh = 5 rdsw = 60 rsw = 30 rdw = 30

+rdswmin = 0 rdwmin = 0 rswmin = 0 prwg = 0

+prwb = 0 wr = 1 alpha0 = 0.074 alpha1 = 0.005

+beta0 = 30 agidl = 0.0002 bgidl = 2.1e+009 cgidl = 0.0002
+egidl = 0.8 aigbacc = 0.012 bigbacc = 0.0028 cigbacc = 0.002
+nigbacc = 1 aigbinv = 0.014 bigbinv = 0.004 cigbinv = 0.004
+eigbinv = 1.1 nigbinv = 3 aigc = 0.0213 bigc = 0.0025889
+cigc = 0.002 aigsd = 0.0213 bigsd = 0.0025889 cigsd = 0.002
+nigc = 1 poxedge = 1 pigcd = 1 ntox = 1
+xrcrg1 = 12 xrcrg2 = 5
+cgso = 7e-011 cgdo = 7e-011 cgbo = 0 cgdl = 7.5e-013
+cgsl = 7.5e-013 clc = 1e-007 cle = 0.6 cf = 1.1e-010
+ckappas = 0.6 ckappad = 0.6 vfbcv = -1 acde = 1
+moin = 15 noff = 1 voffcv = 0
+kt1 = -0.154 kt1l = 0 kt2 = 0.022 ute = -1.1
+ua1 = 1e-009 ub1 = -1e-018 uc1 = -5.6e-011 prt = 0
+at = 33000
+fnoimod = 1 tnoimod = 0 noia = 6.25e+041 noib = 3.125e+026
+noic = 8.75e+009 em = 41000000 af = 1 ef = 1
+kf = 0 tnoia = 1.5 tnoib = 3.5 ntnoi = 1
+jss = 1.2e-006 jsws = 2.4e-013 jswgs = 2.4e-013 njs = 1
+ijthsfwd= 0.1 ijthsrev= 0.1 bvs = 10 xjbvs = 1
+jsd = 1.2e-006 jswd = 2.4e-013 jswgd = 2.4e-013 xjbvd = 1
+pbs = 1 cjs = 0.0018 mjs = 0.5 pbsws = 1
+cjsws = 1.2e-010 mjsws = 0.33 cjswgs = 2.1e-010 cjd = 0.0018
+cjswd = 1.2e-010 mjswd = 0.33 pbswgd = 1 cjswgd = 2.1e-010
+mjswgd = 0.33 tpb = 0 tcj = 0 tpbsw = 0
+tcjsw = 0 tpbswg = 0 tcjswg = 0 xtis = 3
+dmcg = 0 dmci = 0 dmdg = 0 dmcgt = 0
+dwj = 0 xgw = 0 xgl = 0
+rshg = 0.4 gbmin = 1e-010 rbpb = 5 rbpd = 15
+rbps = 15 rbdb = 15 rbsb = 15 ngcon = 1

.model pmos pmos level = 54

+version = 4.0 binunit = 1 paramchk= 1 mobmod = 0
+capmod = 2 igcmod = 1 igbmod = 1 geomod = 1
+diomod = 1 rdsmod = 0 rbodymod= 1 rgatemod= 1

+permod = 1 acnqsmod= 0 trnqsmod= 0

+tnom = 27 toxe = 6.7e-010 toxp = 4e-010 toxm = 6.7e-010

+dtox = 2.7e-010 epsrox = 3.9 wint = 5e-009 lint = 1.35e-009

+ll = 0 wl = 0 lln = 1 wln = 1

+lw = 0 ww = 0 lwn = 1 wwn = 1

+lwl = 0 wwl = 0 xpart = 0 toxref = 6.7e-010 xl = -9e-9

+dlcig = 1.35e-009

+vth0 = -0.25399 k1 = 0.2 k2 = -0.01 k3 = 0

+k3b = 0 w0 = 2.5e-006 dvt0 = 1 dvt1 = 2

+dvt2 = -0.032 dvt0w = 0 dvt1w = 0 dvt2w = 0

+dsub = 0.1 minv = 0.05 voffl = 0 dvtp0 = 1e-011

+dvtp1 = 0.05 lpe0 = 0 lpeb = 0 xj = 7.2e-009

+ngate = 1e+023 ndep = 4.4e+018 nsd = 2e+02 phin = 0

+cdsc = 0 cdscb = 0 cdscd = 0 cit = 0

+voff = -0.13 nfactor = 2.3 eta0 = 0.0037 etab = 0

+vfb = -1.058 u0 = 0.0023 ua = -5e-010 ub = 1.6e-018

+uc = 0 vsat = 78000 a0 = 1 ags = 1e-020

+a1 = 0 a2 = 1 b0 = 0 b1 = 0

+keta = -0.047 dwg = 0 dwb = 0 pclm = 0.1

+pdiblc1 = 0.001 pdiblc2 = 0.001 pdiblcb = 3.4e-008 drout = 0.6

+pvag = 1e-020 delta = 0.01 pscbe1 = 2e+009 pscbe2 = 9.58e-007

+fprout = 0.2 pdits = 0.08 pditsd = 0.23 pditsl = 2300000

+rsh = 5 rdsw = 60 rsw = 30 rdw = 30

+rdswmin = 0 rdwmin = 0 rswmin = 0 prwg = 0

+prwb = 0 wr = 1 alpha0 = 0.074 alpha1 = 0.005

+beta0 = 30 agidl = 0.0002 bgidl = 2.1e+009 cgidl = 0.0002

+egidl = 0.8 aigbacc = 0.012 bigbacc = 0.0028 cigbacc = 0.002

+nigbacc = 1 aigbinv = 0.014 bigbinv = 0.004 cigbinv = 0.004

+eigbinv = 1.1 nigbinv = 3 aigc = 0.012731 bigc = 0.00115

+cigc = 0.0008 aigsd = 0.012731 bigsd = 0.00115 cigsd = 0.0008

+nigc = 1 poxedge = 1 pigcd = 1 ntox = 1

+xrcrg1 = 12 xrcrg2 = 5

+cgso = 7e-011 cgdo = 7e-011 cgbo = 0 cgdl = 3e-011

+cgsl = 3e-011 clc = 1e-007 cle = 0.6 cf = 1.1e-010
+ckappas = 0.6 ckappad = 0.6 vfbcv = -1 acde = 1
+moin = 15 noff = 1 voffcv = 0
+kt1 = -0.14 kt1l = 0 kt2 = 0.022 ute = -1.1
+ua1 = 1e-009 ub1 = -1e-018 uc1 = -5.6e-011 prt = 0
+at = 33000
+fnoimod = 1 tnoimod = 0 noia = 6.25e+041 noib = 3.125e+026
+noic = 8.75e+009 em = 41000000 af = 1 ef = 1
+kf = 0 tnoia = 1.5 tnoib = 3.5 ntnoi = 1
+jss = 2e-007 jsws = 4e-013 jswgs = 4e-013 njs = 1
+ijthsfwd= 0.1 ijthsrev= 0.1 bvs = 10 xjbvs = 1
+jsd = 2e-007 jswd = 4e-013 jswgd = 4e-013 xjbvd = 1
+pbs = 1 cjs = 0.0015 mjs = 0.5 pbsws = 1
+cjsws = 9.4e-011 mjsws = 0.33 cjswgs = 2e-010 cjd = 0.0015
+cjswd = 9.4e-011 mjswd = 0.33 pbswgd = 1 cjswgd = 2e-010
+mjswgd = 0.33 tpb = 0 tcj = 0 tpbsw = 0
+tcjsw = 0 tpbswg = 0 tcjswg = 0 xtis = 3
+dmcg = 0 dmdg = 0 dmcgt = 0 xgw = 0
+xgl = 0
+rshg = 0.1 gbmin = 1e-012 rbpb = 50 rbpd = 50
+rbps = 50 rbdb = 50 rbsb = 50 ngcon = 1