Analysis and Simulation of Three Phase Modified Hybrid Cascaded Multilevel Inverter for Induction Motor

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Submitted by
Snehansu Sekhar Panda
Roll no. 801542018

Under the Guidance of
Dr. Santosh Sonar
Assistant Professor, EIED

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Electrical and Instrumentation Engineering Department
Thapar University, Patiala– 147004
Post Bag No. 32, Punjab (India)

DECLARATION

I hereby certify that the work which is being presented in this dissertation entitled "**Analysis and Simulation of Three Phase Modified Hybrid Cascaded Multilevel Inverter for Induction Motor**" in partial fulfillment of the requirement for the award of degree of Master of Engineering in Power Systems, submitted to Electrical & Instrumentation Engineering Department of Thapar University, Patiala, is an authentic record of my own work carried under the supervision of Dr. Santosh Sonar, EIED. The matter contained in this thesis has not been submitted, neither in part nor in full to any other degree to any other university or institute.

Snehansu Sekhar Panda
801542018

Dr. Santosh Sonar
Assistant Professor
EIED, Thapar University

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Snehansu Sekhar Panda

(801542018)

DEDICATED TO MY MOTHER

ABSTRACT

The power converters are used to modify one form of electrical energy to another. The class of power converter that produce AC power from DC power is known as inverter. Due to high THD and losses, the conventional two level inverters are not suitable for high power applications. So multilevel inverters have drawn tremendous importance in power industries. This dissertation presents different Cascaded H-Bridge inverters. A single phase 5-levels hybrid MLI is implemented by incorporating half-bridge and full-bridge inverter. It is further extended to implement single phase 7 levels hybrid MLI. This also presents single DC source seven level CHB inverter. It uses single DC input while changing other DC source with a capacitor as energy storing element. Then a three phase modified hybrid cascaded multilevel inverter is suggested incorporating standard three leg inverter with H-bridge cells. The switching scheme with multicarrier level shifted SPWM is implemented to produce different possible levels. This MLI is implemented to run an induction motor load. In addition, a second order LC filter is designed to reduce the THD below 5% as per standard IEEE-519. Simulations have been performed using MATLAB to study different topologies, voltage levels, modulation scheme and THD. Finally, the possibilities of future works are addressed.

Key words- Multilevel inverter, THD, cascaded H-bridge. SPWM.

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LIST OF ABBREVIATIONS

AC	Alternating Current
DC	Direct Current
SPWM	Sinusoidal Pulse Width Modulation
THD	Total Harmonic Distortion
MLI	Multilevel Inverter
SVM	State Vector Modulation
SHE	Selective harmonics Eliminations
CHB	Cascaded H Bridge
VSI	Voltage Source Inverter
NPC	Neutral Point Clamped
FC	Flying Capacitor
SVG	Static Var Generator
IGBT	Insulator Gate Bipolar Transistors
GTO	Gate Turn Off Thyristor
PS	Phase Shifted
LS	Level Shifted
CSI	Current Source Inverter
PD	Phase Disposition
POD	Phase Opposite Disposition
APOD	Alternate Phase Opposition Disposition
FACTS	Flexible AC Transmission System
PID	Proportional Integral Derivative

CHAPTER1

INTRODUCTION

1.0 Introduction

The power converters are used to modify one form of electrical energy to another. Depending on type of input and output it can be classified as follows.

1. AC to DC (Rectifier)
2. DC to AC (Inverter)
3. DC to DC (Chopper)
4. AC to AC (Cycloconverters)

The class of power converters that produce AC power from DC power is known as inverters. The output generated would be of constant voltage and frequency. The average output power must be zero. But the real one yields non-sinusoidal output. Because of high total harmonic distortion and losses of the regular square-wave and semi-square waveform inverters, marks them unacceptable for different applications. With the use of semiconductor power switches and different PWM switching techniques the harmonics in output is reduced. The Multilevel inverters yield output voltages nearer to pure sine wave. Therefore, it would minimize harmonics in the output which leads to less power losses. This marks them suitable for high power applications such as AC power supplies, static VAR compensator and drive system. As the number of levels in output voltage achieves infinite then the THD approaches to zero. But the production of possible voltage levels is restricted by constraints such as voltage unbalancing problem and clamping problem. The complex control scheme is implemented to generate switching pulses for MLI.

In this thesis, a three phase hybrid cascaded multilevel inverter is suggested incorporating standard three leg inverters with H-bridge cell. A multicarrier based sinusoidal PWM technique is implemented in order to produce possible voltage levels in the output. The level shifted multicarrier SPWM would be of type such as phase-disposition, phase-opposite-disposition and alternate-phase-opposite-disposition. The suggested model is implemented to run the Induction motor load. LC low pass filter is designed to reduce the voltage harmonics below 5%. The major advantages of LC filters are to minimize the higher order voltage harmonics introduced in to the system due to high switching frequency. The damping resistance is used to damp out the overshoot. The comparative studies are performed for different topologies, voltage levels, modulation scheme and THD in MATLAB environment. Finally, the result is discussed with possibilities of future work.

1.1 Scope of the Work

Multilevel inverters produce less harmonic waveforms at the output voltage. Apart from that MLI generates lower dv/dt , reduced voltage stress across switches and suitable for low switching frequency . This makes them more suitable for high power applications. MLIs are used to fed bulk power to the different loads from renewable sources like solar power and biomass. The multilevel inverters start from three levels. The generation of the possible levels in the output voltage waveform is restricted by the voltage unbalancing problems and packaging constraints. The conventional MLI types are (i) diode clamped, (ii) flying capacitor, and (iii) cascaded inverter. The different modulation techniques have been implemented for MLI. They are such as (i) sinusoidal pulse width modulation (SPWM), (ii) selective harmonic elimination (SHE-PWM), (iii) space vector modulation (SVM) etc.

1.2 Objective of the Study

In this dissertation different Cascaded H-Bridge inverters have been studied and implemented. A single phase hybrid five level CHB is implemented by incorporating half-bridge and full-bridge inverter. The switching scheme with multicarrier level shifted SPWM is implemented to produce different possible levels. It is further extended to implement single phase seven level hybrid CHB by adding one more half-bridge inverter. The above topology has more isolated DC sources and as a remedy single DC source seven level CHB inverter is implemented. It uses single DC input while changing other DC source with a capacitor as energy storing element. The charging and discharging phenomena of capacitor is studied. The capacitor voltage balancing is done using redundant switching states. Then a three phase hybrid cascaded multilevel inverter is suggested incorporating standard three leg inverters with H-bridge cell. It produces nine levels at line to line output voltage. The MLI topology is implemented to run an induction motor load. In addition, a second order LC filter is designed to reduce the harmonics below 5%. Simulations have been performed using MATLAB to study the competence of the CHB MLI.The comparative studies are performed for different topologies, voltage levels, modulation scheme and THD. Finally, the possibilities of future works are addressed.

Thesis Organization

The dissertation report is presented in five Chapters. The brief details of each chapter are as follows:

Chapter1 Introduction

This section provides an overview to multilevel inverters and the switching techniques.

Chapter2 Literature Review

This part describes the related literature studies of the thesis work carried out by different researchers.

Chapter3 Design and Modelling of MLI

This chapter presents design and implementation of hybrid MLI built on cascading of full and half bridge inverter and some other relevant topologies. The related control scheme of multicarrier SPWM is enforced to produce the possible levels at the output.

Chapter4 Simulations and Results Discussions

This chapter presents the simulation results performed in MATLAB Simulink environment to validate the proposed work.

Chapter5 Summary and Conclusions

This briefs the summary of the dissertation work carried out and provides conclusions. This also includes the scope for future studies.

CHAPTER2

LITERATURE REVIEW

2.0 Overview

The multilevel VSI is used in many high power applications. The examples are ac power supplies, FACT devices and AC drive etc. The important benefits of MLI structure is the lesser harmonic production at the voltage output without decreasing the inverter efficiency.

2.1 Studies on Multilevel Inverter

[1] In this paper, a new neutral-point-clamped MLI with sinusoidal PWM control strategies is presented. PWM technique is designed to eliminate lower order harmonics in the output. Hence inverter efficiency and load power factor is improved. It also describes the potential application of this MLI in variable speed drive system. This topology uses more number of power switches compared to conventional NPC MLI but the KVA output is more.

[2] MLI based power converters are evolving as another efficient type of inverter choices for applications such as variable speed drive and reactive power compensation. It presents a comparative study of THD, power switches, clamping diodes and DC bus capacitor requirement among different topologies such as diode clamped, flying capacitor and cascaded MLI. It also describes features like capacitor voltage unbalancing, unequal device rating and reverse voltage blocking of clamping diodes.

[3] CHB MLI with separate isolated dc sources is implemented. It can produce nearly sinusoidal output voltage and solve size and weight problems of traditional multi-pulse inverter. Hence it is used for high-voltage, high-power applications like FACTS devices, power-line conditioning and renewable energy generations. To exhibit the advantage of the CHB MLI, a SVG system using this topology is discussed.

[4] A hybrid MLI is presented with possible levels in the output waveform and thus greatly decreases the low-order harmonics and THD. The harmonic elimination PWM scheme with lower switching frequency is used to reduce switching loses.

[5] It presents topologies such as soft-switching cell and asymmetrical hybrid cell. State vector PWM is used in high power application as it greatly reduces current harmonics. SHE-PWM is used for lower switching frequency and wide range of modulation index.

[6] MLI inverters utmost used due to low electromagnetic interference and high efficiency. It describes the advantages of SVM and fundamental switching control techniques. A special consideration is given to study the loss distribution across power switches. This paper also

debates the leading area of application such as hybrid electric vehicle and discuss about technological glitches such as capacitor unbalancing problem and losses.

[7-8] A cascaded H-bridge MLI is realized using only a single DC source and capacitors. In order to generate 2n + 1 levels in output voltage waveform, it use one DC source with n – 1 capacitor. To reduce switching loses SHE-PWM, fundamental switching method and active harmonics elimination is used. The switching devices features such as switching characteristics, reduced power losses and snubber-less operation are studied for IGBT and GTO.

[9-10] A new asymmetrical cascaded twenty-seven-level inverter is implemented. It reduces THD, switching losses and common mode voltages. The projected topology uses floating, isolated, balanced and sometimes bidirectional dc sources. Due to isolation and voltage scaling problem, it is not used in electric vehicle application. It is used in constant frequency application such as power rectifier and FACT system.

[11] It presents recent advancement in MLI topologies such as hybrid NPC-CHB, hybrid FC-CHB and TCC and modulation technique (PS-PWM). CHB uses phase shifting transformer and multi-pulse rectifier system to improve input power. It also describes MLI applications in areas like HVDC, marine propulsion. It also discusses the LS-SPWM and PS-SPWM and SHE-PWM in great details.

[12] The projected model is obtained by series connection of a flying capacitor MLI structure with H-bridge inverter. The capacitor voltages can be balanced by properly choosing the redundant switching states. This model improves modularity and power factor. Here the model operates as three level inverter if in case H bridge cell fails. So it is fault tolerant.

[13] The crossover switches cell(CSC) MLI harvest a high power output. This typically permits in order to realize high-quality output voltages. It uses less DC sources and power switches. It produces less distortion in output, lower common mode voltage and dv/dt across switches.

[14] A single-phase asymmetrical CHB MLI built on series connection of half and full bridge inverter cells is presented. It uses less number of switches compared to conventional MLI in order to produce same voltage levels.

[15] A 31 level asymmetrical sub-multilevel inverter is implemented. It uses less number of power switches and DC input supplies. It describes switching angle calculation to reduce THD The projected MLI is presented in both symmetric and asymmetric type.

[16] Here a hybrid MLI built on series connection of full and half bridge inverters is presented. The related switching technique with multicarrier LS- PWM is implemented. The switching

method permits the capacitors of the half bridge inverter to have balanced voltage during load changing.

[17] A seven-level cascaded MLI using a single DC source is implemented. The capacitor voltage is controlled at half of the input supply in order to symmetrical level. It presents alternative to interchange dc sources of the H-bridge cells with capacitors. The model is implemented using the phase-shift SPWM technique.

2.2 Studies on Modulation Techniques

There are different types of PWM technique used in order to achieve adjustable at the output. The primarily implemented PWM technique for MLI are Sinusoidal PWM, Space Vector PWM and SHE-PWM. SPWM is preferably used because of its simple realization.

[18] Here PWM scheme for Neutral Point Clamped MLI and Cascaded MLI are introduced. It shows alternative Phase Opposition Disposition SPWM scheme generates the similar spectral component as PSC-PWM technique. It is also suggested to implement the harmonically superior Phase Disposition (PD) PWM scheme.

[19] It presents detail investigation of LS-SPWM schemes for CHB MLI. It was found that APOD-PWM for capacitor-clamped MLI inverters generates the analogous harmonic characteristic as PSC-PWM for CHB MLI inverters.

[20] It implements the SVM and multicarrier-based PWM for MLI. The SVM is used for lower modulation index. It is difficult to implement SVM when number of levels increases. So it transforms modulated wave(vector-ally) of SVM to sinusoidal wave to generate multicarrier-based PWM technique.

[21] Here SHM-PWM and SHE-PWM modulation scheme have been implemented to yield pulses for a three-level neutral point clamped MLI. SHM scheme is used to eliminate non-triplen harmonics and SHE method to the triplen harmonics.

2.3 Studies on Induction Motor

An induction motor is an AC asynchronous motor. It may be either wound rotor type or squirrel-cage rotor type. The squirrelcage induction machine are broadly utilized in industrial drives uses due to recent advancement in power electronics. Induction machine are used in both fixed-speed and variable-frequency drive applications.

[22] The performance of a vector-controlled squirrelcage IM is studied. The IM drive is supplied from a current-controlled MLI system. The speed regulation of induction motor is implemented using closed-loop v/f which employs a fuzzy PID controller.

[23] It presents idea for harmonic minimization and gives a comparative study between active and passive filter. The passive filters are suitable choice for high value nonlinear load. This

also describes the mostly used band pass filters and damped filters. Here restrictions and boundaries for filter design is discussed with recent technique of harmonic study, measurements, and system analysis.

[24] A MLI topology with Octadecagon voltage space vector is suggested. The octadecagon voltage space vectors are implemented by appropriate choice of DC voltages and control technique. It also employs asynchronous motor drives with constant v/f control, vector control, and direct torque control method.

[25] Here a nine-level MLI is implemented for high-voltage asynchronous machine drives application through open-end stator winding.

[26] It suggests a novel six-phase stacked MLI drive for a six phase induction motor .It also describes the v/f control of the induction motor. The dc sources are implemented by series connected capacitors with naturally balanced neutral point current within a switching cycle.

[27] A third order LCL circuit filter is frequently used in the system in order to mitigate the harmonics. It presents the mathematical modeling of LCL filter considering practical cases of connection of capacitors. It may be star or delta connection. It makes the system bulky.

2.4 Research Gap

Literature studies shows that there is possible scope of further development in multilevel inverter. In case of single DC source seven level CHB MLI the major draw-backs of this system is the dependency between modulation index and capacitor voltage. Which limits the operation of this configuration at certain modulation index. By using this a possible modified three-phase MLI topology can be realized incorporating standard three leg inverter with H-bridge cell. It will use single DC source, three DC link capacitors as storage element and eighteen power switches in order to implement the topology. This will produce nine level in line to line output voltage. In this thesis work implementation of modified three-phase MLI topology incorporating standard three leg inverters with H-bridge cell which uses four DC source and eighteen switches is presented. Furthermore, the modified three-phase MLI using single DC source, three DC link capacitors and eighteen switches will be implemented in future work.

CHAPTER 3
DESIGN AND MODELING OF MULTILEVEL INVERTER

3.0 Introduction

The class of power converters that produce AC power from DC power is known as inverters. The output generated would be of constant voltage and frequency. It is broadly classified into two types:

1. Voltage source inverter
2. Current source inverter

In case of VSI the output voltage depends on source voltage where as in CSI the load current depends on source current. For underdamped load the VSI is load commuted and uses feedback diode to supply back the reactive power consumed by load. It uses IGBT switches and applicable in high-power applications. Here we will greatly deal with voltage source inverter. From the connection view point, half bridge and full bridge inverters are introduced. It produces square and semi-square wave voltage output. In case of half-bridge inverter the rms value of fundamental output voltage (v_{01}) is 0.45 v_{dc} .where v_{dc} is input supply. Where as in full bridge inverter v_{01} is 0.9 v_{dc}.Because of high total harmonic distortion and losses of the regular square-wave and semi-square waveform inverters, marks them unacceptable for high power applications. Three single-phase half (or full) bridge can be connected in parallel to form three phase inverter. It is used for high power applications. Now-a-days MLI have created greater impact in power sector. Multilevel inverters yield output voltages nearer to pure sine waveform. Therefore, it has lesser THD which leads to less power losses. This marks them appropriate for high voltage energy conversion system. Then by rising more levels in voltage waveform the power handing capacity is increased without increasing the individual device rating. The MLI is largely classified into three types.

1. Diode clamped MLI.
2. Flying capacitor MLI.
3. Cascaded MLI.

3.1 Diode Clamped MLI

Fig. 3.1 presents functioning of a three-level diode-clamped inverter. Here series-connected capacitors c_1 and c_2 divide the DC-bus voltage. The middle point of the capacitors is considered as the neutral point. The output v_{an} will have three levels $\pm\frac{v_{dc}}{2}$, 0. When switches s_1, s_2 are turned on then $v_{an} = +\frac{v_{dc}}{2}$. while $s'_1, s'_2$are turned on then $v_{an} = -\frac{v_{dc}}{2}$ and for the 0 level s_2, s'_1 *are* on. Then D_1 *and* D_2 are clamping diodes.

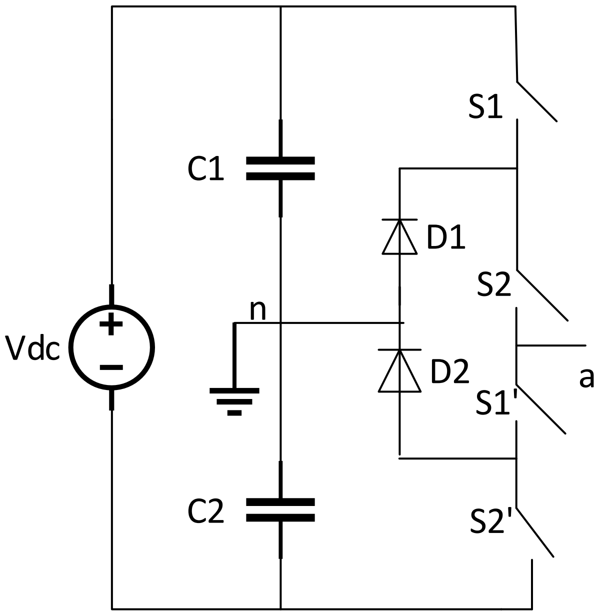


Figure 3.1: Single phase three-level NPC inverter

A m level inverter consists of $m-1$ capacitors ,$(m-1)*(m-2)$ clamping diodes per phase and $2*(m-1)$ power switches.

3.2 Flying Capacitor MLI

Fig. 3.2 describes a three-level flying capacitor inverter. Here series-connected capacitors c_1 and c_2 divide the DC-bus voltage. The middle point of the capacitors is considered as the neutral point. The output v_{an} will have three levels $\pm\frac{v_{dc}}{2}$, 0. When switches s_1, s_2 are turned on then $v_{an} = +\frac{v_{dc}}{2}$. while $s'_1, s'_2$are turned on then $v_{an} = -\frac{v_{dc}}{2}$ and for the 0 level either s_1, s'_1 *or* s_2, s'_2 *are* on. The C is clamping capacitor. A m level inverter consists of $m-1$ DC link capacitors ,$(m-1)*(m-2)/2$ clamping capacitor per phase and $2*(m-1)$ power switches. The clamping capacitor is charged through switch s_1, s'_2 and discharged through s_2, s'_1 .

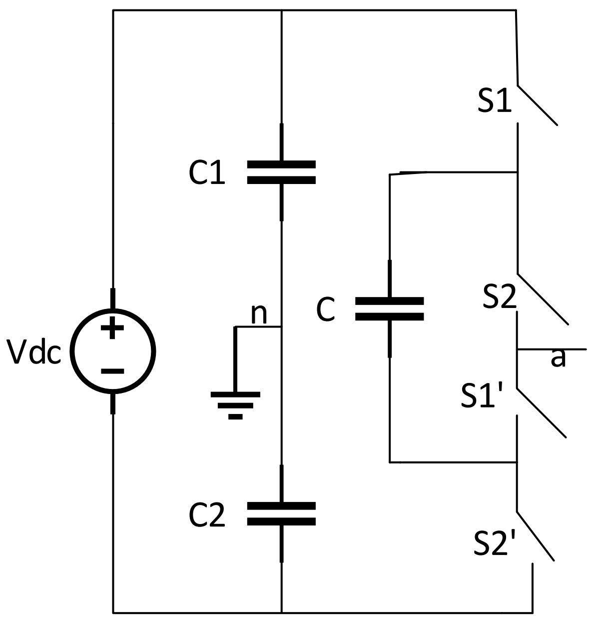


Figure 3.2: Single-phase three-level FC inverter

The benefits of NPL MLI structure is, the control method is simple and as the possible level in the output voltage waveform increases the THD content is less enough in output in order to avoid filter circuit. The major demerits of NPL MLI is the different reverse blocking voltage for diodes. The power rating of the switches are different and capacitor unbalancing problem. As voltage across capacitor is different, so they produce different current. So the charging and discharging time of capacitor is not same. That leads to voltage unbalancing problem. Similarly, Flying-capacitor MLI structure uses more number of capacitors. So both the active and reactive power flow is measured. Here voltage balancing is done using redundancy switching. The major drawbacks are it is bulky and has packaging problem and switching losses is high. The Cascaded MLI has advantages over capacitor clamped MLI and Flying capacitor MLI. It uses less number of electrical components to produce same levels in output voltage waveform. The cascaded MLI has improved circuit design and packaging marks them suitable for practical applications. It uses no extra clamping diode and capacitors. The switching losses can further have reduced by using soft switching method. During power conversion it requires separate isolated DC sources. This MLI is mostly used in renewable generation such as photovoltaic and fuel cell applications. There are different modulation scheme and control strategies that have been implemented for MLI power converters like SPWM, SHE-PWM, SVM, and many others. In this dissertation different Cascaded H-Bridge inverters topologies have been studied. A three phase hybrid cascaded MLI is suggested incorporating standard three leg inverters with H-bridge cell. The control scheme with level shifted multicarrier SPWM is implemented to produce different levels in the output voltage waveform. Here different types of multicarrier SPWM like phase opposite disposition, alternate phase opposite disposition and phase disposition is implemented. The technique also permits to maintain balanced voltage across capacitors of the half bridge inverter during load variations. This implementation is further stretched to more inverters with isolated separate DC supplies to yield possible levels in the output voltage waveform. The suggested topology is using more number of isolated DC sources and as a remedy Single DC source CHB inverter is implemented. Also a second order LC filter is designed to further reduce the harmonics to below 5%. Further the MLI topology has been implemented to run an induction motor load. Simulations have been performed using MATLAB to validate the competence of the CHB MLI with equal and unequal isolated DC supplies. Finally, the possibilities of future works are addressed.

3.3 Cascaded MLI

Here single-phase CHB MLI is described. It produces five-levels in output voltage waveform. Each cell produces three different voltage levels such as $+v_{dc}$,0,$-v_{dc}$. Therefore, to harvest large voltage levels in the output waveform more number of cells are connected in cascading. It will reduce harmonics in output voltage waveform significantly. The cells can use equal or unequal DC sources. As m number of cells are in cascading can able to produce $2m+1$ levels in the output by using equal DC. Figure 3.3 presents a single-phase CHB inverter. It uses two identical isolated DC supply in order to produce five-level in the output.

Output voltage $v_0=v_1+v_2$ (3.1)

Where $v_1 = output\ Voltage\ of\ upper\ full-bridge\ inverter.$

$v_2 = Output\ Voltage\ of\ lower\ full-bridge\ inverter.$

$v_{dc} = Input\ DC\ supply\ to\ full-bridge\ inverter.$

suppose $v_{m1}= v_{m2}= E$

$v_{m1}\ and\ v_{m2}\ are\ input\ DC\ supply.$

The output waveform will be of five-levels such as $\pm 2E, \pm E, 0.$

Suppose $v_{m2}= 2 \times v_{m1}=2E$

The output waveform will be of seven-levels such as $0, \pm E, \pm 2E, \pm 3E.$

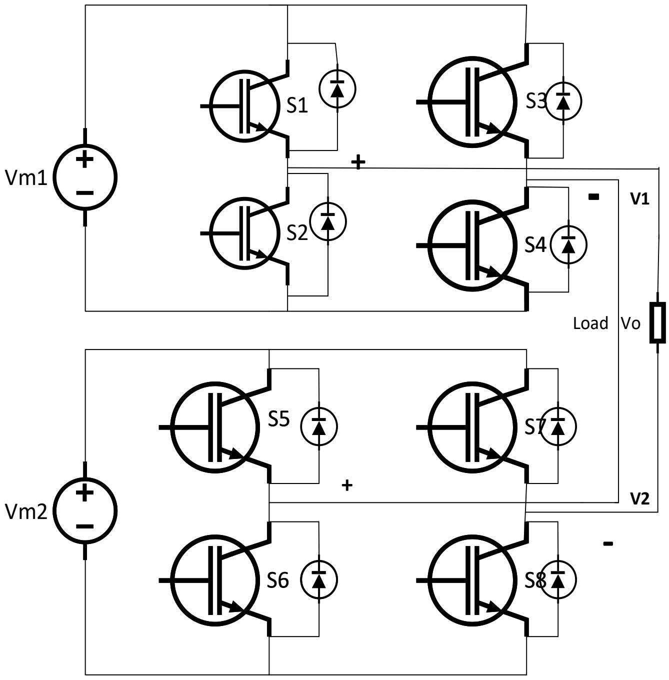


Figure 3.3: Single-phase five-level CHB inverter

If suppose v_{m2} =3× v_{m1}=$3E$

The output waveform will be of nine-levels such as $0, \pm E, \pm 2E, \pm 3E, \pm 4E.$

So by using unequal isolated DC supply we can generate more levels at output voltage. It forces different voltage stresses across power switches.

3.3.1 Single-Phase Hybrid Five-level Cascaded MLI

Here the single phase hybrid CHB MLI is implemented by cascading of half-bridge and full-bridge inverters. This connection will generate the preferred levels at the output voltage waveform. It is found that, during switching only one of the DC supply is in contact with the load. So the half-bridge inverter model can be realized by using one isolated DC supply with two capacitors connected in series. Figure 3.4 presents a five-level Hybrid CHB inverter.

Output load voltage v_0=v_1+v_2

Where v_1 , v_2 $are\ voltages\ of\ upper\ and\ lower\ cell\ respectively$

Here suppose v_{m1}= $2E$ = v_{c1} + v_{c2} and v_{m2}= E.

v_{c1} and v_{c2} are voltage across capacitors c_1 , c_2 respectively .

$v_{m1}\ and\ v_{m2}\ are\ input\ DC\ supply.$

Then the half bridge inverter will yield $\pm E$ and full-bridge inverter will produce $\pm E, 0$. So the five level output wave will be generated like $\pm 2E, \pm E, 0$.

The switching function is implemented below:

$s_i = \{0|\ if\ s_i\ is\ off\ i = 1,2 \dots 6\ \}$ (3.2)

$s_i = \{1|\ if\ s_i\ is\ on\ i = 1,2,3 \dots 6\ \}, Where\ s_i\ is\ switches$ (3.3)

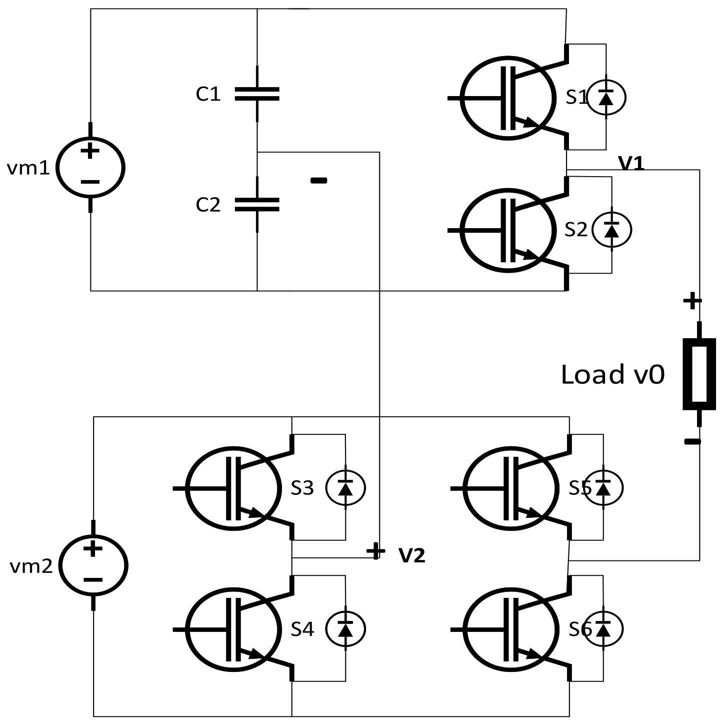


Figure 3.4: Single-phase five-level hybrid CHB inverter

The complementary switches can be realized as following.

$$\begin{cases} s_2 = \overline{s_1} = 1 - s_1 \\ s_4 = \overline{s_3} = 1 - s_3 \\ s_6 = \overline{s_5} = 1 - s_5 \end{cases} \quad (3.4)$$

Using KVL and taking $v_{c1} = v_{c2} = v_{m2}$

$$v_1 = s_1 v_{c1} - s_2 v_{c2} = (2s_1 - 1)E \quad (3.5)$$

$$v_2 = s_3 E - s_5 E = (s_3 - s_5)E \quad (3.6)$$

$v_0 = v_1 + v_2$

Table-3.1 Switching states of hybrid five level CHB MLI inverter

s_1	s_2	s_3	s_4	s_5	s_6	v_1	v_2	v_0
1	0	1	0	0	1	$+E$	$+E$	$+2E$
1	0	1	0	1	0	$+E$	0	$+E$
1	0	0	1	1	0	$+E$	$-E$	0
0	1	1	0	0	1	$-E$	$+E$	0
0	1	1	0	1	0	$-E$	0	$-E$
0	1	0	1	1	0	$-E$	$-E$	$-2E$

3.3.2 Hybrid Seven-level CHB MLI

Further single-phase hybrid seven-level CHB is implemented. It contains two half bridge cell cascading with full-bridge cell. The combination will produce a seven level output like $0, \pm E, \pm 2E, \pm 3E$. Figure 3.5 presents a seven-level Hybrid CHB inverter.

Output load voltage $v_0 = v_1 + v_2 + v_3$

Where v_1 , v_2, v_3 *are cell voltages respectively.*

Then the half bridge inverter will yield $\pm E$ and full-bridge inverter will produce $\pm E, 0$. So the seven level output waveform will be generated like $\pm 3E$, $\pm 2E, \pm E, 0$.

Here a multicarrier based SPWM is designed to produce switching pulses. Here for m level generation $m - 1$ triangular carrier waves are needed. In order to generate switching pulses a carrier wave v_{tri} is compared to reference signal v_{ref} . The intersection of v_{tri} and v_{ref} decides the switching and commutation of modulated signal. When the $v_{ref} \geq v_{tri}$ then output is high otherwise low. Here the carrier signal is high frequency level shifted triangular wave and reference is sinusoidal wave.

Here, suppose $v_{m1} = 2E = v_{c1} + v_{c2}$ and $v_{m2} = 2E = v_{c3} + v_{c4}$ *and* $v_{m3} = E$

v_{c1} , v_{c2} , v_{c3} , v_{c4} are capacitor voltages across c_1 , c_2 , c_3 , c_4 respectively .

The switching function is implemented below:

$s_i = \{0 | \ if \ s_i \ is \ off \ i = 1,2 \ldots 8 \}$

$s_i = \{1 | \ if \ s_i \ is \ on \ i = 1,2,3 \ldots 8 \}$

The complementary switches can be realized as follows.

$$\begin{cases} s_2 = \overline{s_1} = 1 - s_1 \\ s_4 = \overline{s_3} = 1 - s_3 \\ s_6 = \overline{s_5} = 1 - s_5 \\ s_8 = \overline{s_7} = 1 - s_7 \end{cases}$$

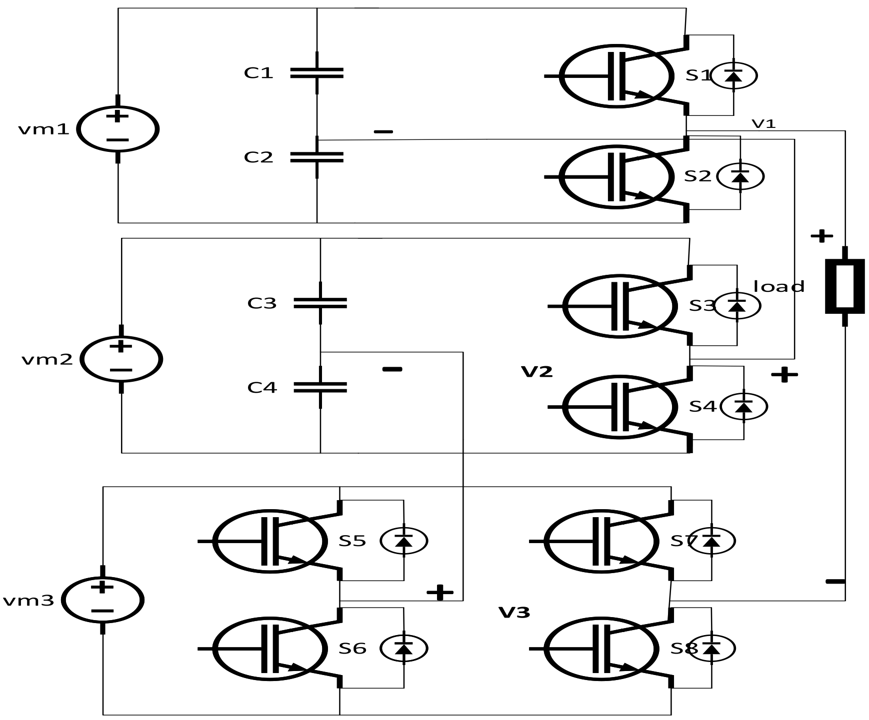


Figure 3.5: Single-phase seven-level hybrid CHB inverter

Using KVL and taking $v_{c1} = v_{c2} = v_{c3} = v_{c4} = v_{m2} = 2E$, $v_{m3} = E$

$$v_1 = s_1 v_{c1} - s_2 v_{c2} = (2s_1 - 1)E \quad (3.7)$$

$$v_2 = s_3 E - s_4 E = (s_3 - s_4)E \quad (3.8)$$

$$v_3 = (s_5 - s_7)E \quad (3.9)$$

$$v_0 = v_1 + v_2 + v_3$$

Table-3.2 Switching states of seven-level hybrid CHB MLI

s_1	s_2	s_3	s_4	s_5	s_6	s_7	s_8	v_1	v_2	v_3	v_0
1	0	1	0	1	0	0	1	$+E$	$+E$	$+E$	$+3E$
1	0	1	0	1	0	1	0	$+E$	$+E$	0	$+2E$
1	0	1	0	0	1	1	0	$+E$	$+E$	$-E$	$+E$
1	0	0	1	1	0	1	0	$+E$	$-E$	0	0
0	1	0	1	1	0	0	1	$-E$	$-E$	$+E$	$-E$
0	1	0	1	1	0	1	0	$-E$	$-E$	0	$-2E$
0	1	0	1	1	1	1	0	$-E$	$-E$	$-E$	$-3E$

Here the switching technique generates more number of control states to produce same output voltage. The redundancy control states are not mentioned in the table-3.2. and used for voltage balancing purpose.

3.3.3 Single-Phase Single DC-source Seven-level Cascaded MLI

A single phase single DC source seven level CHB MLI is presented in Fig. 3.6. The first -full bridge inverter is connected to DC source and second full-bridge is supplied from capacitor. The DC source is used to charge the capacitor at a chosen level in order to get symmetrical level in output waveform. The capacitor discharges through load to produce levels in output. Here the capacitor voltage is set at half of the DC supply value to get 7-level in output voltage waveform. If DC supply value is 2E then capacitor voltage is regulated at E. So output waveform is like $0, \pm E, \pm 2E, \pm 3E$.The main point is using all the possible combinations of DC source and capacitor as two DC links. Fig. 3.6, presents single phase single DC source CHB inverter.

Output load voltage v_0=v_1+v_2

Where v_1 , v_2 $are\ cell\ voltages$

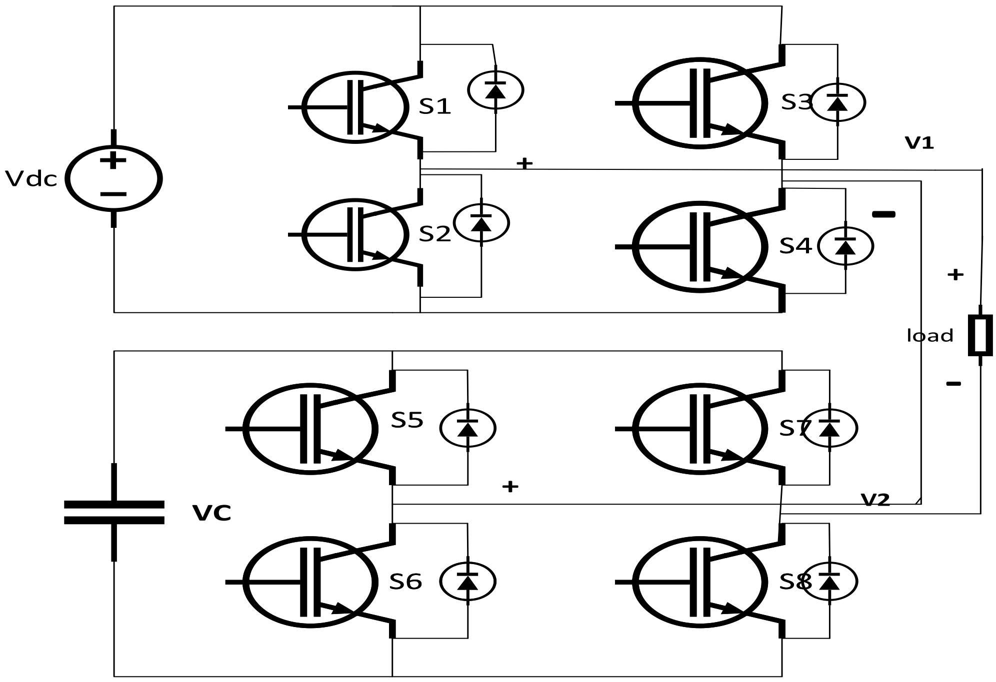


Figure 3.6: Single-phase single DC source seven-level CHB inverter

Here suppose $v_{dc} = 2E$ and capacitor voltage is regulated at $v_c = E$

$s_i = \{0|\ if\ s_i\ is\ off\ i = 1,2 \ldots 8\ \}$

$s_i = \{1|\ if\ s_i\ is\ on\ i = 1,2,3 \ldots 8\ \}$

The complementary switches can be realized as following.

$$\begin{cases} s_2 = \overline{s_1} = 1 - s_1 \\ s_4 = \overline{s_3} = 1 - s_3 \\ s_6 = \overline{s_5} = 1 - s_5 \\ s_8 = \overline{s_7} = 1 - s_7 \end{cases}$$

$$v_1 = (s_1 - s_3)v_{dc} = (s_1 - s_3)2E \quad (3.10)$$

$$v_2 = (s_5 - s_7)v_c = (s_5 - s_7)E \quad (3.11)$$

Table-3.3 Switching states of single phase single DC source seven-level CHB inverter

State	s_1	s_2	s_3	s_4	s_5	s_6	s_7	s_8	v_1	v_2	v_0
1	1	0	0	1	1	0	0	1	$+2E$	$+E$	$+3E$
2	1	0	0	1	1	0	1	0	$+2E$	0	$+2E$
3	1	0	0	1	0	1	1	0	$+2E$	$-E$	$+E$
4	1	0	1	0	1	0	0	1	0	$+E$	$+E$
5	1	0	1	0	1	0	1	0	0	0	0
6	0	1	0	1	0	1	1	0	0	$-E$	$-E$
7	0	1	1	0	1	0	0	1	$-2E$	$+E$	$-E$
8	0	1	1	0	0	1	0	1	$-2E$	0	$-2E$
9	0	1	1	0	0	1	1	0	$-2E$	$-E$	$-3E$

The redundancy switching states are mentioned in the above table. Redundant switching state 3&4 or 5&6 are used for capacitor voltage balancing. State 3&7 responsible for charging the capacitor whereas 4&6 do the discharging job. It is found that states 2,5&8 don't contribute to capacitor voltage. The charging and discharging phenomena of capacitor depends on time constant. Table 3.4 presents switching effect on capacitor.

Table-3.4 Switching effect on capacitors

State	v_1	v_2	v_0	Effect on Capacitor
1	$+2E$	$+E$	$+3E$	Discharging
2	$+2E$	0	$+2E$	No effect
3	$+2E$	$-E$	$+E$	Charging
4	0	$+E$	$+E$	Discharging
5	0	0	0	No effect
6	0	$-E$	$-E$	Discharging
7	$-2E$	$+E$	$-E$	Charging
8	$-2E$	0	$-2E$	No effect
9	$-2E$	$-E$	$-3E$	Discharging

3.4.4 Modified Three Phase Hybrid CHB MLI

Here the suggested three-phase hybrid CHB multilevel inverter comprises of a conventional 3-leg inverter and H-bridge inverters in cascading with inverter leg is implemented. The proposed model will produce five-level in per phase voltage wave form and nine levels in line to line wave form. The mathematical analysis is similar to single phase hybrid topology presented above. The model is presented in fig 3.7

Output load voltage $v_0=v_1+v_2$

Where v_1 , v_2 $are\ cell\ voltages$

Here suppose $v_1= 2E = v_{c1} + v_{c2}$ and $v_{m2}= E = v_2$.

v_{c1} , v_{c2} are capacitor voltages

Then the half bridge inverter will yield $\pm E$ and full-bridge inverter will produce $\pm E, 0$. So the five level output wave will be generated like $\pm 2E, \pm E, 0$.

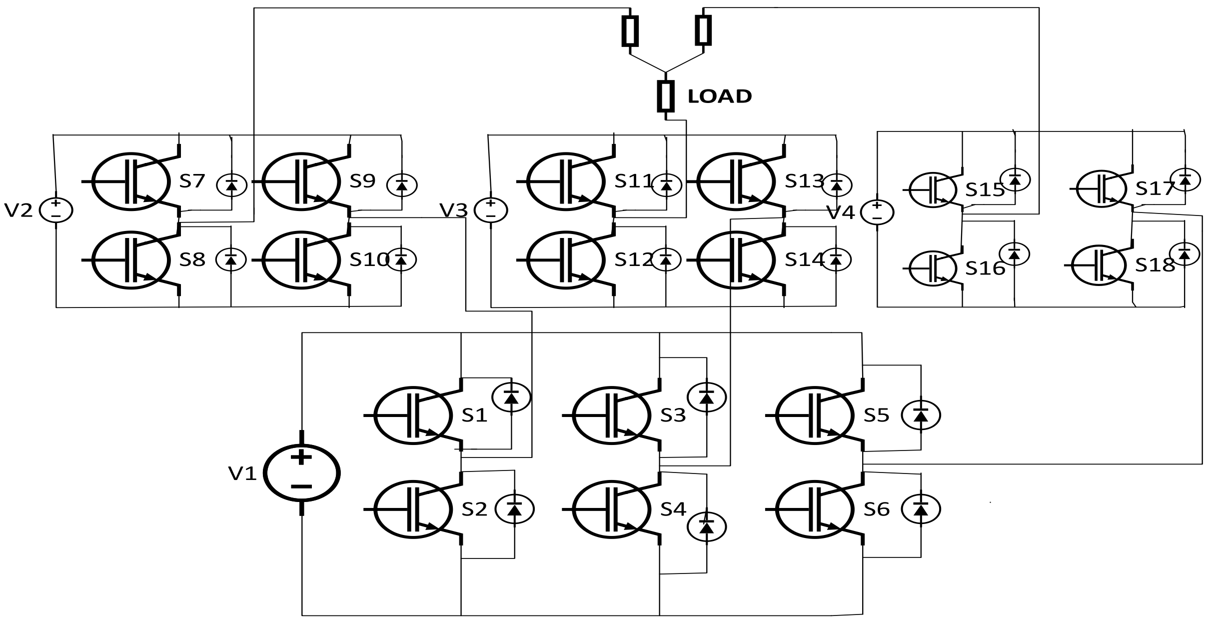


Figure 3.7: Three phase modified hybrid CHB MLI

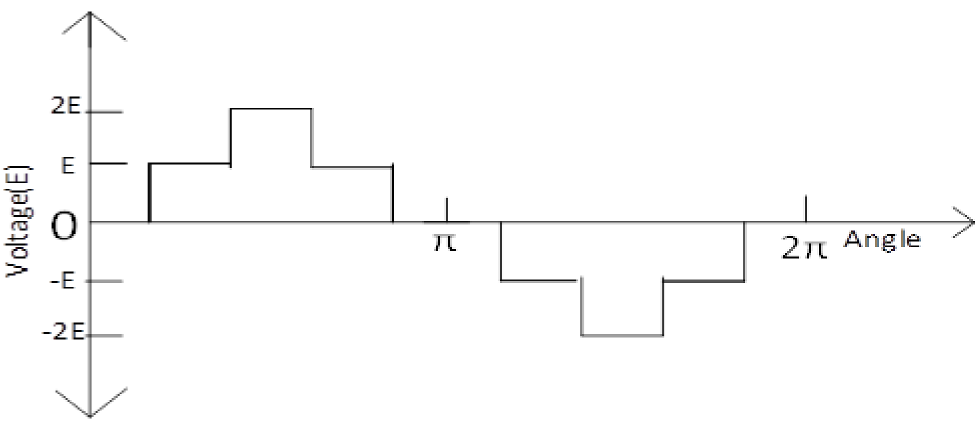


Figure 3.8: Output voltage waveform of single-phase five-level hybrid CHB MLI

3.4 Modulation Technique

PWM is most popular method of controlling the output voltage. It is achieved by adjusting the on off period of inverter switches. It eliminates lower order harmonics. The higher order harmonics can be easily filtered out with the help of LC filter. Different modulation schemes like SPWM, SHE-PWM, SVM have been used for MLI power converters. SPWM is the most popular method amongst all. The basic SPWM may be unipolar or bipolar. In bipolar the switching pulse can be generated by comparing reference sinusoidal signal with high frequency triangular wave. The unipolar needs two sinusoidal signals of 180 degree out of phase. The output waveform changes between 0 to $+v_0$ and between 0 to $-v_0$ during the positive and negative half-cycle respectively. The multicarrier PWM scheme categorized into two and here we will greatly deal with multicarrier SPWM.

(1) phase shifted multicarrier SPWM

(2) level shifted multicarrier SPWM.

3.4.1 Level Shifted Multicarrier SPWM

In order to generate $m\ levels$ $m-1$ carrier signals are vertically shifted to each other. A level-shifted PWM can be classified into following types.

(1) Phase-Disposition: In phase disposition all the carrier signals are in same phase. Modulation Index= $M = \frac{2v_{ref}}{(m-1)v_{tri}}$

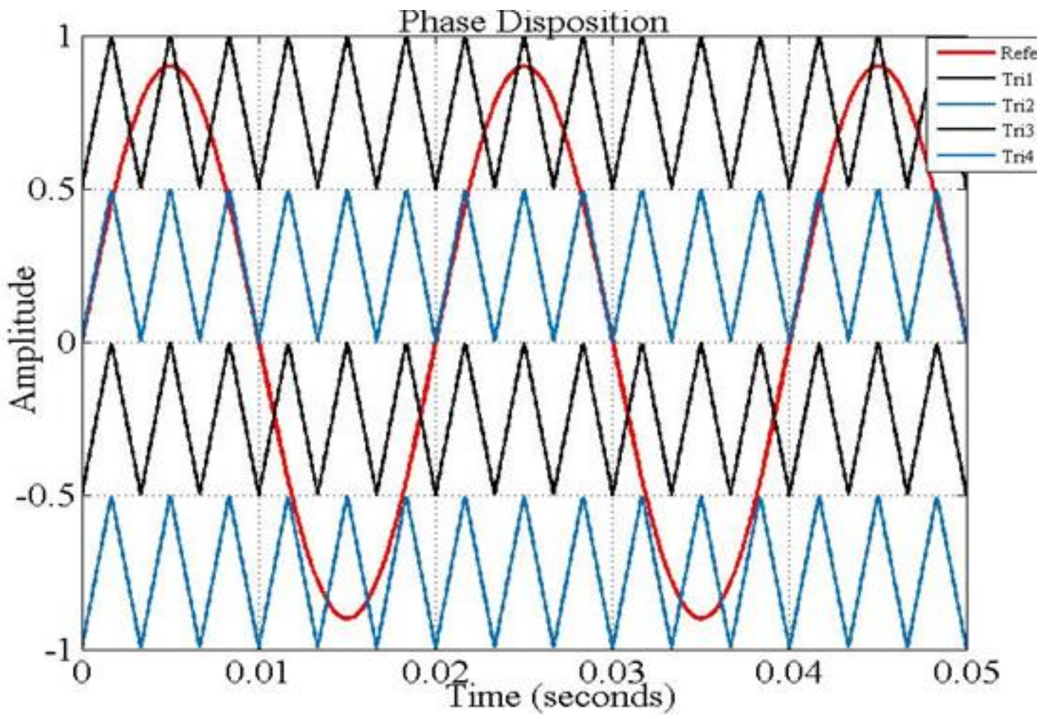


Figure 3.9.: Phase disposition PWM

(2) Phase Opposition Disposition (POD-PWM): In this case all the high frequency carrier waves above the zero are out of phase with those below the zero by 180°.

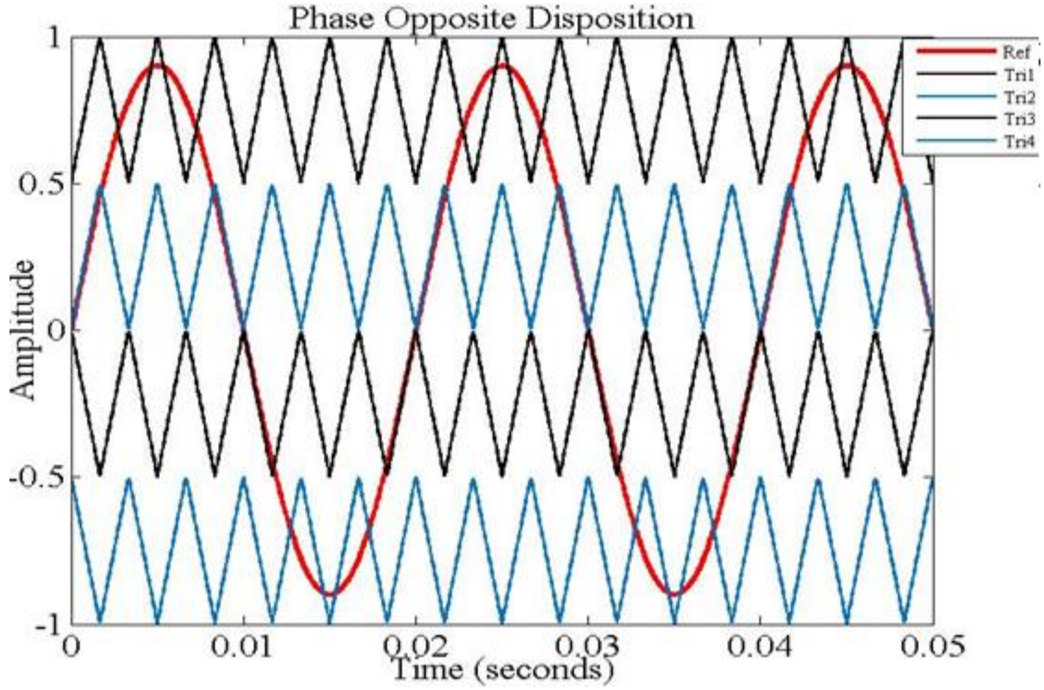


Figure 3.10: Phase opposition disposition PWM

(3) Alternative-Phase-Opposition-Disposition (APOD-PWM): In APOD all the adjacent carrier signals are out of phase by 180º.

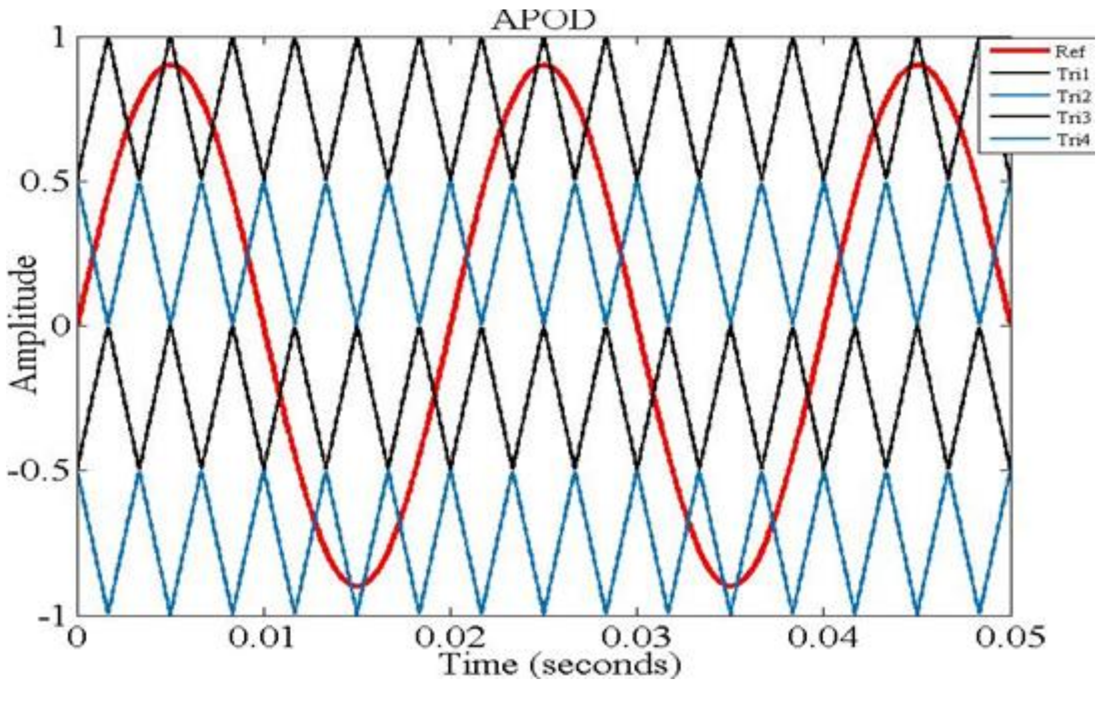


Figure 3.11: Alternative phase opposition disposition PWM

Here for m level generation $m-1$ level shifted triangular carrier waves are needed. In order to generate switching pulses a high frequency triangular carrier signal v_{tri} is compared with sinusoidal reference wave v_{ref} in a comparator.

Mathematically $\begin{cases} If\ v_{ref} \geq v_{tri}\ then\ 1 \\ else \qquad\qquad\qquad 0 \end{cases}$ (3.12)

$where\ v_{ref} = Peak\ value\ of\ refence\ signal\ ,\ v_{tri} = Amplitude\ of\ triangular\ signal$

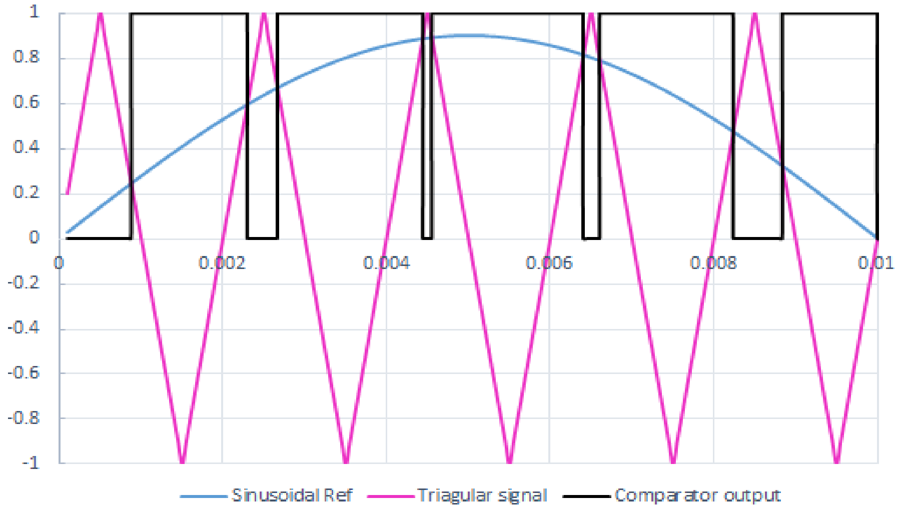


Figure 3.12.: Comparator output

In case of bipolar SPWM, if the $v_{ref} \geq v_{tri}$ then the top device of first leg is on else the bottom device. As the top and bottom switches of the same inverter leg are complementary in nature. But in case of unipolar SPWM two sinusoidal reference signals are required to produce switching pulses. The reference signals are of same magnitude, frequency and 180° out of phase. In case of multicarrier technique, the carriers from top to bottom produce switching pulses related with highest possible voltage level to lowest. Figure 3.13 presents the switching pulses for five level hybrid MLI. Here four level shifted carrier waves(Cr_1 , Cr_2, Cr_3, Cr_4) are compared with sinusoidal reference signal to generate the switching pulses. The table-3.1 presents switching states of hybrid five level CHB MLI inverter. From the figure 3.13 the level 1 switching pulses are fired to switches (s_1, s_3, s_6) to generate voltage $+2E$ .Similarly level 2 is responsible to produce voltage $+E$ .Then pulse levels(3,4,5) produce voltage 0,$-E$,$-2E$ at the output respectively. Here $T_{PWM} = v_{ref} \times T_{tri}$, $0 \leq v_{ref} \leq 1$ $T_{PWM} = Width\ of\ PWM\ signal$,$T_{tri} = Period\ of\ Triangle\ wave$.

Here$N = \frac{f_{tri}}{2f} = pulses\ per\ half\ cycle,\ f_{tri} = frequency\ of\ carrier\ , f = reference\ signal\ frequency$ .If triangular wave matches with zero of reference signal then $N - 1\ pulses\ per\ half\ cycle$.Modulation index $= M = \frac{v_{ref}}{v_{tri}}$, Modulation index controls harmonics in output and fundamental voltage value in the MLI.

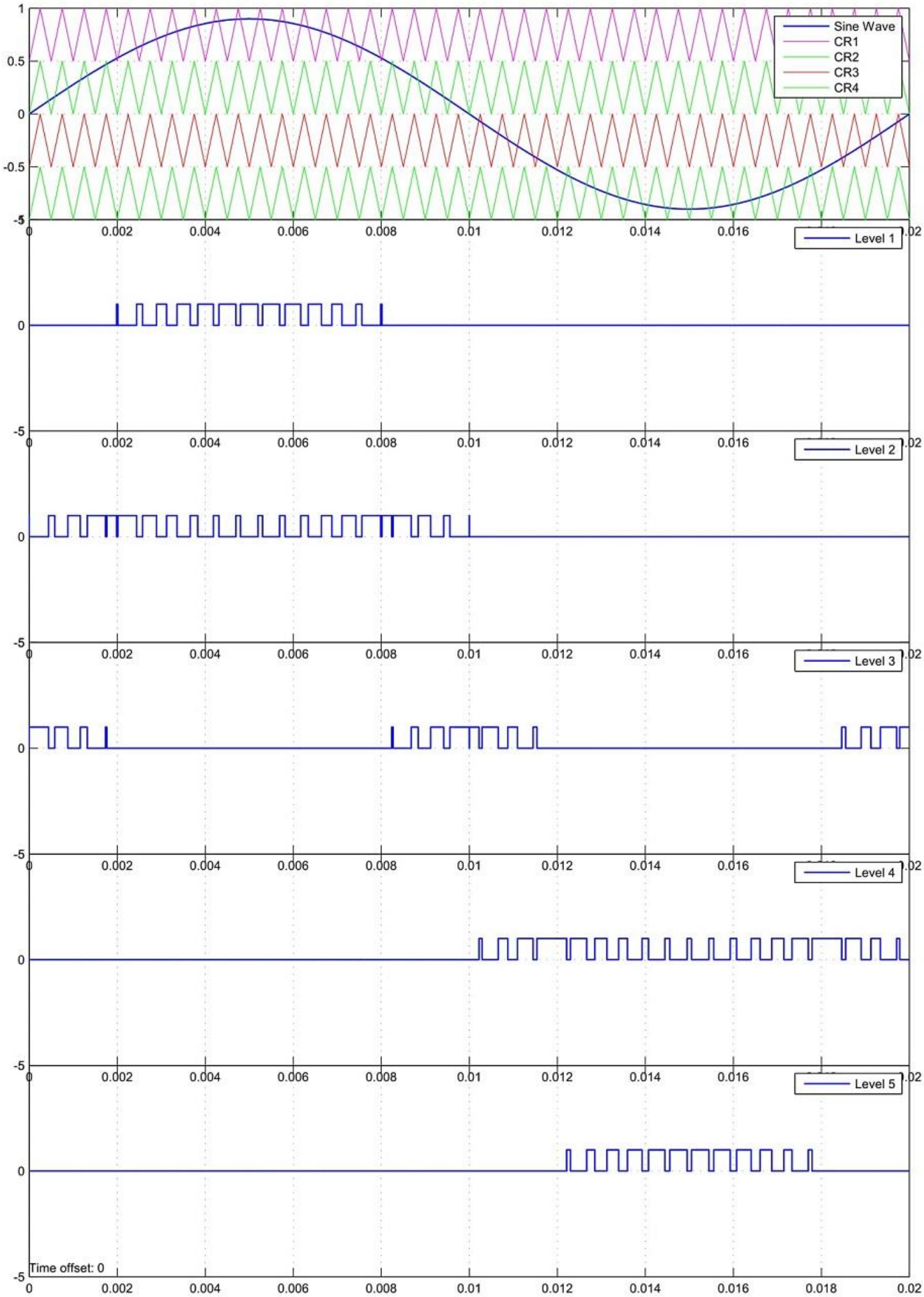


Figure 3.13.: Switching pulses for five level MLI

3.5 Induction Motor Modeling

An induction motor is an AC asynchronous motor which operates on the principle of electromagnetic induction. Due to recent advancement in power electronics induction motor is largely used in electric drives and various applications. It may be either

- wound rotor type
- squirrel-cage rotor type.

In order to produce rotating magnetic field the stator winding of induction machine must be balance i.e. displaced 120° in space and current must be time displaced by 120°.The rotating torque is produced due to the interaction between stator poles and rotor poles. Due to advancement in power electronics various method of speed control for induction machine is developed. Various popular methods of speed control are given below.

3.5.1 Variable Rotor Resistance Method

This technique is used for speed control of wound rotor motor. The external resistance(r_e) would be inserted to rotor circuit during loading condition. This greatly rises the starting torque and decreases the starting current. By choosing suitable value of resistors, the maximum torque can be achieved at starting. It fulfills the requirement of high starting torque. This drive is constant torque variable power drive. The external resistance(r_e) causes additional power losses .

3.5.2 Variable Stator Voltage

The torque produced in an induction motor is proportional to the square of the supply voltage. So by changing the voltage across stator winding, the speed would be controlled. This method is used for narrow range of speed control.

3.5.3 Constant V/f Control

Here the variation of stator voltage and frequency in such a way that ratio $\frac{v}{f}$ remains constant. So by keeping voltage and frequency ratio constant the torque and flux can be maintained throughout the speed range.

Here we will perform direct torque control of an induction motor. It is open loop speed control.

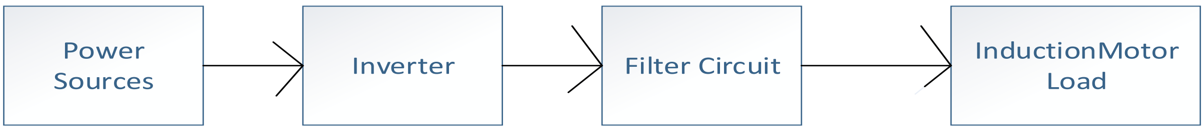


Figure 3.14.: Basic block diagram of proposed system

3.5.4 Induction Motor Analysis

As the three phases system is balanced, the study can be performed by considering only one phase. Figure 3.13. presents the per phase equivalent circuit below:

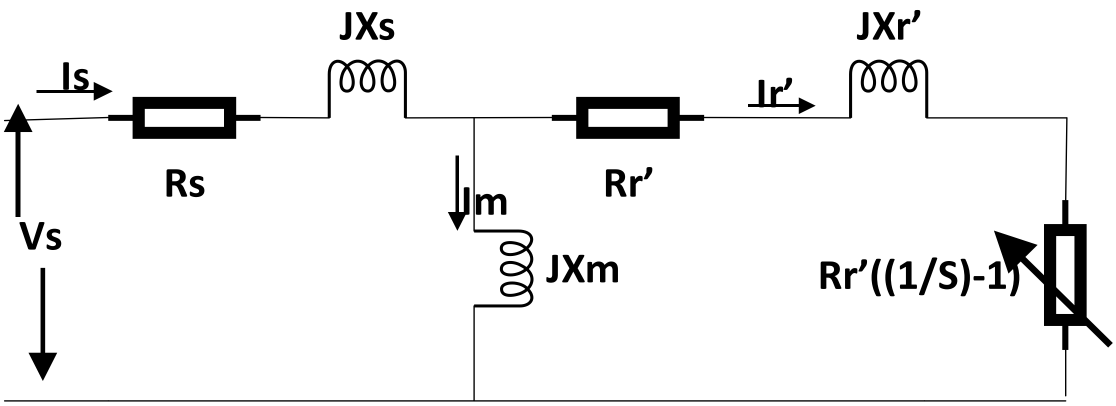


Figure 3.15: Per phase equivalent circuit of induction motor

The Stator circuit parameters are Resistance (R_s), Leakage reactance (X_s)

The rotor circuit parameters are Resistance (R_r), Leakage reactance (X_r).

$X_m = Magnetic\ reactance\ \ , V_s = Supply\ voltage\ \ , I_s = Stator\ current$

$I_r = Rotor\ current\ \ , R_{r'}\ \ X_{r'}\ \ Rotor\ parameter\ referred\ to\ stator\ side$

Now synchronous speed $N_s = \frac{120F}{P}\ \ RPM\ \ where\ F = supply\ frequency$

$P = number\ of\ poles\ per\ phase.$ Slip $S = \frac{N_S - N_r}{N_S}\ \ where\ N_r\ is\ rotor\ speed.$

Air gap power $P_g = \frac{3{I_r}^2 R_r}{S}$ (3.13)

Rotor cupper loss $P_{cu} = 3\ {I_r}^2 R_r$ (3.14)

Net mechanical power $P_m = P_g - P_{cu}$ (3.15)

Torque developed $T_m = \frac{P_m}{w_r}$ (3.16)

$w_r = Rotor\ spped\ in\ rad/sec\ , T_e = Electromagnetic\ Torque$

3.6 LC Filter Design

The filter circuit is used to reduce voltage harmonics and current distortion there by increases power quality. Due to inverter operation the high switching harmonics are introduced into the system. So an LC low pass filter is designed in accordance to IEEE standard. A low pass filter allows to pass lower frequency signal and attenuates signal above the cutoff frequency. In second-order filter the attenuation is at -40 DB/dec .

$Second\ order\ Tranfer\ function\ \ H(s)=\frac{w_n{}^2}{s^2+2\xi w_n s+w_n{}^2}$ (3.17)

$s = Laplce\ operator\ , w_n = Natural\ frequency\ in\ rad/sec\ \ , \xi = Damping\ ratio$

$let\ \xi = 0.707\ , Quality\ factor\ Q = 1/2\xi\ and\ \xi = \alpha/w_n\ , \alpha = 0.2 = attenuation\ rate$

From LC circuit Mathematics

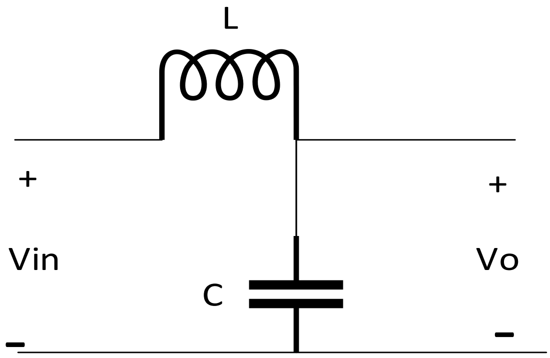


Figure 3.16: Per phase series LC circuit

$\frac{V_o}{V_{in}} = H(s) = \frac{(1/LC)}{s^2+s\ (R/L)+(1/LC)}$ (3.18)

$Where\ L = inductance\ , C = capacitance, R = internal\ resiatance\ of\ inductor$

$From\ \ Eqn\ 3.17\ and\ 3.18\ Q = \frac{1}{R}\sqrt{\frac{L}{C}}\ \ \ and\ \ w_o = resonant\ frequency = \sqrt{L/C}$

During filter design several conditions are taken care of such as switching frequency, filter size, load parameters, voltage drop etc. The constraints are required for the design:

$V_{LL} = E_n = Line\ to\ Line\ RMS\ Inverter\ output\ \ , V_{ph} = Per\ Phase\ \ RMS\ Output\ ,$

$P_n = Rated\ active\ power\ , V_{DC} = DC\ link\ voltage\ , f_g = Grid\ frequency,$

$f_{sw} = Swiching\ frequency\ , f_o = resonant\ frequency$

$Now\ Z_{base} = base\ impedance = E_n{}^2/P_n$ (3.19)

$C_{base} = base\ capacitance = \frac{1}{w_g Z_b}$ (3.20)

$C_f = filter\ capacitance = 0.05C_b \pm 5\%\ where\ 10f_g < f_o < 0.5f_{sw}$ (3.21)

$ripple\ in\ current = \Delta I_l = \frac{2V_{dc}(1-m)mT_{sw}}{3L_a}$

It is studied[26] that maximum peak-to-peak $load\ current\ ripple\ is\ produced\ at\ m = 0.5$

$\Delta I_{lmax} = \frac{V_{dc}}{6f_{sw}L_a}\ \ \ at\ m = 0.5$

$ripple\ in\ current = \Delta I_l = \frac{3V_{dc}}{50f_{sw}L_a}\ \ , m = 0.9$

$m = modulation\ index, T_{sw} = switching\ time\ period\ , L_a = inverter\ side\ inductance$

Here 10% ripple of the rated current is allowed for filter design $\Delta I_{lmax} = 0.1 I_{rated}$

$$Now = L_a = Filter\ inductance = \frac{3V_{dc}}{50 f_{sw} \Delta I_l} \quad (3.22)$$

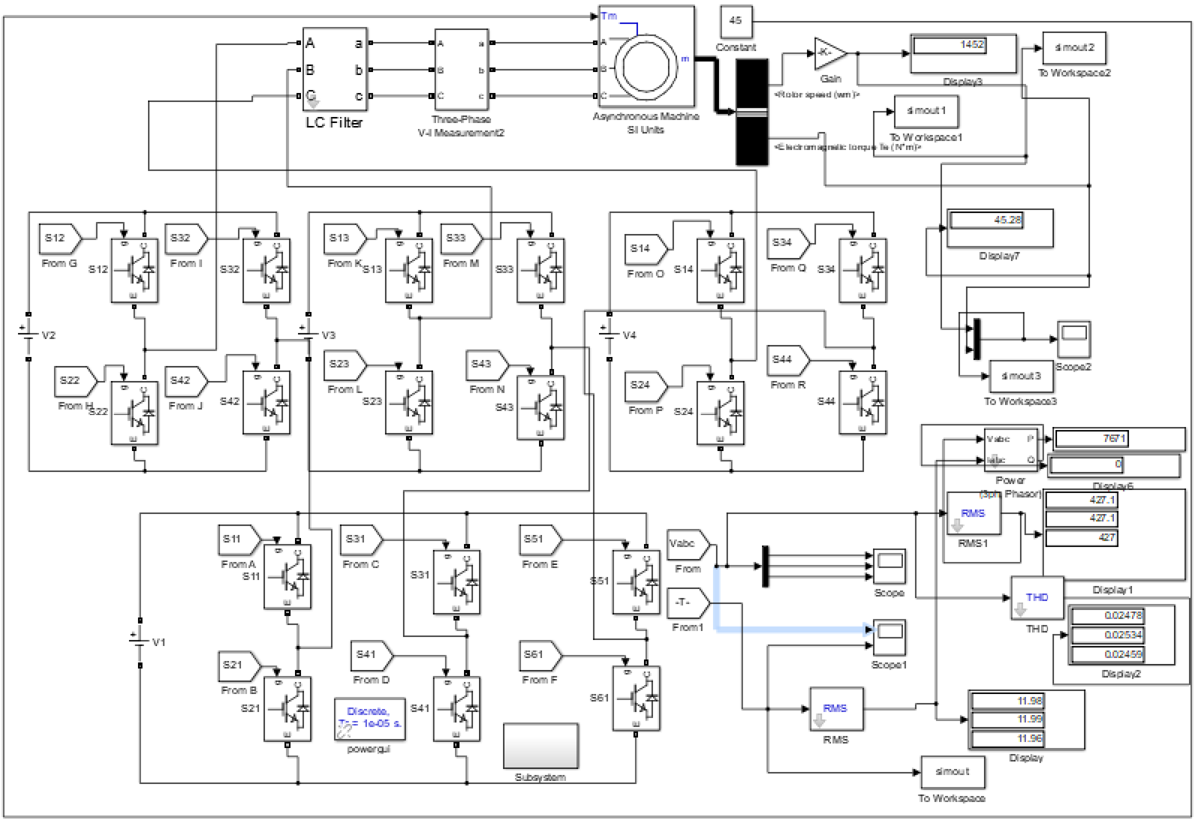


Figure 3.17: MATLAB Simulink model of modified MLI with induction motor load

CHAPTER4

SIMULATIONS AND RESULTS DISCUSSIONS

4.0 Simulation

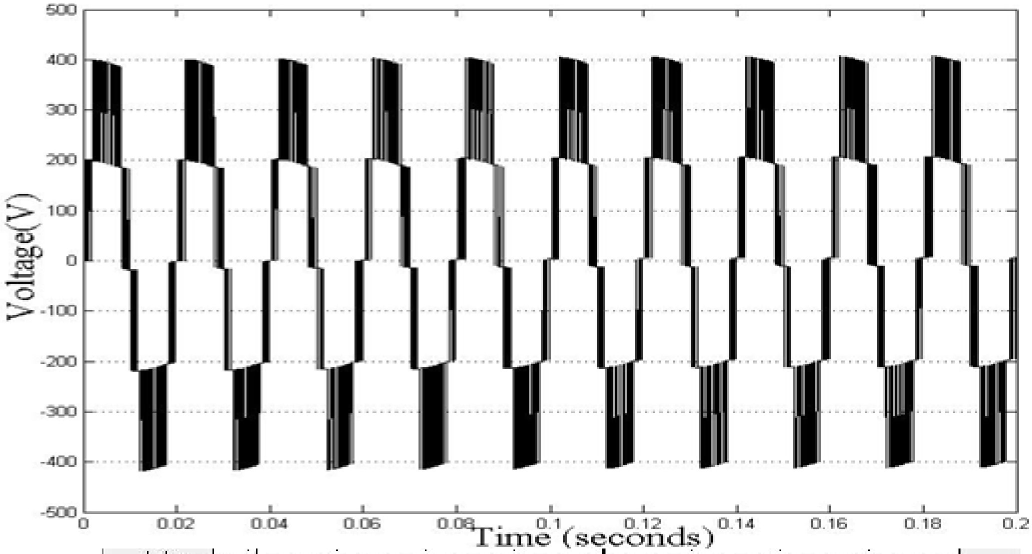
The MATLAB simulation is performed to verify the proposed thesis work. Then comparative analysis of different topologies is done. Parameters like voltage levels, modulation scheme and THD is chosen to analyze the MLIs. To show the performance an induction motor load is simulated with and without filter circuit.

4.1 Simulation of Single-phase Five-level Hybrid CHB Inverter

The five-level hybrid CHB is modelled and simulated based on theoretical concept given in chapter 3. The simulation parameters are listed in table 4.1. Fig. 4.1-4.5 shows the load voltage, THD in voltage waveform, load current, capacitor voltages and load variation effect result without filter. The simulation is performed with phase disposition PWM method. The symmetrical levels in load voltage waveform justify the competence of the system. The THD of load voltage is shown in Fig.4.2. The dominant harmonic order present in waveform is related to switching frequency. Table-4.2 demonstrates modulation index verses THD values for different multicarrier SPWM scheme. The load current contains 1.96% THD. It is observed that while capacitor c_1 is discharging through load then c_2 is getting charged by the DC source and vice-versa. The capacitors have equal voltage values in order to get symmetrical output in voltage waveform. Here the voltage is balanced showing the competence of switching scheme. Finally a study is performed by changing the load from $1Kw$ to $1.2Kw$. It is noted that the load voltage remains constant, load current increases and a change in capacitor voltage waveform. Fig 4.5 shows the load changing results.

Table-4.1 Simulation parameters

Load voltage frequency	$50Hz$
Switching frequency	$2KHz$
Capacitor values(C_1, C_2)	$1\ mF$
DC voltage($v_{m1} + v_{m2}$)	600 volt
Load power	$1kW$
Modulation Index	0.9 (Phase disposition)



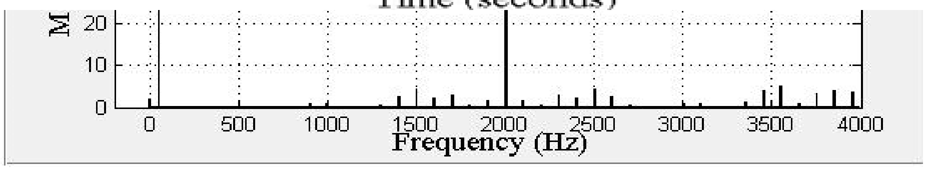


Figure 4.1: Five-level load voltage

Figure 4.2: Harmonic analysis of load voltage

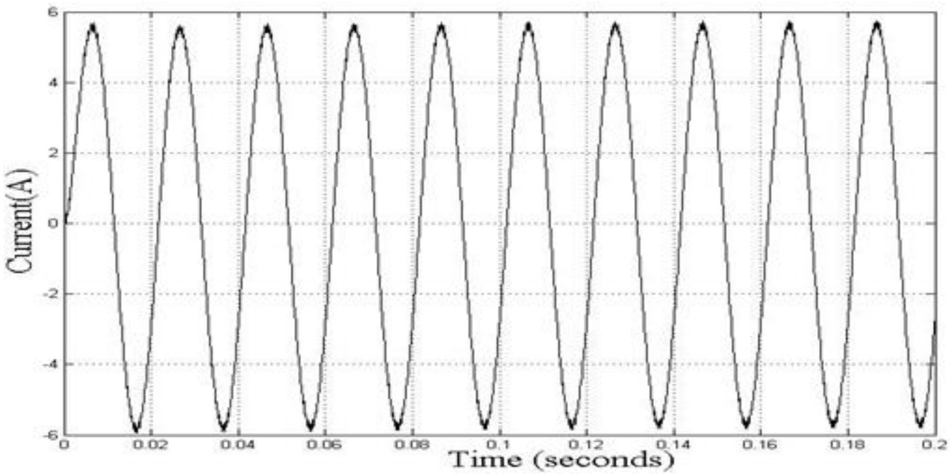


Figure 4.3: Load current waveform

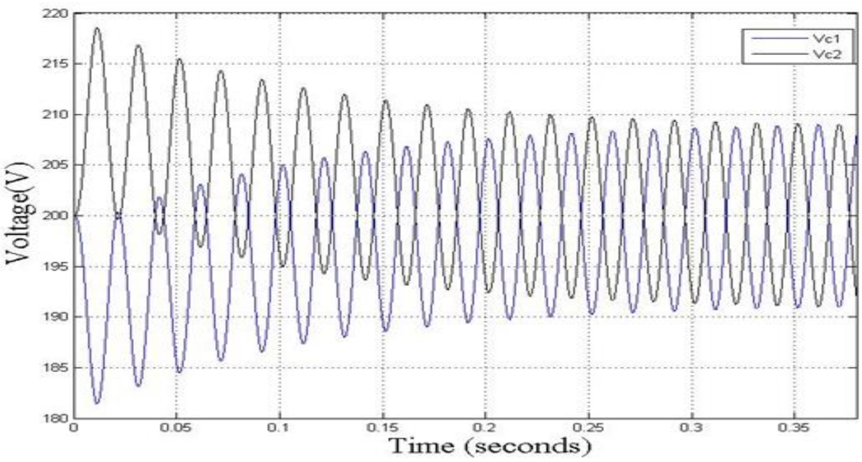


Figure 4.4: Capacitor voltage waveform

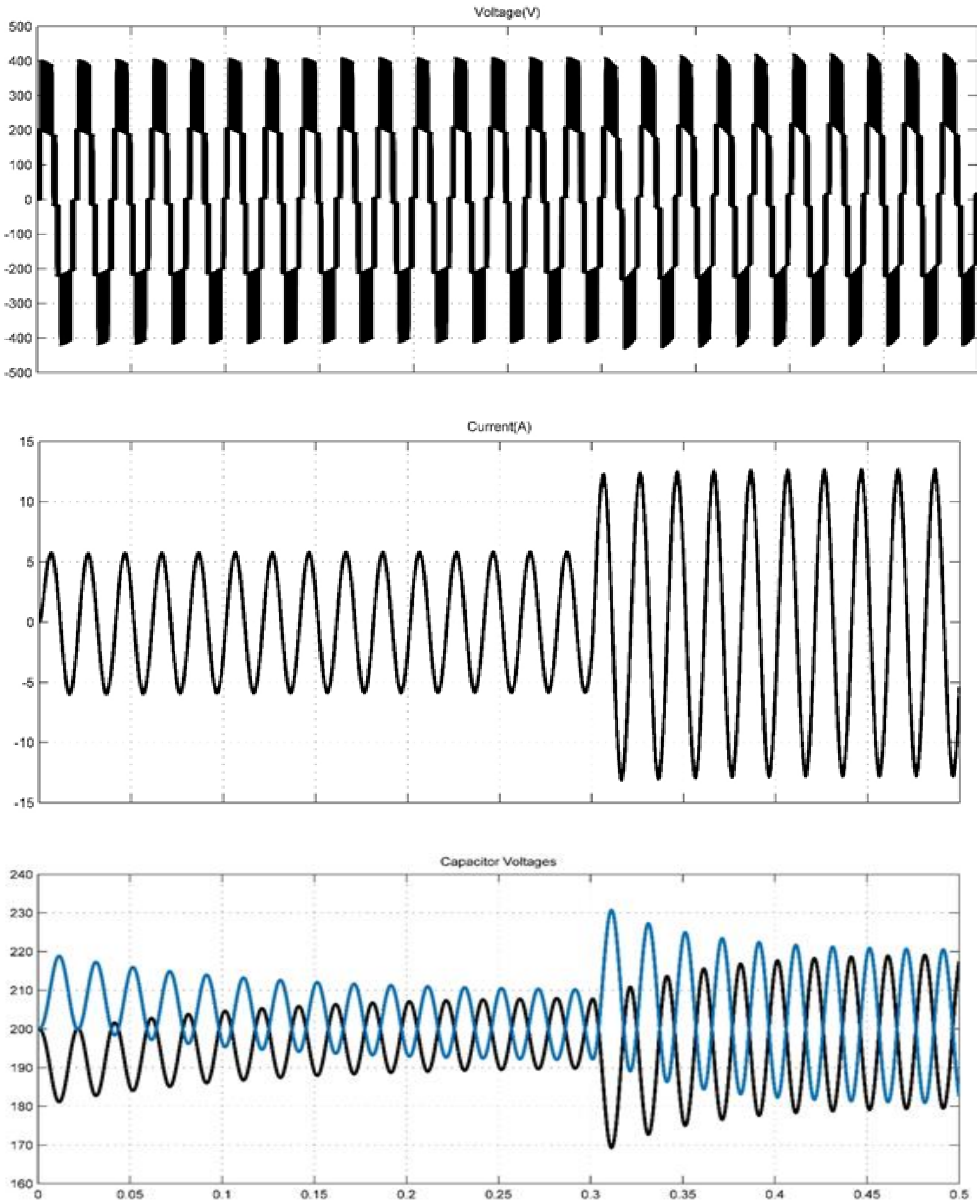


Figure 4.5: Load voltage, current and Capacitor voltages during load changing.

Table-4.2 Modulation index verses THD comparison for five-level inverter

Modulation Index	THD		
	PD	POD	APOD
1	26.07	26.83	27.23
0.95	29.58	30.04	30.33
0.9	32.90	33.04	33.20
0.85	35.41	35.57	35.42
0.8	37.66	37.92	38.05

4.2 Simulation of Single-phase Seven-level hybrid CHB Inverter

The seven-level hybrid CHB is designed and simulated similar to five-level CHB. The simulation parameters are almost same that of five-level listed in table 4.1 except the DC input. Here the DC value is 500 volts like $v_{m1} = v_{m2} = 200v$, $v_{m3} = 100\ v$. Fig. 4.6-4.9 shows the load voltage, THD in voltage waveform, load current, capacitor voltage results without filter. This inverter produces symmetrical levels in load voltage waveform. The THD of load voltage is shown 21.36% in fig.4.7. It is observed that higher order harmonics contributes to THD significantly. But this can be filtered out easily. The table-4.3 exhibits modulation index verses THD values. The load current contains less than 0.98% harmonics. The control scheme maintains the charging and discharging time of capacitor c_1 , c_2 resulting voltage balancing of capacitors. The system is also adaptive to load changing.

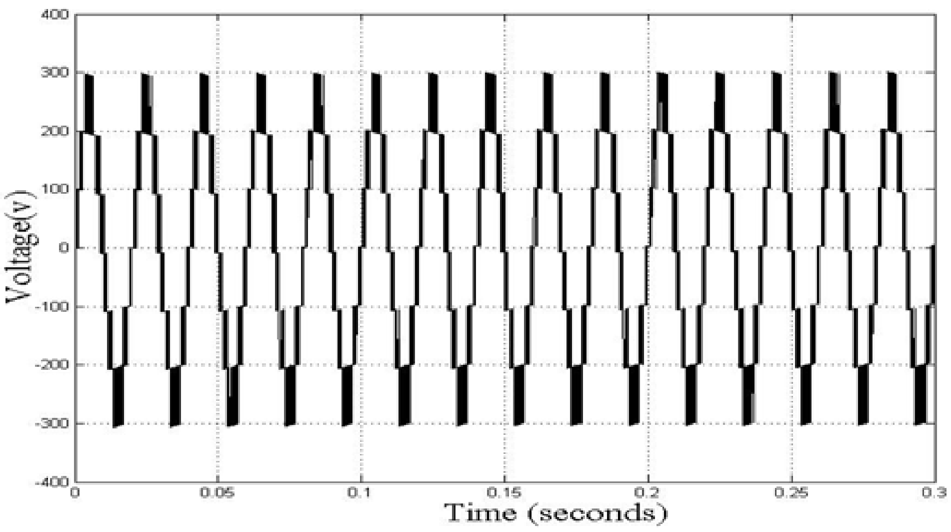


Figure 4.6: Seven-level load voltage

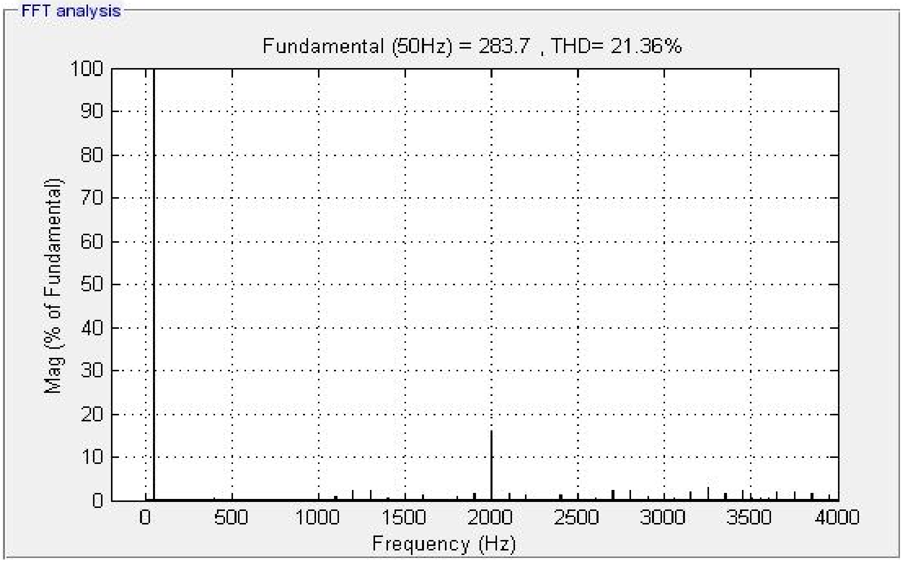


Figure 4.7: Harmonic analysis of load voltage

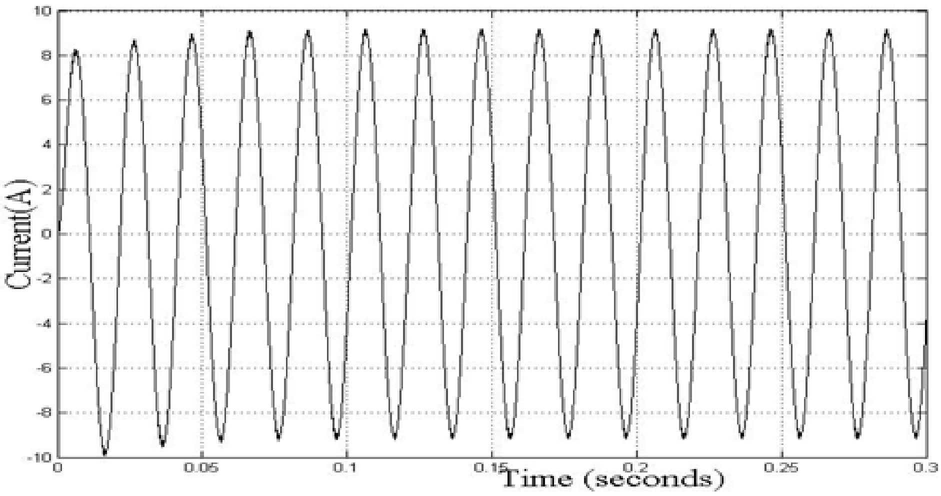


Figure 4.8: Load current waveform

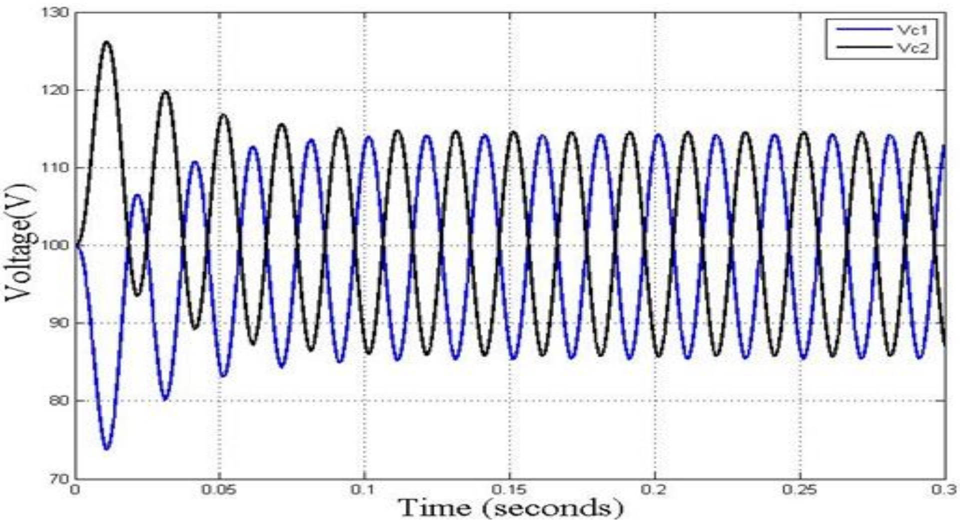


Figure 4.9: Capacitor voltage waveform

Table-4.3 Modulation index verses THD comparison for seven-level inverter

Modulation Index	THD		
	PD	POD	APOD
1	17.33	17.42	17.54
0.95	19.64	19.63	19.29
0.9	21.08	21.36	20.96
0.85	20.40	22.52	22.17
0.8	22.95	23.14	23.06

4.3 Simulation of single DC source seven-level CHB inverter

The seven-level CHB is simulated based on concept presented in chapter 3. The simulation parameters are listed in table 4.4.Fig. 4.10-4.14 shows the load voltage, THD in voltage waveform, load current, THD in current waveform, capacitor voltages result without filter. Fig 4.10 shows the seven-level load voltage output. The capacitor voltage is maintained at half of DC supply. Theoretically the possible voltage levels would be ± 300 , ± 200, ± 100,0 But the result shows little variation due to capacitor charging and discharging phenomena. The relation between modulation index and capacitor voltage is investigated. The modulation index should be properly chosen to get all possible levels in voltage waveform as well as prevents long switching time. So a tradeoff is performed to fix the modulation index and capacitance values. The THD of load voltage is shown in fig.4.11. The dominant harmonic order present in voltage waveform is related to switching frequency. As per IEEE standard individual harmonics values should be limited to 3% of fundamental. Fig 4.12 shows the load current waveform that contains 11.20% THD. A detailed study is presented between switching states and capacitor charging and discharging phenomena. It is noticed form Table-3.3 that switching state 8, 2 and 5 don't contribute to capacitor performance. The switching states 3, 4, 6 and 7 contribute considerably to performance of the system. The switching state 4 and 6 discharges capacitor through load whereas state 3 and 7 charge the capacitor from DC sources. Fig. 4.14 shows the capacitor voltage result. It is settled at 62.42 volt with less than 5% voltage ripple. The system also performs well for load variations. The major draw-backs of this system is the dependency between modulation index and capacitor voltage. Which limits the operation of this configuration at certain modulation index. It would be rectified in future work.

Table-4.4 Simulation parameters

Load voltage frequency	$50Hz$
Switching frequency	$2KHz$
Capacitor values(C_1)	$1\ mF$
DC voltage	200 volt
Load power	$1kW$
Modulation Index	0.85 (Phase disposition)

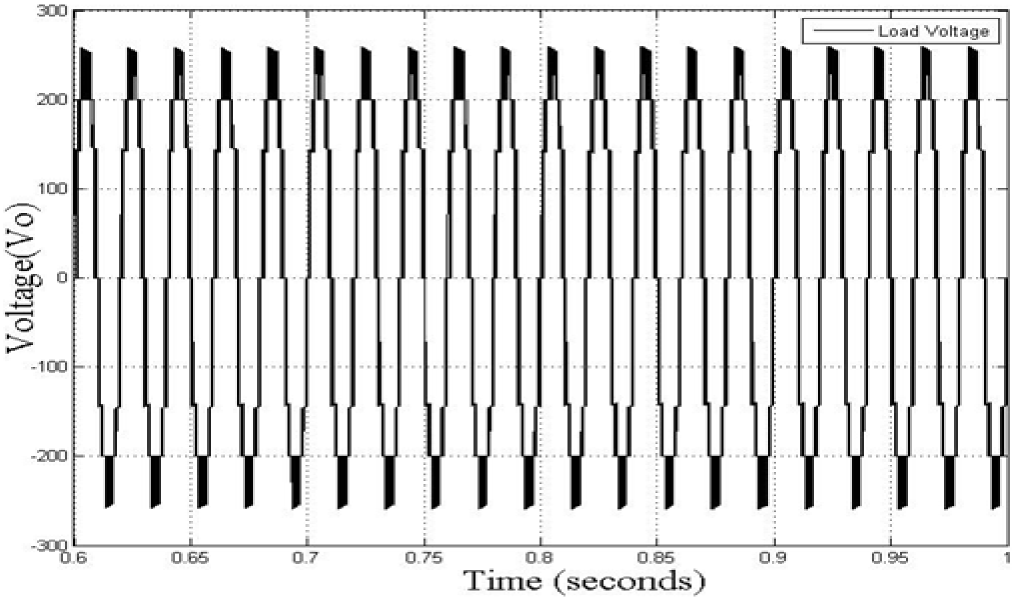


Figure 4.10: Seven-level load voltage

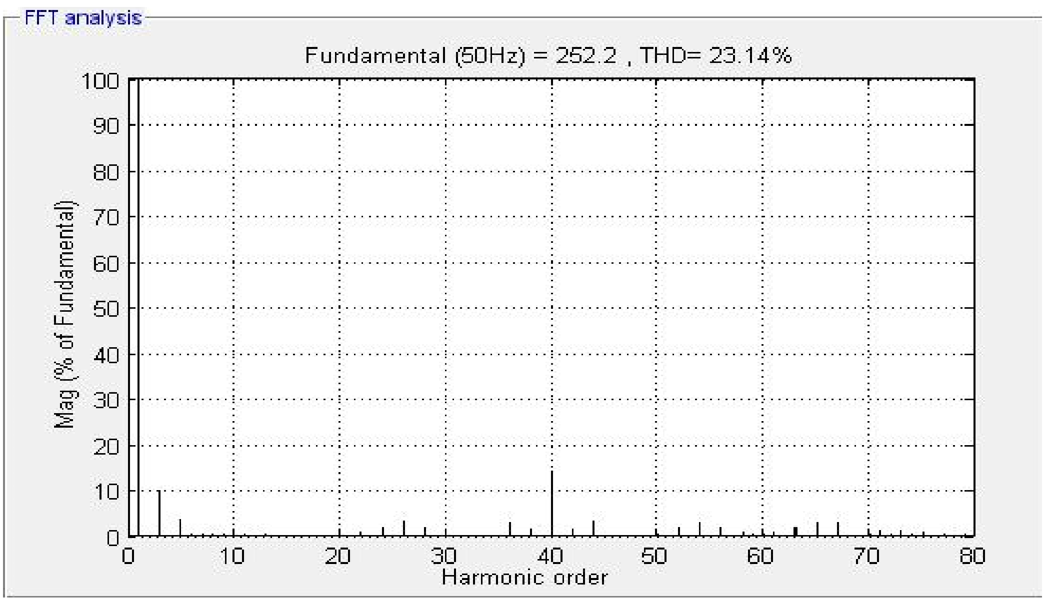


Figure 4.11: Harmonic analysis of load voltage

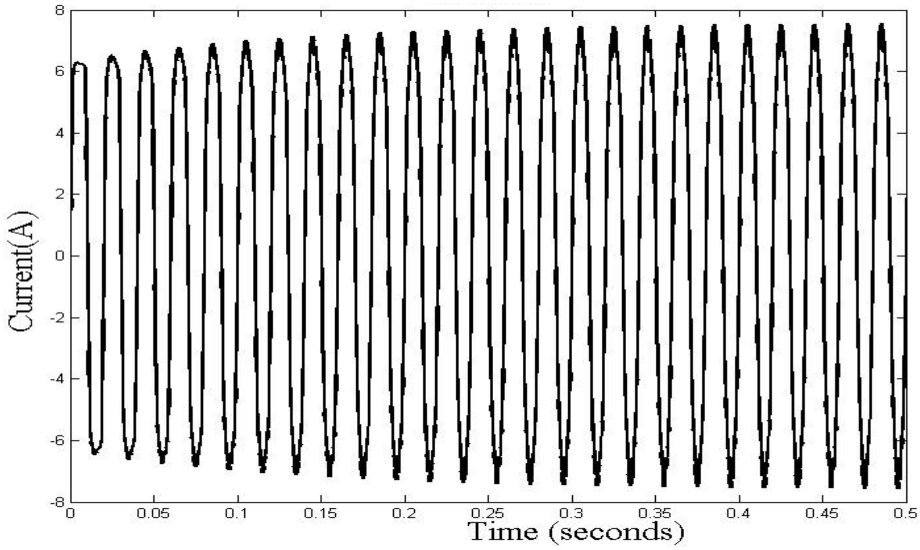


Figure 4.12: Load current waveform

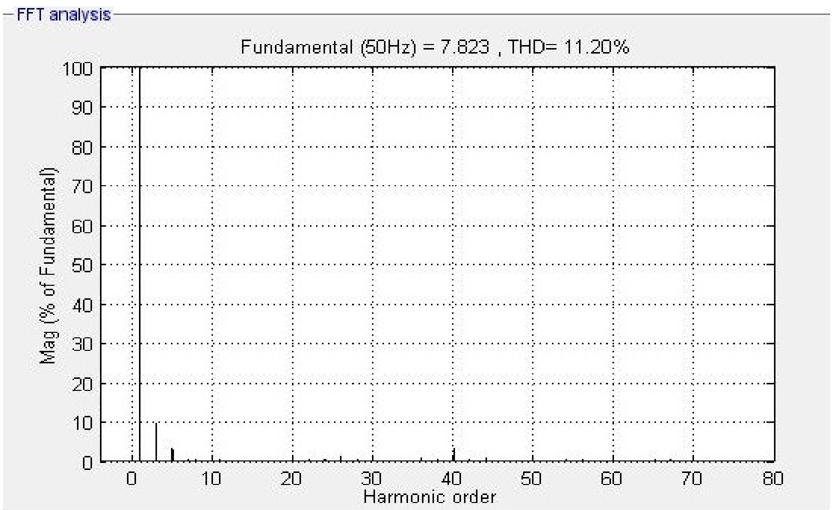


Figure 4.13: Harmonic analysis of load current

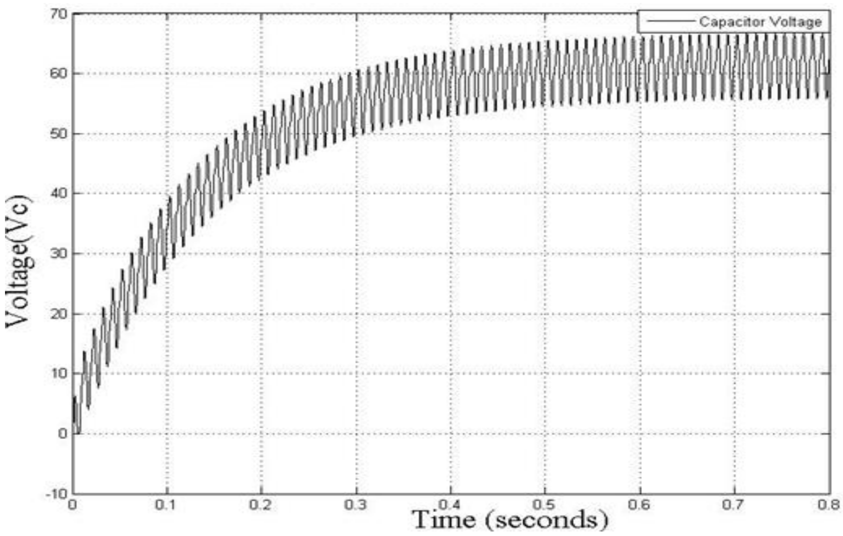


Figure 4.14: Capacitor voltage waveform

4.4 Simulation of Modified Three Phase Hybrid CHB MLI

The five-level modified hybrid three phase CHB is simulated based on concept given above. The simulation parameters are listed in table 4.5. Fig. 4.15-4.22 shows the line-line three phase load voltages, THD in voltage waveform, rotor speed at 90% loading, electromagnetic torque, stator current waveform and speed vs. torque characteristics results without filter respectively. The simulation is performed with phase disposition PWM method. The symmetrical nine levels in line to line load voltage waveform proves the competence of the system. The levels are perfectly balanced like $\pm 800, \pm 600, \pm 400, \pm 200$,0. The proposed model is used to run the induction motor load. The load parameters are listed in table 4.5. The simulation is performed at 90% loading. The direct torque control method is implemented here. The synchronous speed N_s , rated mechanical torque T_m is calculated 49.129 $Nm\ and$ 1500 $RPM\ respectively$.The simulation is performed at T_m=45$N * m$ .It is noted that $T_e = T_m$ during loading. The THD in line-line load voltage is shown in fig.4.16. The dominant harmonic order present in waveform is related to switching frequency. Fig 4.17 shows the rotor speed in RPM. It is found that the model is perfectly verifies the theoretical results and system is balanced. Later on table-4.6 demonstrates torque vs. speed results. Fig 4.18 shows the electromagnetic torque result. Fig 4.19 shows the line-line stator current waveform. It is found that the starting current is very high. In order to limit the staring current without compromising the maximum torque various starting method is there. Fig 4.20 shows the speed vs. torque characteristic. The maximum slip corresponding to maximum torque can also be calculated from Fig 4.20. The starting torque can be marked from the figure 4.20. Fig 4.21 shows the output voltage waveform after using filter circuit. It is noted that that there is drop across filter circuit. A proper tradeoff would be done to minimize losses in future studies. The LC low pass filter circuit parameters are calculated using eqn. 3.21 and 3.22. The THD in voltage waveform is around 2.65% after filtration. Table-4.7 shows a comparison of component requirement among different MLI.

Table-4.5 Simulation parameters

Switching frequency	$2KHz$
DC input($v_1 = 400v, v_2 = v_3 = v_4 = 200v$)	600 volt
Induction motor Load parameters	$7460kW$,$1450RPM, 4\ pole, 50Hz$
Modulation Index	0.9 (Phase disposition)
Filter Parameters	$L_a = 5.13\ mH, C_f = 6\ \mu F, R_f = 5$

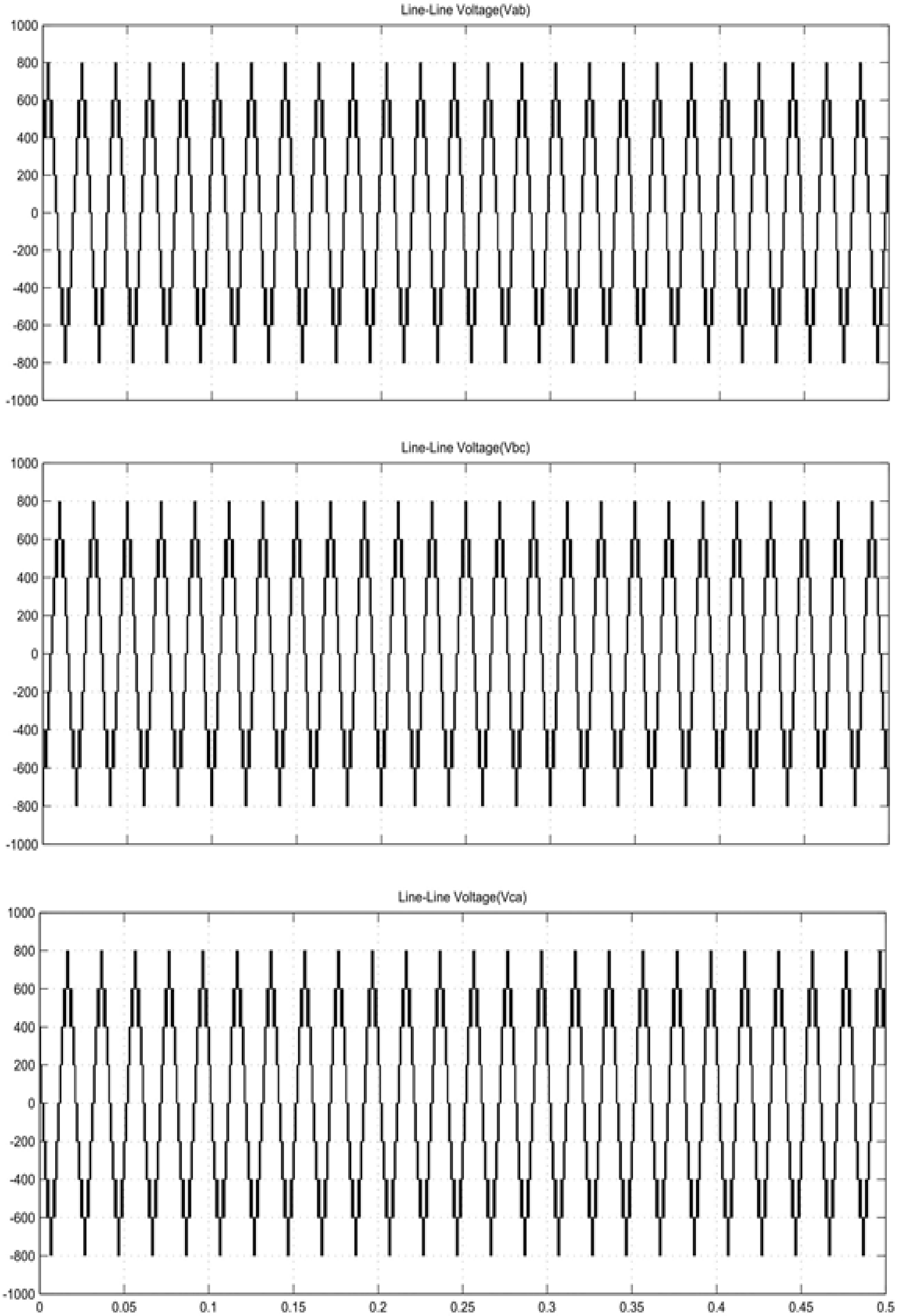


Figure 4.15: Nine-level line- line three phase load voltages

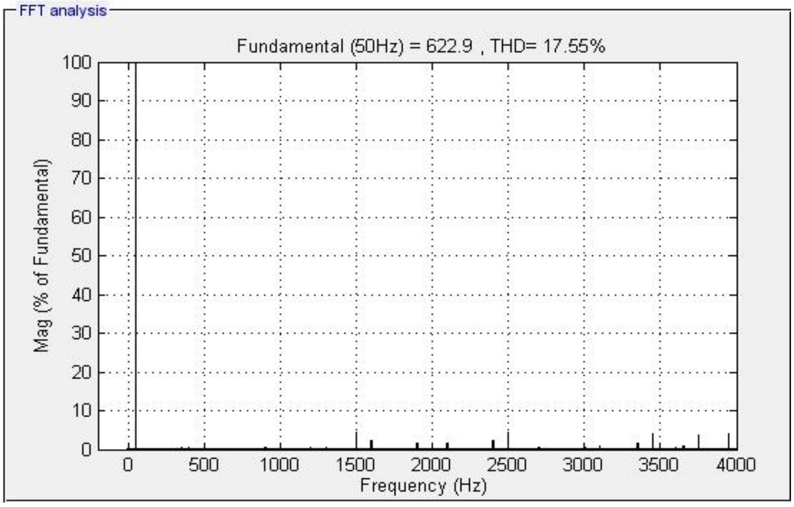


Figure 4.16: THD of line-line load voltage

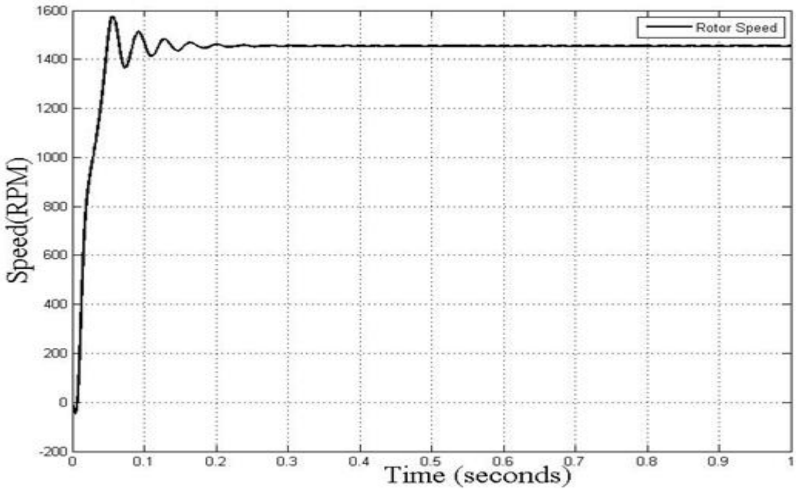


Figure 4.17: Rotor speed variation graph at 90% loading

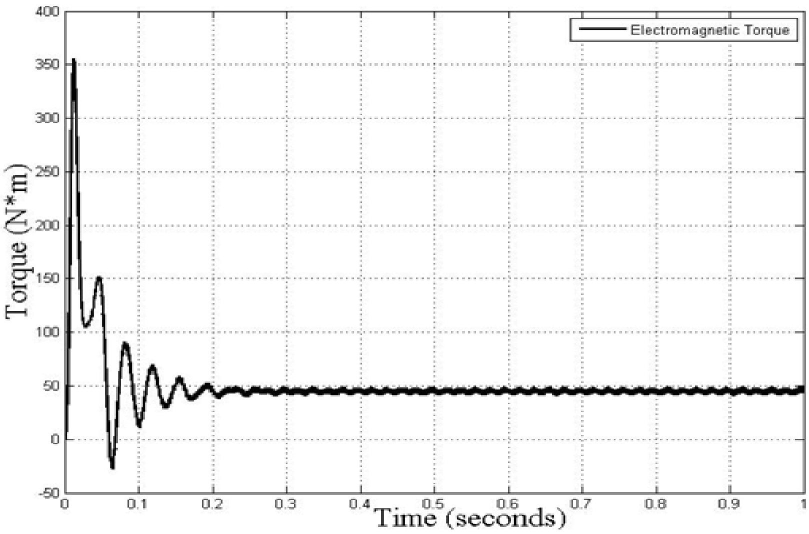


Figure 4.18: Electromagnetic torque graph at 90% loading

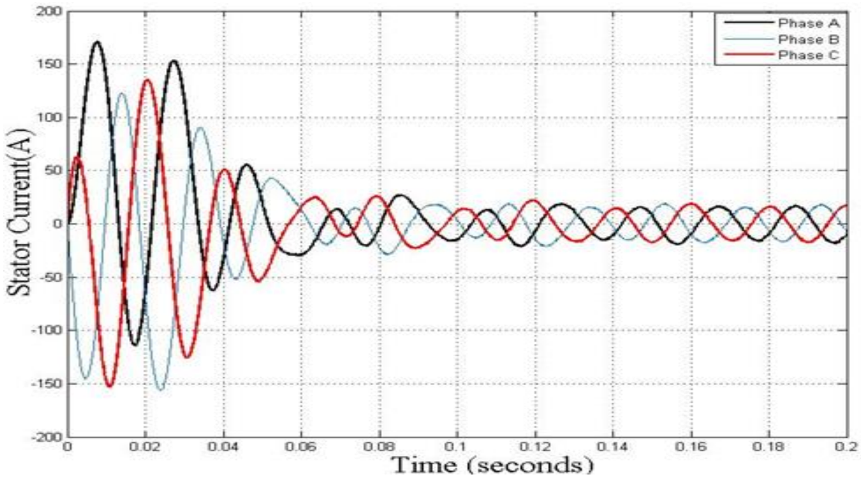


Figure 4.19: Three phase stator current graph

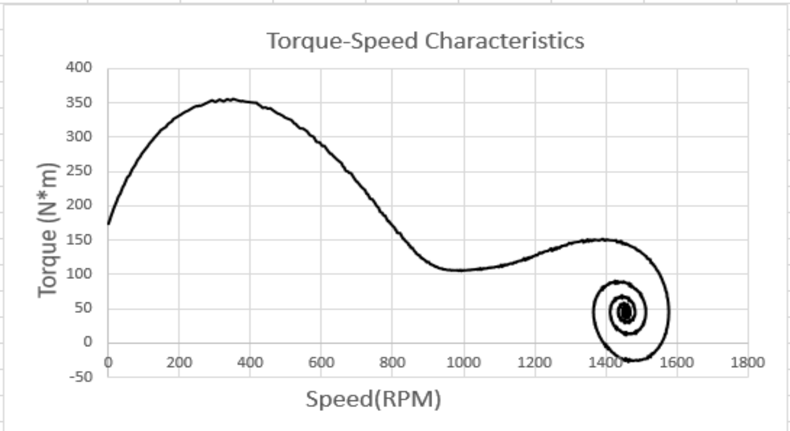


Figure 4.20: Speed verses Torque characteristic at 90% loading

Table-4.6 Load torque verses speed variation simulation result

Torque N*m	Speed in RPM
0	1500
5	1496
10	1491
15	1487
20	1482
30	1472
40	1461

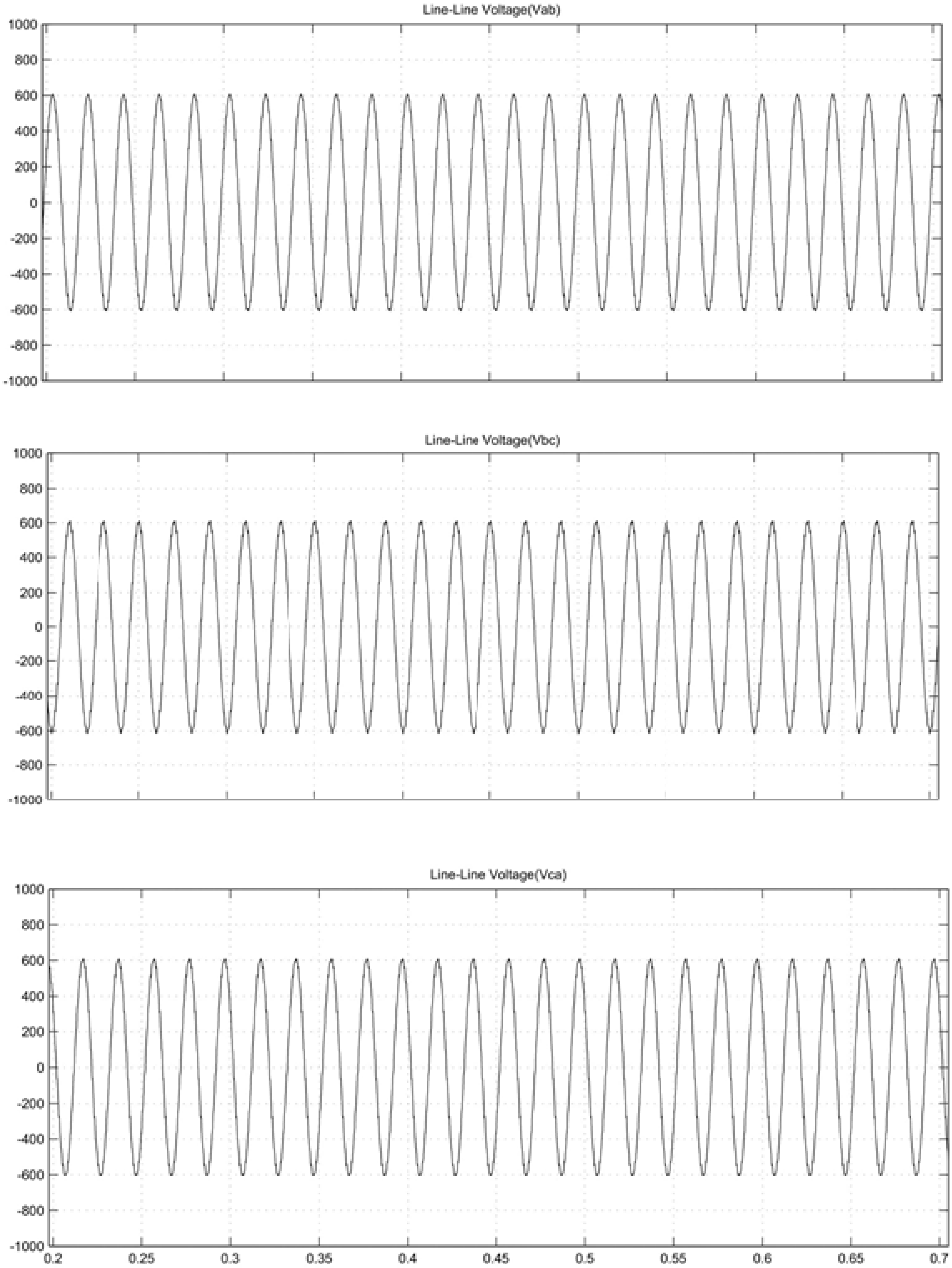


Figure 4.21 Line- Line three phase load voltages after filter circuit

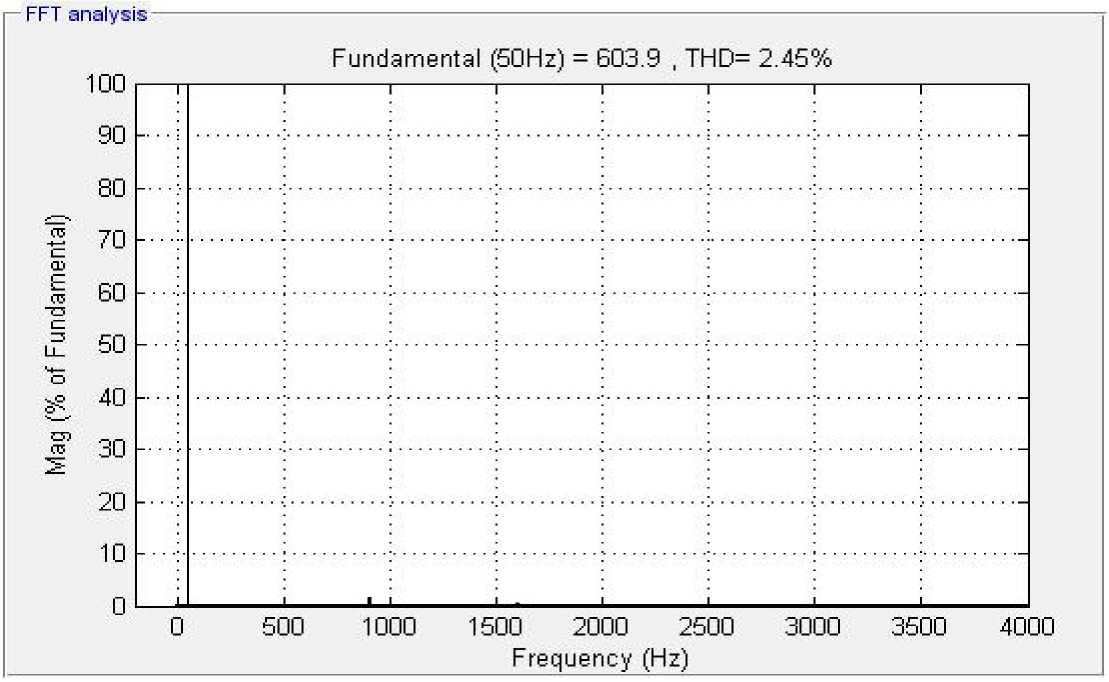


Figure 4.22 THD in voltage waveform

Table-4.7 Comparison of component requirement per phase among different MLI

Converter type	DC bus capacitor	Main switches	Clamping diodes	Balancing capacitor
NPC	m-1	(m-1)*2	(m-1)*(m-2)	0
FC MLI	m-1	(m-1)*2	0	(m-1)(m-2)/2
CHB	(m-1)/2	(m-1)*2	0	0
Hybrid CHB	(m-1)/2	(m-1)*2-2	0	0

CHAPTER5

CONCLUSIONS AND FUTURE WORK

5.0 Conclusion

In this dissertation different Cascaded H-Bridge inverters topologies have been studied and simulated. Firstly, a single phase hybrid five level CHB is implemented by using multicarrier level shifted SPWM. It is further extended to implement single phase seven level hybrid CHB. It is observed that as the number of levels at output increases, THD decreases. These topologies are simulated for different modulation index with PD, POD and APOD SPWM. It is observed that PD technique produced less harmonics at the output. Then single DC source seven level CHB inverter is simulated. Here the dependency between modulation index and capacitor voltage is found. This limits the operation of this model. Then three phase modified hybrid CHB MLI is simulated. The model is implemented to run an 10HP induction motor load. It produced 17.55% THD in the output voltage without filter whereas 2.45% with filter. The torque-speed characteristic of induction motor is verified. Then a comparison between different MLI in terms of component requirement is carried out. It is observed that modified CHB MLI is the most promising alternative for industry application.

5.1 Future work

The modified three-phase MLI using single DC source, three capacitors as storing elements and eighteen switches will be implemented in future work. The dependency between modulation index and capacitor voltage will be rectified. The modulation technique like SHE-PWM and SVM will be implemented. Then close loop speed control of induction motor will be implemented. The potential application of MLI in areas like renewable energy generation, FACTS, AC supplies can be investigated.

REFERENCE

[1] A. Nabae, I. Takahashi, and H. Akagi, “A new neutral-point clamped PWM inverter,” *IEEE Trans. Ind. Applicat.*, vol. IA-17, pp. 518–523, Sept./Oct. 1981.

[2] J.-S. Lai and F. Zheng Peng, “Multilevel converters a new breed of power converters,” *IEEE Trans. Ind. Applicat.*, vol. 32, no. 3, pp. 509–517, May 1985.

[3] F. Z. Peng, J. S. Lai, J.W. McKeever, and J. VanCoevering, “A multilevel voltage-source inverter with separate DC sources for static var generation,” *IEEE Trans. Ind. Applicat.*, vol. 32, pp. 1130–1138, Sept. 1996.

[4] Y.-S. Lai and F.-S. Shyu, "Topology for hybrid multilevel inverter," IEE Proceedings-Electric Power Applications, vol. 149, pp. 449-458,2002.

[5] J. Rodriguez, J. S. Lai, and F. Z. Peng, "Multilevel inverters: a survey of topologies, controls, and applications," *Industrial Electronics, IEEE Transactions on*, vol. 49, pp. 724-738, 2002.

[6] Z. Du, L. M. Tolbert, J. N. Chiasson, B. Ozpineci, H. Li, and A. Q. Huang, "Hybrid cascaded H-bridges multilevel motor drive control for electric vehicles," in 37th IEEE Power Electronics Specialists Conference (PESC), 2006, pp. 1-6.

[7] J. Rodriguez, S. Bernet, B. Wu, J. O. Pontt, S. Kouro, "Multilevel voltage-source-converter topologies for industrial medium-voltage drives", *IEEE Trans. Ind. Electron.*, vol. 54, no. 6, pp. 2930-2945, Dec. 2007.

[8] Z. Du, L. M. Tolbert, B. Ozpineci, and J. N. Chiasson, "Fundamental frequency switching strategies of a seven-level hybrid cascaded Hbridge multilevel inverter," IEEE Trans. Power Electron., vol. 24, no.1, pp. 25-33, 2009.

[9] J. Dixon, J. Pereda, C. Castillo, S. Bosch, "Asymmetrical multilevel inverter for traction drives using only one dc supply", *IEEE Trans. Veh. Technol.*, vol. 59, no. 8, pp. 3736-3743, Oct. 2010.

[10] M. Malinowski, K. Gopakumar, J. Rodriguez, and M. A. Perez, "A survey on cascaded multilevel inverters," *Industrial Electronics, IEEE Transactions on*, vol. 57, pp. 2197-2206, 2010.

[11] S. Kouro, M. Malinowski, K. Gopakumar, J. Pou, L. G. Franquelo, B. Wu, J. Rodriguez, M. A. Perez, and J. I. Leon, "Recent advances and industrial applications of multilevel converters," Industrial Electronics, IEEE Transactions on, vol. 57, pp. 2553-2580, 2010.

[12] P. Roshankumar, P. Rajeevan, K. Mathew, K. Gopakumar, J. I. Leon, and L. G. Franquelo, "A Five-Level Inverter Topology with Single- DC Supply by Cascading a Flying Capacitor Inverter and an HBridge," IEEE Trans. Power Electron., vol. 27, no. 8, pp. 3505-3512, 2012.

[13] H. Vahedi, K. Al-Haddad, Y. Ounejjar, and K. Addoweesh, "Crossover Switches Cell (CSC): A New Multilevel Inverter Topology with Maximum Voltage Levels and Minimum DC Sources," in IECON 2013-39th Annual Conference on IEEE Industrial Electronics Society, Austria, 2013, pp. 54-59.

[14] H. Vahedi and K. Al-Haddad, "Half-Bridge Based Multilevel Inverter Generating Higher Voltage and Power," in *Electric Power and Energy Conference (EPEC),* Canada, 2013, pp. 51-56.

[15] M. F. Kangarlu and E. Babaei, "A Generalized Cascaded Multilevel Inverter Using Series Connection of Submultilevel Inverters," IEEE Trans. Power Electron., vol. 28, no. 2, p. 625, 2013.

[16] H. Vahedi, K. Al-Haddad, P.-A. Labbe, and S. Rahmani, "Cascaded Multilevel Inverter with Multicarrier PWM Technique and Voltage Balancing Feature," in ISIE 2014-23rd IEEE International Symposium on Industrial Electronics, Turkey, 2014, pp. 2151-2156.

[17] H. Sepahvand, J. Liao, M. Ferdowsi, and K. A. Corzine, "Capacitor voltage regulation in single-DC-source cascaded H-bridge multilevel converters using phase-shift modulation," IEEE Trans. Ind. Electron., vol. 60, no. 9, pp. 3619-3626, 2013.

[18] B. P. McGrath, D. G. Holmes, "A comparison of multicarrier PWM strategies for cascaded and neutral point clamped multilevel inverters", Proc. IEEE PESC, pp. 674-679, 2000.

[19] B. P. McGrath, D.G. Holmes, "Multicarrier PWM Strategies for Multilevel Inverters”, IEEE Transactions on industrial electronics, vol. 49, no. 4, august 2002.

[20] W. Yao, H. Hu, and Z. Lu, "Comparisons of space-vector modulation and carrier-based modulation of multilevel inverter," Power Electronics, IEEE Transactions on, vol. 23, pp. 45-51, 2008.

[21] M. Sharifzadeh, H. Vahedi, A. Sheikholeslami, P.-A. Labbé, and K. Al-Haddad, "Hybrid SHM-SHE Modulation Technique for Four-Leg NPC Inverter with DC Capacitors Self-Voltage-Balancing," IEEE Trans. Ind. Electron., vol. 62, no. 8, pp. 4890-4899, 2015.

[22] B. N. Singh, B. Singh, and B. P. Singh, “Fuzzy Control of Integrated Current-Controlled Converter–Inverter-Fed Cage Induction Motor Drive”, IEEE transactions on industry applications, vol. 35, no. 2, march/april 1999.

[23] J. C. Das, “Passive Filters—Potentialities and Limitations”, IEEE transactions on industry applications, vol. 40, no. 1, january/february 2004.

[24] K. Mathew, K. Gopakumar, J. Mathew, N. A. Azeez, A. Dey, Student Member, and L. Umanand, “Medium Voltage Drive for Induction Motors Using Multilevel Octadecagon Voltage Space Vectors”, IEEE transactions on power electronics, vol. 28, no. 7, july 2013.

[25] P. Rajeevan, K. SivaKumar, K. Gopakumar, C. Patel, and H. Abu-Rub, “A nine-level inverter topology for medium-voltage induction motor drive with open-end stator winding,” IEEE Trans. Ind. Electron., vol. 60, no. 9, pp. 3627–3636, Sep. 2013.

[26] A. Reznik, M. G. Simões, A. Al-Durra, and S. M. Muyeen, “LCL Filter Design and Performance Analysis for Grid-Interconnected Systems,” IEEE transactions on industry applications, vol. 50, no. 2, march/april 2014.

[27] V. Nair R, S. Pramanick, K. Gopakumar, and L. G. Franquelo, “Novel Symmetric Six-Phase Induction Motor Drive Using Stacked Multilevel Inverters with a Single DC Link and Neutral Point Voltage Balancing”, IEEE transactions on industrial electronics, vol. 64, no. 4, april 2017.