Studies on OPAMP-Less Pipelined Analog to Digital Converter for Deep Submicron Technologies

Thesis

Submitted for the award of

DOCTOR OF PHILOSOPHY

by

Anil Singh

(Regd. No. 901106001)

Under the supervision of

Dr. Alpana Agarwal
Associate Professor
Electronics & Comm. Engineering Department
Thapar University

Electronics & Communication Engineering Department,
Thapar University, Patiala- 147004
September 2016

Dedicated to

my parents

&

my wonderful wife

CERTIFICATE

I hereby certify that the work which is being presented in the thesis entitled, **"Studies on OPAMP-Less Pipelined Analog to Digital Converter for Deep Submicron Technologies"**, for the award of degree of **Doctor of Philosophy** in Electronics and Communication Engineering Department, Thapar University, Patiala, is an authentic record of my own work carried out under the supervision and guidance of Dr. Alpana Agarwal, Associate Professor, ECED, Thapar University, Patiala.

The results presented in this thesis have not been submitted in part or in full to any other University or Institute for the award of any degree or diploma.

(Anil Singh)

This is to certify that the above statement made by the candidate is correct and true to the best of my knowledge and the contents of the thesis has reached the requisite standards.

23/9/16

Dr. Alpana Agarwal
Associate Professor
ECED, Thapar University,
Patiala, India

ACKNOWLEDGMENT

Before I express my heart-felt gratitude towards all my mentors, first and foremost, I would like to thank my greatest teacher and of course of all: **God**. He has given me the power to believe in myself and my passion to pursue this study. I could never have done this without his blessings.

I want to thank my **parents** for their endless love, support and encouragement throughout my life.

I would like to express my gratitude to my thesis advisor, **Dr. Alpana Agarwal** for motivation, patient guidance and every-time support. She always supported me throughout the work by motivating me from time to time. It would have been very difficult for me to come out with results without her invaluable suggestion. I am thankful to her that she has full confidence in my ability; much of this work would have not been completed without support and encouragement.

I would like to thank **Dr. Sanjay Sharma (Head of Department, ECED)** for all the support in the department and **Dr. O. P. Panday (Dean-Research Sponsored and Planning)** for all the support related to research work in the University.

I would also like to gratefully acknowledge the support of some special individuals. First of all, I would like to thank Ms. Manu Bansal (Assistant Prof., ECED) for providing me the books she has in her possession for reading whenever I was in need. Also, I would like to thank Mr. Arun Kumar Chaterjee (Assistant Prof. ECED) and Ms. Madhu Chaterjee (neighboring Phd student) for clarifying my all MOSFET related doubts and making the entire Ph.D. tenure enjoyable. I want to thank Mr. Manohar Bhardwaj (Lab technician in VLSI Lab) for always be available for the support in the lab. Also, I want to thank Mr. Ankur Sangal, CoreEL Technologies, for his constant support for all the tool related problems. He was always just a phone-call away. I also would like to thank SMDP-VLSP Ph. II and SMDP C2SD sponsored by DietY (Govt. of India) for their financial support in this work. Last but not the least; I would like to thank all the persons who helped me directly or indirectly.

At last I do not know how to begin with saying thank you to my soul mate, my dear wife Veena. Leaving the job, as an Engineer in VLSI, to pursue the dream of higher study was a tough decision but my wife stood with me and bore all that pain that a person with less money goes through. Her support, encouragement, quiet patience and unwavering love made it possible for me to accomplish the Ph.D. Without her support this Ph.D. was not possible.

Along with her, I want to acknowledge my little princess, Prisha who always missed her dad while playing. "I wish I could go back in time and make it all for you. I love you more than anything".

ANIL

ABSTRACT

Pipelined ADC is a popular choice for applications requiring high sampling rates of the range of 50-100 MHz and resolution of up to 12 bits typically which can be extended using different calibration techniques. Resolution is mainly limited by various non-idealities existing in a switched capacitor (SC) implementation of Pipelined ADC stage such as offset, capacitor mismatch, finite amplifier gain, amplifier non-linearity etc. These errors cause linear as well as non-linear errors in the ADC output; the effect of such errors can be mitigated using a calibration technique. So, it is important to understand the various errors, their sources and their impact on total ADC output. Therefore, various pipelined ADC errors occurring in a stage and their impact on overall ADC characteristics are modeled and analyzed using MATLAB.

Targeting low power, low area and low cost, an opamp-less fully differential MOSFET-only pipelined ADC stage is presented in TSMC 0.18µm digital CMOS technology with power supply of 1.8 V. It is based on 1.5-bit/stage architecture and uses the charge pump technique to achieve the inter stage gain of 2. Furthermore, stage is independent of capacitor mismatch and avoids the use of power hungry opamps thus reduces the power consumption and Silicon area. In the present research work, MOSCAPs are used in place of MIMCAPs to reduce the manufacturing cost and Silicon area further.

Proposed MOSFET-only stage suffers from only gain error. A 10-bit 100 MS/s pipelined ADC is designed using the proposed stage and digital background calibration is performed to compensate the missing codes resulted from the gain error. Before calibration SNDR and SFDR of the pipelined ADC is 39.61 dB and 40.39 dB respectively which increase to 66.78 dB and 79.3 dB after calibration. Also DNL improves to +0.6/-0.4 LSB and INL improves from +9.3/-9.6 LSB to within ± 0.5 LSB. Total power consumption of the ADC is 16.53 mW.

A design methodology is proposed to design the MOSFET-only charge pump based pipelined ADC. Following this, a MOSFET-only charge-pump based pipelined ADC can be designed with lesser iterations and design efforts, and reduces the time to market. Designing of various building blocks of the proposed stage along with the tradeoffs are discussed.

CONTENTS

LIST OF FIGURES

LIST OF TABLES

ACRONYMS

ADC	Analogue to Digital Converter
bps	bit per stage
CM	Common Mode
CMFB	Common Mode Feed Back
CMRR	Common Mode Rejection Ratio
DAC	Digital to Analogue Converter
DNL	Differential Non Linearity
ENOB	Effective Number of Bits
GBW	Gain Bandwidth
INL	Integral Non Linearity
LSB	Least Significant Bit
MDAC	Multiplying DAC
MSB	Most Significant Bit
opamp	Operational Amplifier
PM	Phase-Margin
rms	root mean square
SFDR	Spurious-Free Dynamic Range
SNDR	Signal-to-Noise and Distortion Ratio
SNR	Signal-to-Noise Ratio
THD	Total Harmonic Distortion

Chapter 1
Introduction to ADC

1.1 Background

Most of real world signals are analog in nature, they are continuous-time, continuous-valued signals. Compared to analog signal, digital signal has the following advantages:

a) It is immune to electrical noise.

b) It can be manipulated easily (DSP processing).

c) It is easy to store.

d) It is easy to copy and transfer.

Thus, there is a trend to move signal processing from the analog domain to the digital one such as digital signal processing, which, besides above advantages allow for a higher level of accuracy, provides power savings with lesser silicon area, increases the robustness, speeds up the design process, provides programmability, and increases the design reuse possibilities.

Because of the above benefits, there is a need to convert the analog real world signals into digital discrete-time, discrete-value signals. Analog to digital converters (ADC) is one such block that converts the analog signal to digital domain for DSP processors to process and digital to analog converters (DAC) does the reverse. Figure 1.1 shows the analog to digital converter with N number of bits.

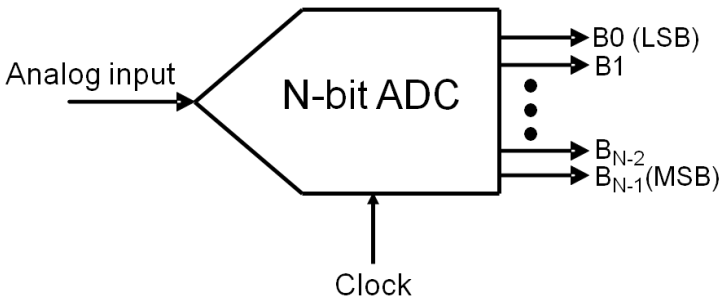


Figure 1.1. Analog to digital converter

Analog to digital conversion is the process where analog signals are mapped onto digital code representations. Although the analog input signal can be represented in several

domains (for example voltage, current, charge), input is assumed to be in the voltage domain in the present work. Also, it is assumed that the digital codes are described in the binary domain. The analog input signal $V_{in}(t)$ is defined for each moment in time and can take any value within a certain range:

$$V_{min} \leq V_{in}(t) \leq V_{max} \tag{1.1}$$

where $V_{\min}$ and $V_{\max}$ are the minimum and maximum amplitude of the input signal.

To represent this signal in a limited amount of digital data, the input signal is sampled on fixed time intervals and quantized in the amplitude domain. The sample frequency f_s of the converter determines the time interval T_S between two consecutive sample moments, according to

$$f_s = \frac{1}{T_s} \tag{1.2}$$

Suppose that the digital output code at each sample moment consists of N bits, and the codes are equally distributed over the allowed input range. Then, the distance between each pair of successive codes is given by

$$V_{LSB} = \frac{V_{\max} - V_{\min}}{2^N} = \frac{V_{FS}}{2^N} \tag{1.3}$$

1.2 ADC Specifications

Using or designing an ADC involves a proper understanding of their specifications. These give the user information about the features and limits. The specifications can be divided into following categories:

a) General features

b) Static specifications

c) Dynamic specifications

Each category will be discussed in the following sections.

1.2.1 General Features

The most important general features of an ADC converter are the following:

Type of Analog Signal

The analog input signal of an ADC can be single ended, pseudo-differential or differential. Single ended signals are referred to an analog ground; pseudo-differential signals are symmetric with respect to a generic fixed voltage; differential signals are the difference between the inputs regardless of the common-mode voltage. The differential mode is the most used because it features, for the same input signal swing, twice the input range, higher common-mode rejection and a higher signal-to-noise ratio (SNR).

Resolution

The resolution (N) is the number of bits that an ADC uses to represent its input. A high resolution ADC divides the input range into a larger number of sub-ranges than a low resolution converter. Thus, for a fixed full scale input range (V_{FS}) a high resolution ADC can resolve smaller signals than a low resolution ADC is able to resolve. Resolution is usually degraded by either noise or nonlinearity. Therefore, for high resolution applications noise and nonlinearity should be as low as possible. Two types of nonlinearity are used to characterize the nonlinearity in ADC: Differential nonlinearity (DNL) and Integral nonlinearity (INL). These two are discussed in the next section 1.2.2.

Dynamic Range

The dynamic range is the ratio between the maximum input voltage and the noise. The dynamic range determines the maximum SNR achievable.

1.2.2 Static Specifications

In the 1950s and 1960s, static performance specifications such as INL, DNL, gain error, offset error, monotonicity, no missing codes, *etc*., were used to characterize the data converters. These specifications were enough during this era, because most of the applications (except Pulse Code Modulation(PCM) and radar, for example) dealt with dc or low frequency signals. These specifications are therefore called Static specifications and are discussed below.

Analog Resolution

The analog resolution is the smallest analog input variation which produces a variation of 1 LSB in the output code and it is given by $\frac{V_{ref}}{2^N}$ where V_{ref} is the input range and N is the resolution.

Analog Input Range

The analog input range is the peak-to-peak input signal (voltage or current) which generates, as output, a full-scale response.

Offset

The offset is the difference between the ideal and the real input signal values to get a null output signal (it can be expressed as Volt, Amperes, LSB). The offset shifts all the quantization steps by the same quantity.

Gain Error

The gain error is the error on the slope of the straight line interpolating the transfer curve, which differs from a straight line of slope 1 (ideal data converter).

Power Consumption

The power consumption is the power consumed by the ADC during normal operations.

Temperature Range

The temperature range is the range of temperatures in which the ADC can operate, while maintaining a proper functionality.

Differential Non-linearity (DNL) Error

Differential Non-linearity (DNL) of the ADC is defined as the difference in least-significant-bit (LSB) of the code widths of two neighboring codes when measured at each vertical step. The output of an ideal data converter changes from one code to the next code for equal change in input voltage. DNL can have the positive or negative LSB. It also tells about the nonmonotonicity. For a DNL value of more than 1 LSB, nonmonotonicity occurs. DNL is also a good measure of about the missing codes in the ADC output and produces higher quantization noise in FFT response of ADC output for large value of DNL. It is shown in Figure 1.2 [1].

Integral Non-linearity (INL) Error

Integral Non-linearity **(**INL) on the other hand is defined as the maximum difference between the ideal ADC characteristic and real ADC characteristic. Like DNL it is also measured in LSB. If DNL is already measured INL can be measured by the summation of all the DNL error. INL can also be measured by other ways such as best-straight line, absolute straight

line or end point line (a line connecting the two end points of the ADC characteristic) [2].

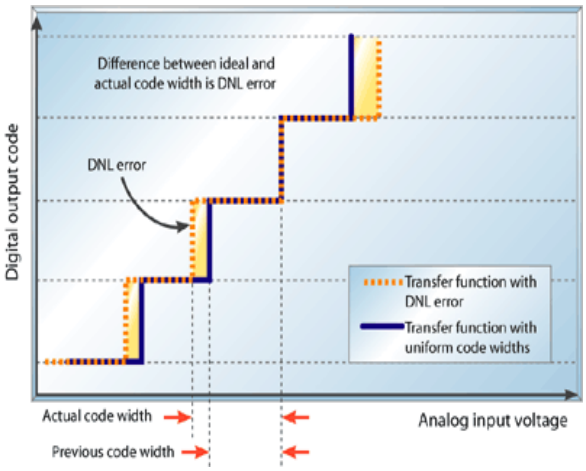


Figure 1.2: DNL Error [1]

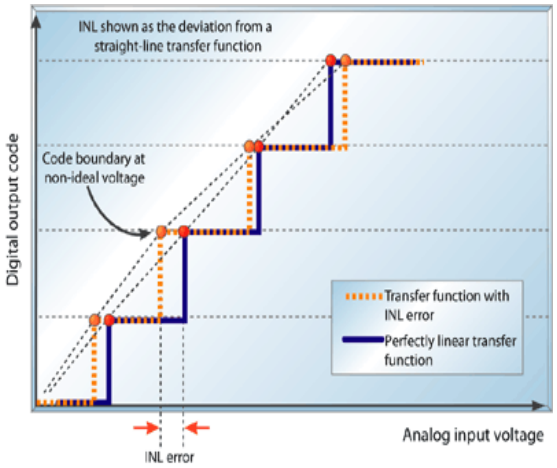


Figure 1.3. INL Error [1]

Like DNL INL can also be positive or negative LSB and is shown in Figure 1.3.

1.2.3 Dynamic Specifications

With the advancements of general purpose microprocessors and digital signal processing (DSP) in the 1970s and 1980s, dynamic performance specifications, such as signal-to-noise ratio (SNR), spurious free dynamic range (SFDR) *etc.*, were required in order to adequately characterize converters for more sophisticated signal processing applications. These specifications are called dynamic specifications and some of them are discussed below. Both static and dynamic specifications are important to characterize the ADC. For instance, significant gain and/or offset errors in ADC can cause signal clipping and thereby degrade SNR and SFDR.

Analog Input Bandwidth

The analog input bandwidth is the frequency at which the output code is −3dB with respect to its low-frequency value.

Signal to Noise Ratio (SNR)

After conversion, digital data is quantized that assume only certain values within a range. The difference between the analog value and quantized output value is termed as quantization error (QE). It is shown in Figure 1.4.

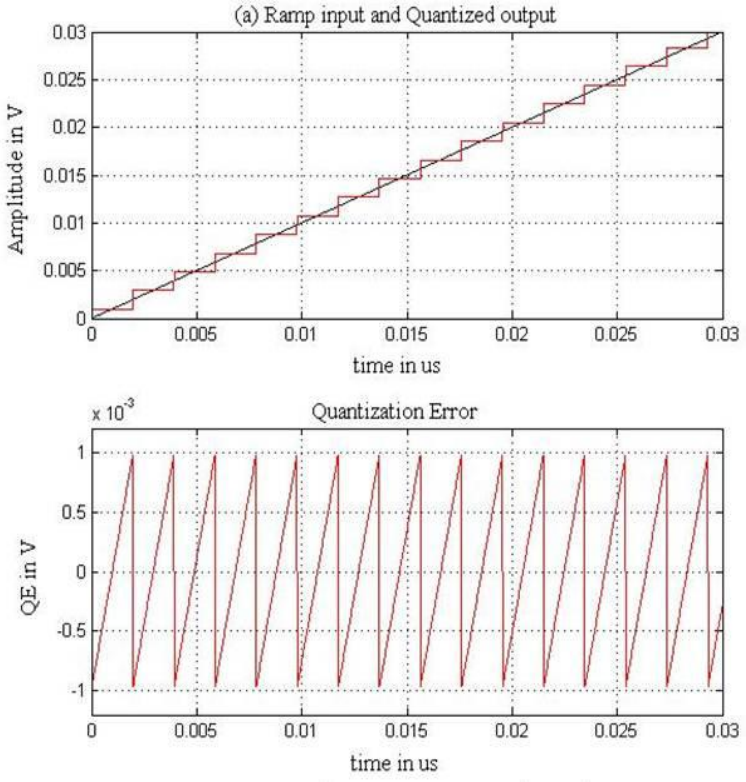


Figure 1.4. Ideal ADC characteristic and quantization error

An ideal ADC with resolution of N-bit has inherited quantization noise due to quantization process of ADC. Its root–mean-square (RMS) value is given by [2]

$$V_{qe\,(RMS)} = \frac{V_{LSB}}{\sqrt{12}} \tag{1.4}$$

where V_{LSB} is given by $V_{FS}/2^N$ with V_{FS} is the full scale input voltage.

The SNR is the ratio between the power of the signal (normally sinusoidal) and the power of quantization noise and circuit noise. It is given in dB by [2]

$$\text{SNR} = 6.02N + 1.76 \tag{1.5}$$

Signal to Noise and Distortion Ratio (SNDR)

The signal to noise plus distortion ratio (SNDR) is often used to measure the performance of an ADC. It measures the degradation due to the combined effect of noise, quantization errors, and harmonic distortion. The SNDR of a system is usually measured for a sinusoidal input and is a function of the frequency and amplitude of the input signal. When a sinusoidal signal of a single frequency is applied to a system, the output of the system generally contains a signal component at the input frequency. Due to distortion, the output also contains signal components at harmonics of the input frequency. Furthermore, the ADC adds noise to the output, and this is noise generally present to some degree at all frequencies. SNDR is given by [2]

$$SNDR_{dB} = 20\log\left(\frac{A_{signal}}{A_{noise}}\right) \tag{1.6}$$

where A_{signal} depicts the output signal level and A_{noise} describes the noise level.

Spurious Free Dynamic Range (SFDR)

The spurious free dynamic range is the ratio of the full scale signal to the highest spur in the ADC output spectrum. This measure is useful because it indicates the amount of dynamic range that can be obtained before distortion becomes dominant over noise.

Effective Number of Bits (ENOB)

For a ADC with only noise, N in equation (1.4) gives the resolution of ADC. However, when distortion is added with noise SNDR is used to check the quality of the ADC and ENOB shows the effective resolution when SNDR comes in the picture. It is given by

$$ENOB = \frac{SNDR - 1.76}{6.02} \tag{1.7}$$

1.3 Types of ADCs

High speed analog-to-digital converter (ADC) plays an important role in many digital signal-processing systems. Recently, the demands of consumer products such as video systems, portable personal communication device, and LCD drivers are growing rapidly. In these applications, high speed and medium to high resolution analog-to-digital converters are

required.

In addition, the personal computing, communication, and various portable equipments, such as mobile phones and tablets, have become more popular. In order to increase the battery lifetime and reduce heat dissipation, the power reduction of integrated circuits has also become a major issue in these battery-based applications, especially in the portable devices. Furthermore, the growing market of portable applications and the process technology scaling are driving the supply voltage of digital integrated circuit down to 1V and even lower. With the evolution of process, the power consumption of digital integrated circuit decreases as the supply voltage scales down. But the reduction of supply voltage makes analog integrated circuits design more challenging as it becomes more prone to noise and increase in leakage current.

For the low speed, successive approximation register (SAR) ADCs are the best candidates. For high-resolution applications such as FM radio, stereo compact disc (CD), digital-audio-tape (DAT), and DVD recordings, sigma-delta ADCs are popular, as a resolution from 12 to 24-bit could be achieved.

For those applications that require both high speed and a moderately high resolution (>8 bits), pipelined ADCs are the best-suited candidates in a wide range of commercial applications such as high-speed data conversion in communication systems, image signal processing and ultrasound front ends. In such applications, high-speed operations along with

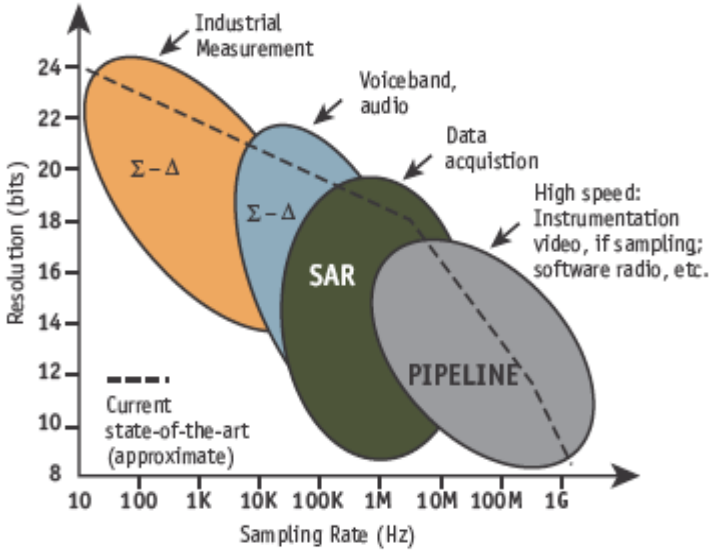


Figure 1.5. ADC architectures, applications, resolution, and sampling rates [3].

the reduction of power consumption are the key design challenges in enhancing functionality and battery life. This trend is shown below in Figure 1.5 [3].

Table 1.1 shows the comparison among various ADCs with advantages and disadvantages.

Table 1.1 Comparisons among various ADCs

ADC Architecture	**Advantages**	**Disadvantages**
Flash ADC	• Fastest among all the ADCs • No latency	• Large number of comparators • Large input capacitance • Required high-speed comparators • Resolution ≤ 6-bits
SAR ADC	• Medium resolution • Easy implementation	• Complex DAC is required • Speed upto few MS/s
Sigma-Delta ADC	High resolution	• Complex design • Slow speed
Dual Slope	• No component matching requirements • Resolution is high • Easy to design	Speed is less
Pipelined ADC	• Very high speed • Low accuracy comparators required • Low input capacitance • Area-Power optimization Possible	Large latency

Among many types of complementary metal-oxide-semiconductor (CMOS) based ADC architectures, the pipelined ADC has an best suited for achieving high resolution at high sampling rate with low design complexity and power consumption. Design of pipelined

ADC is pushed towards higher speed, higher accuracy and lower power dissipation by the rapid growth of process. These features make pipelined ADC more suitable for many applications as compared to other ADCs. Table 1.2 shows the typical applications of the pipelined ADC.

Table 1.2: Typical applications of the pipelined ADC

Resolution (number of bits)	Application
8	• Flat-panel displays • HDTV • Medical imaging (low end product) • WLAN and WAN
10	• Flat-panel displays • HDTV • Medical imaging such as ultrasound • Cellular base stations • modems
12	• Cellular base stations • Professional HDTV cameras • Medical imaging • Test equipment
14	• High end instruments • Military and aerospace • Cellular base stations (for 3G)

1.4 Organization of the Thesis

In Chapter 1, introduction to ADC, its various parameters are briefly discussed. Also different types of ADCs are discussed in this chapter.

In Chapter 2, literature review related to the pipelined ADC and their different architectures are presented.

In Chapter 3, study of various existing pipelined ADC architectures and analysis of their performance parameters is discussed. Also this chapter focuses on various errors in pipelined

ADCs, their mathematical modeling and simulation. MATLAB, an industry standard mathematical tool, is used in the present work to model the various Pipelined ADC errors in 1-bit/stage and 1.5-bit/stage architectures and their impact on overall ADC characteristics

In Chapter 4, proposed MOSFET-only operational amplifier (opamp)-less 1.5-bit pipelined ADC stage is presented. Design considerations and optimization of various blocks along with noise analysis of the proposed ADC stage is discussed.

Chapter 5 presents the digital background calibration of the complete pipelined ADC using the proposed MOSFET-only opamp-less 1.5-bit stage along with simulation results.

In Chapter 6, the design methodology for the design-synthesis of proposed pipelined ADC for given specifications is discussed. It proposes a design methodology for the proposed opamp-less pipelined ADC such that it requires minimum iterations in design cycle to achieve the desired ADC specifications. Also it discusses the tradeoffs between area and power for various ADC parameters such as INL/DNL, SNR and SFDR.

Conclusion and Future Scope is discussed in Chapter 7 at the end.

Chapter 2

Literature Review

2.1 Introduction

In recent years, portable electronic devices, such as wearable battery operated devices, High definition televisions (HDTV), mobile phones or tablets are finding a booming market. There is huge demand for applications having more functionality at reduced cost with longer battery life. In order to meet these requirements, there is a need to design the low-voltage low-power building blocks. Analog-to-digital converter (ADC) is an important building block that converters analog signal to digital signal which is further used for post processing, storage as explained in section 1.1. In order to reduce the cost and power, more and more functionality is getting crammed into a smaller area. Therefore, integrating both digital and analog parts together in a single chip called system-on-chip (SoC) is highly desirable.

With the scaling down of the technology in digital domain, transistor size is getting reduced along with the supply voltage which is necessary to avoid the breakdown of the devices. As a consequence of this it is becoming possible to digital circuits with more functionality at lesser area with high speed and low power. These are the main reasons that make the design of low voltage circuits in deep submicron technology a hot topic.

While moving into nanometer complementary metal-oxide-semiconductor (CMOS) technologies, for low-power high speed applications, certain advantages and disadvantages are foreseen. First due to increase in the vertical electric filed in the device, supply voltage is reduced to avoid the transistor breakdown. The threshold voltage of the transistor is also somewhat low which reduces the overdrive voltage, an advantage in low-voltage applications. Further, as the device size shrinks parasitic capacitances at the various nodes decreases which in turn increases the speed of intrinsic device. In analog circuits it increases the bandwidth of amplifier.

However, the decreased voltage supply and technology scaling gives many challenges to analog circuit designers. Although, in the deep sub-micron technologies speed of the devices increases but their characteristics degrades due to various short channel effects and low voltage swing. There is a decrease in the intrinsic gain of the device with scaling that

limits its use in high resolution application. These challenges force the designers to think for innovative circuit design techniques such as to increase the gain in amplifiers, gain boosting and cascoding is used but at the cost of increase in the power dissipation and increase complexity. The low supply voltage is required to avoid the device breakdown but reduces the voltage swing that limits the signal-to-noise ratio (SNR). In order to increase the swing, it requires devices with low threshold voltage but that increases the leakage current and requires extra fabrication masks and is costly.

Also with the reduction of supply voltage and threshold voltage of devices, driving capability of MOS switches decrease and for that purpose clock bootstrapping switching are generally employed. But there remains a reliability concern of the devices because of increase in the gate voltage. For the ADCs consisting of both analog part and digital part together, the technology scaling is giving maximum benefits to the digital part. Digital circuits are more immune to process, voltage and temperature variations as compared to analog parts. Due to these benefits, in a SoC, there is a trend to keep the analog part as small as possible and shift the most of analog functionality to digital domain. However, analog part in a chip is required in interfacing to external world so cannot be completely removed. These challenges keep motivating the researches to look for solutions for analog part of the converter that consumes less power and has low design complexity.

2.2 Design Challenges of ADCs in Deep Submicron Technologies

First most important challenge that a designer in deep submicron (DSM) technology faces is that reduced gain of the amplifier as a result of decrease in its output impedance. One presented solution to achieve the high gain is cascoding of the transistors. As the number of stacked transistors increases, output impedance of the amplifier increase along with reduction in various short channel effects. However, sum of all the overdrive voltages of each device necessary to keep all the transnsistors in saturation increase which in turn reduces voltage swing of the amplifier and therefore there is a limit on the number of transistors that can be cascoded [4].

In the precision analog circuits, performance of a device can be measured by product of transconductance and output impedence which is defined as the intrinsic voltage gain of the MOS transistor. As the down scaling of the devices continues, transconductance decrease due

to vertical field mobility effect and output impedence decreases due to reduction in drain-induced barrier lowering (DIBL) and hot carrier impact ionization [5]. The maximum intrinsic gain for n-channel MOS transistor in 90 nm is approximately 10 whereas for 0.35 µm technology it is approximately three times more than the former. Furthermore, oxide thickness of the MOS transistor decreases in order to decrease the threshold voltage. This increases the vertical filed and gate leakage current and further causing the effective output impedance to decrease [6-7.

Scaling down of the oxide thickness beneath the gate improves the matching properties of the MOS transistor. However, the mismatch can be larger in the devices with short width or length because of higher order terms [8-10], therefore to improve the matching larger devices are used. With the scaling, as the oxide thickness is decreased further to few atomic layers, extra effects related to quantum starts dominating and hence reduces the matching further.

Another important challenge in precision analog circuit design in deep sub micron technology is the reduced supply voltages. Supply voltage is reduced in order to reduce the vertical fields and improve the reliability of the MOS transistors. But it reduces the output voltage swing of the circuit and signal move closer to the noise therefore decreases the dynamic range (DR) and signal-to-noise ratio (SNR). To increase the DR and SNR, circuit noise must be reduced with the increase in voltage swing. In switched capacitors (SC) such as ADC there are many sources of noise such as noise contributed by the amplifiers, quantization noise and noise due to sampling (kT/C). Sampling noise mainly dominates and can be reduced by increasing the capacitor sizes. However it results in increase in the area and decrease in the speed and requires more power to be invested in order to increase the speed.

Opamp, Comparators and Sample and Hold amplifiers (S/H) are the common building blocks of many ADCs. These blocks mainly decide the accuracy and speed of the overall ADC. In a pipelined ADC, opamp being the main processing block limits the performance. Resolution and settling speed of the pipelined ADC is primarily determined by the gain and bandwidth of opamp. Also it limits the dynamic range, linearity and power consumption. Scaling down of the technology reduces the size of the device and the various parasitic capacitances associated with it that increases the speed of the devices. Therefore amplifier

with wider bandwidth can be designed in lower micron technologies. Also by this higher sampling rate can be achieved. However as explained earlier in this section intrinsic gain of the device decreases that decrease the settling accuracy and limits the resolution that can be achieved. Also analog circuits are more affected by the short channel affects as compared to digital circuits and sensitivity to process, voltage and temperature variations.

Next important drawback is introduced by the MOS switches used the SC circuits in deep submicron technology. ON-resistance of the MOS switches varies with the variation in input voltage that introduces the non-linearity and distortion at the output SC circuits. Scaling reduces the supply voltage at a faster pace than the threshold voltage which reduces the overdrive voltage of MOS transistor and increase the ON-resistance. As a result, bandwidths of the switches start impacting the performance of overall SC circuit. One of the solutions to this problem is to make the ON-resistance independent of the variation in gate voltage by using bootstrapping technique [11-12]. However there remains a reliability concern of the MOS devices due to increase in the gate voltage. Next important concerns related to switches are the charge injection and charge feed through effects which reduces the accuracy of SC circuits.

In order to increase the gain of amplifier in deep submicron technology gain-boosted technique is generally employed. It increases the output impedance of the amplifier by many folds without much affecting the transconductance [13-17]. However, gain-boosting technique requires cascading of MOS transistors therefore reduces the voltage swing, increases the design complexity, area and power. Gain can also be increased by increasing the number of stages in an amplifier (Multistage amplifier) but it requires compensation technique for stability when used in the feedback configuration and consumes more power and has low speed when compared to single stage amplifier, and therefore are less popular.

Another source of error in deep submicron technology is the offset in the comparator and opamp used in the SC circuit. It limits the accuracy of SC circuits. Major source of offset is the mismatch in width or length of the MOS transistors and due to process variation. The offset can be reduced by choosing the width and length more than the minimum offered by the technology, using the differential structure and following the proper layout techniques such as common-centroid technique.

2.3 Advancements in Pipelined ADC in Deep Submicron Technologies

In the recent past there is a huge requirement of battery powered high performance all in – one electronic gadgates. For example present day mobile phones or tablets has many applications within it which replaced many single electronic devices like radios, mobiles, video games and many more. These all required high performance high resolution ADCs to convert the analog signal into digital form for further processing. Resolution of ADCs required in such applications vary in the range of 10-bits or higher and speed above 100 MHz along with low power consumption. Among all the available ADCs, pipelined ADC is the most suitable for such applications but there remains many design challenges to achieve the high performance in pipelined ADC, especially in deep submicron technology.

Opamp is the main processing block used in the pipelined ADC. The conversion rate of entire ADC is limited by the speed of opamp. Due to scaling benefits, operating speed of opamp increases which in turn increases the bandwidth and sampling speed of complete pipelined ADC. However, technology scaling reduces the maximum open loop gain of opamp that limits the resolution of ADC. Reduction in supply voltage reduces the signal swing of opamp and reduces the SNR of complete ADC. Thus technology scaling does not help the designer any more when working in analog domain. Cascoding or gain boosting techniques are employed to increase the gain but it increase the design complexity and makes opamp an power inefficient block. Due to these issues, opamp-less, comparator-based or opamp in open-loop configuration are getting popularity in deep submicron technologies while designing the pipelined ADC.

One such power efficient example in pipelined ADC is the use of opamp in open-loop configuration instead of closed loop to generate the residue voltage [18]. It does not require the high gain opamp thus save power and used digital calibration technique to remove the gain error and non-linearity introduced by the open loop amplification. Another technique that has been also proposed is the incomplete settling which relaxes the tradeoff among the high gain, high swing, and phase margin in low micron technologies [19].

Some of the new architectures also employ comparators [20], current mode processing [21] or zero-crossing detectors [22] instead of opamps. Their use is demonstrated in various pipelined ADCs with different resolution and sampling rate. Because of the comparator,

virtual short properties is not required to maintain, require comparators or zero crossing detectors with small gain and are more suitable to future generations CMOS technologies. Therefore in the deep submicron technologies with reduced channel lengths, it is expected that the Comparator Based Switched Capacitor circuits (CBSC) and zero-crossing based circuits are more power efficient than the traditional opamp based designs. CBSC and zero crossing detectors can be applied to wide range of SC circuits including SC filters and sigma-delta ADCs without changing their basic topology. The full scale swing of upto supply voltage can be obtained by using the dynamic cross-coupled latches after the comparators. However, power efficiency of CBSC and zero based circuits must be improved for their use in low power applications [23].

Some new applications such as wearable medical devices, automatic testing equipments (ATE) and wireless sensor networks (WSN) requires ultra low power ADCs [24]. They require active blocks that consume least power with maximum energy efficiency and forced the researchers to look for opamp-less alternatives since opamp consumes most of the ADC power [25-30].

Another ADC design technique that is getting popularity in current deep submicron technologies is the time-based ADCs [31-32]. In time-based ADCs, the information is converted to a time domain pulse width by the circuit and a time-to-digital converter is used to get the digital output. Operating speed of pipelined ADC is normally limited within the range of 100- 500 MS/s which can be increased by using the time interleaving concept upto the range of gigahertz (GHz) [33].

Gain error is one of the important errors in pipelined ADCs. The most common source of it is the capacitor mismatch in multiplying-digital-to-analog converter (MDAC) stage. In pipelined ADC, with equal values of capacitors, desired gain of 2 is achieved. But due to process variations capacitors values may differ so a gain other than 2 may occur that causes the gain error. Capacitor mismatch is generally mitigated through the use of best practice design and layout strategies. Another source of gain error, not usually a concern for pipeline ADCs, is reference mismatch from stage to stage. The voltage reference is a very-low impedance signal that is sent to each stage of the pipeline ADC [34]. Instead of implementing capacitors in MIM (Metal-Insulator-Metal), Aminzadeh [35] has discussed the design considerations of a 12-bit, 65MS/s pipelined ADC using compensated depletion-mode MOS

capacitors. In this, digital calibration is used to compensate for the distortion caused by employing nonlinear capacitors offered by the MOSFETs (known as MOSCAP) instead of linear MIMCAPs. Also merged-capacitor switching (MCS) technique improves the signal processing speed and the resolution of the ADC by reducing the required number of unit capacitors by half in comparison to a conventional ADC [36]. In order to reduce the power and to compensate both linear and non-linear errors from MDAC, interpolation based digital self-calibration technique is developed to have low power MDAC with small capacitors and low gain opamp [37]. New techniques have been used in implementing pipelined ADC with emphasis on increasing resolution and sampling rate with reduction in area and power [38-49]. Table 2.1 shows the year wise advancements in the pipelined ADC along with the various ADC parameters.

Year	Ref No.	Author (s)	Techn-ology (µm)	Supply (V)	Res. (bits)	Samp. Rate (MS/s)	DNL (LSB)	INL (LSB)	i/p range (Diff.)	SNR (dB)	SNDR (dB)	SFDR (dB)	ENOB (bits)	Power (mW)	Area (mm^2)	FOM pJ/conv
1995	12	Cho & *et al.*	1.2	3.3	10	20	0.5	0.6	±1 V	–	59.1	–	–	35	3.2 x 3.3	–
1999	11	Abo & *et al.*	0.6	1.5	10	14.3	0.5	0.7	± 0.8V	–	58.5	–	–	36	2.3 x 2.5	–
2003	18*	Murmann & *et al.*	0.35	3	12	75	0.5	0.9	2 V	67	–	76	–	290	7.9	–
2004	36	Yoo & *et al.*	0.25	2.5	10	120	± 0.4	± 0.48	2 V	–	54.1	68.4	–	–	1.8 x 2.0	–
2006	20*	Fiorenza & *et al.*	0.18	1.8	10	7.9	± 0.3	1.59	1V (se)**	53	52	62	8.6	2.5	2.9 x 0.4	0.8
2006	38	Bonger & *et al.*	0.13	1.5	14	100	±1.1	± 2	1.5 V	–	66.5	–	–	224	1.02	1.12
2007	19*	Iroaga & *et al.*	0.35	3	12	75	0.64	0.95	2 V	65.1	63.5	71.2	–	273	7.9	–
2007	22*	Brooks & *et al.*	0.09	1.2	8	200	± 0.75	± 1	1V (se)**	62	–	–	6.5	8.5	0.05	0.51
2007	35	Aminzadeh & *et al.*	0.18	1.8	12	65	–	–	–	–	70	78	11.33	–	–	–
2008	39	Choi & *et al.*	0.13	0.8	10	60	0.35	0.49	0.8	–	56	69.6	–	19.2	0.98	–

* opamp less Pipelined ADC architecture; ** se – single ended

Year	Ref No.	Author (s)	Techn-ology (µm)	Supply (V)	Res. (bits)	Samp. Rate (MS/s)	DNL (LSB)	INL (LSB)	i/p range (Diff.)	SNR (dB)	SNDR (dB)	SFDR (dB)	ENOB (bits)	Power (mW)	Area (mm^2)	FOM pJ/step
2008	40	Jiang & *et al.*	0.18	1.8	8	200	0.3	0.34	0.8 V	–	45.2	60.4	–	22	0.8 x 0.4	0.74
2009	41	Lee & *et al.*	0.18	1.8	10	50	± 0.39	± 0.81	1.6 V	56.2	56.2	72.7	9.03	12	0.86	–
2009	42	Sahoo & *et.al.*	0.09	1.2	12	200	0.78	1.7	1.2 V	–	62	–	–	348	0.8 x 1.7	1.22
2009	43	A. Verma & *et al.*	0.09	1.2	10	500	0.4	1	1.2 V	–	53	–	–	55	0.5	0.31
2009	44	Abdinia & *et al.*	0.09	1	10	200	–	–	1 V	–	58.5	–	–	30.9	–	0.22
2009	28*	Brooks & *et al.*	0.09	1.2	12	50	± 0.5	± 3	–	–	62	68	10	4.5	0.3	0.088
2009	29*	Hu & *et al.*	0.09	1.2	9.4	50	± 0.37	+ 1.29 /-0.88	1.1 V	49.7	47.7	–	–	1.44	0.12	0.119
2010	45	Pei & *et al.*	0.18	1.8	9	125	–	–	1 V	–	60.23	73.1	–	6.8	–	–
2010	30*	Ahmed & *et al.*	0.18	1.8	10	50	± 0.35	+0.7/ -0.8	1 V	–	58.2	66	9.4	9.9	1.4	0.3
2011	37	Yuan & *et al.*	0.35	3.3	12	20	0.27	0.2	2 V	–	72.5	84.4	11.8	69.5	4.8 x 4.3	0.96

* opamp less Pipelined ADC architecture

Table 2.1: Year wise literature review in Pipelined ADC

2.4 Gaps in Present Study

Alternative architectures that avoid opamps are highly desirable in implementing the piplined ADCs as opamps contribute to the most of the power consumed by an ADC. But it requires the calibration techniques in order to calibrate the output of ADC. Since calibration techniques increase the hardware so it can be exploited to study the noval calibration techniques without much area overhead.

In addition to it, implementing the opamp-less pipelined ADC will give less area, low power and at the same time gives high resolution. Thus a new architectures for implementing pipelined ADC needs to be studied and analyzed targeting low power and low area.

In today's chip market cost is a main driving factor, designers are constantly under the challenge in implementing larger functionally into the scaled smaller area. Therefore, unlike the traditional approaches of implementing analog and other mixed signal blocks in unlimited area is no longer valid. Therefore, along with power, area tradeoff is an important factor in implementing the blocks of mixed signal circuits.

From the Table 1, it is clear that the DNL and INL of the opamp-less architectures are quite high (well above the desired ± 0.5 LSB) so the techniques to reduce these errors need to be analyzed without compromising other performance parameters.

2.5 Objective of the proposed work

Based on the study, literature survey (as reported) and the understanding established the following objectives are proposed:

1. To study of the existing Pipelined ADC architectures and analysis of their performance parameters.
2. To propose an efficient OPAMP-Less Pipelined ADC architecture.
3. To analyze the tradeoffs between the different sets of performance parameters of the proposed ADC for area, power and noise.
4. To propose the design methodology for the synthesis of the proposed Pipelined ADC for given specifications.

Chapter 3

Pipelined ADC Architectures

3.1 Introduction

Pipelined ADC is a popular choice for high resolution and high speed applications such as video rate and high speed imaging. In CMOS technology, a pipelined ADC stage is implemented by switched capacitor (SC) concept which practically has various non-idealities such as offset, capacitor mismatch, finite amplifier gain, amplifier non-linearity *etc*. that limit the high resolution whereas speed is limited by the speed of internal blocks. These errors cause linear as well as non-linear errors in the ADC output; the effect of such errors can be mitigated using various calibration techniques [50]. So it is very important to understand the various errors, their sources and their impact on total ADC output to find an efficient calibration technique that reduces the design efforts and computational power. This chapter focuses on various such errors, their mathematical modeling and simulation. MATLAB, an industry standard mathematical tool, is used here to model the various pipelined ADC errors in 1-bit/stage and 1.5-bit/stage architectures and their impact on overall ADC characteristics as discussed in the following sections.

3.2 Pipelined ADC Architectures

A pipelined ADC is implemented by using multi-bit stage. But among the various options that exist, 1-bit/stage offers simplest implementation while 1.5-bit/stage is widely used in practical ADCs due to its various advantages over the former [51-52]. Figure 3.1(a) shows a general block diagram of a pipelined ADC stage except the last stage which is a flash type converter. Each stage consists of a Sample-Hold circuit (SH), a Sub-ADC and a Multiplying-DAC (called MDAC) which consists of a Sub-DAC, a subtractor and an amplifier with a gain of 2^n in order to keep the dynamic range of a stage equal to full scale range of applied signal. In 1-bit/stage architecture, n = 1 so stage gain is 2 however, in 1.5 bit/stage architecture, gain of stage is maintained to 2 in order to avoid clipping of residue. Typically a switched capacitor implementation of 1.5-bit converter consists of various switches, capacitors, an opamp and

two comparators comparing the analog input V_{in} to the comparator thresholds, which are –Vref/4 and +Vref/4. A Multiplexer works as a sub-DAC.

The clocks shown in Figure 3.1(b) are non-overlapping in nature and used for sampling (Φ_1=1) and amplification phase (Φ_2=1) respectively. Various switches shown in Figure 3.1 work on these non-overlapping clocks and are implemented by MOS transistors. Figure 3.1(c) and Figure 3.1(d) shows the single ended version of a stage for simplicity but practically whole pipelined ADC is implemented in fully differential form to suppress the common-mode noise, substrate noise etc. In SC implemented pipelined ADC stage, main sources of errors are comparator offset, amplifier offset, sub-DAC errors which are considered as linear errors whereas non-linearity errors are mainly due to amplifier gain non-linearity.

Ideally the transfer function of a pipelined ADC stage is given by

$$V_{res} = 2V_{in} - V_{dac} \tag{3.1}$$

where V_{dac} is the output of sub-DAC which is equal to $-V_{ref}/+V_{ref}$ for 1-bit and $-V_{ref}/0/+V_{ref}$ for 1.5-bit architectures with V_{ref} as the reference voltage of ADC.

Its SC implementation is based on the charge transfer technique and the output voltage called residue, and for an ideal opamp is given by (Chuang and Scualley, 2002) [50]

$$V_{res} = \left(1 + \frac{C_s}{C_f}\right) V_{in} - \left(\frac{C_s}{C_f}\right)(V_{dac}) \tag{3.2}$$

Choosing $C_s = C_f$, equation (3.2) reduces to equation (3.1) with a typical gain of 2.

For 1-bit stage (having only 1 comparator with trip point (V_{trip}) set to mid of signal range), equation (3.1) can be written as

$$V_{res} = \begin{cases} 2V_{in} + V_{ref}, \ \mathrm{B} = 0, \ \mathrm{V_{dac}} = -V_{ref} \ if \ V_{in} < V_{trip} \\ 2V_{in} - V_{ref}, \ \mathrm{B} = 1, \ \mathrm{V_{dac}} = +V_{ref} \ if \ V_{in} \geq V_{trip} \end{cases} \tag{3.2a}$$

For 1.5-bit stage, equation (3.1) can be written as

$$V_{res} = \begin{cases} 2V_{in} + V_{ref}, \ B_1\mathrm{B}_0 = 00, \ \mathrm{V_{dac}} = -V_{ref} \ if \ V_{in} < \frac{-V_{ref}}{4} \\ 2V_{in}, \ B_1\mathrm{B}_0 = 01, \ \mathrm{V_{dac}} = 0 \qquad if \ \frac{-V_{ref}}{4} \leq V_{in} < \frac{V_{ref}}{4} \\ 2V_{in} - V_{ref}, \ B_1\mathrm{B}_0 = 10, \ \mathrm{V_{dac}} = +V_{ref} \ if \ V_{in} \geq \frac{V_{ref}}{4} \end{cases} \tag{3.2b}$$

Residue characteristics for 1-bit and 1.5-bit architectures are shown in Figure 3.2(a) and Figure 3.2(b) respectively. The 1.5-bit stage generates the residue voltage (V_{res}) and two bits B_1B_0 corresponding to the region in which the analog input falls as followed by equation (3.2b) and shown in Figure. 3.2(b). Referring to Figure 3.2, a 1-bit/stage has two regions (0 and 1) and the 1.5-bit/stage characteristic has three regions (00, 01 and 10) on the transfer characteristics and hence named 1.5bit/stage converter. Similarly, a 2-bit stage would have four regions (00, 01, 10, and 11) on the transfer characteristics.

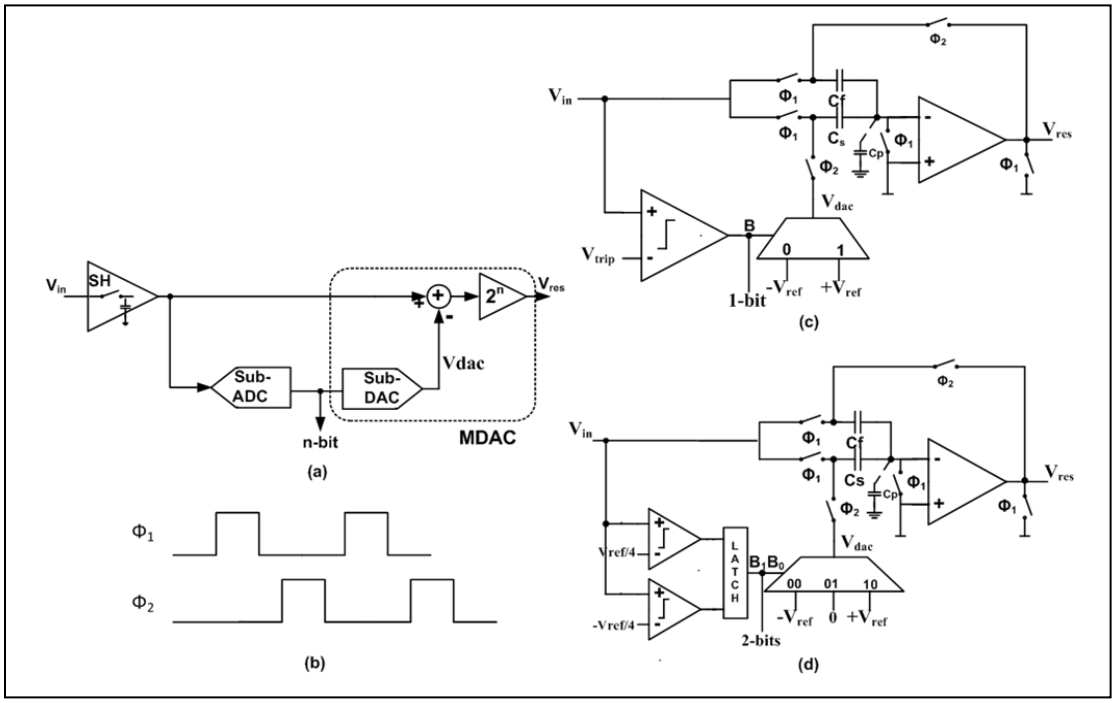


Figure 3.1. A pipelined ADC stage (a) general block diagram and (b) clocks, SC implementation of (c) 1-bit/stage (d) 1.5-bit/stage

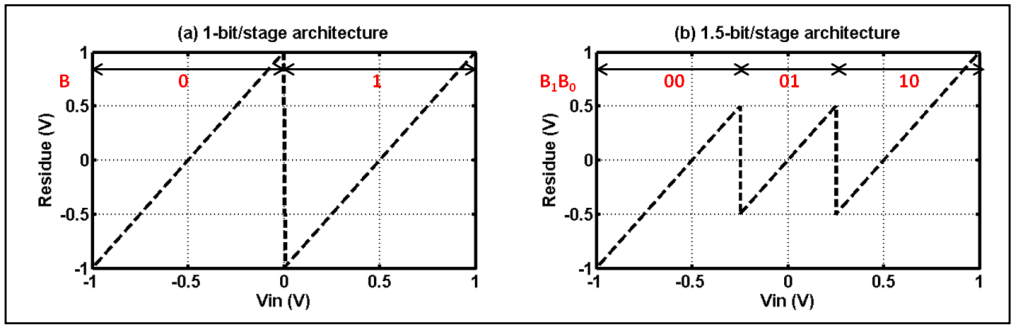


Figure 3.2. Residue characteristics of (a) 1-bit/stage (b) 1.5-bit/stage architecture

Complete n-stage pipelined ADC, shown in Figure 3.3, can be made by cascading such stages in pipeline fashion, except the last stage which consists of only sub-ADC part, thus in this way, at any time every stage will be processing the data, increasing the throughput of the ADC. For instance, if stage 1 is sampling the current input data in Φ_1 phase, stage 2 will be a amplifying the sampled data of 2nd stage (sampled during Φ_2 phase) and so on. The digital outputs ($B_i(n)$) of each stage are stored in digital latches [53] to synchronize all the bits for the final N-bit output in case of 1-bit architecture and in case of 1.5-bit architecture, bits stored in the latches are sent to Digital Error Correcting logic (DECL) [52].

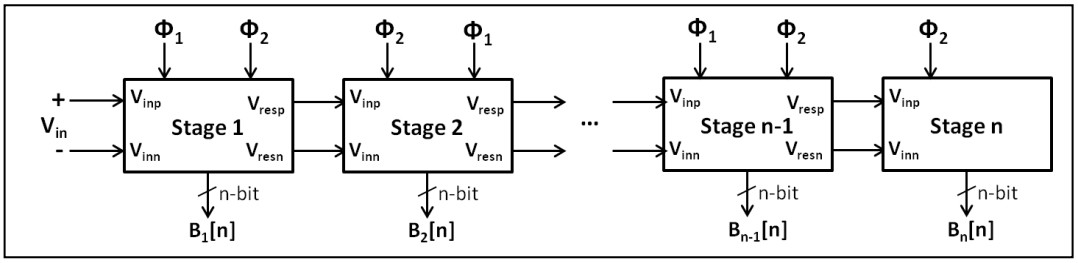


Figure 3.3. Cascading of pipelined ADC stages

The digital outputs of the stages are delayed by latches, a number of clock cycles, to make up for the latency on the analog signal path. In this thesis work, S/H amplifier is not implemented. Output of S/H amplifier, V_{in} is assumed to be available which is discrete in nature.

Last stage does not require any MDAC. It generates 2-bits and gives them to Digital Error Correcting logic for error correction. Since there is no opamp it can have comparator threshold offset error.

From equation (3.1), residue of a stage can be written as

$$V_{res} = 2V_{in} - DV_{ref} \tag{3.3}$$

with D = -1/1 for 1-bit/stage and D= -1/0/+1 in case of 1.5-bit/stage architecture. So using equation (3.3), residue voltage of stages can be written as

$$V_{res1} = AV_{in} - D_1V_{ref}$$

$$V_{res2} = AV_{res1} - D_2V_{ref}$$

$$= A^2 V_{in} - AD_1 V_{ref} - D_2 V_{ref}$$

$$V_{resn} = A^n V_{in} - A^{n-1} D_1 V_{ref} \ldots - D_n V_{ref}$$

$$= A^n \left(V_{in} - \sum_{i=1}^{n} A^{-i} D_i V_{ref} \right) \quad (3.4)$$

where gain of each stage is assumed to be equal (A=2) to simplify the expression. Equation (3.4) shows that the error in the initial stages will be amplified by larger amount down the stages and impact on ADC characteristics will be larger so the design requirements of initial stages become stringent as compared to later stages. In this work a 10-bit, 100 MSamples/s pipelined ADC with $V_{ref} = 1\text{V}$ is chosen for illustration purpose that has maximum quantization levels of 1024 (0 to 2^{10}-1). Since errors due to first stage is severe so only the impact of errors due to first stage are considered assuming all the remaining stages to be ideal. However, this can be extended to the other stages to include or model their errors and see the impact on whole of the ADC performance.

3.3 Various Errors and their Impact on ADC Performance

A pipelined ADC can be implemented using 1-bit/stage or 1.5-bit/stage architecture. Since, the impact of errors on overall ADC characteristics due to the first stage is intense so only impact of the errors due to the first stage are considered in this chapter assuming all the remaining stages to be ideal. Likewise this can be extended to other stages to include or model their errors and see the impact on the ADC performance. A 10-bit, 100 MSamples/s pipelined ADC with $V_{ref} = 1\text{V}$ is chosen for illustration purpose that has maximum quantization levels of 1024 (0 to 2^{10}-1).

3.3.1 Error due to Comparator offset

Comparator(s) used in the sub-ADC and the opamp used in MDAC can have unavoidable offset due to the variation in the process which can be minimized by careful layout. Due to comparator offset, residue voltage moves beyond the $\pm V_{ref}$ near the comparator trip points causing code saturation (*i.e.* same output code for different inputs, also known as wide codes) in 1-bit/stage architecture. Using 1.5-bit/stage, residue voltage never exceeds $\pm V_{ref}$ at comparator trip points so code saturation does not occur. Furthermore, because of digital error correcting logic (DECL) used in 1.5-bit/stage architecture, comparator offset within the

range of ±1/4 V_{ref} (*i.e.* ±0.25 V for $V_{ref} = 1V$) from comparator trip points does not cause any missing or change in output [52**]**. Figure 3.4 shows 1.5-bit/stage architecture with V_{os}' and V_{os} as the comparator offset voltage referred to comparator input and the opamp offset voltage referred to opamp input respectively.

To include the effect of comparator offset (+V_{os}'), equation (3.2a) is modified as

$$V_{res} = \begin{cases} 2V_{in} + V_{ref}, \ \mathrm{B} = 0, \ \mathrm{V_{dac}} = -V_{ref} \ if \ V_{in} < V_{trip} + V_{os}' \\ 2V_{in} - V_{ref}, \ \mathrm{B} = 1, \ \mathrm{V_{dac}} = +V_{ref} \ if \ V_{in} \geq V_{trip} + V_{os}' \end{cases} \quad (3.5)$$

Likewise equation (3.2b) can also be modified to include the comparator offset (+V_{os}') effect in 1.5-bit/stage architecture.

$$V_{res} = \begin{cases} 2V_{in} + V_{ref}, \ B_1\mathrm{B}_0 = 00, \ \mathrm{V_{dac}} = -V_{ref} \ if \ V_{in} < \frac{-V_{ref}}{4} + V_{os}' \\ 2V_{in}, \ B_1\mathrm{B}_0 = 01, \ \mathrm{V_{dac}} = 0 \qquad if \ \frac{-V_{ref}}{4} + V_{os}' \leq V_{in} < \frac{V_{ref}}{4} + V_{os}' \\ 2V_{in} - V_{ref}, \ B_1\mathrm{B}_0 = 10, \ \mathrm{V_{dac}} = +V_{ref} \ if \ V_{in} \geq \frac{V_{ref}}{4} + V_{os}' \end{cases} \quad (3.6)$$

Figure 3.5 shows the effect of V_{os}' on stage residue and overall ADC characteristic. It clearly shows the code saturation (or wide codes) and missing codes in ADC with 1-bit/stage whereas no missing codes in ADC output with 1.5-bit/stage for same comparator offset value. Therefore 1.5-bit/stage is immune to comparator offset as large as ±1/4 V_{ref} as compared to 1-bit/stage. Another cause of offset is due to opamp used in MDAC that is discussed in section 3.3.3.

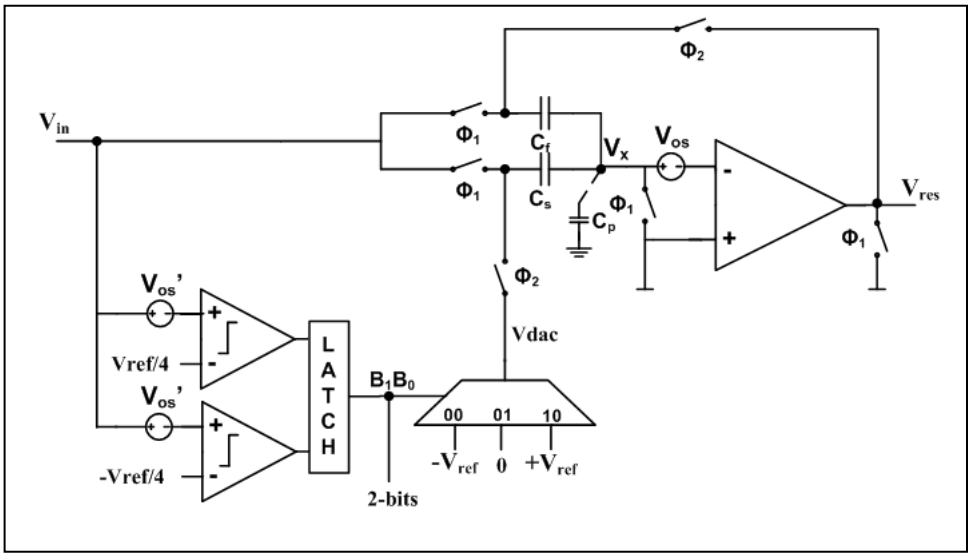


Figure 3.4. 1.5-bit/stages with comparator and opamp input referred offset voltages

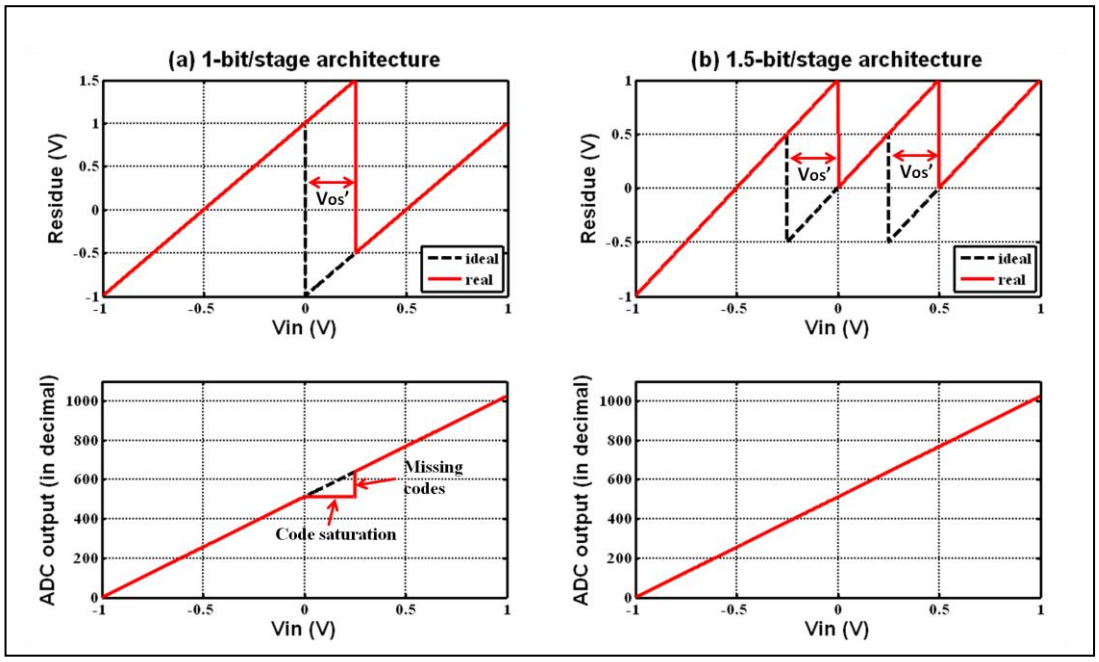


Figure 3.5. Impact with comparator offset of V_{os}'=+0.25V (a) 1-bit/stage (b) 1.5-bit/stage

From Figure 3.5, it is to be noted that a negative V_{os}' value will shift the transition points to the left of ideal curve and correspondingly a shift in code saturation and missing codes in 1-bit/stage architecture.

3.3.2 Error due to capacitor mismatch

From equation (3.2), by choosing $C_s = C_f$ typical gain of 2 is achieved but due to process variations, mismatch in capacitor changes the required gain. Let Δ be relative capacitor mismatch error *i.e.* $\Delta = (C_s - C_f)/C_f$, so to include the effect of capacitor mismatch equation (3.2) is modified to equation (3.7) [54]. This causes a change in stage gain (slope of residue curve) causing gain error as well as a change in sub-DAC value to be subtracted. Putting Δ in equation (3.2) leads to

$$\begin{aligned} V_{res} &= (2+\Delta)V_{in} - (1+\Delta)(V_{dac}) \\ &= [2\,V_{in} - (V_{dac})] + \Delta(V_{in} - V_{dac}) \end{aligned} \tag{3.7}$$

Impact of this error for positive Δ (i.e. $C_s > C_f$) is shown in Figure 3.6 for both 1-bit and 1.5-bit architectures. Due to positive Δ the stage gain is now more than the required gain of 2 causing the residue curve to exceed $\pm V_{ref}$ at the input values close to comparator trip points.

This results in code saturation (same code for different inputs) in the overall ADC characteristic for 1-bit/stage architecture whereas for 1.5-bit/stage ADC characteristic it causes non-monotonicity at the ADC

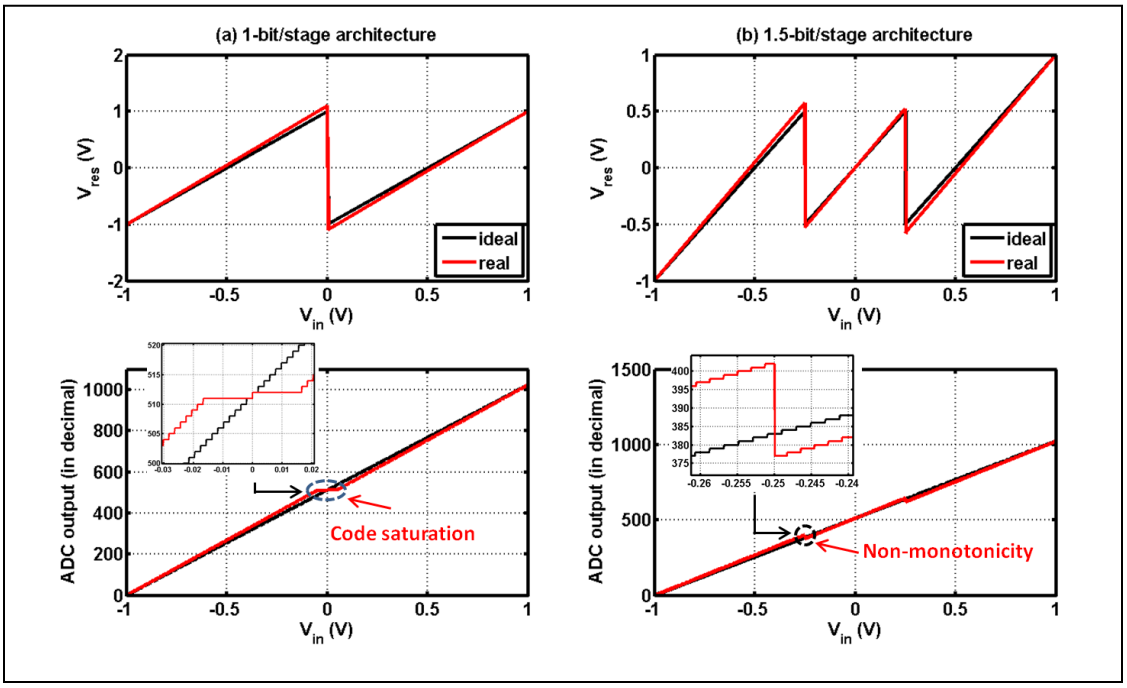


Figure 3.6. Impact with Capacitor mismatch (Δ=+0.2) on (a**)** 1-bit/stage (b) 1.5-bit/stage

output. Code saturation is difficult to remove but non-monotonicity can be avoided by using calibration techniques [51]**.** However, it is to be noted here that since capacitor mismatch is process dependent so relative capacitor mismatch error can be either positive or negative. For negative Δ, since stage gain is less than 2, there will be missing codes in 1-bit/stage and 1.5-bit/stage architecture which can be eliminated by the calibration technique.

3.3.3 Errors due to opamp

In equation (3.2), opamp is assumed to be ideal. However, in reality opamp has a finite gain, non-zero offset, finite GBW product, a non-linear voltage transfer characteristic which limit the performance of a stage and consequently the ADC output.

For high resolution ADC, opamp open-loop gain is required to be high. Low open loop gain causes the gain error which results in missing codes and thus limits the resolution. Let A be the finite open loop DC gain of opamp, due to finite gain virtual node property of opamp gets vanished and $\boldsymbol{V_x}$ node (shown in Figure 3.4) during charge transfer phase (Φ_2=1) is now

equal to $-V_{res}/A$. From Figure 3.4, considering only opamp finite gain effect keeping comparator offset (V_{os}') and opamp offset (V_{os}) zero, the total charge at V_x node during sampling phase is given by

$$q_x(\Phi_1) = (V_x - V_{in})(C_s + C_f) \tag{3.8}$$

and charge at V_x node during amplification phase is given by

$$q_x(\Phi_2) = (V_x - V_{dac})C_s + (V_x - V_{res})C_f + V_x C_p \tag{3.9}$$

where C_p is the parasitic capacitance at V_x node. It is to be noted here that during Φ_1 opamp is reset so C_p does not contribute in charge calculation. Since charge is conserved at V_x node so equating equation (3.8) with equation (3.9) and solve for V_{res} with $V_x(\Phi_1) = 0$ and $V_x(\Phi_2) = -V_{res}/A$ gives [55]

$$V_{res} = \left(\frac{1}{1+\frac{1}{A\beta}}\right)\left[\left(1+\frac{C_s}{C_f}\right)V_{in} - \left(\frac{C_s}{C_f}\right)(V_{dac})\right] \tag{3.10}$$

$$V_{res} \approx \left(1-\frac{1}{A\beta}\right)\left[\left(1+\frac{C_s}{C_f}\right)V_{in} - \left(\frac{C_s}{C_f}\right)(V_{dac})\right] \tag{3.11}$$

where $1/A\beta$ is termed as gain error, denoted by ε_g, which causes the gain of a pipelined ADC stage to become less than the required gain of 2 and β is the feedback factor $\left(\frac{C_f}{C_s+C_f+C_p}\right)$. Since the gain of a stage is now less than 2 so stage output does not reach full swing (*i.e.* V_{ref}), causing missing codes at the ADC output at comparator trip points which can be minimized by using calibration technique. Figure 3.7 shows the impact of finite open loop opamp gain in stage residue curve and ADC output characteristics for both 1-bit and 1.5-bit architectures.

In order to avoid the missing codes due to finite opamp gain, the minimum gain required by the first stage opamp can be obtained by using equation (3.12). The gain error term must be less than the half LSB of the remaining resolution. For instance the gain requirement for first the stage opamp follows

$$\frac{1}{A\beta} \leq \frac{1}{2}\cdot\frac{V_{FS}}{2^{n-1}} \tag{3.12}$$

where n is the resolution of ADC. For $\beta = 0.5$, equation (3.12) results in $A \geq 2^{n+1}$. Therefore, for 10-bit ADC minimum open loop gain required by first stage opamp is 60 dB.

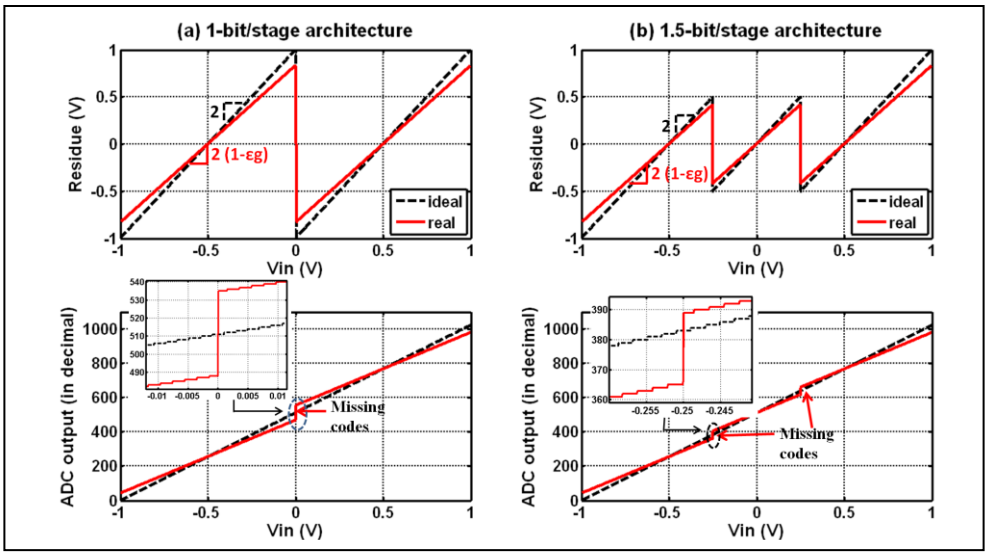


Figure 3.7. Impact of low opamp gain (a) 1-bit (b) 1.5-bit characterstics

In reality, C_p and other parasitic capacitances at V_x node reduces the feedback factor below 0.5 so while designing CMOS opamp, two times more gain is considered. Figure 3.7 shows the impact of open loop opamp gain in a stage residue curve and ADC output characteristics for 1.5-bit architectures. There are large missing codes with low opamp gain as shown in Figure

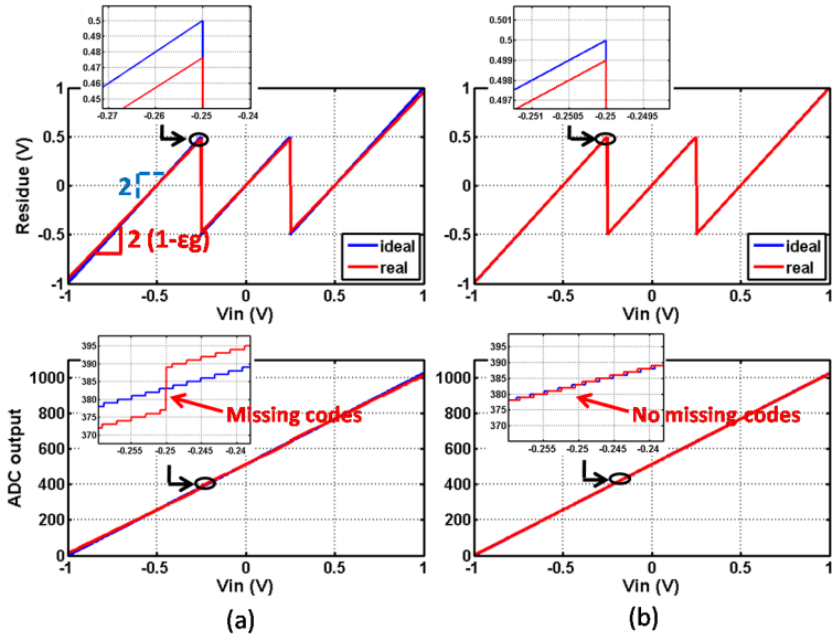


Figure 3.8. Impact of finite opamp gain (a) low gain (b) gain derived from equation (3.12)

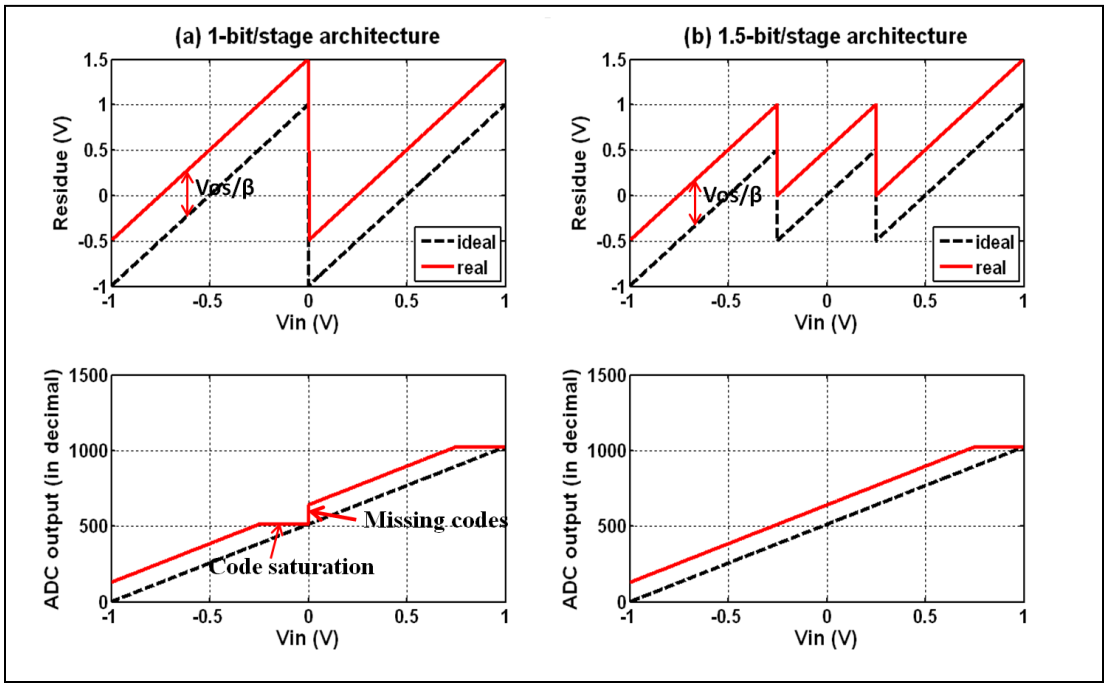


Figure 3.9. Impact of opamp offset of Vos = +0.25V on (a**)** 1-bit/stage (b) 1.5-bit/stage

3.8(a) and no missing codes using sufficiently high gain opamp (following equation (3.12)) in Figure 3.8(b).

There is another offset other than comparator offset that rises due to opamp used in MDAC, modeled by V_{os} as shown in Figure 3.4. Following the same anaylsis of charge conservation as mentioned in section 3.3.3 and incorporating the finite opamp gain effect with opamp offset with $V_x(\Phi_1) = 0, V_x(\Phi_2) = V_{os} - V_{res}/A$ and solving for V_{res} gives

$$V_{res} \approx \left(1 - \frac{1}{A\beta}\right)\left[\left(1 + \frac{C_s}{C_f}\right)V_{in} - \left(\frac{C_s}{C_f}\right)(V_{dac}) + \frac{V_{os}}{\beta}\right] \qquad (3.13)$$

Here considering only the effect of opamp offset and assuming infinite opamp gain, there occurs a vertical shift in residue characterstics from ideal one as clear from equation (3.13). Figure 3.9 shows the impact of positive opamp offset on residue characteristics and the whole ADC output for both the architectures. At comparator trip points, there occurs the code saturation and missing codes in ADC with 1-bit/stage whereas in 1.5-bit/stage for same opamp offset value there is vertical shift in curve above the ideal curve with no missing codes in ADC output. A negative offset will shift the curve below the ideal one. Missing codes can be eliminated by calibration but it is difficult to remove the code saturation problem [51].

In order to avoid the shifting of curve due to opamp offset, the minimum opamp offset required by the first stage opamp can be obtained by using equation (3.14). The offset error term must be less than half LSB of the remaining resolution

$$\frac{V_{os}}{\beta} \leq \frac{1}{2} \cdot \frac{V_{FS}}{2^{n-1}} \tag{3.14}$$

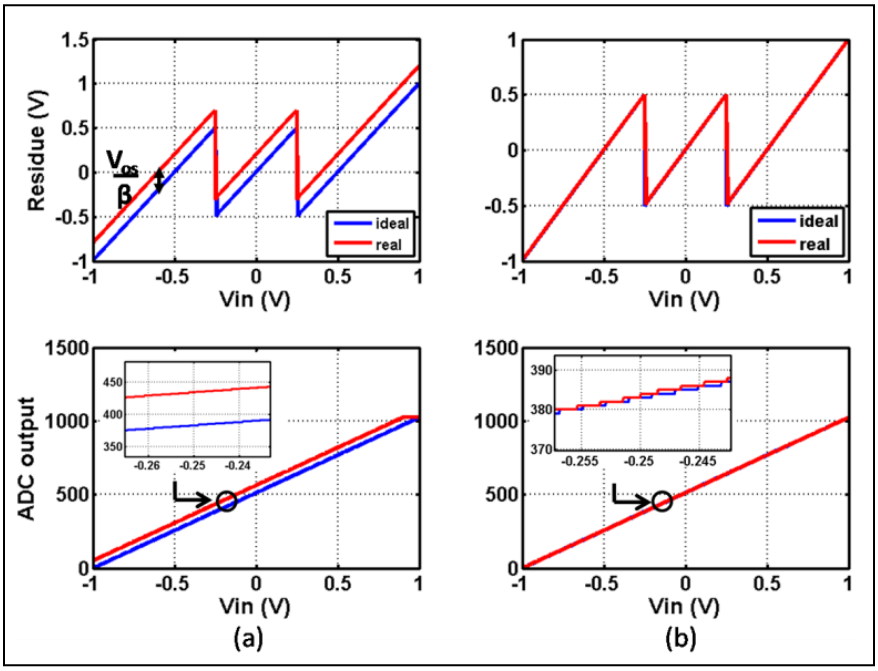


Figure 3.10. Impact of opamp offset

Therefore, in 10-bit pipelined ADC, minimum opamp offset required by first stage opamp should be less than 0.97 mV.

Another cause of error due to opamp is the non-linearity introduced by it which must be avoided. In ideal opamp gain is in linear relation with input whereas in real opamp this relation becomes nonlinear within the signal range $\pm V_{ref}$. This is due to the reason that transistors in opamp output stage enter the linear region (from saturation) near the edges of signal range as shown in Figure 3.11(a) where $\pm V_{sat}$ is the output saturation voltage of opamp. This non-linear relation around $\pm V_{ref}$ causes reduction in gain (shown in Figure 3.11(b)) and further introduces non-linearity [56].

Practically, pipelined ADC is implemented differentially with opamp follows that of odd function, its open loop transfer function can be modelled by including odd order terms as given by

$$V_{outd} = AV_{id} + \alpha_3 \cdot V_{id}^3 + \alpha_5 \cdot V_{id}^5 \tag{3.15}$$

where A is the gain of opamp and α_3, α_5 are the third order and fifth order nonlinearity parameter respectively with V_{id} and V_{outd} as the opamp differential input and output respectively. From equation (3.15) it is clear that for ideal opamp $\alpha_3 = \alpha_5 = 0$, opamp output is linearly proportional to the input and gain remain constant whereas in case of non-ideal opamp nonlinearity increases with the increase in input as shown in Figure 3.11.

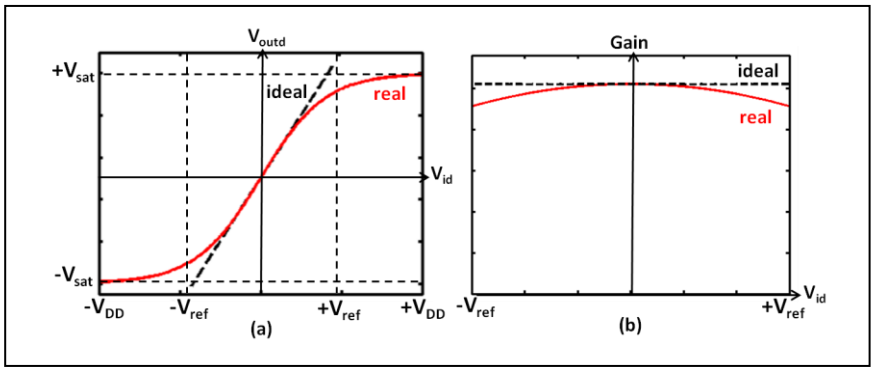


Figure 3.11. Opamp (a) transfer characterstics (b) gain characterstics

Since in a pipelined ADC stage, opamp is used in feedback configuration during Φ_2 phase (from Figure 3.1) so from equation (3.15), transfer function in the closed loop configuration can be written as [57]

$$V_{outd} = \frac{A}{1+A\beta} V_{id} + \frac{\alpha_3}{(1+A\beta)^3} {V_{id}}^3 + \frac{\alpha_5(1+A\beta)-2\beta\alpha_3^2}{(1+A\beta)^5} {V_{id}}^5 \tag{3.16}$$

where $\frac{A}{1+A\beta}$ in the first term is the closed loop gain of stage with ideal value of 2. Let equation (3.1) be rewritten as

$$V_{res1} = 2(V_{in} - 0.5\, V_{dac}) \tag{3.17}$$

Comparing equation (3.16) and equation (3.17) shows the stage residue can be written as

$$V_{res} = V_{res1} + \alpha_3' {V_{res1}}^3 + \alpha_5' {V_{res1}}^5 \tag{3.18}$$

where α_3' and α_5' are third order and fifth order non-linearity parameters of pipelined ADC stage in feedback configuration. Effect of opamp non-linearity is shown in Figure 3.12. It shows the large missing codes at comparator trip points in 1-bit/stage based architecture as compared to 1.5-bit/architecture since nonlinearity is maximum at extreme signal ends.

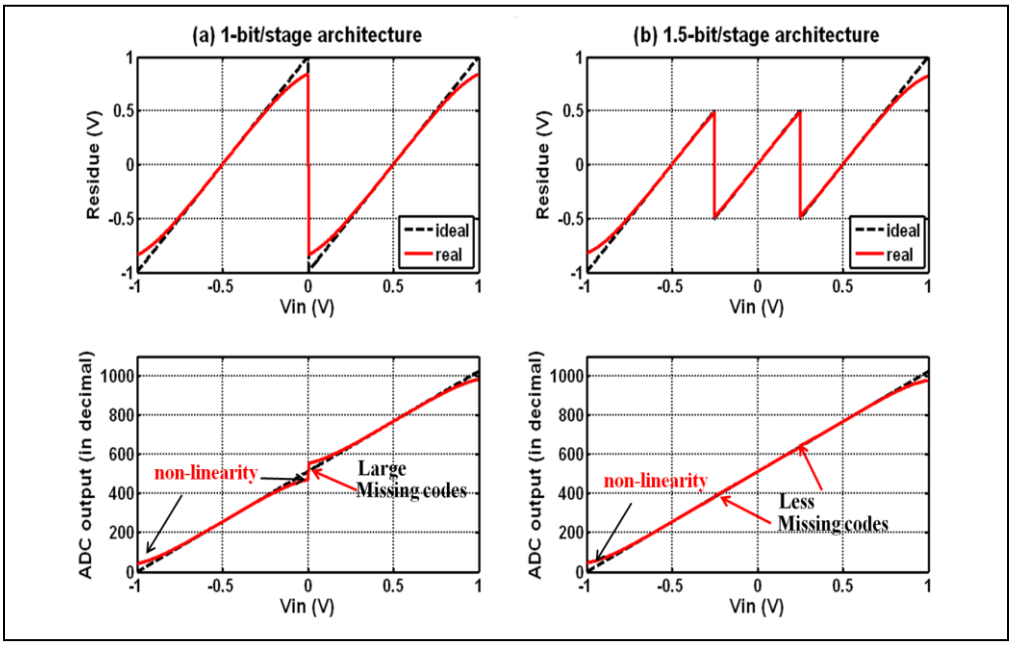


Figure 3.12. Impact with non-linear opamp gain on (a) 1-bit/stage (b) 1.5-bit/stage

All the individual errors defined in equation (3.5) to equation (3.18) can be combined together to see their impact on the individual stage transfer characteristics and overall ADC characteristics of pipelined ADC. All the above errors due to opamp offset ($\pm V_{os}$), due to capacitor mismatch ($\pm\Delta$), due to finite opamp gain (A) and due to opamp nonlinearity are included in equation (3.19) and diagrammatically shown in Figure 3.13 for single stage where

$$x \approx (1-\varepsilon_g)\left((2\pm\Delta)V_{in} - (1\pm\Delta)(V_{dac}) \pm \frac{V_{os}}{\beta}\right) \tag{3.19}$$

with ε_g as the gain error given by $\frac{1}{A\beta}$. For the final residue of a stage, assume $G(x)$ as the non-linearity functional block that includes third order and fifth order polynomial. Including non-linearity the residue of a stage is given by

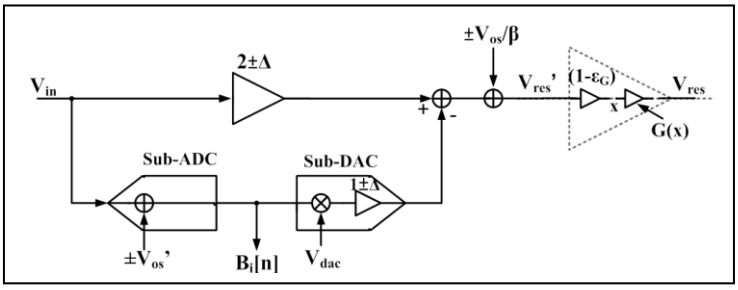


Figure 3.13. Complete pipelined ADC error model for *i*-th stage

$$G(x) = V_{res} = x + a_3x^3 + a_5x^5 \tag{3.20}$$

where a_3 and a_5 are the non-linearity coefficients.

The characteristics including the errors in the first pipelined stage and its impact on overall ADC (assuming rest of the stages ideal) are shown in Figure 3.14.

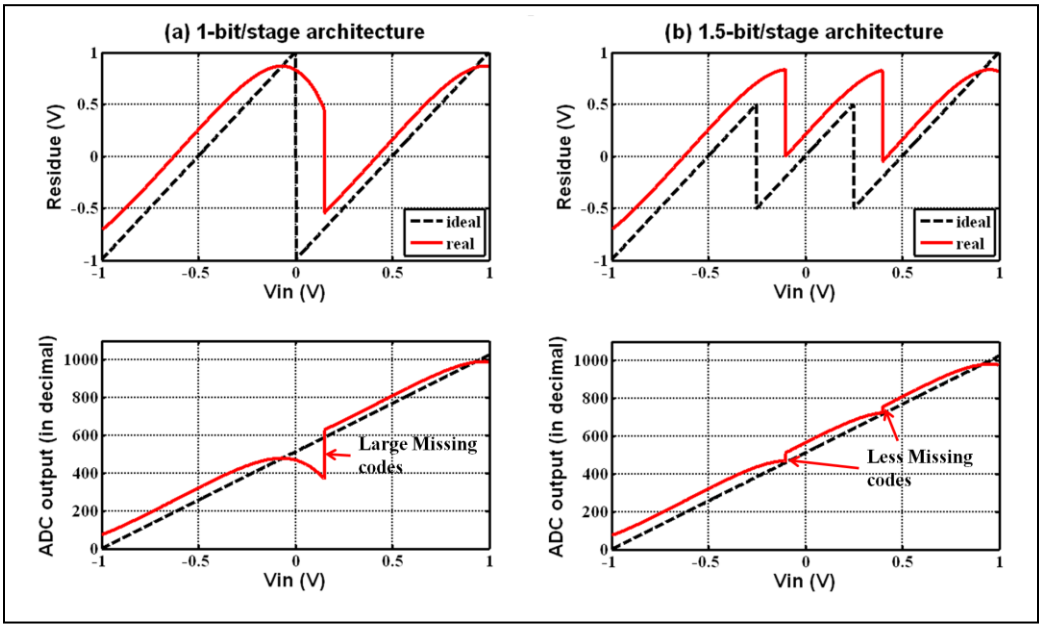


Figure 3.14. Impact of all the errors on (a) 1-bit/stage (b) 1.5-bit/stage with comparator offset (V_{os}') = +0.15V, opamp offset (V_{os}) = +0.1V, finite opamp gain, $\Delta = 0.1$ and non-linearity.

Another important opamp performance limitation is due to its Slew Rate and Settling time. Former is due to opamp's finite sinking/sourcing current capability while latter is due to insufficent Gain Bandwidth product (GBW) and Phase margin (PM). When the differential input (V_{id}) of opamp is within $\pm\sqrt{2}\,(V_{gs} - V_t)$ range, current flowing through opamp is proportional to V_{id}, given by $g_m V_{id}$ where g_m is the transconductance of input MOS transistors otherwise maximum current (I_{ss}) flows [58]. Figure 3.15(a) shows SC circuit with V_{dac} as step input (V_{step}) applied to negative terminal of opamp during amplification phase. Depending upon the amplitude of step input following equations are applied [59].

$$V_{res}(t) = V_{step}\left(1 - e^{-t/\tau}\right) \quad if\ V_{step} \leq V_{lin} \tag{3.21a}$$

$$V_{res}(t) = \begin{cases} SR \times t & if\ t \leq t_{sr} \\ V_{step} - (V_{step} - V_{out}(t_{sr}))e^{(t_{sr}-t)/\tau} & if\ t \geq t_{sr} \end{cases} if\ V_{step} \geq V_{lin} \tag{3.21b}$$

where V_{lin} is the input voltage range for which input MOS transistors are in saturation and behave linearly to input and $V_{out}\,(t_{sr})$ is the output voltage at the end of Slew time. Figure 3.15(b) and Figure 3.15(c) shows the small signal model during slewing time and settling time of SC circuit and Figure 3.15(d) shows the response of SC circuit with negative step applied according to equation (3.21). During slew time, maximum current flows that causes distortions at the ADC output and results in decrease in SNDR and SFDR of an ADC. Whereas in linear settling-time, current flown is proportional to the input signal therefore opamp and consequently ADC behaves linearly to input [60].

Another important parameter in opamp's response to step input is accuracy which in defined by settling error (ε_s) and must be less than 0.5 LSB within the allotted time in ADC design in order to have no missing codes at the ADC output. Figure 3.16 shows the ε_s in the settling followed by slew response of opamp in an ADC.

For instance, for a 10-bit, 100 MS/s pipelined ADC working on two non-overlapping clocks, time available for opamp's charge transfer phase is 5ns and the required accuracy for first stage opamp is 0.0977% so opamp has to settle to the required accuracy of 0.0977% in 5ns. Time response of opamp to step input is modeled by taking the time constant of the circuit which is defined by GBW and feed-back factor (β) for SC circuit. It is given by equation (3.22)

$$\tau = \frac{1}{\beta\ GBW} \tag{3.22}$$

where β is given by $C_f/(C_s+C_f+C_p)$. Considering a first order, settling limited transient response only, transfer function of pipelined ADC stage may be modified to give equation (3.23)

$$V_{res} \approx \left(1 - e^{-t/\tau}\right)\left[\left(1 + \frac{C_s}{C_f}\right)V_{in} - \left(\frac{C_s}{C_f}\right)(V_{dac})\right] \tag{3.23}$$

with settling error (ε_s) given by $e^{-t/\tau}$.

From equation (3.21) and equation (3.22), it is clear that for V_{res} to settle to the required accuracy (*i.e.* less than 0.5 LSB), UGB is required to be high. Otherwise it causes the error at the stage output similar to that of finite opamp gain and further results in missing codes at the ADC output. Figure 3.16 shows the transient response of an opamp in an ADC with slew time of 1τ followed by settling time of 7τ.

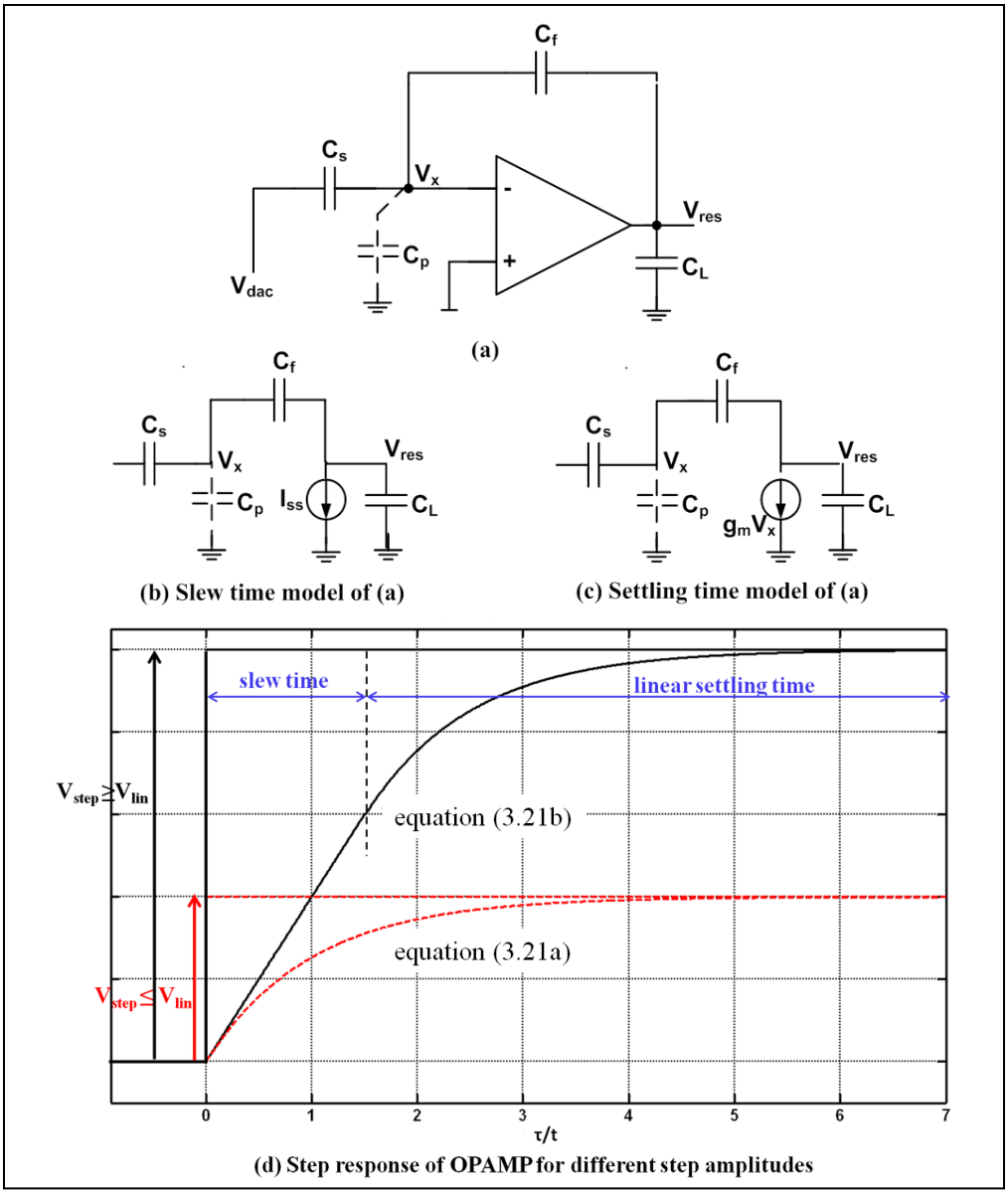


Figure 3.15. Step response of opamp (a) in SC configuration (b) its Slew Rate time model (c) Settling time model and (d) response for different negative step amplitudes vs. τ/t.

Therefore time required for first stage residue voltage, V_{res}, to settle to the required accuracy (i.e. settling error less than 0.5 LSB of remaining resolution) is given by

$$t_{sl} \cong 7\tau$$

$$= 7 \cdot \frac{1}{2\pi\beta\ UGB} \tag{3.24}$$

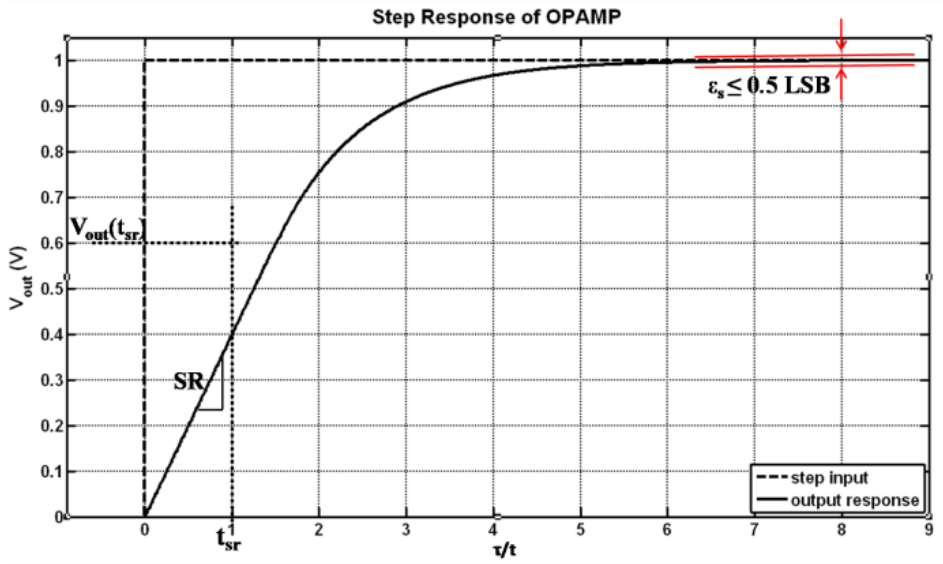


Figure 3.16. Step response of opamp vs. τ/t in SC configuration for negative step

For f_S MS/s Pipelined ADC working on two non-overlapping clocks, available time for opamp's charge transfer phase is $t_S/2$. Therefore considering $t_{sl} < t_S/2$, required UGB of opamp is given by

$$UGB > \frac{7f_S}{\pi\beta} \tag{3.25}$$

For 100 MS/s Pipelined ADC, the minimum UGB required for opamp is 440 MHz. In practice while designing opamp, some time is required in slewing (t_{sr}) therefore time required for settling becomes less and consequently required UGB is high, atleast by a factor of 3.

Based on concepts and modeling approach described in this chapter, a 10-bit pipelined ADC is implemented behaviorally with opamp errors in its initial 6 stages. Its INL/DNL plot and Fast-Fourier Ttransform (FFT) response is shown in Figure 3.17 with SNR of about 47dB and SNDR of 38.6 dB. It shows a significant loss in SNR, SNDR and SFDR values due to various errors inserted in pipelined ADC stages. It is always desirable to have large value of SNR, SNDR and SFDR in order for the ADC to have a quality digital signal at the output. Opamp being the main processing block in pipelined ADC limit the performance of ADC. Therefore much of the design effort is devoted to design a robust opamp that has high open

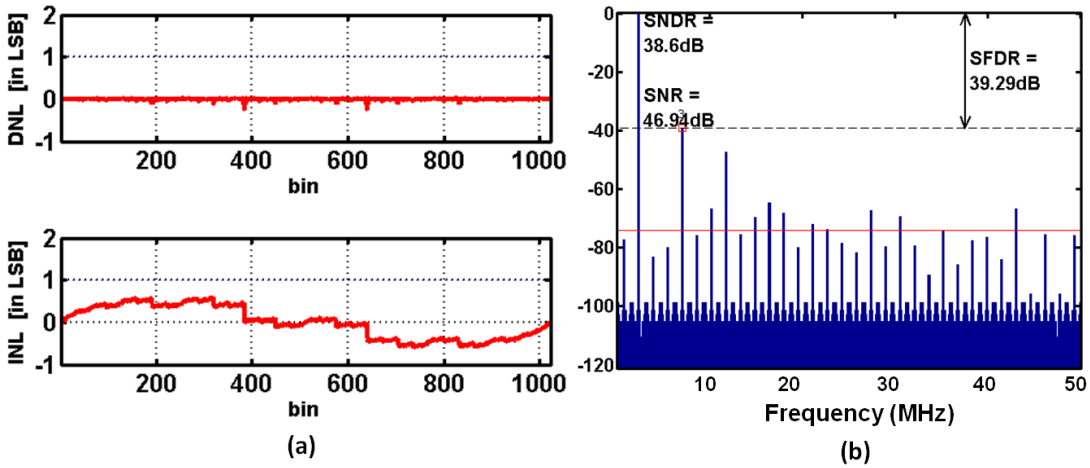


Figure 3.17. (a) INL/DNL plot (b) FFT response with 1024 points

loop gain, high bandwidth and very less offset. In current deep submicron technologies, it becomes a challenging task to design such opamp due to reduced intrinsic gain of devices.

1.5-bit is a modification to 1-bit architecture. Instead of 1-bit/stage, some redundancy is built in 1.5-bit stage to provide a large tolerance against comparator offset and imperfections as shown in Figure 3.5. Therefore a low power, high speed, but high value offset comparator can be used in 1.5-bit architecture which greatly simplifies the design of a pipelined ADC stage. Following is the comparison table of different pipelined ADC stage architectures.

Table 3.1. Comparison table of different pipelined ADC stage architectures

Stage Architecture	1-bit	1.5-bit	2-bit	2.5-bit	3.5-bit
Output bits/stage (N)	1	2	2	3	4
Stage gain	2	2	4	4	8
Required number of Comp	1	2	3	6	14
Ideal Feedback factor (b)	0.5	0.5	0.25	0.25	0.125
Redundancy	No	Yes	No	Yes	Yes
Maximum comparator offset tolerance	No	±Vref/4	No	±Vref/8	±Vref/16

As Table 3.1 shows, increasing the stage resolution to 2.5-bit requires 6 comparators with higher accuracy in its sub-ADC. Required stage gain is 4 and feedback factor is 0.25. The

comparator offset tolerance reduces with increase in stage resolution. Further design complexity increases for 3.5-bit/stage architecture.

From equation 3.2, residue voltage of a stage is dependent upon the feedback factor and opamp bandwidth. As the stage resolution increases feedback factor decreases that results in increase in demand of opamp bandwidth for the same settling accuracy and hence power. Thus for high-speed converters, there's an advantage to have minimum stage resolution. It minimizes the required interstage gain, which in turn maximizes bandwidth for a given power budget.

For an N-bit pipeline ADC, the requirement of capacitor matching ac-curacy for then n-bit first stage is (N–n)-bit. Since capacitor mismatch is inversely proportional to the square root of the total capacitance value, the whole size of the capacitors in the first stage MDAC of a 2.5-bit topology is only half of the 1.5-bit. The reduction of capacitor size evidently decreases the area of a 2.5-bit stage. With decreasing capacitive load, the am-plifier in a 2.5-bit stage is more feasible and power economical. Finally, the 2.5-bit/stage structure benefits more power and area advantage from stage number reduction. Thus for a given area power budget 1.5bit stage is small and fast as compared to 2.5-bit. However for a given ADC resolution it requires lesser number of 2.5-bit stages instead of 1.5-bit stages.

3.4 Summary

Various sources of errors in 1-bit/stage and 1.5-bit/stage architecture and their impact on stage characteristic, and on the ADC characteristic is discussed in the chapter. The 1.5-bit/stage architecture is widely used in high speed high pipelined ADC due to various advantages that are discussed in the chapter. It can tolerate the comparator offset as large as $\frac{V_{ref}}{4}$ and also can be designed to tolerate the opamp offset. Opamp in particular contributes significant errors to pipelined ADC. All such errors have been modeled using MATLAB. Also dynamic performance of opamp is modeled to understand the impact due to low opamp bandwidth along with slew-settling time behavior of opamp is modeled and analyzed.

Chapter 4

OPAMP-less Pipelined ADC Stage

4.1 Introduction

With the rise in the demand of portable devices, circuit designers face many challenges in terms of having more functionality at reduced cost, area with longer battery life. Scaling down of CMOS technology along with supply voltage makes it possible for the designers to meet these challenges. However, in a silicon-on-chip (SoC) with both analog and digital part together, digital part gets the benefits of increase in speed but analog part suffers due to decrease in the voltage signal swing, gain and signal-to-noise ratio (SNR). These problems force the researchers to find the innovative solutions.

Pipelined ADC is best suitable for high speed (10-500 MHz)and high resolution (10-15-bits) applications [18]. One of the major problems in pipelined ADC is power dissipation. Operational amplifier (opamp) is the major contributor to it which is used in multiplying digital-to-analog converter called MDAC. Henceforth, encourages the researchers to look for the other circuit design techniques to avoid the cause of above said problem. Some of solutions found in the literatures are listed in Table 4.1.

Table 4.1. Different techniques used in pipelined ADC (year wise)

Reference	Technique used	Year
[18]	residue amplification using open loop amplifier	2003
[20]	comparator based Switched Capacitor (SC) circuits	2006
[61]	Using open loop amplifier	2007
[22]	zero-crossing based circuits	2007
[19]	incomplete settling	2007
[29]	dynamic source follower based amplification	2009
[30]	capacitive charge pump based technique	2010
[62]	current charge pump based amplification	2011

As a consequence of replacing the opamp, missing codes and nonlinearity occur at the output of the ADC which is compensated by using a digital calibration technique

[18-19, 29-30, 61-62]. Although, there is increase in the area-power in the digital domain but it is much less as compared to whole ADC [18].

Furthermore, linear capacitors are generally used in pipelined ADC in order to avoid any kind of error that occurs due to capacitor mismatch. Linear capacitors in modern technologies are available between the two top metal layers (M5 and M6 in present work), called MIMCAPs. Drawback of using MIMCAPs is the increase in the numbers of fabrication masks and therefore cost. Capacitance density is also poor due to which it consumes larger silicon area for a small capacitance value.

To deal with the problem of area and cost, MIMCAPs can be replaced with the capacitance offered by the MOSFETs (*i.e.* MOSCAP). As compared to MIMCAP, it has higher capacitance density, good matching and readily available in every CMOS process. Despite these benefits it has a disadvantage that its value is dependent on the voltage across it which causes the nonlinearity errors at the ADC output. In earlier works [63-64], MOSCAPs have been used in switched-capacitor (SC) circuits to implement all the capacitors. This approach has also been extended to opamp based pipelined ADC that consumed large area-power. Here, nonlinearity due to MOSCAPs is eliminated by using the digital calibration techniques [65-66].

The present research work is an effort to reduce the power consumption, area and cost. It uses the charge-pump based technique [30] that avoids the opamp to save the power and uses the MOSCAPs instead of linear capacitors to reduce area and manufacturing cost. Present work offers the various advantages over the earlier work [30]. MOSCAPs are since easily available in every CMOS process; it therefore allows the analog blocks to easily integrate with the digital blocks in a system-on-chip (SoC) to reduce the overall cost. Capacitance density of MOSCAP is higher as compared to MIMCAPs therefore it requires lesser silicon area for the same capacitance value, reducing the cost further. To show the effectiveness of the concept, a 1.5-bit pipelined ADC stage is designed in 0.18 µm digital CMOS technology.

4.2 MOSCAP based 1.5-bit Pipelined Stage

This section discusses the brief introduction to MOSCAP and analysis of MOSCAP based 1.5-bit pipelined ADC stage.

4.2.1 MOSCAP using MOSFET

Figure 4.1 shows the MOSCAP C-V characteristics for both n-channel and p-channel with $V_{DS} = V_{BS} = 0$, t_{ox}= 4.1 nm and W=L=10.85µm and vary its gate-to-channel potential (V_{GB}). Here W and L are the width and length of the MOSCAP respectively, and t_{ox} is the thickness of thin SiO_2 beneath the ploy gate. It shows a very small variation in the accumulation as well as in the strong inversion regions but in the depletion region variation is very high [67].

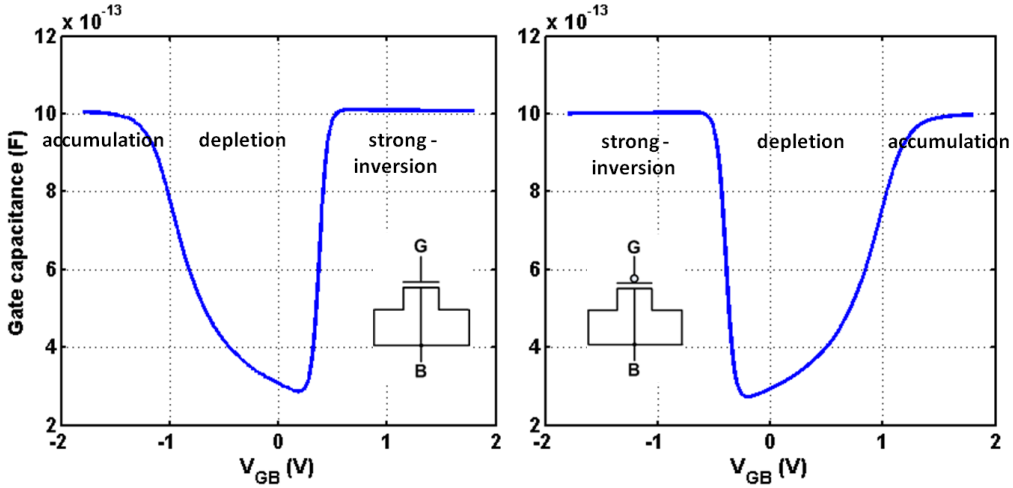
In the strong inversion region capacitance offered by the MOSCAP is mainly due to oxide capacitance and given by

$$C = \frac{\in_{sio_2} WL}{t_{ox}} \tag{4.1}$$

In strong inversion region the variation is small and can be expressed by [68]

$$C(v) = C(1 + \alpha v) \tag{4.2}$$

where α is the coefficient of linearity, expressed in ppm/V and v is the voltage across the MOSCAP. It is clear from the Figure 4.1 that capacitance value is relatively independent of change in voltage across it if biased in the strong inversion region.



(a) (b)

Figure 4.1. MOSCAP curve (a) n-channel (b) p-channel

The area comparison between MOSCAP and MIMCAP for the given Mixed-Mode and Digital 0.18µm CMOS processes is shown in Figure 4.2 with the MOSCAP giving an area advantage of about 8.4 times as compared to MIMCAP for same capacitance value. This

Capacitor (pF)	Area (μm²)	
	MIMCAP	MOSCAP
0.2	196	23.3
0.5	493.51	58.64
1.0	992.25	117.72
2.0	1989.16	235.62
3.0	2986.62	351.56
5.0	4979.42	590.49

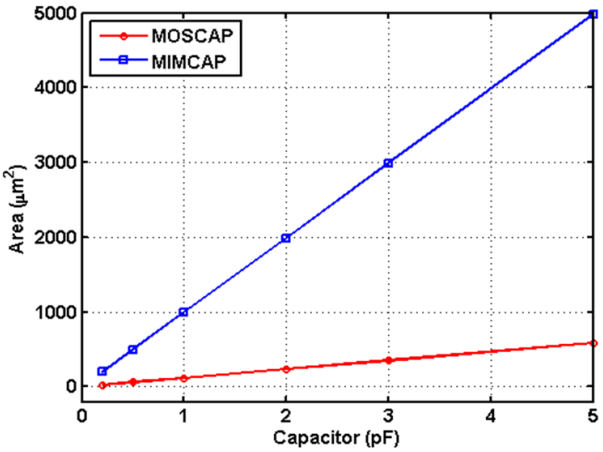


Figure 4.2. Area comparison: MOSCAP vs. MIMCAP in 0.18um technology

stems from the fact that capacitance in MIMCAP is available between top two metal layers (M5 and M6 in current 0.18μm Mixed-Mode process) where oxide layer in between them is thick. Also MOSCAP gives better capacitance matching over the MIMCAP [66, 69].

In the present research work, n-well process is available therefore p-channel MOSCAP is used (as shown in Figure 4.1(b)) and biased in strong inversion region for the whole signal range with the help of some bias potential.

4.2.2 MOSFET-only 1.5-bit Fully Differential Pipelined ADC Stage

Proposed MOSFET-only 1.5-bit fully differential pipelined ADC stage is shown in Figure 4.3 [70]. The clocking scheme as used in traditional opamp based pipelined ADCs is followed in the present work. Two non-overlapping clocks Φ_1 and Φ_2 are the used with Φ_{1e} as the advance version of Φ_1 used for bottom plate sampling. A buffer with the gain A_{buff} is the used to avoid the charge sharing that occurs between the present stage and the next stage. From the analysis, it is found that charge sharing occurs between the nodes $x4/x4'$ of the present stage and V_{inn}/V_{inp} of the next stage when amplification clock (Φ_2) falls. This alters the charge stored on the sampling MOSCAPs. Therefore a buffer is used to prevent the charge sharing, taking into consideration its unidirectional property. Furthermore, buffer is activated only during amplification phase (Φ_2) in order to isolate the output from input.

As explained in section 3.2, two bits (B1, B0) are generated by the sub-ADC block and send to the storage elements (flip-flops) in order to synchronize all the bits generated by the cascading pipelined ADC stages and also to sub-DAC block that generates the reference

voltages $V_{dacp\,(n)}$ [11]. Last stage (Stage n) in Figure 4.3 generates no residue therefore consists of only sub-ADC part.

Figure 4.4 shows the different phases of charge-pump based stage used in the present work. Initially, during the sampling phase ($\Phi_1 = 1$) applied input voltage is sampled on the MOSAPs C_1 and C_2. During the amplification phase ($\Phi_2 = 1$), previously sampled input voltage is added up by connecting the MOSCAPs in series, thus giving a voltage sum of 2. The different phases of entire operation are explained as below.

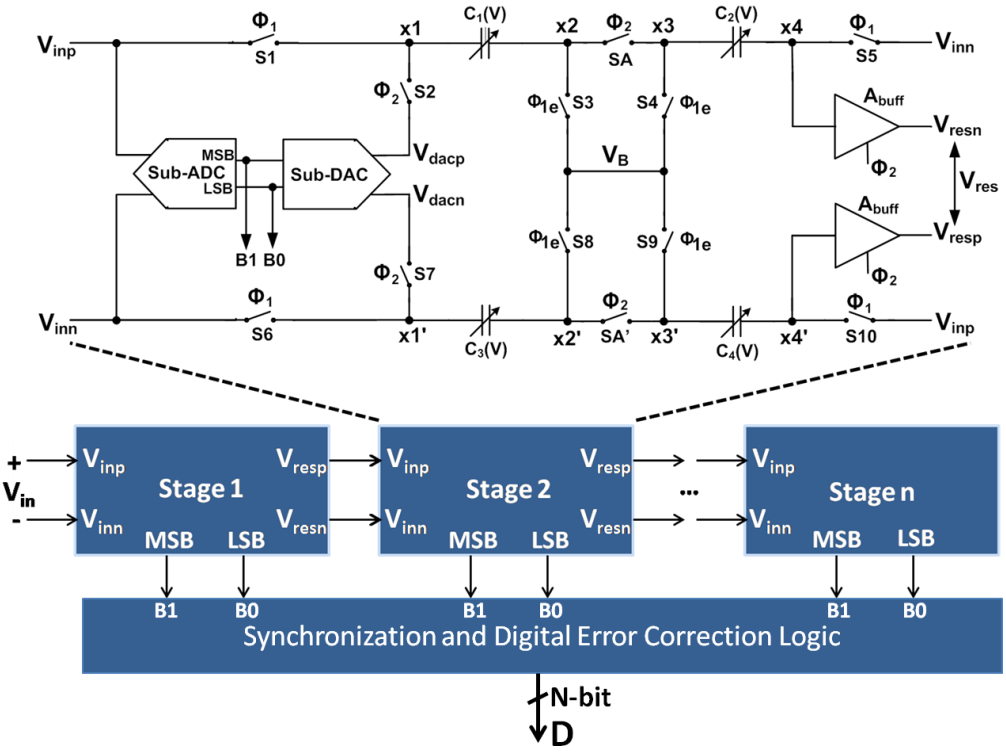


Figure 4.3. N-bit pipelined ADC with proposed pipelined ADC stage

Figure 4.4 shows the single ended version of Figure 4.3 with linear capacitors replaced by MOCAPs. Operation starts with sampling of the input voltage on the MOSCAPs C_1 and C_2 (Figure 4.4(a)). Ignoring the effect of parasitic capacitances at various nodes, the charge stored on the nodes $x2$ and $x3$ is given by

$$Q_{x2}(\Phi_1) = C_1(V_B - V_{inp}) \tag{4.3}$$

$$Q_{x3}(\Phi_1) = C_2(V_B - V_{inn}) \tag{4.4}$$

Amplification phase is shown in Figure 4.4(b). At the start of the amplification phase (rise of Φ_2), output of sub-DAC (V_{dacp}) is connected to $x1$ node, switch SA is closed

causing both the MOSCAPs C_1 and C_2 to come in series. This causes the voltages at $x2$ and $x3$ nodes to be same *i.e.* $V_{x2} = V_{x3} = V_x$. Therefore, total charge stored at V_x node is added up and given by

$$Q_x(\Phi_2) = V_B(C_1 + C_2) - C_1V_{inp} - C_2V_{inn} \tag{4.5}$$

Charge stored at V_x node at the end of amplification clock Φ_2 is given by

$$Q_x(\Phi_2) = C_1\left(V_x - V_{dacp}\right) + C_2(V_x - V_{x4}) \tag{4.6}$$

Following the charge conservation principle at V_x node and using equation (4.5) and equation (4.6) to solve for V_x gives

$$V_x = \frac{1}{(C_1+C_2)}\left(V_B(C_1 + C_2) - C_1V_{inp} - C_2V_{inn} + C_1V_{dacp} + C_2V_{x4}\right) \tag{4.7}$$

Furthermore, as charge is conserved at $x4$ node, therefore equating charges at V_x node during sampling and amplification phase and using Equation (4.7) gives

$$V_{x4} = -\left(V_{inp} - V_{inn}\right) + V_{dacp} \tag{4.8}$$

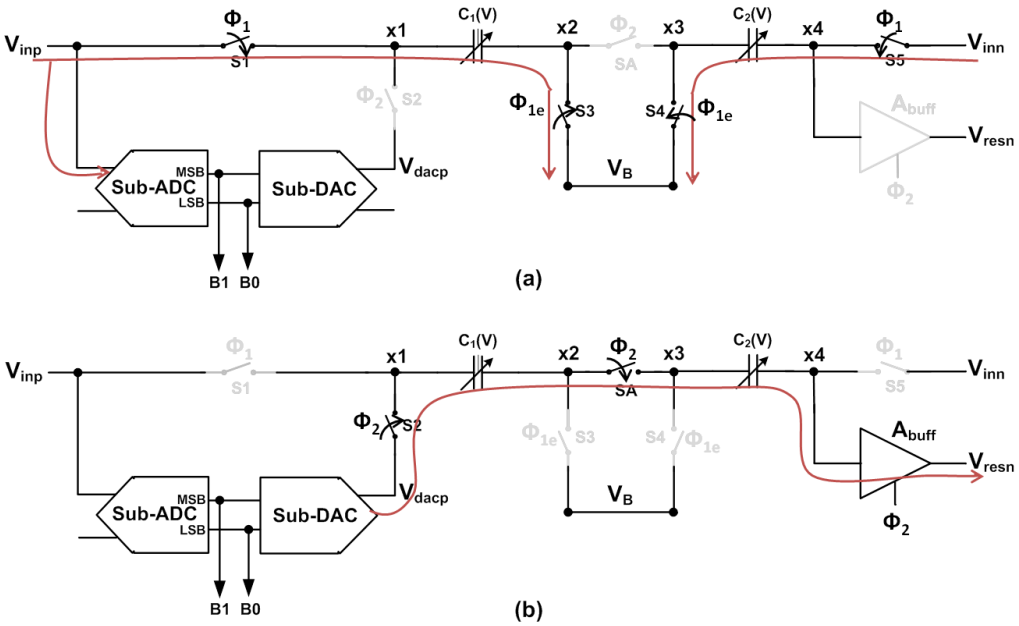


Figure 4.4. (a) sampling phase, $\Phi_1 = 1$ (b) amplification phase, $\Phi_2 = 1$

It is observed from the equation (4.8) that voltage developed at $x4$ node and therefore the residue voltage is insensitive to the capacitor mismatch *(i.e.* $C_1 \neq C_2$). This fact is confirmed by SPICE simulations also considering the mismatch between C_1 and C_2.

During $\Phi_2 = 1$, residue voltage generated at the output of the stage is given by

$$V_{resn} = A_{buff} V_{x4}$$

$$= A_{buff} \left(-\left(V_{inp} - V_{inn}\right) + V_{dacp}\right) \tag{4.9}$$

where A_{buff} is the voltage gain of unity gain buffer with ideal value of 1. It is also clear from the equation (4.9) that the present 1.5-bit stage is independent of common-mode variations. As a result, number of stages can be cascaded one after another in pipelined fashion without any amplification of common-mode voltage.

A similarly analysis can be followed for the lower branch in Figure 4.3 to generate the residue voltage which is given by

$$V_{resp} = A_{buff} \left(V_{inp} - V_{inn} + V_{dacn}\right) \tag{4.10}$$

Subtracting equation (4.9) from equation (4.10) for fully differential implementation gives

$$V_{resp} - V_{resn} = A_{buff} \left[\left(2(V_{inp} - V_{inn}) - (V_{dacp} - V_{dacn}\right)\right] \tag{4.11}$$

This can be written as

$$V_{res} = A_{buff} \left(2V_{in} - V_{dac}\right) \tag{4.12}$$

where $V_{res} = V_{resp} - V_{resn}$, $V_{in} = V_{inp} - V_{inn}$ and $V_{dac} = V_{dacp} - V_{dacn}$. From equation (4.12), assuming the ideal buffer with $A_{buff} = 1$, the required inter stage gain of 2 can be achieved using the technique presented here. Assuming the ideal buffers in the stage, equation (4.13) summarizes the transfer function of Figure 4.3 with V_{ref} as the reference voltage and is plotted in Figure 4.5

$$V_{res} = \begin{cases} 2V_{in} + V_{ref}\ ,\ V_{dac} = -V_{ref}\ if\ V_{in} < \frac{-V_{ref}}{4} \\ 2V_{in}\ ,\ V_{dac} = 0 \qquad\qquad if\ \frac{-V_{ref}}{4} \le V_{in} < \frac{V_{ref}}{4} \\ 2V_{in} - V_{ref}\ ,\ V_{dac} = V_{ref}\ if\ V_{in} \ge \frac{V_{ref}}{4} \end{cases} \tag{4.13}$$

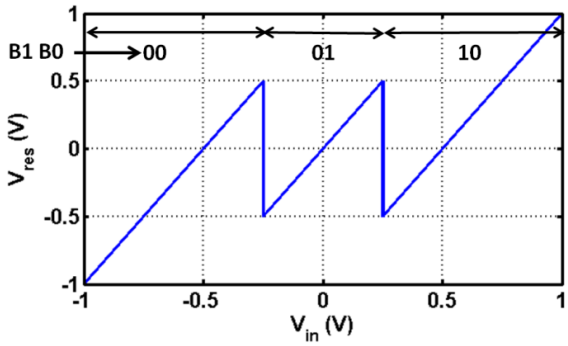


Figure 4.5. Output residue curve of the proposed stage

As MOSCAP variation in the strong inversion region is relatively independent of the voltage across it and from the analysis discussed in this section, it is clear that the residue voltage of proposed stage is independent of exact capacitance values (equation 4.12). Therefore, linear capacitors (used as the earlier work [30]) can be replaced by MOSCAP in Figure 4.3 and Figure 4.4 without any change in the analysis and stage characteristics.

To keep the p-channel MOSCAPs in strong inversion region for the whole signal range, its gate-to-bias potential difference V_{GB} should be negative (Figure 4.1(b)). This can be achieved with the help of an external bias potential V_B as shown in Figure 4.3.

4.3 Design and Optimization

Next, targeting a 10-bit, 100 MS/s pipelined ADC, design and optimization of various components of the proposed 1.5-bit/stage are discussed. Figure 4.6 shows the cascading of two fully differential implementation of MOSFET-only charge pump based 1.5-bit/stage architecture [70]. Fully differential input V_{in} $(= V_{inp} - V_{inn})$ is applied to both the sides of a stage.

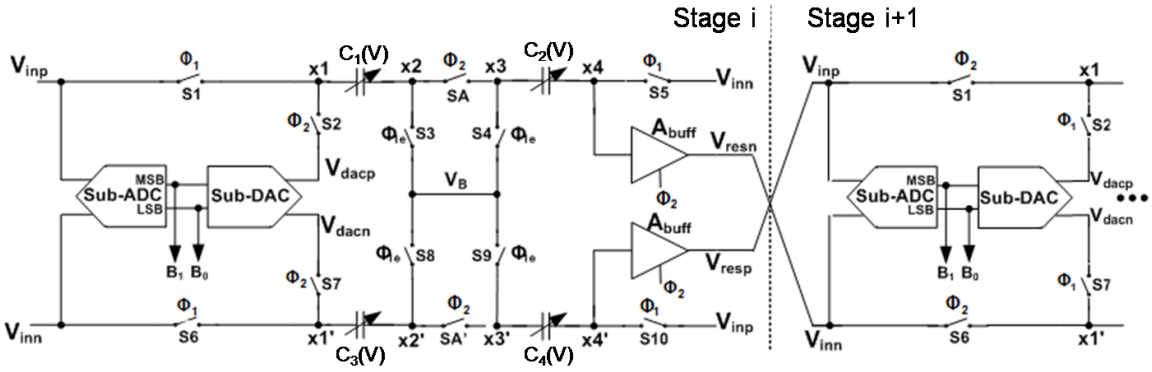


Figure 4.6. Cascading of fully differential charge pump based 1.5-bit/stage.

Considering the upper half (along V_B horizontally) in Figure 4.6 along with the parasitic capacitances formed at different nodes, it can be proved that the residue voltage of a stage i is given by [30]

$$V_{res} = A_{buff} \frac{1}{1+X}\left[(2+X)\left(V_{inp} - V_{inn}\right) - \left(V_{dacp} - V_{dacn}\right)\right] \tag{4.14}$$

where $V_{res} = V_{resp} - V_{resn}$, $X = \left(1+\frac{C_{px}}{C_1}\right)\left(1+\frac{C_{px\,4}}{C_2}\right) - \left(1-\frac{C_{px\,4}}{C_1}\right)$ which is a factor due to parasitic capacitances formed at various nodes and A_{buff} is the voltage gain of the buffer. Also, C_{px4} is the parasitic capacitance formed at $x4$ node and C_{px} is the parasitic capacitance formed at x node after the switch SA is closed. It is to be noted here that after switch SA is closed, nodes $x2$ and $x3$ are connected to each other and termed as a new node x here. During this period both the capacitors are connected in series causing the voltages at the nodes $x2$ and $x3$ to be same (*i.e.* $V_{x2} = V_{x3} = V_x$). Ideally the value of X is required to be zero with $A_{buff} = 1$. Considering these in equation (4.14) gives

$$\begin{aligned} V_{res} &= \left[2\left(V_{inp} - V_{inn}\right) - \left(V_{dacp} - V_{dacn}\right)\right] \\ &= 2V_{in} - V_{dac} \end{aligned} \tag{4.15}$$

where $V_{in} = V_{inp} - V_{inn}$ and $V_{dac} = V_{dacp} - V_{dacn}$.

From equation (4.14), there occur various non-idealities that impact the stage residue voltage. One is the parasitic capacitances formed at various nodes (lumped together as factor X) and another is the buffer gain (A_{buff}). Therefore, to achieve the desired inter stage gain of 2 it is important to minimize the effect of parasitic capacitances and maximize the buffer gain to approach unity.

4.3.1 Sampling Capacitance Value

In the conventional opamp based pipelined ADCs, sampling capacitances are decided by the noise and matching. However, in the proposed design values of sampling MOSCAPs ($C_1 - C_4$), are mainly decided by the sampling noise and speed considerations. For the sampling noise to have a negligible effect on the ADC's signal-to-noise ratio (SNR), $\frac{\mathrm{kT}}{\mathrm{C}}$ noise is chosen to be less than the quantization noise [71]. For only 1dB degradation in the value of ideal SNR, the required sampling capacitance is

$$C_i \geq \frac{48\ kT\,2^{2n}}{{V_{FS}}^2} \tag{4.16}$$

where n is the resolution of pipelined ADC, T is the temperature, k is the Boltzmann's constant and V_{FS} is the full scale range. By adjusting the W and L of MOSCAP as given in equation (4.1), the required value of C that satisfy the equation (4.16) can be obtained.

In order to reduce the effect of parasitic capacitances at various nodes it is required that $C_i \gg C_{pV_x}, C_{px4}$ such that factor X (in equation (4.14)) becomes small enough to have an impact on the output of pipelined ADC. This can be achieved by choosing the large MOACAPs values, and optimized designing and layout of the switches used in the design to reduce the various parasitic capacitances. For relatively large value of C_i, the ratio of parasitic capacitance to C_i and therefore factor X (in equation (1)) becomes small enough to have an impact on V_{res}. This also significantly reduces the common-mode error at the output of the stage [30].

However, the large MOSCAP value increases the RC time constant that is formed due to ON resistance of the switch and MOSCAP and decreases the speed of the stage. Therefore various switches shown the Figure 4.6 (and 4.3 and 4.4) are implemented by CMOS transmission gate to reduce the ON resistance and SPICE simulations are used to optimize them.

4.3.2 Output Buffer

Another important parameter in equation (4.14) that effects the residue voltage is the gain of buffer A_{buff}. In earlier work [30], CMOS source follower is used as a buffer that consumes less power but suffers from low output swing. Since SNR is the ratio of signal power to noise power, it is important to maximize the signal swing and minimize the noise to achieve a high SNR value. Noise level at the output node of an amplifier consists of the amplifier noise and the sampling noise with the later being the dominated one. The sampling noise power is given by

$$\overline{v_n{}^2} = \frac{kT}{C_L} \tag{4.17}$$

Therefore signal to noise ratio (SNR) is given by

$$SNR = \frac{C_L V_P^2}{2kT} \tag{4.18}$$

where C_L is the load capacitance at the output node of the buffer and V_P is the signal amplitude. It shows that for the same load capacitance, SNR increases with the increase in

signal amplitude V_P. Also for the same SNR, increasing the signal range decreases the load capacitance value C_L which in turn reduces the current requirement for the same speed. Therefore, it is always beneficial to maximize the output voltage swing unless nonlinearity comes in the picture. The increased swing increases the circuit's immunity towards noise and relaxes the comparator design specifications in sub-ADC, further saving the power.

Low-power consumption without hitting the performance is one of the design objectives in a pipelined ADC. Since power, area and speed are the main tradeoffs in a CMOS circuit a design, the relation between SNR, speed and power quantify the ADC performance and is given by

$$\frac{SNR \cdot Speed}{Power} = \frac{\frac{V_P^2}{\frac{kT}{C_L}} \cdot \frac{g_m}{C_L}}{I_s \cdot V_{DD}}$$

$$\alpha \frac{V_P^2}{V_{DD}} \tag{4.19}$$

where $g_m \alpha I_s$ is considered.

From equation (4.19) it can be observed that for a given technology (hence fixed V_{DD}), higher SNR and low power can be achieved by maximizing the voltage swing of amplifier. Also while scaling down the technology; supply voltage V_{DD} is also scaled down which in turn reduces the signal swing. Therefore in order to maintain the same SNR, thermal noise must also be reduced proportionally. This requires increase in the sampling capacitance value (C_L) that in turn increases the area and power consumption to compensate the degradation in speed.

The amplifier used at the output of the stage in the ADC determines the speed, power and noise. The non-linearity that comes at the output of the ADC can be lessened by maximizing the output signal swing of the amplifier by trade-off its open-loop gain. It increases the dynamic range (DR), SNR, reduces the $\frac{kT}{C}$ noise and power dissipation.

Figure 4.7(a) shows a differential amplifier in negative feedback configuration is one such implementation with low power and low area. This results in a single-pole system that requires no compensation, and thus maximizes the speed and stability. An extra MOS transistor M6 is used in the differential amplifier which activates it during amplification

phase and save the power. And simulations results confirm the reductions in power dissipation upto 50% in one clock cycle.

For a differential amplifier in unity gain configuration (feedback factor, β=1), its closed loop gain is given by

$$A_{cl} = \frac{A_0}{1+A_0} \tag{4.20}$$

$$A_{cl} \simeq 1 \cdot \left(1 - \frac{1}{A_0}\right) \tag{4.21}$$

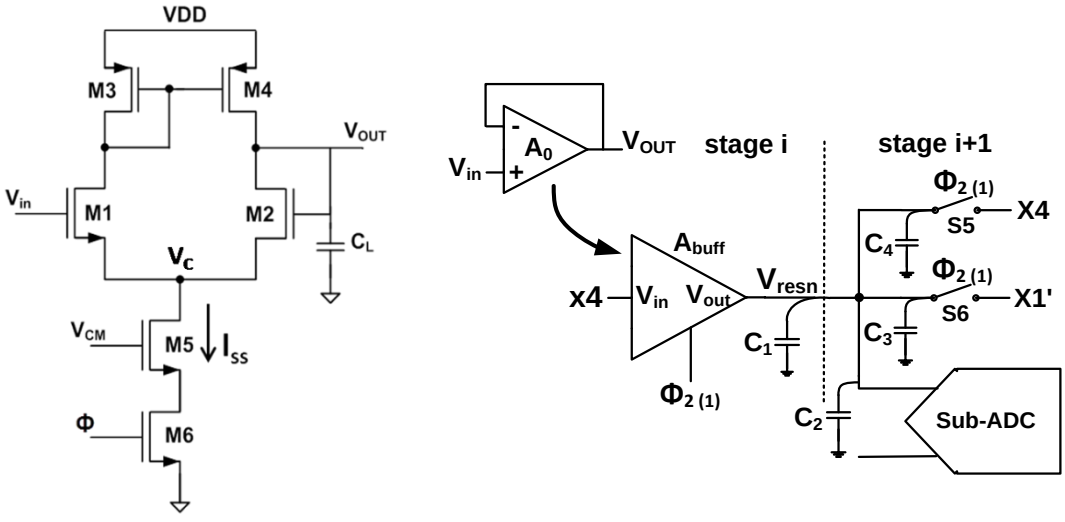
This is the actual gain of buffer A_{buff} shown in Figure 4.3 and Figure 4.6 with A_0 as its open loop gain.

Using equation (4.21), equation (4.12) can be written as

$$V_{res} = 1 \cdot \left(1 - \frac{1}{A_0}\right)(2V_{in} - V_{dac}) \tag{4.22}$$

with $1/A_0$ as the gain error limiting the accuracy of the stage and ADC. Gain error can be minimized by increasing the open loop gain A_0 which in turn increases the power and area. Another way to minimize the gain error is using the digital calibration techniques by using digital output of the ADC. This is a preferable choice in current deep submicron technologies due to scaling benefits.

In a 10-bit pipelined ADC, for the gain error to be less than half LSB, minimum



(a) (b)

Figure 4.7. (a) Differential amplifier as unity gain buffer (b) various parasitic capacitances loading the stage output node

required open loop gain of differential amplifier in 1st stage is 512. Therefore, in comparison to the traditional opamp based designs with β=0.5, power requirement in the present work is less for the same error budget.

Another requirement of differential amplifier is to properly settle to certain accuracy during amplification phase to avoid any settling error. It requires a large bandwidth of differential amplifier with its unity-gain frequency given by

$$UGB = \frac{g_{mi}}{C_L} \tag{4.23}$$

where g_{mi} is the transconductance of the M1 and M2 MOS transistors, and C_L is the load capacitance of the buffer at the output node as shown in Figure 4.7(b). C_L mainly consists diffusion capacitance at the output node of the buffer (C_1), sampling capacitors and input capacitance of sub-ADC C_2) of the next stage

Incorporating the finite gain and finite bandwidth affects on stage output, equation (4.22) is modified to (assuming identical buffers)

$$V_{res} = 1 \cdot \left(1 - \frac{1}{A_0}\right)(1 - e^{-t \cdot UGB})(2V_{in} - V_{dac}) \tag{4.24}$$

Maximum time available for amplification phase is 5ns in a 100 MS/s pipelined ADC. The differential amplifier in first stage requires a minimum bandwidth of 220.6 MHz in order to have the settling error to less than half LSB which can be obtained easily. It is to be noted that in a traditional opamp based pipelined ADC, β becomes less than half while considering the gate capacitance of the opamp. However, in the present research work since β=1, therefore power requirement is less in comparison to opamp based designs for the same UGB.

It is observed from the equation (4.14) that C_{px4} has larger impact on the stage output than the other parasitic capacitances. C_{px4} mainly consist of the input capacitance of the buffer, therefore sizes of M1 and M2 MOS transistors in the buffer are kept small trading-off mainly with its gain. While designing the buffer, it is also important to maximize its ICMR so that whole signal range of the pipelined ADC lies within the ICMR while keeping all the MOSCAPs in strong inversion region.

Figure 4.8 shows the variation of the open loop gain and UGB with the tail current (I_{ss}) of the differential amplifier. Open loop gain can be increased by increasing the current

I_{ss} and sizes of the input MOS transistors M1 and M2 [72]. However, this increases the power dissipation and reduces the signal swing [73-74]. However, from equation (4.18), for the same SNR, reduction in signal range increases the capacitance value that degrades the speed and requires further power to be invested to increase the speed.

Key design considerations while designing the differential amplifier are low area-power, high dynamic range and high SNR along with the design simplicity. A CMOS differential amplifier is designed accordingly that has an open loop gain of 30.01 dB (≅ 32 V/V), PM of 77º and UGB of 457 MHz with a total current of 320 µA. This much of UGB is sufficient for the settling accuracy of 10-bit at 100 MS/s. It gives a inter stage gain of 1.94 ($2(1-1/A_0)$) with a relative gain error of 3%.

Variation in output voltage of differential amplifier has an impact on its current which introduces the nonlinearity at the ADC output. Therefore, length of MOS transistor M5 is chosen appropriately larger than minimum to minimize the effect. The simulation results of the CMOS differential amplifier as a unity gain buffer are shown in Figure 4.9. Figure 4.9(a) shows the change in V_{out} with change in input common mode voltage (V_{CM}) with the linear region and nonlinear region at the top end. Nonlinearity occurs due to the fact that as V_{out} increases, V_{SD} of M4 transistor decreases and it enters linear region from saturation. Figure 4.9(b) shows the 1024 points FFT response with a sinusoidal signal of 1 Vpp single ended at 10 MHz is applied to unity gain differential amplifier. It shows 2nd, 3rd harmonics of the amplitude below 75dB.

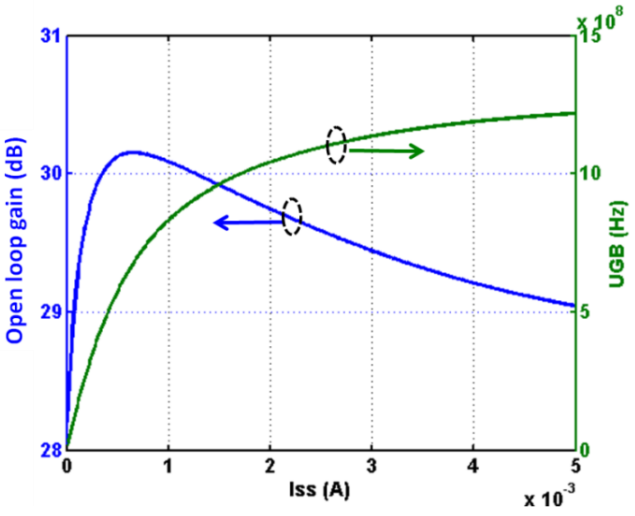
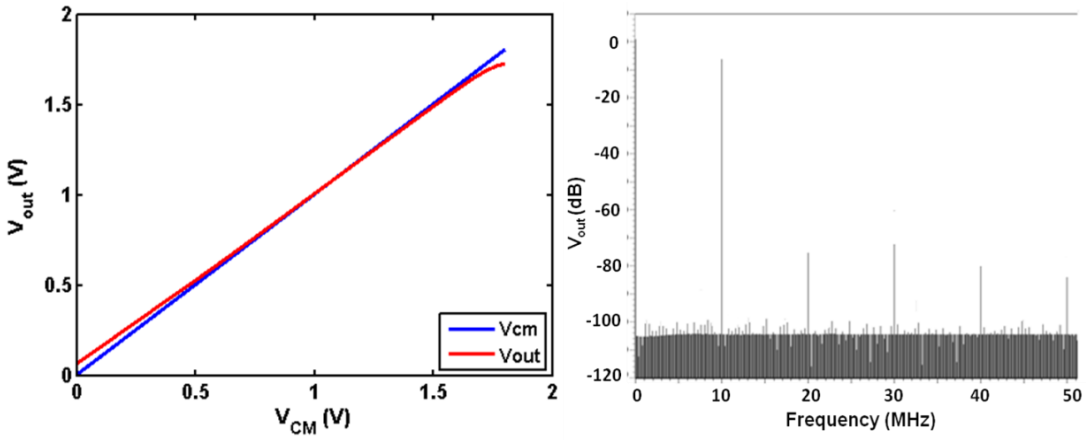
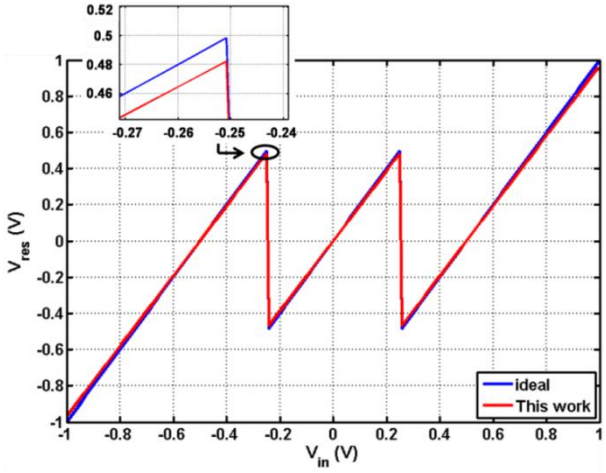


Figure 4.8. Open loop gain and UGB of differential amplifier vs. I_{ss}.

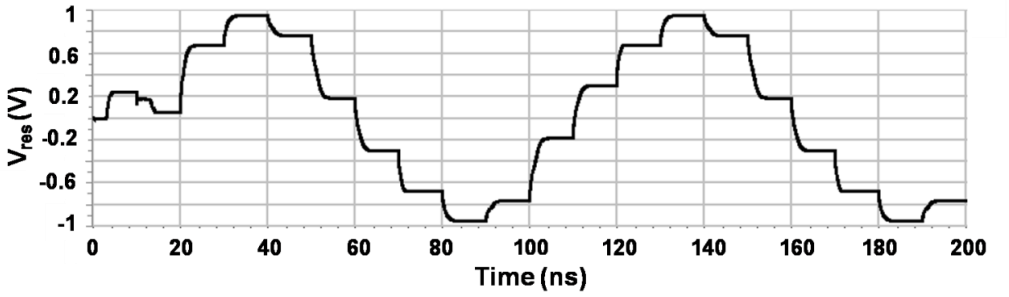


(a) (b)

Figure 4.9. Differential amplifier in unity gain configuration (a) transfer characteristic (b) FFT response



(a)



(b)

Figure 4.10. Simulated stage results (a) residue curve (b) transient response

Simulation results of the proposed 1.5-bit MOSFET-only stage are shown in Figure 4.10. Figure 4.10(a) shows its voltage residue curve when slow ramp is given and Figure

4.10(b) shows the transient response when sampled (at 100 MHz) sinusoidal signal of 1 Vpp single ended is given. Results clearly show that there occurs only gain error in the proposed stage.

Table 4.2 shows the comparison of some of earlier power efficient designs with the proposed one. For the same voltage supply the full scale signal swing of 2 Vp-p differential is achieved in the present work which is wider than the other designs. This may result in higher SNR after completing the pipelined ADC design. Hence, relaxes the comparator design requirements in sub-ADC by increasing the tolerance of comparators towards offset. Also, proposed ADC stage is designed using standard digital CMOS technology which is cheaper than Mixed-Mode process and therefore reduces the overall manufacturing cost of SoC.

Table 4.2. Performance comparison of an ADC stage

Parameters	**[18]**	**[19]**	**[61]**	**[30]**	**[62]**	**This work**
Technology (µm)	0.35	0.35	0.18	0.18	0.09	0.18
Supply (V)	3	3	1.8	1.8	1	1.8
CMOS Process	double-poly M4		deep n-well		-	std. digital
Sampling Rate (MHz)	75	75	800*	50	100	100
Full scale swing (Vpp differential)	2	2	0.4	1	0.04	2
Errors in stage	linear gain error, non-linearity	linear gain error, non-linearity	linear gain error, non-linearity	linear gain error	linear gain error	Linear gain error

* used interleaving

Proposed stage is fully differential in nature and thus able to reject the common-mode and substrate noise.

Furthermore, from Table 4.2 it is clear that most of the non-idealities that occur in the ADC are eliminated in the present work except small gain error as compared to the traditional opamp based and other designs which suffers from the non-linearity gain-error, and capacitor mismatch errors.

4.4 Noise Analysis

Figure 4.11 show the noise equivalent circuit of the proposed MOSFET-only pipelined ADC stage in the sampling and amplifications phase. Here conducting CMOS switches are replaced by the ON resistance R_{on} and equivalent noise voltage V_{ns}. Its power spectral density is given by $\overline{v_{ns}^2} = 4kTR_{on}$ in V^2/Hz.

Consider the single ended input V_{inp} applied to the stage with negligible parasitic capacitance of CMOS switches. During the sampling phase, $\Phi_1 = 1$ as shown in Figure 4.11(a), noise along with the input V_{inp} is sampled by MOSCAPs C_1 and C_4 [75]. Sampled noise is given by

$$\overline{v_{n(\Phi_1)}^2} = \frac{kT}{C_1 + C_4} \tag{4.25}$$

Figure 4.11(b) shows the amplification phase, $\Phi_2 = 1$. During this phase MOSCAPs come in series and buffers is activated and generates the noise with the input referred noise of buffer given by $\overline{v_{nbuff}^2} = \frac{16}{3}\frac{kT}{g_{mi}}\left(1 + \frac{g_{m3}}{g_{mi}}\right)$.

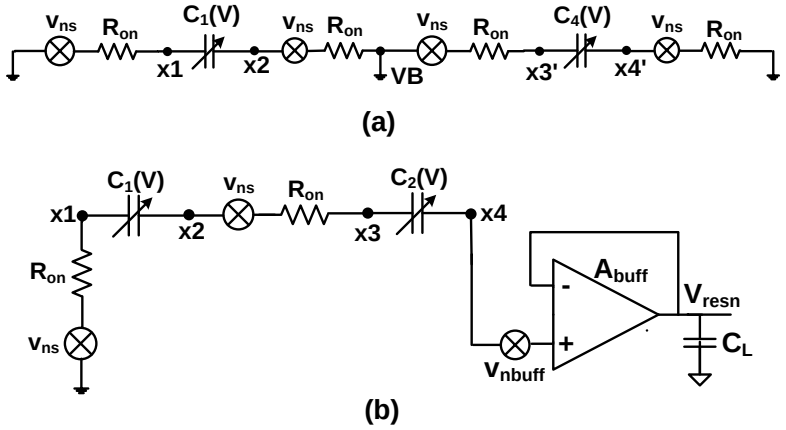


Figure 4.11. Noise equivalent circuit during (a) sampling phase (b) amplification phase.

Transfer function of the buffer (with bandwidth $BW = \frac{g_{mi}}{C_L}$) will modulate the total noise generated at the output [76] and given by

$$\overline{v_{n(\Phi_2)}^2} = \left(2 \cdot \overline{v_{ns}^2}. + \overline{v_{nbuff}^2}\right)\frac{BW}{4}$$

$$= 2kTR_{on}\frac{g_{mi}}{C_L} + \frac{4}{3}\frac{kT}{C_L}\left(1 + \frac{g_{m3}}{g_{mi}}\right) \tag{4.26}$$

where g_{mi} is the transconductance of input MOS transistors ($g_{mi} = g_{m1} = g_{m2}$) and g_{m3} is the transconductance of load transistor M3 ($g_{m3} = g_{m4}$) of differential amplifier.

Total noise when referred to single ended input (V_{inp}) is given by [30]

$$\overline{v_{in,stage}^2} = \frac{kT}{2C} + \frac{1}{A^2}\left(2kTR_{on}\frac{g_{mi}}{C_L} + \frac{4}{3}\frac{kT}{C_L}\left(1 + \frac{g_{m3}}{g_{mi}}\right)\right) \quad (4.27)$$

where A is the inter stage gain with $C = C_1 = C_4$. Total noise when referred to the input of fully differential stage is two times the noise given by equation (4.27).

For the complete fully differential 10-bit pipelined ADC, total input referred noise is given by

$$\overline{v_{in,ADC}^2} = 2 \cdot \overline{v_{in,stage}^2} \cdot \sum_{n=0}^{9}\left(\frac{1}{A^2}\right)^n \quad (4.28)$$

4.5 Summary

An opamp-less fully differential MOSFET-only 1.5-bit pipelined ADC stage is presented in TSMC 0.18µm digital CMOS technology with power supply of 1.8 V. It uses the charge pump technique to achieve the inter stage gain of 2. In the present research work, MOSCAPs are used in place of MIMCAPs to reduce the manufacturing cost and Silicon area. Proposed stage is independent of MOSCAP mismatch and avoids the use of power hungry opamps thus reduces the power consumption and Silicon area. Various blocks of the proposed stage have been designed with emphasis on low power, low area and high signal swing. Comparison of proposed stage with the earlier power efficient designs has also been discussed. At the end, noise analysis of the proposed stage is carried out.

Chapter 5

Complete Pipelined ADC

5.1 Introduction

From equation (4.14), the parasitic capacitances formed at various nodes modify the stage gain from 2 and the Sub-DAC output voltage subtracted at the stage output, and results in the missing codes at the ADC as shown in Figure 5.1. It shows that the effect of parasitic capacitances is similar to that of gain error with missing codes at the ADC output.

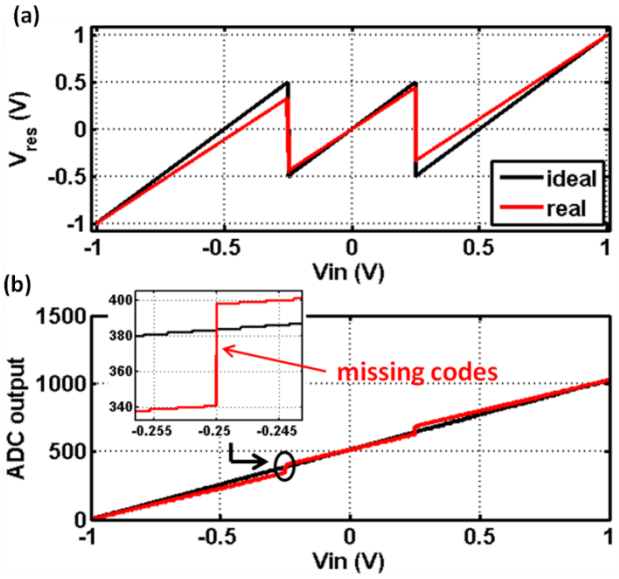


Figure 5.1. (a) Stage transfer characteristics with effect of parasitic capacitances (b) impact on 10-bit ADC characteristics with V_{ref} =1V.

From equation (4.14) it can be observed that in order to reduce the effect of parasitic capacitances at various nodes it is required that $C_i \gg C_{pV_x}, C_{px4}$ such that factor X becomes small enough to have an impact on ADC output.

Also as discussed in section 4.3.2, due to low DC gain of differential amplifier there occurs gain error and cause missing codes at the ADC output. The effect of low open loop gain on 1st stage residue characteristic and its impact on 10-bit ADC characteristic is shown in Figure 5.2 depicting the missing codes at the ADC output. These missing codes can be corrected by using a digital calibration technique. This is a preferable choice in today's deep

submicron technologies without a significant increase in area and power [18, 30, 55] and is discussed in Section 5.2.

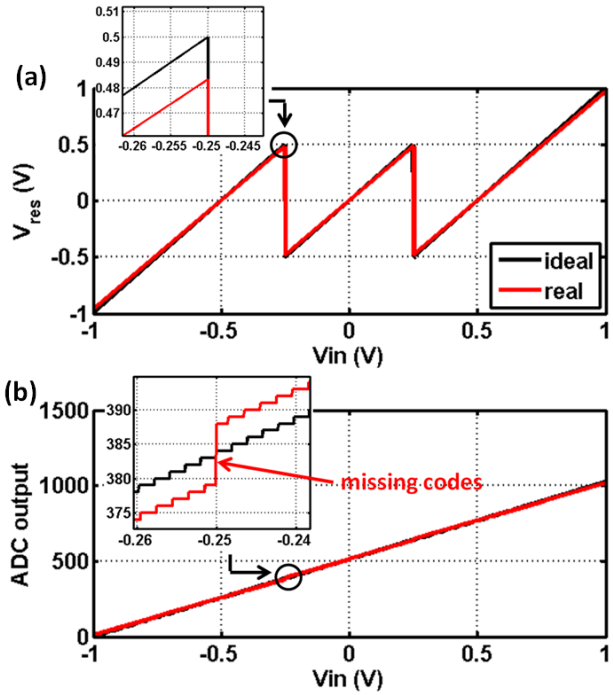


Figure 5.2. Effect of low open loop gain on (a) 1st stage characteristics (b) 10-bit ADC output characteristics

5.2 Digital Background Calibration

In earlier work [30], a charge pump based technique followed by a source follower that reduces the inter stage gain and introduces the gain error. It uses a digital foreground calibration to compensate the missing codes due to the gain error. However, it interrupts the normal ADC conversion cycle and is unable to track the temperature and voltage variations during normal ADC conversion cycle. In the present work, instead of a source follower, a differential amplifier in unity-gain feedback configuration is used, targeting high swing and high speed, and trading gain to save the power. Low open loop gain of the differential amplifier results in missing codes at the ADC output that are compensated by using a digital background calibration technique. It does not interrupt the normal ADC conversions and continuously tracks the temperature and voltage variations.

Taking the benefit of technology scaling, digital calibration is generally used to calibrate the various non-idealities occurring in a pipelined ADC [77-81]. In the earlier charge pump

based work [30], digital foreground calibration is used in which normal operation of the ADC is interrupted. However in the present work, digital background calibration is used to correct the gain error [82]. It works continuously in the background without interrupting the normal operation of the ADC conversion cycle.

Equation (4.21) can be written as

$$V_{in} = \frac{1}{2} V_{dac} + \frac{V_{res}}{2\left(1-\frac{1}{A_0}\right)} \tag{5.1}$$

Digital equivalent of equation (5.1) can be written as

$$D_{in} = \frac{1}{2} D + \frac{D_{res}}{2\left(1-\frac{1}{A_0}\right)} \tag{5.2}$$

where $D \in (-1, 0, 1)$, D_{in} and D_{res} are the digital equivalent of the input and the output of a stage respectively. Consider a three stage pipelined ADC as shown in Figure 5.3, using equation (5.2), it can be written that

$$D_{in,1} = \frac{1}{2} D_1 + \frac{D_{res,1}}{2\left(1-\frac{1}{A_{01}}\right)} \tag{5.3}$$

$$D_{in,2} = \frac{1}{2} D_2 + \frac{D_{res,2}}{2\left(1-\frac{1}{A_{02}}\right)} \tag{5.4}$$

$$D_{in,3} = \frac{1}{2} D_3 + \frac{D_{res,3}}{2\left(1-\frac{1}{A_{03}}\right)} \tag{5.5}$$

Since $D_{in,i+1} = D_{res,i}$ above equations results in

$$D_{in,1} = \frac{1}{2}\left[D_1 + \frac{1}{2\cdot\left(1-\frac{1}{A_{01}}\right)}\left(D_2 + \frac{1}{2\cdot\left(1-\frac{1}{A_{02}}\right)}\left(D_3 + \frac{D_{res,3}}{2\cdot\left(1-\frac{1}{A_{03}}\right)}\right)\right)\right] \tag{5.6}$$

$$D_{in,1} = \frac{1}{2}\left[D_1 + w_1(D_2 + w_2 D_3)\right] \tag{5.7}$$

where w_i the weight of the stage with the residue of the last stage discarded and is given by

$$w_i = \frac{1}{2\cdot\left(1-\frac{1}{A_{0i}}\right)}$$

To demonstrate the approach, an input voltage of V_{in}= -1V is applied to 3-bit pipelined ADC shown in Figure 5.3. Applied input voltage is fully differential in nature. Residue voltage of each stage with digital output is $V_{res,1} = -1$ V, $V_{res,2} = -1$ V, D_1= -1, D_2= -1 and D_3= -1. Applying equation (5.7) with ideal weigths (w_i=0.5) gives $D_{in,1}$= -0.875 V which is equal to applied voltage with some quantization error. For 3-bit ADC quantization error is ±0.125 V. Similarly for other applied input voltages, equation (5.7) can

be applied. Table 5.1 shows the results for other input voltages, considering all the stages ideal in Figure 5.3. Thus a basic of calibration is to find the weights (w_i) such that the equivalent of the applied input voltage is retrieved at the output in digital form.

Table 5.1. Results for different applied input voltages in Figure 5.3

V_{in} (V)	$V_{res,1}$ (V)	$V_{res,2}$ (V)	D_1	D_2	D_3	D_{out} (V)=$D_{in,1}$
1	1	1	1	1	1	0.875
-0.6	-0.2	-0.4	-1	0	-1	-0.625
-0.4	0.2	0.4	-1	0	1	-0.375
0.3	-0.4	0.2	1	-1	0	0.25
0.6	0.2	0.4	1	0	1	0.625

Equation (5.7) can be extended to N number of stages as

$$D_{in,1} = \frac{1}{2}[D_1 + w_1(D_2 + w_2(D_3 + \cdots + w_{N-1}D_N))] \tag{5.8}$$

A visual representation of equation (5.8) for N=10 with D_{out} $(= D_{in,1})$ is shown in Figure 5.4. Therefore, digital equivalent of the applied analog input can be obtained by beginning from least significant stage and moving towards the first stage. Equation (5.8) forms the basis

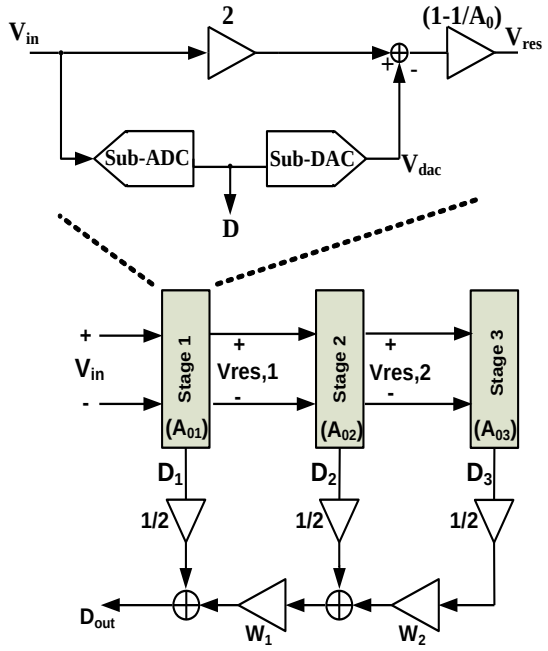


Figure 5.3. Cascading of 3 stages in a pipelined ADC.

of digital calibration algorithm for whole ADC.

Figure 5.4 shows the complete pipelined ADC architecture with the calibration logic. From chapter 4, achieved DC gain of differential amplifier is A_0=30.01 dB ≈32 V/V. Gain of a stage is therefore $2(1-1/A_0)$=1.9375. For 10-bit linearity total number of bits required is $\log_{1.9375} 2^{10} = 11$-bits. Therefore, it requires 9 MOSFET-only charge pump based stages with a 2-bit flash ADC at the end.

Calibration begins from the least significant stage and moves towards the most significant stage. After the stage i is calibrated, calibration of stage i-1 is carried out and so on until the most significant stage (stage 1) is reached. In ideal ADC $w_i = 0.5$ whereas in case of real ADC w_i is different from 0.5 and is derived from the calibration algorithm to find out the digital equivalent of the input.

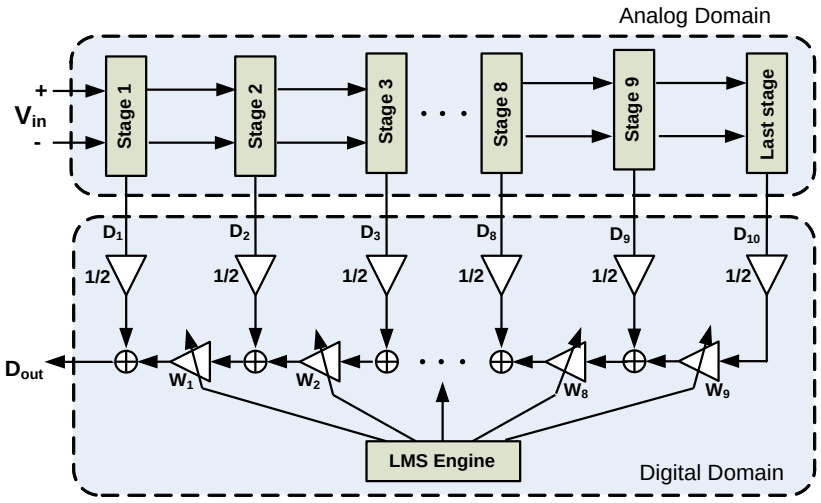


Figure 5.4. Complete 10-bit pipelined ADC architecture.

Figure 5.5 shows the complete calibration logic used in this work. Accuracy of weights w_i calculated through calibration process depends upon the resolution of the residue that is converted to the digital equivalent by the following stages. Therefore, to get the accurate digital representation of V_{resi}, extra two stages are added at the end. These extra stages are considered to be accurate therefore do not undergo calibration and are activated only during the calibration cycle to initiate the calibration process.

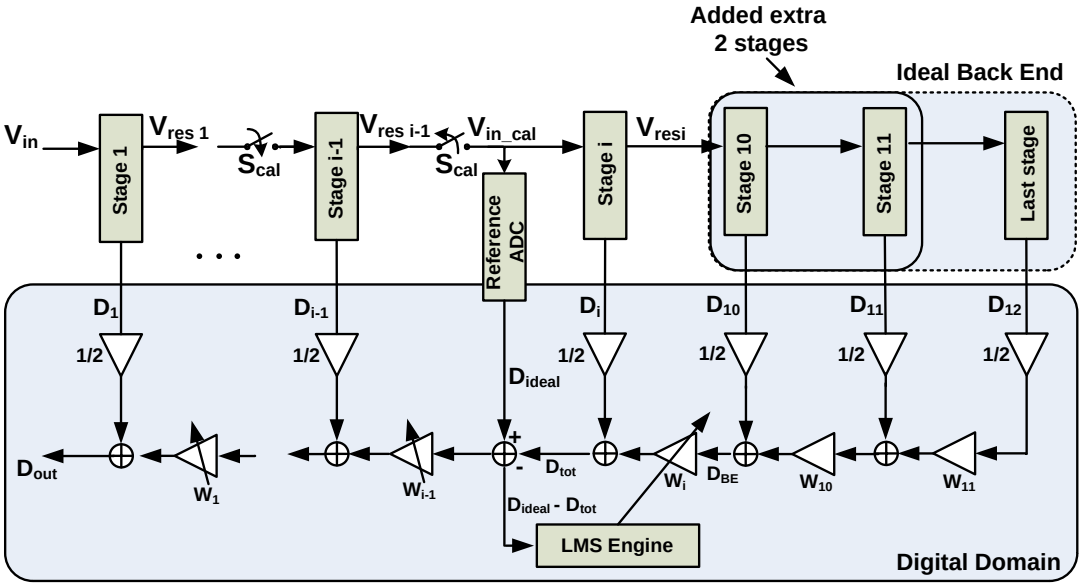


Figure 5.5. Calibration logic (ADC analog signal path is fully differential) [82]

Adding extra stages adds little to the area and power overhead. This forms the ideal low resolution ADC with V_{resi} as its input and termed as ideal backend ADC as shown in Figure 5.5 with D_{BE} as the digital reprenstation of V_{resi} plus the quantization noise of ideal back ADC. The digital output of back end ADC can be written as

$$D_{BE} = \frac{1}{2}(D_{10} + W_{10}(D_{11} + W_{11}D_{12})) \tag{5.9}$$

Figure 5.5 show that the calibration of stage i (stage 9 here) begins by applying a predefined DC input (V_{in_cal}) to it and to a reference ADC which is a high resolution and slow speed ADC [55, 83] used to generate D_{ideal}. With V_{in_cal} stage i produces D_i, backend ADC produces D_{BE} which is digital representation of residue voltage under calibration and the reference ADC generates D_{ideal} which is used to compare D_{tot} coming from back end ADC. Considering the stage i as a stage under calibration, from Figure 5.5 it can be written that

$$D_{tot} = \frac{1}{2}D_i + w_i D_{BE} \tag{5.10}$$

where w_i is the weight of the ith stage with ideal value of 0.5. In case of non-ideal stage, the weight of the stage i can be found by using an adaptation algorithm such as least-mean-square (LMS) algorithm [84-86]. As given in equation (5.10) D_{BE} is multiplied by a weight w_i and added with D_i to produce D_{tot} which in ideal case must be equal to D_{ideal}. In case of non-

ideality in stage i, $D_{ideal} - D_{tot}$ gives an error value that must be minimized. For that purpose a adaptation algorithm such as LMS algorithm is used that adjust the weight such that mean square of $D_{ideal} - D_{tot}$ is driven to zero according to

$$w_i(n+1) = w_i(n) + \mu(D_{ideal} - D_{tot})D_{BE} \tag{5.11}$$

where μ is the update adaptation parameter that controls the convergence of adaptation algorithm. Increasing the value of μ reduces the time to reach the convergence but increases the variation around the converged value in the steady state whereas the lower value of μ increases the convergence time and therefore the calibration time. After finding the optimized weight w_i, D_{tot} is treated as the new D_{BE} and the reference ADC is switched to the input of stage $(i-1)$ and same updating process (equation (5.9) to equation (5.11)) is followed using the LMS algorithm.

The calibration algorithm initiates in foreground mode and subsequently moves to the background mode. The foreground calibration is carried out at the startup of ADC, once the weights w_i of different stages are calculated and stored, it switches to background mode during the normal ADC conversion. It keeps tracking the gain variation due to change in temperature or other factors. In this work, the pipelined ADC operates at a sampling rate of 100 MS/s while the calibration is performed at the speed of Reference ADC (a slow but accurate ADC) working at 3.125 MS/s. In this way, it samples 1 out of every 32 input samples and performs the calibration. On successive calibration cycles, the calibration algorithm works in background without interrupting the normal ADC conversions. This fastens the calibration process as calibration algorithm only checks and updates the changes in weights calculated earlier. The complete pipelined ADC implemented fully differentially hence rejects the common-mode and substrate noise.

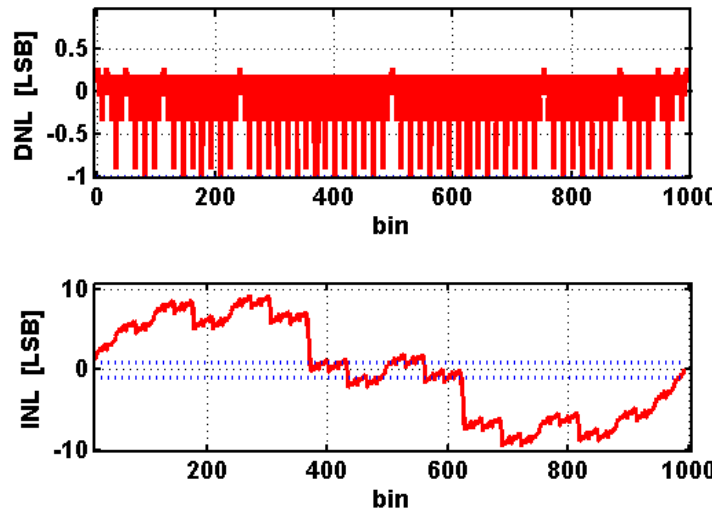
5.3 Simulation Results

Based on the design and optimization process described in section 2 and 3, the analog part of the pipelined ADC is designed and simulated in SPICE using the TSMC 0.18 µm CMOS process operating on a 1.8 V power supply voltage. Its calibration part is developed using MATLAB.

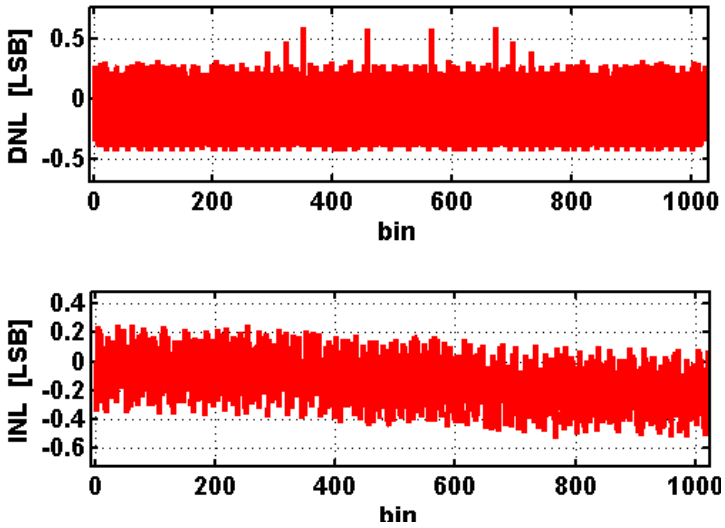
In order to show the ability of calibration algorithm, same stages are used with linear

gain error in all the 9 stages. Calibration algorithm is applied in all the 9 stages. Power consumption of complete ADC (excluding that of calibration part) is 16.53 mW.

Figure 5.6 shows the DNL and INL curves for the both un-calibrated and calibrated 10-bit pipelined ADC. After calibration, DNL improves to +0.6/-0.4 LSB and INL improves from+9.3/-9.6 LSB to within ± 0.5 LSB, thus illustrating the effectiveness of the calibration in the charge pump based pipelined ADC.



(a)



(b)

Figure 5.6. DNL and INL response of ADC (a) uncalibrated (b) calibrated.

Figure 5.7 shows the uncalibrated and calibrated ADC's digital output. Before calibration there is a large number of missing codes which are compensated by the calibration

technique. Figure 5.8 shows the dynamic response of 10-bit 100 MS/s pipelined ADC. For input frequency of 13.965 MHz, FFT response (1024 points) shows that after calibration SNDR and SFDR improves by about 27 dB and 39 dB respectively with spurious components below -79 dB.

Figure 5.9 shows the variations of SNDR and SFDR versus input frequency varied over Nyquist band for a 10-bit pipelined ADC running at 100 MS/s. It is evident that after calibration both SNDR and SFDR improve significantly with ENOB of 10.3 bits.

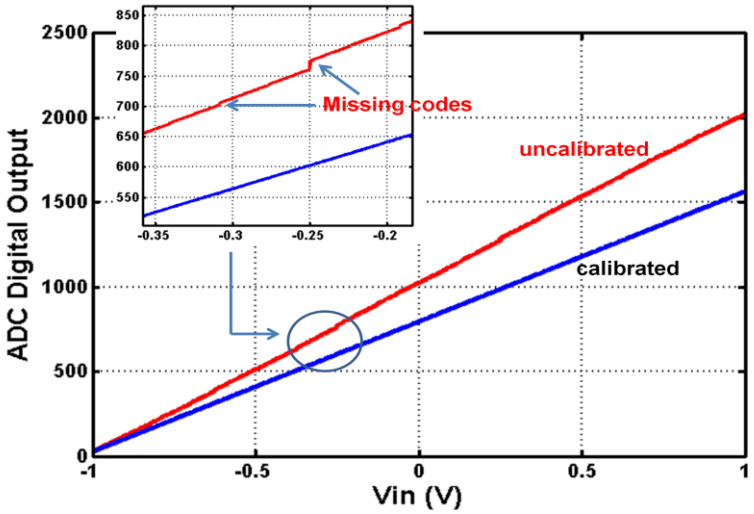


Figure 5.7. Uncalibrated and calibrated ADC characteristic

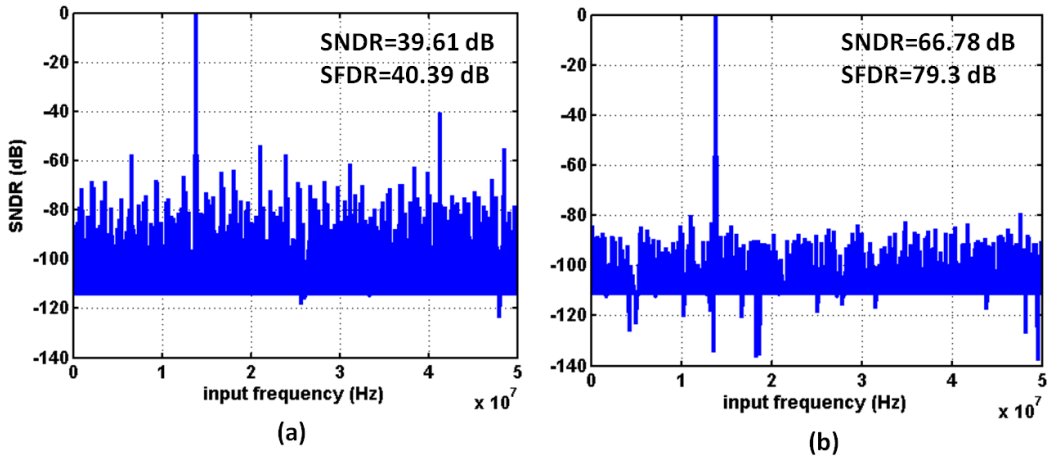


Figure 5.8. FFT response of (a) uncalibrated (b) calibrated ADC.

Table 5.2 shows the performance results of present work with some of the earlier published work using digital calibration techniques. From Table 5.2, it is clear that this work

has the smallest power consumption for the same sampling rate and achieves a good DNL and INL after calibration. The SFDR and SNDR of this calibrated 10-bit pipelined ADC

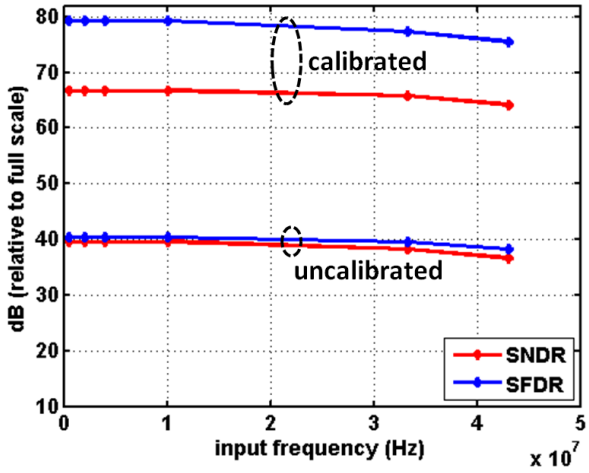


Figure 5.9. SNDR/SFDR versus input frequency.

Table 5.2. Performance summary and comparison

Parameters		Liren [77]	Ahmed [30]	Kexu [80]	Yuan [81]	Aminzadeh [66]	This work
Supply (V)		1.8	1.8	3.3	3.3	1.8	1.8
Technology (µm)		0.18	0.18	-	0.35	0.18	0.18
Resolution (bits)		12	10	14	12	12	10
Sampling Rate (MS/s)		100	50	100	20	65	100
Voltage Swing (Vpp)		-	1		2	-	2
Type of digital calibration		Back-ground	Fore-ground	Foreground & Background	Back-ground	-	Back-ground
DNL (LSB)	bc	-	+1.6/-1	-	1.47	1.26	+0.24/-1
	ac	+0.1/-0.08	+0.35/-0.35	-	0.27	1	+0.6/-0.4
INL (LSB)	bc	1.9	+15.7/-17.9	-	7.85	57.59	+9.3/-9.6
	ac	+0.4/−0.6	+0.7/-0.8	-	0.2	0.67	± 0.5
SNDR (dB): bc/ac		-/66	33.9/58.2	-	41.3/72.5	43/70	39.61/66.8
SFDR (dB): bc/ac		66/82	38/66	57.9/102	52.5/84.4	44 /78	40.39/79.3
ENOB (bits)		-	9.4	12.6	11.8	-	10.3
Power (mW)		205	9.9	-	56.3	-	16.53

bc: before calibration; ac: after calibration

approach the values of some of the 12-bit designs. Compared to earlier work [30] power consumption in the present research high is more because of higher sampling rate.

5.4 Summary

A 10-bit 100 MS/s pipelined ADC is designed using the proposed MOSFET-only 1.5-bit stage in TSMC 0.18 µm digital CMOS technology operating on a 1.8 V supply voltage. Stage suffers from only gain error and results in missing codes at the ADC output. A digital background calibration technique is used to calibrate the gain error. Before calibration SNDR and SFDR of the pipelined ADC is 39.61 dB and 40.39 dB respectively which increase to 66.78 dB and 79.3 dB after calibration. Also DNL improves to +0.6/-0.4 LSB and INL improves from +9.3/-9.6 LSB to within ± 0.5 LSB. Total power consumption of the ADC is 16.53 mW.

Chapter 6

Design Methodology and Tradeoffs

6.1 Introduction

The designing of a pipelined ADC starts with the converter specifications such as resolution (n), sampling rate (f_s), power budget, SNDR, SFDR, ENOB *etc*. During the entire design process, designer explores various alternatives, study the various design trade-offs, find out the various constraints and optimize his design in terms of power consumption, area, design effort and cost. To accomplish the task it requires a systematic design methodology that is presented in this chapter for the charge pump based pipelined ADC that requires minimum iterations in design cycle.

Figure 6.1 shows the design flow of a typical pipelined ADC. It starts with the ADC specifications such as f_s, n, required SNR, SNDR and SFDR *etc*. Once the specifications are freezed next step is to choose the ADC architecture (Flash, SAR, Pipeline *etc*.). In chapter 1, various ADC architectures are discussed with tradeoffs. For a resolution of n=10-bit and f_s=100 MS/s, the pipelined ADC is the best suited candidate consuming relatively low area and power.

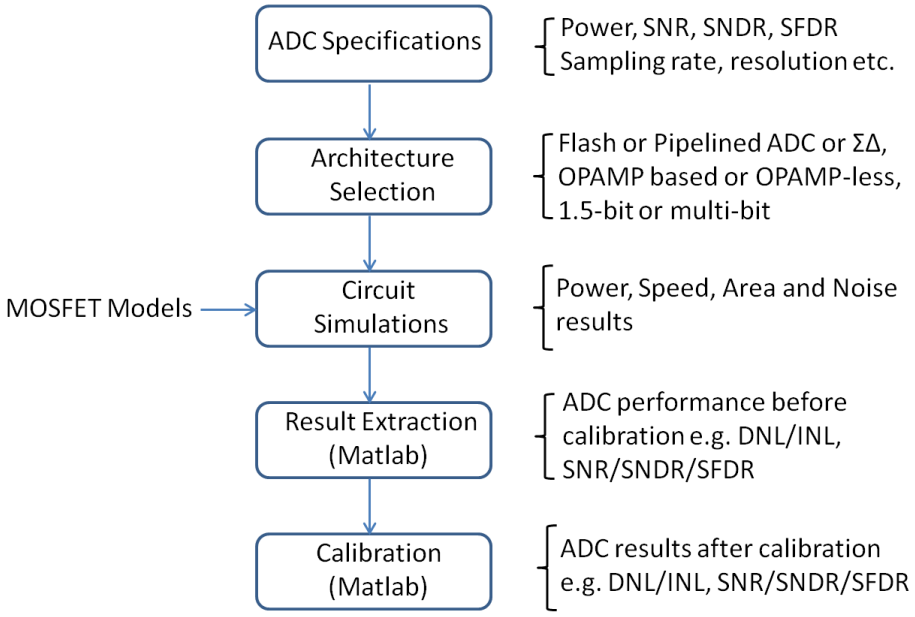


Figure 6.1. A Pipelined ADC design flow

In a pipelined ADC with the multi-bit architecture (1.5-bit/2.5-bit architecture), generally, redundancy is used to take care of the offset of the comparator used in sub-ADC. Next task is to choose MDAC architecture either using opamp or opamp-less. Since, opamp is the main power hungry block in the pipelined ADC that also consumes huge area. So, in the present work, an opamp-less pipelined ADC is utilized in order to reduce the power and area.

Once the pipelined ADC stage architecture is selected, next step is to implement the ADC specifications into physical level (Silicon level) through circuit designing at transistor level. Based on ADC specifications the required sampling capacitors values, open-loop gain of the differential amplifier (A_o), UGB, phase margin (*PM*) *etc*. are decided. These design parameters are transferred into actual physical dimensions by adjusting the width (*W*) and length (*L*) of the MOS transistors [74]. In this entire design flow, there occurs various tradeoffs while achieving the pipelined ADC specification. For example, achieving the higher ADC speed requires more power to be invested with more Silicon area. Increase in area would increase the various parasitic capacitances that effect the ADC performance (equation 4.14). Therefore it requires several iterations to fine tune the results with bottom-up approach which is a time consuming task and increases the time to market for mixed-signal ICs.

Main objective of this chapter is to propose a design methodology so that it requires less iterations and hence save designer's time to design a pipelined ADC for the given specifications. For pipelined ADC, specifications chosen in the present research work are n=10-bit, f_s=100MS/s, $SNR \geq$60dB, $SFDR \geq$ 70dB. Target technology is 0.18 μm, n-well digital CMOS at the supply voltage of V_{DD}=1.8V.

As it can be seen from Figure 6.1, after freezing the ADC specifications (Step 1) and choosing 1.5-bit opamp-less pipelined ADC (Step 2) in digital CMOS technology as discussed in Chapter 3, next step is to design a stage, its various components. Complete pipelined ADC is cascading of such stages. Further steps are discussed in the following sections.

6.2 Circuit Implementation and Tradeoffs

An opamp-less pipelined ADC stage is shown in Figure 4.3. A N-stage pipelined ADC is cascading of such stage except the last stage which is a flash based architecture as shown in Figure 6.2. Whole pipelined ADC implementation goes through various steps and

iterations. In the present research work, a MOSFET-only charge pump based 1.5-bit pipelined ADC is used as explained in section 4.2.2. In this section, a design methodology to design a MOSFET-only stage is discussed to achieve the given specifications.

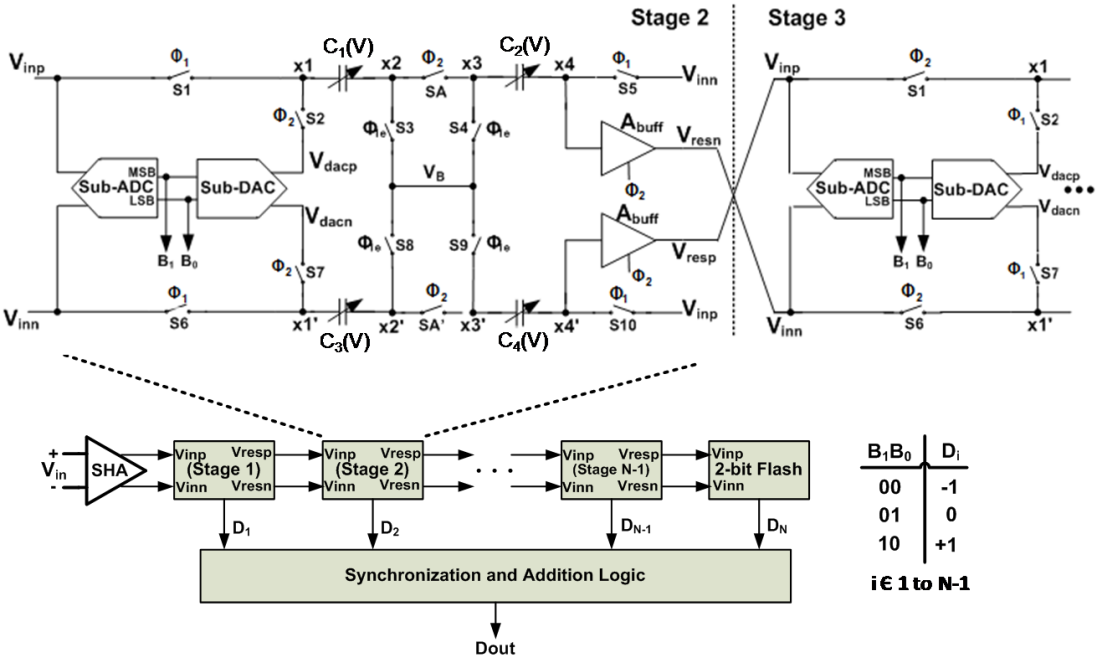


Figure 6.2. Charge pump based N-stage pipelined ADC

From equation (4.14), both A_{buff} and X affects the residue voltage of a stage. It is the prime design objective to maximize the A_{buff} to unity and minimize the effect of parasitic capacitances. Also it is evident from the equation (4.14) that effect of parasitics can be minimized by choosing the value of sampling capacitors such that $C_i \gg C_{pV_x}, C_{px4}$ that diminishes the ratio $\frac{C_{px}}{C_1}$ and $\frac{C_{px4}}{C_2}$ to a low value. However, choosing a high value of C_i decreases the speed and increases the load of the buffer which in turn requires high power to be invested to increase the speed. Thus, it is important to find the appropriate sampling capacitors values that help in meeting the ADC specifications. So designing of a stage starts with choosing the sampling capacitor values.

6.2.1 Sampling Capacitors

To design a stage and further n-bit f_s MS/s pipelined ADC, first step is to decide the value of sampling capacitors C_i ($i \in$ 1-4) in a stage. A sampling capacitor value is mainly decided by thermal noise and speed. Load at the output of the buffer mainly consist of sampling

capacitors of the next stage. Therefore, using the low capacitor values increases the bandwidth of the buffer and consequently the speed of whole ADC. On the other hand, decreasing the capacitance value increases the thermal noise ($\frac{kT}{C}$)and decrease the SNR of the ADC. Therefore, there are trade-offs among speed, power and SNR [87] and the capacitors values, therefore, impact the performance of an ADC.

SNR of a pipelined ADC is the ratio of signal power to noise power and is given by (including both thermal and quantization noise)

$$SNR = \frac{V_{FS}^2/2}{\overline{v_{qn}^2} + \overline{v_{tn}^2}} \tag{6.1}$$

where $V_{FS}$is the signal swing, $\overline{v_{qn}^2}$ is the quantization noise and $\overline{v_{tn}^2}$ is thermal noise. Quantization noise arising due to analog to digital conversion is given by

$$\overline{v^2{}_{qn}} = \frac{V^2{}_{LSB}}{12} = \frac{V^2{}_{FS}}{2^{2n} \cdot 12} \tag{6.2}$$

There are other noise sources inside the ADC such as noise due to various components, switching noise along with on-resistance noise of switches. All these noise sources contribute to overall ADC noise floor but mainly dominated by on-resistance of the switches and given by $\frac{kT}{C}$. Since the first stage contributes a significant noise so it is important to choose the sampling capacitance values so as to keep the noise as low as possible [71]. Therefore, for the switch noise to have negligible effect on SNR of the ADC, generally it is followed that $\frac{kT}{C}$ noise is less than ¼ of the quantization noise. This causes only 1dB degradation in the value of ideal SNR.

$$\frac{kT}{C_i} = \frac{1}{4} \cdot \overline{v^2{}_{qn}} \tag{6.3}$$

which in turn gives the value of C_i as

$$C_i \geq \frac{48\ kT\, 2^{2n}}{V^2{}_{FS}} \tag{6.4}$$

where k is the Boltzman's constant and T is the temperature. This is plotted in Figure 6.3 for n =10. Thus maximizing the signal swing decreases the sampling capacitor value which in turn reduces the current requirements to achieve a given speed.

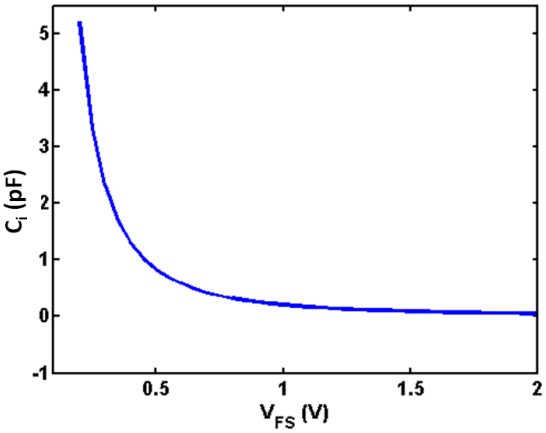


Figure 6.3. Sampling capacitor versus signal swing

Exact value of the sampling capacitor is decided by the constraints on power, speed and area. A particular value of C can be obtained by adjusting the W and L of the MOSCAPs as given by equation (4.1).

Furthermore, as buffer is the only active block in a stage so most of the power is consumed by the buffer which is dependent upon the load that a buffer needs to drive. Figure 6.4 shows that SNR versus sampling capacitor value for various signal swing. It is clear from the Figure 6.4 that with higher signal swing higher SNR can be achieved with low capacitance values and thus low area and power. Signal swing is mainly restricted by the buffer. Thus maximizing the output signal swing of buffer is one of the design objectives in buffer design.

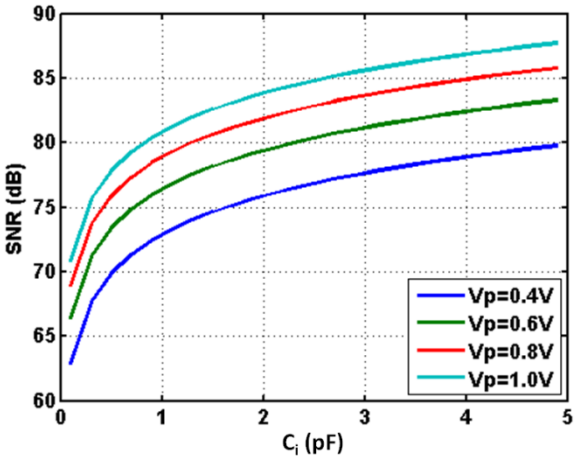


Figure 6.4. SNR vs Sampling capacitor

6.2.2 Output Buffer Design

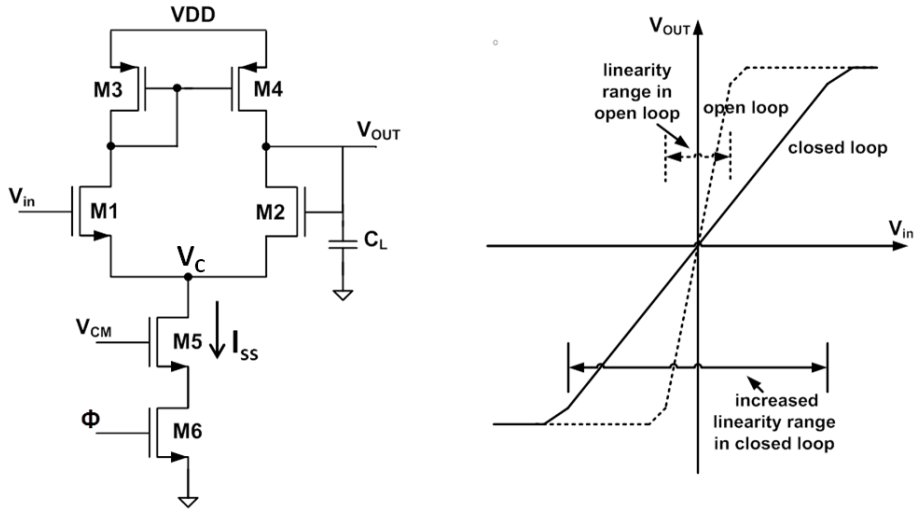
Gain and bandwidth are the two important factors that affect the accuracy of switched capacitor (SC) circuits such as ADCs [88]. As discussed in the section 4.3.2, a differential amplifier in unity-gain feedback is chosen as a buffer. Closed-loop gain of a differential amplifier in unity gain configuration (β=1) is given by

$$A_{cl} = \frac{A_0}{1+A_0} \simeq 1 \cdot \left(1 - \frac{1}{A_0}\right) \tag{6.5}$$

where A_0 is the open loop gain of differential amplifier. Including the closed loop gain of the buffer, residue voltage of a stage is given by

$$V_{res} = 1 \cdot \left(1 - \frac{1}{A_0}\right)(2V_{in} - V_{dac}) \tag{6.6}$$

with $1/A_0$ as the gain error limiting the accuracy of the stage and ADC. Gain error can be inimized by increasing the open loop gain A_0 which in turn increases the power and area. Another way to minimize the gain error is using the digital calibration techniques by using digital output of the ADC. This is a preferable choice in current deep submicron technologies due to scaling benifits.



(a) (b)

Figure 6.5. (a) Differential amplifier as a buffer (b) transfer characteristic

Another requirement of differential amplifier is to properly settle to certain accuracy during amplification phase in order to avoid any settling error. It requires a large bandwidth of differential amplifier with its unity-gain frequency given by

$$UGB = \frac{g_m}{C_L} \tag{6.7}$$

where g_m is the transconductance of the transistors M1 and M2 (i.e. $g_m = g_{m1} = g_{m2}$) and C_L is the load capacitance at the output node of the buffer (shown in Figure 4.7(b)).

Incorporating the finite gain and finite bandwidth affects on stage output, equation (6.6) is modified to (assuming identical buffers)

$$V_{res} = 1 \cdot \left(1 - \frac{1}{A_0}\right)(1 - e^{-t \cdot UGB})(2V_{in} - V_{dac}) \tag{6.8}$$

Maximum time available for amplification phase is 5ns in a 100 MS/s pipelined ADC. The differential amplifier in first stage requires a minimum bandwidth of 220.6 MHz in order to have the settling error to less than half LSB which can be obtained easily.

Neglecting the body effect of input MOS transistors M1 and M2, gain of the differential amplifier is given by

$$A_0 = g_m(r_{out\,2} \parallel r_{out\,4}) \tag{6.9}$$

where g_m is the transconductance of the transistor M1 or M2 and $r_{out\,2}$ and $r_{out\,4}$ are the output impedances of the transistors M2 and M4, respectively.

For n-bit f_s MS/s sampling rate pipelined ADC, the required UGB for the first stage buffer is given by

$$UGB = \frac{nln\,(2)f_s}{\pi} \tag{6.10}$$

From the equation (6.10) the minimum required UGB for first stage buffer in 10-bit 100-MS/s pipelined ADC is 220.6 MHz. Minimum UGB of 450 MHz (2 times) is chosen as design specification while designing the differential amplifier. Next step is to design the differential amplifier. The minimum required trans-conductance of the input MOS transistors is given by equation (6.7) i.e. $g_m = 2.83\,mS$. It is now required to decide the current in differential amplifier to get the required transconductance.

In the analog design, the first step is to decide and freeze the channel length of the MOS transistors. Generally, it is chosen to be twice of the minimum channel length in order to minimize the various short channel effects that are encountered in small sized MOS transistors. Figure 6.6 shows the MOS transistor drain current I_{ds} versus V_{gs} for W=10 μm size. Current I_{ds} decreases with increase in channel length L. Transconductance (g_m) of MOSFET versus V_{gs} is shown in the Figure 6.7. For the same V_{gs}, g_m decreases with

increase in the channel length (L), because of the decrease in MOS transistor drain current as shown in Figure 6.6. Figure 6.8 shows the I_{ds} versus V_{ds} for different transistor lengths L and keeping the transistor width W=10 μm. There are several short channel effects for L=0.18μm that decreases the output impedance of a MOS transistor (as shown in Figure 6.9) which ultimately reduces the intrinsic gain of the transistor [89]. Therefore, increasing the channel length increases the output impedance of a MOS transistor but reduces the current and consequently the g_m of a MOS transistor and consequently the UGB. Considering these tradeoffs a minimum channel of L=0.36 μm is chosen while designing the differential amplifier. Also increasing the W or L of transistor improves the matching [90].

As the transconductance and the drain current in a MOSFET are related by

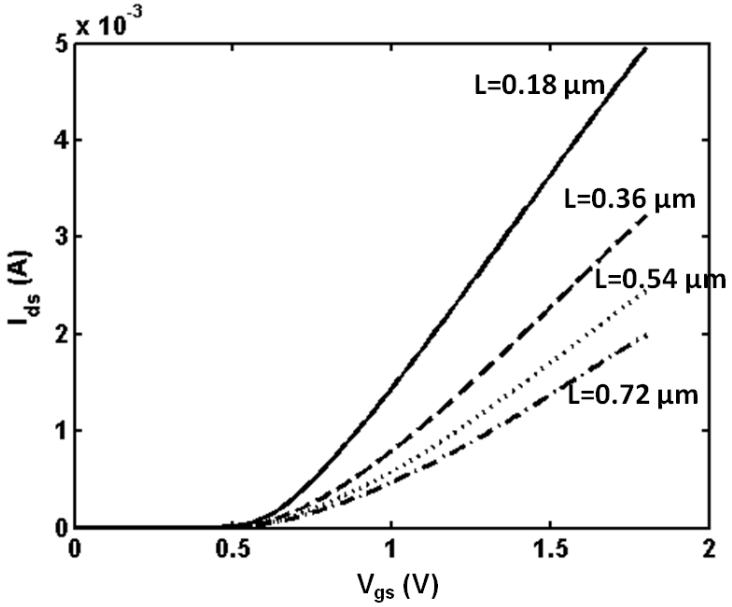


Figure 6.6. I_{ds} vs V_{ds} for a MOS transistor with different channel lengths

$$g_m = \frac{2I_D}{V_{GS}-V_{TH}} \tag{6.11}$$

For an overdrive voltage of 0.2 V (=$V_{GS} - V_{TH}$) the required current to get $g_m = 2.83\,mS$ is 337.3 μA. Transconductance g_m of the input MOS transistors is related to the current as $g_m \propto \sqrt{I_{SS}}$ and the output resistance as $r_{out} \propto \frac{1}{I_{SS}}$ therefore gain A_0 (product of g_m and r_{out}) will be proportional to $\frac{1}{\sqrt{I_{SS}}}$. For $UGB = \frac{gm}{C_s}, UGB \propto \sqrt{\frac{I_{ss}}{C_s}}$ for the same speed requirement, I_{ss} can be reduced quardratically. Here I_{SS} is the current flowing through the

differential amplifier as shown in Figure 6.5a

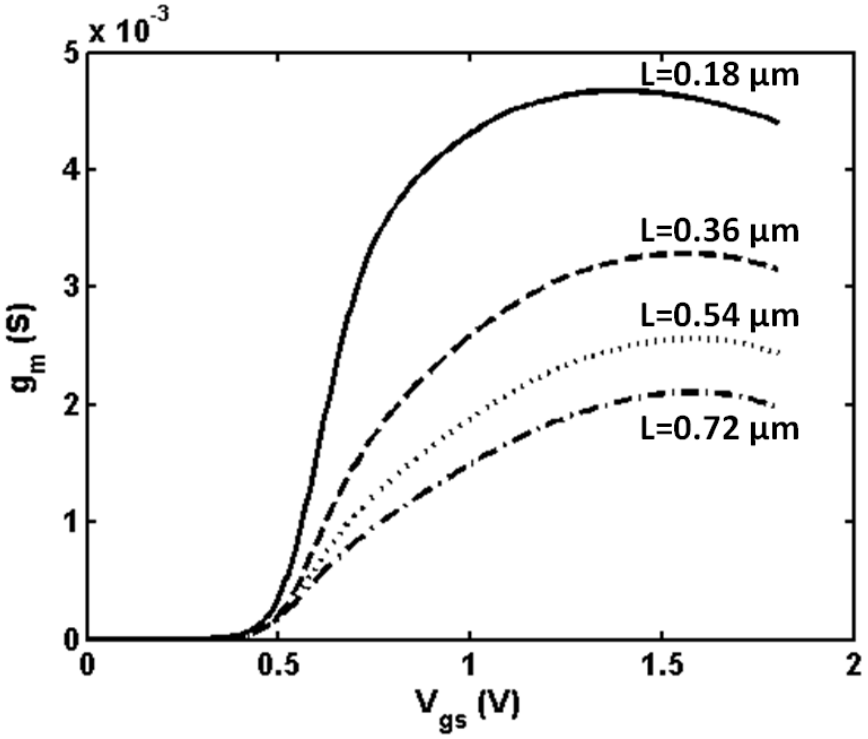


Figure 6.7. g_m vs V_{gs} for a MOS transistor with different channel lengths

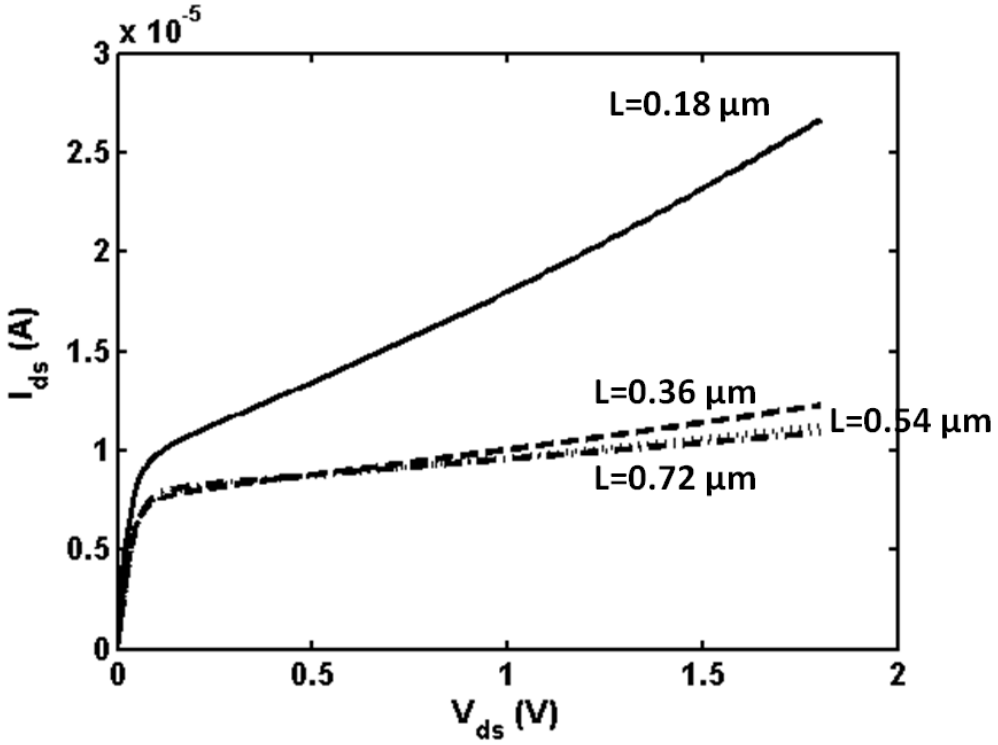


Figure 6.8. I_{ds} vs V_{ds} for a MOS transistor with different channel lengths

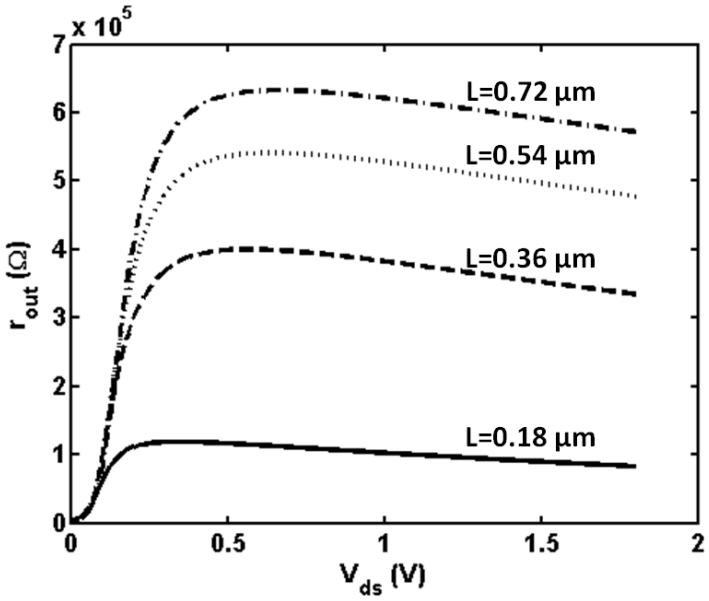


Figure 6.9. r_{out} vs V_{ds} for a MOSFET for different channel length

Figure 6.10 shows the g_m and r_{out} variation with I_{SS} and Figure 6.11 shows the DC gain A_0 and UGB variation with I_{ss}. It is clear that with the increase in the differential amplifier current I_{ss}, gain decreases and the UGB increases. Thus, a higher speed of ADC can be achieved by increasing the current I_{ss} (hence more power dissipation) trading open loop gain. Differential amplifier with an UGB of 450 MHz is chosen as primary design

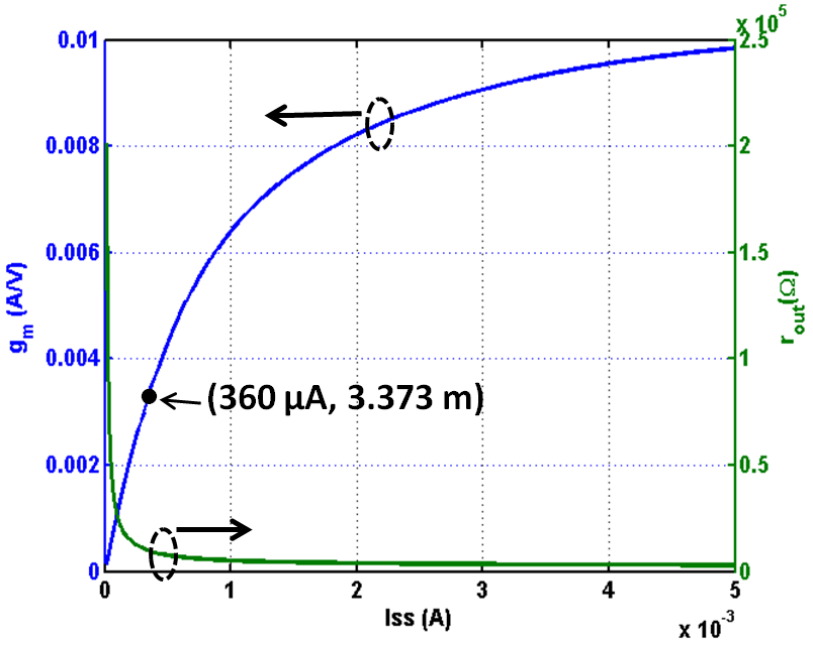


Figure 6.10. g_m and r_{out} versus I_{ss}

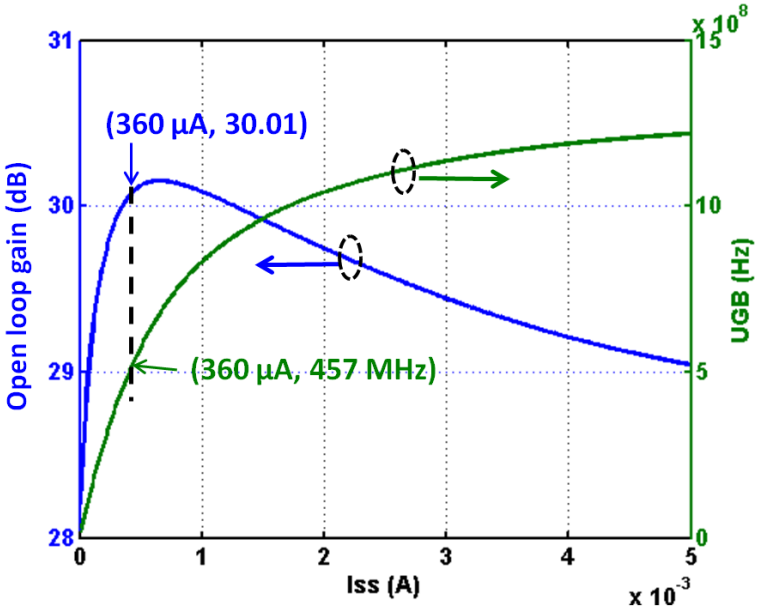


Figure 6.11. Open loop and UGB versus I_{ss}.

Table 6.1: hand calculation and simulation results

Parameters	Calculations	Simulations
UGB	450 MHz	457 MHz
g_m	$2.83\ mS$	$3.373 mS$
I_{ss}	337.3 µA	360 µA
W (M1/M2)	54 µm	80 µm

objective to achieve the desired speed of 100 MS/s. Simulation results show that it requires a current of 360 uA for UGB of 457 MHz that corresponds to a DC gain of 30.01 dB and g_m of 3.373 mS. Table 6.1 summarizes the calculation and the simulation results. The difference in the two is due to the fact that in the hand calculations square law model based equations are used that are not taking care of the various short channel effects.

For a fixed current, transconductance g_m can also be written as

$$g_m = \mu_n C_{ox} \left(\frac{W}{L}\right)_1 (V_{GS} - V_{th}) \tag{6.12}$$

Thus, another way of increasing the trans-conductance and hence the gain is obtained by increasing the W/L ratio of the input MOS transistor without increasing the current and hence power. This is shown in Figure 6.12 and Figure 6.13 for a fixed I_{SS}.

As shown in Figure 6.13, open loop gain initially increases when the input MOS transistors are in sub-threshold region (low current region) and decreases after reaching a maximum value as the current increases [91]. The maxima (of gain) can be increased by increasing the sizes of the input MOS transistors M1 and M2 [72]. However, this results in an increase in the power dissipation and the reduction in signal swing [73] which in turn reduces the SNR. Therefore, in order to maintain the same SNR, reduction in signal range increases the capacitance value that degrades the speed and requires further power to be invested to

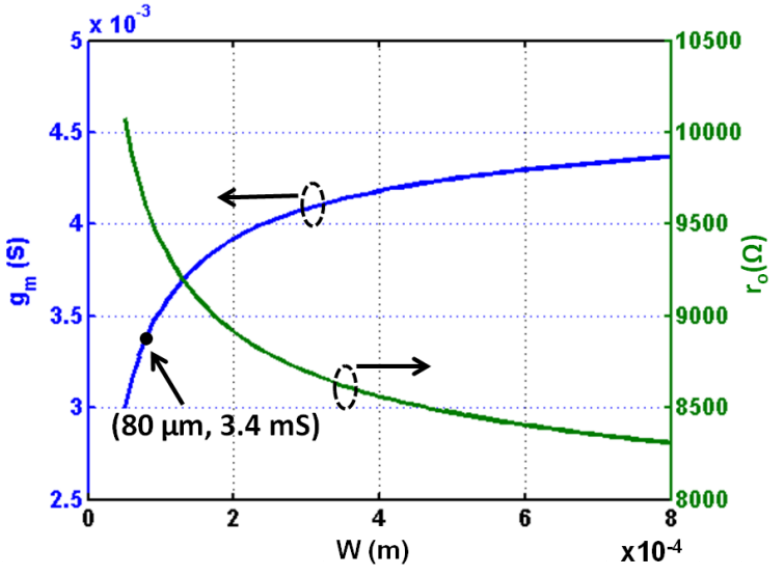


Figure 6.12. g_m and r_{out} vs W of input MOS transistors

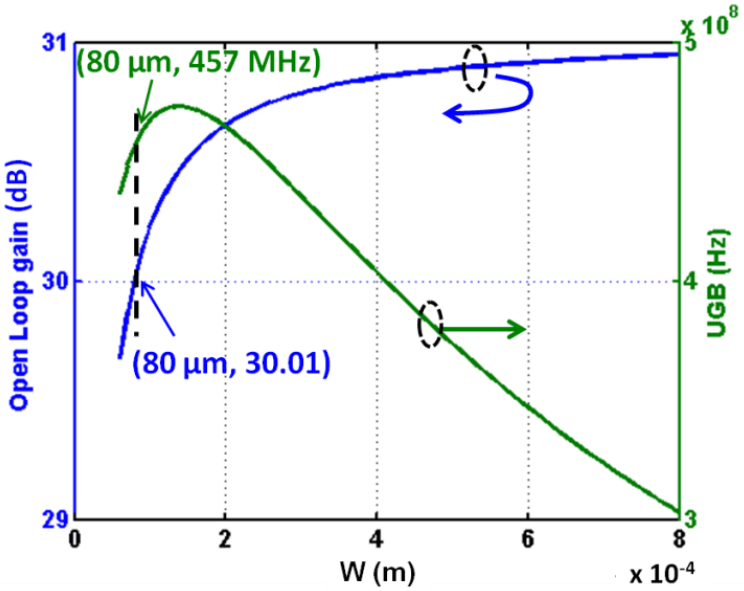
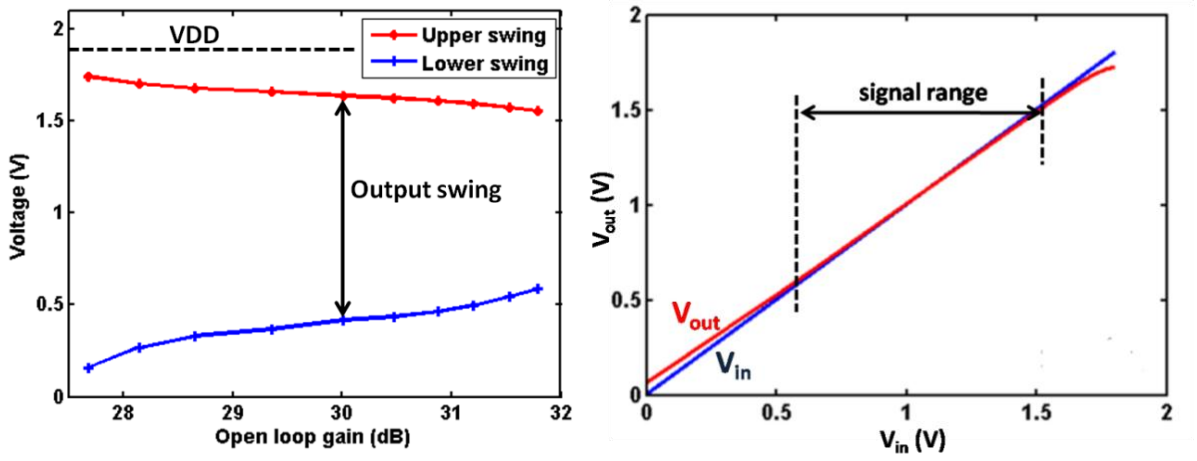


Figure 6.13. Open loop gain and UGB vs W of input MOS transistors.

increase the speed. Therefore, optimizing the low power amplifiers for desired performance is always a design challenge [92].

A simulation result of the increase in open loop gain versus output voltage swing is plotted in Figure 6.14(a). It clearly shows that with the increase in gain, output voltage swing decreases. Upper swing in Figure 6.14(a) is the saturation voltage of the MOS transistor M4 ($V_{dsat\,4}$) and Lower swing is given by $V_{dsat\,2} + V_C$ where $V_{dsat\,2}$ is the saturation voltage of the MOS transistor M2 and V_C is the voltage at drain terminal of M5 transistor. Difference of the two gives the output signal swing of the differential amplifier.

Since the differential amplifier is used in the unity gain feedback configuration and the open loop gain diminishes by a factor of $(1 + A_0)$ while in the closed-loop gain and harmonic distortion also diminishes by $(1 + A_0)$ factor. This also results in an increase in the linearity range of the amplifier.. Figure 6.14(b) shows the simulations results of the differential amplifier as a buffer. It shows the signal range where V_{out} is linear as the input voltage varies from 0 to V_{DD} and nonlinear region at the top end. Nonlinearity occurs due to the fact that as V_{out} increases, V_{SD} of M4 transistor decreases and it enters linear region from saturation. It is to be noted here that considering the signal level beyond linear range gives non-linearity at the ADC output and decrease the SNDR of an ADC. Therefore region of operation is confined to linear range in order to reduce the distortion component.



(a) (b)

Figure 6.14. (a) voltage swing vs open loop gain (b) transfer characteristics of unity-gain configuration of differential amplifier

6.2.3 Effect on DNL

Insufficient DC gain A_0 causes the missing codes at the ADC output. One of the way to measure the missing codes is Differential Nonlinearity (DNL) test. DNL caused by the gain error of the first stage in a pipeline ADC is the largest and is given by

$$DNL\ (LSB) = \left(\frac{G_{ideal} - G}{G_{ideal}}\right)\left(\frac{G_{ideal} - 1}{n_c}\right)\frac{2^n}{G_{ideal}} \tag{6.13}$$

where G_{ideal} and G(given by $2(1 - 1/A_0)$) are the ideal and the real gain of a stage respectively, n_c is the number of comparators per stage and n is the ADC resolution. Figure 6.15 shows the DNL in LSB versus stage gain. It shows that DNL decreases with the increase the in stage gain and hence requires larger DC gain of differential amplifier. To increase the DC gain, it requires larger input MOS transistors M1 and M2 with more current. However, it results in more area, more power dissipation with reduced signal swing. For the same SNR, reduced signal swing requires larger capacitances and further increases the area.

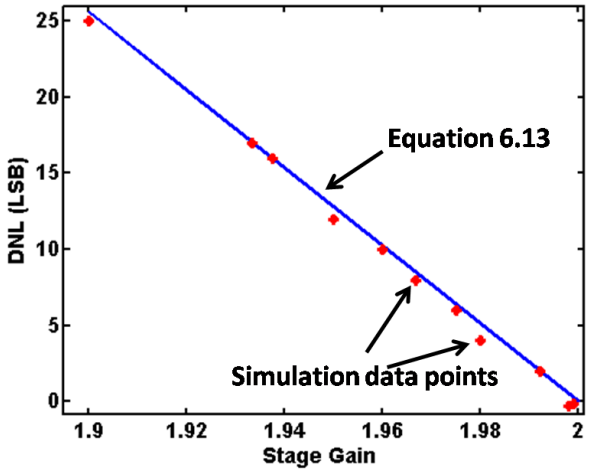


Figure 6.15. DNL vs stage gain (G)

Figure 6.16 shows the DNL (in LSB) versus open loop gain A_0 for both opamp based and current charge pump based work. It shows that the DNL decreases with the increase in A_0 for both the cases trading area and power. However for the same A_0, DNL in the present work is about a half of that in the opamp based pipelined ADC due to unity feedback factor in former. Therefore for the same DNL it requires lesser A_0 and hence requires lesser power and area in charge pump based pipelined ADC as compared to the conventional opamp based

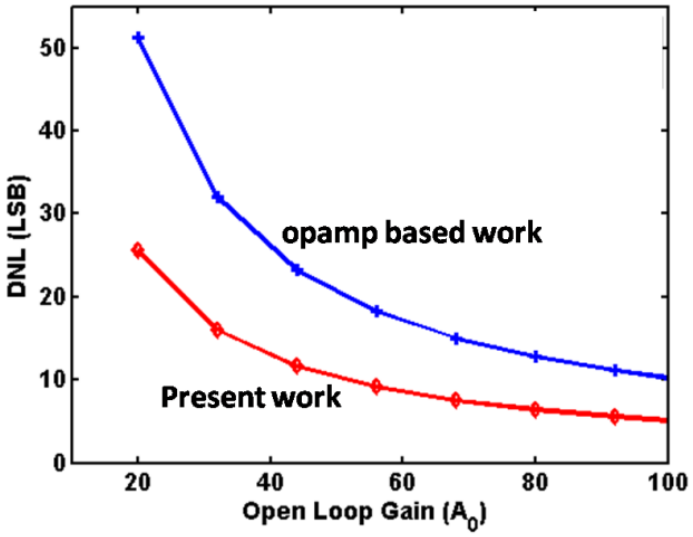


Figure 6.16. Effect of open loop gain (A_0) on DNL.

pipelined ADC. INL can be obtained by the summation of DNL

$$INL(i) = \sum_{j=1}^{i} DNL(j) \tag{6.14}$$

where j corresponds to the code j.

6.2.4 Effect on SFDR

SFDR is another important dynamic performance parameter in an ADC that is effects by the gain error. It is defined as the ratio of signal power to the power of the largest spurious harmonics in the ADC output spectrum.

$$SFDR = 10\log\left(\frac{signal\ \ power}{largest\ \ spurious\ \ power}\right) \quad (dB) \tag{6.15}$$

In an ADC, due to the nonlinearity in the transfer function and low finite gain of the amplifier, harmonics are introduced in the output spectrum [93-94]. Harmonics not only degrade the dynamic range of an ADC but also reduce the ENOB [95]. Thus it is essential to reduce the harmonic components to improve the ADC dynamic performance parameters.

In the pipelined ADC with 1.5-bit/stage, it requires a gain of 2 in every stage. Low finite gain of the differential amplifier introduces the gain error (ε_g) that reduces the gain of a stage from 2 to $2(1-\varepsilon_g)$. Reduced gain causes missing codes at the output transfer characteristics and harmonics at the ADC output spectrum. With gain error, SFDR is given by [94]

$$SFDR \approx 9.03b - c - 20\log(\varepsilon_g)\ (dB) \tag{6.16}$$

where b is the number of bits in the first stage and c takes the value from 0 to 6 [94]. Figure 6.17 shows the SFDR versus A_0 with $c = 2$.

Next, it is important to understand the effect of parasitic capacitance, present at the input of the buffer on the performance of pipelined ADC. As clear from equation (4.14) parasitic capacitance at node $x4$ (i.e C_{px4}) impacts the stage residue more as compared to other parasitic capacitances. C_{px4} consists of the gate capacitance of the buffer and the

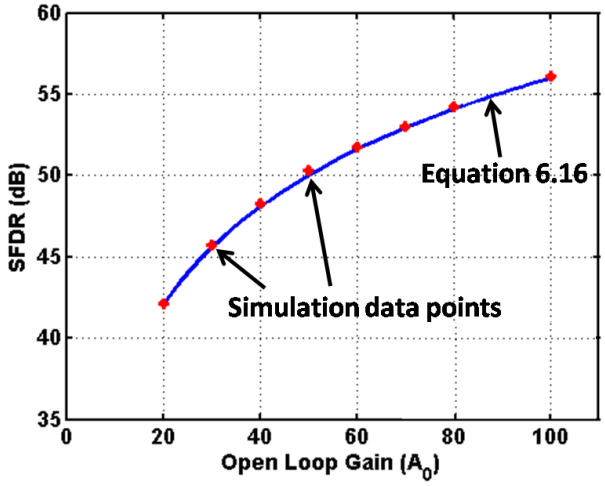


Figure 6.17. SFDR vs open loop gain (A)

diffusion capacitance at that node, with dominated by former dominating the later. For a high open loop gain and UGB, the sizes of the input MOS transistors are generally required to be high.

However, with the increase in the W/L ratio of the input MOS transistors, gate capacitance increases which in turn increases the C_{px4} and X. Since, the buffer gate capacitance dominates in factor X, the sizes of the input MOS transistors should be carefully chosen. Large value of C_{px4} alters the gain of a stage from 2 and causes the missing codes at the ADC as shown in Figure 5.1. It can be seen that the effect of the parasitic capacitances is similar to the gain error with missing codes at the ADC output. Thus there is a trade-off in choosing the size of input MOS transistors as larger input size decrease the gain error but increase the gate capacitance that in turn increases the number of missing codes. Therefore, sizes of the input MOS transistors in unity-gain buffer are kept small trading mainly with its open loop gain.

Another single stage amplifier that can be used as a buffer is folded cascade amplifier in unity gain feedback configuration. A folded cacscode amplifier is shown in Figure 6.18. Table 6.2 shows the comparison between differential amplifier and folded cascode amplifier. Folded cascode amplifier has high gain as compared to differential amplifier because of its cascode structure that offers high output impedance. Its ICMR is also high as compared to

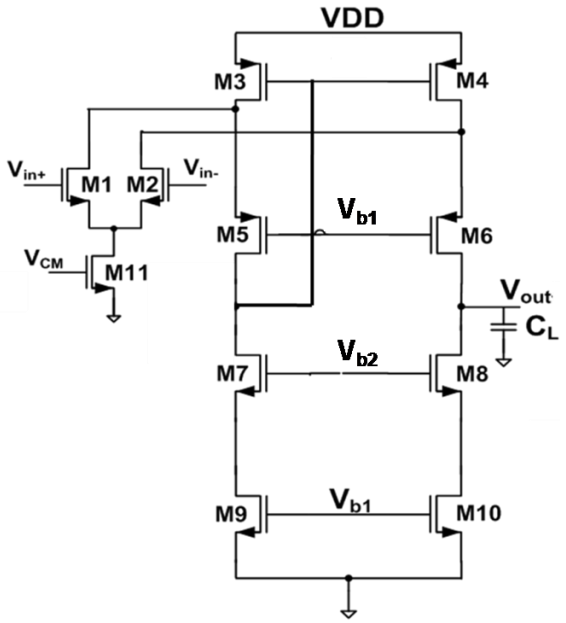


Figure 6.18. A folded cascade amplifier

Table 6.2. Comparison between differential amplifier and folded cascode amplifier

Amplifier Parameters	**Differential**	**Folded cascode**
Gain	low	high
ICMR	high	high
Output swing	high	low
Design complexity	low	high
Speed	high	less
UGB	high	low
Area	low	high
Input referred noise	$\frac{16kT}{3g_{m1}}\left(1+\frac{g_{m3}}{g_{m1}}\right)$	$\frac{16kT}{3g_{m1}}\left(1+\frac{g_{m3}}{g_{m1}}+\frac{g_{m9}}{g_{m1}}\right)$

differential amplifier but folded cascode amplifier suffers from low output swing because of its cascode nature and low speed due to larger parasitic capacitances at different nodes. Also, designing a folded cascade amplifier is more cumbersome as compared to differential amplifier.

Table 6.3 shows the comparison when differential amplifier/folded cascade amplifier is used in a pipelined ADC stage. Because of low output swing ADC with folded cascade will have low SNR and SNDR value as compared to ADC with differential amplifier.

Table 6.3. Comparison of ADC parameters for different amplifiers

ADC Parameters	**Differential Amplifier**	**Folded cascade Amplifier**
Speed	high	low
SNR	high	low
SNDR	high	low
Power consumption	less	high
Si area	less	high

6.3 Simulation Results

Comparator used in the present research work is based on dynamic comparator [96] and network as shown in [42]. Figure 6.19 shows the simulation results of the sub-ADC and sub-DAC (shown in Figure 4.3a) for a linear ramp varying from 0.6V to 1.6V fully differentially. Clocks used in the Figure are non-overlapping clocks as mentioned in section 4.2.2. B1 and B0 are the two output bits from the sub-ADC and V_{dacp} and V_{dacn} are the output voltage levels of sub-DAC.

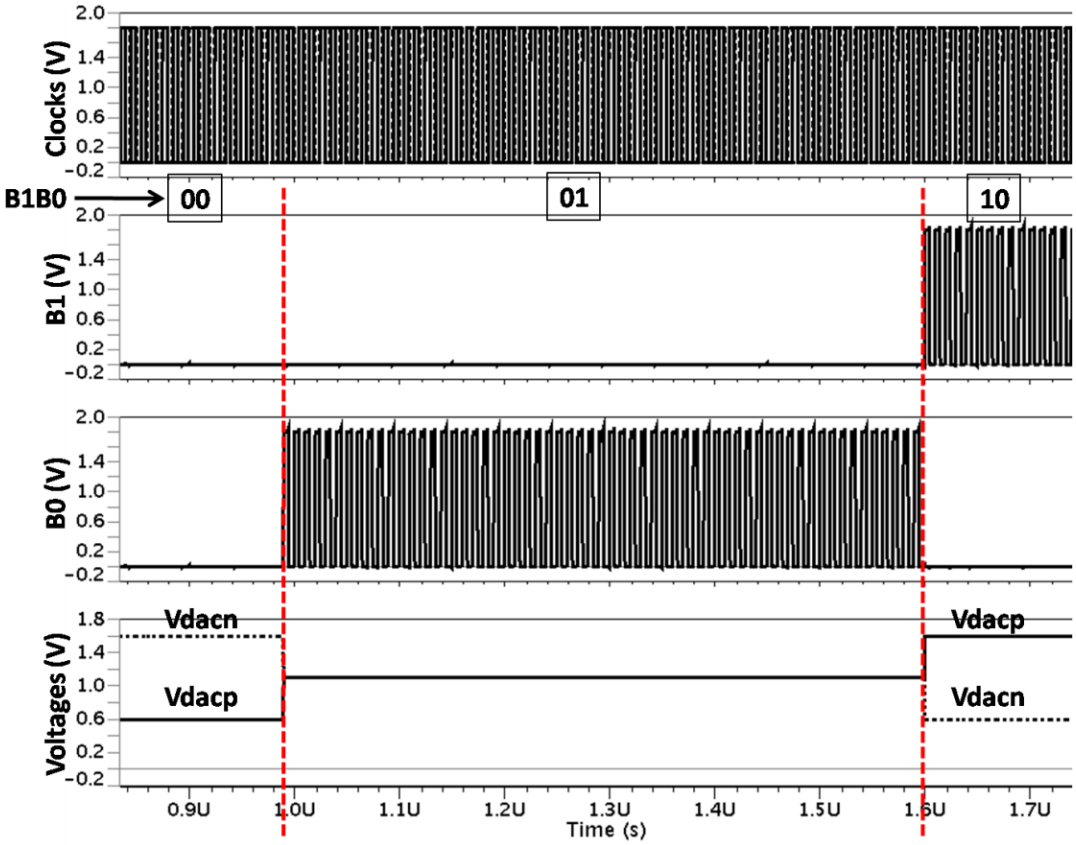


Figure 6.19. Simulation results of Sub-ADC and Sub-DAC

Key design considerations while designing the differential amplifier are low area, low power, high dynamic range and high SNR along with the design simplicity. A CMOS differential amplifier is designed accordingly that has an open loop gain of 30.01 dB (≅ 32 V/V), PM of 77º and UGB of 457 MHz with a 320 µA total current. This much of UGB is sufficient for the settling accuracy of 10-bit at 100 MS/s. It gives a inter stage gain of 1.94 ($2(1-1/A_0)$) with a relative gain error of 3%. A signal swing of 0.6V to 1.6V *i.e* 1V is achieved at the output of the differential amplifier in the unity-gain feedback configuration as shown in Figure 6.14(b).

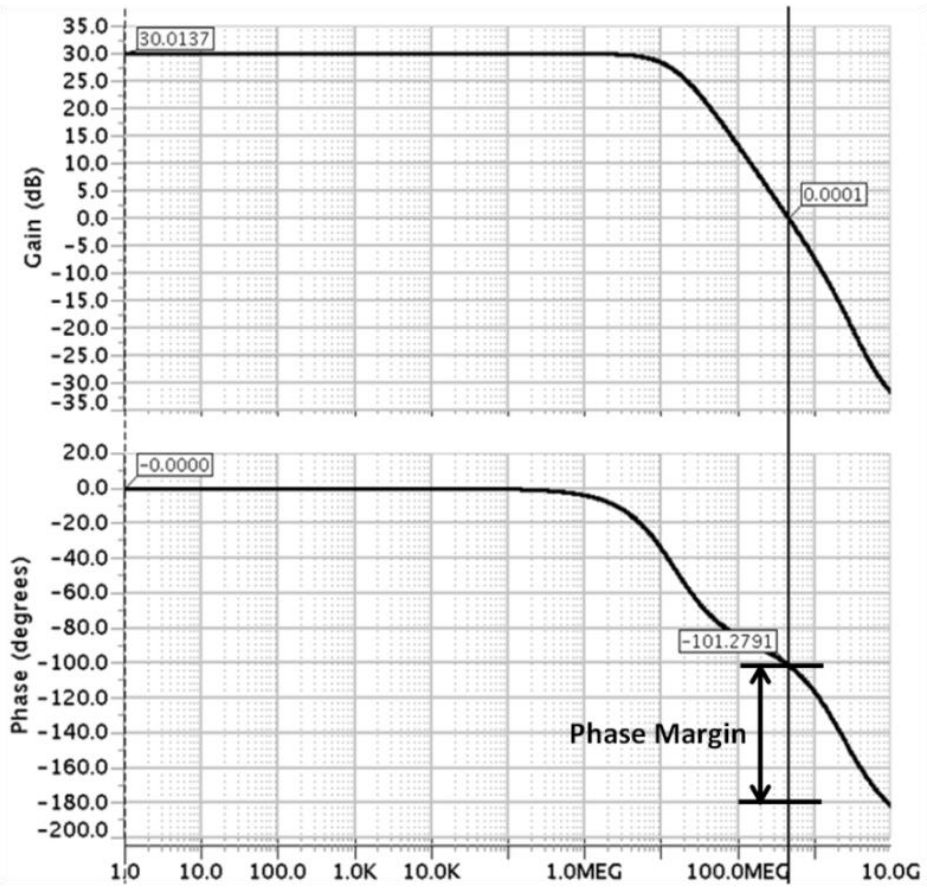
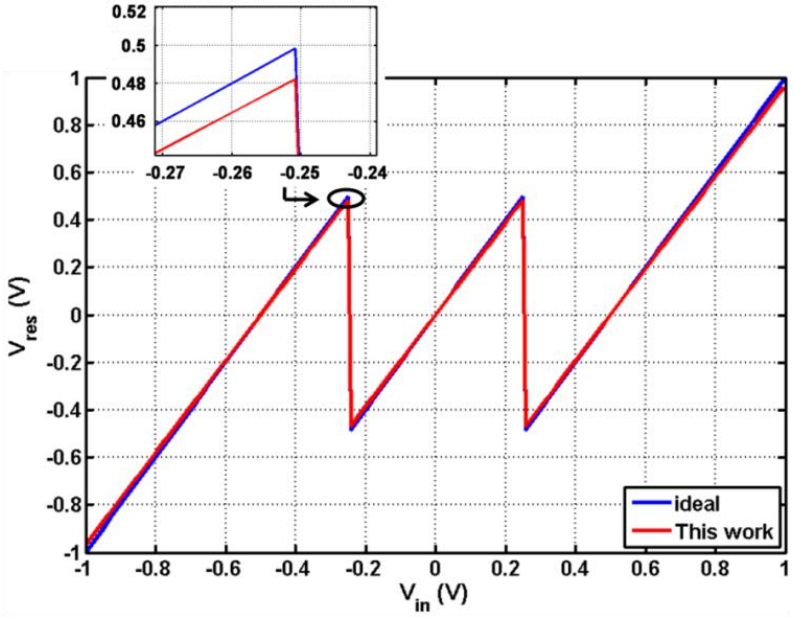
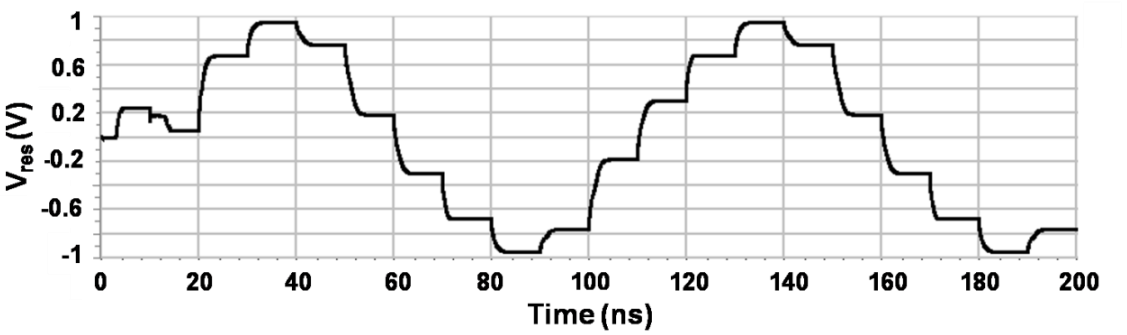


Figure 6.20. Frequency response of differential amplifier



(a)



(b)

Figure 6.21. Simulated stage results (a) residue curve (b) transient response

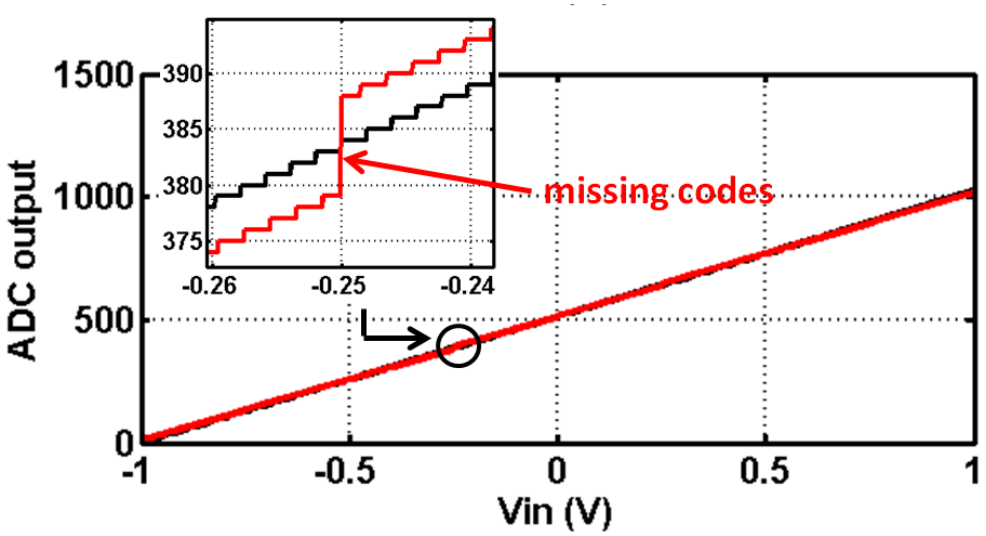


Figure 6.22. Effect of low open loop gain of 1st stage on 10-bit ADC

Figure 6.20 shows the AC response of the buffer. Figure 6.21(a) shows the residue curve of the 1.5-bit stage with 1V single ended ramp (varying from 0.6V to 1.6V) given at the input of the stage. Figure 6.21(b) shows the transient response when sampled sinusoidal signal of 1 Vpp single ended at 100 MHz is given. Results show that there occurs only gain error in the proposed stage.

Figure 6.22 shows the effect of the low open loop gain of 1st stage on the 10-bit ADC characteristics, assuming rest of the stages to be ideal. It shows the missing codes at the ADC output. Various ADC performance parameters such as DNL, INL, SNDR, SFDR can be extracted by using MATLAB programs and are uncalibrated results.

Further layout of proposed single stage and three stage pipelined ADC is drawn, parasitics extracted and post layout simulation is performed using BSIM3v3 model

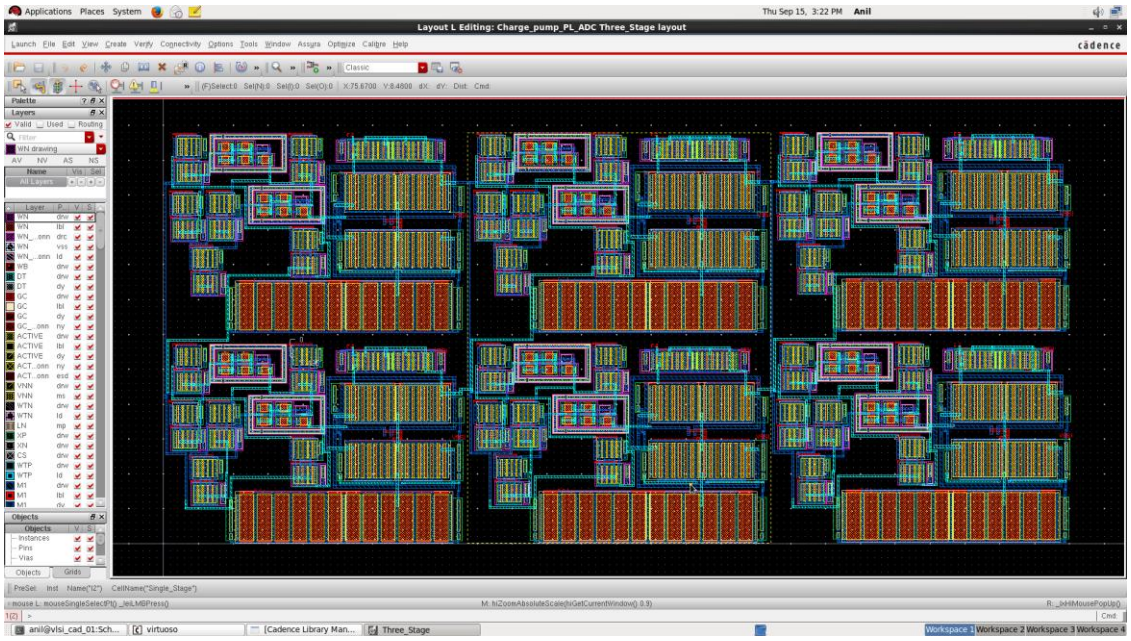


Figure 6.23. Layout of the proposed 3-stage pipelined ADC.

parameters.

Figure 6.23 shows the layout of the proposed 3-stage pipelined ADC with MOSCAP and buffer in common-centroid layout technique. Fig. 6.24 shows the comparison of pre-layout (dark lines) with post layout simulation (dotted lines) for input signal of 1 Vpp single ended and frequency of 10 MHz. Mismatch at some points is due to the effect of parasitics.

The proposed stage suffers from only one non-ideality *i.e.* gain error and is left for the correction in digital domain by using digital calibration technique. Digital calibration is one of the preferred choices to correct the missing codes in today's deep submicron technologies. Although, adding a calibration logic increases the area and power but it is far less as compared to the areas and power of the total ADC [18]. A complete pipelined ADC can be designed by cascading the proposed MOSFET-only 1.5-bit stage and the gain error can be compensated by using the digital background calibration technique as discussed in Chapter 5. After calibration, ADC parameters are again extracted to know the effectiveness of the calibration.

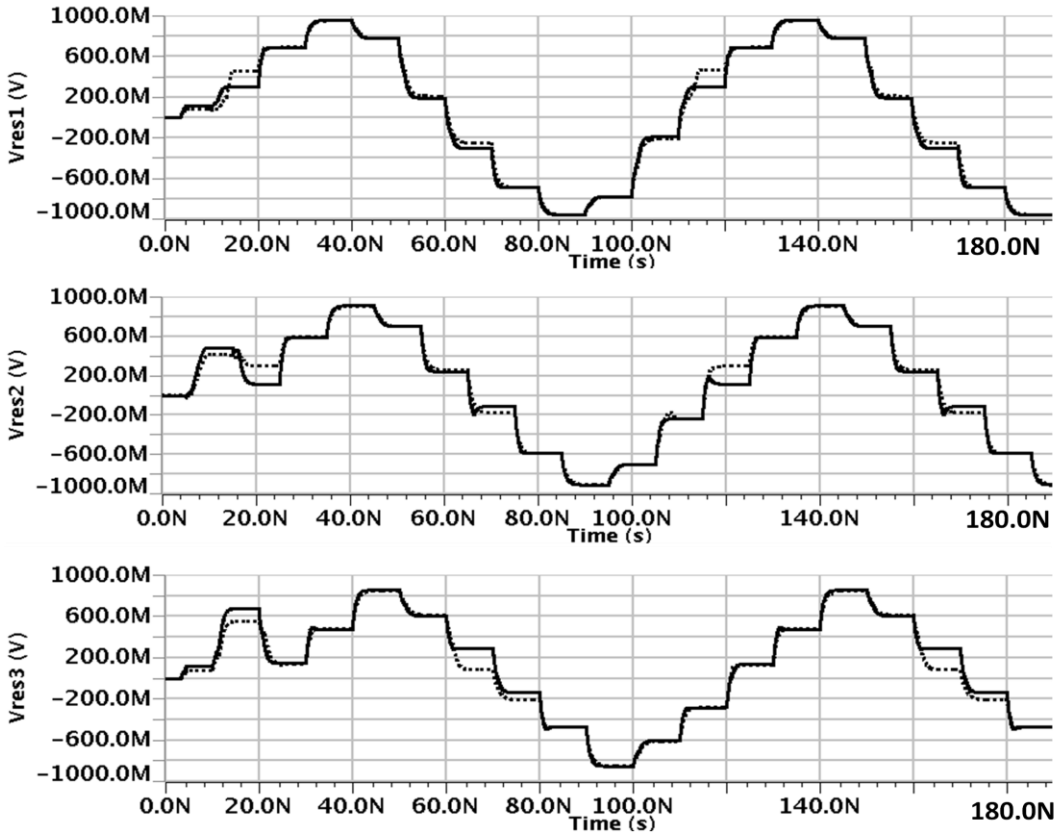


Figure 6.24. Pre-layout (solid line) and post-layout simulation (dotted line) results of different stages

6.4 Summary

This chapter presented the design methodology for the proposed MOSFET-only charge pump based pipelined ADC. Following this, a MOSFET-only charge-pump based pipelined ADC can be designed with lesser iterations and design efforts. Designing of various building blocks of the proposed stage along with tradeoffs were discussed in this chapter. Effect of low gain of the buffer on various ADC performance parameters such as signal swing, DNL, INL, SNR and SFDR were also discussed.

Chapter 7

Conclusion and Future Scope

7.1 Conclusion

Pipelined ADC is the most suitable ADC for medium to high resolution and high speed applications. Scaling of CMOS technology has benefited the digital circuits due to increase in performance with reduction in area whereas analog or mixed signal circuits (such as ADCs) designers face new design challenges with every downscaling node. This is the reason why ADC circuit designers remain stick to older or know technologies to meet the design specifications. Increase in performance of digital circuits cannot be replicated to analog blocks and therefore in an SoC having both digital and ADC blocks, performance of whole SoC will be decided by the performance of ADCs.

Due to scaling, supply voltage (VDD) reduces which limits the available signal swing. In scaling even if the absolute noise-level is kept constant, the relative noise-floor still increases due to the reduced swing and hence DR and SNR reduces. Therefore scaling of digital and analog circuits in pipelined ADC will not scale at the same rate in the future [7]. SNR decreases with the decrease of the signal amplitude which requires a larger sampling capacitance value to maintain the same SNR. This, however, leads to an increase of power consumption and area in pipelined ADC.

In order to improve future pipelined ADC's static and dynamic performance, it is essential to find new design techniques. Most propelling reason of this is to enable the VLSI industry to integrate as many functions as possible on a single silicon chip at reduced price with longer battery life.

A promising trend to increase the performance of pipelined ADC and its power efficiency is to find the new power efficient architectures such opamp-less or comparator based architectures and replaces the analog operations by imprecise analog blocks and removes the errors due to imperfections in digital way. This means take most of the analog functionality towards digital side and adopting digital means of correcting analog circuit

imperfections. This seems to be helpful to researchers and designers to achieve high performance at low cost with longer battery life.

This chapter outline the significant contributions of current research work:

- Various sources of errors in the pipelined ADC have been analyzed and modeled using MATLAB. Also, their impact on the stage and overall pipelined ADC characteristic has been presented.
- The design of a 10-bit 100 MS/s pipelined ADC has been carried out using MOSCAPs instead of linear MIMCAPs (available between top metal layers). It offers higher capacitance density, readily available in every CMOS process and reduces the manufacturing cost.
- Pipelined ADC employs the use of charge pump based technique to achieve the inter stage gain of 2 and avoids the use power hungry opamp leading to a total power consumption of 16.53mW, which is reasonably less as compared to other pipelined ADCs with the same number of resolution bits and sampling-rate found in the literature.
- A buffer circuit targeting low power, low area and high swing is designed trading mainly gain. This approach in the design is not only power-area efficient but also provides high output swing that results in a marked improvement in the signal-to-noise ratio along with reduction in the overall area and power consumption of the ADC.
- The low value of open loop gain of the buffer causes the gain error of about 3% that leads to missing codes at the ADC output. A digital calibration technique is, therefore, used to compensate the gain error taking the benefits of technology scaling. After calibration, the differential non linearity DNL, improves from -1 to +0.6/-0.4 LSB and integral non linearity INL, improves from +9.3/-9.6 LSB to within ± 0.5 LSB. Also, the SNDR and SFDR of 66.78 dB and 79.3 dB is obtained, respectively.
- Design methodology of the proposed MOSFET-only charge pump based pipelined ADC is discussed targeting lesser iterations and design efforts for a given ADC specifications. Designing of various building blocks of the proposed ADC stage along with tradeoffs on various ADC performance parameters such as signal swing, DNL, INL, SNR and SFDR are also discussed.

7.2 Future Work

In the future work, speed of the ADC can be further increased by using time division multiplexing technique. Also, the present design uses charge-pump based 1.5-bit/stage architecture that can be replaced by a 2.5-bit or 3.5-bit per stage. It will reduce the number of cascading stages and power. Since, buffer is the only block that limits the speed and resolution so some other power efficient block or approach needs to be discovered. Also, scaling of the pipelined ADC stages that includes the capacitor sizes and current requirements needs to be investigated.

References

[1] Len Staller, Understanding analog to digital converter specifications, Design Article, EE- Times, Feb. 2005

[2] R. Jacob Baker, CMOS Mixed Signal Circuit Designs, 1st Edition, Wiley-IEEE Press, 2002

[3] Walt Kester, Which ADC Architecture Is Right for Your Application? Analog Dialogue, Analog Devices, 39, Jun. 2005

[4] A. Matsuzawa, "Technology Trend of ADCs," IEEE International Symposium on VLSI Design, Automation and Test, 176-179, 2008

[5] A. Matsuzawa, "Nano-scale CMOS and Low Voltage Analog to Digital Converter Design Challenge," IEEE - 8th Solid-State and Integrated Circuit Technology Conference, 1676-1679, Oct. 23-26, 2006

[6] K. Uyttenhove and M.S.J. Steyaert, "Speed-Power-Accuracy tradeoff in High Speed CMOS ADCs," IEEE Transactions on Circuits and Systems-II: Analog and Digital Signal Processing, 49, 280-287, 2002

[7] Y. Chiu, B. Nikolic and P. R. Gray, "Scaling of Analog-to-Digital Converters into Ultra-Deep-Submicron CMOS," Proc. of IEEE-Custom Integrated Circuit Conference, 375-382, 2005

[8] M. J. M. Pelgrom, A. C. J. Duinmaijer and A.P.G. Welbers, "Matching properties of MOS transistors," IEEE Journal of Solid State Circuits, 24, 1433-1439, 1989

[9] M. J. Pelgrom, H.P. Tuinhout and M. Vertregt, "Transistor matching in analog CMOS applications," International Electron Devices Meeting, 915-918, 1998

[10] M. Steyaert, J. Bastos, R. Roovers, P. Kinget and W. Sansen, "Threshold voltage mismatch in short-channel MOS transistors," Electronics Letters, 30, 1546-1548, 1994

[11] M. Abo and P. R. Gray, "A 1.5-V, 10-bit, 14.3-MS/s CMOS pipeline analog-to-digital converter," IEEE Journal of Solid State Circuits, 34, 599-606, 1999

[12] T. B. Cho and P.R. Gray, "A 10 b, 20 MS/s, 35 mW pipeline A/D converter," IEEE Journal of Solid State Circuits, 30, 166-172, 1995

[13] Feng Wenxiao, Lu Tiejun and Wang Zongmin, "Analysis and Design of Fully Differential Gain-Boosted Op-amp for 14bit 100MS/s Pipelined Analog-to-Digital Converter," 5th International Joint Conference on INC, IMS and IDC, 66–69**,** Aug. 25-27, 2009

[14] Weibiao Zhang and Marwan Hassoun, "A Small Signal Analysis of a Gain Boosting Amplifier," Southwest Symposium on Mixed-Signal Design, 141–146, Feb. 27-29, 2000

[15] Yi Yang and David M. Binkley, "Modeling and Optimization of Fast-Settling Time Gain-Boosted Cascode CMOS Amplifiers," Proceedings of the IEEE Southeast Conference, 33-36, Mar. 18-21, 2010

[16] M. Mezbah, Uddin Shaber and Svante Signell, "Fully Differential Gain-Boosted Ota Design for Pipeline DA-converter in 180nm CMOS Technology," 12th IEEE International Conference on Electronics, Circuits and Systems, 1–4, Dec. 11-14, 2005

[17] Su Li and Qiu Yulin, "Design of a Fully Differential Gain-Boosted Folded-Cascode Op Amp with Settling Performance Optimization," IEEE Conference on Electron Devices and Solid-State Circuits, 441–444, 2005

[18] B. Murmann and B. E. Boser, "A 12-bit 75-MS/s pipelined ADC using open-loop residue amplification," IEEE Journal of Solid-State Circuits, 38, 2040–2050, 2003

[19] E. Iroaga and B. Murmann, "A 12 b, 75 MS/s pipelined ADC using incomplete settling," IEEE Journal of Solid State Circuits, 42, 748-756, 2007

[20] J. K. Fiorenza and T. Sepke, P. Holloway, C. G. Sodini and H.S. Lee, "Comparator-based switched-capacitor circuits for scaled CMOS technologies," IEEE Journal of Solid-State Circuits, 41, 2658–2668, 2006

[21] S. R. Krishna, M. S. Baghini and J. Mukherjee, "Current-mode CMOS Pipelined ADC," IEEE-EUROCON, St. Petersburg, Russia, 205-210, 2009

[22] L. Brooks and H.S.Lee, "A Zero-Crossing-Based 8-bit 200 MS/s Pipelined ADC," IEEE Journal of Solid State Circuits, 42, 2677- 2687, 2007

[23] H. S. Lee and C. G. Sodini, "Analog-to-Digital Converters: Digitizing the Analog World," IEEE Proceedings, 96, 323-334, 2008

[24] H. Zhang, M.M. Elsayed and E. Sanchez-Sinencio, "New Applications and Technology Scaling Driving Next Generation A/D Converters," European Conference on Circuit Theory and Design, 109-112, 2009

[25] van Veldhoven, R. H. M. Rutten, R. and L. J. Breems, "An Inverter-Based Hybrid ΣΔ Modulator," IEEE Solid State Circuits Conference, 493-494, 2008

[26] Y. Chae and G. Han, "Low Voltage, Low Power, Inverter-Based Switched-Capacitor Delta-Sigma Modulator," IEEE Journal of Solid State Circuits, 44, 458-472, 2009

[27] H. Luo, Y. Han, R. C. C. Cheung , X. Liu, and T. Cao, "A 0.8-V 230-μW 98-dB DR Inverter-Based Modulator for Audio Applications," IEEE Journal of Solid State Circuits, 48, 2430 - 2441, 2013

[28] L. Brooks and H. S. Lee, "A 12b 50MS/s Fully Differential Zero-Crossing-based ADC without CMFB," IEEE Solid State Conference, 166-167, 2009

[29] J. Hu, N. Dolev and B. Murmann, "A 9.4-bit, 50-MS/s, 1.44-mW Pipelined ADC Using Dynamic Residue Amplification," IEEE Journal of Solid State Circuits, 44, 1057-1066, 2009

[30] I. Ahmed and D. A. Johns, "A Low Power Capacitive Charge Pump Based Pipelined ADC," IEEE Journal of Solid State Circuits, 45, 1016-1027, 2010

[31] A. Agnes, E. Bonizzoni, P. Malcovati and F. Maloberti, "A 9.4-ENOB 1V 3.8μW 100kS/s SAR ADC with Time-Domain Comparator," IEEE Solid State Conference, 246-247, 2008

[32] S. Naraghi, M. Courcy and M. Flynn, "A 9b 14μW 0.06 mm^2 PPM ADC in 90nm Digital CMOS," IEEE Solid State Conference, 168-169, 2009

[33] S. Gupta, M. Choi, M. A. Inerfield and J. Wang, "A 1 Gs/s 11 b ADC with 55-dB SNDR, 250-mW Power Realized by a High Bandwidth Scalable Time-Interleaved Architecture," IEEE Journal of Solid State Circuits, 41, 2650-2657, 2006

[34] W. I. Mok, Pui-In Mak, Seng-Pan U and R. P. Martins, "Modeling of Noise Sources in Reference Voltage Generator for Very-High-Speed Pipelined ADC," IEEE 47th Midwest Symposium on Circuits and Systems, 5 - 8, 2004

[35] H. Aminzadeh, M. Danaie and R. Lotfi, "Design of High-Resolution MOSFET-Only Pipelined ADCs with Digital Calibration," IEEE Europe Conference & Exhibition on Design, Automation and Test, 1 - 6, 2007

[36] Sang-Min Yoo, Jong-Bum Park, Seung-Hoon Lee and Un-Ku Moon, "A 2.5-V 10-b 120-MSample/s CMOS pipelined ADC based on merged-capacitor," IEEE Transactions on circuits and Systems II, 51, 269 - 275, 2004

[37] J. Yuan, S. W. Fung, K. Y. Chan and R. Xu, "A 12-bit 20 MS/s 56.3 mW Pipelined ADC With Interpolation-Based Nonlinear Calibration," IEEE Transactions on Circuits and Systems I, 7, 1 - 11, 2011

[38] P. Bogner, Franz Kuttner, Claus Kropf , Thomas Hartig, Markus Burian and Hermann Eul "14 b 100 MS/s digitally self-calibrated pipelined ADC in 0.13 um CMOS," IEEE International Solid State Circuit Conference, 832 - 841, 2006

[39] Hee-Cheol Choi, Young-Ju Kim, Si-Wook Yoo, Sun-Young Hwang, and Seung-Hoon Lee, "A Programmable 0.8-V 10-bit 60-MS/s 19.2-mW 0.13-um CMOS ADC Operating Down to 0.5 V," IEEE Transactions on Circuits and Systems II, 55, 4, 319 - 323, 2008

[40] Shan Jiang, Manh Anh Do, Kiat Seng Yeo and Wei Meng Lim, "An 8-bit 200-MSample/s Pipelined ADC With Mixed-Mode Front-End S/H Circuit," IEEE Transactions on and Systems I, 55, 6, 1430 - 1440, 2008

[41] Byung-Geun Lee and Robin M. Tsang, "A 10-bit 50 MS/s Pipelined ADC with Capacitor- Sharing and Variable-g_m Opamp," IEEE Journal of Solid State Circuits, 44, 883 - 890, 2009

[42] B. Sahoo and B. Razavi, "A 12-bit 200 MHz CMOS ADC," IEEE Journal of Solid State Circuits, 44, 2366–2380, 2009

[43] Ashutosh Verma and B. Razavi, "A 10-bit 500-MS/s 55mW CMOS ADC," IEEE Journal of Solid State Circuits, 44, 3039–2380, 2009.

[44] Sahel Abdinia and Mohammad Yavari, "A New Architecture for Low-Power High-Speed Pipelined ADCs Using Double-Sampling and Opamp-Sharing Techniques," 16th IEEE International Conference on Electronics Circuits and Systems, 395 - 398, 2009.

[45] Fei Pei, Honghui Deng and Yongsheng Yin, "Design of Power Scaleable MDAC in High Performance Pipelined ADC," International Conference on Anti-Counterfeiting Security and Identification in Communication, 108 - 111, 2010.

[46] Chun-Ying Chen, Jiangfeng Wu, Juo-Jung Hung, Tianwei Li, Wenbo Liu and Wei-Ta Shih "A 12-Bit 3 GS/s Pipeline ADC With 0.4 mm^2 and 500 mW in 40 nm Digital CMOS," IEEE Journal of Solid State Circuits, 47, 1013 - 1021, 2012.

[47] Longxing Shi, Wei Zhao, Jianhui Wu and Chao Chen, "Digital Background Calibration Techniques for Pipelined ADC Based on Comparator Dithering," IEEE Transactions on - Circuits and Systems II: Express Briefs, 59, 239–243, 2012.

[48] Sunghyuk Lee, A.P. Chandrakasan and H. S. Lee, "A 12 b 5-to-50 MS/s 0.5-to-1 V Voltage Scalable Zero-Crossing Based Pipelined ADC," IEEE Journal of Solid State Circuits, 47, 1603 - 1614, 2012

[49] J. K.R Kim and B. Murmann, "A 12-b, 30-MS/s, 2.95-mW Pipelined ADC Using Single-Stage Class-AB Amplifiers and Deterministic Background Calibration," IEEE Journal of Solid State Circuits, 47, 1 – 11, 2012

[50] S.Y. Chuang and T.L. Scualley, "A Digitally Self-Calibrating 14-bit 10-MHz CMOS Pipelined A/D Converter," IEEE Journal of Solid-State Circuits, 37, 674-683, 2002

[51] A.N Karanicolas, H. S. Lee, and K.L. Barcrania, "A 15-b 1-Msample/s Digitally Self-Calibrated Pipeline ADC," IEEE Journal of Solid-State Circuits, 28, 1207-1215, 1993

[52] H. S. Lee, "A 12-b 600 ks/s Digitally Self-Calibrated Pipelined Algorithmic ADC," IEEE Journal of Solid-State Circuits, 29, 509-515, 1994

[53] Y. M. Lin, B. Kim and P. R. Gray, "A 13-b 2.5 MHz Self Calibrated Pipelined A/D Converter in 3-um CMOS," IEEE Journal of Solid-State Circuits, 26, 628-636, 1991

[54] A. Delic-Ibukic and D.M. Hummels, "Continuous Digital Calibration of Pipelined A/D Converters," IEEE Transactions on Instrumentation and Measurement, 55, 1175-1185, 2006

[55] J. P. Keane, P. J. Hurst, and S. H. Lewis, "Background Interstage Gain Calibration Technique for Pipelined ADC," IEEE Transactions on Circuits and Systems-I:Regular Papers, 52, 32-43, 2005

[56] D. L. Shen, and T.C. Lee, "A Linear-Approximation Technique for Digitally-Calibrated Pipelined A/D Converter," in proceedings of the 2005 IEEE International Symposium on Circuits and Systems in Kobe, Japan, 1382-1385, 2005

[57] W.Sansen, "Distortion in Elementary Transistor Circuits," IEEE Transactions on Circuits and Systems - II: Analog and Digital Signal Processing, 46, 315-325, 1999

[58] J.C. Lin and J. H. Nevin, "A Modified Time-Domain Model for non-linear analysis of an Operational Amplifeir," IEEE Journal of Solid-State Circuits, 21, 478-483, 1986

[59] A. A. Hamoui, T. Alhajj and M. Taherzadeh-Sani, "Behavioral Modeling of Opamp Gain and Dynamic Effects for Power Optimization of Delta-Sigma Modulators and Pipelined ADCs," in proceedings of the 2006 International Symposium on Low Power Electronics and Design in Tegernsee, Germany, 330-333, 2006

[60] W. M. C Sansen, H. Qiuting, and K. A. I. Halonen, "Transient Analysis of Charge Transfer in SC Filters—Gain Error and Distortion," IEEE Journal of Solid-State Circuits, 22, 268-276, 1987

[61] D. L. Shen and Tai-C. Lee, "A 6-bit 800MS/s Pipelined A/D Converter with Open-Loop Amplifiers," IEEE Journal of Solid-State Circuits, 42, 258 – 268, 2007.

[62] J. Shen and P. R. Kinget, "Current-Charge-Pump Residue Amplification for Ultra Low-Power Pipelined ADCs," IEEE Transaction on Circuit and System-II: Express Briefs, 58, 412-416, 2011

[63] H. Yoshizawa, H. Yunteng, P. F. Jr. Ferguson and G. C. Temes, "MOSFET only Switched capacitor circuits in Digital CMOS technology," IEEE Journal of Solid-State Circuits, 34, 734-747, 1999

[64] H. Yoshizaawa and G. C. Temes, "High-linearity Switched capacitor circuits in Digital CMOS technology," Proceedings of IEEE International Symposium on Circuits and Systems, 2, 1029-1032, 1995

[65] H. Charkhar, A. Asadi, and R. Lotfi, "A 1.8V, 10-bit, 40MS/s MOSFET-only Pipeline Analog-to-Digital Converter," Proceedings of IEEE International Symposium on Circuits and Systems, 5363-5366, 2006

[66] H. Aminzadeh, ”MOSFET only pipeline analogue-to-digital converters: non-linearity compensation by digital calibration,” International Journal of Electronics, 101, 158-173, 2014

[67] A. T. Behr, M. C. Schneider, F. S. Noceti and C. G. Montoro, “Harmonic Distortion Caused by Capacitors Implemented with MOSFET Gates,” IEEE Journal of Solid-State Circuits, 27, 1470-1475, 1992

[68] K. Leelavattananon, C. Toumazou and J. B. Hughes, “Linearity Enhancement Technique for MOSFET only SC Circuits,” Proceedings of the IEEE International Symposium on Circuits and Systems, 5, 453-456, 2000

[69] J. L. McCreary, “Matching properties, and voltage and temperature dependence of MOS capacitors,” IEEE Journal of Solid-State Circuits, 16, 608-616, 1981

[70] Anil Singh and Alpana Agarwal, ”Charge pump based MOSFET-only 1.5-bit Pipelined ADC stage in Digital CMOS technology,” accepted for publication in International Journal of Electronics, 2016

[71] T. Sundstrom, B. Murmann and C. Svensson, “Power Dissipation Bounds for High Speed Nyquist Analog-to-Digital Converters,” IEEE Transactions on Circuits and Systems- I:Regular Papers, 56, 509-518, 2009

[72] K. R. Laker and W. M. Sansen, “Design of Analog Integrated Circuits and Systems,” 1st ed. McGraw-Hill, 1994

[73] J. Kim, S. Limotyrakis, and C. K. Yang, “Multilevel Power Optimization of Pipelined A/D Converters,” IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 19, 832-845, 2011

[74] S. C. Bose, V. Sunitha and Chandra Shekhar, “Design Synthesis of CMOS Operational Amplifiers from User Specifications,” 5th VLSI Design and Test (VDAT) Workshop, Bangalore, August, 2001

[75] R. Schreier, J. Silva, J. Steensgaard and G. C. Temes, “Design-Oriented Estimation of Thermal Noise in Switched-Capacitor Circuits,” IEEE Transactions on Circuits and Systems-I: Regular Papers, 52, 2358-2368, 2005

[76] D. A. Johns and K. Martin, “Analog Integrated Circuit Design,” New Jersey, John Wiley & Sons Inc, 1996

[77] Z. Liren, L. Lei, Y. Fan, X. Jun and R. Junyan, "A 12-bit 100 MS/s pipelined ADC with digital background calibration," Journal of Semiconductors, 30, 115007-(1-5), 2009

[78] N. Sun, H. S. Lee and D. Ham, "Digital Background Calibration in Pipelined ADCs Using Commutated Feedback Capacitor Switching," IEEE Transaction on Circuit and System-II: Express Briefs, 55, 877-881, 2008

[79] Un-Ku Moon and B. S. Song, "Background Digital Calibration Techniques for Pipelined ADC's," IEEE Transaction on Circuit and System-II: Analog and Digital Signal Processing, 44, 102-109, 1997

[80] S. Kexu, & H. Lenian, "A fast combination calibration of foreground and background for pipelined ADCs," Journal of Semiconductors, 33, 065007-(1-11), 2012

[81] J. Yuan, , S. W. Fung, K. Y. Chan, and R. Xu, "A 12-Bit 20 MS/s 56.3 mW Pipelined ADC With Interpolation-Based Nonlinear Calibration," IEEE Transactions on Circuits and Systems I: Regular Papers, 59, 555–565, 2012

[82] Anil Singh and Alpana Agarwal, "Digital Background Calibration of Charge Pump based Pipelined ADC," accepted for publication in International Journal of Electronics Letters, 2016

[83] T. Cheongyuen, C. Yun , J. Vanderhaegen, S. Hoyos, C. Chen, R. Brodersen and B. Nikolic, "Background ADC calibration in digital domain," Proc. IEEE Custom Integrated Circuits Conference, San Jose, CA, pp. 301-304, 2008

[84] S. S. Haykin, "Adaptive Filter Theory," 3rd ed. New Jersey, USA, Prentice-Hall, 1996

[85] J. B. Foley and F. M. Boland, "Comparison between Steepest Descent and LMS Algorithms in Adaptive filters," IEE Proceeding-F Communications, Radar and Signal Processing, 134, 283 -289, 1987

[86] F. M. Boland and J. B. Foley, "Stochastic convergence of the LMS algorithm in adaptive systems", Elsevier – Signal Processing, 13, 339 – 352, 1987

[87] Eid El-Sayed and H. El-Dib, "Design of an 8-bit Pipelined ADC with Lower than 0.5 LSB DNL and INL without Calibration", 4th International Design and Test Workshop (IDT), 1 – 6, 15-17 Nov. 2009

[88] Pragya Varshney , Maneesha Gupta and G.S. Visweswaran**, "**Implementation of switched capacitor fractional order differentiator (PD^{δ}) circuit", International Journal of Electronics, 95, 531-547, 2008

[89] S. C. Bose, S. Srivastava, Chandra Shekhar and W. S. Khokle, "Review of MOS Models for Use in Computer Aided Design (Circuit Simulation) of LSI Circuits," IETE Technical Review, 3, 1986

[90] Kanhu Ch Behera, M. Santosh, S. C. Bose**, "**A low-power 12-bit SAR ADC for remote pressure measurement", Analog Integrated Circuits & Signal Processing, 86, 99-114, 2016

[91] Balaji Jayaraman and Navakanta Bhat, "Performance Analysis of Subthreshold Cascode Current Mirror in 130 nm CMOS Technology" Journal of Low Power Electronics, 5, 484-496, 2009

[92] M. J. Burke and D. T. Gleeson, "A Micropower Dry-Electrode ECG Preamplifier", IEEE Transactions on Biomedical Engineering, 47, 155-162, 2000

[93] Y.C Jenq, "Measuring harmonic distortion and noise floor of an A/D convertor using spectral averaging" IEEE International Symposium on Circuits and Systems, 3, 2569 – 2572, 7-9 Jun. 1988

[94] Hui Pan and A. A. Abidi, "Spectral spurs due to quantization in Nyquist ADCs", IEEE Transactions on Circuits and Systems I: Regular Papers, 51, 1422 - 1439, 2004

[95] H. Mendonca Sousa, J. Machado da Silva and J. S. Matos, "Computing ADC harmonic content from a reduced number of values" Proceedings of the 20th Instrumentation and Measurement Technology Conference, 2, 1217 – 1220, 20-22 May 2003

[96] Christen, T. "A 15-bit 140-W Scalable-Bandwidth Inverter-Based Modulator for a MEMS Microphone With Digital Output," IEEE Journal of Solid-State Circuits, 48, 1605 – 1614, 2013

LIST OF PUBLICATIONS

SCI Journals

1. Anil Singh and Alpana Agarwal, “Charge pump-based MOSFET-only 1.5-bit pipelined ADC stage *in* digital CMOS Technology,” International Journal of Electronics, Vol. 103, 10, pp - 1713-1725, 2016.
2. Anil Singh and Alpana Agarwal, “Power and Area efficient Pipelined ADC stage in Digital CMOS technology,” (accepted for publication), IETE-Technical Review, 2016, doi: 10.1080/02564602.2016.1142396
3. Anil Singh and Alpana Agarwal, “Digital Background Calibration of Charge Pump based Pipelined ADC,” International Journal of Electronics, Vol. 103, 11, pp - 1941-1953, 2016.

Conference

Anil Singh and Alpana Agarwal, "Modeling Errors in Pipelined ADC using Matlab ", 3rd National Conference on Advances in Metrology (AdMet –2014), 21-22nd Feb.,2014, Thapar University, Patiala, Punjab.