GENAI POWERED DESIGN VERIFICATION

A Thesis submitted in partial fulfillment of the requirement for the Award of the Degree of

MASTER OF TECHNOLOGY

VLSI Design

Submitted By:

VARSHA SINGH

602362040

Under Supervision of

Dr. Rahul Upadhyay
Associate Professor

Dr. Geetanjali Chandwani
Assistant professor

THAPAR INSTITUTE
OF ENGINEERING & TECHNOLOGY
(Deemed to be University)

ELECTRONICS AND COMMUNICATION ENGINEERING DEPARTMENT

THAPAR INSTITUTE OF ENGINEERING &
TECHNOLOGY, PATIALA, PUNJAB

JULY, 2025

DECLARATION

I, **Varsha Singh** hereby declare that the work presented in this thesis entitled "**GenAI Powered Design Verification"** in partial fulfillment of the requirement for the award of degree of **Master of Technology (VLSI Design**) submitted at **Electronics and Communication Engineering** , Thapar Institute of Engineering & Technology (Deemed to be University), Patiala is an authentic record of work carried out under supervision of **Dr. Rahul Upadhyay** (**Associate Professor, Electronics and Communication Engineering, Thapar Institute of Engineering and Technology**) from **August 2024** to **June 2025**. The matter presented in this has not been submitted either in part or full to any other university or institute for the award of any other degree.

Varsha Singh
602362040

Date : 15.07.25

Dr.Rahul Upadhyay
Associate Professor
DECE
TIET,Patiala
Punjab

Dr. Geetanjali Chandwani
Assistant Professor
DECE
TIET,Patiala
Punjab

CERTIFICATE

Industry Mentor-Certificate (For Industry Internship)

Qualcomm

QUALCOMM India Private Limited

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DLF Centre, 3rd Floor,
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India

www.qualcomm.com.in

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This is to certify that Varsha Singh worked as an Interim Engineering Intern at Qualcomm from 21st August 2024 to 27th June 2025

Varsha's performance, behavior, and conduct remains good during the internship.

We wish her all the best for her future endeavors.

27th June 2025

Date

Aarathi Kumar

Director Staffing

Other offices:
Mumbai: Unit no. 1102, Platina Building, G Block 11th Floor, Plot # C-59, Bandra Kurla Complex, Mumbai, India 400051 India. Tel: +91-22-67041400; Fax: +91-22-67041500
Hyderabad: 5th Floor, Bldg # 8 Mindspace, Hitec City, Madhapur, Hyderabad, 500 081, Andhra Pradesh, India. Tel: 91-40-3011-0000; Fax: 91-40-3011-0001
Bangalore: Plot no. 125-127, EPIP IInd Phase, Whitefield, Bangalore, Karnataka 560 066, India. Tel: 91-80-3984-1800; Fax: 91-80-3984-2001

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ABSTRACT

In nowadays changing semiconductor industry, precision is very important for designers, verification engineers, and layout professionals. Due to the high costs and tight schedules involved in chip design, verification, and fabrication, achieving success in first time is important. But this level of accuracy is difficult to get and without a well defined methodology guiding the entire ASIC development process is difficult. Without skilled engineers, rtl design engineers the success in this semiconductor industry is very tough.

The increasing design complexity is one of the most major challenge in semiconductor industry nowadays. Many traditional approaches are there but they are very much time taking and inefficient. Compared to the, Artificial Intelligence provides automated and vast number of solutions by reducing manual efforts. After the arrival of GENAI driven techniques, verification process has been made easier and lots of manual efforts have been reduced. This change in semiconductor industry not only increases the verification abilities of engineers but also reduces time required in overall manufacturing cycle to a great extent.

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CHAPTER 1
INTRODUCTION

The rapidly increasing involvement of Artificial Intelligence in manufacturing processes is providing very huge advancements in the semiconductor industry. Generative Artificial Intelligence(GenAI) is among one of the various AI techniques that is concerned about the generation of new data, designs and insights based on the learned patterns and now is emerging as a powerful tool in advanced manufacturing [1] . This emerging technology is using many new models like Generative Adversarial Networks(GANS) and Large Language Models(LLMS) who have the potential to revolutionize various aspects of the manufacturing process which include from product design and prototyping to process optimization and predictive maintenance. The semiconductor industry at this point of time is affected by the relentless demand for a very high performance, lower consumption and increased functionality of all the electronic devices [2]. In Figure 1.1-1, the integration of semiconductor with GenAI is shown which indicates towards an efficient and automated workflow.

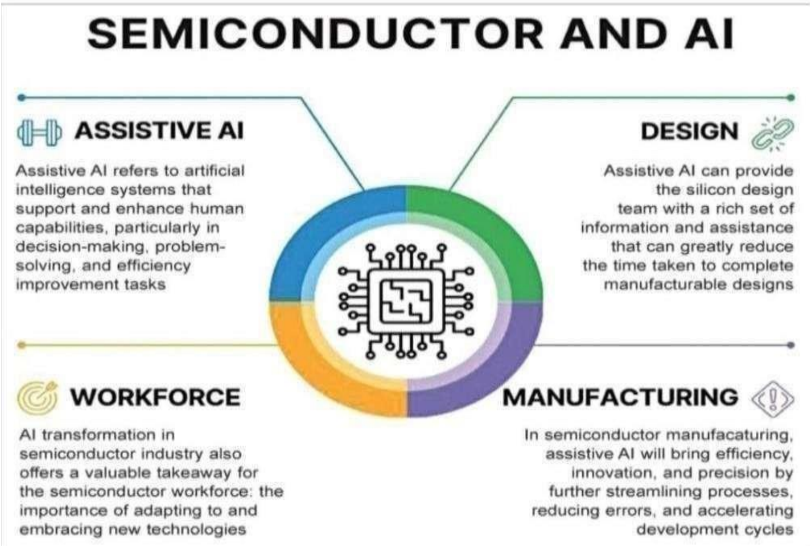

Figure 1.1-1 AI in semiconductor design [2]

As the complexity in semiconductor industry is increasing nowadays the intricacy of the corresponding manufacturing system intensifies. These elaborating systems make it necessary for engineering experts for effective operations and analysis of any semiconductor product [3].

The semiconductor business is a very huge force behind the innovation in technology and artificial intelligence has the capacity to drastically cut costs, improve the quality of manufacturing and improve the product quality by decreasing the faults and making the best use of the materials [4].

This integration of artificial intelligence in the semiconductor industry, makes artificial intelligence to generate ethical and rational responses based on a broad understanding of language, knowledge, and concepts. It's as if you have someone by your side who knows everything and is ready to always assist you [5].

Generative Artificial Intelligence which is also called known as GenAI, is a kind of artificial intelligence which we can say is can create various kinds of contents lik e texts, conversations, stories, images and music. It can make us learn about different topics in the world like languages, programming, music, art, science and many more and use this knowledge to solve new problems. It is a transformative force which redefines the landscape of VLSI and semiconductor manufacturing. The integration of AI techniques like Machine Learning and Deep Learning are offering unparalleled opportunities to address persistent challenges in the variability of processes [6] . In Figure 1.1-2, it is shown that how AI-driven techniques have proven to outperform traditional methods in terms of accuracy, scalability and cost efficiency.

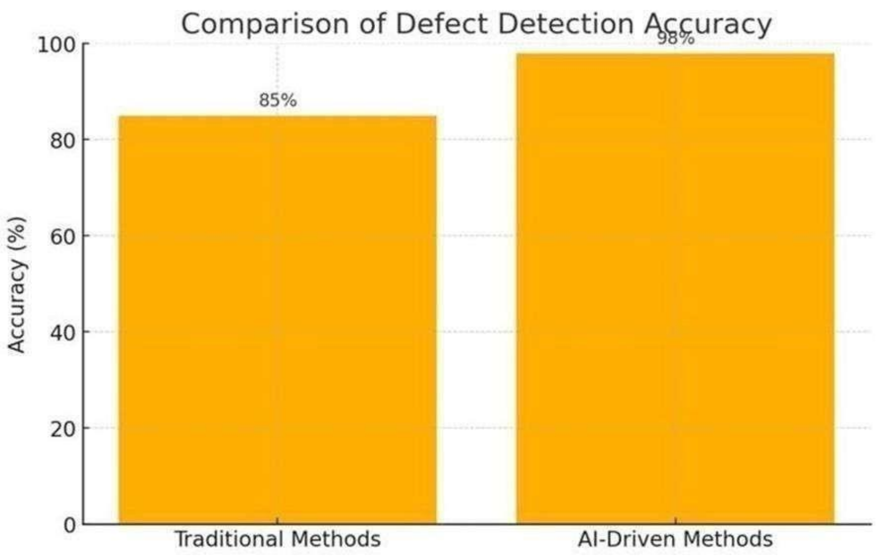

Figure 1.1-2 Comparison of Defect Detection Accuracy [6]

1.1 USES OF GENAI IN SEMICONDUCTOR DESIGN

1.1.1 SIGNIFICANCE OF GENAI IN SEMICONDUCTOR INDUSTRY

The introduction of generative AI and semiconductor technology have done a huge shift with huge advantages for both industry and whole world's economy. GenAI has become one of the mot transformative technologies in modern manufacturing by offering capabilities that go beyond the the traditional techniques. While classical AI models are mostly aligned towards with the prediction and classification, generative models are designed to create the new instances like designs or materials or production schedules that meet most of the goals [7].

Generative AI usually works on the principles of learning patterns which they take from large datasets and by making use of these learning patterns they create some new datasets that resemble the original distribution. The primary types of generative models are GANs, VAEs and Transformer based models which are defined as follows:

i. GANs: GANs consists of two competing networks which are a generator and a discriminator. The role of the generator is to produce the new data instances and the role of the discriminator is to evaluate whether the data is real or generated. This relationship between generator and driver tends the generator to create t he realistic outputs. In semiconductor manufacturing nowadays, GANs are being used to generate new product designs, simulate manufacturing processes and create synthetic datasets for process optimization [7].

ii. VAEs: VAEs are another class of generative models that use probabilistic techniques to learn a compressed representation of of inputs which are sampled to generate new datasets. They are mainly used for tasks that involve creating variations of a design. VAEs can help reduce material waste and improve energy efficiency during production by allowing manufacturers to efficiently explore design trade-offs [7].

iii. Transformer Based Models: Transformer Based Models are mostly used in generative tasks such as time-series forecasting or generating optimized manufacturing schedules. These models are learning from the dependencies across the design steps by making them ideal for dynamic applications like supply chain management [7].

The largest boost which is credited to artificial intelligence is in the field of research and chip design. The most crucial and sensitive parts of chip design are physical layout and verification but by the process of cutting down labour costs and time to market by fully automating these processes, even for analog designs. In Figure 1.1-3 it is shown that semiconductor companies are already getting huge benefits from the use of artificial intelligence. The benefits are introducing the cost cutting into the physical design and verification process which is used by the artificial intelligence in the field on chip design and manufacturing [8].

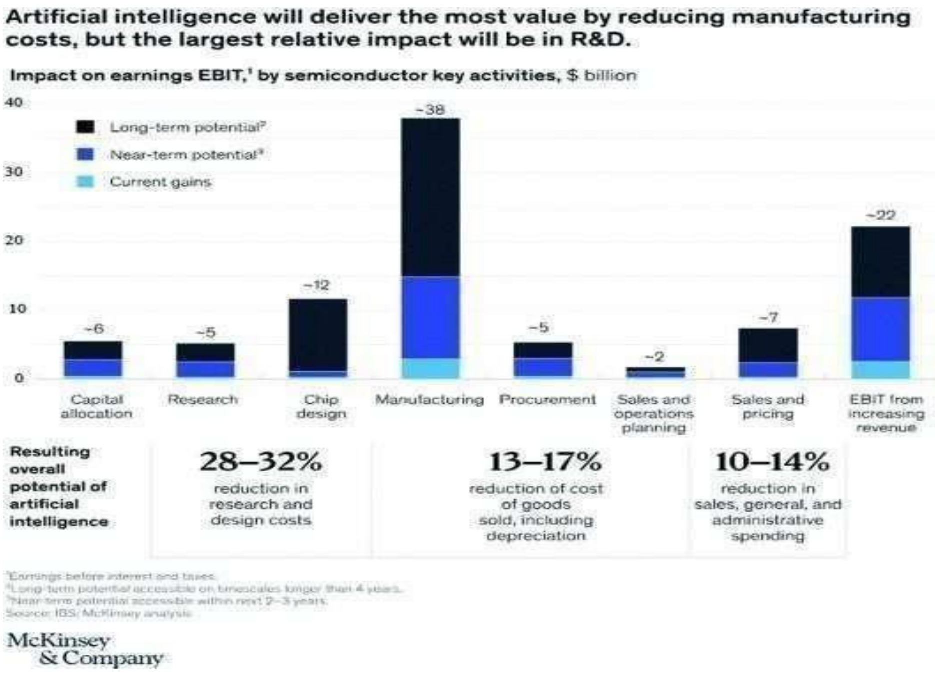

Figure 1.1-3 Benefits from AI [8]

The evolving impact of GENAI in the semiconductor industry in today's world is very far beyond the level chip design and manufacturing process. It will create many new opportunities for marketing for retailers and also market people as they will be nowadays by the help of GenAI are getting a very large profit compared to the software side from technology point of view.

As seen by a very good businessman's angle, semiconductor industry in today's world is playing a very big role in business sector but also by introducing many updated technologies in compute, memory, storage, and networking. This change introduced by GENAI is providing more variety in different product models and robust business model that is giving them position of enabling something new in semiconductor market.

As seen by a very good economist's angle, the addition of GENAI into the semiconductor industry is giving very good results we can say it is giving the ability to increase huge economic growth by creating new business opportunities and enhancing productivity. Nowadays the increase in demand for GENAI-optimized semiconductors is indicating more towards the research and development and also to facilities, and human resources. This is known to create a very large impact in global economic output and prosperity of country.

We can say that the economic benefits of GENAI integration are not without difficulties. For getting the full advantage of GENAI, semiconductor companies should understand the need to investigate complexities of data privacy. However, the process of managing the change of an economy driven by GENAI requires a careful balance which makes sure that the benefits of GENAI are widely distributed to each member of economy and that potential displacement of workers due to automation should be taken into consideration.

1.1.2 CHANGING ROLE OF GENAI IN SEMICONDCUTOR INDUSTRY

Due to the rise of machine learning and artificial intelligence the semiconductor industry is now going through a new process by how it is now going to approach the manufacturing. Advanced machine learning and artificial intelligence are offering manufacturers to optimize the testing processes and achieve a very high level of cost effectiveness. Machine learning can be trained to identify the different patterns and the relationships between various datasets which makes them capable to analyze the vast amount of data that are generated during the process of semiconductor manufacturing and testing [9]. ML and AI solutions are highly beneficial by using data collected on the field to monitor the operating conditions of production equipment and optimize the operation scheduling in a way that is aware of ongoing processes. Tools like Synopsys DSO. GenAI™ are playing a big role in enhancing this transformation and making people realize that how AI can improve our lives in every phase.

1.1.3 APPLICATION OF GENAI IN AUTOMATION

Automation Engineering is mainly concerned on developing systems that require very little interference from the human beings or outside world. It works by integrating most of the advanced technologies related to the fields of robotics, control systems, sensors and very large softwares to gain the efficiency, precision and safety in the various industrial processes. GenAI makes automation engineering very highly efficient in the field of designing and verification of the semiconductor chips. With very large databases generative models can do the optimization of various semiconductor designs and they select the best ones for components and systems and hence they do the acceleration of prototyping process and hence by reducing time to market and ensuring overall system performance [10].

1.1.4 MANUFACTURING WORKFLOW WITH GENAI

In Figure 1.1-4, the optimization of workflow through the process using the techniques of artificial intelligence is given. Many manufacturers work under the pressure to improve the production processes, optimize the supply chains, deliver the high quality products to the clients and adjusting to the dynamic market changes. To make these difficulties easy, the implementation of artificial intelligence becomes very much tempting and facilitates highly efficient and interconnected operations done in the industry [11].

Figure 1.1-4 Artificial Intelligence Product Development [11]

1.1.5 GENAI ROLE IN SEMICONDUCTOR MANUFACTURING

GenAI has performed a very huge role in the enhancement of semiconductor manufacturing processes through the techniques of defect classification, anomaly detection, predictive maintenance and simulation [12].

For the complex processes like defect classification and anomaly detection, generative AI models can be trained on the huge datasets of semiconductor wafer images to learn the normal patterns of images and identify the deviations from these patterns. That is how when any new image comes into the picture then these models can analyze the new images and detect if any probability of occurrence of error is there. These models are highly accurate. Generative Adversarial Networks are very much trustful because of their ability to generate synthetic defect images to augment training data. This process makes artificial intelligence to learn to recognize a variety of defects which includes rare ones also [12].

i. Generative artificial intelligence models can also be used in simulating and optimizing the semiconductor manufacturing process. By the process of creating digital twins of production lines, these models can run the thousands of virtual experiments to identify the optimal process parameters, test new designs and remove issues without disturbing the actual production of the chips. We can take example of how generative artificial intelligence model can simulate how changes in temperature, pressure or chemical concentration might affect the wafer quality of the chip when it is being fabricated in the lab, making engineers to correct processes virtually before implementing changes in the actual chip [12].

ii. Furthermore, generative artificial intelligence can help in chip design by automatically generating and evaluating the physical layouts of the designs that are being manufactured. This can speed up the design process to a very big extent and making the huge chip architectures very much efficient. Artificial Intelligence can go through a process of iterating through countless design variations and factors such as power consumption, heat consumption and performance [12].

1.2 WORKING OF GENAI

1. **Training:** This phase consists of creation of a foundation model which is typically a large language model(LLM) for text generation, by training a deep learning model on a large amount of raw, unstructured data. The model learns the ability to predict the next element which is present in the sequence. It does this by performing millions of ‘fill in the blanks’ exercises.

2. **Tuning:** The foundation model is after that fine-tuned for specific tasks by feeding the labeled data relevant to the specific application. This process can contain reinforcement learning with human feedback(RLHF), where the human beings evaluate the generated content to improve the accuracy.

3. **Generation:** The tuned model generates new content based on user inputs. Develop and users continuously try to assess and refine the model’s outputs to enhance quality.

1.3 CHALLENGES WITH GENAI

Given below are the four very important limitations of artificial intelligence that as per our point of view represents a large number of restrictions for the practical use. The following limitations are technical in nature as they tell us the way in which generative artificial intelligence models draw conclusions as they are model-specific. This means that very long term limitations are known to exist with repercussions at the system and application levels.

i. Results with errors

Generative artificial intelligence models can provide errors in the results. This might be due to the result producing characteristic of machine learning models which highly depend on the probilistic methods to draw the conclusions. For example, generative artificial intelligence can provide the most likely answer given by a prompt but it may or may not be the correct one. In this way many difficulties can occur since many people can assume this wrong material to be the right material and can assume that results are correct [13].

ii. Environmental Issues

The application and development of generative artificial intelligence systems can give rise to serious environmental issues because they are usually based on very large scale neural networks which have a huge negative carbon footprint during development and operation. Due to this various attempts are being made in research related to the artificial intelligence to build and implement artificial intelligence methods in a such a way that is less harmful to the environment via the use of more effective training algorithms, smaller neural network topologies and better hardware [13].

1.4 FUTURE OF GENAI

The following are some of the uses of generative artificial intelligence in the electronics industry:

i. Optimizing Automated Circuit Design

Creation of generative artificial intelligence algorithms that can be used for designing and optimization of electrical circuits while considering other factors like manufacturability, power consumption, area and performance into account. This includes combining artificial intelligence methods with genetic algorithms to effectively explore the large design space and provide the best circuit designs.

ii. Self-Healing Electronics

GenAI can used to develop self-healing electrical systems which can identify and solve their problems on their own. Artificial Intelligence approach can introduce real -time monitoring and decision making of electronic systems to ensure their life dependency.

iii. Energy-Efficient Hardware Design

GenAI techniques can be used to optimize hardware structure of all the electrical devices for maximum energy efficiency. This requires using artificial intelligence approaches to forecast energy usage and performance trade-offs and genetic algorithms to investigate various design configurations.

CHAPTER 2
LITERATURE SURVEY

In this chapter, the difference between artificial intelligence and traditional methods are highlighted. In this chapter, we will discuss the various methodologies and changes in GENAI implementation from history till now. From the analysis of the literature, we shall conclude the proper methodology for the implementation of Artificial Intelligence.

2.1 INTRODUCTION TO LITERATURE SURVEY

The semiconductor sector has long employed very complicated automation systems, particularly for huge standardized and repetitive operations. However, evolving requirements are including manufacturing flexibility demands, produ ct a diversification, operational complexity, and the shift toward autonomous systems with enhanced human-machine collaboration which have accelerated GENAI adoption across a huge production environment.

These advanced solutions are now being implemented in throughout the product lifecycle, from digital product definition and knowledge-based risk evaluation to visual inspection systems for defect identification in both front -end and back-end processes, along with briefly occurring detection across manufacturing sequences.

Recent advances nowadays in deep learning and machine learning methodologies have enhanced semiconductor research initiatives by providing powerful tools to manage the growing complexity of manufacturing nodes and by the expanding array of process control parameters. The concluding portion presents four innovative applications which demonstrates GENAI implementation and focusing on practical deployments of computer vision systems and neural network architectures within semiconductor fabrication workflows [13].

In today's world, Generative AI has become a trusted best friend for humans beings and working alongside with us to achieve incredible things. Imagine a painter creating a masterpiece, while they focus on the vision, Generative AI nowadays acts as their assistant, mixing colors, suggesting designs, or even sketching ideas, as in the painter remains in control, but the AI makes the process faster and more exciting to paint.

2.2 DIFFERENCE BETWEEN AI AND TRADITIONAL METHODS:

The working capabilities and usage of intelligent systems have gone through the major changes due to the introduction of artificial intelligence. Traditional artificial intelligence methods focus mostly on embedding explicit human knowledge to solve a particular kind of a problem. It was done through a set of rule based systems and expert systems.

In comparison to that, current artificial intelligence techniques focus on knowledge acquisition from data to learn, adapt and execute very complicated tasks. This is done by the improvements done in the methods through machine learning and deep learning. Traditional artificial intelligence which was distinguished by many expert systems, which always display human skills in specialized behavior like in medical and in automation field. But these systems were struggling with different kind of complexities and could not generate anything beyond a given set of rules which they were given when they are created. Modern methods of artificial intelligence have introduced a huge change by using methodologies that are data- driven to improve the intelligence of the systems [14]

Due to its various advantages over conventional research methodologies, artificial intelligence is now being applied to a various number of study disciplines. Using the process of evaluation of data of a student and suggesting activities, artificial intelligence can trailor learning experiences in the classroom. Artificial intelligence, in particular neural networks has been shown to perform better in many fields in comparison to the traditional methods. Recurrent neural networks have surpassed the traditional techniques in the prediction of conditional volatility. Forecasting ability was increased to a greater extent by the introduction of Khashei & Bijari’s hybrid model which combined auto- regressive integrated moving average(ARIMA) methods with the artificial neural networks.

As shown in the below Figure 2.1-1, more than half of the people are using artificial intelligence based tools for more detailed research of their relevant work. Artificial intelligence focuses on the organization and management of the references and the processing of synthetic information which is being used [15].

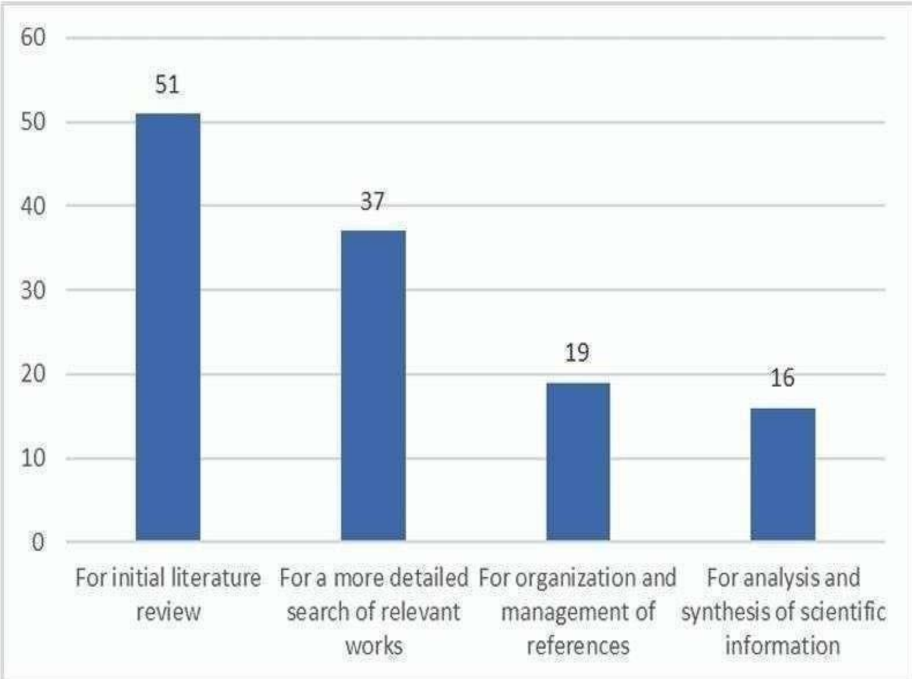

Figure 2.1-1 Academic purpose of using AI tools [15]

2.3 HISTORY OF ARTIFICIAL INTELLIGENCE

Generative AI has come a long way from its early beginnings. Here the description is given that how it has evolved over the time, step by step:

1. Early Days- Rule-Based Systems

AI followed strict rules written by the humans to produce the results. These systems can only produce results for the things only for which they were programmed for, they could not develop anything on their own. For example, we can say that a program can create various shapes but it could not develop anything on its own like a landscape.

2. Introduction of Machine Learning (1990s – 2000s)

Machine learning is a mechanism that helped AI to learn data instead of just following the rules. The AI was fed large datasets like pictures of animals and learned it to identify patterns and make predictions. For example, AI can identify dog in the picture, but it cannot create a picture of dog on its own.

3. Emergence of Deep Learning(2010s)

Deep learning has improved AI a lot by introducing the concept of neural networks, which copies the way human brain works. Using this AI can process a lot of data and generate new content. For example, AI could create new drawing s of dog by learning from the dog's photo.

4. Generative Adversarial Networks in today's world (2014)

GANs were introduced in 2014 by using two AI systems that work together one generates a new content and other checks whether it looks real or not. This made generative AI very much better at creating realistic images, videos and sounds.

5. Large Language Models (LLMs)

Models like Chat GPT-3 and Chat GPT-4 can understand and generate human like text. They are trained on massive amounts of data from books, websites and other sources. AI can now start conversations with people, write essays and can speak also. For example, ChatGPT can help you to create a poem or write an essay or story.

6. Multimodal Generative Artificial Intelligence (Present)

New AI models can handle multiple types of data at once example text, images, audio, and video. This allows AI to create content that combines different formats. For example AI can take a written description and turn it into an animated video or song by different models integrating together in a framework.

CHAPTER 3

PROBLEM STATEMENT

3.1 ABOUT BLACKBOX

A gate-level netlist presents us a visual representation of a circuit design, detailing either logic gate interconnections or transistor-level configurations. The diagram of blackbox is in Figure 3.1-1. This synthesized output which is generated from HDL code through any synthesis tools, maintains functional equivalence with its original RTL representation while undergoing many changes relating to potential structural modifications during physical implementation. The placement -and-routing (PNR) process uses this netlist to a great extent to generate the chip's physical layout in the end producing a post-layout netlist that always maintains the design's logical behavior which is actually represented in RTL design. By using these types of netlists, black box elements represent modules or components whose functionality always remain hidden for higher-level design purposes.

The reduction of elapsed time and simulation time using black boxes in a netlist offers several significant benefits:

Reduced Simulation Complexity:

1. **Abstracting Internal Details:** Black boxes now serve as abstracted representations of complex modules by hiding their internal functionality while exposing only the input and output ports. They always enable the tool just to produce outputs by hiding the internal implementation details. This architectural approach mostly decreases computational overhead during process.

2. **Simplified Models**: Abstracting design components now days through by simplifying things decreases simulation complexity. This approach creates a much more efficient management and execution of verification processes and particularly for complicated, large-scale circuit designs.

3. **Faster Simulations**: The reduction in processing requirements to a larger scale nowdays enabling significantly faster simulation cycles. This performance boost proves particularly valuable during iterative development phases which require repeated verification runs to optimize large circuit designs very effectively.

4. **Resource Efficiency**: The streamlined design approach that the industry is gained in this era through blackboxing minimizes computational requirements, reducing both memory usage and processor overload. These simultaneous gains enhances various simultaneous simulations and allow operation on less advanced hardware configurations, improving both the affordability and expandability of the entire asic design workflow.

Effective Iterations:

1. **Rapid Feedback Loop**: Enhanced simulation cycles usually create a more focused development process. Engineers can execute many tests and analyze outcomes, and implement modifications within a very less time. This expedited and large iteration cycle proves critical for design optimization and a good mechanism for early defect detection.

2. **Focused Testing:** Black box methodology enables many designers to concentrate on module interface verification rather than individual components implementation. This approach significantly improves the detection and resolution of all system -level integration challenges.

3. **Parallel Development**: Concurrent development of chips becomes possible as separate teams can focus on different design aspects simultaneously. While some engineers refine a module's internal implementation, others can perform system integration and verification using its abstracted black box model. This parallel workflow significantly accelerates all the project timelines.

. 4. **Incremental Improvements**: This development process enables progressive design enhancements of the chips through successive refinements. Each cycle usually incorporates lessons from previous implementations and systematically optimizing both functional performance and operational stability.

5. **Early Detection of Issues**: Frequent design iterations are useful in facilitating earlier identification and resolution of all potential issues. By detecting problems during initial development phases it minimizes costly late stage redesigns, optimizing both schedule and resource allocation. Through the simplified simulation requirements and enhanced iteration efficiency, black box abstraction on a very large scale improves the design verification workflows by accelerating overall development timelines.

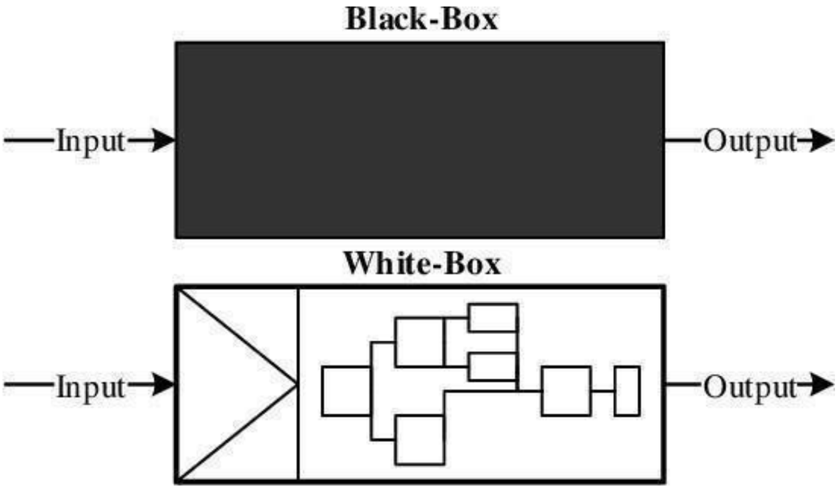

Figure 3.1-1 Representation of blackbox[16]

3.2 PROBLEM: NEED OF POWER PORTS IN BLACK BOX OF A NETLIST

Omitting power connections in black box representations may introduce simulation errors to a huge extent and cause compilation failures during design elaboration. Proper declaration and integration of these power ports is very important nowdays for achieving precise simulation outcomes and ensuring error-free implementation of the circuit.

Compilation and Elaboration Errors

The absence of power ports can also lead to compilation and elaboration errors:

i. **Unresolved References**: Omitting power connections in black box representations might introduce a very large number of simulation errors and cause compilation failures during the design elaboration. Proper declaration and integration of these power ports is very important for achieving exact simulation outcomes and ensuring error-free circuit implementation.

ii. **Incomplete Module Definitions**: Power connections nowdays contain all the essential elements of a module's interface specification. Their omission from modules creates an incomplete definition that triggers elaboration failures as of the fact the tool cannot properly instantiate or integrate the module within the hierarchical design structure.

iii. **Simulation Failure**: Undefined power connections are usually the main cause of simulation initialization failures and resulting in operational errors during runtime. These issues prove majorly challenging in diagnosing and correcting since they originate from foundational flaws in the power distribution framework.

3.3 USE OF GENAI TO INSERT POWER PORTS IN THE BLACKBOXED MODULES OF A NETLIST

As in this problem statement shown in Figure 3.1 -2 the given problem is to insert the power ports into the Verilog module of a netlist so we are using Copilot Tool for it. In the below image a prompt has been given in GenAI that says "provide a code that takes inputs starting from 'vdd' and 'vss' from one Verilog file and add them into input port declarations of another Verilog file". Here the ports starting from 'vdd' and 'vss' are the power ports and they have to be inserted into the module after it is blackboxed.

The AI will generate a python script that will be helping in the automation process by automating the task of inserting the power ports into the module so that the manual efforts of verification engineers, design engineers as well as physical design engineers can be reduced upto a great extent by allowing a lot of power ports to be inserted into the module of a Verilog file automatically instead of writing them manually.

This integration of AI into the verification industry has streamlined the verification process to a greater extent by making the jobs of the semiconductor industry very easy. This is also helping in the growth of hardware engineers as well as the software engineers. It helps in generating a millions lines of code written in any language within seconds just by giving prompts and hence enhancing the effectiveness and growth of the engineers.

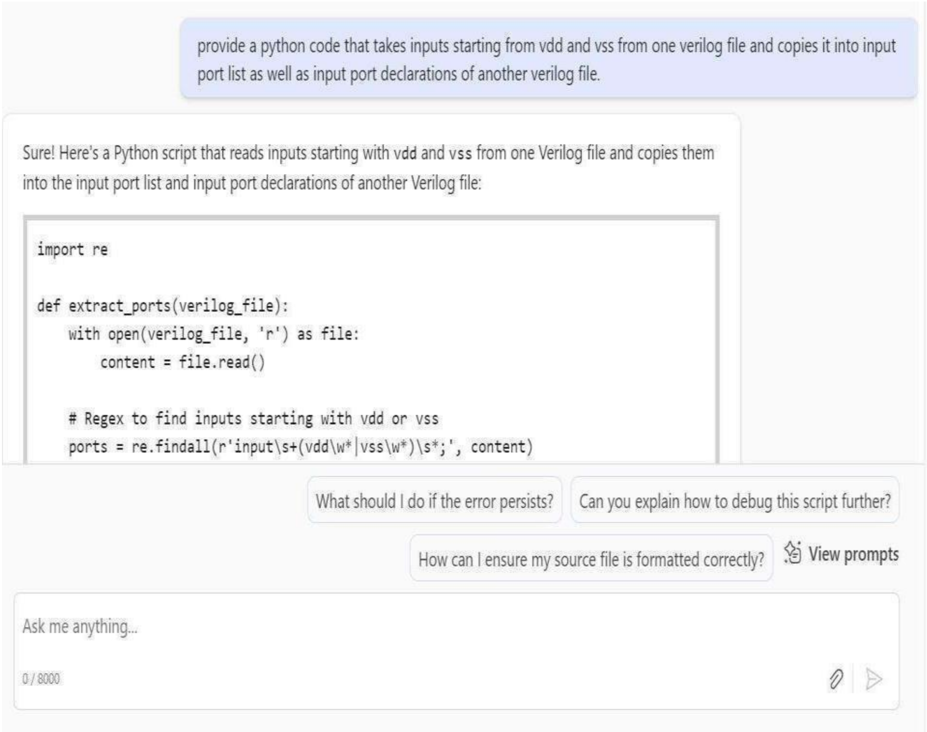

Figure 3.1-2 Prompt given to AI

GenAI is also used as a mechanism for error detection as well as error detection in any python or any other language code. The user can give the error produced while running the code as prompt and after that the GenAI can correct that error by providing a solution to that error.

In the below Figure 3.1-3 an error has been produced by running the given python script so we are providing that error as a prompt to the GenAI so that it can analyze the error and provide an error free python code that can help us to insert the power ports inside the blackboxed modules so that verification process can be easier for the verification engineers.

This error shows that how artificial intelligence can be proved to be a huge factor in making mistakes. We always cannot rely on artificial intelligence as it can also produce errorful results. If we assume it to be always right then it would be a huge harm to us.

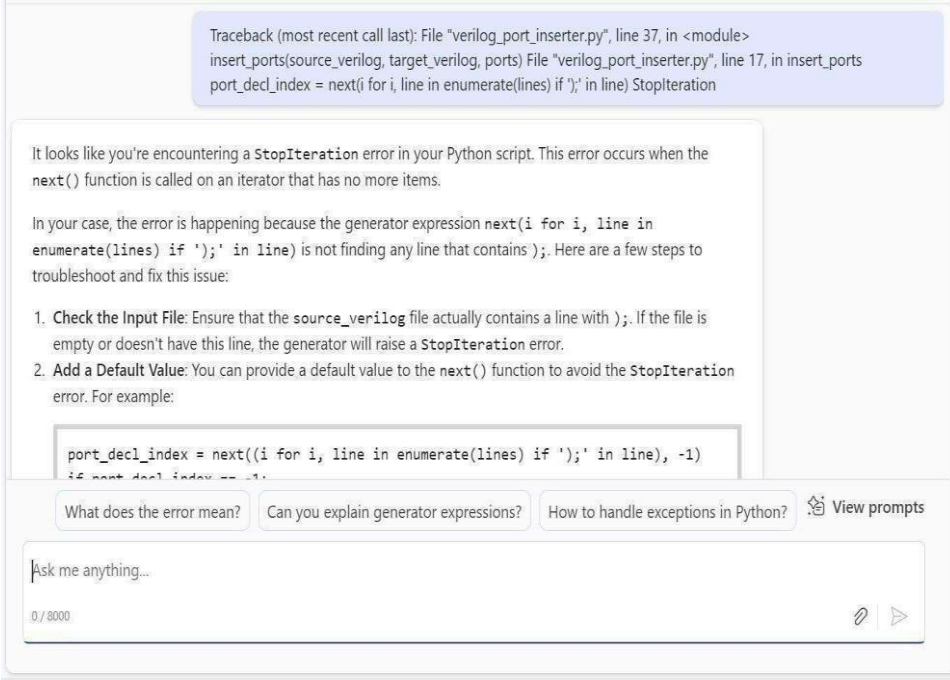

Figure 3.1-3 Error prompt given to AI

Here prompts are given to GENAI to do something for us like creating, summarizing or editing. Prompting is basically how we ask GENAI to do anything we want. Prompting basically means having a conversation with GENAI using plain but clear language so that it can understand what exactly do we want from it and provide the accurate results so that we do not have to do any further modifications. It basically saves our time and most important of all is it reduces human efforts.

CHAPTER 4

IMPLEMENTATION OF GENAI

4.1 REPRESENTATION OF CODE

In a this task,2 verilog files were provided to me, out of them one Verilog file was containing some modules which were blackboxed which means there wa s no functionality represented between the inputs and outputs of those module, it only contained the declaration of inputs and outputs without the implementation of any kind of functionality. We can say that the implementation details are hidden of this module.

While the 2nd verilog file is containing all the modules which are not blackboxed. We can say that netlist generated by that verilog file contains no blackboxed modules. So in this task we have to take the power ports which are present inside the modules which are going to get blackboxed in the second verilog file and copy them to the inputs outputs port declaration of the second verilog file.

In the below Figure 4.1-1, flowchart representation of the code is given which GENAI has done by producing a code that takes the power nets from the module before it was blackboxed and inserted into the module after it was blackboxed. The code is written in python language.

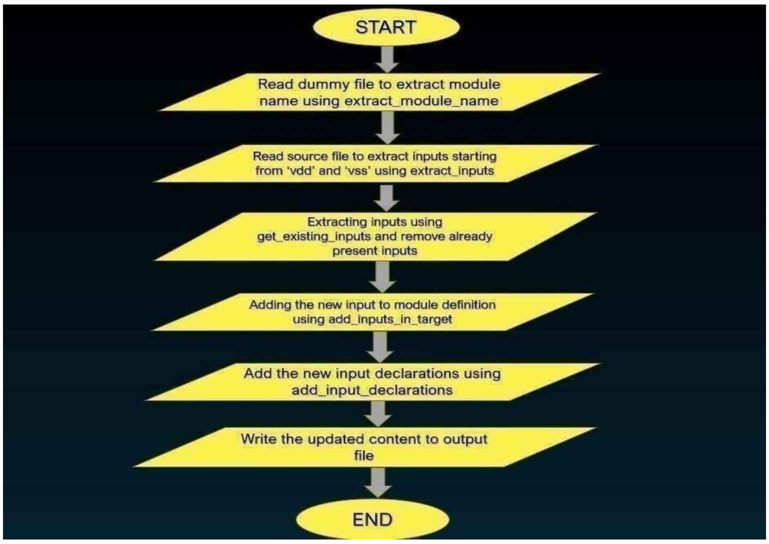

Figure 4.1-1 Flowchart of the code

Below are the screenshots of the codes which GenAI has produced by inserting the power ports into the modules after they were blackboxed. This whole script is written in python. It takes 2 verilog files and automates the task by producing a code that takes the power ports which were declared in the 1 st verilog file and copies them to the module which contains declarations of the 2nd verilog file. In this way the below code is working.

This code in Figure 4.1-2 is using python features like regular expressions by importing module re. It is also working on the file handling feature of the python. It is handling the file in read and writing mode such that power ports from the 1st verilog file can be taken and added to the input output ports declarations of the 2nd verilog file.

```python
    match = re.search(pattern, file_content, re.DOTALL)
    if match:
        # Extract existing input declarations
        existing_declarations = match.group(1).split(',')
        # Add new input declarations with each input on a new line
        updated_declarations = existing_declarations + [f'input {inp};' for inp in new_inputs]
        # Remove duplicates while preserving order
        updated_declarations = list(dict.fromkeys([decl.strip() for decl in updated_declarations]))
        # Replace the input declarations with updated declarations
        new_content = file_content[:match.start(1)] + '\n'.join(updated_declarations) + file_content[match.end(1):]
        return new_content
    return file_content

# Ensure the script is called with the correct number of arguments
if len(sys.argv) != 4:
    print("Usage: python gfx_dummy_csv.py <source_file> <target_file> <output_file>")
    sys.exit(1)

# Read the content of the dummy file to determine the module name
with open(sys.argv[2], 'r') as f:
    dummy_file_content = f.read()

module_name = extract_module_name(dummy_file_content)
if not module_name:
    print("Module name not found in the dummy file.")
    sys.exit(1)

# Read the content of the source file
with open(sys.argv[1], 'r') as f:
    source_file_content = f.read()

# Extract inputs from the source file
inputs_to_add = extract_inputs(source_file_content, module_name)

# Get existing inputs from the dummy file
existing_inputs = get_existing_inputs(dummy_file_content, module_name)

# Filter out inputs that are already present in the dummy file
inputs_to_add = [inp for inp in inputs_to_add if inp not in existing_inputs]
print(inputs_to_add)

# Add inputs in the dummy file with extracted inputs
new_dummy_file_content = add_inputs_in_target(dummy_file_content, inputs_to_add, module_name)

# Add input declarations in the dummy file with extracted inputs
new_dummy_file_content = add_input_declarations(new_dummy_file_content, inputs_to_add, module_name)

# Write the modified content back to the output file
with open(sys.argv[3], 'w') as f:
    f.write(new_dummy_file_content)

print(f"Inputs have been successfully added and declared from {sys.argv[1]} to {sys.argv[2]}.")
```

Figure 4.1-2 Snippet of the code

4.2 EXPLAINATION OF THE CODE

Step 1: 2nd file which is containing the inputs of blackbox module is opened in the read mode and using the function 'extract_module_name' which contains file name as the argument. It searches for the module name using the regular expression and the module name is extracted using extract_module_name function **.**

Step 2: 1st file is opened using the file handling operation and inputs containing power nets 'vdd' and 'vss' are extracted using extract_inputs function which is containing file_content and module_name of second file as arguments.

Step 3: Some of the inputs are already present containing 'vdd' and 'vss' they are removed using get_existing_inputs function and only those which are not present are kept. Inputs to be added are given in the list named as inputs_to_add.

Step 4: New inputs are added to the blackbox module definition using function add_inputs_in target which is containing inputs_to_add, module_name and dummy_file_content as the arguments.

Step 5: New inputs are also added to blackbox module input port declaration using function add_inputs_declarations.

4.3 IMPLEMENTATION RESULTS

Here the results which are generated by running the python script. First part of the Figure 4.1-3 contains the inputs which are presented in the 1st file means in this file the modules are not getting blackboxed and power ports are extracted from this file which are starting from 'vdd' and 'vss'.

```
input a
input b
input c
input d
input e
input f
input g
input vdd_a
input vdd_b
input vss_c
input vss_r
input vss_p
input vss_k
```

Figure 4.1-3 Inputs before the addition of power ports

Below is the list of inputs given in Figure 4.1-4 after the addition of power ports to the blackboxed module. They are required in blackbox modules to reduce any errors or disperancies. Above is the list of input ports after the addition of ports starting from ‘vdd’ and ‘vss’. These ‘vdd’ and ‘vss’ ports are the power ports which are used to insert inside the blackbox for the proper compilation and simulation of the gate level netlist.

```
input vdd_a
input vdd_b
input vss_c
input vss_r
input vss_p
input vss_k
input s
input f
input c
input j
input r
input o
```

Figure 4.1-4 Input ports after addition of power ports

In the implementation results, in Figure 4.1 -3 are the power ports present in the 1st Verilog file which have to be extracted and inserted into the module declarations and definitions in the 2nd verilog file which contains the blackboxed module. Figure 4.1-4 contains the inputs which have been inserted into the module of 2nd verilog file which contains the blackboxed module.

CHAPTER 5

CONCLUSION AND FUTURE SCOPE

The research work presented in this thesis is representing a very effective approach in automating the insertion of power ports in Verilog blackboxed modules using the generative artificial intelligence. By using AI based techniques to a great extent, the proposed methodology significantly reduces manual efforts and also ensuring consistency and efficiency in various hardware designs. This solution very successfully handles the blackboxed modules in which the internal details of the module are hidden, making it mainly useful for the hierarchical and IP based design flows. This automation just not only reduces the human errors but also enhances the ASIC/FPGA design process which leads to time and cost saving. Overall, this work highlights the increasing role of GenAI in electronic design automation(EDA).

As this work is establishing a good framework for AI implemented port insertion, many directions remain open for future research. Enhancing the tool dynamically to insert power ports inside a module which is based on multi- voltage blocks can further optimize the power-aware design strategies. Improvement of verilog models by training it on large verilog datasets can improve it’s accuracy and potential, mainly for power structures like power gating and retention cells. By expanding the solutions to handle various hierarchical and multi module verilog designs increases it’s utility to large projects.

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