COMPARATIVE ANALYSIS OF WIMAX DECODER USING VHDL

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CERTIFICATE

I hereby certify that the thesis entitled — **Comparative Analysis of WiMAX decoders using VHDL** is an authentic record of my study carried out as partial requirement for the award of degree of Master of Engineering in Electronic and Communication at Thapar University, Patiala, under the supervision of Dr. Alpana Agarwal Associate Professor, Electronics and Communication Engineering Department, Thapar University, Patiala.

I have not submitted the matter presented in the Thesis for the award of degree to any other university.

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ABSTRACT

WiMAX is a part of fourth generation which provides wireless broadband services. It provides fixed and mobile services based on IEEE standards also called WiMAX standards. It is capable of providing services at data rate of 70Mbps with channel bandwidth up to 20MHz. It is capable of providing speed of 10Mb/s at 10 Km distance. WiMAX is based on WMAN which provides throughput over large distance in case of NLOS propagation.

Different types of decoders are used in WiMAX receivers. Decoders are multiple input- multiple output model. These codes handle various types of channel conditions and requirements for the specific applications. Viterbi Decoder is used in applications of wireless communication where convolutional codes are required to be decoded. This decoding technique is very powerful in case of forward error correction. The working of this is as per the design as well as implementation of Convolutional encoder along with Viterbi decoder when used FPGA. Turbo Decoder is first decoder which approached Shannon limit approximately. Turbo encoder consists of two Convolutional encoders connected by a interleaver so that output is delayed by time. These schemes achieve most reliable data through communication to Signal to noise ratio near to Shannon limit. In LDPC codes, IEEE 802.16e standard are used with number of iterations. They fall under the category of block codes. They have overcome Turbo decoders as there is less delay in LDPC decoders as no interleaver is required in LDPC decoders.

Successful implementation of Viterbi Decoder, Turbo Decoder as well as LDPC Decoder using Xilinx yields the area of 16 slices in LDPC decoder, which is low among these three decoders. Minimum power of 0.459 is consumed by LDPC with the frequency of 166.6MHz as compared to other two decoders. But LDPC is block code, in case of linear codes Viterbi decoder has minimum area utilization in comparison to Turbo decoders.

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LIST OF ACRONYMS

ADC	Analog to Digital Converter
AVD	Adaptive Viterbi Decoder
APP	posterior probability
AES	Advanced Encryption Standards
ACS	Add Compare and Select Unit
BER	Bit Error Rate
BIP	Block-Interleaved Pipelining

BMU	Branch Metric Unit
BS	Base Station
BWA	Broadband Wireless Access
CBR	Constant Bit Rate
CC	Convolutional Codes
CIR	Channel Impulse Response
DAC	Digital to Analog Converter
DMC	Discrete Memory less Channel
DSL	Digital Subscriber lines
FEC	Forward Error Correction
FFT	Fast Fourier Transform
FILO	First In Last Out Buffer
FPGA	Field Programmable Gate Array
GVA	Generalized Viterbi Algorithm
HDL	Hardware Description Language
IP	Internet Provider
IFFT	Inverse Fast Fourier Transform
LDPC	Low-Density Parity-Check Code
LLR	Log-Likelihood Ratio
MAC	Media Access Control
MAP	Maximum A. Posteriori
MLD	Maximum Likelihood Decoding
MS	Mobile Station
NRC	Non-Recursive Convolutional coders
OFDM	Orthogonal Frequency Division Multiplexing
PMP	Point-to-Multipoint
PSS	Probability Selecting States
PTP	Point to Point
RTL	Register Transistor Logic
RSC	Recursive Systematic Convolutional coders
SISO	Serial Input Serial Output

SS	Subscriber Station
SOFDM	Scalable Orthogonal Frequency Division Multiplexing
SOVA	Soft Output Viterbi Algorithm
TBU	Trace back Unit
LOS	Line of Site
NBLDPC	Non-Binary Low-Density Parity-Check Codes
NLOS	Non Line of Site
IEEE	Institute of Electrical and Electronics Engineering
ISP	Internet Service Provider
UMTS	Universal Mobile Telecommunication
VHDL	Very High Description Language
VLSI	Very Large Scale Integration
WiMAX	Worldwide Interoperability for Microwave Access

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CHAPTER - 1

INTRODUCTION

1.1 INTRODUCTION TO WiMAX

In today world of communication recent developments in wireless industry continues to drive requirement of large network coverage, reliability, high data throughput over long distances. Increase in use of mobile internet, multimedia applications video conferences etc has been the main factor in development of Worldwide Interoperability for Microwave Access (WiMAX) which provides broadband services. For broadband wireless communication IEEE 802.16 is a rising standard that is gaining a lot of aid from service provider as well as hardware producers as it is a substitute to wired services or technology to offer broadband wireless services over large distance. Point-to-point or point-to-multipoint applications. In 1999, Institute of Electrical and Electronics Engineering (IEEE) developed a standard named as 802.16 which is back bone of WiMAX also known as WiMAX standards [34] [35].

In 2001 WiMAX promoted abidance and connectivity between to end operators or between operator and Internet Service Provider (ISP) but in 2005, there was a tremendous growth in this field after the release of 802.16e.It is also called as Broadband Wireless Access (BWA).BWA means bringing the feel of broadband while using wireless access along with some unique bandwidth and comfortablility in using technology. BWA is a replacement to cabled connections networks like optical fibers and Digital Subscriber lines (DSL). WiMAX network provides air link connectivity and vendor for roaming. It is capable of handling data rates up to 70 Mbps and channel bandwidth lies in range from 1.25 MHZ to 20 MHZ [34].

WiMAX device possibly provides a speed of 10Mb/s at 10 Km distance while using directional antennas whereas while using Omni-directional antennas speed obtained is 10Mb/s at 2Km distance. WiMax is based on Wireless Metropolitan Area Network (WMAN) which provides very high data throughput over long distance (20 or 30 miles) in Non Line of Site (NLOS) propagation. WiMAX is included as a part Fourth Generation (4G)[15].

1.2 WiMAX Forum

WiMAX Forum is accomplished in order to contribute two types of BWA services [34] [15]:

1. Fixed Wireless Broadband

Fixed wireless broadband also known as fixed WiMAX provides services for fixed and nomadic applications. This operates at frequency between 2 GHz to 11GHz with transmission rate of 75 Mbps up to the distance of approx 50Km and uses single carrier modulation. The IEEE802.16d-2004 standards are used for fixed WiMAX access service. This service is an alternate to DSL or Cable modem.

2. Mobile Wireless Broadband.

Mobile wireless broadband is the first solution founded using IEEE 802.16e-2005 standard which supports both fixed and portable applications and is also known as Mobile WiMAX. Mobile service is based on Multi-carrier OFDM technology and operates at frequency between 2GHz to 6GHz with transmission data rate of 75 Mbps within an acceptable distance of 15 Kms. The Mobile WiMAX network based on IEEE 802.16 which accomplishes point-to-multipoint (PMP) communication, serves multiple Subscriber Stations (SSs) from single Base Station (BS) simultaneously. The parameters used for the analysis of this network are:

- Modulation techniques.
- Coding rates.
- Cyclic prefix factors.
- FFT sizes.
- Bandwidths.

To fulfill the desired performance for the above mentioned services two versions are as follows [15]:

1. IEEE 802.16d-2004, is a version that is found from IEEE 802.16 standard which make use of Orthogonal Frequency Division Multiplexing (OFDM) for the availability of LOS as well as NLOS for both fixed and nomadic access. In this version the frequency band for WiMAX is from 3.5GHz to 5.8 GHz.
2. IEEE 802.16e WiMAX Forum utilizes Scalable Orthogonal Frequency Division Multiplexing (SOFDM) which makes use of sub-channelization. It provides support for the access in roaming as well as for fixed access. Table 1.1 shows various parameters of

IEEE 802.16.

Table No.1.1: Basic Data on IEEE 802.16 Standards [16]

	802.16	**802.16-2004**	**802.16e-2005**
Frequency Band	10GHz-66GHz	2GHz-11GHz	2GHz-11GHz for Fixed 2GHz-6GHz for Mobile applications
Applications	Fixed LOS	Fixed NLOS	Fixed and Mobile LOS
MAC Architecture	Point to Multi-point, Mesh	Point to Multi-point, Mesh	Point to Multi-point, Mesh
Transmission Scheme	Single Carrier	Single Carrier, 256 OFDM, 2048 OFDM	Single Carrier, 256 OFDM, 2048 OFDM with 128, 512,1024,2048 subcarriers
Modulation	QPSK,16QAM, 64QAM	QPSK,16QAM, 64QAM	QPSK, 16QAM, 64QAM
Gross Data Rate	32Mbps-134.4Mbps	1Mbps-75Mbps	1Mbps-75Mbps
Duplexing	TDD and FDD	TDD and FDD	TDD and FDD
Channel Bandwidth	20MHz,25MHz and 28MHz	1.75MHz,3.5MHz, 7MHz,14MHz, 1.25MHz,5MHz, 10MHz,15MHz, 8.75MHz	1.75MHz,3.5MHz,7MHz14MHz,1.25MHz,5MHz10MHz,15MHz, 8.75MHz
Air-interface Designation	Wireless MAN-SC	WirelessMAN-SCa Wireless MAN-OFDM Wireless MAN-OFDMA WirelessHUMAN[a]	Wireless MAN-SCa Wireless MAN-OFDM Wireless MAN-OFDMA WirelessHUMAN[a]

1.3 WiMAX ARCHITECTURE

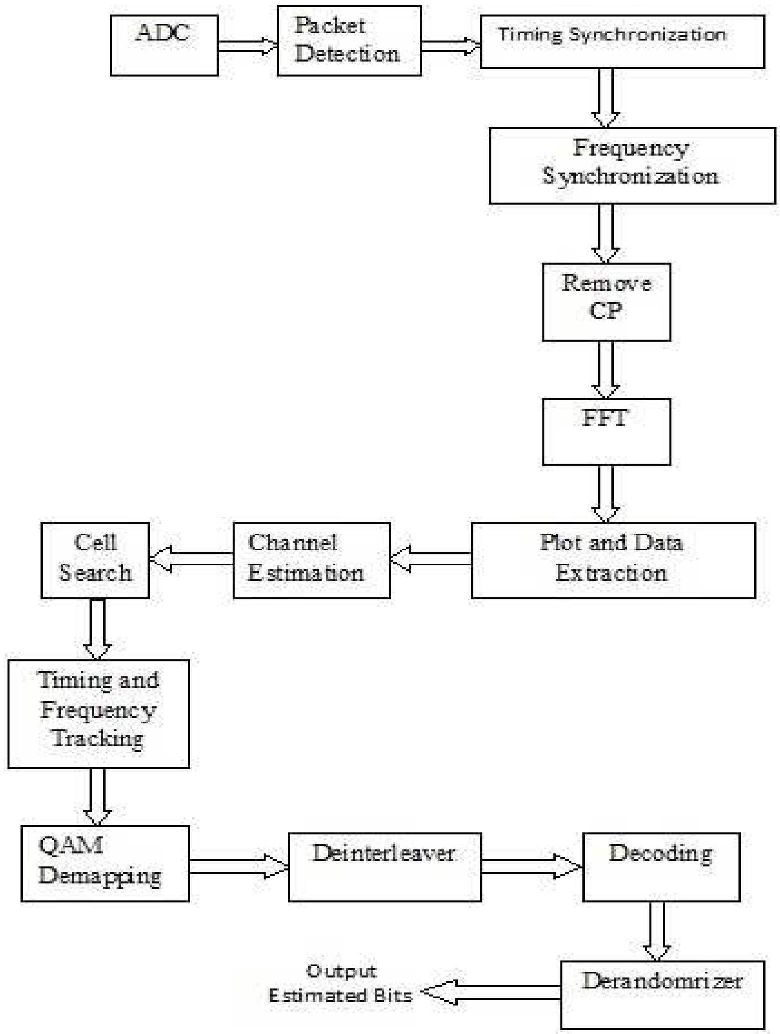

Figure 1.1: Block Diagram of Receiver

At the time of transmission, symbols sent over the channel faces serious consequences because of channel conditions which increases various parameters alike noise, interference including fading due to many factors involved with users working in same frequency band as well as outside the band. The output from channel is fed into receiver and is designed in such a way that it is able to recover the losses occurred in channel. To make a reduction in these losses, a synchronizing block is introduced along with channel estimation. Figure 1.1 shows the block diagram of WiMAX receiver [36].

1.3.1 Timing Synchronization

The motive to introduce this block at the receiver is to distinguish between starting and ending of pattern received, so that data processing can start-off. Timing Synchronization in case of OFDM system composed of Packet Detection, Timing of Symbol and sampling clock. The packet detection is used to find out whether a new frame has been appeared at the input of receiver and symbol timing intimates the receiver to find the start and stop of symbol. Sampling clock tracks pay up for the frequency offset among Digital to Analog Converter (DAC) and Analog to Digital Converter (ADC) at transmitter and receiver respectively.

1.3.2 Frequency Synchronization

Frequency synchronization is a part of receiver which is used to remove errors caused due to frequency offset which has serious consequences on system performance. This offset frequency is produced due to the mismatch between local oscillators of both transmitters as well as receiver end. Frequency Synchronization is done by using coarse frequency offset, fine frequency offset as well as frequency offset tracking.

1.3.3 FFT

FFT is used to converse the function performed by IFFT at transmitter side. FFT produce OFDM symbols in frequency domain. After this operation data as well as pilot subcarrier are removed from OFDM asymbol with null subcarrier removed.

1.3.4 Cell Search

Cell search is made to detect cell along with segment related to mobile segment it belongs. This is carried over with assistance of preamble. Total number of different preambles used in 802.16e is 114.

1.3.5 Channel Estimation

The Channel Impulse Response (CIR) is buckled down by using channel estimation. Channel puts up its impression on attenuation of magnitude as well as phase and rotation of subcarriers in terms of frequency. These all errors are being compensated at the receiver end.

1.3.6 Demapper

Demapper is used to reconstructs the original data stream from the received one. It is required to produce soft estimated bits so that those bits can be used by decoder.

1.3.7 Decoding

Decoding is a process of converting the received coded data stream into its original form. The method of decoding depends on the type of coding technique used at the receiver. When convolutional coding is compulsory to be used at the transmitter side than Viterbi decoding is used at the receiver end.

1.3.8 Derandomrizer

It extracts the original data which was randomized at another end. Random bits are generated using PRBS and modulo-2 operation is performed between these bits and data output from decoder to get final bits.

1.4 FEATURES OF WIMAX

WiMAX a broadband wireless technology is wealthy in features as explained below [15].

1.4.1 Scalability

IEEE 802.16e is based on SOFDM which fix up a scalable bandwidth and that permits dynamic support to the user that roams crossing different networks.

1.4.2 QoS

In WiMAX Media Access Control (MAC) layer provides support to various applications along different QoS demands like applications based on best effort, real time as well as non-real time applications, Constant Bit Rate (CBR) with Variable Bit Rate (VBR) applications.

1.4.3 Mobility

WiMAX facilitates many users within the coverage area of about 50 Km. In providing the facility of mobile applications power saving phenomena is used where Mobile Station (MS) along with Base Station (BS) are required to have various functions to the WiMAX systems.

1.4.4 Security

WiMAX provides high security techniques as Advanced Encryption Standards (AES). It also describes the procedures used for the authentication and maintains private encryption keys.

1.5 ADVANTAGES OF WiMAX

Following are the advantages that are provided by the 802.16-2004 WiMAX to the fixed networks [15] [16]:

- Fixed systems are functional with simpler modulation schemes as OFDM but do not support mobility.
- Fixed deployments have been successful in using license exempted bands where ever interference level is low. This is the reason, maximum profiles license-exempt bands are because of 802.16-2004.

- High throughput is obtained when higher spectrum band is selected in case of 802.16-2004 profiles. This is useful while dealing enterprise users having high traffic.
- As products of 802.16-2004 was only commercially available earlier so operators were able to meet the requirement of connectivity and were able to gain the market share

Some of the operators decide to work as per 802.16e profiles because of following advantages:

- Products of 802.16e are best utilized for mobility and support handoffs at till 120 kph. The support of the product in case of power-saving as well as sleep mode extends the battery life of mobile devices.
- 802.16e provides good indoor coverage which is achieved by sub channelization. Outdoor antennas are capable of compensating for limited indoor coverage when there is fixed deployments but cannot be used in case of mobile users with laptop.
- Resource management of the spectrum is very flexible as sub channelization introduces the ability of using intelligence of network to allocate the resources to the user as per their need. This leads to more effective use of spectrum, resulting in higher throughput and improved indoor coverage, in few issues it results in reduced deployment costs.[15]

1.6 SECURITY ISSUES OF WiMAX

The different security obligations found in IEEE 802.16e, are [25]

- Unverified messages which their imitation could restrict or obstruct the communication carried over among the two i.e. mobile station and base station.
- Unencrypted management: Communications between mobile station and base station is not encrypted. If an antagonist hears the traffic, he will be able to congregate large amount of knowledge from both sides.
- Both multicast services and broadcast services in WiMAX are used where keys sharing can cause members of the group to duplicate the messages or can circulate theirs traffic keying material hence governing the contents of multicast and broadcast.

1.7 DECODERS USED IN WIMAX RECEIVERS

Decoder is a hardware that reverses the operation done by the encoder. It is made-up of combination of circuits that is used to convert binary information of n-input into 2^n different outputs. Decoder can appear in multiple-input and multi-output model. For a pliable together with candid WiMAX selects various types of codes like Convolutional Codes (CC). These codes are capable of dealing with several channel conditions and requirements of applications. The design of capable architecture for the implementation of these types of channel decoder is irreverent by high throughput needed by WiMAX system and that is 75Mb/s per channel.

Decoders used in WiMAX are:

1.7.1 Viterbi Decoder

Viterbi algorithm is named after the name of person who proposed it, A.J. Viterbi. Moreover it is called as Maximum Likelihood Decoding (MLD) algorithm. Viterbi is used in wireless digital communication system for decoding convolutional codes. This algorithm works by developing of trellis and that is traced in backward direction for the decoding. Viterbi decoding has been detected as most adequate for the benefit that its decoding time is fixed. As the number of states increases, the decoder becomes more complicate [43].

1.7.2 Turbo Decoder

Turbo codes was represented in 1993 but was later proved in 19448 by Claude E. which is a parallel concatenated channel coding scheme. They have high correction capability which approaches Shannon limit. Because of this Turbo codes are added in various standards like WiMAX. He demonstrated that is transmitted over the channel with greater reliability with condition that R i.e. Rate of transmission should not increase beyond the value of C i.e. channel capacity. Shannon limit is attained at attainable decoding complexity by using posterior probability (APP) decoding [32].

1.7.3 Low-Density Parity-Check Code (LDPC)

Gallager proffered concept of LDPC in 1963 during his PhD thesis and was reorganized by Mckay during late 1990s. LDPC codes have become popular as they have capability to operate near capacity error i.e. coding is strong enough to provide acceptable long code word. These codes can be used along more parallelism when compared to Turbo Codes because the execution of decoding algorithm is sequentially in case of

Turbo Codes. LDPC codes are directly used at desired rate. They are ranked in the category of Block Codes [1].

1.8 APPLICATIONS OF WiMAX

WiMAX has been flourished to facilitates the services which are penny saving, excellence in quality as well as moldable. WiMAX make it possible for the users to access wireless services in faraway areas. WiMAX has its application on enormous scale [24].

1.8.1 WMAN

Adoration of WiMAX is due to its capability to implement wireless broadband access to metropolitan areas along with the results which are same as MAN. WiMAX overcomes the drawback of MAN by reducing the problems faced during regulating and preserving medium through which transmission takes place. The wired broadband techniques cause a barrier of bandwidth in debt of conflict in between a narrow bandwidth and large number of users. The key to this problem is providing high-capacity connections however it cost very high, another solution is to use DSL or else cable modem. Although these modems are challenging along with time consuming to implement. There is a limitation of distance and quality wiring in case of QoS. WMANs are estimated to accommodate wireless services at less cost still provides high capacity as compares to MAN or wired services [24].

1.8.2 Rural Area Broadband Services

The broadband provides services in highly populated areas by using DSL or cable in a very mannered way but these services are still not delivered in areas which are remotely located. Many areas are still delivered low-speed services using Dial-up systems else no internet access. Provision of nationwide broadband services has this as a challenge at high priority because there is large difference among both areas.

By using wired services will not be a better choice as it will reduce quality and will be costly. The quality depends upon network that is accessed and the connection among the local access point along with backhaul. This backhaul cost is high at larger distances. So this increase the cost, difficulty and also time to spread in these areas by implementing wired services. Satellites are used to provide services to these areas but have certain demerits like upstream bandwidth is limited, spectrum is unavailable along with high delay. So the better choice is to use WiMAX because of low cost and easy to implement. It provides high scalability. WiMAX can be used in small business areas located at remote [24].

1.8.3 Last-Mile High-Speed Access to Buildings

The present wired broadband services faces problems during the time services are delivered at last-mile broadband access for buildings like as internet at high-speed access for residential users, small office or home users, institutions, hospitals etc. As this service is costly and consumes more time, so instead of using this we can go with WiMAX. WiMAX delivers services at less cost and in a very ductile way [24].

1.8.4 Wireless Backhaul

Backhaul means connectivity among subscriber and provider along with provider and core network. High-capacity backhaul is used in WiMAX that is able to serve number of cells simultaneously also capable of expanding for future a small cost. The effectiveness of WiMAX network is maximized by using LOS connectivity including PTP.

1.8.5 Wireless Video Surveillance

The flourishing demands of video surveillance for high-security, safety of the public, need a system which is less costly, tractile, along with safety. For monitoring places, Wireless video surveillance is used and that is a combination of IP as well as WiMAX which is used by public as well as private framework on large scale. On the ground that it can advantage the IP that is existing for transferring security video by secured as well as private IP connectivity, further is capable of covering remote or hard-to-reach areas. Wireless video surveillance is set off in various positions like shops, retailers, transportation centers, military bases, and parks. Traffic, fire, and flood monitoring are examples of wireless surveillance applications [24].

1.8.6 Other Applications

WiMAX are also used in the applications as follows:

- Automatic teller machines
- Multimedia communication
- Medical applications
- Vehicular data and voice
- Sensor networks
- Backup/redundancy to existing wired networks.
- Telematics and telemetry.
- Mobile transmission of information in emergency situations.

- Real-time monitoring, alerting, and controlling the process of dangerous works.
- Wireless transmission of information about fingerprints, photos, Warrants and other images to and from law-enforcement field Personnel.

1.9 OUTLINE OF THE DISSERTATION:

Chapter 1: Introduces the readers to the world of WiMAX, its standards, architecture, features, applications where it is used introduction to decoders used in WiMAX.

Chapter 2: Literature Survey.

Chapter 3: This Chapter consists of Convolutional Encoder, Viterbi Algorithm along with Viterbi decoder used in WiMAX along with the method used and simulation results.

Chapter 4: This chapter gives details about Turbo Decoder along with Encoder and Decoding algorithm. It also consists of the simulation results obtained.

Chapter 5: In this chapter LDPC Decoder is described along with encoder and decoding techniques with the results.

Chapter 6: This chapter deals with the conclusion obtained from results and the future scope.

CHAPTER - 2

LITERATURE SURVEY

Gallager [1] gave idea about LDPC codes which are special example of block codes. He explained the code words of parity check codes which are formed by the combination of binary information. He explained that these codes contains maximum of 1's and less 0's. He explained that equations from matrix can be used for the coding of these codes to find check digit as sum of information bits. He explained that the rate at which LDPC codes are used is bounded to maximum channel capacity. He showed that distance property of code word was exponentially related to length of the block. In case code rate is less than P (e) decreases exponentially depending upon block length.

Bahl et al. [2] considered a discrete memory less channel by which a posteriori probabilities along with the transition of Markov source. They derived an optimum decoding algorithm for decoding of linear block as well as convolutional codes so as to reduce symbol error probability. They observed a noisy discrete memory less channel (DMC), estimated a posteriori probabilities (APP) for the states and markov source estimation. They deployed algorithm for linear codes which similar to concept of the method of Chang and Hancock so as to remove Inter Symbol Interference.

Hekstra [3] gave some of the ways to make implementation easy. He gave rescaling scheme in which metrics having smaller value was subtracted by all other metrics and he also proposed two's complement arithmetic's as another way for the implementation. This resulted in saving of hardware, increase in loop of metrics update which affects the decoder throughput. He showed that modulo provides a large range and is symmetrical about zero when it is applied to metric which results in overflow and reduction in cost of hardware. This resulted in simplification of design and computational throughput. He exploded properties of Viterbi algorithm which are path selection depends upon difference of the metrics and this difference between matrices is bounded. He proposed rescaling scheme in which the smallest metric is deducted. An alternative to rescaling was developed called as 2's complement method. He found that 2's complement method saved hardware and any types of deduction is avoided. It also speeds up the updating of loop resulting in increase through put.

Sun Ping et al. [4] proposed Probability Selecting States (PSS) mode as simplified Viterbi decoder scheme. He proved that PSS mode was more reasonable as compared to Generalized Viterbi Algorithm (GVA) in eliminating decoder states which is applicable to the optimum distance codes. They proved that the decision using MAP was optimum decision criteria as compared with ML decision. They showed that PSS type decoder has same BER but half of the hardware is required as in standard Viterbi decoder with specification of r = ½, k =7 (147,135). To reduce more complexity they introduced a new algorithm for decoding along with SST configuration the method. They proposed three techniques which are advantageous as compared to GVA-type decoder. Firstly this method worked for the optimum code having good distance property, secondly this algorithm was applied to PSS-type decoder with optimum decoding .Lastly it made use of likelihood property.

Felstrom et al. [6] constructed convolution codes described by Low-density parity-check matrix having memory as 1025; 2049 and 4097 which showed that at a BER of 10^{-5} they were only 1 dB away from the capacity limit and the complexity of decoder was of equal magnitude as compared to a Viterbi decoder in case of codes with memory M=10.They implemented a pipeline decoder to know BER of these codes. They introduced new type of codes different than LDPC and turbo codes. They found that low-density CC performs better than Turbo codes for small interleaver. They represented a class of codes which lies in the category of Convolutional codes along with decoding algorithm which is iterative in nature. The results of their codes proved that they are better performer than Turbo codes. They implemented a pipeline decoder for simulating in AWGN channel to get brief knowledge about BER. They do not produce an effect of BER probability in case of decoding of codes with large SNR. At last they showed that with small interleaver a low-density Convolutional code performs better than Turbo codes.

Sae-Young Chung et al. [8] designed LDPC codes which are based on density evolution which is discretized along with the use of iterative linear programming for optimization degree distribution. They found a code with rate ½ having a threshold ratio of 0.0045dB of Shannon limit of AWGN channel. They gave the design which can be used with in rates of 0 and 1. They suggested that as the block length increases to infinity, the sum – product algorithm for decoding reaches the Shannon limits. The design they proposed is capable of designing LDPC codes of random rate 0 along with 1. When n numbers of quantization levels are used the complexity of the calculations at check nodes is given by O (n^2).

Richardson et al. [9] designed LDPC codes which perform approximately near to Shannon capacity which they used with bipartite graph which was irregular having degree patterns. They proved that probability density posse's symmetry at message node, assuming that there is symmetry in channel used. They showed that there was an increase in message densities with increase in number of iterations towards infinity assuming no cycles while assuming channel symmetry. Moreover they proved a stability conditions that makes the fraction of errors limited to upper bound that can be corrected by decoder when used for a code with the help of bipartite graph. They proved stability condition which imposes upper limit on part of errors which belief-propagation decoder is corrected when used with the graph. They found these codes by optimizing the graph in terms of degree.

Luby M.G. et al. [10] improved the Gallager's LDPC codes. They introduced irregular parity-check matrix along with new analysis of hard-decision decoding based on martingales. They gave methods for constructing irregular graphs and make the performance better. They used belief propagation algorithm. They verified the results of efficiency on Gaussian channel as well as binary-symmetric. LDPC codes can correct errors up to 16% while the code designed by them can correct up to 17%. They contributed towards LDPC codes using irregular graphs which produced better results than codes using regular graphs and they introduced a new way out for analyzing LDPC codes which used concentration bounds. There gave a concentration theorem which was based on martingales. They developed a density evolution algorithm which is used for the approximation of noise threshold within which belief algorithm was success.

Anastasopoulos [11] further carried over the analysis of min-sum algorithm for binary codes. A comparative analysis for LDPC codes as well as RA Codes is done for both discretized sum-product and min-sum algorithms. From the comparison of both codes he found that after doing a modification in min-sum algorithm a great improvement was achieved. The result showed that there was a performance degradation of 0.27-1.03 dB in case of min-sum algorithm. He showed that min-sum was slightly modified resulted in nearly sum-product algorithm which executes similar to sum-product algorithm. But there was a loss in the performance for min-sum algorithm.

Wang et al. [12] proposed two approaches for the better performance of SOVA based Turbo decoder which includes normalization of output from decoder by using variables and mapping functions which are applied to calculate target scaling factor for the normalizing information that is received at the output of decoder. The second approach that they used was the metric difference of competing paths was computed by setting upper bound which is based on reliability of channel. By using first approach they obtained more coding gain of 0.5dB while using AWGN channel in which no extra latency is required. They showed that by use of these two approaches SOVA-based decoder approximately reaches MAP-based turbo decoder of about 0.1db with low BER. They represented an architecture which is area efficient with parallel decoding for the designing of high-throughput turbo/SOVA decoders. They used two-level interleaver to solve the multiple memory access occurred in the implementation of efficient parallel decoding. They showed that the interleaver proposed needs less storage of random patterns.

Yanhui et al. [13] performed a comparison between algorithms of different turbo decoders for the performance and design complexity. They designed an (RTL) Register Transistor Logic fixed-point turbo decoder which was based on Log-MAP algorithm which offers good compromise between performance and complexity. They implemented turbo decoder by using VHDL using RTL model and by using C-language. They proved that optimal performance is obtained by log-MAP algorithm along with less complexity. They obtained the design of turbo decoder for low speed decoding but were modified by increasing number of SISO decoders in parallel operation. They designed turbo decoder for low-speed decoding and more SISO decoders can be added so as to make it high-speed decoding.

Douillard et al. [14] illustrated that better performance can be achieved by replacing rate ½ components by rate (+1) RSC codes. They explained the reason for the Turbo codes with two level of permutation performing better than one-input TC which are both binary. They designed an encoding scheme that performed better in low error regions along with its decoding reaching theoretical limits approximately. On the way to search channel coding perfect for this they faced two challenges. Firstly, they were required to achieve large minimum distance and secondly decoding to be achieved was close to theoretical limits. They found that a parallel concatenated RSC circular codes causes flexibility in codes which becomes adaptive to large block of data and coding rates

Fili S. [15] on the behalf of WiMAX forum has explained the different IEEE standards under which types of WiMAX services are provided. She explained different services along with various parameters that are covered under those services. She has given detail about various frequency bands, modulation schemes, channels, devices used, speed etc of different type of applications under the standards. She has given a road map of development of different stages of WiMAX. She has explained various modulation schemes used along with their benefits

Cole et al. [17] gave three steps method to determine low BER of LDPC codes having moderate length without knowing information about spectrum of error event weight or Monte Carlo simulation was restored. They applied this method to different types of decoding as belief propagation of message passing algorithm where as min-sum approximation to this algorithm. This method allowed checking error performance at BER. The method they designed that used a search method so as to find dominant errors and then uses impulse of error to find which event comes under the category of truly dominant error event. The method is also capable of providing the capability to accurately analyze and adjust the behavior of coder as well as decoder in the error region. The min-sum algorithm used is as good as in other cases where as they proved that this algorithm even gives better results than belief propagation algorithm at high SNR.

Hema et al. [18] represented an implementation using FPGA of a Viterbi decoder which had input data of length 11 along with code rate of 1/3. They showed that increase in the length resulted in production of powerful code. They gave a viterbi algorithm which entirely depends upon trellis of the states in decoding of Convolutional codes. They modeled the decoder using Xilinx and proved that by using error correcting codes, data corruption can be reduced. They implemented the design and simulated which was based on both RTL as well as code generated by Xilinx design manager after post synthesis.

Andrews et al. [19] described the design, research, implementation and standards that has been carried over at Jet propulsion Laboratory for turbo codes as well as LDPC codes which standardized in various spacecrafts. They developed turbo codes in which design included selection of polynomials, design of interleaver which imposed the weight distribution, error floors in the decoder, threshold of iterative decoding. They designed LDPC codes by using photographs along with circulants which depends upon threshold of decoding and a procedure in which loops in code graph are avoided. LDPC encoders as well as decoders are used in implementing in hardware of spacecraft.

Martina et al. [20] proposed architecture of turbo decoder for WiMax which contained new innovation of switching between Universal Mobile Telecommunication (UMTS) to WiMax duo-binary turbo decoder and decoder architecture are parallel and collision free. They proposed architecture and achieved decrease in complexity of memory and logic of 17.1% and 27.3% .This architecture can be described by the parameters of performance along with complexity which is capable of handling throughout more than 70Mb.They presented a flexible UMTS/WiMAX decoder architecture for Turbo codes along with parallel architecture of WiMAX interleaver. The proposed architecture has complexity within limits.

Savin [21] proposed decoding algorithm for decoding non-binary codes which are having low complexity and are quasi-optimal. He gave algorithm Min-Max algorithm implemented with canonical selective resulted in decrease in number of operations required for decoding in each iteration but did not affect the performance. He derived these algorithms having iterations with correct metrics in decoding of non binary LDPC codes. The complexity scales with the square of Galois field's cardinality. The message exchange between these two algorithms of LDPC are in the form of metrics representing distance between symbol as well as the one like to happen. The Euclidean distance and

Min-Max algorithms are used. Min-Max algorithm becomes very useful because of low complexity as well as quasi-optimal performance.

Darabiha et al. [22] described architecture of parallel decoder which is parallel having low routing and then they proposed a way out to detect convergence of iterative decoder as earliest so that computation can be terminated. They proposed the architecture of LDPC decoder with BER of 10^{-5} and having throughput of 3.3 G b/s. They proposed these two methods for decreasing the power consumption, superior speed and energy efficiency of fully parallel LDPC decoder on the cost of its scalability which depends upon big area and complexity of interconnect network. They fabricated a fully parallel LDPC decoder which was fabricated on a 0.13-m CMOS process. This prototype is able to decode at early transmission with 10.4pJ/bit/iteration which performs within Shannon limit at 3dB at BER of 10^{-5}.

Charot et al. [23] proposed the design in terms of parallel as well as modular architecture which was compatible to 802.16 WiMax standard code classes. They found that while comparing either four or six designs of FPGA module had resulted as throughput between 10 and 30Mb/s at clock frequency 160MHz by using 20 iterations. These are good results for the use of design with the WiMax communication requirement in terms of throughput.

Ibikunle et al. [25] explained various security issues related to WiMAX also called as IEEE 802.16 standard which is used over large distance. They analyzed security of Mobile WiMAX and found various threats along with various vulnerabilities. They proposed some improvements as well as solution to wipe out vulnerabilities. IEEE 802.16 is a standard for broadband wireless communication which is used as an alternate to wired services over long distance and is popular now a days. The security issues they considered are unauthenticated messages, unencrypted management communication along with shared keys when multicast and broadcast services used in WiMAX. They applied all the changes the security of Mobile WiMAX has significantly increased.

Arai et al. [26] proposed a new architecture named Block-Interleaved Pipelining (BIP) to provide high energy efficiency and throughput in case of Turbo decoders. They used BIP along with tailbiting in place of SW which resulted in reduction of warm-up calculations up to 50% and memory size seizes to constant value depending on number of pipeline stages used. Conventional sliding window (SW) BIP was replaced as this type of turbo decoder suffers from large calculations and increased memory size. They implemented 4 pipeline stages in area of 3.8 mm^2 using a 0.18μm CMOS technology.

Zhang et al. [27] described a design to map LDPC to hardware along with decrease in BER and decrease in error that occurs in various other LDPC codes. They proposed a relation between fixed point quantization and error correcting capability of sum-product decoder. The proposed sum-product algorithm removes log-tanh functions. They implemented LDPC decoder with high throughput but with reduced error rate.

Salbiyono et al. [28] compared the LDPC decoder performance using two algorithms which involves sum product algorithm and min-sum algorithm and concluded that while using min-sum algorithm performance was reduced when number of iteration used are less than 20 when compared with sum product algorithm. When they increased the number of iterations from 20 to 25, a slight improvement was seen the performance and same results were obtained while using min-sum algorithm.

Harikrishna et al. [29] implemented a high level of FFT for an OFDM modulator as well as demodulator having high performance. They used Verilog to code and implemented using Xilinx on Spartan3 FPGA. They proposed the radix-2 algorithm for the use in OFDM system. This design was implemented as well as applied on WIMAX or IEEE 802.16d standard and the results obtained were compared. The architecture has many advantages like less number of iterations for the reduction of power consumed, clock frequency is increased by using pipelined radix-2 butterfly and the utilization efficiency is evenly distributed in respect to memory access. Their design used less number of gates along with low cost and power usage.

Wang et al. [30] proposed a algorithm in which LDPC code which is irregular and quasi-cyclic (QC) was divided into number of several parts and were organized in a way that a reusable multimode architecture was designed for the processing of the task. They made the processing of tasks easier by introducing Memory address generators which overcome the problems faced in the realization of low-complexity decoder with multi mode feature, which supported different type of QC-LDPC codes. A moderate encoding throughput of 800 Mb/s was achieved by full-mode WiMAX codec along with area of 0.679mm. They devised an LMPD-ICM based algorithm so as to make processing task for different types of QC-LDPC codes in such a way that operation of decoding can be carried out in unified task processor which helps in reducing difficulties in the realization of multimode decoders. The throughput of the codec designed is almost independent of codec length and the resource used also provides early termination which results in decrease in power consumption.

Nan et al. [31] analyized LDPC with simple cycles and represented these cycles with minimal. They represented cycles with length variations along with minimal matrices for these cycles. These simple cycles used in LDPC codes with equal length are equal as obtained after permutation of row or column. They worked for research of different cycles other than simple and balance cycles. An expanded matrix was introduced for circulant permutation when cycle was a combination of two simple cycles. They proved that minimal matrices of 2k- simple cycles was given by $\frac{(k-1)! \, . \, P_k^{k-}}{2}$ for k>3.

They researched the cycles formed by twice of simple cycle and will induce this cycle in the matrix form.

Martina et al. [32] discussed the implementation of Max while using turbo and LDPC codes. They presented architecture for the implementation of Max operation along with VLSI design. They proposed architecture implemented using Max operation along with turbo-LDPC and achieved necessary BER which was optimal having low complexity in terms of computation when compared with turbo-LDPC decoder in dual mode. The architecture they proposed is used where joint decoding architecture employed to decode turbo as well as LDPC code. Coders with generalized max* operator are implemented with r = 3, r = 4 with results obtained as optimal BER and low computational complexity.

Lennin et al. [33] presented architecture of LDPC decoder in which they reduced the complexity of design by eliminating interleaver but did not affect the performance. They implemented the VLSI architecture to represent 3GPP2 standard turbo decoder which was based on Log-MAP algorithm. They considered hardware issues along with changes of the conventional structure of the decoder and the verification of implemented design was done by comparing this with fixed-point model. They approached the results obtained by using sliding window in case of real-time decoding and this was implemented on Altera devices. The architecture they proposed results in reduced latency and various modes of operation are used to achieve data throughput needed by CDMA2000 standard. They implemented this architecture on Altera's Stratix II FPGA and compared with Xilinx turbo decoder which shows excellent results.

Kene et al. [34] gave a simulated model of WiMAX physical layer so as to make the understanding clear about system and various parameters along with their role in WiMAX system. They used MATLAB 7.5 to develop this model. They studied the effect of BER under different types of channels. They studied different parameters and their effects like modulation techniques, Coding rates, FFT size etc. so as to make understanding clear. The model they represented can be used for implementing of coding as well as modulation schemes. From all this data and results user is capable of choose best possible solution to their needs. From result they concluded that BPSK modulation needs low signal power as compared to higher order modulation schemes. But they optimized the system performance using adaptive modulation. To increase the transmission rate, 64QAM was used so as to settle a compromise between higher order modulation scheme and less coding redundancy.

Pariet et al. [35] explained the evolution of WiMAX. They gave an article related to the survey on all the related activities that happened among three organizations. Those three groups are IEEE involved because of technology development and formation of standards, WiMAX Forum to carry over product certification and ITU for the recognizing internationally .They overview have revealed the importance of an attempt to provide innovative and add new ideas to it.

Pham et al. [36] developed a high data rate LDPC decoder with Multi-Gbps using a high level modeling tools and then implemented using FPGA. The Multi-Gbps decoder designed by them can be used in high data rate wireless communication. The design they proposed resulted in great benefit in various aspects like design complexity, the time required for processing. They represented methodology for modeling synthesis as well as implementation of LDPC decoders. Their FPGA design proved design methodology to be effective, efficient as well as error free. Their methodology has been proved to be of great importance as it has advantages in various aspects like effort and time compared to HDL design, complexity of the design. This design is of great value as it is cost effective and pays the way for reuse of complex high performance LDPC decoders.

Pujara et al. [37] gave analysis between numbers of FPGA devices for architecture to optimized implementation of viterbi decoder. They analyzed the result on the basis of comparison of simulation as well as synthesis of the design using different FPGA devices. They analysized that Spartan 3A FPGA device can be used with less resources at frequency of 33.124MHz for the proposed design. They found that for the same design, FPGA device VERTEX 5 can function at maximum frequency 113.104MHz when compared to all FPGA devices. They gave a design of Viterbi decoder which is resource optimized and they used trace back method. Viterbi decoder has its compatibility with many standards as 3GPP, 3GPP2, LTE etc.

Tsang [38] proposed a decoding algorithm for LDPC codes which was less complex and implemented on FPGA using VHDL code with device Spartan-3E XC3S500E FPGA chip. They introduced a processing scheme which is highly efficient at check node unit which was able to decrease the delay in processing and this scheme is proposed for min-max algorithm. Decoder was designed to explain who efficient this scheme was. NBLDPC codes are the main form of FEC. Flexible NB-LDPC decoder was not able to achieve high throughput as well as low power required for the applications, so they implemented prototype architecture of NB-LDPC codes.

Made et al. [39] proposed a design of Adaptive Viterbi Decoder in which survivor path are used with different parameters of communication in order to decrease the power and reduce the cost with speed increased. They developed a design in which trace back algorithm was removed and resulted in increase in processing time. They used algorithms which includes survivor path along with units of reconfigure Viterbi decoder and adaptive Viterbi decoder. They proposed new design of Viterbi decoder and applied on a SPARTAN 3. They found that survival path decoder supported frequency up to 790MHz within constraint length of 7and 9 with rate 1/3 as well as survival path 4. They tried to solve the problem associated with Viterbi decoder which is a important part of physical layer. They implemented their design on FPGA using Xilinx ISE 9.1 for synthesis.

Martina et al. [40] proposed an approximation algorithm which involves n-input max operations along with its hardware architecture. The algorithm they proposed are more simpler and requires less area than constant Log-MAP algorithm but this is achieved at the cost of slight decrease in performance of about 0.1db. They achieved the simplification by the use of a digital circuit to find the two maximum values from a set of n data which is used in computing right time. They implemented a architecture is 30%, a Log-MAP chip area is used with equal delay. The results are obtained at cost of degradation of performance by 0.1db up to average bit error rate, for turbo codes having 10^{-5}. The algorithm they described similar Log-MAP turbo code performance in case of both binary as well as double-binary codes but there is no increase in complexity.

Nirmal et al. [41] implemented a simulated soft core of viterbi decoder having constrain length =3 along with code rate of 2/3. They represented a trellis based decoding of convolutional codes using Viterbi decoder which caused a decrease in data corruption because of error correcting property. The tool they used was Xilinx ISE and modeled in Verilog. They represented the design of (AVD) Adaptive Viterbi Decoder in which survivor path is used along with parameters of communication so as to reduce power as well as cost with speed. Researched have worked in this field so as to reduce power required and decoder to be used at high frequency in various applications like 3GPP, DVB etc. FPGA is highly configurable used in implementing difficult signal processing task.

Tsang [42] developed a processing scheme for the implementation of NBLDPC decoder in which the delay was greatly decreased as compared with other implementations. He proposed Min-Max decoding algorithm along with check node unit. He succeeds in obtaining less than 52% decrease in latency of check node unit. The code proposed by him achieved a 0.8db coding gain over other codes. They demonstrated the efficiency of the technique for (620,310) NBQC-LDPC decoder. Their study showed the effect of parameter change on the performance which is called as sensitivity analysis. Various parameters can be varied like throughput etc. Throughput showed the rate with which steady state action is performed. They observed that sensitivity of number of devices on throughput transit as compared to the FB-Min-Max, nm = 32, floating and nm = 16, floating modulation for nm = 16. Maximum iterations used are 15.they included FFT-BP algorithm and FB min V max so as to do comparison.

Sivasankar et al. [43] analysized design of viterbi decoder with the code length of 3 and 7 along with the code rate of ½ using verilog HDL and synthesized by using Xilinx 9.1on Spartan 3E device. They analysized that viterbi decoder has high complexity that results in the limitation of use of this decoder in applications of convolutional codes having code length not greater than 10. They analysized the performance with respect to resources used in Viterbi decoder using Verilog HDL. The design they proposed required less

number of resources as compared to other designs, which is concluded as low complexity in the hardware. Their results showed that the power absorbed by the Viterbi decoder is 0.081 watts. They concluded that the constraint length increases, the complexity in the hardware also rises.

Selvi et al.[44] realized Convolutional Encoder and Viterbi Decoder with a code having code rate of1/2 using FPGA and simulation tool used was Xilinx 13.1i.The code designed was having a constrain length of K=9.They designed Convolutional encoder for encoding the input data that was sent over a channel. At the decoder end, they used Viterbi decoder to decode the transmitted sequence into the approximated input data. They used Convolutional encoder and Viterbi Decoder which are having excellent error control execution. The signal transmitted over the channel is corrupted by noise and maximum likelihood detection is done by Viterbi decoder

CHAPTER - 3

VITERBI DECODER

The data sequence is encoded preceding the transmission of the sequence is done by enumerating redundant bits to it that is used by the receiver to reconstruct the original sequence. Reconstructing the sequence is done in an effective way which results in reduction of error probability that is introduced by noisy channel. Various bit sequences have been generated using different type of codes called as Channel Coding. The different bit sequences that are generated are called as Code words. Decoder use these enumerated redundant bits to detect and correct number of bit errors, a particular code can permit. Coding is categorized into two main categories as Block Codes and Convolutional Codes. Block codes are generally used to decode block of data whereas Convolutional code is capable of decoding consecutive data bits along with block of data. Convolutional codes are based on detecting smallest path across a graph that shows a trellis of Convolutional codes. There have been few convolutional decoding method like sequential as well as Viterbi decoding out of which maximum used is Viterbi algorithm[37].

Viterbi decoder uses Viterbi Algorithm to decode a stream of bits which has been encoded using Convolutional codes. Viterbi algorithm is utmost resource consuming. Viterbi decoding is a potent Forward Error Correction (FEC) method which is especially suited for a prolonged data stream. Viterbi is used on a large scale in wireless and mobile communication so as to provide optimal decoding of Convolutional codes. It is used in digital modems as well as cellular telephones in which latency is less along with cost and power consumption [43].

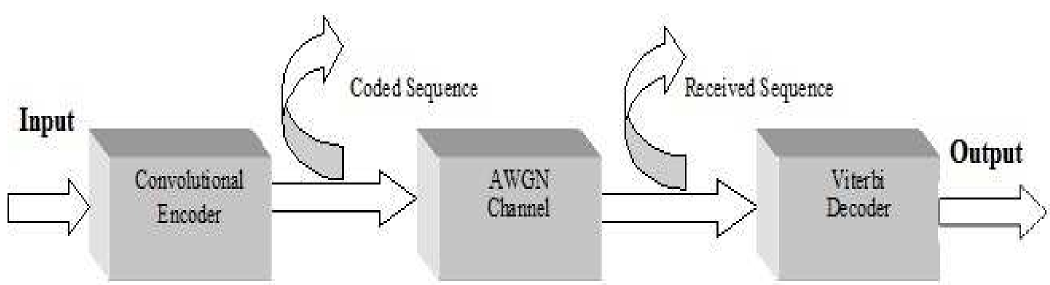

Figure 3.1: Block Diagram of Convolutional Encoding and Viterbi Decoding

3.1 CONVOLUTIONAL ENCODER:

Convolutional encoder is made up of constant number of shift register as shown in figure 3.2. Input bit is fed into the shift register and output is obtained by combining the bits.

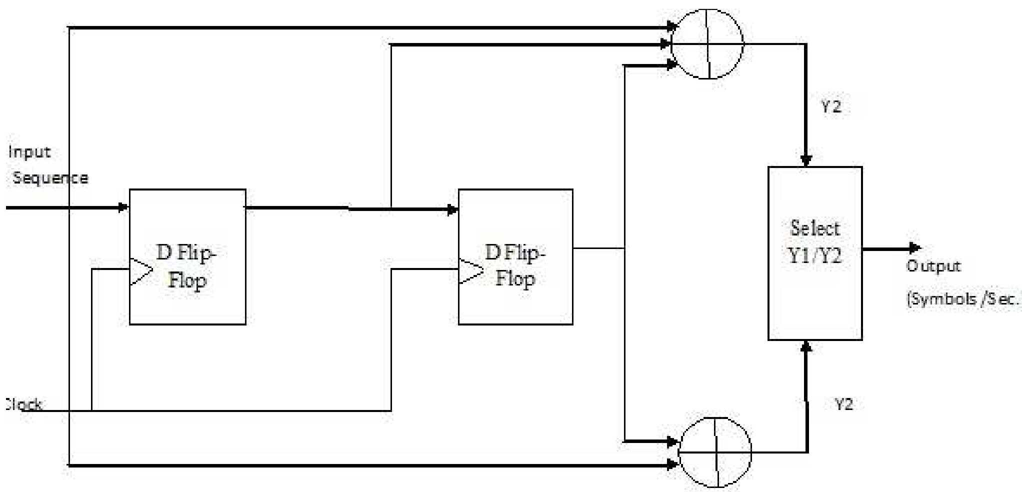

Figure 3.2: Convolutional Encoder (rate= ½)

The output bits are produced which depend on number of modulo-2 adders which are incorporated with shift registers. The notation used to specify these codes is (n, k, m) where n is number of output bits, k is number of input bits, m is number of memory registers as well as code rate is given by r = k/n bit/source which defines bandwidth efficiency of code [44].

In Convolutional codes, modulo 2 additions is done to encode the bits. In the example shown encoder produces two bits corresponding to each input. Consequent input bits will encoded by bit knowledge by generating four adder bits. Thus by neglecting some bits, left out bits will deliver the knowledge i.e. original data bits. Convolutional encoder is Mealy Finite State Machine in which output depends upon state and commenced input. The Figure 3.3 shows concerned state diagram for the convolutional encoder. After state diagram, Convolutional encoder is represented in form of trellis which the relation between the states and path measure at each particular sample of time as shown in figure 3.4. The initial state is 0 because all registers contains 0. The place of stages is determined by generator polynomial. It is also used for determining minimum hamming distance which shows how many bits are different within its decoding performance [4] [39].

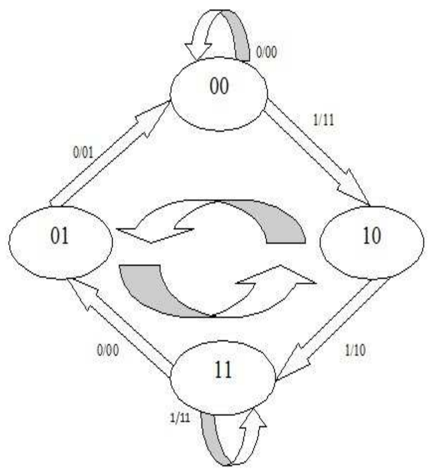

Figure 3.3: State Diagram

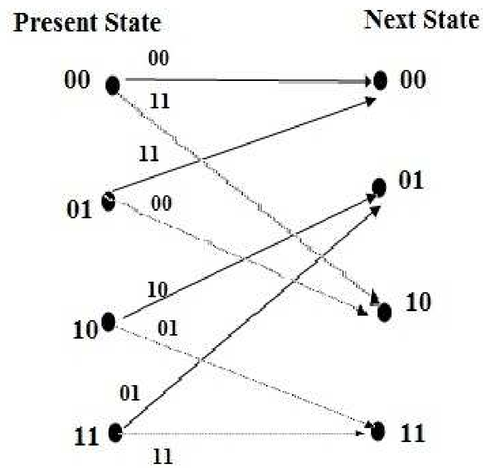

Figure 3.4: Trellis Diagram

3.2 VITERBI ALGORITHM

This algorithm is useful in approach in decoding Convolutional codes. A data is encoded and the encoded bit stream is passed through a channel and reaches receiver. During the transmission through the channel, the received code word does not match the transmitted one because of noise present in channel. The decoder used is fed with received signal which generates sequences which is estimate of transmitted one. Maximum Likelihood Decoder chooses the estimated data sequence which produces maximum probability p(r/z) as per Bayer's law

$$p(r/z)\ \ p(z) = p(z/r)\ p(r)$$

Finally initialization is done of Viterbi decoder to machine state along with trellis diagram. Figure 3.5 shows the flow chart of Viterbi Algorithm. Then decoder calculates the branch metric's hamming distance for the four possible states. Add Compare and Select Unit (ACS) calculates the hamming distance of two possible paths and choose the path having smallest value. ACS also keeps the record of the path with smallest branch metric. Along the way trellis is formed at each transition state and needed information is noted like Path Metric as well as decision bit. After receiving all data bits, last stage becomes the first stage and the trellis is traced back and decoded data is output from the decoder [44]. Figure shows the flow chart of Viterbi Decoding: [37]

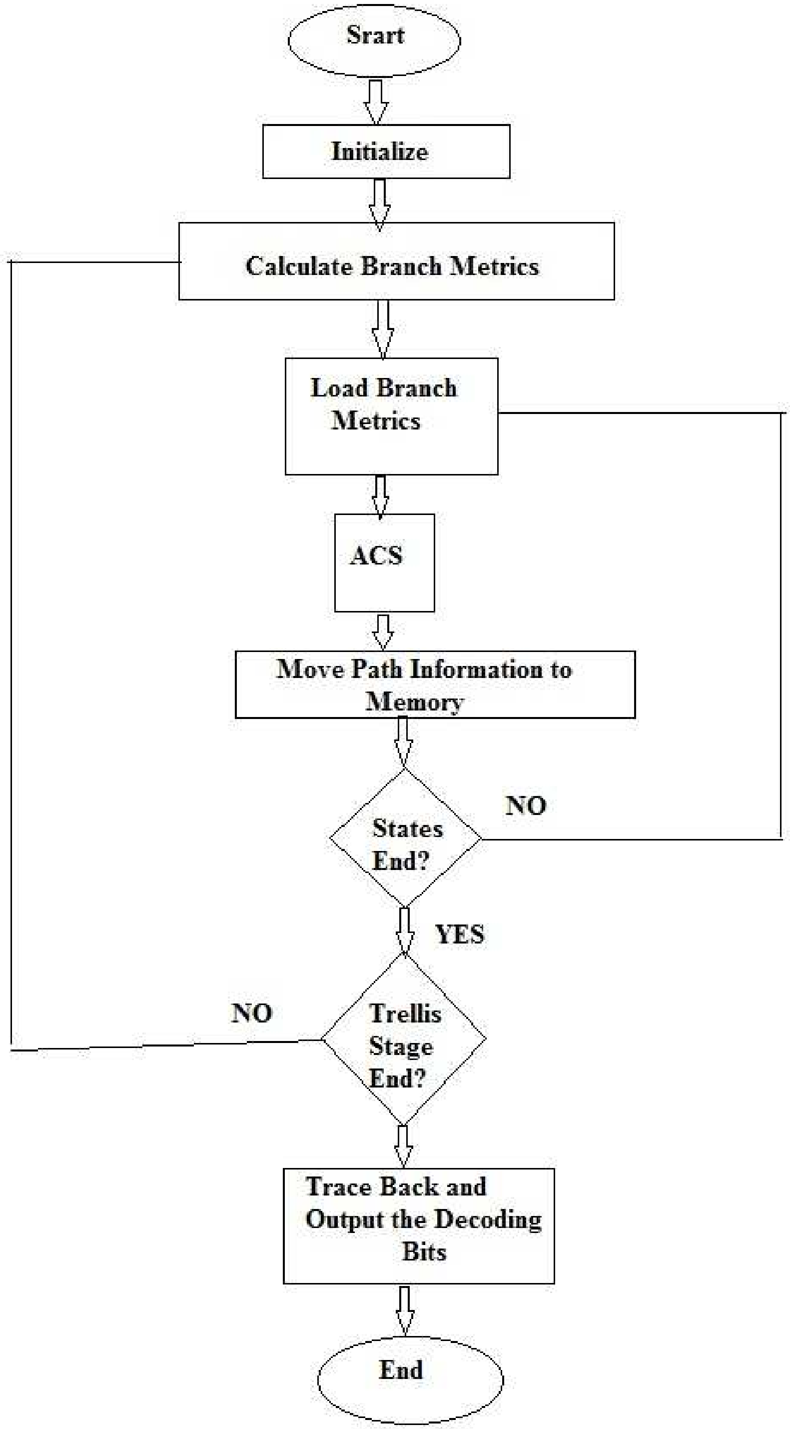

Figure 3.5: Flowchart of Viterbi Decoding

3.3 VITERBI DECODER

Viterbi decoder is used to resolve Convolutional codes. This is important for safe transmission and safely fetched at receiver. This decoding is more efficient and effective as it reduces the redundancy in the codes. Performance of decoder is determined by Bit Error Rate (BER) i.e. number of decoded bits which are wrong and do not match transmitted bits [37].

Viterbi decoder comprises of three parts as shown in figure 3.6:

- Branch Metric Unit
- Add Compare and Select Unit
- Trace Back Unit
- First In Last Out Buffer

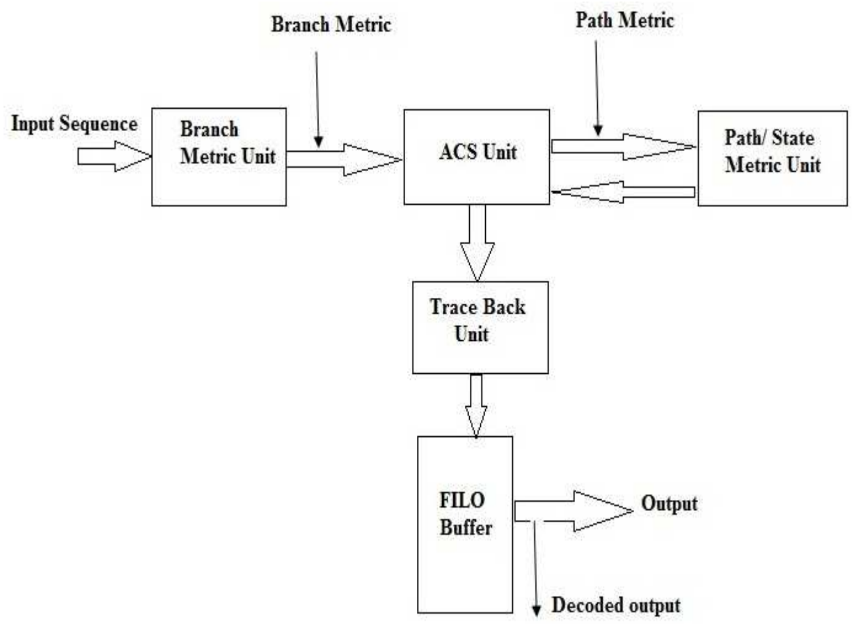

Figure 3.6: Block Diagram of Viterbi Decoder

3.3.1 Branch Metric Unit (BMU)

BMU is responsible to calculate branch metric hamming distance or Euclidean distance for the four possible cases i.e. “00”, “01”, “10” and “11”. This is based on look-up table containing different bit metrics .Look-up table is used to calculate metric associated with each branch and added them to produce branch metric as shown in figure 3.7.

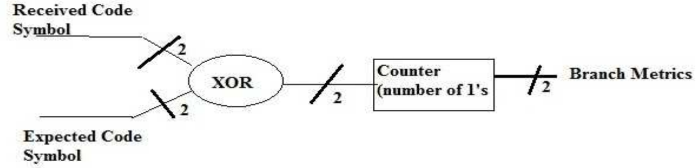

Figure 3.7: Metrics Computation Block

The geometer distance between ideal code words and an discretionary purpose during this area provides the branch metrics. By increasing the quantity of soppy bits the quantity of attainable values for branch metrics conjointly will increase. It shows the branch metric diagram for Associate in 8-level decoder. The branch metric uses the overacting distance for the four attainable methods. First, we tend to initialize four completely different received overacting distance search table. Then at on every occasion instant, we tend to check the input image, we tend to get the four attainable distances. The BMU perform straightforward check and choose operations on the choice bits to get the output. The hardware implementation is shown within the figure

3.3.2 Add Compare and Select Unit (ACS)

ACS receives path metric value as well as branch metric value. The present branch metric value is summed up with past value of path metric and distances are compared in ACS unit. Speed of Viterbi decoder can be calculated by number of units as well as time consumed by ACS unit. ACS is made up of two summers, comparators as well as selector.

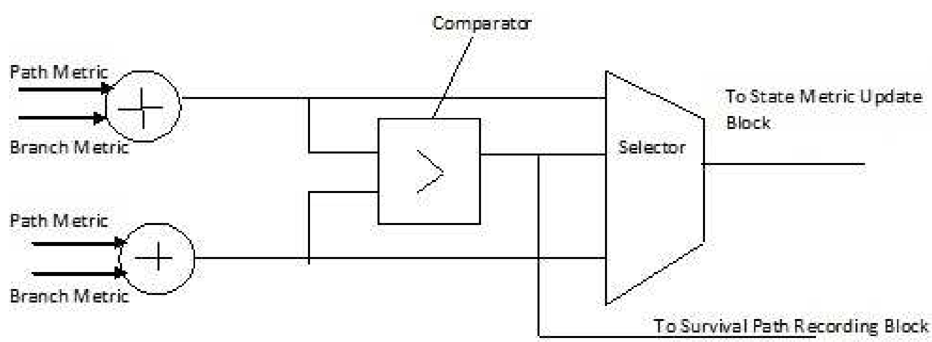

Figure 3.8: ASC Unit

When the four attainable input distances is prepared, the ACS block, butterfly module adds the results of previous state metric and therefore the connected distance worth to urge 2 methods for every sixty four states. The butterfly module is shown in figure 6.2. We've total thirty two butterflies. Every butterfly computes four attainable methods and selects the 2 smaller distance methods.

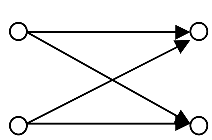

Figure 3.9: Butterfly Module

For each state, the ACS module selects a smaller one because the survival path and stores them to the accumulated state metric storage block and therefore the survivor path metric. The decoder continues during this thanks to advance deeper into the trellis and to create choices on the computer file bits by eliminating all methods however one.

3.3.3 Path Metric

It is used to compute the total metrics of path at nodes of trellis by adding the branch metric of all the branches participating in the formation of path.

3.3.4 Trace back Unit (TBU)

Trace back unit is also called as Survivor Management Unit. Trace back and register exchange techniques are the ways to provide path management. Trace back consumes more time but need less area when related to register exchange technique. Extra hardware is required in register exchange method for reversing the bits. The cost of register exchange is very high specifically when sequence is very large so more source are required.

When the trellis diagram is finished, the trace-back module can search the utmost probability (ML) path from the ultimate state that is state 0 to the start state that is additionally state 0. Each time, the trace-back block simply left shifts one little bit of the binary state range and add one bit from the survivor path metric to figure of the previous state. By eight Bit Full Adder eight Bit Full Adder > Accumulated state metric storage zero one Survivor PM forty three doing this, the foremost probability path is found.

3.3.5 The Decryption Block

The buffer is used at end of decoding so that the output from trace back can be produced in its original sequence at the output**.** When finding the foremost probability path, the last step is to rewrite the initial information. Initiative begins with time sample zero at the state 0. Each time, by checking consequent state in cc path and comparison it with the corresponding state within the Next state table store, we tend to may realize the computer file, one or zero. Hence, the Maximum probability path is decoded.

3.4 RESULTS OF VITERBI DECODER

Figure 3.10 shows the top level implementation of the Viterbi Decoder. Viterbi decoder uses Trellis diagram to back trace the result. Figure 3.11 shows the simulation of various different blocks used in the viterbi algorithm**.**

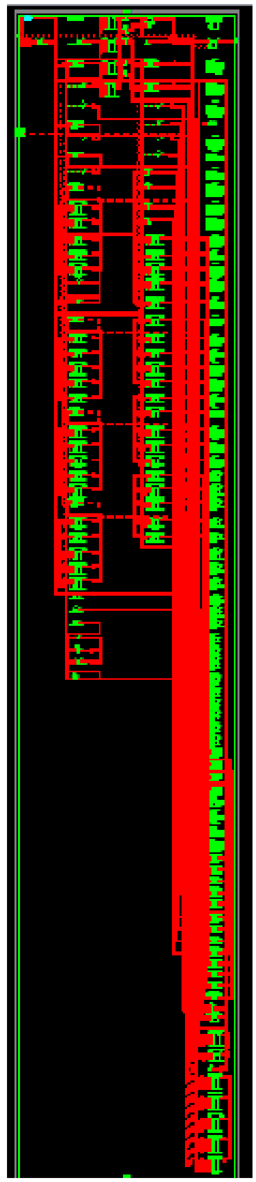

Figure 3.10: Top level Implementation of Viterbi Decoder

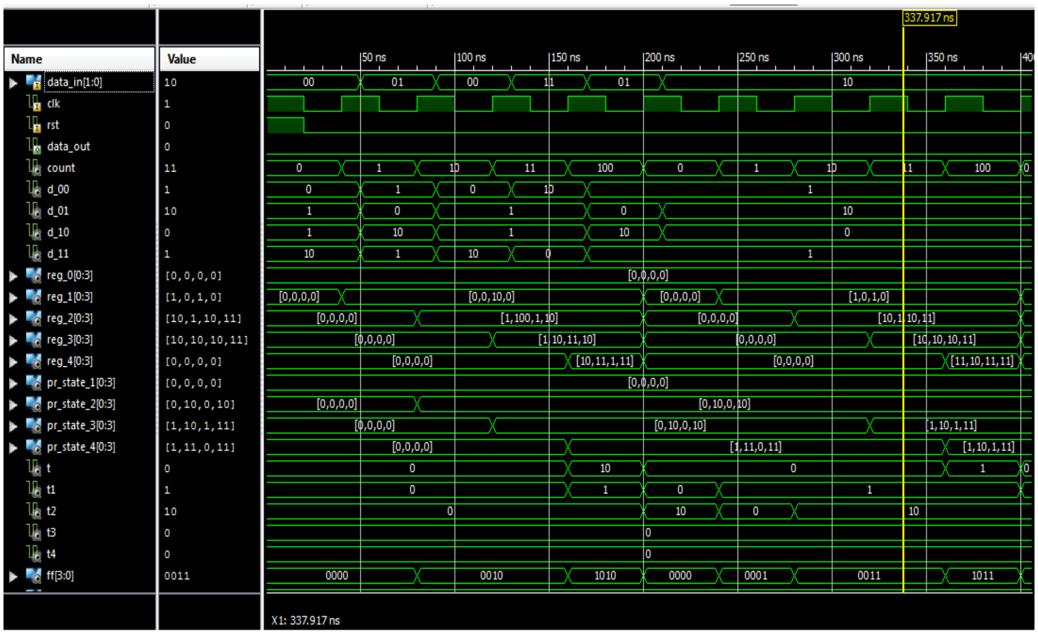

Figure 3.11: Simulation of Viterbi Decoder

CHAPTER - 4

TRUBO DCODERS

Shannon demonstrated that it is probable to send information with high-safety with condition that rate of transmission should not cross a defined value of channel capacity C which is given by

$$C = \frac{1}{2} \log 2\,(1+SNR) \text{ bits/channel}$$

Turbo codes are a category of high execution Forward Error Correction (FEC) codes. Theses codes were the first codes which were practically able to reach channel capacity. Turbo codes were brought in the picture by Berru in 1993. These codes are made up of two or more than two component codes with different interleaved sequences of the same data. In the system along two component codes, A convolutional Turbo code improves the system performance as compared to Convolutional codes. Turbo codes are used in applications where high-speed communication system as required on a very large scale because of its properties that reaches Shannon limit. It is used in 3GPP, WiMAX etc [19].

Turbo decoding consists of passing soft decision from decoder output of one to the decoder input of other. This mechanism is carried out number of times so that creates more promising decisions. Turbo codes comprises of two components connected and a feedback used between the output of a decoder to the input of another decoder in a repetitive manner. Hard decision decoders are not used as it reduces system performance. Therefore soft input- soft output decoders are required in case of Turbo codes. Turbo codes overthrow the condition of employing recursive coder as well as iterative soft coders. Convolutional codes having short constrained length emerge as block code having large length, along with this soft decoders refine the estimated received message [7].

4.1 TURBO ENCODERS

To accomplish turbo codes, a distinct type of Convolutional coders are used. Figure 4.1 shows decoder having ‘a’ as input whereas ‘a’ as well as c2 as outputs. The output of c1 is folded back and is related to its output to the input of the decoder which makes it recursive in nature**.**

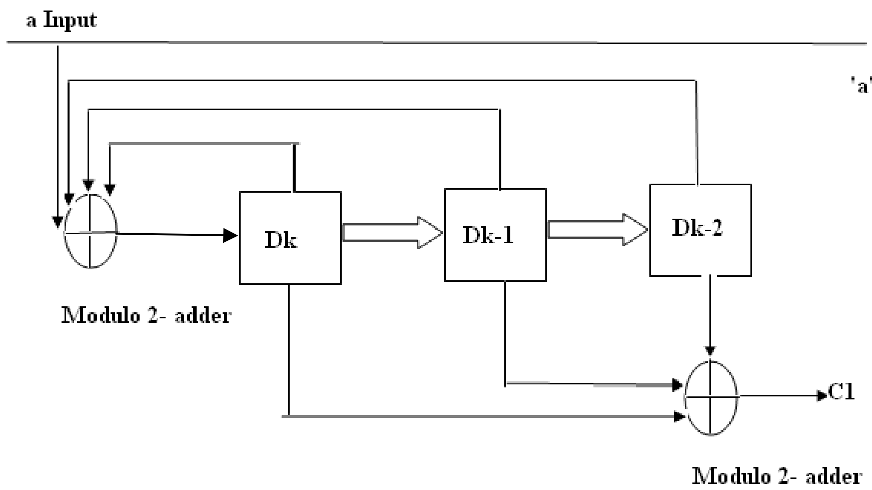

Figure 4.1: Recursive Systematic Convolutional Coder

This causes increase in input block length despite of any change in certain length. The input to coder is also produced as one of the output of the coder, so as to make it systematized. These types of coders are known as Recursive Systematic Convolutional (RSC) coders. In Non-Recursive Convolutional (NRC) coders zeros are used to add to coder so that decoder reaches its end state. This flushing of zeros is not effective in case of recursive coders.

Turbo code is parallel combination of number of RSC coders as shown in figure 4.2. Usually two RSC coders are combined so that complexity does not increase along the overhead. If this parameter increases, performance will degrade [7].

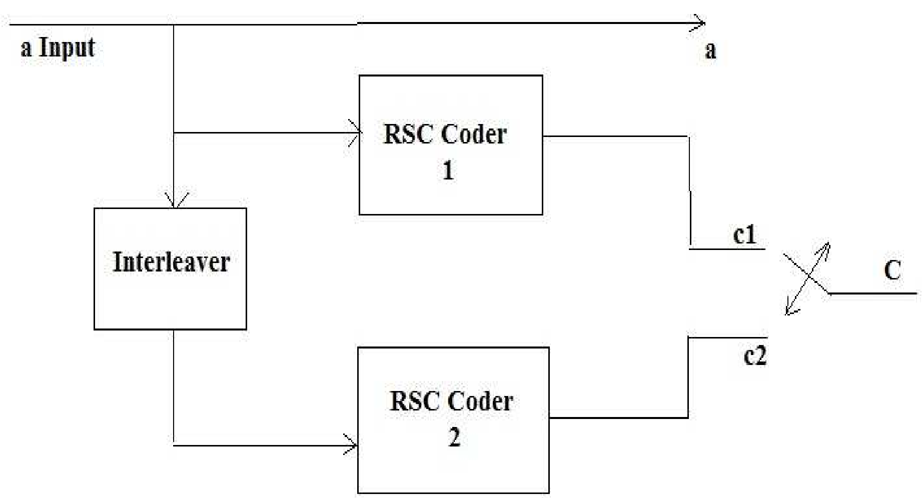

Figure 4.2: Block Diagram of Turbo Encoder (Punctured Rate= ½ Turbo Coder)

In this code input fed into second coder is interleaved interpretation of the orderly input a. This makes the output of RSC coder1 as well as RSC coder 2 being separated by time which is developed from single input sequence. The output will contain the input sequence only once. The output from two coders can be obtained by multiplexing into a sequence of data with rate R= 1/3. On the other hand output from two coder can be developed by puncturing with rate R=1/2 code as shown in figure 4.2. Interleaver is used so that coder performance can be improved. As codes with low weight can generate bad error performance, so as to make a better error performance it is necessary that any one of the two coders should be able to develop good weight codes. This is made possible by feeding interleaved interpretation of input 'a' to the RSC coder 2 which generates good weight codes where as output from the RSC coder 1 will develop low-weight codes. Block interleaver as well as pseudo random interleaver can be used but their performance is different [7] [27].

4.2 TURBO DECODING ALGORITHM

Two important decoder algorithms used are Maximum A. Posteriori (MAP) as well as Soft Output Viterbi Algorithm (SOVA).

MAP was first suggested by Bahl and was used by Berrou. He used this algorithm for use of optimal decoder. MAP finds the most apparent value corresponding to all received bits through calculating conditional probability of transformation against previous bit, when probability of previous bit is known. Transition or else state change are two focal points in the trellis which draws on Log-Likelihood Ratio (LLR) for the probability measure in case of MAP. MAP finds the most likely bit received.

SOVA is almost same as Viterbi Algorithm. It finds out the survival path using trellis and then analyzes and the sequences used to form non-survival paths. The section at which both survival path as well as non survival paths overlay each other, likelihood of the section is added to correct path and the section where there is difference between the two, likelihood of that point is decreased. After each decoding stage, the bit in the sequence are escalated the probability of excessively optimized soft outputs. Theses sequence of bits and the concerned reliability factor are assigned to interleaver for more iteration. After this SOVA decoder produces the output having maximum likelihood [12].

4.3 TURBO DECODER

Using above mentioned algorithm, decoder works when signal received at the receiver end is demodulated including the noise added to it along the channel as a consequence soft output is feed to the decoder. The soft output considers the quantized value of bit along with noise associated to it either probability related to it.

LLR is described as

$$\hat{}i = \ln p\ (m_i = 1/r')/p\ (m_i = 0/r')$$

LLR is evaluation of probability when a received soft sequence input r' is known and message bit m_i is related to change in trellis as 1 or 0. If there is equal probability of occurrence of both value than output is 0 where as any probability of m_i close to 0 or 1 results in positive or negative value of ^i.

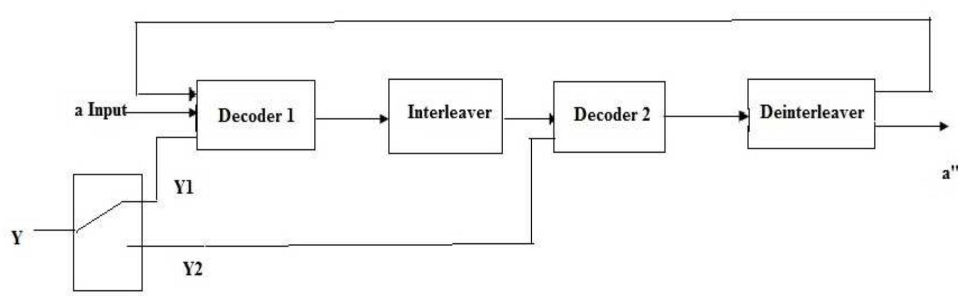

Figure 4.3: Turbo Decoder

Figure 4.3 shows the components of Turbo decoders. The input to the decoder 1 is the received sequence r' similar to the codes, where input sequence 'a' is feed to the Convolutional coder without interleaving. Similar input to the decoder 2 is the output of decoder 1 passed through interleaver as in case of codes where Convolutional coder 2 has input same as Convolutional coder 1 after interleaving. Decoder needs some information about the probability of transmitted signal i.e. a priori knowledge exists at the decoder used for the assistance which counts up to the information received from decoding process called as a posteriori output. Decoder makes best use of all information known so as to make good estimation of received sequence. Output is then feed into deinterleaver and feedback to decoder1 so to make good estimation. This process of decoding using interleaver and deinterleaver makes the estimated output equal to input [7].

4.3.1 Top Level Controller

Turbo decoder operates on blocks of knowledge, the external memory is employed to produce a standardized interface between modules. Every module receives a listing of memory pointers for its inputs and outputs. This methodology preserves the flexibleness and mobility of the look, and it's the extra advantage of eliminating temporal order problems that might occur if the modules were directly interfaced on the FPGA. The highest level controller, whose purpose is to activate the modules within the correct order and to perform access, manages the turbo decryption method, Individual modules area unit activated once the management unit sends ”start” signal and a group of memory tips to that module. The active module is then connected to the memory by the memory arbitration unit. The management unit, that performs the particular access, deactivates the present module upon receiving “done” signal from that module. The controller then activates extra modules so as to finish the present decryption iteration. Extra decryption iterations area unit performed during this manner till the iteration limit or a given convergence criteria is met. as a result of the management theme and memory arbitration stop correspondence, modules is created rather generically. Generic module styles area unit ready to serve over one purpose and this ultimately reduces chip space by avoiding unneeded duplication of hardware logic on the FPGA. The decoder module will operate as either SISO #1 or SISO #2, and therefore the interleave module is capable of each interleaving and interleaving a knowledge frame.

4.3.2 Interleaver Module

Although the operation of interleaver module for an improved turbo decoder remains unchanged from initial implementation, the FSM had to be altered since information is accessible sooner when a memory request. The interleaver uses a read\write theme while which just one interleaving pattern is keep in memory. This methodology was chosen owing to its quantify ability and move ability. Once operational in interleaving mode, the module reads information in keeping with the interleaving pattern and writes the information linearly. Once operational in interleaving mode, the module reads information linearly and writes the result in keeping with the interleaving pattern.

4.3.3 Adder Module

The adder module for an improved decoder is a smaller amount complicated than the initial adder. The adder module reads 2 values from memory, adds them along, thus writes the result to memory. Initial the number is requested from memory. Then within the next state the number is registered, and therefore the number is requested from memory. Associate in idle state is inserted to register the number. Finally, add is written, and therefore the method repeats. Once the counter is adequate to the frame size, the process loop is broken, and therefore the adder returns to its prepared state.

4.3.4 Decoder Module

Because the SISO decoder's area unit computationally is similar, the decryption module is meant to control as either the primary or second constituent decoder. This protects chip-area by avoiding the unneeded duplication of hardware logic; the decoders, however, area unit enforced in slightly other ways owing to their several practicality. The improved decoder module has been altered slightly from the initial style. These changes area unit mirrored in an each the decoder's simultaneous VHDL statements and in its FSM.

4.4 RESULTS OF TURBO DECODER

Figure 4.4 shows the top level module of the turbo decoder. In turbo decoder two viterbi decoder units are used along with the interleaver and deinterleaver. Figure 4.5 shows the simulation of turbo decoder.

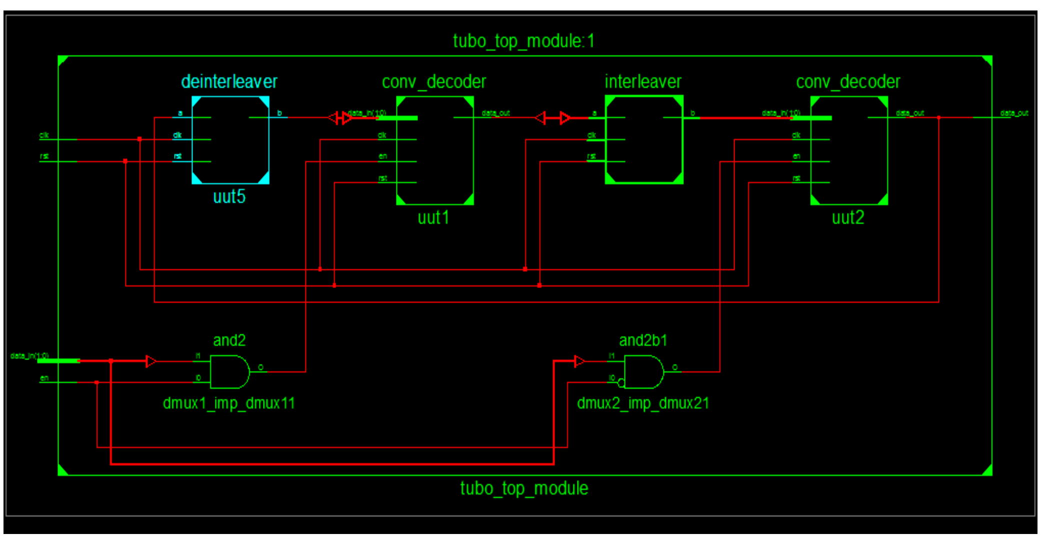

Figure 4.4: Top Module of Turbo Decoder

Figure 4.5: Simulation of Turbo Decoder

CHAPTER - 5

LOW-DENSITY PARITY-CHECK DECODERS

Low-density parity-check (LDPC) codes are a category of Block codes which was originally discovered by Gallager but were reconsidered later and become Mackay-Neal code which replaced Turbo codes being FEC method. They found that the decoding algorithm for turbo codes seems to be a exclusive case of LDPC codes that were determined by Gallager. Presently LDPC codes are designed such that they approach Shannon's capacity. LDPC codes are mentioned using a matrix containing maximum number of 0's and less number of 1's. A (n, j, k) is LDPC code having block length n where each column includes a very small amount of j i.e. number of 1's in row. LDPC codes procure near to Shannon's channel capacity. In 1981, Tanner gave a graphical representation method to represent LDPC codes which came to be known as Tanner graph.

LDPC has gained more popularity as its capacity to execute near capacity and strong coding method with enough large code word length. LDPC codes produced a very throughput due to its mechanism of parallel processing where as Turbo cannot have parallel processing mechanism as it executes sequentially. A large delay is produced while using Turbo codes where as there is no need of interleaver in LDPC codes [1].

5.1 PARITY-CHECK ENCODER

In FEC codes, the important is to add the redundant bits to message bits to generate code words. The check bits are combined in way that the code words generated are all unique. Let 7-bit ASCII code for S is $[\mathbf{1010011}]$ and parity bit is added at eight bit. Therefore the codeword C becomes as

$$\boldsymbol{C} = [\boldsymbol{c1}, \boldsymbol{c2}, \boldsymbol{c3}, \boldsymbol{c4}, \boldsymbol{c5}, \boldsymbol{c6}, \boldsymbol{c7}, \boldsymbol{c8}]$$

Where the value of all these bits is either 0 or 1 and to generate parity i.e. value of eight bit must satisfy following equation.

$$\boldsymbol{C1} \oplus \boldsymbol{C2} \oplus \boldsymbol{C3} \oplus \boldsymbol{C4} \oplus \boldsymbol{C5} \oplus \boldsymbol{C6} \oplus \boldsymbol{C7} \oplus \boldsymbol{C8} = \boldsymbol{0}$$

The above equation is called as Parity Check equation for single parity which consists of modulo 2 additions. If a code consist of six elements i.e. $\boldsymbol{C} = [\boldsymbol{c1}\ \boldsymbol{c2}\ \boldsymbol{c3}\ \boldsymbol{c4}\ \boldsymbol{c5}\ \boldsymbol{c6}]$

Then it should satisfy the following three equations for generating parity bits.

$$\boldsymbol{C1 \oplus C2 \oplus C4 = 0}$$
$$\boldsymbol{C2 \oplus C3 \oplus C5 = 0}$$
$$\boldsymbol{C1 \oplus C2 \oplus C3 \oplus C8 = 0}$$

A generator matrix (G Matrix) is used at the encoder and parity check matrix (H Matrix) is used at encoder and decoder respectively. H and G matrices are orthogonal to each other in nature. H Matrix has m number of rows and n number of columns where m represents check nodes and n represents variable nodes. When number of 1's in column are same and number of 1's in column are different than the matrix so called is Regular Matrix. In another case H matrix is called Irregular Matrix. The structure of H matrix helps in defining BER. The above equations can be written in matrix form as

$$\begin{bmatrix} 1 & 1 & 0 & 1 & 0 & 0 \\ 0 & 1 & 1 & 0 & 1 & 0 \\ 1 & 1 & 1 & 0 & 1 & 1 \end{bmatrix} \begin{bmatrix} c1 \\ c2 \\ c3 \\ c4 \\ c5 \\ c6 \end{bmatrix} = \begin{bmatrix} 0 \\ 0 \\ 0 \end{bmatrix}$$

Rows of H matrix represent Parity Check equation and Column of matrix represents bits. H matrix is of dimension m× n matrix where m is number of parity check constrain and n is length of codeword in matrix. Therefore for a codeword to be valid

$y = [c1, c2, c3, c4, c5, c6]$ and

H matrix is related as $HyT = 0$. So code constraint can be written as

$$c4 = c1 \oplus c2$$
$$c5 = c2 \oplus c3$$
$$c6 = c1 \oplus c2 \oplus c3$$

The bits c1, c2, c3 are three message bits in codeword where as c4, c5, c6 are parity bits. For example if three message bits are [111] then codeword can be written as

$$[c1, c2, c3, c4, c5, c6] = [u1, u2, u3] \begin{bmatrix} 1 & 0 & 0 & 1 & 0 & 1 \\ 0 & 1 & 0 & 1 & 1 & 1 \\ 0 & 0 & 1 & 0 & 1 & 1 \end{bmatrix}$$

G is a Generator matrix. Therefore

$$C = [U]\,[G]$$

Where message bits $U = [u1, u2, u3]$

$$G = \begin{bmatrix} 1 & 0 & 0 & 1 & 0 & 1 \\ 0 & 1 & 0 & 1 & 1 & 1 \\ 0 & 0 & 1 & 0 & 1 & 1 \end{bmatrix}$$

G matrix is k× n matrix where k is number of message bits as well as length of codeword is n. Rate of code is defined as k/n .the code is said to be symmetric if the starting k bits of codeword represents the message bits. G and H matrices can be obtained by using Gauss-Jordan Elimination method on H and the obtained will be

$$H = [P, In - k]$$

Where p is binary matrix of (n-k) × k and I_{n-k} is identity matrix of order (n-k) and generator matrix is given by

$$G = [I\ k, PT]$$

From above it is concluded that two rows of G matrix are orthogonal to H matrix .For a proper decoding $GH^T = 0$. For detection and correction of the error the equation used is

$$S = HyT$$

Here S is syndrome of y. Syndrome tells which parity-check equation gives a value which do not satisfy y. The hamming distance calculated between two code words is the number of positions of bits they differ. The hamming distance between [10100110] as well as [10000111] is two [1] [32].

5.2 BELIEF-PROPAGATION DECODER ALGORITHM

Belief-Propagation Algorithm (BP) was proposed by Judea Pearl in 1982 and is graph based algorithm that is used for decoding. It is iterative in nature as works as follow. Message travels in both directions along the edge. The message from node is computed depending upon all the messages that have reached the particular node at the time of previous iterations. At the time all the iterations are completed, persuasion in context to each variable is approximated depending upon the all the messages that have reached that variable node. Messages are updated depending upon weather graph is cyclic or acyclic. If it is acyclic then belief approaches exactly same solution marginals where as in case of cyclic graphs it doesn't give marginal values [26].

5.3 DECODING OF LDPC CODES

LDPC codes are generally made up of pseudo random sequence and are represented I graphical way. Tanner graph is made up of two apex, one is bit node which are n in number representing codeword and another is check node which are m in number to represent Parity check equations. An edge is used to join bit node to check node if that particular bit is represented in Parity-check equation. This concludes that number of edges in Tanner graph represent. Let H parity check matrix for a code is given as

$$H = \begin{bmatrix} 1 & 1 & 0 & 1 & 0 & 0 \\ 0 & 1 & 1 & 0 & 1 & 0 \\ 0 & 0 & 1 & 1 & 0 & 1 \end{bmatrix}$$

The Tanner Graph for the above matrix is shown in figure 5.1. The bit apex is denoted by circular node also called as left node or variable node and check apex is denoted by square nodes which are also called as right node or constraint node. The cycle is chain of apex connected and that starts and ends at same apex of the graph where as other vertices should not exist more than once. Length of the cycle is considered as total number of edges in the cycle and size of smallest cycle is called as grith of graph [1][40]

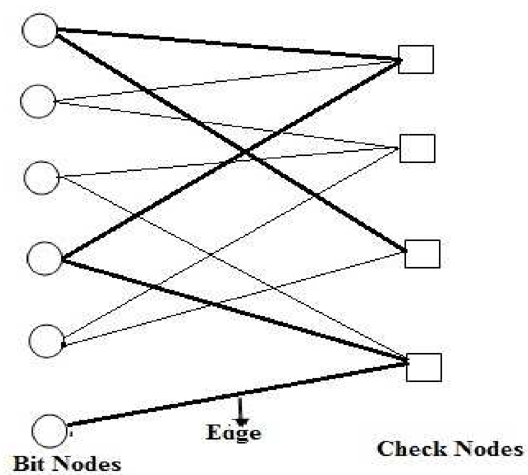

Figure 5.1: Tanner Graph

5.4 METHODOLOGY FOR LDPC DECODERS

A linear code includes a check matrix illustration and a bipartite Tanner graph. All linear codes aren't sparsely drawn. A distributed graph includes a property that in an exceedingly n x m matrix, the amount of 1's in an exceedingly row of row weight and therefore the number of 1's in an exceedingly column of column weight satisfies that the 1's square measure a lot of but the matrix dimension ($\boldsymbol{w_r} \ll \boldsymbol{m}, \boldsymbol{w_c} \ll \boldsymbol{n}$). This kind of code that is drawn during this manner is thought as tenacity Parity check Code (LDPC).

The algorithmic rule projected during this work is difficult call coding algorithmic rule and is popularly referred to as BP (Belief Propagation) algorithm.

The graph for BP algorithm is displayed in figure 5.2.

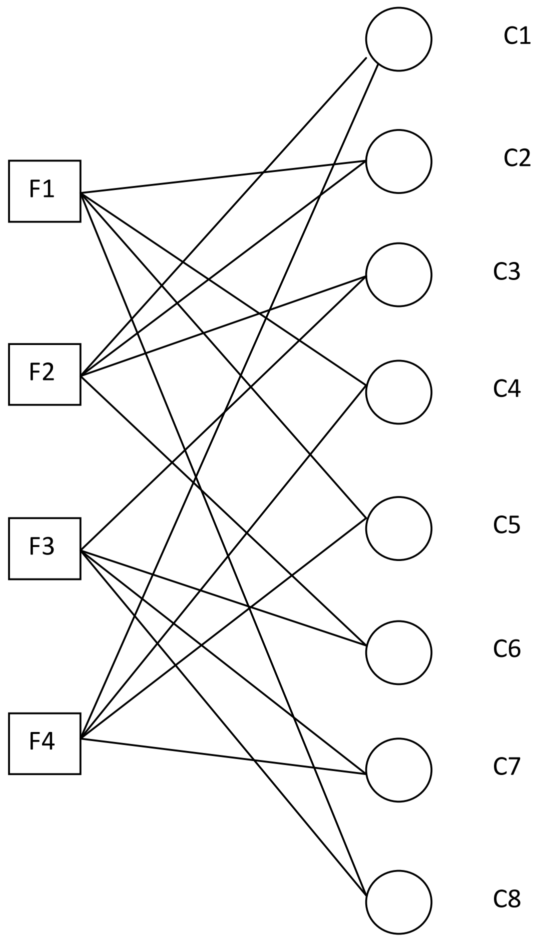

Figure 5.2: Graph of BP Algorithm

The parity check matrix of code shown in figure 2 is given as

$$\begin{bmatrix} \mathbf{0} & \mathbf{1} & \mathbf{0} & \mathbf{1} & \mathbf{1} & \mathbf{0} & \mathbf{0} & \mathbf{1} \\ \mathbf{1} & \mathbf{1} & \mathbf{1} & \mathbf{0} & \mathbf{0} & \mathbf{1} & \mathbf{0} & \mathbf{0} \\ \mathbf{0} & \mathbf{0} & \mathbf{1} & \mathbf{0} & \mathbf{0} & \mathbf{1} & \mathbf{1} & \mathbf{1} \\ \mathbf{1} & \mathbf{0} & \mathbf{0} & \mathbf{1} & \mathbf{1} & \mathbf{0} & \mathbf{1} & \mathbf{0} \end{bmatrix}$$

Suppose we receive codeword and error free code $\boldsymbol{y} = [\mathbf{1\ 1\ 0\ 1\ 0\ 1\ 0\ 1}]^{\boldsymbol{T}}$ and the error free codeword $\boldsymbol{c} = [\mathbf{10010101}]^{\boldsymbol{T}}$. The Algorithm used for the procedure is represented in steps as:

Step 1: Within the opening move, all message nodes send a message to their connected check nodes. During this case, the message is that the bit they believe to be correct for them. As an example, message node c2 receives a one (y2=1), therefore it sends a message containing one to ascertain nodes f1 and f2. Table 5.1 illustrates this step.

Step 2: Within the second step, each check nodes calculate a response to its connected message nodes victimization messages they receive from step one. The response message during this case is that the price (0 or 1) that the check node believes the message node has supported the knowledge of alternative message nodes connected thereto check node. This response is calculated victimization the parity-check equations that force all message nodes hook up with a specific check node to total to zero (mod 2). In Table 5.1, check node f1 receives one from c4, 0 from c5, one from c8 so it believes c2 has zero (1+0+1+0=0), and sends that data back to c2. Similarly, it receives one from c2, 1 from c4, one from c8 so it believes c5 has one (1+1+1+1=0), and sends one back to c5. At now, if all the equations the least bit check nodes square measure happy, that means the values that the check nodes calculate match the values they receive, the algorithmic rule terminates. If not, we have a tendency to go on to step three.

Step 3: During this step, the message nodes use the messages they get from the check nodes to make a decision if the bit at their position may be a zero or a one by philosophy. The message nodes then send this hard-decision to their connected check nodes. Table 5.1, a pair of illustrates this step to form it clear, allow us to scrutinize message node c2. It receives a pair of 0's from check nodes f1 and f2. alongside what it already has y2 = one, it decides that its real price is zero. It then sends this data back to ascertain nodes f1 and f2.

Step 4: Repeat step a pair of till either exit at step a pair of or a precise range of iterations has been passed. During this example, the algorithmic rule terminates right once the primary iteration as all parity check equations are happy. c2 is corrected to zero.

Table 5.1: Message Passing Table

Check Nodes	Activities				
F1	Receive	$c_2 \rightarrow 1$	$c_4 \rightarrow 1$	$c_5 \rightarrow 0$	$c_8 \rightarrow 1$
	Send	$0 \rightarrow c_2$	$0 \rightarrow c_4$	$1 \rightarrow c_5$	$0 \rightarrow c_8$
F2	Receive	$c_1 \rightarrow 1$	$c_2 \rightarrow 1$	$c_3 \rightarrow 0$	$c_6 \rightarrow 1$
	Send	$0 \rightarrow c_1$	$0 \rightarrow c_2$	$1 \rightarrow c_3$	$0 \rightarrow c_6$
F3	Receive	$c_3 \rightarrow 0$	$c_6 \rightarrow 1$	$c_7 \rightarrow 0$	$c_8 \rightarrow 1$
	Send	$0 \rightarrow c_3$	$1 \rightarrow c_6$	$0 \rightarrow c_7$	$1 \rightarrow c_8$
F4	Receive	$c_1 \rightarrow 1$	$c_4 \rightarrow 1$	$c_5 \rightarrow 0$	$c_7 \rightarrow 0$
	Send	$1 \rightarrow c_1$	$1 \rightarrow c_4$	$0 \rightarrow c_5$	$0 \rightarrow c_7$

Table 5.2: Final Result

Message Nodes	y_i	Message from Check Nodes		Decision
C1	1	$f_2 \rightarrow 0$	$f_4 \rightarrow 0$	1
C2	1	$f_1 \rightarrow 0$	$f_2 \rightarrow 0$	0
C3	0	$f_2 \rightarrow 0$	$f_3 \rightarrow 0$	0
C4	1	$f_1 \rightarrow 0$	$f_4 \rightarrow 0$	1
C5	0	$f_1 \rightarrow 0$	$f_4 \rightarrow 0$	0
C6	1	$f_2 \rightarrow 0$	$f_3 \rightarrow 0$	1
C7	0	$f_3 \rightarrow 0$	$f_4 \rightarrow 0$	0
C8	1	$f_1 \rightarrow 0$	$f_3 \rightarrow 0$	1

The proposed methodology is implemented on Xilinx Spartan 3 FPGA. The language used for coding the methodology is VHDL and the tools used for synthesis and simulation is Xilinx ISE.

5.5 RESULTS OF LDPC DECODER:

LDPC is implemented using the Belief Propagation algorithm and the top module of the approach is shown in Figure 5.3.

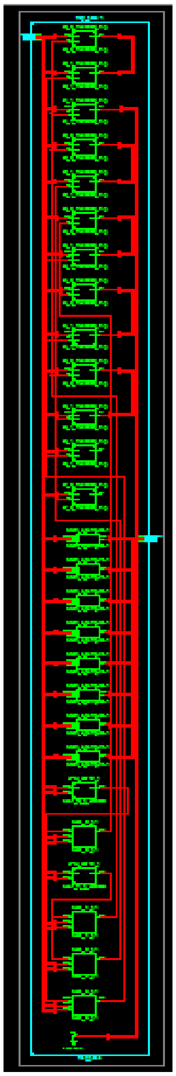

Figure 5.3: LDPC Implementation

Figure 5.4 shows the various simulation waveforms, and is performed on few test cases and the waveform shows the correct implementation of the same.

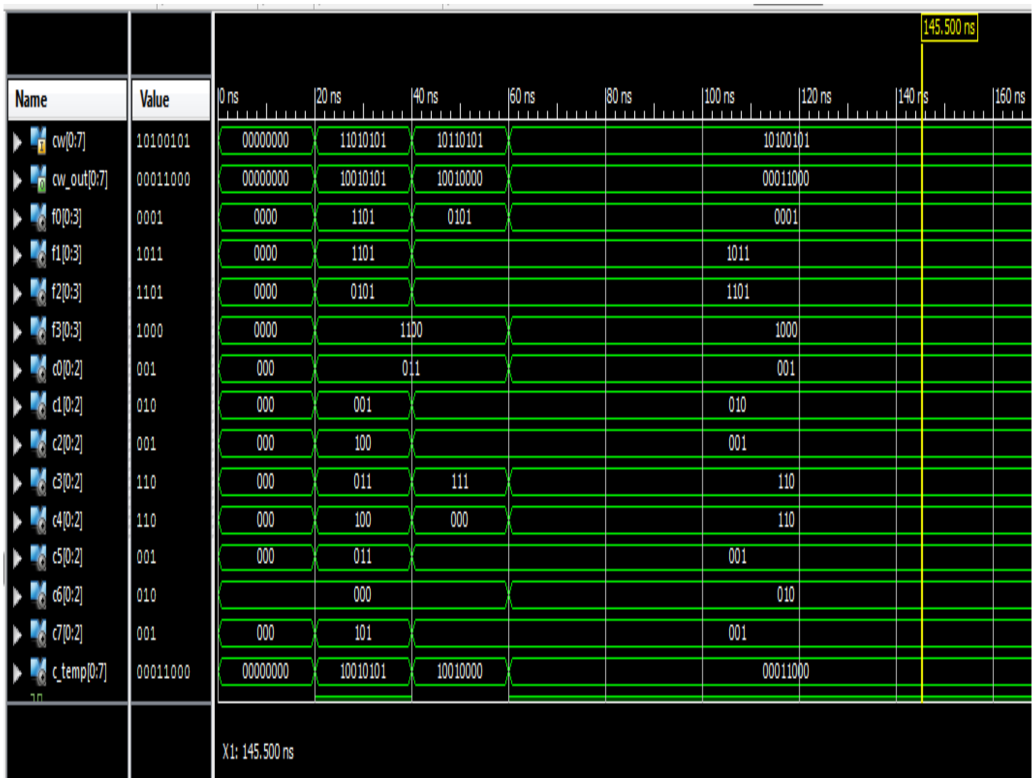

Figure 5.4: Simulation of Low Density Parity Check Code

CHAPTER - 6

CONCLUSION AND FUTURE SCOPE

6.1 CONCULSION

Three decoding techniques used in WiMAX have been implemented using Spartan 3 FPGA and result is verified. The result is analyzed on the basis of area used, power consumed, frequency required and the delay in obtaining the output. Table 6.1 shows the comparison of the decoders proposed in the last section. Various performance parameters are considered for the comparison like number of resources used, operating frequency, power utilized by the circuit and delay.

Table 6.1: Comparison Table for Decoders

Parameters	LDPC Decoder	Viterbi Decoder	Turbo Decoder
No. of Slices Used	16	175	349
No. of 4 input LUTs	17	310	612
No. of Bonded IOs	5	5	6
No. of Slice flip flops	29	74	147
Delay (ns)	6.0	6.21	6.28
Frequency (MHz)	166.6	161.03	159.23
Power (mW)	0.459	8.37	16.524

Following Conclusions have been obtained from these results.

- Low Density Parity Check code takes less area and less power compared to the other two codes. As these codes are simple and easy to implement, they are less suitable for many applications which requires high robustness and are only used in blocks of data.

- Viterbi and Turbo decoders are implemented. Out of these Turbo decoders uses more area as it requires two Convolutional decoders.
- The delay provided by the Turbo decoder is slightly more of about 0.07ns than Viterbi decoder but consumes more power. Theses both codes are used in linear decoding techniques.

6.2 FUTURE SCOPE OF WORK

In future, other decoding algorithms must be implemented and Viterbi decoder must also be implemented using some other logic like Log-Map decoder and their results must be compared and tested. The change in the parameters with the increase in size of decoder using the above mentioned algorithms can also be verified.

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