LOW-VOLTAGE CMOS ANALOG MULTIPLIERS

A thesis submitted in partial fulfilment of the requirements for the award of degree of

Master of Technology (VLSI design and CAD)

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CERTIFICATE

I hereby declare that the work, which is being presented in the thesis, entitled **"LOW-VOLTAGE CMOS ANALOG MULTIPLIERS"** in partial fulfilment of the requirements for the award of degree of Master of Technology in VLSI Design & CAD at Department of Electronics and Communication Engineering, Thapar University, Patiala, is an authentic record of my own work carried out under the guidance of Mr. Rishikesh Pandey, Assistant Professor, ECED.

The matter presented in this thesis has not been submitted in any other University/Institute for the award of any degree.

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ABSTRACT

Real-time analog multiplication of two signals is one of the most important operations in analog signal processing. Multiplier is such an important element which contributes substantially to the total power consumption of the system. On VLSI level, the area also becomes quite important as more area means more system cost. Speed is another key parameter while designing a multiplier for a specific application. These three parameters power, area and speed are always traded off. The multiplier is used not only as a computational building block but also as a programming element in systems such as filters, neural networks, and as mixers and modulators in a communication system. Different multipliers based on different topologies such as V-I convertor, differential amplifier, summing and squaring circuits, etc have been discussed. These structures of multipliers have been simulated using spectre (Cadence) tool. The simulation results of the multiplier presented in this thesis have been compared which confirm the effectiveness of the circuits.

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LIST OF SYMBOLS

K Transconductance parameter

V_{gs} Gate to Source voltage

V_{dd} Supply voltage

I_d Drain current

V_{th} Threshold voltage

V_o Output voltage

C_L Load Capacitance

W Width of MOSFET

L Length of MOSFET

V_d Differential input voltage

V_c Common mode voltage

V_{ss} Source voltage

CHAPTER

1 INTRODUCTION

1.1 MOTIVATION AND INTRODUCTION

The main motivation for choosing Analog multiplier is its importance in nonlinear analog signal processing function finding application of a wide variety in adaptive filtering, modulation, frequency translation, automatic gain controlling, neural network, fuzzy integrated systems, etc. The linearity, speed, supply voltage and power dissipation are the main goals of design. At present, the power consumption is a key parameter in the design of high performance mixed-signal integrated circuit.

MULTIPLIERS perform linear products of two signals x and y yielding an output z =kxy where k is a multiplication constant with suitable dimension. Multipliers are often categorized as single-quadrant (x and y are unipolar), two-quadrant (where x or y can be bipolar), and four-quadrant multipliers (where both x and y can be bipolar). Noise and bandwidth are often not optimized for multipliers. Modulator and mixer are particular cases of multipliers that are designed with noise and frequency constraints. The history of the analog multipliers is originated from its use as a mixer and as an amplitude modulator which involves a multiplication of two signals.

The basic idea of the multiplier implementation is illustrated in Fig. 1.1 Two signals, $v_1(t)$ and $v_2(t)$ are applied to a nonlinear device, which can be characterized by a high- order polynomial function. This polynomial function generates terms like $v_2^2(t)$, $v_1^2(t)v_2(t)$, $v_2^2(t)$ and many others besides the desired $kv_1(t)v_2(t)$ .Then it is required to cancel the undesired components. This is accomplished by a cancellation circuit configuration.

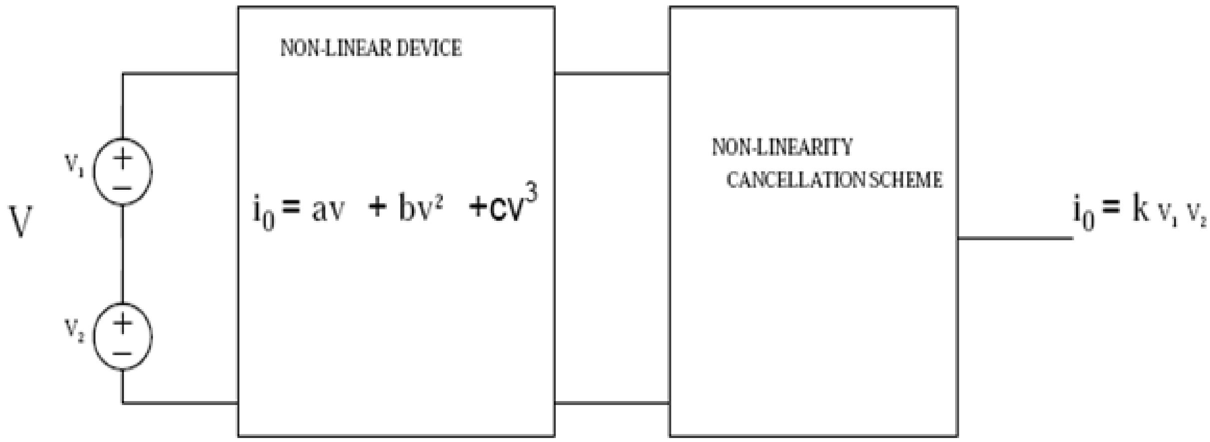

Figure: 1.1 Basic multiplier circuit [4]

The basic four quadrant analog multiplier can be implemented using single quadrant multipliers and square devices. The multiplier has two inputs so there are four combinations (X, Y), (-X, Y), (-X,-Y), (X.-Y).

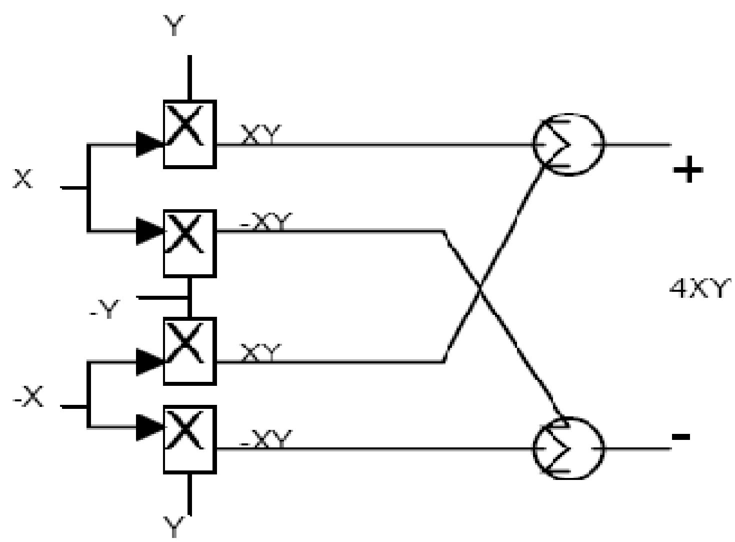

Figure1.2 Four quadrant multiplier using single quadrant multipliers [4]

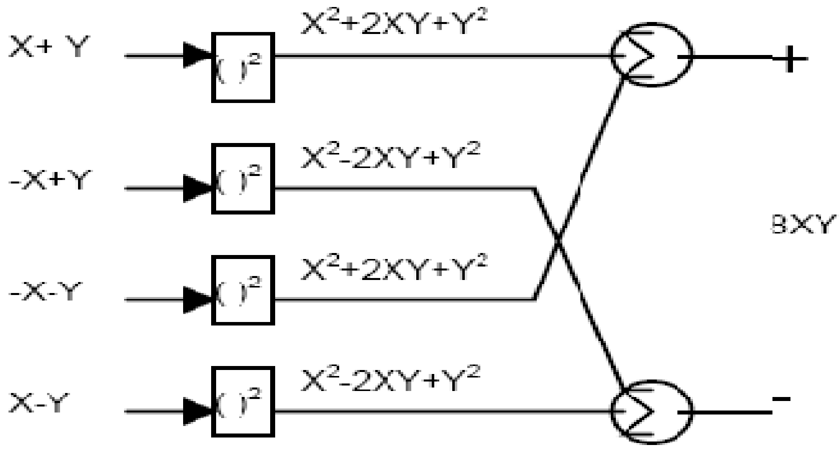

Figure1.3 Four quadrant multiplier using square devices [4]

The basic symbol of the multiplier is given below.

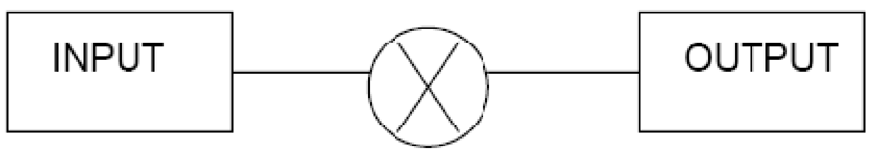

Figure 1.4 Basic multiplier symbol [5]

The Main specifications of a multiplier are:

LINEARITY: It indicates the factor by which the output is dependent on the input parameters linearly. for a multiplier the error in linearity should be very less so that for any change in the inputs output changes linearly.

SUPPLY VOLTAGE AND POWER CONSUMPTION: This factor tells us the amount of power supply required for the whole circuit and according to the power supply requirements and the components used power consumption can be determined. For a multiplier low power supply voltage is required and minimum no of transistors should be used so that power consumption is less.

BANDWIDTH: The range of frequencies for which the gain of a particular circuit is constant gives the bandwidth of the system. For a multiplier the bandwidth should be high so that it works properly for high frequencies.

TOTAL HARMONIC DISTORTION: The total harmonic distortion, or THD, of a signal is a measurement of the harmonic distortion present and is defined as the ratio of the sum of the powers of all harmonic components to the power of the fundamental frequency. Lesser THD allows the components in a loudspeaker, amplifier or microphone or other equipment to produce a more accurate reproduction by reducing harmonics added by electronics and audio media. A THD rating < 1% is considered to be in high-fidelity and inaudible to the human ear.

When a signal passes through a non-ideal, non-linear device, additional content is added at the harmonics of the original frequencies. THD is a measurement of the extent of that distortion. When the input is a pure sine wave, the measurement is most commonly the ratio of the sum of the powers of all higher harmonic frequencies to the power at the first harmonic, or fundamental frequency.

In the case of a multiplier, the value of THD should be less, this can be reduced by reducing the non-linear terms that exist in the output of the multiplier.

The main applications of a multiplier is in communication systems to process any given analog signals which include Frequency mixers, Amplitude modulators, Adaptive filters, Phase-locked loop, Automatic gain control

BRIEF LITERATURE REVIEW:

Several multiplier circuits have been proposed in literature. Bult and Wallinga [2] have proposed a CMOS four quadrant multiplier, which consists of pair of linear V-I converters and current mirrors. Prommee and Somdunyakanok [3] have presented CMOS wide range four quadrant multiplier by using an active attenuator and shunt feedback circuit. Akshatha and Kumar [5] have suggested a low-power, low-voltage .high linearity analog multiplier which is developed by using cascaded structure of NMOS transistors and a differential amplifier. Wang [6] has presented a four transistor four quadrant multiplier by using a pair of differential amplifiers. Boonchu and Surakampontorn [7] have proposed a NMOS voltage mode multiplier, which consists of summer and subtractor circuits. Naderi, Mojarrad, Ghasemzadeh, Khoei and Hadidi [8] have presented a four quadrant CMOS analog multiplier using a current mode squarer and subtractor circuits. Chih**,** Tian, Ole, and Torben [9] have proposed a low power fully differential ultra wide band CMOS multiplier which is developed by using two pairs of differential amplifiers and PMOS transistors as load. Chutham, Andreas, and Pal [10] have presented a low voltage low power high linearity CMOS multiplier using a combiner and subtractor circuits.

1.2 THESIS ORGANIZATION:

This thesis is organized as follows

Chapter 1 Introduction:

This chapter presents the introduction of analog multiplier, applications and specifications of analog multiplier and a brief literature review of analog multipliers

Chapter 2 CMOS Analog Multipliers

This chapter presents basic CMOS analog multipliers which are mostly used in various applications based on differential amplifier and linear V- I convertor and their internal description is presented

Chapter 3 Low-Voltage Analog Multipliers

This chapter presents low-voltage analog multipliers which use simple subtractor, combiner, summing and squarer circuits to implement a multiplier. The two multipliers are discussed in detail along with the mathematical equations associated with them.

Chapter 4 Simulation and Layout Results

This chapter presents the simulation results and layout of low-voltage analog multipliers discussed in chapter 3 and the results are compared.

Chapter 5 Conclusions and further development

Finally the thesis is concluded and scope for further development is discussed in this chapter.

CHAPTER

2 CMOS ANALOG MULTIPLIERS

2.1 INTRODUCTION

An analog multiplier is an importance basic building block for the design of analog nonlinear function circuits. Usually, the variable transconductance technique which operates on Gilbert's translinear circuit is widely used for the design of multiplier circuits in Bipolar and CMOS technologies. The other approaches in CMOS technology are that based on square-law characteristics of MOS transistor which are biased in saturation region and that based on the current voltage characteristics of MOS transistor in the nonsaturation region Unfortunately, many of the techniques require resistors to obtain the output signal in voltage form. The use of resistors may require external resistors, or occupy large chip area to implement in IC form and also cause of the multiplier frequency degradation. Only few types of the multipliers that can produce the output voltage without the use of resistors. In this chapter two types of basic CMOS analog multipliers are discussed. The organization of this chapter is as follows: Differential multiplier is discussed in section 2.2 and simple CMOS multiplier is discussed in section 2.3.

2.2 DIFFERENTIAL MULTIPLIER

Differential Multiplier uses the basic concept of BJT GILBERT multiplier. This circuit is the most commonly used analog multiplier in various applications as it gives high linearity. It uses two differential pairs to form a four quadrant analog multiplier

2.2.1 TWO QUADRANT MULTIPLIER USING DIFFERENTIAL AMPLIFIER

Two quadrant multiplier shown in Figure 2.1 is formed by taking the difference of two output currents of a normal differential amplifier. The drain current of a NMOS transistor is given as

$$I_d = \frac{K}{2}\ (v_{gs} - v_t)^2 \qquad (2.1)$$

where $K = \mu C_{ox}\frac{W}{L}$, μ is the mobility of the carriers, C_{ox} is the gate capacitance per unit area, W and L are channel width and length of the device, v_{gs} is the gate to source voltage, v_t is threshold voltage. From (2.1) the drain currents of M1 and M2 are

$$I_{d1} = \frac{K}{2}(\frac{V_x}{2} - V_B - V_t)^2 \qquad (2.2)$$

$$I_{d2} = \frac{K}{2}(-\frac{V_x}{2} - V_B - V_t)^2 \qquad (2.3)$$

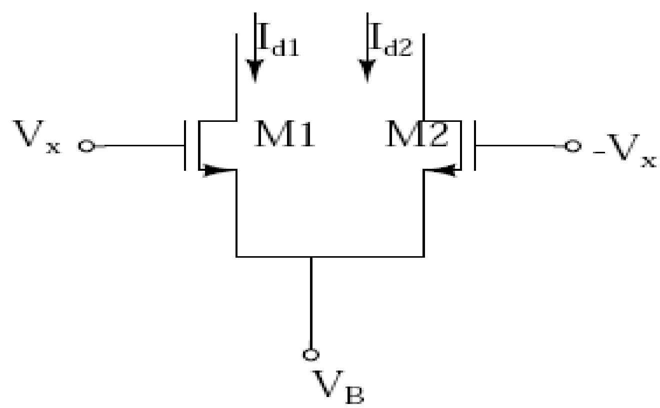

Figure 2.1 two quadrant multiplier [6]

The difference of currents gives

$$I_{d1} - I_{d2} = -K(V_B + V_t)V_x \qquad (2.4)$$

From (2.4) it can be seen that difference of currents is the multiplication of two input voltages V_B and V_x .

Thus a normal differential amplifier can be operated as a two quadrant multiplier. Differential Four quadrant multipler shown in figure 2.2 is formed by duplicating two quadrant multiplier and resistors are connected as load.

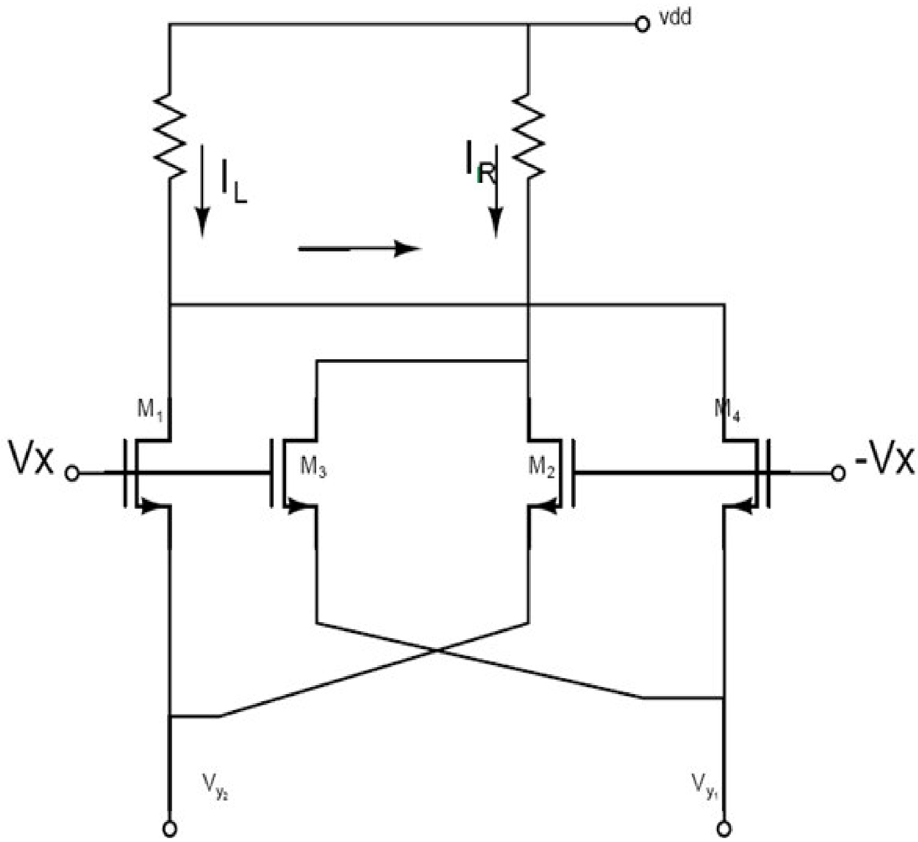

Figure 2.2 differential four quadrant multiplier [6]

$$I_L - I_R = (I_{D1} - I_{D2}) - (I_{D3} - I_{D4}) \tag{2.5}$$

$$I_{D1} - I_{D2} = -k(V_{Y2} + V_T)V_X \tag{2.6}$$

$$I_{D3} - I_{D4} = -k(V_{Y1} + V_T)V_X \tag{2.7}$$

Substituting (2.6) and (2.7) in (2.5) and the whole equation is multiplied by R we get output voltage V_0 as

$$V_0 = R\,(I_L - I_R) = KRV_XV_Y \tag{2.8}$$

Thus from (2.8) it can be seen that output voltage V_0 is multiplication of two input voltages V_X and V_Y.

2.3 SIMPLE CMOS MULTIPLIER

Simple CMOS Multiplier is implemented using a V-I convertor, this V-I convertor is duplicated to form a two quadrant multiplier. It uses less no of transistors, PMOS transistors are used as load instead of resistors to improve accuracy.

2.3.1 V-I CONVERTOR

A pair of NMOS transistors connected as shown in figure 2.3 makes V-I convertor. The gate–source voltages of the two identical MOS transistors Ml and M2 are, respectively, v_{gs1}andv_{gs2}. The sum of the gate–source voltages is kept at a constant voltage V_2

$$v_{gs1} + v_{gs2} = V_2 \tag{2.9}$$

$$I_{d1} = k(v_{gs1} - v_t)^2 \tag{2.10}$$

$$I_{d2} = k(v_{gs2} - v_t)^2 \tag{2.11}$$

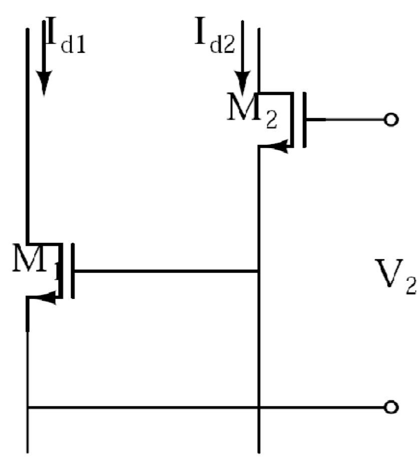

Figure 2.3 The basic V-I circuit [2]

Applying A^2-B^2 to the equations (2.10) and (2.11) and simplifying them results to

$$I_{d1} - I_{d2} = k\,(V_2 - 2V_t)(V_{gs1} - V_{gs2}) \tag{2.12}$$

Thus for constant V_2 the output current $I_{d1} - I_{d2}$ is linearly dependent on v_{gs2} or v_{gs1}. Extension of v_2 the circuit in Fig. 2.3 with another identical transistor M3 as shown in Figure 2.4 enables us to control V_{gs2} via V_{gs3} because M2 and M3 have the same drain current and both devices have the same geometry, the gate–source voltages are equal, now a controlling voltage is added to the V-I convertor

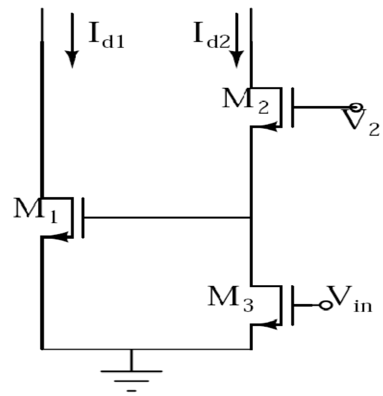

Figure 2.4 Voltage controlled V-I circuit [2]

$$v_{gs1} - v_{gs2} = v_2 - 2\,v_{gs2} = 2v_{gs1} - v_2 \tag{2.13}$$

$$v_{gs2} = v_{gs3} = v_{in} \tag{2.14}$$

Substituting (2.14) and (2.13) in (2.12) results to

$$I_{d1} - I_{d2} = k\,(V_2 - 2V_t)(V_2 - 2V_{in}) \tag{2.15}$$

From equation (2.15) it can be seen that a linear relationship between $I_{d1} - I_{d2}$ and V_{in} .for proper operation all three transistors must be operated in saturation region.

Duplicating the voltage controlled V-I convertor and cross-coupling the output currents results in two quadrant multiplier shown in Figure 2.5, with two input voltages V_1 andV_2 .

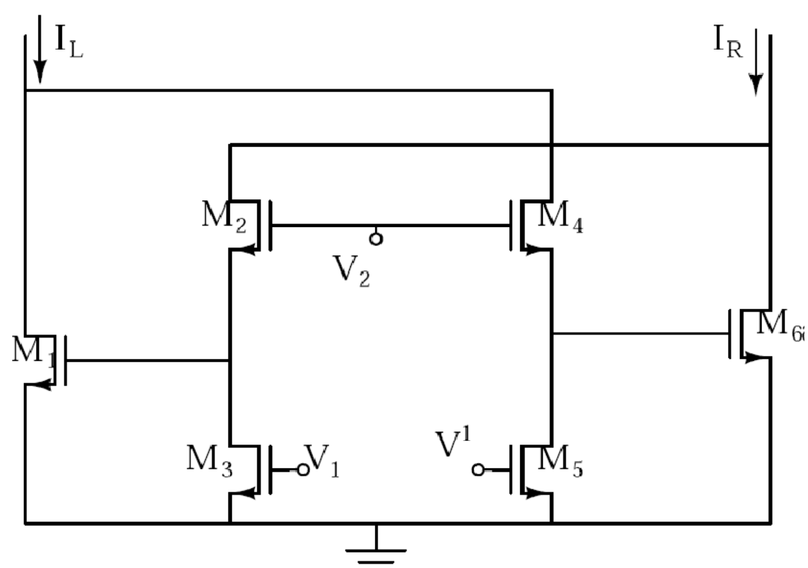

Figure 2.5 Two quadrant multiplier [2]

$$I_L - I_R = 2k(V_2 - 2V_t)(v^1 - V_1) \quad (2.16)$$

Eliminating the non-linear terms in the equation (2.16), the difference of currents is the multiplication of input voltages V_1 and V_2, representing a two quadrant multiplier.

By again duplicating two quadrant multiplier and cross coupling currents, four quadrant multiplier is obtained as shown in Figure 2.6. Current mirrors have been added to obtain a single ended output.

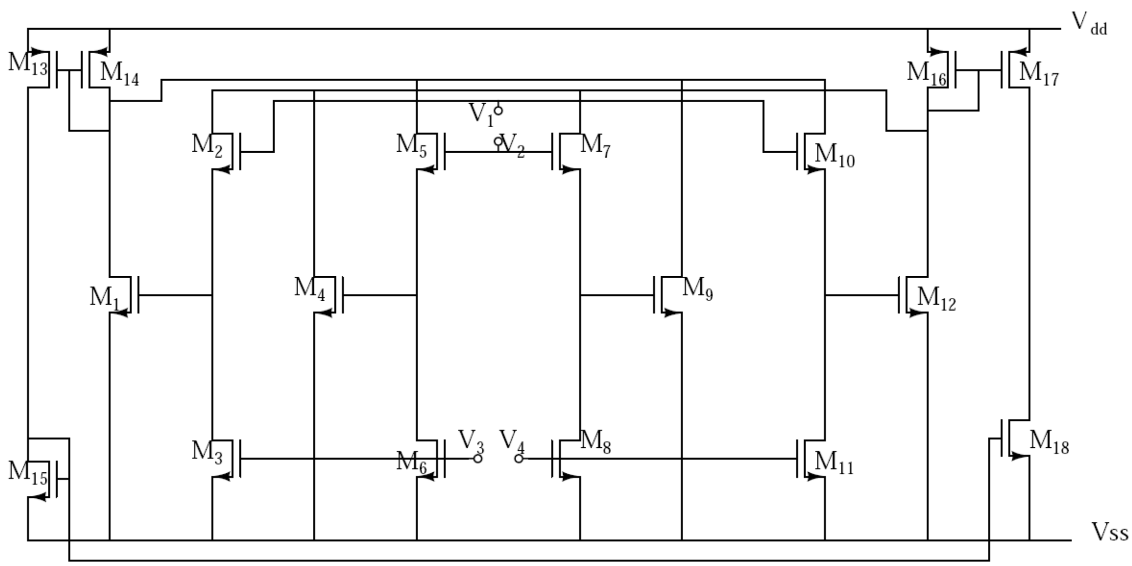

Figure 2.6 Four quadrant multiplier [2]

The output current is $I_{out} = 2k(V_2 - V_1)(V_4 - V_3)$ (2.17)

From equation (2.17) it can be seen that output current is the multiplication of two differential input voltages $(V_2 - V_1)$ and $(V_4 - V_3)$, resulting in a four quadrant multiplier.

CHAPTER

3 LOW-VOLTAGE ANALOG MULTIPLIERS

3.1 INTRODUCTION

Analog multipliers have numerous applications such as frequency mixers, variable frequency oscillators, adaptive filters, etc. In order to improve the overall power efficiency of such applications which is now regularly required for modern analog and mixed signal design dedicated for portable equipments, the analog multiplier to be used must be able to operate under a reduced supply voltage and consume low current. In this chapter two different types of low-voltage analog multipliers are discussed.

The chapter is organized as follows. The low-voltage analog multiplier is discussed in section 3.2. In section 3.3, NMOS four quadrant multiplier is addressed.

3.2 LOW-VOLTAGE ANALOG MULTIPLIER

This low-voltage analog multiplier is achieved using a simple combiner and subtractor circuit, the subtractor output is given as a input to the combiner and the combiner squares the given input. The difference of the two outputs of the combiner circuits gives the multiplication of two inputs, so the quarter square algebraic identity required to implement a analog multiplier is done by using very small amount of transistors which leads to small power consumption and differential pairs are used to achieve high linearity.

3.2.1 COMBINER CIRCUIT

The combiner circuit shown in Figure 3.1 takes the given set of input voltages and gives a output, which is sum of square of the input voltages. It can be seen that the drain and source terminals of the NMOS transistors M_1 and M_2 are connected to each other, the input voltages V_1 and V_2 control the drain currents and these are summed in the load resistor R. Assuming matched devices and operation in the saturation region, and neglecting channel length modulation and mobility degradation.

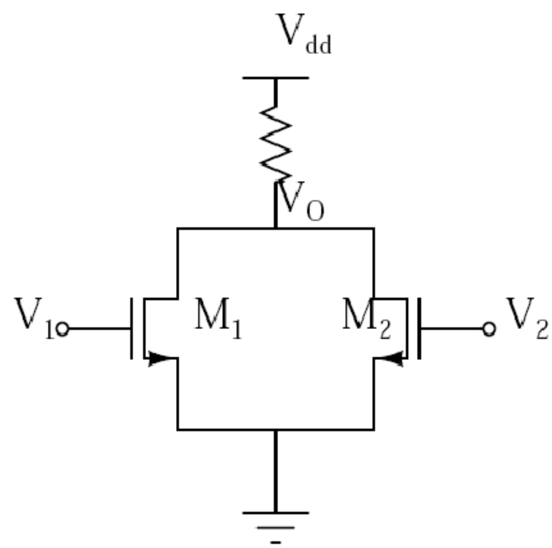

Figure 3.1 Combiner circuit [10]

The output voltage of the combiner may be expressed as

$$V_O = V_{DD} - k_n R \left[(V_1 - V_{tn})^2 + (V_2 - V_{tn})^2 \right] \tag{3.1}$$

where k_n is transconductance parameter, V_{tn} is threshold voltage.

From (3.1) it can be seen that output voltage V_O is combination of two input voltages V_1 and V_2.

3.2.2 SUBTRATOR CIRCUIT

The subtractor circuit shown in Figure 3.2 takes a set of inputs and provides an output which is the difference of two input voltages along with additional bias voltage. The output voltage V_Z differs from the input voltage V_X by the same amount as the source-gate voltage of M_X, and the source-gate voltage of M_X is related to the input voltage V_Y. Thus, for the case of identical M_X and M_Y devices, the equation of V_Z is

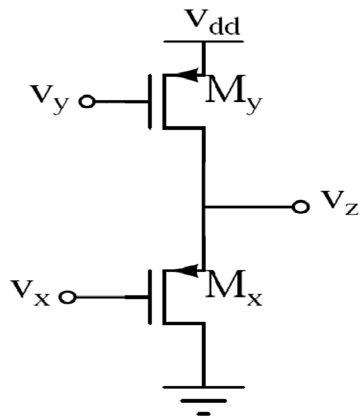

Figure 3.2 Subtractor circuit [10]

$$V_z = V_X + V_{tp} + \sqrt{\frac{I_{DX}}{K_p}} \tag{3.2}$$

$$I_{DX} = I_{DY} = k_p(V_{DD} - V_Y - |V_{tp}|)^2 \tag{3.3}$$

Substituting I_{DX} in (3.2) and simplifying, the output V_Z is

$$V_z = V_X - V_Y + V_{DD} \tag{3.4}$$

The low-voltage analog multiplier shown in Figure 3.3 is implemented using a combination of subtractor cells and combiner circuits. The output of subtractor is given as an input to the combiner circuit, and the combiner circuit squares the two outputs of subtractor.

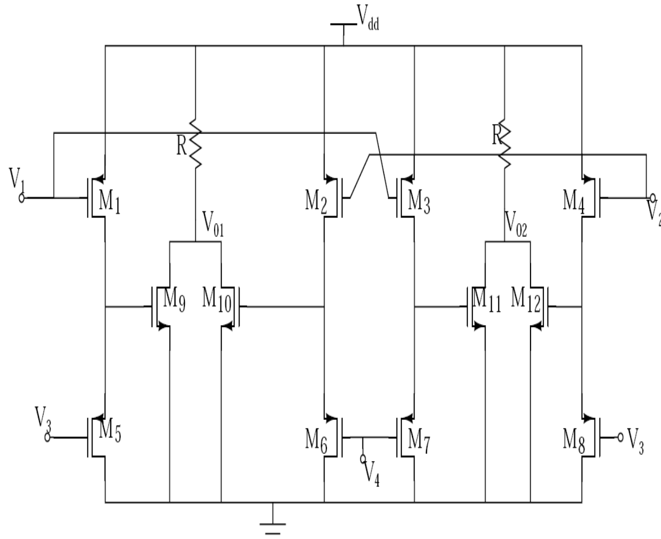

Figure 3.3 low-voltage analog multiplier [10]

Differential input voltages, defined by $V_{id1} = V_1 - V_2$ and $V_{id2} = V_3 - V_4$, are applied to input terminals of the four subtractor cells (M_1 & M_5, M_2 & M_6, M_3 & M_7 and M_4 & M_8), the outputs of which are connected to input terminals of the two combiner cells (M_9, M_{10} & R and M_{11}, M_{12} & M_{13}). Applying the concept of subtractor circuit and combiner circuit to the Figure 3.3, the two output voltages results to

$$V_{01} = V_{DD} - k_n R[(V_{31} - V_{tn} + vdd)^2 + (V_{42} - V_{tn} + vdd)^2] \quad (3.5)$$

$$V_{02} = V_{DD} - k_n R[(V_{41} - V_{tn} + vdd)^2 + (V_{32} - V_{tn} + vdd)^2] \quad (3.6)$$

Taking $V_{os} = V_{DD} - V_{tn}$ and simplifying (3.5) and (3.6) the values of the two outputs of the combiner circuits are

$$V_{01} = V_{DD} - k_n R[V_{41}^2 + V_{32}^2 + 2V_{os}(V_{41} + V_{32}) + 2V_{os}^2] \quad (3.7)$$

$$V_{02} = V_{DD} - k_n R[V_{31}^2 + V_{42}^2 + 2V_{os}(V_{31} + + V_{42}) + 2V_{os}^2] \quad (3.8)$$

where $V_{os} = V_{DD} - V_{tn}$ is an undesired term which is eliminated by fully differential operation. The differential output voltage can be obtained by subtracting the above two equations, yielding

$$V_{out} = k_n R\,(V_{31}^2 + V_{42}^2 - V_{41}^2 - V_{32}^2) = -(2k_n R)V_{id1}V_{id2} \quad (3.9)$$

From (3.9) it can be seen that output voltage is multiplication of two differential input voltages V_{id1} and V_{id2} resulting in a four quadrant multiplier.

3.2 NMOS FOUR- QUADRANT MULTIPLIER

This NMOS four-quadrant multiplier configuration has great advantage as it cancels all non-linear components at the output of the multiplier .The multiplier configuration is achieved using quarter square algebraic identity , to implement the quarter square algebraic identity we use a summer and squarer circuit.

3.2.1 SUMMING CIRCUIT

The fully differential summing circuit is shown in Figure 3.4.This circuit is implemented by using basic MOS differential pairs M_1-M_4 and the active loads M_5-M_6. Assuming that transistors M_1-M_4 are matched with transconductance parameter K_1 and transistors M_5-M_6 are matched with K_5

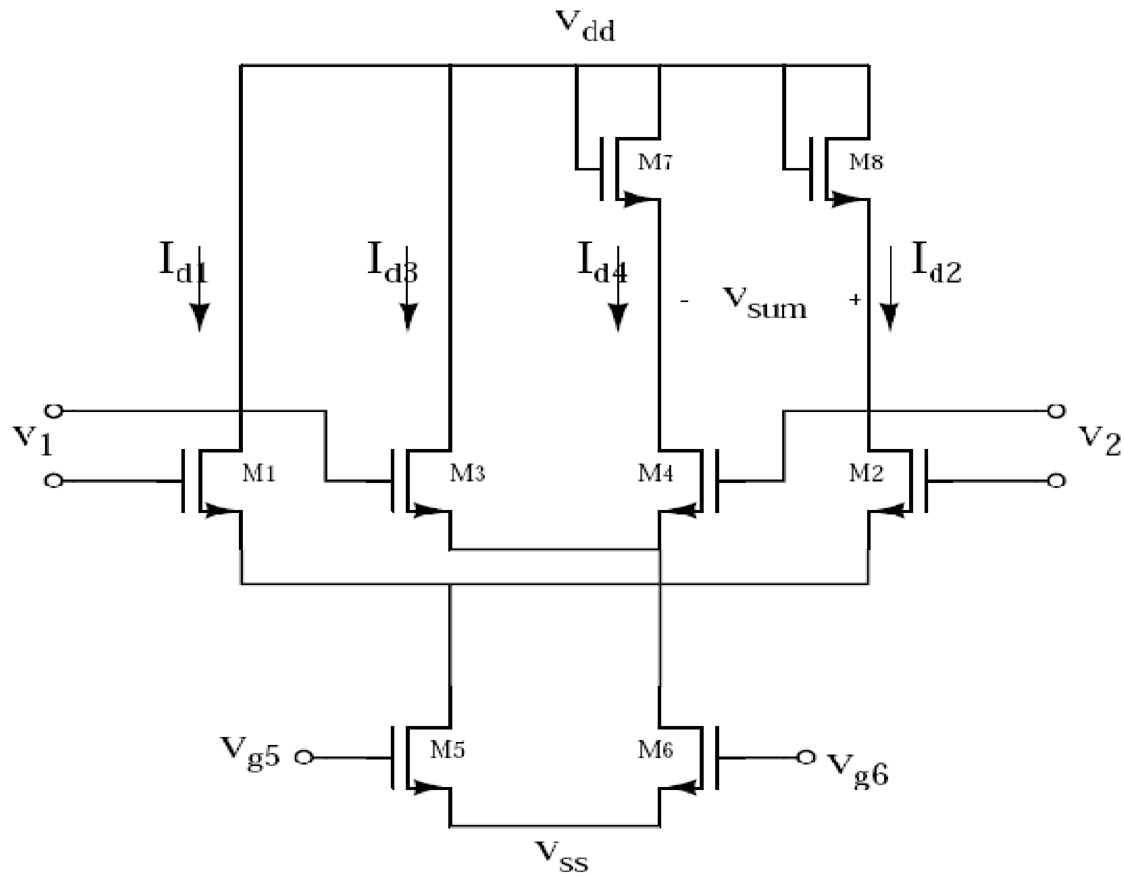

Figure 3.4 Summing circuit [7]

If all devices operate in saturation region, applying the differential input voltages v_1 and v_2 , the loop equations of the gate-to-source voltages of the two differential amplifiers M_1-M_2 and M_3-M_4 are

$$\left(\frac{V_1}{2} + \frac{V_2}{2}\right) = V_{gs1} - V_{gs2} \quad (3.10)$$

$$-\left(\frac{V_1}{2} + \frac{V_2}{2}\right) = V_{gs3} - V_{gs4} \quad (3.11)$$

By replacing $v_{gs} = \sqrt{\frac{I_d}{K}} + V_t$ in (3.10) and (3.11) results to

$$\left(\frac{v_1}{2} + \frac{v_2}{2}\right) = \sqrt{\frac{I_{d1}}{K_1}} - \sqrt{\frac{I_{d2}}{K_1}} \quad (3.12)$$

$$-\left(\frac{v_1}{2} + \frac{v_2}{2}\right) = \sqrt{\frac{I_{d3}}{K_1}} - \sqrt{\frac{I_{d4}}{K_1}} \quad (3.13)$$

Subtracting (3.12) and (3.13) results to

$$(V_1 + V_2) = \left(\sqrt{\frac{1}{K}}\right)((\sqrt{I_{d1}} + \sqrt{I_{d4}})\_(\sqrt{I_{d2}} + \sqrt{I_{d3}})) \quad (3.14)$$

As $I_{d1} = I_{d4}$ and $I_{d2} = I_{d3}$ of two differential amplifier pairs, substituting the current values in (3.14) results to

$$\sqrt{I_{d4}} - \sqrt{I_{d2}} = \sqrt{K_1} \left(\frac{V_1}{2} + \frac{V_2}{2}\right) \quad (3.15)$$

From output loop $V_{SUM} = V_{gs7} - V_{gs8}$ and $I_{d7} = I_{d4}$,$I_{d8} = I_{d2}$, the output voltage V_{SUM} is

$$V_{SUM} = \left(\frac{\sqrt{I_{d4}} - \sqrt{I_{d2}}}{\sqrt{K_5}}\right) \quad (3.16)$$

Substituting (3.15) into (3.16) results to

$$V_{SUM} = \sqrt{\frac{k_1}{4K_5}} (V_1 + V_2) \quad (3.17)$$

From (3.17) it can be seen that the output voltage is directly proportional to sum of input voltages.

3.2.2 SQUARING CIRCUIT

The squaring circuit shown in Figure 3.5 is implemented by using a simple differential amplifier, the transistors M_1-M_5 are bias in saturation region. If the differential input voltage V_d with the same common-mode V_c is applied, the drain currents of the transistors can be given by

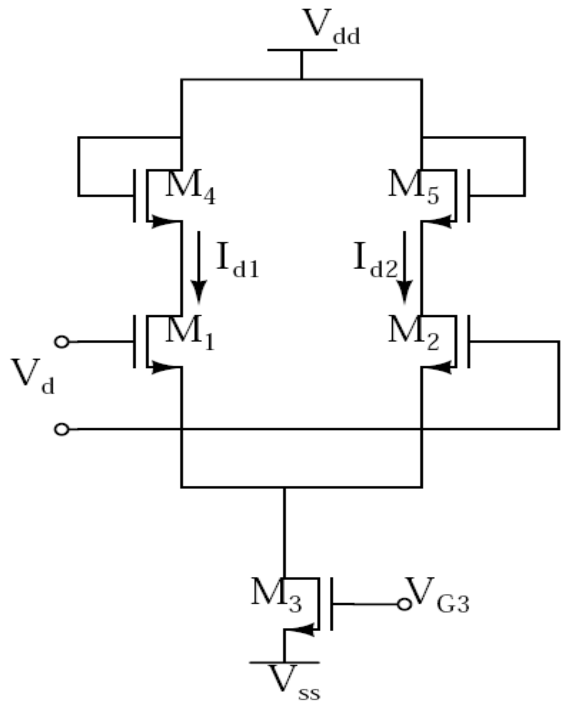

Figure 3.5 squaring circuit [7]

$$I_{d1} = K_1(V_c + \frac{V_d}{2} - V_{sq} - V_{th})^2 \quad (3.18)$$

$$I_{d2} = K_2(V_c - \frac{V_d}{2} - V_{sq} - V_{th})^2 \quad (3.19)$$

$$I_{d3} = K_3(V_{G3} - V_{ss} - V_{th})^2 \quad (3.20)$$

$$I_{d1} + I_{d2} = I_{d3} \quad (3.21)$$

where K_1,K_2 and K_3 are transconductance parameter of the transistors M_1-M_2, and V_{th} is the threshold voltage of the transistors, respectively substituting (3.18), (3.19) ,(3.20) in (3.21) results to

$$V_{sq} = V_c - V_{G3} + V_{ss} + \frac{V_d^2}{8(V_{G3} - V_{ss} - V_{th})} \quad (3.22)$$

From equation (3.22) it can be seen that V_{sq} is directly proportional to the square of V_d resulting in a squarer output.

The combination of summer and squarer circuit forms a NMOS four-quadrant multiplier shown in Figure 3.6, summer circuits gives a sum of two input voltages and this output is applied to squarer circuit. The squarer circuit squares the given input, the two outputs of the squarer is given to a differential amplifier. The differential amplifier gives the difference of the two outputs of the squarer, which produces the multiplication of given two inputs.

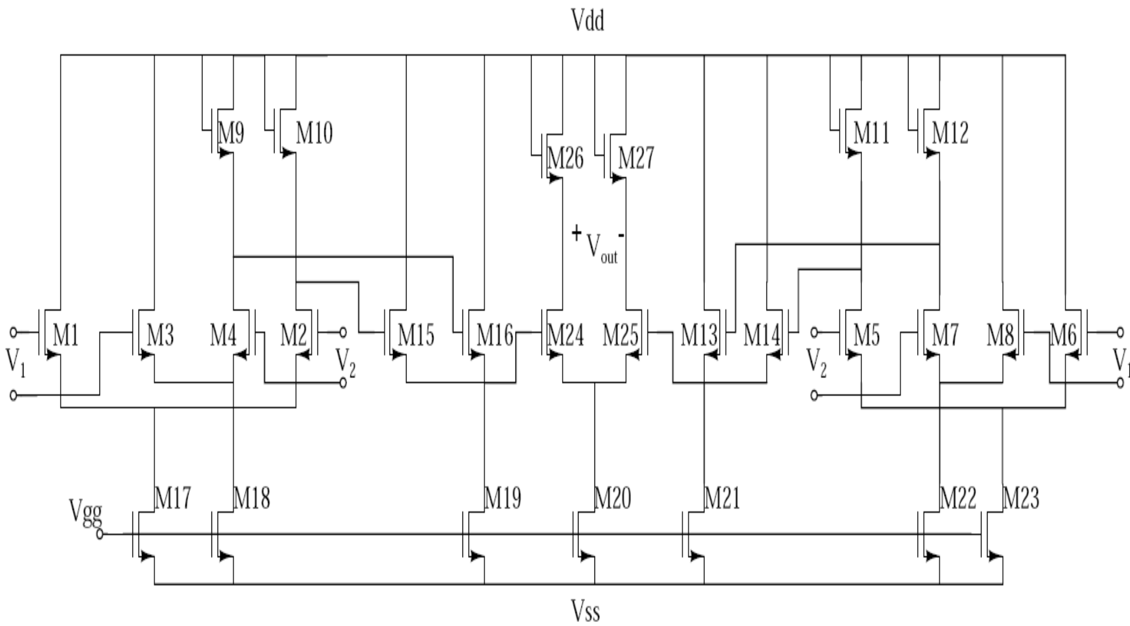

Figure 3.6 NMOS four-quadrant multiplier [7]

The output voltage V_0 of NMOS four-quadrant multiplier can be obtained using (3.17) and (3.22) and can be expressed as

$$V_0 \;=\; \frac{\frac{k_1}{4K_5}}{8(V_{G3}-V_{ss}-V_{th})}\left[(V_1+V_2)^2-(V_1-V_2)^2\right] \qquad (3.23)$$

$$V_0 \;=\; \frac{\frac{k_1}{K_5}}{8(V_{G3}-V_{ss}-V_{th})}\left[V_1\,V_2\right] \qquad (3.24)$$

Transistors M_1-M_{12} form the summing circuits that produce the output voltage in term of the sum and difference of input signals. The sum and difference outputs from these stages are applied to the squarer circuits formed by M_{13}-M_{16} and M_{24}-M_{27} form NMOS voltage amplifier, Finally, the output voltage of the multiplier can be written as

$$V_o = \left[\frac{\frac{K_1K_{24}}{K_9K_{26}}}{8(V_{G3}-V_{ss}-V_{th})}\right]V_1\,V_2 \qquad (3.25)$$

From (3.25) it can be seen that V_0 is directly proportional to multiplication of two input voltages V_1 and V_2 resulting in a multiplier.

CHAPTER

4

SIMULATION RESULTS AND LAYOUT

4.1 INTRODUCTION

In this chapter simulation results and layout of the low-voltage analog multiplier, NMOS four-quadrant multiplier .This chapter is organized as follows: The simulation results of low-voltage analog multiplier are discussed in section 4.2. The simulation results of NMOS four-quadrant multiplier results are discussed in section 4.3. The layout of low-voltage analog multiplier is presented in section 4.4

4.2 SIMULATION RESULTS OF LOW-VOLTAGE ANALOG MULTIPLIER

The low-voltage analog multiplier has been simulated using spectre (Cadence) tool for 0.18 µm CMOS technology. The transistor dimensions are listed in Table 4.1. The values of input voltageV_{id1}, supply voltage Vdd are chosen as 100 mV, 1000 mV respectively.

Table 4.1 Dimensions of low-voltage analog multiplier

Transistor	W(µm)	L(µm)
M_1-M_8,M_{13}-M_{14}	10	2
M_9-M_{12}	4	2

4.2.1 DC CHARACTERISTICS

The DC characteristics of low-voltage analog multiplier is shown in Figure 4.1, the input voltage V_{id1} is varied from -0.1 to 0.1V with increment of 0.05V.The output is obtained by varying V_{id1} for different values of V_{id2} .

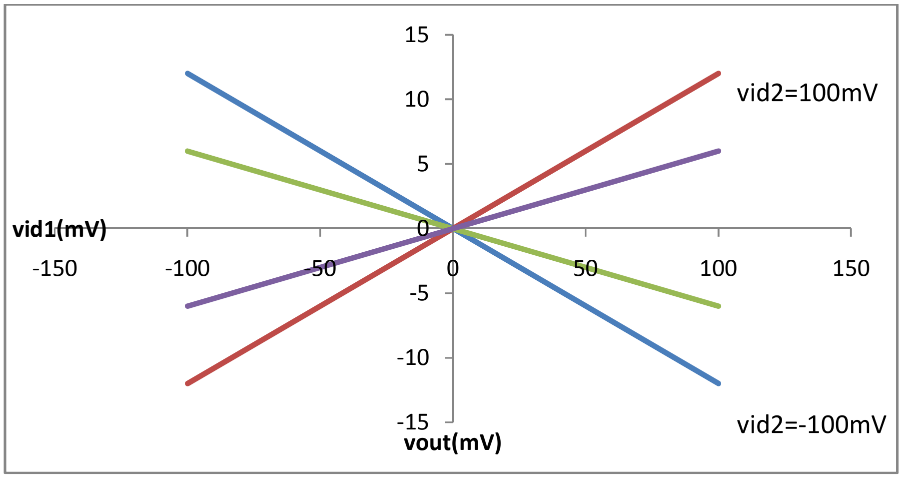

Figure 4.1 DC characteristics of low-voltage analog multiplier

4.2.2 AC CHARACTERISTICS

The frequency response of low-voltage analog multiplier is shown in Figure 4.2, the 3-db bandwidth obtained with a load C_L=1 fF is around 64MHz.

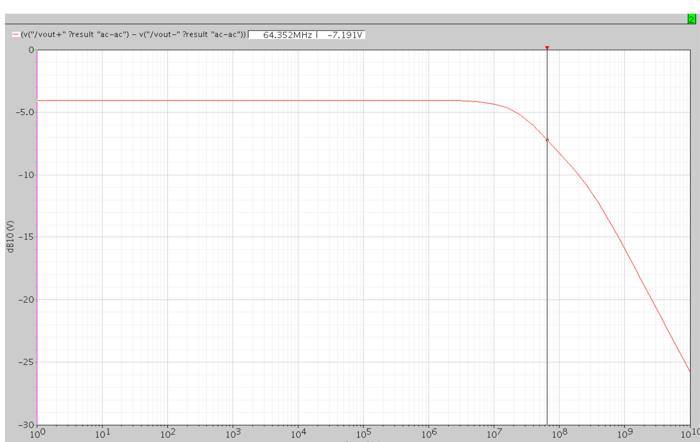

Figure 4.2 AC response of low-voltage analog multiplier

4.2.3 TRANSIENT CHARACTERISTICS

The transient response of the low-voltage analog multiplier is shown in Figure 4.3.Two sinusoidal input voltages V_{id1} with 0.1V amplitude, 25KHz frequency V_2 with 0.1V amplitude, 1KHz frequency are applied giving an amplitude modulated output wave of 25mV amplitude and 25KHz frequency. Total harmonic distortion is measured by applying V_{id1} with 0.1V amplitude 100MHz frequency and input is kept at constant dc value, THD value obtained is -43dB.

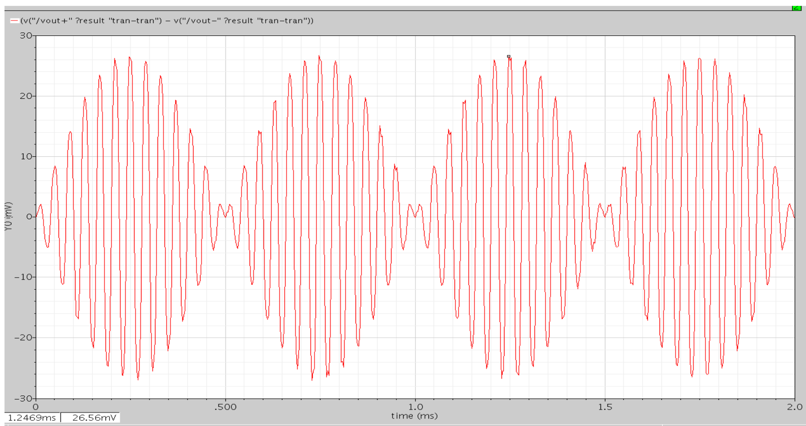

Figure 4.3 Transient response of low-voltage analog multiplier

Table 4.2 Comparison of performance between simulated low-voltage analog multiplier and low-voltage analog multiplier reported in [10]

Performance factor	low-voltage analog multiplier [10]	Simulated Low-voltage analog multiplier[10]
Technology used(µm)	0.35	0.18
Bandwidth(MHz)	110	64
Power consumption(µW)	34	22
Total harmonic distortion(dB)	-60	-43

From the Table 4.2, it is observed that the simulated low-voltage analog multiplier has lower power dissipation, as compared to low-voltage analog multiplier reported in [10].

4.3 SIMULATION RESULTS OF NMOS FOUR-QUADRANT MULTIPLIER

The NMOS four-quadrant multiplier has been simulated using Spectre (Cadence) tool for 0.18 µm NMOS technology. The transistor dimensions are listed in Table 4.3. The values of input voltageV_1, supply voltage Vdd are chosen as 100mV, 900mV, 900mV respectively

Table 4.3 Dimensions of NMOS four-quadrant multiplier

Transistor	W(µm)	L(µm)
M_1-M_{12},M_{13}-M_{16},M_{26}-M_{27}	3	3
M_{17}-M_{25}	6	3

4.3.1 DC CHARACTERISTICS

The DC characteristics of NMOS four-quadrant multiplier is shown in Figure 4.4.The input voltage V_1 is varied from -0.1 to 0.1V with increment of 0.05V.The output is obtained by varying V_1 for different values of V_2 , the output is simple linear multiplication of input voltages V_1 andV_2.

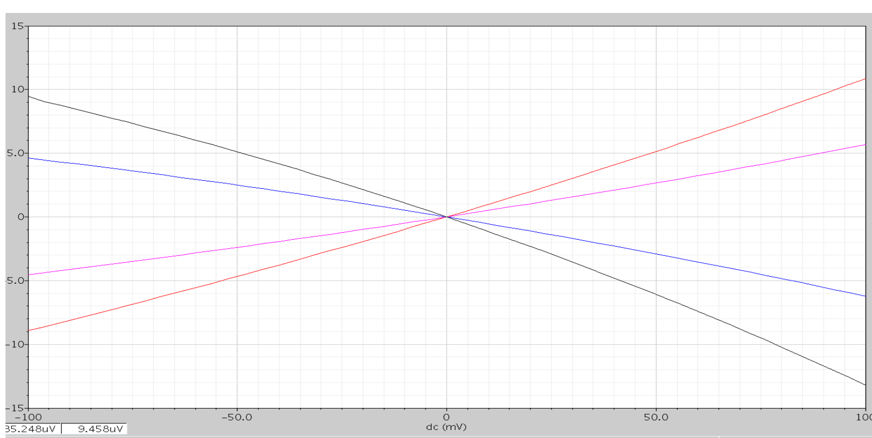

Figure 4.4 DC characteristics of NMOS four-quadrant multiplier

4.3.2 AC CHARACTERISTICS

The frequency response of the NMOS four-quadrant multiplier is shown in Figure 4.5, the 3-db bandwidth obtained with a load C_L=1 fF is around 60MHz

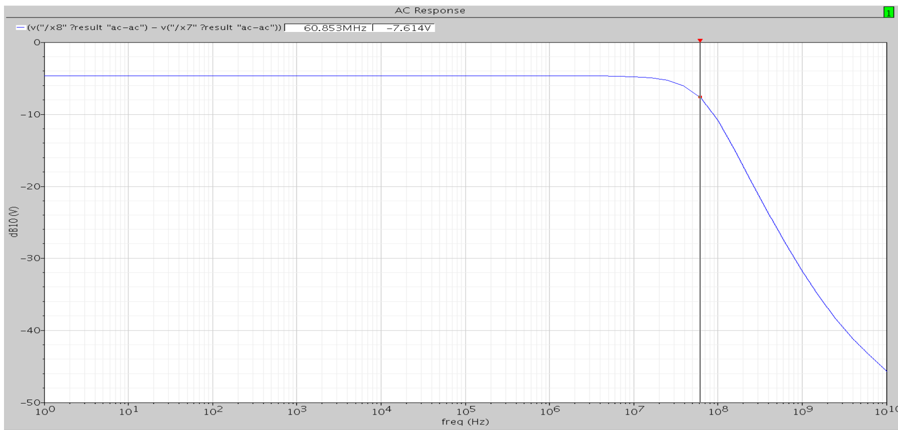

Figure 4.5 AC response of NMOS four-quadrant multiplier

4.3.3 TRANSIENT CHARACTERISTICS

The transient response of the NMOS four-quadrant multiplier is shown in Figure 4.6 .Two sinusoidal input voltages V_1 with 0.1V amplitude , 1MHz frequency V_2 with 0.1V amplitude, 50KHz frequency are applied giving an amplitude modulated output wave of 40mV amplitude and 1MHz frequency. Total harmonic distortion is measured by applying V_1 with 0.1V amplitude 100MHz frequency and input is kept at constant dc value, THD value obtained is 0.89%.

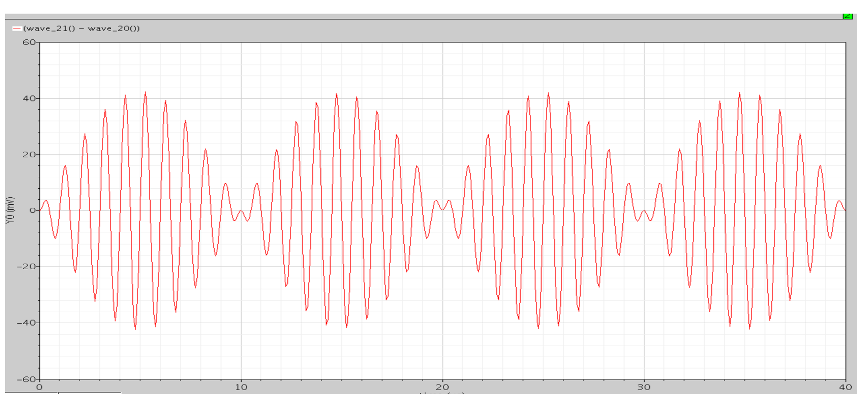

Figure 4.6 Transient response of NMOS four-quadrant multiplier

Table 4.4 Comparison of performance between simulated NMOS four-quadrant multiplier and NMOS four-quadrant multiplier reported in [7]

Performance factor	NMOS four-quadrant multiplier [7]	Simulated NMOS four-quadrant multiplier[7]
Technology used(µm)	0.5	0.18
Power consumption(mW)	3.6	0.2
Bandwidth(MHz)	120	60

From the Table 4.4, it is observed that the simulated NMOS multiplier has lower power dissipation, as compared to NMOS four-quadrant multiplier reported in [7].

4.4 LAYOUT

Layout is the process by which a circuit specification is converted to a physical implementation with enough information to deduce all the relevant physical parameters of the circuit. The physical mask layout of any circuit to be manufactured using a particular process must conform to a set of geometric constraints or rules, which are generally called layout design rules. These rules specify the minimum allowable line widths for physical objects on-chip such as metal and polysilicon interconnects or diffusion areas, minimum feature dimensions, and minimum allowable separations between two such features. If a metal line width is too small, it is possible for the line to break during the fabrication process resulting in an open circuit, so to avoid such errors certain design rules are followed while making a layout.

Some of the design rules used by virtuso tool (Cadence) for 0.18um technology are

Minimum diffusion width- 0.24um

Minimum poly width-0.18um

Minimum poly spacing-0.34um

Minimum metal1 width-0.24um

Minimum metal1 spacing-0.24um

Maximum N-well width-20um

4.4.1 LAYOUT VERSUS SCHEMATIC (LVS)

The Layout Versus Schematic (LVS) is the class of Electronic Design Automation (EDA) verification software that determines whether a particular integrated circuit layout corresponds to the original schematic of circuit diagram of the design. A successful Design Rule Check (DRC) ensures that the layout conforms to the rules designed required for faultless fabrication. However, it does not guarantee if it really represents the circuit you desire to fabricate. This is where an LVS check is used. LVS checking software recognizes the drawn shapes of the layout that represent the electrical components of the circuit, as well as the connections between them. The software then compares them with the schematic or circuit diagram. In most cases the layout will not pass LVS the first time requiring the layout engineer to examine the LVS software's reports and make changes to the layout.

4.4.2 CIRCUIT EXTRACTION

Another important tool in the custom-design methodology is the circuit extractor, which derives a circuit schematic from a physical layout. By scanning the various layers and their interconnections, the extractor reconstructs the transistor network, including the sizes of the devices and the interconnections. Further the resulting extracted circuit diagram contains precise information of parasitic, such as the diffusion and wiring capacitances and resistances. This allows for a more accurate simulation and analysis.

4.4.3 LAYOUT OF LOW-VOLTAGE ANALOG MULTIPLIER

Layout of the low-voltage analog multiplier cell has been designed using tool virtuso (cadence) for 0.18 μm CMOS technology libraries. Extracted Layout diagram of CMOS analog multiplier is shown in Figure 4.7. The Design Rule Check (DRC), Layout versus Schematic (LVS) and Extraction (RCX) checking has also been performed using tool spectre (CADENCE).

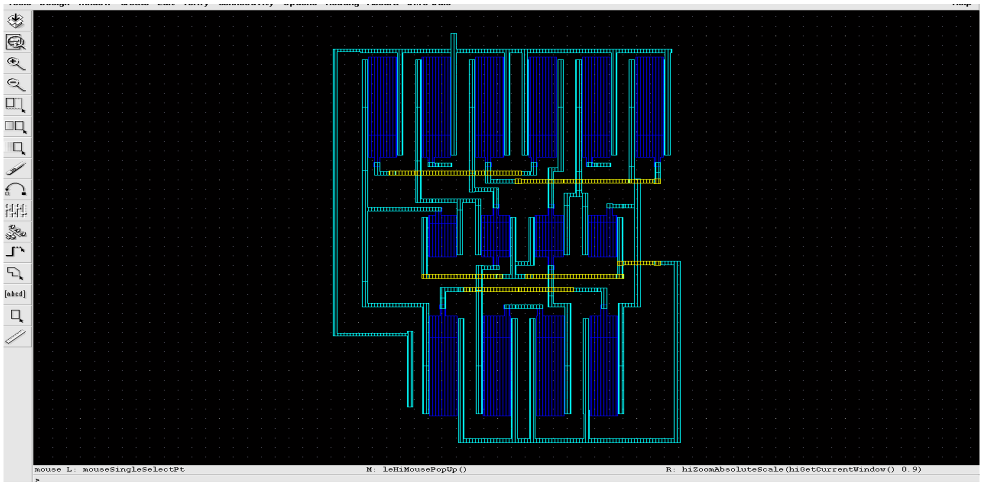

Figure 4.7 Extracted layout of low-voltage analog multiplier

To overcome the shorts and misconnections in the layout metal2 is used to connect between two metal1 layers which cross other metal1 layers, to connect metal1 and metal2 via's are used . After making the layout DRC check is performed and some metal to metal spacing errors were found and removed by making proper changes. After passing the DRC rule check, layout versus simulation (LVS) is performed.

4.4.3.1 LVS REPORT OF LOW-VOLTAGE ANALOG MULTIPLIER

The below LVS report tells us that after comparing all the nets, devices, wires, input and output pins of both the layout and basic schematic circuit of low power multiplier have no mismatches .

```
************************************************************************
********
****** mul2 schematic mohan1  <vs>  mul2 layout mohan1
************************************************************************
********


Filter/Reduce statistics only. Network matching was OK.


Pre-expand Statistics
======================                         Original
Cell/Device                               schematic  layout
(N_18_MM) MOS                                     4       4
(P_18_MM) MOS                                    10      10
                                             ------  ------
Total                                            14      14

Schematic and Layout Match
```

CHAPTER

5

CONCLUSION AND FURTHER DEVELOPMENT

5.1 CONCLUSION

In this thesis two low-voltage analog multipliers, low-voltage analog multiplier [10] ,NMOS four-quadrant multiplier[7], are simulated using spectre (Cadence) tool for 0.18 µm CMOS technology. The simulated result has produced very less static power consumption. The input voltage range for all the multipliers is ±0.1V. The layout diagrams of both the multipliers is made using virtuso (Cadence) tool for 0.18µm CMOS technology and LVS is matched.

5.2 SUGGESTIONS FOR FURTHER DEVELOPMENT

In low voltage analog multiplier [10], the power and accuracy of the circuit can be improved using a PMOS transistor as a load instead of resistor. This multiplier can also be used for high frequencies by improving the bandwidth of the circuit which can be done by adding a zero in the transfer function of multiplier.

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APPENDIX A

(A)MODEL PARAMETERS FOR PMOS TRANSISTORS

- model p_18_mm bsim3v3 type=p
- + mobmod=3.0000e+00 version=3.2000e+00 capmod=2.0000e+00
- + binunit=1.0000e+00 nqsmod=0.0000e+00
- + tox=4.2000e-09 + dtox_p_18_mm toxm=4.2000e-09
- + xj=1.0000e-07 nch=6.1310e+17 ngate=1.0000e+23
- + vth0= - 4.5550e-01 + dvth0_p_18_mm k1=5.7040e-01
- + k2=6.9730e-03 k3=-2.8330e+00 k3b=1.3260e+00
- + w0=-1.9430e-07 nlx=2.5300e-07 dvt0=4.8850e-01
- + dvt1=7.5780e-02 dvt2=1.2870e-01 dvt0w=-1.2610e-01
- + dvt1w=2.4790e+04 dvt2w=6.9150e-01 lint=-1.0410e-08
- + wint=-1.5250e-07 dwg=-1.1510e-07 dwb=-1.0390e-07
- + u0=1.1450e+02 + du0_p_18_mm ua=1.5400e-09
- + ub=2.6460e-19 uc=-9.5870e-02 vsat=5.3400e+04
- + a0=1.3500e+00 ags=3.8180e-01 b0=-3.0880e-07
- + b1=0.0000e+00 keta=1.0440e-02 a1=0.0000e+00
- + a2=1.0000e+00 voff=-1.0730e-01 nfactor=1.5350e-00
- + cit=-1.0670e-03 cdsc=7.5780e-04 cdscd=-2.8830e-05
- + cdscb=1.0000e-04 eta0=1.0710e+00 etab=-9.2910e-01
- + dsub=1.9191e+00 pclm=2.6530e+00 pdiblc1=0.0000e+00
- + pdiblc2=5.0000e-06 pdiblcb=0.0000e+00 drout=1.4570e+00
- + pscbe1=4.8660e+08 pscbe2=2.8000e-07 pvag=1.1620e+00
- + rdsw=7.9210e+02 prwg=0.0000e+00 prwb=0.0000e+00
- + alpha0=0.0000e+00 alpha1=0.0000e+00 beta0=3.0000e+01
- + cgdo=2.0540e-10 + dcgdo_p_18_mm cgbo=0.0000e+00
- + cgso=2.0540e-10 + dcgso_p_18_mm xpart=1.0000e+00
- + cf=1.5330e-10 dlc=5.6000e-08 cgsl=0.0000e+00
- + cgdl=0.0000e+00 ckappa=6.0000e-01 clc=1.0000e-07
- + cle=6.0000e-01 dwc=0.0000e+00 vfbcv=-1.0000e+00
- + noff=1.0000e+00 voffcv=0.0000e+00 acde=1.0000e+00
- + moin=1.5000e+01 lmin=1.8000e-07 lmax=5.0000e-05
- + wmin=2.4000e-07 wmax=1.0000e-04
- + xl= - 2.0000e-09 + dxl_p_18_mm
- + xw=0.0000e+00 + dxw_p_18_mm js=3.0000e-06
- + jsw=4.1200e-11 cj=1.1400e-03 + dcj_p_18_mm
- + mj=3.9500e-01 pb=7.6200e-01
- + cjsw=1.7400e-10 + dcjsw_p_18_mm mjsw=3.2400e-01
- + tnom=2.5000e+01 ute=-4.4840e-01 kt1=-2.1940e-01
- + kt1l=-8.2040e-09 kt2=-9.4870e-03 ua1=4.5710e-09

- + ub1=-6.0260e-18 uc1=-9.8500e-02 at=1.2030e+04
- + prt=0.0000e+00 xti=3.0000e+00 ww=1.2360e-14
- + lw=-2.8730e-16 ll=6.6350e-15 wl=0.0000e+00
- +wln=1.0000e+00 wwn=1.0000e+00 wwl=0.0000e+00
- + lln=1.0000e+00 lwn=1.0000e+00 lwl=0.0000e+00
- + llc=-7.4500e-15 lwc=0.0000e+00 lwlc=0.0000e+00
- + wlc=0.0000e+00 wwc=0.0000e+00 wwlc=0.0000e+00
- + lvth0=4.4000e-03 + dlvth0_p_18_mm
- + wvth0= - 1.4800e-02 + dwvth0_p_18_mm
- + pvth0=3.2000e-03 + dpvth0_p_18_mm lnlx=-1.5840e-08
- + wrdsw=1.0070e+01 weta0=0.0000e+00 wetab=0.0000e+00
- + wpclm=0.0000e+00 wua=2.6300e-09 lua=-8.1530e-11
- + pua=5.8550e-11 wub=0.0000e+00 lub=0.0000e+00
- + pub=0.0000e+00 wuc=0.0000e+00 luc=0.0000e+00
- + puc=0.0000e+00 wvoff=-9.8160e-03 lvoff=-9.8710e-04
- + pvoff=-9.8330e-05 wa0=-4.8070e-02 la0=-2.8100e-01
- + pa0=8.6610e-02 wags=-4.1770e-02 lags=4.4540e-02
- + pags=-4.0760e-02 wketa=0.0000e+00 lketa=-1.2000e-02
- + pketa=0.0000e+00 wute=-2.6820e-01 lute=0.0000e+00
- + pute=0.0000e+00 wvsat=-1.4200e+04 lvsat=0.0000e+00
- + pvsat= - 4.3400e+02 + dpvsat_p_18_mm lpdiblc2=3.0120e-03
- + cjswg=4.200e-10 + dcjgate_p_18_mm wat=-6.4050e+03
- + wprt=2.1660e+02 n=1.0000e+00 pbsw=6.6500e-01
- + cta=1.0000e-03 ctp=7.5300e-04 pta=1.5500e-03
- + ptp=1.2400e-03 ldif=8.0000e-08 rsh=8.0000e+00
- + rd=0.0000e+00 rsc=0.0000e+00 rdc=0.0000e+00
- + hdif=2.6000e-07 rs=0.0000e+00
- + noimod=2 noia=3.57456993317604E+18 noib=2500
- + noic=2.61260020285845E-11 ef=1.1388
- + em=41000000

(B) MODEL PARAMETERS OF NMOS TRANSISTOR

-
- model n_18_mm bsim3v3 type=n
-
- + version=3.2000e+00 binunit=1.0000e+00 mobmod=1.0000e+00
- + capmod=2.0000e+00 nqsmod=0.0000e+00
- + tox=4.2000e-09 + dtox_n_18_mm toxm=4.2000e-09
- + xj=1.6000e-07 nch=3.7446e+17 rsh=8.0000e+00
- + ngate=1.0000e+23 vth0=3.0750e-01 + dvth0_n_18_mm
- + k1=4.5780e-01 k2=-2.6380e-02 k3=-1.0880e+01
- + k3b=2.3790e-01 w0=-8.8130e-08 nlx=4.2790e-07
- + dvt0=4.0420e-01 dvt1=3.2370e-01 dvt2=-8.6020e-01
- + dvt0w=3.8300e-01 dvt1w=6.0000e+05 dvt2w=-2.5000e-02
- + lint=1.5870e-08 wint=1.0220e-08 dwg=-3.3960e-09
- + dwb=1.3460e-09 u0=3.1410e+02 + du0_n_18_mm
- + ua=-9.2010e-10 ub=1.9070e-18 uc=4.3550e-11
- + vsat=7.1580e+04 a0=1.9300e+00 ags=5.0720e-01

- + b0=1.4860e-06 b1=9.0640e-06 keta=1.7520e-02
- + a1=0.0000e+00 a2=1.0000e+00 voff=-1.0880e-01
- + nfactor=1.0380e+00 cit=-1.5110e-03 cdsc=2.1750e-03
- + cdscd=-5.0000e-04 cdscb=8.2410e-04 eta0=1.0040e-03
- + etab=-1.4590e-03 dsub=1.5920e-03 pclm=1.0910e+00
- + pdiblc1=3.0610e-03 pdiblc2=1.0000e-06 pdiblcb=0.0000e+00
- + drout=1.5920e-03 pscbe1=4.8660e+08 pscbe2=2.8000e-07
- + pvag=-2.9580e-01 rdsw=4.9050e+00 prwg=0.0000e+00
- + prwb=0.0000e+00 wr=1.0000e+00 alpha0=0.0000e+00
- + alpha1=0.0000e+00 beta0=3.0000e+01 xpart=1.0000e+00
- + cgso=2.3500e-10 + dcgso_n_18_mm
- + cgdo=2.3500e-10 + dcgdo_n_18_mm cgbo=0.0000e+00
- + cgsl=0.0000e+00 cgdl=0.0000e+00 ckappa=6.0000e-01
- + cf=1.5330e-10 clc=1.0000e-07 cle=6.0000e-01
- + dlc=2.9000e-08 dwc=0.0000e+00 vfbcv=-1.0000e+00
- + noff=1.0000e+00 voffcv=0.0000e+00 acde=1.0000e+00
- + moin=1.5000e+01 lmin=1.8000e-07 lmax=5.0000e-05
- + wmin=2.4000e-07 wmax=1.0000e-04
- + xl= - 1.0500e-08 + dxl_n_18_mm
- + xw=0.0000e-00 + dxw_n_18_mm js=1.0000e-06
- + jsw=7.0000e-11 cj=1.0300e-03 + dcj_n_18_mm
- + mj=4.4300e-01 pb=8.1300e-01
- + cjsw=1.3400e-10 + dcjsw_n_18_mm mjsw=3.3000e-01
- + tnom=2.5000e+01 ute=-1.2860e+00 kt1=-2.2550e-01
- + kt1l=-4.1750e-09 kt2=-2.5270e-02 ua1=2.1530e-09
- + ub1=-2.6730e-18 uc1=-3.8320e-11 at=1.4490e+04
- + prt=-1.0180e+01 xti=3.0000e+00 wl=0.0000e+00
- + wln=1.0000e+00 ww=7.2620e-16 wwn=1.0000e+00
- + wwl=0.0000e+00 ll=-1.0620e-15 lln=1.0000e+00
- + lw=2.9960e-15 lwn=1.0000e+00 lwl=0.0000e+00
- + llc=-2.1400e-15 lwc=0.0000e+00 lwlc=0.0000e+00
- + wlc=0.0000e+00 wwc=0.0000e+00 wwlc=0.0000e+00
- + lvth0= - 1.0000e-03 + dlvth0_n_18_mm
- + wvth0=6.027e-02 + dwvth0_n_18_mm pvth0=0 + dpvth0_n_18_mm
- + lnlx=-2.8540e-08 wnlx=0.0000e+00 pnlx=0.0000e+00
- + wua=-1.8800e-11 wu0=5.4000e-01 + dwu0_n_18_mm
- + pub=3.8000e-20 pw0=1.3000e-09 wrdsw=0.0000e+00
- + weta0=0.0000e+00 wetab=0.0000e+00 leta0=1.5740e-03
- + letab=0.0000e+00 peta0=0.0000e+00 petab=0.0000e+00
- + wpclm=0.0000e+00 wvoff=-4.0780e-04 lvoff=-4.2080e-03
- + pvoff=-3.7880e-04 wa0=-4.7310e-02 la0=-4.6670e-01
- + pa0=-2.6490e-02 wags=4.2420e-03 lags=3.0280e-01
- + pags=0.0000e+00 wketa=0.0000e+00 lketa=-1.9420e-02
- + pketa=0.0000e+00 wute=6.3730e-02 lute=0.0000e+00
- + pute=0.0000e+00 wvsat=5.0660e+03 lvsat=0.0000e+00
- + pvsat=0.0000e+00 + dpvsat_n_18_mm lpdiblc2=-4.7520e-03
- + wat=7.0670e+03 wprt=0.0000e+00 ldif=8.0000e-08
- + hdif=2.6000e-07 n=1.0000e+00 pbsw=8.8000e-01
- + cjswg=5.0000e-10 + dcjgate_n_18_mm ctp=9.1400e-04

- + ptp=9.2400e-04 cta=9.1900e-04 pta=1.5800e-03
- + elm=5.0000e+00 tlevc=1.0000e+00
- + noimod=2 noia=1.3182567385564E+19 noib=144543.977074592
- + noic=-1.24515794572817E-12 ef=0.92

- + em=41000000

APPENDIX B

(A)SOURCE NETLIST OF NMOS FOUR-QUADRANT MULTIPLIER:

```
// Library name: mohan
// Cell name: nmos analog multiplier
// View name: schematic
V1 (0 v2) vsource mag=1 type=sine ampl=50m freq=50K
V0 (v1 0) vsource mag=1 type=sine ampl=50.0m freq=50K
C0 (vout\- 0) capacitor c=1f
C1 (vout\+ 0) capacitor c=1f
M12 (vout\- net097 vdd vdd) p_18_mm w=10u l=2u ad=4.9e-12 as=4.9e-12 \
    pd=20.98u ps=20.98u m=(1)*(1)
M13 (vout\+ net095 vdd vdd) p_18_mm w=10u l=2u ad=4.9e-12 as=4.9e-12 \
    pd=20.98u ps=20.98u m=(1)*(1)
M11 (0 net065 net10 vdd) p_18_mm w=10u l=2u ad=4.9e-12 as=4.9e-12 \
    pd=20.98u ps=20.98u m=(1)*(1)
M10 (net10 v1 vdd vdd) p_18_mm w=10u l=2u ad=4.9e-12 as=4.9e-12 pd=20.98u \
    ps=20.98u m=(1)*(1)
M6 (net0108 v2 vdd vdd) p_18_mm w=10u l=2u ad=4.9e-12 as=4.9e-12 pd=20.98u \
    ps=20.98u m=(1)*(1)
M1 (0 net0102 net060 vdd) p_18_mm w=10u l=2u ad=4.9e-12 as=4.9e-12 \
    pd=20.98u ps=20.98u m=(1)*(1)
M7 (0 net065 net0108 vdd) p_18_mm w=10u l=2u ad=4.9e-12 as=4.9e-12 \
    pd=20.98u ps=20.98u m=(1)*(1)
M0 (net060 v1 vdd vdd) p_18_mm w=10u l=2u ad=4.9e-12 as=4.9e-12 pd=20.98u \
    ps=20.98u m=(1)*(1)
M9 (0 net073 net0104 vdd) p_18_mm w=10u l=2u ad=4.9e-12 as=4.9e-12 \
```

```
    pd=20.98u ps=20.98u m=(1)*(1)
M8 (net0104 v2 vdd vdd) p_18_mm w=10u l=2u ad=4.9e-12 as=4.9e-12 pd=20.98u \
    ps=20.98u m=(1)*(1)
M5 (vout\+ net10 0 0) n_18_mm w=4u l=2u ad=1.96e-12 as=1.96e-12 pd=8.98u \
    ps=8.98u m=(1)*(1)
M4 (vout\+ net0104 0 0) n_18_mm w=4u l=2u ad=1.96e-12 as=1.96e-12 pd=8.98u \
    ps=8.98u m=(1)*(1)
M3 (vout\- net0108 0 0) n_18_mm w=4u l=2u ad=1.96e-12 as=1.96e-12 pd=8.98u \
    ps=8.98u m=(1)*(1)
M2 (vout\- net060 0 0) n_18_mm w=4u l=2u ad=1.96e-12 as=1.96e-12 pd=8.98u \
    ps=8.98u m=(1)*(1)
V112 (net073 0) vsource dc=250m type=dc
V113 (net065 0) vsource dc=300m type=dc
V90 (0 net097) vsource dc=500m type=dc
V92 (net0114 0) vsource type=dc
V18 (vdd net0114) vsource dc=1 type=dc
V91 (0 net095) vsource dc=500m type=dc
V114 (net0102 0) vsource dc=250m type=dc
```

(B) SOURCE NETLIST OF LOW-VOLTAGE ANALOG MULTIPLIER:

```
// Library name: mohan
// Cell name: low voltage analog multiplier
// View name: schematic
M7 (net49 net49 net0116 net0116) p_18_mm w=9u l=3u ad=4.41e-12 as=4.41e-12 \
    pd=18.98u ps=18.98u m=(1)*(1)
M8 (net45 net45 net0116 net0116) p_18_mm w=9u l=3u ad=4.41e-12 as=4.41e-12 \
    pd=18.98u ps=18.98u m=(1)*(1)
M6 (x7 x7 net0116 net0116) p_18_mm w=9u l=3u ad=4.41e-12 as=4.41e-12 \
    pd=18.98u ps=18.98u m=(1)*(1)
M1 (net113 net113 net0116 net0116) p_18_mm w=9u l=3u ad=4.41e-12 \
```

```
    as=4.41e-12 pd=18.98u ps=18.98u m=(1)*(1)
M5 (x8 x8 net0116 net0116) p_18_mm w=9u l=3u ad=4.41e-12 as=4.41e-12 \
    pd=18.98u ps=18.98u m=(1)*(1)
M4 (net106 net106 net0116 net0116) p_18_mm w=9u l=3u ad=4.41e-12 \
    as=4.41e-12 pd=18.98u ps=18.98u m=(1)*(1)
V2 (net0248 0) vsource mag=1 type=sine
V1 (net0139 0) vsource mag=1 type=sine
V5 (0 net0197) vsource mag=1  type=sine
V3 (net0156 0) vsource mag=1 type=sine
V4 (0 net0120) vsource mag=1  type=sine
V7 (0 net0241) vsource mag=1  type=sine
V6 (0 net0112) vsource mag=1  type=sine
C1 (x7 0) capacitor c=1f
C2 (x8 0) capacitor c=1f
V86 (net0167 0) vsource type=dc
V87 (net0158 net0139) vsource dc=50m type=dc
V88 (net0249 net0248) vsource dc=50m type=dc
V89 (net0154 net0156) vsource dc=50m type=dc
V14 (0 net17) vsource dc=300m type=dc
V0 (net0116 net0167) vsource dc=900.0m type=dc
V15 (0 net0186) vsource dc=900.0m type=dc
V76 (0 net0161) vsource dc=450m type=dc
M33 (net0116 net106 net96 net96) n_18_mm w=3u l=3u ad=1.47e-12 as=1.47e-12 \
    pd=6.98u ps=6.98u m=(1)*(1)
M34 (net0116 net113 net96 net96) n_18_mm w=3u l=3u ad=1.47e-12 as=1.47e-12 \
    pd=6.98u ps=6.98u m=(1)*(1)
M41 (net33 net17 net0186 net0186) n_18_mm w=6u l=3u ad=2.94e-12 \
    as=2.94e-12 pd=12.98u ps=12.98u m=(1)*(1)
M42 (net42 net17 net0186 net0186) n_18_mm w=6u l=3u ad=2.94e-12 \
    as=2.94e-12 pd=12.98u ps=12.98u m=(1)*(1)
```

```
M37 (net124 net17 net0186 net0186) n_18_mm w=6u l=3u ad=2.94e-12 \
    as=2.94e-12 pd=12.98u ps=12.98u m=(1)*(1)
M48 (net0116 net0158 net33 net33) n_18_mm w=3u l=3u ad=1.47e-12 \
    as=1.47e-12 pd=6.98u ps=6.98u m=(1)*(1)
M47 (net0116 net0197 net42 net42) n_18_mm w=3u l=3u ad=1.47e-12 \
    as=1.47e-12 pd=6.98u ps=6.98u m=(1)*(1)
M49 (net49 net0154 net42 net42) n_18_mm w=3u l=3u ad=1.47e-12 as=1.47e-12 \
    pd=6.98u ps=6.98u m=(1)*(1)
M50 (net45 net0120 net33 net33) n_18_mm w=3u l=3u ad=1.47e-12 as=1.47e-12 \
    pd=6.98u ps=6.98u m=(1)*(1)
M39 (net82 net0161 net0186 net0186) n_18_mm w=6u l=3u ad=2.94e-12 \
    as=2.94e-12 pd=12.98u ps=12.98u m=(1)*(1)
M38 (net96 net17 net0186 net0186) n_18_mm w=6u l=3u ad=2.94e-12 \
    as=2.94e-12 pd=12.98u ps=12.98u m=(1)*(1)
M45 (net0116 net49 net79 net79) n_18_mm w=3u l=3u ad=1.47e-12 as=1.47e-12 \
    pd=6.98u ps=6.98u m=(1)*(1)
M46 (net0116 net45 net79 net79) n_18_mm w=3u l=3u ad=1.47e-12 as=1.47e-12 \
    pd=6.98u ps=6.98u m=(1)*(1)
M43 (x8 net96 net82 net82) n_18_mm w=6u l=3u ad=2.94e-12 as=2.94e-12 \
    pd=12.98u ps=12.98u m=(1)*(1)
M44 (x7 net79 net82 net82) n_18_mm w=6u l=3u ad=2.94e-12 as=2.94e-12 \
    pd=12.98u ps=12.98u m=(1)*(1)
M40 (net79 net17 net0186 net0186) n_18_mm w=6u l=3u ad=2.94e-12 \
    as=2.94e-12 pd=12.98u ps=12.98u m=(1)*(1)
M10 (net128 net17 net0186 net0186) n_18_mm w=6u l=3u ad=2.94e-12 \
    as=2.94e-12 pd=12.98u ps=12.98u m=(1)*(1)
M3 (net113 net0241 net124 net124) n_18_mm w=3u l=3u ad=1.47e-12 \
    as=1.47e-12 pd=6.98u ps=6.98u m=(1)*(1)
M2 (net0116 net0112 net124 net124) n_18_mm w=3u l=3u ad=1.47e-12 \
    as=1.47e-12 pd=6.98u ps=6.98u m=(1)*(1)
```

```
M32 (net106 net0249 net128 net128) n_18_mm w=3u l=3u ad=1.47e-12 \
    as=1.47e-12 pd=6.98u ps=6.98u m=(1)*(1)
M0 (net0116 net0158 net128 net128) n_18_mm w=3u l=3u ad=1.47e-12 \
    as=1.47e-12 pd=6.98u ps=6.98u m=(1)*(1)
```

(C) LAYOUT NETLIST OF LOW-VOLTAGE ANALOG MULTIPLIER

```
*
*
*
*          LINUX     Tue Jul  5 13:54:34 2011
*
*
*
*  PROGRAM  advgen
*
*  HSPICE LIBRARY
*
*
*
.GLOBAL vdd gnd
*
.SUBCKT muld v1 v2 vgg vout1 vout2
*
*
*  caps2d version: 10
*
*
*     TRANSISTOR CARDS
```

```
*
*
M44    vout1#6 net187  net184  gnd    N_18_MM L=3U    W=6U
+ effW=6e-06
M45    vdd    net175  net187#10      gnd    N_18_MM L=3U    W=3U
+ effW=3e-06
M40    net187#3      vgg#9   gnd    gnd    N_18_MM L=3U    W=6U
+ effW=6e-06
M46    vdd    net179#3      net187#7      gnd    N_18_MM L=3U
+ W=3U  effW=3e-06
M41    net137  vgg#11  gnd    gnd    N_18_MM L=3U    W=6U
+ effW=6e-06
M50    net179#5      v2#12   net137#7      gnd    N_18_MM L=3U
+ W=3U  effW=3e-06
M42    net160  vgg#20  gnd    gnd    N_18_MM L=3U    W=6U
+ effW=6e-06
M49    net175#7      v2#15   net160#7      gnd    N_18_MM L=3U
+ W=3U  effW=3e-06
M47    vdd    v1#9    net160#4      gnd    N_18_MM L=3U    W=3U
+ effW=3e-06
M48    vdd    v1#11   net137#5      gnd    N_18_MM L=3U    W=3U
+ effW=3e-06
M39    net184#5      vgg#7   gnd    gnd    N_18_MM L=3U    W=6U
+ effW=6e-06
M2     vdd    v1#1    net204#3      gnd    N_18_MM L=3U    W=3U
+ effW=3e-06
M0     vdd    v1#6    net212#4      gnd    N_18_MM L=3U    W=3U
```

```
+ effW=3e-06
M32   net97#5 v2#3   net212  gnd   N_18_MM L=3U   W=3U
+ effW=3e-06
M10   net212#5      vgg#1  gnd   gnd   N_18_MM L=3U   W=6U
+ effW=6e-06
M3    net89#2 v2#5   net204  gnd   N_18_MM L=3U   W=3U
+ effW=3e-06
M37   net204#5      vgg#3  gnd   gnd   N_18_MM L=3U   W=6U
+ effW=6e-06
M34   vdd   net89#8 net132#6      gnd   N_18_MM L=3U
+ W=3U  effW=3e-06
M38   net132  vgg#5  gnd   gnd   N_18_MM L=3U   W=6U
+ effW=6e-06
M43   vout2#1 net132#9      net184#3      gnd   N_18_MM
+ L=3U  W=6U   effW=6e-06
M33   vdd   net97#10      net132#7      gnd   N_18_MM L=3U
+ W=3U  effW=3e-06
M4    net97#6 net97  vdd   vdd   P_18_MM L=3U   W=9U
+ effW=9e-06
M1    net89#5 net89#7 vdd   vdd   P_18_MM L=3U
+ W=9U  effW=9e-06
M5    vout2#4 vout2#8 vdd   vdd   P_18_MM L=3U
+ W=9U  effW=9e-06
M6    vout1#3 vout1#5 vdd   vdd   P_18_MM L=3U
+ W=9U  effW=9e-06
M8    net179#8      net179  vdd   vdd   P_18_MM L=3U   W=9U
+ effW=9e-06
```

```
M7     net175#10      net175#5       vdd     vdd     P_18_MM L=3U
+ W=9U  effW=9e-06
*
*
*      RESISTOR AND CAP/DIODE CARDS
*
Rh1    v1#1    v1#2      38.5633
Rh2    v1#6    v1#3      22.5675
Rh3    v2#3    v2#1      20.5867
Rh4    vgg#1   vgg#2     37.9490
Rh5    net97   net97#2    41.7490
Rh6    v2#5    v2#6      34.2379
Rh7    vgg#3   vgg#4     37.9490
Rh8    net89#7 net89#6    29.7490
Rh9    net89#8 net89     27.4119
Rh10   vgg#5   vgg#6     37.9490
Rh11   vout2#8 vout2#6    29.7490
Rh12   net132#9       net132#3         34.1490
Rh13   net97#10       net97#9    27.4276
Rh14   vgg#7   vgg#8     37.9490
Rh15   vout1#5 vout1#1    26.7490
Rh16   net187  net187#2         45.9490
Rh17   net175  net175#2         32.1445
Rh18   vgg#9   vgg#10    37.9490
Rh19   net179  net179#2         41.7490
Rh20   net179#3       net179#4         37.1445
Rh21   vgg#11  vgg#12    37.9490
```

Rh22	net175#5	net175#6	41.7490
Rh23	v2#12	v2#9	21.7427
Rh24	vgg#20	vgg#13	25.9490