SPLIT GATE JL MOSFET WITH UTB FOR SENSING THE DOPING CONCENTRATION

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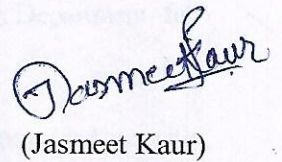
DECLARATION

I, hereby declare that the dissertation titled **"Split gate JL MOSFET with UTB for sensing doping concentration"** in the partial fulfillment of the requirement for degree of Master of Technology in VLSI DESIGN submitted in Electronics and Communication Engineering Department of Thapar Institute of Engineering and Technology, Patiala is an authentic record of my study carried out as under the guidance of **Mr. Arun Kumar Chatterjee** (Assistant Professor, ECED) during 2017-2019.



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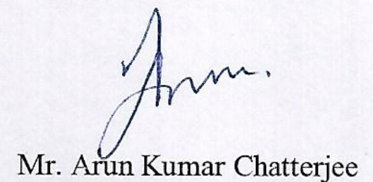

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ABSTRACT

In the conventional bulk MOSFET, as the size of the MOSFET reduces the Short Channel Effects are introduced. To overcome the issues that are occurring due to scaling of the bulk MOSFET, modification in the bulk MOSFET such as Silicon on insulator, Multi-gate devices that is double gate MOSFET , triple gate MOSFET and Fin Field Effect transistor structure. With the help of the mentioned devices there is a reduction in Short Channel Effects of conventional MOSFET. Devices which are based on the silicon on insulator, reduce the problems of leakage mechanism like GIDL, DIBL and drain to body leakage current etc. In the devices which has the multi-gate structure that device has the better control of the gate voltage on the drain current.

To overcome the issues that are occurring in the conventional mutigate devices can be resolved with the help of the Junctionless DG MOSFET. JL DG MOSFET based sensors can be used fir biosensing applications. In this thesis work two different JL DG MOSFET as we studied and compared. Each one can be used to sense the biomoleccules and concentration of the micro nutrients in the water by just sensing the small change in Dielectric constant of the biomolecules.

A Junctionless DG MOSFET sensor is designed on SILVACO TCAD Tool. Here, we have four-split gates and the underlap region between two gates has been used for sensing application. The underlap region is coated by the biomolecule (biopolymer) with particular concentration of the micro-nutrients. This gives a finite value of the dielectric constant of this mixture by varying the concentration of the micro nutrient in the mixture. The dielectric constant will change the conductivity of the underlap region two channels, which can be easily sensed by the MOSFET operation of the sensor.

A new quadruple split gate JL MOSFET has also been designed and stimulated. The stimulation results show that the new proposed sensor has larger sensitivity than other sensors for the sensing of micro nutrients in the biomolecule. Here the underlap channel region in between the gates has been coated with the biomolecule with the particular concentration of the micro-nutrients. Different concentration ($1X10^{16}$ to $1X10^{17}$ cm^{-3}) of the boron has been sensed by the biosensor, in terms of threshold voltage of the quadruple split gate JL MOSFET.

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ACRONYMS

ICs	Integrated circuits
MOSFETs	Metal oxide semiconductor field effect transistor
CMOS	Complementary metal oxide semiconductor
SCEs	Short Channel Effects
DG	Double gate
JL	Junctionless
DG MOSFET	Double gate MOSFET
DG JL MOSFET	Double gate junctionless MOSFET
UTB	Ultra Thin Body
DIBL	Drain induced barrier lowering
GIDL	Gate induced drain leakage current
SOI	Silicon on insulator
FET	Filed effect transisitor
SDG	Symmetric double gate
ADG	Asymmetric double gate
JLT	Junctionless transistor

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CHAPTER 1

INTRODUCTION

1.1 BACKGROUND

In the early years of the development of integrated electronics, integrated circuits (ICs) contained only a few transistors. With the ever increasing complexity in the circuits, the number of components in these circuits increased steadily. To meet this growing demand of increasing components in a chip, scaling of components started. Metal Oxide Semiconductor Field Effect Transistors (MOSFETs) use Metal Insulator Semiconductor (MIS) as their main component, are now majorly used for IC development over the past two decades. With the advancing technology, silicon based MOSFETs have continually delivered performance gain with reduction in the cost of manufacturing. Moore's law states that after every 18 months the number of transistors will be double in an integrated (ICs) circuits. Semiconductor industry has kept up with this law with tremendous advancements in the field of device scaling. The dimensional scaling of CMOS has been one of the key driving forces behind the evolution of semiconductor electronics. Today, CMOS based semiconductor electronics can be found everywhere around us, ranging from portable electronics to the telecommunications sector. Channel length of the MOSFET is decreasing day-by-day in the industry then due to that the the short channel effets (SCEs) [1] arises in the MOSFET and because of the SCEs the performance of the MOSFETs gets reduced. So to overcome (or reduce) the SCEs in the MOSFET and improve the performance of the device at that time the MULTI-GATE device come into industry. So at that time DG MOSFET is one of the best device that come into use in the industry.

A lot of research and tremendous amounts of resources have gone into device layout from the past thirty year. The development of DG JL MOSFET is used to overcome most of the issues related to the normal silicon used devices and it is also for the semiconductor used devices. Here it becomes very challenging to manufacture a device with the 3rd and 5th compound materials inside the short channel effects and the ultra thin bodies. In nanometer regime there should have a accurate control of doping is wanted because of the sharply specified junctions, because of that an expensive techniques are going to be used for the fabrication like ultra-fast annealing method. There is also a lot of issues like loss of electrostatic charges take place in the channel. Hence the multigate devices has been proposed. Because of these issues the JL DG MOSFET is fabricated to overcome the issues that are taking place in the single gate MOSFET. There should be a two key parameters which are going to be used in plotting the structure of Junctionless MOSFET [2]:

1. High doping concentration in the approximately thin and confined body, which creates the flow of the current from the source to drain when V_{gs} is apply.
2. Use of gate material with the high work function, so that the fine body will be depleted fully during its off state.

1.1.1 Short Channel Effects

1. **Drain Induced Barrier Lowering (DIBL) and Punch through:**

   Punch through arises in the depletion regions when it is encircling by the drain which is boarden towards the source because of the reverse bias and after certain time it get merges in the source. It can be reduced with the help of the larger doping in the substrate, fine oxides and the shallower junctions. Current flows in the MOSFET over an inversion layer. This inversion layer is formed by applying gate bias that is greater than its threshold voltage. If the voltage applied on the gate voltage is less from threshold voltage of MOSFET, potential barrier reduces, and the carriers can move from source to drain even at low gate voltages. Thus, even if gate voltage has not increases beyond the threshold voltage, sub-threshold current flows in the device. This phenomenon of the reduction in the potential barrier because of voltage that is applied on the drain is known as drain induced barrier lowering (DIBL) [1].

2. **PN Junction Leakage Currents:**

   Source and Drain to well junctions are reverse biased (R.B.) and there is a reverse biased current associated with this biasing. This reverse bias current is comprised of two components, minority carrier current and current due to recombination of charges. The minority carriers current and current due to drift/diffusion in the depletion region. This reverse bias current mainly depends on the junction area and doping. With the increase in the concentration of PN junction doping with the halo implants, then band to band tunneling current dominates reverse bias current [1].

3. **Hot Electrons:**

   Hot electrons [1] result from the high electric field in the device due to small geometry. Electrons present inside the substrate region gain enough energy so that it can overcome barrier formed by the potential and enter the oxide region. The accumulation of these electrons in the oxide region result in the increase of threshold voltage and thus affects the reliability of solid state devices greatly. It adversely affects the gate control over the drain current. These electrons cause leakage currents within the device and result in larger power dissipation.

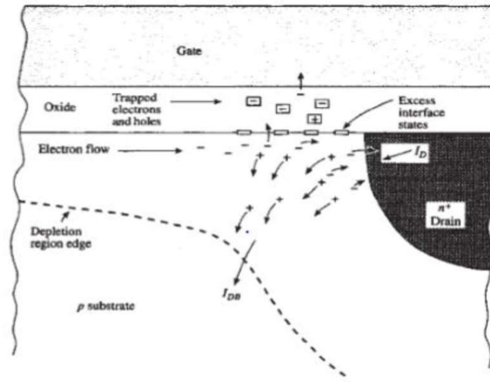

Figure 1.1 Hot electrons [3]

4. **Impact Ionization:**

   Because of the presence of the high velocity of electrons in longitudinal field which are capable of generating electron and the hole pairs with the impact of the atmos of silicon and ionizing them, due to that, an unacceptable short channel effect [1] happens. With the proper biasing, large number of electrons are attracted towards drain and the holes are substituting the parasitic current by entering into the substrate. The space between source and the drain acts as a base of N-P-N transistors, with that of the source and the drain are acting as emitter and collector. The hole current is formed with the help of the holes that are composed with the source, a voltage drop is created and the previously reverse biased substrate source junction begins to conduct. This situation get worse if the electrons that are generated by the high fields which enter the substrate and affect the nearby devices.

5. **Surface Scattering:**

   With the expansion of the depletion layer inside the region of channel, then the channel turns in smaller and longitudinal electric field lines enhances, and as a result the mobility of the surface depends on the field. Surface scattering occurs when the collisions take place between the electrons that are attracted towards the interface of the transistor. This phenomenon results in reduction of mobility to that of the bulk mobility.

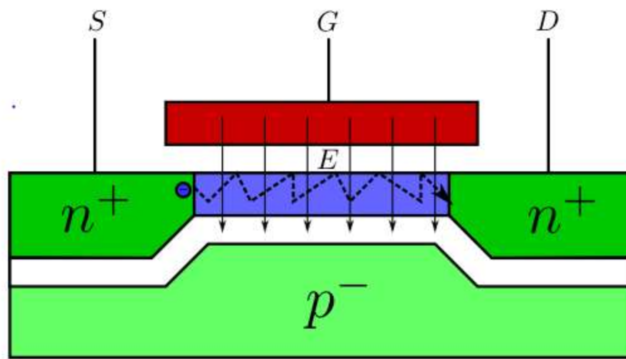

Figure 1.2 Surface Scattering

6. **Oxide Leakages:**

   Oxide leakage are caused within the device through gate to the substrate due to reduction in the gate oxide thickness. Electron start tunneling through the gate to substrate. Oxide leakage results in higher power dissipation in the device. These leakage can be reduced by using high k dielectric material for gate terminal.

7. **Gate Induced Drain Leakage(GIDL):**

   With the scaling and increased voltages, electric field at drain overlap becomes extremely high[4]. This increased electric field results in depletion of carriers into drain overlap region. The valence band of gate and conduction band of drain region overlaps. This overlapping results in band to band tunneling of electrons from gate to drain

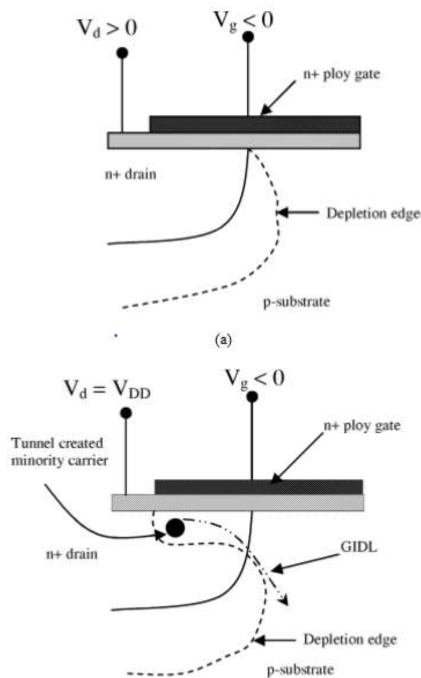

Figure 1.3 GIDL [1]

1.1.2 Technologies That Overcome Challenges of Scaling

To overcome challenges imposed by scaling the complexity in fabrication of conventional MOSFET is increased due to incorporation of techniques called strained silicon, epitaxial layer formation, isolation techniques etc. Alternate approaches such as SOI MOSFETs, tunnel FETs, FINFETs, and many other unconventional techniques are used to overcome scaling issues. Among all junctionless field effect transistors used in place of bulk MOSFETs.

1. **DG MOSFET**

Double gate MOSFET is the most important individual from the MG-MOSFET device. DG MOSFET has higher trans-conductance(g_m) and better switching capability than that of the single gate MOSFET. Most important thing for the double gate MOSFET is to have a control on the silicon channel and minimize the silicon channel width and apply the contact of the gate on both the sides of the channel. These both the ideas are going to help the SCEs and increases the current in comparision to that of the single gate metal oxide semiconductor FET.

As the count of the gate increases then it make the better electrostatic control on the channel of the DG MOSFET and it also help in diminishes the SCE, threshold voltage (Vth), leakage current and DIBL [2].

DG MOSFET is pointed as the regular MOSFET structure [4], here the second gate is placed below the substrate where the channel is formed. It is one of the most effective MOSFET where both gates are connected to the same voltage and the dielectrics of both the top and bottom gate of the MOSFET has same thickness.

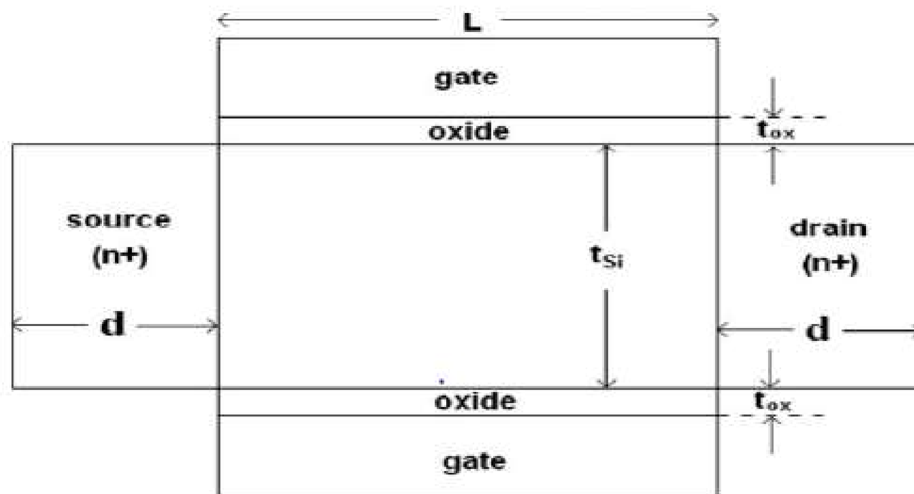

Figure 1.4 Double gate MOSFET

There are two types of DG MOSFET [3]:

1) Symmetric DG MOSFET: symmetric double gate MOSFET is that which have identical material used for both the gates or they have the same work function in the structure. In SDG MOSFET both the gates are connected to the same bias. When the DG MOSFET is in ON state then the two conducting channels are formed in the MOSFET on both the sides of the substrate [4]. SDG MOSFET shows higher carrier mobility because of the lower electric field.
2) Asymmetric DG MOSFET: in asymmetric Double Gate MOSFET different materials are used on both gate or their work functions are different. In ASD MOSFET switching can be obtained by applying the different bias on both the gate of the MOSFET [4]. In ADG MOSFET single channel is formed until operation voltage is high. The V_{th} (threshold voltage) of ADG MOSFET can be balanced by the substrate thickness of the device or with the thickness of the oxide thickness.

It is possible to scale DG MOSFET more than the bulk MOSFET because the silicon layer of the device can be made thinner as compared to the depletion layer. Thus length of the gate will be scaled to a smaller value. The capacitor divider effect is negligible in DG.

There are three operations are DG MOSFET:

1) Three terminal operations: In 3T there are 3 different voltages are applied to that the device i.e. the same value of voltage is used on the both the sides of gates (they act like a shorted). 3T-operation is most widely used in DG MOSFET because less number of voltages are required in comparison to that of the independent configuration [5].
2) Four terminal operation: here different biasing is done on the gates of the DG MOSFET. Because of the different bias it is known as the independent configuration. In 4T one of the gate act as the controlling gate where as the second i.e. is the back gate act as a supported gate which help in altering the threshold voltage [5].

Advantages of DG MOSFETS on single MOSFET:

1) In DG MOSFET the efficiency of the transistor is greatly increased as the device is scaling down in comparison to that of the single gate MOSFET.
2) As gate to channel coupling is doubled in the DG MOSFET which is useful in suppressing the SCE's of the device.
3) Here very low doped or undoped channel are used in DG MOSFET which provide the better carrier mobility in decreased dimension and hence it provide the better switching time. Hence the leakage current or the off-state current is reduced.
4) Here the current driving of the DG MOSFET is double to that of the planar CMOS because of that the DG MOSFET operated at the much lower input and (Vth) threshold voltage. Hence the power consumed by the DG MOSFET is less.

5) Gates on both the sides of the DG MOSFET have a control on the electric field, which help in determining the quantity of the current flowing from the channel of MOSFET. Hence DG MOSFET are going to be operated on the lower voltage [6][7].

2. Junctionless Transistors

A JL device is the device which has uniform doping concentration and of the same type from source to drain including the channel region. This device overcome the issues that are faced by the conventional nanoscale device. In JLT's (junctionless transistors) channel region has the high doping concentration because of which it act as the fully depleted in it's OFF state. In junctionless transistors the high K gate metals are used. There should be high work function difference as compare to that of the channel. To form a conducting channel between source and drain, biasing is to be done on the gate to bring the channel out of the depletion. In JL MOSFET there should be single semiconducting bar with the constant doping concentration is present between the source and drain. Doping of this bar should be high for conductance between the source and drain. This device is modeled like a resistor, the resistance of which can be controlled by the gate.

The depletion width in a JLT is very small as the doping is very high, an ultra-thin silicon body is required for JLT.

3. Double Gate Junctionless Transistor

The scaling in the channel length of the MOSFETs, shows rising severe challenges as leakage current and the short-channel effects which are increasing due to reducing controlling ability of gate on channel of the device. In a Multi gate MOSFET, the gate electrode is all around a silicon surface, creating a multi-gate structure which has an perfect control on potential of channel region, so let one to be FD the channel. In short-channel devices, with the development of the pointed source and drain junctions it is entirely a challenge and set a extreme conditions on doping techniques and on the thermal cost of the device. The Junctionless transistor is a resistor which has same doping throughout. The doping concentration is consistent throughout the drain, channel and source. When the doping concentration is not present then it removes the diffusion of impurities and issues of pointed doping profile formation as a whole. Any rise in the temperature results in variation of the electrical specification of Metal Oxide Semiconductor devices (e.g., increase in leakage current, shift in the threshold voltage and reduction of mobility). Currently, a double gate junctionless FET has been stated as promising candidate for the forthcoming technology growth. Technically, all undoped DG MOSFETs are junctionless, if the doping concentration in the channel region of the consistent as source and drain. The fabricated junctionless devices which has high value of impurity concentration within the channel, source and the drain regions requires no junctions and demonstrate many advantages, like the simple fabrication method nearly ideal subthreshold slope, high on-off current ratio, small value of Source/drain series resistance, and

small drain induced barrier lowering. Moreover, the JL transistor shows many interesting characterstics, like conductance oscillations at low temperature and high temperature behavior.

The JLT is a densely doped Silicon on insulator resistor with Metal oxide semiconductor gate which controls the flow of current. Doping concentration is fixed and consistent throughout the device and its range is from 10^{17} and 10^{20} per cm^3. The device characteristics bulk conduction in place of surface channel conduction. The operational principal of an n-channel DG JL MOSFET is distinct from the standard n-channel DGJL MOSFET. In the sub-threshold region, a heavily doped channel is FD; so, it can grasp a large electric field. By rising the gate voltage, the electric field starts reducing in the channel as far as the neutral channel region is formed inside the channel. At this point, it is important to describe the threshold voltage so a current in the bulk starts to flow through the middle of the channel region. After that, by further rising (increasing) the voltage at the gate, width of the depletion region starts reducing until a completely neutral channel region is created. This happens, when the voltage at the gate is equals to the flat band voltage. At the beginning of the condition, the current in the bulk start reaching its maximum value. After that, by rising, the voltage at the gate terminal, then the negative charges accumulating on the surface of channel region. These charges help in flowing the current at the surface, which is similar to that of the basic n-channel DGJL FET. However, the current at the surface start flowing at a gate voltage which is much higher than that of the threshold voltage for the current in the bulk. Thus, the bulk start driving the total current inside the Junctionless transistors.

In comparision to that of the regular junction based devices, principal of the working(operations) of the DGJL Metal oxide semiconductor FETs is depend on the current flowing through the silicon layer at place of Si-SiO2 interface. Ideally, the doping density of the channel of DGJL Metal oxide semiconductor FETs becomes quite high to drive the high current densities. Otherwise, turning off the device, needs to be FD the channel region of the mobile charges, which become difficult, if the doping concentration is exceeding largly. By considering a n-type doped channel, by assuming the layer of silicon which is heavily doped and the thick, it is impossible to FD the channel region from the electrons, even at the lower gate voltages which the device can bear. Depending upon the technical parameters, a hole inverted layer has also been build up at the interface of the channel, then by further screening the electric field at the gate and securing the electrons depletion at the centre of the channel.

1.2 LITERATURE REVIEW

1.2.1 Background

To understand transformation of the integrated electronics and according to its present day development, its must to comprehend the fundamental concept of Metal oxide semiconductor FET, then history of MOSFET leds to the advancement of the Metal oxide semiconductor FETs. Then, the basic performance of the Metal oxide semiconductor FET, their distinctive region of operations and approximate approaches of device. These papers are going to discuss the various

characteristic of the devices that are formed between the drain current and voltages of drain and gate of the device on a linear and on a logarithmic scales. The capacitances and their effects, which are created between distinct region of the device is studied [8].

With the understanding of the devices, it gave us concept of fabricating the device on a single wafer by rising the integrity. Which help in lowering the area which are important for the transistor in chip, which doubles after every twenty fourth months [9].

Basically, concept of integrating the device on a single chip undergoes to a scaling. So, scaling is a method of decreasing the dimension, supplied voltage and the other specification of the device in the order of increasing the integrity. Scaling with respect to different parameters leads to distinct type of scaling [10][11].

Normally, scaling devices results in the compressing the device dimensions, thereby decreasing their length of the channel, width of the channel and the other specifications. These decreasing dimensions results in the SCEs are to be studied [1]. SCEs are going to affect the working and the dependability of device and it provide the unwanted outputs and the prominent SCEs is the leakage current. Leakage current is that which flood in the device in a weak inversion region [12]. These current due to leakage arises because of the different mechanism which are needed in study so that reduction techniques are studied.

There are certain distinct techniques that are compensate the current of leakage in bulk Metal oxide semiconductor FET [13]. These reduction techniques [14] will be differentiaited depending on the new materials.

Order, to solve these issues of the short channels effects, a new design of the single bulk MOSFET is introduced. In the new architectural design device there should be slight changes in the fabrication of the bulk MOSFET. These devices be SOI, DG and multiple gate Field Effect Transistor structures. A very concise study of the devices are completed and the analysis of these devices, their performance, action and advantages over the bulk MOSFET. Multi gate devices are used to help in decreasing the SCEs of the conventional bulk MOSFET. Silicon on insulator make better the short channel effects by take off the terminal at the body of the conventional MOSFET, rather it consist of the BOX layer. By taking off the body, it decreases the leakage mechanism that is in DIBL, GIDL, drain to leakage current of the body et.al. silicon on insulator is fundamentally classified as PD and FD SOI. Classification of the Silicon on insulator is studied depending on the silicons thickness in comparison of the depletion layer. Partially depleted SOI has a compact body which are represented as the floating terminal, when it is't grounded. This terminal of the floating body of the device give boost to the kink effects which diverge the mechanism of current from its characteristics behavior. Absence of kink effect in the fully depleted SOI because of the absence of the body terminal [14][15].

Then with the further conversion of the silicon on insulator give acceleration to the double gate MOSFET, which are having the dual gates that is at the back gate and front gate. Because of the dual gate it provides the better control of the voltage of gate upon the threshold voltage (Vth).

Hence, by rising the number of gates around the channel it will support in increasing the gate controllability over V_t. this type of concepts give rise to the multi gate FET structures. Short channel effects are the present extent in the devices.

Therefore, for reducing the SCEs, then a new device is brought into, that is the junctionless transistors. In the junctionless device the uniform doping is done along the region of the channel-source and the channel-drain regions which are overcomed by the objections that are faced by the nano scale devices. In these there is low leakage current and it has easy fabrication method in comparision to that of the conventional MOSFET [16]. Due to the heavily doped concentration in the region of channel, it origin results in the reduction of the mobility of carrier which concluded in small current and the transconductance of junctionless MOSFETs. Today, in junctionless MOSFET here the maximum value of voltage is applied on the gate terminal and then the there is the decrease in the drain current of the saturation region. This occur due to the source/drain implantation, which decreases the same order resistances but on a same time it start rising the parasitic capacitance by creating the delay inside the circuits.

To understand how there surface potential vary, there drain current and subthreshold slope and current. Duarte et al.[17] here the author proposed the bulk model of current which is relying on the depletion approximation of the Junctionless DG MOSFET however neglecting the accumulation condition. Then the Sallese et al. [18] has proposed a JL DG MOSFET for the space charge based models for calculating the density of charge and the drain current, although it results in the convergence related issues. Later, Duarte at al. [19] has proposed a non- piecewise modelled device for junctionless double gate MOSFET which is depended on the parabolic potential approximation with the help of the uniform charge potential relationship. To established a surface potential which is depend on the compressed model, few studies which are carried out to introduce a junctionless DG MOSFET which is valid for all the regions, which comprises of a physical and define the details of the transistor behavior that is usually accepted in the compressed modeled applicatons.

Then Chen et al. [20] had proposed a model which has the surface potential depend on the drain current which has longest channel of DG JL MOSFET. Here the model is on abrupt depletion that is taking place between the depleted and neutral region of the device, which shows discontinuities in the surface potential and current of drain characteristics of the device. Then Jazaeri et al. [21] here author investigating the technical constraints and the design limitation of a UTB for JL double gate MOSFET. Author developed the analytical approach which assure the devices that will effectively switched OFF the device at the given value of current by proposing the relationship between thickness of the silicon and that of the density of the doping for the longest channel double gate MOSFET. And then the ON current, maximum operating voltage and I_{on} and I_{off} ratio has been investigated. Then Jazaeri et al. [22] has develop a solution for the trans-capacitances in long channel double gate junctionless MOSFET which are going to be valid for all the regions of operations. Here use a fully charge based model, by adopting the ward-dutton

partitioning principal. Then a complete network of the capacitance is obtained, which step the technology more towards the compact model circuit simulation.

Chowdhury et al. [23] proposed a new modeled device for the long channel of symmetric double gate junctionless MOSFET which is depend on the gradual depletion inside the region of the channel. This approach is used determine the surface potential. Characteristics of the surface potential become smooth between the fully depleted regions and that of the partially depleted regions. This proposed model has a improved performance to that of the chen et al. [20] who propsed the a surface potential model which is based on the drain current of junctioless double gate MOSFET.in this model shows the smooth chracteristics formed between the neutral and depleted regions as compared to that of the chen et al. [20] in chen device he shows the sudden depletion between the neutral and the depleted region. This model is not derived for short channel devices and quantum effects. This new proposed model of the device is validated for all the regions of device operation and it supply the continous transition from one region of the device to other region. This features of continuity make the device model better for studying the operation of the device and characteristics of the junctionless double gate MOSFET. Now, Jazaeri et al. [24] proposed a model which is based on the charged dependent model of the SDG JL field effect transistor which accounts to the inverted layer which is biased on the gate voltage in deep depletion. In this paper the transcapcitance model of Jazaeri [22] and core model transcapacitance core model network by sallese is used [18] here. This model of the new device is now able to define the sudden rise in capacitances of the gate which is biased device in the deep depletion including the theoretical limits of the off current. From this model author concluded that this model is helpful in calculating the electron and the hole densities [25] in junctionless double gate MOSFET and junctionless network from depletion inversion. It is based on the two charged equations which arises from the common root, distribution of potential along the channel which has been achieved as the charging density. Then, sidewall are come into the double gate junctionless MOSFET by Manish gupta et al. [26] studied the force of the sidewall spacer thickness on the swing of the subthreshold in a SDG junctionless transistor of silicon and germanium. So, the impact of the ionization can be improved with correct narrow spacer where as use of the non-optimized wide spacer is going to lower the degree of the with the influence of the fringing field of the device. Here the author analyzes the 60 mV/ drain per decade subthreshold slope of the drain which is transitioned form off state to the on state. Because of the spacing at the sidewall there are various aspects for the steep switching MOSFET take place in the nanoscale and it is going to govern the impact of the generation rate. Side wall spacer parameters are selected very carefully and that are beneficial for energy efficient steep switching.

Y.V.Bhuvaneshwari et al. [27] derived a new methodology for extracting the mobility of bulk and accumulation in the DG JL MOSFET. Here author uses the McLarty function to differentiate and extract the values of the mobility and consistent with the current flow mechanism with junctionless double gate MOSFET. Here the author investigated the doping dependence of

mobility and it is proved that the accumulation mobility will indeed exceeds the bulk mobility because of the screening effects. Here the methodology of the extraction can overcomes the degradation which is coming in the current- voltage characteristics and which is going to preserve the much needed linearity to extract the accurate mobility values which are well compare with the given results. Obtained results are useful for the compact modeling of the mobility in the junctionless devices. Author's new work extract and interpret doping dependence of the mobility values in the accumulation mode and the junctionless devices.

Work done on the biosensor DG JL MOSFET:

Firstly ajay et al. [28] proposed the dielectric modulated double gate junctionless MOSFET. Which is used as the biosensor of the label free electrical detection of the biomolecule. Here author divide the channel region into three parts in which I and III regions are same and SiO2 is used as the oxide material but in that of the II region HfO2 is used as the oxide material. Here the different channel lengths are compared to each other. It showed that sensitivity is good for the shorter channel lengths. It define the biggest change in the potential of the surface, band of the energy and the electric field for negatively charged analyets as compared to that of positively charged analytes.

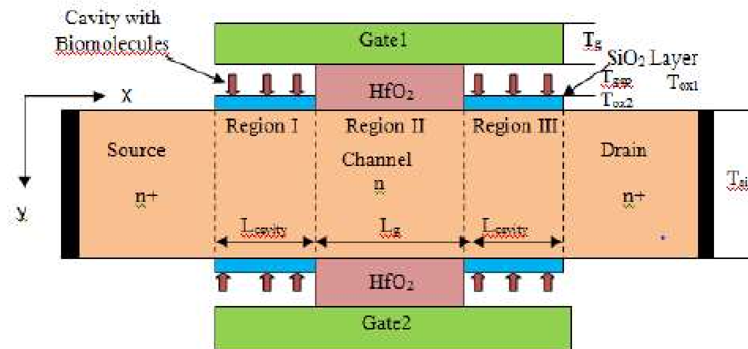

Figure 1.5 Structure of n-type double gate JL MOSFET [28]

Then the ajay et al. [29] start making new changes in the symmetric double gate junctionless MOSFET, in which author proposed the analytical model for a four-gate DM MOSFET which are used for detection of the electrical characteristics of the biomolecules. Author uses Al2O3 and SiO2 as the oxide material. Here the region of the channel of the MOSFET is left open which are normally covered with the gate electrode in the double gate junctionles MOSFET. Because of that the electrical characteristics are going to be affected with the neutral and charged analytes which are bounded in the underlap region of the channel. Here the variation in threshold voltage of the device is used as the sensing parameter for the detecting the biomolecules when the bimolecule are not in motion in the open region of the device. Author developed this device for device electrostatic parameters which are surface potential, dran current and the threshold voltage. Here the author make a conclusion that device is more sensitive to the negatively charges analytes as compare to that of the positively charged analytes. Here the Ion and Ioff ratio for the negatively

charged analytes starts decreasing as compare to that of the positively charged analytes, therefore sensitivity of the negatively charged is more sensitive to that of the other one. Therefore the sensitivity of the dielectric modulated double gate MOSFET is one of the best device for the biosensing applications due of their highest sensitivity and electrical detection.

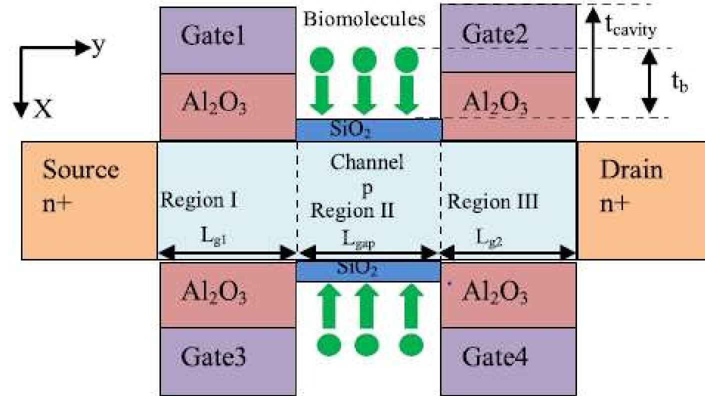

Figure 1.6 four gate JL MOSFET [29]

Then ajay et al. [30] then again an analytical model is developed which are used to detect the biomolecules, here the new device proposed with the help of ajay [29]. Here the author uses only the SiO2 as the oxide material. Here the author fabricated the device with the help of the tool of sentaurus. Here surface potential and the threshold voltage of the device, its drain current and its sensitivity factor for the n-type is more affected by the analytes of the negatively charges. Here the threshold voltage of the device reduces when the analytes are drying out.

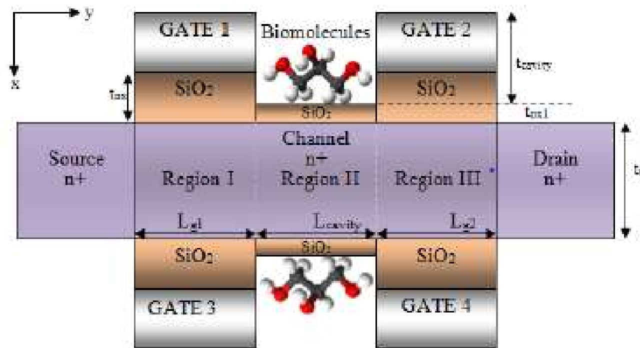

Figure 1.7 split gate JL MOSFET [30]

1.2.2 Gaps In Literature Review:

From the literature survey's point of view, it has been observed that the of the MOSFET devices has been in the industry from the past few decades. From the conventional MOSFET ruled in the industry from many decades until it become difficult to scale down the device to nanometer scale by following the Moore's law and it obtain the higher performances and the low voltage characterstics because of the prevailing SCEs and also the limitation of the scaling. To overcome the issues that are occurring due to the scaling are solved by different techniques which are

designhed to to reduce the leakage currents. New structural devices or MOSFET has been designed to have an advantages over the problems of the bulk MOSFET in the terms of the short channel effects and scalability issues. Now recently developments have been made to develop the devices which have better controllability in short channel such as the DG MOSFET, GAA MOSFET and FINFET.

Therefore, to the decreases the short channel effects, a new devices has been formed that is known as the Junctionless transistors. In the junctionless transistor device having the consistent doping concentration along with the channel region, source and the drain to reduce the issues that are faced by the conventional MOSFET with junction. But when the doping concentration in the channel is high, then the decrease in the carrier mobility take place which is going to results in the low current and transconductance of junctionless MOSFETs.

CHAPTER 2

ANALYSIS OF SPLIT GATE JUNCTIONLESS BIOSENSOR MOSFET BASED FOR DIELECTRIC CONSTANT

2.1 INTRODUCTION

Here the split gate junctionless (JL) MOSFET, which is working as the bio-transistor. This bio-transistor device is used to detect the biomolecules or biopolymer such as DNA, Protien, enzymes etc. by using the DM method. When only the dielectric constant values of the biopolymer is vary then that is known as the neutral analytes. Here the neutralization of the charged analytes is going to take place when the charges are reduced by dry off [30]. This device which is knows as Split gate JL MOSFET which has been fabricated and its electrostatic properties of the device has been simulated by the TCAD tool. Its analytical model is going to be investigated by solving the 2D poisson equations. Here the underlap region which is also known as the open cavity region which is going to be formed by etching the gate and small part of the oxide material. This open cavity region is generated for the immobilization of the bio-spieces. Here the changes in the threshold voltage of the device and transfer characteristics are used as the sensing parameters which is going to help us in detecting the biomolecule or biopolymer in its dry environment. Here by varying the thickness of the device and comparing there threshold voltage and the sensitivity that which one is better device. In this chapter two devices are formed by scaling. One is according to the change in the concentration of the device and other is by doing the scaling of the device. Here the scaling is done with respect to the thickness of silicon substrate of the device. All the devices Id/Vg curve are threshold voltage and sensitivity curves are going to be compared. Here the comparison of the different substrate doping concentration is also done and there Id/Vg curve and threshold Voltage and sensitivity waveform are compared. According to both the concentration and from the scaling method, which is better sensitive to biopolymer is going to find out.

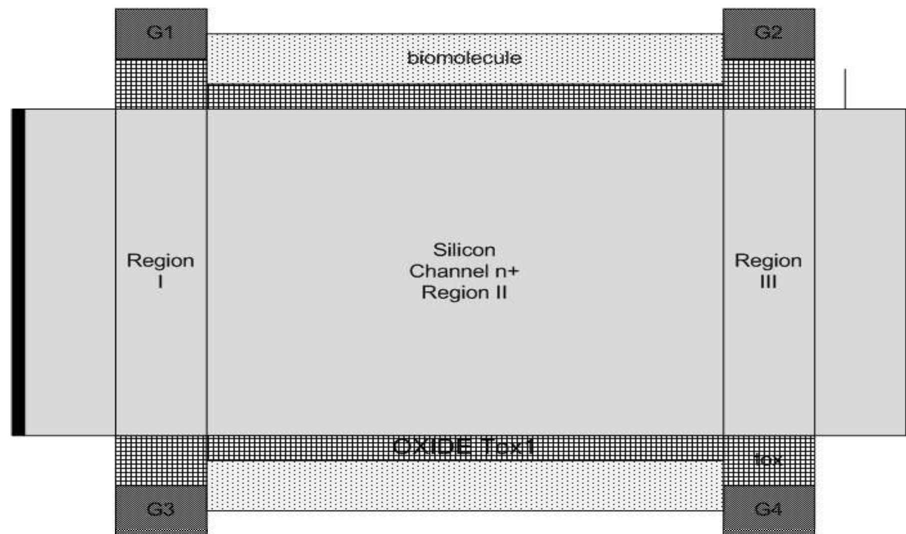

Figure 2.1 schematic structure of the n-type split gate JL MOSFET with varying thickness and varying doping concentration in the substrate

2.2 SPLIT GATE JL BIOSENSOR

Figure.2.1 is going to be modelled with the help of the TCAD tool. Here the n-type region of channelis going to be fabricated in the split gate junctionless MOSFET. Channel doping and its thickness is selected in such a way so that device should be in fully depleted in it's OFF state. Here the channel region is divided into three regions (region I, region II and region III). Dimension of the region I and III are same i.e. L_{g1} and L_{g2} are 25nm. Region I and region III are known as the gate overlap region because in both of the region's the oxide layer is covered with the gate (p.poly material). Although the region II is known as the gate underlap region (i.e. where the biomolecule communicate with the device) and sense the changes in the threshold voltage of the device according to the variation in the dielectric constant. The length of the underlap region is defined by L_c which is taken as 50nm. Thickness of the channel region (i.e. t_{si}) is 20nm and 30nm. Here the source, drain and channel region has the invariable doping (i.e. N_D=1X 10^{18} cm^{-3} and N_D=1X$10^{17}$$cm^{-3}$). Here the $t_{ox1}$and t_{ox} are defined as the width of the oxides of the underlap region and overlap region, although t_c is define as the width of the cavity region where the biomolecule is placed.

In this device, 0.05V drain voltage is applied and -1 V gate voltage is applied to the device at the G1, G2, G3 and G4. Gate voltage is varied from -2V to 1V for noticing the variation in drain current of the device. This device is going to be stimulated on the n-type DG JL MOSFET.

Here as the dielectric constant of the biomolecule changes, the threshold voltage of the devices increases linearly with the dielectric constant. Threshold voltage parameter is used for defining the sensitivity of the device.

2.3 POISSON'S EQUATION

To model the physical nature of the split gate JL MOSFET of the device at the sub-nano-meter regime, potential variation wrt different region of the device with different gate and drain bias condition must be analyzed. This device is going to act similar to that of the double gate MOSFET only the biomolecule part is different. There potential distribution concept is similar as that of the DG MOSFET. Different from that of the single gate MOSFET, in double gate MOSFET there are two gates present on both the side of the substrate (i.e. front gate and back gate) because of the presence of these two gate there potential distribution is different from that of the single gate MOSFET. Depletion approximation method is used in the poisson equation to determine the potential in the silicon film of the double gate MOSFET. In DG JL MOSFET the 2-D poisson's equation is used to determine the potential. This similar method is used in split gate DG JL MOSFET of the device. In the 2-D poisson equation partial double derivative is used for finding the potential distribution. In 2-D we are going to take x-direction in horizontal axis and y-direction in vertical direction for describing the model. It is also helpful in finding the potential along the surface of the channel. Poisson equation is going to derived from the coulomb's law and gauss law it is useful in finding the potential for the given charge distribution.

$$E = -\nabla\emptyset \tag{2.1}$$

now by doing the single derivative of the (2.1) equation it gives us the poission equation

$$\nabla . E = \nabla^2\emptyset = -\frac{\rho}{\varepsilon_{si}} \tag{2.2}$$

in 2-Dimensional $\nabla^2$is represented as

$$\nabla^2 = \left(\frac{d^2}{dx^2} + \frac{d^2}{dy^2}\right) \tag{2.3}$$

where,

$$\rho = qN_d \tag{2.4}$$

put the (2.3) and(2.4) equation in (2.2) equation 2-D poission equation [30]

$$\frac{d^2\emptyset_j(x,y)}{dx^2} + \frac{d^2\emptyset_j(x,y)}{dy^2} = -\frac{qN_d}{\varepsilon_{si}} \tag{2.5}$$

Where 'Φ' represents the potential, j represent the region I,II and III, 'x' and 'y' represents the two dimensions of the axis along which potential vary, 'ρ' is the total charge density and 'ε_{si}' is the permittivity of the silicon.

2.4 MATHEMATICAL ANALYSIS FOR THE DEVICE

2.4.1 Basic Voltage And Charge Equations

According to the basic MOS capacitor the applied gate voltage is sum of the voltages drop across the oxide and the semiconductor of the device that is

$$V_{gsj} = V_{ox} + V_{fbj} + \emptyset_s \tag{2.6}$$

Then the voltage across oxide is,

$$V_{ox} = V_{gsj} - V_{fbj} - \emptyset_s$$

$$V_{ox} = \emptyset_{gsj} - \emptyset_s \tag{2.7}$$

Where, V_{ox} is the voltage across oxide, V_{gs} is gate voltage, Φ_s is surface potential , Φ_{si} is the work function of the channel material, Φ_m is work function of the gate material, E_g is the energy band gap, T is temperature, K_B is Boltzmann concept, , $\aleph_{si}$ is the electron affinity.

Let's assume there is no change in parasitic oxide and also consider that interface trap charge density are also negligible then flat band voltage (V_{fb}) is equal to the work function difference between the gate material and the substrate body. Then the flat band voltage for the region I and III are same as compare to that of the region II is,

$$V_{fb1} = V_{fb3} = \emptyset_m - \emptyset_{si} \tag{2.8}$$

$$V_{fb2} = V_{fb1} - \frac{qN_f}{C_{eff}} \tag{2.9}$$

Where,

$$\emptyset_{si} = \aleph_{si} + \frac{E_g}{2} - \frac{K_B T}{q} \log\left(\frac{N_d}{n_i}\right) \tag{2.10}$$

then, the flat band voltage for I and III region is

$$V_{fb1} = V_{fb3} = \emptyset_m - \aleph_{si} - \frac{E_g}{2} + \frac{K_B T}{q} \log\left(\frac{N_d}{n_i}\right) \tag{2.11}$$

In JL double gate MOSFET the oxide capacitance across the gate material for region I and III is

$$C_{ox1/3} = \frac{\varepsilon_{ox}}{t_{ox\,1/3}} \tag{2.12}$$

and capacitance across the oxide in region II due to the presence of the biopolymer is,

$$C_{eff} = \frac{C_{ox\,1} C_{fr}}{C_{ox\,1} + C_{fr}} \tag{2.13}$$

Fringing capacitance occur in the overlap region of the device, so the fringing capacitance can be calculated with the help of the conformal mapping transformation method, so x and y values are,

$$\left(x - L_{g1/2}\right) + jny = M\sinh(u + jv) \tag{2.14}$$

$$\left(x - L_{g1/2}\right) + jny = M\sinh(u)\cosh(v) + jM\cosh(u)\sinh(v) \tag{2.15}$$

By equating (2.15) equation then,

$$x - L_{gi} = M\sinh(u)\cosh(v)$$

$$x = M\sinh(u)\cosh(v) + L_{gi}$$

$$L_{ch} = L_{gi} + L_{cavity}$$

then,

$$L_{gi} = L_{ch} - L_{cavity}$$

Where L_{gi} is the channel length of I and III region.

$$ny = M\cosh(u)\sinh(v) \tag{2.16}$$

where,

$$n = \frac{L_{cavity}}{(t_{ox} - t_{ox\,1})\sinh\left(\cosh^{-1}\left(\frac{(t_{ox} - t_{ox\,1}) + t_g}{(t_{ox} - t_{ox\,1})}\right)\right)} \tag{2.17}$$

and

$$M = \frac{L_{cavity}}{\sinh\left(\cosh^{-1}\left(\frac{(t_{ox} - t_{ox\,1}) + t_g}{(t_{ox} - t_{ox\,1})}\right)\right)} \tag{2.18}$$

put the (2.17) and (2.18) equation in (2.16) then y is

$$\frac{yM}{(t_{ox} - t_{ox1})} = M\cosh(u)\sinh(v)$$

then,

$$y = (t_{ox} - t_{ox1})M\cosh(u)\sinh(v)$$

Then the fringing capacitance can be calculated with the help of the given expression

$$C_f = \varepsilon_{cav}\frac{u_{B'D'} - u_{A'C'}}{v_{C'D'} - v_{A'B'}} \tag{2.19}$$

In x-y coordinate system there are points that is ABCD which are transformed into the A'B'C'D' in u-v coordinate system. In x-y coordinate system the dimensions of the ABCD is with respect to the dimension of the device A(t_{ox1},L_{gi}), B(t_{ox1}, L_{gi}+L_{cav}), C(t_{ox}- t_{ox1},L_{gi}) and D(t_{ox}- t_{ox1}+t_g, L_{gi}). But u-v coordinate system is with respect to the angle so A'(t_{ox1},L_{gi}), B'(t_{ox1}, M), C'(mπ/2,0) and D'(mπ/2,M). now by substituting these values into the (2.19) equation, then fringing gate capacitance is

$$C_f = \varepsilon_{cav} \frac{2}{m\pi M} \quad (2.20)$$

2.4.2 Boundary Conditions

Firstly the boundary condition [30] are given as:

1) Potential distribution at the y=0 and y=t_{si} is same because of the same gate voltage is applied at all the split gates of the MOSFET.

$$\emptyset(x,0) = \emptyset(x,t_{si}) = \emptyset_f(x) \quad (2.21)$$

$$\emptyset(x,0) = \emptyset_{sj}(x) + C_i(x)y + C_j(x)y^2 \quad (2.22)$$

By putting y=0 in equation (2.7) then we gate surface potential

$$\emptyset_f(x) = \emptyset_{sj}(x) \quad (2.23)$$

2)

$$\left.\frac{d\emptyset(x,y)}{dy}\right]_{y=0} = \frac{\varepsilon_{ox}}{\varepsilon_{si}} \frac{\emptyset_f(x)-\emptyset_{gs}}{t_{ox}} \quad (2.24)$$

$$\left.\frac{d\emptyset(x,y)}{dy}\right]_{y=0} = \frac{d}{dy}(\emptyset_s(x) + C_1(x)y + C_2(x)y^2)$$

$$= C_1(x) + 2C_2(x)y$$

$$= C_1(x)$$

So,

$$\left.\frac{d\emptyset(x,y)}{dy}\right]_{y=0} = \frac{\varepsilon_{ox}}{\varepsilon_{si}} \frac{\emptyset_f(x)-\emptyset_{gs}}{t_{ox}} = C_1(x) \quad (2.25)$$

From equation (2.10) it is clear that the device is symmetric, so it is wise to use Neumann boundary condition at this point. This will in reducing the complexity of the computation.

3)

$$\left.\frac{d\emptyset(x,y)}{dy}\right]_{y=t_{si}} = -\frac{\varepsilon_{ox}}{\varepsilon_{si}} \frac{\emptyset_f(x)-\emptyset_{gs}}{t_{ox}} \quad (2.26)$$

By comparing (2.11) equation with the (2.10) equation then

$$\left.\frac{d\phi(x,y)}{dy}\right]_{y=t_{si}} = -\frac{\varepsilon_{ox}}{\varepsilon_{si}}\frac{\phi_f(x)-\phi_{gs}}{t_{ox}} = -C_1 \quad (2.27)$$

$$\left.\frac{d\phi(x,y)}{dy}\right]_{y=t_{si}} = \frac{d}{dy}(\phi_s(x) + C_1(x)y + C_2(x)y^2) \quad (2.28)$$

$$= C_1(x) + 2C_2(x)y$$

$$= C_1(x) + 2C_2(x)t_{si} \quad (2.29)$$

Now equating the (2.14) equation to the (2.12) equation then $C_2(x)$ is

$$C_2(x) = \frac{-C_1(x)}{t_{si}} \quad (2.30)$$

2.4.3 Calculation of The Surface Potential

To create a model of the n-type split gate junctionless MOSFET, poisson's equation is going to solve separately for all the regions of the device. So the poisson's equation for the potential distribution in each of the region is going to be expressed as [31]:

$$\frac{\partial^2\phi_j(x,y)}{\partial x^2} + \frac{\partial^2\phi_j(x,y)}{\partial y^2} = -\frac{qN_d}{\varepsilon_{si}} \quad (2.31)$$

Where ε_{si} is dielectric permittivity of the silicon, q is the electron charges in the substrate and N_d is the channel doping concentration in n-type substrate. Where $\Phi_j(x,y)$ is the potential in the channel region j which is changing with respect to the x and y dimension of the device.

With the help of the parabolic approximation method equation (2.31) can be written as:

$$\phi_j(x,y) = \phi_{sj}(x) + C_j(x)y + C_j(x)y^2 \quad (2.32)$$

where, j is representing the region I, II and III. Region I and III are symmetric around region II.

By using the boundary conditions in equation (2.32) then the potential is

$$\phi(x,y) = \phi_f(x) + \left[\frac{\varepsilon_{ox}}{\varepsilon_{si}}\frac{\phi_f(x)-V_{gs}+V_{fb}}{t_{ox}}\right]y + \left[-\frac{\varepsilon_{ox}}{\varepsilon_{si}t_{si}}\frac{\phi_f(x)-V_{gs}+V_{fb}}{t_{ox}}\right]y^2 \quad (2.33)$$

by taking the double derivative of the (2.33) equation w.r.t x and y and by adding then

$$\frac{d^2\phi(x,y)}{dx^2} + \frac{d^2\phi(x,y)}{dy^2} = \frac{d^2\phi_f(x)}{dx^2} + \frac{\varepsilon_{ox}}{\varepsilon_{si}t_{ox}}\frac{d^2\phi_f(x)}{dx^2}y - \frac{\varepsilon_{ox}}{\varepsilon_{si}t_{si}t_{ox}}\frac{d^2\phi_f(x)}{dx^2}y^2 - \frac{2\varepsilon_{ox}}{\varepsilon_{si}t_{si}}\frac{\phi_f(x)-V_{gs}+V_{fb}}{t_{ox}} \quad (2.34)$$

$$-\frac{qN_d}{\varepsilon_{si}} = \frac{d^2\phi_f(x)}{dx^2}\left[1 + \frac{\varepsilon_{ox}}{\varepsilon_{si}t_{ox}}y - \frac{\varepsilon_{ox}}{\varepsilon_{si}t_{si}t_{ox}}y^2\right] - \frac{2\varepsilon_{ox}}{\varepsilon_{si}t_{si}}\frac{\phi_f(x)-V_{gs}+V_{fb}}{t_{ox}} \quad (2.35)$$

consider the surface potential at $y=t_{si}/2$

$$-\frac{qN_d}{\varepsilon_{si}} = \frac{d^2\phi_f(x)}{dx^2}\left[1 + \frac{\varepsilon_{ox}}{\varepsilon_{si}t_{ox}}\frac{t_{si}}{2} - \frac{\varepsilon_{ox}}{\varepsilon_{si}t_{si}t_{ox}}\frac{t_{si}^2}{4}\right] - \frac{2\varepsilon_{ox}}{\varepsilon_{si}t_{si}}\frac{\phi_f(x) - V_{gs} + V_{fb}}{t_{ox}}$$

Equating the above equation change in electric field is

$$\frac{d^2\phi_f(x)}{dx^2} = \left[\frac{2\varepsilon_{ox}}{\varepsilon_{si} t_{si}} \frac{\phi_f(x) - V_{gs} + V_{fb}}{t_{ox}} - \frac{qN_d}{\varepsilon_{si}}\right]\left[\frac{2\varepsilon_{si} t_{ox}}{2\varepsilon_{si} t_{ox} + \varepsilon_{ox} t_{si}}\right]$$

$$\frac{d^2\phi_f(x)}{dx^2} - \frac{2\varepsilon_{ox}}{\varepsilon_{si} t_{ox} t_{si}} K_s \phi_f(x) = K_s \left[\frac{-qN_d}{\varepsilon_{si}} - \frac{2\varepsilon_{ox}}{\varepsilon_{si}} \frac{(V_{gs} - V_{fb})}{t_{ox} t_{si}}\right] \tag{2.36}$$

where,

$$K_s = \frac{2\varepsilon_{si} t_{ox}}{2\varepsilon_{si} t_{ox} + \varepsilon_{ox} t_{si}}$$

$$\frac{d^2\phi_f(y)}{dy^2} - \alpha_i \phi_s(y) = \beta_i \tag{2.37}$$

Compare the equation (2.36) with the (2.37) then α_i and β_i for region I and III are

$$\alpha_i = \alpha_1 = \alpha_3 = \frac{2\varepsilon_{ox}}{\varepsilon_{si} \varepsilon_{ox} t_{si}} K_s$$

$$\beta_i = \beta_1 = \beta_3 = K_s \left[\frac{-qN_d}{\varepsilon_{si}} - \frac{2\varepsilon_{ox}}{\varepsilon_{si}} \frac{\left(V_{gs} - V_{fb\frac{1}{3}}\right)}{t_{ox} t_{si}}\right]$$

$$\omega_i = \omega_1 = \omega_3 = \sqrt{\alpha_i}$$

$$\sigma_i = \sigma_1 = \sigma_3 = -\frac{\beta_i}{\alpha_i}$$

by doing the partial differential equation of (2.37) then surface potential variation w.r.t x axis is

$$\phi_s(x) = \phi_f(x) = A_{1/3} e^{-\omega_{1/3} x_{1/3}} + B_{1/3} e^{\omega_{1/3} x_{1/3}} + \sigma_{1/3}$$

For region I:

At y=0 and x=0 position surface potential variation w.r.t x is

$$\phi_s(0) = A_1 e^0 + B_1 e^0 + \sigma_1 \tag{2.38}$$

$$V_{bi} = A_1 + B_1 + \sigma_1$$

$$A_1 = V_{bi} - B_1 - \sigma_1 \tag{2.39}$$

$$\phi_0 = A_1 e^{\omega_1 L_{g1}} + B_1 e^{\omega_1 L_{g1}} + \omega_1 \tag{2.40}$$

By using the (2.39) equation in (2.40) equation then B_1 is

$$B_1 = \frac{(V_{bi} - \sigma_1)e^{\omega_1 L_{g1}} - (\emptyset_0 - \sigma_1)}{2\sinh(\omega_1 L_{g1})}$$

similarly, for region III at y=0 and x=$L_{g1} + L_{cavity}$ the value of A_3 and B_3 is

$$A_3 = \emptyset_1 - \sigma_3 - B_3$$

$$B_3 = \frac{(\emptyset_1 - \sigma_3)e^{\omega_3 L_{g2}} - (V_{ds} + V_{bi} - \sigma_3)}{2\sinh(\omega_3 L_{g2})}$$

For region II:

$$\emptyset_2(x,y) = \emptyset_s(x) + C_{12}(x)y + C_{22}y^2 \quad (2.41)$$

By taking the double derivative of the above equation w.r.t x and y and using the boundary equation in it the variation in electric field is

$$-\frac{qN_d}{\varepsilon_{si}} = \frac{d^2\emptyset_f(x)}{dx^2} + \frac{C_{eff}}{\varepsilon_{si}}\frac{d^2\emptyset_f(x)}{dx^2}y - \frac{C_{eff}}{t_{si}\varepsilon_{si}}\frac{d^2\emptyset_f(x)}{dx^2}y^2\, 2\left[-\frac{C_{eff}}{t_{si}\varepsilon_{si}}(\emptyset_s(x) - V_{gs} + V_{fb2})\right] \quad (2.42)$$

then the variation at y= $t_{si}/2$ is

$$-\frac{qN_d}{\varepsilon_{si}} = \frac{d^2\emptyset_f(x)}{dx^2} + \frac{C_{eff}}{\varepsilon_{si}}\frac{d^2\emptyset_f(x)}{dx^2}\frac{t_{si}}{2} - \frac{C_{eff}}{t_{si}\varepsilon_{si}}\frac{d^2\emptyset_f(x)}{dx^2}\left(\frac{t_{si}}{2}\right)^2 + 2\left[-\frac{C_{eff}}{t_{si}\varepsilon_{si}}(\emptyset_f(x) - V_{gs} + V_{fb2})\right] \quad (2.43)$$

$$\frac{d^2\emptyset_f(x)}{dx^2} = \left(2\left[\frac{C_{eff}}{t_{si}\varepsilon_{si}}(\emptyset_f(x) - V_{gs} + V_{fb2})\right] - \frac{qN_d}{\varepsilon_{si}}\right) X \left(\frac{\varepsilon_{si}}{\varepsilon_{si} + 2t_{si}C_{eff}}\right)$$

$$\frac{d^2\emptyset_f(x)}{dx^2} - 2\frac{C_{eff}K_s}{t_{si}\varepsilon_{si}}\emptyset_f(x) = K_s\left[-2\frac{C_{eff}(V_{gs} - V_{fb2})}{t_{si}\varepsilon_{si}} - \frac{qN_d}{\varepsilon_{si}}\right] \quad (2.44)$$

$$\frac{d^2\emptyset_f(x)}{dx^2} - D_0\emptyset_f(x) = D_1 \quad (2.45)$$

Compare the equation (2.44) and (2.45) then

$$D_0 = 2\frac{C_{eff}K_s}{t_{si}\varepsilon_{si}}$$

$$D_1 = K_s\left[-2\frac{C_{eff}(V_{gs} - V_{fb2})}{t_{si}\varepsilon_{si}} - \frac{qN_d}{\varepsilon_{si}}\right]$$

$$\sigma_2 = -\frac{D_1}{D_0}$$

$$\mu = \sqrt{D_0}$$

now by doing the partial differention of the (2.45) equation then

$$\emptyset_s(L_{g1}) = A_2e^0 + B_2e^0 + \sigma_2$$

$$\emptyset_0 = A_2 + B_2 + \sigma_2$$

$$A_2 = \emptyset_0 - \sigma_2 - B_2 \quad (2.46)$$

Put the (2.46) equation in equation then

$$\emptyset_1 = (\emptyset_0 - \sigma_2 - B_2)e^{(\frac{\mu}{M}L_{cavity})} + B_2e^{(\frac{-\mu}{M}L_{cavity})} + \sigma_2$$

$$B_2 = \frac{(\emptyset_0 - \sigma_2)e^{\left(\frac{\mu}{M}L_{cavity}\right)} - (\emptyset_1 - \sigma_2)}{2\sinh\left(\frac{\mu}{M}L_{cavity}\right)}$$

Drain current for linear region in I, II and III region is

$$I_{d1} = \frac{\mu C_{ox}W}{L_{g1}}\left((V_g - V_{th})V_{p1} - \frac{{V_{p1}}^2}{2}\right) \quad (2.47)$$

$$I_{d2} = \frac{\mu C_{eff}W}{L_{cav}}\left((V_g - V_{th})(V_{p2} - V_{p1}) - \frac{(V_{p2} - V_{p1})^2}{2}\right) \quad (2.48)$$

$$I_{d3} = \frac{\mu C_{ox}W}{L_{g2}}\left((V_g - V_{th})(V_{ds} - V_{p2}) - \frac{(V_{ds} - V_{p2})^2}{2}\right) \quad (2.49)$$

By equating I_{d1} and I_{d2}

$$I_{d1} = I_{d2}$$

$$\frac{\mu C_{ox}W}{L_{g1}}\left((V_g - V_{th})V_{p1} - \frac{{V_{p1}}^2}{2}\right) = \frac{\mu C_{ox}W}{L_{g1}}\left((V_g - V_{th})(V_{p2} - V_{p1}) - \frac{(V_{p2} - V_{p1})^2}{2}\right)$$

$$-\frac{1}{2}\left(\frac{C_{ox}}{L_{g1}} + \frac{C_{eff}}{L_{cav}}\right){V_{p1}}^2 + \left(\frac{C_{ox}}{L_{g1}}(V_g - V_{th}) + \frac{C_{eff}}{L_{cav}}(V_g - V_{th})\right)V_{p1} - \frac{C_{eff}}{L_{cav}}\left((V_g - V_{th})V_{p2} - \frac{{V_{p2}}^2}{2}\right) = 0 \quad (2.50)$$

then by comparing the (2.50) equation with the

$${V_{p1}}^2R_1 + V_{p1}R_2 + R_3 = 0 \quad (2.51)$$

then,

$$R_1 = -\frac{1}{2}\left(\frac{C_{ox}}{L_{g1}} + \frac{C_{eff}}{L_{cav}}\right)$$

$$R_2 = \left(\frac{C_{ox}}{L_{g1}}(V_g - V_{th}) + \frac{C_{eff}}{L_{cav}}(V_g - V_{th})\right)$$

and

$$R_3 = -\frac{C_{eff}}{L_{cav}}\left((V_g - V_{th})V_{p2} - \frac{{V_{p2}}^2}{2}\right)$$

similary, by equating $I_{d3}$and I_{d2}

$$I_{d3} = I_{d2}$$

$$\frac{\mu C_{ox} W}{L_{g2}}\left((V_g - V_{th})(V_{ds} - V_{p2}) - \frac{(V_{ds} - V_{p2})^2}{2}\right) = \frac{\mu C_{ox} W}{L_{g1}}\left((V_g - V_{th})(V_{p2} - V_{p1}) - \frac{(V_{p2} - V_{p1})^2}{2}\right)$$

$$\frac{1}{2}\left(\frac{C_{ox}}{L_{g2}} + \frac{C_{eff}}{L_{cav}}\right){V_{p2}}^2 - \left(\frac{C_{ox}}{L_{g2}}(V_g - V_{th}) + \frac{C_{eff}}{L_{cav}}(V_g - V_{th})\right)V_{p2} + \frac{C_{ox}}{L_{g2}}(V_g V_d - V_{th} V_d) - \frac{C_{ox}}{L_{g2}}\frac{{V_d}^2}{2} + \frac{C_{eff}}{L_{cav}}(V_g - V_{th})V_{p1} - \frac{C_{eff}}{L_{cav}}\frac{{V_{p2}}^2}{2}$$

(2.52)

By comparing (2.51) equation with

$$ {V_{p2}}^2 H_1 + V_{p2} H_2 + H_3 = 0 \quad (2.53)$$

then,

$$H_1 = \frac{1}{2}\left(\frac{C_{ox}}{L_{g2}} + \frac{C_{eff}}{L_{cav}}\right)$$

$$H_2 = \frac{C_{ox}}{L_{g2}}(V_g - V_{th}) + \frac{C_{eff}}{L_{cav}}(V_g - V_{th})$$

and

$$H_3 = \frac{C_{ox}}{L_{g2}}(V_g V_d - V_{th} V_d) - \frac{C_{ox}}{L_{g2}}\frac{{V_d}^2}{2} + \frac{C_{eff}}{L_{cav}}(V_g - V_{th})V_{p1} - \frac{C_{eff}}{L_{cav}}\frac{{V_{p2}}^2}{2}$$

CHAPTER 3

SPLIT GATE JL MOSFET WITH UTB FOR SENSING THE DOPING CONCENTRATION

3.1 INTRODUCTION

By modifying the device, defined in previous chapter, as we know, the device is used for sensing the different biopolymer by using the dielectric constant in neutral analytes. In Pervious device when dielectric constant is changed it shows some variation in threshold voltage. Further, we introduce the doping concentration in the biopolymer, however, it doesn't show variations in the threshold voltage of the device. So we proposed a new device for sensing the different doping concentration in the device by showing the variation in the threshold voltage. Example, when the boron present in the water, Boron-containing compounds are present in the environment which is known as borates. Borates gets dissolve in the water which get adsorb and desorb from the distict surfaces which are found in the rivers and the streams. Depending on the water's pH and on the concentration of the borate in water which is going to help in finding the amount of the adsorption of the borates. Borates which get dissolved in the water are one of the most stable, and does not react with oxygen or with the other chemicals which are present inside the water, or which undergo's from the changes from one type of borate to other. So to find the changes that are taking place in the water due to the boron presence is find with the help of this device. This new modeled device is used to help in finding the amount of boron concentration present in the water.

3.2 ARCHITECTURE

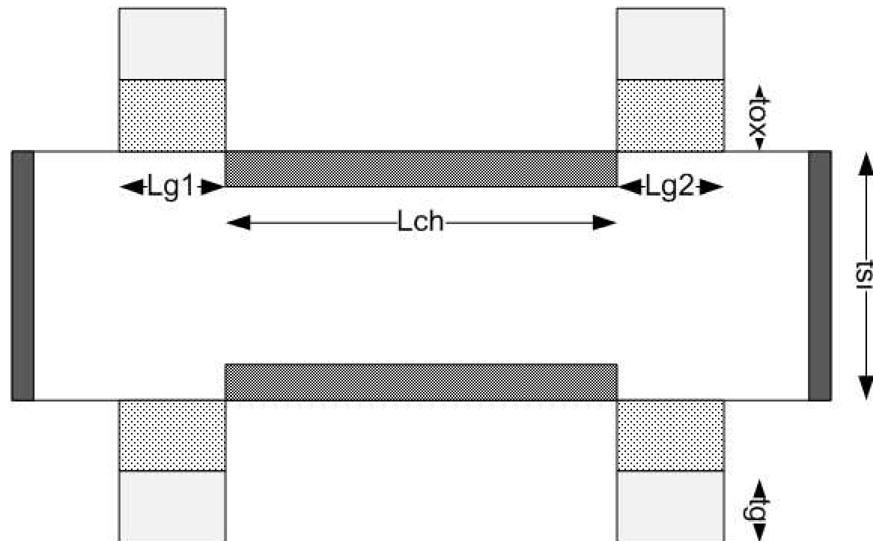

Figure 3.1 Schematic structure of n-type split gate JL MOSFET with analytes bind in the underlap region of junction in the channel region of the device. Doping in source , drain and channel is uniform i.e. $1X10^{18}$ m^{-3}.

Figure.3.1 shows a schematic diagram of a four gate junctionless MOSFET which is used as biosensor which is going to sense the impurity atoms in the biomolecule. This structure is similar to that of the DG MOSFET, only difference is that there is an underlap region which is modeled by etching the gate material, SiO2 and the substrate part is etched from the channel, from both the front end and back side of the DG MOSFET.

Now, biopolymer's are implant inside the channel region which are uncovered from there upper side. The biopolymer which are introduced in the cavity region are immobilized. In biopolymer region of the device, n-type or p-type impurity are introduced. This doping concentration is vary between the the $1X10^{16}$ to $9X10^{17}$. Now this developed model is validate when the simulation results obtained from the SILVACO device. Electrical properties of the Semiconductor device are characterized through the software that is through SILVACO tool.

In the neutral analyte, doping concentration of boron is introduced from $N_a = 1X10^{16}$ to $9X10^{17}$ where N_a is the acceptor concentration of the material. Now to simulate the effect of charge of the biomolecule negative or positive charge are introduce on the interface i.e. from $-5X10^{11}$ to $5X10^{11}$ cm^{-3} .Various model parameter has been performed in simulation are as follow: Shockley-read-hall recombination model, Fermi-dirac model, concentration dependent mobility, field dependent mobility.

From the above model device we can find the potential variation and the electric field variation due to variation of doping concentration in biopolymer which has constant dielectric constant and also due to the gate because of that the three regions are taking place in which I and III regions are going to act the same as compare to that of the II region.

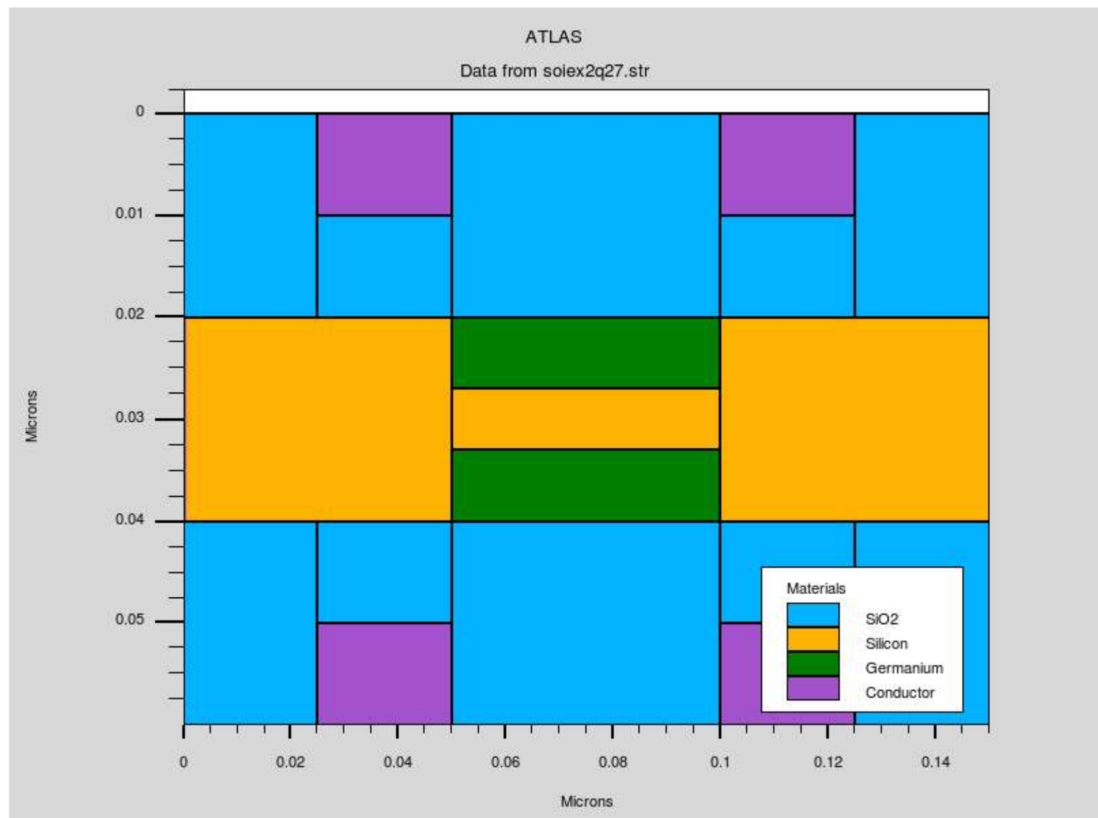

Figure 3.2 Schematic structure of n-type split gate JL MOSFET modeled on SILVACO TOOL with channel concentration is equal to $5X10^{16}$ cm^{-3}

Figure.3.2 is going to be modelled with the help of the TCAD tool. n-type channel region is introduced, in four gate junctionless MOSFET. Thickness of the channel region and doping concentration of the device is selected in such a way so that it should be in fully depleted in it's OFF state. Channel region is divided into three regions, I and III are of same dimensions, where, as region II is of different dimension. So, channel length of the region I and III are L_{g1} and L_{g2} of 25nm. Region I and region III are known as the gate overlap region because in both of the region's the oxide layer is covered with the gate (p.poly material). Although the region II is known as the gate underlap region. Channel length of the underlap region is represented as L_{cv} which is taken as 50nm. Thickness of the channel region (i.e. t_{si}) is 20nm. $t_{ox1}$and t_{ox} are defined as the width of the oxides of the underlap region, although t_c is define as the width of the cavity region where the biopolymer is implanted. Doping concentration of the channel region is uniform throughout the source, drain and channel region that is N_D=1X 10^{18} cm^{-3}.

In this device, 0.05V drain voltage is applied and -1 V gate voltage is applied to the device at the G1, G2, G3 and G4. Gate voltage is varied from -2V to 1V. As the gate voltage is varied, there should be change in the drain current (Id) is noticed. This device is going to be stimulated on the n-type DG JL MOSFET. Here in this device we can sense the change in the doping concentration

of the device is noticed with the help of the variation in the threshold voltage values. If the change in the threshold voltage is maximum w.r.t change in the doping concentration of the biopolymer.

3.3 BASIC VOLTAGE AND CHARGE EQUATIONS

According to the basic MOS capacitor the applied gate voltage is sum of the voltages drop across the oxide and the semiconductor of the device that is

$$V_{gsk} = V_o + V_f + \emptyset_{su} \tag{3.1}$$

Then the voltage across oxide is,

$$V_o = V_{gsk} - V_f - \emptyset_{su}$$

$$V_o = \emptyset_{gsk} - \emptyset_{su} \tag{3.2}$$

Let's assume there is no change in parasitic oxide and also consider that interface trap charge density are also negligible then flat band voltage (V_f) is equal to the work function difference between the gate material and the substrate body. Then the flat band voltage for the region I and III are same as compare to that of the region II is,

$$V_{fp\,1} = V_{fp\,3} = \emptyset_m - \emptyset_{si} \tag{3.3}$$

$$V_{fp\,2} = V_{fp\,1} - \frac{q N_f}{C_{eff}} \tag{3.4}$$

Where,

$$\emptyset_{si} = \aleph_{si} + \frac{E_g}{2} - \frac{K_B T}{q} \log\left(\frac{N_d}{n_i}\right) \tag{3.5}$$

then, the flat band voltage for I and III region is

$$V_{fp\,1} = V_{fp\,3} = \emptyset_m - \aleph_{si} - \frac{E_g}{2} + \frac{K_B T}{q} \log\left(\frac{N_d}{n_i}\right) \tag{3.6}$$

Where, V_o is the voltage across oxide, V_{gsk} is gate voltage, Φ_{gsk} is surface potential , Φ_{si} is the work function of the channel material, Φ_m is work function of the gate material, E_g is the energy band gap, T is temperature, K_B is Boltzmann concept, , $\aleph_{si}$ is the electron affinity.

In JL double gate MOSFET the oxide capacitance across the gate material for region I and III is

$$C_{oxk} = \frac{\varepsilon_{ox}}{t_{oxk}} \tag{3.7}$$

and capacitance across the oxide in region II due to the presence of the biopolymer is,

$$C_{eff} = \frac{C_{ox\,1} C_f}{C_{ox\,1} + C_f} \tag{3.8}$$

Fringing capacitance occur in the overlap region of the device, so the fringing capacitance can be calculated with the help of the conformal mapping transformation method [32], so x and y values are,

$$\left(x - L_{gap}\right) + jny = N\sinh(u + jv) \tag{3.9}$$

$$\left(x - L_{gap}\right) + jny = N\sinh(u)\cosh(v) + jN\cosh(u)\sinh(v) \tag{3.10}$$

By equating (3.10) equation then,

$$x - L_{gap} = N\sinh(u)\cosh(v)$$

$$x = N\sinh(u)\cosh(v) + L_{gp}$$

$$L_{channel} = L_{gap} + L_{cavity}$$

then,

$$L_{gap} = L_{channel} - L_{cavity}$$

Where L_{gp} is the channel length of I and III region.

$$ny = N\cosh(u)\sinh(v) \tag{3.11}$$

where,

$$n = \frac{L_{cavity}}{(t_{ox} - t_{ox\,1})\sinh\left(\cosh^{-1}\left(\frac{(t_{ox} - t_{ox\,1}) + t_g}{(t_{ox} - t_{ox\,1})}\right)\right)} \tag{3.12}$$

and

$$N = \frac{L_{cavity}}{\sinh\left(\cosh^{-1}\left(\frac{(t_{ox} - t_{ox\,1}) + t_g}{(t_{ox} - t_{ox\,1})}\right)\right)} \tag{3.13}$$

put the (27) and (28) equation in (26) then y is

$$\frac{yN}{(t_{ox} - t_{ox1})} = N\cosh(u)\sinh(v)$$

then,

$$y = (t_{ox} - t_{ox1})N\cosh(u)\sinh(v)$$

Then the fringing capacitance can be calculated with the help of the given expression

$$C_f = \varepsilon_{cavity}\,\frac{u_{B'D'} - u_{A'C'}}{v_{C'D'} - v_{A'B'}} \tag{3.14}$$

In x-y coordinate system there are points that is ABCD which are transformed into the A'B'C'D' in u-v coordinate system. In x-y coordinate system the dimensions of the ABCD is with respect to the dimension of the device A(t_{ox1},L_{gi}), B(t_{ox1}, L_{gi}+L_{cav}), C(t_{ox}- t_{ox1},L_{gi}) and D(t_{ox}- t_{ox1}+t_g, L_{gi}). But u-v coordinate system is with respect to the angle so A'(t_{ox1},L_{gi}), B'(t_{ox1}, M), C'(mπ/2,0) and D'(mπ/2,M). now by substituting these values into the (3.14) equation, then fringing gate capacitance is

$$C_f = \varepsilon_{cav} \frac{2}{m\pi N} \tag{3.15}$$

3.4 BOUNDARY CONDITIONS

1) Potential distribution at the y=0 and y=t_{si} is same because of the same gate voltage is applied at all the split gates of the MOSFET.

$$\emptyset(x,0) = \emptyset(x,t_{si}) = \emptyset_f(x) \tag{3.16}$$

$$\emptyset(x,0) = \emptyset_{sj}(x) + C_i(x)y + C_i(x)y^2 \tag{3.17}$$

By putting y=0 in equation (3.17) then we gate surface potential

$$\emptyset_f(x) = \emptyset_{sj}(x) \tag{3.18}$$

2)

$$\left.\frac{d\emptyset(x,y)}{dy}\right]_{y=0} = \frac{\varepsilon_{ox}}{\varepsilon_{si}} \frac{\emptyset_f(x) - \emptyset_{gs}}{t_{ox}} \tag{3.19}$$

$$\left.\frac{d\emptyset(x,y)}{dy}\right]_{y=0} = \frac{d}{dy}(\emptyset_s(x) + C_1(x)y + C_2(x)y^2)$$

So,

$$\left.\frac{d\emptyset(x,y)}{dy}\right]_{y=0} = \frac{\varepsilon_{ox}}{\varepsilon_{si}} \frac{\emptyset_f(x) - \emptyset_{gs}}{t_{ox}} = C_1(x) \tag{3.20}$$

From equation (3.16) it is clear that the device is symmetric, so it is wise to use Neumann boundary condition at this point. This will in reducing the complexity of the computation.

3)

$$\left.\frac{d\emptyset(x,y)}{dy}\right]_{y=t_{si}} = -\frac{\varepsilon_{ox}}{\varepsilon_{si}} \frac{\emptyset_f(x) - \emptyset_{gs}}{t_{ox}} \tag{3.21}$$

By comparing (3.17) equation with the (3.16) equation then

$$\left.\frac{d\emptyset(x,y)}{dy}\right]_{y=t_{si}} = -\frac{\varepsilon_{ox}}{\varepsilon_{si}} \frac{\emptyset_f(x) - \emptyset_{gs}}{t_{ox}} = -C_1 \tag{3.22}$$

$$\left.\frac{d\emptyset(x,y)}{dy}\right]_{y=t_{si}} = \frac{d}{dy}(\emptyset_s(x) + C_1(x)y + C_2(x)y^2) \tag{3.23}$$

$$= C_1(x) + 2C_2(x)y$$

$$= C_1(x) + 2C_2(x)t_{si} \tag{3.24}$$

Now equating the (3.24) equation to the (3.22) equation then $C_2(x)$ is

$$C_2(x) = \frac{-C_1(x)}{t_{si}} \tag{3.25}$$

3.5 CALCULATION OF THE SURFACE POTENTIAL

To create a model of the n-type split gate junctionless MOSFET, poisson's equation is going to solve separately for all the regions of the device. So the poisson's equation of the potential distribution in each of the region is going to be expressed as [31]:

$$\frac{\partial^2 \emptyset_j(x,y)}{\partial x^2} + \frac{\partial^2 \emptyset_j(x,y)}{\partial y^2} = -\frac{qN_d}{\varepsilon_{si}} \tag{3.26}$$

Where ε_{si} is dielectric permittivity of the silicon, q is the electron charges in the substrate and N_d is the channel doping concentration in n-type substrate. Where $\Phi_j(x,y)$ is the potential in the channel region j which is changing with respect to the x and y dimension of the device.

With the help of the parabolic approximation method equation (3.26) can be written as:

$$\emptyset_k(x,y) = \emptyset_{sk}(x) + C_k(x)y + C_k(x)y^2 \tag{3.27}$$

where, k is representing the region I, II and III. Region I and III are symmetric around region II.

By using the boundary conditions in equation (3.27) then the potential is

$$\emptyset(x,y) = \emptyset_f(x) + \left[\frac{\varepsilon_{ox}}{\varepsilon_{si}} \frac{\emptyset_f(x)-V_{gs}+V_{fp}}{t_{ox}}\right] y + \left[-\frac{\varepsilon_{ox}}{\varepsilon_{si}\, t_{si}} \frac{\emptyset_f(x)-V_{gs}+V_{fp}}{t_{ox}}\right] y^2 \tag{3.28}$$

by taking the double derivative of the (3.28) equation w.r.t x and y and by adding then

$$\frac{d^2\emptyset(x,y)}{dx^2} + \frac{d^2\emptyset(x,y)}{dy^2} = \frac{d^2\emptyset_f(x)}{dx^2} + \frac{\varepsilon_{ox}}{\varepsilon_{si}\, t_{ox}} \frac{d^2\emptyset_f(x)}{dx^2} y - \frac{\varepsilon_{ox}}{\varepsilon_{si}\, t_{si}\, t_{ox}} \frac{d^2\emptyset_f(x)}{dx^2} y^2 - \frac{2\varepsilon_{ox}}{\varepsilon_{si}\, t_{si}} \frac{\emptyset_f(x)-V_{gs}+V_{fp}}{t_{ox}} \tag{3.29}$$

$$-\frac{qN_d}{\varepsilon_{si}} = \frac{d^2\emptyset_f(x)}{dx^2}\left[1 + \frac{\varepsilon_{ox}}{\varepsilon_{si}\, t_{ox}} y - \frac{\varepsilon_{ox}}{\varepsilon_{si}\, t_{si}\, t_{ox}} y^2\right] - \frac{2\varepsilon_{ox}}{\varepsilon_{si}\, t_{si}} \frac{\emptyset_f(x)-V_{gs}+V_{fp}}{t_{ox}} \tag{3.30}$$

consider the surface potential at $y = t_{si}/2$

$$-\frac{qN_d}{\varepsilon_{si}} = \frac{d^2\emptyset_f(x)}{dx^2}\left[1 + \frac{\varepsilon_{ox}}{\varepsilon_{si}\, t_{ox}} \frac{t_{si}}{2} - \frac{\varepsilon_{ox}}{\varepsilon_{si}\, t_{si}\, t_{ox}} \frac{{t_{si}}^2}{4}\right] - \frac{2\varepsilon_{ox}}{\varepsilon_{si}\, t_{si}} \frac{\emptyset_f(x) - V_{gs} + V_{fp}}{t_{ox}}$$

Equating the above equation change in electric field is

$$\frac{d^2\emptyset_f(x)}{dx^2} = \left[\frac{2\varepsilon_{ox}}{\varepsilon_{si}\, t_{si}} \frac{\emptyset_f(x) - V_{gs} + V_{fp}}{t_{ox}} - \frac{qN_d}{\varepsilon_{si}}\right]\left[\frac{2\varepsilon_{si}\, t_{ox}}{2\varepsilon_{si}\, t_{ox} + \varepsilon_{ox}\, t_{si}}\right]$$

$$\frac{d^2\emptyset_f(x)}{dx^2} - \frac{2\varepsilon_{ox}}{\varepsilon_{si}\,t_{ox}\,t_{si}} K_s \emptyset_f(x) = K_s\left[\frac{-qN_d}{\varepsilon_{si}} - \frac{2\varepsilon_{ox}}{\varepsilon_{si}}\frac{(V_{gs} - V_{fp})}{t_{ox}\,t_{si}}\right] \quad (3.31)$$

where,

$$K_s = \frac{2\varepsilon_{si}\,t_{ox}}{2\varepsilon_{si}\,t_{ox} + \varepsilon_{ox}\,t_{si}}$$

$$\frac{d^2\emptyset_f(y)}{dy^2} - \alpha_i \emptyset_s(y) = \beta_i \quad (3.32)$$

Compare the equation (3.31) with the (3.32) then α_i and β_i for region I and III are

$$\alpha_i = \alpha_1 = \alpha_3 = \frac{2\varepsilon_{ox}}{\varepsilon_{si}\,\varepsilon_{ox}\,t_{si}} K_s$$

$$\beta_i = \beta_1 = \beta_3 = K_s\left[\frac{-qN_d}{\varepsilon_{si}} - \frac{2\varepsilon_{ox}}{\varepsilon_{si}}\frac{\left(V_{gs} - V_{fp\frac{1}{3}}\right)}{t_{ox}\,t_{si}}\right]$$

$$\omega_i = \omega_1 = \omega_3 = \sqrt{\alpha_i}$$

$$\sigma_i = \sigma_1 = \sigma_3 = -\frac{\beta_i}{\alpha_i}$$

by doing the partial differential equation of (3.32) then surface potential variation w.r.t x axis is

$$\emptyset_s(x) = \emptyset_f(x) = J_{1/3}e^{-\omega_{1/3}x_{1/3}} + K_{1/3}e^{\omega_{1/3}x_{1/3}} + \sigma_{1/3}$$

For region I:

At y=0 and x=0 position surface potential variation w.r.t x is

$$\emptyset_s(0) = J_1e^0 + K_1e^0 + \sigma_1 \quad (3.33)$$

$$V_{bi} = J_1 + K_1 + \sigma_1$$

$$J_1 = V_{bi} - K_1 - \sigma_1 \quad (3.34)$$

$$\emptyset_0 = J_1e^{\omega_1 L_{g1}} + K_1e^{\omega_1 L_{g1}} + \omega_1 \quad (3.35)$$

By using the (3.34) equation in (3.35) equation then B_1 is

$$K_1 = \frac{(V_{bi} - \sigma_1)e^{\omega_1 L_{g1}} - (\emptyset_0 - \sigma_1)}{2\sinh(\omega_1 L_{g1})}$$

similarly, for region III at y=0 and x=$L_{g1} + L_{cavity}$ the value of J_3 and K_3 is

$$J_3 = \emptyset_1 - \sigma_3 - K_3$$

$$K_3 = \frac{(\emptyset_1 - \sigma_3)e^{\omega_3 L_{g2}} - (V_{ds} + V_{bi} - \sigma_3)}{2\sinh(\omega_3 L_{g2})}$$

For region II:

$$\emptyset_2(x, y) = \emptyset_s(x) + C_{12}(x)y + C_{22}y^2 \quad (3.36)$$

By taking the double derivative of the above equation w.r.t x and y and using the boundary equation in it the variation in electric field is

$$-\frac{qN_d}{\varepsilon_{si}} = \frac{d^2\emptyset_f(x)}{dx^2} + \frac{C_{eff}}{\varepsilon_{si}}\frac{d^2\emptyset_f(x)}{dx^2}y - \frac{C_{eff}}{t_{si}\varepsilon_{si}}\frac{d^2\emptyset_f(x)}{dx^2}y^2\, 2\left[-\frac{C_{eff}}{t_{si}\varepsilon_{si}}(\emptyset_s(x) - V_{gs} + V_{fp\,2})\right] \quad (3.37)$$

then the variation at y= $t_{si}/2$ is

$$-\frac{qN_d}{\varepsilon_{si}} = \frac{d^2\emptyset_f(x)}{dx^2} + \frac{C_{eff}}{\varepsilon_{si}}\frac{d^2\emptyset_f(x)}{dx^2}\frac{t_{si}}{2} - \frac{C_{eff}}{t_{si}\varepsilon_{si}}\frac{d^2\emptyset_f(x)}{dx^2}\left(\frac{t_{si}}{2}\right)^2 + 2\left[-\frac{C_{eff}}{t_{si}\varepsilon_{si}}(\emptyset_f(x) - V_{gs} + V_{fp\,2})\right] \quad (3.38)$$

$$\frac{d^2\emptyset_f(x)}{dx^2} = \left(2\left[\frac{C_{eff}}{t_{si}\varepsilon_{si}}(\emptyset_f(x) - V_{gs} + V_{fp\,2})\right] - \frac{qN_d}{\varepsilon_{si}}\right) X \left(\frac{\varepsilon_{si}}{\varepsilon_{si} + 2t_{si}C_{eff}}\right)$$

$$\frac{d^2\emptyset_f(x)}{dx^2} - 2\frac{C_{eff}K_s}{t_{si}\varepsilon_{si}}\emptyset_f(x) = K_s\left[-2\frac{C_{eff}(V_{gs} - V_{fp\,2})}{t_{si}\varepsilon_{si}} - \frac{qN_d}{\varepsilon_{si}}\right] \quad (3.39)$$

$$\frac{d^2\emptyset_f(x)}{dx^2} - M_0\emptyset_f(x) = M_1 \quad (3.40)$$

Compare the equation (3.39) and (3.40) then

$$M_0 = 2\frac{C_{eff}K_s}{t_{si}\varepsilon_{si}}$$

$$M_1 = K_s\left[-2\frac{C_{eff}(V_{gs} - V_{fp\,2})}{t_{si}\varepsilon_{si}} - \frac{qN_d}{\varepsilon_{si}}\right]$$

$$\sigma_2 = -\frac{D_1}{D_0}$$

$$\mu = \sqrt{D_0}$$

now, by doing the partial differention of the (3.38) equation then

$$\emptyset_s(L_{g1}) = J_2e^0 + K_2e^0 + \sigma_2$$

$$\emptyset_0 = J_2 + K_2 + \sigma_2$$

$$J_2 = \emptyset_0 - \sigma_2 - K_2 \tag{3.41}$$

Put the (3.41) equation in (3.36) equation then

$$\emptyset_1 = (\emptyset_0 - \sigma_2 - K_2)e^{(\frac{\mu}{M}L_{cavity})} + K_2 e^{(\frac{-\mu}{M}L_{cavity})} + \sigma_2$$

$$K_2 = \frac{(\emptyset_0 - \sigma_2)e^{\left(\frac{\mu}{M}L_{cavity}\right)} - (\emptyset_1 - \sigma_2)}{2\sinh\left(\frac{\mu}{M}L_{cavity}\right)}$$

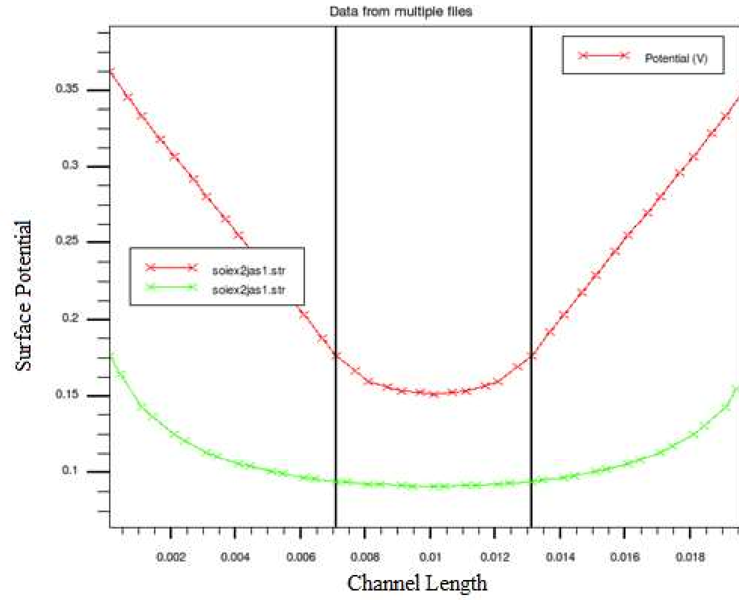

Figure 3.3 variation in the surface potential in different region of operation

By, equating the above equation of the surface potential, potential curve is obtained for all the regions. Here, potential curve for the region I and III are same as compare to that of the region II. Region II potential curve is different because of the presence of the biomolecule in the channel region of the device above the underlap region.

CHAPTER 4

RESULT AND DISCUSSION

4.1 Comparison of The Scaling Device of Biosensor With Respect To Different Dimension:

1. **Drain current:**

a) **For dielectric constant:**

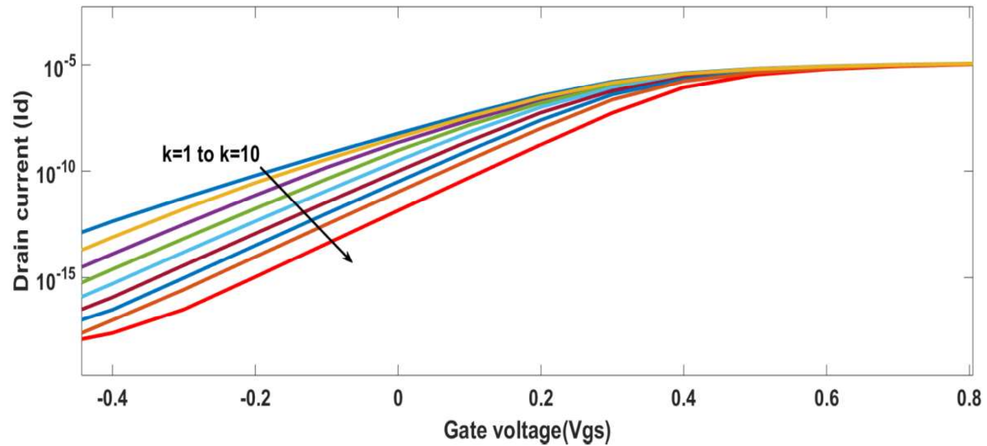

Figure 4. 1 shows Id-Vg curve for different dielectric constant at 20nm substrate thickness. When substrate doping concentration is $1X10^{18}$.

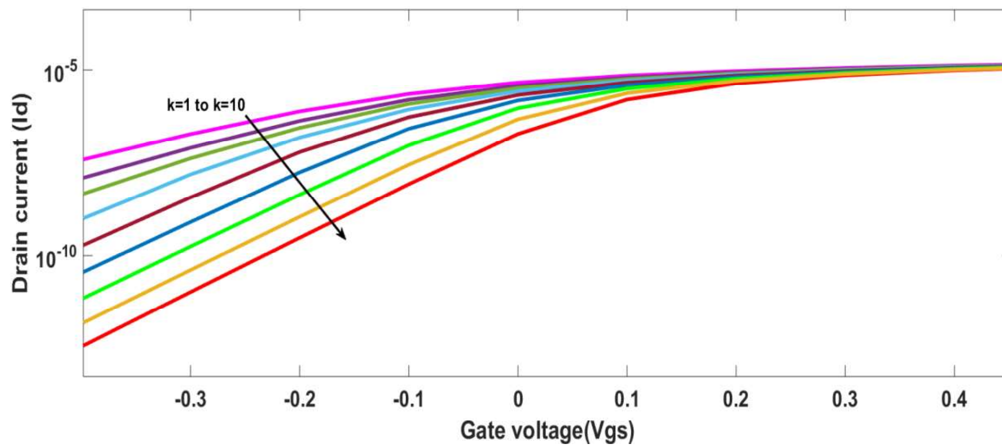

Figure 4. 2 shows Id-Vg curve for different dielectric constant at 30 nm substrate thickness. When substrate doping concentration is $1X10^{18}$.

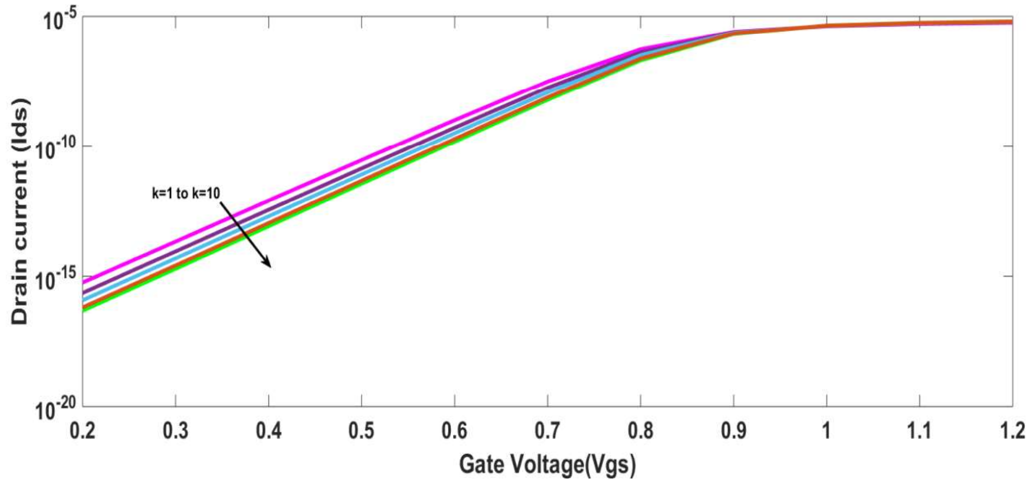

Figure 4. 3 shows Id-Vg curve for different dielectric constant for 20nm sub thickness. When substrate doping concentration is $1X10^{17}$.

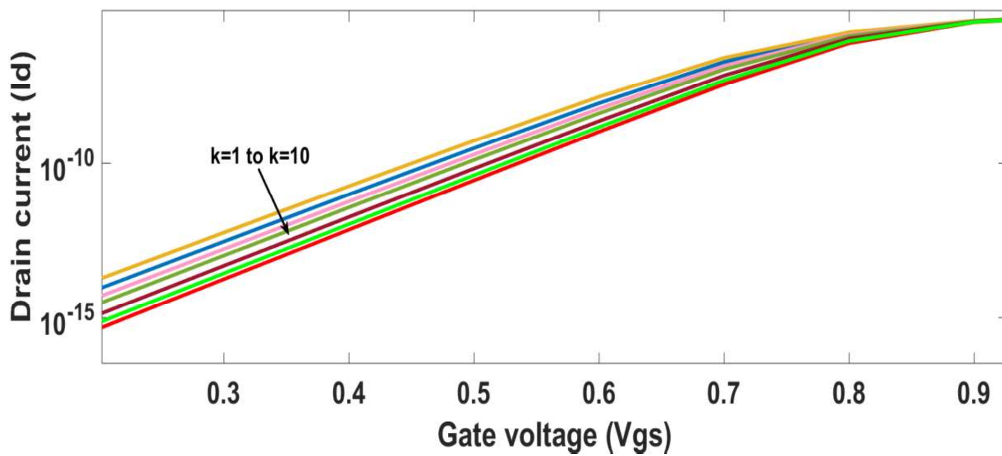

Figure 4. 4 shows Id-Vg curve for different dielectric constant for 30nm sub thickness. When substrate doping concentration is $1X10^{17}$.

figure 4.1 ,figure 4.2,figure 4.3 and figure 4.4 shows the Id-Vg curves for dielectric constant for different dimensions that for thickness of substrate concentration is 20nm and 30nm. In table 4.1 shows the variation in the threshold voltage of the device with respect to different dimensions at $1X10^{18}$ and $1X10^{17}$ substrate concentration. Threshold voltage of the device vary as the value of the dielectric constant vary that is threshold voltage increases with the dielectric constant value. When dielectric constant is unity then the analyte is neutral, by comparing that neutral analyte to the other analyte then it show maximum variation in 30nm device as comparison to that of the 20nm device that is 170 mv and 140mv shows in table 4.1.

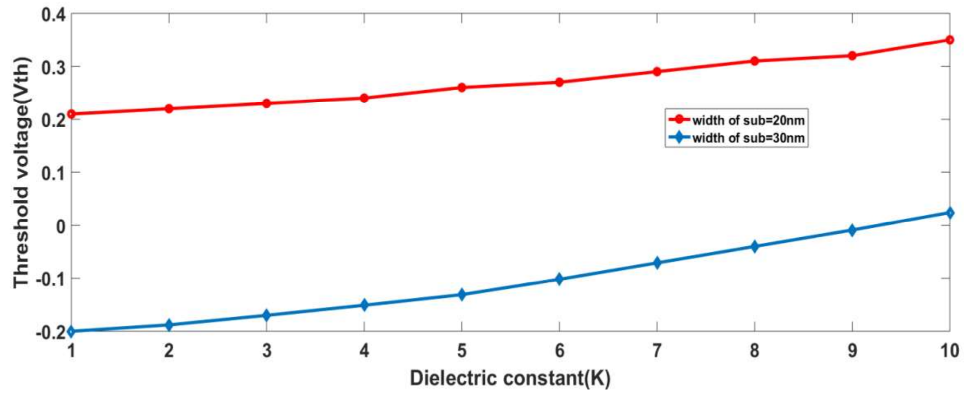

Figure 4. 5 variation in threshold voltage with respect to change in the dielectric constant value for $1X10^{18}$ substrate doping concentration.

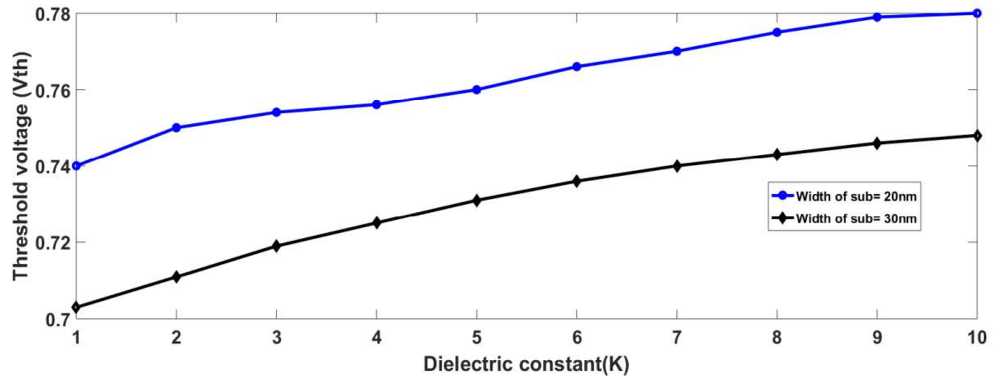

Figure 4. 6 variation in threshold voltage with respect to change in the dielectric constant value for $1X10^{17}$ substrate doping concentration.

Table 4.1: Variation in the threshold voltage with respect to the increase in the dielectric constant for substrate concentration=$1X10^{18}$

Dielectric constant (K)	Threshold voltage(Vth) with sub width=20nm (substrate conc.=$1X10^{18}$)	Threshold voltage(Vth) with sub width=30nm (substrate conc.=$1X10^{18}$)
1	0.21	-0.2
2	0.22	-0.188
3	0.23	-0.17
4	0.24	-0.151
5	0.26	-0.131
6	0.27	-0.102
7	0.29	-0.071
8	0.31	-0.04
9	0.32	-0.009
10	0.35	0.024

Table 4.2: Variation in the threshold voltage with respect to the increase in the dielectric constant for substrate concentration=1X10^17

dielectric constant (K)	Threshold voltage(Vth) with sub width=20nm (substrate conc.=1X10^17)	Threshold voltage(Vth) with sub width=30nm (substrate conc.=1X10^17)
1	0.74	0.703
2	0.75	0.711
3	0.754	0.719
4	0.756	0.725
5	0.76	0.731
6	0.766	0.736
7	0.77	0.74
8	0.775	0.743
9	0.779	0.746
10	0.78	0.748

By comparing the table 4.1 and 4.2 for both substrate concentration1X10^18 and 1X10^17. It is shown in the table that maximum threshold voltage variation is shown in the 1X10^18 (0.17mv for 30nm and 0.14 mv for 20nm). That is if there is maximum change in the threshold voltage than that device shows maximum sensitivity. So, 1X10^18 with 30nm is more sensitive as compare to that of the 1X10^17 .

b) For interface charges:

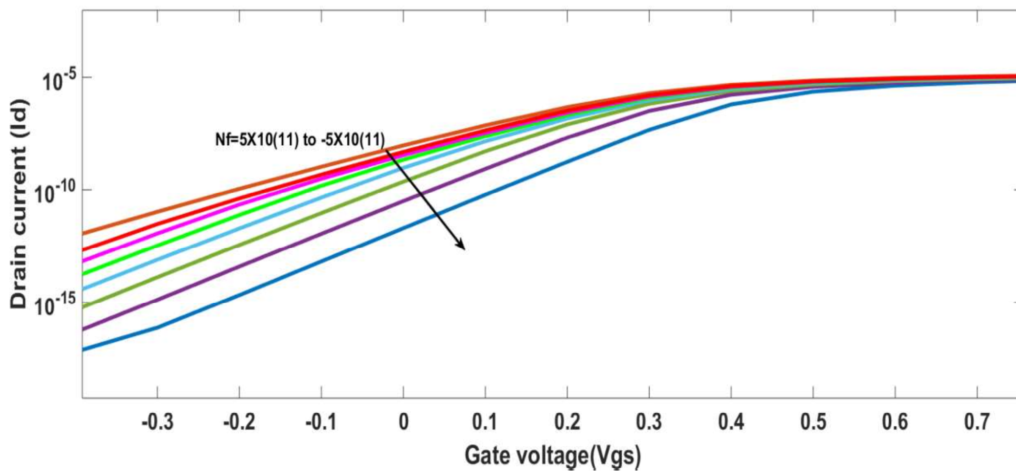

Figure 4. 7 represents Id-Vg curve for the interface charges at the surface for different substrate thickness 20nm. When substrate concentration is 1X10^18 .

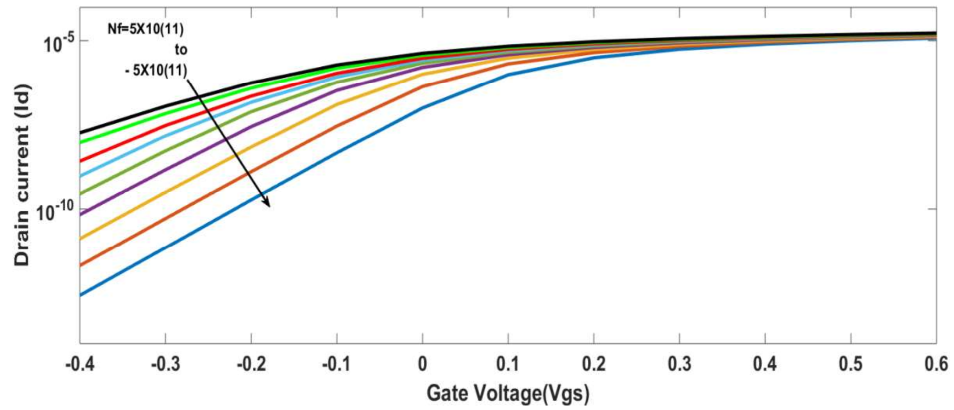

Figure 4. 8 represents Id-Vg curve for the interface charges at the surface for different substrate thickness 30nm. When substrate concentration is $1X10^{18}$.

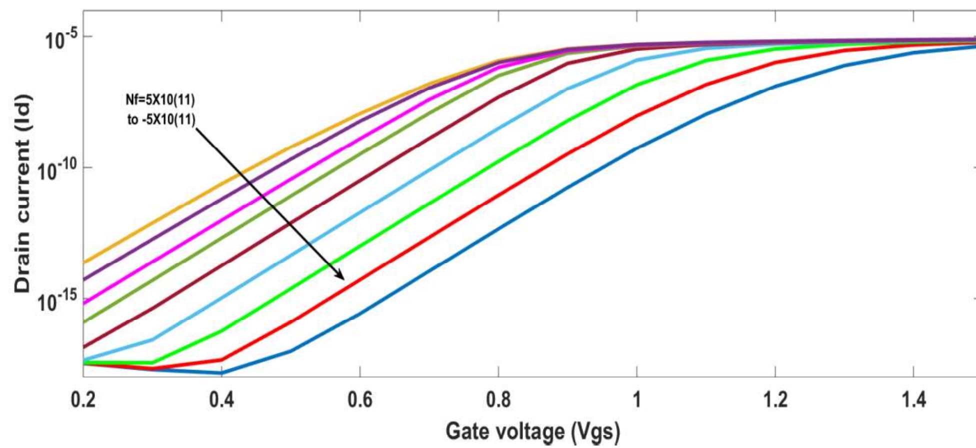

Figure 4. 9 represents Id-Vg curve for the interface charges at the surface for different substrate thickness 20nm. When substrate concentration is $1X10^{17}$.

Figure 4.7, figure 4.8, figure 4.9 and figure 4.10 represents Id-Vg curve for the interface charges at the surface for different substrate thickness 20nm and 30nm. There is variation in threshold voltage of the device take place as the interface charges vary from negative interface charges (-$5X10^{11}$) to positive interface charges ($5X10^{11}$).

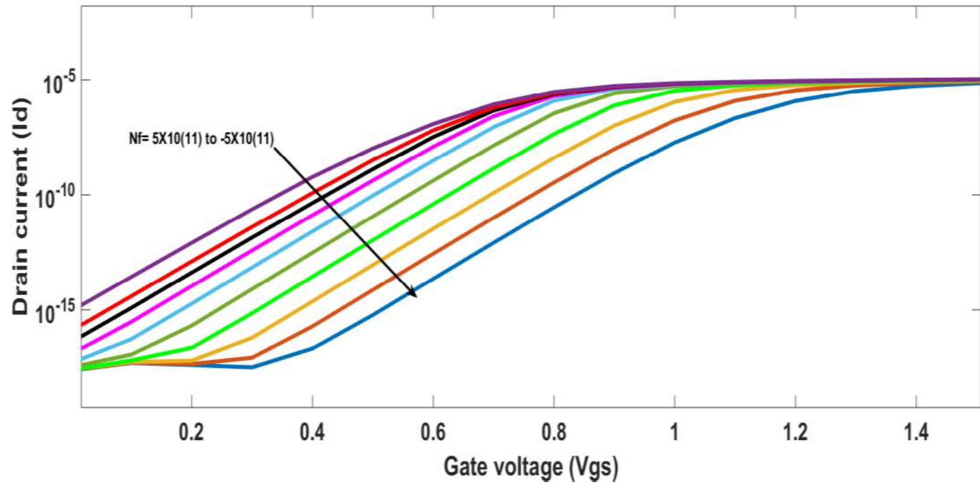

Figure 4. 10 represents Id-Vg curve for the interface charges at the surface for different substrate thickness 30nm. When substrate concentration is $1X10^{17}$.

Table III and IV shows how the threshold voltage decreases as the interface charges increase from negative interface charges to positive interface charges. There is a maximum change in the threshold voltage for the negative interface charges to that of the positive interface charges in comparison to that of the neutral charged analyte. As we can see in figure 4.11 and figure 4.12 the threshold voltage of the 20nm device is linearly decreasing in comparison to that of the 30nm device.

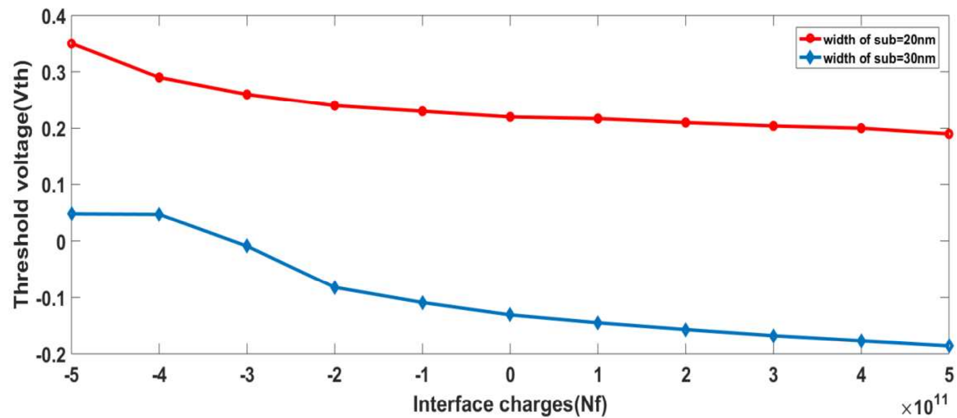

Figure 4. 11 variation in threshold voltage with respect to change in the interface charges with substrate concentration $1X10^{18}$.

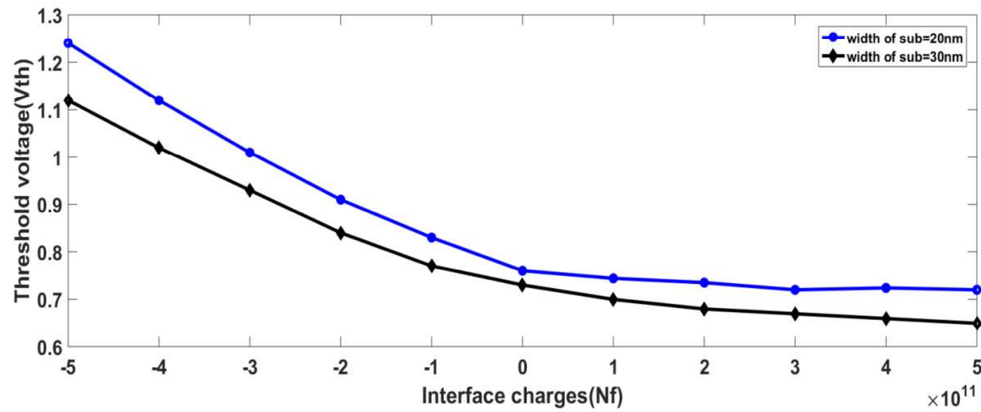

Figure 4.12 variation in threshold voltage with respect to change in the interface charges with substrate concentration $1X10^{17}$.

Table 4.3: Variation in the threshold voltage with respect to the variation in the interface charges for substrate concentration=$1X10^{18}$

Interface charges	Threshold voltage(Vth) with sub width=20nm (substrate conc.=$1X10^{18}$)	Threshold voltage(Vth) with sub width=30nm (substrate conc.=$1X10^{18}$)
-5E+11	0.35	0.048
-4E+11	0.29	0.047
-3E+11	0.26	-0.009
-2E+11	0.24	-0.082
-1E+11	0.23	-0.109
0	0.22	-0.131
1E+11	0.217	-0.145
2E+11	0.21	-0.157
3E+11	0.204	-0.168
4E+11	0.2	-0.177
5E+11	0.19	-0.186

Table 4.4: Variation in the threshold voltage with respect to the variation in the interface charges for substrate concentration=1X10^{18}

Interface charges	Threshold voltage(Vth) with sub width=20nm (substrate conc.=1X10^{17})	Threshold voltage(Vth) with sub width=30nm (substrate conc.=1X10^{17})
-5E+11	1.24	1.12
-4E+11	1.12	1.02
-3E+11	1.01	0.93
-2E+11	0.91	0.84
-1E+11	0.83	0.77
0	0.76	0.73
1E+11	0.744	0.7
2E+11	0.735	0.68
3E+11	0.72	0.67
4E+11	0.724	0.66
5E+11	0.72	0.65

In fig.4.13 and 4.14 shows the variation in the sensitivity of the device for the various dimensions for 20nm and 30nm thickness of silicon substrate with doping concentration of the 1X10^{17} and 1X10^{18} cm^{-3}. There is relationship of the sensitivity with the threshold voltage of the devices which is mentioned in the equation 4.1 and 4.2. With the help of these equation the sensitivity of the device is

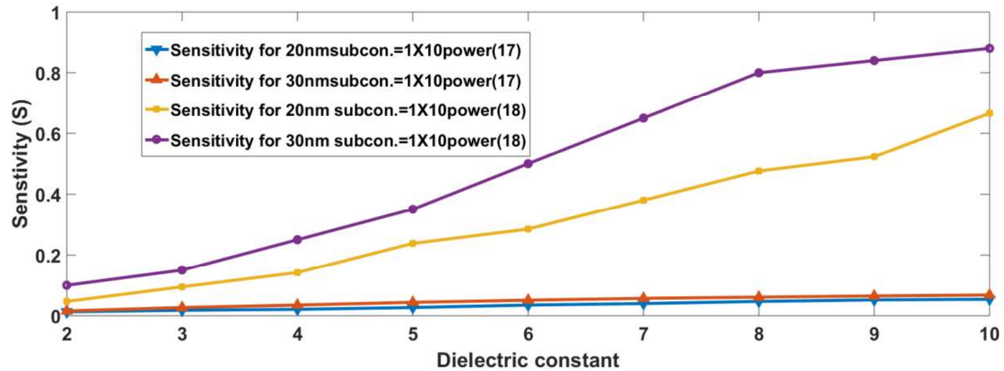

Figure 4. 13 comparison in the sensitivity of the device for different devices for dielectric constant

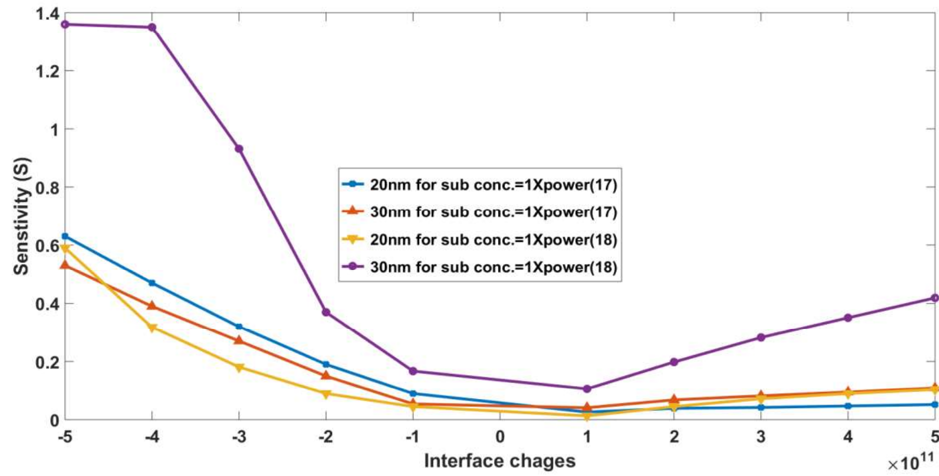

Figure 4. 14 comparison in the sensitivity of the device for different devices for interface charges

$$S_n = \left| \frac{V_{th}\,(\text{neutral}\ \ k=1) - V_{th}\,(k>1)}{V_{th}\,(\text{neutral}\ \ k=1)} \right| \tag{4.1}$$

$$S_n = \left| \frac{V_{th}\,(\text{neutral biomolecule}) - V_{th}\,(\text{charged biomo lecule})}{V_{th}\,(\text{neutral biomolecule})} \right| \tag{4.2}$$

going to be founded. In figure4.13 increase in the sensitivity of the device with an increase in value of the dielectric constant of the device. From the comparison of the different dimensions of the devices with the different doping concentration in the substrate. It shows that the device whose doping concentration in the substrate is $1X10^{18}$ cm^{-3} which the substrate thickness is 30nm shows better sensitivity and it increases more linearly in comparison to other dimensions. In figure 4.14 similarly the sensitivity for the device whose doping concentration in the substrate is $1X10^{18}$ cm^{-3} which the substrate thickness is 30nm shows better sensitivity in comparison to others. So we can say that device with doping concentration $1X10^{18}$ cm^{-3} and with substrate thickness 30nm is the better device.

4.2 Split gate JL biosensor with UTB:

1. **Drain current :**

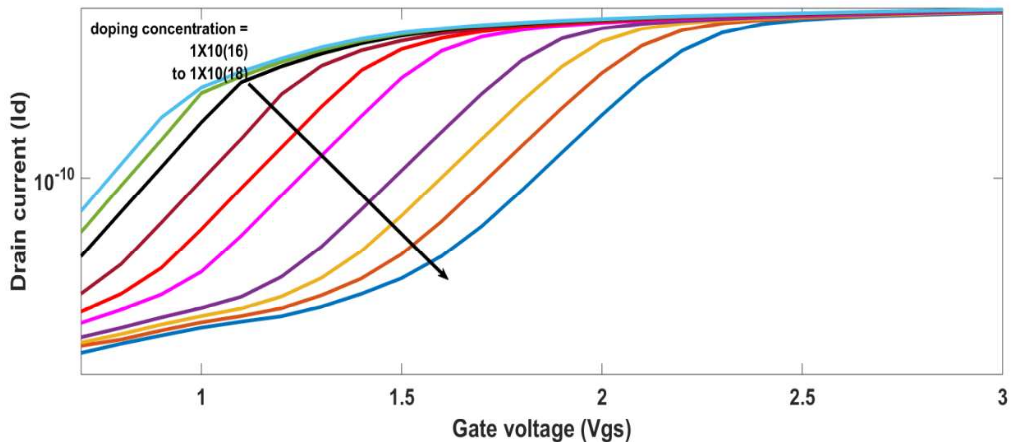

Figure 4. 15 variation in the drain current with the variation in the doping concentration with respect to the gate voltage.

Neutral analytes with doped concentration and of charges analytes shows there impact on the drain current on the n-type split gate JL bio-transistor. In figure 4.15 presents the result of the drain current variation w.r.t the neutral analyte with increase in the doping concentration in open cavity region. Device off-current starts decreasing as the doping concentration in the netural analyte increases, although the on-current of the device remains constant that is unchanged. When the doping concentration in the cavity region of the device is more than $9X10^{17}$ then the modelled device does not work properly. This happens when the chitosane of dielectric constant is 5.5 with increasing doping concentration.

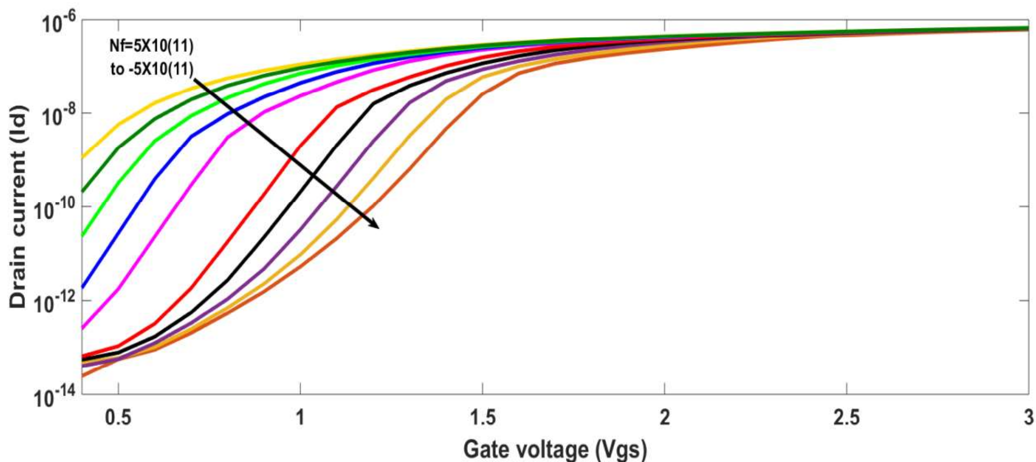

Figure 4. 16 variation in the drain current with interface charges w.r.t the gate voltage.

Figure 4.16 shows the impact of the charged analytes on the drain current, which are not moving inside the cavity region. The off-current of the charges analytes that is for the off current

decreases for negatively charged analytes but that of the positive analytes it increases in comparision to that of the neutral analyte, it happen when the chitosane of dielectric value is 5.5.

2. Threshold voltage:

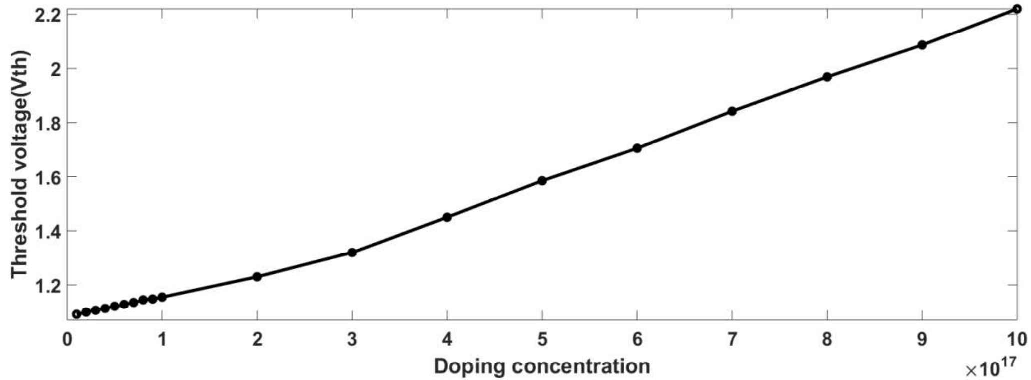

Figure 4. 17 variation in the threshold voltage w.r.t increse in the doping concentration of the device.

Figure 4.17 and Figure 4.18 shows the change in the threshold voltage of the device with respect to the increase in doping of the neutral analytes and the with respect to the charged analytes. In the study of the device, the threshold voltage is treated as the parameter of the device which helps in detecting the interaction analytes (neutral with doped concentration and charged) with the sensing area of the n-type SG JL biosensor. In Figure 4.17 the outcome of the neutral analytes in the open cavity region, with increase in doping concentration of the cavity region from $1X10^{16}$ to the higher doping concentration then the threshold voltage increases. When the doping concentration of the $2X10^{17}$,3 $X10^{17}$,5 $X10^{17}$ and 9 $X10^{17}$ then the threshold voltage is 80mv, 170mv, 430mv and 690mv respectively.

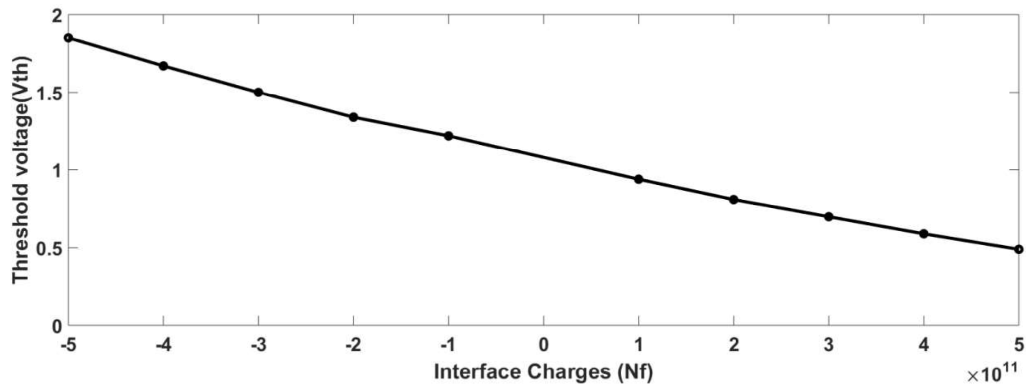

Figure 4. 18 change in the threshold voltage with respect to interface charges.

Figure 4.18 shows the threshold voltage impact of the charged analytes on the threshold voltage of the device. For the negatively charged analytes the threshold voltage increases but that of the

positively charged analytes it decreases as compared to that of the neutral analytes. The variation in the threshold voltage of device is 75 mv for the negatively charged that is for $-5X10^{11}$ and 61 mv for the positively charged analyte that is for $5X10^{11}$ in comparison to that of the chitosane which has the dielectric constant of 5.5. As the threshold voltage of the is changes more for the negative analyte then that of the positive analyte.

3. Sensitivity:

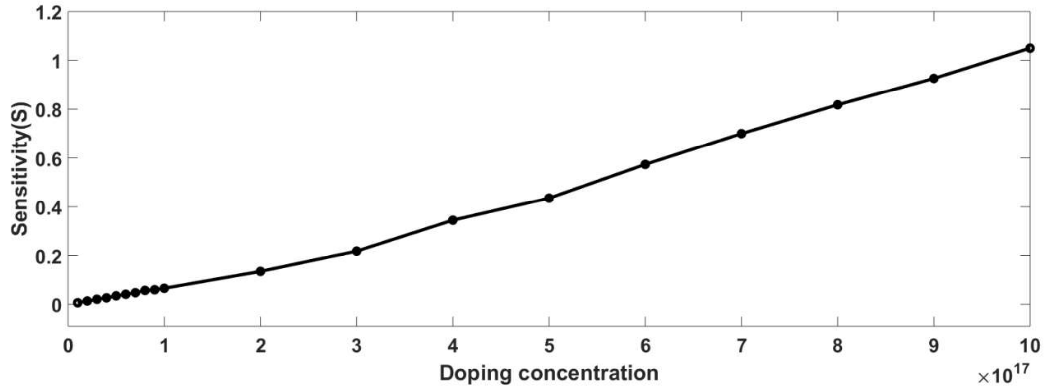

Figure 4. 19 variation in the sensitivity doping concentration

There are two different cases that is the neutral analyte and charged analyte in the open cavity region of the device then the sensitivity of a device then the following two mathematical for the equation (4.3) and in equation (4.4) is

$$S_n = \left| \frac{V_{th}\,(\text{neutral} \;\; k=5.5) - V_{th}\,(\text{neutral} \;\; \text{with} \;\; \text{doping} \; > 1X10)}{V_{th}\,(\text{neutral} \;\; k=5.5)} \right| \tag{4.3}$$

$$S_n = \left| \frac{V_{th}\,(\text{neutral} \;\; \text{biomolecule} \;\;) - V_{th}\,(\text{charged} \;\; \text{biomolecule} \;\;)}{V_{th}\,(\text{neutral} \;\; \text{biomolecule} \;\;)} \right| \tag{4.4}$$

Here the impact of the neutral analyte with doping concentration and charged analyte on the sensitivity of n-type SG JL biosensor is modeled by the equation (4.3) and it is depicted in figure 4.19. Sensitivity of the device increases linearly as the doping concentration of the neutral analyte increases from $1X10^{16}$ to the higher doping concentration. The effect of the charged analytes is depicted with the help of (4.4) equation and showed in figure 4.20. When the negatively charged analytes ($-5X10^{11}$) is bounded in the cavity region of the device then, device sensitivity increased by 0.6 V and that of the positively charged analyte ($5X10^{11}$) the sensitivity is increased by 0.34 V. Therefore the n-type SG JL biosensor is more sensitive to the negatively charged analyte to that of the positively charged analyte.

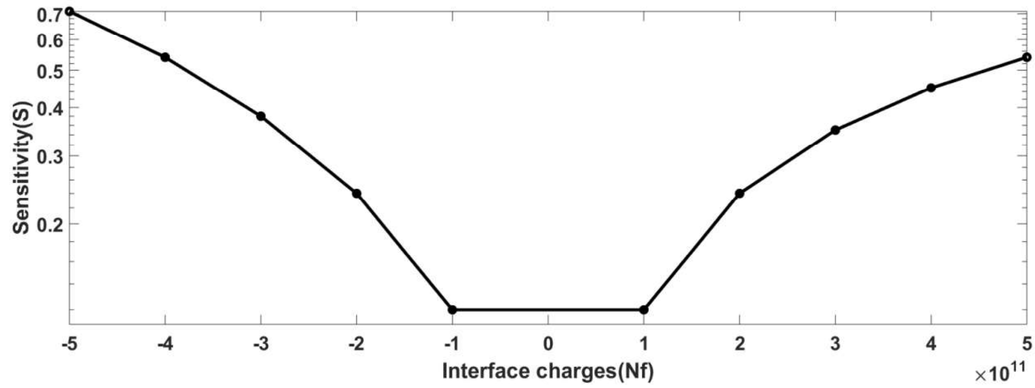

Figure 4. 20 variation in the sensitivity doping concentration

4. Surface potential:

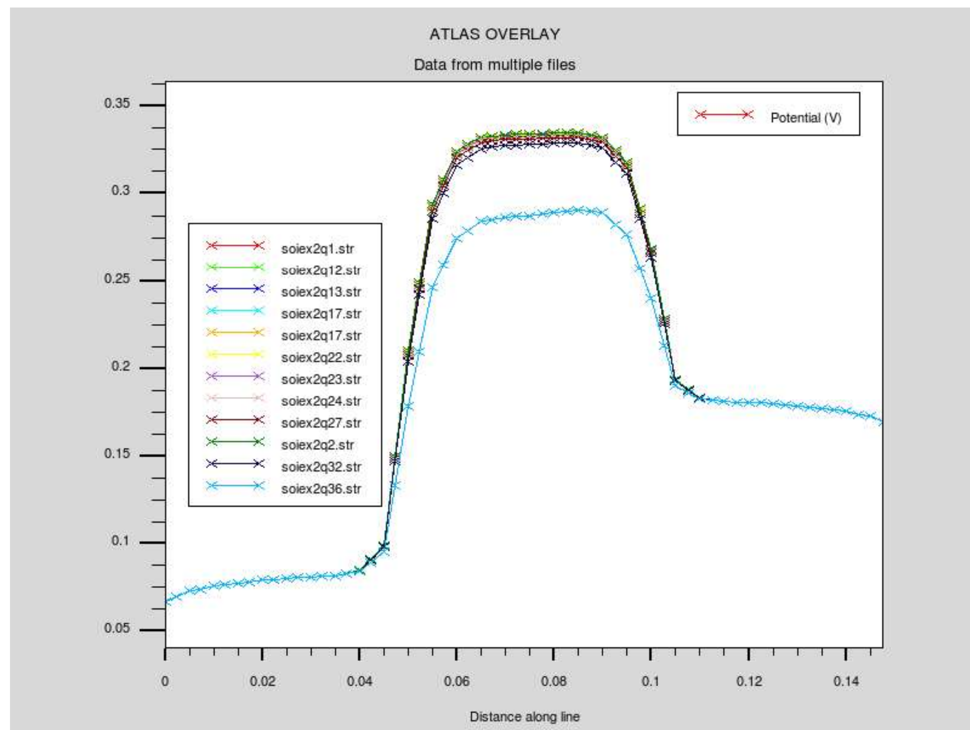

Figure 4. 21 variation in surface potential with respect to dielectric constant

Distribution of the electrostatic potential in the region of channel of the device for both doped concentration in the neutral analyte same for the charged analyte is depicted in figure 4.21. When the cavity which is open is empty then the dielectric constant value of the cavity region is taken to be unity and the new dielectric constant is assigned to the cavity region that is chitosane 5.5 and then the corresponding electrostatic potential in the cavity region increases. Now the neutral analyte bounded inside the cavity region, in that the doping concentration in that neutral analyte increases, then the potential of the surface changes. So, as the doping concentration increases of the sensing area, then the surface potential start decreasing of open cavity region.

In figure 4.22 the impact of the charged analytes are shown on the surface potential of the device is depicted. The charged analyte in the open cavity of the device, the surface potential of the SG JL biosensor are going to decrease for the negatively charged analytes and it is going to increase to the positively charges analyte as compare to that of the neutral analyte.

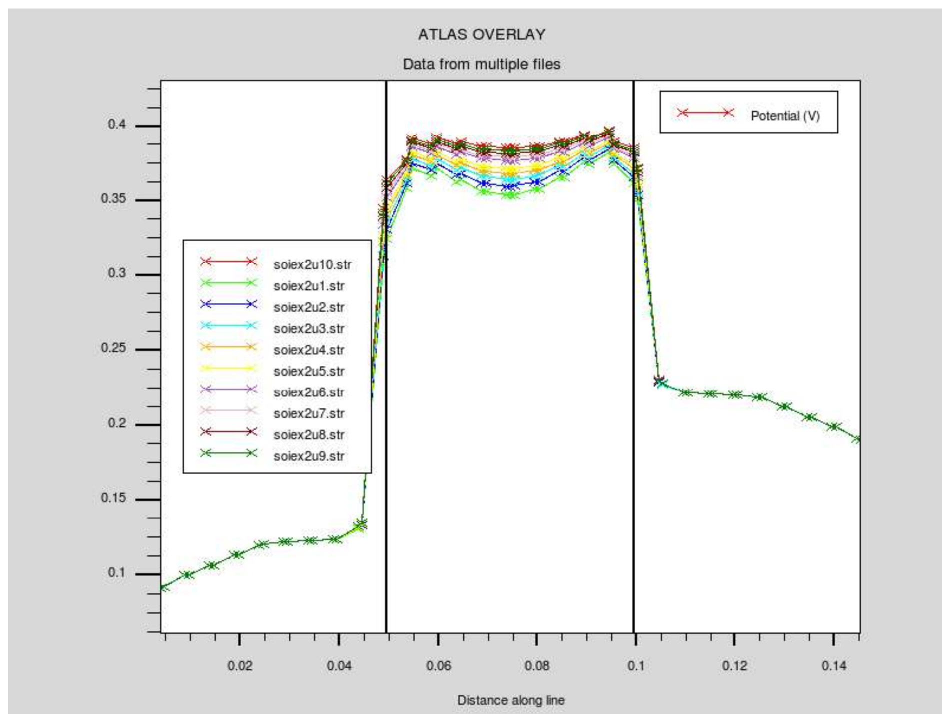

Figure 4. 22 variation in surface potential with respect to interface charges

CHAPTER 5

CONCLUSION AND FUTURE SCOPE

In the study, of new device here the model of n- type split gate JL MOSFET with the UTB are used for investigating the biosensing application for detecting the doping analytes. This device has been basically simulated on the SILVACO (TCAD) tool. Because of the impact of the of doping in the biomolecule and charged analytes on the electrical characterstics that is the threshold voltage, sensitivity and surface potential of n-type gate JL MOSFET are examined. Here doping and the charged analysed show there impact on the threshold voltage as the doping increases from $1X10^{16}$ to $9X10^{17}$ it shows the increase in the threshold voltage of the device, that is the large change in the threshold voltage of the tell us that the device is more sensitive that is it is sensing the change in the small change in the doping of the device. Similarly for the interface charges the threshold voltage starts decreasing. It is concluded that the more the variation in the threshold voltage more sensitive is the device. Threshold voltage of the device is going to be reduced when the analyte charges are going to be reduce due to the drying out. All the electrical characteristics of the device are going to be more influenced by the negatively charged analytes not by the positively charged analytes, because the device shows more positive threshold value in comparison to that of the positive charged analytes.

There are some changes can be made on the present work:

1) This work related to different Junctionless devices in terms of its electrical characteristics, are compared to the different scaling devices of the Junctionless MOSFET. And then by checking them that which one is better biotransistor in comparison to that of the other.
2) This work can also be extended to the other multi-gate device that is to the tunnel-gate MOSFET, gate all around MOSFET and CNT MOSFET which increases the better control of the gate on the channel and help in getting the better sensitivitys.

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