Design & Analysis of Folded Cascode OTA

A Thesis

Submitted in the partial fulfillment of

requirement for the award of the degree of

Master of Engineering
In
Electronics and Communication

Submitted by

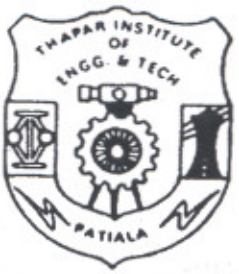
MANU BANSAL

Regn. No. 8004152

Under the guidance of

MRS. ALPANA AGARWAL

Assistant Professor, Department of Electronics & Communication Engineering



Department of Electronics & Communication Engineering

THAPAR INSTITUTE OF ENGINEERING AND TECHNOLOGY

(Deemed University)

PATIALA-147004

Certificate

This is to certify that the thesis entitled "***Design & Analysis of Folded Cascode OTA***" submitted by Ms. Manu Bansal, in partial fulfillment of the requirement for the award of the degree of **Master of Engineering** in **Electronics & Communication** to Thapar Institute of Engineering & Technology (Deemed University), Patiala, India, is a record of candidate's own work carried out by her under my supervision and guidance. The matter embodied in this dissertation has not been submitted in part or full to any other university or institute for the award of any degree.

Alpana 16 Sept 2003

(Mrs. Alpana Agarwal)
Assistant Professor,
Department of Electronics & Communication Engineering,
T.I.E.T., Patiala

COUNTERSIGNED

P.K.Bansal 16/9/2003

(Dr.P.K.Bansal)
Professor & Head, ECED
T.I.E.T., Patiala

(Dr.D.S.Bawa)
Dean of Academic Affairs
T.I.E.T., Patiala

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Manu Bansal

(MANU BANSAL)

Regn. No 8004152

ABSTRACT

The outside world is actually of analog nature and to be able to interact with computers etc., we need some amount of analog and mixed analog/digital circuits. Among various analog circuits *Operational Amplifier* has a very dominant role. It is used in almost all-analog applications. Its main characteristics are high input resistance, low output resistance, high gain, high CMRR, high unity gain bandwidth and high Common Mode Range (CMR) etc. Performance of any analog application depends upon these characteristics, if they are meeting the desired specifications. Once the topology is been selected the main thing, which put impact on characteristics, is design (values) of components.

A fully differential CMOS folded-cascode OTA is analyzed and the results are presented in the form of design equations and procedures. In this study a CAD tool has been developed using Turbo C for determining the component values and transistor dimensions for CMOS Folded Cascode OTA. Trade-offs among such factors as DC Gain, Unity Gain Bandwidth, Phase Margin, Output Swing, Slew Rate, Common Mode Gain, PSRR and Offset etc are made evident. A number of Op-amp circuits with varying specifications have been synthesized with the tool. The synthesized circuits have been simulated using Tanner tools. On the basis of simulation results the performance analysis has been done. A graphical representation of the relationships among the gain, phase margin for different capacitive loadings is presented to visually illustrate one form of design optimization.

CONTENTS

LIST OF ABBREVIATIONS

CMOS	Complementary Metal Oxide Semiconductor
OP-AMP	Operational Amplifier
CMRR	Common Mode Rejection Ratio
ICMR	Input Common Mode Range
SR	Slew Rate
PSRR	Power Supply Rejection Ratio
CM	Common Mode
DM	Differential Mode
IC	Integrated Circuit
GBW	Gain Bandwidth

LIST OF FIGURES

CHAPTER 1

CHAPTER 2

CHAPTER 5

1. OPERATIONAL AMPLIFIER

1.1. INTRODUCTION

An operational amplifier is a high gain amplifier. It is a versatile device that can be used to amplify dc as well as input signals. It was originally designed for computing such mathematical functions as addition, subtraction, multiplication and integration. Thus the name Operational Amplifier stems from its original use for these mathematical operations and is abbreviated to op-amp. A symbol used to represent an operational amplifier in schematics is shown in Fig. 1.1

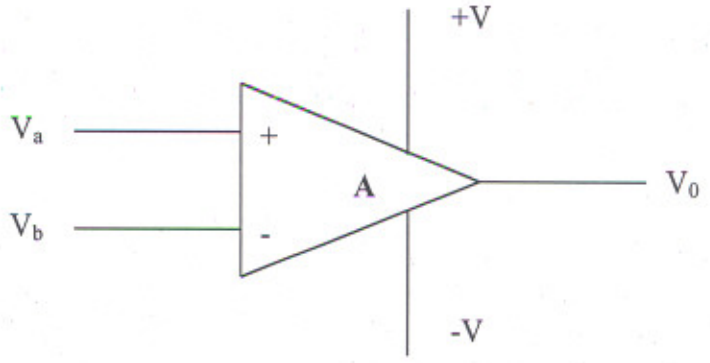


Figure 1.1: Symbol of operational amplifier

The operational amplifier has two inputs and only one output. One input is called the **inverting** input and is denoted by minus sign. A signal applied to this input appears as an amplified but phase inverted signal at the output as an amplified signal, which has the same phase as that of the input signal.

The availability of two input terminals simplifies feedback circuitry and makes the operational amplifier a highly versatile device. If a feedback is applied from the output to the inverting input terminal, the result is negative feedback, which gives a stable amplifier with precisely controlled gain characteristics. On the other hand, if the feedback is applied to the non-inverting input, the result is positive feedback, which gives

oscillators and multivibrators. Special effects are obtained by combination of both types of feedbacks.

The operational amplifier needs a dual symmetrical power supply as shown in Fig. 1.1. This enables the operational amplifier to amplify dc signals of both polarities, positive or negative, with respect to ground. The circuit is so designed that if both inputs are connected to ground, the dc output voltage is zero. However, because of small internal unbalances, a small dc voltage may appear at the output.

CMOS op-amp has an input impedance which is greater than $10^{12}\Omega$ and bias and offset currents on the order of 10fA. Input offset voltage is about 1mV with drift around 1μV/°C. Early CMOS op-amps suffered from seriously reduced gain bandwidth and slew rate, especially when driving loads less than 10kΩ. But there are now available CMOS op-amps with gain bandwidth over 1MHz and slew rate of 1V/μsec. In addition to exceptional DC input characteristics, CMOS op-amps have very low power supply voltage and current requirements.

Because each transistor within the op-amp is controlled by voltage, and has an insulator at its input, the total current drawn from the power supply by a CMOS op-amp is on the order of 100μA. It is classified into two groups:

- General-purpose op-amp
- Special-purpose op-amp

General-purpose op-amp can be used in variety of applications. Such as integrator, differentiator, summing amplifier, and others.

On the other hand, special-purpose op-amps are used only for the specific applications they are designed for. For example, the op-amp used only for audio power applications.

1.2 BLOCK DIAGRAM OF TYPICAL OP-AMP

Since an op-amp is a multistage amplifier, it can be represented by a block diagram as shown in Fig. 1.2.

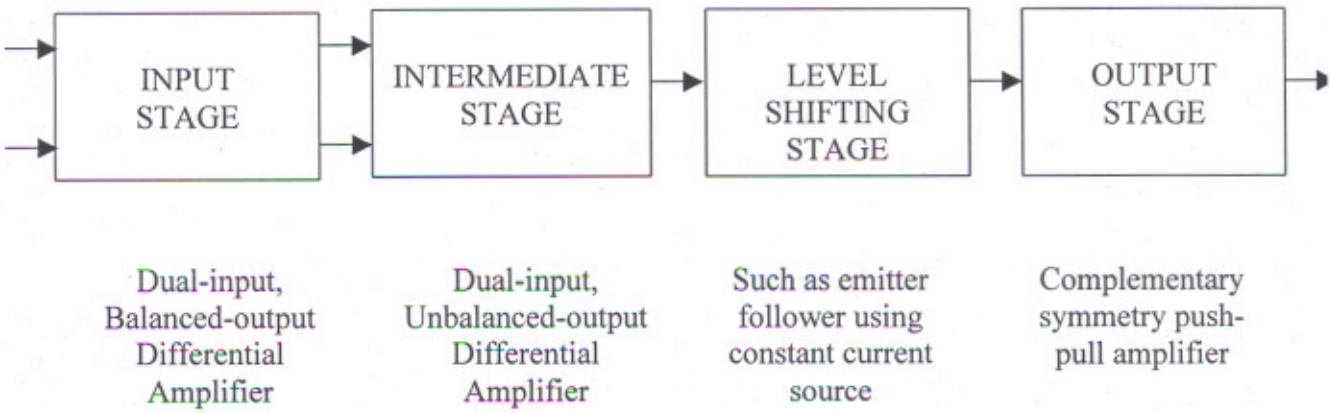


Figure 1.2: Block diagram of Op-Amp

- **INPUT STAGE**

The input stage is the dual-input, balanced-output differential amplifier. This stage generally provides most of the voltage gain of the amplifier and designed so that it provides a high input impedance, large common mode rejection ratio, power supply rejection ratio, low offset voltage, low noise and high gain.

- **INTERMEDIATE STAGE**

In most cases the gain provided by the input stages is not sufficient and additional amplification is required. This is provided by intermediate stage, which is another differential amplifier, driven by the output of the first stage. It serves other purpose also. As this stage uses differential input unbalanced output differential amplifier, so it provide required extra gain as well as convert the differential signal to single ended signal. So that rest of the stages need not contain symmetrical differential stages.

▪ LEVEL SHIFTING STAGE

As direct coupling is used in operation amplifier, the dc voltage at the output of intermediate stage is well above ground potential. This increase in dc level tends to shift the operating point of the succeeding stages and, therefore limits the output voltage swing and may even distort the output signal. Therefore generally the level translator (shifting) circuit is used after the intermediate stage to shift the dc level at the output of the intermediate stage to zero volts with respect to ground.

▪ OUTPUT STAGE

This stage is output buffer. It provides the low output impedance and larger output current needed to drive the load of op-amp. It normally does not contribute to the voltage gain. If op-amp is the internal component of switched capacitor circuit, the output load is usually a capacitor and the buffer need not provide a large current or very low output impedance. However, if the op-amp is at the circuit output, it may have to drive a large capacitor and low resistive load. This requires large current driving capability and very low output impedance, which can only be attained by using large devices with appreciable dc bias currents.

This is usually a push-pull complementary amplifier output stage. The output stage increases the output voltage swing and raises the current supplying capability of the op-amp. A well-designed output stage also provides low output resistance.

Circuit of CMOS operational amplifier showing its different stages and various components is shown in Fig. 1.3

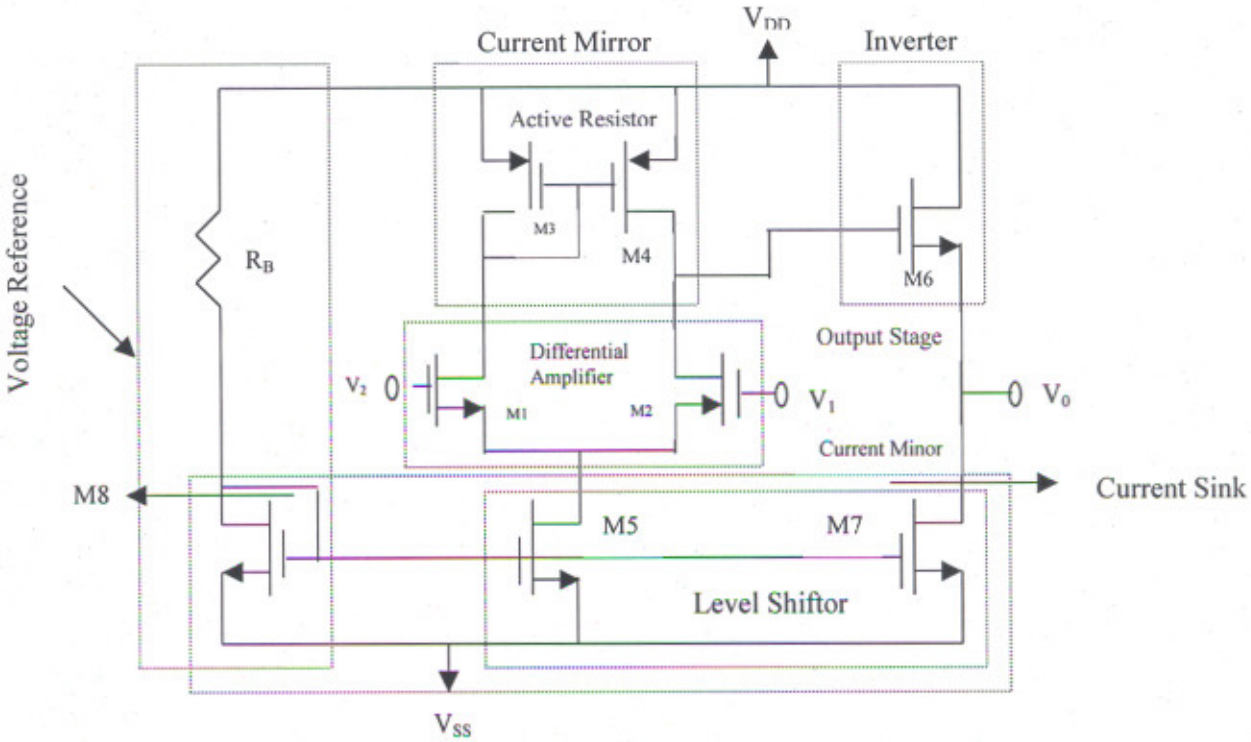


Figure 1.3: CMOS OP-AMP illustrating its various components.

1.3 OP-AMP CHARACTERISTICS

The power selection of which op-amp to use in a particular application is often the key factor which determine the success or failure of the circuit. There is a wide spectrum of op-amps available, from those requiring only 1 volt supplies with bias currents in the 10^{-15}. A range, to those that will output hundreds of volts at tens of amps, op-amps specialized for precision DC performance, with only 10's KHz bandwidth to video op-amps which amplify from DC to GHz. So, with all of this variety, how can one go about selecting the right IC? First one must determine several IC characteristics like:

- **GAIN**

Ideally the gain is infinity but for practical op-amps, the voltage gain is finite. Typical values for low frequencies and small signals are A = 10^3 to 10^5, corresponding to 60 to 100 dB gain.

- **UNITY GAIN BANDWIDTH**

It is also called frequency response or gain bandwidth product. Because of the capacitances associated with devices making up the op-amp circuit, the gain decreases at high frequencies. This fall-off must usually be enhanced by the addition of extra capacitance called compensation capacitance in the circuit to ensure that the circuit does not oscillate. This aspect of op-amp behavior is characterized by the unity gain bandwidth, which is the frequency f_0 at which the open-loop voltage gain ($|A(f_0)| = 1$) is equal to unity. For CMOS op-amps, f_0 is usually in the range 1 to 100MHz. It can be measured with the op-amp connected in a voltage follower configuration.

- **SLEW RATE**

For large input step voltage, some transistors in the op-amp may be driven out of their saturation regions or cutoff completely. As a result, the output will follow the input al slower finite rate.

The rate at which the voltage gain can change is primarily limited by the frequency compensation capacitor. The voltage across a capacitor cannot change instantaneously, but is governed by the size of the capacitor and the amount of current available to change the capacitor.

$$\frac{dv_{capacitor}}{dt} = \frac{I}{C}$$

The maximum rate of change dv_0/dt is called the slew rate. For typical CMOS op-amps, slew rates of 1 to 20 V/μs can be obtained.

- **INPUT COMMON MODE RANGE (CMR)**

When the same voltage is applied to both input terminals, the voltage is called a common mode voltage V_{cm} and the op-amp is said to be operating in the common mode configuration.

CMR is one of the most important characteristics of op-amp. The input common mode range specifies the range of the common mode input voltage values such that the

differential stage continues to amplify the differential input voltage with approximately same differential gain.

▪ OUTPUT VOLTAGE SWING

Output voltage swing is the range over which the output voltage can vary without excessive distortion. Infect the output voltage swing gives the values of the maximum positive and negative voltages above which transistor will out of saturation.

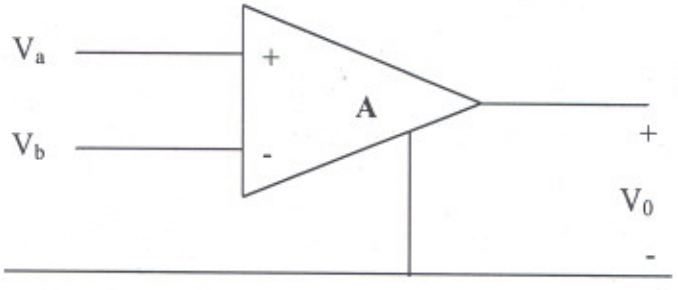
Normally the maximum value of V_0 for linear operation is somewhat smaller than the positive dc supply voltage; the minimum value of V_0 is somewhat positive with respect to the negative supply.

▪ COMMON MODE REJECTION RATIO

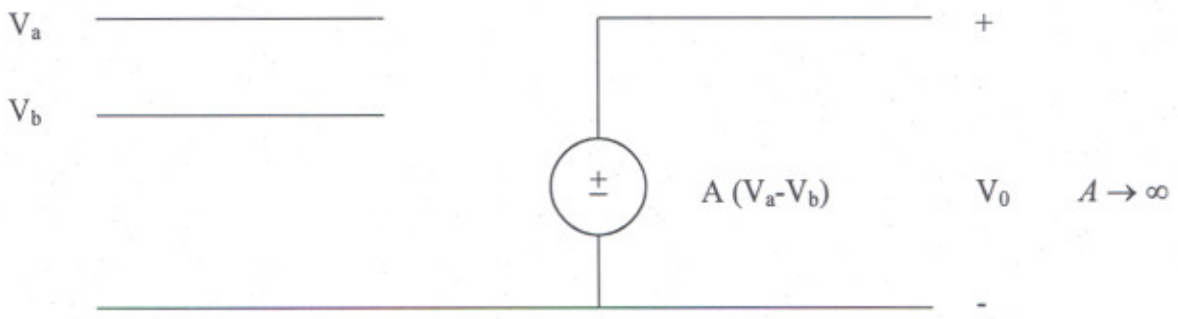
The common mode rejection ratio (CMRR) of an operational amplifier is the ratio of the differential mode gain to the common mode gain. Where A_D is

$$A_D = \frac{V_0}{V_a - V_b}$$

As shown in Fig.1.4b. Also the common mode gain A_c, which can be measured as shown in fig. below, where $A_c = V_0/V_{in,c}$, where $V_{in,c} = (V_a+V_b)/2$.



(a)



(b)

Figure 1.4: (a) Symbol for ideal op-amp (b) equivalent circuit

The CMRR is defined as A_D/A_C or (in logarithmic units)

$$CMRR=20 \log_{10} (A_D/A_C) \quad \text{in decibel}$$

More meaningful characterization from an application standpoint is to regard the CMRR as the change in input offset voltage that results from a unit change in common mode input voltage. Assume for example, that we apply zero common mode input voltage to the amplifier and then apply just enough differential voltage to the input to drive the output voltage to the zero. The dc voltage we have applied is just the input offset voltage V_{OS}. If we keep the applied differential voltage constant and increase the common mode input voltage by an amount ΔV_{ic} the output voltage will change, by an amount

$$\Delta V_0 = A_{cm} \Delta V_{ic}$$

In order to drive the output voltage back to zero, we will have to change the differential input voltage by an amount

$$\Delta V_{id} = \Delta V_0 / A_{dm} = \Delta V_0 = (A_{cm} \Delta V_{ic}) / A_{dm}$$

Typical CMRR rules values for CMOS amplifiers are in the range 60 to 80 dB. The CMRR measures how much the op-amp can suppress noise, and hence a large CMRR is an important requirement.

▪ POWER SUPPLY REJECTION RATION (PSRR)

This is also called *supply voltage rejection ratio* (SVRR) or *power supply sensitivity* (PSS). If a power supply voltage contains an incremental component v due to noise, hum and so on, a corresponding voltage A_{pv}, will appear at the op-amp output. The PSRR is defined as A_D/A_P, where $A_D = A$ is the differential gain. It is common to express the PSRR in decibels; then PSRR = 20 $\log_{10}$ (A_D/A_P). Usual PSRR value range from 60 to 80 dB for the op-amp alone.

▪ OUTPUT RESISTANCE

For real CMOS op-amps, the open-loop output impedance is nonzero. It is usually resistive and is on the order of 0.1 to 5kΩ for op-amps with unbuffered output. This affects the speed with which the op-amp can charge a capacitor connected to its output, and hence the highest signal frequency.

▪ OFFSET VOLTAGE

For an ideal op-amp, if $V_a = V_a$ (which is easily obtained by short circuiting the input terminals), $V_0 = 0$. In real devices, this is not exactly true, and a voltage $V_{0,\,off} \neq 0$ will occur at the output for shorted inputs. Since $V_{0,\,off}$ is usually directly proportional to gain, the effect can be more conveniently described in terms of input offset voltage $V_{in,\,off}$, defined as the differential input voltage needed to restore $V_0 = 0$ in the real device. For MOS op-amps, $V_{in,\,off}$ is typically $\pm$ 2 to 10mV. This effect can be modeled by a voltage source of value $V_{in,\,off}$ in series with one of the input leads of the op-amp as shown in Fig. 1.5:

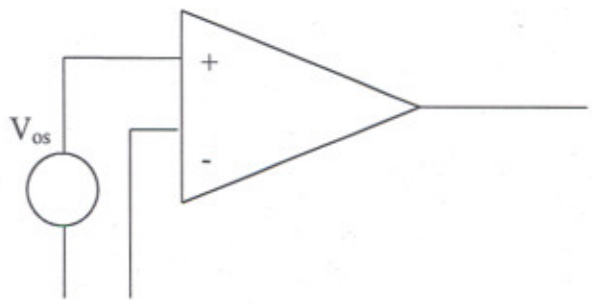


Figure 1.5: Offset voltage at the input of op-amp

This offset voltage can further be divided into two groups:-

- Systematic offset
- Random offset

Systematic Offset

It depends upon circuit architecture

$$V_{os} = V_{os1} + \frac{V_{os2}}{A_1}$$

Random offset

This is caused by components mismatch used in pairs.

- **Noise**

MOS transistor generates noise, which can be described in terms of an equivalent current source in parallel with the channel of the device.

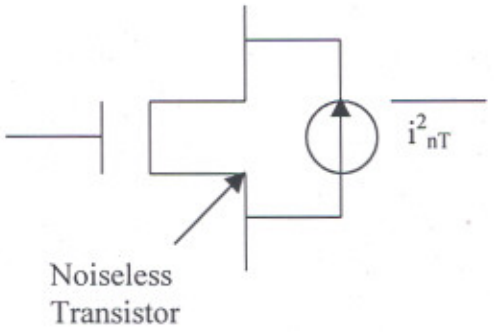


Figure 1.6: Equivalent model for noise in a MOSFET

The noisy transistor in an op-amp give rise to a noise voltage V_{on} at the output of the op-amp; this can again be modeled by an equivalent voltage source $V_n = V_{on}/A$ at the op-amp input. Unfortunately, the magnitude of this noise is relatively high, especially in low frequency band, where the flicker noise of the input device is high (in the MOS transistor,

extra electron energy states exists at the boundary between the Si and SiO_2. These can trap and help release electrons from the channel, and hence introduce noise, which is called flicker noise. Since the process is relatively slow, most of the noise energy will be at low frequencies); it is about 10 times the noise occurring in an op-amp fabricated in bipolar technology. In a wide band (in the range 10Hz to 1MHz), the equivalent input noise source is usually on the order of 10 to 50μV achievable for low noise bipolar op-mps.

- **POWER DISSIPATION**

Power consumption Pc is the amount of quiescent power ($V_{input} = 0$) that must be consumed by the op-amp in order to operate properly. Ideal op-amps require no dc power dissipated in the circuit; real ones do. Typical values for a CMOS op-amp range from 0.25 to 10mW dc power drain.

As in present day electronic systems a basic building block is the op-amp therefore, a better understanding of the characteristics of op-amps and their importance to overall circuit operation is essential.

2. FOLDED CASCODE CMOS OTA

2.1 INTRODUCTION

The operational transconductance amplifier (OTA) is basically an op-amp without output buffer. An OTA without buffer can only drive loads. An OTA can be defined as an amplifier where all nodes are low impedance except the input and the output nodes. The transconductance of the OTA is set by the transconductance of the input differential amplifier. A useful feature of the OTA is that its transconductance can be adjusted by the bias current. Filters made using the OTA can be tuned by changing the bias current labeled as I_{bias} in fig. 2.1. The symbol for the OTA is shown in fig. 2.1.

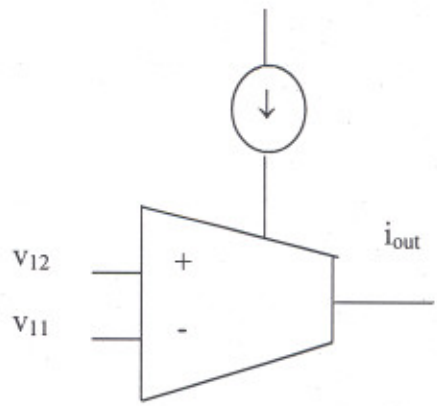


Fig. 2.1. Symbol of an OTA

OTA shown in fig. 2.2 was developed to improve the input common mode range and power supply rejection of two stage op-amps. The folded cascode does not required perfect balance of currents in the differential amplifier because excess dc current can flow into or out of the current mirror. Because the drains of M1 & M2 are connected to the drains of M4 & M5, the positive input common mode voltage is achieved. The bias current I_3, I_4 & I_5 of the folded-cascode OTA should be designed so that the dc current in the cascode current mirror never goes to zero. Suppose V_{in} is large enough so that M1

is on and M2 is off. Then, all of I_3 flows through M1 & none through M2, resulting in $I_1=I_3$ & $I_2 = 0$. If I_4 & I_5 is not greater than I_3, then the current I_6 will be zero. To avoid this, the values of I_4& I_5 are normally between the values of I_3& $2I_3$.

The small signal differential input voltage gain of the folded cascode op-amp is shown in fig. 2.3. The resistances designated as R_A & R_B are the resistances looking into the sources of M6 & M7, respectively.

$$R_A = \frac{r_{ds6} + R_2 + \dfrac{1}{g_{m10}}}{1 + g_{m6} r_{ds6}} \approx \frac{1}{g_{m6}}$$

$$R_B = \frac{r_{ds7} + R_9}{1 + g_{m7} r_{ds7}} \approx \frac{R_9}{g_{m7} r_{ds7}}$$

where

$$R_9 = g_{m9} r_{ds9} r_{ds11}$$

The small signal voltage transfer function can be found as follows. The current i_{10} is written as

$$i_{10} = \frac{-g_{m1}\left(r_{ds1} \| r_{ds4}\right) v_{in}}{2\left(R_A + \left(r_{ds1} \| r_{ds4}\right)\right)} = \frac{-g_{m1} v_{in}}{2}$$

and the current i_7 can be expressed as

$$i_7 = \frac{g_{m2} v_{in}}{2\left(1 + \dfrac{R_9 (g_{ds2} + g_{ds5})}{g_{m7} r_{ds7}}\right)} = \frac{g_{m2} v_{in}}{2(1+k)}$$

Typical values of k are greater than one.

$$k = \frac{R_9 (g_{ds2} + g_{ds5})}{g_{m7} r_{ds7}}$$

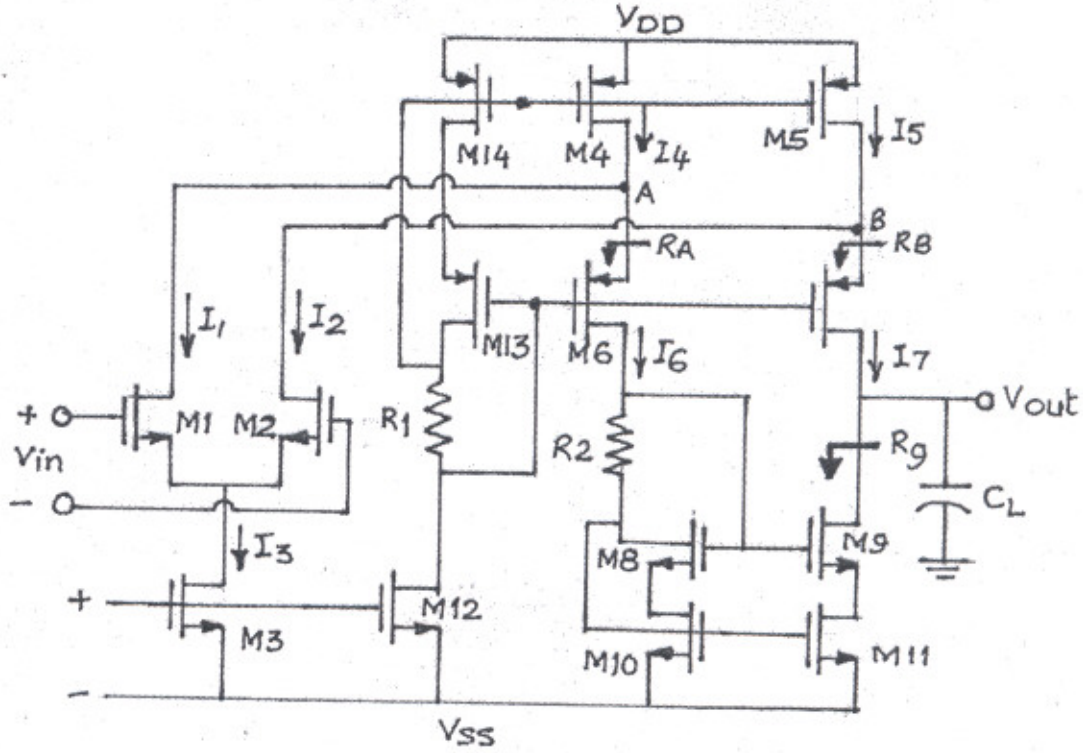


Fig2.2 Practical Version of OTA

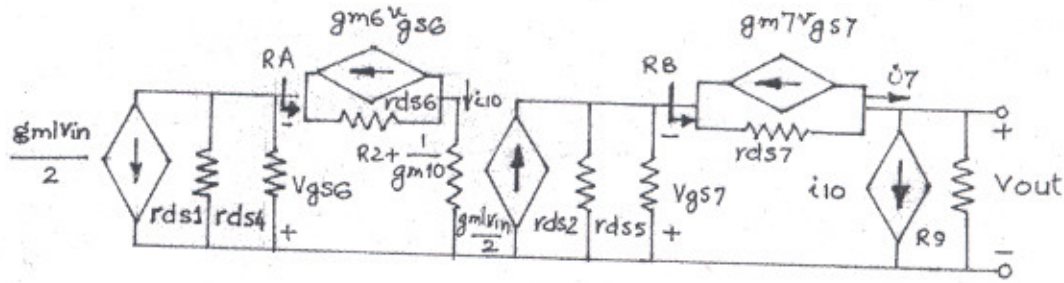


Fig 2.3 Small signal model of an OTA

The output voltage v_{out} is equal to the sum of i_7 & i_{10} flowing through R_{11}. Thus,

$$\frac{v_{out}}{v_{in}} = \left(\frac{g_{m1}}{2} + \frac{g_{m2}}{2(1+k)} \right) R_{11} = \left(\frac{2+k}{2+2k} \right) g_{m1} R_{11}$$

where the output resistance, R_{11}, is given as

$$R_{11} \approx g_{m9} r_{ds9} r_{ds11} \left\| \left(g_{m7} r_{ds7} \left(r_{ds2} \| r_{ds5} \right) \right) \right.$$

3. DESIGN PROCEDURE FOR FOLDED CASCODE OTA

3.1. NECESSARY PARAMETERS:

The following design procedure assumes that specification for the following parameters are given:

- Gain at dc (A_v)
- Unity gain bandwidth (GB)
- Input common-mode range [V_{in} (min)) and V_{in} (max)]
- Load capacitance (C_L)
- Slew rate (SR)
- Output voltage swing (V_{out} (max) and V_{out} (min)))
- Power Dissipation (P_{diss})

3.2. DESIGN STEPS:

1. Choose the smallest design device length that will keep the channel modulation parameter λ constant and give good matching for current mirrors.

2. Determine the value for the tail current I_3 for the largest of the two values.

$$I_3 = SR*C_L$$

3. Determine the value of bias current in the output cascodes. Avoid zero current in the cascodes.

$$I_4 = I_5 = 1.2\ I_3 \text{ to } 1.5\ I_3$$

4. Design for S_5 and S_7 from the maximum output voltage.

Let $S_4 = S_{14} = S_5 = S_{13}$ and $S6 = S_7$

$$S_5 = \left(\frac{W}{L}\right)_5 = \frac{2.I_5}{K_p} * (V_{sd5})^2$$

$$S_7 = \left(\frac{W}{L}\right)_7 = \frac{2.I_7}{K_p} * (V_{sd7})^2$$

where

$$V_{sd5}(sat) = V_{sd7}(sat) = \frac{V_{dd} - V_{out}(max)}{2}$$

5. Design for S_{11} and S_9 from the minimum output voltage.

Let $S_{10} = S_{11}$ and $S_8 = S_9$

$$S_{11} = \left(\frac{W}{L}\right)_{11} = \frac{2.I_{11}}{K_n} * (V_{ds11})^2$$

$$S_9 = \left(\frac{W}{L}\right)_9 = \frac{2.I_9}{K_n} * (V_{ds9})^2$$

where

$$V_{ds9}(sat) = V_{ds11}(sat) = \frac{V_{out}(min) - |V_{ss}|}{2}$$

6. Calculation of the resistances R_1& R_2.

$$R_1 = \frac{V_{sd13}(sat)}{I_{12}}$$

$$R_2 = \frac{V_{sd8}(sat)}{I_6}$$

7. Design of S_1 & S_2 from unity-gain bandwidth and load capacitor C_L.

$$S_1 = S_2 = \frac{GB^2.C_L{}^2}{K_n.I_3}$$

8. Design of S_3 from minimum input common mode voltage

$$S_3 = \left(\frac{W}{L}\right)_3 = \frac{2.I_3}{K_n\left[V_{in}(min) - V_{ss} - \sqrt{\frac{I_3}{K_n.S_1}} - V_{t1}\right]^2}$$

9. Design of S_4 & S_5 from maximum input common mode voltage

$$S_4 = S_5 = \frac{2.I_4}{K_p[V_{dd} - V_{in}(max) + V_{t1}]^2}$$

We need to check that the values of S_4 & S_5 are large enough to satisfy the maximum input common mode voltage.

10. Calculate the small signal, differential-input voltage gain

$$A_v = \left(\frac{2+k}{2+2k}\right).g_{m1}.R_{11}$$

11. Calculate the power dissipation

$$P_{diss} = (V_{dd} - V_{ss})(I_3 + I_{12} + I_{10} + I_{11})$$

3.3. AN EXAMPLE OF A FOLDED-CASCODE OTA WITH THE FOLLOWING SPECIFICATIONS:

- Slew rate = 10V/μs
- The load capacitor is 10pF
- The maximum and minimum output voltages are ± 2V for ± 2.5V power supplies
- The gain bandwidth is 7 MHz
- The minimum input common-mode voltage is –1.5V
- The maximum input common-mode voltage is 2.5V
- The differential voltage gain should be greater than 5000
- Power Dissipation should be less than 5mW

3.4. DESIGN STEPS FOR 3.3

1. $I_3 = SR*C_L$

   $= 10*10^6*10^{-11} = 100\mu A$

2. $I_4 = I_5 = 1.25*100*10^{-6}$

   $= 125\mu A$

3. Let $S_4 = S_{14} = S_5$ and $S_{13} = S_6 = S_7$

$$S_5 = S_4 = S_{14} = S_{13} = \frac{2*125*10^{-6}}{2.63544*10^{-5}(0.25)^2} = 151.78$$

$$S_6 = S_7 = \frac{2*75*10^{-6}}{2.63544*10^{-5}(0.25)^2} = 91.066$$

Where, $V_{sd5}(sat) = V_{sd7}(sat) = \frac{V_{dd} - V_{out}(max)}{2} = \frac{2.5-2}{2} = 0.25V$

4. Let $S_{10} = S_{11}$ and $S_8 = S_9$

$$S_8 = S_9 = S_{10} = S_{11} = \frac{2*75*10^{-6}}{6.322664*10^{-5}(0.25)^2} = 37.9586$$

Where, $V_{ds9}(sat) = V_{ds11}(sat) = \frac{V_{out}(min) - |V_{ss}|}{2} = \frac{-2+2.5}{2} = 0.25V$

5. $$R_1 = \frac{V_{sd13}(sat)}{I_{12}} = \frac{0.25V}{125\mu A} = 2000\Omega$$

$$R_2 = \frac{V_{sd8}(sat)}{I_6} = \frac{0.25V}{125\mu A} = 2000\Omega$$

6. $$S_1 = S_2 = \frac{GB^2 . C_L^{\ 2}}{K_n . I_3} = \frac{(14\pi . 10^6)^2 (10^{-11})^2}{6.322664 * 10^{-5} * 100 * 10^{-6}} = 30.5956$$

7.

$$S_3 = \left(\frac{W}{L}\right)_3 = \frac{100 * 10^{-6} * 2}{6.32664 * 10^{-5}\left[-1.5 + 2.5 - \sqrt{\frac{100 * 10^{-6}}{6.32664 * 10^{-5} * 30.5956}} - 0.62249\right]^2} = 140.092$$

8. $$S_4 = S_5 = \frac{2 * 125 * 10^{-6}}{2.63544 * 10^{-5}[2.5 - 2.5 + 0.62249]^2} = 10.2$$

We need to check that the values of S_4 & S_5 are large enough to satisfy the maximum input common mode voltage.

9. $$S_{12} = \frac{125}{100} * 140.092 = 175.115$$

10. $$P_{diss} = (2.5 - (-2.5)(100 + 125 + 75 + 75) = 1.875 mW$$

11. The small signal voltage requires the following values to evaluate

$$S_5, S_4, S_{14}, S_{13}; g_m = \sqrt{2 * 125 * 10^{-6} * 2.63544 * 10^{-5} * 151.78} = 1000 \mu S$$

$$g_{ds} = 125 * 10^{-6} * 0.01 = 1.25 \mu S$$

$$S_6, S_7; g_m = \sqrt{2 * 75 * 10^{-6} * 2.63544 * 10^{-5} * 91.066} = 600 \mu S$$

$$g_{ds} = 75 * 10^{-6} * 0.01 = 0.75 \mu S$$

$$S_8, S_9, S_{10}, S_{11}; g_m = \sqrt{2 * 75 * 10^{-6} * 6.322664 * 10^{-5} * 37.9586} = 600 \mu S$$

$$g_{ds} = 75 * 10^{-6} * 0.01 = 0.75\mu S$$

$$S_1, S_2 ; g_{m1} = \sqrt{2 * 50 * 10^{-6} * 6.322664 * 10^{-5} * 62.44} = 628\mu S$$

$$g_{ds} = 50 * 10^{-6} * 0.01 = 0.5\mu S$$

Thus,

$$R_9 \approx g_{m9} * r_{ds9} * r_{ds11} = 600\mu S * \frac{1}{0.75\mu S} * \frac{1}{0.75\mu S} = 1066.67M\Omega$$

$$R_{11} \approx (1066.67M\Omega) \| (600\mu S) \left[\frac{1}{0.75\mu S} \right] \left[\frac{1}{0.75\mu S} \| \frac{1}{1.25\mu S} \right] = 290.71M\Omega$$

$$k = R_9 \left(\frac{g_{ds2} + g_{ds4}}{g_{m7} r_{ds7}} \right) = \frac{1066.67M\Omega (0.5\mu S + 1.25\mu S)(0.75\mu S)}{600\mu S} = 2.3333$$

The small signal, differential-input voltage gain is

$$A_v = \left(\frac{2+k}{2+2k} \right) g_{m1} R_{11} = \left(\frac{2+2.3333}{2+4.6666} \right) * 628 * 10^{-6} * 290.71 * 10^{+6} = 118668 V/V$$

4. CAD TOOLS

The design-synthesis tool was developed using C language and validated using Tanner Tools.

4.1 DESIGN SYNTHESIS TOOL DEVELOPED

The design-synthesis tool was developed in C language. The various steps involved in the tool for designing and synthesizing of the folded-cascode OTA are explained below:

STEP 1

For folded-cascode OTA specifications are defined, which are required to be met by designed circuit. The parameters considered are given in Table 4.1

STEP 2

DC bias conditions are set in this step, which decides the quiescent of the op-amp. Quiescent power is the minimum power required by the design to keep the all MOS transistors in saturation region.

STEP 3

Using defined specifications in fixed equation mentioned in chapter 3, section 3.3 for designing of the op-amp, width/length (W/L or S) ratio of various transistors is calculated in this step. These W/L ratios are used to calculate the width and lengths of the various transistors by multiplying the W/L ratio with the device length.

STEP 4

In this step, T-spice compatible files are generated. These files are used for doing various analysis like AC analysis, Slew Rate, $PSRR^{+}$, $PSRR^{-}$, Common mode gain, Transfer function, etc. Each T-spice compatible file contains mainly three things, first, Design description of the folded-cascode OTA, secondly, include model file and finally simulation commands related with the analysis for which the file is made for.

Table 4.1:Input Parameters for folded-cascode OTA

CONSTRAINTS	TYPICAL VALUE
Power Supply	±2.5V
Open Loop Gain	>5000
GBW (MHz)	7 MHZ
Slew Rate	10 V/us
V_{out} range (V)	±2V
ICMR (V)	-1.5 to 2.5
Load Capacitance	10pf
Minimum Device Length	2 um
Power Dissipation	<5mW

4.2 Tanner Tools

Tanner tool is a VLSI Design Tool used for analysis and simulation of electronic circuits. Tanner tool consists of many Engine Machines. The following engine machines were used in the current analysis.

1. S-EDIT (Schematic Edit)
2. T-EDIT (Simulation Edit)
3. W-EDIT (Waveforms Edit)

Using these engine tools, spice program provides facility to the user to design & simulate new ideas in Analog Integrated Circuits before going to the time consuming & costly process of chip fabrication.

SCHEMATIC EDIT TOOL (S-EDIT)

S-Edit is hierarchy of files, modules & pages. It introduces symbol & schematic modes. S-Edit provides the facility of:

1. Beginning a design.
2. Viewing, drawing & editing of objects.
3. Design connectivity.
4. Properties, net lists & simulation.
5. Instance & browse schematic & symbol mode.

S-Edit has two viewing modes:

1) **Schematic Mode:** to create or view a schematic, we operate in schematic mode.

2) **Symbol Mode:** it represents symbol of a larger functional unit such as operational amplifer.

WAVEFORM-EDIT

The ability to visualize the complex numerical data resulting from VLSI circuit simulation is critical to testing, understanding & improving these circuits. W-Edit is a waveform viewer that provides ease of use, power & speed in a flexible environment designed for graphical data representation.

Numerical data is input to W-Edit in the form of plain or binary text files. Header & Comment information supplied by T-Spice is used for automatic chart configuration. Runtime update of results is made possible by linking W-Edit to a running simulation in T-Spice.W-Edit saves data with chart, trace, axis & environment settings in files with the WDB (W-Edit Database).

CIRCUIT SIMULATOR (T-SPICE)

The heart of T-Spice operation is the input file (also known as the circuit description, the net list & the input deck). This is a plain text file that contains the device statement & simulation commands, drawn from the SPICE circuit description language with which T-Spice constructs a model of the circuit to be simulated. Input files can be created and modified with any text editor.

T-Spice is a tool used for simulation of the circuit. It provides the facility of

1. Design Simulation

2. Simulation Commands
3. Device Statements
4. User-Designed External Models
5. Small Signal & Noise Models

T-Spice uses Kirchoff's Current Law (KCL) to solve circuit problems. To T-Spice, a circuit is a set of devices attached to nodes. The voltage at all nodes represents the circuit state. T-Spice solves for a set of node voltage that satisfied KCL (implying that sum of currents flowing into each node is zero).

In order to evaluate whether a set of node voltages is a solution, T-Spice computers and sums all the current flowing out of each device into nodes connected to it (its terminals). The relationship between the voltages at device terminals and the currents through the terminal is determined by the device model for a resistor of resistance R is

$$I = \Delta V / R$$

Where ΔV represents the voltage difference across the device.

1. D.C. Analysis - used for DC operating point calculations.
2. Transient Analysis - T-Spice solves for a circuit's behaviour over sometime interval

.dc → performs dc transfer analysis to study the voltage or current at one set of points in a circuit as a function of voltage or current at another complement from a specified file.
.Include → includes the parameters of analog component from a specified file.

After creating files in step 4 above, these files are simulated using Tanner tools and verified for the specifications. If the specifications are met then OK otherwise again files are created by changing some parameters in the next iteration of the program. Again synthesized circuit is verified using the same tool. So procedure is iterated till the optimum result come.

5. RESULTS & DISCUSSIONS

In the present work, the performance of folded-cascode OTA is examined by carrying out simulation studies. Schematic of CMOS folded-cascode OTA is shown in fig.5.1(a) and fig 5.1(b) shows the model file ml2_125.md.

5.1 OFFSET VOLTAGE

Offset voltage is defined as the differential input voltage needed to restore output zero in the real device. So before we start simulations it is necessary to check for the offset voltage of the configuration and do necessary compensation for that to get the actual results from the simulations.

Fig. 5.1.1 shows the netlist generated through design-synthesis tool

Fig. 5.1.2 shows the transfer function for folded-cascode OTA, with offset.

5.2 AC ANALYSIS

Simulation results for Unity GBW, Phase Margin and DC Gain are presented.

Fig. 5.2.1 shows netlist generated through design-synthesis tool

Fig.5.2.2 shows the AC analysis at 7 MHz Design GBW and 10-pf load.

- **Using different frequencies**

Design GBW (MHz)	Obtained Unity GBW (MHz)	Phase Margin (degrees)	DC Gain (dB)	Slew rate (V/us)
10	0.46	90.13	34.85	1.43
9	0.90	90.80	36.93	1.79
8	1.23	91.88	42.36	2.38
7	2.64	92.26	49.14	3.85
6	2.2	43.51	2.73	6.25
5	6.71	85.73	18.51	4.76
4	7.32	67.74	8.12	1.96
3	1.27	90.89	36.63	3.33
2	0.16	88.05	25.64	0.217

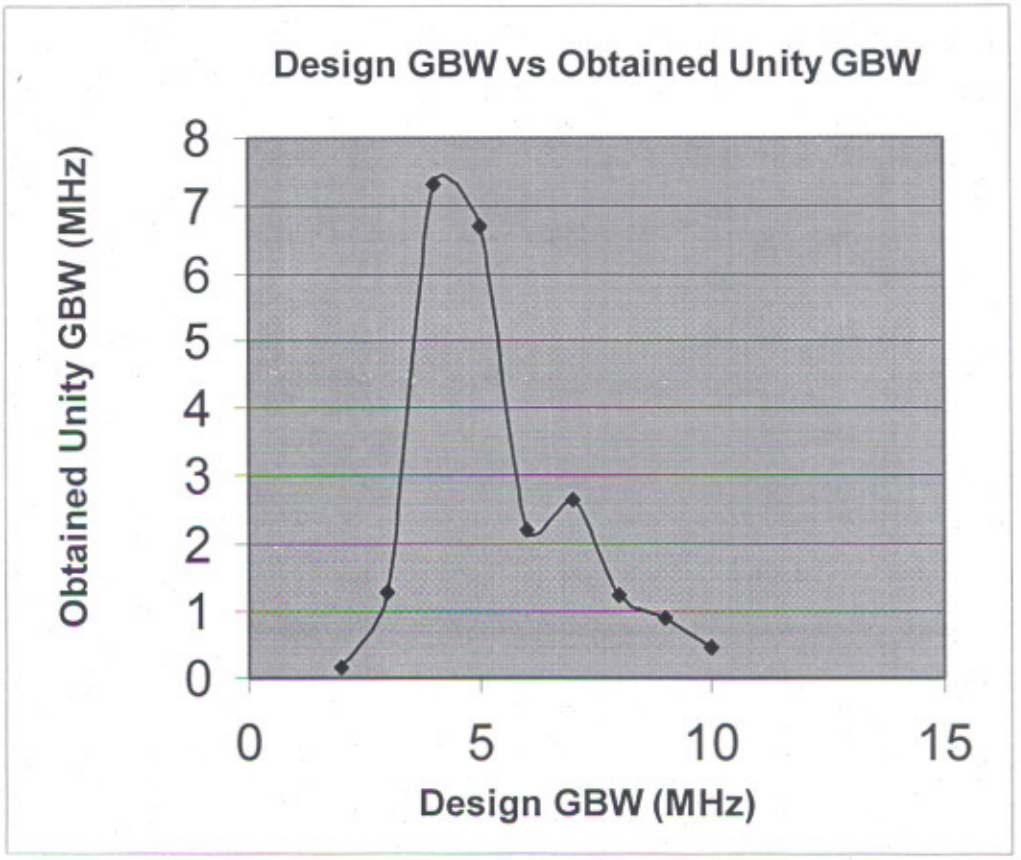


Fig.5.2.3 Obtained Unity GBW at different design GBW

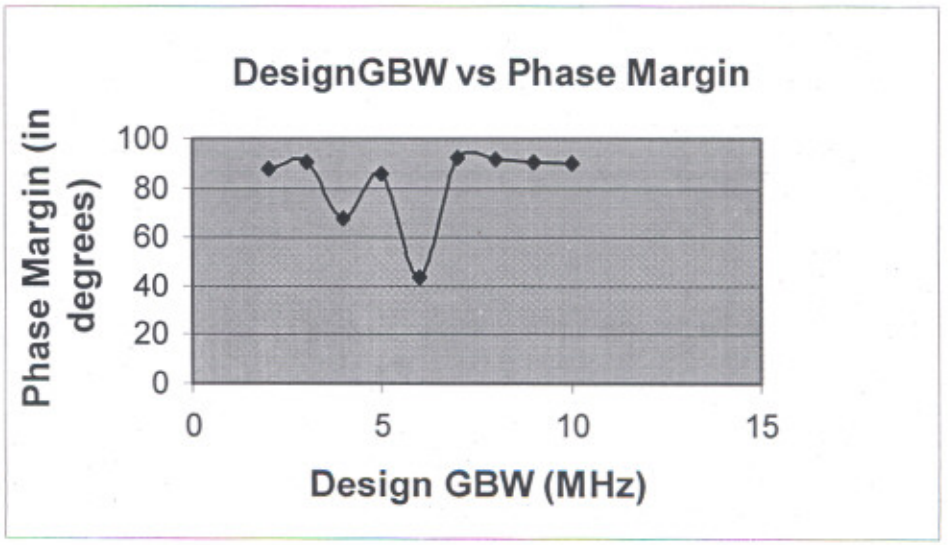


Fig 5.2.4 Phase Margin at different design GBW

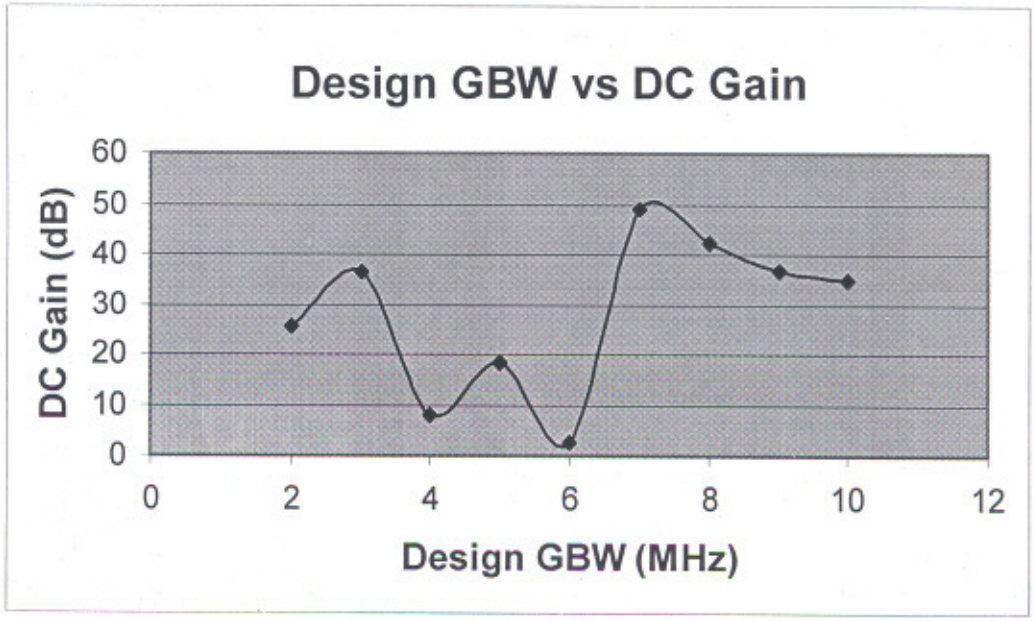


Fig. 5.2.5 DC Gain at different design GBW

From the above graphs it was found that

- The obtained unity gain bandwidth (GBW) is comparable to designed gain bandwidth within the range 3 MHz to 7 MHz.

- The Phase Margin is almost constant at all design GBWs but at 4 MHz and 6 MHz the phase margins are 43.51° and 67.71° respectively.

- DC Gain is small at 4 to 6 MHz and maximum at 7 MHz among all the designs.

- **Using different loads**

A unity GBW of 7 MHz was selected and analysis was done for varying load capacitance. The results are shown in Table 5.2.2:

Load (pf)	Unity GBW (MHz)	Phase Margin (In degrees)	DC Gain (dB)	Slew Rate (V/us)	Common Mode Gain (dB)
100	2.52	92.58	49.42	3.85	-76.98
75	2.52	92.58	49.60	3.85	-75.28
50	2.52	91.88	49.59	3.85	-72.72
25	2.45	91.92	49.55	3.85	-69.23
12.5	2.52	92.70	49.54	3.85	-66.73
10	2.60	92.74	49.58	3.85	-64.61
8	2.60	92.78	49.54	3.85	-64.18
5	2.52	92.21	49.78	3.85	-62.05
2.5	2.67	92.57	44.76	3.85	-57.78
1	2.67	93.17	44.20	3.85	-51.59

Table 5.2.2: Values of Obtained Unity GBW, Phase Margin, DC Gain, Slew Rate and Common Mode Gain at varying load

From the above table we found that the design is stable at different loads varying from 1pf to 100pf.

- Obtained Unity GBW, Phase Margin, Slew Rate is almost same at different loads.
- Common Mode Gain is decreasing as load varies from 100pf to 1pf.
- DC Gain varies from 44.20 to 49.42dB. It is about 49 dB from 5pf to 100pf and at 1pf and 2.5pf it decreases to around 44 dB.

The graphs drawn for Obtained Unity GBW, Phase Margin and DC Gain for varying loads and shown in figures 5.2.6,5.2.7 and 5.2.8.

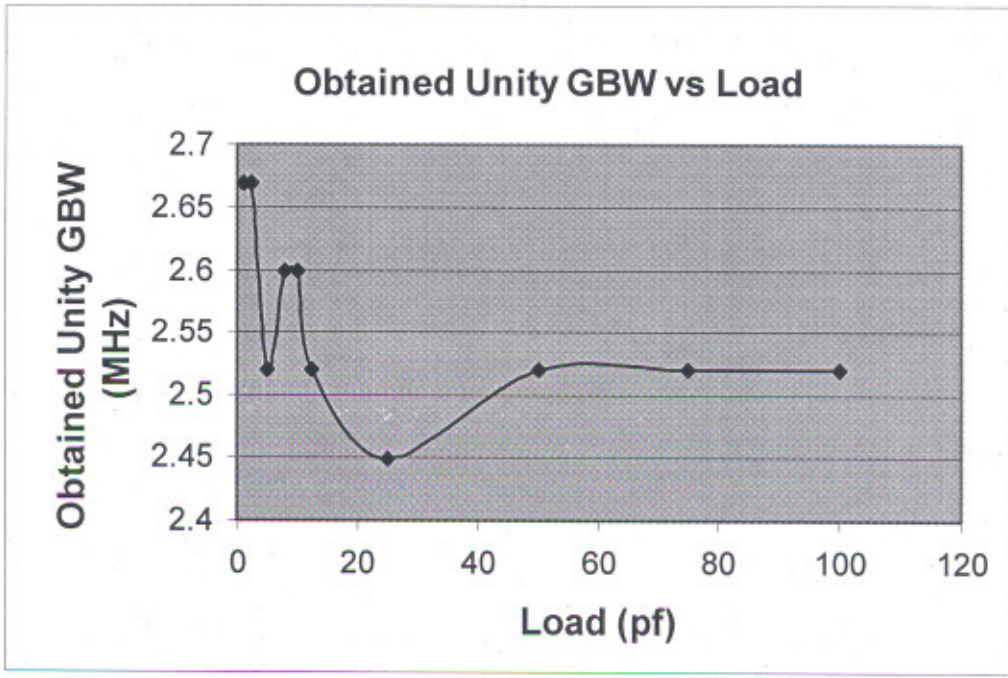


Fig 5.2.6 Obtained Unity GBW with varying loads

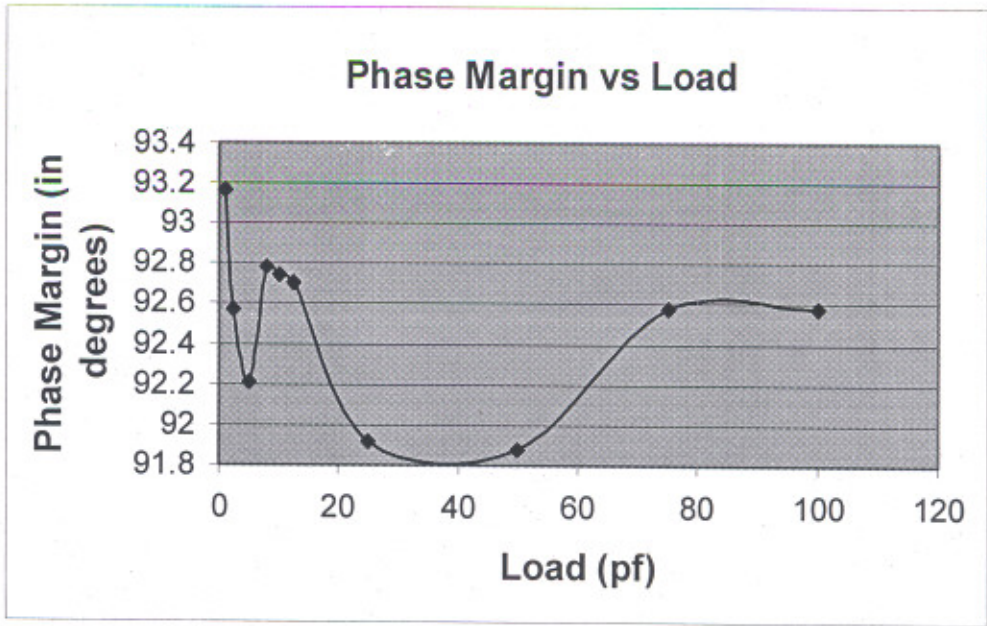


Fig 5.2.7 Phase Margin with varying Loads

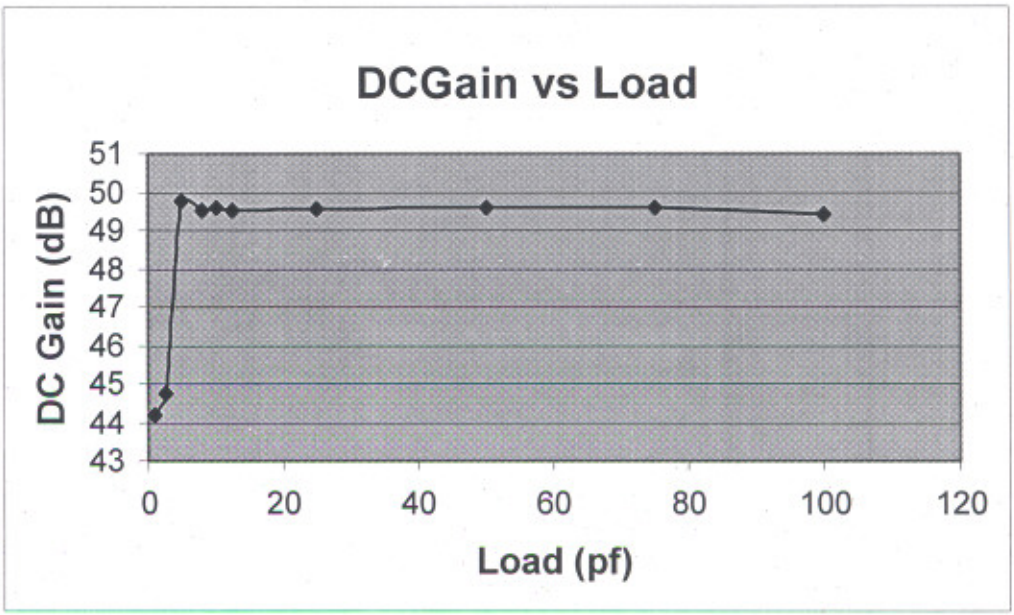


Fig 5.2.8 DC Gain with varying loads

5.3 OUTPUT SWING

Output voltage swing is the range over which the output voltage can vary without excessive distortion. Infact the output voltage swing gives the values of the maximum positive and negative values above which the transistor will go out of saturation.

Folded-cascode OTA gives an output swing of at positive excursion and at negative excursion.

Fig 5.3.1 shows netlist generated through design-synthesis tool

Fig 5.3.2 shows Output Swing for folded-cascode OTA

5.4 SLEW RATE

The maximum rate of change dv_0/dt is called the slew rate. For the large input step voltage, some transistors in the op-amp may be driven out of their saturation region or cut-off completely. As a result, the output will follow the input at slower finite rate.

Fig 5.4.1 shows netlist generated through through design-synthesis tool

Fig 5.4.2 shows Slew Rate for folded-cascode OTA

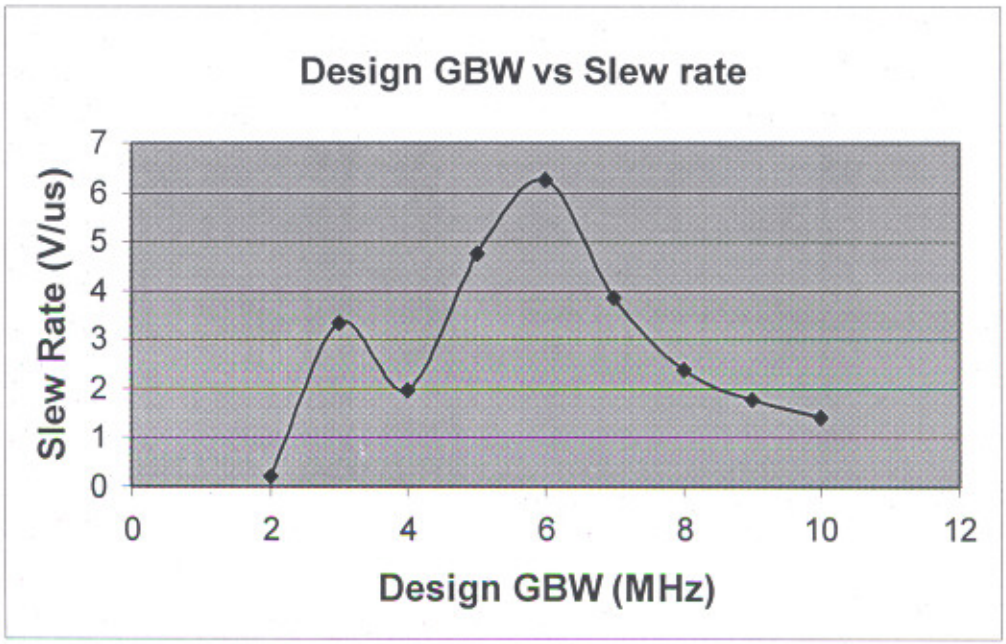


Fig 5.4.3 Slew Rate varying with design GBW

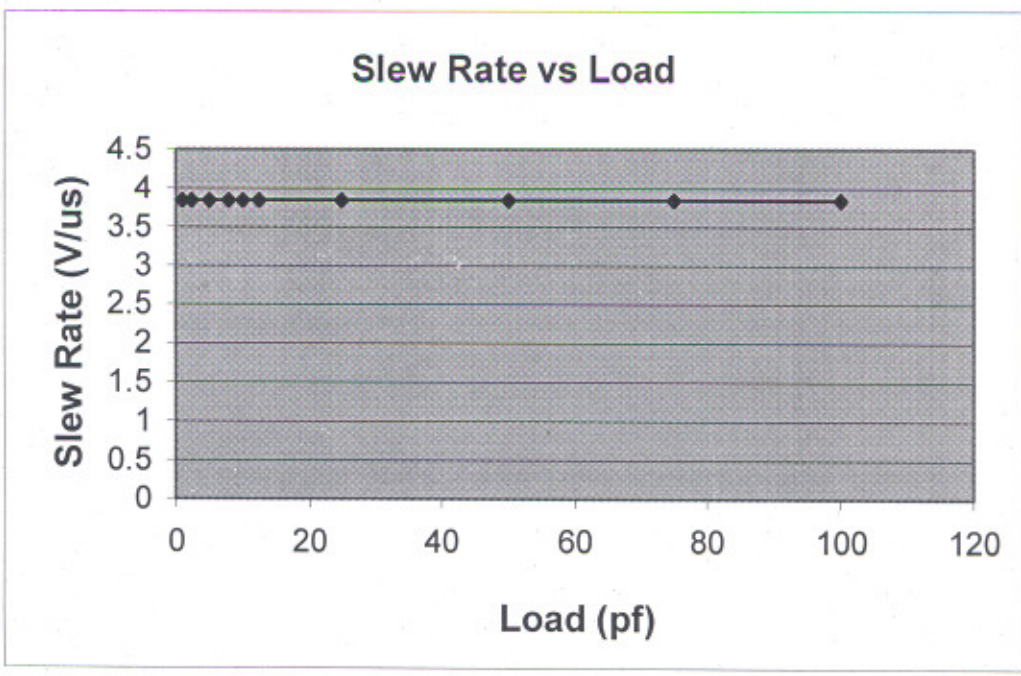


Fig 5.4.4 Slew Rate varying with loads

- Slew rate is changing for different design GBW from fig 5.4.3

- Slew rate is constant over the entire range of load capacitors from fig. 5.4.4

5.5 POWER SUPPLY REJECTION RATIO (PSRR)

This is also called *supply voltage rejection ratio* (SVRR) *power supply sensitivity* (PSS). If a power supply voltage contains an incremental component v due to noise, hum and so on, a corresponding voltage A_{pv}, will appear at the op-amp output. The PSRR is defined as A_D/A_P, where A_D = A is the differential gain. It is common to express the PSRR in decibels; then PSRR = 20 $\log_{10}$ (A_D/A_P). Usual PSRR value range from 60 to 80 dB for the op-amp alone.

At 7MHz, taking different values of signal voltage magnitude the values of $PSRR^+$ (noise on Vdd rail) and $PSRR^-$ (noise on Vss rail) were recorded in Table 5.5.1

Design GBW = 7MHz		
Signal Voltage Magnitude (Volts)	**$PSRR^+$ (dB)**	**$PSRR^-$ (dB)**
0.1	70.00	22.58
0.09	70.85	23.67
0.08	71.98	24.72
0.07	72.89	25.90
0.06	74.14	27.18
0.05	76.20	28.67
0.04	78.41	30.78
0.03	80.38	33.25
0.02	83.90	36.77
0.01	89.82	42.81

Table 5.5.1 $PSRR^+$ & $PSRR^-$ with varying signal voltage at 7 MHz

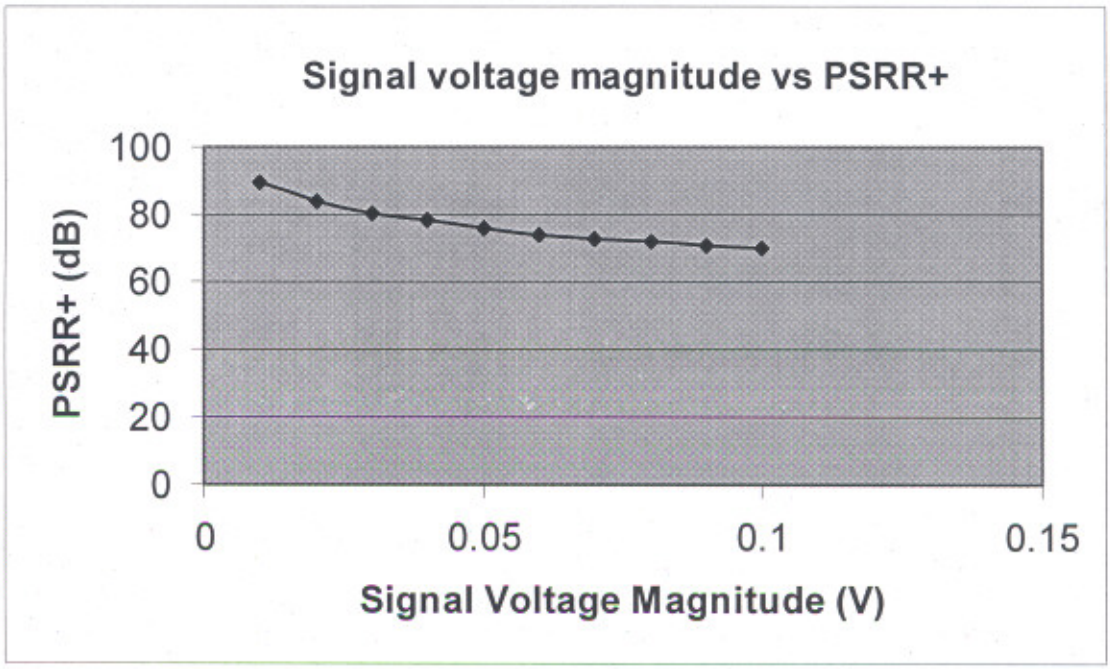


Fig 5.5.1 PSRR^{+} with varying signal voltage magnitude at 7MHz

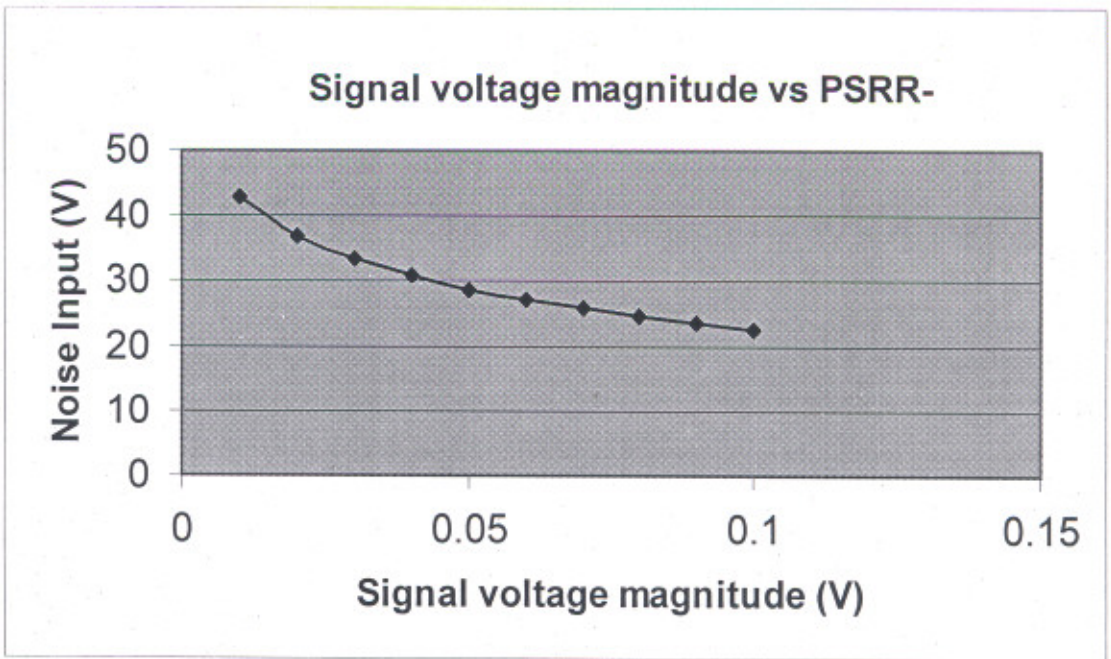


Fig 5.5.2 PSRR^{-} with varying signal voltage magnitude at 7MHz

After this a value of signal voltage magnitude was chosen arbitrarily and by varying the design GBW the values of $PSRR^+$ and $PSRR^-$ were recorded in Table 5.5.2

Signal Voltage Magnitude (Volts) = 0.05V		
Design GBW (MHz)	**$PSRR^+$ (dB)**	**$PSRR^-$ (dB)**
1	66.29	43.48
2	80.77	27.35
3	86.58	27.09
4	24.24	19.49
5	38.70	27.00
6	26.78	26.64
7	76.20	28.67
8	77.63	26.71
9	60.44	26.13
10	66.46	26.73

Table 5.5.2 $PSRR^+$ & $PSRR^-$ with varying design GBW at 0.05V

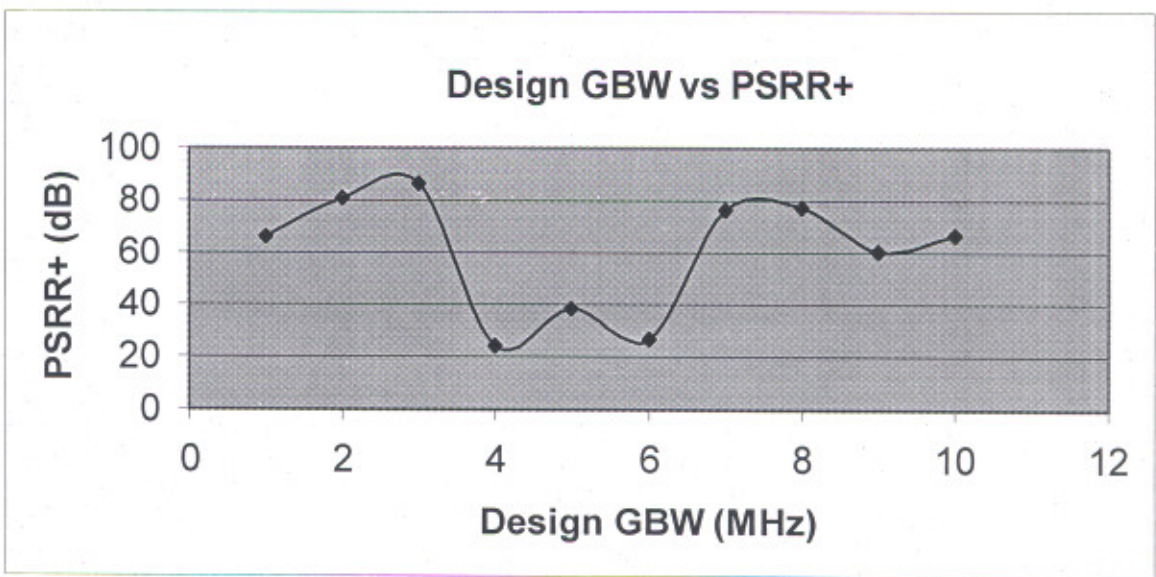


Fig 5.5.3 $PSRR^+$ for different design GBW at 0.05V

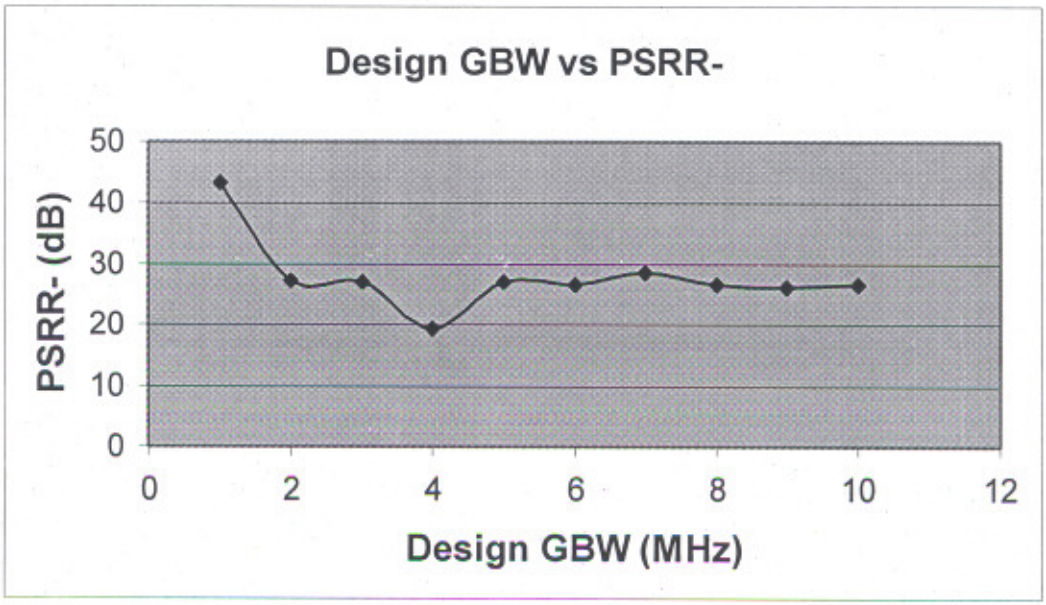


Fig 5.5.4 PSRR$^-$ for different design GBW at 0.05V

Fig 5.5.5 shows netlist generated through design synthesis tool for PSRR$^+$.

Fig 5.5.6 shows PSRR$^+$ (dB) at 7 MHz and 0.05 V.

Fig 5.5.7 shows netlist generated through design synthesis tool for PSRR$^-$.

Fig 5.5.8 shows PSRR$^-$ (dB) at &MHz and 0.05 V.

STEP 5.6 COMMOM MODE GAIN

Common Mode Gain is the open loop voltage gain with a small signal applied to both the input terminals.

Fig 5.6.1 shows netlist generated through design synthesis tool

Fig 5.6.2 shows Common Mode Gain (dB) at 7 MHz

From table 5.2.2 we obtained Common Mode Gain versus load, which is not same for different loads. It is decreasing with the increase in load.

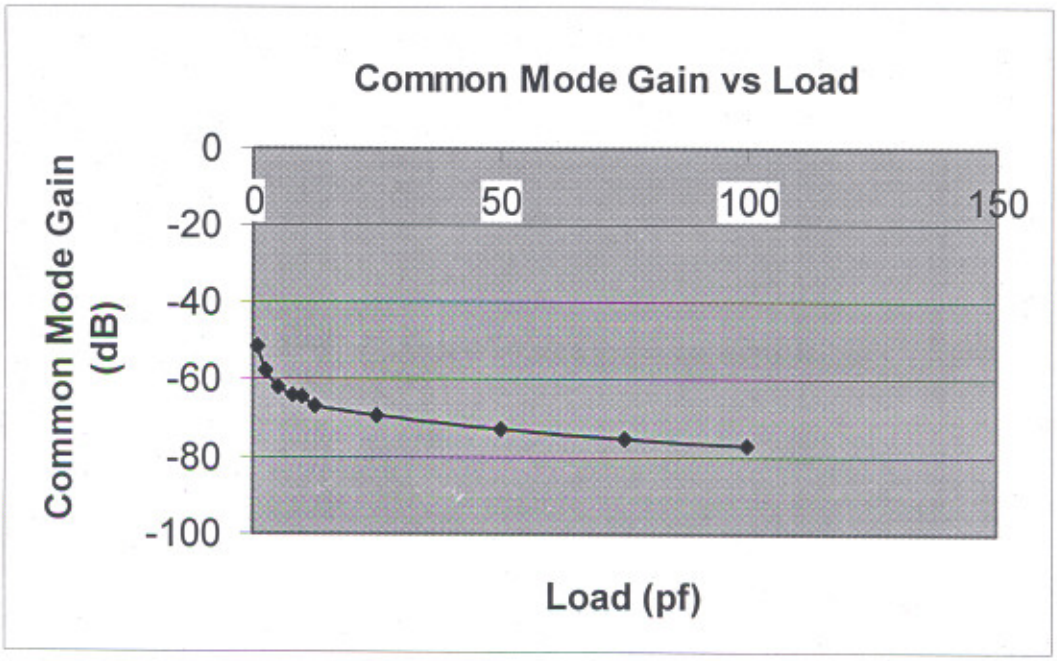


Fig 5.6.3 Common Mode Gain with varying loads

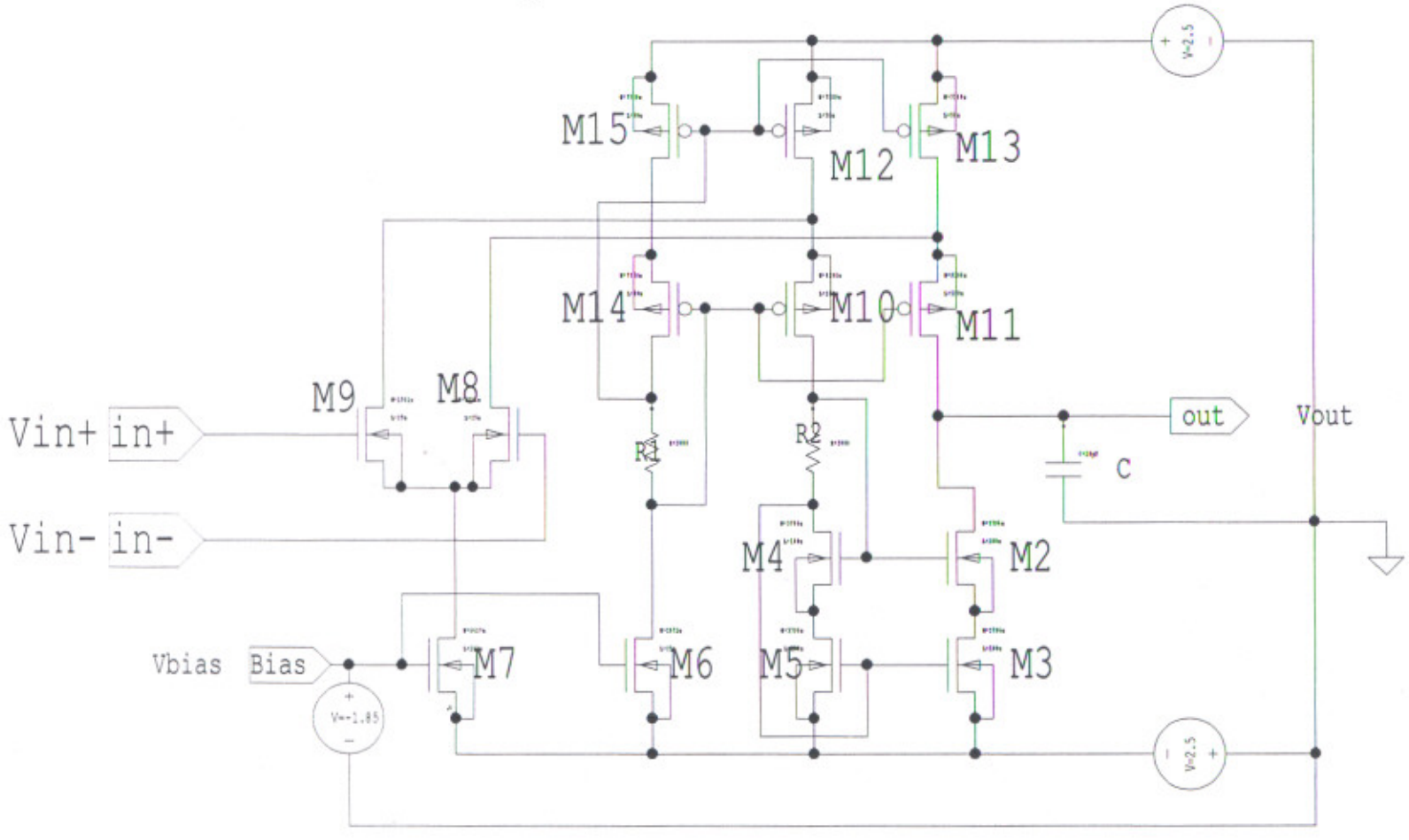


Fig 5.1(a) Schematic of folded cascode OTA

```
**********************************************************
**
** MCNC 1.25um CMOS Process
** Nominal Level 2 MOSFET Parameters
** 2/26/87
**
**********************************************************

.model nmos nmos
+    Level=2            Ld=0.0u          Tox=225.00E-10
+    Nsub=1.066E+16     Vto=0.622490     Kp=6.326640E-05
+    Gamma=.639243      Phi=0.31         Uo=1215.74
+    Uexp=4.612355E-2   Ucrit=174667     Delta=0.0
+    Vmax=177269        Xj=.9u           Lambda=0.01
+    Nfs=4.55168E+12    Neff=4.68830     Nss=3.00E+10
+    Tpg=1.000          Rsh=60           Cgso=2.89E-10
+    Cgdo=2.89E-10      Cj=3.27E-04      Mj=1.067
+    Cjsw=1.74E-10      Mjsw=0.195

.model pmos pmos
+    Level=2            Ld=.03000u       Tox=225.000E-10
+    Nsub=6.575441E+16  Vto=-0.63025     Kp=2.635440E-05
+    Gamma=0.618101     Phi=.541111      Uo=361.941
+    Uexp=8.886957E-02  Ucrit=637449     Delta=0.0
+    Vmax=63253.3       Xj=0.112799u     Lambda=0.01
+    Nfs=1.668437E+11   Neff=0.64354     Nss=3.00E+10
+    Tpg=-1.00          Rsh=150          Cgso=3.35E-10
+    Cgdo=3.35E-10      Cj=4.75E-04      Mj=.341
+    Cjsw=2.23E-10      Mjsw=0.307
```

Fig 5.1(b) Model file ml2_125.md

```
D:\pranav\offset.sp
Page 1

* SPICE netlist written by Manu Bansal
* Waveform probing commands
.probe
.options probefilename="Folded_cascode_OTA_offset.dat"
+ probesdbfile="c:\Folded_cascode_OTA_offset.sdb"
+ probetopmodule="offset"
* Main circuit: offset
C1 out Gnd 10pF
.include "D:\pranav\ml2_125.md"
M2 out N5 N13 N13 NMOS L=2u W=75u AD=66p Pd=24u AS=66p PS=24u
M3 N13 N6 N10 N10 NMOS L=2u W=75u AD=66p Pd=24u AS=66p PS=24u
M4 N6 N5 N7 N7 NMOS L=2u W=75u AD=66p Pd=24u AS=66p PS=24u
M5 N7 N6 N10 N10 NMOS L=2u W=75u AD=66p Pd=24u AS=66p PS=24u
M6 N9 BIAS N10 N10 NMOS L=2u W=351u AD=66p Pd=24u AS=66p PS=24u
M7 N11 BIAS N10 N10 NMOS L=2u W=281u AD=66p Pd=24u AS=66p PS=24u
M8 N3 in- N11 N11 NMOS L=2u W=61u AD=66p Pd=24u AS=66p PS=24u
M9 N2 in+ N11 N11 NMOS L=2u W=61u AD=66p Pd=24u AS=66p PS=24u
M10 N5 N9 N2 N2 PMOS L=2u W=182u AD=66p Pd=24u AS=66p PS=24u
M11 OUT N9 N3 N3 PMOS  L=2u W=182u AD=66p Pd=24u AS=66p PS=24u
M12  N2  N4 N14 N14 PMOS  L=2u W=303u AD=66p Pd=24u AS=66p PS=24u
M13  N3  N4 N14 N14 PMOS  L=2u W=303u AD=66p Pd=24u AS=66p PS=24u
M14  N4  N9 N1 N1 PMOS  L=2u W=303u AD=66p Pd=24u AS=66p PS=24u
M15  N1  N4 N14 N14 PMOS  L=2u W=303u AD=66p Pd=24u AS=66p PS=24u
R16 N4 N9 2000.0 TC=0.0,0.0
R17 N5 N6 3333.3 TC=0.0,0.0
v18 in+ in- 0.0  AC 0.0,0.0
v19 N14 Gnd 2.5
v20 Gnd N10 2.5
v21 Bias Gnd -1.85
.dc v18 -0.1 0.1 0.005
.print dc  v(out,gnd)
* End of main circit: offset
```

Fig 5.1.1 Netlist generated through design Synthesis tool

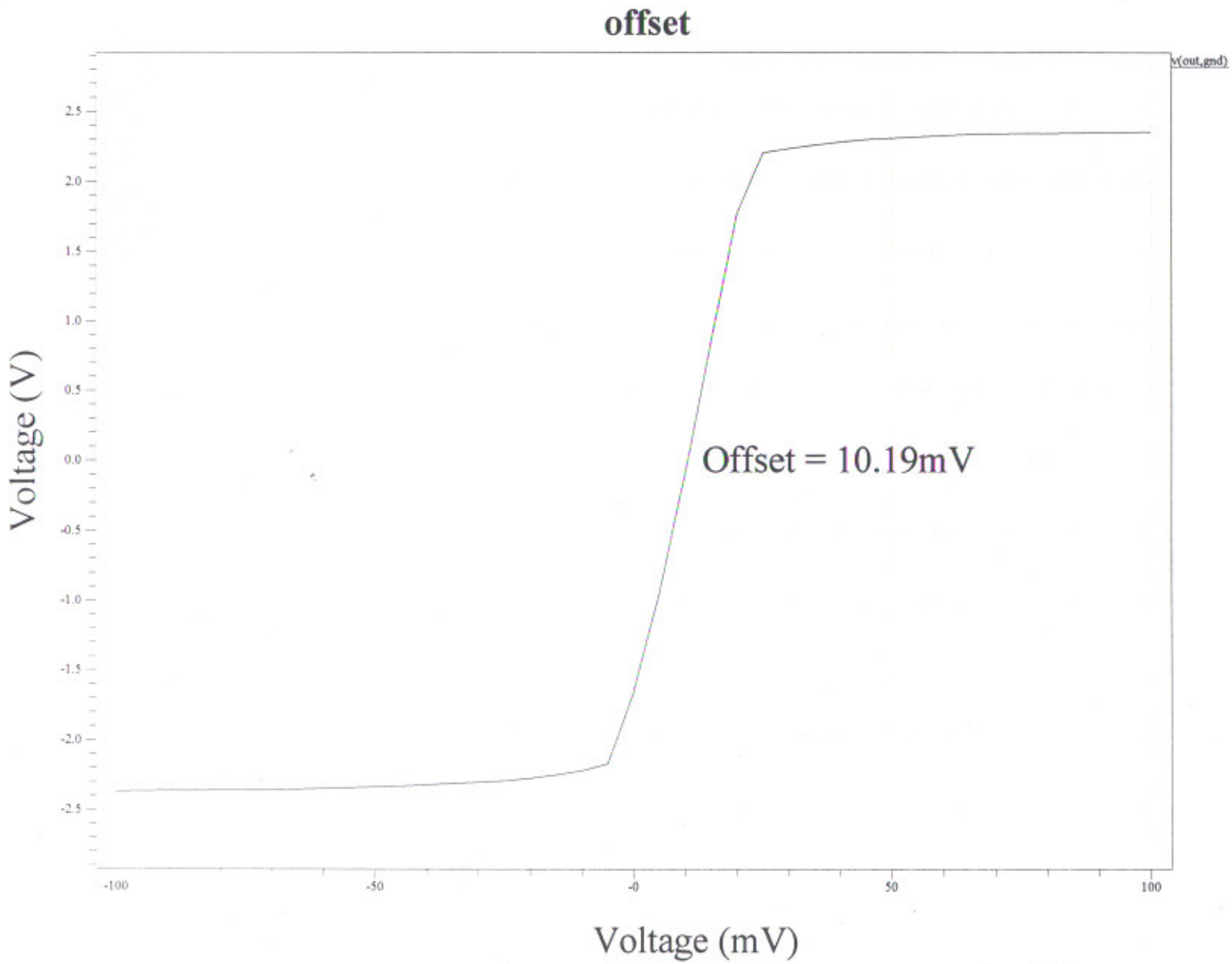
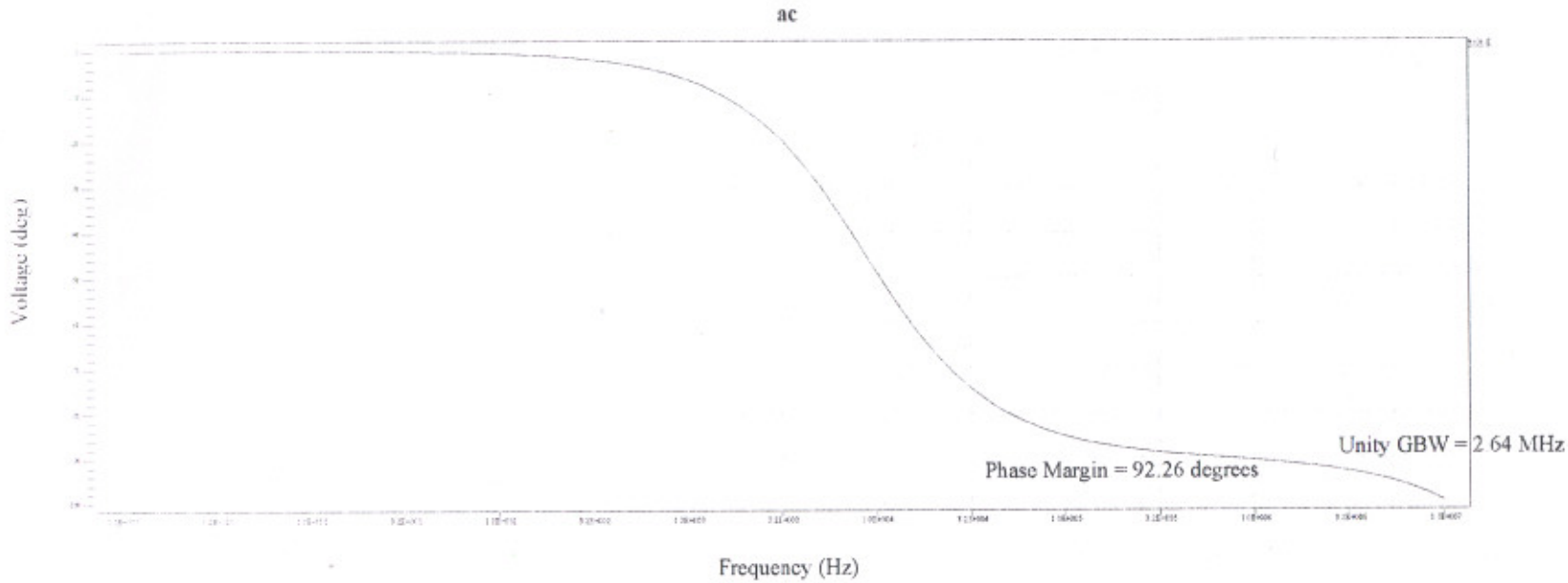


FIG. 5.1.2 Transfer function with offset of folded-cascode OTA

```
D:\pranav\ac.sp
Page 1

* SPICE netlist written by Manu Bansal
* Waveform probing commands
.probe
.options probefilename="Folded_cascode_OTA_ac.dat"
+ probesdbfile="c:\Folded_cascode_OTA_ac.sdb"
+ probetopmodule="ac"
* Main circuit: ac
C1 out Gnd 10.000000pF
.include "D:\pranav\ml2_125.md"
M2 out N13 N4 N4 NMOS L=2u W=75u AD=66p Pd=24u AS=66p PS=24u
M3 N4 N10 N9 N9 NMOS L=2u W=75u  AD=66p Pd=24u AS=66p PS=24u
M4 N10 N13 N14 N14 NMOS L=2u W=75u AD=66p Pd=24u AS=66p PS=24u
M5 N14 N10 N9 N9 NMOS  L=2u W=75u AD=66p Pd=24u AS=66p PS=24u
M6 N15 BIAS N9 N9 NMOS L=2u W=351u AD=66p Pd=24u AS=66p PS=24u
M7 N3 BIAS N9 N9 NMOS L=2u W=281u AD=66p Pd=24u AS=66p PS=24u
M8 N5 N17 N3 N3 NMOS L=2u W=61u AD=66p Pd=24u AS=66p PS=24u
M9 N2 N8 N3 N3 NMOS L=2u W=61u AD=66p Pd=24u AS=66p PS=24u
M10 N13 N15 N2 N2 PMOS L=2u W=182u AD=66p Pd=24u AS=66p PS=24u
M11 OUT N15 N5 N5 PMOS L=2u W=182u AD=66p Pd=24u AS=66p PS=24u
M12 N2 N1 N7 N7 PMOS L=2u W=303u AD=66p Pd=24u AS=66p PS=24u
M13 N5 N1 N7 N7 PMOS L=2u W=303u AD=66p Pd=24u AS=66p PS=24u
M14 N1 N15 N6 N6 PMOS L=2u W=303u AD=66p Pd=24u AS=66p PS=24u
M15 N6 N1 N7 N7 PMOS L=2u W=303u AD=66p Pd=24u AS=66p PS=24u
R16 N1 N15 2000.0 TC=0.0,0.0
R17 N13 N10 3333.3 TC=0.0,0.0
V18 N18 N17 0.0 AC 0.5 0.0
V19 N8 N16 0.0 AC 0.5 0.0
v20 N7 Gnd 2.5
v21 Gnd N9  2.5
v22 Bias Gnd -1.85
v23 N16 Gnd 0.0087
v24 Gnd N18 0.0087
.ac dec 10 1 10MEG
.print ac vdb(out) vp(out)
*   End of main circit : ac
```

Fig 5.2.1 Netlist generated through design synthesis tool



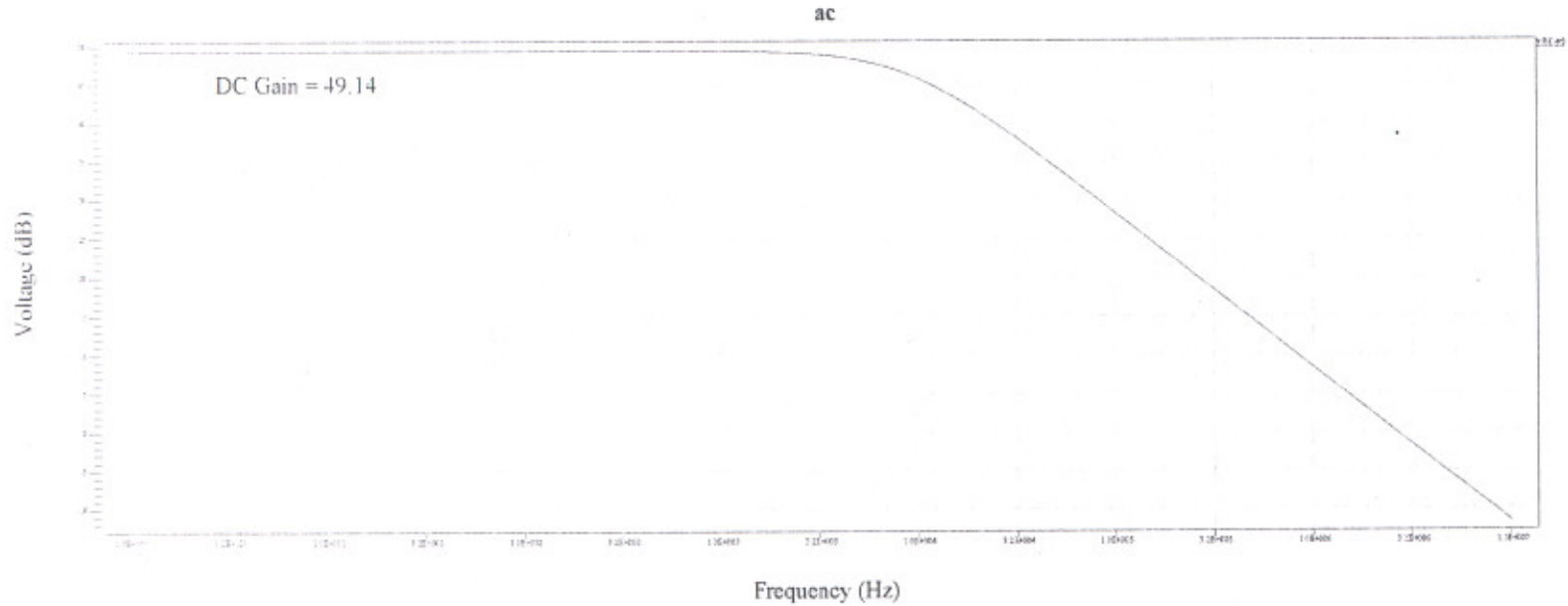


FIG. 5.2.2 AC analysis at 7MHz Design GBW

```
D:\pranav\opswing.sp
Page 1

* SPICE netlist written by S-Edit Win32 6.02
* Written on Apr 1, 2001 at 06:38:42

* Waveform probing commands
.probe
.options probefilename="Folded_cascode_OTA_os.dat"
+ probesdbfile="D:\pranav\Folded_cascode_OTA_os.sdb"
+ probetopmodule="opswing"

* Main circuit: opswing
C1 out Gnd 10pF
.include "D:\pranav\ml2_125.md"
M2 out N13 N4 N4 NMOS L=100u W=3796u AD=66p PD=24u AS=66p PS=24u
M3 N4 N10 N9 N9 NMOS L=100u W=3796u AD=66p PD=24u AS=66p PS=24u
M4 N10 N13 N14 N14 NMOS L=100u W=3796u AD=66p PD=24u AS=66p PS=24u
M5 N14 N10 N9 N9 NMOS L=100u W=3796u AD=66p PD=24u AS=66p PS=24u
M6 N15 Bias N9 N9 NMOS L=25u W=2071u AD=66p PD=24u AS=66p PS=24u
M7 N3 Bias N9 N9 NMOS L=100u W=6627u AD=66p PD=24u AS=66p PS=24u
M8 N5 in- N3 N3 NMOS L=25u W=1561u AD=66p PD=24u AS=66p PS=24u
M9 N2 in+ N3 N3 NMOS L=25u W=1561u AD=66p PD=24u AS=66p PS=24u
M10 N13 N15 N2 N2 PMOS L=100u W=9106u AD=66p PD=24u AS=66p PS=24u
M11 out N15 N5 N5 PMOS L=100u W=9106u AD=66p PD=24u AS=66p PS=24u
M12 N2 N1 N7 N7 PMOS L=50u W=7589u AD=66p PD=24u AS=66p PS=24u
M13 N5 N1 N7 N7 PMOS L=50u W=7589u AD=66p PD=24u AS=66p PS=24u
M14 N1 N15 N6 N6 PMOS L=50u W=7589u AD=66p PD=24u AS=66p PS=24u
M15 N6 N1 N7 N7 PMOS L=50u W=7589u AD=66p PD=24u AS=66p PS=24u
R16 N1 N15 2000 TC=0.0, 0.0
R17 N13 N10 2000 TC=0.0, 0.0
v18 in+ in- 0.0174 AC 0.0 0.0
v19 N7 Gnd 2.5
v20 Gnd N9 2.5
v21 Bias Gnd -1.85
.dc v18 -0.5 0.5 0.005
.print dc v(out)
* End of main circuit: opswing
```

Fig 5.3.1 Netlist generated through design synthesis tool

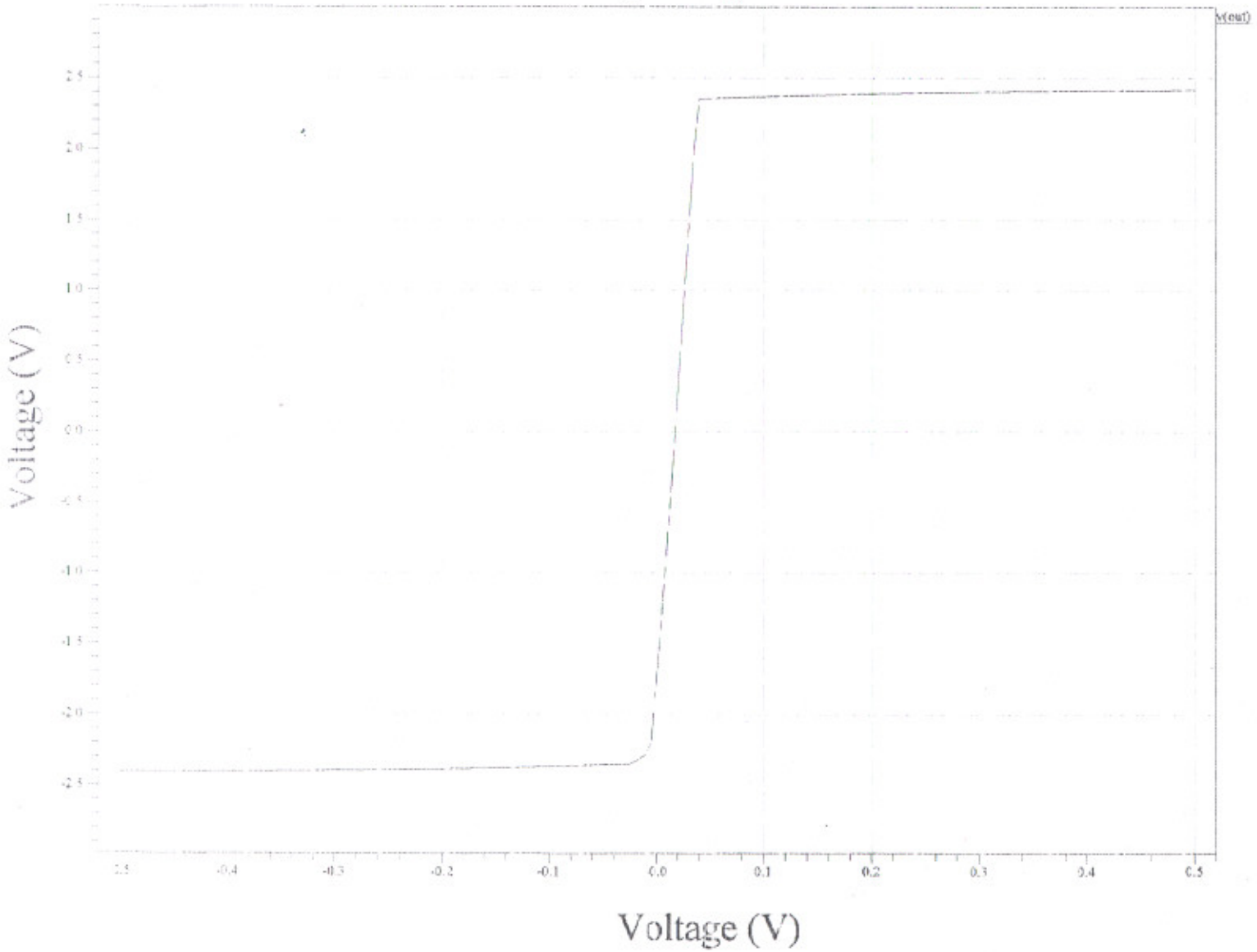


Fig 5.3.2

```
D:\pranav\slewrate.sp
Page 1

* SPICE netlist written by Manu Bansal
* Waveform probing commands
.probe
.options probefilename="Folded_cascode_OTA_slewrate.dat"
+ probesdbfile="c:\Folded_cascode_OTA_slewrate.sdb"
+ probetopmodule="slewrate"
* Main circuit: slewrate
C1 out Gnd 10.000000pF
.include "D:\pranav\ml2_125.md"
M2 out N5 N13 N13 NMOS L=2u W=75u AD=66p Pd=24u AS=66p PS=24u
M3 N13 N6 N14 N14 NMOS L=2u W=75u AD=66p Pd=24u AS=66p PS=24u
M4 N6 N5 N7 N7 NMOS L=2u W=75u AD=66p Pd=24u AS=66p PS=24u
M5 N7 N6 N14 N14 NMOS L=2u W=75u AD=66p Pd=24u AS=66p PS=24u
M6 N9 BIAS N14 N14 NMOS L=2u W=351u AD=66p Pd=24u AS=66p PS=24u
M7 N11 BIAS N14 N14 NMOS L=2u W=281u AD=66p Pd=24u AS=66p PS=24u
M8 N3 in- N11 N11 NMOS L=2u W=61u AD=66p Pd=24u AS=66p PS=24u
M9 N2 in+ N11 N11 NMOS L=2u W=61u AD=66p Pd=24u AS=66p PS=24u
M10 N5 N9 N2 N2 PMOS L=2u W=182u AD=66p Pd=24u AS=66p PS=24u
M11 OUT N9 N3 N3 PMOS L=2u W=182u AD=66p Pd=24u AS=66p PS=24u
M12 N2 N4 N12 N12 PMOS L=2u W=303u AD=66p Pd=24u AS=66p PS=24u
M13 N3 N4 N12 N12 PMOS L=2u W=303u AD=66p Pd=24u AS=66p PS=24u
M14 N4 N9 N1 N1 PMOS L=2u W=303u AD=66p Pd=24u AS=66p PS=24u
M15 N1 N4 N12 N12 PMOS L=2u W=303u AD=66p Pd=24u AS=66p PS=24u
R16 N4 N9 2000.0 TC=0.0,0.0
R17 N5 N6 3333.3 TC=0.0,0.0
v18 N12 GND  2.5
v19 Gnd N14  2.5
v20 Bias GND -1.85
V21 in+ in- pulse(-2.5 2.5 0 5u 200u)
.tran/op 5u 10u
.print tran v(in+,in-)
.print tran v(out)
* End of main circit: slewrate
```

Fig 5.4.1 Netlist generated through design synthesis tool

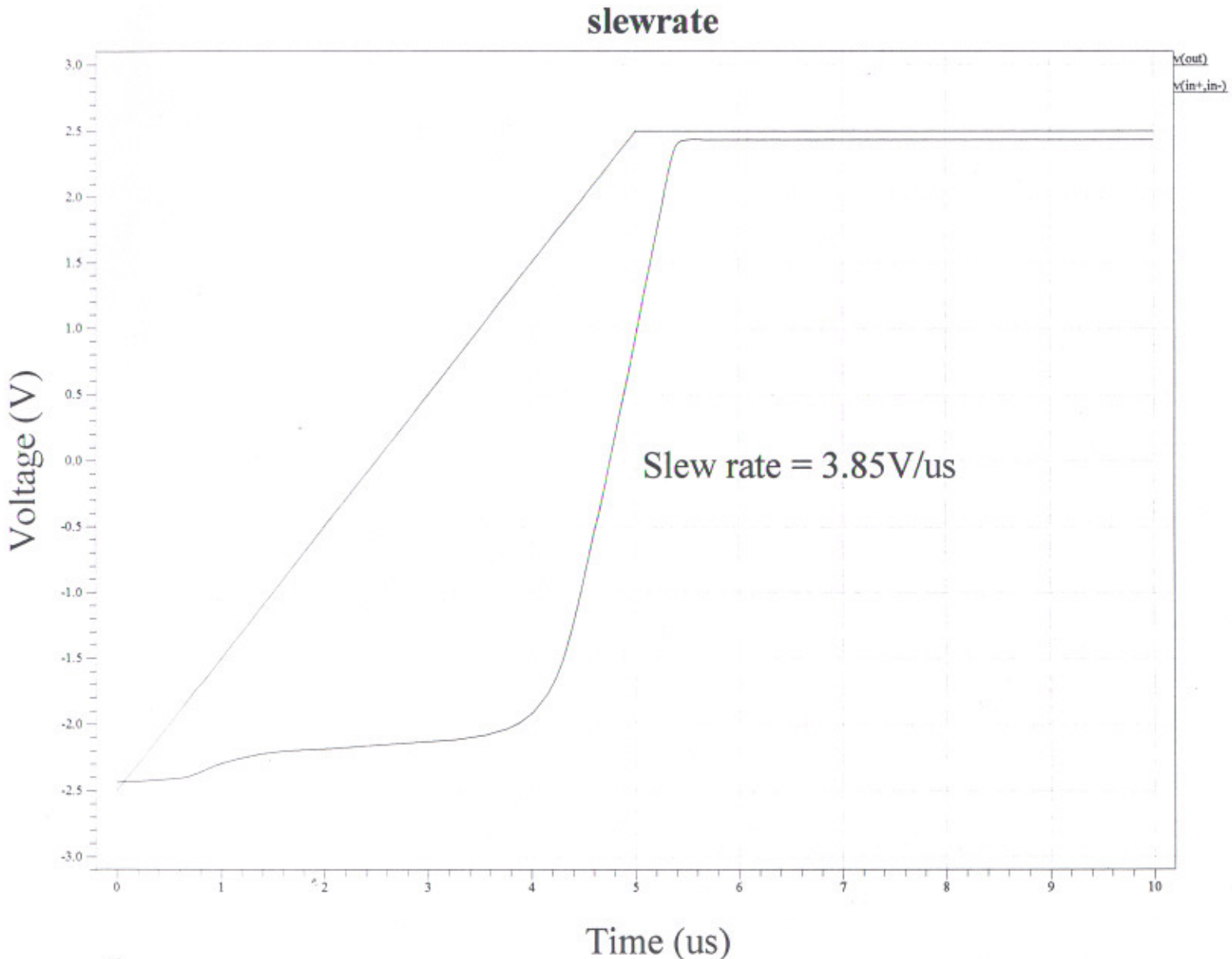


Fig. 5.4.2

```
D:\pranav\psrr.sp
Page 1

* SPICE netlist written by Manu Bansal
* Waveform probing commands
.probe
.options probefilename="Folded_cascode_OTA_psrr.dat"
+ probesdbfile="c:\Folded_cascode_OTA_psrr.sdb"
+ probetopmodule="psrr"
* Main circuit: psrr
C1 out Gnd 10pF
.include "D:\pranav\ml2_125.md"
M2 out N5 N13 N13 NMOS L=2u W=75u AD=66p Pd=24u AS=66p PS=24u
M3 N13 N6 N10 N10 NMOS L=2u W=75u AD=66p Pd=24u AS=66p PS=24u
M4 N6 N5 N7 N7 NMOS L=2u W=75u AD=66p Pd=24u AS=66p PS=24u
M5 N7 N6 N10 N10 NMOS L=2u W=75u AD=66p Pd=24u AS=66p PS=24u
M6 N9 BIAS N10 N10 NMOS L=2u W=351u AD=66p Pd=24u AS=66p PS=24u
M7 N11 BIAS N10 N10 NMOS L=2u W=281u AD=66p Pd=24u AS=66p PS=24u
M8 N3 in- N11 N11 NMOS L=2u W=61u AD=66p Pd=24u AS=66p PS=24u
M9 N2 in+ N11 N11 NMOS L=2u W=61u AD=66p Pd=24u AS=66p PS=24u
M10 N5 N9 N2 N2 PMOS L=2u W=182u AD=66p Pd=24u AS=66p PS=24u
M11 OUT N9 N3 N3 PMOS L=2u W=182u AD=66p Pd=24u AS=66p PS=24u
M12 N2 N4 N8 N8 PMOS L=2u W=303u AD=66p Pd=24u AS=66p PS=24u
M13 N3 N4 N8 N8 PMOS L=2u W=303u AD=66p Pd=24u AS=66p PS=24u
M14 N4 N9 N1 N1 PMOS L=2u W=303u AD=66p Pd=24u AS=66p PS=24u
M15 N1 N4 N8 N8 PMOS L=2u W=303u AD=66p Pd=24u AS=66p PS=24u
R16 N4 N9 2000.0 TC=0.0,0.0
R17 N5 N6 3333.3 TC=0.0,0.0
v18 N8 N14 0.0 AC 0.05 0.0
v19 in+ in- 0.0174 AC 0.0 0.0
v20 N14 Gnd 2.5
V21 Gnd N10 2.5
v22 Bias Gnd -1.85
.ac dec 10 1 10MEG
.print ac vdb(out)
* End of main circit: psrr
```

Fig 5.5.5 Netlist generated through design synthesis tool

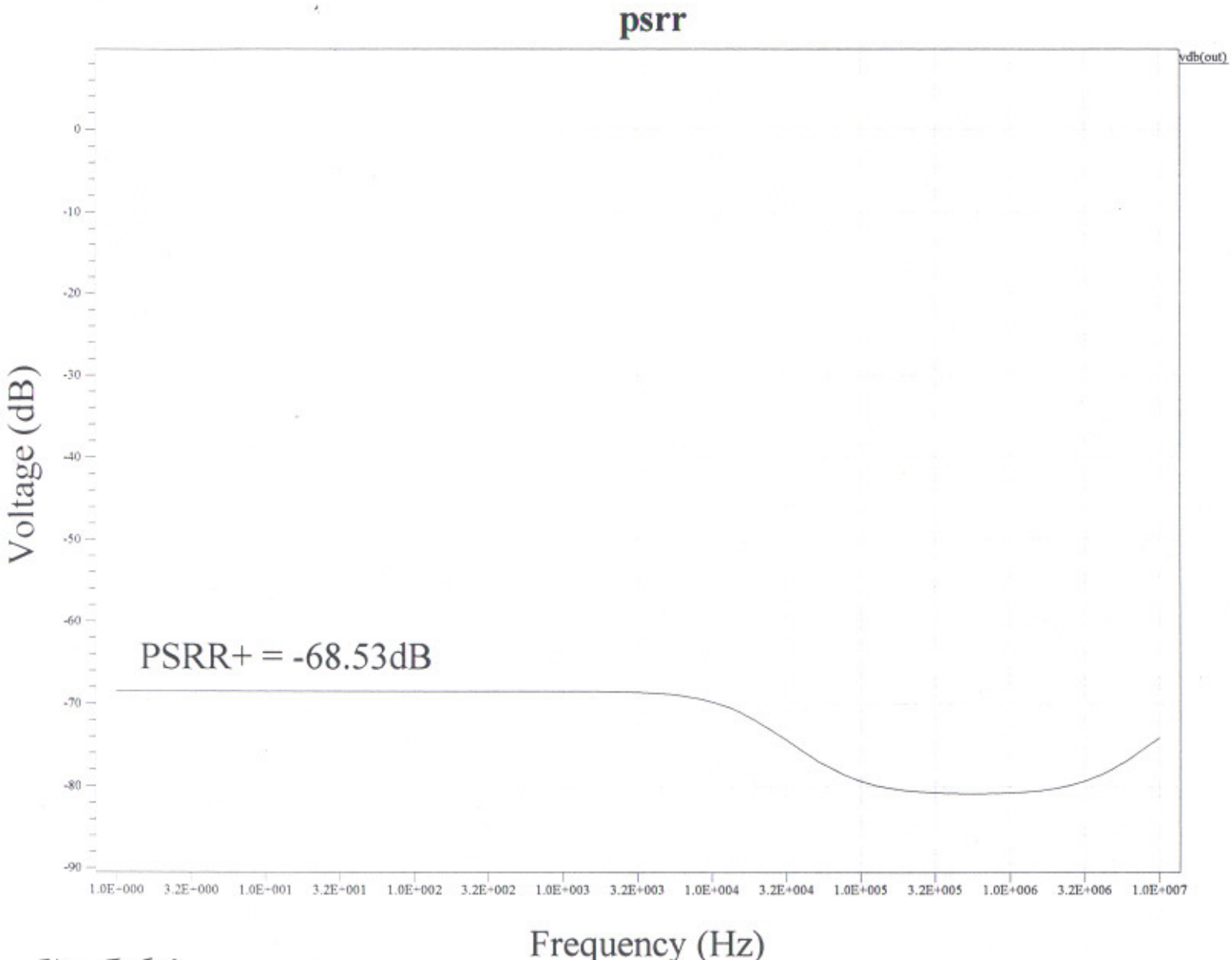


Fig. 5.5.6

```
D:\pranav\psrrn.sp
Page 1

* SPICE netlist written by Manu Bansal
* Waveform probing commands
.probe
.options probefilename="Folded_cascode_OTA_psrrn.dat"
+ probesdbfile="c:\Folded_cascode_OTA_psrrn.sdb"
+ probetopmodule="psrrn"
* Main circuit: psrrn
C1 out Gnd 10pF
.include "D:\pranav\ml2_125.md"
M2 out N5 N8 N8 NMOS L=2u W=75u AD=66p Pd=24u AS=66p PS=24u
M3 N13 N6 N8 N8 NMOS L=2u W=75u AD=66p Pd=24u AS=66p PS=24u
M4 N6 N5 N7 N7 NMOS L=2u W=75u AD=66p Pd=24u AS=66p PS=24u
M5 N7 N6 N8 N8 NMOS L=2u W=75u AD=66p Pd=24u AS=66p PS=24u
M6 N9  BIAS N8 N8 NMOS L=2u W=351u AD=66p Pd=24u AS=66p PS=24u
M7 N11 BIAS N8 N8 NMOS L=2u W=281u AD=66p Pd=24u AS=66p PS=24u
M8 N3 in- N11  N11 NMOS L=2u W=61u AD=66p Pd=24u AS=66p PS=24u
M9 N2 in+ N11 N11 NMOS L=2u W=61u AD=66p Pd=24u AS=66p PS=24u
M10 N5 N9 N2 N2 PMOS L=2u W=182u AD=66p Pd=24u AS=66p PS=24u
M11 OUT N9 N3 N3 PMOS  L=2u W=182u AD=66p Pd=24u AS=66p PS=24u
M12 N2 N4 N12 N12 PMOS  L=2u W=303u AD=66p Pd=24u AS=66p PS=24u
M13 N3 N4 N12 N12 PMOS  L=2u W=303u AD=66p Pd=24u AS=66p PS=24u
M14 N4 N9 N1 N1 PMOS  L=2u W=303u AD=66p Pd=24u AS=66p PS=24u
M15 N1 N4 N12 N12 PMOS  L=2u W=303u AD=66p Pd=24u AS=66p PS=24u
R16 N4 N9 2000.0 TC=0.0,0.0
R17 N5 N6 3333.3 TC=0.0,0.0
v18 N10 N8 0.0 AC 0.05 0.0
v19 in+ in- 0.0174 AC 0.0 0.0
v20 N12 Gnd 2.5
v21  Gnd N10 2.5
v22 Bias Gnd -1.85
.ac dec 10 1 10MEG
 .print ac vdb(out)
* End of main circit: psrrn
```

Fig 5.5.7 Netlist generated through design synthesis tool

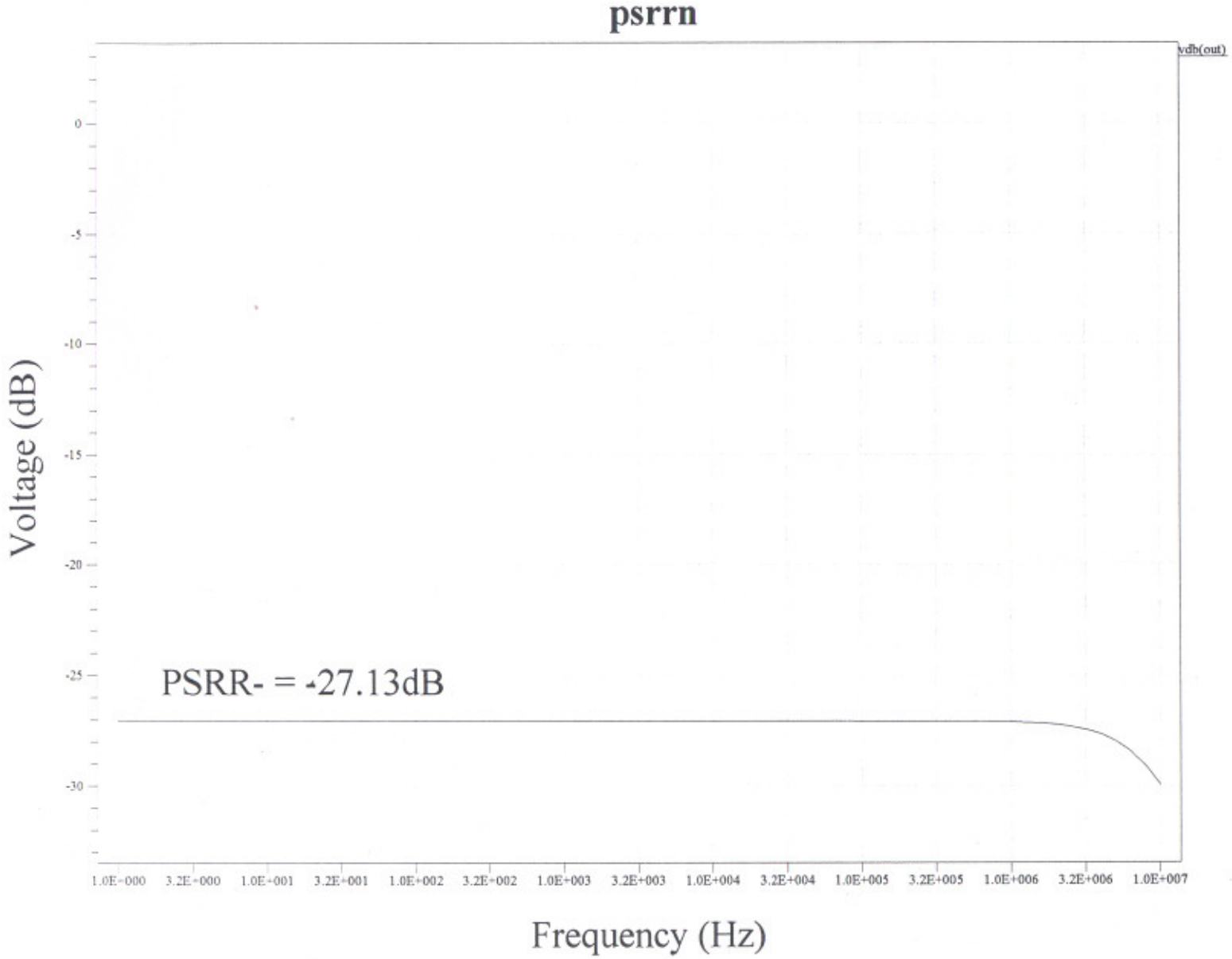
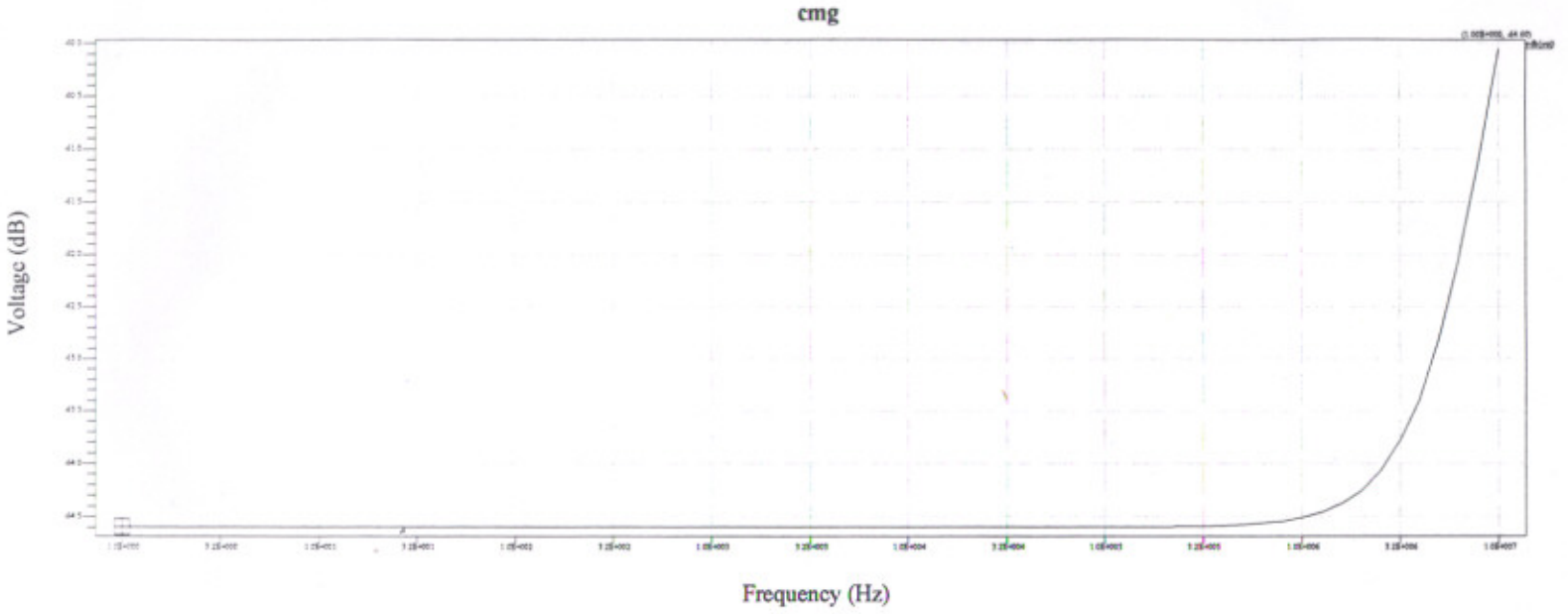

psrrn
vdb(out)
Voltage (dB)
0
-5
-10
-15
-20
-25
-30
PSRR- = -27.13dB
1.0E-000
3.2E-000
1.0E-001
3.2E-001
1.0E+002
3.2E-002
1.0E+003
3.2E+003
1.0E+004
3.2E+004
1.0E+005
3.2E+005
1.0E+006
3.2E+006
1.0E+007
Frequency (Hz)

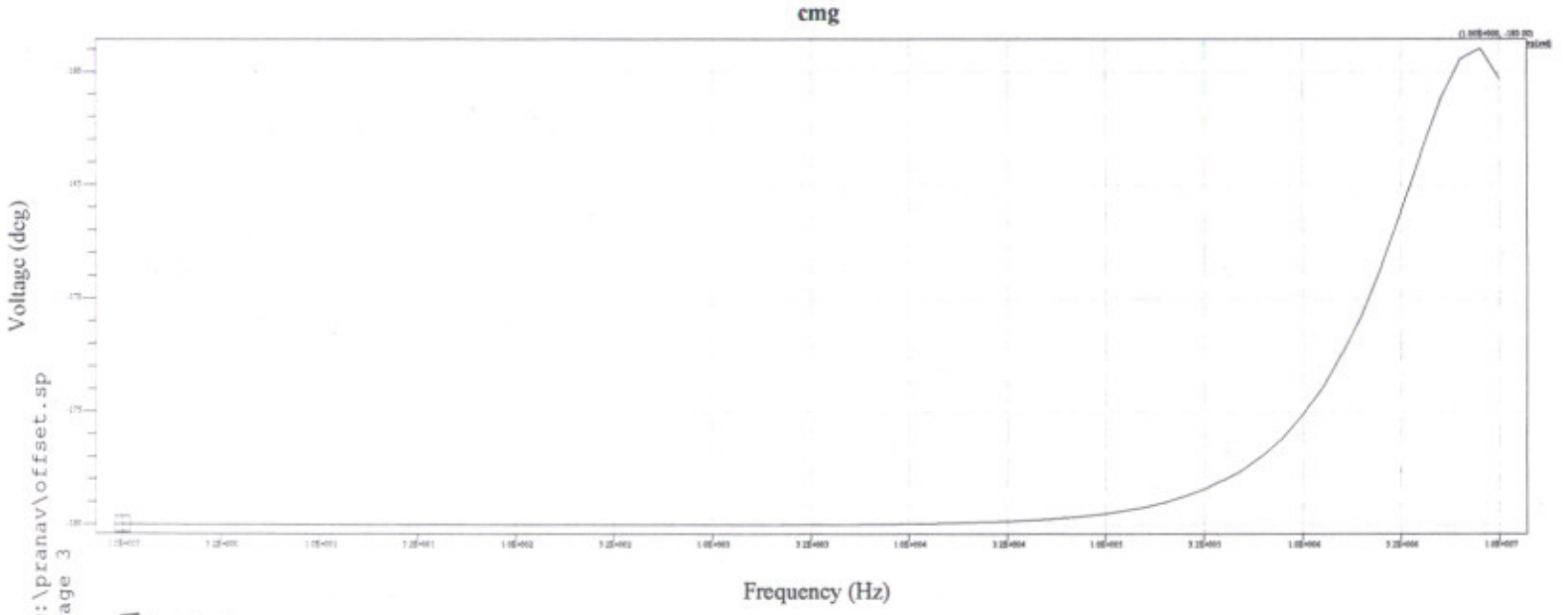
Fig. 5.5.8

```
D:\pranav\cmg.sp
Page 1

* SPICE netlist written by Manu Bansal
* Waveform probing commands
.probe
.options probefilename="Folded_cascode_OTA_cmg.dat"
+ probesdbfile="c:\Folded_cascode_OTA_cmg.sdb"
+ probetopmodule="cmg"
* Main circuit: cmg
C1 out Gnd 10.000000pF
.include "D:\pranav\ml2_125.md"
M2 out N13 N4 N4 NMOS L=2u W=75u AD=66p Pd=24u AS=66p PS=24u
M3 N4 N10 N9 N9 NMOS L=2u W=75u AD=66p Pd=24u AS=66p PS=24u
M4 N10 N13 N14 N14 NMOS L=2u W=0u AD=66p Pd=24u AS=66p PS=24u
M5 N14 N10 N9 N9 NMOS L=2u W=75u AD=66p Pd=24u AS=66p PS=24u
M6 N15 BIAS N9 N9 NMOS L=2u W=351u AD=66p Pd=24u AS=66p PS=24u
M7 N3 BIAS N9 N9 NMOS L=2u W=281u AD=66p Pd=24u AS=66p PS=24u
M8 N5 N11 N3 N3 NMOS L=2u W=61u AD=66p Pd=24u AS=66p PS=24u
M9 N2 N11 N3 N3 NMOS L=2u W=61u AD=66p Pd=24u AS=66p PS=24u
M10 N13 N15 N2 N2 PMOS L=2u W=182u AD=66p Pd=24u AS=66p PS=24u
M11 OUT N15 N5 N5 PMOS L=2u W=182u AD=66p Pd=24u AS=66p PS=24u
M12 N2 N1 N7 N7 PMOS L=2u W=303u AD=66p Pd=24u AS=66p PS=24u
M13 N5 N1 N7 N7 PMOS L=2u W=303u AD=66p Pd=24u AS=66p PS=24u
M14 N1 N15 N6 N6 PMOS L=2u W=303u AD=66p Pd=24u AS=66p PS=24u
M15 N6 N1 N7 N7 PMOS L=2u W=303u AD=66p Pd=24u AS=66p PS=24u
R16 N1 N15 2000.0 TC=0.0,0.0
R17 N13 N10 3333.3 TC=0.0,0.0
v18 N11 Gnd 0.0 AC 1.0 0.0
v19 N7 Gnd 2.5
v20 Gnd N9 2.5
v21 Bias Gnd -1.85
.ac dec 10 1 10MEG
.print ac vp(out) vdb(out)
* End of main circit: cmg
```

Fig 5.6.1 Netlist generated through design sunthesis tool





D:\pranav\offset.sp
Page 3

Fig. 5.6.2

CONCLUSION& FUTURE SCOPE

Operational amplifier is the basic building block of today's Analog Electronic Systems. We cannot think of an analog Circuit without Op-Amp. The design procedure and design synthesis tool was developed for folded-cascode OTA. The netlist files generated are then simulated using T-spice enviornment. AC analysis and DC analysis is done in the current thesis work.

The development of a design equation based procedure provided a quick and effective mechanism for directly estimating the MOS circuit parameters of the op amp from the performance requirements. Op amps designed with these calculated circuit values were able to satisfy these requirements to a good extent as evidenced by the T-spice simulations. This considerably reduced the total number of T-spice runs for the design. The design equations also highlighted the principal factors affecting the performance specifications, which made it very easy to redesign the circuit for different sets of specifications.

The relative simplicity of these design equations makes them efficient candidates for integration into knowledge-based analog CAD tools. These equations could also be used to generate a set of multidimensional curves on a workstation, with each dimension represented by circuit parameter or performance specifications. This would enable the designer to visually identify the effect of variations in a particular parameter on the rest of the circuit, thereby providing an insight into the trade-offs and other limitations in a particular design situation.

More studies can be carried out in following areas

- Alternative design procedures can be developed for higher frequencies, low power constraints, etc.
- Newer topologies can be designed and explored.
- Another layout synthesis tool can be developed which will generate automatic layouts from the netlist files generated from the current netlist synthesis tool.

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[3] Allen and Holberg, "Analog CMOS Subcircuits". Http://www.ece.utexas.edu/~holberg/lecture_notes/chap8.pdf

[4] Allen and Holberg, "Analog CMOS Subcircuits". Http://www.ece.utexas.edu/~holberg/lecture_notes/chap9.pdf

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