

# **Energy Efficient Memristor Based Non-Volatile Memory Cell Design**

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award of degree of

**Master of Technology  
in  
VLSI Design**

Submitted by

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## DECLARATION

I, hereby declare that the thesis entitled “ENERGY EFFICIENT MEMRISTOR BASED NON-VOLATILE MEMORY CELL DESIGN” in the partial fulfillment of the requirement for the award of degree of M.Tech (VLSI Design) submitted in Electronics and Communication Department of Thapar University, Patiala is an authentic record of my own work carried out under the supervision and guidance of Dr. Sanjay Sharma, Professor and Head, ECED and Ms. Sakshi Bajaj, Assistant Professor, ECED.

To the best of my knowledge, the matter embodied in this thesis work has not been submitted for award of any other degree at this or any other university.

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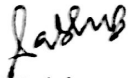
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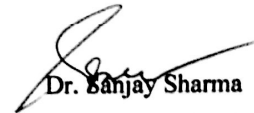
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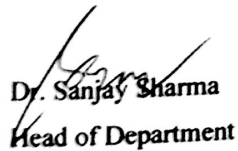


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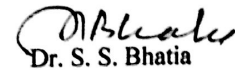


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## ABSTRACT

Memories form an integral part in computing, microprocessor and modern electronic devices. With the ever increasing demand of storing, large digital information which needs to be reliable, scalable, quickly accessible and also power efficient, different memory technologies unfolded with time. Memristor based circuits is an emerging technology, especially in memory architecture offering attractive combination of reliability, high speed and low power making it a powerful and efficient candidate for next generation memories. However, memristor device and its circuit level characterization still lies at its infancy stage and hence, it demands an extensive research and development to take its full benefit for various applications.

With the advancement towards latest technology nodes, the reliability of conventional memories gets significantly affected for lower supply voltage. Conventional memories like SRAM, DRAM, and flash memories have limitations and are unable to serve the growing demand of high density and low power. Thus, new semiconductor memories need to be explored and recently found memristor presented itself as a promising substitute for future memories or circuits. Memristor is a passive device which has a property of retaining its past value in the form of physical entity called memristance. Memristive devices need only two terminals to operate, being compatible with the today's predominant CMOS technology, uses less wafer space, and most suitable for memory architecture as in this resistance is used as a stored variable. In this thesis work, new approach of designing a memristor based non-volatile memory cell is proposed. The simulation results have also been shown to demonstrate the proper functioning of the memory cell and its advantages in terms of energy, area and speed of operation making memristor based memory cell as a promising substitute for the future.

The design was simulated in GPDK 45nm CMOS technology with a supply voltage of 1V using VTEAM memristor model in Cadence Virtuoso Analog Design environment

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## LIST OF ACRONYMS

VLSI	Very Large Scale Integration
ULSI	Ultra Large Scale Integration
GPS	Global Positioning System
PDA	Personal Digital Assistants
RAM	Random Access Memory
RRAM	Resistive RAM
FeRAM	Ferroelectric RAM
MRAM	Magnetic RAM
PRAM	Phase change RAM
RWM	Read Write Memory
ROM	Read Only Memory
SRAM	Static Random Access Memory
6T	Six Transistors
7T	Seven Transistors
DRAM	Dynamic Random Access Memory
PROM	Programmable ROM
EPROM	Erasable PROM
EEPROM	Electrically EPROM
VTEAM	Voltage ThrEshold Adaptive Memristor Model
TEAM	ThrEshold Adaptive Memristor Model

MOSFET	Metal Oxide Semiconductor Field Effect Transistor
NMOS	n-channel MOSFET
PMOS	p-channel MOSFET
CMOS	Complementary Metal Oxide Semiconductor
EDP	Energy Delay Product
MTCMOS	Multi-Threshold CMOS
AMS	Analog and Mixed Signal
PVT	Process Voltage Temperature
HP	Hewlett Packard

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# CHAPTER 1

## INTRODUCTION

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Rapid growth of electronics industry has driven excessive advancement of semiconductor technology leading new revolution in the field of VLSI technology. Application of VLSI technology is widely spread towards high end and mobile computing, various consumer electronics such as smart phones, 3D gaming, GPS positioning systems, defense and military operations, ubiquitous sensors and medical devices, global communication systems, radars, satellites, *etc.* In various applications, memories play a significant role in making these systems intelligent. To fulfill the increasing demand of higher performance, large amount of memory (on-die or embedded) having high data bandwidth need to be supported by the system. Various classifications of memories are available to fulfill various applications.

### 1.1 Motivation

#### 1.1.1 Increasing market demand of solid state non-volatile memory

Non-volatile memories are the storage devices in which even after the removal of power supply retain data indefinitely. With the introduction of video players and semiconductor audio players the need of storing data indefinitely (non-volatile storage) skyrocketed [1]. Classification of non-volatile memories includes flash memory, magnetic tapes, floppy disks, optical disks etc. Now a day, solid state non-volatile storage devices like NAND or NOR based flash memories become most popular as storage media. Traditional non-volatile storages (magnetic tapes, optical disks) involve some movable part for accessing data, resulting into higher latency. Solid state memory removes this downside but at the expense of cost.

General classifications of memories depend on type of data storage which are volatile or non-volatile and the type of data access method such as random or serial. ROMs (Read Only Memories) are non-volatile memories permitting retrieval of previously stored data only and do not allow modification of data during normal

operation. Similarly, RWMs (Read Write Memories) have both read and write feature, but are volatile in nature [2]. To meet the growing demand of high performance, mostly newly emerging non-volatile memories utilizes the resistance change feature of the material when some voltage level is reached or some current is applied to it like ReDox memory, Phase change memory etc., and opening new dimension of research in this regard.

Memristor based memories combine feature of various existing memories at one place. It emerges out to be very attractive possibility for future memory hierarchies having speed advantage of SRAM, non-volatile feature of flash and high density of DRAM.

### **1.1.2 Increasing demand of high density memories**

Silicon memories have grown in size, density and speed over the last decade with the advent of new computing technologies. This trend has been largely made possible with the ever shrinking dimensions of the MOSFET, following the so-called the Moore's Law according to which transistor count doubles in every 18 months [3]. However, memory scaling is losing pace with silicon scaling due to increase in device variation. To continue with the ever increasing demand of memory scaling, new memory circuits that can tolerate increased silicon variation are needed.

In contemporary digital designs, large portion of the silicon area is dedicated towards storing huge quantity of digital information like data values and program instruction. Although, the memory requirement of a system depends on the type of application, but generally the number of transistors utilized for storing information is much larger as compared to the number of transistors used in logic computation and for other purposes [2]. In high performance microprocessor more than half of the transistors of the system are devoted to cache memories [1]. Altogether, these have driven the demand for larger data storage capacity driving fabrication technology and new memory development solutions towards more compact design rules. Memristor-based memories came along a promising solution because of its low dimension area.

While a significant movement in today's ever increasing technology is towards more compact and portable systems in which the memories are embedded along with it, the demand of high density memory is also at pace. To meet the increasing demand of memory (MB or KB), the design of single memory cell must be such that it can occupy less area. Further reduction in area can be achieved at system or architecture level, but minimizing at the lowest level (single bit) of hierarchy results into significant improvement in the overall reduction in area. Thus, a new wave of research is going to find more compact and efficient solution towards compact memory and circuit design. Because of its compact nature memristor can be used to fulfill high density demand.

### **1.1.3 Growing demand of energy efficient devices**

Now a day, with the increasing prominence of the portable electronic devices and systems as well as the need to limit power consumption (and hence, heat dissipation) in very high density ULSI chips have led to rapid and innovative developments in low-voltage, low-power design techniques. The driving forces behind these developments are consumers' demand for portable device such as smart phones, notebook computers, and Personal Digital Assistants (PDAs) etc applications to have low power dissipation and high throughput. In most of the devices, the specification of long battery life must be met along with equally demanding goals of portability (area constraint) and high throughput. Therefore, to maintain the commercial viability of a product it is very important that the device should offer: a long battery life, smaller dimensions for easy handling and achievement of the desired functionality without heating up. Hence, low-power energy efficient design of digital integrated circuits need to have memory architecture to be optimized resulting into active and rapidly developing field in this domain. Memristor based memory architecture fulfils this demand by consuming almost negligible power.

With the increasing growth of VLSI technology, the energy efficiency of the system become integral factor. Energy efficiency is defined as the combination of reduced energy consumption and improving performance. Improvement in energy efficiency is also a byproduct of the Moore's law [3]. With more and more transistors lying on a single chip, physical interconnections among various blocks is reduced resulting into more energy efficient devices. However, due to scaling, the energy

efficiency advantage resulting from the Moore's law is threatening due to increase in leakage currents. Here, memristor based circuits can be a better alternative.

#### **1.1.4 Requirement of high speed of operation**

While being energy efficient and fulfilling demand of high storage density, memories need to be operable at high speed. With the new advancement in the material science, new techniques evolved being supplemented by traditional approaches. These results in new devices which allow memory developers to organize and mechanize memories, offering system engineers a new level of efficient improvement of performance concerning focus on speed, power, area, and cost [4].

Access of the memory, both read and write must be achievable with minimum latency in order to meet the speed of the presently, high frequency microprocessor. Data access speed has also evolved from the earlier Toshiba's SmartMedia card, which had a maximum data transfer rate of 2 MB/s [5], to devices such CompactFlash® memory cards that currently reaches data transfer rate of 133MB/s [6]. The growing market demands high speed, large storage capacity, and energy efficient or low power non-volatile memory devices, all together impetus to incentivize research in the field of designing a non-volatile memory. Memristor based memories emerges as a strong and promising candidate fulfilling requirements of next generation memories but as it is not present off the shelf it still requires an extensive research to come to consumers.

## **1.2 Organization of Thesis**

The thesis is organized as follows:

**Chapter 1** presents a brief overview of emerging memory technologies along with current trends and need of next generation memories.

**Chapter 2** gives a brief description of the research that has been reported in literature in the field of memristor modelling and memristor based circuits.

**Chapter 3** introduces basic concepts of memristor, its device structure and its operation. It also described the advantages offered by it over other conventional devices.

**Chapter 4** presents modelling of memristor along with its simulation results demonstrating its characteristics for proper functioning of memristor in the circuit.

**Chapter 5** describes the proposed memory cell, and the simulation results of it have been presented. The results have been compared with the previous work available in literature and compared on various design constraints.

**Chapter 6** concludes the report while also mentioning the future possibilities to carry forward the research in this domain.

## CHAPTER 2

### LITERATURE SURVEY

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Memristor is a passive two terminal fourth fundamental circuit element having unique characteristics. Since its discovery new wave of research is introduced exploiting its features. The following literature survey includes the main properties of memristor, mathematical representations, physical models, types, and some applications in different areas of research. Various technique of modeling a memristor and utilizing it for design (circuit architecture level) techniques are discussed as below.

#### 2.1 Introducing Memristor

**L. Chua, 1971 [7]** led to the discovery of fourth fundamental circuit element-memristor as a mathematical entity. Various laboratory explanation of memristor's existence and proof of its properties were described. Some circuit mutators are also presented for modeling of memristor. Memristor application in various areas is presented in detail with required mathematical explanation.

**D. Strukov *et al.*, 2008 [8]** analyzed memristor considering its physical existence, they have explained how some nano-scale system possess properties similar to memristor and thus be useful in deriving memristor's physical model. The hysteresis I-V curve detected in many thin-film nano-dimensional devices like titanium dioxide based seems to be useful for making memristor. The physics of operation for such devices in explained in detail along with mathematical representation of device characteristics.

#### 2.2 Memristor Models

**S. Kvatinsky *et al.*, 2012 [9]** presented various mathematical model of memristors so that the behavior can be approximated and utilized in further memristive circuits. Various window functions and models are coded via Verilog AMS code; also more models can be added. The parameters can be redefined before simulation thus provides opportunity to the user to study and fully control of the behavior of the memristor.

**H. J. B. da Costa *et al.*, 2012 [10]** presented a behavior model of a memristor using Verilog AMS and a methodology to perform simulations using the model in memristive circuits. The model presented can be utilized in a mixed circuit containing memristor model and SPICE components. The proposed memristor Verilog-AMS description was presented as a solution to the limitations from approach of using equivalent circuits to emulate memristive behavior. The model suitability when stimulated using current or voltage sources assuring their limits and validating the memristive and resistive behavior together.

**S. Kvatinsky *et al.*, 2013 [11]** proposed new memristor model TEAM (ThrEshold Adaptive Memristor Model) being flexible to fit in any practical memristive device. The proposed model is compared with other existing models and proved to be reasonably accurate and computationally efficient, thus being more appropriate for circuit simulation.

**S. Kvatinsky *et al.*, 2014 [12]** proposed voltage controlled model of Memristor- VTEAM (Voltage ThrEshold Adaptive Memristor) and explained its efficiency w.r.t to other proposed models especially current controlled models. Proposed VTEAM model is accurate (around below 1.5% in terms of relative root mean squared error) and computationally efficient as compared to existing memristor models and experimental results describing different memristive technologies. Also, the presented model has the advantages of the previously proposed TEAM model (i.e., flexibility, generality, and sufficiently accurate).

### **2.3 Memristor based circuits (Memory Applications)**

**Y. Ho *et al.*, 2009 [13]** analyzes memristor and derived equation needed for accessing its properties. They examine various ways to perform read and write operation into a memristor and especially describes ways to perform non-destructible read operation. Emphasizes on the importance of memristor in memory related operations and proposes a memory cell utilizing memristor.

**P. Junsangri *et al.*, 2013 [14]** presents non-volatile memory cell design using ambipolar transistor and memristor. Ambipolar transistor was modeled using CMOS transistors and

transmission gates and memristor was modeled via Spice. Different operations of memory, read and write are performed and compared with the existing non-volatile memories like NAND/NOR based flash memories. The proposed memristor based cell had improved results depicting the increasing demand of memristor based non-volatile memory architecture for future.

**S. S. Sarwar *et al.*, 2013 [15]** design a new non-volatile SRAM memory utilizing combination of memristors (HP model) and NMOS transistors which are utilized as a switch and compared its characteristics like area, read margin and write margin with the conventional 6T SRAM. Except write '1' operation the results of proposed memristor based cell came out to be much better than the 6T SRAM, opening new dimension for non-volatile memories. The non-volatile characteristics obtained from the design is an attractive feature for the future memories.

**P. Junsangsri *et al.*, 2014 [16]** proposed a new approach of designing a memory cell using memristor and ambipolar transistors. Using combination of ambipolar transistor and MOS acting as switches they have designed a new scheme of memory cell. Memory cells must be designed such that read and write operations are successfully performed. To fulfill such need of memory cell architecture they have tuned switching between transistors and ambipolar transistors in such a way that no refresh mechanism (requirement for voltage controlled memristor based memory cell) is required in order to overcome the destructible read operation.

**V. S. Baghel *et al.*, 2015 [17]** designed memristor based 7T SRAM and MTCMOS based 7T memristor SRAM at 45 nm technology, in order to improve the data retention capacity of simple SRAM for high speed memory operations-read/write and to reduce power dissipation. Furthermore, they determined and compared the leakage power and total power of conventional 7T SRAM, memristor based 7T SRAM and MTCMOS based 7T memristor SRAM, and thus established that the MTCMOS based 7T memristor SRAM is better than other two this design has total power 0.984 nW and leakage power 5.30 nW making it prominent for low power memory applications.

The literature survey to demystify a memristor, its characteristics and its usage in the circuit is studied in detail. Various models utilized for its modeling and the parameters needed to characterize it were explored. Also memory circuits utilizing memristor as a circuit element towards improving the performance of the cell based on various design constraints like area, power, and speed of operation is facilitated through the papers studied.

## CHAPTER 3

# DEMYSTIFYING THE FOURTH FUNDAMENTAL CIRCUIT ELEMENT: MEMRISTOR

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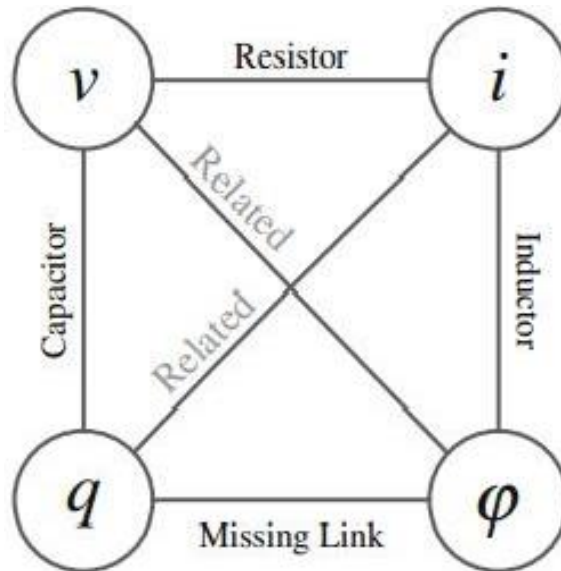
This chapter aims at providing the comprehensive overview of memristor, the fourth fundamental circuit element. This majorly includes fundamental aspects, features, characteristics and working principle altogether putting foundation of memristor theoretically and technically.

### 3.1 Fundamental Circuit Elements

Until recent years, in electronics following three elements –Resistor ( $\Omega$ ), Capacitor (F) and Inductor (H) has been accepted as the basic fundamental circuit elements as any circuit component can be described in terms of these elements. These together define relationships among fundamental circuit variables elements: charge  $q$ , current  $I$ , voltage  $V$  and flux  $\phi$ , five out of six possible combinations  $\{(v, \phi); (i, q); (v, i); (v, q); (i, \phi); (\phi, q)\}$ , are defined by these elements [18].

**Table 3.1** Fundamental Circuit elements before the discovery of memristor [21]

S.No.	Known Fundamental Elements	Expression
1.	Resistor	$R = \frac{dv}{di}$
2.	Capacitor	$C = \frac{dq}{dv}$
3.	Inductor	$I = \frac{d\phi}{di}$



**Figure 3.1** Fundamental relationships of the circuit components [21]

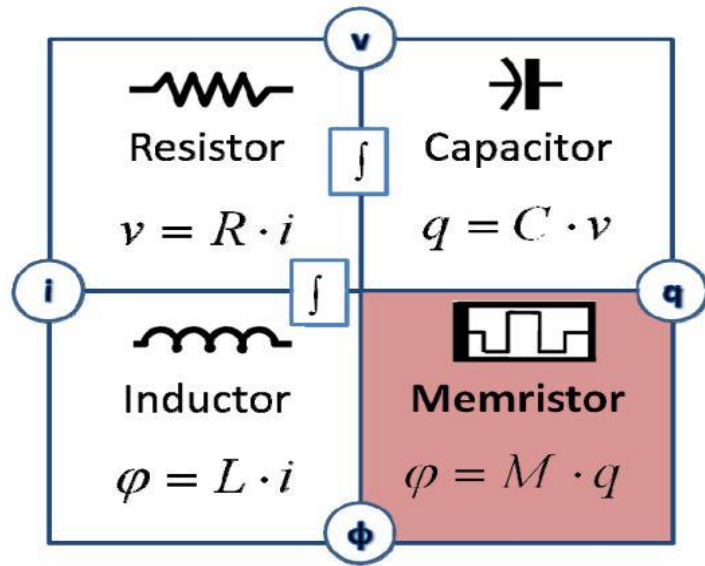
### 3.1.1 Missing fundamental circuit element: Memristor

In 1971, L. O. Chua [7] conceived the fact that the fourth fundamental circuit element (two-terminal) was found in addition to the existing ones- Resistor, Inductor and Capacitor. Chua postulated the missing link by carefully examining pair-wise, the mathematical relationships relating different fundamental circuit variables. The existence of the missing element was reasoned by examining the six possible combinations of relationship among the following fundamental electric circuit variables – electric charge  $q$ , electric current  $I$ , voltage  $V$ , and flux  $\phi$ . The behavior it exhibits cannot be duplicated by any other device that is the reason why it is declared as the fourth fundamental circuit element. Memristor defines the relationship between charge and flux, its resistance is a function of flux (which is time integral of the voltage applied across the device) linked to the device or the charge passed through the device.

Unlike other fundamental circuit elements memristor carries a unique feature of sustaining memory of its past and also recalls how much power was linked before and for how long. This effect of memristor is radically different from others and also cannot be reproduced or duplicated by any other circuit configuration, because of which memristor genuinely fit into the race of fundamental circuit element. Although, it is possible technically that the mechanism exhibited by memristor can be replicated using circuit

elements like transistors (switching mechanism) and capacitors (storing mechanism), but the number of such elements to do this job is large in place of single memristor [19].

In actual, memristor is a resistance with memory (short form of memory resistor) its resistance changes when a particular voltage is applied across it, when the applied source is removed the memristor hold the same resistance value, thus suitable in memory applications.



**Figure 3.2** Fundamental Relationships of all Passive Components [20]

Thus, memristor conceptually describes and fully satisfies the symmetry relationship among various fundamental circuit variables.

### 3.2 Theory of Memristor

Memristor defines the missing relationship between charge ( $q$ ) and flux ( $\phi$ ). It is defined as a two terminal circuit element for which magnetic flux ( $\phi$ ), linked with its terminals is a function of the total quantity of charge passed through it [20]. Memristor's terminals in any literature are not described as positive or negative but as per the study these can be defined in terms of state reached when electrical signal is applied to it. When higher potential is applied at darker side memristance increases till it reaches  $R_{OFF}$  value. While when the polarity of the signal is reversed memristance decreases to attain  $R_{ON}$  value. It is a passive device represented symbolically as shown in Fig. 3.3.



**Figure 3.3** Memristor Symbol

Mathematically, memristor is characterized by describing its memristance as a function of charge- linked through it [21].

$$M = \frac{d\phi}{dq} \quad (3.1)$$

From the Faraday's law of induction, magnetic flux can be described as time integral of voltage, likewise charge is defined as time integral of current, using these relations time dependent memristance can be conveniently described as

$$M(t) = M(q(t)) = \frac{\frac{d\phi}{dt}}{\frac{dq}{dt}} = \frac{V(t)}{I(t)} \quad (3.2)$$

From the above equation it can be concluded that memristance actually is a charge-dependent resistance. This being the reason it is called memristor contraction of “memory and resistor” [19]. If  $M(t)$  does not vary with charge it simply shows linear relationship between current and voltage following conventional Ohm's law. Furthermore, memristor is static which means that it is not altered by changes in electrical quantities such as device charge and flux, their history, integrals, derivative etc. [19].

### **What is Memristance?**

Memristance is the characteristics of an electronic component called memristor, which has ability to retain its resistance value in standby mode i.e. power shutoff mode and recollect (or recall) the last resistance value achieved by it before being shutoff.

## **Memristor v/s Resistor**

Memristor has characteristics similar to resistor and even shares its unit of measurement (ohms). However, the resistance of ordinary resistor is permanently fixed, while the memristance of memristor may be varied. Its value can be programmed to have different switching states depending upon the history of the applied electrical signal [19]. As seen graphically the characteristics of both lies in first and third quadrant only, the resistor has linear characteristics while that of memristor is quite complicated. The memristor behaves as resistor at higher frequency of operation or when the applied signal varied slightly.

### **3.2.1 Memristor fingerprints**

Memristors exhibits certain unique set of characteristics which distinguishes it from other resistive switching electronic devices [18], [21]:

1. Pinched hysteresis loop in current-voltage plane.
2. Frequency dependent pinched hysteresis loop area.

### **Pinched Hysteresis Loop in current-voltage plane**

When a bipolar periodic signal is applied across memristor, the device must exhibit a pinched hysteresis loop in the current-voltage plane for all frequencies, amplitudes and other initial conditions. In other words, it can be said that there lies no time delay (i.e. phase shift) between current and voltage waveforms. The loci due to variation of any periodic signal must be pinched at the origin and always irrespective of type, magnitude or any other signal characteristics. Associated with a particular memristor distinct periodic signals results into distinct pinched hysteresis loops. This means that the excitation signals establish an “identity card” unique for that particular device. The non-volatile feature of a memristor is a by-product of this and the state dependent Ohm’s law described in Eq. (3.2). If memristor is either open circuited or short circuited having a resistance  $R_0$  at  $t=t_0$ , it does not lose this value instead it retains its state forever [18].

The pinched hysteresis characteristics obtained for the typical memristor is as shown in Fig. 3.4. The curve obtained is for sinusoidal input voltage.

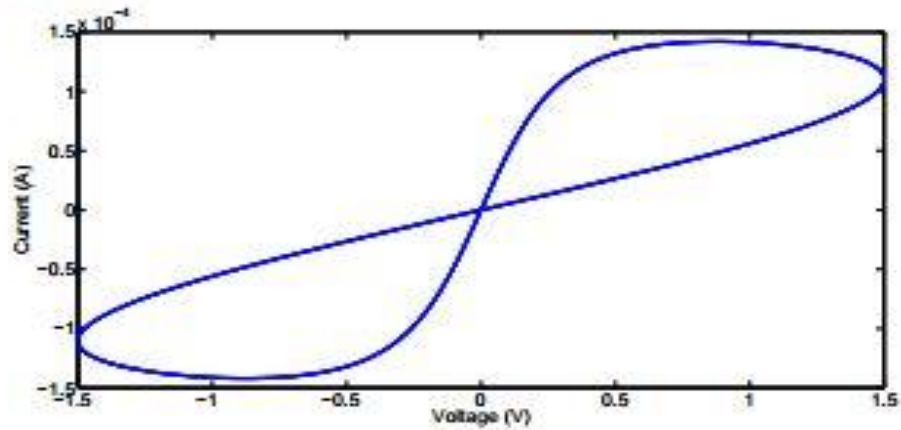


Figure 3.4 Bow Tie type characteristics of Memristor [18]

### Frequency dependent pinched hysteresis loop area

For any periodic signal, as the frequency increases the pinched hysteresis area lying in the first and third quadrant of the current-voltage plane decreases monotonically. Along with this, the lobe area shrinks and deforms continuously as the excitation frequency increases and collapse to a single valued function passing through the origin [18]. When the frequency tends to infinity pinched hysteresis shrinks into a straight line exhibiting characteristics similar to a resistor, this means high frequency signals does not provide memristor enough time to change its state [21]. Any purported system must exhibits both of the above characteristics to behave as a memristor, failing any of two will deter to fully utilize the actual characteristics of memristor.

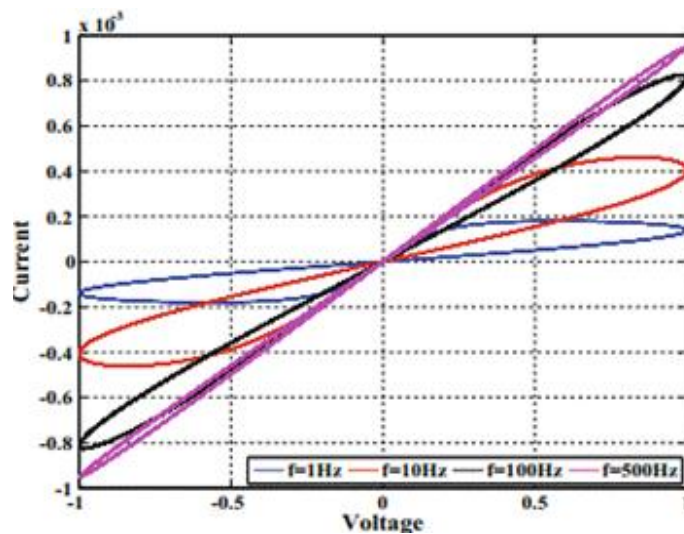


Figure 3.5 I-V characteristics for sinusoidal input at different frequencies [21]

### 3.2.2 Remembers history

Memristor resistance called memristance depends on the magnitude and polarity of the voltage applied across it and the period of time that voltage has been applied [18]. When power is down i.e. when the voltage source is turned off, the memristor memorizes its most recent resistance until the next time power is turned on again, independent of turn-off time.

#### Pipe and water analogy

Analogy memristor with a water pipe, taking water as equivalent to electric charge in the circuit. The diameter of the pipe is similar to resistor obstruction towards the flow of electric charge in the circuit: the narrower the pipe, the higher the resistance likewise, the broader the pipe the lower the resistance. Conventional resistor is a pipe having fixed diameter, differently memristor is a pipe that alters its diameter as per the amount and direction of water that flows through it. If the flow of water is in one direction, it expands i.e. electrically becoming less resistive while reversing flow of water results in shrinking of pipe i.e. electrically becoming more resistive. Furthermore, the memristor memorizes its diameter when water last went through. Turning off the flow, makes the pipe “freezes” until the water is turned back on [19]. Thus, the pipe does not store water like a bucket (or a capacitor) – it remembers how much water flowed through it. This property of memristor suits brilliantly for computer memory making it a strong candidate of non-volatile memory.

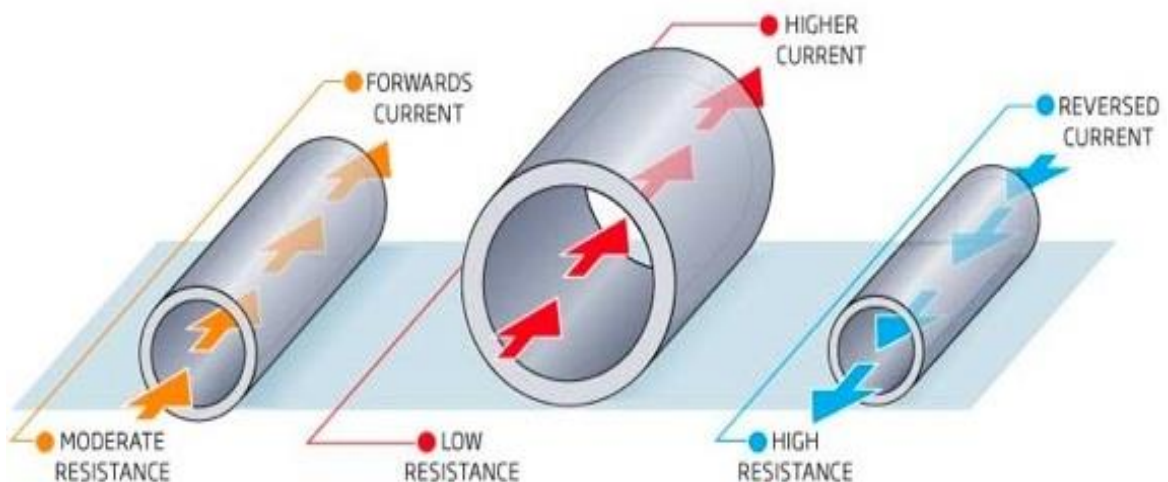
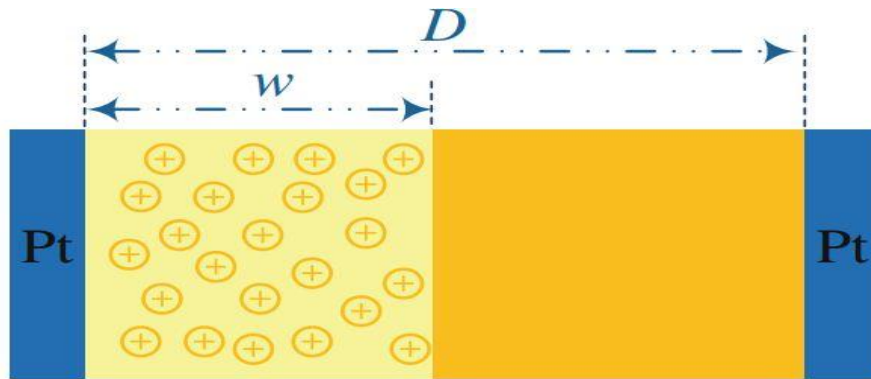


Figure 3.6 Memristor’s analogy with pipe [19]

### 3.3 Underlying Physics

Transition metal oxides which include pure titanium oxide can also act as semiconductor. Similar to other semiconductors, in intrinsic state these are highly resistive and their electrical conductivity can be increased via doping. To achieve this titanium oxide can be doped by intentionally reducing the ratio of oxygen atoms from its stoichiometric form. Removing the negatively charged oxygen atoms from the  $\text{TiO}_2$  molecule, a positive ion is formed due to the deficiency of electron. Thus, oxygen vacancies are assumed to be positive charged ions acting as charge carriers. Thus, the oxygen deficient upper layer  $\text{TiO}_{2-x}$  (where  $x$  represents the amount of oxygen deficiencies or vacancies) of the molecule is a semiconductor having small resistance and stoichiometric  $\text{TiO}_2$  is an insulator having very high resistance [19]. However, different from other semiconductors like silicon in which ionized doping atoms remains immobile in the lattice structure, oxygen deficiencies of titanium oxide can move in any direction of current when electric field is applied across it.



**Figure 3.7** Memristor Physical Structure [18]

Whenever an electric field is applied, the oxygen vacancies i.e. charge carriers drift changing the boundary between the high-resistance and low-resistance layers. Upon application of positive potential across the vacancy rich  $\text{TiO}_{2-x}$  layer w.r.t. the un-doped  $\text{TiO}_2$ , the oxygen deficiencies which are positively charged will be repelled and begin to drift towards the un-doped  $\text{TiO}_2$  thus, causing the shifting of the boundary of  $\text{TiO}_{2-x}/\text{TiO}_2$  and reducing the effective thickness of the  $\text{TiO}_2$  layer increasing the ratio of conductor to insulator. As a consequence of this, the overall device resistance decreases ( $R_{ON}$ ) making it more conductive. Likewise when the polarity is reversed, the oxygen

vacancies will be attracted back to the  $\text{TiO}_{2-x}$  shifting the  $\text{TiO}_{2-x}/\text{TiO}_2$  boundary in the opposite direction increasing the thickness of the un-doped  $\text{TiO}_2$ . This results into a device with high resistivity ( $R_{\text{OFF}}$ ) thus lowering overall conductivity [18]. Thus it can be concluded that the resistance of the film as a whole is a function of how much charge has been passed through it in a particular direction, which changes as per the polarity and duration of the electrical signal changes

During standby mode the system freezes at its instant condition and the oxygen deficiencies of the gap remains stationary [19]. When the power of the system is returned back the resistance of the system will either increase or decrease depending upon the polarity of applied voltage.

For turning off the memristor ‘on’ application of positive voltage the titanium oxide layer with vacancies must be kept as the top layer while inversely to turn on a memristor on application of positive voltage the layers need to be reversed.

### **3.4 Applications of Memristor**

Memristor has wide range of applications in various domains. Some of these include analog and digital circuits, memory architecture, neural networks etc. For some major applications brief overview is described below

#### **3.4.1 Analog applications**

##### **1) Programmable Analog Circuits**

Many analog circuits like amplifiers and filters need resistors to be programmed for adaptation to particular applications or for compensation of PVT (Process, Voltage, and Temperature) variations [21]. The most popular method used to realize programmable resistors is composed of an array of weighted resistors and switches, taking the form of switch-controlled resistors, but it has drawback of state dependent large parasitic capacitances and resistances due to introduction of MOS. To overcome all these memristors can be employed for introducing programmability in analog circuits in which variable resistance provides the necessary tuning. Thus, analog circuits in which resistors were utilized like active filters, oscillators etc. can be replaced by memristors. But before utilizing memristor for such applications, one should carefully

verify the undesirable behavior introduced by it, if any, lies within the acceptable range [21].

## **2) Neuromorphic Electronics**

Neuromorphics has been defined as a mixed mode analog–digital system mimicking neurobiological architectures to pattern neurons by real-time simulation, computation and emulation of the nervous system. Since memristors integrate both the aspects of memory storage and signal processing at one place similar to neural synapses thus seems to be ideal candidate for creating a synthetic electronic system similar to the human brain [21].

Researchers at HP said that “New memristor found can remember and associate series of events in a manner similar to the way a human brain recognizes patterns.” Memristor has a unique feature that could be used to make devices that require "learn from experience" feature such as brain-like systems, would allow for vastly improved facial or biometric recognition, although such research is at its infancy stage [8].

### **3.4.2 Digital applications**

#### **1) Non-volatile Memory**

Memristor is a promising candidate for non-volatile memory; it is the dominant area where memristor technology is highly pursued. This is the direct consequence of its resistive switching behaviour as it has a metal–insulator–metal configuration. Prior to the physical evolution of the memristor, high density memory applications of resistive switching exist in literature in which the insulating layer (responsible for resistive nature) works as a storage medium. Likewise, Resistive Random Access Memories (RRAM) are two-terminal device in which the switching medium is sandwiched between top and bottom electrodes and its resistance can be modulated upon application of electrical signal (current or voltage) across the electrodes.

Ferroelectric RAM (FeRAM), phase change of material states RAM (PRAM) and Magnetic RAM (MRAM), are few such existing examples which shows large electrical non-volatile resistance changes [21]. Memristor fall under the same category for memory applications, the memristor non-volatility feature has the capability to

build such computer system which will turn on without rebooting and there will be no requirement of physical RAM separately. Non-volatile state can be accomplished by memristor because its state is encoded by impedance (physical state) not voltage.

### **Future of flash drives or all existing memories:**

Memristor is used as a cheaper and faster alternative to flash memory. Non-volatile memory is built with memristors, meaning that unlike DRAM they'll retain information even when you turn off the power. Memristor runs 10 times faster while using 10 times less power than flash memory [14]. Memristors could eventually store data and process data.

In PCs, HP foresees memristors being used to make new types of system memory that can store information even after they lose power, unlike present DRAM [8]. With memristor-based system RAM, PCs would no longer need to go through a boot process to load data from the hard drive into the memory, which would save time and power, as users could simply switch off systems instead of leaving them in a "hibernate" or "sleep" mode.

## **2) Logic Computation**

Another exciting application of memristors lies in logic gate implementation. This usage of memristor technology is less furnished as compared to memory architectures but the research in this area has already sown seeds of innovation can be referred in [26]. Memristor shows two state switching behaviours (switching between  $R_{MAX}$  and  $R_{MIN}$ ) which can be beneficial for representing binary signals most important for Boolean operations [21]. In the areas of reconfigurable computing architectures such as FPGAs, memristors appear particularly important as in such architecture the arrangement between arrays of basic logic gates can be altered by reprogramming the wiring interconnections. Memristors may be ideal for re-configurability of such systems as well as to improve the integration density.

The memory characteristics and latching capability along with nanometer dimensions of memristor enables better alternatives of existing nano-computing methods. The nanometer scale device provides very high density and less power hungry

circuit. In addition, the fabrication process of nano-devices is simpler and cheaper than the conventional CMOS fabrication and all these comes at the cost of extra device defects.

### **3.5 Advantages of Memristor Technology**

The memristor opens a new door of opportunity for realization of innovative circuits. With its introduction in electronics, supplanting or supplementing transistors in several applications, a new wave of research at circuit or architecture level creates new pathways in various dimensions. Memristor provides indefinite advantages such as:

1. Simple well-ordered periodic structure, beneficial for nano-scale resolution
2. Scalability down to sub-10 nm possible physically its length can be as small as 3nm
3. Non-volatility as remembers history
4. Fast switching speed
5. Energy efficiency or low power
6. Cheap or cost effective but at the cost of other device features due to nano-scale dimensions.
7. Compatible with CMOS technology, this is important from the fabrication point of view because logic circuits are majorly dominated by CMOS.
8. Provides unconventional computation framework, combining information processing or logic functionality and memory or storage at one place.
9. Multi bit storage capability unlike other conventional devices which use only 0 and 1, memristor can use anything between 0 and 1 (0.3, 0.8, 0.5 etc.)
10. High density or large storage capacity.
11. High inherent defect-tolerance capability and flexibility, necessary for good yield.
12. Provides greater resiliency and reliability when power is interrupted in data centres.

Thus, memristor-based circuit potential embrace grandest technology challenges, defining new pathways for the exploration of advanced computing architectures as promising alternatives to conventional integrated circuit technologies, which are facing serious challenges related to continuous scaling [22]. Implementation of logic circuits

using memristors is gaining considerable attention, as memristor possess switching characteristics useful in binary digital circuits, where it would operate as a two-state switch, whose value toggle between max and min resistance.

### **3.6 Disadvantages of Memristor technology**

- a) If a computer is infected with a virus, the memristors may cause the computer to keep rebooting with the same problem because the memory will not be lost after reboot.
- b) Memristors ability to learn from patterns, if a bad pattern is present at an early stage, the computer's problem could grow worse and worse at a rapid rate.
- c) They store data can never be deleted.

## CHAPTER 4

### MEMRISTOR MODELLING

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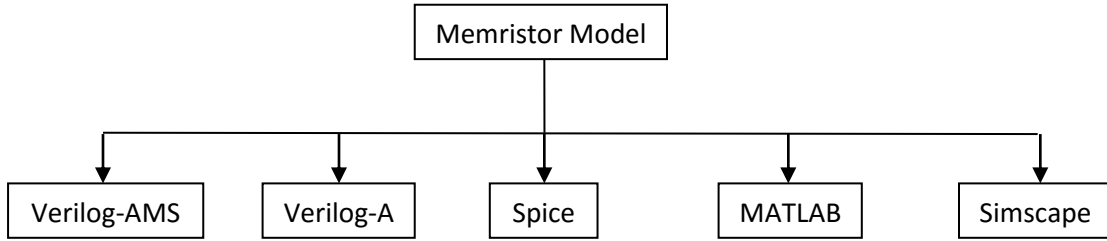
This chapter describes the modeling of memristor using VTEAM model [12]. The VTEAM model describes the behavior of memristor implemented in Verilog-AMS and used via Cadence® Virtuoso Analog Design Environment for simulations. Electrical characterization of the device is explored and carefully examined.

#### 4.1 Device Characterization

Memristors have variable aspects, different from the theoretical description of the device envisioned by L. Chua [7], to the mathematically extended theory, to the countless different technologies and applications evolved in recent years. Since, the discovery of the memristor by L. Chua [7], memristor device and circuit research is still in its infancy stage. Standardization of device characteristics still need to be done as memristor research is still immature. The desired or required characteristics vary from application to application. Understanding the required characteristics for particular applications beforehand seem to be helpful and may facilitate device and material engineers in furnishing the needed appropriate behavior as per the application during fabrication, thereby optimizing memristor as per available applications. Memristor is not available as a physical entity although, some research institutes had fabricated memristor like HP Labs [8] for their own research purpose only. Thus, researchers have to rely on models of memristor which are either published in literature or else model themselves.

#### 4.2 Device Modeling

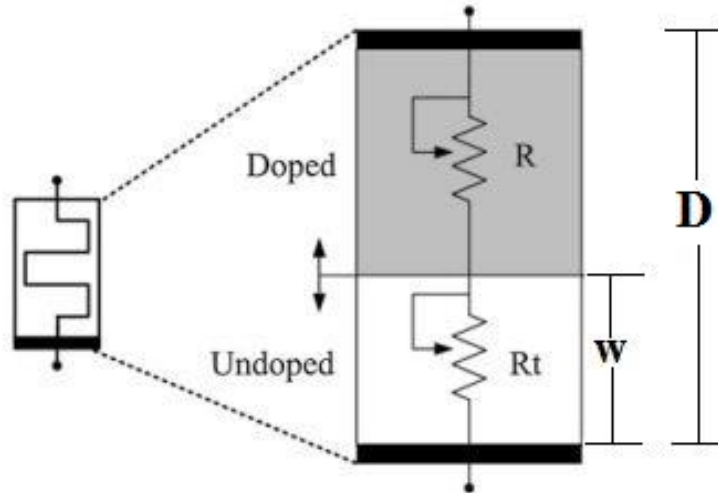
Innumerable models of memristor have been developed and available in literature as discussed in Chapter 2. Depending on application the memristor characteristics may vary. In this research, an available mathematical model – VTEAM model is used. This is flexible and has specific application in memory and can also fit to other practical memristive device [12]. It is reasonably accurate and computationally efficient, and is more appropriate for circuit simulation than other previously published models.



**Figure 4.1** Different Methods of Memristor models

#### 4.2.1 Physical model

Hewlett Packard (HP) Labs, in 2008 reported that they had realized a memristor by exploiting the nano-scale properties of thin film titanium-dioxide ( $\text{TiO}_2$ ) [8], [20]. Although, the model presented by HP revolutionized the memristor based systems but it does not match real device characteristics. Various other models, coupling the spin transport at nano-scale dimensions and current flow being used to realize memristor behavior [23], [24].



**Figure 4.2** Memristor physical model [18]

Fig. 4.2 show the physical model of memristor in which the state of memristor is described in terms of resistance attained.  $R$  is the ohmic resistance and  $R_t$  is the tunneling resistance [18]. Strukov et al. [8] proposed a model defining the physical behavior and characteristics of the memristor. Thus, a new wave of research using memristor in the circuit design was introduced. The mathematical model of the memristor is characterized by the time dependent resistance called memristance.

Memristance value depends on the history of the device (which is the quantity of the charge passed through it or on the flux linked through the device).

The proposed structure as shown in Fig. 4.2 is a semiconductor thin film (which is electrically switchable) sandwiched between two metal (Pt) nano-wires [8]. The film consist of doped ( $\text{TiO}_{2-x}$  which is a semiconductor containing vacant oxygen atoms) and un-doped ( $\text{TiO}_2$  which is an insulator) regions having a total length (D). On applying external voltage, the doped region width (w) varies due to charge dopant drifting [25] affecting the memristance of the device. Thus, the total resistivity (resistance) of the device changes as per supply voltage. If the applied voltage is such that the total doped region ( $\text{TiO}_{2-x}$ ) extends to the full length i.e.  $w/D=1$  the total equivalent resistance is  $R_{ON}$  being dominated by the low resistivity region of the device. Similarly the total resistance is  $R_{OFF}$  when the undoped region ( $\text{TiO}_2$ ) extends to full length of the device i.e  $w/D=0$ .

Time invariant memristive devices are represented by Eq (4.1) and (4.2):

$$v(t) = M(t).i(t) \quad (4.1)$$

$$M(t) = R_{ON} \frac{w(t)}{D} + \frac{R_{OFF}(1-w(t))}{D} \quad (4.2)$$

where,  $M(t)$  is the Memristance which is a function of  $w(t)$ , internal state variable.  $R_{ON}$  is the equivalent resistance of the completely doped region and  $R_{OFF}$  is the equivalent resistance of the completely un-doped region. The memristor dynamic, which gives the relation between internal state variable and current is

$$\frac{dw}{dt} = f(w, i) \quad (4.3)$$

The non-volatile characteristic of the memristor is due to its non-linear nature which make it an attractive candidate for future memory circuits.

#### 4.2.2 VTEAM model

Various models describing behavior of memristor are presented in the existing literature. In this research VTEAM model [12] which is a novel memristor model, which not only being flexible but fulfill variable threshold voltage requirement which is

beneficial for memory architecture. Memristors having such feature exhibits better performance and being reliable for memory operation, because for such application the applied power or voltage across each cell of memory architecture is fixed. The procedure of turning OFF memristor is unrelated to the variable resistance. For the mathematical modeling of memristor the state variable is defined as the ratio of its conductive or resistive part with reference to its physical length. From the physical model the state is defined as  $w/D$  i.e. ratio of doped region ( $w$ ) to the whole length of memristor ( $D$ ), and this normalize the conductive nature of memristor. The state variable derivative [12] in VTEAM model is defined as follows:

$$\frac{dw}{dt} = \begin{cases} k_{\text{off}} \cdot \left( \frac{v(t)}{v_{\text{off}}} - 1 \right)^{\alpha_{\text{off}}} \cdot f_{\text{off}}(w), & 0 < v_{\text{off}} < v \\ 0, & v_{\text{on}} < v < v_{\text{off}} \\ k_{\text{on}} \cdot \left( \frac{v(t)}{v_{\text{on}}} - 1 \right)^{\alpha_{\text{on}}} \cdot f_{\text{on}}(w), & 0 < v_{\text{on}} < v \end{cases} \quad (4.4)$$

where,  $\alpha_{\text{off}}$ ,  $k_{\text{off}}$ ,  $\alpha_{\text{on}}$ ,  $k_{\text{on}}$  are constants while  $v_{\text{off}}$ ,  $v_{\text{on}}$  are threshold voltages. The functions  $f_{\text{on}}(w)$  and  $f_{\text{off}}(w)$  act as window functions, limiting the state variable lying within the limits  $w \in [w_{\text{on}}, w_{\text{off}}]$ .

### 4.3 Simulation Results of VTEAM Model

The characteristics of the memristor is a function of type of electrical signal, and other characteristics of its like amplitude, frequency etc. Depending on the application the mathematical model of the memristor is modeled and examined to fit appropriately in the following approach.

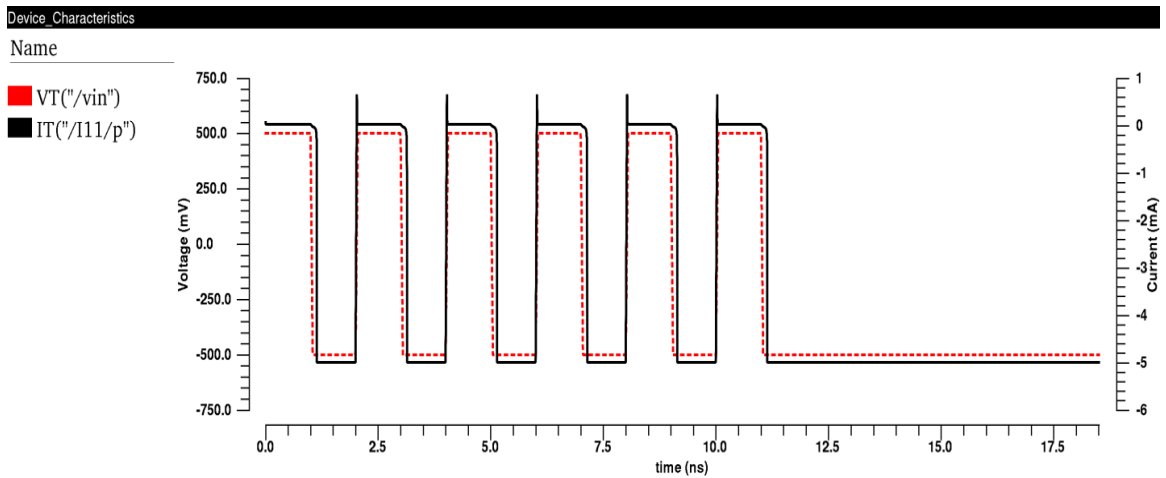
Unless stated the parameters used for modeling and simulation of memristor and circuit based on this are described in Table 4.1. Table 4.1 briefly specifies the parameters used for modeling and their value for operating the memristor at high frequency of operation of around 1 GHz. Later in the chapter some parameter variation results and their explanation is also given.

**Table 4.1** Memristor Parameters for VTEAM model

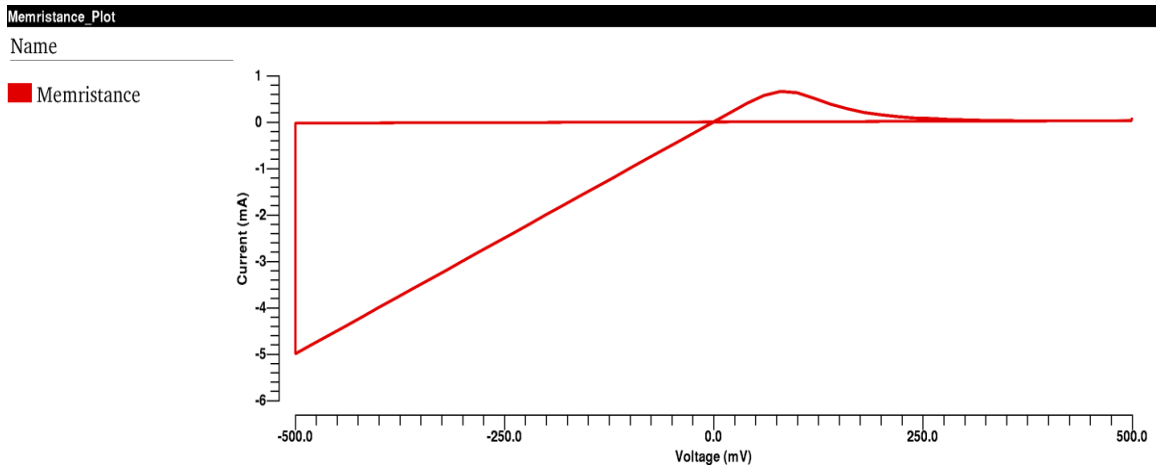
S.No.	Parameter	Description	Value
1.	dt	Infinitesimal time with which state changes, must be kept three order lower than the signal time period.	1e-12s
2.	$k_{on}$	Negative number indicating swiching rate of memristor for ON state.	-15
3.	$k_{off}$	Positive number indicating swiching rate of memristor for OFF state.	9e-2
4.	$V_{on}$	Negative number Threshold voltage for higher potential at negative terminal	-0.22V
5.	$V_{off}$	Positive no. threshold voltage for higher potential at positive terminal	0.02V
6.	$x_{on}$	Length of doped charged carriers when memristor is ON	0
7.	$x_{off}$	Length of doped charged carriers when memristor is OFF	3e-9 m
8.	$\alpha_{on}$	Non-linearity factor for higher potential at positive terminal	3
9.	$\alpha_{off}$	Non-linearity factor for higher potential at negative terminal	3
10.	$\mu_v$	Mobility of device material	350e-9 m <sup>2</sup> /Vs
11.	D	Total length of memristor	3e-9 m
12.	$R_{ON}$	ON resistance of memristor	100 $\Omega$
13.	$R_{OFF}$	OFF resistance of memristor	20 k $\Omega$

The VTEAM memristor model is simulated for different types of electrical signals and the characteristics obtained are studied. The memristor parameters must be calculated beforehand as per signal property such that the memristor switches its state completely i.e. full swing of resistance ( $R_{ON}$  to  $R_{OFF}$ ) is achievable. In the following section, square wave signals is applied across the memristor and obtained characteristics of memristor are examined and plotted.

**4.3.1 Square wave excitation:** An input square wave of amplitude 1V peak to peak and frequency 2 GHz is applied. The following graphs are obtained

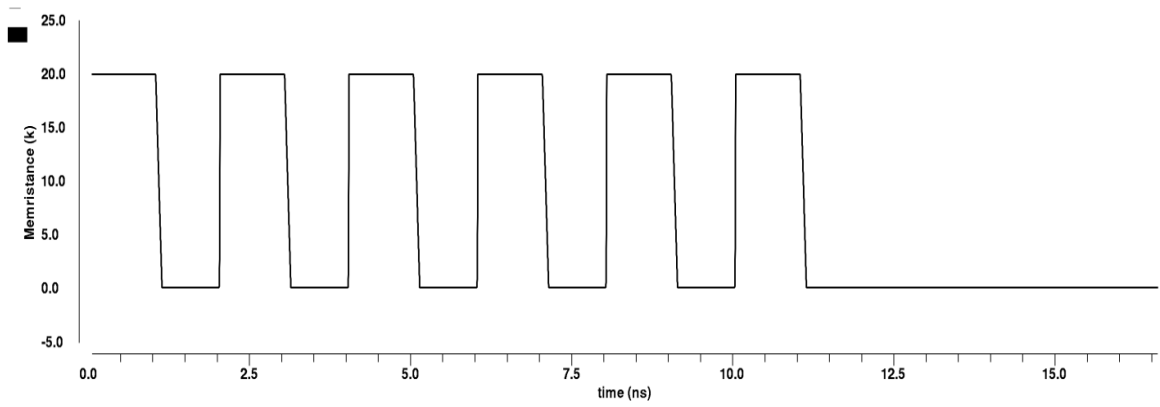


(a)



(b)

Memristance\_Plot

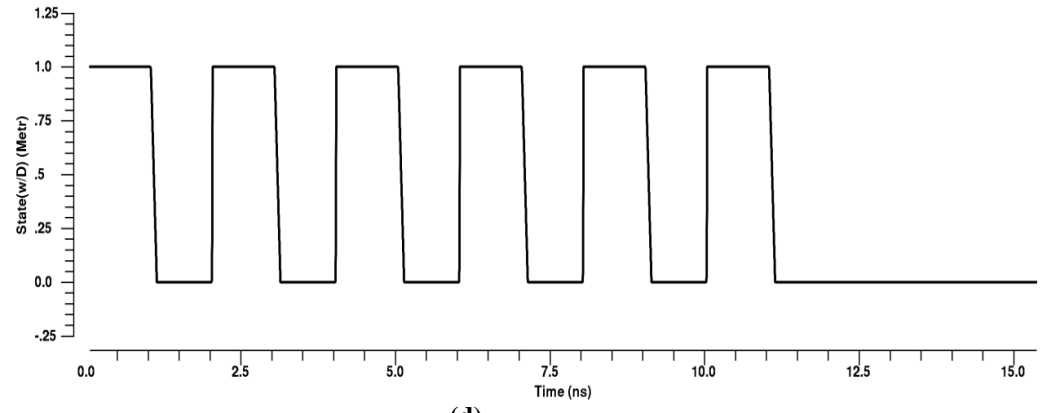


(c)

Memristance\_State

Name

■ /w



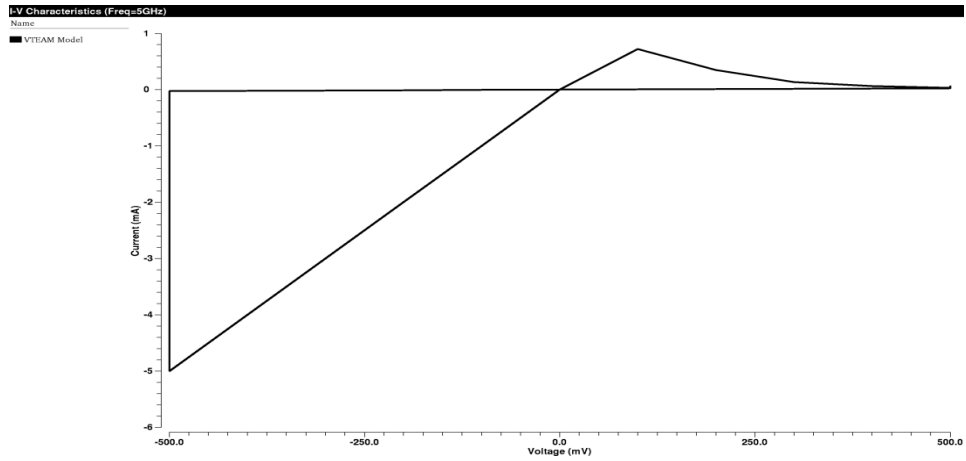
(d)

**Figure 4.3** VTEAM model simulation for square wave signal (a) Transient Response of current passing through the memristor and voltage applied across the memristor, (b) I-V characteristics of memristor, (c) Memristance ( $R_{ON}=100\Omega$  and  $R_{OFF}= 20k\Omega$ ), (d) State variable.

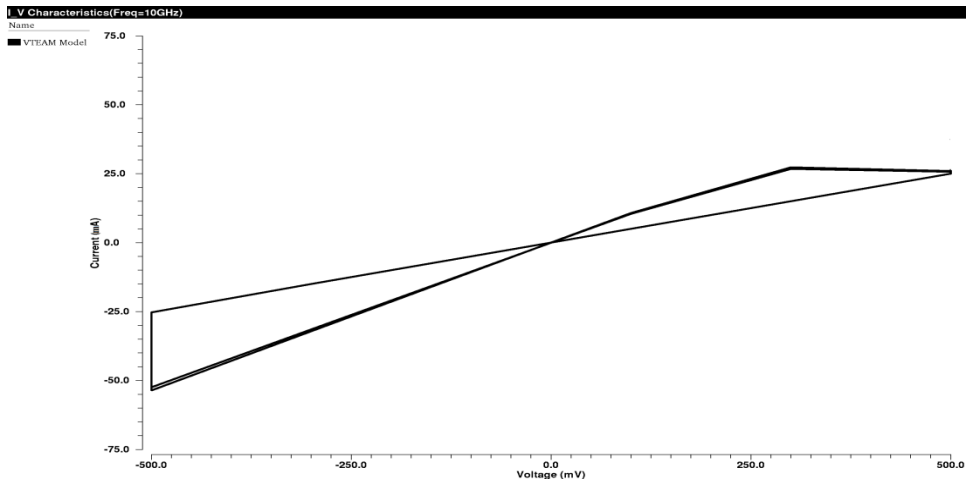
**4.3.2 Parameter Variation**

The VTEAM model of memristor is examined under different parameter variation of threshold voltage. The chosen threshold voltage is such that memristance or state variable is switched completely and the delay lies within the limits.

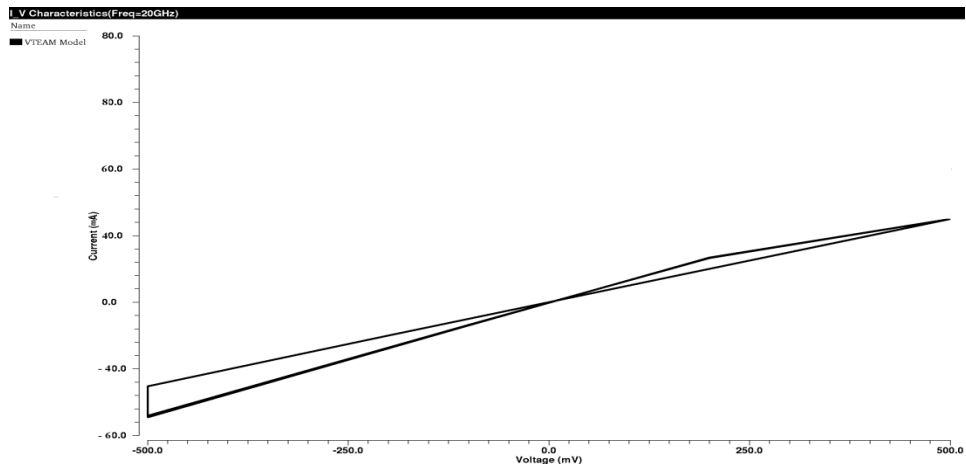
# 1) Frequency Variation



(a)



(b)

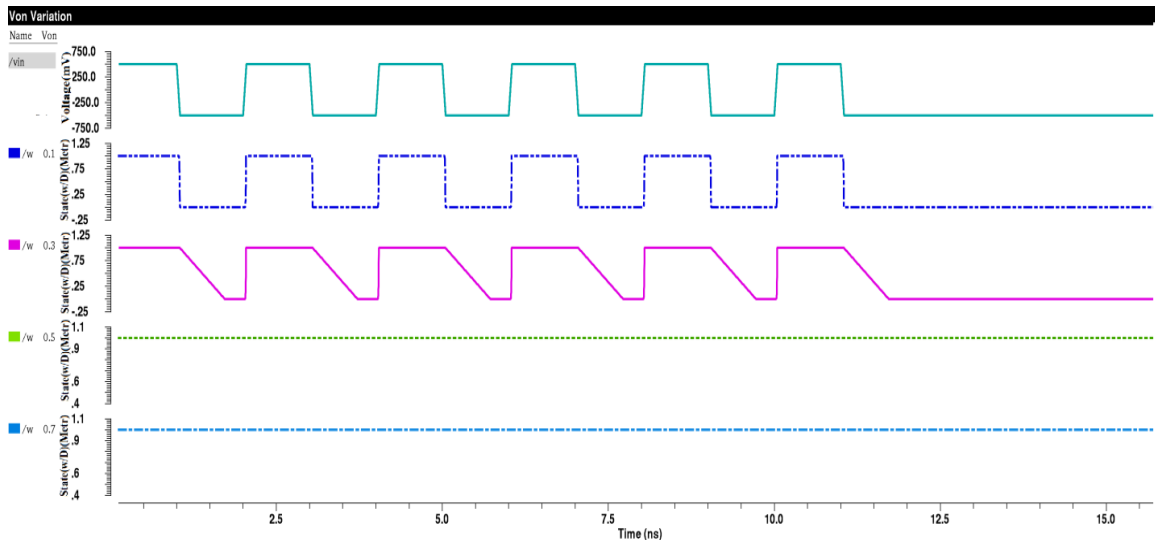


(c)

Figure 4.4 I-V curve at operating frequency (a) 5 GHz, (b) 10 GHz, (c) 20 GHz

When the frequency of applied electrical signal varied, the I-V curve was obtained shown in Fig. 4.4. The above results are simulated for input signal having a peak to peak voltage of 1V and different values of operating frequency 5 GHz, 10 GHz and 20 GHz. As the frequency increases, the peak to peak current increases also since the memristance depends on the history of current passed through it previously, therefore as the electrical signal switches to higher frequency the polarity of the signal switches faster resulting into less change in memristance. The loop continues to shrink and at very high frequency, the characteristics follow a straight line and memristor will simply act as resistor.

## 2) $v_{on}$ variation

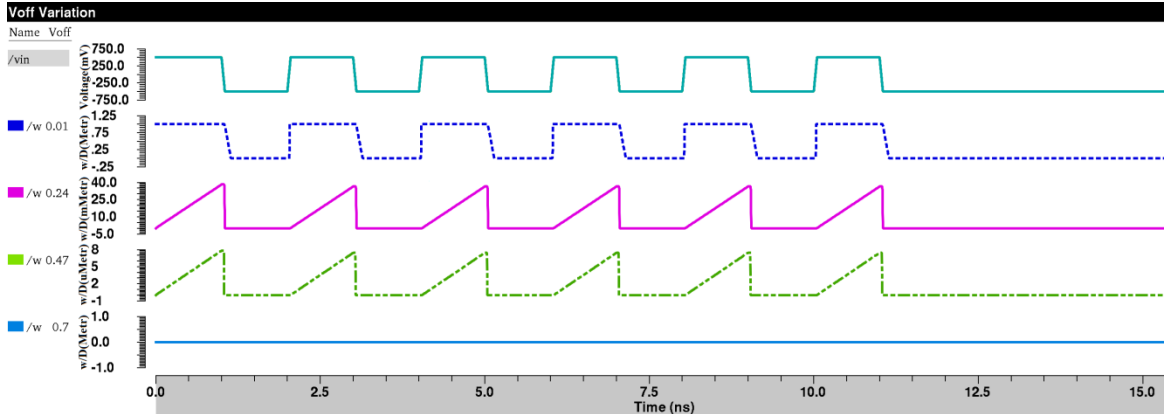


**Figure 4.5** Effect of variation of  $v_{on}$  parameter on state variable of memristor

When the threshold voltage,  $v_{on}$  varied the internal state of memristor ( $w/D$ ) gets affected. The threshold voltage  $v_{on}$  is a negative number which affects the change in memristor's state when the polarity of the applied signal is such that the negative terminal of memristor is at higher potential w.r.t its positive terminal. Fig. 4.5 depicts the memristor internal state as a function of  $v_{on}$ . The above results are simulated for input signal having a peak to peak voltage of 1V and different values of  $v_{on}$  -0.1V, -0.3V, -0.5V and -0.7V with threshold voltage,  $v_{off}$  fixed to 0.02V [12]. The simulation result shows that the applied signal amplitude in reverse polarity must be less than the threshold

voltage,  $v_{on}$  in order to make internal state or equivalently the memristance to switch completely. As the amplitude of the electrical signal increases beyond  $v_{on}$  the memristor retain its previous state only.

### 3) $v_{off}$ variation



**Figure 4.6** Effect of variation of  $V_{off}$  parameter on state variable of memristor

Similar to threshold voltage  $v_{on}$ , when the threshold voltage  $v_{off}$  varies the internal state of memristor ( $w/D$ ) gets affected but for reversed polarity of applied signal as described in case of  $v_{on}$  variation. Fig. 4.6 depicts the memristor internal state as a function of  $v_{off}$ . The above results are simulated for input signal with  $1V_{p-p}$  and for different values of  $v_{off}$  0.01, 0.24, 0.47 and 0.7 here also, same behavior is observed as described in  $v_{on}$  variation case but opposite state retains if the applied signal amplitude goes beyond the threshold voltage.

The VTEAM model of memristor is simulated for various parameters and different input signals. The parameters used for simulation are examined for memory application purpose.

## **CHAPTER 5**

# **DESIGNING OF ENERGY EFFICIENT MEMRISTOR BASED NON-VOLATILE MEMORY CELL**

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This chapter describes the design of the memristor based non-volatile memory cell using VTEAM model described in Chapter 4. The cell is compared with the existing memristor based memory cell in the literature [15], both the cells are compared on the basis of following design constraints- energy, area, speed of operation etc.

### **5.1 Proposed Memory Cell Design**

A new approach towards the design of memristor based memory cell using combination of MOS (Metal-Oxide Semiconductor) and memristor is proposed. The major advantage of the proposed cell is in terms of energy and hence, power as compared with previous work. The nonvolatile feature of the memristor is exploited for designing of memory cell in the proposed scheme making it more attractive for the non-volatile memory design.

#### **5.1.1 NMOS as a switch**

Switch is generally implemented using MOS either NMOS or PMOS or pair of complementary transistors connected in parallel called transmission gate. The controlling signal is applied at the gate terminal of MOS and the signal to be passed at the source terminal. To utilize MOS as a switch it is operated either in the saturation or cutoff mode. In the designing of the proposed memory cell NMOS is used as a switch.

#### **5.1.2 Memristor as a memory element**

Memristor as explained in chapter 3 can be utilized for memory application purpose. Like latch in SRAM or combination of one transistor and one capacitor in DRAM used for storing data, in the proposed memory cell design, memristor is utilized as a memory element. Although, memristor is not available as built-in library components in conventional circuit simulators, these simulators can still be used for

verification of the memristor based circuits by using suitable model of memristor. The proposed cell uses VTEAM model of memristor. The component description parameters of memristors used for simulation of proposed and referenced memory cell are given in table 5.1

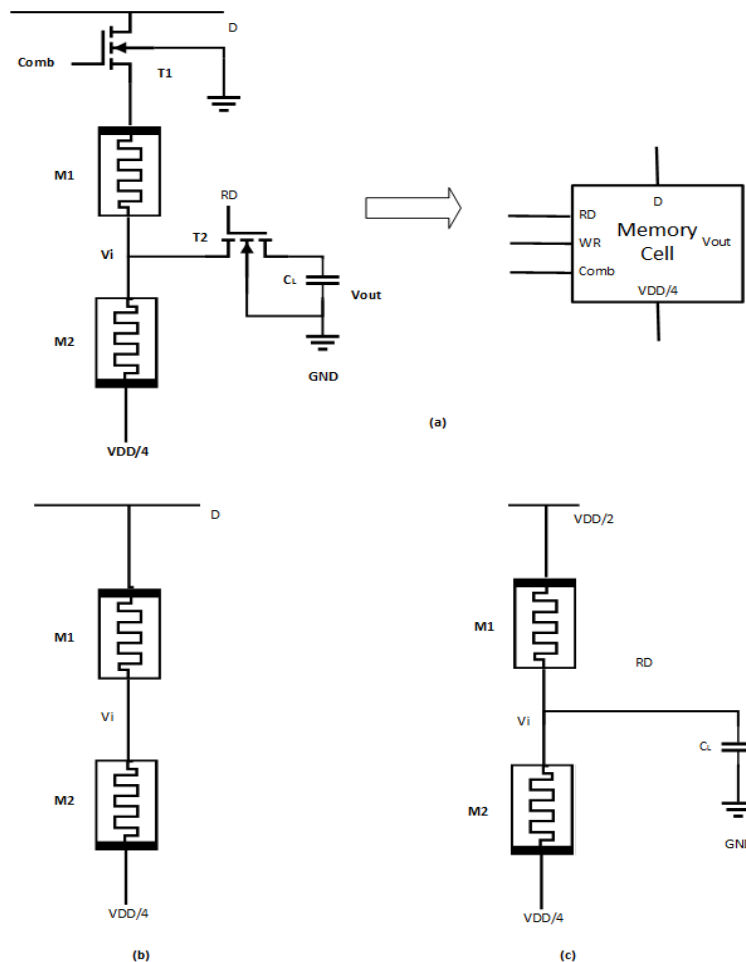
**Table 5.1** Memristor parameters for proposed and referenced memory cell

Parameters	Proposed Cell		Referenced Cell	
	M1	M2	M1	M2
$k_{on}$	-15	-15	-15	-15
$k_{off}$	9e-2	9e-2	9e-2	9e-2
$V_{T,ON}$	-0.22	-0.048	-0.22	-0.1
$V_{T,OFF}$	0.02	0.02	0.02	0.02
$x_{on}$	0	0	0	0
$x_{off}$	3nm	3nm	3nm	3nm
$\alpha_{ON}$	3	3	3	3
$\alpha_{OFF}$	3	3	3	3
$R_{ON}$	100 $\Omega$	100 $\Omega$	100 $\Omega$	100 $\Omega$
$R_{OFF}$	20k $\Omega$	20k $\Omega$	20k $\Omega$	20k $\Omega$
D	3nm	3nm	3nm	3nm
$\mu_v$	350e-9	350e-9	350e-9	350e-9

For VTEAM memristor model to fit with other previously defined memristor models low values of  $v_{off}$  is taken for simulation as explained in [12]. The value of  $v_{on}$  is dependent upon the voltage difference appears across memristor during different

memory operations. Due to different bias configuration involved in designing of memory cell the value of  $v_{on}$  varies for different memristors used in the design.

The proposed cell is shown in Fig. 5.1 the cell is made of two NMOS transistors and two memristors together acting as memory cell. The memristors act as non-volatile storage elements, while MOS transistors acting as switches are used for controlling the memristance of the cell during different operations. The transistor T1 is used to electrically isolate the memory cell from other cells of the memory array structure during different cell operations (read and write). The input gate voltage of T1 is Comb signal which electrically is the logical OR of  $W_R$  and  $R_D$  signals. The transistor T2 is used during read operation of the cell; its gate input voltage is  $R_D$  signal.



**Figure 5.1** (a) Proposed cell (b) Write operation when  $W_R=1$  and  $Comb=1$  and (c) Read operation when  $R_D=1$  and  $Comb=1$

Different memory operations on the cell are performed to confirm the workability and proper functioning. The cell was checked for non-volatility by removing all the power sources and the state of the memristor was examined before and after the power made down, also the content of the cell was studied to satisfy the proposed non-volatile feature of the memory cell.

## 5.2 Memory Operations

For the proposed memristor based memory cell the workability is defined in terms of read and write operations involved.

### 5.2.1 Write operation in proposed memory cell

During write operation, the arrangement of the cell is such that the two memristors M1 and M2 are connected (with opposite polarity) in series in a complementary resistor switch structure (or complementary memristor structure). By this arrangement the state of one of the memristor (w/D) is at 1 and the state of the other memristor (w/D) is at 0 according to the voltage levels applied. For write operation, if a bit is to be written, the  $R_D$  signal is driven LOW and the Comb signal is driven HIGH. Due to this arrangement following circuit of Fig. 5.1(b) is formed. The voltage level across the two memristors is  $(V_D - V_{DD}/4)$ . According to the voltage applied at terminal (D) the voltage across memristors is either positive (when  $V_D$  is  $V_{DD}$ ) or negative (when  $V_D$  is 0V). The arrangement of the cell is such that the change in the memristance of the two takes place in opposite direction.

For Write '0' operation, the voltage applied at terminal 'D' is 0V which make the state of memristor M1 to switch from 0 to 1 while the state of memristor M2 is switched from 1 to 0. During this operation, the voltage at the intermediate node  $V_i$  comes out to be around  $V_{DD}/4$ .

For Write '1' operation the voltage applied at terminal 'D' is  $V_{DD}$  which make the state of memristor M2 to switch from 0 to 1 while the state of memristor M1 is switched from 1 to 0. During this operation the voltage at the intermediate node,  $V_i$  comes out to be around  $V_{DD}/2$ .

### 5.2.2 Read operation in proposed memory cell

During read operation the two memristors are still connected in series. For performing read operation the gate voltage of T1, Comb signal is driven HIGH and the voltage at the intermediate node is read out by turning on the transistor T2, by applying HIGH voltage at its gate terminal  $R_D$ . Due to this arrangement following circuit of Fig.5.1(c) is formed. The stored voltage at intermediate node according to resistor divider rule [15] is given as:

$$V_i = \left( \frac{V_{DD}}{2} - \frac{V_{DD}}{4} \right) \times \frac{R_1}{(R_1 + R_2)} + \frac{V_{DD}}{4} \quad 4.2$$

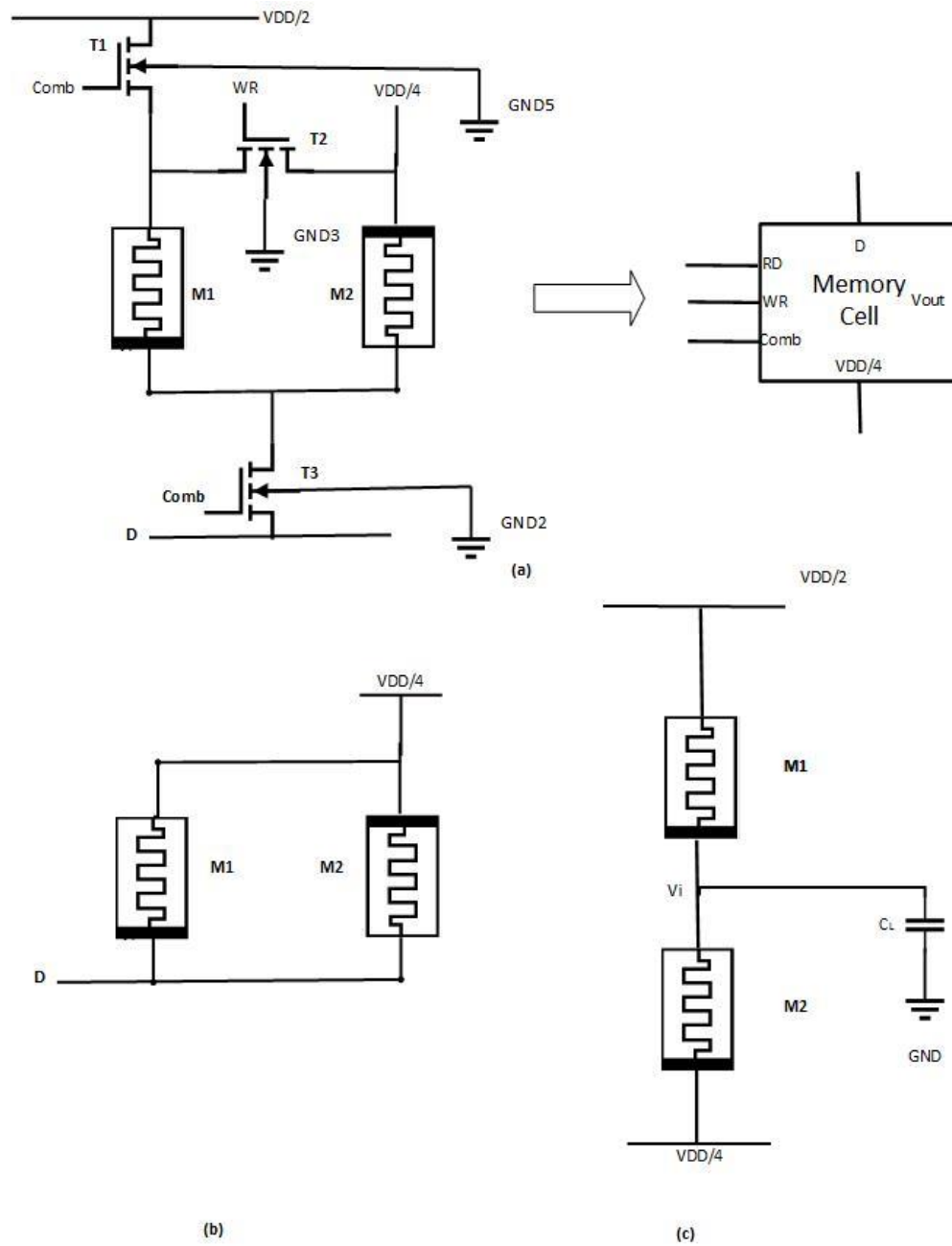
where,  $R_1$ ,  $R_2$  are the resistances i.e. memristances attained by M1 and M2 respectively. For performing write '0' operation the change in the memristances is in such a way that  $R_1$  switch to  $R_{ON}$  and  $R_2$  switch to  $R_{OFF}$  and the voltage at the intermediate node,  $V_i$  lies close to  $V_{DD}/4$ . While if '1' was written previously,  $R_1$  becomes  $R_{OFF}$  and  $R_2$  becomes  $R_{ON}$  and thus the voltage at the intermediate node,  $V_i$  lies close to  $V_{DD}/2$ . For obtaining proper voltage level swing at the intermediate node, the ratio of  $R_{OFF}/R_{ON}$  which can be represented as  $\beta$ , must be taken as high as possible.

### 5.3 Simulation Results

For the workability of any memory cell different memory operation-read and write need to be examined. The write operation of memory cell must be such that the required state successfully gets stored and read operation must be non-destructive. For the proposed cell the simulation results are presented to fulfill these requirements.

The newly proposed memory cell (in Fig. 5.1a) and the cell in [12] (also shown in Fig. 5.2a) are evaluated at GPDK 45nm CMOS technology and simulated using Cadence® Virtuoso Design tool. The nominal power supply voltage,  $V_{DD}$  is 1V. The simulations were performed for a load capacitance of 0.1fF. The actual load capacitance depends on the memory array structure and size and the fabrication process involved. The non-volatile feature of the cell has been examined and verified. Data into the cells is fed through bit-line (D). The switching of different cell operations-read and write is accomplished by the transmission gates. The voltage level at the output terminal can be interpreted correctly by giving it to the sense amplifier whose one voltage can be fixed at

say  $V_{DD}/3$  or by using CMOS inverter at the output which makes the HIGH and LOW level of the cell  $V_{DD}$  and GND respectively. Several simulations were done to test the working of the cell during different operations and also to verify that the proposed cell is non-volatile. The proposed cell is compared with the referenced cell in terms of robustness, write time, read time, area, power and energy.

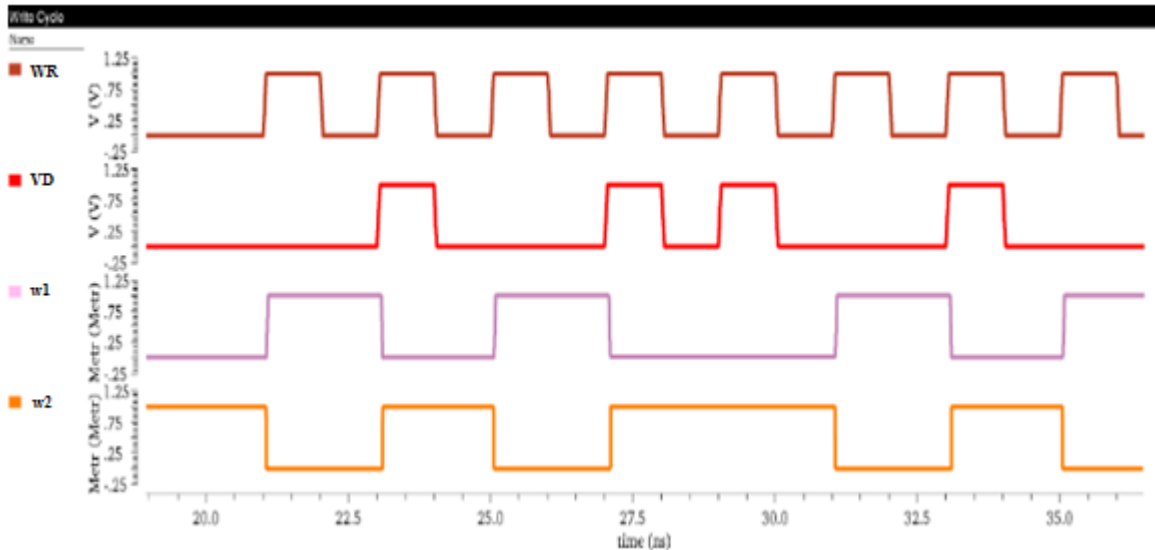


**Figure 5.2** (a) Referenced cell [15] (b) Write operation when WR=1 and Comb=1 and (c) Read operation when RD=1 and Comb=1

As shown in Fig. 5.1a different from [15] also shown in Fig. 5.2a, a new circuit configuration and bias approach is used for designing of memory cell. By using this new circuit arrangement significant improvement is observed in terms of power, area, delay and energy.

### 5.3.1 Write mode

During the first write cycle, ‘0’ was written to cell by driving the gate signal, Comb HIGH of transistor T1 and a voltage of 0V is applied at the D terminal of the cell. Write ‘0’ cycle starts from 20ns and during this, the memristor M1 attains state ‘1’ and M2 attains state ‘0’. In the next write cycle, ‘1’ was written to the same cell from 22 ns and to achieve this, a voltage level of  $V_{DD}$  is applied at the D terminal. During this M1 switches from state “1” to ‘0’ and M2 switches from state ‘0’ to ‘1’. Fig. 5.3 plot the state/memristance alteration showing the successful write operation into the memristor memory cell.

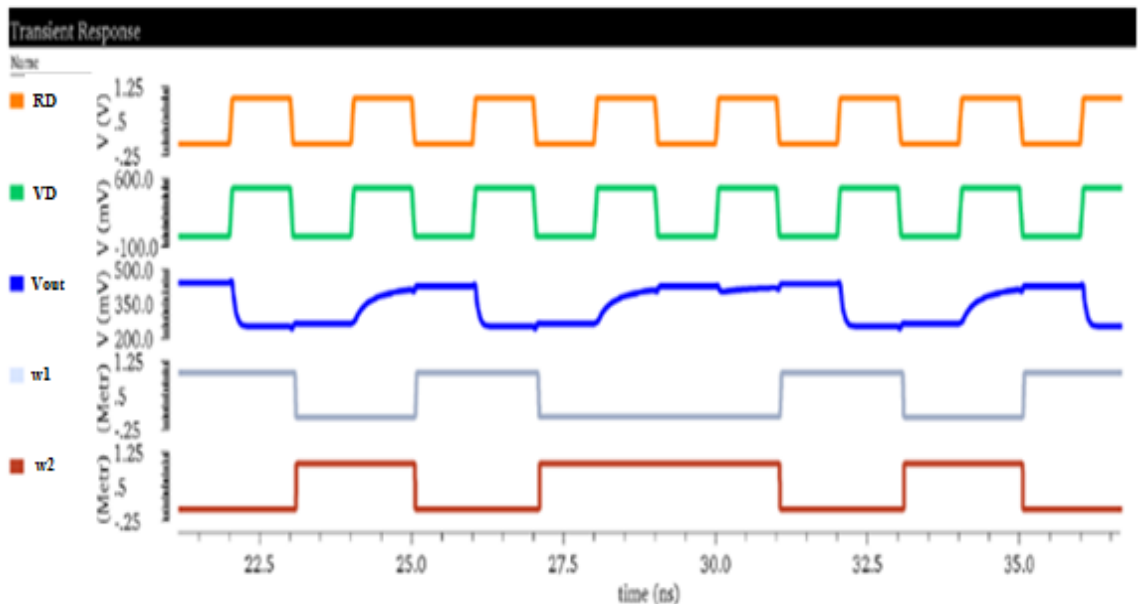


**Figure 5.3** Timing diagram during write operation

### 5.3.2 Read mode

Read operation is performed after write operation has been done successfully. This need to be non-destructive i.e. it must not change the states of the memristors which will alter the previously held data. For attaining this, proper voltage is applied across the memristors and also by selecting appropriate value of threshold voltage  $V_{T,ON}$  and  $V_{T,OFF}$ .

The memristor will not change its state until the voltage across it is greater than the threshold voltage. To read out the stored data the gate voltage signal of T1 (Comb signal) and T2 ( $R_D$  signal) are driven HIGH also a voltage of  $V_{DD}/2$  is applied at the D terminal of the cell. After writing “0” read operation is performed and the voltage of the intermediate node,  $V_i$  is read out and it comes out to be 0.228V close to 0.25 ( $V_{DD}/4$ ) LOW level of the cell. Similarly, after writing “1” from 23 ns read operation is performed again on the cell and during this time it comes out to be 0.409V close to 0.5 ( $V_{DD}/2$ ) HIGH level of the cell. Fig. 5.4 plots the timing diagram of read cycle, and it shows that the data found is exactly the same as being written previously into the cell. Thus, the cell shows that the read and write operations are happening successfully.

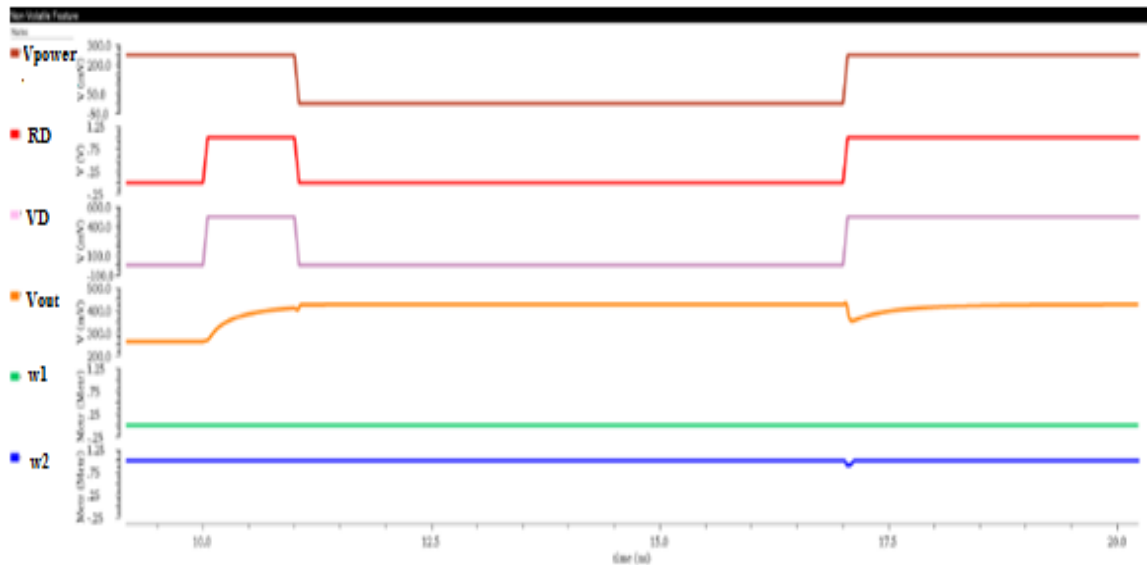


**Figure 5.4** Timing diagram during read operation

### 5.3.3 Stand-by mode (Non-volatile feature)

The proposed memory cell is non-volatile in nature. After writing “1” into the cell, the memory cell was powered down (standby) i.e. all power sources were removed during the time interval 11-17 ns (Fig. 5.4). For performing read operation all the power sources are turned on and the content of the cell is found to be “1” same as before turning off all the power sources. This verifies the non-volatile nature of the proposed cell. A slight dip (negative) in the voltage level is seen when reading the content of the cell after standby mode. This happens due to injection of current into the supply, when

the output slightly overshoots power supply voltage as a result of capacitive coupling between input and output terminals of the circuit.



**Figure 5.5** Timing Diagram during Standby mode

## 5.4 Comparative Analysis

The proposed memory cell and the cell in [15] are simulated for various memory operations. Different operation of memory (read followed by write) are verified and the delay found by simulation are tabulated in Table 5.1.

**Table 5.1** Comparison of read/write time of proposed memory cell and cell reported in [15]

Memory Operations	Proposed Cell (ps)	Referenced Cell (ps)	Percentage Improvement
Write '0'	57.88	60.61	4.5
Read '0'	198.3	273.2	27.42
Write '1'	74.86(51.86)	57.14	9.24
Read '1'	357.9	384.8	6.99

The read cycle time of the memory cell majorly depends on the performance of the sense amplifier, its sensitivity and responsiveness. Speed of operation of memory cell which is determined by the delay of the circuit is an important design constraint. The frequency of operation of the memory cell can be derived by the worst case delay of all the combination of memory cell.

The total power dissipation curve of the memory cell was found during the simulation. Since energy is the product of power and time therefore integration was done to obtain the energy dissipated per cycle for different read (read “1” and read “0”) and write (write “1” and write “0”) operations. The results obtained are summarized in Table 5.2 & 5.3. The energy/cycle is the quality measure of the cell which determines its performance. The proposed cell has a much low value of energy/cycle and hence power dissipation, which is suitable for designing high density memory. Since read time is a function of sense amplifier it can be reduced further as the author [15] has also suggested by designing more efficient and faster sense amplifier which reduces the read time further and hence the power.

EDP combines measure of performance and energy together and is a more relevant design metric. EDP has voltage dependence for higher supply voltages delay is reduced but energy gets harmed similarly, for low supply voltages delay is harmed while energy is improved. The table 5.2 and 5.3 also shows the EDP obtained via simulations.

The authors in [15] used spice model for simulating their memristor based memory cell and compared their results with the conventional 6T SRAM. The results of the reported cell were better in terms of delay, energy and power. Only the write ‘1’ of the reported memristor based cell came higher than that of conventional 6T SRAM. Also the area of the referred cell is much smaller than the conventional 6T SRAM.

In order to compare the proposed memory cell described in this thesis work, with the referred cell, the referenced cell (Fig. 5.2a) is also simulated using VTEAM model of memristor and the simulation results obtained are analyzed for comparison.

**Table 5.2** Comparison of Energy and Power dissipation during write operation of proposed memory cell and cell reported in [15]

	Write '0'			Write '1'		
Parameters	Proposed Cell	Referenced Cell	Percentage Improvement	Proposed Cell	Referenced Cell	Percentage Improvement
Energy(fJ)	10.34	84.53	87.77	13.43	899.1	98.51
Peak Power ( $\mu$ W)	520.51	579.68	10.21	456.69	1016.08	55.05
EDP (fJ ns)	598.48	5123.36	88.32	696.48	51374.57	98.64

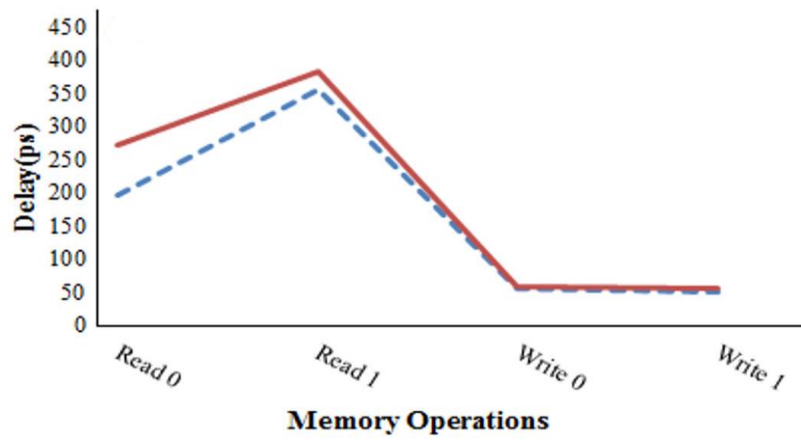
**Table 5.3** Comparison of Energy and Power dissipation during read operation of proposed memory cell and cell reported in [15]

	Read '0'			Read '1'		
Parameters	Proposed Cell	Reference d Cell	Percentage Improvement	Proposed Cell	Referenced Cell	Percentage Improvement
Energy(fJ)	10.92	14.83	26.37	13.97	25.53	45.28
Peak Power ( $\mu$ W)	429.52	385.49	-10.25	498.41	980.58	49.17
EDP(fJ ns)	2165.44	4051.56	46.55	4999.86	9823.94	49.10

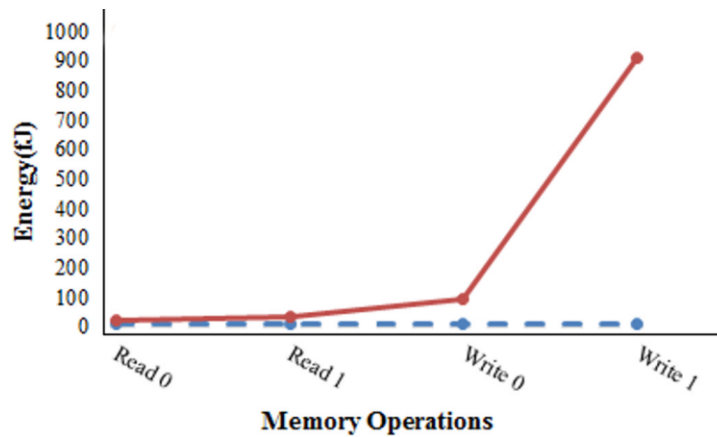
For the proposed cell and the cell in [15] different memory operations are performed and the simulations results obtained for major design scenarios delay, energy,

energy delay product (EDP) and peak power are plotted in Fig. 5.6. The cells have lower cell margin as can be seen from the simulation results during read “0” the maximum voltage seen at the capacitive node is  $V_{DD}/4$ , similarly during read “1” operation it comes out to be “ $V_{DD}/2$ ”. From memory design perspective, the reduced noise margin is tolerable within memory core, where noise conditions and signal interferences can be carefully controlled. Full voltage swing is required to be restored when signals goes into the external world. This is achieved by using highly efficient peripheral devices like sense amplifier. Other alternatives like CMOS inverter which has appropriately adjusted switching threshold voltage can also be used.

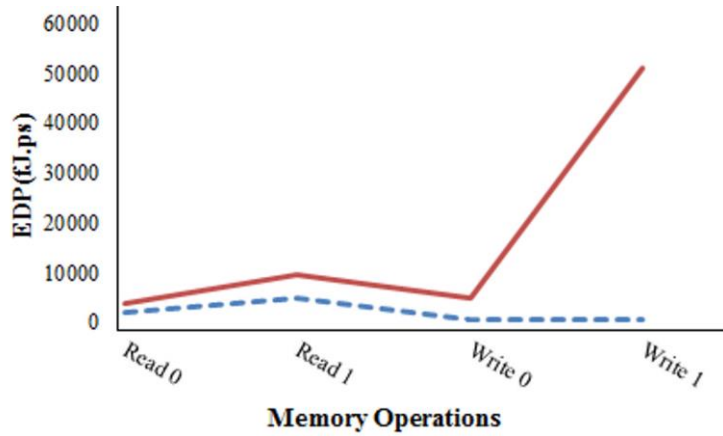
It has also been observed from the circuit diagram of the proposed cell that it consumes less area as compared to the referenced cell. Further reduction in area can also achieved by switching to more recent fabrication technologies.



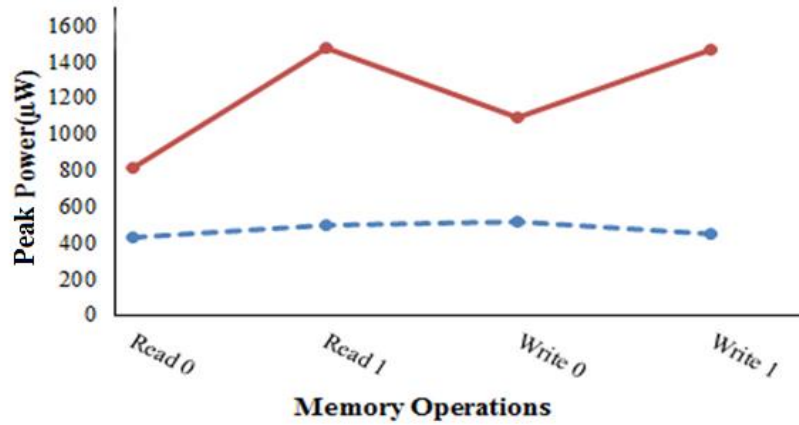
(a)



(b)



(c)



(d)

**Figure 5.6** Performance vs Memory operations (a) Delay (b) Energy (c) EDP (d) Peak power

The plot shown in Fig. 5.6 depicts that the proposed cell is more robust than the previously proposed memristor-based cell in literature [12]. In the proposed memory structure the read and write terminals are separated, which results into significant improvement in various performance criteria. The performance of the previously proposed memristor cell is improved in terms of power, energy, area and speed of operation. One of the major advantages of the proposed cell is in terms of energy/cycle. As energy of the circuit is a measure of the amount of power drawn from the power supply over a period, also energy majorly affects circuits mainly battery operated a system so minimizing energy of the memory cell for such system is essential.

## CHAPTER 6

### CONCLUSION AND FUTURE PROSPECTS

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#### 6.1 Concluding Remarks

With the increasing demand of high storage memories either embedded or on die new technologies has to be proposed. These new technologies should fulfil the demand of scalability, reliability and high density. They have to be energy or power efficient and should have low manufacturing cost. Since the introduction of memristor many research efforts have been put in using it for various applications but its major scope lies in memory architecture especially non-volatile.

The research work in the thesis presents non-volatile memory cell utilising memristor as a memory element. The circuit find wide applications in areas of data storage. The simulation results using Cadence Virtuoso Analog Design Environment at 45nm technology have been used to demonstrate the functioning of the proposed memory cell. Based on the simulation results, it is concluded that this memory cell circuit exhibits low power dissipation and consumes less energy. Being energy-efficient it can be used for the implementation of the applications majorly in areas of battery operable devices. A vast improvement in the speed of operation of the circuit is also observed which further improves the circuit performance. Also the observed area, which is an important aspect for achieving high density, is quite less as compared to previous quoted work [15].

#### 6.2 Future Prospects

The research work proposed in the thesis presents Memristor as a memory element and demonstrate a memory cell technique that can help design of non-volatile memory applications overcoming various design constraints described earlier. By utilising the proposed memory cell of this work as building blocks for high density memory architecture, especially for low voltage/ low power and dense circuits such as battery driven can be easily developed with greater reliability and higher performance. In

recent years many memristor based circuit techniques has been reported in literature which offers many advantages in various aspects.

The future scopes of memristor based circuits are as follows:

- Memristors can be as small as 3nm. Thus, the area of the memristor based memory cell can be reduced further by switching to more recent fabrication technologies.
- The proposed memory cell can be designed to operate at lower supply voltage, resulting into further reduction in power dissipation.
- The voltage levels obtained for logic '1' and logic '0' state can be improved to obtain rail to rail swing.

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## LIST OF PUBLICATIONS

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- Kavita Bhagnani, Sanjay Sharma, Sakshi Bajaj “Design of low power memristor based non-volatile memory cell” communicated in *Microelectronics Journal, Elsevier*.

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