

Design of a high speed and low power Sense Amplifier

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the requirement for the award of degree of*

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in

VLSI Design & CAD

Submitted by

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Declaration

I hereby declare that the dissertation report entitled "Design of a high speed and low power Sense Amplifier" is an authentic record of my work carried out as requirement for the award of degree of M.Tech (VLSI Design & CAD) at Thapar University, Patiala, under the supervision of Mr. Arun Kumar Chatterjee, Assistant Professor, ECED and refers other researcher's work which are duly listed in the reference section.

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It is certified that the above statement made by the student is correct to the best of my knowledge and belief.

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Abstract

Sense Amplifier is one of the most important part of the memory. It is used to access the stored data in bit cell during read cycle. Sense amplifier amplifies the small difference between bitlines to the full swing level. Its performance affects the access time and power dissipation of memory and hence by reducing the sensing delay and power consumption of sense amplifier the performance of memory improves.

A 6T SRAM has been designed using Cadence Spectre 5.1.4 1_ISR for the various sizes of transistors to store the data and to retrieve the data from it. The layout of 6T SRAM has been also designed to calculate the bitline capacitance of a bit cell using Cadence Virtuoso 5.1.4 1_ISR layout editor and for RC extraction of layout Cadence Assura 3.2.0 is used. The different circuits of sense amplifiers such as cross coupled, clamped bitline, latch type and hybrid type are studied and compared. On basis of different circuits of sense amplifiers a new high speed and low power sense amplifier has been designed at 0.18 μm technology.

Extensive results at 0.18 μm CMOS technology using Cadence Spectre 5.1.4 1_ISR simulation tools have been observed for different sense amplifier circuits. The sensing delay of different types of sense amplifiers are evaluated with respect to variation in bitline capacitance and variation in power supply. The average power for different values of bitline capacitance has been also analyzed. From these results it has been observed that delay of sense amplifier circuit is dependent mainly on the capacitance of the bitlines from the memory cell. By isolating these bitline capacitances the sensing delay can be reduced very much. The comparison of designed sense amplifier has been carried out with the different types of sense amplifiers using 0.18 μm technology. The designed sense amplifier has been about 40-80% faster than other sense amplifiers.

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List of Symbols

dQ	Charge stored on precharged bitlines
V_{DD}	Positive supply voltage
GND	Ground
I_{DATA}	Memory cell current during read
dV_{BL}	Bitline voltage swing
K_p	PMOS process trans-conductance parameter
K_n	NMOS process trans-conductance parameter
W	Channel Width
L	Channel length
μ_n	Mobility of electrons
μ_p	Mobility of hole
C_{BL}	Bitline capacitance
R_{BL}	Bitline Resistance
V_{Tn}	Threshold voltage of NMOS
V_{Tp}	Threshold voltage of PMOS
μm	micro meter
pF	pico Farad
mW	milli Watt
ns	nano second
V	volt
mV	milli Volt

Abbreviations

SRAM	Static Random Access Memory
CMOS	Complementary Metal Oxide Semiconductor
VLSI	Very Large Scale Integration
IC	Integrated Circuit
ITRS	International Technology Roadmap for Semiconductors
MOSFET	Metal Oxide Semiconductor Field Effect Transistor
BL	Bitline
BLB	Bitline bar
CR	Cell Ratio
PR	Pull up Ratio
SE	Sense Enable
EN	Enable
PRE	Precharge
NMOS	N-channel Metal Oxide Semiconductor
PMOS	P-channel Metal Oxide Semiconductor
CAD	Computer Aided Design
VTCMOS	Variable Threshold Complementary Metal Oxide Semiconductor
MTCMOS	Multi Threshold Complementary Metal Oxide Semiconductor
6T	Six Transistor
cbl	clamped bitline

1.1 INTRODUCTION

Sense amplifiers [1] are one of the most important critical circuits in the periphery of CMOS memories. Their performance strongly affects both memory access time, and overall memory power dissipation. As with other ICs today, CMOS memories are required to increase speed, improve capacity and maintain low power dissipation. These objectives are somewhat conflicting when it comes to memory sense-amp design. With increased memory capacity usually comes increased bitline parasitic capacitance. This increased bitline capacitance which in turn slows down voltage sensing and makes bitline voltage swings energy expensive resulting in slower and more energy hungry memories.

Due to their great importance in memory performance sense amplifiers have become a very large class of circuits. Their main function is to sense or detect stored data from a read selected memory cell. Figure 1.1 shows a typical use of a sense amplifier.

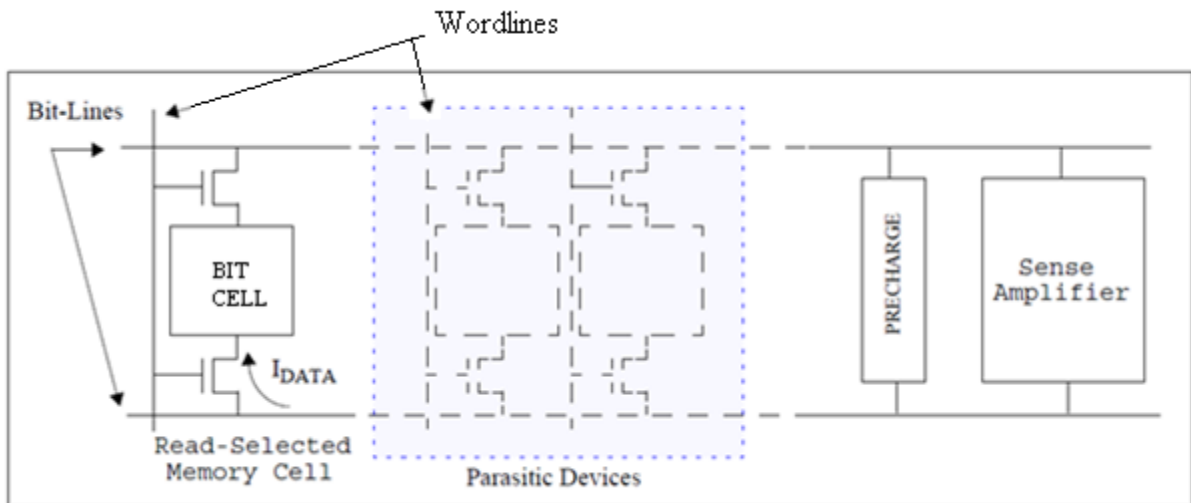


Figure 1.1 Typical use of a sense amplifier

The memory cell being read produces a current " I_{DATA} " that removes some of the charge(dQ) stored on the precharged bitlines. Since the bitlines are very long, and are shared by other

similar cells, the parasitic resistance " R_{BL} " and capacitance " C_{BL} " are large. Thus, the resulting bitline voltage swing (dV_{BL}) caused by the removal of " dQ " from the bitline is very small $dV_{BL} = dQ/C_{BL}$. Sense amplifiers are used to translate this small voltage signal to a full logic signal that can be further used by digital logic.

The need for large memory capacity, high speed, and low power consumption has defined a new operating environment for future sense amplifiers. There are some of effects of large memory capacity and low supply voltage:

- 1) With increase in the number of memory cells per bitline increases C_{BL} , while an increase in length of the bitline increases R_{BL}
- 2) For large memory capacity integrate more memory on a single chip reduces the current I_{DATA} . This coupled with increased C_{BL} causes an even smaller voltage swing on the bitline.
- 3) With low supply voltage results in smaller noise margins.

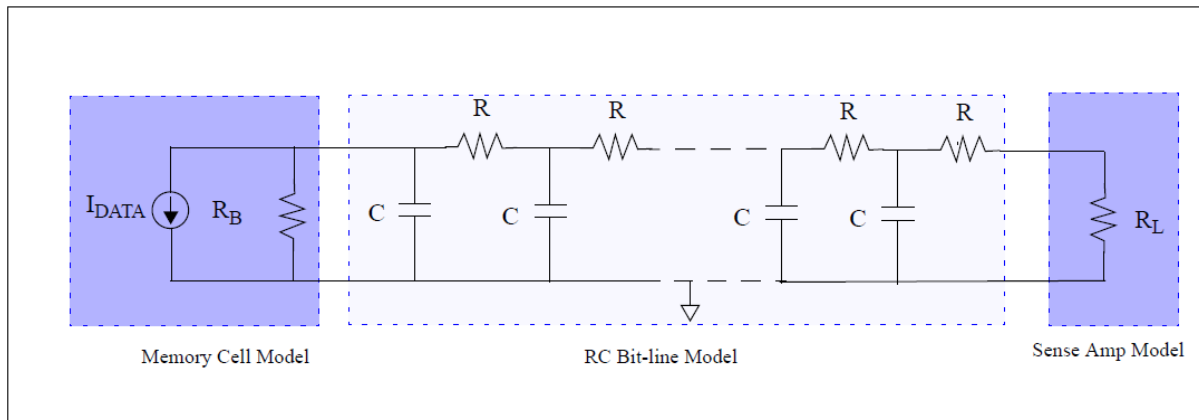


Figure 1.2 Equivalent sensing circuits [2]

From the above model shown in Figure 1.2 we can derive the delay transfer function [3] as:

$$\delta_T = \frac{(R_T * C_T)}{2} \left(\frac{R_B + \frac{R_T}{2} + R_L}{R_B + R_T + R_L} \right) + (R_B * C_T) \left(\frac{R_L}{R_B + R_T + R_L} \right) \quad 1.1$$

where R_T and C_T are the total bit-line resistance and capacitance

Since voltage-sense amplifier has close to infinite input impedance while the current sense amplifier has zero input impedance, the above delay equation 1.1 simplifies to the following two equations, 1.2 voltage sensing delay [3] and 1.3 current sensing delays [3]

$$\delta_T = \frac{(R_T * C_T)}{2} \left(1 + \frac{2R_B}{R_T} \right) \quad 1.2$$

$$\delta_T = \frac{(R_T * C_T)}{2} \left(\frac{R_B + \frac{R_T}{3}}{R_T + R_B} \right) \quad 1.3$$

1.2 Motivation

Modern digital systems require the high speed memories for storing and retrieving large amounts of data. Among all memories, SRAM (Static Random Access Memory) is widely used due to its high speed and low power consumption. According to 2002 ITRS [4](International Technology Roadmap for Semiconductors), the 90% area of a chip is occupied by memory by 2013. As the operating speed increases, the chip size also increases so with increase in chip size the power consumption by circuit becomes very important. Each generation of CMOS SRAMs has advanced by reducing the memory cell size by about one-third and increasing the chip size by approximately 1.5 times with the advances in integrated circuit technology, the density of SRAMs in embedded applications has grown substantially in recent years. This has resulted in increase in bit and data lines capacitances thereby constituting a major bottleneck in achieving higher sensing speed in memory systems.

The three most important parameters in a memory system are

- Power
- Speed
- Area

The speed of VLSI chips is increasingly limited by signal delay in long interconnect lines. Major speed and power improvements are possible when using current mode rather than voltage mode signal transporting techniques. Moreover, with current mode sensing, reduction in the size of memory cell is another possibility. Since most of the memory related operations are read operations, this causes a large saving in the overall power dissipated by the memory. Also as sense amplifiers dissipates large quantity of short circuit power as opposed to the dynamic power dissipated by the cell array, large power is saved.

The need for the robust design of low power high speed CMOS analog VLSI circuits is growing tremendously. This growth is due to the technological forces that comes from the reduction of the minimum feature size to scale down the chip area. Scaling down the transistor size can then integrate more circuit components in a single chip area and lowers the cost. Also smaller geometry usually lowers the parasitic capacitances, which means higher operating speed and lower power consumption.

1.3 Thesis organization

Chapter 1 describes introduction and motivation for Sense amplifier used in SRAM.

Chapter 2 describes the architecture of SRAM, operation and different types of sense amplifiers.

Chapter 3 includes design of sense amplifier.

Chapter 4 deals with results and comparison.

Chapter 5 deals with conclusions and future scope.

2.1 SRAM architecture

A conceptual block diagram of SRAM architecture [5] shown in Figure 2.1 below. The description of various blocks of SRAM is as:

2.1.1 Bit Cell: The data storage cells arranged in an array of horizontal rows and vertical columns. Each bit cell is capable of storing one bit of data. This structure can access any cell by accessing a particular row and a column. The horizontal lines, which are driven from outside of bit cell to store or retrieve the data, are called wordline, while the vertical lines through which data flow into and outside of array are called bitlines.

2.1.2 Row Decoder: To access a particular bit cell, corresponding wordline and bitline must be selected according to address coming from the address buffer. Row selection operations are performed using row decoder. The row decoder selects one out of 2^n wordlines according to n-bit row address.

2.1.3 Column decoder: Column selection operations are performed using column decoder, this circuit selects one out of 2^m bitlines according to an m-bit column address. Once a memory cell is selected using row and column decoder, data read and write operation is performed. The column decoder also routes the corresponding data content in a selected row to the output through the data output buffers.

2.1.4 Precharge Circuit: Various read and write operations are being performed on bit cell so before any operation is to be performed we have to set the bitlines at a particular level, so precharge circuit is used to pull up the bitlines. Precharge circuit is also used to equalize the potential at bitlines.

2.1.5 Sense Amplifier: One of the most important circuitry of SRAM, it is used to amplify the small difference of bitlines upto full swing. Sense amplifier is related with the read

access time. Sense amplifier is an active circuit that reduces the time of signal propagation from an accessed memory cell array.

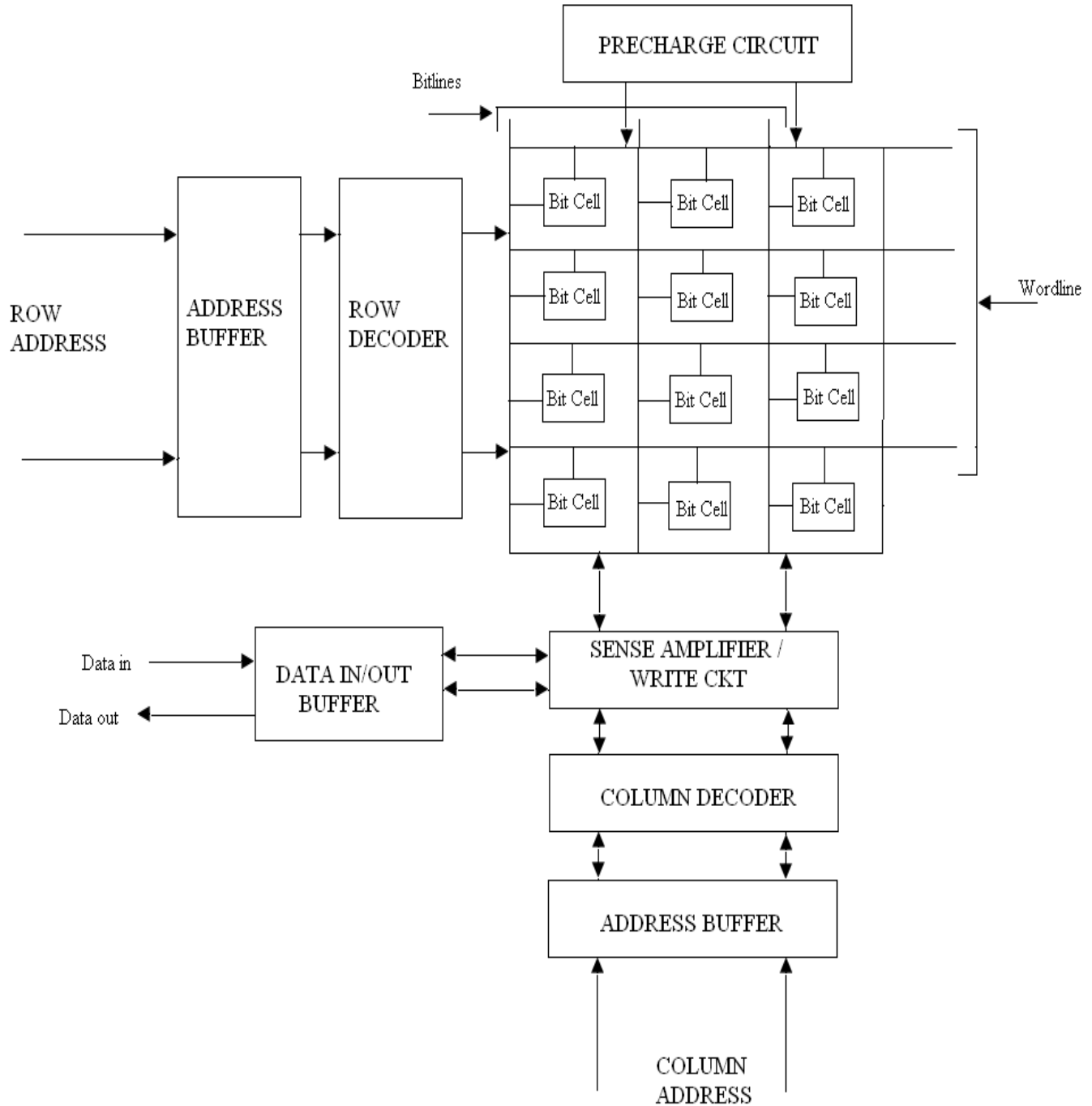


Figure 2.1 Block diagram of SRAM architecture [5]

2.2 Static Random Access Memory (SRAM)

SRAM [6] utilizes a flip flop mechanism, it does not need to be refreshed but it is volatile memory. The SRAM cell should be sized as small as possible to achieve high memory densities. Reliable operation of the cell imposes some sizing constraints. The Six-transistor CMOS RAM cell is shown below in Figure 2.2:

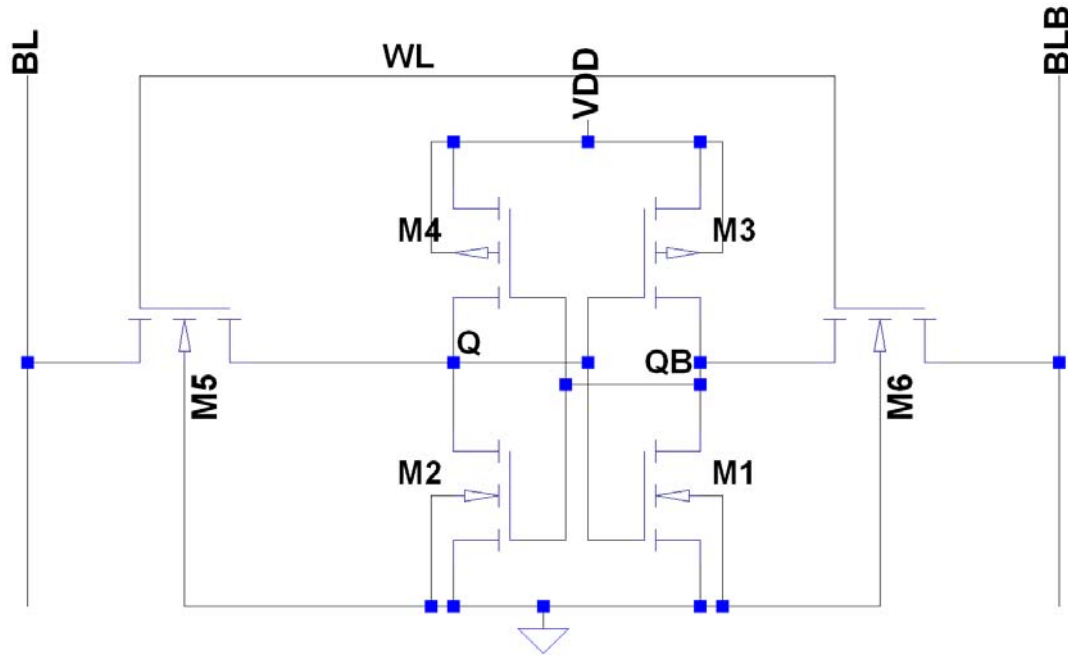


Figure 2.2 Six transistor CMOS SRAM cell. [6]

To understand the operation of memory cell, let us consider the read and write operations.

2.2.1 SRAM Read Operation

In read operations let consider that 0 is stored at Q. Both bitlines are precharged to V_{DD} before the read operation is initiated. The read cycle is initiating by enabling the wordline high, both transistors M5 and M6 turns on. During correct read operation, the values stored in Q and QB are transferred to BL and BLB by leaving BLB at its precharge value and and by discharging BL through M5 and M2 transistors. A careful sizing of transistors must be there to avoid any false results.

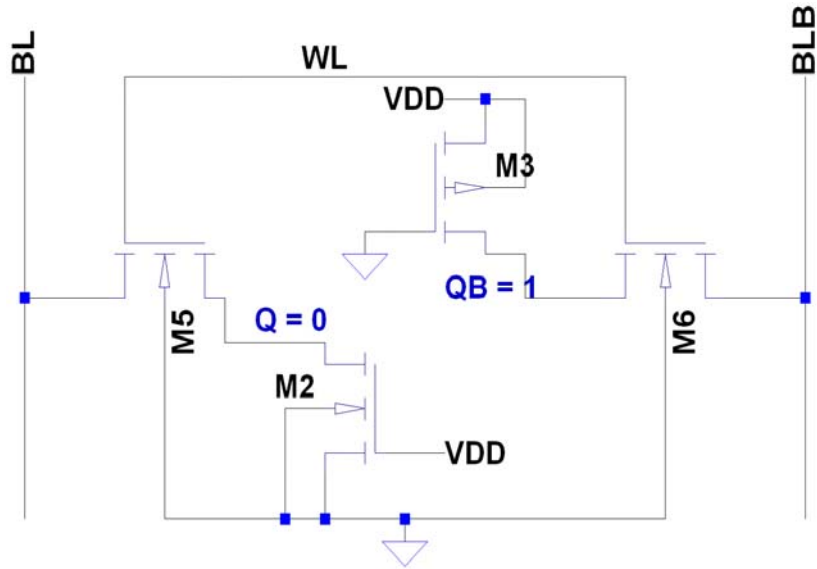


Figure 2.3 CMOS SRAM cell during read. [7]

The boundary constraints on the device sizes can be derived by solving the current equation at the maximum allowed value of voltage ripple ΔV . We ignore the body effect on transistor M5 for simplicity and write

$$k_{n,M5}((V_{DD} - \Delta V - V_{Tn})V_{DSATn} - \frac{V_{DSATn}^2}{2}) = k_{n,M2}((V_{DD} - V_{Tn})\Delta V - \frac{\Delta V^2}{2}) \quad 2.1$$

$$\Delta V = \frac{V_{DSATn} + CR(V_{DD} - V_{Tn}) - \sqrt{V_{DSATn}^2(1+CR) + CR^2(V_{DD} - V_{Tn})^2}}{CR} \quad 2.2$$

Where CR is called the cell ratio and is defined as

$$CR = \frac{W_2/L_2}{W_5/L_5} \quad 2.3$$

To keep the node voltage from rising above the transistor threshold, the cell ratio (CR) must be greater than 1.2 [7]

2.2.2 SRAM Write Operation

The operation of writing 0 or 1 is accomplished by forcing one bitline low while other remains at V_{DD} . In Figure 2.2, to write 1, BLB is forced low and to write 0, BL is forced low. In Figure 2.3, we have to write 0, so BL is forced low. The cell must be designed that the conductance of M3 is several times larger than M6 so that drain of M3 is pulled below V_S . This initiates a regenerative effect between the two inverters. Eventually M1 turns off and its drain voltage rises to V_{DD} due to pull up action of M5 and M2. At the same time M2 turns on and assist M5 to pulling output Q to low value. By keeping the proper sizes of the transistors, the transistor M5 will discharge the node Q very fast as compare to the charging of the node by transistor M3

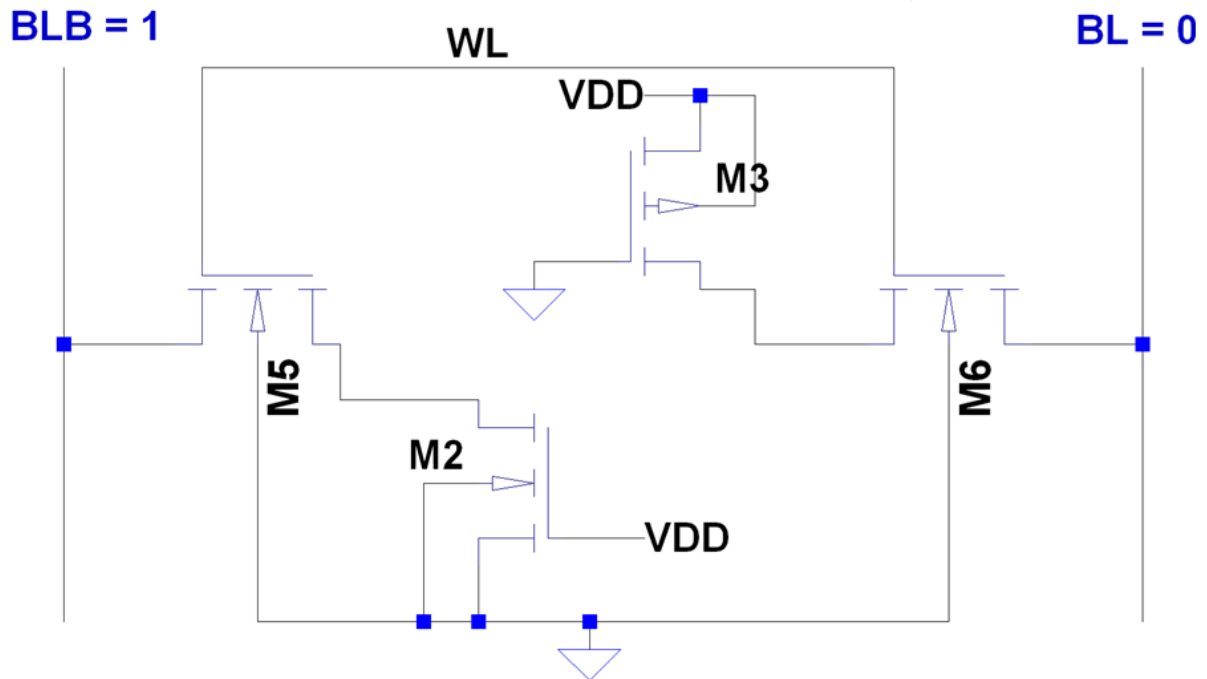


Figure 2.4 CMOS SRAM cell during write. [7]

A reliable writing of the cell is ensured if we can pull node Q low enough, this is below the threshold value of transistor M1. The conditions for this to occur can be derived by writing out dc current equations at the desired threshold point, as follows:

$$k_{n,M6} \left((V_{DD} - V_{Tn})V_Q - \frac{V_Q^2}{2} \right) = k_{p,M3} \left((V_{DD} - V_{Tp})V_{DSATp} - \frac{V_{DSATp}^2}{2} \right) \quad 2.4$$

Solving for V_Q leads to

$$V_Q = V_{DD} - V_{Tn} - \sqrt{(V_{DD} - V_{Tn})^2 - 2 \frac{u_p}{u_n} \left((V_{DD} - V_{Tp})V_{DSATp} - \frac{V_{DSATp}^2}{2} \right) * PR} \quad 2.5$$

Where the PR is the pull up ratio of the cell defined as the ratio between the PMOS pull up transistor and the NMOS pass transistor

$$PR = \frac{W_3/L_3}{W_6/L_6} \quad 2.6$$

If we wish to pull the node below V_{Tn} , the Pull up ratio (PR) has to be below 1.8 [7]

2.3 Sense Amplifier

A key component in the periphery of the memory is a ‘sense amplifier’ which amplifies a small difference in the bitlines resulting in reduced power dissipation while maintaining the performance. Its main function is to sense or detect stored data from the read selected memory cell. A sense amplifier is an active circuit that reduces the time of signal propagation from an accessed memory cell array, and converts the arbitrary logic levels occurring on the bitline to the digital logic levels. In the voltage mode, the circuits amplify a small differential voltage in the bitlines to a full swing output. In the current mode, it amplifies a small differential current. The use of current sense amplifiers [8] has a number of benefits over voltage sensing amplifiers.

2.3.1 Basic Differential Voltage Sense Amplifier

The basic MOS differential voltage sense amplifier [6] circuit contains all elements required for differential sensing. A differential amplifier takes small signal differential inputs and amplifies them to a large signal single ended output. The effectiveness of a differential

amplifier is characterized by its ability to reject common noise and amplify true difference between the signals. Because of rather slow operational speed provided at considerable power dissipation and inherently high offset basic differential voltage amplifier is not applied in memories. The basic differential voltage sense amplifier is shown in Figure 2.5, it comprise of two NMOS transistors M1 and M2 and three resistors R1, R2 and R3. This circuit amplifies the small difference at bitlines to full swing at output nodes.

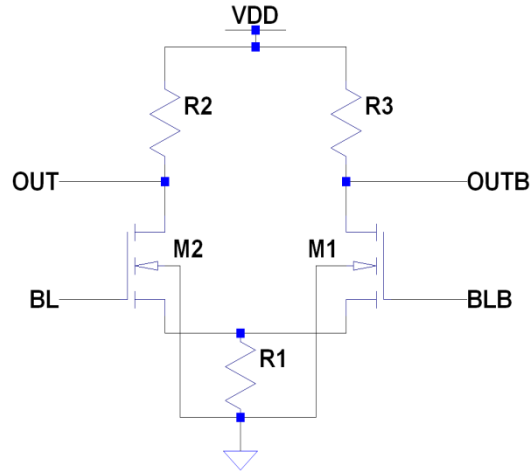


Figure 2.5 Differential voltage sense amplifier [6]

2.3.2 Positive Feedback Differential Voltage Sense Amplifier

Positive feedback sense amplifier [5] is shown in Figure 2.6, it comprise of M1-M4 transistors as positive feedback amplifier and M5 , M6 are used to enable the sense amplifier, M7 is used to precharge the output node during precharge mode. The positive feedback amplifier has two data nodes BL/OUT and BLB/OUTB and three control nodes SEN, SEP and PRE. Nodes BL/OUT and BLB/OUTB act as both input and output to the sense amplifier. Its operation is as follows, the data nodes are equalized using PRE and the memory cell being read is asserted and a small voltage difference forms on BL/OUT and BLB/OUTB . While M1 and M2 are biased to be operating in the saturation region. M6 is turned on by SEN. As both BL/OUT and BLB/OUTB are decreasing in voltage so is the difference between them and one of them decreases much faster than the other and causes M1 or M2 to enter cutoff while the other starts operating in triode, at this point M5 is turned on by SEP which pulls the signals rapidly apart. At this point since BL/OUT and

BLB/OUTB, are directly connected to the bit-lines the data is automatically written to the destructively read memory cell.

Due to its positive feedback this voltage sensing amplifier achieves a very high differential gain. This high gain minimizes sensing time by being able to sense small voltage swings on the bitline.

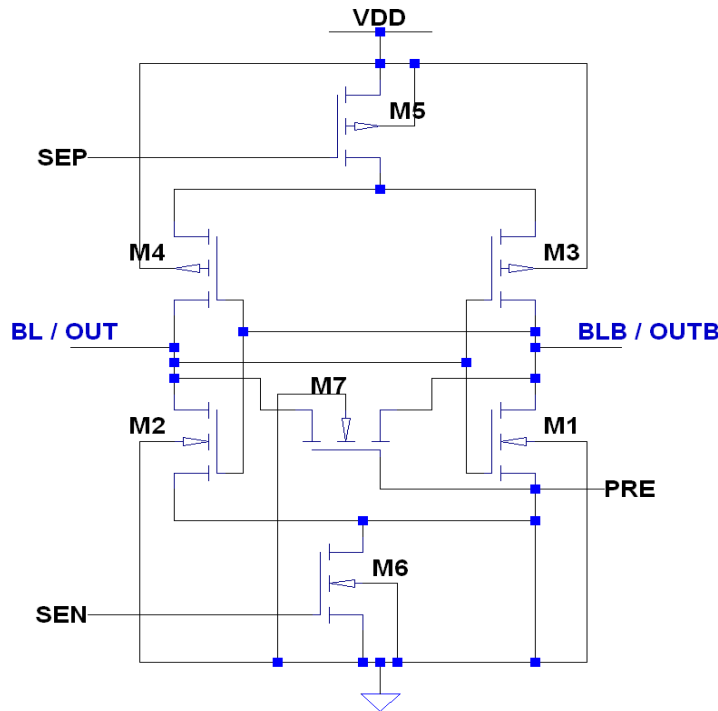


Figure 2.6 Positive feedback differential voltage sense amplifier [5]

2.3.3 Latch Type Sense Amplifier

Among all peripheral components of an SRAM circuit, a sense amplifier, which detects the small differential signal on a bitline pair and amplifies it to a full swing signal at data output port, plays an important role. The latch-type sense amplifier [1] shown in Figure 2.7, it comprise of M1- M4 transistor as high gain positive feedback amplifier and M5 And M6 are used to precharge the output node and M9 is used to enable the sense amplifier, M7 and M8 are act as common source differential amplifier. Latch type sense amplifier is commonly used due to its advantages of low power dissipation and high speed.

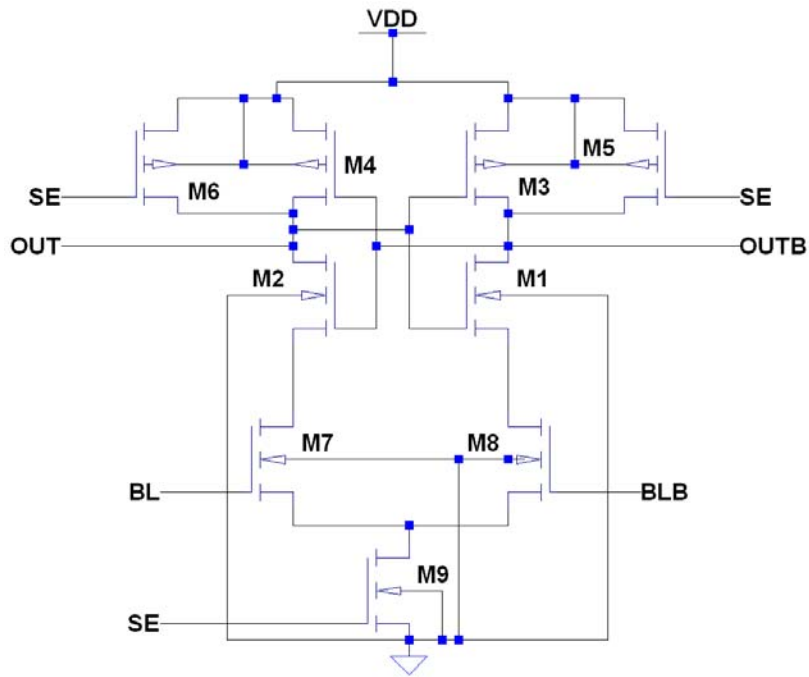


Figure 2.7 Latch type sense amplifier [1]

2.3.4 Conventional Current Mode Sense Amplifier

The operation of the sense amplifiers presents two common phases: precharge and sense signal amplification. In the precharge phase the appropriate signals to force the sensing nodes to certain potentials are applied. At the sense operation a comparison is made between the currents of the sensing nodes. The content of the selected memory cell is retrieved as a result of this comparison. The conventional current mode sense amplifier [9] is illustrated in Figure 2.8. The design of the sensor is based on the classic cross-coupled latch structure (M1 M2 M3 M4) with extra circuitry for sensor activation (M5) and bit-line equalization (M6 M7 M8). In the precharging phase the EQ signal is low and the bit-lines are precharged to V_{DD} . In the sensing phase the EQ and EN signals go to high. This activates the cross coupled structure and drives the outputs to the appropriate values.

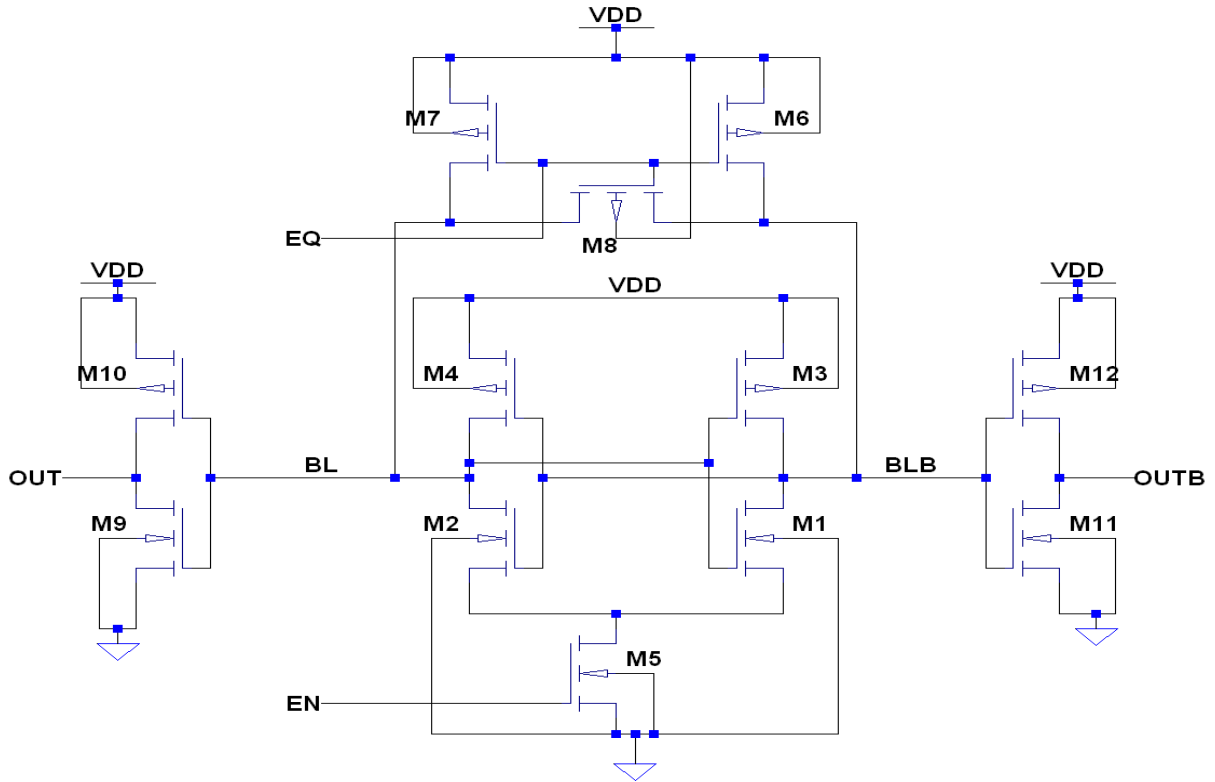


Figure 2.8 Conventional current mode sense amplifier [9]

2.3.5 Clamped Bitline Sense amplifier

A commonly used current mode sensing amplifier is the clamped bitline sense amplifier [10] shown in Figure 2.9. By clamping the voltage on the bitline to a stable voltage (V_{REF}) the signal current produced by the cell can be transferred to an internal sense amp node without charging/discharging the large bitline capacitance. As a result both sensing delay and dynamic power consumption are significantly decreased. This sense amplifier uses three precharge and equalization transistors (M7, M8 and M9), two current sensing transistors (M5 and M6) and four back to back inverter configuration transistors for the voltage output stage (M1, M2, M3, M4). Its operation follows two stages pre-charge/equalization, and sensing. The following is the timing schedule transistors M7, M8, M9 are turned on to precharge and equalize the sensing nodes, transistors M7 and M8 are turned off and the memory cell accessed, the current from the cell starts being sourced by one of the transistors M1 and M3 and a voltage difference starts forming on one of the output nodes, this voltage is further amplified by the positive feedback amplifier until it reaches the latched state.

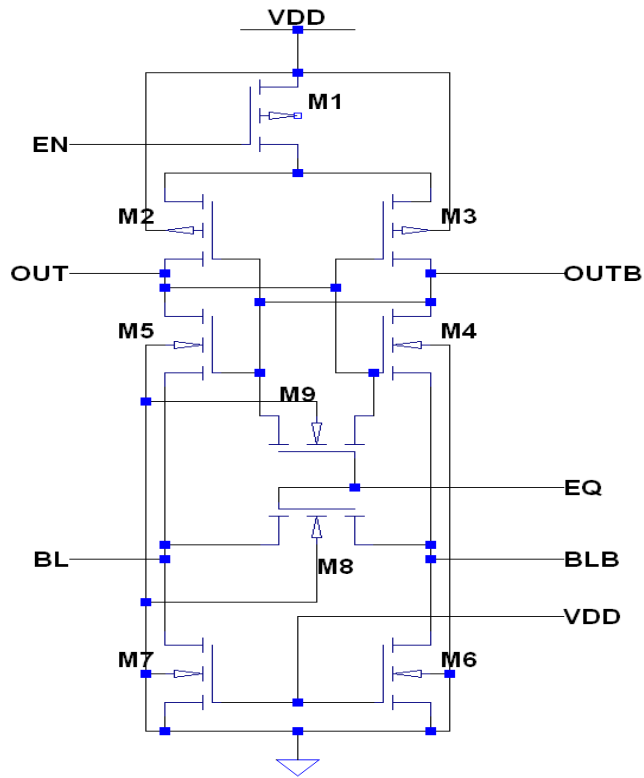


Figure 2.9 Clamped bitline sense amplifier [10]

2.3.6 Alpha Latch Sense Amplifier

The alpha latch sense amplifier [11] is shown in Figure 2.10.

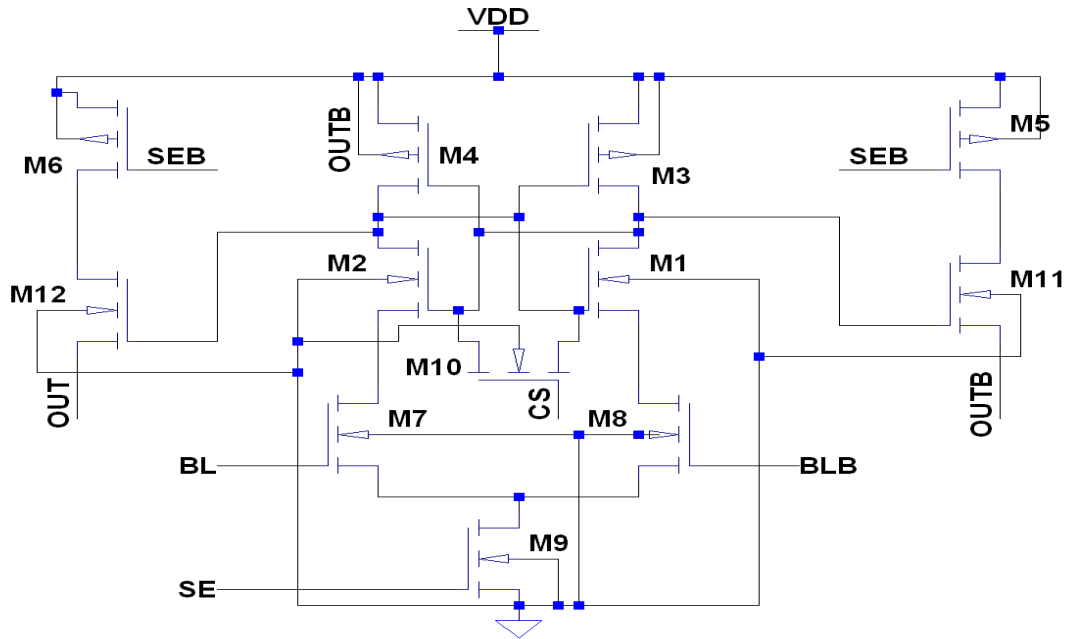


Figure 2.10 Alpha latch sense amplifier [11]

The NMOS transistor M9 is used to turn the amplifier off during standby. When the sense amplifier is activated by the enable signal (SE), the differential input from the complementary bitlines induces a differential transconductance in M7 and M8. As a result, voltage and current differences will appear at the drains of M7 and M8, i.e., the sources of M1 and M2. Since the CS signal turns off M10 and M1-M4 positive feedback amplifier amplifies the difference to full swing at drain terminal of M1 and M2. During standby SE, is kept low to turn M5 and M6 off. During sensing mode, both M5 and M6 are turned on but one of M11 and M12 is turned off, thus only one current will flow to the datalines

2.3.7 Decoupled Latch Sense Amplifier

The decoupled latch sense amplifier [11] consists of six NMOS and two PMOS transistors, as shown in Figure 2.11.

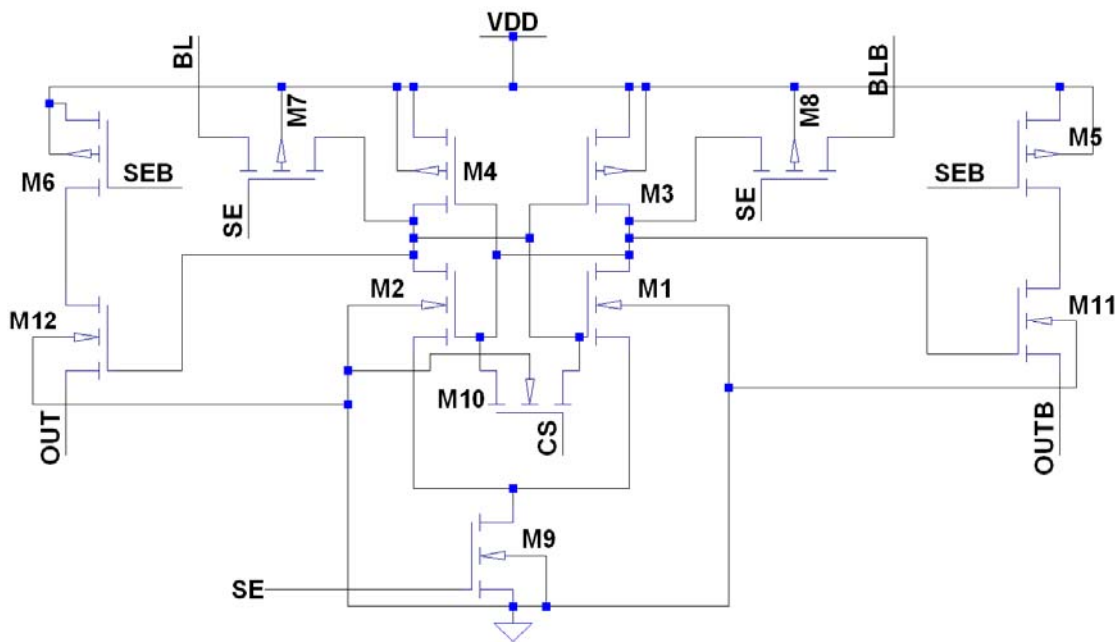


Figure 2.11 Decoupled latch sense amplifier [11]

Similar to the alpha latch, its M9 is used to save power. Once the bitline differential signal is induced at source terminal of transistor M1 and M2, the latch is enabled by turning off M10 but turning on M9. Concurrently, M7 and M8 are turned off to decouple the bitlines from the high swing output nodes. The use of M7 and M8 helps reducing the impact of the bitline

capacitances on the switching activity, hence significantly reducing both sensing delay and power consumption.

2.3.8 Conventional current mirror sense amplifier

Conventional current mirror sense amplifier [1] is shown in Figure 2.12. It comprises of two current mirror circuits one consist of M6 and M8 transistors and other consist of M9 and M11 transistors. M7 and M10 are used to precharge the output node to full supply voltage during precharge mode. M1, M4, M2 and M5 are used as a common source differential amplifier. M3 is used to enable the sense amplifier.

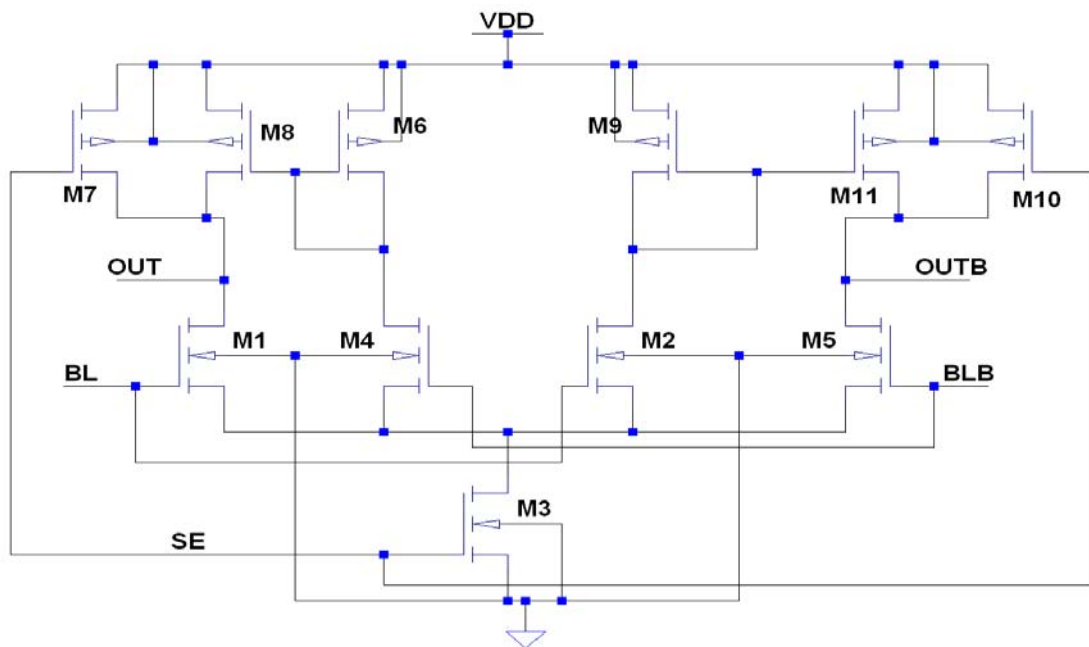


Figure 2.12 Conventional current mirror sense amplifier [1]

Sense amplifier operates in two mode precharge mode and sensing mode, in precharge mode SE signal is low which turns on the M7 and M10 transistors by which our outputs are precharge to the supply voltage. In sensing mode SE signal is high so both M7 and M10 turns off whereas M3 turns on and sensing operation starts. The small difference at bitlines is sensed by the common source difference amplifier and corresponding current mirror copies the current at output node and at output we got high and low value. Current mirror has good common mode rejection ratio, but the large area is required and power consumption is also very high.

2.3.9 Fully current sense amplifier

Fully current sense amplifier [12] is shown in Figure 2.13. This circuit consist of two sensing stage local and global.

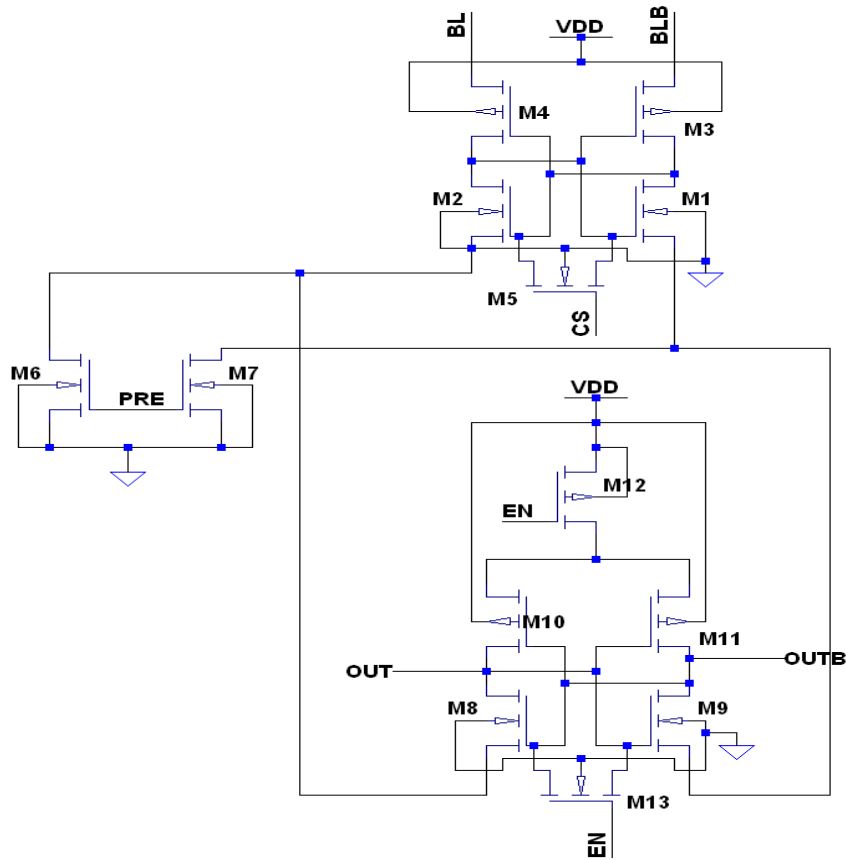


Figure 2.13 Fully current sense amplifier [12]

The local stage is formed by M1-M5 five transistors (two M3 and M4 PMOS and three NMOS M1, M2 and M5) and the global stage is formed by M7-M13 five NMOS transistors (M6, M7, M8, M9 and M13) and three PMOS transistors (M10, M11 and M12). CS and EN signals are used to equalize the potential at out terminals and drain terminal of M1 and M2. PRE signal is used to ground the source terminal of M8 and M9. When EN is low, M12 transistor turns on and our sense amplifier got activated and corresponding small difference at bitlines is amplified to full swing at output nodes. This type of sense amplifier has high speed and low power consumption.

2.3.10 Hybrid current sense amplifier

Hybrid sense amplifier [13] is shown in Figure 2.14. Here M1,M2,M5,M6 forms the high gain positive feedback amplifier and M9 is used to enable the sense amplifier. M10 is used to equalize the output at same potential. In precharge phase EQ signal is low so M10 turns on and our output nodes are forced at same potential. During sensing phase SE signal is high and the small current difference from the bitlines is sensed by the source terminal of M5 and M6 transistor than positive feedback amplifier amplify the small difference to full swing.

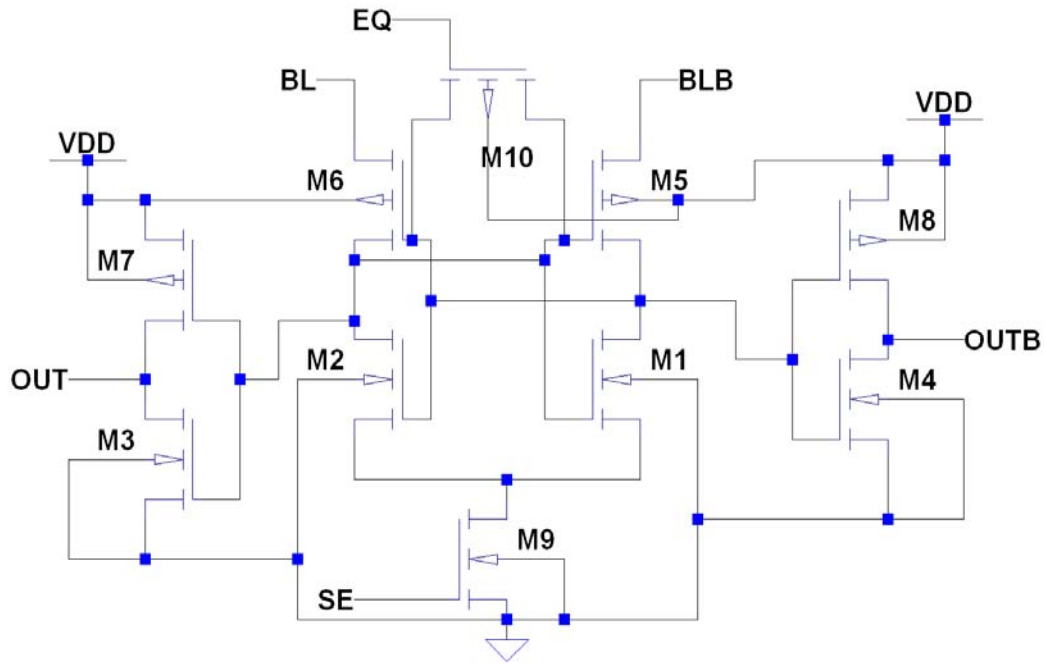


Figure 2.14 Hybrid current sense amplifier [13]

2.3.11 Current Conveyor Based Sense Amplifier

Current conveyor based sense amplifier [14] consists of four identical M1-M4 PMOS transistors connected in a feedback structure as shown in Figure 2.15. The complementary bitlines BL and BLB are precharged to supply voltage and M1- M4 transistors operate in saturation region during the read operation. The sense amplifier is activated by setting CS signal low. As all four transistors are in saturation, their source-to-drain currents are only dependent on their gate-to-source voltages. As a result, voltage at the bitline terminals is the

same. The current conveyor therefore has the ability to convey the differential current from the bitlines to the dataline without waiting for the discharging of the highly capacitive bitlines. Thus, this design achieved both higher sensing speed and lower power consumption when compared to the conventional voltage mode designs in which large voltage difference must be developed between the bitlines.

This circuit consists of four M5-M8 NMOS transistors. These NMOS devices form two current-mirrors to intensify the output currents and to the datalines.

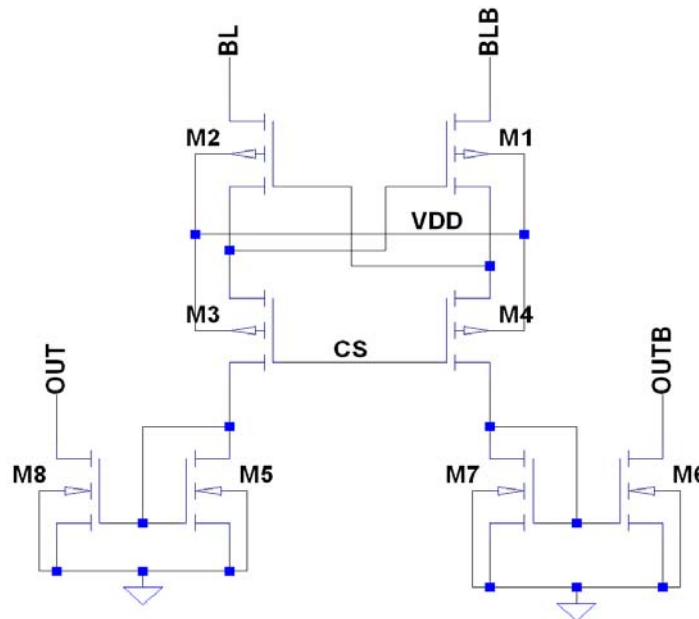


Figure 2.15 Current conveyor based sense amplifier [14]

2.4 Power Reduction Techniques

In CMOS circuit the power dissipation is due to the standby leakage current and the performance of a circuit is described by its high speed, low power and low area. So to reduce the power dissipation in the CMOS circuits various techniques are used.

2.4.1 Variable Threshold CMOS (VTCMOS)

Variable threshold CMOS (VTCMOS) [15] is a body biasing design technique as shown in Figure 2.16. In order to achieve different threshold voltages, a self substrate bias circuit is

used to control the body bias. In the active mode, a nearly zero body bias is applied. While in sleep mode, a deeper reverse body bias is applied to increase threshold voltage and to cut off leakage current. Furthermore, in active mode, a slightly forward substrate bias can be used to increase the circuit speed while reducing short channel effect.

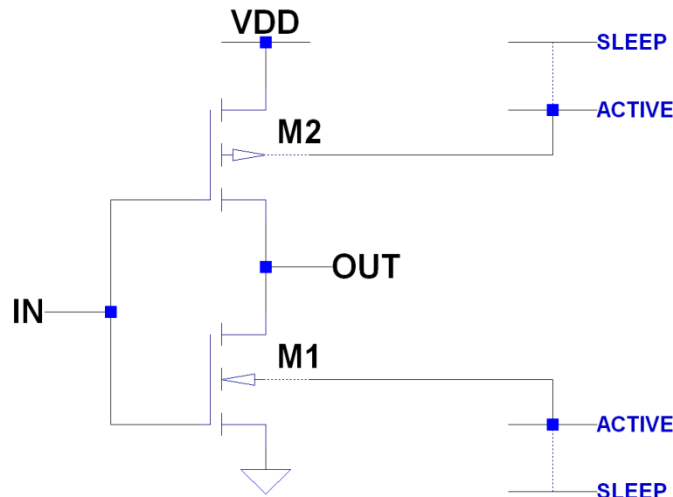


Figure 2.16 Variable Threshold CMOS [15]

2.4.2 Multithreshold CMOS (MTCMOS)

The multithreshold-voltage CMOS (MTCMOS) [16] circuit was proposed by inserting high threshold devices in series into low V_{th} circuitry, as shown in Figure 2.17. Here M1-M4 transistors are low V_{th} device where M5 and M6 are high V_{th} device. A sleep control scheme is introduced for efficient power management. Two high V_{th} transistors are used, high V_{th} PMOS M5 is connected to the power supply, where NMOS M6 is connected to the ground. Due to these transistors a virtual power supply and ground are appears respectively on the drain terminal nodes of the both transistors. In the active mode, SL is set low and SLB is high so M5 and M6 are turned on. Since their on-resistance is small, the virtual supply voltage (V_{DD} and GND) almost function as real power lines. In the standby mode, SL is set high, M5 and M6 are turned off and the leakage current is very low.

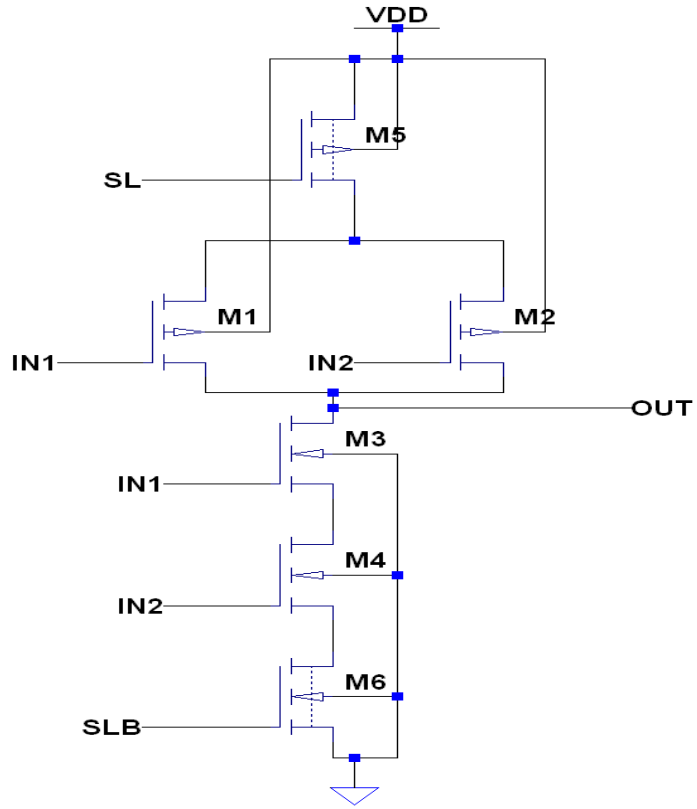


Figure 2.17 Multi threshold CMOS [16]

2.5 Gaps in Study

Table 1.1 shows the various architecture of the sense amplifier with their sensing delay and the supply voltage used for their operation. In this table the technology used by different type of sense amplifier is also mentioned.

Table 1.1 Gaps in study for different type of sense amplifiers.

Year	Technology	Author	Features	Sensing Delay(ns)	Supply Voltage(V)
2002	0.25um	A Chrisanthopoulos et al.	Conventional Sense Amp.[9]	7.1	2.5
2002	0.25um	A Chrisanthopoulos et al.	Clamped Bitline Sense Amp.[9]	0.35	2.5
2002	0.25um	K.-S. Yeo, et al.	Low power current sense Amp.[18]	1.04	2.0
2002	0.25um	A Chrisanthopoulos et al.	Simple Four Transistor Sense Amp.[9]	1.85	2.5
2004	0.35um	Chun- lung Hsu et al.	High Speed Sense Amp.[1]	0.51	1.8
2005	0.18um	Z. H. Kong et al.	Ultra low power. [19]	1.46	1.8
2007	0.18um	Sandeep Patil et al.	Self-Biased Charge-Transfer Sense Amp. [20]	0.723	1.8
2008	0.18um	Ya-Chun Lai et al.	Latch Type Sense Amp.[21]	0.33	1.8
2008	0.18um	Anh-Tuan Do et al.	Fully Current Mode Sense Amp.[12]	0.38	1.8
2008	0.18um	Do Anh-Tuan et al.	High Speed Sense Amp.[13]	0.26	1.8
2011	65nm	Anh-Tuan Do et al.	Alpha Latch Sense Amp.[11]	0.566	1
2011	65nm	Anh-Tuan Do et al.	Decoupled Sense Amp.[11]	0.214	1

3.1 Designing of Sense Amplifier

Following are the performance metrics to be considered during the design of sense amplifier:

1. Minimum sensing delay,
2. Maximum voltage swing,
3. Minimum power consumption,
4. Optimized layout area,
5. High reliability,
6. Specified environmental tolerance.

3.2 Specifications of Sense Amplifier

- Number of memory cells per column = 1024
- Bitline capacitance of a cell = 10 fF
- Sensitivity = 50 mV
- Supply voltage = 1.8 V
- Circuit designed at 0.18 μm technology

3.3 SRAM with precharge circuitry

Precharge circuit is used in the memory design for pull up or charging of the bitlines. Before performing any read or write operation bitlines are to be precharged upto supply voltage. The 6T SRAM cell with the precharge circuit is shown in the Figure 3.1. Transistors M7 and M8 are used for the charging of the bitlines up to the supply voltage V_{DD} and transistor M9 is used to equalize the potential at *bitline*(BL) and *bitline-bar*(BLB). Bitlines are connected to the supply voltage through the PMOS. When the PC signal given to the transistors M7, M8 and M9 is low, then all the transistors are turned on and charging of the bitlines takes place.

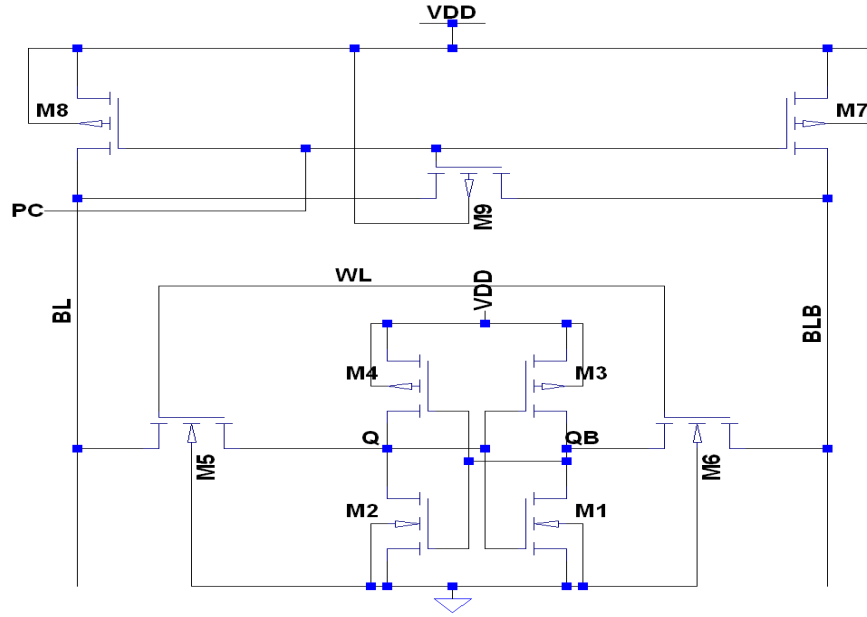


Figure 3.1 SRAM with precharge circuit [6]

Transistors M5 and M6 are the access transistors which are connected to the word and bit lines. Transistors M1, M2 and M3, M4 are connected to form cross coupled inverters. Size of all the transistors used in 6T SRAM with precharge circuit, is shown below in Table 3.1:

Table 3.1: Size of all the transistors of 6T SRAM with Precharge circuit at 0.18 μm technology

S.No.	Transistor	Type	Width(μm)
1.	M1	NMOS	3.6
2.	M2	NMOS	3.6
3.	M3	PMOS	1.6
4.	M4	PMOS	1.6
5.	M5	NMOS	2.4
6.	M6	NMOS	2.4
7.	M7	PMOS	1.6
8.	M8	PMOS	1.6
9.	M9	PMOS	1.6

To write the '0' and '1' in bit cell initially both bitlines are precharged by enabling M7, M8 and M9 transistors. When we enable the M5 and M6 transistors by giving WL signal high then the data at bitline is being stored at Q node and its inverse values is stored at QB. The various waveforms for storing '0' and '1' at bitcell are shown in Figure 3.2 and 3.3

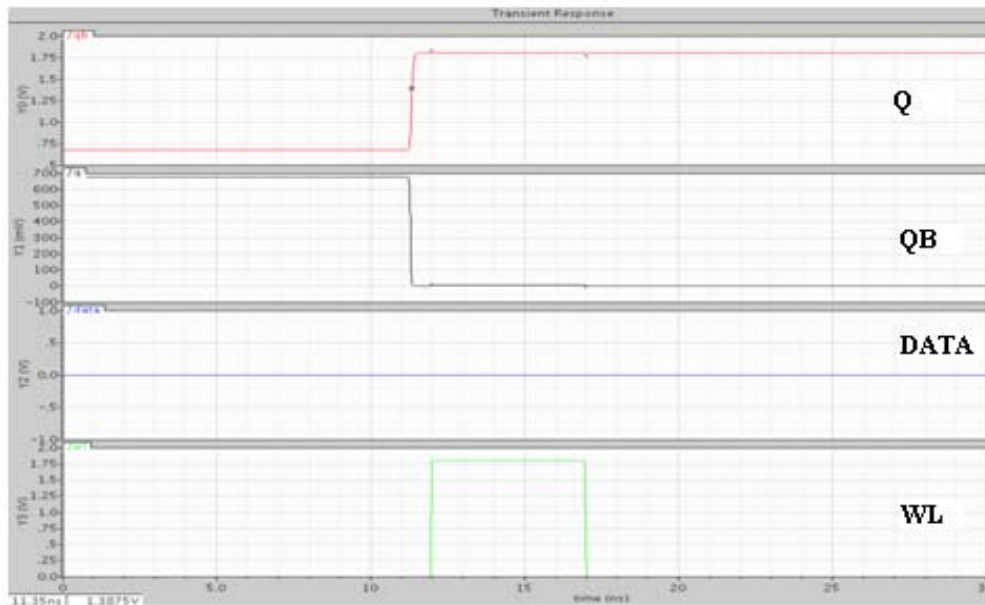


Figure 3.2 Waveforms for storing '0' in bit cell

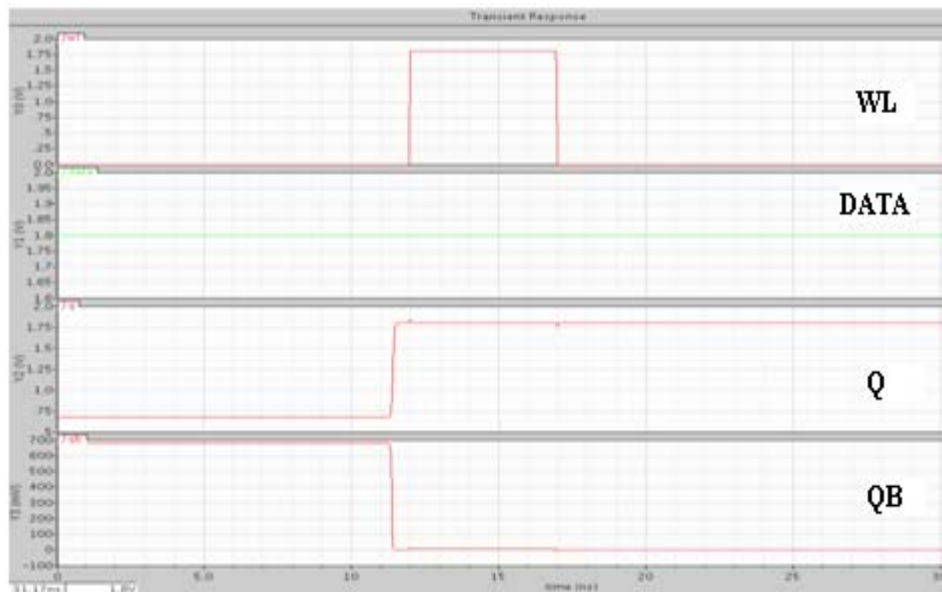


Figure 3.3 Waveforms for storing '1' in bit cell

3.4 6T SRAM layout

The layout of 6T SRAM is shown in Figure 3.4. Here the layout of 6T is designed to calculate the bitline capacitance associated with a bit cell. 6T SRAM layout is designed using Cadence Virtuoso 5.1.4 1_ISR layout editor and for RC extraction of layout Cadence Assura 3.2.0 is used. After RC extraction the capacitance of each transistor is calculated. The av extracted view of 6T SRAM is shown in Figure 3.5. From this RC extraction the bitline capacitance of single bitcell comes out nearly to be 10 fF.

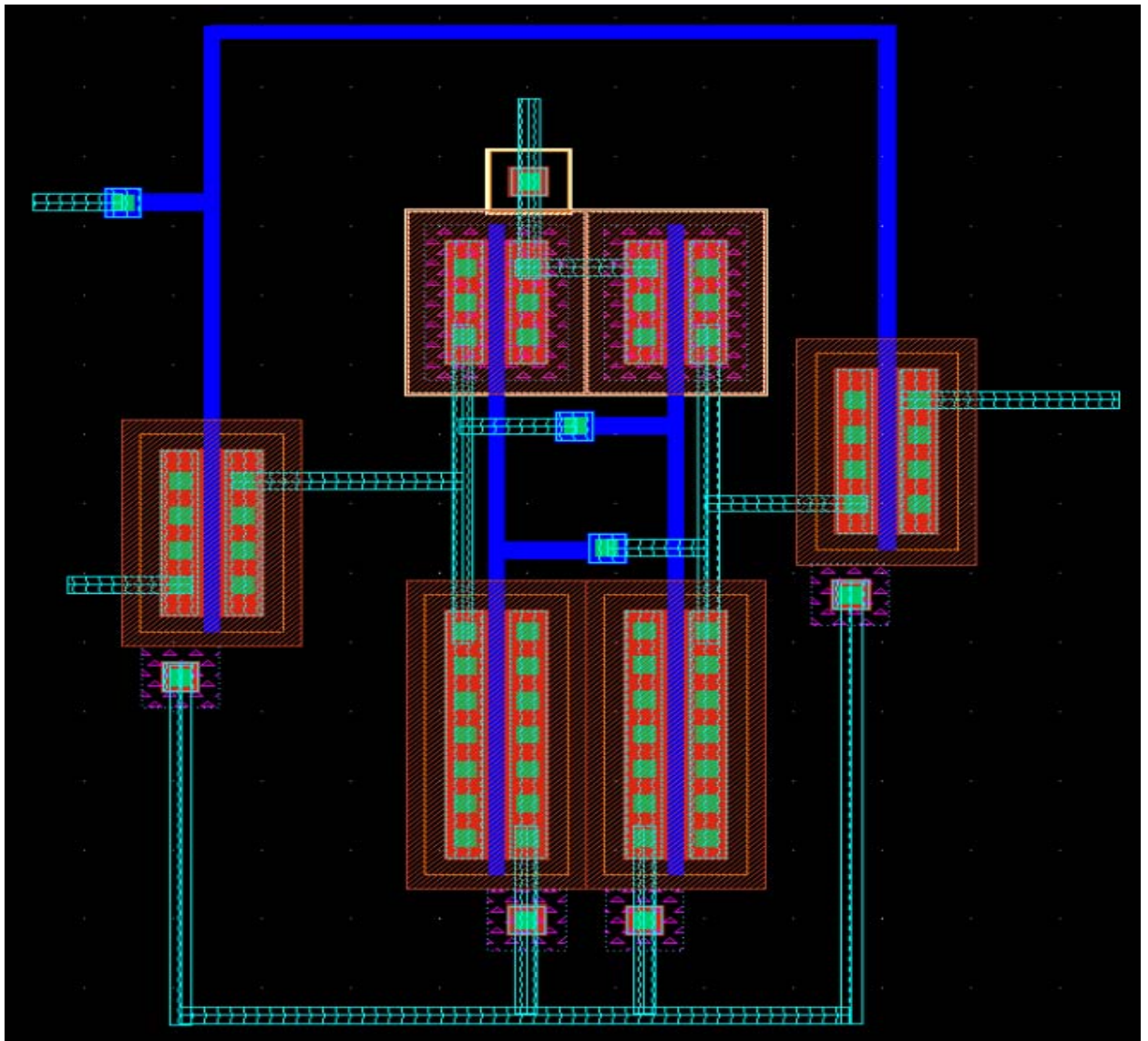


Figure 3.4 Layout of 6T SRAM cell

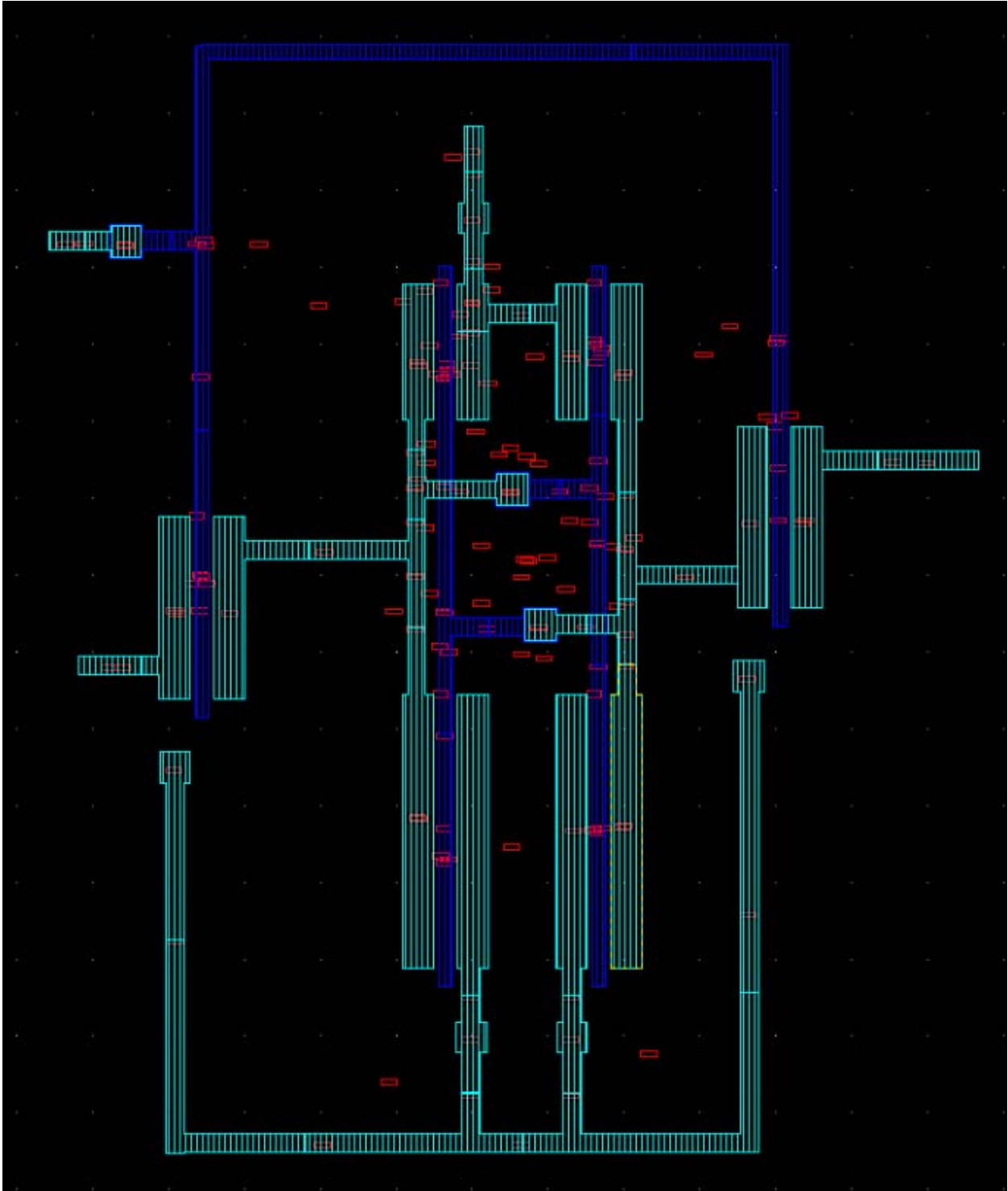


Figure 3.5 AV extracted view of 6T SRAM cell

3.5 Different types of Sense Amplifiers

3.5.1 Clamped Bitline Sense Amplifier

The clamped bitline sense amplifier [10] is shown in Figure 3.6. Here M2-M5 act as a high gain positive feedback sense amplifier. M6 and M7 operate in linear region and provide a low impedance clamp between the bitline and ground. M8 and M9 are used to equalize the potential on bitlines. M1 is used to enable the sense amplifier. Sense amplifier operates in two phase precharge phase and sensing phase. In precharge phase EQ signal and EN signal are high so MOS M5 and M6 turns on and forcing the bitlines to same potential and M1 is off. During sensing phase EQ and EN both signals are low so sense amplifiers got enabled and the current difference between the bitlines is sensed by the source terminal of M4 and M5 and corresponding the small difference is amplified by the positive feedback circuitry. Output waveforms of clamped bitline sense amplifier is shown in Figure 3.7 , when EN signal goes high than amplifier got enabled and the small difference is amplified by positive feedback circuitry and at OUT and OUTB we get the full swing voltage.

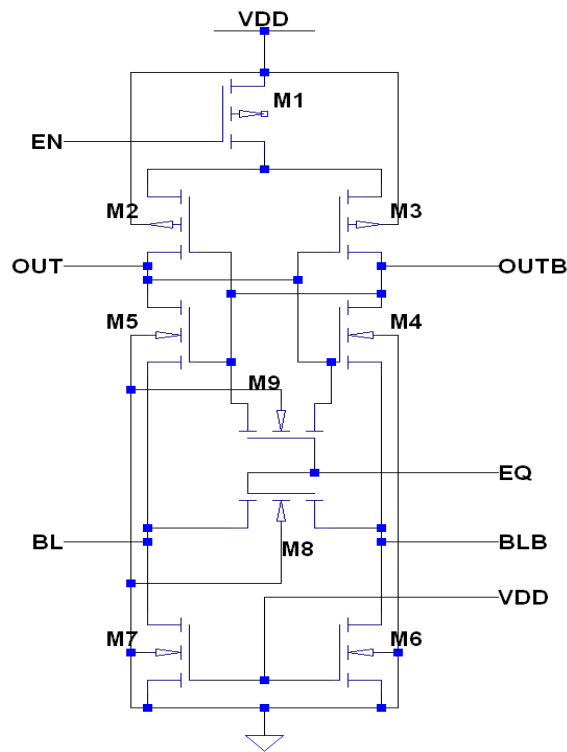


Figure 3.6 Clamped bitline sense amplifier [10]

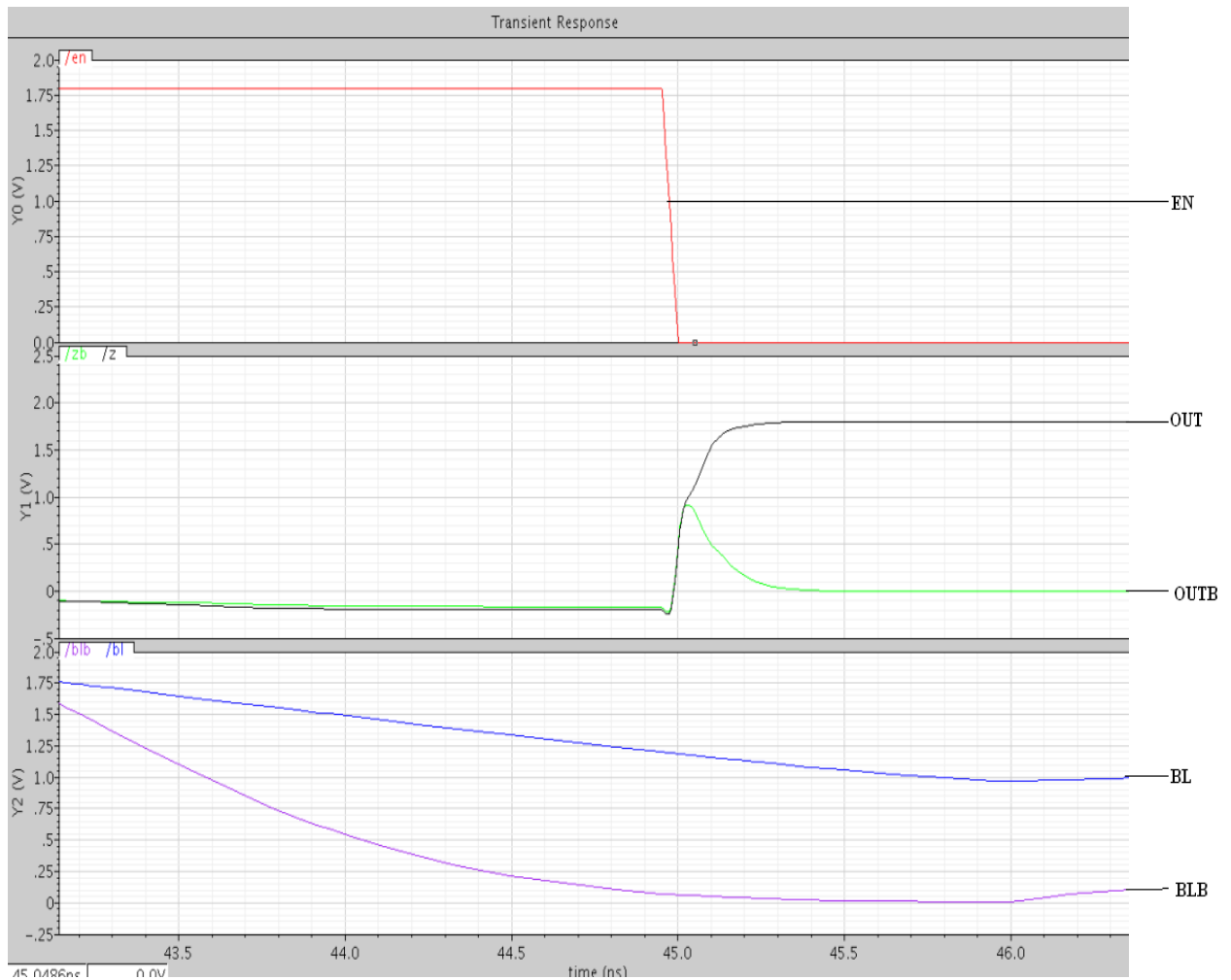


Figure 3.7 Output waveforms of clamped bitline sense amplifier

3.5.2 Latch Type Sense Amplifier

Latch type sense amplifier [1] is shown in Figure 3.8 Here M1-M4 act as high gain positive feedback sense amplifier. M7 and M8 are used to sense the small difference at the bitlines. M5 and M6 are used to precharge the output nodes. M9 is used to enable the sense amplifier. In precharge phase SE signal is low so M5 and M6 turns on and charge the output node. In sensing phase SE signal is high M9 turns on and M7 and M8 act as common source

differential amplifier. M1-M4 amplifies the small difference to full swing at output node. Latch type sense amplifier is used due to its high speed and low power consumption and output is also isolated from bitline capacitance. The drawback of latch type sense amplifier is that the failures caused due to insufficient sensing margin by the input offset voltage.

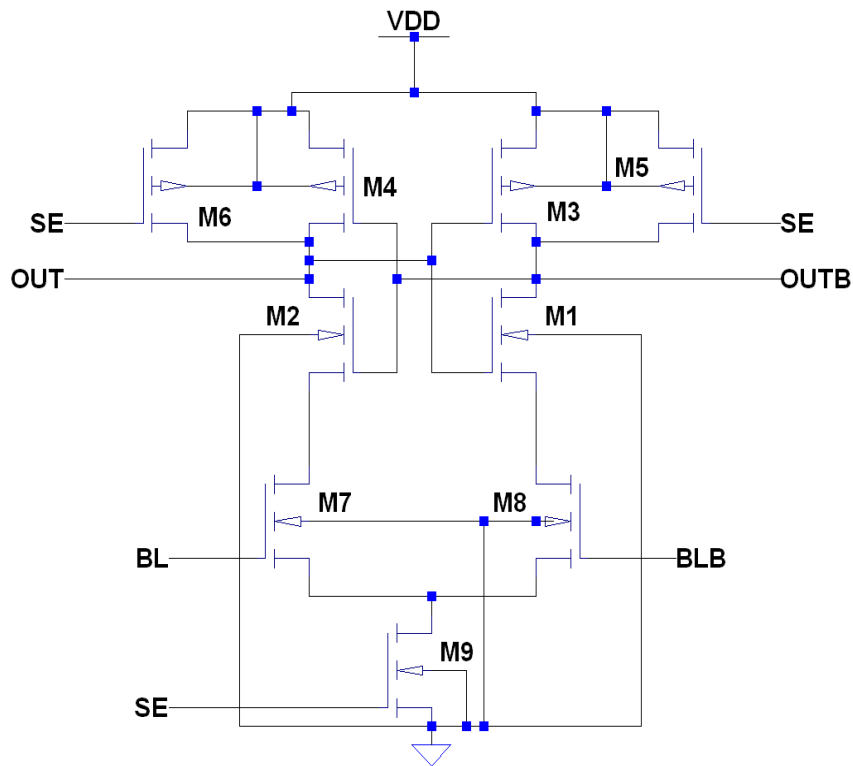


Figure 3.8 Latch type sense amplifier [1]

The output waveforms for latch type sense amplifier is shown in Figure 3.9, when our enable signal SE is low than OUT and OUTB precharged to supply voltage. As our enable signal SE goes high precharge circuitry is disabled and common source differential circuit and positive feedback amplifier got enabled. So the small difference between bitlines is amplified to the full swing value.

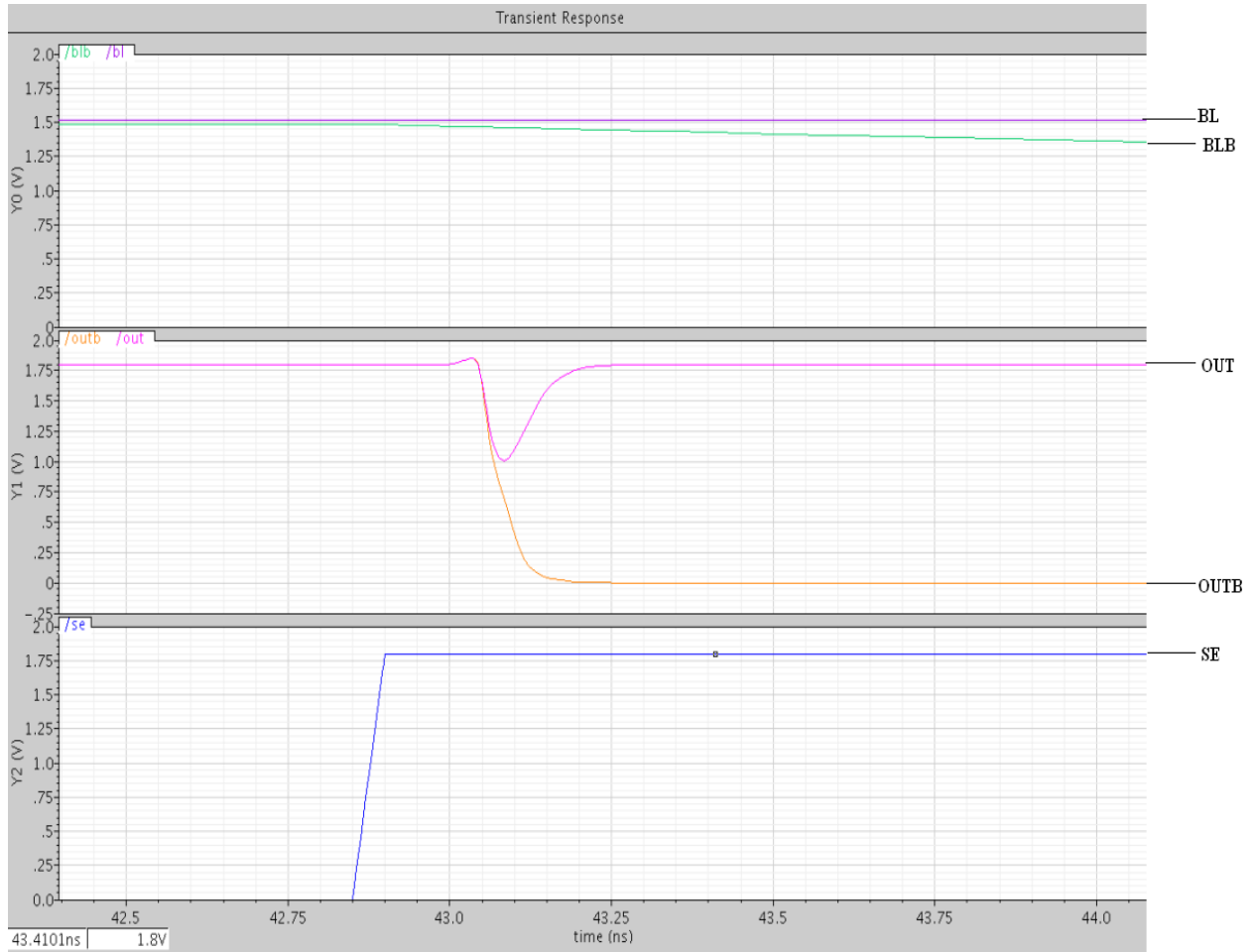


Figure 3.9 Output Waveforms of latch type sense amplifier

3.5.3 Cross Coupled Sense Amplifier

Cross coupled sense amplifier [23] is shown in Figure 3.10. Here M1-M4 act as high gain positive feedback sense amplifier. M5 is used to enable the sense amplifier. M8 is used to equalize the output nodes. Here M1 and M2 is biased in saturation region, M5 is turned on by SAE signal. The small voltage difference at input nodes is amplified by the high gain positive feedback amplifier. The output waveform for the cross coupled sense amplifier is shown in Figure 3.11. When the enable signal is low the OUT and OUTB both are at full supply voltage, as the enable signal SAE goes high the positive feedback amplifier amplifies the small difference between the bitlines to full swing.

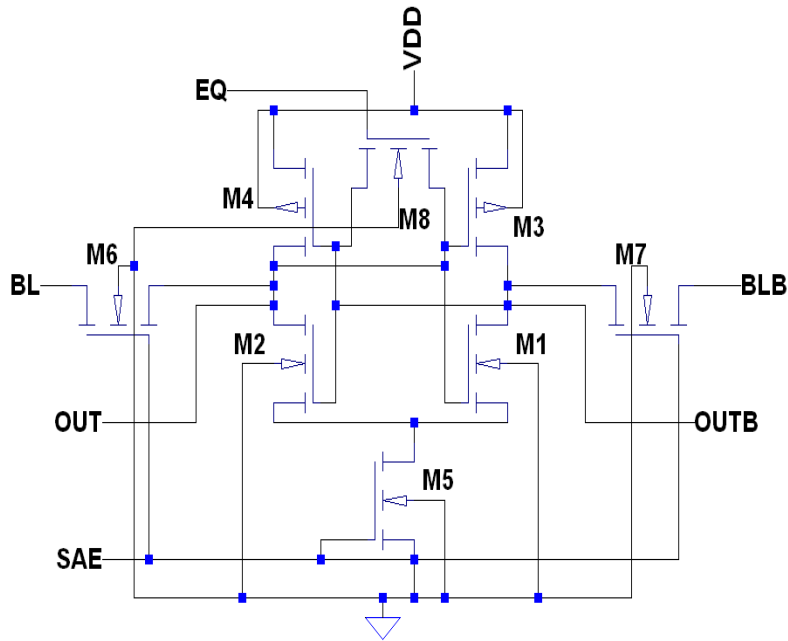


Figure 3.10 Cross coupled sense amplifier [23]

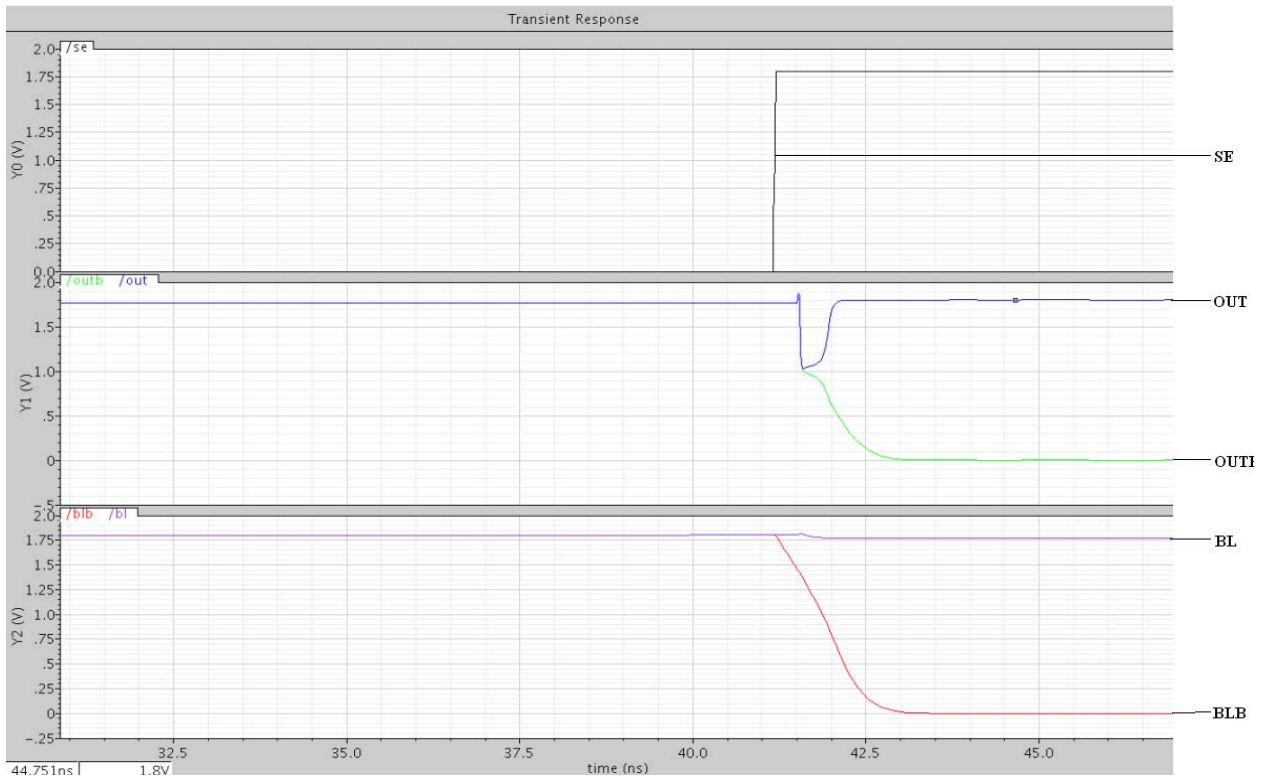


Figure 3.11 Output waveforms of cross coupled sense amplifier

3.5.4 Hybrid Sense Amplifier

Hybrid sense amplifier [13] is shown in Figure 3.12. Here M1,M2,M5,M6 forms the high gain positive feedback amplifier and M9 is used to enable the sense amplifier. M10 is used to equalize the output at same potential. In precharge phase EQ signal is low so M10 turns on and output nodes are forced at same potential. During sensing phase SE signal is high and the small current difference from the bitlines is sensed by the source terminal of M5 and M6 transistor than positive feedback amplifier amplify the small difference to full swing. The main advantage of this type of sense amplifier is that here output node is totally independent of bitline parasitic capacitance so due to which the sensing delay is quite low or we can say that the speed of operation is high.

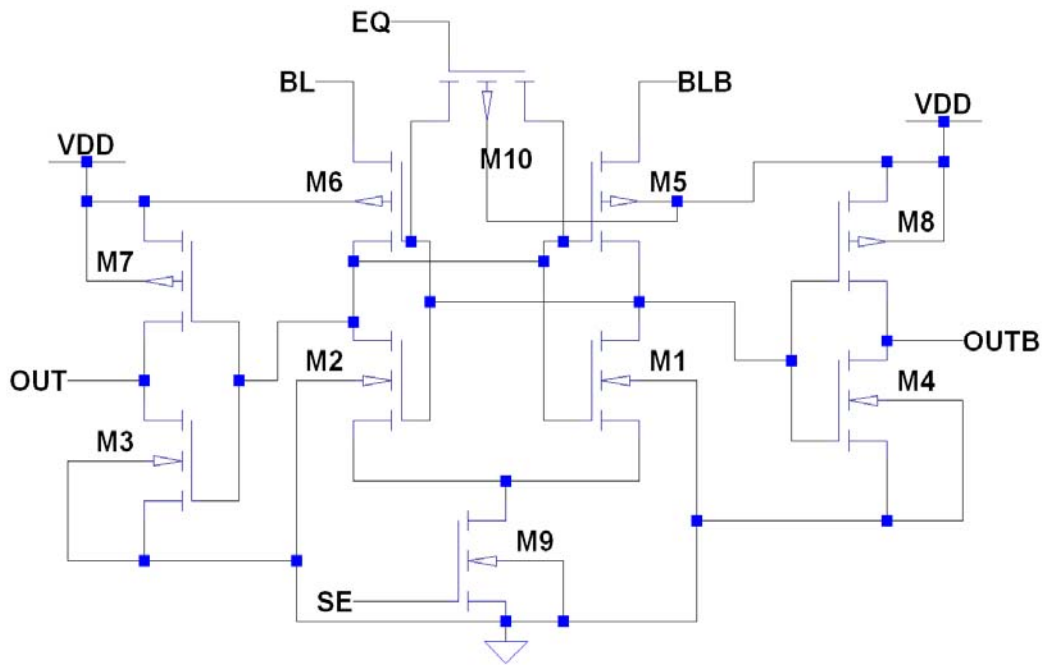


Figure 3.12 Hybrid sense amplifier.[13]

The output waveforms for hybrid sense amplifier is shown in Figure 3.13. When enable signal SE is at low value then sense amplifier is in off mode and at the same time EQ signal is low to equalize the voltage at OUT and OUTB node. But as enable signal SE goes high positive feedback circuit starts its working and amplifies the small difference between bitlines to full swing.

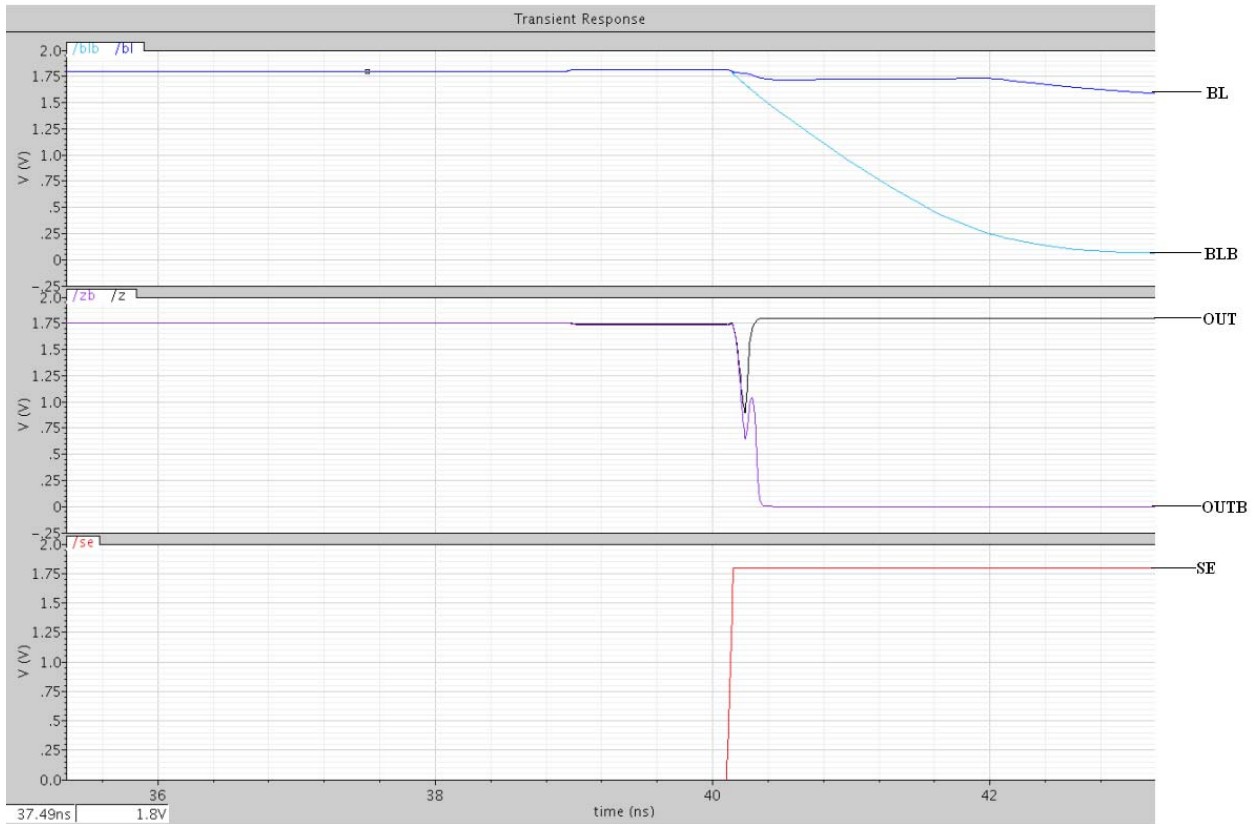


Figure 3.13 Output waveforms of hybrid sense amplifier

3.6 Proposed Sense Amplifier

A sense amplifier has been proposed on the basis of the previous latch type sense amplifier and pass transistor logic. In case of latch type sense amplifier shown in Figure 3.8 there are four transistors are being cascaded between supply voltage and ground, due to which large time is required to charge and discharge the output node, by which the sensing delay of circuit increases and corresponding power consumption is also more. So to overcome this problem a sense amplifier has been proposed as shown in Figure 3.14. Here M9, M10, M11 and M13 transistors are used to pass the small difference signal from the bitlines to the common source differential amplifier. M7 and M8 has been acted as common differential source amplifier and M1- M4 has been acted as positive feedback sense amplifier. M5 and M6 are used to precharge the output node to full swing.

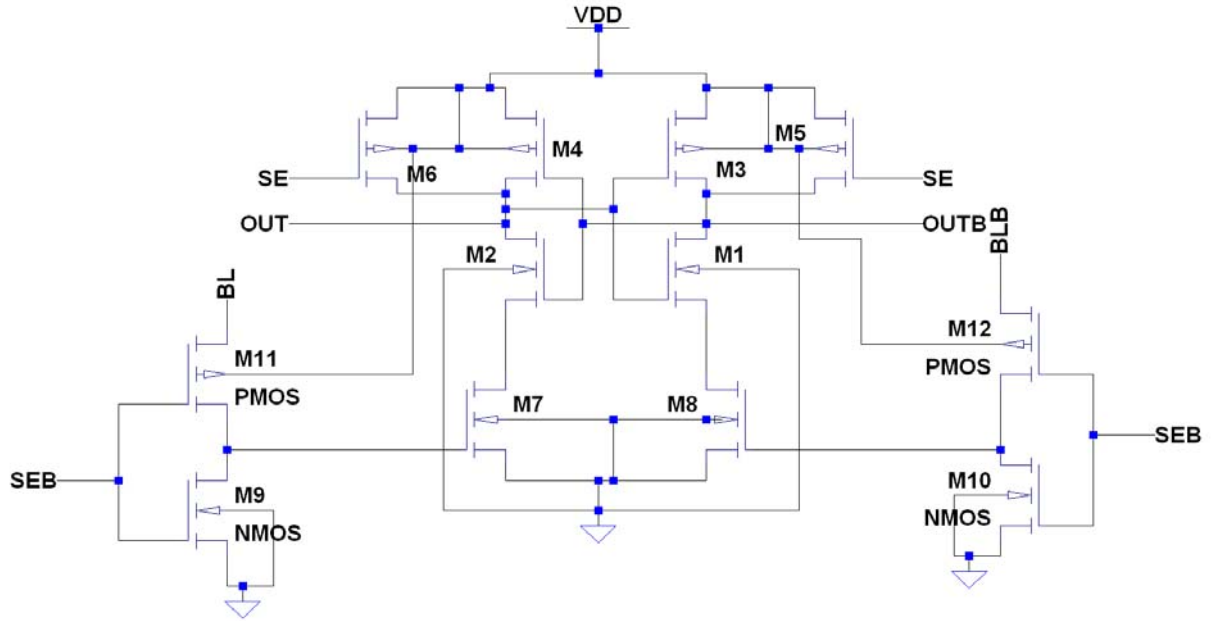


Figure 3.14 Proposed Sense Amplifier

Here sense amplifier operates in two modes precharge mode and sensing mode.

3.6.1 Precharge Mode

The sense amplifier in precharge mode is shown in Figure 3.15 in this case enable signal SE is low so M5 and M6 turns on and the OUT and OUTB nodes precharge to full supply voltage.

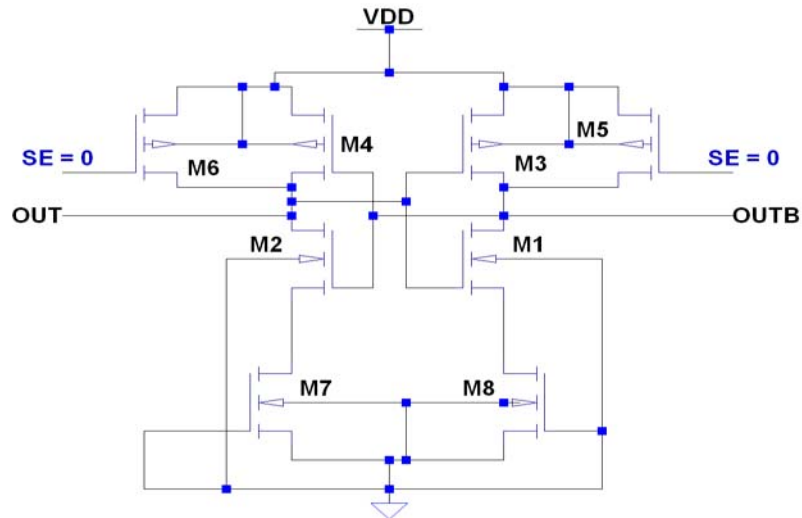


Figure 3.15 Proposed Sense Amplifier in precharge mode

Table 3.2 Size of all transistors in Proposed Sense Amplifier using 0.18 μm technology

S.No.	Transistor	Type	Width(μm)
1.	M1	NMOS	1.44
2.	M2	NMOS	1.44
3.	M3	PMOS	0.96
4.	M4	PMOS	0.96
5.	M5	PMOS	3
6.	M6	PMOS	3
7.	M7	NMOS	1.72
8.	M8	NMOS	1.72
9.	M9	NMOS	2.4
10.	M10	NMOS	2.4
11.	M11	PMOS	3
12.	M12	PMOS	3

3.7 Layout of Proposed Sense Amplifier

The layout for proposed sense amplifier is shown in Figure 3.17. here layout is designed using CADENCE VIRTUOSO tool in 0.18 μm technology. The layout is designed with minimum area and fullfill the all design rules

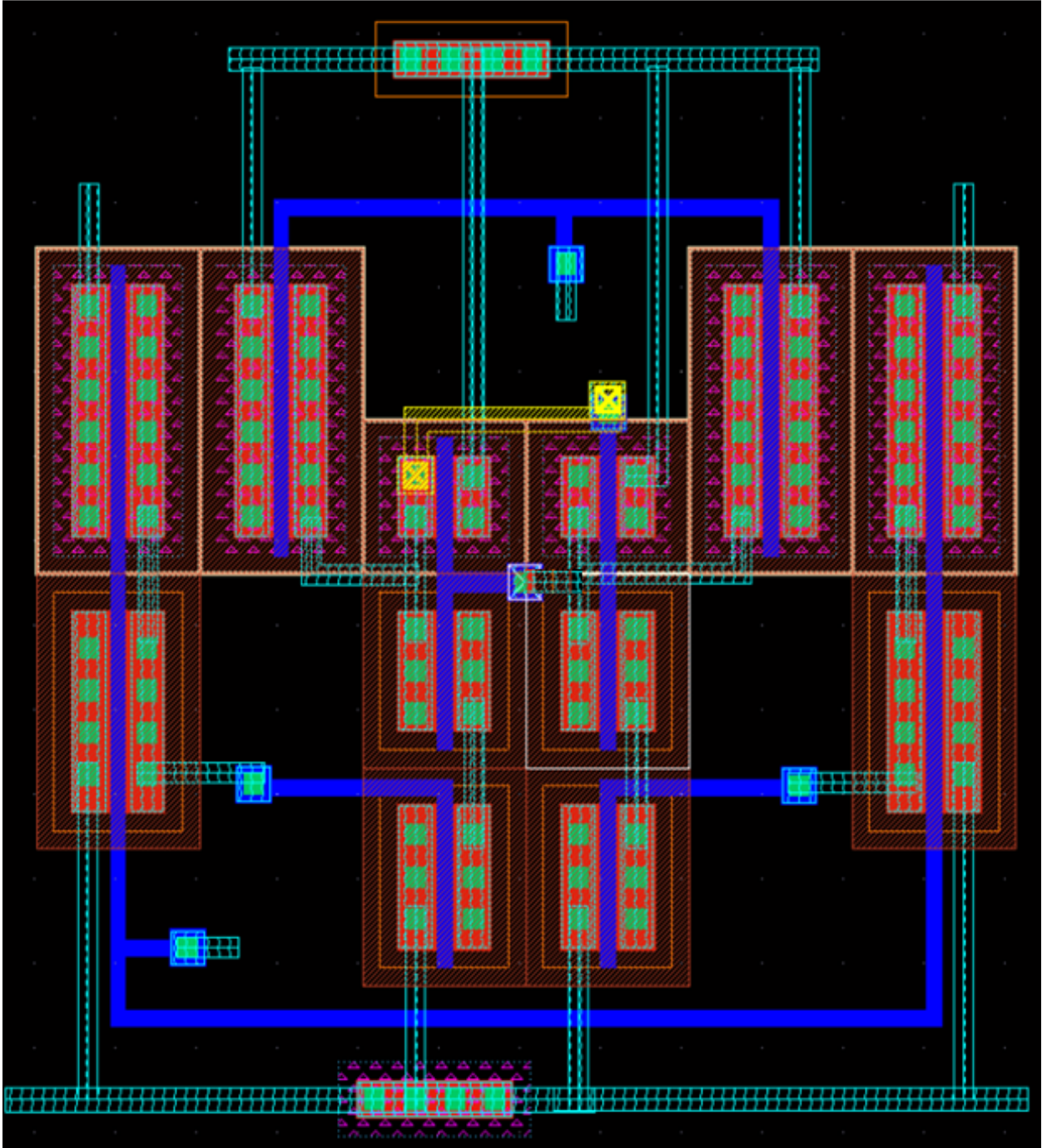


Figure 3.17 Layout of Proposed Sense Amplifier

4.1 Output Waveforms: Output waveforms of proposed sense amplifier is shown in the Figure 4.1, when the enable signal SE is low then the sense amplifier operates in precharge mode and output nodes precharge upto supply voltage. When the enable signal SE goes high sense amplifier got enabled and the common source differential amplifier and the positive feedback circuit amplifies the small difference at bitlines to full swing.

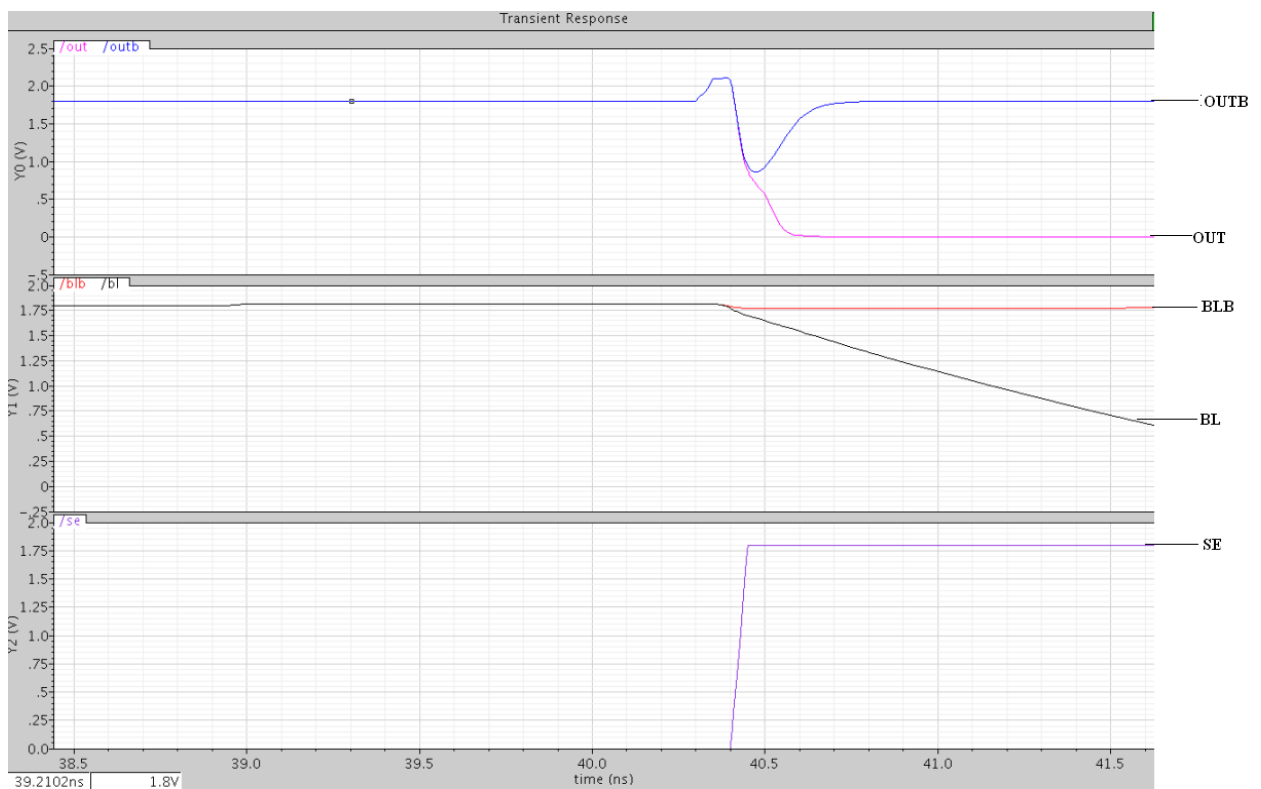


Figure 4.1 Output waveforms of Proposed Sense Amplifier

4.1.1 Variation of sensing delay w.r.t bitline capacitance

The variation of sensing delay with increase in bitline capacitance is shown in Figure 4.2 , from these waveforms we analyze that with increase in bitline capacitance the sensing delay of the sense amplifier also increases by which the speed of the memory reduces. So to overcome this problem output should be isolated from the bitline capacitance.

his problem output should be isolated from the bitline capacitance.

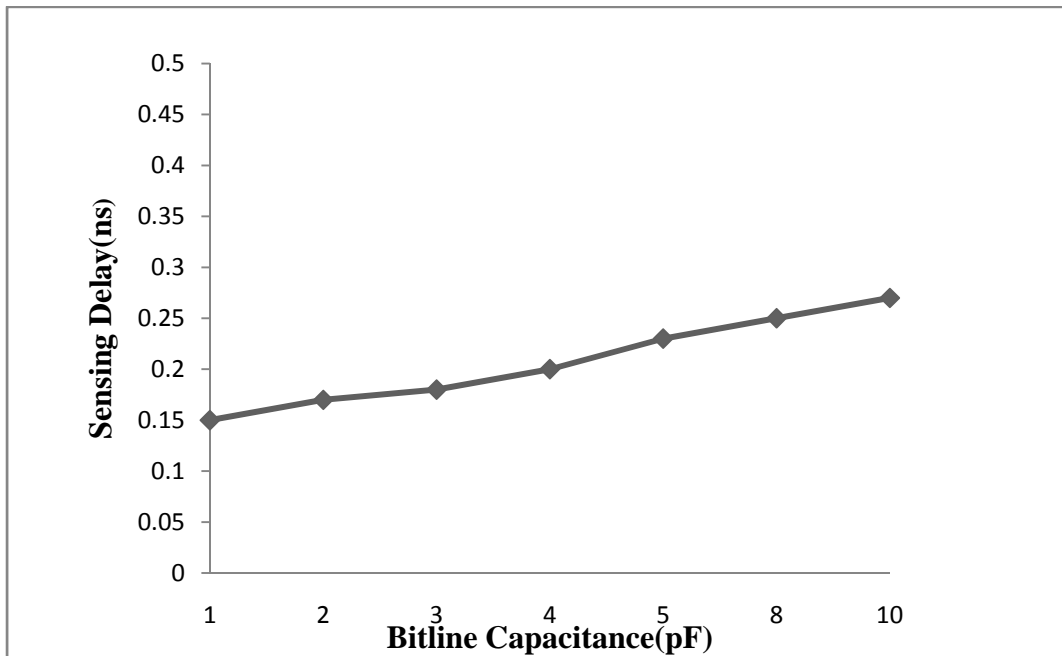


Figure 4.2 variation of sensing delay with respect to bitline capacitance for proposed sense amplifier

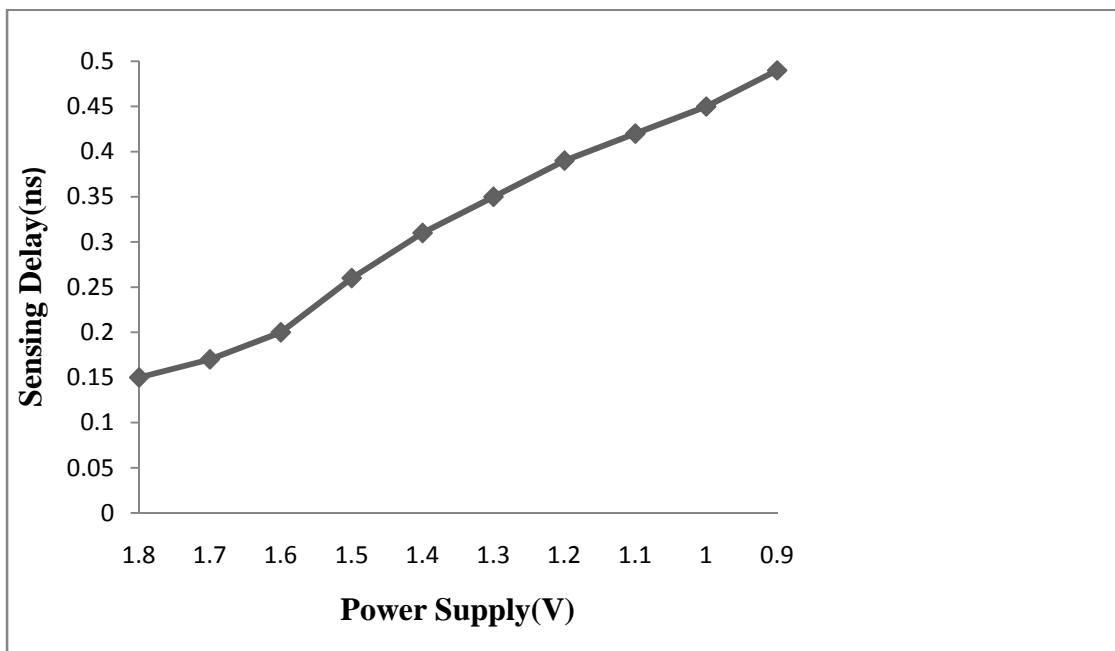


Figure 4.3 variation of sensing delay with respect to power supply for proposed sense amplifier

4.1.2 Variation of sensing delay w.r.t power supply

For operation of the our circuit it should operate at minimum supply voltage so that it can be easily portable and high efficient. The variation of sensing delay with variation in power supply is shown in Figure 4.3. With decrease in power supply the sensing delay of sense amplifier also increases. So at low supply voltage the delay of circuit is high but at the same time the power delay of the circuit is about constant.

4.1.2 Variation of average power w.r.t bitline capacitance

Power is one of the most important parameter in the operation of electronics circuits, the power consumed by the circuit should be as low as possible so that our system become highly reliable and more efficient. The variation of average power with increase in bitline capacitance is shown in Figure 4.4. From these waveforms it is observed that with increase in bitline capacitance the power consumed by the circuit also increases.

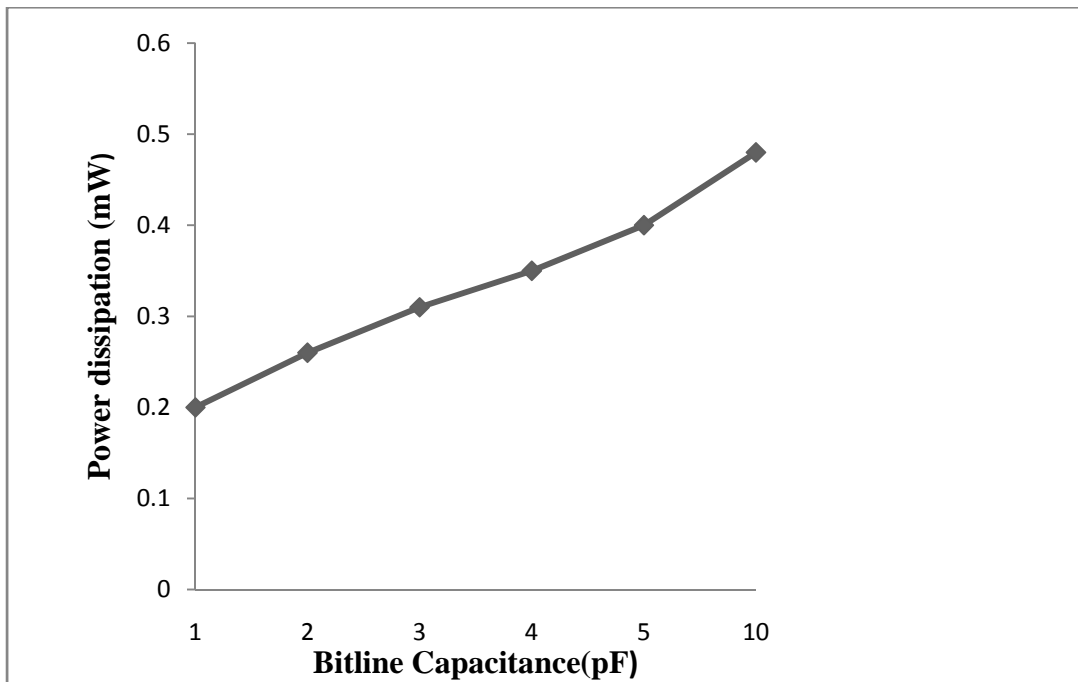


Figure 4.4 variation of average power w.r.t bitline capacitance for proposed sense amplifier

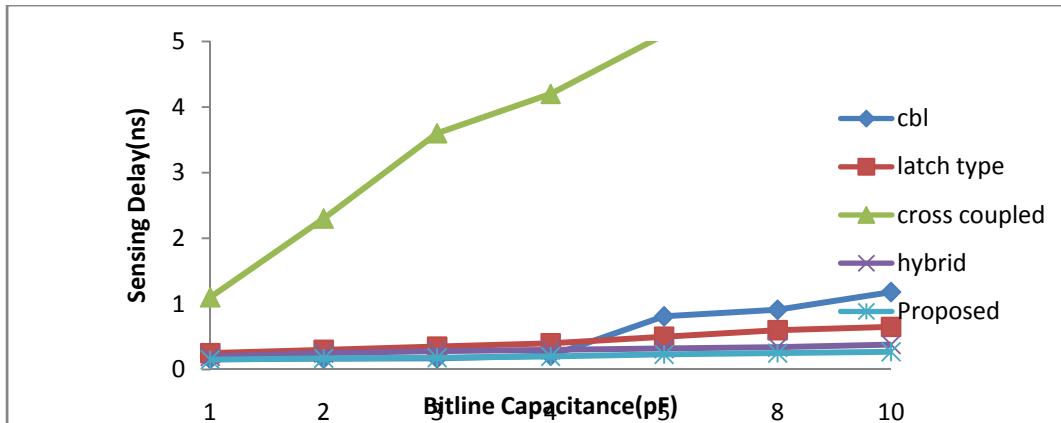
4.2 Comparison of different Sense Amplifiers

The comparison of cross coupled, clamped bitline, alpha latch, hybrid and proposed sense amplifier is analyzed, here we compare the variation of sensing delay with increase in bitline capacitance and decrease in power supply. Also the average power variation with bitline capacitance is analyzed here. For different sense amplifiers the variation of sensing delay with respect to bitline capacitance is shown in Table 4.1, from these results it has been observed that with increase in bitline capacitance the sensing delay also increases which reduces the speed of the sensing amplifier. So to overcome this problem we should isolate the output node from the bitlines.

Table 4.1: Variation of Sensing delay with respect to bitline capacitance for different Sense Amplifiers

Sense Amplifier	Cross Coupled Sense Amplifier	Clamped Bitline Sense Amplifier	Latch Type Sense Amplifier	Hybrid Sense Amplifier	Proposed Sense Amplifier
Bitline Capacitance					
1 pF	1.1	0.16	0.25	0.2	0.15
2 pF	2.3	0.165	0.3	0.25	0.17
3 pF	3.6	0.17	0.35	0.28	0.18
4 pF	4.2	0.21	0.4	0.3	0.2
5 pF	5.1	0.81	0.5	0.32	0.23
8 pF	7.1	0.91	0.6	0.34	0.25
10 pF	8.2	1.18	0.65	0.38	0.27

In Figure 4.5 the variation of sensing delay with respect to bitline capacitance is shown from here it is observed that in case of cross coupled Sense Amplifier the variation is very large as compare to other sense amplifiers and also proposed sense amplifier has least delay variation with increase in bitline capacitance, so the proposed sense amplifier can be used in high speed applications.

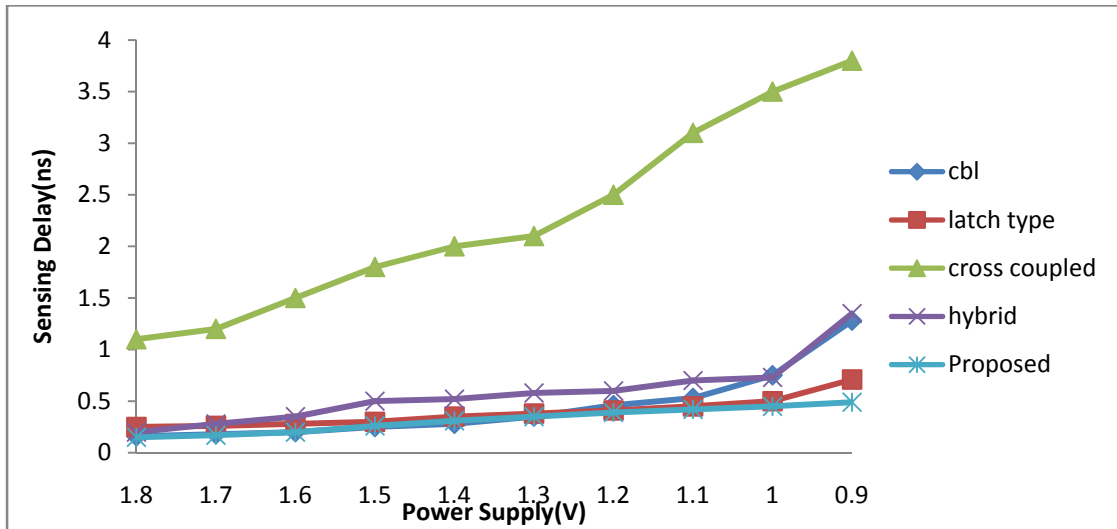


Channel length = 0.18 μm , Supply voltage = 1.8 V, Load capacitance = 1 pF

Figure 4.5 Sensing delay of different sense amplifiers with respect to Bitline Capacitance. In Table 4.2 and Figure 4.6 the variation of Sensing delay with respect to Power Supply is shown, from above observation with decrease in power supply the sensing delay of sense amplifier increases. So at low supply voltage the delay of sense amplifier is high. The variation in case of cross coupled is maximum and in case of Proposed sense amplifier is minimum.

Table 4.2: Variation of sensing delay w.r.t Power Supply for different Sense Amplifiers

Sense Amplifier	Cross Coupled Sense Amplifier	Clamped Bitline Sense Amplifier	Latch Type Sense Amplifier	Hybrid Sense Amplifier	Proposed Sense Amplifier
Power Supply					
1.8	1.1	0.16	0.25	0.2	0.15
1.7	1.2	0.18	0.26	0.28	0.17
1.6	1.5	0.2	0.28	0.35	0.2
1.5	1.8	0.25	0.3	0.5	0.26
1.4	2	0.28	0.35	0.52	0.31
1.3	2.1	0.35	0.38	0.58	0.35
1.2	2.5	0.46	0.41	0.6	0.39
1.1	3.1	0.53	0.45	0.7	0.42
1.0	3.5	0.75	0.5	0.73	0.45
0.9	3.8	1.28	0.71	1.35	0.49



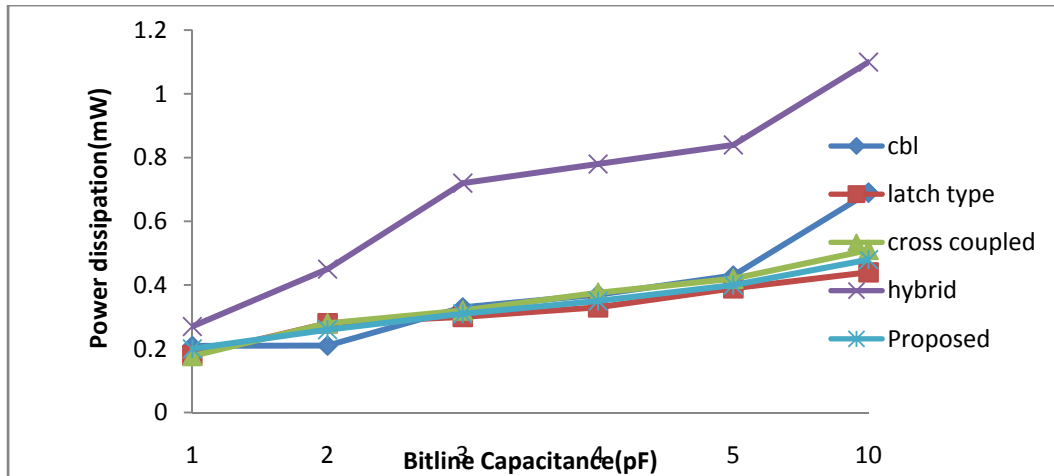
Supply voltage = 1.8 V, Bitline Capacitance=1 pF, Load Capacitance = 1pF

Figure 4.6 Sensing delay with respect to Power supply

In Table 4.3 and Figure 4.7 the variation of Average Power with respect to bitline capacitance is shown, from these results it is observed that with increase in bitline capacitance the average power also increases. In case of hybrid sense the variation of average power with increase in bitline capacitance is maximum and in case of latch type sense amplifier variation of average power is minimum.

Table 4.3: Variation of Power dissipation with respect to bitline capacitance for different Sense Amplifiers

Sense Amplifier	Cross Coupled Sense Amplifier	Clamped Bitline Sense Amplifier	Latch Type Sense Amplifier	Hybrid Sense Amplifier	Proposed Sense Amplifier
Bitline capacitance					
1 pF	0.177	0.209	0.18	0.27	0.2
2 pF	0.28	0.21	0.28	0.45	0.26
3 pF	0.32	0.33	0.3	0.72	0.31
4 pF	0.376	0.37	0.33	0.78	0.35
5 pF	0.42	0.43	0.39	0.84	0.4
10 pF	0.51	0.69	0.44	1.1	0.48



Supply voltage = 1.8 V, Bitline Capacitance=1 pF, Load Capacitance = 1pF

Figure 4.7 Average Power with respect to bitline parasitic capacitance

4.3 Delay power comparison of different Sense Amplifiers

The power and delay are two parameters which determine that how efficient is your system, so for a highly efficient system the power and delay both should be minimum or in other words power delay product should be minimum. Power delay product comparison of different Sense Amplifiers is shown in Table 4.4. From these results it is observed that in case of cross coupled sense amplifier the power delay product is maximum where in other cases the power delay product is optimum but in case of proposed sense amplifier the power delay product is minimum.

Table 4.4 Power delay product comparison of different Sense Amplifiers

Sense Amplifier	Power (μW)	Delay (ns)	Power-Delay product ($\mu W - ns$)
Cross Coupled	0.177	1.1	0.1947
Clamped Bitline	0.209	0.16	0.03344
Alpha Latch	0.18	0.25	0.045
Hybrid Type	0.27	0.2	0.054
Proposed	0.2	0.15	0.03

Power delay product comparison of different sense amplifier with increase in bitline capacitance is shown in Figure 4.8. From these results it is observed that in case of cross coupled sense amplifier the power delay product is maximum for all value of bitline capacitance but in case of proposed sense amplifier the value of power delay product is minimum for all value of bitline capacitance. So proposed sense amplifier can be used in high speed and low power applications.

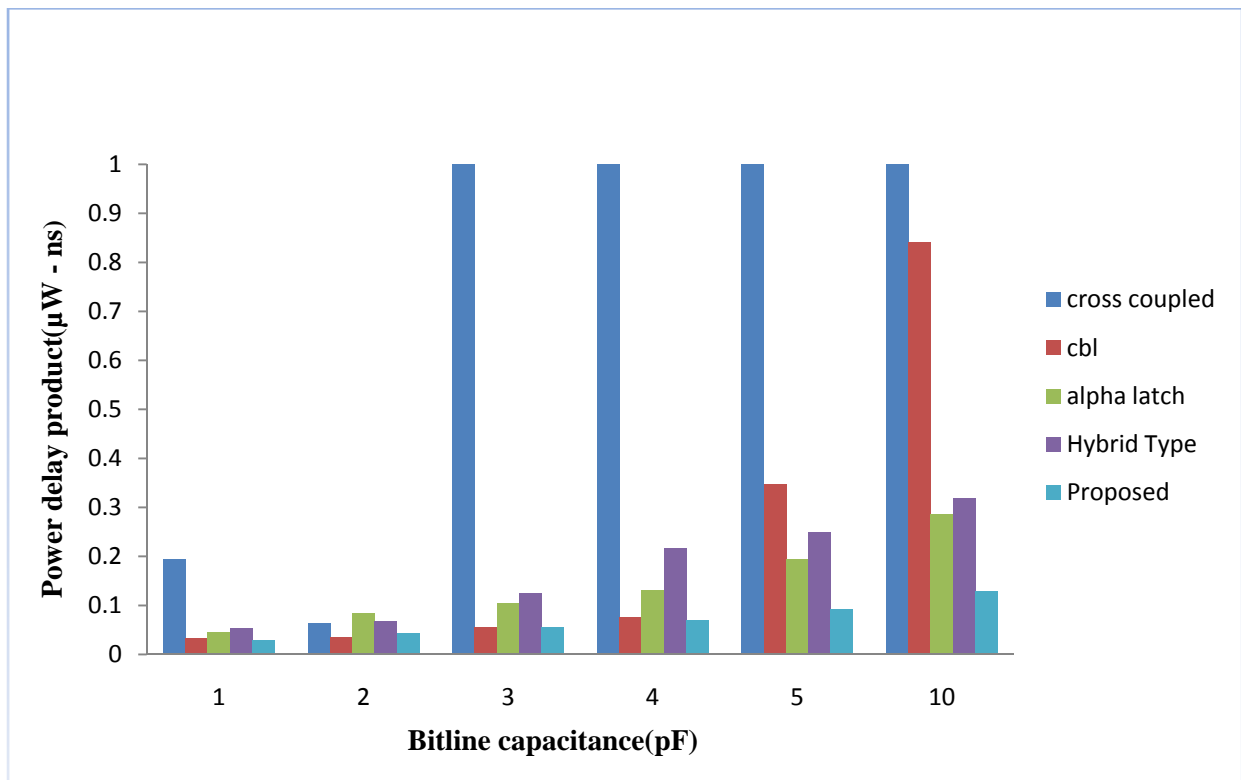


Figure 4.8 Power delay product comparison of different Sense Amplifiers with respect to bitline capacitance

5.1 Conclusion

The proposed Sense Amplifier has been designed in standard 180 nm technology. The design of proposed sense amplifier has been done on the basis of the characteristics of various sense amplifiers. The latch type sense amplifier has been found to be most efficient sense amplifier among these. The performance of latch sense amplifier has been further enhanced by isolating its input by inserting the pass transistors. This type of sense amplifier can be used in the SRAM for achieving high speed with low power. This sense amplifier circuit achieves a nominal value of sensing delay of 0.15 ns and average power of 0.2 mW, for the bitline capacitance of 1 pF and supply voltage of 1.8 V. These simulated results indicate that the designed sense amplifier has been 40% faster than latch type sense amplifier without any increment in power consumption.

The designed sense amplifier has been compared with the existing sense amplifiers. Here a lot of improvements have been observed in sensing delay with respect to variation in bitline capacitance or power supply.

By comparing the results it has been found that when bitline capacitance increases the designed sense amplifier shows minimum delay and less power dissipation than others. By analyzing Table 4.1 and 4.3, it has been seen that when bitline capacitance increases, there is a small change in the sensing delay and the power dissipation of latch type, clamped bitline and hybrid sense amplifiers while in cross coupled sense amplifier the delay is very large but power dissipation is less. Also variation in sensing delay with respect to power supply has been compared and it has been found that in the designed sense amplifier the delay is much lesser than the other sense amplifiers.

By analyzing the above and all other results it can be concluded that the delay of sense amplifier is reduced if the output is isolated from bitline capacitance.

5.2 Future Scope

In case of sense amplifier the small difference between the bitlines is amplified to the full digital level. So there may be a chance of false switching of output due to small offset voltage at the input. By employing offset compensation techniques this problem can be overcome. Also by using low power and high speed logic techniques such as Multi Threshold CMOS (MTCMOS) and Variable threshold CMOS (VTCMOS) the power dissipation can be further reduced and the speed of circuit can be further enhanced

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REFERENCES:

1. Chun-Lung and Mean-Hom Ho “High Speed Sense Amplifier for SRAM applications” IEEE Asia-Pacific conference on circuits and systems pp 577-580 december 6-9,2004.
2. E. Sccevinck, P. J. van Beers, and H. Ontrop, “Current-Mode Techniques for High-Speed VLSI Circuits with Application to Current Sense Amplifier for CMOS SRAMs,” IEEE Journal of Solid-State Circuits vol.26 No.4 pp.525-536 April 1991.
3. Tegze P.Haraszti, “CMOS memory circuits”, Kluwer Academic Publishers”, 2000, pp 165-275.
4. 2002 International Technology Roadmap for Semiconductors.
5. Kiyoo Itoh, “VLSI Memory Chip Design”, Springer International Edition, 1st edition 2001
6. Hodges and Jackson, “Analysis and Design of Digital Integrated Circuits”, Tata Mcgraw Hill publication, 2nd edition , 2004.
7. John M. Raebey, A. Chandrakasan and B. Nicolic, “Digital Integrated Circuits”, PHI publication, 2nd edition , 2003.
8. Anh-Tuan Do, Jeremy Low Yung Shern, Zhi-Hui Kong, Kiat-Seng Yeo, and Joshua Low Yung Lih “A Full Current-mode Sense Amplifier for Low-power SRAM Applications” IEEE conference publications pp :1506 -1515, 2001.
9. A. Chrisanthopoulos, Y. Moisiadis, Y. Tsiatouhas and A. Arapoyanni “Comparative study of different current mode sense amplifiers in submicron CMOS technology”, IEE Proc.-Circuits Devices Syst., vol. 149, No. 3, June 2002.
10. Blalock, T.N. and Jaeger, R.C.,”A High-speed Clamped Bit-line Current-mode Sense Amplifier”, IEEE Journal of Solid-State Circuits, vol. 26, no. 4, pp542-548, April 1991.
11. Anh-Tuan Do, Zhi-Hui Kong, Kiat-Seng Yeo, and Jeremy Yung Shern Low “Design and Sensitivity Analysis of a New Current-Mode Sense Amplifier for Low-Power SRAM” IEEE Transactions on Very large Scale Integration(VLSI) Systems, vol. 19, no. 2, Feb 2011.

12. Anh Tuan Do, Jeremy Low Yung Shern, Zhi Hui Kong, Kiat Seng Yeo and Josuha Low Lih, "A Full Current mode Sense Amplifier for Low Power SRAM applications" IEEE Divison of Circuits and Systems 2008.
13. Do Anh Tuan, Kong Zhi Hui, and Yeo Kiat Seng, "Hybrid mode SRAM sense amplifiers new approach on transistor sizing" IEEE transactions on circuits and systems vol. 55, no.10 october 2008.
14. K. S. Yeo, "New current conveyer for high-speed low-power current sensing," IEE Proc. Circuits Dev. Syst., vol. 145, no. 2, pp. 85–89, Apr.1998.
15. Sung – Mo Kang, Yusuf Leblebici "CMOS Digital Integrated Circuits", Tata Mcgraw Hill publication, 3rd edition, 2003.
16. James T. Kao and Anantha P. Chandrakasan, "Dual-Threshold Voltage Techniques for Low-Power Digital Circuits", IEEE Journal Of Solid-state Circuits, vol. 35, No. 7, pp.1009-1018, 2000.
17. A. Chrisanthopoulos, Y. Tsiatouhas, A. Arapoyanhi and Th. Haniotakis "SRAM oriented memory sense amplifier design in 0.18um CMOS technology", IEEE conference publications vol. 5 pp V-145-148 2002.
18. K. S. Yeo, W. L. Goh, Z. H. Kong, Q. X. Zhang, and W. G. Yeo, "High performance, low-power current sense amplifier using a cross-coupled current-mirror configuration," IEE Proc. Circuits Dev. Syst., vol. 149, no. 5–6, pp. 308–314, Oct./Dec. 2002.
19. Z. H. Kong, K. S. Yeo, and C. H. Chang, "An ultra low-power current mode sense amplifier for SRAM applications," J. Circuits, Systems & Computers, vol. 14, no. 5, pp. 939-951, 2005.
20. S. Patil, M. Wieckowski, and M. Margala, "A self-biased charge transfer sense amplifier," in IEEE Int. Symp. Circuits and Syst., vol. 4, pp. 3030-3033, 2007.
21. Ya Chun Lai and Shi Yu Huang, "A Resilient and Power Efficient Automatic Power Down Sense Amplifier for SRAM Design", IEEE transaction on circuits and systems vol.55, no. 10, october 2008.

22. R. Singh and N. Baht, "An offset compensation technique for latch type sense amplifiers in high-speed low-power SRAMs," *IEEE Trans. VLSI Syst. Trans. Briefs*, vol. 12, no. 6, pp. 652–657, Jun. 2004.
23. Hajimiri and R. Heald, "Design issues in cross-coupled inverter sense amplifier," in *Proc. IEEE Int. Symp. Circuits Syst.*, 1998, vol. 2, pp. 149–152.

APPENDIX A

LAYOUT DESIGN RULES

The basic design rules are summarized below:

Metal 1 to metal 1 spacing	0.24 μm
Minimum contact size	0.24 μm *0.24 μm
Poly to poly spacing	0.24 μm
Poly to metal spacing	0.28/0.00 μm
Contact overlap to p+ diffusion	0.1 μm
Metal 1 width	0.24 μm
Poly extension beyond active	0.22 μm
Minimum contact spacing	0.26 μm
N well overlap p+ diffusion	0.43 μm
Diffusion contact to poly spacing	0.15 μm
Minimum p+ implant overlap p+ diffusion	0.22 μm
Poly width	0.18 μm
Minimum poly extension on to field region	0.22 μm
Poly contact to diffusion edge spacing	0.18 μm
Minimum poly overlap contact	0.1 μm
Minimum metal area	0.1764 μm * μm
Minimum metal2 width	0.28 μm
Metal1 and metal2 overlap over via	0.08 μm
Minimum equal potential N-well spacing	0 μm or ≥ 0.9 μm
Minimum non equal potential 1.8 V N well spacing	2 μm

APPENDIX B

A.1 PTM level 53 model

This model is used for simulation of equivalent circuit model on Cadence.

.model nmos level = 53

```
+version = 4.0          binunit = 1          paramchk= 1          mobmod = 0
+capmod = 2            igcmod = 1          igbmod = 1          geomod = 1
+diomod = 1           rdsmod = 0          rbodymod= 1         rgatemod= 1
+permod = 1           acnqsmod= 0        trnqsmod= 0
+tnom = 27            toxex = 6.5e-010   toxp = 4e-010       toxm = 6.5e-010
+dtox = 2.5e-010      epsrox = 3.9       wint = 5e-009       lint = 1.35e-009
+ll = 0               wl = 0             lln = 1             wln = 1
+lw = 0               ww = 0             lwn = 1             wwn = 1
+lwl = 0              ww1 = 0            xpart = 0           toxref = 6.5e-010 xl
= -9e-9
+dlcig = 1.35e-009
+vth0 = 0.3692        k1 = 0.2           k2 = 0             k3 = 0
+k3b = 0              w0 = 2.5e-006     dvt0 = 1           dvt1 = 2
+dvt2 = 0             dvt0w = 0         dvt1w = 0         dvt2w = 0
+dsub = 0.078         minv = 0.05        voffl = 0          dvtp0 = 1e-011
+dvtp1 = 0.1         lpe0 = 0           lpeb = 0           xj = 7.2e-009
+ngate = 1e+023       ndep = 1.2e+019   nsd = 2e+020       phin = 0
+cdsc = 0             cdsch = 0          cdsd = 0           cit = 0
+voff = -0.13         nfactor = 2.3      eta0 = 0.0045      etab = 0
+vfb = -1.058         u0 = 0.0181        ua = -5e-010       ub = 1.7e-018
+uc = 0               vsat = 200000      a0 = 1             ags = 0
+a1 = 0               a2 = 1             b0 = 0             b1 = 0
+keta = 0.04          dwg = 0            dwb = 0            pclm = 0.06
+pdibl1 = 0.001       pdibl2 = 0.001     pdiblc = -0.005    drou = 0.5
+pvag = 1e-020        delta = 0.01        pscbe1 = 2.0e+009  pscbe2 = 1e-007
+fprout = 0.2         pdits = 0.01       pditsd = 0.23      pditsl = 2300000
```

+rsh = 5	rds = 60	rsw = 30	rdw = 30
+rdsmin = 0	rdwmin = 0	rswmin = 0	prwg = 0
+prwb = 0	wr = 1	alpha0 = 0.074	alpha1 = 0.005
+beta0 = 30	agidl = 0.0002	bgidl = 2.1e+009	cgidl = 0.0002
+egidl = 0.8	aigbacc = 0.012	bigbacc = 0.0028	cigbacc = 0.002
+nigbacc = 1	aigbinv = 0.014	bigbinv = 0.004	cigbinv = 0.004
+eigbinv = 1.1	nigbinv = 3	aigc = 0.0213	bigc = 0.0025889
+cigc = 0.002	aigsd = 0.0213	bigsd = 0.0025889	cigsd = 0.002
+nigc = 1	poxedge = 1	pigcd = 1	ntox = 1
+xrcrg1 = 12	xrcrg2 = 5		
+cgso = 7e-011	cgdo = 7e-011	cgbo = 0	cgdl = 7.5e-013
+cgsl = 7.5e-013	clc = 1e-007	cle = 0.6	cf = 1.1e-010
+ckappas = 0.6	ckappad = 0.6	vfbcv = -1	acde = 1
+moin = 15	noff = 1	voffev = 0	
+kt1 = -0.154	kt1l = 0	kt2 = 0.022	ute = -1.1
+ua1 = 1e-009	ub1 = -1e-018	uc1 = -5.6e-011	prt = 0
+at = 33000			
+fnoimod = 1	tnoimod = 0	noia = 6.25e+041	noib = 3.125e+026
+noic = 8.75e+009	em = 41000000	af = 1	ef = 1
+kf = 0	tnoia = 1.5	tnoib = 3.5	ntnoi = 1
+jss = 1.2e-006	jsws = 2.4e-013	jswgs = 2.4e-013	njs = 1
+ijthsfwd = 0.1	ijthsrev = 0.1	bvs = 10	xjbvs = 1
+jsd = 1.2e-006	jswd = 2.4e-013	jswgd = 2.4e-013	xjbvd = 1
+pbs = 1	cjs = 0.0018	mjs = 0.5	pbsws = 1
+cjsws = 1.2e-010	mjsws = 0.33	cjswgs = 2.1e-010	cjd = 0.0018
+cjswd = 1.2e-010	mjswd = 0.33	pbswgd = 1	cjswgd = 2.1e-010
+mjswgd = 0.33	tpb = 0	tcj = 0	tpbsw = 0
+tcjsw = 0	tpbswg = 0	tcjswg = 0	xtis = 3
+dmcg = 0	dmc = 0	dmdg = 0	dmcgt = 0
+dwj = 0	xgw = 0	xgl = 0	

```

+rshg = 0.4      gbmin = 1e-010      rbpb = 5      rbpd = 15
+rbps = 15      rbdb = 15      rbsb = 15      ngcon = 1
.model pmos level = 53
+version = 4.0      binunit = 1      paramchk= 1      mobmod = 0
+capmod = 2      igcmod = 1      igbmod = 1      geomod = 1
+diomod = 1      rdsmod = 0      rbodymod= 1      rgatmod= 1
+permod = 1      acnqsmod= 0      trnqsmod= 0
+tnom = 27      toxex = 6.7e-010      toxp = 4e-010      toxm = 6.7e-010
+dttox = 2.7e-010      epsrox = 3.9      wint = 5e-009      lint = 1.35e-009
+ll = 0      wl = 0      lln = 1      wln = 1
+lw = 0      ww = 0      lwn = 1      wwn = 1
+lwl = 0      ww1 = 0      xpart = 0      toxref = 6.7e-010      xl = -9e-9
+dlcig = 1.35e-009
+vth0 = -0.25399      k1 = 0.2      k2 = -0.01      k3 = 0
+k3b = 0      w0 = 2.5e-006      dvt0 = 1      dvt1 = 2
+dvt2 = -0.032      dvt0w = 0      dvt1w = 0      dvt2w = 0
+dsusb = 0.1      minv = 0.05      voffl = 0      dvtp0 = 1e-011
+dvtp1 = 0.05      lpe0 = 0      lpeb = 0      xj = 7.2e-009
+ngate = 1e+023      ndep = 4.4e+018      nsd = 2e+02      phin = 0
+cdsc = 0      cdscb = 0      cdsd = 0      cit = 0
+voff = -0.13      nfactor = 2.3      eta0 = 0.0037      etab = 0
+vfb = -1.058      u0 = 0.0023      ua = -5e-010      ub = 1.6e-018
+uc = 0      vsat = 78000      a0 = 1      ags = 1e-020
+a1 = 0      a2 = 1      b0 = 0      b1 = 0
+keta = -0.047      dwg = 0      dwb = 0      pclm = 0.1
+pdiblc1 = 0.001      pdiblc2 = 0.001      pdiblc3 = 3.4e-008      droul = 0.6
+pvag = 1e-020      delta = 0.01      pscbe1 = 2e+009      pscbe2 = 9.58e-007
+fproul = 0.2      pdits = 0.08      pditsd = 0.23      pditsl = 2300000
+rsh = 5      rdsu = 60      rsw = 30      rdw = 30
+rdsuimin = 0      rdwimin = 0      rswimin = 0      prwg = 0

```

+prwb = 0	wr = 1	alpha0 = 0.074	alpha1 = 0.005
+beta0 = 30	agidl = 0.0002	bgidl = 2.1e+009	cgidl = 0.0002
+egidl = 0.8	aigbacc = 0.012	bigbacc = 0.0028	cigbacc = 0.002
+nigbacc = 1	aigbinv = 0.014	bigbinv = 0.004	cigbinv = 0.004
+eigbinv = 1.1	nigbinv = 3	aigc = 0.012731	bigc = 0.00115
+cigc = 0.0008	aigsd = 0.012731	bigsd = 0.00115	cigsd = 0.0008
+nigc = 1	poxedge = 1	pigcd = 1	ntox = 1
+xrcrg1 = 12	xrcrg2 = 5		
+cgso = 7e-011	cgdo = 7e-011	cgbo = 0	cgdl = 3e-011
+cgsl = 3e-011	clc = 1e-007	cle = 0.6	cf = 1.1e-010
+ckappas = 0.6	ckappad = 0.6	vfbcv = -1	acde = 1
+moin = 15	noff = 1	voffcv = 0	
+kt1 = -0.14	kt1l = 0	kt2 = 0.022	ute = -1.1
+ua1 = 1e-009	ub1 = -1e-018	uc1 = -5.6e-011	prt = 0
+at = 33000			
+fnoimod = 1	tnoimod = 0	noia = 6.25e+041	noib = 3.125e+026
+noic = 8.75e+009	em = 41000000	af = 1	ef = 1
+kf = 0	tnoia = 1.5	tnoib = 3.5	ntnoi = 1
+jss = 2e-007	jsws = 4e-013	jswgs = 4e-013	njs = 1
+ijthsfwd= 0.1	ijthsrev= 0.1	bvs = 10	xjbvs = 1
+jsd = 2e-007	jswd = 4e-013	jswgd = 4e-013	xjbvd = 1
+pbs = 1	cjs = 0.0015	mjs = 0.5	pbsws = 1
+cjsws = 9.4e-011	mjsws = 0.33	cjswgs = 2e-010	cjd = 0.0015
+cjswd = 9.4e-011	mjswd = 0.33	pbswgd = 1	cjswgd = 2e-010
+mjswgd = 0.33	tpb = 0	tcj = 0	tpbsw = 0
+tcjsw = 0	tpbswg = 0	tcjswg = 0	xtis = 3
+dmcg = 0	dmdg = 0	dmcgt = 0	xgw = 0
+xgl = 0			
+rshg = 0.1	gbmin = 1e-012	rbpb = 50	rbpd = 50
+rbps = 50	rbdb = 50	rbsb = 50	ngcon = 1