Role of AI in VLSI Device Modelling

A Thesis submitted in partial fulfillment of the requirement for the Award of the Degree of

MASTER OF TECHNOLOGY

in VLSI DESIGN

Submitted By

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DECLARATION

I, **Jitendra Kumar** hereby declare that the work presented in this thesis entitled **"Role of AI in VLSI Device Modelling"** in partial fulfillment of the requirement for the award of degree of **Master of Technology (VLSI Design)** submitted at Electronics & Communication Department**,** Thapar Institute of Engineering & Technology (Deemed to be University), Patiala is an authentic record of work carried out under the supervision of **Dr. Rajneesh Sharma and Dr. Ashu Sharma** (Assistant Professor, Electronics & Communication Department, Thapar Institute of Engineering &Technology)

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Abstract

The rapid advancement of Artificial Intelligence (AI) has significantly impacted various scientific and engineering disciplines, including Very Large-Scale Integration (VLSI) device modeling. Traditional modeling approaches in VLSI rely on physics-based equations and empirical data, often requiring extensive computational resources and time. AI-driven methodologies, particularly machine learning and deep learning techniques, offer a more efficient and accurate alternative for device modeling and performance prediction.

This thesis explores the role of AI in VLSI device modeling, emphasizing the use of neural networks, regression models, and reinforcement learning to predict critical device parameters such as current-voltage characteristics, leakage currents, and threshold voltages. By leveraging AI-based models, the research demonstrates improved accuracy and reduced computational complexity compared to conventional techniques. The study also evaluates various AI algorithms, including artificial neural networks (ANNs), convolutional neural networks (CNNs), and recurrent neural networks (RNNs), in predicting semiconductor device behavior.

Furthermore, this work examines the integration of AI with physics-based modeling to enhance interpretability and reliability. Comparative analysis with industry-standard simulation tools highlights the effectiveness of AI-driven approaches in optimizing VLSI device design. The research findings indicate that AI can significantly improve predictive accuracy, accelerate the design cycle, and enable real-time optimization of VLSI circuits.

The study concludes that AI will play a crucial role in the future of semiconductor modeling, paving the way for more efficient, intelligent, and scalable VLSI design methodologies. This work serves as a foundation for further research into AI-driven automation in semiconductor technology.

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LIST OF ABBREVIATIONS

ML: Machine Learning

AI: Artificial Intelligence

ReLU: Rectified Linear Unit

RNN: Recurrent Neural Network

TCAD: Technology Computer-Aided Design

CNN: Technology Computer-Aided Design

MLP: Multilayer Perceptron

CAD: Computer-Aided Design

DNN: Computer-Aided Design

Tanh: Hyperbolic Tangent

MSE: Mean Squared Error

ADAM: Adaptive Moment Estimation

LG: Gate length

Wsi: Silicon Body width

Wf: Gate work function

Tox: Gate oxide thickness

CL: Channel Length

Tsi: Silicon Body Thickness

Chapter 01

INTRODUCTION

Computer-Aided Design tool is very helpful in automation of design; with the help of CAD tool, we solve the any specific design tasks along with more efficiently. but, when that kind of tool putting together on one place, their capability and functionality may be decrease. to avoid that kind of problem at different level of the design process, researchers solve this kind of problem with the help of Artificial Intelligence (AI) techniques into VLSI design automation. Artificial intelligence, machine learning, and neural network are playing an important role in nanoscale semiconductor device modelling because it can manage complicate, non-linear relationships between the physical parameters and its electrical behavior. conventional physics-based models can be time-consuming and may not grape all the complex behaviors, especially in advanced semiconductor technologies. AI/ML/NN approach can fast analyzed bulk data set, improved accuracy, and predict device characteristics under various conditions, and provide faster design cycles, optimization, and improved over all performance like Low power, low leakage and high speed in semiconductor devices [12].

1.1 Handling complex Device behavior:

Nonlinear characteristics: Now days modern semiconductor devices like MOSFETs decrease in size (e.g., below 7nm), they show highly non-linear behavior because of different kind of effects like quantum mechanics, short-channel effect, and parasitic. Conventional physics-based models struggle to accurately grape these behaviors, mainly when the scale of device near to nano-meter.

Device performance depends various kind of parameters like material properties, geometry, temperature. With the help of different data set of devices, we can excel AI/ML/NN model to identifying complex relationships between these variables, provide more accurate predictions without going in detailed [12].

1.2 Efficiency in Simulation and Design:

Time-consuming Traditional Models: traditional approach like (TCAD) simulations are computationally very costly and time consuming. These kinds of method require deep physics modelling, and that phenomena can take huge time for advanced, complex structures. With the help of huge data set once AI/ML models are trained, it is able to generate accurate device prediction in a little bit of the time. These models use past experimental data or result from initial simulations to make faster predictions about device behavior under various conditions, hence speeding up the design cycle significantly [10].

1.3 Acceleration of Device Simulations:

Conventional device simulation, like those which is driven by Technology Computer- Aided Design (TCAD), it is depends on physics-based models like drift-diffusion or Poisson equation. It provides highly accurate simulation and model, but that consume huge time and computing power, in case of when we dealing with large and complex circuits or new device structure like FinFets, Tunnel Fet and CNT.

Machine learning and Artificial Neural Network (ANNs), perform simulation how device behave much faster by learning from the huge datasets which is created by conventional simulations like TCAD. Once trained, an Artificial Neural Network that can be predict important device features (like current-voltage or capacitance-voltage relationships) in fast manner, with similar accuracy which is observed in conventional mechanism. It is very helpful to reduce time require for test and new designs or enhance existing ones [10].

1.4 Reduction in Computational Costs:

AI-based simulation consumes very less computer resources for semiconductor device modelling. In place of AI-based simulation if we use conventional physics-based simulations need powerful supercomputers or special hardware, while we use AI-based simulation no need of supercomputers or special hardware like this thing. AI model scan run on normal computers, this makes the process faster and more accessible.

Chapter 02

Literature Survey

N. BOURBAKIS *et al*. Present ML/AI mechanism have great potential to reduce various obstacles in VLSI design automation. AI/ML methods including expert system and heuristic algorithms, have provided solution to complex design tasks. Because traditional algorithmic methods face hardness to provide solution for complex design. This literature talks about the CAD tools need to become more user friendly and easier to use. It is able to opt various IC Technologies and enhance users interact with them, to make tools more useful and effective that change is important.

Even with advancement, the paper points out various challenges still in using AI in CAD Tool. AI/ML faced various difficulty of handling unclear tasks, so further more research and development are needed. To take fully advantage of AI/ML in VLSI automation [1].

Huifan Zhang *et al*. This literature overcome dependency of CAD tool with the help of M/L and artificial neural networks (AANs). Machine learning provides a framework to use artificial neural networks to model the I-V (current-voltage) and C-V (capacitance- voltage) behavior of FinFet devices. In this approach considering different inputs like gate voltage and the shape of the device, helps to predict current and capacitance accurately. 3D semiconductor device like FinFets, that are replaced traditional planar MOSFETs due to FinFets provide better performance.

The authors suggest a two-phase machine learning technique adjusting continuous curves and using an ANN to predict critical spots on the I-V and C-V curves. Additionally, compared to conventional techniques, our ML-based model can enhance device performance more quickly, negating the need for many simulations. By employing this technique, the authors are able to anticipate device performance with a high degree of accuracy (98.6%), which is confirmed by more conventional simulation techniques like TCAD.

The model grape accuracy with only 160 samples, it is not depending on millions of simulations. The ML model uses two kinds of neural networks for various voltage ranges to forecast the I- V (current-voltage) and C-V (capacitance-voltage) curves. The device performance is then mostly enhanced by RC delay minimization and switching ratio (Ion/Ioff) maximization through parameter combinations. This approach produces results that nearly resemble TCAD simulations while being quicker than conventional simulations [2]

G. F *et al*. Presents collaborate physics and machine learning get better performance and enhance result; in this literature we minimize TCAD dependency or work with limited data. The framework combines physics, ML, it is able to optimization and increase CNTFET design and performance. It reduces the need of a huge data by using genetic algorithms and machine learning to predict metrics and also makes the device fast. conventionally CMOS transistors are less useful because if we scaled down the transistor power requirements are increase. Because of their higher performance, CNTFETs are an alternative better option and can be used in transistors of the future. To enhance CNTFET design, the authors provide a design framework that combines machine learning (ML), device physics, and optimization. We use Sentaurus TCAD for design and simulation of (CNTFETs), during the simulation various design parameters like channel length, gate length, and gate dielectric thickness. And Mult objective optimization was applied to find the best and accurate designs. Focusing on how adjusting gate structure and contact metal affects performance. By placing the gate near to the source, the ON current (Ion) is improved, and the OFF current (Ioff) is reduced [3].

J. Wan *et al*. Presents the advancement of artificial neural network, a new transistor model can be simulating analog circuit by using ANNs, it is able to grape electrical characteristics of transistors in place of physical-driven model. The authors highlight the limitation of widely used BSIM3 model, this is based on empirical physical equations. ANN model uses data from n-type and p-type MOSFETs which is fabricated by 0.18 μm process. And predict relationship between terminal voltages and output current. ANN consists of three layers, each having 32 neurons, and six input parameters: transistor terminal voltages (Vbs, Vgs, Vds), width, length, and temperature [4].

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P. Ojala *et al*. (2019) Presents Prior efforts have sought to predict Independent of specific technologies, the authors provide a fast and accurate neural network tool that acts as a link between circuit simulation and device modelling. Using this tool trains the network using Levenberg- Marquardt, conjugate gradient, and modified backpropagation optimization techniques. Using neural network generated device having one advantages it is monotonicity, which is very important for circuit simulation purposes.

This method is also giving the favorable outcomes, were testing face difficulty on GaAs MESFET and Si MOSFET device. The neural network generates smooth and continuous models; it is enhanced version of traditional methods. It achieved a low error rate of 2.26%, much better than the usual 5-10% accuracy of traditional models. The authors added a neural network model to the SPICE circuit The neural network model that the authors implemented to the SPICE circuit simulator performed well for both time-varying (transient) and steady-state (DC) analysis. The model's smoothness helped in avoiding any convergence issues. This shows how well neural networks work in circuit simulations [5].

Y. Lei *et al*. Presents Deep neural network provides faster and more accurate models for electronic device; the study proposes to use a deep neural network (DNN). Transconductance is the main tool used to ensure that the models function properly and provide no odd or unexpected results. This literature talks about traditional neural network model which may give unrealistic outcome if they not consider actual device physics. To compensate this, a new approach uses transconductance (instead of current) for better accuracy. This model includes some extra feature, uses techniques to avoid overfitting, and works well in all conditions without giving unrealistic results [6].

Q. Yang *et al*. Presents Combination of machine learning and physics-based modelling provide acceleration for device modelling. This paper provides a hybrid model that combination of machine learning along with physics-based modelling for better predict Nano transistor behavior, this method enhance accuracy and by focusing on transistor ballisticity, which is less susceptible to bias voltage fluctuations than current values, the training process can be made simpler. This model accurately captures exponential variation of source-drain current with gate voltage and the linear to quadratic behavior in the above-threshold region. This model is accurate and easy way to predict source- drain current since it only requires two fitting parameters. It also focusing on capacitances, charge density, and potential barriers and define transistor performance limitations. To provide a complete dataset, NEGF simulations for CNTFETs are performed with different gate oxide thicknesses and gate lengths taken into consideration. This model is 18,000 times fast compared to traditional NEGF simulations; it gives a significant performance [7].

In 1992, the first neural network-based MOS transistor model was created. The choice of mapping function presents difficulties for black box modeling. Models of microwave transistors were used to test multilayer perceptron neural networks. In 2003, the adjoint neural network approach was put out for sensitivity analysis. NeuroFET and DynaFET are two examples of measurement-based neuro models. Using tiny models, MLCM approach speeds up RF circuit analysis. The ANN method describes the S- parameters, noise, and current in HEMTs. Neural network modeling approaches have been used to a variety of semiconductor FETs [15].

Chen et al. propose a human approach using hill climbing and support vector regression for optimizing silicon on insulator (SOI) lateral power devices. Zhang et al. (2020) integrate deep neural networks (DNNs) and evolutionary algorithms (EAs) to address wear and tear effects and process variations in FinFET SRAM cells. Ashai et al. (2023) tackle the challenge of parameter extraction for the BSIMCMG semiconductor device model using a deep learning architecture combining CNN and GPT-3.5. Wang et al. (2022) employ High Throughput Virtual Screening (HTVS), Global Optimization (GO), and Generative Models (GM) for material design with specific characteristics. Huang et al. (2019) propose a strategy for efficient inverse design of structural color in photonic devices using supervised learning and reinforcement learning.[16]

Esmaeilzadeh *et al*. (2022) Presents Evaluation of machine learning models employing mean absolute percentage error (ALE) and maximum absolute percentage error (LALE) for predicting unknown target clock frequencies and configurations. When comparing the performance of several machine learning models (GBDT, RF, ANN, and Ensemble) for ASIC and FPGA implementations, average rankings reveal that the RF and Ensemble models perform better than the others. The utility of ensemble models is demonstrated by applying ML models to FPGA implementations to anticipate energy, power, system runtime, and backend performance. Utilizing ML models on VTA and Axiline platforms, design space exploration produces the finest accelerator implementations with the least amount of energy and runtime.[17]

Xufan Li *et al*. (2024) Presented as a competitive alternative for future CMOS technology nodes due to their high carrier velocity and excellent electrostatic control. The compact model for CNFETs is based on the virtual-source concept and accounts for non- idealities such as contact resistances and parasitic capacitances. The authors demonstrate the model's capability by optimizing the CNFET structure to minimize gate delay, revealing that contact resistance significantly limits performance. The findings indicate that further scaling of CNFETs is constrained by direct source-to- drain tunneling leakage current, particularly due to the small band gap of carbon nanotubes.[18]

Deepthi Amuru *et al.* Presents Traditional VLSI design is difficult, time-consuming, and resource-intensive due to design complexity and process uncertainty. Traditional approaches need human involvement at multiple abstraction levels, delaying and costing more. Data-driven AI/ML may learn complicated design and manufacturing concepts, saving labor. In device modeling, design-for-test, and yield optimization, AI increased prediction and fault diagnostics. Empirical studies show AI enhances manufacturing turnaround, IC production, and cross-layer data processing. Future deep learning and reinforcement learning advances will allow real-time adaptive design for faster, smarter, and more efficient VLSI implementations.[19]

Xufan Li *et al*. presents Ultra-scaled devices show that threshold-voltage, surface- potential, and charge-based compact models cannot capture near-threshold behavior, quantum effects, and full-chip stress. The semiconductor modeling community embraced machine-learning-assisted compact modeling (MLCM), which uses neural networks trained on TCAD or measurement data to learn complicated I–V mappings. Early MLCM models are data-driven (i-type), physics-informed (ii-type), and hybrid with a physics-based core and AI corrective layer. These approaches save simulation time by automating TCAD-to-SPICE parameter extraction, dataset curation, algorithm selection, Verilog-A code creation, and circuit simulation. Physical consistency, sub model accuracy, and dataset standardization are continuing concerns. Li et al. classified i-, ii-, and iii-type MLCM initiatives to show how a hybrid AI–physics strategy may connect theory and fabrication. Next-generation semiconductor operations benefit from hybrid models with device physics and high-fidelity I–V forecasts for design- technology co-optimization.[20]

Kam et al. Presents After decades of compact model development, such as the BSIM family and FinFET geometries, new research used machine learning to capture device nonlinearities beyond curve-fitting Physics-informed neural networks enhance semiconductor device simulation extrapolation under different bias and temperature circumstances by conserving charge and current. Lightweight neural networks and drift-diffusion solvers forecast MOSFET I-V with sub-percent accuracy and lower processing costs than TCAD simulations. Modern Verilog ML-augmented models work well with SPICE simulators for pre-silicon analog and mixed-signal circuit evaluation. Parallel capacitance-voltage and leakage modeling on shallow neural networks exhibit RF and low-power design potential. TFETs and III-V nanowire transistors benefit from data-driven correction terms in first-principles equations. Circuit simulations may be exact and expandable using compact neural networks and transistor physics.[21]

P. H. Solomon *et al*. Presents Early circuit-level power reduction research employed heuristic and evolutionary methods to improve transistor size and gate-level functionality for energy efficiency. Later work simulated power-performance trade-offs across functional blocks using regression and grouping to improve voltage and frequency scaling. DVFS runtime selections were based on SVM and Gaussian process regression forecasts of dynamic energy use under different workloads. Recent reinforcement learning systems may provide real-time performance feedback for DVFS, power gating, and resource allocation. Deep neural networks enhance circuit power profile prediction by capturing complicated nonlinear operating conditions and component behaviors. EDA power optimization benefits from simulations and lightweight data-driven correction terms. Initial AI-driven optimization in commercial EDA tools found scalable feedback loop topologies that reduced computation cost. These breakthroughs allow AI-enabled circuit optimization to conserve energy without sacrificing performance.[22]

Y. Guo *et al*. BSIM and EKV physics-based equations accurately modeled FET I-V and C-V characteristics in the first compact-model investigations, but nanoscale effects and unpredictability posed challenges. Subsequent research used regression and spline- based surrogate models to enhance SPICE turnaround, although requiring parameter fitting. Recent experiments demonstrate that shallow neural networks, using physics- informed loss functions, achieve sub-percent accuracy in I-V reproduction while effectively capturing device symmetries and conservation laws. The first work on automated ANN scaling and model retargeting demonstrated the equilibrium between model complexity, accuracy, and simulation duration.[23]

J. Wang et al. This paper addresses validation and implementation issues in DTCO procedures for ANN-based compact models for semiconductor devices. It implements Gummel symmetry and addresses discontinuities between forward and reverse transistor operating modes in a novel way. Novel loss functions for current and charge derivatives improve model accuracy to within 2%, enhancing fidelity over earlier ANN models. Comparative research with physics-based compact models for GAA standard cell libraries shows that the ANN model allows circuit simulations four times faster while maintaining delay and power prediction errors within 1%.[24]

W. Dai *et al*. Presents ANN-based device modeling improves by combining a physics- driven core from the BSIM-CMG compact model with a lightweight deep neural network to predict GAAFET I–V characteristics correctly. The hybrid model embeds a 3-layer network (6–18 neurons per layer) on the BSIM-CMG foundation to retain physical consistency, Gummel symmetry, and 3-sigma errors of 1.3% (I–V), 4.1% (output conductance), and 2.9% (transconductance) for a 12 nm GAAFET Compared to data-driven methods, physics-based features reduce training data and increase prediction fidelity. The 4× speedup and sub-1.5% error in circuit-level simulations demonstrate the potential of deep learning-augmented compact models for next- generation MOSFET design and DTCO flows.[25]

H. Kam *et al.* This work simulates GAA junction less nanowire FETs (GAA-JL- NWFETs) with significant short-channel effects using ANN-based device modeling. Using a 3-layer neural network and TCAD-generated training data, the authors achieved sub-2% RMSE for key parameters (Ids, DIBL, V_t, SS, I_{on}, I_{oo}F) and R^2 scores > 0.91, equivalent to physics Unlike previous techniques that focused on planar MOSFETs or data preprocessing, this study improves model robustness via training- loss, scatter, and density-error visualizations. The article shows that ANN models mimic complicated device behavior fourfold quicker at 350 K and 450 K. An efficient, proven ANN framework combines TCAD accuracy with circuit-level performance for next-generation semiconductor devices, boosting the industry.[26]

Abhishek Raj and Shashi Kant Sharma Presents Previous Monte Carlo TCAD simulations examined the statistical distributions of device attributes affected by line edge roughness (LER) and other variable factors in scaled MOSFET process modifications. Although lacking resolution, Gaussian process regression and polynomial chaos expansions swiftly forecasted fluctuations in threshold voltage and leakage current. Recent shallow neural networks and kernel approaches predict sub- millisecond, complex, nonlinear LER profile-device I–V interactions. In TCAD- comparable distribution matching, two-stage artificial neural networks using LER inputs anticipate mode-dependent threshold voltages and comprehensive Id–Vg curve parameters with greater efficiency.[27]

Changhwan et al. Early statistical circuit simulation approaches used Monte Carlo TCAD runs or simple lookup-table and ANN surrogates fitted to measurement data. Still, they needed large data samples or physical parameter distribution information. Under near-threshold bias, Gaussian and polynomial chaos expansions boosted speed but required large parameter information and exhibited nonlinear I–V responses. Despite variational autoencoders generating realistic data from a few samples in several fields, the moderate fluctuations and flat surface of MOSFET I–V characteristics constrain their use in compact device modeling. This VAE-based approach can encapsulate LER-induced variability from 20 device curves and provide TCAD- comparable distributions of ring-oscillator period and power for rapid, low-data- overhead statistical simulation.[28]

Kasprowicz *et al*. (2024) Presents Diffusion models have lately outperformed GANs and VAEs in data fidelity; hence, this research employs them to generate synthetic data for VLSI design. Preliminary generative techniques for enhancing electrical design data were ineffective, often demonstrating instability or insufficient generalization with limited datasets. Employing diffusion models in CMOS 22nm HSPICE simulations improves future machine learning models, such as gradient-boosting regressors, by leveraging previous research on circuit performance prediction. This suggests that diffusion-based synthetic data might improve design efficiency in data-constrained VLSI applications.[29]

P. Srivastava *et al*. In this literature, we add to what has already been learned about using machine learning to help build devices by focusing on the inverse modeling of transistor measurements using performance points like gain and bandwidth. Forward modeling of device behavior has been studied before, but dimension prediction using multi-output regression and ensemble methods has not been looked at as much. This study is more accurate than others because it uses Random Forest and log-transformed fine-tuning. Innovation is encouraged by better feature engineering, and chip design can be automated in a way that is efficient and based on data.[30]

Fredo Chavez *et al.* took a big step forward in their use of deep learning to find parameters for nanoscale models that are very small. With old optimization methods, there are lots of issues because of measurement noise and devices that are hard to predict, especially when the gate lengths are not all the same. To get BSIM-CMG numbers from I-V traits, they use Monte Carlo simulations and a deep learning method in their work. One thing that makes this model unique is that it has a strong global fitting method that can fix issues with the way it was made. It shows a possible way to measure a lot of small models properly and automatically in this case.[31]

Carrillo-Nuñez *et al.* propose using neural networks (NNs) instead of traditional TCAD simulations to predict performance measurements in silicon junction less nanowire transistors (JL-NWTs). A multi-layer neural network (NN) that was trained on 1380 devices with a variety of dopant configurations accurately predicted the metrics IOFF, ION, subthreshold slope (SS), and threshold voltage VTH, and NNs outperform generic linear models in terms of prediction quality and simulation time, resulting in a reduction of the simulation time from thousands to minutes. Their results suggest that machine learning can be implemented to improve the efficiency of research and simplify the modeling of semiconductor devices.[32]

Woo *et al.* predicted silicon nanowire feedback field-effect transistor electrical performance using TCAD-ML. The random forest regression model correctly predicted forward and reverse I-V characteristics with R^2 values of 0.9938 and 0.9953. The analysis accurately predicted memory window, saturation drain current, and latch- up/down voltages. TCAD-ML was faster and more realistic than normal TCAD simulations. The hybrid modeling technique shows how machine learning speeds device analysis and optimization. They found TCAD-ML helps advanced transistor design. The study advises using ML and physics-based models for semiconductor development.[33]

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Min-Hye Oh *et al*. used NN to analyze semiconductor device process factors and electrical property sensitivity. Unlike linear models, this method successfully incorporates nonlinear and parameter relationships for complicated device modeling. GLMs using feedback field-effect transistor (FBFET) TCAD data fared worse than NN-based sensitivity estimates. Vth and ION were accurately calculated using 1055 TCAD simulations and actual data. The technology accelerates process optimization and complex device SPICE model development. Component analysis shows process control parameter impacts. Combines innovative gadget ideas with circuit integration.[35].

TABLE I. STUDY OF IMPLEMENTING AI IN DEVICE MODELLING

Refs	Model Used	Weakness	Strength
3	Use of Support Vector Regression Chain for predictions. Multi-Output Regressors method for design metric prediction.	Potential well formation reduces ON-current efficiency	Achieves low prediction error of 1.59% with limited data. Uncovers unique trends in CNTFET behavior.
5	Evaluation using root mean square error (RMSE). Coefficient of determination (R2-score) analysis.	Potential overfitting issues are not addressed. Limited scope on device parameters analyzed.	RMSE values indicate low prediction errors for key parameters.
7	Multilayer perceptron(MLP). Recurrent neural network (RNN). Random Forest Regressor (RFR).	Careful selection of ML components. Limited training data Complexity in capturing all device parameter interactions.	It enhances interpretability & streamlines training processes. High accuracy achieved with limited training data.
8	A self-augmentation strategy using variational autoencoder (VAE) is proposed. A DNN-based regression model verifies the augmented data.	The proposed method may not generalize to all semiconductor applications.	The approach significantly reduces mean absolute error by 70%
9	Artificial neural network-based algorithm for accuracy. Surrogated NSFET-based ring oscillator simulations.	Dependence on Training Data. Complexity of Physical Phenomena.	High Accuracy Efficiency in Handling Variations.

23	A two-stage ANN model. Regression algorithms to capture core electrical parameters.	The ML-based approach can simulate performance curves efficiently without convergence issues.	TCAD simulations face severe convergence and low-efficiency issues, complicating performance simulation and structure design.
24	ANN-based compact model with Design-Technology-Cooptimization (DTCO) and pathfinding activities.	Accurately reproduce the current-voltage (I-V) and charge-voltage (Q-V) characteristics of advanced field-effect transistors (FETs).	ANN models may degrade SPICE simulation TAT due to increased size and complexity.
25	Model utilizes a feedforward artificial neural network (ANN) structure with 177 parameters and 176 operations per propagation.	The ANN model demonstrates improved accuracy with a focus on current derivatives in device modeling	The accuracy of ANN models in device simulations has not been fully validated in various application scenarios
26	Deep-learning-assisted partially physics-based model.	The model demonstrates outstanding 3-sigma errors of 1.3%, 4.1%, and 2.9% for IV.	Not capture purely Physics based model.

Chapter 03

Research Gaps & Research Objectives

3.1 Limited Quality Datasets:

To train AI models for effective modelling, requirement of huge different and good-quality data. It is very difficult to collect all the necessary and accurate information, especially for new and modern semiconductor devices. This makes it difficult to build effective AI models.

3.2 Scalability of AI Models:

Research on the suitability of AI models to various semiconductor device types and production processes is limited. The majority of AI models are made for particular device types, such as MOSFET or FinFET, and it's questionable if these models will function well with other technologies or devices**.**

3.3 Performance Prediction Under Uncertainty:

AI models find it hard to predict how devices will act when things are uncertain or unusual, like rare events. This is important for making sure devices work reliably in all situations. Right now, AI isn't good at handling this uncertainty. More research is needed to help AI better understand and predict in these conditions. This will make the models more reliable and accurate for real- world use.

Research Objectives

3.4 Developing AI models for device characterization and performance enhancement:

Utilizing machine learning techniques to anticipate optimal configurations and analyze device behavior. AI can help identify crucial performance factors, optimize energy efficiency, and detect problems in real time. AI gives gadgets the ability to adapt, be more dependable, and process information more rapidly**.**

3.5 Enhance Predictive Accuracy:

AI models can significantly enhance the predictive accuracy of device performance, exceed traditional modeling approaches. By learning complex relationships from large datasets, AI provides more precise and reliable predictions. This results in improved device optimization and design, reducing error and increasing efficiency

3.6 Reduce Computational Costs:

AI techniques can reduce the amount of time and resources needed for complex device simulations. AI speeds up and increases process efficiency since it can evaluate data more quickly than conventional methods. This leads in faster outcomes and less processing work**.**

Chapter 04

Proposed Methodology

4.1 Data Generation

Device-level data is generated using Nano Hub TCAD tools, focusing on GAAFET structures.

Simulations are carried out over a range of electrical inputs (Vgs, Vds) and physical parameters such as:

- Oxide thickness: (Tox)
- Silicon thickness: (Tsi)
- Channel length: (L)
- Gate work function: (WF)

4.2 Data Preprocessing

- All data is cleaned and normalized using **Min-Max scaling** to ensure proper training convergence.
- The dataset is split into **training** and **testing** sets.
- For RNN models, input data is reshaped to match the sequential input format

4.3 Model Development

Artificial Neural Network (ANN)

- A fully connected feedforward ANN model is developed using PyTorch.
- Multiple hidden layers with Tanh activation functions are used.
- The model outputs the predicted ID for given input conditions.

Recurrent Neural Network (RNN)

- An RNN model with 2 hidden layers and 64 units is implemented to capture nonlinear dependencies.
- The model is trained using the Adam optimizer with Mean Squared Error (MSE) as the loss function.

4.4 Model Training and Validation

- Models are trained over 100 epochs using batch sizes of 64.
- The Adam optimizer and MSE loss function are used.
- Model performance is validated using unseen test data

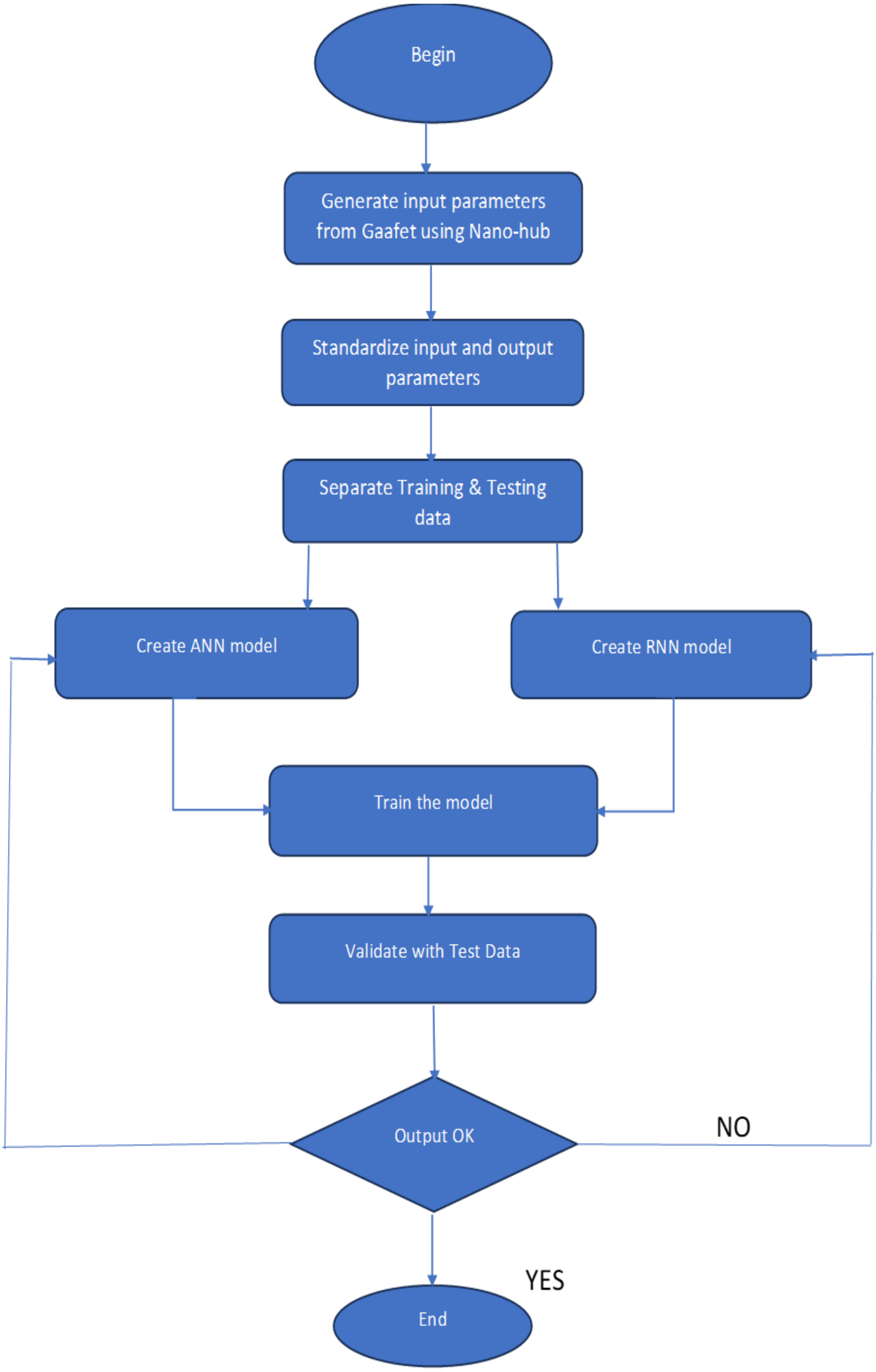

Fig 4.1: Flowchart of the Proposed Methodology

Chapter 05

Proposed Work

5.1 Device Parameter

The GAA-FET structure used in this study was designed with nanoscale dimensions suitable for advanced technology nodes. Table 5.1 summarizes the key geometrical parameters of the device. The gate length and channel length were set to 12 nm, while the width and thickness of the channel were kept at 6 nm to ensure symmetric electrostatics. Spacer and source/drain lengths were each 6 nm, and the silicon body thickness was also maintained at 6 nm to enhance gate control over the channel.

Table: 5.1 Device parameter

Parameter	Variable	Value
Gate length	Lg	12 nm
Channel width	W	6 nm
Channel Thickness	Ct	6 nm
Spacer Thickness	Sp	6 nm
Source/Drain Length	Lsd	6 nm
Channel Length	Lc	12 nm
Silicon Body Thickness	Tsi	6 nm

5.2 Device view:

The figure 6.1 illustrates a nanoscale MOSFET (Metal-Oxide-Semiconductor Field-Effect Transistor) structure, generated using the NanoHUB simulation tool. This transistor is based on Silicon-On-Insulator (SOI) technology, which improves electrostatic control over the channel and minimizes short-channel effects.

(a) Side View (Cross-Section Along the Channel)

The transistor consists of n+ source and n+ drain regions, with a p-type channel in between. The gate length (Lg) defines the active channel controlled by the gate voltage. The source/drain extensions (Lsd) represent the overlap regions adjacent to the channel. The oxide layer (Tox) is positioned above the channel, acting as an insulating barrier between the gate and the semiconductor.

(b) Top-Down View (Cross-Section Along the Width)

The silicon body width (Wsi) represents the width of the conducting channel.

The buried oxide layer (Tbox) lies beneath the silicon channel, providing electrical isolation from the substrate.

The gate oxide thickness (Tox) and oxide width (Wox) are critical parameters affecting device performance.

Significance of the Design

The thin-body structure enhances gate control, reducing short-channel effects (SCEs) and leakage currents.

The SOI architecture improves speed and power efficiency by reducing parasitic capacitances. Such transistors are ideal for low-power and high-speed applications in modern integrated circuits.

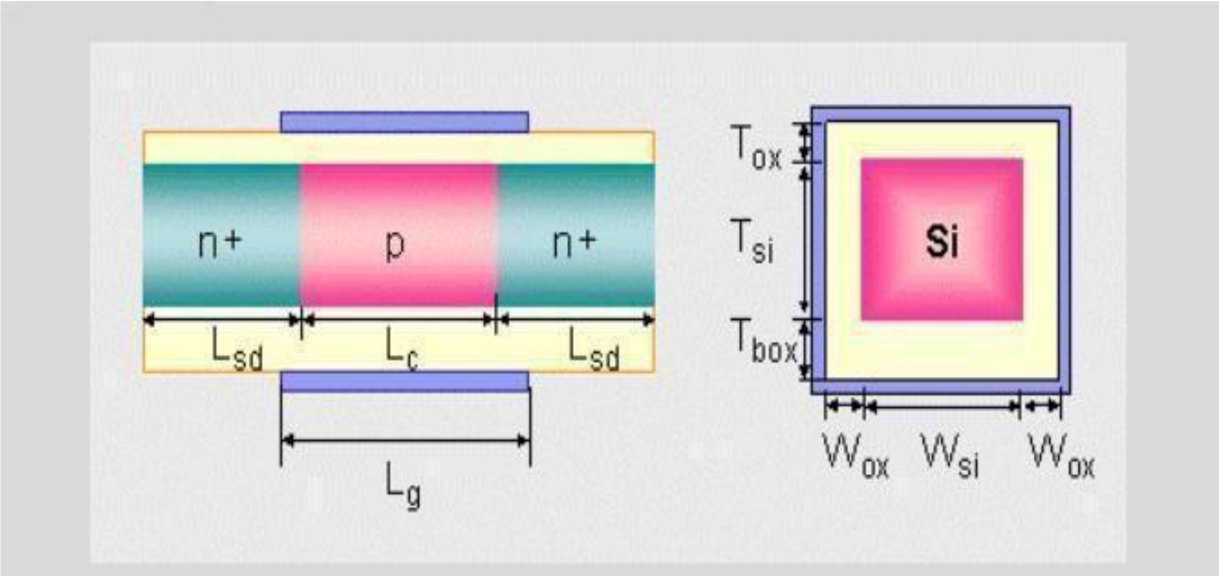

Fig: 5.1 Device structure

5.3 Artificial Neural Network Architecture for Id Prediction:

The artificial neural network (ANN) used for predicting drain current (I_D) from gate voltage (V_G) and drain voltage (V_D) consists of the following layers:

Network Layers and Neurons

- **Input Layer:** 2 neurons (representing V_G and V_D)
- **Hidden Layer 1:** 18 neurons with ReLU activation
- **Hidden Layer 2:** 18 neurons with ReLU activation
- **Output Layer:** 1 neuron with linear activation (representing Id)

Table 5.2 Neural Network Summary

Layer	Type	No of Neurons	Activation Function
Input	Dense	2	None
Hidden 1	Dense	18	ReLU
Hidden 2	Dense	18	ReLU
Output	Dense	1	Linear

Data Preprocessing

- The dataset consists of three key variables: V_G, V_D, and I_D
- Input features (V_G, V_D) and the target variable (I_D) were **normalized** using MinMaxScaler.

Training Process

- Optimizer: **Adam**

  The Adam (Adaptive Moment Estimation) optimizer is commonly used to improve deep learning model training. It adapts the learning rate for each parameter to combine the advantages of AdaGrad and RMSProp. To accelerate convergence, Adam maintains running averages of the gradients (first instant) and squared gradients (second moment). It is memory-efficient, computationally efficient, and good for large datasets and high-dimensional parameter spaces. This research tuned neural network parameters for exact device modeling using Adam.

- Loss function: **Mean Squared Error (MSE)**
- Number of epochs: **500**
- Batch size: **8**

Model Performance

- **Test Loss (MSE):** 0.0443
- **Accuracy:** 98%

5.4 Recurrent Neural Network Architecture

To model and predict the drain current ID of GAAFET devices based on physical and biasing parameters, a Recurrent Neural Network (RNN) was developed. The RNN was selected due to its ability to capture sequential dependencies and nonlinear relationships between input features and the output current.

The architecture details are as follows:

1. **Input Layer:**
   - **Input Features:** The model takes in two transformed inputs derived from the original gate voltage (V_G) and drain voltage (V_D):
     - $u1=2V_G-V_D$
     - $u2=(V_D)$^2
2. **Hidden Layers:**
   - **First Hidden Layer:**
     - Number of hidden units: **64**
     - Activation function: **Tanh**
   - **Second Hidden Layer:**
     - Number of units: **64**
     - Activation function: **Tanh**
3. **Output Layer:**
   - **Number of neurons: 1**
   - **Activation function: Linear**
   - **Output:** The predicted value of drain current ID corresponding to the given input parameters.
4. **Training Process:**
   - **Loss Function:** Mean Squared Error (MSE)
   - **Optimizer:** Adam (Learning rate = 10^-4)

     The Adam (Adaptive Moment Estimation) optimizer is commonly used to improve deep learning model training. It adapts the learning rate for each parameter to combine the advantages of AdaGrad and RMSProp. To accelerate convergence.
   - **Batch Size:** 64
   - **Epochs:** 1000
5. **Accuracy & Predictions:**
   - The model accuracy = 99%

Chapter 06

Results and Discussion

Device Parameter:

Simulations were carried out using the Nano Hub simulation platform to investigate the effects of channel length scaling on GAA-FET performance. In this configuration, the channel length was reduced to 5 nm while keeping all other device parameters unchanged. The table 6.1 below summarizes the geometrical and material parameters used for the simulation.

Table: 6.1 Device parameter

Parameter	**Variable**	**Value**
Gate length	Lg	12 nm
Silicon Body width	Wsi	5 nm
Gate work function	Wf	4.61 eV
Gate oxide thickness	Tox	1 nm
Channel Length	Cl	5 nm
Silicon Body Thickness	Tsi	6 nm

This graph 6.1 shows how the drain current I_D changes with the drain voltage V_D, based on predictions from the RNN and ANN models, compared to the reference data from Nano-Hub simulations. We evaluated the models at multiple gate voltages, specifically VGS. RNN and ANN match simulation results, with RNN matching better at higher V_D levels. The graph shows that trained neural networks can properly mimic GAAFET device nonlinear I–V behavior under varied bias conditions, making them suitable for compact modeling

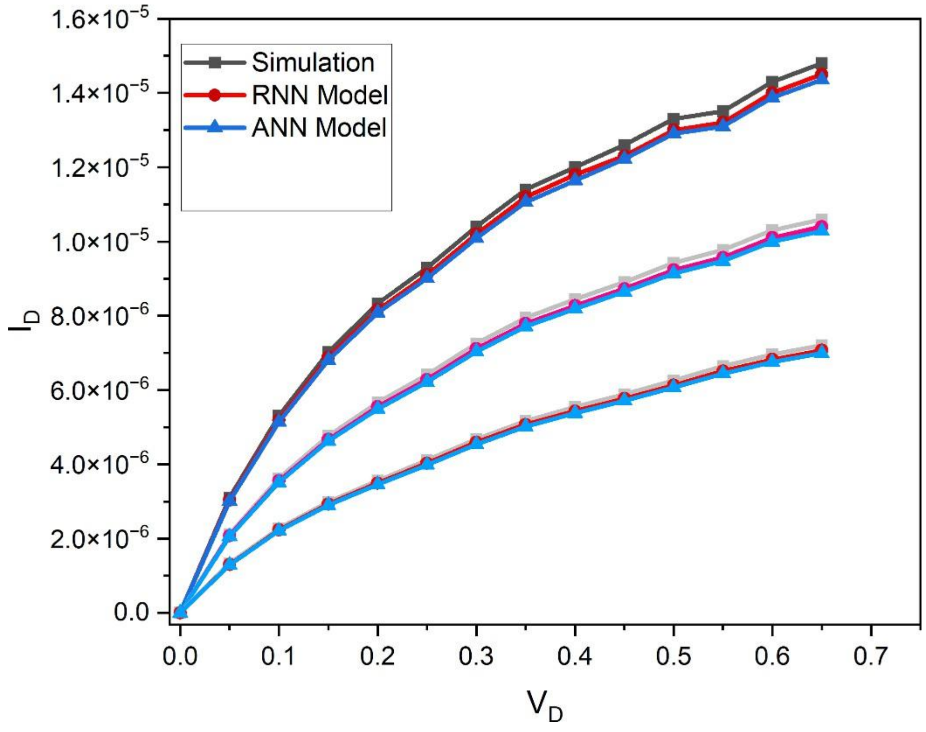

Fig 6.1: I_D vs V_D for Varying Channel Length

This graph 6.2 shows the fluctuation of the drain current I_D as a function of gate voltage V_G, using RNN and ANN models, with reference simulation data for comparative analysis. Both models accurately depict the exponential increase in current as V_G rises, demonstrating GaaFET characteristics. The RNN model is a bit more accurate than the simulation at higher gate voltages, showing that it works well for modeling complex device behavior. The close match of all curves validates the use of neural networks for accurate and rapid I–V prediction

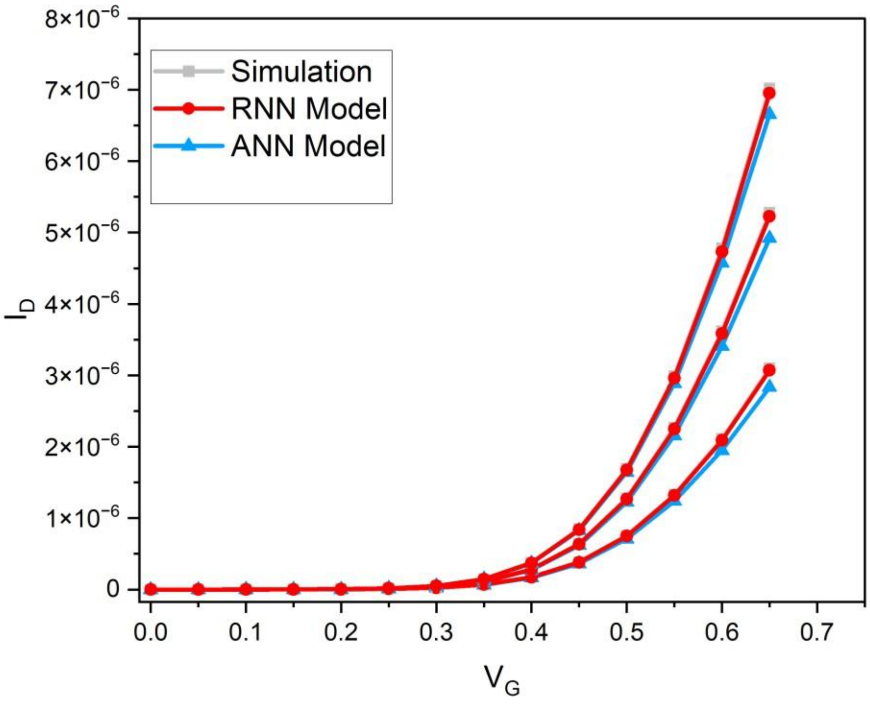

Fig 6.2: I_D vs V_G for Varying Channel Length

Simulations were carried out using the Nano Hub platform to study the influence of gate oxide thickness on the electrostatic control and overall performance of GAA-FETs. In this simulation, the gate oxide thickness was increased to 2 nm while all other device parameters were kept constant. This variation helps in understanding the trade-offs between gate control and leakage currents. The complete list of device parameters used in this configuration is presented in Table 6.2.

Table: 6.2 Device parameter

Parameter	**Variable**	**Value**
Gate length	Lg	12 nm
Silicon Body width	Wsi	5 nm
Gate work function	Wf	4.61 eV
Gate oxide thickness	Tox	2 nm
Channel Length	Lc	5 nm
Silicon Body Thickness	Tsi	5 nm

In Fig 6.3 I-V characteristic demonstrates the relationship between the drain current I_D and the drain voltage V_D in a GAAFET device. The simulation data was produced utilizing the Nano Hub Tool, and the expected outcomes were derived from trained ANN and RNN models. The oxide thickness Tox was adjusted to examine its effect on device performance. The plot compares how accurately both neural network models Show the simulation behavior. As observed, both ANN and RNN models follow the simulation trend closely with 98% and 99% accuracy, respectively, with RNN showing slightly better alignment. This confirms the effectiveness of machine learning models in predicting I– V behavior based on physical parameter variations.

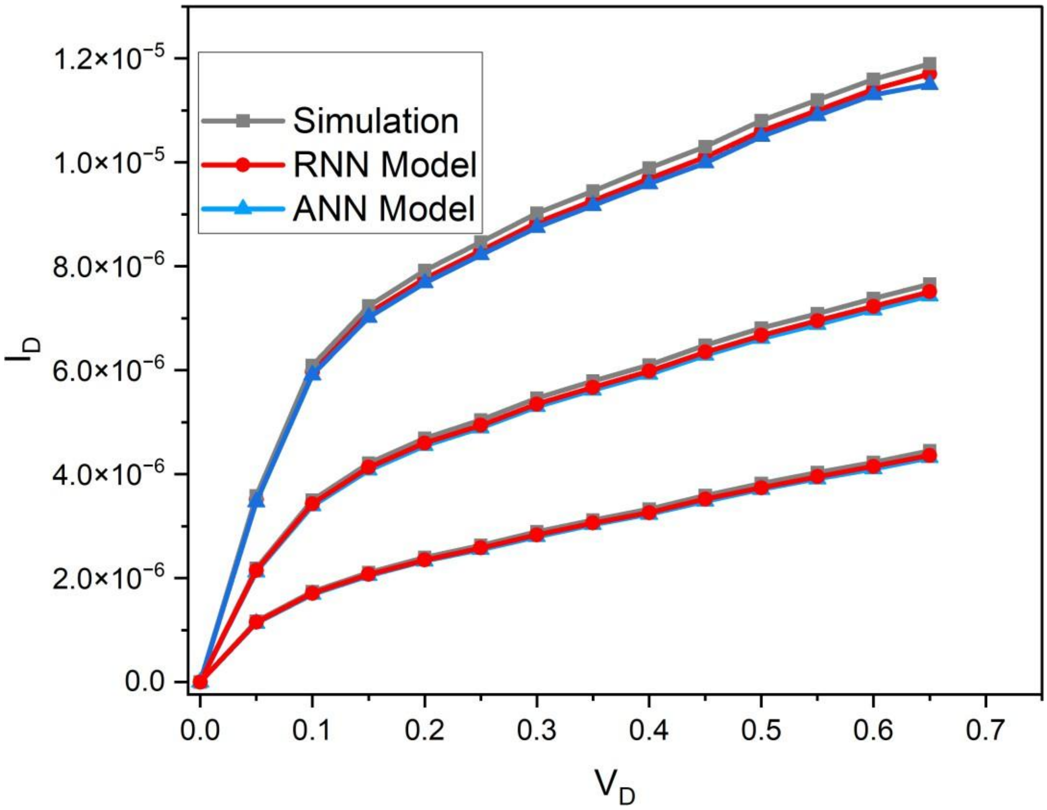

Fig 6.3: I_D vs V_D for varying Tox

In Fig 6.4 I-V characteristic demonstrates the relationship between the drain current I_D and the drain voltage V_G in a GAAFET device. The simulation data was produced utilizing the Nano Hub Tool, and the expected outcomes were derived from trained ANN and RNN models. The oxide thickness Tox was adjusted to examine its effect on device performance. The plot compares how accurately both neural network models Show the simulation behavior. As observed, both ANN and RNN models follow the simulation trend closely with 98% and 99% accuracy, respectively, with RNN showing slightly better alignment. This confirms the effectiveness of machine learning models in predicting I–V behavior based on physical parameter variations

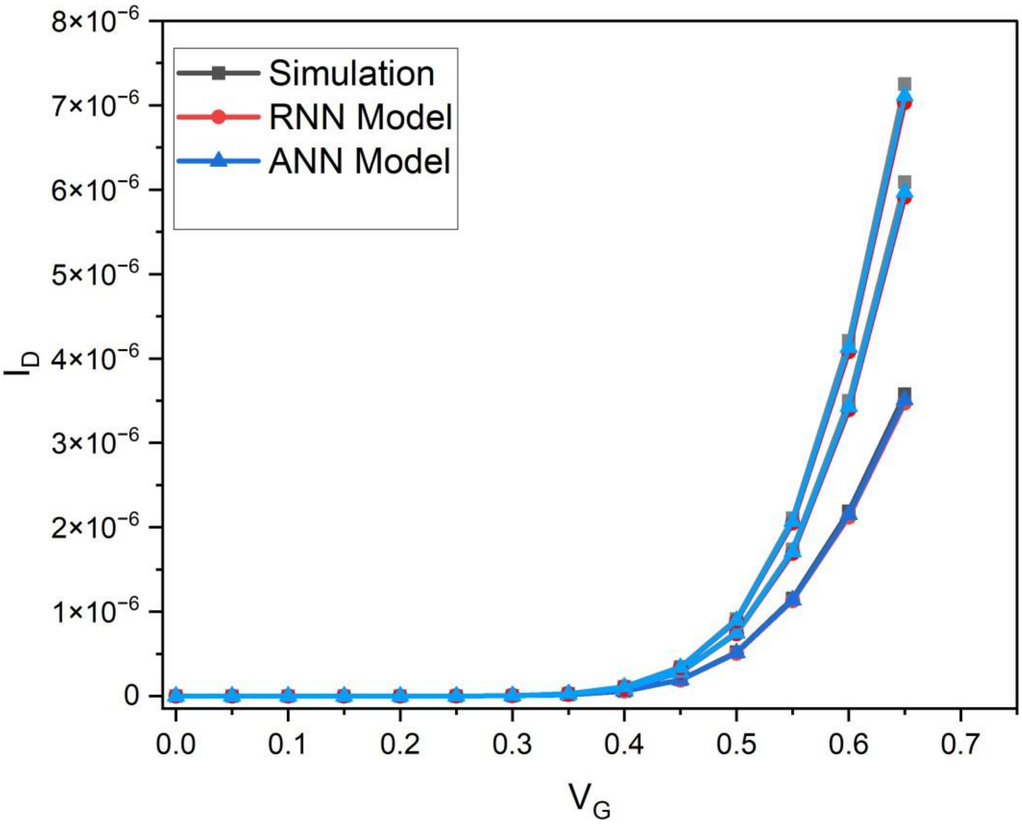

Fig 6.4: I_D vs V_G for varying Tox

Device Parameter:

This simulation investigated the impact of silicon body thickness on the electrical performance of a Gate-All-Around FET (GAA-FET) inside the Nano Hub simulation environment. A reduced silicon body thickness may enhance electrostatic gate control and alleviate short-channel effects. To achieve this goal, the silicon body thickness Tsi was set at 5 nm, while all other device parameters remained unchanged. The complete set of device configurations used for this simulation is shown in Table 6.3.

Table: 6.3 Device parameter

Parameter	**Variable**	**Value**
Gate length	Lg	12 nm
Silicon Body width	Wsi	5 nm
Gate work function	Wf	4.61 eV
Gate oxide thickness	Tox	1 nm
Channel Length	Lc	5 nm
Silicon Body Thickness	Tsi	5 nm

The I-V characteristic 6.5 demonstrates the relationship between the drain current I_D and the drain voltage V_D in a GAAFET device. The simulation data was produced utilizing the Nano Hub Tool, and the expected outcomes were derived from trained ANN and RNN models. The Silicon Body thickness (Tsi) was adjusted to examine its effect on device performance. The plot compares how accurately both neural network models Show the simulation behavior. As observed, both ANN and RNN models follow the simulation trend closely with 98% and 99% accuracy, respectively, with RNN showing slightly better alignment. This confirms the effectiveness of machine learning models in predicting I– V behavior based on physical parameter variations.

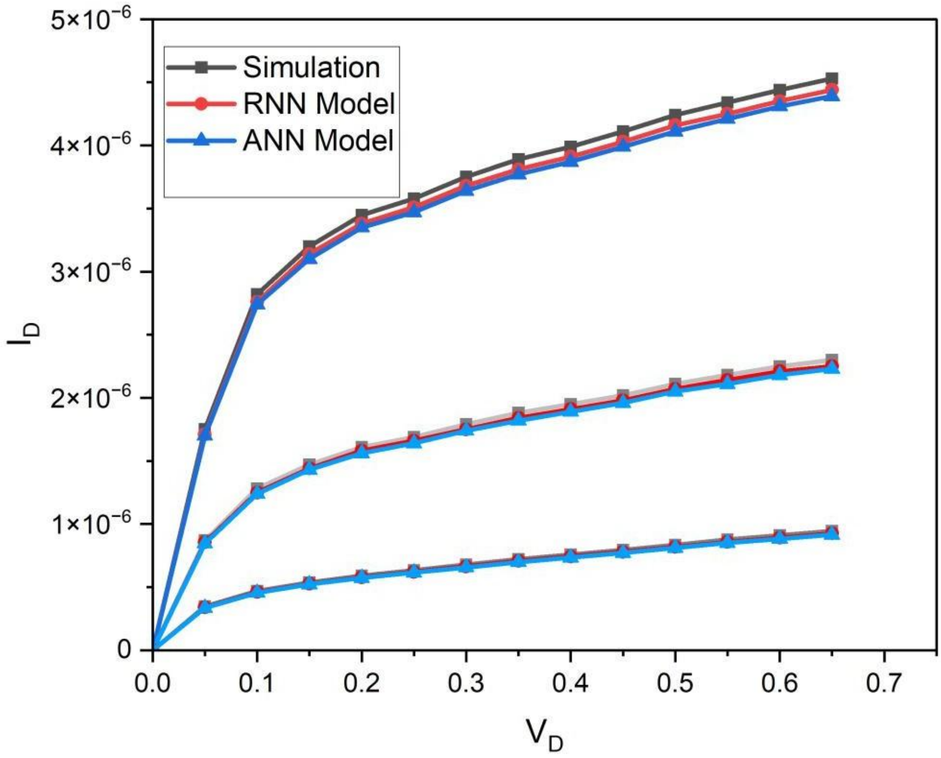

Fig 6.5: I_D vs V_D for varying Tsi

The I-V characteristic 6.6 demonstrates the relationship between the drain current I_D and the drain voltage V_G in a GAAFET device. The simulation data was produced utilizing the Nano Hub Tool, and the expected outcomes were derived from trained ANN and RNN models. The Silicon Body thickness (Tsi) was adjusted to examine its effect on device performance. The plot compares how accurately both neural network models Show the simulation behavior. As observed, both ANN and RNN models follow the simulation trend closely with 98% and 99% accuracy, respectively, with RNN showing slightly better alignment. This confirms the effectiveness of machine learning models in predicting I– V behavior based on physical parameter variations.

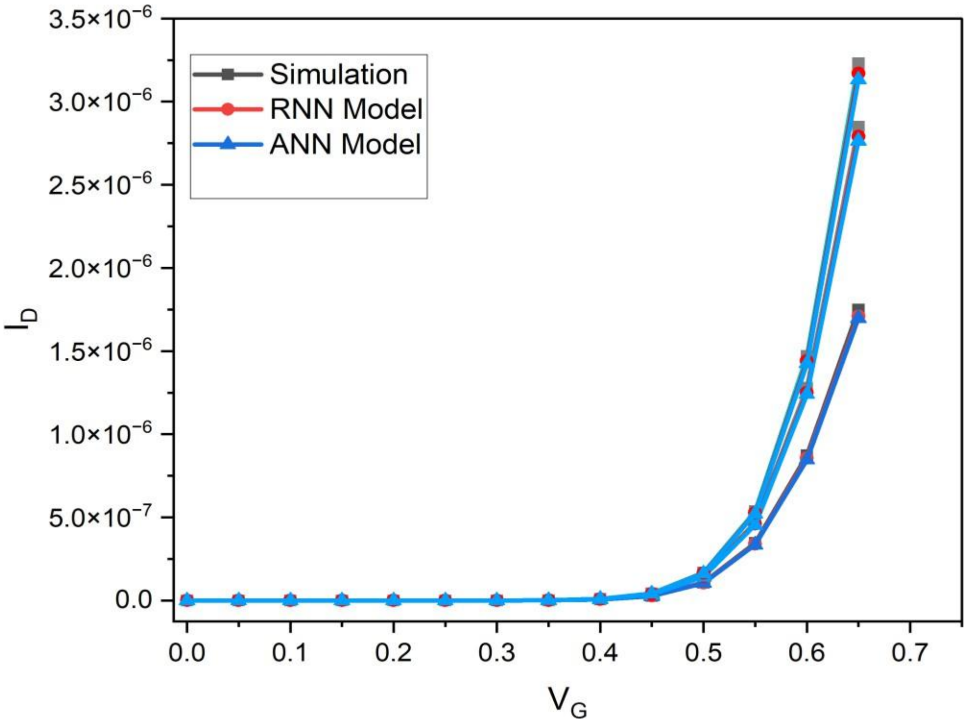

Fig 6.6: I_D vs V_G for varying Tsi

Device Parameter:

Simulations were conducted on the Nano Hub platform to evaluate the influence of silicon body thickness on the electrostatic control and performance of GAA-FETs. The silicon body thickness Tsi was established at 5 nm, with all other device parameters remaining constant. Minimized silicon designs are recognized for enhancing gate control and alleviating short-channel effects. The table 6.4 below delineates the device parameters used for this setup.

Table: 6.4 Device parameter

Parameter	**Variable**	**Value**
Gate length	Lg	12 nm
Silicon Body width	Wsi	5 nm
Gate work function	Wf	4.5 eV
Gate oxide thickness	Tox	1 nm
Channel Length	Lc	5 nm

Silicon Body Thickness	Tsi	5 nm

This figure 6.7 shows I_D vs. V_D at different bias conditions. The RNN and ANN models obtain 99% and 98% prediction accuracy, respectively. The findings indicate that both neural networks successfully capture the influence of Work function on device performance, with the RNN indicating slightly higher accuracy.

The I-V characteristic demonstrates the relationship between the drain current I_D and the drain voltage V_D in a GAAFET device. The simulation data was produced utilizing the Nano Hub Tool, and the expected outcomes were derived from trained ANN and RNN models. The Gate work function (wf) was adjusted to examine its effect on device performance. The plot compares how accurately both neural network models Show the simulation behavior. As observed, both ANN and RNN models follow the simulation trend closely with 98% and 99% accuracy, respectively, with RNN showing slightly better alignment. This confirms the effectiveness of machine learning models in predicting I– V behavior based on physical parameter variations.

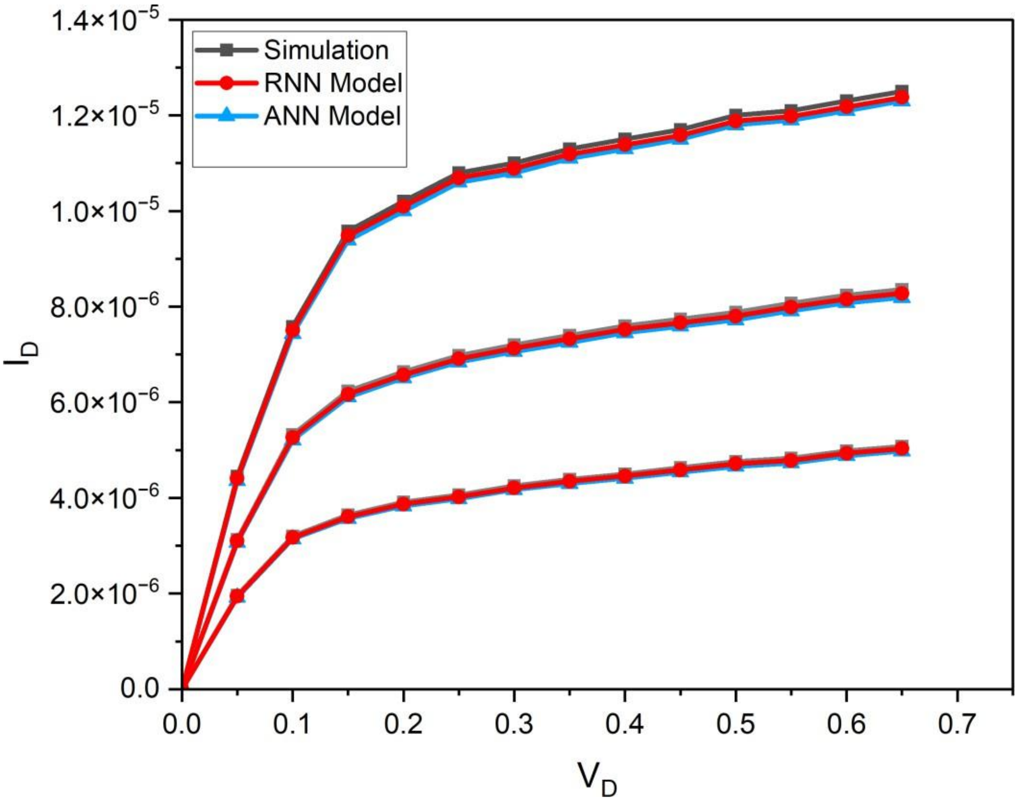

Fig 6.7: I_D vs V_G for Varying WF

The I-V characteristic in Fig 6.8 demonstrates the relationship between the drain current I_D and the drain voltage V_G in a GAAFET device. The simulation data was produced utilizing the Nano Hub Tool, and the expected outcomes were derived from trained ANN and RNN models. Gate work function (wf) was adjusted to examine its effect on device performance. The plot compares how accurately both neural network models Show the simulation behavior. As observed, both ANN and RNN models follow the simulation trend closely with 98% and 99% accuracy, respectively, with RNN showing slightly better alignment. This confirms the effectiveness of machine learning models in predicting I–V behavior based on physical parameter variations.

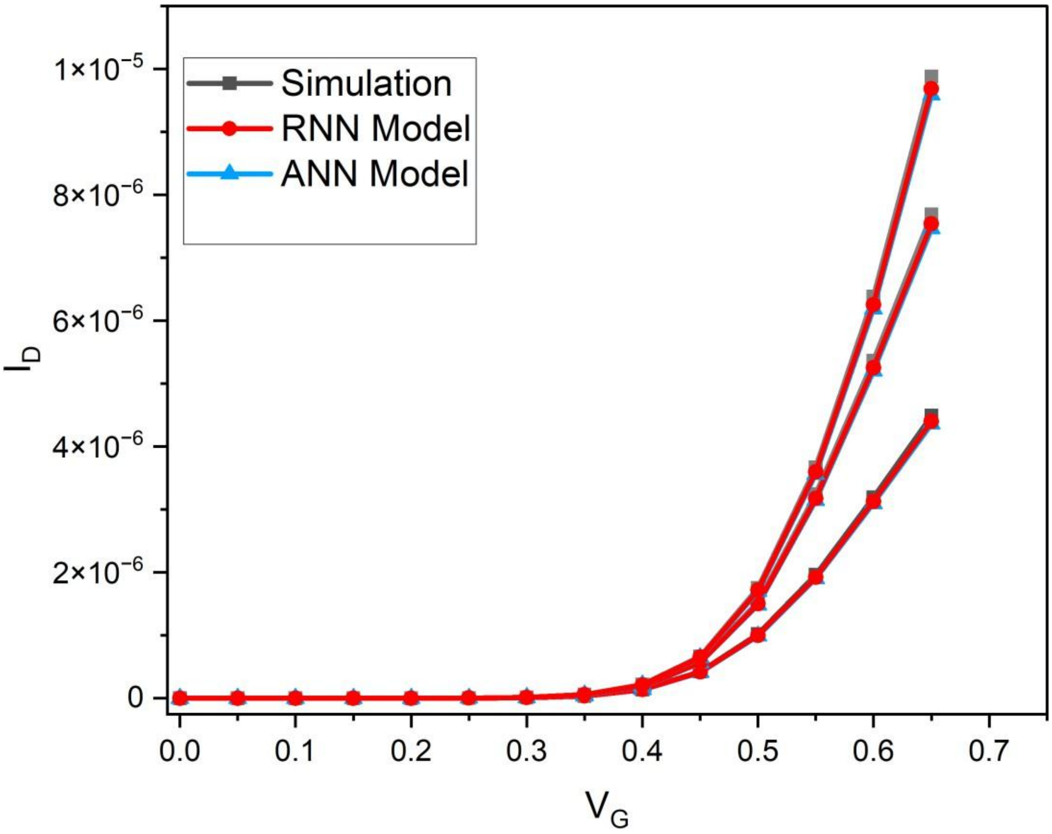

Fig 6.8: I_D vs V_G for Varying Work Function

Chapter 07

Conclusion and Future Scope

Conclusion:

This work successfully developed AI-driven models for describing devices and enhancing their performance using modeling data from Nano Hub. The RNN and ANN models demonstrated the capability to produce precise predictions by effectively replicating the intricate nonlinear interactions among input and output variables, such as gate voltage (V_G), drain voltage (V_D), and drain current (I_D). The AI models surpassed the traditional physics-based models due to their superior accuracy, reduced prediction errors, and immediate visibility into device performance. AI accelerated and reduced operational costs while enhancing the process of constructing and improving devices.

When compared to traditional modeling techniques, the use of Artificial Intelligence (AI) into device modeling has shown to be a game-changing strategy, providing previously unheard-of levels of accuracy, speed, and flexibility. AI makes it easier to predict intricate, nonlinear interactions between device parameters by utilizing data-driven algorithms. This makes optimization and performance predictions more effective. Furthermore, high reality and physical understanding are the best of both worlds when AI is combined with physics-based models.

This study has shown how AI may be used to solve important device modeling problems including behavior analysis in novel settings, defect prediction, and parameter estimation. Deep learning approaches have demonstrated potential in reducing computing overhead while preserving excellent accuracy. The findings highlight the significance of AI as a fundamental technique for existing device design and analysis, as well as an additional tool.

With the progress, there are still issues, such the necessity for strong generalization across various device kinds and situations, model explainability, and huge, high-quality datasets. For AI-driven methods to be widely adopted in both academia and industry, these issues must be resolved.

Future Scope

7.1 Enhanced Data Availability and Quality:

Development of open-access, high-quality datasets tailored for AI-based device modeling. Leveraging synthetic data generation techniques to address data scarcity.

7.2 Sustainability:

Use AI to design energy-efficient devices, contributing to sustainability goals in electronics and other industries. Reduce material waste and energy consumption in device manufacturing.

7.3 Regulatory and Ethical Considerations:

Address ethical issues, such as data privacy, bias in AI models, and their implications in device development and deployment. Work with regulatory bodies to standardize AI applications in device modelling.

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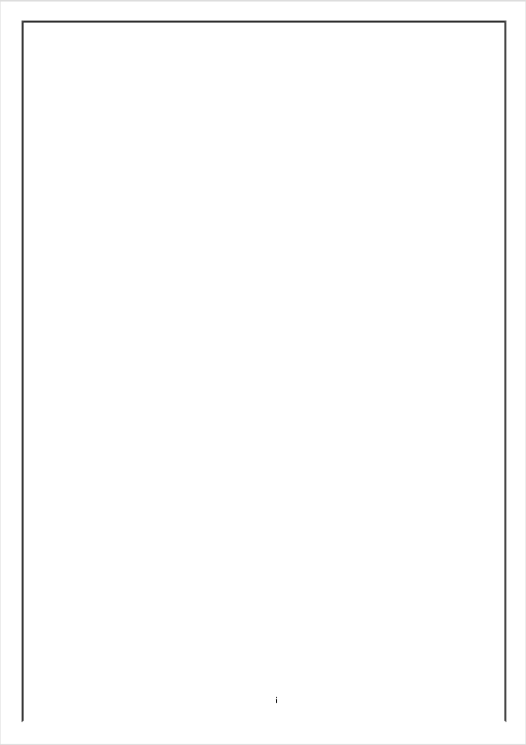

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