"Design of CMOS Current Conveyors for Analog VLSI"

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DECLARATION

I hereby declare that the thesis report entitled **"Design of CMOS Current Conveyors for Analog VLSI"** is an authentic record of my own work carried out as requirement for the award of **Master of Technology in VLSI Design & CAD at Thapar University, Patiala** under the guidance of Mr. Rishikesh Pandey, Assistant Professor, ECED.

The matter embedded in this thesis has not been submitted in any other University/Institute for the award of any degree.

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It is certified that the above statement made by candidate is correct to the best of my knowledge and belief.

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ABSTRACT

Current conveyor is a high performance analog circuit design block based on current mode approach. It is basically a unity gain element that exhibits high linearity, wide dynamic range, high bandwidth and better high frequency performance. The current conveyor is a combination of voltage as well as current follower.

The second and third generation current conveyors, based on translinear loop, having voltage and current gain closer to unity are presented in this thesis. The main feature of these current conveyors is their high voltage and current transfer bandwidth which make them suitable for high frequency applications.

The current conveyors are simulated using UMC 0.35μm CMOS 1P6M process parameters with power supply of ±1.5V in Cadence® Virtuoso Analog Design Environment. Layouts of the circuits have been designed in Cadence® Virtuoso XL Design Environment. The post-layout simulations at different process corners along with temperature and supply variations have been presented to validate the performance of these current conveyors.

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LIST OF SYMBOLS

C_{gs}	Gate to source capacitance
C_{gd}	Gate to drain capacitance
C_{db}	Drain to substrate capacitance
C_m	Miller capacitance
C_n	Node capacitance
g_{mi}	Transconductance of MOSFET
i_o	Output current
i_{in}	Input current
v_o	Output voltage
v_{in}	Input voltage
z_o	Output impedance
z_{in}	Input impedance
r_o	Output resistance
ω_p	Pole frequency
ω_{in}	Input pole frequency
ω_o	Output pole frequency
R_s	Source resistance
C_{in}	Input capacitance
J_i	Strength of current source
$S_{V_{DD}}^{i_0}$	Supply voltage sensitivity
V_{DD}	Positive supply voltage
V_{SS}	Negative supply voltage
I_D	Drain current
K_p	PMOS process trans-conductance parameter

K_n	NMOS process trans-conductance parameter
W	Channel Width
L	Channel length
μ_n	Mobility of electrons
μ_p	Mobility of holes
C_{OX}	Oxide capacitance
I_o	Bias current
V_T	Threshold voltage
V_{GS}	Gate to source voltage
V_{DS}	Drain to source voltage
I_{REF}	Reference current
R_{in}	Input resistance
λ	Channel length modulation parameter

ABBREVIATIONS

CMC	Current Mode Circuits
VMC	Voltage Mode Circuits
Opamp	Operational Amplifier
CMOS	Complementary Metal Oxide Semiconductor
CCI	First Generation Current Conveyor
CCII	Second Generation Current Conveyor
CCIII	Third Generation Current Conveyor
ESD	Electrostatic Discharge
MOS	Metal Oxide Semiconductor
MOSFET	Metal Oxide Semiconductor Field Effect Transistor
PTAT	Proportional to Absolute Temperature
NMOS	N-channel Metal Oxide Semiconductor
PMOS	P-channel Metal Oxide Semiconductor
RF	Radio Frequency
CAD	Computer Aided Design
UMC	United Microelectronics Corporation
BJT	Bipolar Junction Transistor
CM	Current Mirror
SS	Slow NMOS Slow PMOS
TT	Typical NMOS Typical PMOS
FF	Fast NMOS Fast PMOS
SF	Slow NMOS Fast PMOS
FS	Fast NMOS Slow PMOS

CHAPTER 1

INTRODUCTION

1.1 INTRODUCTION

With the reduction in the supply voltage and device threshold voltage of CMOS technology, the performance of CMOS voltage-mode circuits has greatly affected which results in a reduced dynamic range, an increased propagation delay and reduced low noise margins. The influence of supply voltage reduction on the performance of current-mode circuits, however, is less severe as compared with that of voltage-mode circuits. This is because the design emphasis of current-mode circuits is on branch currents rather than nodal voltages. The usefulness of CMOS current-mode circuits in overcoming the difficulties arising from the reduction of the supply voltage and the increase in the operation speed has received an increasing attention from the industry [1].

Current Conveyors represent the emerging class of high performance analog circuit design based on current-mode approach. They have simple structure, wide bandwidth and capability to operate at low voltages. Current conveyors are unity gain active elements exhibiting higher linearity, wider dynamic range and better high frequency performance.

1.2 MOTIVATION FOR CURRENT-MODE DESIGN

The current-mode design technique is a good alternative for the high performance analog circuit design as it offers voltage independent high bandwidth. In current-mode design, the stress is more on the current levels for the operation of the circuits and the voltage levels at various nodes are immaterial. In voltage-mode circuits (VMCs), such as operational amplifiers (op amp), the performance of the circuit is determined in terms of voltage levels at various nodes including the input and the output nodes. But all these circuits suffer from the following disadvantages:

- Output voltage cannot change instantly when there is a sudden change in the input voltage due to stray and other circuit capacitances.
- Bandwidth of the op amp based circuits is usually low because of finite unity gain bandwidth.
- Slew rate is dependent on the time constants associated with the circuit.
- Circuits do not have high voltage swings.
- Require higher supply voltages for better signal-to-noise ratio.

Therefore, VMCs are not suitable for high frequency applications.

When signals are widely distributed as voltages, the parasitic capacitances are charged and discharged with the full voltage swing, which limits the speed and increases the power consumption of voltage-mode circuits. Current-mode circuits cannot avoid nodes with high voltage swing either but these are usually local nodes with less parasitic capacitances [2]. Therefore, it is possible to achieve higher speed and lower dynamic power consumption with current-mode circuit techniques.

When the signal is conveyed as a current, the voltages in MOS transistor circuits are proportional to the square root of the signal, if the devices are assumed to be operating in saturation region. Therefore, a compression of voltage signal swing and a reduction of supply voltage are possible. This feature is utilized in log domain filters, switched current filters and in non-linear current-mode circuits [3]. However, as a result of the device mismatches, this non-linear operation may generate an excessive amount of distortion and cannot be used for the applications where high linearity is required. Thus, linearization techniques are utilized in current-mode circuits to reduce the nonlinearity of the transistor transconductance and in this case the voltage signal swing is also not reduced.

1.3 ORGANIZATION OF THE THESIS

This thesis is organized as follows:

CHAPTER 1: This chapter gives an overview of current mode approach.

CHAPTER 2: The comparative study of current-mode and voltage-mode circuits with respect to input and output impedance, bandwidth, slew rate, propagation delay, power supply rejection ratio etc is discussed in this chapter. It also explains all the three generations of current conveyors with their applications.

CHAPTER 3: This chapter discusses the mathematical analysis and design considerations of the second and third generation current conveyors.

CHAPTER 4: In this chapter, the simulations results of second and third generation current conveyors have been discussed.

CHAPTER 5: The layout and RC extracted view of the current conveyors have been presented in this chapter and this chapter also discusses the post-layout simulation results of the current conveyors.

CHAPTER 6: A brief conclusion and possible improvements have been discussed in this chapter.

CHAPTER 2

CURRENT CONVEYORS

2.1 INTRODUCTION

This chapter gives the basic description of current conveyors and its applications. In section 2.2, the ideal current-mode and voltage-mode circuits have been discussed. Section 2.3 explains the comparative study of the voltage-mode and current-mode circuits on the basis of input and output impedance, bandwidth, propagation delay etc. Section 2.4 gives the detail analysis of current conveyors and its all generations with applications.

2.2 IDEAL CURRENT-MODE CIRCUITS

An ideal voltage-mode circuit has infinite input impedance, zero output impedance and a constant voltage gain. The best example of voltage mode circuit is an ideal operational amplifier. The infinite input impedance and a zero output impedance of operational amplifiers enable an easy cascade without loading effect and also ensure that the characteristics of these circuits are determined by the external elements [1].

Unlike ideal voltage-mode circuits, an ideal current-mode circuit has the characteristics of zero input impedance, infinite output impedance and a constant current gain. The current amplification will result in a high level of static power consumption, therefore, the current gain of ideal current-mode circuits is set to unity. This constant current gain up to large frequency range enables current-mode circuits to be used for high frequency applications. On the contrary, the gain of voltage-mode circuits falls at high frequencies [2].

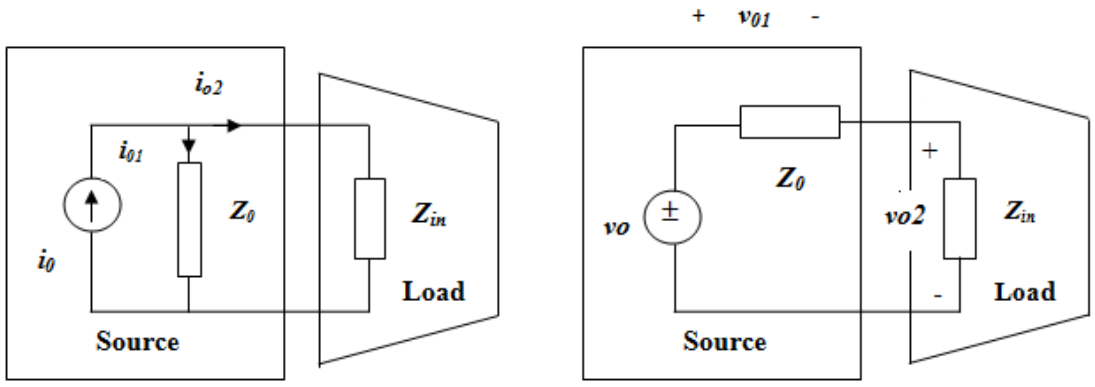
2.3 CHARACTERISTICS OF CURRENT-MODE CIRCUITS

In this section, the comparison between voltage-mode and current-mode circuit with respect to input/output impedance, bandwidth, propagation delay, slew rate, power supply sensitivity and electrostatic discharge has been discussed.

2.3.1 INPUT AND OUTPUT IMPEDANCES

A voltage-mode circuit is characterized by large input impedance and low output impedance. On the other hand, a current-mode circuit is characterized by low input impedance and high output impedance. The loading effect resulting from the finite output impedance of current-mode circuits can be studied using figure 2.1(a). In this circuit, the input source is represented by its Norton equivalent and load current is given by eq. (2.1)

$$i_{02} = \frac{1}{1+\frac{z_{in}}{z_o}} i_0 \approx \left(1 - \frac{z_{in}}{z_0}\right) i_0 \tag{2.1}$$



(a) (b)

Figure 2.1 Loading effect in current-mode and voltage-mode circuits [1].

where z_o and z_{in} are the output and input impedance of the driving and driven stage respectively. In order to simply eq. (2.1) and to minimize the loading effect, $z_{in} << z_o$ is required for current-mode circuits. Similarly when the input is represented by its Thevenin equivalent, the loading effect of voltage-mode circuits can be studied using figure 2.1(b) and the load voltage is given by eq. (2.2)

$$v_{02} = \frac{1}{1+\frac{z_o}{z_{in}}} \approx (1 - \frac{z_0}{z_{in}}) v_0 \tag{2.2}$$

To minimize the loading effect, $z_{in} >> z_o$ is required for voltage-mode circuits [1].

2.3.2 BANDWIDTH

The comparison of the bandwidth of voltage and current-mode circuits can be done by using their basic building blocks as shown in figure 2.2. Because a current-mode circuit has large output impedance and small input impedance, therefore the condition for load

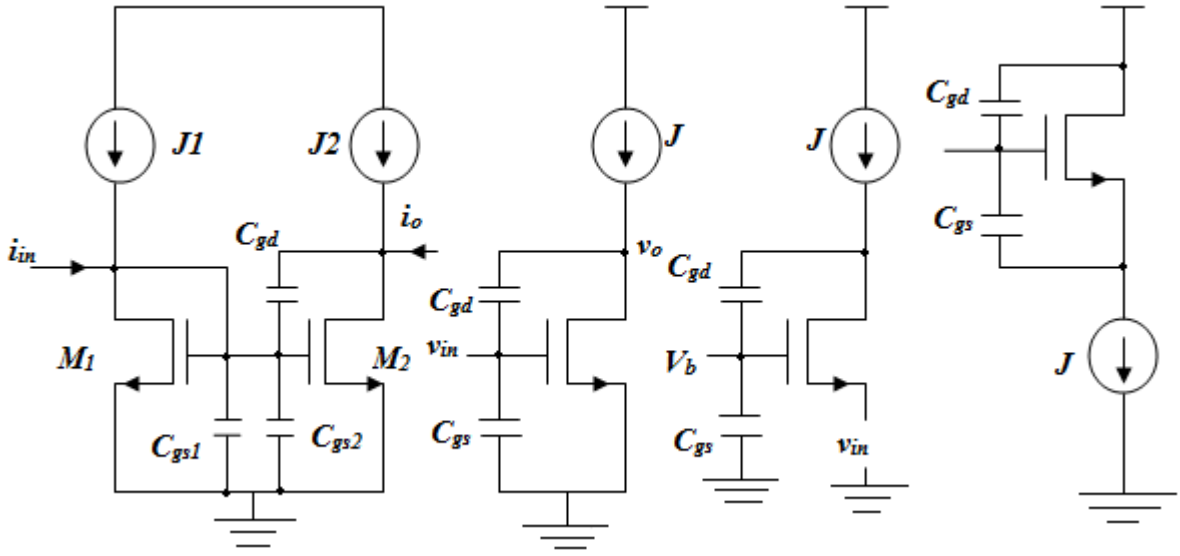
impedance $z_l \approx 0$ holds. As a result of this, transistor M_2 of the basic current mirror of figure 2.2 (a) is not subject to Miller effect. The only pole of this configuration is at the gate of $M_{1\sim2}$ with the pole frequency given by eq. (2.3)

$$\omega_p \approx \frac{g_{m\,1}}{C_{gs1} + C_{gs2} + C_{gd2}} \tag{2.3}$$

On the other hand, due to the presence of the gate-drain capacitor C_{gd}, the common-source configuration of figure 2.2 (b) is subject to Miller effect with Miller capacitances $C_{m1} = C_{gd}(1+ g_m r_o)$ at the gate and $C_{m2} = C_{gd}(1+ 1/g_m r_o)$ at the drain terminal, where g_m and r_o are the transconductance and output impedance of the transistor respectively. The pole at the input is called "Miller pole" and is given by eq. (2.4)

$$\omega_{in} = \frac{1}{R_s(C_{gs} + C_{gd}(1 + g_m r_0))} \tag{2.4}$$

where *Rs* is the resistance of the source.



(a) (b) (c) (d)

Figure 2.2 Bandwidth comparison of current-mode and voltage-mode circuits, (a) Basic Current mirror, (b) Common-source amplifier, (c) Common-gate amplifier, (d) Source follower [1].

The output pole of common-source amplifier is calculated from eq. (2.5)

$$\omega_o = \frac{1}{r_0(C_{gd} + C_{in})} \tag{2.5}$$

where C_{in} is the input capacitance of the load stage.

The common-gate configuration of figure 2.2(c) is not subject to Miller effect due to the absence of floating capacitors. Therefore, the pole at the input is given by eq. (2.6)

$$\omega_{in} \approx \frac{1}{R_s C_{gs}} \tag{2.6}$$

and the pole at the output of this configuration is calculated from eq. (2.7)

$$\omega_0 \approx \frac{1}{r_0(C_{gd} + C_{in})} \tag{2.7}$$

The source follower shown in figure 2.2 (d) is also free of Miller effect because its small signal voltage gain is approximately unity. The Miller capacitances at the gate and source terminals are given by $C_{m1} \approx C_{m2} \approx 0$. Therefore, pole at the input is given by eq. (2.8)

$$\omega_{in} \approx \frac{1}{R_s C_{gd}} \tag{2.8}$$

and the dominant pole at the output is calculated from eq. (2.9)

$$\omega_0 \approx \frac{1}{r_0 C_{in}} \tag{2.9}$$

For practical applications, C_{in} and r_o are usually large and the dominant pole of the common-source, common-gate and source follower amplifiers is at the output node. The pole frequency of the basic current mirror is therefore smaller as compared with the pole frequency of the basic voltage-mode amplifiers [1].

2.3.3 PROPAGATION DELAY

For digital circuits, the average propagation delay is used as a figure-of-merit in depicting the transient behavior of the circuits. It is directly related to the swing of the signal [1]. If both the resistance and inductance are neglected, then the average rising (falling) time, denoted by Δt, of the voltage of a node is determined from eq. (2.10)

$$C_n(\Delta v_n) = \int_0^{\Delta t} i(t)dt = I_{avg}\Delta t \tag{2.10}$$

where I_{avg} is the average current charging or discharging the node, C_n is the node capacitance, $i(t)$ is the net current flowing into or out of the node and Δv_n is the voltage swing of the node. It can be seen from eq. (2.10) that a small propagation delay can be achieved by:

- Minimizing the voltage swing of the node.
- Maximizing the current charging and discharging the capacitance of the node.

For voltage mode circuits, Δv_n is constrained by the signal to noise ratio requirements and must be kept sufficiently large which results in a slow transient response.

Unlike voltage-mode circuits, the information carriers of current-mode circuits are branch currents. The variation of nodal voltages can be kept small as long as the current of the branches associated with the nodes is large. Consider the figure 2.3, from this it is found that

$$\Delta v_n = z_n \left(\sum_{b_1=1}^{B_1} \Delta i_n b_1 - \sum_{b_2=1}^{B_2} \Delta i_{0,b_2} \right) \tag{2.11}$$

where z_n is the impedance of the node and B_1 and B_2 are the number of input and output branches connected to the node respectively. From this it is clear that for a given Δv_n, a large current variation can be obtained as long as z_n is kept small. The small nodal voltage variation of current-mode circuits lowers the amount of time needed to charge/discharge the capacitance (C_n) and thus resulting in a faster transient response. This is one of the major advantages of current mode circuits [1].

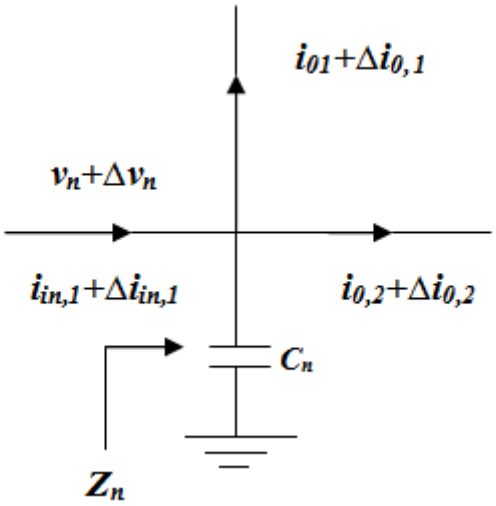


Figure 2.3 Variation of nodal voltages and branch currents of current-mode circuits.

2.3.4 SLEW RATE

The comparison of the slew rate of voltage and current-mode circuits can be done by using the basic building blocks shown in figure 2.4. When a pulse of current is applied to the basic current mirror, the transistor M_1 is in saturation region and i_{DS1} is independent of

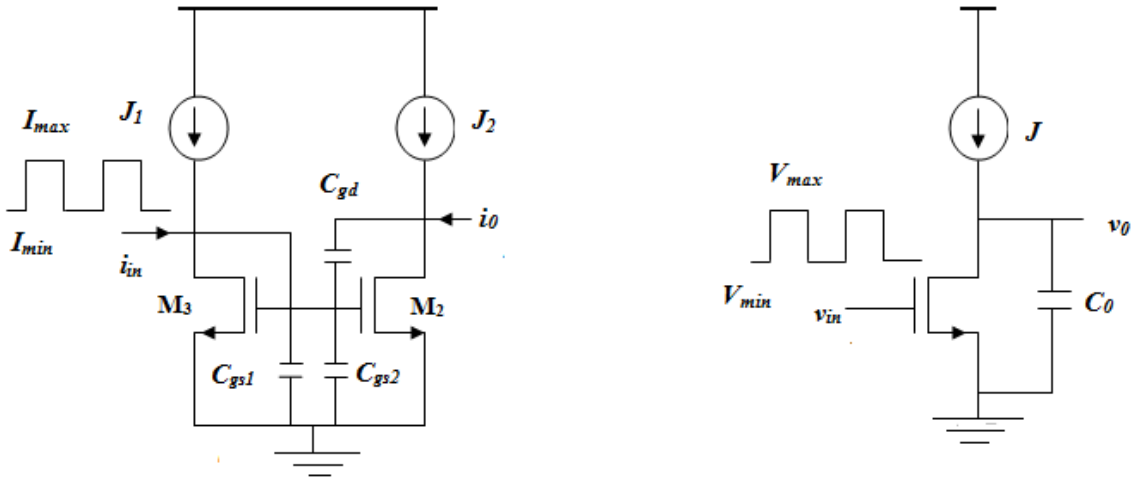
v_{DS1} (neglecting the channel length modulation). The rate of change of the output current depends upon how fast the capacitance, $C_{gs1\sim2} = C_{gs1} + C_{gs2}$ is charged or equivalently how fast the gate voltage of $M_{1\sim2}$ rises. Because

$$\frac{dv_{GS1\sim2}}{dt} + \frac{1}{2}\mu_n C_{ox}\frac{W}{L}(V_{GS1} - V_T) = J_1 + i_{in} \tag{2.12}$$

therefore, $v_{GS1\sim2}$ increases with i_{in}. For fixed biasing currents, larger is the amplitude of the input higher is the slew rate of the output current.

For voltage mode circuits, the slew rate is usually determined by the output stage because of the large width of transistors in the output stage and the large load capacitance. Consider the common-source amplifier shown in figure 2.4 (b), when a sufficiently low voltage V_{min} is applied to the input, the transistor switches off and C_0 is charged by J only then we have

$$\left[\frac{dv_0}{dt}\right]_{rise,max} = \frac{J}{C_o} \tag{2.13}$$



(a) (b)

Figure 2.4 Slew rate comparison of current-mode and voltage-mode circuits, (a) Basic current mirror, (b) Common-source amplifier.

When $V_{in} = V_{max}$, C_o is discharged through transistor with the slew rate given by eq. (2.14)

$$\left[\frac{dv_0}{dt}\right]_{fall,max} = \frac{1}{R_{on}C_o} \tag{2.14}$$

where R_{on} is the channel resistance of the transistor in the triode region. The above results reveal that the slew rate of common-source amplifier is set by the biasing current, the

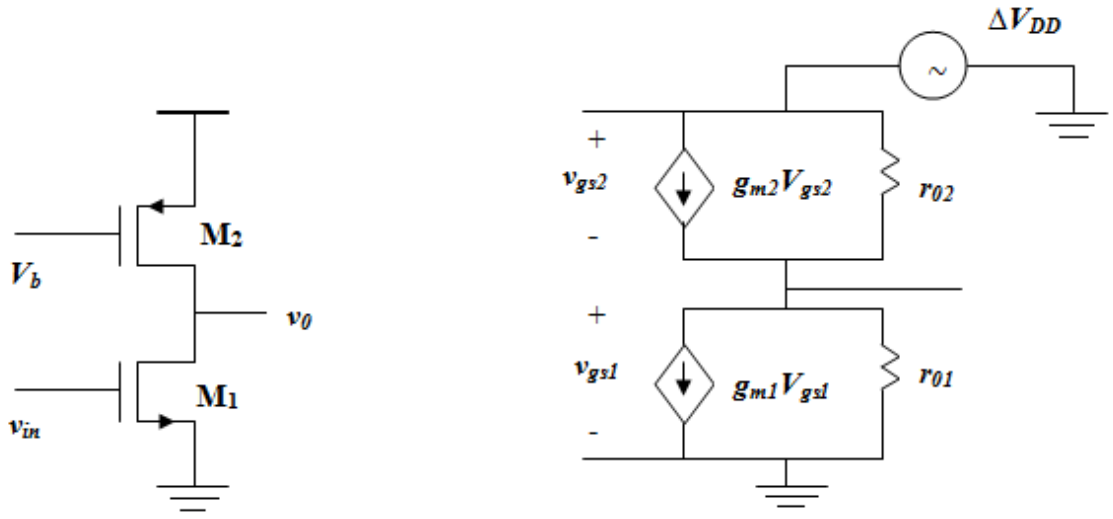
width of the transistor and the output capacitance. It is independent of the amplitude of the input voltage.

2.3.5 SUPPLY VOLTAGE SENSITIVITY

The effect of V_{DD} and ground fluctuations on the output voltage or current of CMOS circuits is of a great concern in mixed-mode circuits because both analog and digital circuits often share the same supply voltage and ground. Supply voltage sensitivity, defined as

$$S_{V_{DD}}^{v_o} = \frac{\partial v_0}{\partial V_{DD}} \tag{2.15}$$

is a measure of the effect of the variation of the supply voltage on the response of the circuits. Assuming that there is a change in supply voltage from V_{DD} to $V_{DD} + \Delta V_{DD}$ and ΔV_{DD} is a random variable with zero mean. For all the practical circuits, the condition $\Delta V_{DD} << V_{DD}$ holds and the small signal analysis can be used to analyze the effect of ΔV_{DD} on the response of the circuits.



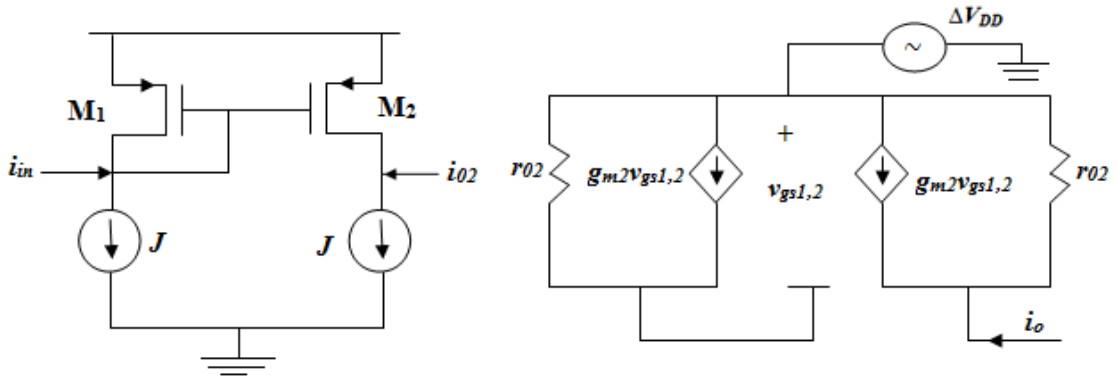
(a) (b)

Figure 2.5 Supply voltage sensitivity analysis of voltage-mode circuits, (a) Common source amplifier, (b) Small-signal equivalent circuit [1].

Consider the common-source amplifier shown in figure 2.5(a). Here transistor M_2 is biased in the saturation region and thus behaves as a current source. The small signal equivalent circuit of this amplifier for supply voltage sensitivity analysis is shown in figure 2.5(b). At low frequencies the capacitances, C_{gs} and C_{gd} are neglected and we have

$$S_{V_{DD}}^{v_o} = \frac{g_{m2}}{g_{01} + g_{02}} = (r_{01} || r_{02}) \tag{2.16}$$

The above result shows that ΔV_{DD} is directly amplified with a large voltage gain.



(a) (b)

Figure 2.6 Supply voltage sensitivity analysis of current-mode circuits, (a) Current mirror amplifier, (b) Small-signal equivalent circuit [1].

Now consider the circuit shown in figure 2.6 (a). Here, the load is a current mirror with the source current provided by an ideal current source *J*. Using a small-signal analysis, it can be shown that

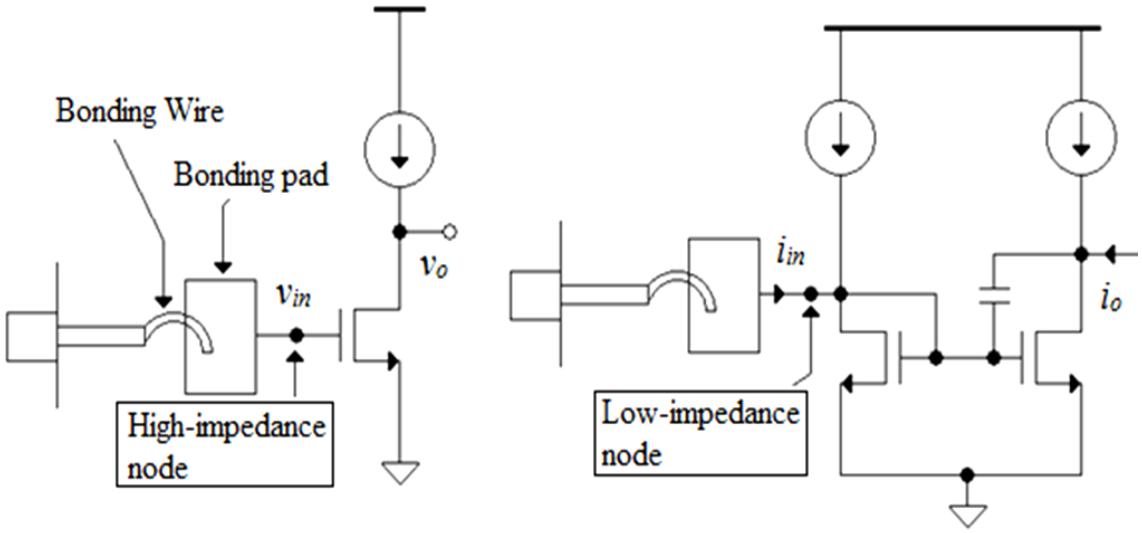
$$S_{V_{DD}}^{i_o} = g_{02} \tag{2.17}$$

As compared with eq. (2.16), because $g_o << g_m$ the current-mode circuit is less sensitive to the fluctuation of the supply voltage. Also, the effect of ΔV_{DD} on v_o is mainly due to the finite output impedance r_{o2} of the load current mirror [1]. Thus voltage-mode circuits are more sensitive to supply voltage variations

2.3.6 ELECTROSTATIC DISCHARGE

The oxide thickness t_{ox} is scaled down aggressively in deep submicron CMOS processes. This results in large number of ESD (electrostatic discharge) induced damages of MOSFETs mainly due to the breakdown of the gate oxide insulator. Voltage-mode circuits are particularly more vulnerable to ESD strikes as the input of these circuits is usually the gate of MOSFETs, which is a high impedance node [1]. No low impedance paths from the input pads to the ground exist to discharge electrostatic charge accumulated at the pads, as shown in figure 2.7(a). On the other hand, the low impedance

characteristics of the input pads of current-mode circuits prevent the accumulation of static charge at the pads, as shown in figure 2.7(b).



(a) (b)

Figure 2.7 ESD sensitivity (a) Voltage-mode circuits (b) Current-mode circuits [1].

2.4 CMOS CURRENT CONVEYORS

The current conveyor is a basic building block that can be implemented in analog circuit design. This was introduced by Sedra and Smith in 1968 but its real advantages and innovative impact was not clear at that time [4]. In recent years, current-mode circuits have emerged as an important class of circuits with properties of accuracy, high frequency range and versatility in a wide range of applications. Current conveyor represents the emerging class of high performance analog circuit design based on current mode approach. It has simple architecture, wider bandwidth and capability to operate at low voltage.

Current conveyors can be used in variety of applications ranging from multifunction and universal filters [5], oscillators and immittance design to integrators and differentiators. Unlike operational amplifier, current conveyors do not have a low frequency dominant pole and their utilizable frequency range is much higher.

The current conveyors can be classified into three generations:

- First Generation Current conveyor, CCI.
- Second Generation Current conveyor, CCII.
- Third Generation Current conveyor, CCIII.

All the three generations have similar structures but their characteristics are different. Figure 2.8 shows the black box representation of the current conveyor and it consists of three ports X, Y and Z.

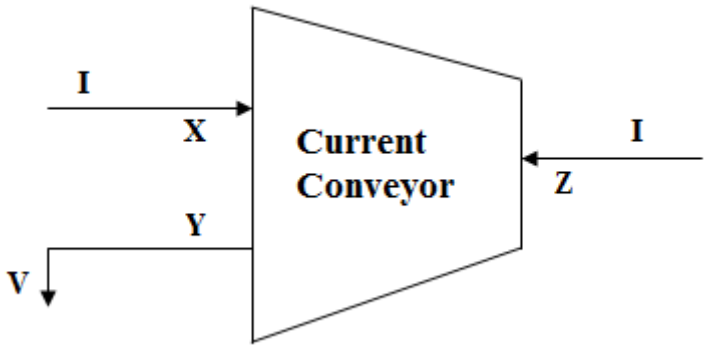


Figure 2.8 Representation of Current Conveyor [2].

- Port X is a hybrid port and functions as input port for current signals and output port for voltage signals at the same time.
- Port Y is a voltage input port.
- Port Z is a current output port, which can either sink or source current equal to the current injected into port X.

When a voltage source is applied to port Y, then the same potential will appear on the port X and if a current is forced through port X, an equal current will flow through port Y (depending upon the nature of the CC). The same current is also conveyed to output port Z, which is at a high impedance level.

In other words, current conveyor ensures two functionality between its ports:

- Voltage following action between ports Y and X.
- Current following action between ports X and Z.

In order to get ideal characteristics, the resistance at port X of current conveyor should be designed as small as possible since the port X is a current input and voltage output port. Similarly, the output resistance at port Z should be designed as high as possible since it is a current input port [6]. In addition to this, the voltage and current following action should be performed as accurate as possible over a wide range of frequency. Current mirrors play an important role in mirroring of current from port X to port Z, so these should be designed accurately in order to ensure proper mirroring with minimum offset.

2.4.1 FIRST GENERATION CURRENT CONVEYOR (CCI)

The first ideal current mode circuits were first generation current conveyors introduced by Sedra and Smith in 1968. These are denoted by CCI±, where polarity specify the direction of the output current is same as that of current flowing into port X or not. It is basically a three terminal device as shown in figure 2.9.

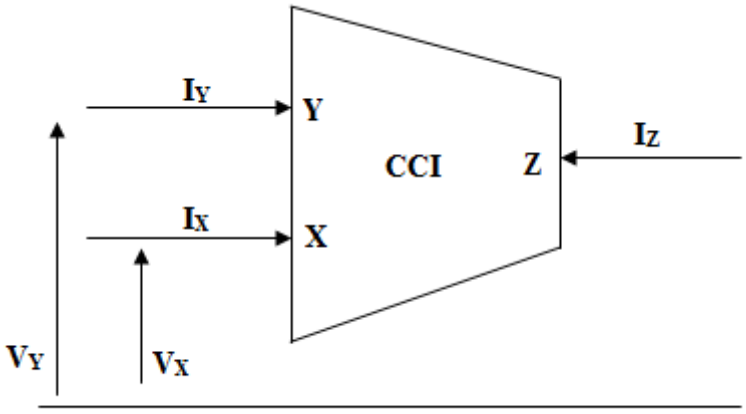


Figure 2.9 Block representation of CCI [2].

The relation between the terminal voltages and current of CCI can be given by the following matrix relation,

$$\begin{bmatrix} I_Y \\ V_X \\ I_Z \end{bmatrix} = \begin{bmatrix} 0 & 1 & 0 \\ 1 & 0 & 0 \\ 0 & \pm 1 & 0 \end{bmatrix} \begin{bmatrix} V_Y \\ I_X \\ V_Z \end{bmatrix} \quad (2.18)$$

From the above matrix description it is found that, if a potential is applied on port Y then equal voltage will appear at port X and this voltage is independent of current supplied to port X. Thus circuit exhibits a virtual short circuit at port X.

Also, the current flows through port Y is equal to the current supplied to port X and this current is independent of voltage at port Y. Thus circuit exhibits a virtual open at port Y. Finally, the current supplied to X is also conveyed to the output port Z which is at a high impedance level.

The impedance level at different ports of first generation current conveyor is listed in table 2.1

Table 2.1 Impedance level at ports of CCI [2].

CCI Ports	Impedance Level
X	Low (ideally zero)
Y	Low (ideally zero)
Z	High (ideally infinite)

The application of CCI± becomes difficult because both the ports X and Y have zero input impedance in order to sink currents. The port Y needs to control a current rather than to control a voltage, which is usually difficult to obtain in practical designs. This is the perhaps the greater limit of the CCI device and this reduces its flexibility and versatility.

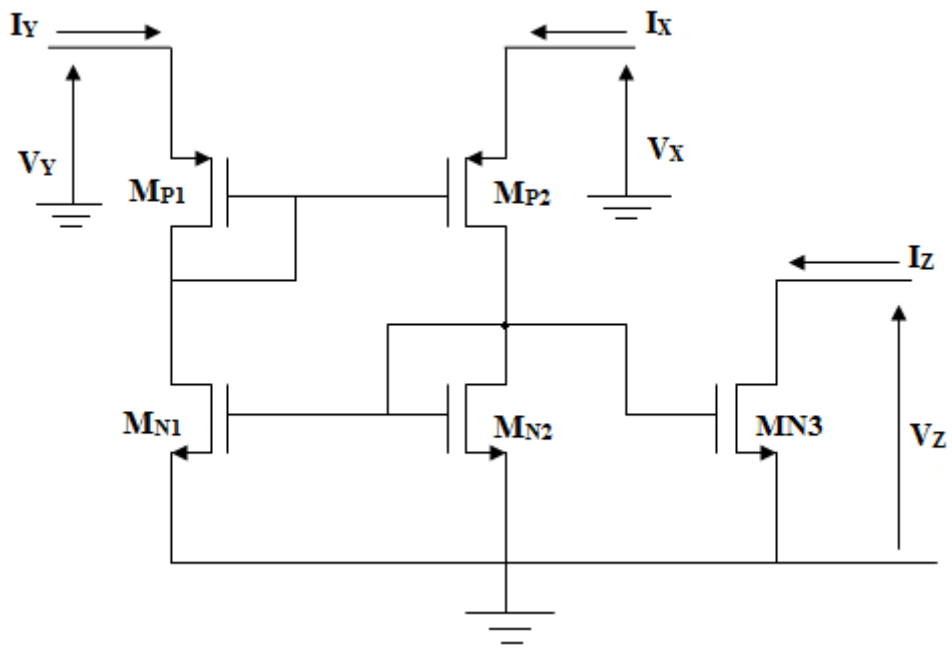


Figure 2.10 Class A implementation of current conveyor [2].

The simple MOS implementation of first generation current conveyor using class A topology is shown in figure 2.10. In this configuration, the transistors M_{P1} and M_{P2} perform the voltage following action between ports X and Y, therefore voltage at port X follows the voltage at port Y irrespective of the current flowing in port X. The current mirror formed by the transistors M_{N1} and M_{N2} provides a current I_Y equal to that of

current flowing in port X. And with the use of transistor M_{N3}, the same current is conveyed to the high impedance port Z.

2.4.1.1 PUSH-PULL CURRENT CONVEYOR

The current handling capability of the first generation current conveyor can be extended by constructing a push-pull current conveyor as shown in figure 2.11. The positive half of the ac signal goes through the lower conveyor comprising of transistors M_1-M_5 whereas the negative half of the signal goes through the upper conveyor comprising of transistors M_6-M_{10}.

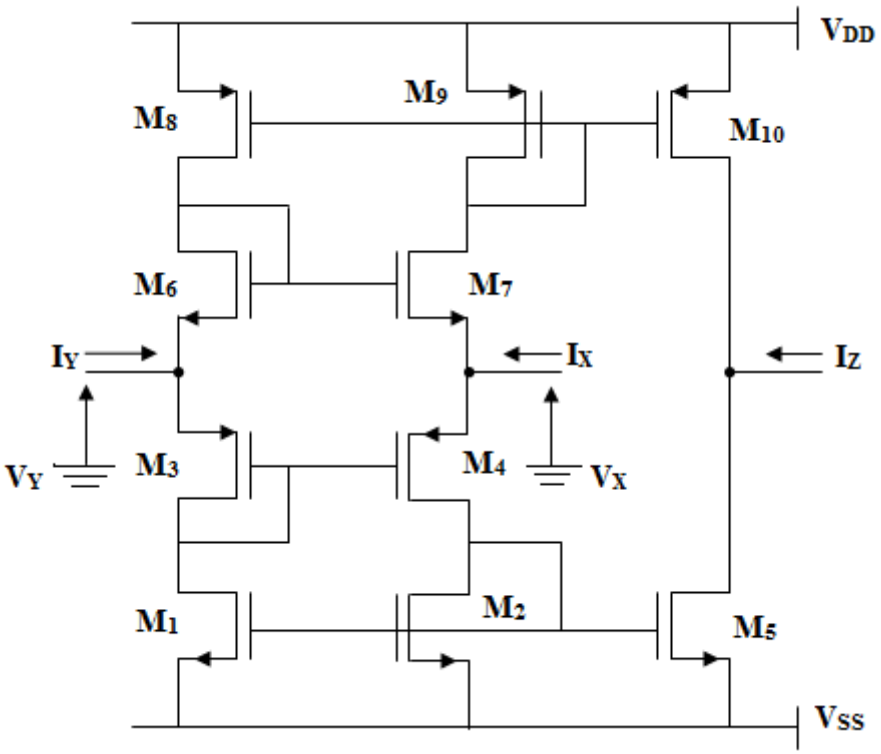


Figure 2.11 Push-Pull Current Conveyor [7].

The quiescent current of this push-pull current conveyor depends on several mechanisms and is very difficult to derive. However, an approximation of this current can be represented as,

$$I_Q \approx \frac{I_Q^{'} + I_Q^{''}}{2} \tag{2.19}$$

where,

$$I_Q^{'} = \frac{\beta_6 + \beta_8}{2\left(\sqrt{\beta_6} + \sqrt{\beta_8}\right)^2}(V_{DD} - V_{T6} - |V_{T8}|)^2 \tag{2.20}$$

$$I_Q^{"} = \frac{\beta_1 + \beta_3}{2\left(\sqrt{\beta_1} + \sqrt{\beta_3}\right)^2}(V_{DD} - V_{T1} - |V_{T3}|)^2 \qquad (2.21)$$

are the quiescent currents of the upper and lower half circuit respectively. From these equations, it can be seen that the quiescent current strongly depends upon the supply voltage.

In this push-pull configuration, if the current mirrors are ideal with infinite drain to source impedance then the quiescent current in the X-input branch must equal to the quiescent current in the Y-input branch. But in actual practice, the current mirror gain is not exactly one and this adds significant variation to the quiescent current. This current variation may be even so large that few milivolts of threshold voltage mismatch may turn off the quiescent current [8].

2.4.1.2 APPLICATIONS OF CCI

The first generation current conveyor, CCI is a basic building block can be used for variety of applications. The following are the application of CCI:

- The low impedance at the input terminal allows this current conveyor to be used as a current amplifier.
- The DC-voltage level at the current input port X can be easily set to a desired value by the voltage at the Y-terminal and input voltage-to-current conversion is easier than in the case of a current-mirror. This is shown in figure 2.12.

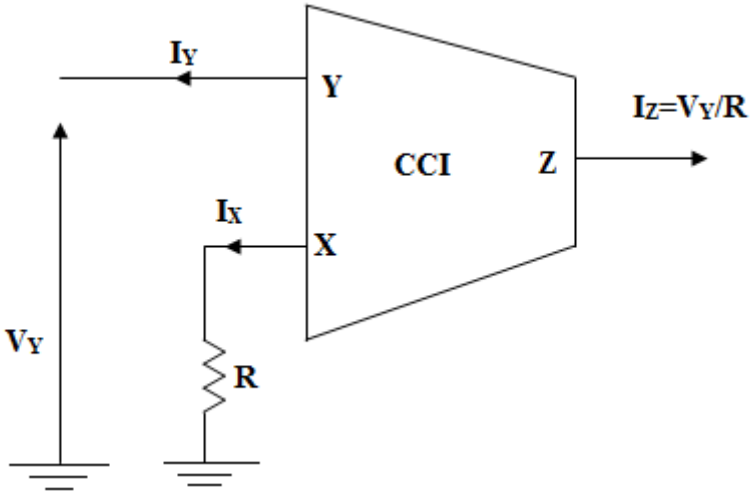


Figure 2.12 Voltage-to-Current Conversion [2].

- The first generation current conveyor can also be used as a negative impedance converter. If port Y is terminated with a grounded resistance R, then the impedance at

the port X equals to

$$Z_X \approx -R \qquad (2.22)$$

and thus impedance conversion takes place at port X.

- This current conveyor can also be used in current and voltage reference circuits. The core of a typical CMOS PTAT or Bandgap-reference is a first generation current conveyor [9]. Since this application generally has no specific speed requirements, both the variation of input impedance and the input offset voltage can easily be minimized by using large input transistors.
- The application of CCI also involves the linearization of MOS transistor transconductance in transconductance-C filters. Because the transconductance of a MOSFET in triode region strongly depends on its drain-source voltage, therefore CCI can be used to force the drain voltage to a fixed potential and mirror the drain current to the high-impedance Z-output.
- This block is widely used in the design of all pass filters, universal filters and sinusoidal oscillators. The realization of an all pass filter using CCI is shown in figure 2.13. All-pass filters, also called phase equalizers, are needed to shift the phase while keeping the amplitude constant. This circuit employs a single first generation current conveyor and reduced number of passive elements mainly two resistors and one capacitor. Here CCI is implemented using Class AB topology.

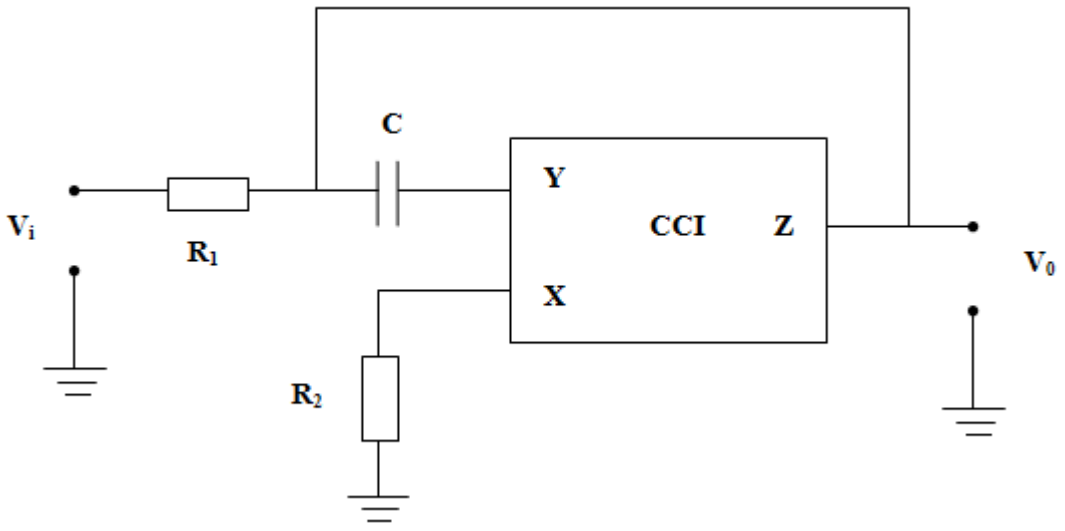


Figure 2.13 All pass filter implemented through CCI [10].

2.4.2 SECOND GENERATION CURRENT CONVEYOR (CCII)

The second generation current conveyor (CCII) is one of the most versatile current-mode building block. For many applications, a high impedance input port is preferable in order to avoid loading effect. So, second generation current conveyor was developed to fulfill this requirement. It has one high and one low impedance input port rather than the two low impedance input ports of CCI.

Since its introduction in 1970, it has been used in a wide range of applications and several circuits have been realized using this block. The CCII can be considered as the basic analog circuit design block because all the active devices can be made of a suitable connection of one or two CCIIs. It is a three terminal device and the block representation of this conveyor is shown in figure 2.14.

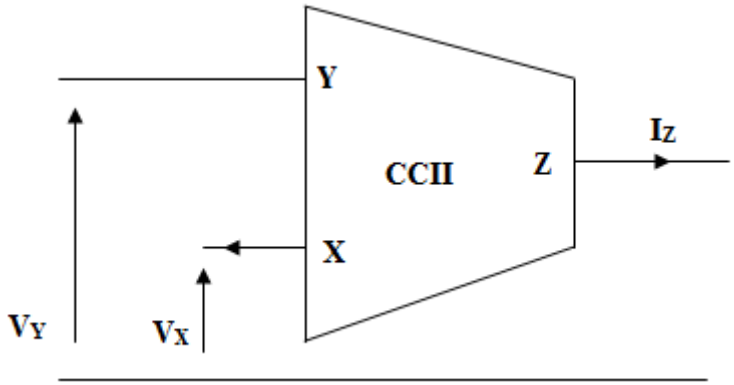


Figure 2.14 Block representation of CCII [2].

The relation between the terminal voltages and current of CCII can be given by the following matrix relation,

$$\begin{bmatrix} I_Y \\ V_X \\ I_Z \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 \\ 1 & 0 & 0 \\ 0 & \pm 1 & 0 \end{bmatrix} \begin{bmatrix} V_Y \\ I_X \\ V_Z \end{bmatrix} \quad (2.23)$$

This current conveyor differs from the first generation current conveyor in a sense that the port Y is a high impedance port i.e. there is no current flowing into port Y. The port Y of the second generation current conveyor is used as a voltage input and port Z is used as a current output port. Whereas, the port X can be used as a voltage output or as a current input port. Therefore, this current conveyor can be used to process both voltage and

current signals.

There are two types of second generation current conveyors:

- Positive current conveyor (CCII+) in which the currents i_x and i_z have the same direction as in a current mirror.
- Negative current conveyor (CCII-) in which currents i_x and i_z have the different direction as in a current buffer. These two conveyors are shown in figure 2.15.

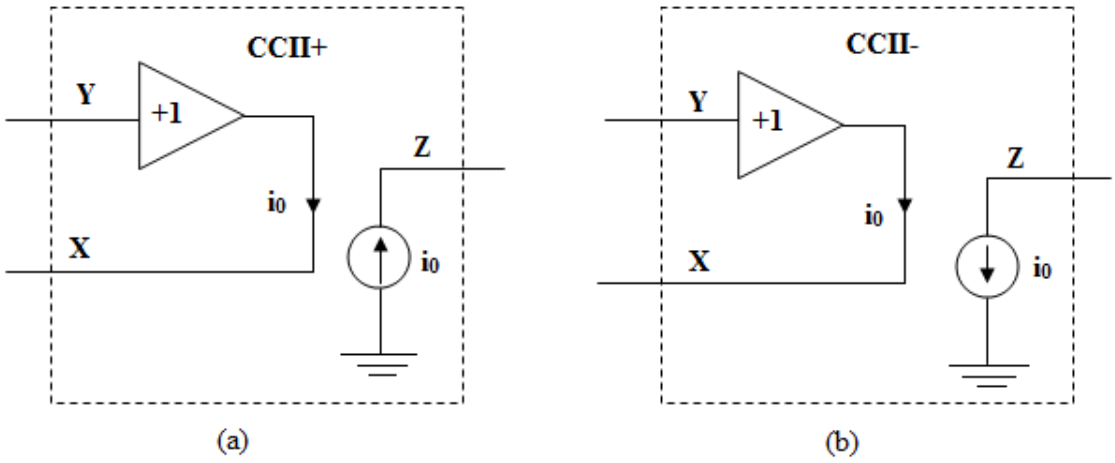


Figure 2.15 (a) Positive CCII+, (b) Negative CCII- [3].

The impedance level at various ports of second generation current conveyor is shown in the table 2.2. Impedance at input and output ports of current conveyors plays an important role in determining its characteristics.

Table 2.2 Impedance level at ports of CCII [2].

CCII Ports	**Impedance Level**
X	Low (ideally zero)
Y	High (ideally infinite)
Z	High (ideally infinite)

In ideal current conveyor, the value of voltage and current gain is unity ideally. But in actual practice due to some non-linearity, there is some deviation from the ideal characteristics. Figure 2.16 shows a real or non-ideal model of CCII where α and β

parameters are taken in account to consider the non-perfect voltage and current buffer characteristics, even if real values are very close to unity.

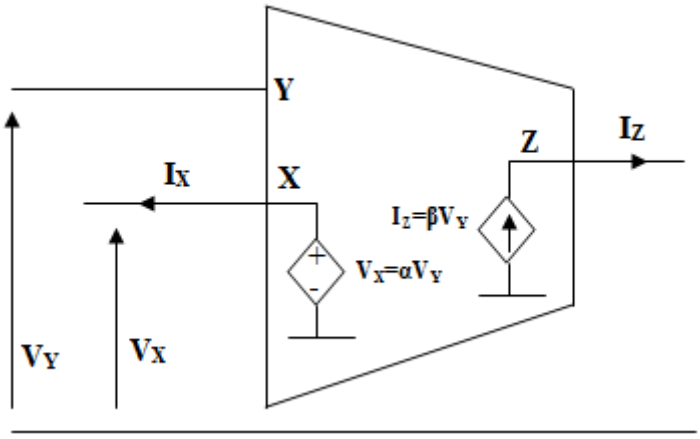


Figure 2.16 Non ideal model of CCII [2].

The NMOS transistor as shown in figure 2.17 can be regarded as a CCII. This not only gives the idea of the importance and usefulness of CCII, but also introduces a particular analogy between transistor and conveyor.

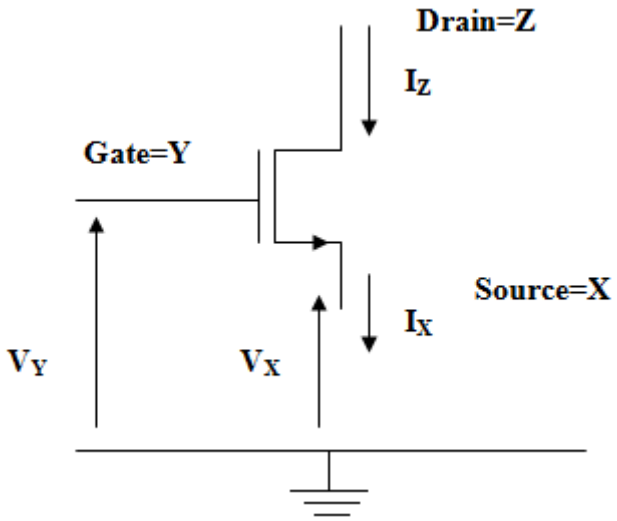


Figure 2.17 NMOS transistor and its equivalence with CCII [2].

Due to the source follower effect, the signal applied to the gate of MOSFET is almost equal to that obtained at the source terminal. This voltage transfer function between port X and Y is expressed by the 'α' parameter and is given by eq. (2.24)

$$\propto = \frac{V_X}{V_{G2}} = \frac{g_m\, r_0\, R_{XLoad}}{1 + g_m\, r_0\, R_{XLoad}} \qquad (2.24)$$

The small signal model of this NMOS transistor is shown in figure 2.18. From this, it can be seen that the currents I_X and I_Z are equal.

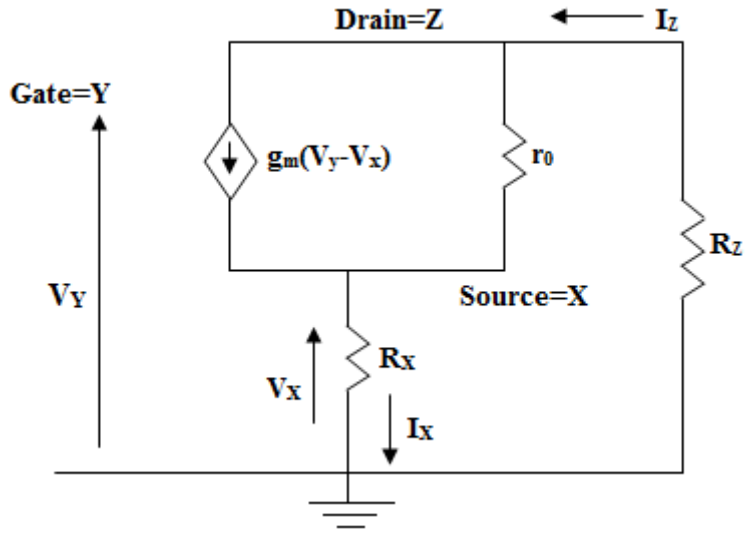


Figure 2.18 Small-signal model of NMOS transistor [2].

The current transfer ratio between ports X and Z is given by the 'β' parameter and is unity in this case.

$$\beta = \frac{I_z}{I_x} = 1 \tag{2.25}$$

From the small signal model of NMOS transistor, it can be found that:

- Impedance at port Y is given by the transistor gate capacitance, so it is quite high, which is required by theoretical specifications.
- Impedance at port X is affected by the load connected to the port Z.
- While the impedance at port Z is related to the load connected to the port X.

The impedance at ports X, Y and Z as calculated from small signal model is expressed as,

$$Z_Y = \gamma\, WLC_{OX} \tag{2.26}$$

$$Z_X = \frac{r_0\, R_{ZLoad}}{1 + g_m\, r_0} \approx \frac{1}{g_m} \tag{2.27}$$

$$Z_Z = r_0 + (1 + g_m r_o) R_{XLoad} \tag{2.28}$$

Here γ is a constant parameter whose value is 2/3 in saturation region and 1 otherwise, C_{OX} is the gate oxide capacitance and W and L being the width and length of the NMOS

transistor respectively. Thus a single NMOS transistor can be seen as a second generation current conveyor but the biasing voltages at ports X and Y show a relative difference of about one threshold voltage. This difference can be eliminated by considering NMOS current mirror which can also be considered as a CCII. The traditional NMOS current mirror is shown in figure 2.19.

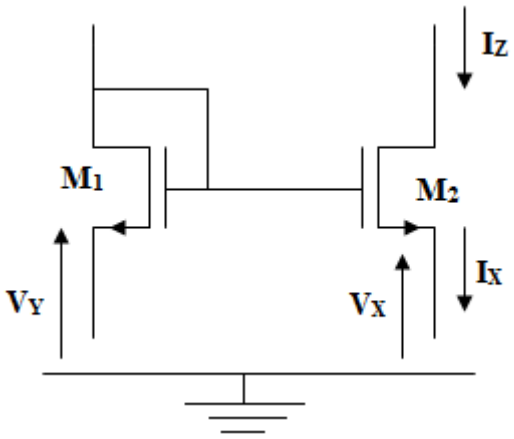


Figure 2.19 NMOS Current Mirror [2].

For this current mirror, the voltage at port X can be expressed as a function of the voltage at gate of M_2 and is given by eq. (2.29)

$$\frac{V_X}{V_{G2}} = \frac{g_{m2}\, r_{02}\, R_{XLoad}}{1 + g_{m2}\, r_{02}\, R_{XLoad}} \tag{2.29}$$

In order to calculate the voltage transfer function 'α', the voltage at the gate of transistor M_2 (V_{G2}) can be determined as a function of V_Y by considering the circuit depicted in figure 2.20. From this, we can write

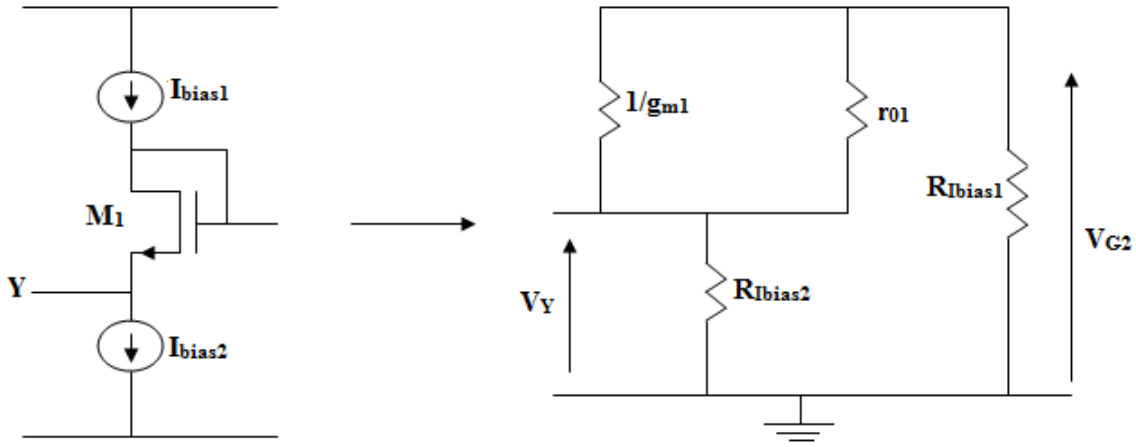


Figure 2.20 Half NMOS current mirror and its small-signal equivalent [2].

$$V_{G2} = \frac{R_{IBIAS\ 1}}{R_{IBIAS\ 1} + \frac{r_{01}}{1 + g_{m1} r_{01}}} V_Y \cong V_Y \qquad (2.30)$$

2.4.2.1 CLASS AB TOPOLOGY

The class AB topology of second generation current conveyor has been shown in figure 2.21. In order to ensure correct operation the bias currents, I_{Bias1} and I_{Bias2} have to be equal.

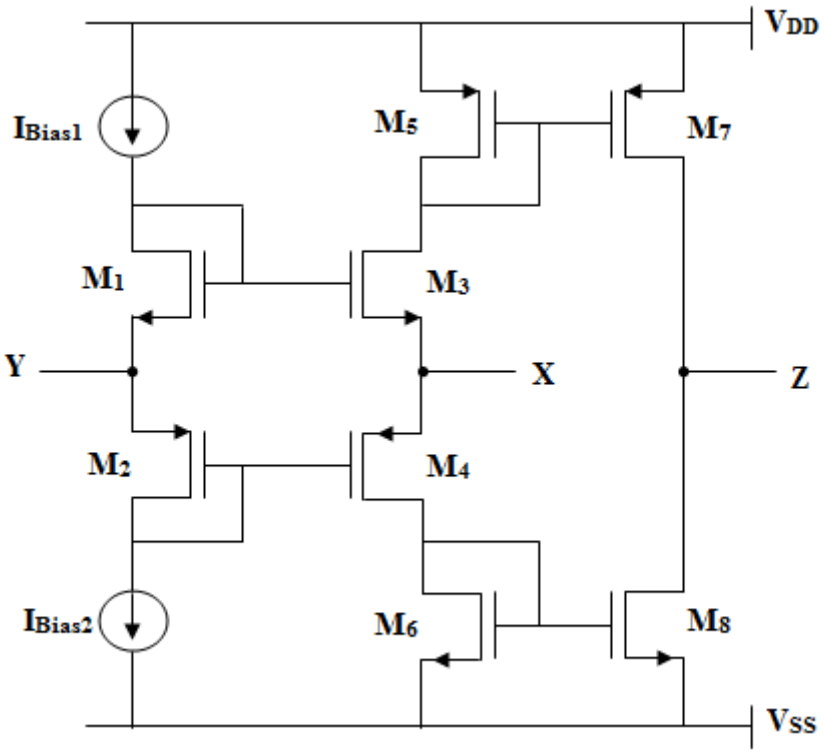


Figure 2.21 Class AB topology of CCII [11].

If the product $g_m r_o$ is much greater than 1, then the voltage transfer characteristic is very close to unity and is given as

$$\alpha = \frac{V_X}{V_Y} = \frac{1}{1 + \frac{1}{(g_{m3} + g_{m4})(r_{03} // r_{04})}} \cong 1 \qquad (2.31)$$

The loads connected to the ports X and Z show negligible impedances with respect to the output impedance of MOS transistor and the expression of β can be expressed as

$$\beta = \frac{I_Z}{I_X} \cong \frac{g_{m3} g_{m6} g_{m7} + g_{m4} g_{m5} g_{m8}}{g_{m5} g_{m6} (g_{m3} + g_{m4})} = 1 \qquad (2.32)$$

The impedance level at port Y can be affected by the output impedance of the two current sources. Therefore, a high impedance level can be ensured by using good biasing sources having high output impedances. The expression for the impedance at port Y is given as

$$Z_Y = \left(\frac{r_{01}}{1 + g_{m1} r_{01}} + R_{IBIAS\ 2}\right) // \left(\frac{r_{02}}{1 + g_{m2} r_{02}} + R_{IBIAS\ 2}\right)$$

$$\cong R_{IBias1} // R_{IBias2} \tag{2.33}$$

The impedance at port X of this topology can be derived as

$$Z_X \cong \frac{1}{g_{m3} + g_{m4} + \frac{r_{03} + r_{04}}{r_{03} r_{04}}} \cong \frac{1}{g_{m3} + g_{m4}} \tag{2.34}$$

The impedance seen at port Z is typically high and is given by eq. (2.35)

$$Z_Z \cong \frac{r_{07} r_{08}}{r_{07} + r_{08}} \tag{2.35}$$

2.4.2.2 APPLICATIONS OF CCII

The CCII can be considered as the basic circuit block because all the active devices can be made of a suitable connection of one or two CCIIs. The various applications of CCII are:

- Voltage Controlled Current Source (VCCS)
- Current Controlled Voltage Source (CCVS)
- Current Amplifier
- Current Differentiator
- Current Integrator

2.4.3 THIRD GENERATION CURRENT CONVEYOR (CCIII)

The third generation current conveyor can be considered as a current controlled current source device with a unity gain. This type of current conveyor is useful to take out the current flowing through a floating branch of a circuit and can be utilized in realization of various multifunction filters, inductance simulation and all pass sections [12]. High performance current mirrors are required in the CMOS structure realization of CCIII in order to provide the good dynamic swing and high output resistance which enables cascadability [13].

The main features of the CCIII are:

- Low gain errors (high accuracy)
- High linearity
- Wide frequency response

The CCIII is a three port device and the relation between terminal voltages and currents of this current conveyor can be given by the following matrix relation,

$$\begin{bmatrix} I_Y \\ V_X \\ I_Z \end{bmatrix} = \begin{bmatrix} 0 & -1 & 0 \\ 1 & 0 & 0 \\ 0 & \pm 1 & 0 \end{bmatrix} \begin{bmatrix} V_Y \\ I_X \\ V_Z \end{bmatrix} \quad (2.36)$$

That is, it has a +1 voltage gain between ports X and Y, a +1 current gain between ports X and Z and a -1 current gain between ports X and Y. The latter property enables the use of this circuit as an integrated floating current sensing device [14].

The basic building blocks for the realization of CMOS CCIII are shown in figures 2.22 and 2.23. Figure 2.22 shows a schematic diagram of the circuit which implements the port X-Y relationship in a first generation current conveyor. If all the transistors M_A-M_D are in saturation region then it can be easily found that the current Ix entering at port X is equal to the current I_Y and that the relation $Vx = V_Y$ holds for the voltages at ports X and Y.

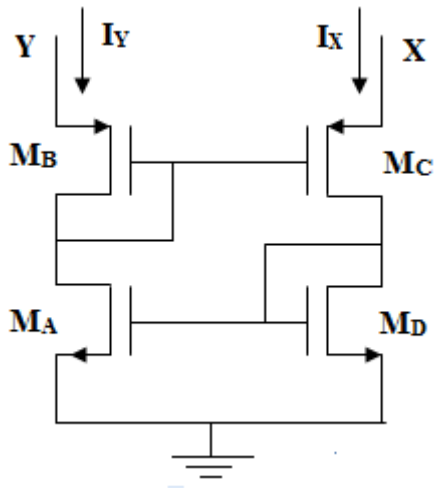


Figure 2.22 Building block of CCIII [15].

The circuit shown in figure 2.23 acts as an inverting class AB current follower. By using the translinear principle, the current I_P entering at port P is found to be equal to the current I_Q entering at port Q.

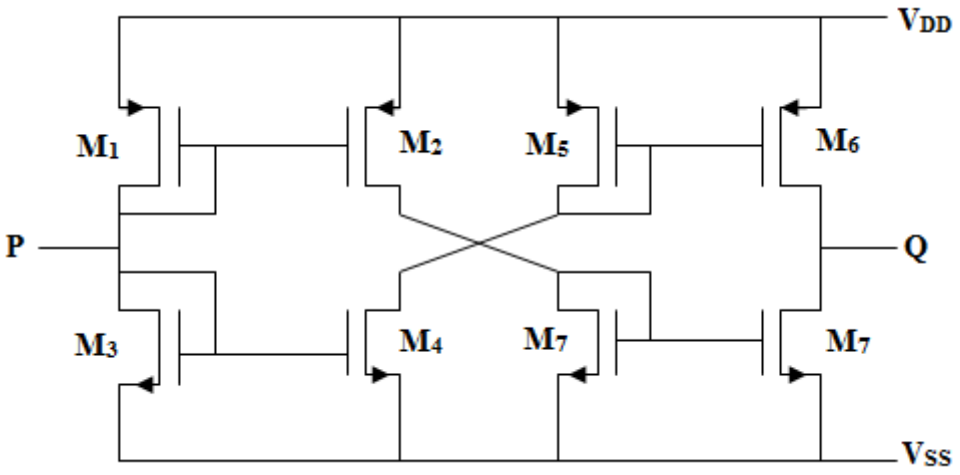


Figure 2.23 Inverting Class AB Current Follower [15].

2.4.3.1 APPLICATION OF CCIII

The third generation current conveyor can be used as an active current probe. The typical current measurement set-up is shown in figure 2.24, where the voltage drop over a small shunt resistor is amplified with a voltage amplifier, is problematic if a low shunt resistance is required. In such a case, a large voltage gain is needed to amplify this small voltage drop across the resistor *R*, which limits the measurement bandwidth and makes the measurement more sensitive to offset voltage, noise, and RF-interference [3].

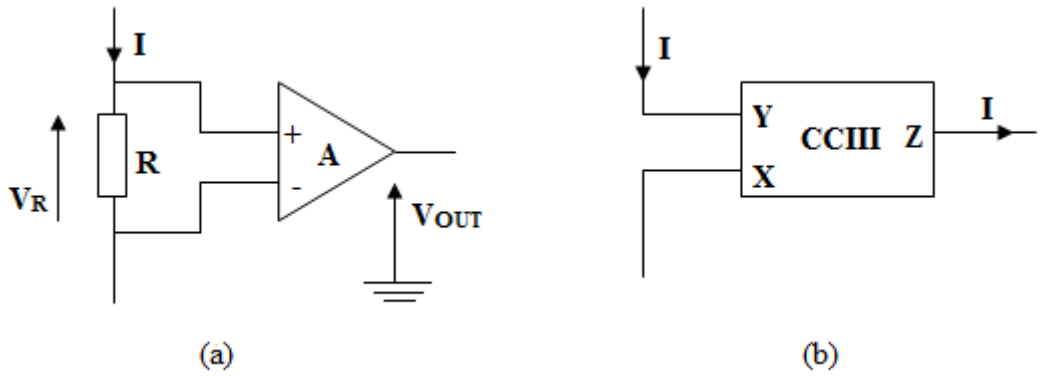


Figure 2.24 Current measurement (a) with a voltage amplifier (b) with a CCIII [3].

By using the CCIII in preference to the shunt resistor, the voltage drop can be maintained small without other problems arising.

CHAPTER 3

DESIGN OF CMOS CURRENT CONVEYORS

3.1 INTRODUCTION

This chapter explains the design approach of dual output second and third generation current conveyors. In section 3.2, the circuit description of high performance second generation current conveyor has been discussed. Section 3.3 discusses the circuit description of high performance third generation current conveyor. Section 3.4 gives the idea of design specifications used for designing these circuits and in section 3.5, the CMOS technology parameters and CAD tools have been discussed.

3.2 CIRCUIT DESCRIPTION OF SECOND GENERATION CURRENT CONVEYOR

The current-mode circuits are widely being used in high frequency circuit design applications and the second generation current conveyor (CCII) is the most widely used active element in signal processing applications. The CCII circuits based on the translinear loop have excellent wideband current and voltage following behavior.

So this circuit is designed to meet the desired high voltage and current following action (upto 1 GHZ). In an analog circuit, different active devices should be properly biased in order to get high performance. For example, most of the transistors in a CMOS circuit have to be biased in a saturation region to work properly. Almost all of the CMOS CCII circuits need additional voltage or current source in order to bias the transistors. These additional biasing sources results in various drawbacks such as area and power overhead and also these are highly sensitive to supply and temperature variations [16].

The high performance second generation current conveyor has been simulated using UMC 0.35μm CMOS process parameters (BSIM3v3 model) in Cadence Design Environment.

The BSIM3v3 model is an accurate and industry standard model which includes all the second order effects. The circuit diagram of this second generation current conveyor is shown in figure 3.1.

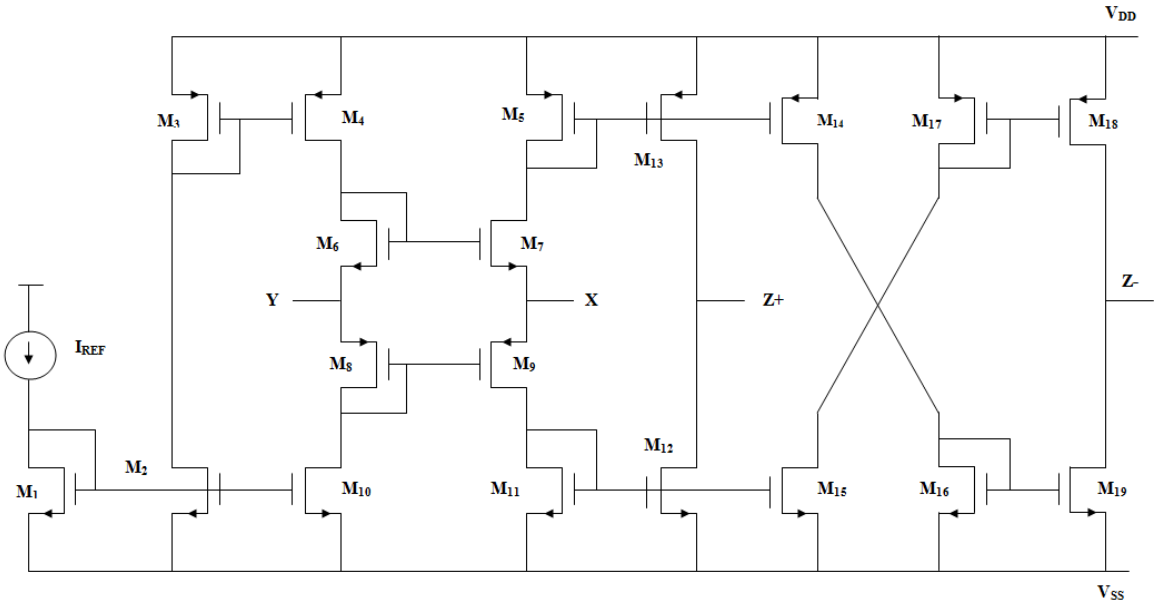


Figure 3.1 Schematic of Second Generation Current Conveyor [17].

This structure performs the following two functions:

- Voltage following action from port Y to port X
- Current following action from port X to port Z+ and Z-

3.2.1 DIFFERENT BLOCKS OF CCII

The circuit comprises of four different blocks:

- Transistors M_6-M_9 form the translinear loop whose role is to provide equal voltage in both X and Y ports. This input cell presents high impedance at the input port Y and a low impedance at the output port X.
- Transistors M_4 and M_{10} allow the mixed loop to be biased by the dc current I_o.
- Transistors (M_{11}, M_{12}) and (M_5, M_{13}) form the NMOS and PMOS current mirrors which supply the current being supplied at port X to the port Z+, which is at a high impedance level.
- The cross coupled structure formed by transistors M_{14}-M_{16} convey the same current but in inverting mode to the output port Z-, which is also at high impedance level.

The biasing current of the circuit plays an important role in determining the power consumption and the resistance at port X. So it is set to 50μ in order to meet the desired specifications.

3.2.1.1 MOS TRANSLINEAR LOOP

The term "translinear" was first introduced by Gilbert in 1975, which emphasizes on the fact that trans-conductance (g_m) is linear with current for the case of BJT transistor and also for MOS transistor operating in weak inversion. However, when transconductance is linear with the voltage instead of the current like eq. (3.1)

$$g_m = \frac{dI}{dv} = bV \tag{3.1}$$

where b is a scaling factor, then it leads to an another class of translinear circuits that can be implemented with the quasi quadratic law of the MOS transistor. Solving eq. (3.1) for dI in terms of V and then integrating we get,

$$I = \frac{b}{2}V^2 + B \tag{3.2}$$

Here B is an arbitrary constant and this fact is considered as an extension of the translinear principle, known as MOS (or voltage) translinear principle.

The equation of the current for MOS transistors operating in the strong inversion and saturation region is given as,

$$I_D = K_n \frac{W}{2L}(V_{GS} - V_T)^2 \tag{3.3}$$

Here $V_{GS,}$ V_T, K_n, W and L are the gate-to-source voltage, threshold voltage, MOS transconductance parameter, width and channel length respectively. Comparing eq. (3.2) and (3.3) we get,

$$b = \frac{W}{L}k_n \tag{3.4}$$

$$V = V_{GS} - V_T \tag{3.5}$$

$$B = 0 \tag{3.6}$$

According to eq. (3.3), the MOS translinear principle is stated as follows: In a loop with an even number of gate-source connections and with the same number of transistors arranged in clockwise (CW) and counterclockwise direction (CCW), then eq. (3.7) holds

$$\sum_{CW} \sqrt{\frac{I_D}{\frac{W}{L}}} = \sum_{CCW} \sqrt{\frac{I_D}{\frac{W}{L}}} \tag{3.7}$$

The eq. (3.7) holds only if it is assumed that all the transistors operate in strong inversion and saturation region. Another important characteristic arising from this is that the resulting relationship between drain currents ideally does not depend on temperature or process variations.

Mobility reduction and velocity saturation effects in deep sub-micron technologies degrade the square law performance of small devices. Due to such short-channel effects, the transconductance parameter (K_n) and the threshold voltage (V_T) of eq. (3.3) is no longer constant and showing some dependences on V_{GS} and V_{DS}.

In order to overcome such effects, the length of the transistors that form the translinear loops is chosen to be somewhat larger than the minimum length provided by the technology [18]. This choice also reduces mismatching and channel length modulation effects. But there is a decrement in bandwidth due to the increase in length.

The input cell comprises of transistors M_6-M_9 form the translinear loop and is shown in figure 3.2. This cell is the main core of the circuit as it provides equal voltages at ports X and Y, thus provide the voltage following action. This input cell presents high input impedance at the input port Y and a low impedance at output port X.

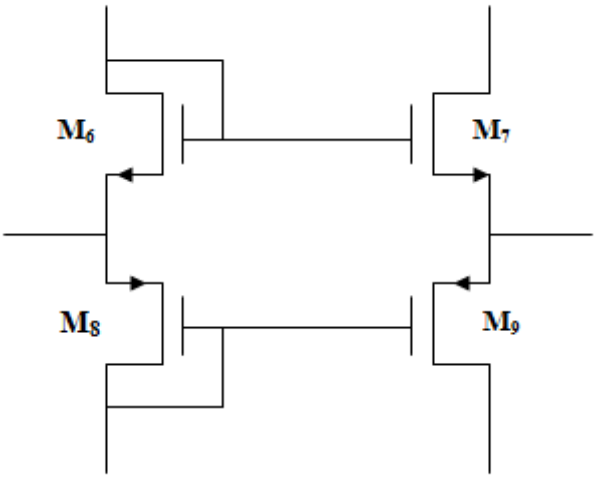


Figure 3.2 Mixed Translinear Loop.

The mixed translinear loop formed by the transistors is characterized by the following relationship between drain currents as,

$$\sqrt{\frac{I_{D6}}{\beta_n}} + \sqrt{\frac{I_{D8}}{\beta_p}} = \sqrt{\frac{I_{D7}}{\beta_n}} + \sqrt{\frac{I_{D9}}{\beta_p}} \tag{3.8}$$

where β_n and β_p are the gain of the NMOS and PMOS transistors respectively and are given by,

$$\beta_n = \frac{\mu_n C_{OX} W_n}{2L_n} \tag{3.9}$$

$$\beta_p = \frac{\mu_p C_{OX} W_p}{2L_p} \tag{3.10}$$

where μ_n and μ_p are respectively the electron and holes mobility and C_{OX} is the oxide capacitance and are technology dependent.

Taking $\beta_n=\beta_p$ we get,

$$2\sqrt{I_0} = \sqrt{I_{D7}} + \sqrt{I_{D9}} \tag{3.11}$$

The voltage gain of the circuit is given by,

$$\alpha = \frac{V_X}{V_Y} = \frac{1}{1 + \frac{1}{(g_{m7} + g_{m9})(r_{07} // r_{09})}} \cong 1 \tag{3.12}$$

From the eq. (3.12) it is clear that in order to maximize the voltage gain, the transconductance of the transistors M_7 and M_9 must be high so that the term in the denominator can be neglected. So for a given bias current I_0 and length of transistor, the g_m can only be increased by increasing the width of the transistors. Therefore, in order to maximize the voltage gain, the width of the transistors forming the translinear loop is kept large while designing the circuit.

3.2.1.2 CURRENT MIRRORS

The current mirror is one of the main building blocks of analog circuit design. For high performance applications, the accuracy and output impedance are the most important parameters to determine the performance of the current mirror. It is widely used in the biasing or the loading elements. The current variations due to the supply and the temperature can be reduced by using current mirror as the biasing elements.

Ideal CM has zero input and infinite output resistance, which implies that input voltage does not vary with input currents and output currents are independent of applied output voltage. However, the practical CMs have non zero input and finite output

resistances and thus do not copy the current properly. Therefore, special design approach has to be taken while designing CMs in order to ensure proper mirroring of current.

The design of current sources in analog circuits is based on copying currents from a reference with the assumption that one precisely defined current source is already available. Two identical MOS devices that have equal gate-to-source voltages and operate in saturation carry equal currents (if λ=0).

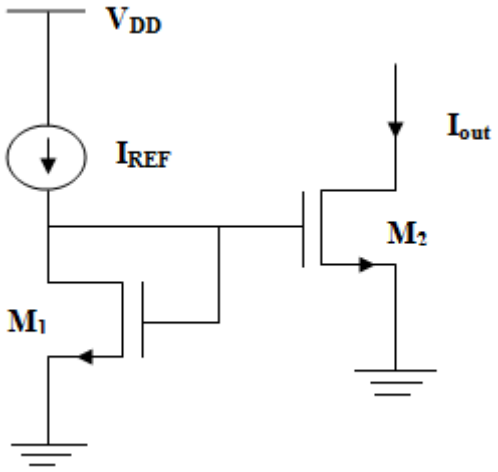


Figure 3.3 Basic Current Mirror [19].

The structure consisting of transistors M_1 and M_2 in figure 3.3 is called "current mirror". If channel length modulation effect is neglected, then current equation can be written as

$$I_{REF} = \frac{1}{2}\mu_n C_{OX}\left(\frac{W}{L}\right)_1 (V_{GS} - V_{TH})^2 \quad (3.13)$$

$$I_{OUT} = \frac{1}{2}\mu_n C_{OX}\left(\frac{W}{L}\right)_2 (V_{GS} - V_{TH})^2 \quad (3.14)$$

From above two equations we get,

$$I_{OUT} = \frac{(W/L)_2}{(W/L)_1} I_{REF} \quad (3.15)$$

The key property of this topology is that it allows precise copying of current with no dependence on process and temperature. Here I_{OUT} can track I_{REF} with reasonable accuracy by properly selecting the device dimensions.

Two stage Current Mirror is shown in figure 3.4. In order to calculate the relationship between I_{OUT} and I_{REF}, all the transistors are assumed to be in saturation

region and channel length modulation effect is neglected. Different drain current equations for this circuit are given as,

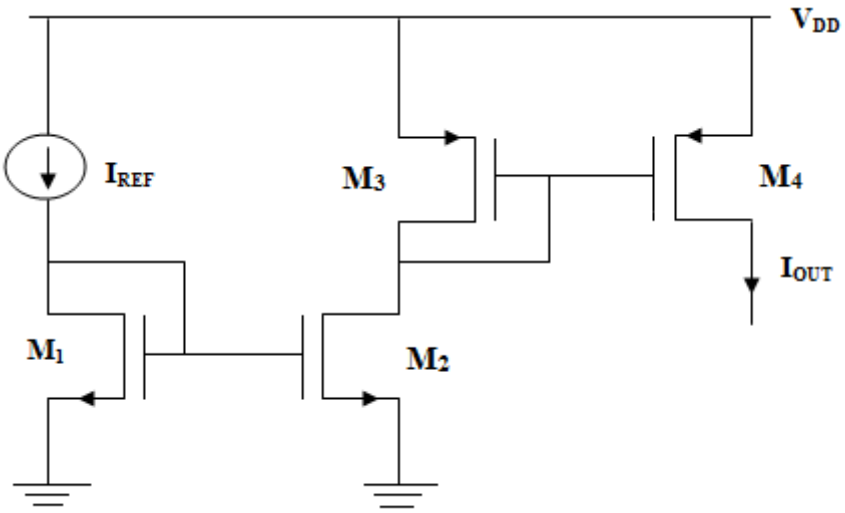


Figure 3.4 Two Stage Current Mirror [19].

$$I_{D2} = I_{REF}\left[\frac{(W/L)_2}{(W/L)_1}\right] \tag{3.16}$$

$$|I_{D3}|=|I_{D2}| \tag{3.17}$$

$$I_{D4} = I_{D3}\left[\frac{(W/L)_4}{(W/L)_3}\right] \tag{3.18}$$

Thus, $I_{D4}= \alpha\beta I_{REF}$ (3.19)

Where, $\alpha = \left[\frac{(W/L)_2}{(W/L)_1}\right]$ $\beta = \left[\frac{(W/L)_4}{(W/L)_3}\right]$ (3.20)

By properly selecting the value of α and β, a well defined current can be ensured between the two terminals.

Current mirrors employ the same length for all the transistors in order to minimize errors due to the side diffusion of the source and drain areas (L_D). This is because if L_{Drawn} is doubled, then L_{eff} = L_{Drawn}-2L_D is not. Also, the threshold voltage of short channel devices exhibits some dependence on the channel length. Thus, current ratioing is achieved only by scaling the width of transistors. So, only the width of the transistors in the circuit design is scaled in order to avoid above effects [19].

In summary, the current mirrors should have desirable characteristics:

a) Current transfer ratio must be precisely set by the (W/L) ratio and it should be independent of temperature.
b) Very high output resistance (high R_{out}) so that the output current is independent of output voltage.
c) Low input resistance (Low R_{in}).
d) Low input and output compliance voltages.

3.2.1.3 INVERTING CLASS AB CURRENT FOLLOWER

The cross coupled structure formed by transistors, M_{14}-M_{17} convey the same current but in inverting mode to the output port Z-, which is also at high impedance level. This inverting class AB current follower structure is shown in figure 3.5.

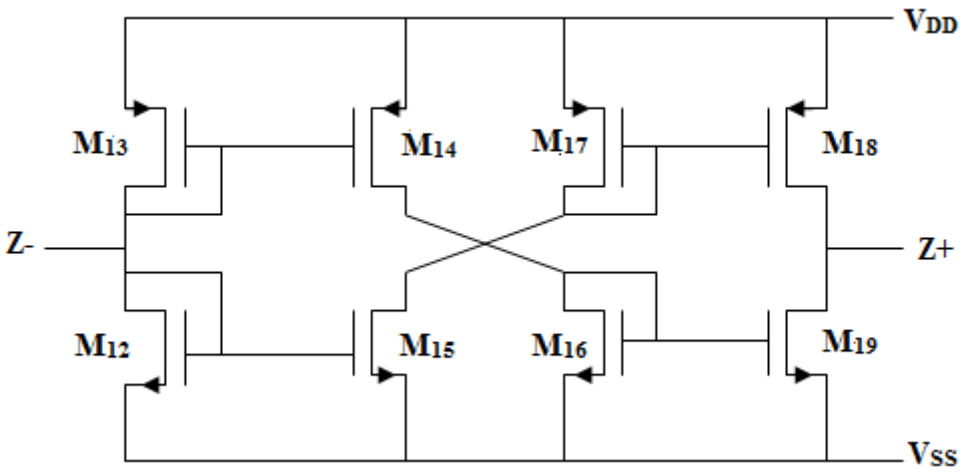


Figure 3.5 Cross Coupled Structure [15].

The current gain at port Z- depends upon the amount of current mirror to that branch, so the aspect ratio of the transistors is properly chosen in order to allow perfect current mirroring and also to have less offset of current. The circuit is designed to have unity current gain at the ports Z+ and Z-.

3.2.2 SMALL SIGNAL ANALYSIS OF CCII

The small signal analysis of the second generation current conveyor has been done in order to calculate the resistances at port X, Y and Z and its small signal model is shown in figure 3.6. The theoretical expression for the resistance at port X is given by,

$$R_X = \frac{1}{g_{m7} + g_{m9}} = \frac{1}{2\sqrt{K_P \frac{W_P}{L_P} I_0} + 2\sqrt{K_N \frac{W_N}{L_N} I_0}} \tag{3.21}$$

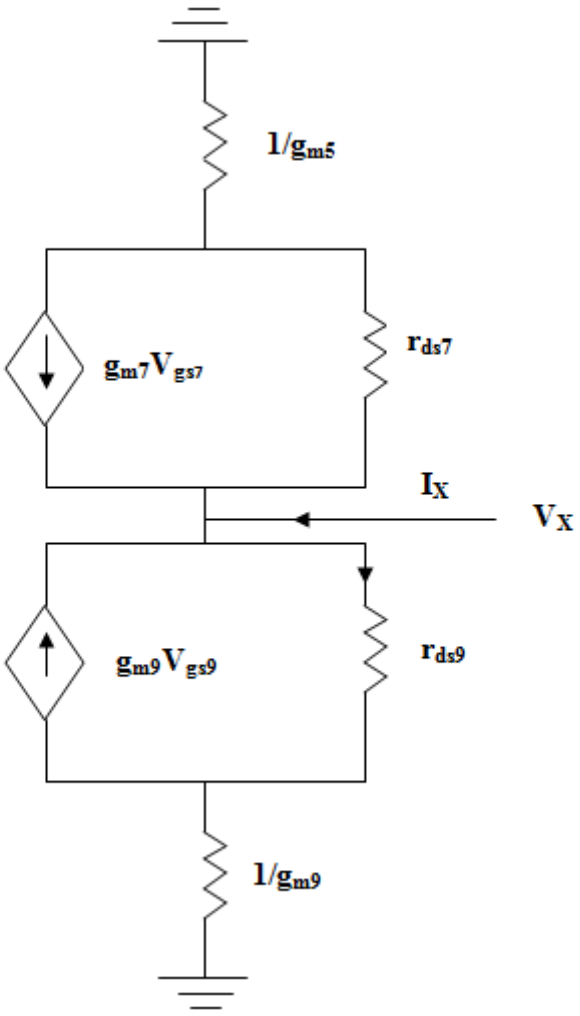


Figure 3.6 Small signal model at port X.

From the eq. (3.21), it can be seen that the resistance at port X depends upon the value of bias current of the circuit. So the value of bias current is properly chosen in order to have minimum value of resistance at port X.

In the same way, the small signal analysis at port Y and Z gives the value of resistance at these ports. The expression of the resistance at port Y and Z is given by,

$$R_Y = \left(\frac{1}{g_{m6}} + r_{04}\right)//\left(\frac{1}{g_{m8}} + r_{010}\right) \tag{3.22}$$

$$R_Z = r_{012}\left(1 - \frac{g_{m12}}{4 \propto \sqrt{I_0\beta}}\right)//r_{013}\left(1 - \frac{g_{m13}}{4 \propto \sqrt{I_0\beta}}\right) \tag{3.23}$$

From the above expressions (3.21), (3.22) and (3.23) it is clear that the bias current I_0 directly affects the parasitic resistances at port R_X, R_Y and R_Z.

3.3 CIRCUIT DESCRIPTION OF THIRD GENERATION CURRENT CONVEYOR

The third generation current conveyor (CCIIIs) can be considered as a current controlled current source with a unity gain. This type of the current conveyor is useful to take out the current flowing through a floating branch of a circuit and can be utilized in realization of various multifunction filters, inductance simulation and all pass sections. The circuit diagram of this conveyor is shown in figure 3.7

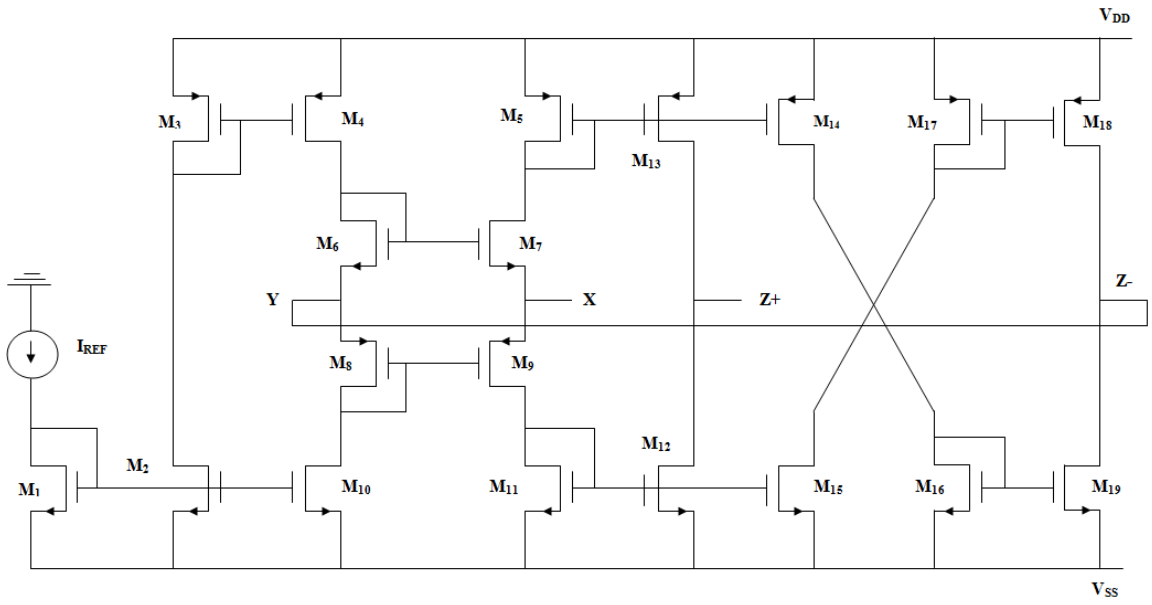


Figure 3.7 Schematic of Third Generation Current Conveyor [17].

The main features of this CCIII are

- Low gain errors (high accuracy)
- High linearity
- Wide frequency response

The only difference between second and third generation current conveyor is the flow of current in port Y. So, all the design considerations that are assumed for designing second generation current conveyor are also applied to this third generation current conveyor. There is only a small change in the design part of this conveyor and a feedback from port Z- to port Y has been introduced in order to allow the current flow in port Y. The rest of the circuit is same as second generation current conveyor. The current in port Y of third generation current conveyor flows in the opposite direction as that of current flows in the port X.

3.4 DESIGN SPECIFICATIONS

The dual output second and third generation current conveyors have been designed for following specifications listed in table 3.1.

Table-3.1 Design Specifications.

Parameters	**Value**
Technology	UMC 0.35μm
Supply Voltage	±1.5 V
Bias Current	50μ
Voltage Gain	≈1
Current Gain	≈1
Current bandwidth	>1 GHZ
Voltage Bandwidth	>1 GHZ

3.5 TECHNOLOGY PARAMETERS AND CAD TOOLS

Following are the technology parameters and CAD tools used in the present work for the design and verification.

3.5.1 TECHNOLOGY PARAMETERS

Foundary Specifications : UMC 0.35μm CMOS 1P6M process

Supply Voltage : ±1.5V

Spice MOS Model : BSIM3v3 (Level 49)

3.5.2 CAD TOOLS

Schematic Entry : Cadence Schematic Entry Analog Design Environment

Simulator : Cadence Spectre

Layout	:	Cadence Virtuoso
Layout Verification	:	Cadence Assura DRC/LVS
Extraction	:	Cadence Assura XRC Extraction Tool

3.5.3 BSIM3v3 MODEL BEHAVIOR

BSIM3v3 is the latest industry-standard MOSFET model for deep submicron digital and analog circuit designs from the BSIM Group at the University of California at Berkeley. Before starting the designing process, it is very essential to understand the behavior of models to know what these models are actually doing. It helps in design and analysis of MOS based circuits.

For the older CMOS processes greater than 2um, generally hand calculations and simulation results were comparable. The older devices followed “square-law” which were analytical and matched SPICE (Simulation Program with Integrated Circuit Emphasis) Level 1 and 2 models. These models provide the results that match with the hand calculations. However, if these hand calculations are used in the deep submicron process, the error is generally well above 25%.

As the dimensions of the MOSFET continue to scale down, a square law model become less accurate. Modern MOS transistors have non linear behavior so simulation is necessary to accurately predict the detailed circuit behavior. The simulators accept the model of reality provided by the designer and gives us the results, so it is very important to have accurate models.

In today’s small dimension MOS transistors, BSIM is more accurate, silicon proven and widely accepted in the industry. The BSIM3v3 model includes various short channel effects such as mobility degradation, threshold voltage variation, channel length modulation (CLM) effect and drain induced barrier lowering (DIBL).

CHAPTER 4

SIMULATION RESULTS

4.1 INTRODUCTION

The second and third generation current conveyors have been simulated using UMC 0.35μm CMOS technology process parameters in Cadence Design Environment. This chapter is organized as follows: The simulations results of second generation current conveyor are discussed in section 4.2. Section 4.3 presents the simulation results of third generation current conveyor.

4.2 SIMULATION RESULTS OF SECOND GENERATION CURRENT CONVEYOR

In this section, the CCII has been simulated by performing dc, ac and transient analysis in order to obtain desired parameters that are required for verifying the functionality of the present work.

4.2.1 DC ANALYSIS

The dc analysis of the CCII is performed in order to observe:

- Voltage transfer characteristics between ports Y and X.
- Current transfer characteristics between ports X and Z+, Z-.

For voltage transfer characteristics, a varying voltage source is applied at port Y and corresponding output is taken at port X. The input voltage is varied along X axis and from the figure 4.1 it can be seen that output follows the input for a range of -0.5v to 0.5v i.e. 1V which is about 33% of the total supply voltage (±1.5V) and there is an offset of about 8mV. During this analysis, the port Z was at ground terminal.

For current transfer characteristics, a varying current source is applied at port X and corresponding output is taken at ports Z+ and Z-. The input current is varied from

50µA to +50µA and the desired output current characteristics are shown in figures 4.2 and 4.3 and during this analysis, the port Y was at ground terminal.

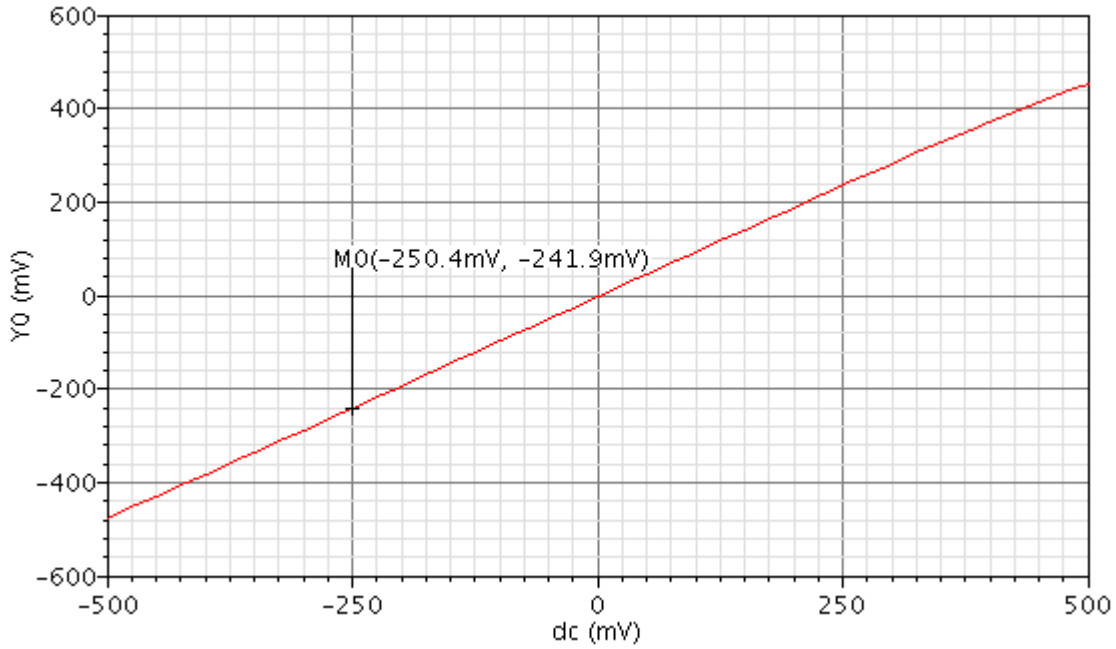


Figure 4.1 DC voltage characteristics at port X.

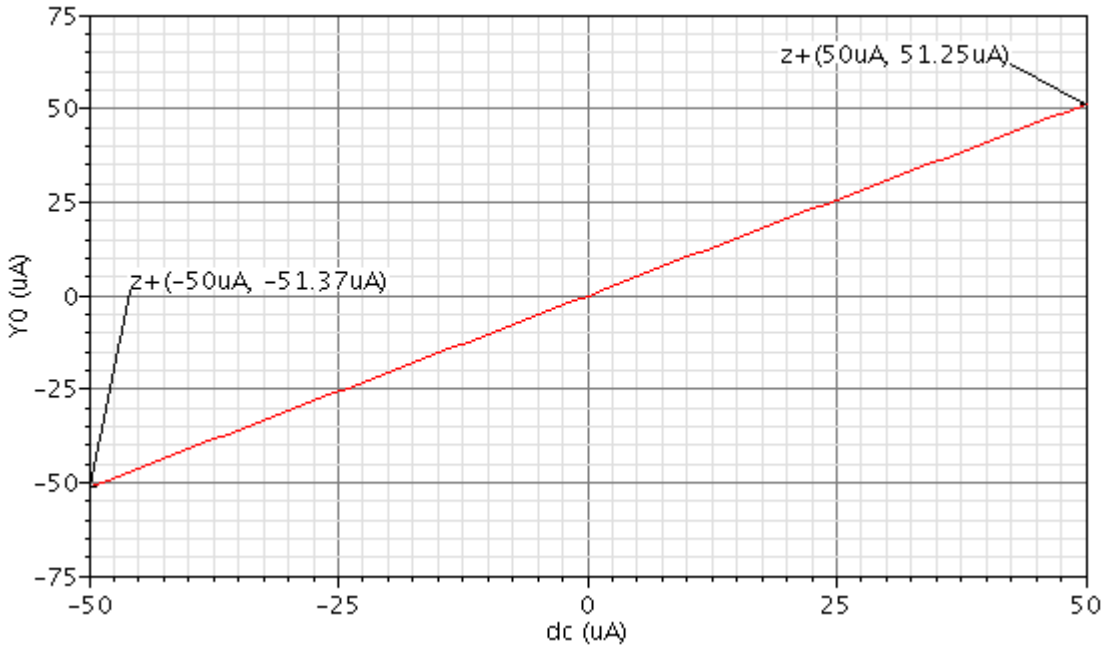


Figure 4.2 DC current characteristics at port Z+.

From the figure 4.2 it can be seen that there is an excellent current following action from port X to Z+ and an offset is found to be about 1µA. But the offset of about 3µA is found in the current following action from port X to Z-. This type of dc current characteristics

validates the performance of CCII as current follower between ports X and Z.

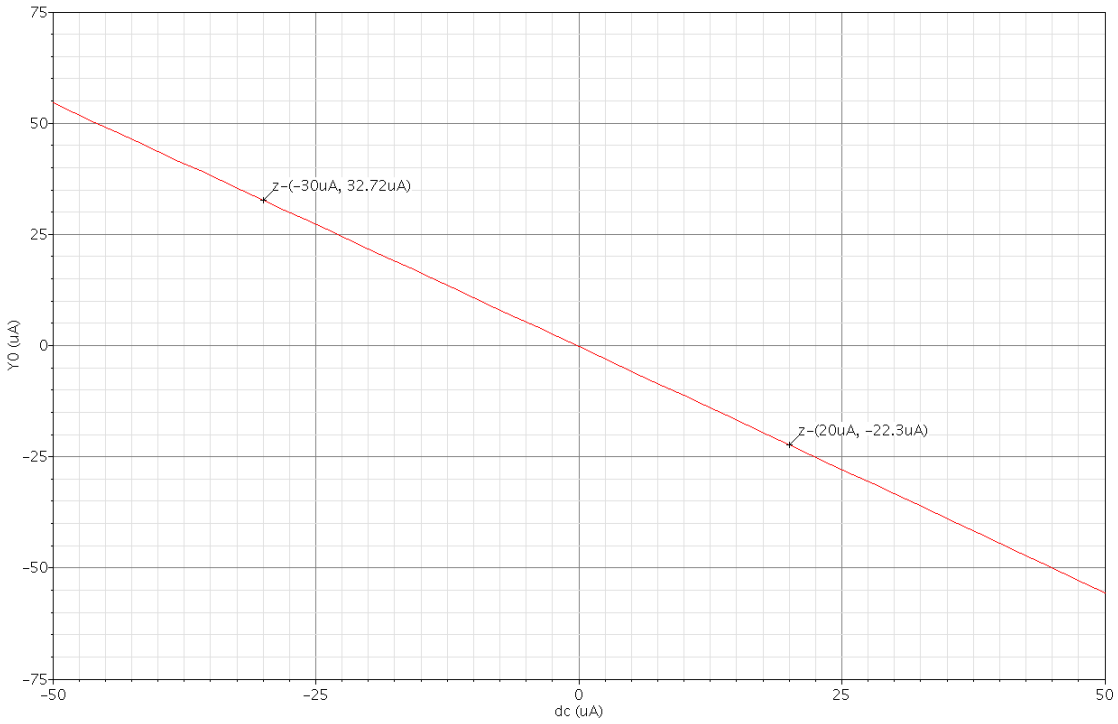


Figure 4.3 DC current characteristics at port Z-.

4.2.2 TRANSIENT ANALYSIS

Transient analysis of the CCII is performed in order to examine the voltage transfer characteristics between ports Y and X with respect to time. It is performed by applying two different voltage sources at port Y:

- Firstly by applying an AC voltage source of amplitude 0.4V peak-to-peak and having frequency 100 MHz at port Y and its transient response is shown in figure 4.4.
- Secondly, a pulse having amplitude ranging from -0.2V to +0.2V and frequency 100 MHz is applied at port Y and transient response is shown in figure 4.5. The rise and fall time of the pulse is taken as 5ns.

It can be seen from the figure 4.4 that output follows the input correctly and an offset is found to be 9.3mV between input and output. This type of characteristics validates the performance of CCII as voltage follower between ports Y and X. The output offset voltage can be minimized by increasing the width of the transistors that forming the translinear loop. But this increase in the width of transistors increases the capacitances

associated with these transistors and this reduces the voltage transfer bandwidth.

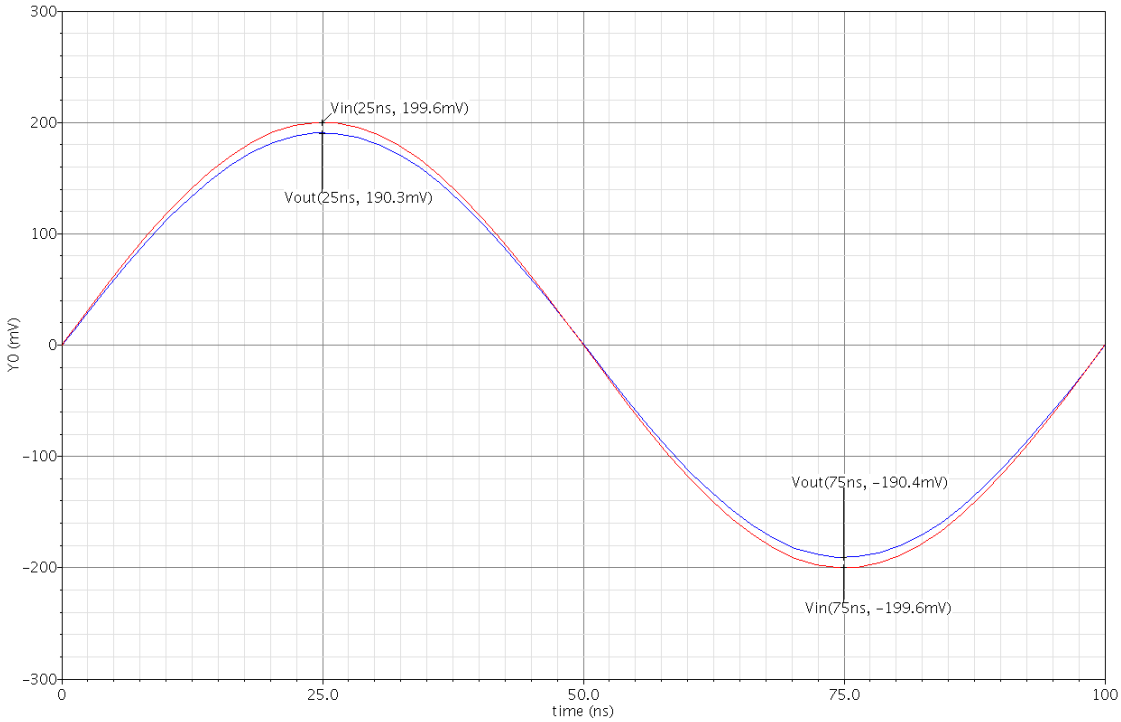


Figure 4.4 Voltage transfer characteristics by applying a sine wave.

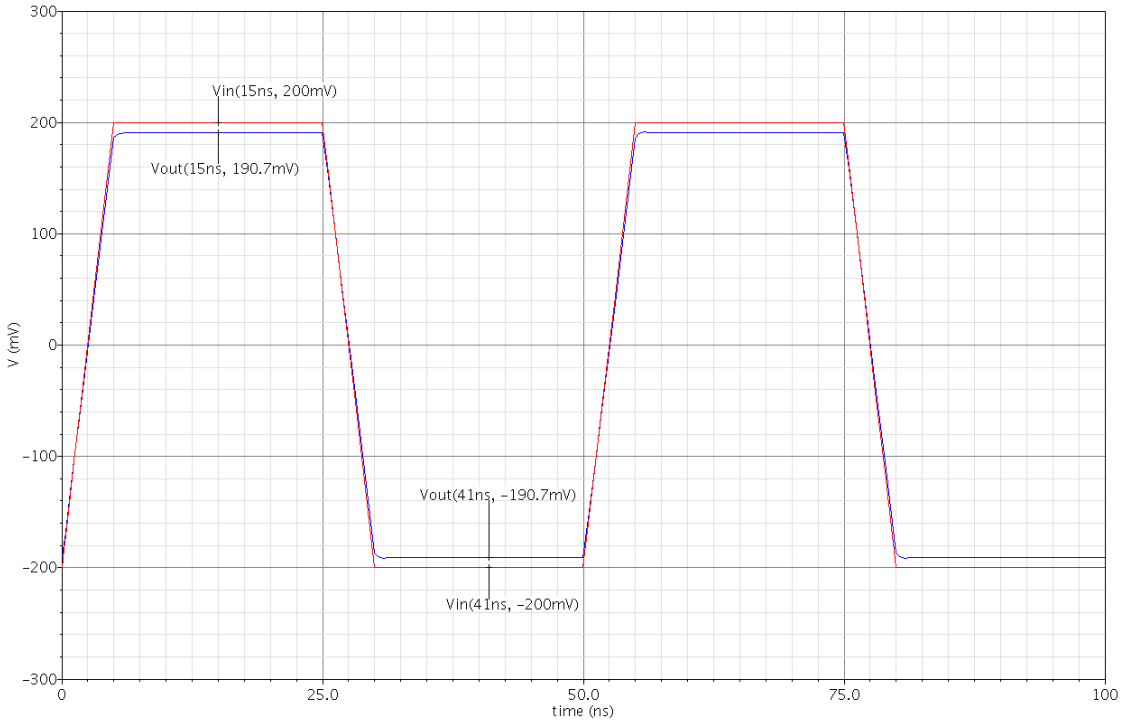


Figure 4.5 Voltage transfer characteristics by applying a pulse.

4.2.3 AC ANALYSIS

The frequency response of the voltage gain at port X is shown in figure 4.6 and its value comes out to be 0.956. Figure 4.7 shows the frequency response of current gain at ports Z+ and Z- and value of current gain at both the outport ports is found to be closer to unity.

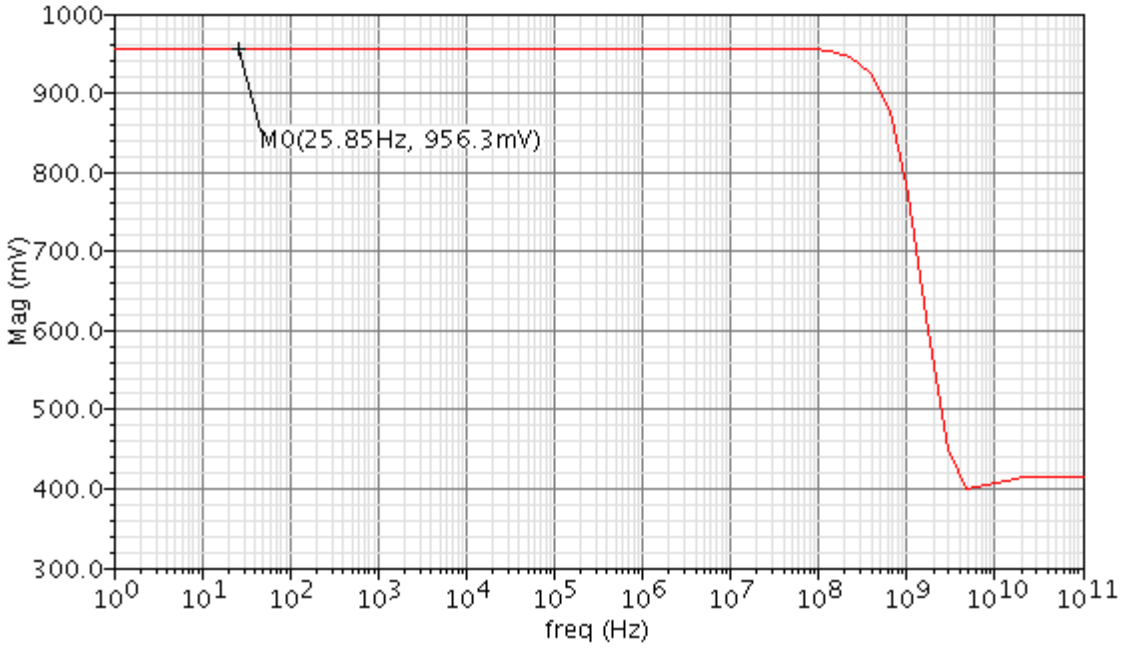


Figure 4.6 Frequency response of voltage gain at port X.

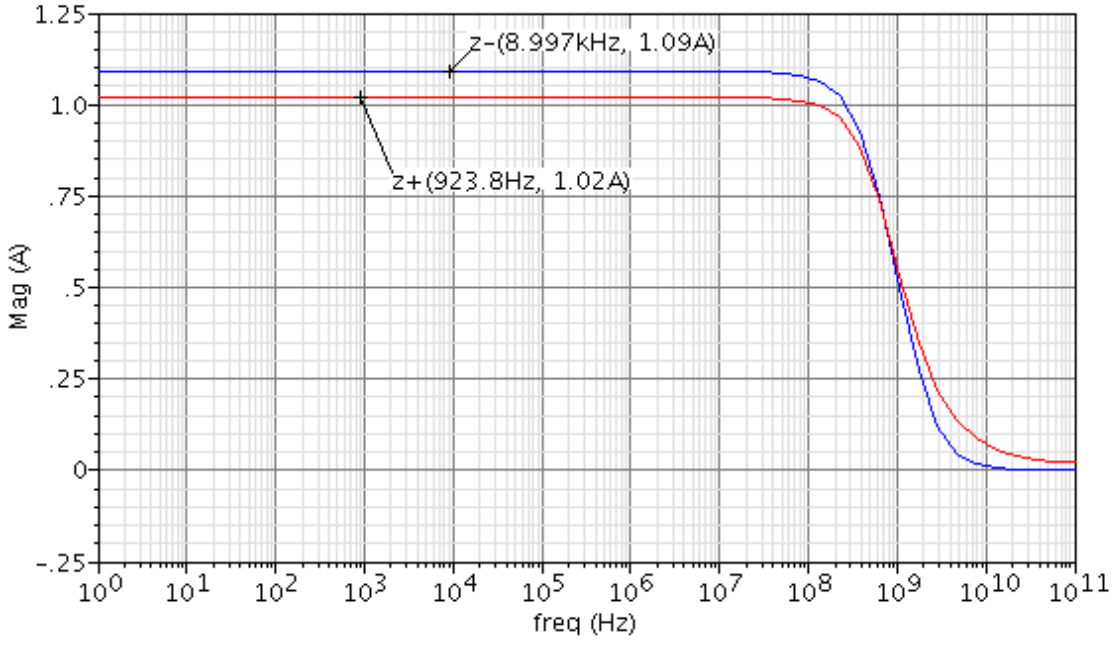


Figure 4.7 Frequency response of current gain at ports Z+ and Z-.

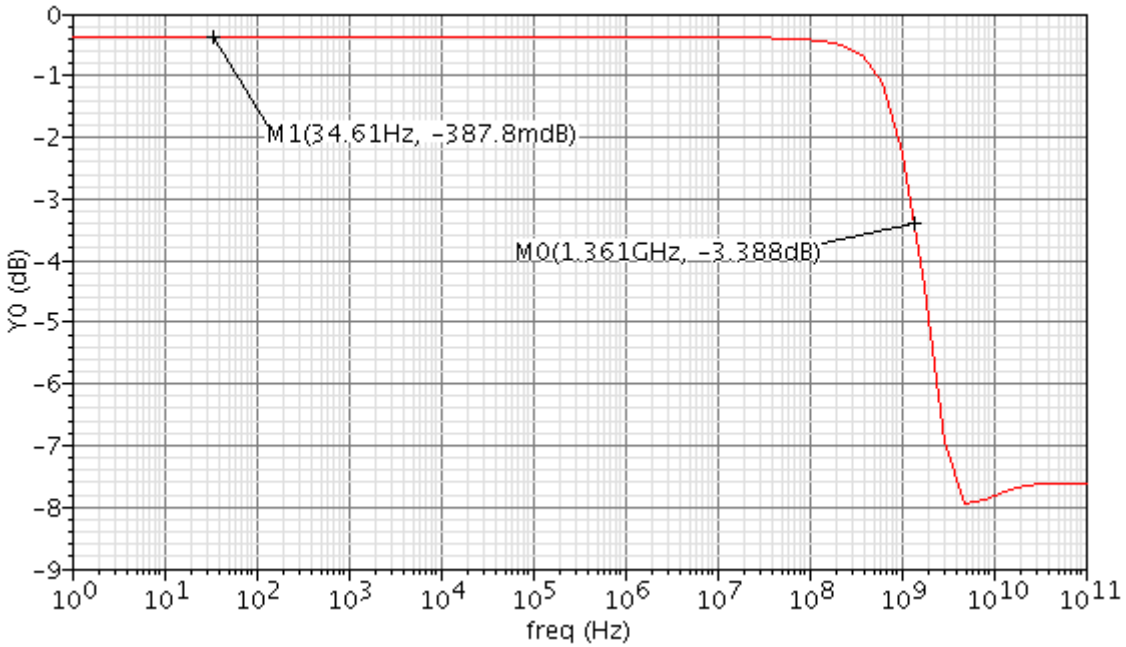


Figure 4.8 Frequency response of voltage transfer bandwidth at port X.

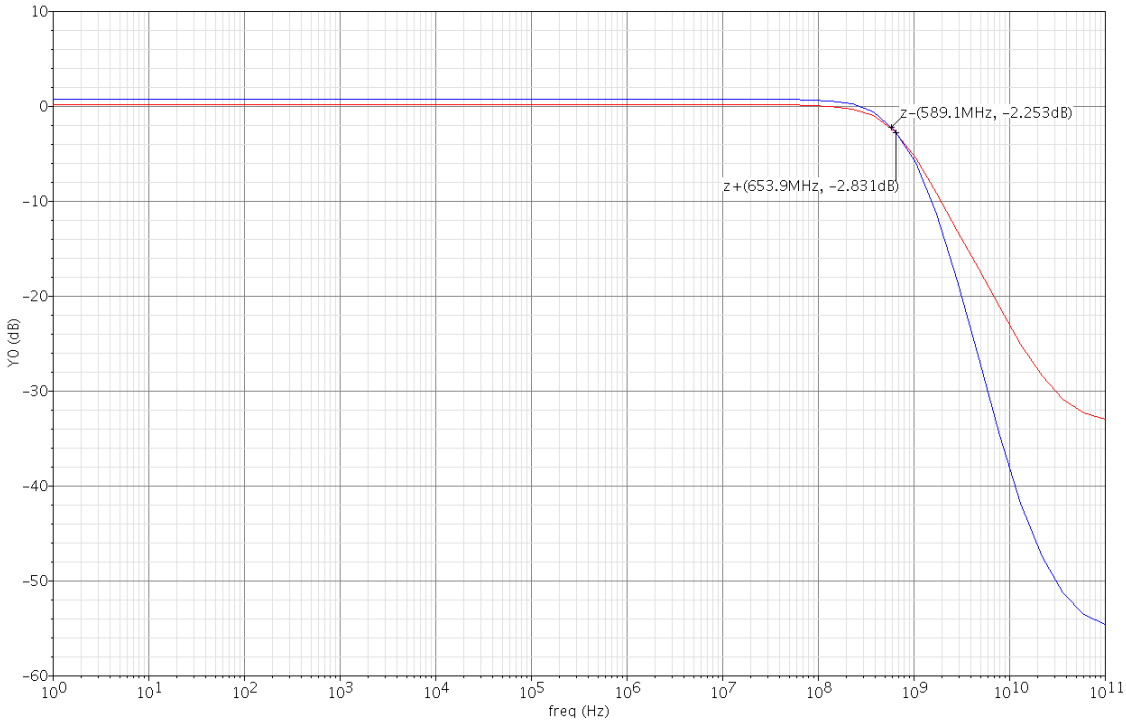


Figure 4.9 Frequency response of current transfer bandwidth at ports Z+ and Z-.

Figure 4.8 shows the frequency response of voltage transfer bandwidth at port X and from this it can be seen that its value comes out to be 1.361 GHz which is very high and make this CCII suitable for high frequency applications. The frequency response of current

transfer bandwidth at ports Z+ and Z- is shown in figure 4.9 and its value at the output ports Z+ and Z- comes out to be 653.9 MHz and 589.1 MHz respectively.

Table 4.1 shows the comparison of high performance CCII with other CCIIs proposed in the literature [5] and [17]. It can be seen that the CCII designed in this thesis work has lower supply voltage requirement as compared with others current conveyors reported in [5] and [17].

Table 4.1 Comparison of high performance CCII with different CCIIs proposed in [5] and [17].

PARAMETERS	**[5]**	**[17]**	**High Performance CCII**
Simulation Technology	0.35µm	0.35 µm AMS	0.35µm UMC
Supply Voltage	±2.5V	±2.5V	±1.5V
Bias Current	100 µA	100 µA	50µA
Current Gain, β	1.05	1.09	1.02
Voltage Gain, α	0.954	0.96	0.9563
Current B.W	960 MHz	1.58 GHz	653.9 MHz
Voltage B.W	1.5 GHz	6.506 GHz	1.361 GHz
Output Offset Voltage	-	19.93mV	10mV
Output Offset Current	-	17.5µA	3µA
Power Consumption	-	-	1.12 mW

From the table 4.1, it can be seen that high performance CCII has lower value of output offset current and voltage and also, the value of voltage and current gain of this CCII is comparable with the CCIIs reported in [5] and [17]. The current bandwidth of this CCII is somewhat lower because of low biasing current used in design specifications. It can be increased by increasing the biasing current but at the cost of higher power consumption.

4.2.4 SIMULATION RESULTS AT DIFFERENT PROCESS CORNERS

A process corner is an example of a design-of-experiments technique that refers to a variation of fabrication parameters used in applying an integrated circuit design to a semiconductor wafer.

Process corners represent the extremes of these parameter variations within which a circuit that has been etched onto the wafer must function correctly. If the circuit does not function at all or any of these process extremes, then the design is considered to have inadequate design margin. Therefore, the designer has to take into account these process corners while designing a circuit. If the circuit works well at all the process corners, then it will be sent to the foundary for the fabrication. Since the purpose of corners is to accept the extreme of extreme results, so one can define lowest supply voltage with highest temperature for slow-slow simulation and highest supply voltage with lowest temperature for fast-fast simulation.

The table 4.2 shows the different corners with particular temperature and supply value for the simulation of second generation current conveyor. There is $\pm$10% variation in supply voltage is taken into account i.e. $\pm$1.65V is used for FF corner and $\pm$1.35V is used for SS corner.

Table 4.2 Corners simulation table.

Corners	Supply voltage	Temperature
TT	±1.5V	27^{o}C
SS	±1.35V	80^{o}C
FF	±1.65V	-20^{o}C
SF	±1.5V	27^{o}C
FS	±1.5V	27^{o}C

The simulation results of CCII at different process corners and the simulation results of CCII with temperature and supply variations are listed in table 4.3 and table 4.4, respectively.

Table 4.3 Simulation results at different process corners.

Parameters	**TT**	**SS**	**FF**	**SF**	**FS**
Current Gain at Z+	1.0165	1.006	1.027	1.019	1.0158
Current Gain at Z-	1.083	1.055	1.109	1.0857	1.084
Voltage gain	0.956	0.957	0.955	0.957	0.954
-3 dB Voltage BW (GHz)	1.361	1.243	1.494	1.322	1.408
-3 dB Current BW at Z+ (MHz)	566.9	653.9	716	662.6	638.4
-3 dB Current BW at Z- (MHz	505.3	589.1	658.9	595.2	575.3
Power (mW)	1.12	1.24	1.38	1.21	1.33

Table 4.4 Simulation results with temperature and supply variations.

Parameters	**SS**	**FF**
Current Gain at Z+	0.994	1.044
Current Gain at Z-	1.024	1.149
Voltage Gain	0.948	0.958
Power (mW)	0.921	1.68

4.3 SIMULATION RESULTS OF THIRD GENERATION CURRENT CONVEYOR

The frequency response of the voltage gain of CCIII at port X is shown in figure 4.10 and its value comes out to be 0.956.

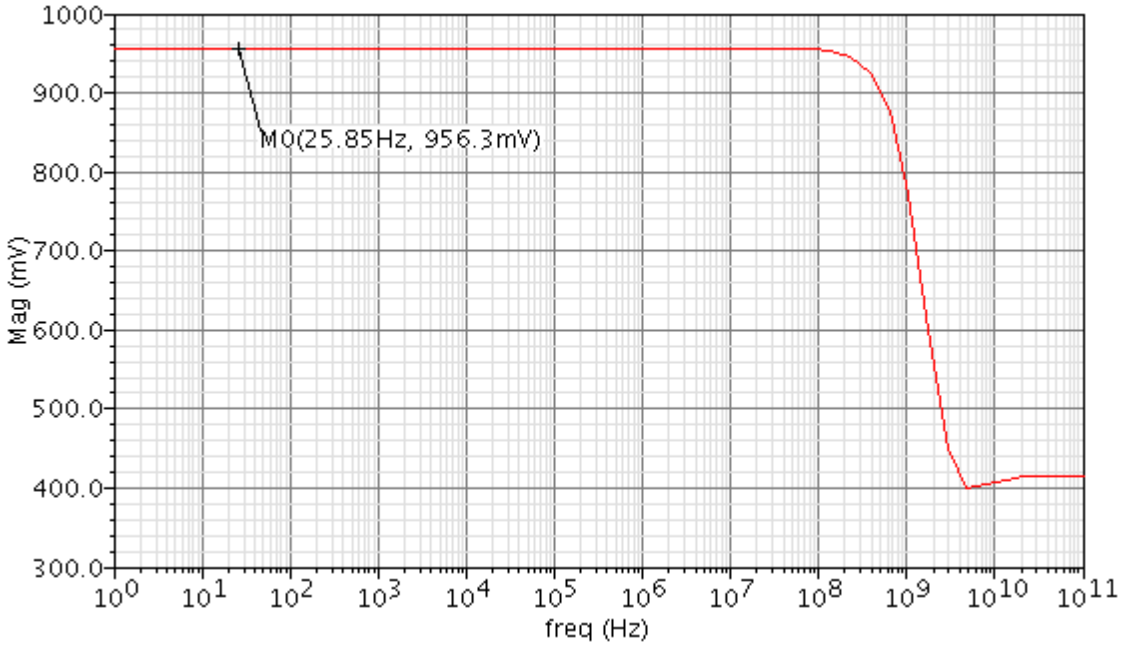


Figure 4.10 Frequency response of voltage gain at port X.

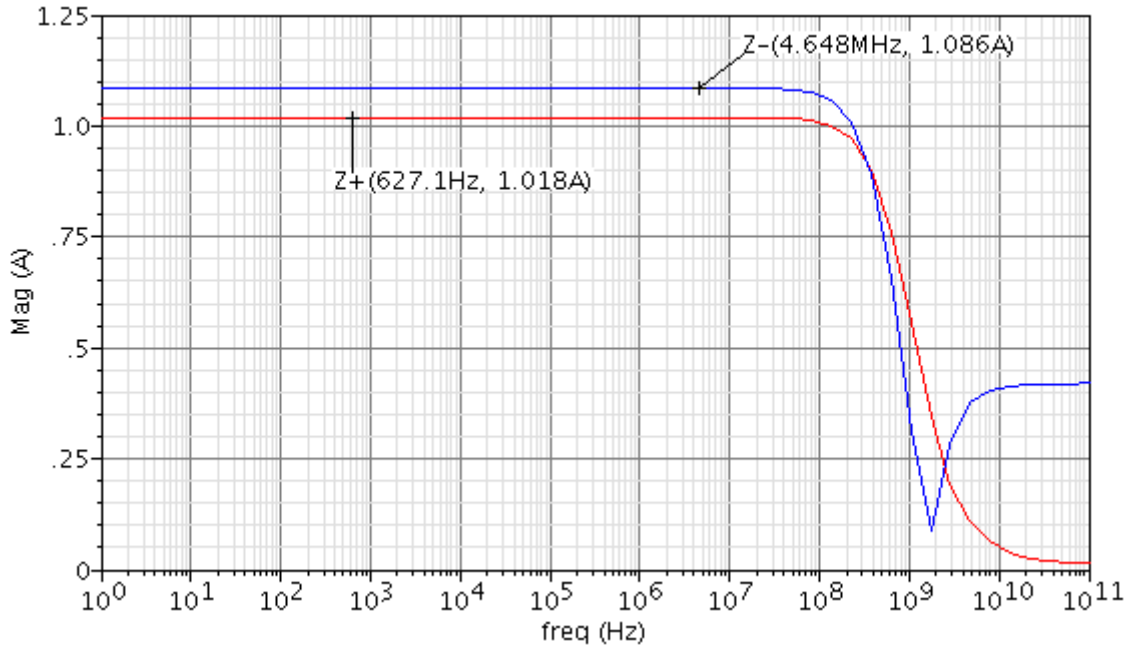


Figure 4.11 Frequency response of current gain at ports Z+ and Z-.

Figure 4.11 shows the frequency response of current gain at ports Z+ and Z-. It can be seen from this figure that the value of current gain at both the ports Z+ and Z- comes out be 1.018 and 1.086 respectively, which is greater than unity and meets with the desired specifications that were chosen for designing this circuit. This type of response validates the effectiveness of CCIII designed in this thesis work.

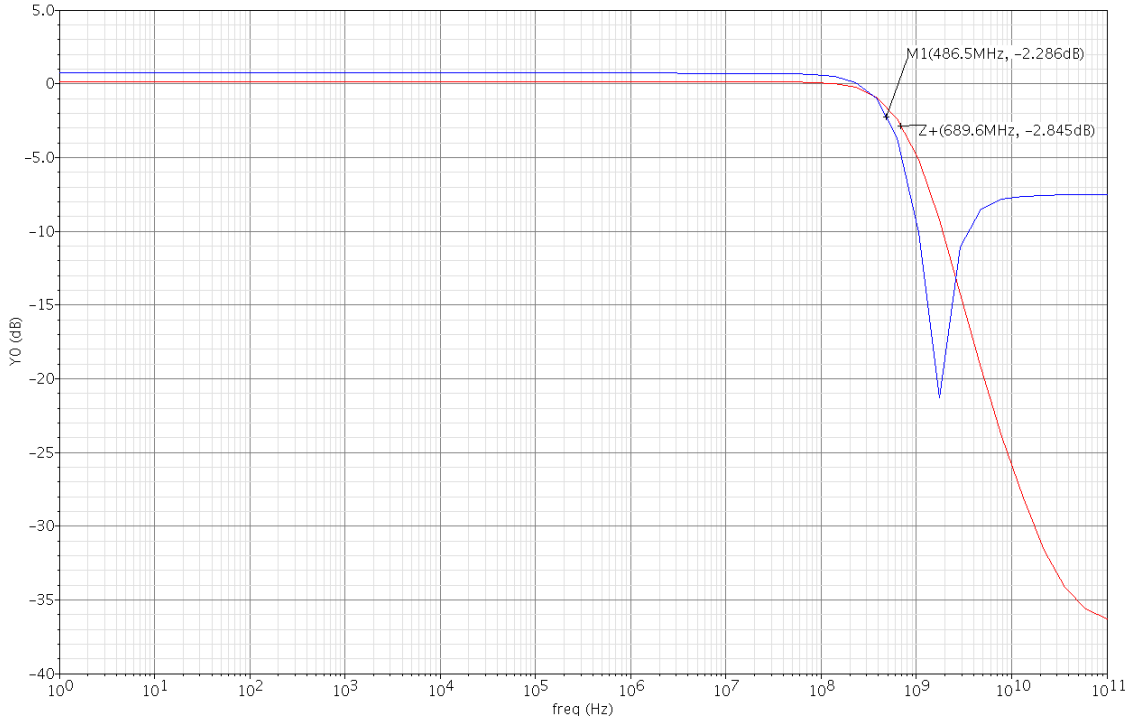


Figure 4.12 Frequency response of current transfer bandwidth at ports Z+ and Z-.

The frequency response of current transfer bandwidth at ports Z+ and Z- is shown in figure 4.12. It can be seen from this figure that the current transfer bandwidth at ports Z+ and Z- comes out to be 689.6 MHz and 486.5 MHz.

4.3.1 SIMULATION RESULTS AT DIFFERENT PROCESS CORNERS

The simulation results of CCIII at different process corners are listed in table 4.5 and table 4.6 lists the simulation results with temperature and supply variations.

Table 4.5 Simulation results at different process corners.

Parameters	**TT**	**SS**	**FF**	**SF**	**FS**
Current Gain at Z+	1.018	1.006	1.029	1.019	1.018
Current Gain at Z-	1.085	1.054	1.114	1.086	1.088
Voltage gain	0.956	0.957	0.955	0.957	0.954
Voltage B.W (GHz)	1.36	1.243	1.494	1.322	1.408

Current B.W at Z+ (MHz)	689.6	635.9	746.9	708.1	667.8
Current B.W at Z- (MHz)	486.5	438	538.6	495.2	476.4
Power (mW)	1.25	1.136	1.38	1.224	1.292

Table 4.6 Simulation results with temperature and supply variations.

Parameters	**SS**	**FF**
Current Gain at Z+	0.994	1.043
Current Gain at Z-	1.024	1.149
Voltage Gain	0.948	0.985
Power (mW)	0.930	1.682

CHAPTER 5

LAYOUTS OF CMOS CURRENT CONVEYORS

5.1 INTRODUCTION

This chapter describes the layout design of CMOS current conveyors. The physical layout design has been made in standard UMC 0.35µm CMOS 1P6M process technology. Cadence Virtuoso layout editor tool is used for the layout design and DRC, LVS and RCX have been performed by using Cadence Assura.

Design Rule Check (DRC) is performed in order to verify that layout fulfills all electrical and geometric rules provided by foundary and finally, LVS (Layout VS Schematic) is performed on the layout design to provide equivalence between the layout and schematic. This chapter is organized as follows: Section 5.2 describes the layout of CCII and in section 5.3, post-layout simulation results of CCII is discussed. Section 5.4 describes the layout of CCIII and section 5.5 discusses the post-layout simulation results of CCIII.

5.2 LAYOUT OF SECOND GENERATION CURRENT CONVEYOR (CCII)

The layout of the second generation current conveyor is shown in figure 5.1. Multifinger transistors are used in the layout design to minimize the source/ drain junction area and the gate resistance. The fingering of transistors also reduces the parasitic and thus improves the post simulation results. Thumb rule of fingering is that "the width of each finger is chosen such that the resistance of the finger is less than the inverse transconductance associated with the finger [19].

Process variations during fabrication may limit the accuracy and may limit desired performance of analog circuits. Matching between the components of analog circuits is an important issue in many designs such as current mirrors and differential pairs. As the current mirrors are the core components of current conveyors, so Interdigitization

technique is used while drawing the layout of CCII in order to reduce the first order gradient effects and thus provide accurate mirroring of current.

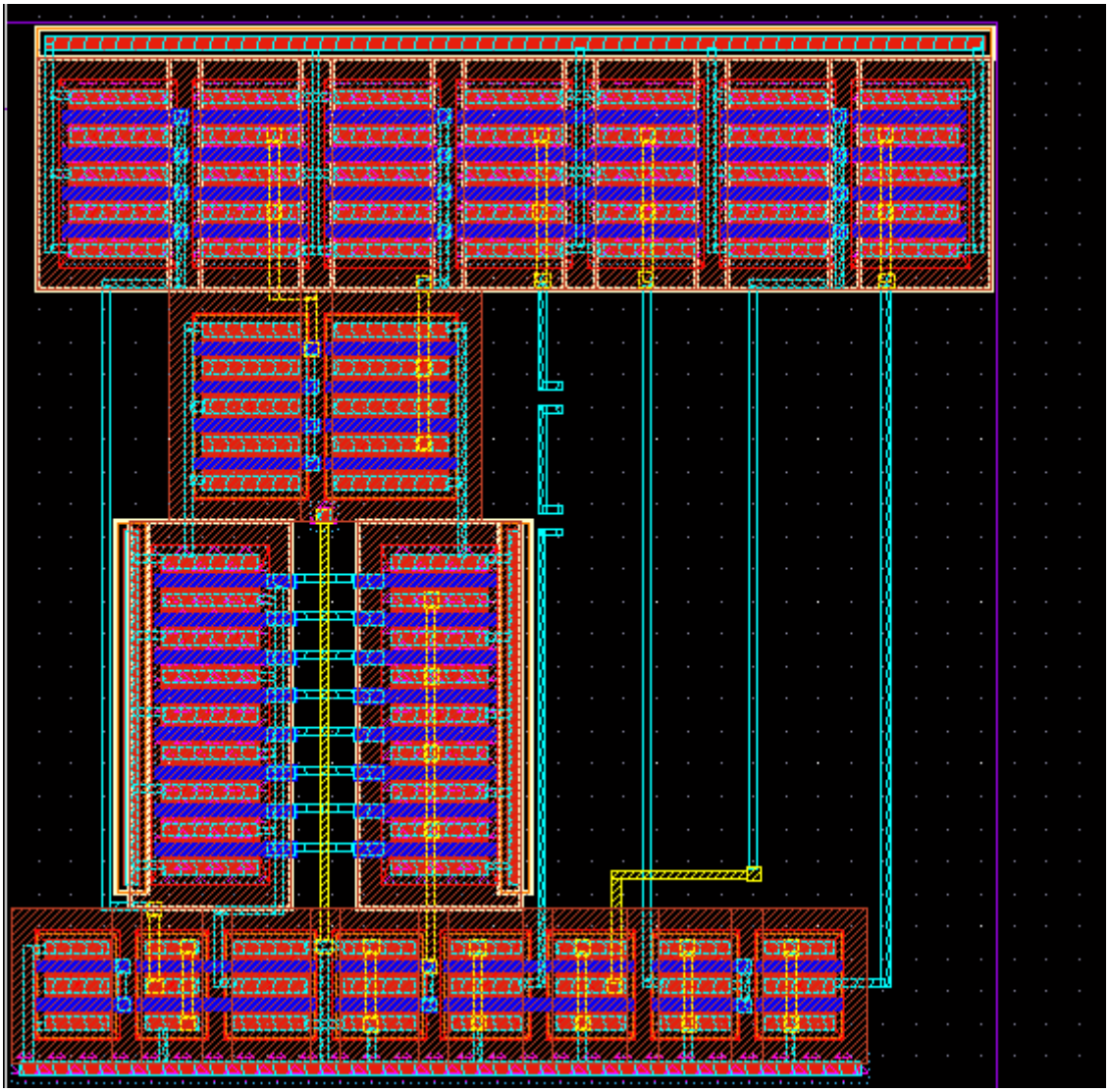


Figure 5.1 Layout of Second Generation Current Conveyor.

Interdigitization technique not only avoids the process variations but also reduces area and parasitic capacitances at various nodes. In order to remove the IR drop, long metal wires with proper widths are used in the layout design. The RC extracted view of CCII is shown in figure 5.2 .The basic design rules are summarized below:

Metal 1 to metal 1 spacing	0.24 µm
Minimum contact size	0.24 µm*0.24 µm
Poly to poly spacing	0.24 µm
Poly to metal spacing	0.28/0.00 µm
Contact overlap to p+ diffusion	0.1 µm

Metal 1 width	0.24 µm
Poly extension beyond active	0.22 µm
Minimum contact spacing	0.26 µm
N well overlap p+ diffusion	0.43 µm
Diffusion contact to poly spacing	0.15 µm
Minimum p+ implant overlap p+ diffusion	0.22 µm
Poly width	0.18 µm
Minimum poly extension on to field region	0.22 µm
Poly contact to diffusion edge spacing	0.18 µm
Minimum poly overlap contact	0.1 µm
Minimum metal area	0.1764 µm*µm
Minimum metal2 width	0.28 µm
Metal1 and metal2 overlap over via	0.08 µm
Minimum equal potential N-well spacing	0 µm or >=0.9 µm
Minimum non equal potential 1.8 V N well spacing	2µm

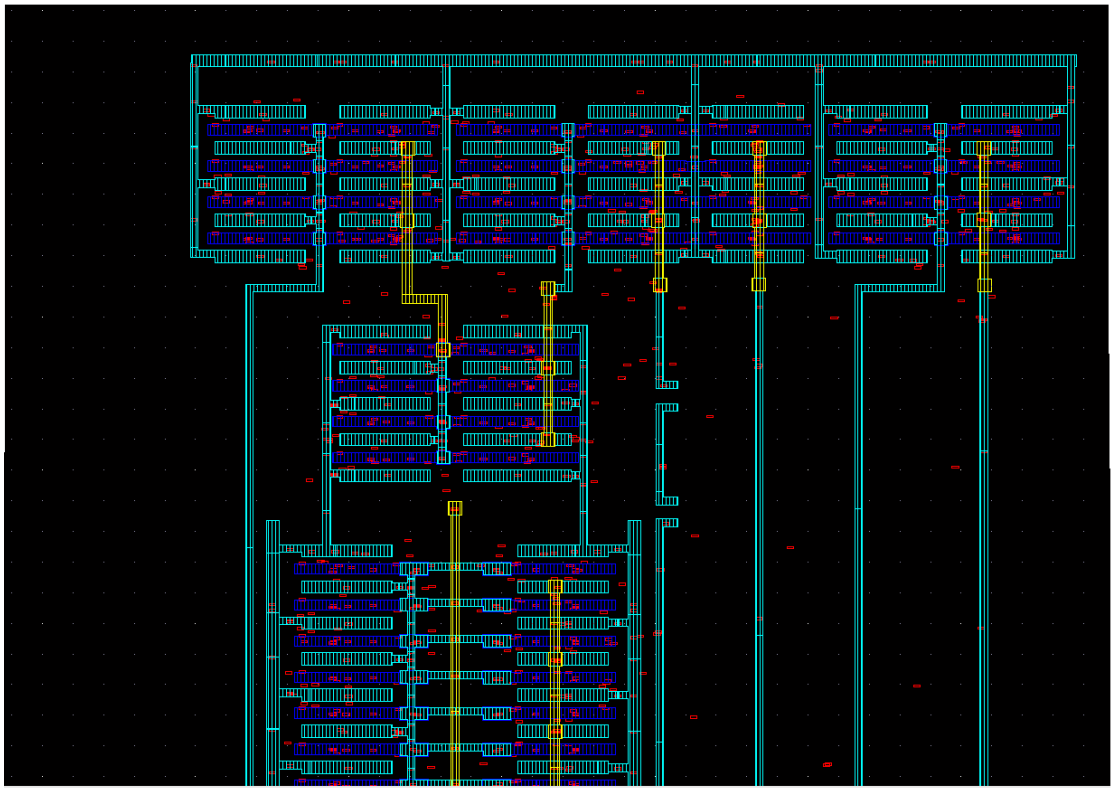


Figure 5.2 RC extracted view of CCII.

5.3 POST-LAYOUT SIMULATION RESULTS OF CCII

The frequency response of current gain at ports Z+ and Z- of CCII obtained after post layout simulation is shown in figure 5.3. The value of current gain at ports Z+ and Z- comes out to be 1.02 and 1.09 respectively

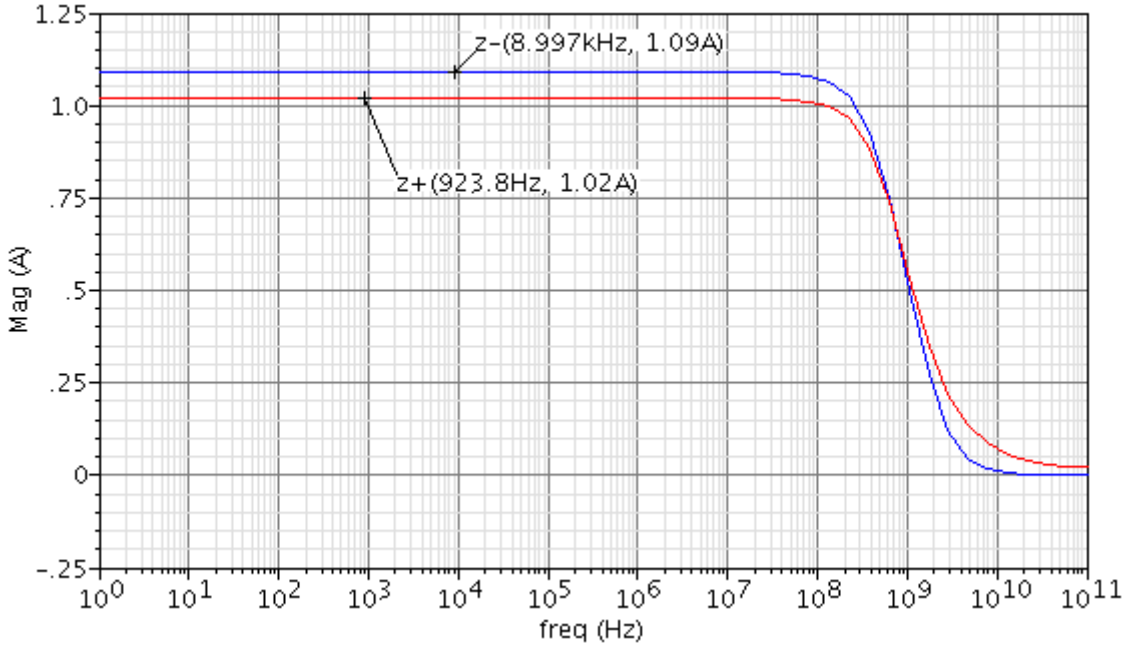


Figure 5.3 Frequency response of current gain at ports Z+ and Z-.

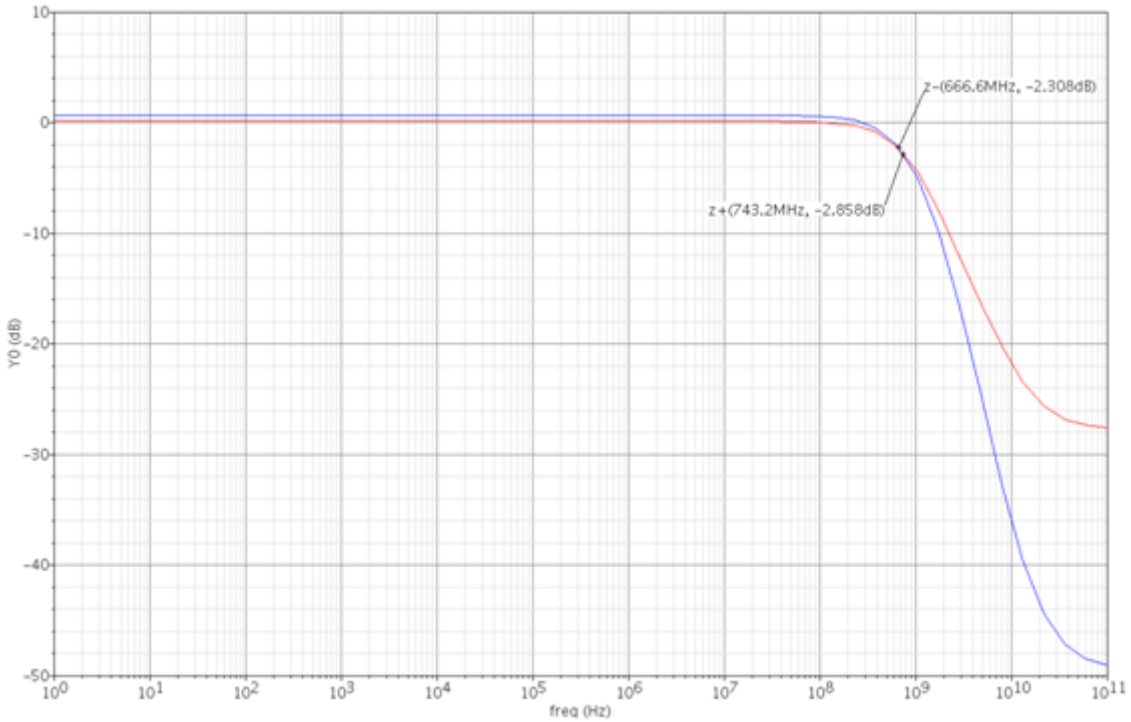


Figure 5.4 Frequency response of current transfer bandwidth at ports Z+ and Z-.

Figure 5.4 shows the frequency response of current transfer bandwidth at ports Z+ and Z- of CCII obtained after post-layout simulation. The current transfer bandwidth at ports Z+ and Z- comes out to be 743.2 MHz and 666.6 MHz respectively.

The post-layout simulation results of CCII at different process corners and the post-layout simulation results of CCII with temperature and supply variations are listed in table 5.1 and table 5.2, respectively.

Table 5.1 Post-layout simulation results at different process corners.

Parameters	**TT**	**SS**	**FF**	**SF**	**FS**
Current Gain at Z+	1.02	1.01	1.03	1.02	1.01
Current Gain at Z-	1.089	1.062	1.117	1.093	1.091
Voltage gain	0.9562	0.9568	0.9556	0.957	0.9539
Voltage B.W (GHz)	1.423	1.325	1.694	1.567	1.546
Current B.W at Z+ (MHz)	743.2	664.9	819.8	754	723.3
Current B.W at Z- (MHz	666.6	580.6	726.8	670.4	644.3
Power (mW)	1.231	1.106	1.362	1.19	1.273

Table 5.2 Post-layout simulation results with temperature and supply variations.

Parameters	**SS**	**FF**
Current Gain at Z+	0.992	1.039
Current Gain at Z-	1.0191	1.1415
Voltage Gain	0.9469	0.958
Power (mW)	0.9117	1.654

5.4 LAYOUT OF THIRD GENERATION CURRENT CONVEYOR (CCIII)

The layout of third generation current conveyor is shown in figure 5.5. The layout design techniques that are applied to the layout of second generation current conveyor are also applied to the layout design of third generation current conveyor.

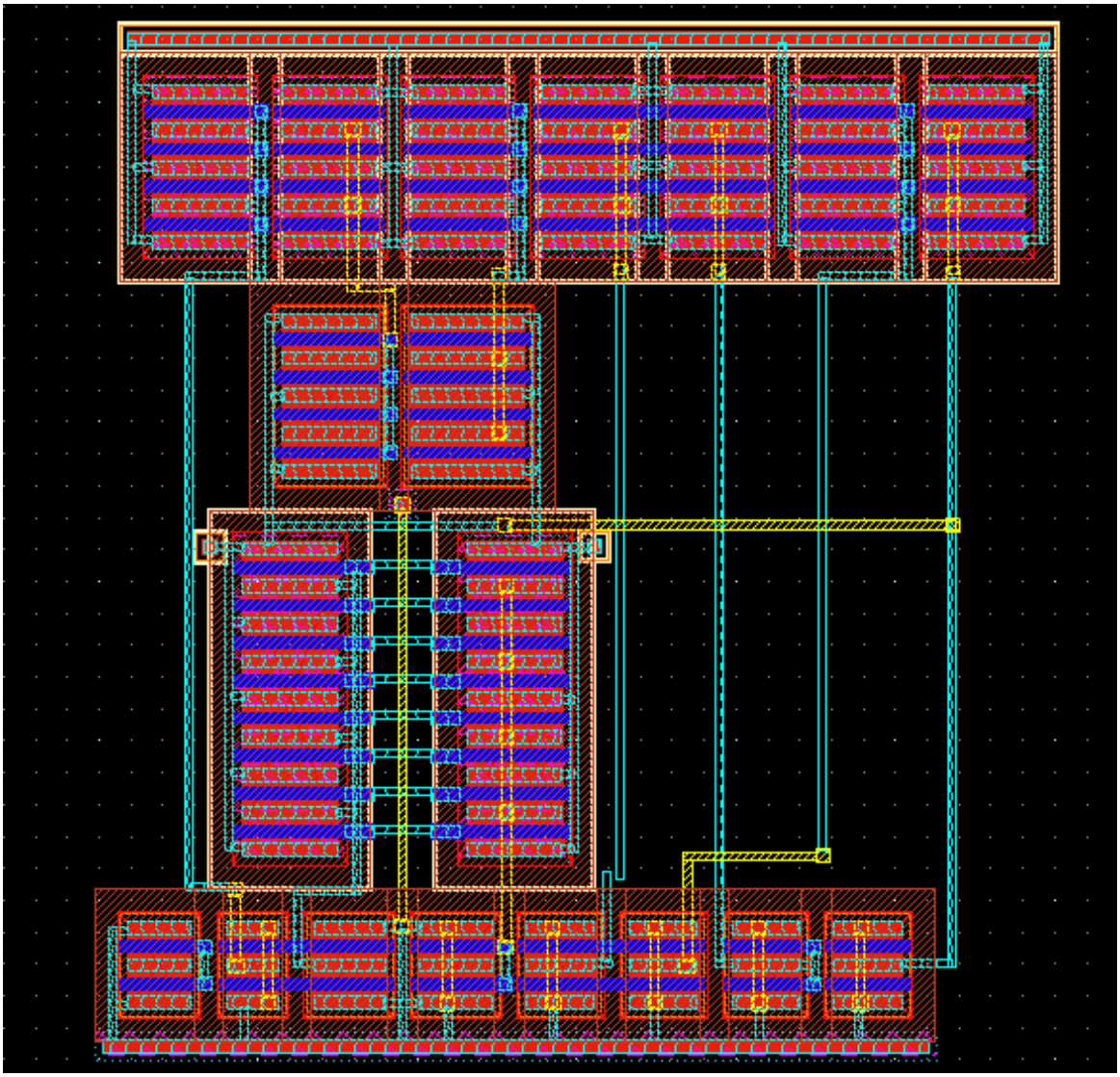


Figure 5.5 Layout of Third Generation Current Conveyor.

The layout design is verified with the DRC and LVS steps and then RCX (Resistance and Capacitance Extraction) is done in order to generate the RC extracted view. The RCX is done in order to figure out the various parasitic that are created during layout design. These parasitic affect the post simulations results so various layout techniques such as interdigitization is used in the layout design in order to minimize these parasitic. The RC extracted view of CCIII is shown in figure 5.6.

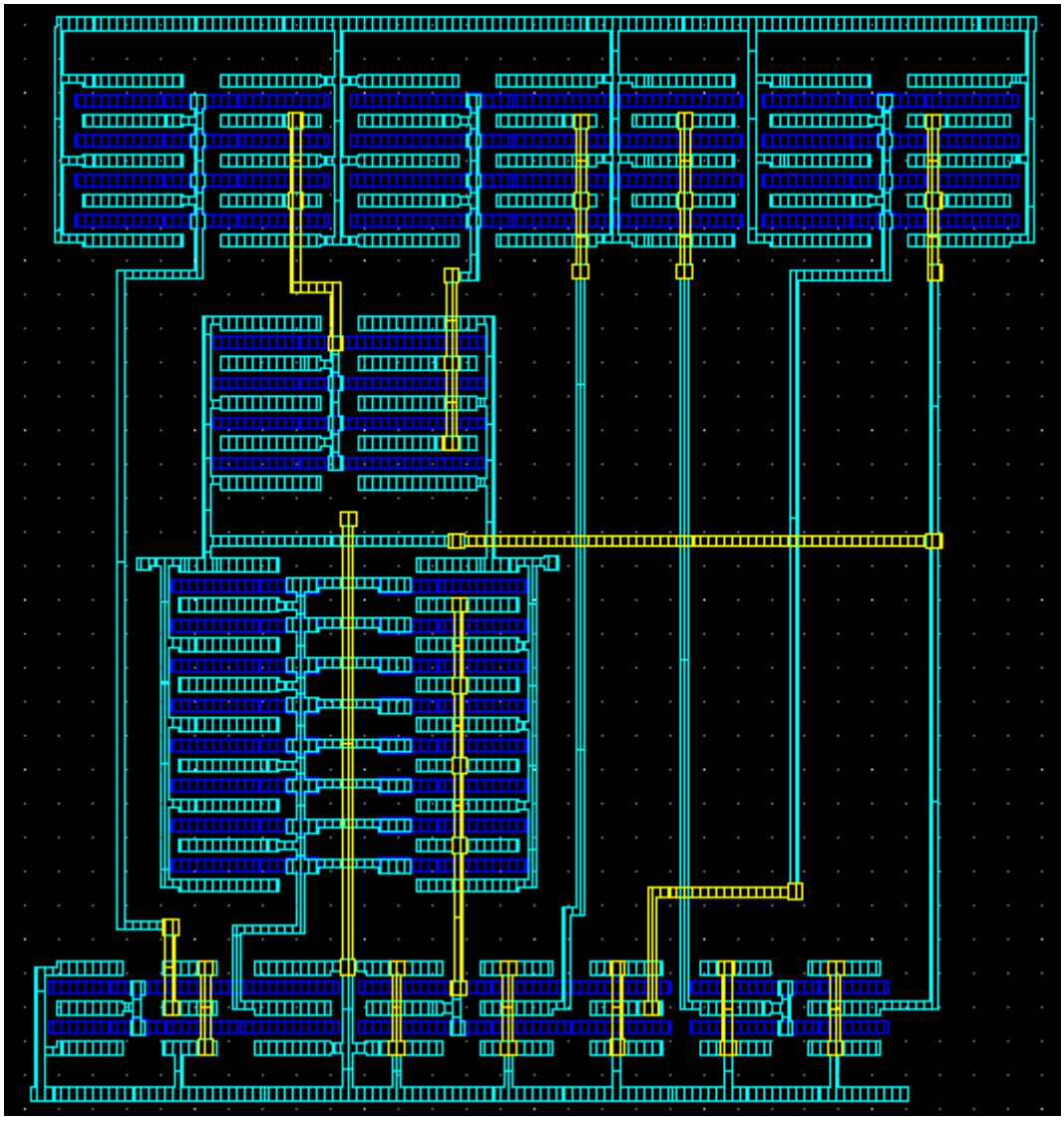


Figure 5.6 RC extracted view of CCIII.

5.5 POST-LAYOUT SIMULATION RESULTS OF CCIII

The frequency response of current gain at port Z+ and Z- of CCIII obtained after post layout is shown in figure 5.7. From this figure it can be easily seen that the value of current gain at ports Z+ and Z- comes out to be 1.018 and 1.086.

Similarly, figure 5.8 shows the frequency response of current transfer bandwidth of CCII after post-layout simulation. The value of this current bandwidth at ports Z+ and Z- comes out to be 758.6 MHz and 521.8 MHz respectively. Due to parasitic capacitance and resistance formation in the layout, there is change in the value of parameters obtained after post-layout simulation.

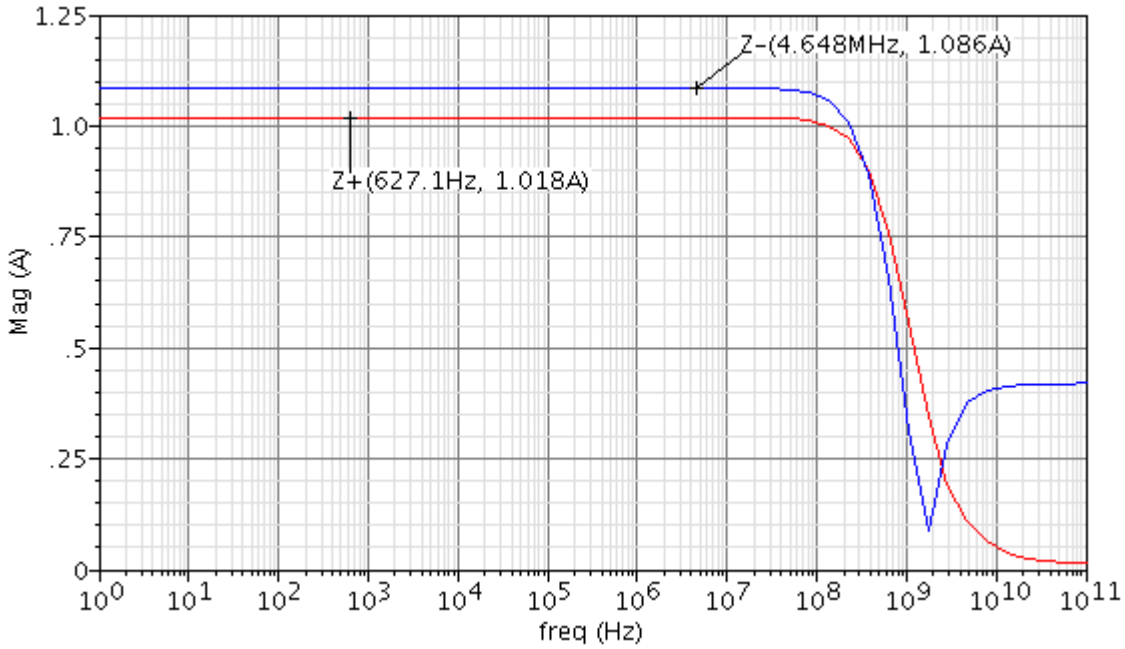


Figure 5.7 Frequency response of current gain at ports Z+ and Z-.

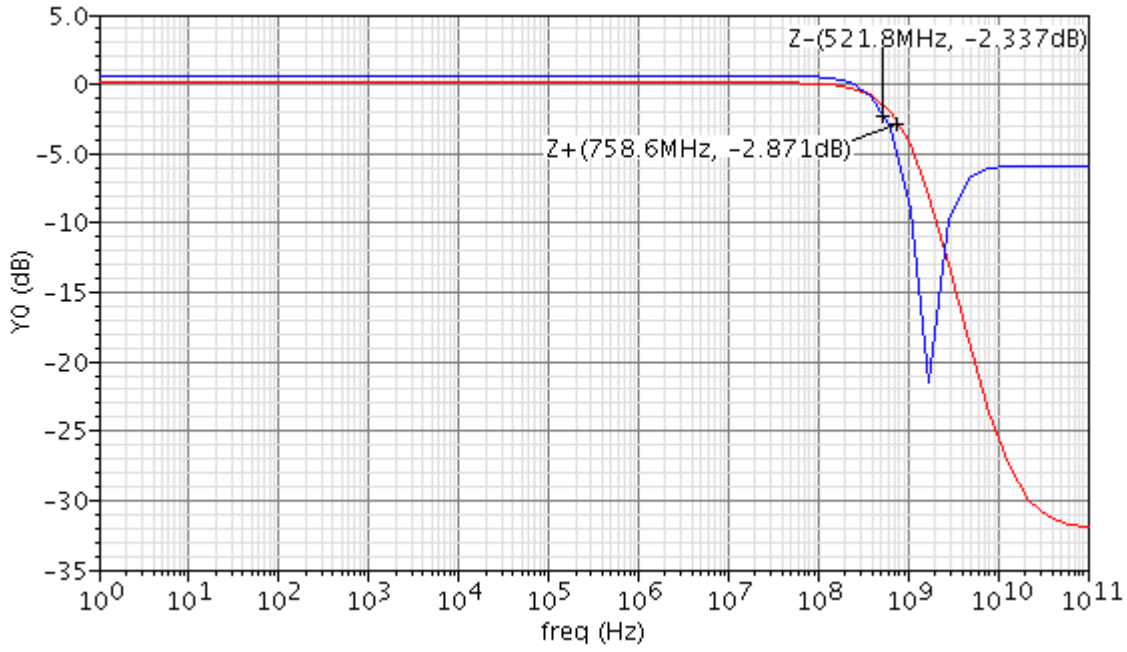


Figure 5.8 Frequency response of current transfer bandwidth at ports Z+ and Z-.

The post-layout simulation results of CCIII at different process corners and the post-layout simulation results of CCIII with temperature and supply variations are listed in table 5.3 and table 5.4, respectively.

Table 5.3 Post-layout simulation results at different process corners.

Parameters	**TT**	**SS**	**FF**	**SF**	**FS**
Current Gain at Z+	1.014	1.003	1.026	1.016	1.015
Current Gain at Z-	1.079	1.048	1.108	1.079	1.082
Voltage gain	0.9562	0.9568	0.9556	0.957	0.9539
Voltage B.W (GHz)	1.423	1.325	1.694	1.567	1.546
Current B.W at Z+ (MHz)	758.6	697.6	824.1	780.7	733
Current BW at Z- (MHz	521.8	466.6	588.2	531.8	510.6
Power (mW)	1.241	1.123	1.362	1.208	1.275

Table 5.4 Post-layout simulation results with temperature and supply variations.

Parameters	**SS**	**FF**
Current Gain at Z+	0.992	1.039
Current Gain at Z-	1.019	1.142
Voltage Gain	0.946	0.958
Power (mW)	0.921	1.654

CHAPTER 6

CONCLUSIONS AND FUTURE SCOPE

6.1 CONCLUSIONS

In this thesis, CMOS Current Conveyors for high frequency applications have been presented. Two current conveyors, namely, Second Generation Current Conveyor (CCII) and Third Generation Current Conveyor (CCIII) have been analyzed and designed using UMC 0.35μm CMOS technology process parameters. The simulation results and layouts have been presented to demonstrate the feasibility of the circuits.

The design of second generation current conveyor provides a voltage gain of 0.956 and current gain of 1.02. For a biasing current of 50μA, the circuit provides the voltage and current bandwidth of 1.361 GHz and 653.9 MHz respectively, hence this circuit can be used for high frequency applications. The excellent current following action is also achieved from input port to the output port.

The design of third generation current conveyor provides a voltage gain of 0.9562 and current gain of 1.018. For a biasing current of 50 μA, the circuit provides voltage and current bandwidth of 1.36 GHz and 689.6 MHz respectively. Multiple fingers transistors are used in the layout design in order to reduce the parasitic and to provide good post-layout simulation results.

6.2 FUTURE SCOPE

The main feature of the present work is its high voltage and current transfer bandwidth, so this work can be extended to the design of filters that operate at high frequencies in the microwave range. Also, CCII is the most versatile analog building block in current mode approach so various active blocks such as current integrator, current differentiator, tuneable active filters and multipliers can be made by suitable connection of two or more CCIIs. But still there is a requirement to further improve the present work.

- Simulation results show that the current conveyors have current transfer bandwidth greater than 600 MHz. This bandwidth can be further increased by using the bandwidth enhancement techniques.
- The static power dissipation of the circuits can be reduced by selecting low biasing currents.
- The present work is designed at a supply voltage of ±1.5V in order to have satisfactory dc voltage following action. If the simple current mirrors are replaced by low voltage FGMOS current mirrors then the present work can be designed at low supply voltages with low biasing currents and static power dissipation is also low in this case.
- The output offset current errors are strongly dependent on the matching accuracy of the current mirrors. This offset can be minimized by matching the current mirrors by careful layout techniques like common centroid and unit cell layout techniques.

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