Modelingof Drain Current for Lightly Doped Symmetrical Double Gate MOSFETIncluding Short Channel Effects

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June, 2014

CANDIDATE DECLARATION

I do hereby declare that the work presented in this dissertation entitled "**Modeling of Drain Current for Lightly Doped Symmetrical Double Gate MOSFET Including Short Channel Effects**", submitted in the partial fulfillment of the degree of Masters of Technology (VLSI Design), at the Electronics and Communication Department of Thapar University, Patiala, is an authentic record of my original work carried out under the guidance of **Mr. Arun Kumar Chatterjee, Assistant Professor, ECED** due acknowledgements have been made in the text of the thesis to all other material used. This thesis work was done in full compliance with the requirements and constraints of the prescribed curriculum and has not been submitted in any other University/Institute for the award of any other degree.

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ABSTRACT

Symmetrical double gate has become one of the preferable choices for scaling CMOS devices down to nanometer size as they have excellent control over short channel effects and provide lower gate leakage current, higher on-current and better subthreshold slope reduction. Several analytical surface potential and charge based drain current models has been proposed earlier for DG MOSFETs but the development of anappropriate analytical drain current model for nano-MOSFETs is still under research.

In this thesis, a drain current model for lightly doped symmetrical DG MOSFET in sub-nanometer regime is presented by considering weak and strong inversion regions including short channel effects, series source/drain resistance and channel length modulation parameters. This two dimensional-potential-distribution based drain current model alsoincludes the effects of subthreshold slope and threshold voltagevariations. Lastly the effect of the fixed oxide trap charges on the drain current has been studied and evaluated.

Further, for 32 nm and 45 nm technologies the current-voltage characteristics of drain current model for DG-MOSET are compared and validated with the simulation resultsforall regions of its operation and SILVACO (Atlas) TCAD tool is used for simulation.The series source/drain resistance effect has also been studied in C-V characteristics. From the above results it is found that the model and the simulation results are in good agreementfor devices having channel length to silicon film thickness ratio greater than or equal to 2. Subthreshold slope and threshold voltage models are also compared with simulation results at different channel lengths and silicon film thickness.Finally, the fixed-oxide trap charge effect on drain current for different gate voltages shows remarkable agreement for large range of its value but starts showing deviation with the simulation results at its very high values.

ACRONYMS

MOS	Metal Oxide Semiconductor
MOSFET	Metal-Oxide-Semiconductor Field Effect Transistor
SOI	Silicon-On-Insulator
UTB	Ultra-Thin Body
DG MOSFET	Double Gate MOSFET
SCE	Short Channel Effect
CMOS	Complementary MOS
ITRS	International Technology Roadmap for Semiconductors
GIDL	Gate-Induced Drain Leakage
DIBL	Drain-Induced Barrier Lowering
SS	Subthreshold Slope
BJT	Bipolar Junction Transistor
PD-SOI	Partially Depleted SOI
FD-SOI	Fully Depleted SOI

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Chapter 1

1 Introduction

1.1 MOSFETsscalingand Moore's Law

Moore's law stated in 1965 helped advancement of integrated circuit technology over the past years andallowed the doubling ofIC's complexity every two years byincreasingthe chip's transistor count[1] by continuous scaling of metal-oxide-semiconductor field-effect transistor (MOSFET) to smaller physical dimensions. The advantages of MOSFET dimensions scaling are cost reduction by increasing number of chips obtained per wafer, power supply scaling which decreasedpower consumption, faster circuits obtained due to reduced capacitive delay which also enabled more functions per unit area of silicon. Thus, denser silicon integrated circuits (ICs) can be realized, resulting in incredible reductions of cost per-function with enhanced performance as shown inFigure 1-1 andFigure 1-2.

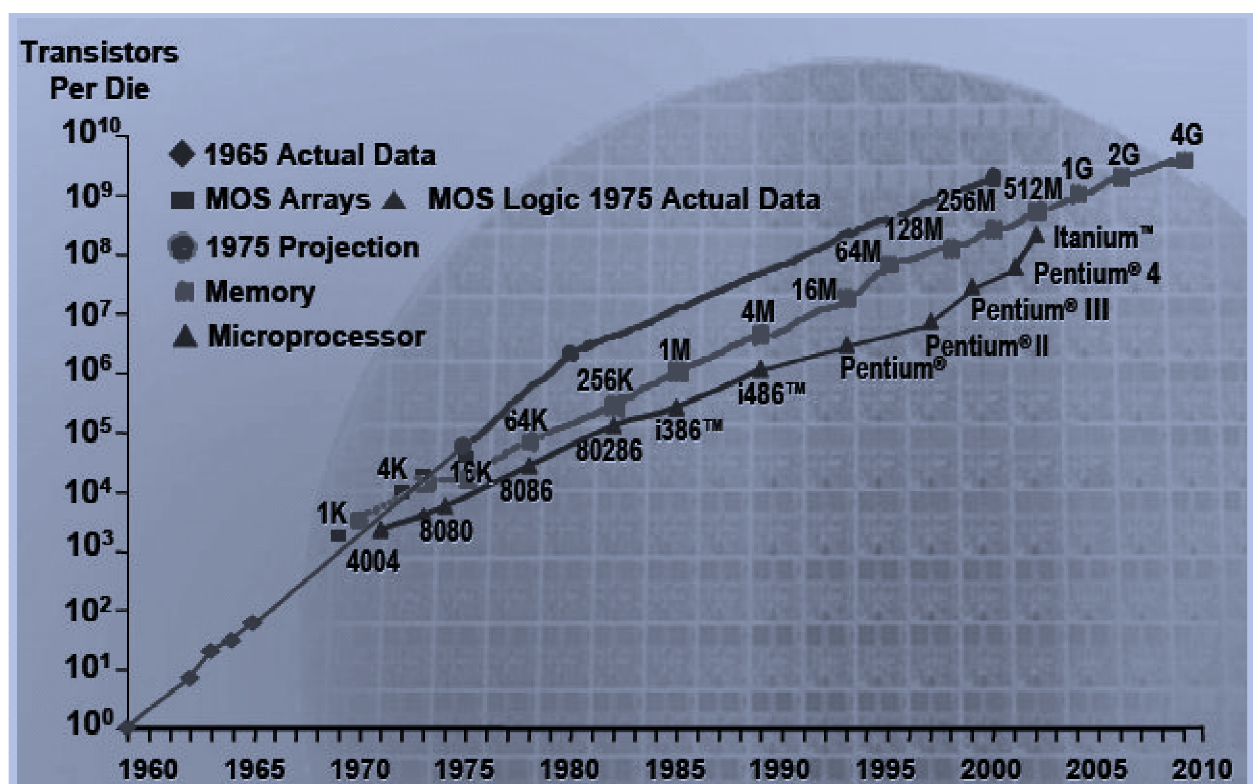

Figure 1-1: Number of transistors on a die in accordance with the first year of production[2].

International technology roadmap for semiconductor(ITRS) was born by an initiative to precisely predict the future of the semiconductor industry by a team of semiconductor companies and academia since early 1990's. An early report is issued by the ITRS serves as a benchmark for semiconductor industry. These reports describe thetechnology, design and meteorology tools andequipment that have to be developed in order to keep the semiconductor industry growth exponential as predicted by Moore's law.

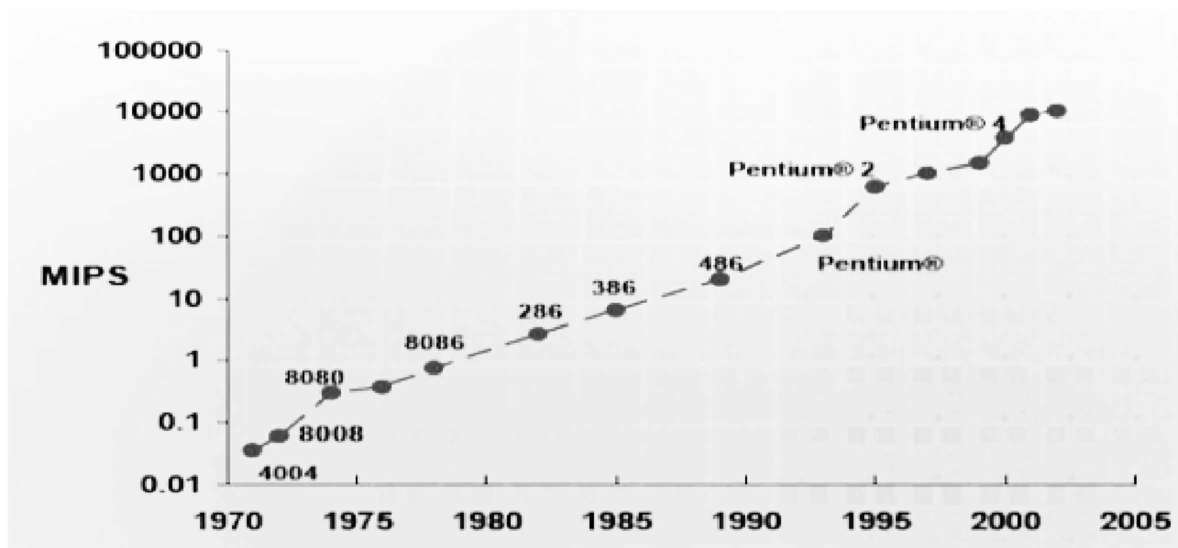

Figure 1-2: Increase in chip performance in terms of millions of instructions persecond (MIPS) with scaling over years[2]

1.2 Bulk Si-MOSFET scaling challenges

The basic building blocks of Integrated circuits areMOSFETs. The conventional planar bulk MOSFET is shown inFigure 1-3. The decrease in the gate length (L) of a MOSFET reduces its capacitive control on the channel potential and thus on the flow of current along the channel increasing the capacitive coupling of the channel potential to the source and drain terminals due to small separation between the source and drain regions, resulting in several undesirable effects called as short channel effects (SCE) such as threshold voltage (V_{th})roll-off and drain- induced barrier lowering (DIBL) which manifest into increased off-state transistor leakage(I_{off}). Static power consumption of the device due toI_{off} severely affects high-performance logic technologies and CMOS scaling [2].

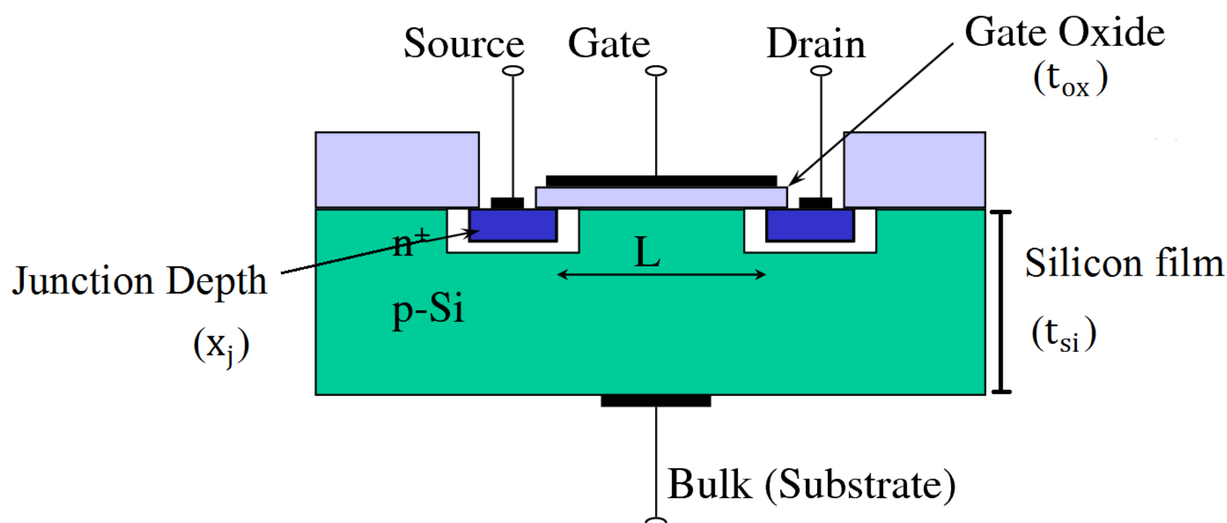

Figure 1-3: Conventional bulk n-type MOSFET

SCE of conventional bulk MOSFETcan be reduced through scaling of vertical device dimensions such as the gate dielectric thickness (t_{ox}),junction depth of source and drain regions(x_j) and depletion depth of channel (x_{dep}) along with channel length (L).

For t_{ox} (<2nm) severe gate leakage current flows through the silicon dioxidebased gate dielectric because of quantum mechanical tunnelling[3]. Thus, higher permittivity gate dielectric materials known as high-k gate dielectrics are used to further reduce the equivalent oxide thickness (EOT) with a physicallythick dielectric to suppress gate leakage current. However, many fabrication challenges are still involved in this technology such as optimizing interfacial layer to improve carrier mobility degradation [4].

To scale down x_{dep} channel doping concentration is increased, makingV_{th} high due to increased channel potential relative to the source, high channel doping also eliminates current leakage paths far away from the oxide interface reducing off-current but it increases vertical electrical field and scattering due to presence of dopant atomscausing reduction of mobility of carriers.Gate-induced drain leakage (GIDL) and the reverse-biased drain junction band-to-band tunnelling increases by high doping andnon-uniformityof channel dopants cause'sV_{th}variations[5].

Shallow source and drain junctions x_j,decrease the coupling of the source/drain to the channel thereby reducing the junction capacitance. But it increases theunwantedseries resistance, reducing the on-state drive current. Source and drain regions are raised to reduce parasitic series resistance by shallow junctions. Ultra shallow junctions are limited by fabrication difficulties for minimization of dopant diffusion.

1.3 Advanced MOSFET structures

In nanometre regime traditional scaling of bulk MOSFETs has reached its practical limits. Thus, silicon-on-insulator technology based advanced MOSFET structures such as ultra-thin-body (UTB) and double-gate (DG) MOSFETs are used to overcome these scaling challenges. Thus, special gate structures are used to eliminate the encroachment of the drain electric field lines into the channel as shown inFigure 1-4, these devices are Double gate transistor, Triple gate devices, FINFET, Delta-channel SOI MOSFET, Gate all-around device etc. These devices has shown tremendous improvement in SCE and give high drive current as they have more than one inversion layer for current conduction.

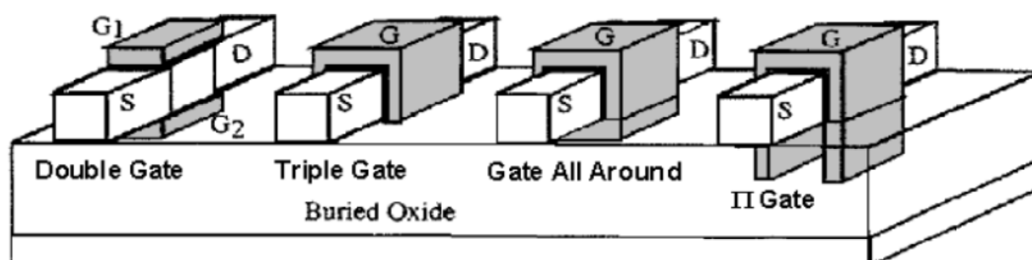

Figure 1-4: FD SOI Devices with Multiple gates [6]

Advanced MOSFETs manufacturing is still challenging. Due to the process complexity many different proposed methods to fabricate these devices are unemployable. FINFET gives relaxation tot_{si}constraints by utilizing the top surface of fin as a channel and easily implementing a third gate[7]. It is the most manufacturable advanced MOSFETs structure due to self-aligned gate electrodes compatible with conventional planar bulk CMOS process.

1.4 Short Channel Effects

When the channel length of a MOS transistor becomes comparable to the Source/Drain depletion width the MOSFET is known as short channel device [8].In scaling the terminal voltages are also scaled down to reduce power consumption but voltage scaling is not reduced in proportion to other device geometrical dimension. The device threshold voltage is scaled in proportion to the supply voltage scaling to have high on current and performance. This threshold voltage scaling and small device dimensions leads toadverse SCEs increasingthe device leakage currents.

1.4.1 Subthreshold Leakage

Subthreshold or weak inversion region of a transistoroccurs before the formation of the inversion layer at the gate voltages below the threshold voltage when the minority carrier concentration in the channel is small for significant current conduction but is not zero and thus, a small amount of current flows betweensource and drain in this region[8]. This current variation with gate voltage below threshold is shown as the linear region of the semi-log plot of the transfer curve in Figure 1-5. The current is plotted on a logarithmic scaleso that even the small exponentially dependdiffusion current, can be clearly indicated.

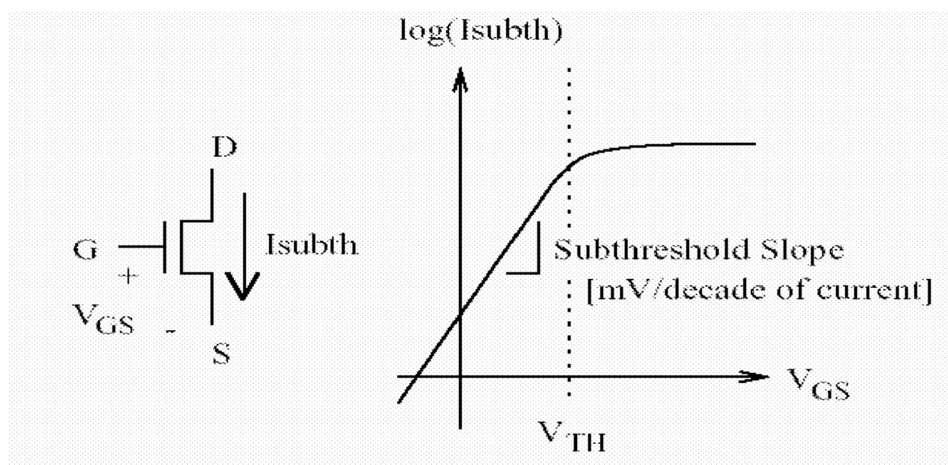

Figure 1-5: Semi-log Subthreshold leakage plot in n-channel metal–oxide–semiconductor (NMOS) transistor[9]

The channel formation through minority carriers in weak inversion region in n-channel MOSFET is shown in Figure 1-6. The subthreshold current occurs due to diffusion of these minority carriers along the channel unlike strong inversion where drift current dominates. The weak inversion drain current equation is defined as[10]

$$I_D = \mu_0 C_{ox} \frac{W}{L} (V_T)^2 e^{1.8} e^{(V_g - V_{th}/nV_T)} \left(1 - e^{-V_d/V_T}\right)$$

Where, μ_0 is the zero bias mobility, C_{ox} is the gate oxide capacitance , W is the width of the device, L is the length of the device, $V_T$is the thermal voltage whose value is given as $V_T = {}^{KT}/_{q}$, n is thesubthreshol swing coefficient $V_g$is the applied gate voltage , $V_{th}$is the threshold voltage, and V_d is the applied drain voltage.

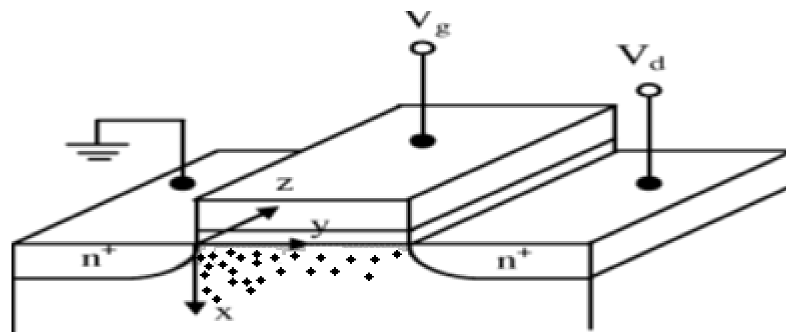

Figure 1-6: Minority carrier concentration variation in the channel of a MOSFET biased in the weak inversion.

An important parameter in weak inversion region is subthreshold slope (SS) which is defined as the inverse of the slope of the semilog transfer characteristic of the device between $\log_{10} I_D$ and V_g[8]and is given by

$$SS = \left(\frac{d(\log_{10} I_D)}{dV_g}\right)^{-1}$$

The value of subthreshold slope indicates rate of decrease of I_D below $V_{th}$and is measured in terms of millivolts per decade.The ideal value of SS at $t_{ox} = 0$ is 60mV/decade. The value of SS should be made as small as possible making the device turn off faster belowV_{th}. The subthreshold swing coefficient which is also known as body factor is given as

$$n = S_t / V_t \ln 10$$

1.4.2 Drain Induced Barrier Lowering:

In long-channel devices, a potential barrier height exists between the source and channel regions formed through the equilibrium established betweendrift and diffusion carrier flow components among these regions. This barrier is ideally controlled by gate voltagein long channel devices as theirsource and drain regions are far apart and their depletion regions do not influence the potential distribution or electric field pattern in the channel. Thus,the threshold voltage of long channel devices is independent of the channel length and drain bias voltage.Inshort-channel devices, source and drain depletion widths are close enough to significantly influence the channel electric field or potential resulting in a threshold voltage dependent on the channel length and drain bias applied. This effect is termed asDIBL [11]and generally occurs when the barrier height experienced by the source carriers is lowered by the influence ofhigh drain electric fields helping carrier injection into the channeland thus increasing the off–current. Short channel devices,drain current is a function of both gate and drain bias due to DIBL.

Figure 1-7 shows the cause ofDIBL in short channel devices. Line1of the energy band diagram inFigure 1-7(b) shows barrier height($q\phi_{bi}$) between source/drain and channel regions at flatband voltage(V_{FB})in long channel which can be lowered by applying gate bias (line 2 inFigure 1-7(b)).The voltage and energy are inversely related thus, as voltage increases the energy decreases. On applying drain bias the barrier at drain endfurther reduces without affecting the source barrier (line 3 inFigure 1-7 (b)). Similar changes are observed in short channel devices inFigure 1-7(d)showinga barrier between source/drain and channel at $V_{FB}$by line 1 and which islowered applying gate bias in line 2 but when drain voltage is applied then due to small distance between source and drain the source potential also gets lowered causing drain current to depend on drain bias given by line3 of Figure 1-7(d).

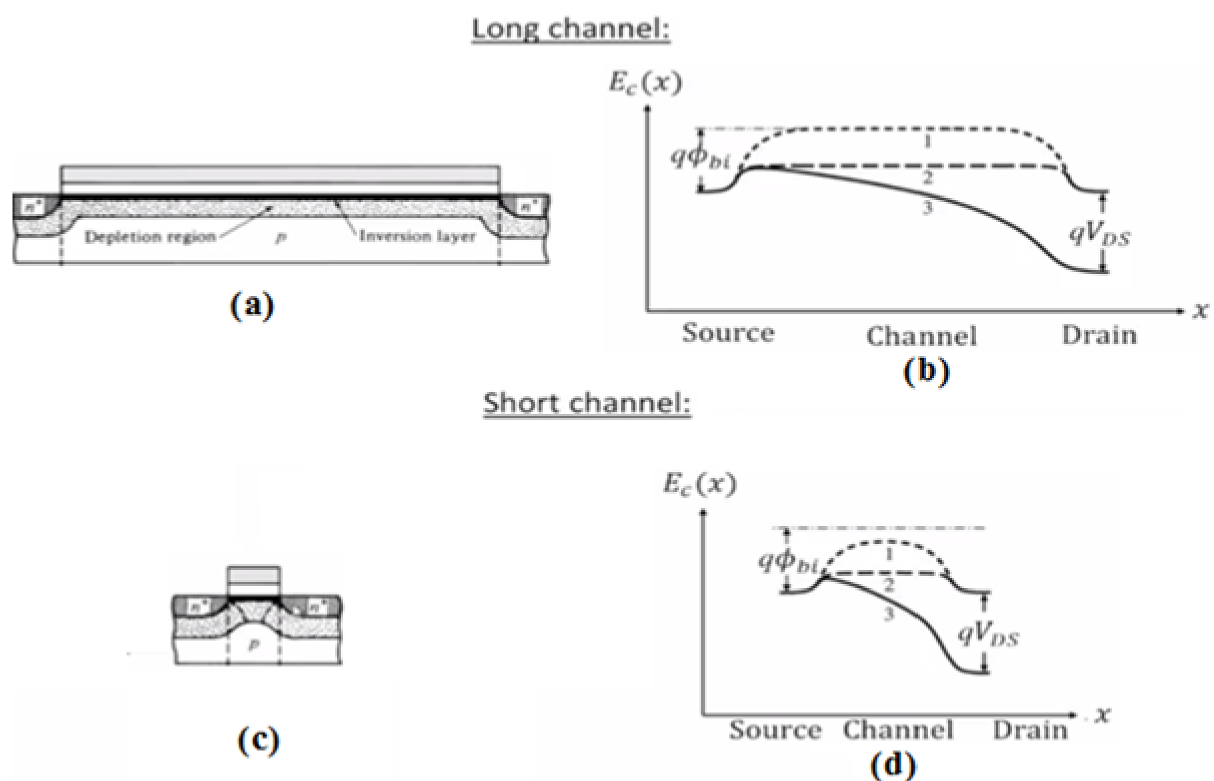

Figure 1-7: Energy barrier variation along the position in channel for applied gate and drain voltages.

1.4.3 Punchthrough

Punchthrough is the extreme case of DIBL. It causes flow of electrons from source to drain directly without the need of applying gate voltage as the source and channel potential barrier is reduced through high drain voltages, especially in short channel devices because the source and drain regions are close and their depletion regions interact by extending towards each other and merging at high reverse bias drain voltages.

Punchthrough can occur along the channel surface called as surface punchthrough or in the bulk known as bulk punchthrough. Figure 1-8 shows both these types

a) Surface punchthroughoccurs in uniformly doped structure, when the source/drain depletion region reaches each other without applying the gate bias or in the absence of gate depletion region.
b) Bulk punchthroughoccurs for ion-implanted channels with higher concentration at the surface keeping depletion regions away from the surface and in bulk of the MOSFET.

It degrades subthreshold slope giving high leakage current. To avoid punchthroughaddition ofimplants or highly doped layers at the bottom of source/drain regionsand halo doping are few potential methods [12].

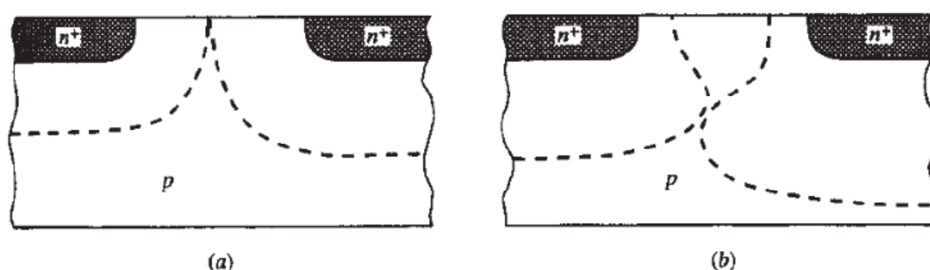

Figure 1-8: (a) Surface punchthrough and **(b)** bulk punchthrough

1.4.4 Threshold voltage roll off

The reduction of threshold voltage by reducing the channel length is called as threshold voltage roll off and is shown in Figure 1-9. The reason of threshold voltage roll off in short channel devices is 2-D field patterns originating due to small separation of source and drain regions [15] rather than1-D field patterns of long channel devices.However, in short-channel devicessource and drain regions are pretty close and their depletion regions cover significant part of the channel and can interact with each other resulting in strong lateral electric fields and depleting part of the channel earlier depleted by the gate in long channels, this is known as charge sharing. Thus, lower gate voltageto invert the channel reducing the threshold voltage for short channel devices. Charge sharing at higher drain voltages is more due to wider drain depletion region. The source/drain regions and their depletion regionsare far apart in long channel devices.

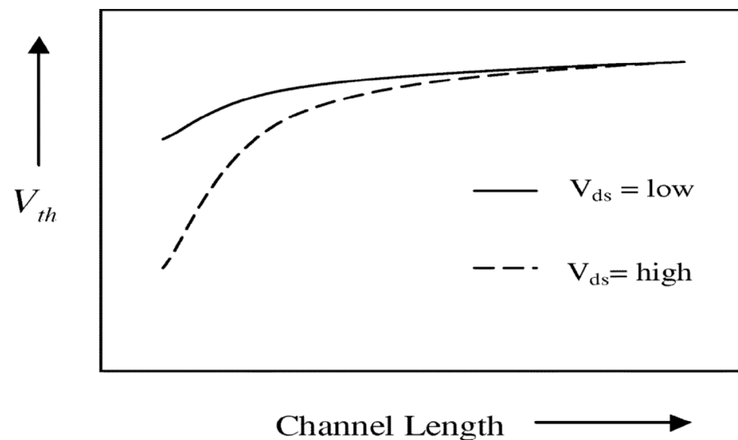

Figure 1-9: Threshold voltage roll-off with change in channel length at different drain bias

1.4.5 Hot carrier effect

The electric field component along the channel increases from source to drain end. In short channel devices high drain voltages causes avalanche breakdown at the drain end due to high electric field generated, giving rise to carriers which further contribute toleakage current. This phenomenon is known as hot carrier effect and can be explained through series of effects occurring consequently as depicted in Figure 1-10.

At high applied drain voltages the drain current constituting carriers are accelerated at the drain endunder high electric field acquiring large kinetic energy which causes theircollision with depletion region ions and silicon lattice atom generating electron/hole pairthrough impact ionization. Theholes are swept away to the bulk and theelectrons moves to the drain or towards the silicon-oxide interface where they get trapped as interface charge thus reducing the device reliability and degrading itsperformance.

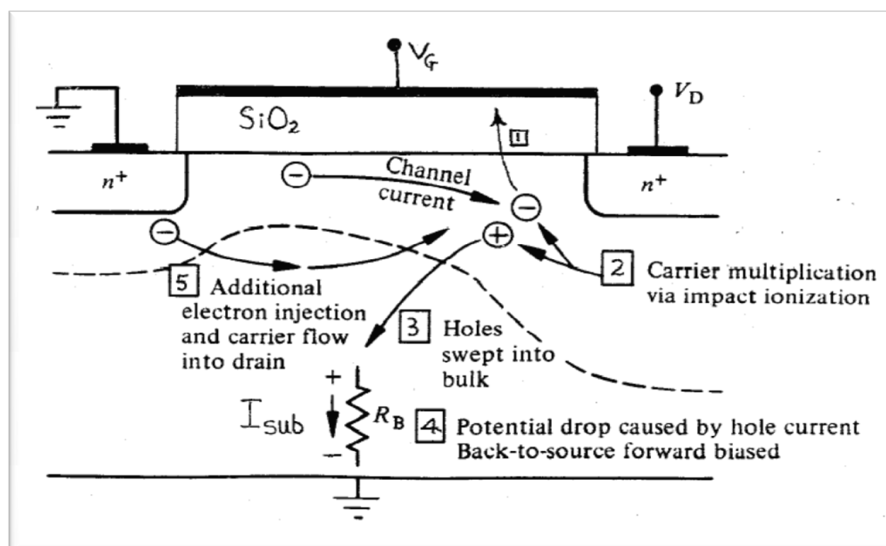

Figure 1-10: Hot Carrier effects in NMOS [13]

1.4.6 Gate Induced Drain Leakage

Gate induced drain leakage generally known as GIDL occurs owing to presence of high drain electric field. When the voltage applied on the gate is such as to create an accumulation layer at the siliconsurface, the doping concentration at the surface become higher in comparison to substrate doping whichcauses lower depletion layer width at the surface than in bulk as shown inFigure 1-11(a). The narrow depletion layer near surface gives rise to local electric field enhancing high field effects in this region[14].

At large accumulation creating gate bias, the gate overlapped drain regiongets depleted and at very high gate voltages it even gets inverted(Figure 1-11(b)), causing high field values and densefield lines in this region, giving carrier multiplication and electron/hole pair generation below the gate through impact ionization and band to band tunnelling [14]. These generatedminority carrier's movesin the substrate contributing GIDL current. GIDL increases when the fields are high and gate dielectric is thin and it is worst for moderate drain doping but can be minimized by using high drain doping with abrupt junction.

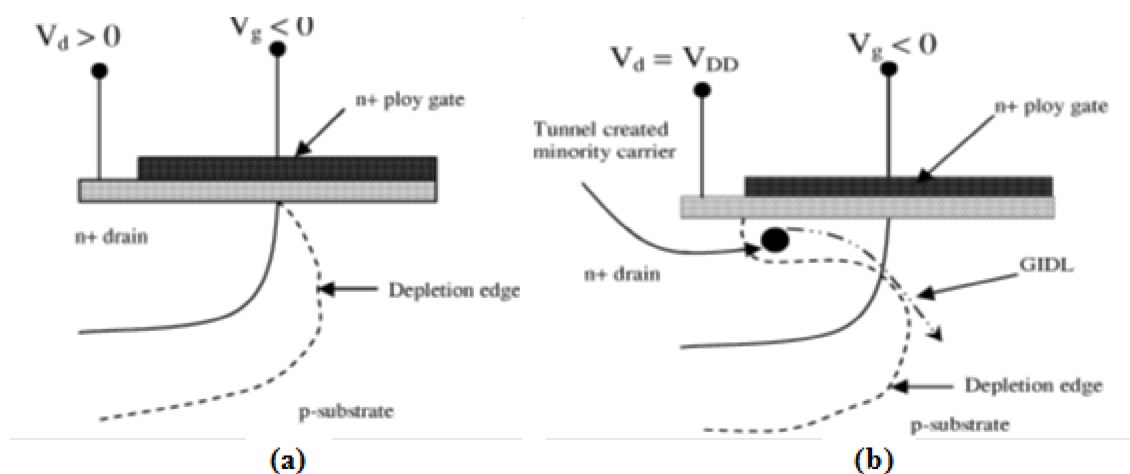

Figure 1-11: Condition of the depletion region near the drain-gate overlap region of an NMOS transistor when (a) surface is accumulated with low negative gate bias and (b) n+ region is depleted or inverted with high negative gate bias[8].

1.5 Organization of the Thesis Work

CHAPTER-1INTRODUCTION: -

This chapter starts from Moore's law and then discusses about scaling in bulk MOSFETs, its challenges and their solution in the form of advance MOSFETs. Then,it looks upon the major SCEs in conventional short channel devices.

CHAPTER-2 LITERATURE SURVEY: -

This chapter starts with small introduction about need of SOI devices and then tells about SOI MOSFETs,its advantages, types and advance SOI devices. The next section gives light on the Double gate MOSFETs, its advantages and types.

CHAPTER3-3 TWO DIMENSIONAL DRAIN CURRENT MODELING OF DOUBLE GATE MOSFET: -

In this chapter 2D potential function id derived and then an expression for potential based subthreshold slope and threshold voltage is obtained. Next, these derived expressions are used to model drain current and fixed oxide charge effect is studied over this model.

CHAPTER-4 RESULTS AND DISCUSSION: -

This chapter contains the comparison of the device simulation results of the double gate MOSFET from SILVACO (Atlas) TCAD tool with the model results.

CHAPTER-5 CONCLUSION AND FUTURE SCOPE: -

A brief conclusion and possible improvements have been discussed in this chapter.

Chapter 2

2 Literature Survey

In nanometre regime, short channel effects such as DIBL and threshold voltage roll-off severely degrades the performance of bulk MOSFETs. Silicon-on-Insulator (SOI) technology based advance MOSFETs has the capability to meet all the requirements of ITRS in nanometre regime and provide high speed, low power consumption and better scalability for the next generation technology[16].

2.1 Silicon on Insulator (SOI)

The SOI structure shown in Figure 2-1comprises of a single-crystal silicon film usually thin and in the range of tens of nanometre in thickness separated from silicon substrate by an electrically insulating material layer generally of silicon dioxide and called as buried oxide layer (BOX)which is relatively thicker than silicon film.The gate formed between the silicon film, buried oxide and substrate is also referred to as back gate.

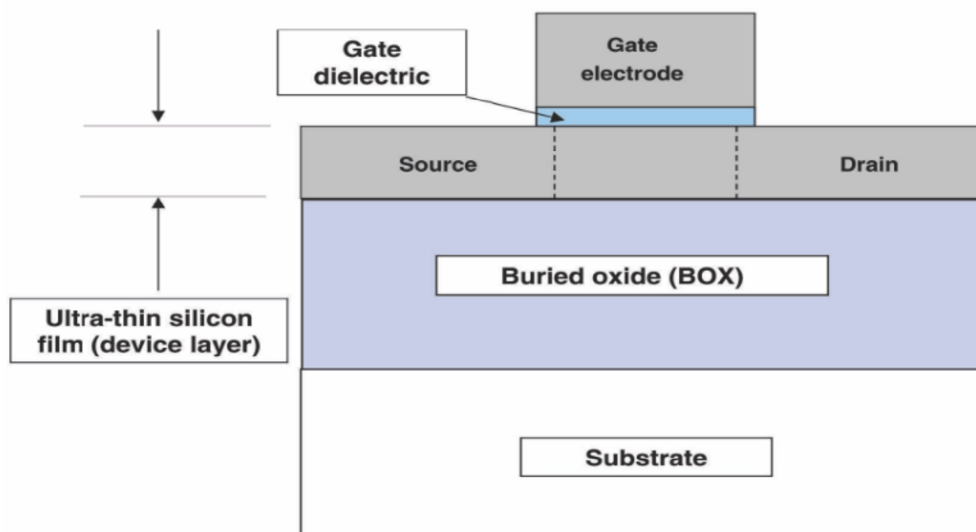

Figure 2-1: Cross-section of aSilicon OnInsulator device [16]

2.1.1 Advantages of SOI technology

1) **Lower parasitic capacitance: -** In conventional bulk MOSFET a capacitance exists between the drain/source and substrate and drain/source and the channel stop implant under thick field oxide but in SOI MOSFET the source/drain junction regions end on the insulating buried oxide layer, eliminating these capacitance This reduction of parasitic capacitance helps to improve the speed making the switching operations faster of the device.
2) **Reduced leakage paths: -** Thin silicon films eliminate sub-surface leakage currents flowing through the substrate regions which were not under gate control in conventional bulk MOSFET. In SOI MOSFETs, with thin silicon film and BOX gate have better control over the channel reducing sub-surface leakages [18].
3) **Better dielectric isolation: -** The SOI MOSFET gives dielectric isolation both vertically and laterally. The vertical isolation is obtained from the presence of thick insulating BOX layer and lateral isolation is from the oxide grown by shallow trench or LOCOS techniques.
4) **Latchup elimination: -**Presence of inherent parasitic BJTforming aPNPN thyristorshown inFigure 2-2is the biggest limitation of a CMOS structure.Scaling lateral dimensions of the deviceenhances the gain of these parasitic BJT'sand increases the risk of turning the thyristor on causing latchup and flow of large amount of leakage current. But, in SOI CMOSthe silicon islands for NMOS and PMOS formation areisolatedfrom oneanother laterally as well as verticallythrough a dielectric layer eliminating the current pathsbetween substrate and device responsible for the latchup[18].

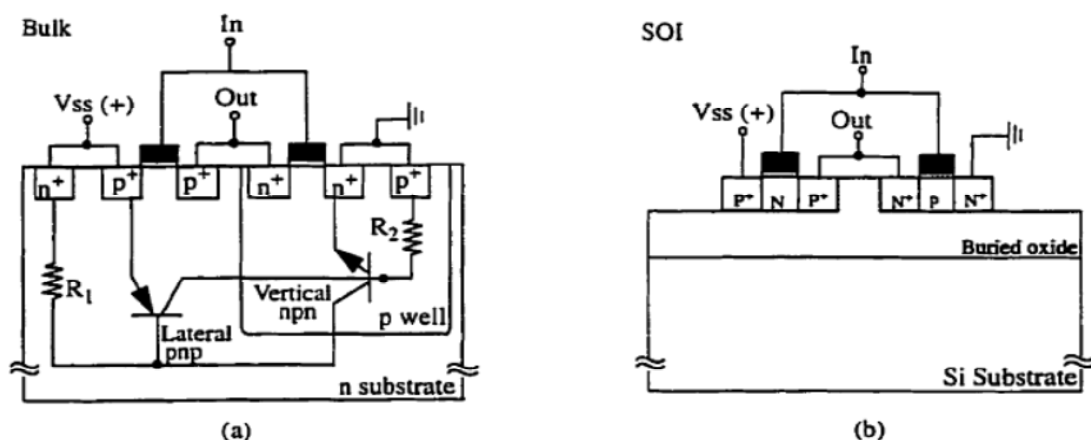

Figure 2-2: Cross section of (a) bulk CMOS Inverter and (b) SOI CMOS Invertor [18]

2.1.2 Types of SOI MOSFET

There are basically twotypes of SOI devices distinguished on the basis oftheir silicon filmthickness and doping concentration:

1) Partially depleted(PD) or non-fully depleted (NFD) SOI MOSFET

Partially depleted SOI MOSFET hast_{si}greater than twicethe sum of maximum depletion width of the front and back gates ($2x_{dmax}$) assuming both gate have same maximum depletion widths.These front and back depletion regions remains decoupled due to the neutral film region existingbeneath these depletion regions and hence there is no interaction between them. This neutral silicon film region isknown as "Body" which is generally grounded through a contact called as "body contact". When the neutral region is grounded it behaves in a similar manner as the bulk MOSFET. While if the body is kept electrically floating then the floating body effect such as the kink effect in which holes generated due to impact ionization at the drain junction gets stored in the neutral body modulating the device threshold voltage giving a kink in the output characteristic and parasitic open base NPN bipolar transistor between source and drain influences the device properties[19].

2) Fully depleted (FD) SOI MOSFET

In Fully Depleted devices the silicon film gets completely depleted at threshold voltage i.e. the sum of maximum depletion widths ($2x_{dmax}$) of front and back gateissmaller than or equal to t_{si}.Complete depletion of silicon filmfrom the interaction between the two gates depletion regions causes coupling of the front gate threshold voltage with the back gate thus, giving an additional control over it through back gate. Further there are two modes of operation in FD SOI device according tothe gate material and silicon film doping as well as concentration. These modes are:Inversion and Accumulation. The silicon surface is inverted and accumulated in these modes respectively.Advantages of FD over PD are[20]:

1. It is free from kink effect
2. Near ideal subthreshold slope approx. 70mV/decade
3. Higher circuit speed and gain
4. Reduced power requirements and higher soft error immunity
5. Schematic of(a) Partially depleted SOI MOSFET(b) Fully Depleted SOI MOSFET

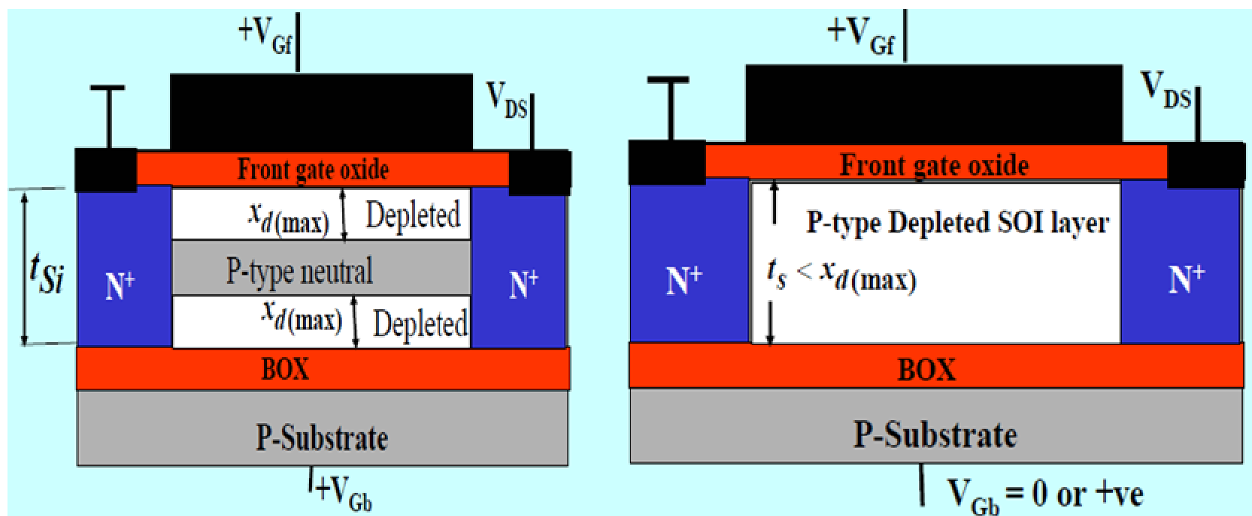

Figure 2-3: Schematic of(a) Partially depleted SOI MOSFET(b) Fully Depleted SOI MOSFET

2.1.3 Advance SOI devices

Drain electric field encroachment in the channel region is the main reason for SCE in SOI devices. This encroachment takes place from different directions (as shown inFigure 2-4) such as from the top but there thegate electrode protectsthe channel region from these drain electric field lines. Laterally from the drain region and from the bottom where these field lines penetrate the channel from underneath through buried oxide and substrate**.**

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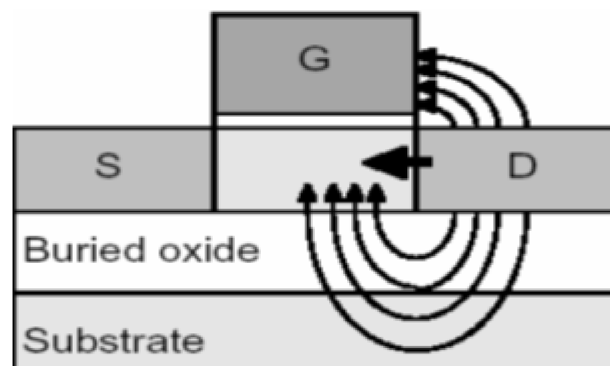

Figure 2-4: Drain electric field encroachment in SOI devices [6]

These SCE because of drain field can be reduced or even eliminated through different SOI device structures, some of them are [6]:-

1) Raised source and drain thin body FD SOI.
2) Metal electrode source/drain FD-SOI MOSFET.
3) Metal gate electrodeSOI.

4) Buried oxide dielectric engineered devices.
5) Fully depleted SOI with Ground plane.
6) FD-SOI MOSFET with Multiple gates.

2.2 Double-Gate MOSFET

Among several multiple-gate FDSOI devices,double-gate (DG) MOSFET is one of the promising device structures to scale CMOS to sub-nanometre regime to form devices with gate lengths as small as 15nm and below [6] because of its high immunity to short channel effects(SCE).The double-gate concept was first reported in 1984 [21]and has been fabricated by several groups since then. The use of a double gate results in enhanced trans-conductance, due to the volume inversion effect [22][23]and better subthreshold slope.

2.2.1 Attractive features of Double Gate MOSFET

1. **Thin silicon film**: - The silicon film thickness is one of the parameter which reduces with scaling to reduce leakage currents from SCE. An ultra-thin body with t_{si}less than50% of channel length is necessary to effectively suppress these leakage current but in DG- MOSFETs due to enhanced channel controlby the two gatest_{si}can be relaxed to be 50% to 70% of L_g.
2. **Low body doping**: -The maximum channel depletion width under the gate dependents on the body thickness rather than channel doping density and thus, high channel doping density are not required to minimize x_{dep}. This eliminates dopant fluctuation and mobility degradation problems in DG-MOSFETs.
3. **Shallow S/D junctions**: - The source and drain junction depths $(X_j)$are defined by silicon film thicknesst_{si} thus shallow junctions can beeasily implemented by thin silicon film withoutdeveloping complicated doping and structural techniques.
4. **Low leakage currents**: - Thin silicon films in DG-MOSFETs eliminate those leakage paths of the channel which were earlier far away from the reach of gate to control them by providing a better control of the channel from the two electrically coupled gates.

Regardless of the superiority of DG MOSFET and SCE immunity its manufacturing is still challenging. In vertical devices, FINFET is the DG structure which is comparatively easily manufacturable due to its process compatibility with conventional bulk MOSFET. The

planar DG MOSFET has the problem of gate alignment which makes their fabrication complicated.

2.2.2 Types of DG MOSFET

Basically there are two types of double gate MOSFET depending on the method of application of gate bias voltage:-

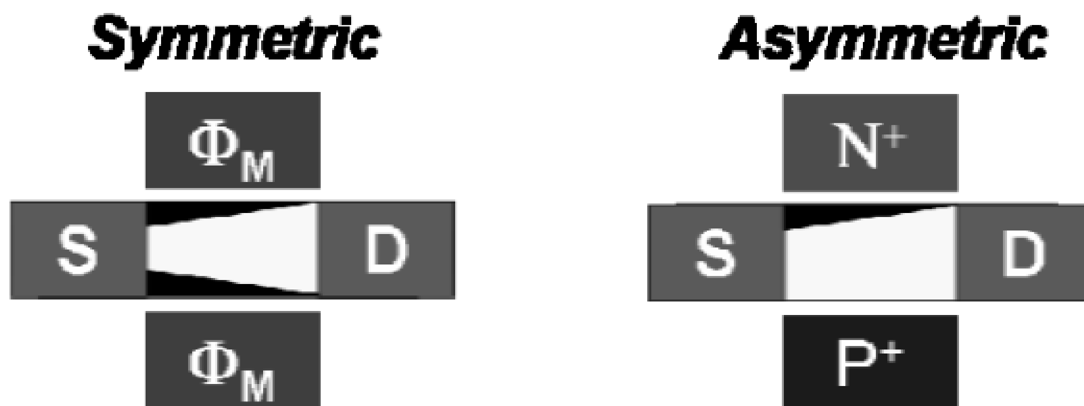

Figure 2-5: Symmetric and Asymmetric DG MOSFET structures.

2.2.2.1 Symmetric Double gate MOSFET (SDG):-

The workfunction of both the gates are similar in these devices i.e. the material for both the front and back gate are identical and thus if front gate is of N+ poly-Si then back gate is also of the same materialtype and doping or same metal is used for both front and back gate electrode.This allows both gates to influences the operation of the device in an identical manner.The SDG is structurally symmetrical at both the top and back gate with same gate oxide thickness and generally same voltages are applied at both the gates[24]. When voltage is applied to the gates of SDG, two channels are formed one near the top boundary between silicon and insulator and other at the bottom interface. These two channels are separated by enough distance as to be independent of each other creating two independent transistors on the same piece of silicon. Each gate can control half of the device and its operation is completely independent of the other. The total current through the device is equal to the sum of the currents through the separates channels. The performance of the symmetrical DG MOSFET is increased by higher channelmobility compared to bulk MOSFET, since the average electric field in the channel is lower, which reduces interface roughness scattering according to the universal mobility model

2.2.2.2 Asymmetric double gate MOSFET (ADG):-

In these devices both gate can have different workfunctionmaterials for front and back gate electrode i.e. if using N+ poly-Si for front gate then can use P+ poly-Si for the back gate thus front and back gate can have different material, type and doping.For asymmetric devices different strength can be obtained by different oxide thickness at front and back gates. Thus, ADG is asymmetrical structurally and with gate workfunction. In on statewhen both the gates have same applied bias only one inversion layer is formed until the voltage applied is extremely high to form other inversion layer because of the different workfunction at both gates generating different threshold voltages for these gates. The threshold voltage of ADG is also a function of body thickness and oxide thickness other than gate workfunction thus, can in any one of them causes threshold voltage variation [25].

Chapter 3

3 Two Dimensional Drain Current Modeling of Double Gate MOSFET

3.1 Introduction

In long channel MOSFETs the large spacing between source/drain regions provides very small value of lateral electric field component (i.e. along the channel length)thus the "edge effect"along the sides of the channel can be neglected and only perpendicular electric field (i.e. along the silicon film thickness) is assumed to exist at the surface everywhere reducing the analysis to only one dimension based on gradual channel approximation. Such one dimensional analysis fail in short channel devices as the source and drain are much closer to each othercausing the drain electric field to influence the channel potential. Thus, a two dimensional analysis is required for short channel devices with large channel width and a three dimension approach is adopted for short channel devices with narrow width.

In this chapter, a two dimensional expression for the potential distribution in the silicon film as function of channel length and silicon film depth is derived for the symmetrical double gate MOSFETs in weak inversion. Further, this 2D potential distribution expression is used to derive the analytical expression for the subthreshold slope and threshold voltage. Finally a drain current model for undoped symmetrical DG MOSFET is presented. The drain current modeling is done considering two major regions of its operation namely weak inversion and strong inversion including short channel effects, series resistance and channel length modulation parameters.

3.2 Fully Depleted DG-MOSFET Structure and Parameter

A schematic cross sectional view of symmetric n-channel FD-DG MOSFET with structural definition and co-ordinate system is shown in Figure 3-1. The front and back gate are of mid-gap metal with workfunction of 4.74eV, both the front and back gate oxide thickness (t_{ox}) is 2nm with silicon film thickness (t_{si}) of 10nm. The doping in the p-type body is kept almost undoped (or very lightly doped) with a doping of $N_a = 10^{15} cm^{-3}$and n+ source and drain are doped with the dopant density of$N_d = 10^{20} cm^{-3}$.

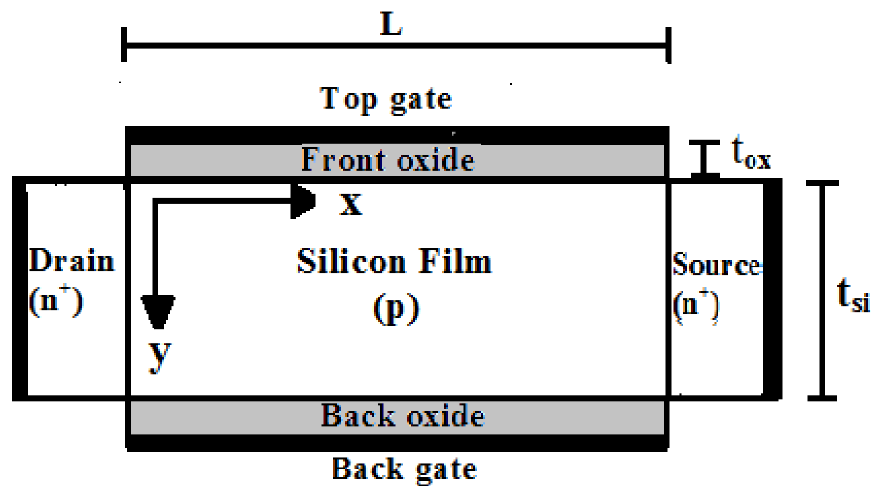

Figure 3-1: Schematic diagram of symmetric n-channel Double Gate MOSFET with structural definition and coordinate system

3.3 Potential Distribution

To model the physical behavior of symmetrical FD-DG MOSFET at nanometer domain and below the potential distribution across the thin silicon film under different drain and gate bias conditions must be explicitly obtained. Presence of two gates and thin silicon film causes the potential distribution in DG MOSFET to be different than single gate MOSFET and the maximum potential do not occur at the surface but at some depth in the film.Many differentapproaches have been proposed to analytically determine the potential along the channel of DG MOSFET in the literature.One of them is using depletion approximation for solving Poisson's equation in weak inversion region.

The Poisson's equation in the form of electric field variation along all the three dimensions can be written as:-

$$\frac{\partial \vec{E}_x}{\partial x} + \frac{\partial \vec{E}_y}{\partial y} + \frac{\partial \vec{E}_z}{\partial z} = \frac{qNa}{\epsilon_{Si}} \qquad (1)$$

where, $\vec{E}_x = \frac{\partial \phi(x,y,z)}{\partial x}$, $\vec{E}_y = \frac{\partial \phi(x,y,z)}{\partial y}$, $\vec{E}_z = \frac{\partial \phi(x,y,z)}{\partial z}$ are the electric field component in x, y and z direction respectively and $\phi(x, y, z)$is the potential distribution in the channel. This equation predicts that the sum of electric field variation in all three dimensions at any point (x,y, z) in the silicon film is always a constant whose value is given through the ratio of depletion region charge (qNa) and permittivity of the material (ϵ_{Si}). Thus for equilibrium it is necessary that if any one or two component of the electric field changes then the other should also vary in opposite way to keep their sum a constant.

$\vec{E}_x$represents the drain electric field influence on the channel. A large value of $\vec{E}_x$ is responsible for creating various SCEs in the device which can bereduced by increasing channel length, usingmulti-gate architecturesor reducing silicon film thickness and/or channel width.

The electric field variation along the z direction is negligible due to its very small values in wide DG MOSFETs and hence it can be considered that$\partial\vec{E}_z/\partial z$ is zero and equation (1) reduces to$\frac{\partial\vec{E}_x}{\partial x} + \frac{\partial\vec{E}_y}{\partial y} = \frac{qNa}{\epsilon_{Si}}$

$$\frac{\partial\vec{E}_x}{\partial x} + \frac{\partial\vec{E}_y}{\partial y} = \frac{qNa}{\epsilon_{Si}} \qquad (2)$$

for strong inversion region the above equation (2) is not valid as the channel potential along x direction in strong inversion is modulated by inversion charge [26]-[27]. The potential distribution along the silicon film thickness i.e. vertical y direction is taken as a cubic function ofx(i.e. along channel length) as proposed by Toyabe and Asai[28]and is valid for all values of drain voltages.

$$\phi(x,y) = a_0(y) + a_1(y)x + a_2(y)x^2 + a_3(y)x^3 \qquad (3)$$

here, coefficients $a_0, a_1, a_2$and a_3 are the function of only y dimension. In symmetrical DG MOSFET due to structural symmetry the front and back oxide-silicon interface have same potential distribution along the channel which can be defined as

$$\phi(x,0) = \phi(x,t_{si}) = \phi_1(x) \qquad (4)$$

The boundary conditions are obtained by applying gauss law in the vertical direction at the gate oxide transverse electric field$\vec{E}_y$ on the front and back gates.

$$\vec{E}_y(\text{at } y = 0) = \frac{Q_0}{\epsilon_{Si}} \qquad (5)$$

$$\vec{E}_y(\text{at } y = t_{si}) = \frac{Q_{t_{si}}}{\epsilon_{Si}} \qquad (6)$$

Where, C_{ox} is the gate oxide capacitance and is given in terms of dielectric constant of gate oxide (ϵ_{ox}) and oxide thickness (t_{ox}) as $\epsilon_{ox}/t_{ox}$and $Q_0 = C_{ox}V_f$ and $Q_{t_{si}} = C_{ox}V_b$ are the charge atthe front and back oxide-silicon interface respectively. $V_f = \phi_1(x) - V_g'$and$V_b =$

$V_g' - \phi_1(x)$ respresents voltage difference along the oxide thickness at both front andback gates responsible for capacitive action.The virtual gate voltage (V_g') appearing at the front and back gate is always smaller than the actual applied gate voltage (V_g) as some amount of gate voltage is required to cancel out the effect of contact potentials and potential developed due to oxide trapped charges which is known as Flat band voltage V_{FB}. The flat band voltage assuming trap charges to be zero is given by$W_{ms} = -(KT/q)\ln\frac{Na}{ni}$for mid-gap metal gate DG- MOSFET. Equations (4)-(6) are used to obtain the coefficient values of the cubic potential distribution in equation (3) as

$$a_0 = \phi_1(x) \tag{7}$$

$$a_1 = \frac{C_{ox}V_f}{\epsilon_{Si}} \tag{8}$$

$$a_2 = -\frac{a_1}{t_{si}} = \frac{C_{ox}V_b}{\epsilon_{Si}} \tag{9}$$

$$a_3 = 0 \tag{10}$$

Solving (3) and (2) using (7)-(10), the differential equation in terms of surface potential is obtained as

$$\frac{\partial^2\phi_1(x)}{\partial x^2} - \beta_0\phi_1(x) = \beta_1 \tag{11}$$

where, $\beta_0 = \frac{2C_{ox}}{\epsilon_{Si}t_{si} + C_{ox}t_{si}y - C_{ox}y^2}$and $\beta_1 = \frac{qN_at_{si} - 2C_{ox}V_g'}{\epsilon_{Si}t_{si} + C_{ox}t_{si}y - C_{ox}y^2}$

Next, solving (11) using boundary conditions $\phi_1(x) = \phi_{bi}$ at x=0 and $\phi_1(x) = \phi_{bi} + V_d$ at x=L gives the expression for surface potential as

$$\phi_1(x) = c_1e^{x/\lambda_1} + c_2e^{-x/\lambda_1} + A_1 \tag{12}$$

Where,$\phi_{bi} = V_t \ln N_aN_d/n_i^2$ is the built in potential across the source/drain and channel junction,V_d is the drain voltage,c_1 and c_2 are the coefficients and $A_1$is a constant given as

$$C_1 = \frac{\phi_{bi}(1 - e^{-L/\lambda_1}) + V_d + A_1(e^{-L/\lambda_1} - 1)}{(e^{L/\lambda_1} - e^{-L/\lambda_1})}$$

$$C_2 = \frac{\phi_{bi}(1 - e^{L/\lambda_1}) + V_d + A_1(e^{L/\lambda_1} - 1)}{(e^{-L/\lambda_1} - e^{L/\lambda_1})}$$

$$A_1 = \frac{-\beta_1}{\beta_0} = V_{g'} - \frac{qN_a t_{si}}{2C_{ox}}$$

$\lambda$is the natural length and λ_1 is its value at the interfaces i.e. at y=0 and t_{si}[29]. Natural length is defined as the parameter which indicates the drain field influence on the channel and thus characterizes the SCE. It mainly depends on the geometrical dimensions and its value should be as small as possible.

$$\lambda = \frac{1}{\sqrt{\beta_0}} = \sqrt{\frac{\epsilon_{Si} t_{si} + C_{ox} t_{si} y - C_{ox} y^2}{2C_{ox}}} \qquad (13)$$

$$\lambda_1 = \frac{1}{\sqrt{\beta_0 (\text{at } y=0)}} = \sqrt{\frac{\epsilon_{Si} t_{si}}{2C_{ox}}} \qquad (14)$$

In DG MOSFETs the potential at the surface is less than the potential at the effective conductive path which is taken at $y = t_{si}/4$[30]. Thus, it becomes necessary to determine the potential as the function of channel depthwhich can be done by defining the potential in terms of surface potential using equations (3)

$$\phi(x, y) = \alpha_1 \phi_1(x) - \alpha_2 V_g' \qquad (15)$$

where,$\alpha_1 = 1 + \frac{C_{ox} y}{\epsilon_{Si}} - \frac{C_{ox} y^2}{\epsilon_{Si} t_{si}}and\alpha_2 = \frac{C_{ox} y}{\epsilon_{Si}} - \frac{C_{ox} y^2}{\epsilon_{Si} t_{si}}$. Using equations (15) and (11) the differential equation for potential is obtained as

$$\frac{\partial^2 \phi(x,y)}{\partial x^2} - \beta_0' \phi(x, y) = \beta_1' \qquad (16)$$

Where, $\beta_0' = \beta_0$,$\beta_1' = \frac{2C_{ox} V_g'(C' - 1) + qN_a t_{si}}{\epsilon_{Si} t_{si}}$and $C' = \frac{C_{ox} t_{si} y - C_{ox} y^2}{\epsilon_{Si} t_{si} + C_{ox} t_{si} y - C_{ox} y^2}$

The solution for the above differential equation (16)using boundary conditions $\phi(x,y) = \phi_{bi}$ at x=0 and $\phi(x,y) = \phi_{bi} + V_d$ at x=L is expressed as

$$\phi(x,y) = c_1' e^{x/\lambda} + c_2' e^{-x/\lambda} + \Lambda A_2 (17)$$

where,

$$c_1' = \frac{\phi_{bi}\left(1 - e^{-L/\lambda}\right) + V_d + A_2\left(e^{-L/\lambda} - 1\right)}{\left(e^{L/\lambda} - e^{-L/\lambda}\right)}$$

$$c_2' = \frac{\phi_{bi}\left(1 - e^{L/\lambda}\right) + V_d + A_2\left(e^{L/\lambda} - 1\right)}{\left(e^{-L/\lambda} - e^{L/\lambda}\right)}$$

$$A_2 = \frac{-\beta_1'}{\beta_0'} = V_g' - \frac{qN_a(\epsilon_{Si}\, t_{si} + C_{ox} t_{si} y - C_{ox} y^2)}{2\, C_{ox}\, \epsilon_{Si}}$$

Substituting the values of y at the two gates i.e. 0 andt_{si}, equation (17) reduces to (13) indicating that it is valid for determining potential in all regions in the channel.

3.4 Minimum potential

The lateral channel position x_{min} at which the channel potential reaches its minimum value (ϕ_{min}) can be determined by considering potential minima along the lateral x direction [31].

$$\frac{\partial \phi(x,y)}{\partial x} (\text{at } x_{min}) = 0$$

$$x_{min} = \frac{L}{2} - \frac{\lambda}{2} \ln\left[\frac{(\phi_{bi} - A_1)(e^{L/\lambda} - 1) + V_{ds} e^{L/\lambda}}{(\phi_{bi} - A_1)(e^{L/\lambda} - 1) - V_{ds}}\right] \qquad (18)$$

Equation (18) shows that the position of the minimum channel potential depends on the applied drain voltage. For zero drain voltage the minimum channel potential is at themiddle of the channel length while it moves towards the source end as the drain voltage increases. The value of ϕ_{min}evaluated by using (17) and (18) is

$$\phi_{min} = c_1' e^{x_{min}/\lambda} + c_2' e^{-x_{min}/\lambda} + A_2 \qquad (19)$$

3.5 Subthreshold slope

The subthreshold slope (SS) is defined as the reciprocal of the slope of semilog I_D-V_g characteristic and it shows the rate of decrease in drain current with gate voltage below threshold level. Its unit is given in mV/decade.[37]

$$SS = \left(\frac{\partial \log I_D}{\partial V_g}\right)^{-1} \quad (20)$$

An analytical subthreshold slope expression is obtained based on the assumption that SS basically depends on the carrier concentration n_{min} at minimum channel potential ϕ_{min} located at a depth y in the silicon film[32]-[33]. The carrier concentration n_{min} is given by $n_{min} = (n_i^2/N_a)\, e^{\phi_{min}/V_t}$

$$SS = \frac{\partial V_g}{\partial \log I_D} \approx \ln 10 \frac{\partial V_g}{\partial \ln n_{min}} = \frac{V_t \ln 10}{\partial \phi_{min}/\partial V_g} \quad (21)$$

$$\partial \phi_{min}/\partial V_g = 1 + \frac{1}{(e^{2L/\lambda - 1})}[(e^{3L/2\lambda} - e^{L/2\lambda})((\phi_{bi} - A_2)X_1 - Ps) + X_2] \quad (22)$$

Where,

$$X_1 = \frac{1}{2}\left[V_d(e^{2L/\lambda} - 1)/\left((\phi_{bi} - A_2)(e^{L/\lambda} - 1) - V_d\right)^2\right](x_s^{-1/2} - x_s^{-3/2})$$

$$x_s = \frac{(\phi_{bi} - A_2)(e^{L/\lambda} - 1) + V_d e^{L/\lambda}}{(\phi_{bi} - A_2)(e^{L/\lambda} - 1) - V_d}$$

$$Ps = (x_s^{-1/2} + x_s^{1/2})$$

$$X_2 = -\frac{1}{2}V_d\left[V_d(e^{2L/\lambda} - 1)/\left((\phi_{bi} - A_2)(e^{L/\lambda} - 1) - V_d\right)^2\right](e^{3L/2\lambda}x_s^{-3/2} - e^{L/2\lambda}x_s^{-1/2})$$

The subthreshold swing coefficient also known as the body effect coefficient is given in terms of subthreshold slope as

$$n = \frac{SS}{V_T \ln 10} \quad (23)$$

3.6 Threshold voltage

For ultra-thin double gate MOSFET with very small silicon film doping $N_a \leq 10^{16} cm^{-3}$[26], the threshold voltage definition may be given as the gate voltage where minimuminversion sheet charge density Q_{inv} required for current conduction reaches the value Q_{th}[36]. This method of evaluating V_{th} is similar to the constant drain currentV_{th} extraction method where$I_D/(W/L)$ = constant.

The minimum potential inversion sheet charge density is obtained by integrating their spatial density for the entire thickness of the silicon film.

$$Q_{inv} = \int_0^{t_{si}} n_i e^{\phi_{min}/V_T} dy \quad (24)$$

At$y = t_{si}/4$,

$$Q_{inv} = \frac{t_{si}}{4} n_i e^{\phi_{min}/V_T} \quad (25)$$

At gate voltage equal to the threshold voltage V_{th} the value of inversion charge is $Q_{inv} = Q_{th}$[42]. Upon evaluating equation (25) the expression for V_{th} is obtained as

$$V_{th} = V_{FB} + \frac{qN_a(\epsilon_{Si} t_{si} + C_{ox} t_{si}^2/4 - C_{ox} t_{si}^2/16)}{2\, C_{ox} \epsilon_{Si}} + A\kappa - B(\phi_{bi} - \kappa)^{1/2}(\phi_{bi} + V_d -$$

κ12−C2ϕbi+Vd (26)

where,$\kappa = V_T \ln \frac{Q_{th}}{n_i t_{si}}$, $A = \frac{e^{4L/\lambda} - 2e^{2L/\lambda} + 1}{(e^{L/\lambda} - 1)}$, $B = \frac{2e^{L/2\lambda}(e^{L/\lambda} + 1)}{(e^{L/\lambda} - 1)^2}$and

$C = \frac{2e^{L/2\lambda} - 4e^{2L/\lambda} + 2e^{L/\lambda}}{(e^{L/\lambda} - 1)^4}$.

Equation (26) shows thatV_{th}depends on both the channel length and the silicon film thickness of the DG MOSFET.In long channel devices since the value of $\phi(x, y) = A_2$[37]thus, the threshold voltage for long channel DG MOSFET is given as

$$V_{th} = V_{FB} + \frac{qN_a(\epsilon_{Si} t_{si} + C_{ox} t_{si}^2/4 - C_{ox} t_{si}^2/16)}{2\, C_{ox} \epsilon_{Si}} + \kappa \quad (27)$$

Now, the threshold voltage roll-off showing the drop in threshold voltage of a device with reduction in its channel length can be determined by taking the difference of short channel threshold voltage at a particular drain voltage and long channel threshold voltage. The analytical expression of threshold voltage thus obtained is

$$\delta V_{th} = (A-1)\kappa - B(\phi_{bi} - \kappa)^{1/2}(\phi_{bi} + V_d - \kappa)^{1/2} - C(2\phi_{bi} + V_d) \quad (28)$$

The value of Q_{th} has been evaluated from the expression

$$Q_{th} = 2 \times 10^{15} + \frac{1.9 \times 10^{12}}{L(m)} m^{-2} \quad (29)$$

which is generally obtained through a relationship that best matches the analytical expression of an undoped DG MOSFET with the simulation results. The value of Q_{th} used in this paper is given as

3.7 Drain current

To study the behavior and evaluate the characteristics of the DG MOSFET it is necessary to divide thetransistor operation in two major regions and they are weak inversion region and strong inversion region. The current conduction mechanism from source to drain and the factors constituting current in these two regions are different as in weak inversion the current is due to diffusion because of few minority carriers and depletion region generated potential distribution and in strong inversion it is the drift current generated by the flow of inversion layer carriers under the electric field influence in the channel.

3.7.1 Subthresholdregion current($I_{D,sub}$)

A subthreshold region is also known as the weak inversion region that occurs at gate voltages lower than threshold voltage. The current in this region is basically due to minority carrier diffusion along the channel. Thesubthreshold current influenced by lower drain voltages close to 0V are modeled by BSIM drain current model [45]. But at high drain voltages, drain induced barrier lowering and channel length modulation influence the device characteristics to a large extent. In order to account these effects an additional parameter is included in the model equation, thus, an improved model is obtained for subthreshold current of symmetrical DG MOSFET.

The channel length modulation representing the shortening of channel length at higher drain voltages due to large drain field [47]can be modeled as

$$\mathrm{CLM} = 1 + \left(\frac{\lambda}{L}\right)^{u-\sqrt{\lambda/L}}\left(\frac{V_{def}}{V_{gef}-V_{th}}\right) \quad (30)$$

where, $\gamma = 1 - \sqrt{\lambda/L}u$ is an empirical fitting parameter varying with channel length and series source to drain resistance.

Drain induced barrier lowering introduced at high drain voltages is modeled by introducing a drain voltage dependentparameter ηV_din the exponential term which was earlier only the function of gate voltage. Hence, the model proposed by meindl and swanson[46]to represent the DIBL parameter related to the geometry of the transistor is modified by introducing an empirical fitting parameter D is expressed as

$$\eta = \frac{\epsilon_{si} D}{C_{ox} L}$$

Thus, the subthreshold current equation to better model for DG MOSFET is obtained as

$$I_{D,sub} = \mu C_{ox}\frac{2W}{L}V_T^2 e^{\varphi/V_T}\left(1 - e^{-V_d/V_T}\right)\mathrm{CLM} \quad (31)$$

where, $\varphi = \frac{(V_g - V_{th})}{n} + \eta V_d$, n is the subthreshold coefficient taken from (23) andV_{th} is the short channel threshold voltage (26).

3.7.2 Strong inversion current ($I_{D,si}$)

When the MOSFET operates in the turn on condition with large inversion carrier density above threshold voltage it is said to be in the strong inversion region andthe current conduction in this region is due to drift. Based on the work done by A. Tsormpatzoglou et al [47]the strong inversion drain current equation is taken as

$$I_{D,si} = \mu C_{si}\frac{16W}{L}V_t^2\left[(q_s - q_d) - \frac{C_{si}}{C_{ox}}({q_s}^2 - {q_d}^2)\right]\mathrm{CLM}(32)$$

The R_{sd} term accounts for the series source/drain resistance; CLM gives the channel length modulation from (30) and V_{th} is the short channel threshold voltage taken from (26). The normalized sheet charge density q_i is given through lambert function as

$$q_i = \frac{C_{ox}}{2C_{si}} \text{lambertW} \left[\frac{q}{C_{ox}} \sqrt{\frac{n_i^2 \in_{Si}}{2KTN_a}} e^{\frac{V_g - \delta V_{th} - V_{FB} - V}{2V_T}} \right]$$

where, V is the electron quasi fermi potential varying from 0V at the source to $V_d$at the drain. Thus the source normalized sheet charge density $q_s$is calculated at V=0 and drain normalized sheet charge densityq_d is obtained at V=V_d. The SCE is included by the δV_{th} parameter (28).

To obtain a compact drain current model a suitable interpolation function is used to match the subthreshold and strong inversion modes around threshold voltage of the form as follows

$$I_D = \frac{I_{D,sub} \times I_{D,si}}{\left(I_{D,sub}{}^{\alpha} + I_{D,si}{}^{\alpha}\right)^{1/\alpha}} \tag{33}$$

$$\alpha = 1.9 - \sqrt{1.2V_{ds}} \tag{34}$$

Equation (33) gives the drain current in the DG MOSFET at all values of gate and drain voltages and (34) show the interpolation function α expression used to best fit the simulation results.

The obtained model is also studied by considering the effect of fixed oxide charges present in thin oxide layers. This effect is included in the flatband voltage expression as

$$V_{FB} = W_{ms} - \frac{qN_f}{C_{ox}} \tag{35}$$

where, W_{ms} represents the workfunction difference between the metal and the semiconductor for the mid-gap metal gates. $N_f$is the fixed oxide charge density in cm^{-3}.

Chapter 4

4 Results and Discussion

The above derived drain current model expression and its parameters subthreshold slope and threshold voltage expressions are verified by comparison with the simulated result of the SILVACO (Atlas) TCAD simulator results using the classical drift diffusion approach. The results are obtained for devices with L/t_{si} ratio greater than 2 and taking the geometrical dimensions of the device as silicon film thickness t_{si}=10nm, silicon film doping concentration $N_a = 10^{15}cm^{-3}$, source/drain doping concentration $N_d = 10^{20}cm^{-3}$, channel width W=50nm, oxide thickness $t_{ox} = 2nm$, workfunction of mid-gap metal gate as W_{ms} = 4.74eV and a constant mobility of $\mu = 500\ cm^2/Vs$ is used for simplicity.

4.1 Subthreshold Slope

Figure 2 shows the calculated values from the analytical subthreshold slope expression obtained in (21) is in good agreement with the simulated result for subthreshold slope for all values of channel length that are taken into consideration. The subthreshold slope values are evaluated for drain voltage valueV_d=1V and effective conducting path at $y = t_{si}/4$.

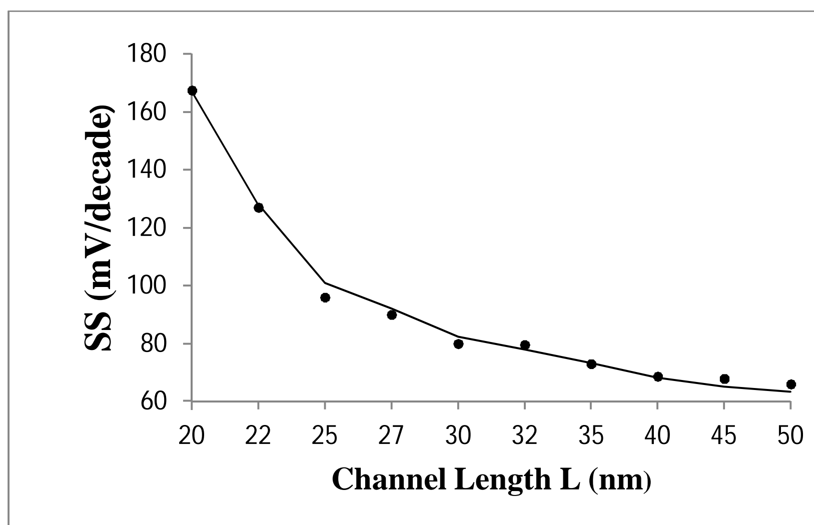

Figure 4-1: Comparison between the simulated (symbol) and analytical modeled (solid lines) subthreshold slope versus channel length

4.2 Threshold Voltage

The simulated and calculated threshold voltage valuesare plotted against different channel lengths for t_{si}= 5, 10 and 15nm. The calculated threshold voltage values agrees well with simulation results over complete range of L value investigated for t_{si}= 5nm and 10nm while it deviates slightly for t_{si}=15 nm as the condition $L/t_{si} \geq 2$ is not satisfied for silicon film thickness of 15nm. Thus, it can be concluded that for devices satisfying $L/t_{si} \geq 2$ condition, this model adequately describesV_{th}. The drain voltage of $V_d = 1V$ is used and the value of Q_{th} has been evaluated from the expression given in equation (29).

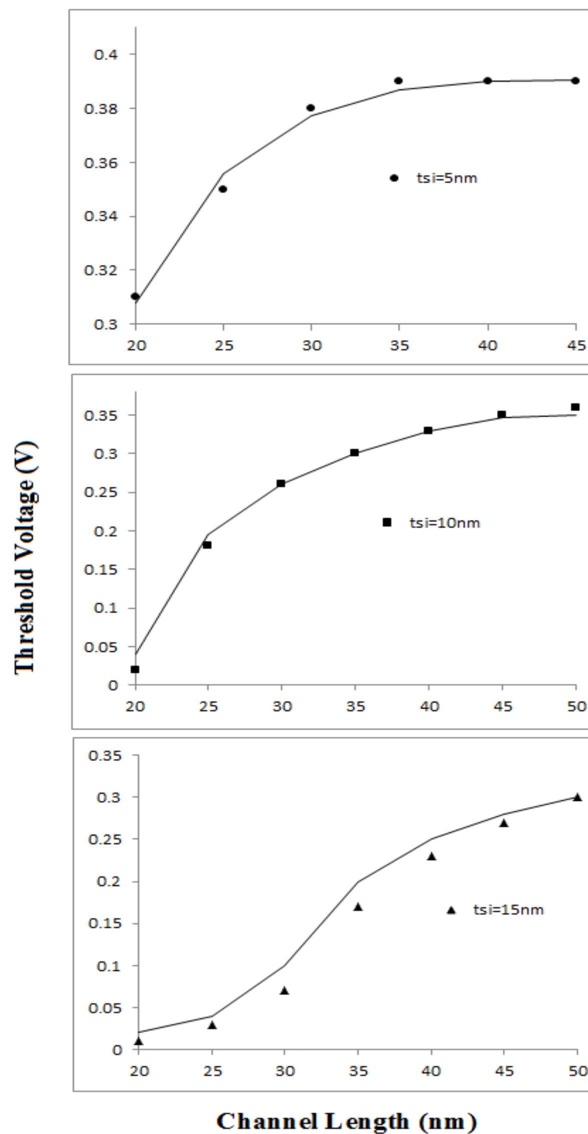

Figure 4-2: Threshold voltage of undoped DG MOSFET at different silicon thickness and channel length. The symbols are simulated values while the solid lines represent the analytical values.

4.3 Drain Current

To study the behavior and evaluate the characteristics of the DG MOSFET it is necessary to divide the transistor operation in two major regions and they are weak inversion region and strong inversion region. The current conduction mechanism from source to drain and the factors constituting current in these two regions are different as in weak inversion the current is due to diffusion because of few minority carriers and depletion region generated potential distribution and in strong inversion it is the drift current generated by the flow of inversion layer carriers under the electric field influence in the channel.

Figure 4-3and Figure 4-4 shows the characteristics of the symmetrical DG MOSFET for a channel length of 32nm and 45 nm respectively with zero series source to drain resistance by keeping the source and drain lateral length value to 5nm. The output characteristic shown in Figure 4-3(a) andFigure 4-4(a) is obtained at three different gate voltages V_g= 0.65, 0.8 and 1V. Similarly the linear and semi-logarithmic representation of the transfer characteristic shown in Figure 4-3 and Figure 4-4 (b) and (c) are obtained for drain voltages V_d= 0.02, 0.3 and 1V giving the model accuracy in both weak and strong inversion regions and for all range of drain voltage values. The threshold sheet charge carrier density used to define the threshold voltage is taken as $Q_{th} = 2.8 \times 10^{15} cm^{-3}$for evaluating the C-V characteristics of the DG MOSFET at both the channel lengths 32 nm and 45 nm. Agood agreement is achieved between the simulated and analytical results for both the channel lengths as seen through the results.

A finite source to drain series resistance significantly affects the device current-voltage characteristics. In Figure 4-5the current-voltage characteristics of the analytical model is examined for a series resistance of $R_{sd} = 180\,\Omega$ by taking the source/drain lateral length to be 50nm. Figure 4-5(a) shows the output characteristic of the device for different gate voltages while Figure 4-5(b) and (c) shows the linear and semi-logarithmicrepresentation of the transfer characteristic at different gate voltage to verify the results for all regions of operation of a MOSFET. The analytical model and simulated results are obtained for a device of channel length 32nm. The proposed model is thus validated for different channel lengths and different series resistance in all regions of operation showing remarkable agreement with the simulated results.

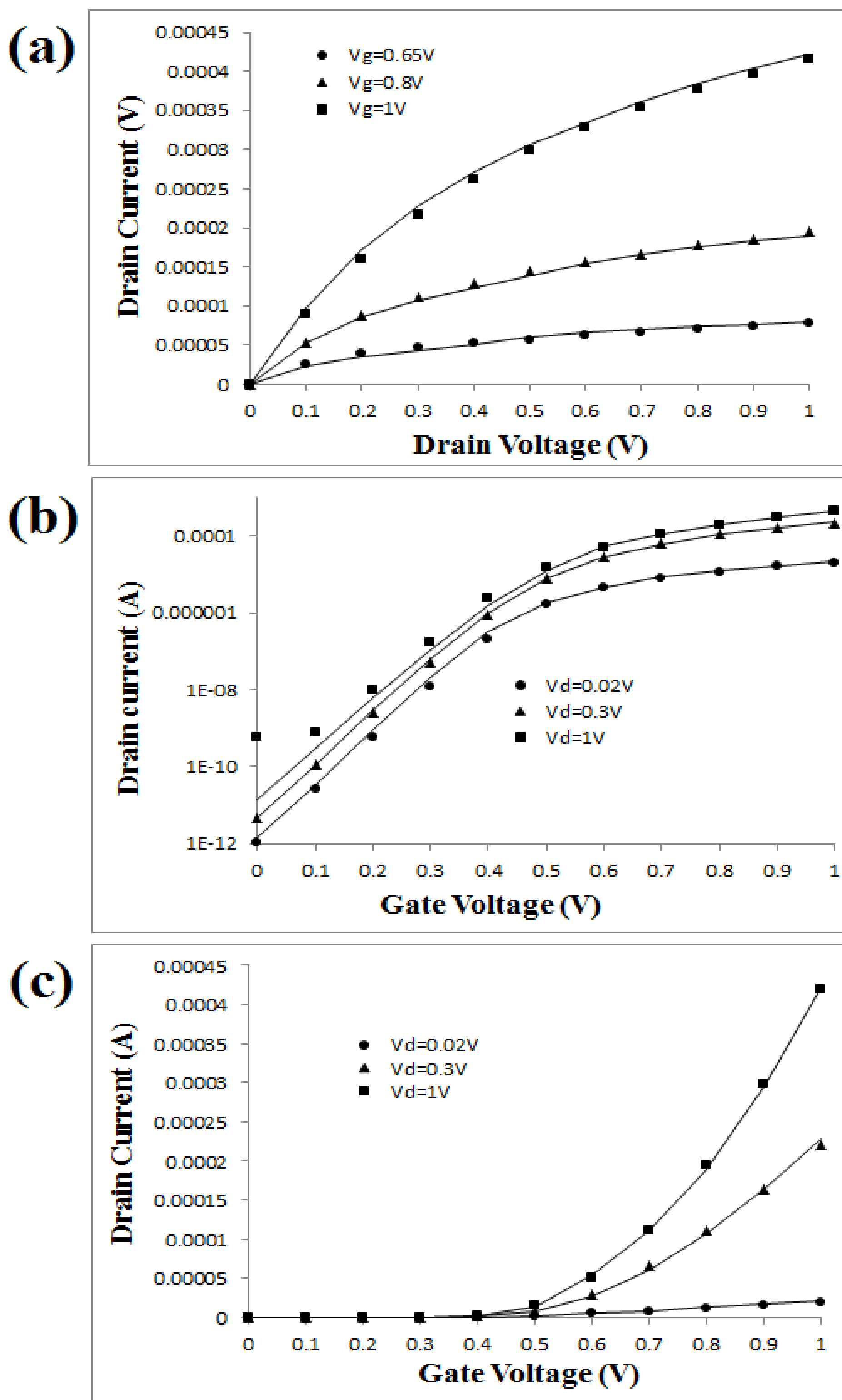

Figure 4-3: Simulated(symbols) and model (solid lines) (a) output characteristic (b) transfer characteristic in linear representation (c) semi-logarithmic representation of the transfer characteristics of symmetrical DG MOSFET for channel length L=32nm, t_{si}=10nm, t_{ox}=2nm and R_{sd}=0.

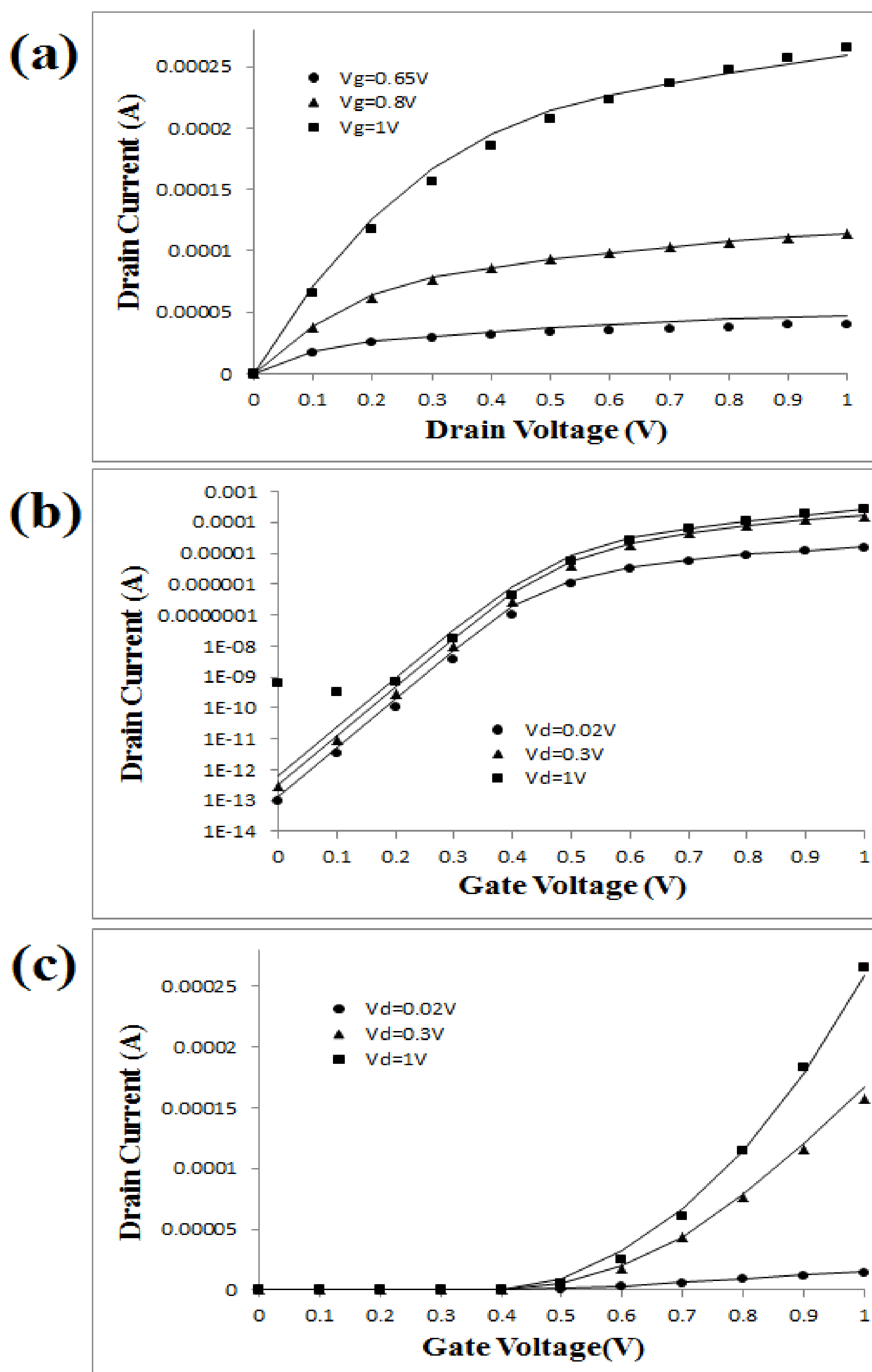

Figure 4-4: Simulated(symbols) and model (solid lines) (a) output characteristic (b) transfer characteristic in linear representation (c) semi-logarithmic representation of the transfer characteristics of symmetrical DG MOSFET for channel length L=45nm, t_{si}=10nm, t_{ox}=2nm and R_{sd}=0.

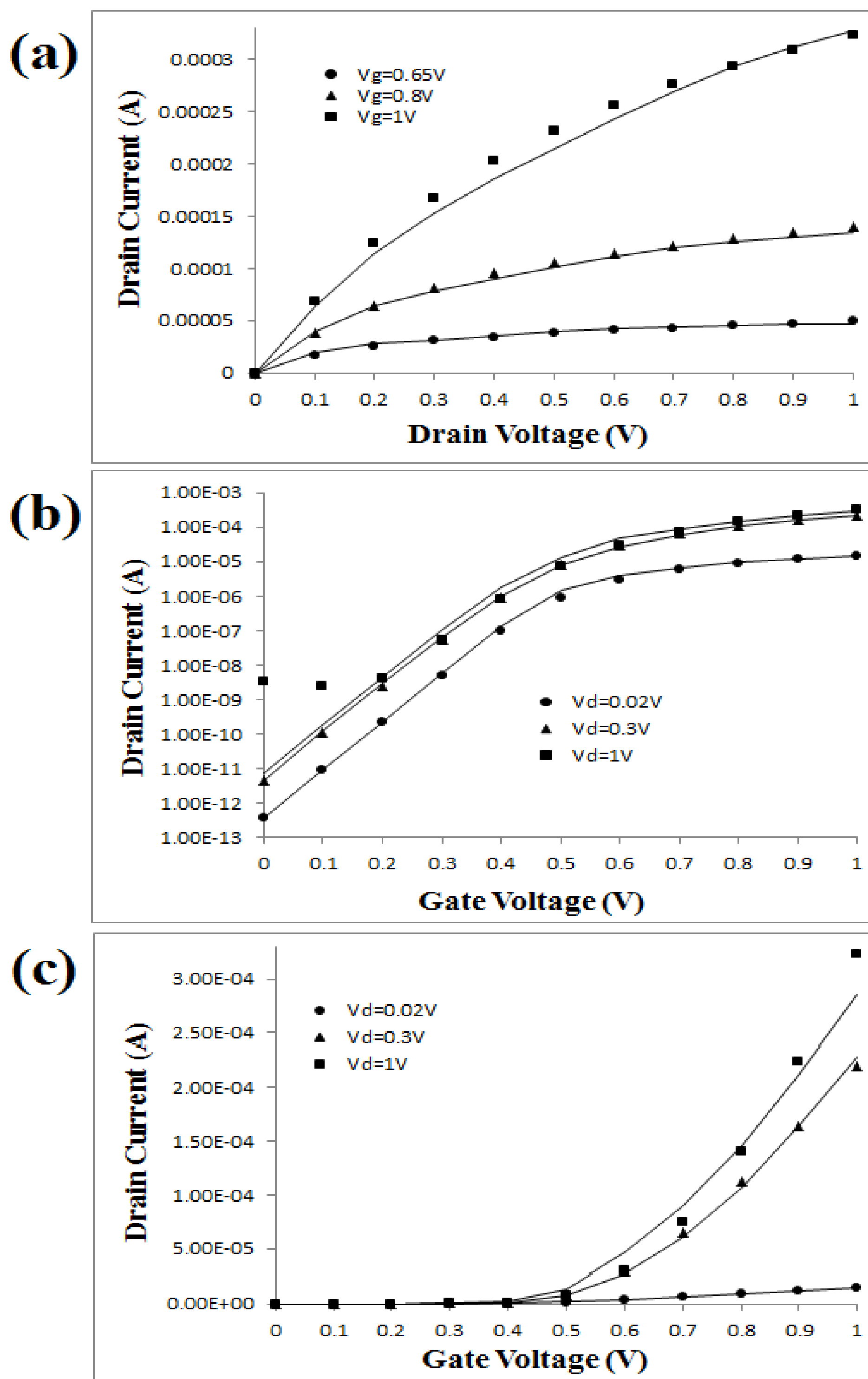

Figure 4-5: Simulated(symbols) and model (solid lines) (a) output characteristic (b) transfer characteristic in linear representation (c) semi-logarithmic representation of the transfer characteristics of symmetrical DG MOSFET for channel length L=32nm, t_{si}=10nm, t_{ox}=2nm and R_{sd}=180 ohm.

4.4 Fixed Oxide Charge

The obtained current model is also studied by considering the effect of fixed oxide charges present in thin oxide layers and Figure 4-6 shows the effect offixed oxide charge on the modeled and simulated drain current for different gate voltages. The drain current increases at higher values of fixed oxide charges due to decrease of the threshold voltage at these fixed oxide charges values.

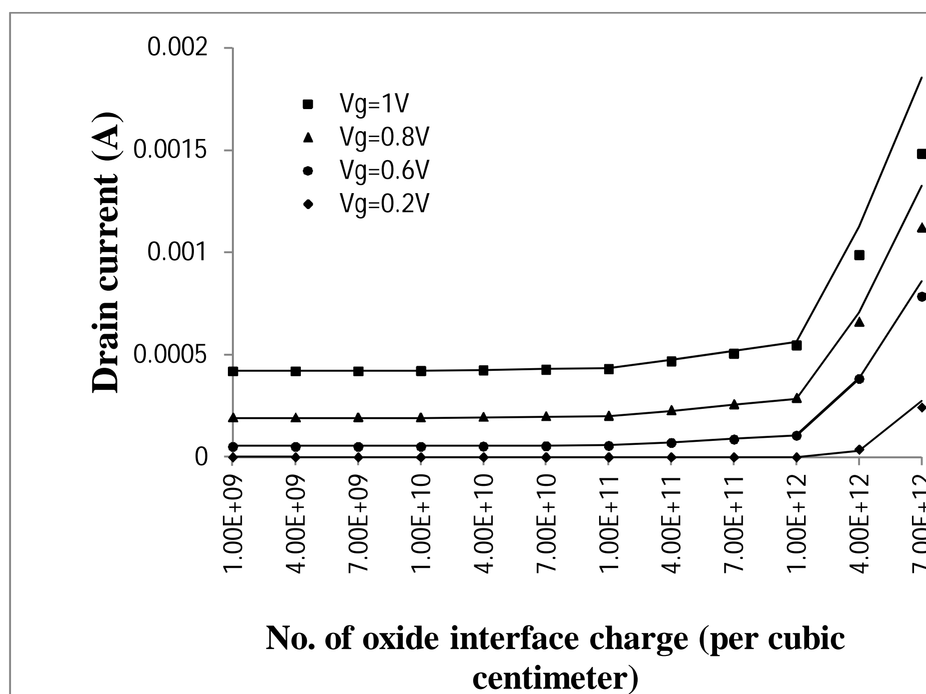

Figure 4-6: Drain current variation simulated (symbol) and model (solid lines) with the oxide interface charge at different gate voltages

Chapter 5

5 Conclusion and Future Work

5.1 Conclusion

A 2D potential distribution based subthreshold slope and threshold voltage expressions have been obtained and embedded within the drain current model of symmetrical DG-MOSFET. These analytical model expressions are verified with the simulated results of SILVACO (Atlas) TCAD tool.

The subtheshold slope and threshold voltage variation for different channel length devices have been obtained. The output and transfer characteristics of the proposed drain current model at channel lengths of 32 nm and 45 nm with and without series source/drain resistance are compared with the simulation results. Finally, the effect of fixed oxide trap charges have been observed and compared with simulation results. The developed drain current model is in good agreement with the simulated results and may be feasible for compact model applications for well-designed devices with L/t_{si} ratio value greater than 2.

5.2 Scope for future work

This problem has several possible extensions that could be attempted as ongoing research work. Some specific recommendations based on the present work are as follows:

1. Present study can be well extended by adding other SCEs which are not considered such as GIDL, hot carrier effect etc and by taking mobility degradation and velocity saturation into consideration.
2. The present model follows classical drift-diffusion approach and can be studied for semi-classical modelingas well.
3. Quantum effects such as quantum confinement and nanoscale effects can also be incorporated into the model so that a more précised results are obtained.

APPENDIX A

A.1 SILVACO CODE for FD-DG MOSFET Transfer Characteristics for Channel length L=32nm and lateral Source/Drain length is 1nm

```
COMMENT    Program begins
go atlas

COMMENT    Specifying rectangular MESH
meshspace.mult=1.0

COMMENT  X-MESH with channel length 32nm and Source/Drain length 1nm
x.meshloc= -0.001spac=0.0025
x.meshloc=0.000spac=0.0025
x.meshloc=0.032   spac=0.0025
x.meshloc= 0.033spac=0.0025

COMMENT  Y-MESH with oxide thickness 2nm and silicon film thickness 10nm
y.meshloc=-0.002   spac=0.001
y.meshloc=0.000spac=0.0001
y.meshloc=0.010 spac=0.001
y.meshloc=0.012 spac=0.001

COMMENTDefining regions
regionnum=1 y.min=-0.002 y.max=0.000  x.min=0.000x.max=0.032 oxide
regionnum=2 y.min=0.000y.max=0.010 x.min=-0.001x.max=0.033 silicon
regionnum=3 y.min=0.010  y.max=0.012 x.min=0.000x.max=0.032 oxide
regionnum=4 x.min=-0.001x.max= 0.000    y.min=-0.002 y.max=0.000 oxide
regionnum=5 x.min=0.032x.max=0.033y.min=-0.002 y.max=0.000 oxide
regionnum=6 x.min=-0.001x.max=0.000   y.min=0.010 y.max=0.012 oxide
regionnum=7 x.min=0.032 x.max=0.033y.min=0.010 y.max=0.012 oxide

COMMENTDefining electrodes
electrode    name=gate   x.min=0.000x.max=0.032 y.min=-0.002 y.max=-0.002
electrode    name=gate2  x.min=0.000  x.max=0.032 y.min=0.012 y.max=0.012
electrode    name=source x.min=-0.001x.max=0.000  y.min=0.000y.max=0.000
electrode    name=drain x.min=0.032x.max=0.033y.min=0.000y.max=0.000

COMMENTDefining doping concentrations
doping uniform conc=1e15 p.typex.min=0 x.max=0.032 y.min=0 y.max=0.010
doping uniform conc=1e22 n.typex.min=-0.001x.max=-0.000001 y.min=0 y.max=0.010
doping uniform conc=1e22 n.typex.min=0.03299999 x.max=0.033y.min=0 y.max=0.010

COMMENT Saving the structure obtained from above code
saveoutf=dd_mos.str

COMMENT Defining constant mobility for silicon as 500cm²/Vs
MATERIAL MATERIAL=silicon MUN=500
```

COMMENT Gate workfunction specification and connecting both gates together
CONTACT NAME=gate WORKFUNCTION=4.74
CONTACT NAME=gate2 WORKFUNCTION=4.74 COMMON=gate short

COMMENT Saving the structure and plotting it on tonyplot
structoutfile=stucture_dg.str
tonyplotstructure_dg.str

COMMENT Solving method specification

METHOD GUMMEL NEWTON trap

SOLVE init

save outf=dd_dgmos_1.log

COMMENT Drain voltages specification to obtain family of curves in output characteristic
solvevdrain=0.02OUTF=solve_vdrain1
solvevdrain=0.30OUTF=solve_vdrain2
solvevdrain=1.00OUTF=solve_vdrain3

COMMENT Ramp gate voltage
LOAD INFILE=solve_vdrain1
LOG OUTFILE=dgmos_vdrain_sweep1.log
SOLVE NAME=drain VGATE=0 VFINAL=1 VSTEP=0.1

LOAD INFILE=solve_vdrain2
LOG OUTFILE=dgmos_vdrain_sweep2.log
SOLVE NAME=gate VGATE=0 VFINAL=1.0 VSTEP=0.1

LOAD INFILE=solve_vdrain3
LOG OUTFILE=dgmos_vdrain_sweep3.log
SOLVE NAME=gate VGATE=0 VFINAL=1.0 VSTEP=0.1

Quit

A.2 SILVACO CODE for FD-DG MOSFET Output Characteristic for Channel length L=32nm and lateral Source/Drain length is 1nm

```
COMMENT    Program begins
go atlas

COMMENT    Specifying rectangular MESH
meshspace.mult=1.0

COMMENT  X-MESH with channel length 32nm and Source/Drain length 1nm
x.meshloc= -0.001spac=0.0025
x.meshloc=0.000spac=0.0025
x.meshloc=0.032   spac=0.0025
x.meshloc=  0.033    spac=0.0025

COMMENT  Y-MESH with oxide thickness 2nm and silicon film thickness 10nm
y.meshloc=-0.002   spac=0.001
y.meshloc=0.000spac=0.0001
y.meshloc=0.010 spac=0.001
y.meshloc=0.012 spac=0.001

COMMENTDefining regions
regionnum=1 y.min=-0.002 y.max=0.000  x.min=0.000x.max=0.032 oxide
regionnum=2 y.min=0.000y.max=0.010 x.min= -0.001x.max= 0.033 silicon
regionnum=3 y.min=0.010  y.max=0.012 x.min=0.000x.max=0.032 oxide
regionnum=4 x.min= -0.001x.max= 0.000    y.min=-0.002 y.max=0.000 oxide
regionnum=5 x.min=0.032x.max= 0.033y.min=-0.002 y.max=0.000 oxide
regionnum=6 x.min= -0.001 x.max=0.000   y.min=0.010 y.max=0.012 oxide
regionnum=7 x.min=0.032 x.max= 0.033  y.min=0.010 y.max=0.012 oxide

COMMENTDefining electrodes
electrode    name=gate   x.min=0.000x.max=0.032 y.min=-0.002 y.max=-0.002
electrode    name=gate2  x.min=0.000  x.max=0.032 y.min=0.012 y.max=0.012
electrode    name=source x.min=-0.001  x.max=0.000  y.min=0.000y.max=0.000
electrode    name=drain x.min=0.032x.max=0.033  y.min=0.000y.max=0.000

COMMENTDefining doping concentrations
doping uniform conc=1e15 p.typex.min=0 x.max=0.032 y.min=0 y.max=0.010
doping uniform conc=1e22 n.typex.min=-0.001x.max=-0.000001 y.min=0 y.max=0.010
doping uniform conc=1e22 n.typex.min=0.03299999 x.max=0.033y.min=0 y.max=0.010

COMMENT Saving the structure obtained from above code
saveoutf=dd_mos.str

COMMENT Defining constant mobility for silicon as 500cm²/Vs
MATERIAL MATERIAL=silicon MUN=500

COMMENT Gate workfunction specification and connecting both gates together
CONTACT NAME=gate WORKFUNCTION=4.74
CONTACT NAME=gate2 WORKFUNCTION=4.74 COMMON=gate short
```

COMMENT Saving the structure and plotting it on tonyplot
structoutfile=stucture_dg.str
tonyplotstructure_dg.str

COMMENT Solving method specification

METHOD GUMMEL NEWTON trap

SOLVE init

save outf=dd_dgmos_1.log

COMMENT Gate voltages specification to obtain family of curves in output characteristic
solvevgate=0.65 OUTF=solve_vgate1
solvevgate=0.80OUTF=solve_vgate2
solvevgate=1.00OUTF=solve_vgate3

COMMENT Ramp drain voltage
LOAD INFILE=solve_vgate1
LOG OUTFILE=dgmos_vgate_sweep1.log
SOLVE NAME=drain VDRAIN=0 VFINAL=1 VSTEP=0.1

LOAD INFILE=solve_vgate2
LOG OUTFILE=dgmos_vgate_sweep2.log
SOLVE NAME=gate VDRAIN=0 VFINAL=1.0 VSTEP=0.1

LOAD INFILE=solve_vgate3
LOG OUTFILE=dgmos_vgate_sweep3.log
SOLVE NAME=gate VDRAIN=0 VFINAL=1.0 VSTEP=0.1

Quit

A.3 SILVACO CODE for FD-DG MOSFET Output Characteristics for Channel length L=32nm and lateral Source/Drain length is 50nm

```
COMMENT    Program begins
go atlas

COMMENT    Specifying rectangular MESH
meshspace.mult=1.0

COMMENT  X-MESH with channel length 32nm and Source/Drain length 50nm
x.meshloc= -0.05   spac=0.0025
x.meshloc=0.000spac=0.0025
x.meshloc=0.032   spac=0.0025
x.meshloc= 0.082   spac=0.0025

COMMENT  Y-MESH with oxide thickness 2nm and silicon film thickness 10nm
y.meshloc=-0.002   spac=0.001
y.meshloc=0.000spac=0.0001
y.meshloc=0.010 spac=0.001
y.meshloc=0.012 spac=0.001

COMMENTDefining regions
regionnum=1 y.min=-0.002 y.max=0.000  x.min=0.000x.max=0.032 oxide
regionnum=2 y.min=0.000y.max=0.010 x.min=-0.050 x.max=0.082 silicon
regionnum=3 y.min=0.010  y.max=0.012 x.min=0.000x.max=0.032 oxide
regionnum=4 x.min=-0.050 x.max= 0.000    y.min=-0.002 y.max=0.000 oxide
regionnum=5 x.min=0.032x.max=0.082 y.min=-0.002 y.max=0.000 oxide
regionnum=6 x.min=-0.050x.max=0.000   y.min=0.010 y.max=0.012 oxide
regionnum=7 x.min=0.032 x.max=0.082 y.min=0.010 y.max=0.012 oxide

COMMENTDefining electrodes
electrode    name=gate   x.min=0.000x.max=0.032 y.min=-0.002 y.max=-0.002
electrode    name=gate2  x.min=0.000  x.max=0.032 y.min=0.012 y.max=0.012
electrode    name=source x.min=-0.050 x.max=0.000  y.min=0.000y.max=0.000
electrode    name=drain x.min=0.032 x.max=0.082 y.min=0.000y.max=0.000

COMMENTDefining doping concentrations
doping uniform conc=1e15 p.typex.min=0 x.max=0.032 y.min=0 y.max=0.010
doping uniform conc=1e22 n.typex.min=-0.050 x.max=-0.000001 y.min=0 y.max=0.010
doping uniform conc=1e22 n.typex.min=0.03299999 x.max=0.082 y.min=0 y.max=0.010

COMMENT Saving the structure obtained from above code
saveoutf=dd_mos.str

COMMENT Defining constant mobility for silicon as 500cm²/Vs
MATERIAL MATERIAL=silicon MUN=500

COMMENT Gate workfunction specification and connecting both gates together
CONTACT NAME=gate WORKFUNCTION=4.74
CONTACT NAME=gate2 WORKFUNCTION=4.74 COMMON=gate short
```

COMMENT Saving the structure and plotting it on tonyplot
structoutfile=stucture_dg.str
tonyplotstructure_dg.str

COMMENT Solving method specification

METHOD GUMMEL NEWTON trap

SOLVE init

save outf=dd_dgmos_1.log

COMMENT Gate voltages specification to obtain family of curves in output characteristic
solvevgate=0.65 OUTF=solve_vgate1
solvevgate=0.80OUTF=solve_vgate2
solvevgate=1.00OUTF=solve_vgate3

COMMENT Ramp drain voltage
LOAD INFILE=solve_vgate1
LOG OUTFILE=dgmos_vgate_sweep1.log
SOLVE NAME=drain VDRAIN=0 VFINAL=1 VSTEP=0.1

LOAD INFILE=solve_vgate2
LOG OUTFILE=dgmos_vgate_sweep2.log
SOLVE NAME=gate VDRAIN=0 VFINAL=1.0 VSTEP=0.1

LOAD INFILE=solve_vgate3
LOG OUTFILE=dgmos_vgate_sweep3.log
SOLVE NAME=gate VDRAIN=0 VFINAL=1.0 VSTEP=0.1

Quit

A.4 SILVACO CODE for FD-DG MOSFET Transfer Characteristics for Channel length L=32nm and lateral Source/Drain length is 50nm

```
COMMENT    Program begins
go atlas

COMMENT    Specifying rectangular MESH
meshspace.mult=1.0

COMMENT  X-MESH with channel length 32nm and Source/Drain length 50nm
x.meshloc= -0.05   spac=0.0025
x.meshloc=0.000spac=0.0025
x.meshloc=0.032   spac=0.0025
x.meshloc= 0.082   spac=0.0025

COMMENT  Y-MESH with oxide thickness 2nm and silicon film thickness 10nm
y.meshloc=-0.002   spac=0.001
y.meshloc=0.000spac=0.0001
y.meshloc=0.010 spac=0.001
y.meshloc=0.012 spac=0.001

COMMENTDefining regions
regionnum=1 y.min=-0.002 y.max=0.000  x.min=0.000x.max=0.032 oxide
regionnum=2 y.min=0.000y.max=0.010 x.min=-0.050 x.max=0.082 silicon
regionnum=3 y.min=0.010  y.max=0.012 x.min=0.000x.max=0.032 oxide
regionnum=4 x.min=-0.050 x.max= 0.000    y.min=-0.002 y.max=0.000 oxide
regionnum=5 x.min=0.032x.max=0.082 y.min=-0.002 y.max=0.000 oxide
regionnum=6 x.min=-0.050x.max=0.000   y.min=0.010 y.max=0.012 oxide
regionnum=7 x.min=0.032 x.max=0.082 y.min=0.010 y.max=0.012 oxide

COMMENTDefining electrodes
electrode    name=gate   x.min=0.000x.max=0.032 y.min=-0.002 y.max=-0.002
electrode    name=gate2  x.min=0.000  x.max=0.032 y.min=0.012 y.max=0.012
electrode    name=source x.min=-0.050 x.max=0.000  y.min=0.000y.max=0.000
electrode    name=drain x.min=0.032 x.max=0.082 y.min=0.000y.max=0.000

COMMENTDefining doping concentrations
doping uniform conc=1e15 p.typex.min=0 x.max=0.032 y.min=0 y.max=0.010
doping uniform conc=1e22 n.typex.min=-0.050 x.max=-0.000001 y.min=0 y.max=0.010
doping uniform conc=1e22 n.typex.min=0.03299999 x.max=0.082 y.min=0 y.max=0.010

COMMENT Saving the structure obtained from above code
saveoutf=dd_mos.str

COMMENT Defining constant mobility for silicon as 500cm²/Vs
MATERIAL MATERIAL=silicon MUN=500

COMMENT Gate workfunction specification and connecting both gates together
CONTACT NAME=gate WORKFUNCTION=4.74
CONTACT NAME=gate2 WORKFUNCTION=4.74 COMMON=gate short
```

COMMENT Saving the structure and plotting it on tonyplot
structoutfile=stucture_dg.str
tonyplotstructure_dg.str

COMMENT Solving method specification

METHOD GUMMEL NEWTON trap

SOLVE init

save outf=dd_dgmos_1.log

*COMMENT*Drain voltages specification to obtain family of curves in output characteristic
solvevdrain=0.02OUTF=solve_vdrain1
solvevdrain=0.30OUTF=solve_vdrain2
solvevdrain=1.00OUTF=solve_vdrain3

COMMENT Ramp gate voltage
LOAD INFILE=solve_vdrain1
LOG OUTFILE=dgmos_vdrain_sweep1.log
SOLVE NAME=drain VGATE=0 VFINAL=1 VSTEP=0.1

LOAD INFILE=solve_vdrain2
LOG OUTFILE=dgmos_vdrain_sweep2.log
SOLVE NAME=gate VGATE=0 VFINAL=1.0 VSTEP=0.1

LOAD INFILE=solve_vdrain3
LOG OUTFILE=dgmos_vdrain_sweep3.log
SOLVE NAME=gate VGATE=0 VFINAL=1.0 VSTEP=0.1

Quit

APPENDIX B

B.1 MATLAB CODE of FD-DG MOSFET output characteristics obtained with proposed Drain Current Model t

```
clearall;
clc;

VT= 26e-3 ;%thermal voltage in (V)
ni= 1.45e16 ;                  %intrinsic concentration in (1/m^3)
q= 1.6e-19 ;%electronic charge (C)
esi= 1.05315e-10;              %silicon dielectric constant=11.7 multiplied with e0=8.85e-12 (F/m)
eox= 3.4515e-11;     %oxide dielectric constant=3.9 multiplied with e0=8.85e-12  (F/m)
tox=2.0e-9;               %oxide thickness (m)
tsi=10.0e-9;                      % silicon thickness (m)
T=300;                         % room temperature (K)
K=1.381e-23;                     %boltzmanconstant(J/K)
W=50e-9;                       %   width of channel (m)
L=32e-9;                       %length of channel (m)
Nd=1e26;                        %doping concentration of source/drain (1/m^3)
Na=1e21;                        %doping concentration of channel (1/m^3)
u0=500e-4;                     % mobility (m^2/Vs)
Vbi= VT*log((Na*Nd)/ni.^2) %built in potential of source/drain and channel junction (V)
FPp=VT*log(Na/ni); %fermi potential of bulk(i.e. ptype substrate)(V)
Vfb1= - (VT*log(Na/ni)); %mid band gap metal flat band voltage (V)
Nf=5e16;%    oxide trap charge density (1/m^3)
Cox=eox/tox; %    Oxide capacitance per unit area (F/m^2)
OIC=(q*Nf)/Cox;  %oxide charges (C)
Vfb=Vfb1-OIC;                         %    flatband voltage (V)
I= esi*tox*tsi;
J= 2*eox;
M= eox*3*tsi;
N= esi*16*tox;
lamda= sqrt((I/J)*(1+(M/N)));       % Natural length (m)
c=1;
for Vg=0:0.01:1
if (Vg==0.65 || Vg==0.8 || Vg==1)
e=1;
forVd=0:0.1:1

%threshold voltage calculation

Qth=(2e11+(0.9e10/L))*1e4;         %  threshold voltage sheet charge carrier density (1/m^3)
   Ai3=(q*Na*((esi*tox*tsi)+(0.75*eox*(tsi.^2))))/(2*eox*esi);
   Xt1=VT*log(Qth/(ni*tsi));
   Xt2=L/lamda;
Zt=exp(Xt2)-1;
   At=(exp(4*Xt2)-(2*exp(2*Xt2))+1)/(Zt.^4);
```

```
Bt=((2*exp(Xt2/2))*(1+exp(Xt2)))/(Zt.^2);
   Ct=((2*exp(3*Xt2))-(4*exp(Xt2*2))+(2*exp(Xt2)))/(Zt.^4);

   Vth=Vfb+Ai3+((At*Xt1)-(Bt*sqrt(Vbi-Xt1)*sqrt(Vbi+Vd-Xt1))-(Ct*((2*Vbi)+Vd)));
%threshold voltage short channel

dVth=((At-1)*Xt1)-(Bt*sqrt(Vbi-Xt1)*sqrt(Vbi+Vd-Xt1))-(Ct*(2*Vbi+Vd));
% threshold voltage roll-off

%Vthcaln ends

% subthreshold region calculation

   Xs1=(exp((2*L)/lamda))-1;
   A3=Vg-Vfb-Ai3;
   Xs2=Vbi-A3;
   Xs3=(exp(L/lamda))-1;
Xs=(Vd*Xs1)/(((Xs2*Xs3)-Vd).^2);
xs=((Xs2*Xs3)+(Vd*(exp(L/lamda))))/((Xs2*Xs3)-Vd);
   a=xs.^(-0.5);
   b=xs.^(-1.5);
   c=exp((3*L)/(2*lamda));
   d=exp(L/(2*lamda));
   Xss1=0.5*Xs*(a-b);
   Xss2=(-0.5)*Vd*Xs*((b*c)+(a*d));
   K1=1/((exp((2*L)/lamda))-1);
   K2=c-d;
   Ps=(xs.^(-0.5))+(xs.^0.5);
   Xss3=1+K1*((K2*(((Vbi-A3)*Xss1)-Ps))+Xss2) ;
n =1/Xss3;
ss=Vt*log(10)*n;

%subthreshold slope calc ends

% Channel length modulation calculation
u =1;
O= lamda/(L);
A= u-sqrt(O);
P= 2*Vths;
R= (Vg/Vths).^2;
Vgeff= P+((Vg-P)*tanh(R));
S=(1.5*Vd)/Vgeff;
Vdeff= Vd*tanh(S*S);
Fclm= 1+((O.^A)*(Vdeff/(Vgeff-Vths)));

% Channel length modulation calculation ends

%  drain current calculation

%series resistance parameter calculation
```

```
rsd=180;
r= (4*W*ueff*Cox*rsd*(Vg-Vth))/L;
Rsd=1/(1+r);

% calculation ends

%DIBL parameter calculation

D=0.4;
neta= (esi*D)/(Cox*L);
nw= ((Vg-Vths)/(n*VT))+((neta*Vd)/VT);
A1= exp(nw);

% calculation ends

B= 1-exp(-Vd/VT);

%   subthreshold current equation

Isub(e)=((u0*2*W*eox*(Vt*Vt)*(exp(nw))*A1*B)/(L*tox))*Fclm;

%strong inversion drain equation

D1= (ni*ni*esi)/(2*K*T*Na);
E= (q*tox)/eox;
F= sqrt(D1);
G=2*Vt;
H=(eox*tsi)/(2*esi*tox);
Cs= (Vg+dVth-Vfb);
Cd= (Vg+dVth-Vfb-Vd);
qis= H*lambertw(E*F*exp(Cs/G));
qid= H*lambertw(E*F*exp(Cd/G));

U=(u0*2*W*2*esi)/(L*tsi);
U1=G*G;
U2= (esi*tox)/(eox*tsi);

Idsi(e)= U*U1*((qis-qid)+(U2*((qis.^2)-(qid.^2))))*Fclm*Rsd;
x=1.2*Vd;
m=1.9-sqrt(x);
%  total drain current
Id(e)=(Isub(e)*Idsi(e))/(((Isub(e).^m)+(Idsi(e).^m)).^(1/m));
e=e+1;
end
Vd=0:0.1:1
Plot(Vd,Id);
end
 c=c+1;
end
```

B.2 MATLAB CODE of FD-DG MOSFET transfer characteristics obtained with proposed Drain Current Model t

```
clearall;
clc;

VT = 26e-3 ;%thermal voltage in (V)
ni= 1.45e16 ;                    %intrinsic concentration in (1/m^3)
q= 1.6e-19 ;%electronic charge (C)
esi= 1.05315e-10;                 %silicon dielectric constant=11.7 multiplied with e0=8.85e-12 (F/m)
eox= 3.4515e-11;    %oxide dielectric constant=3.9 multiplied with e0=8.85e-12  (F/m)
tox=2.0e-9;                  %oxide thickness (m)
tsi=10.0e-9;                          % silicon thickness (m)
T=300;                         % room temperature (K)
K=1.381e-23;                     %boltzmanconstant(J/K)
W=50e-9;                       %   width of channel (m)
L=32e-9;                        %length of channel (m)
Nd=1e26;                         %doping concentration of source/drain (1/m^3)
Na =1e21;                         %doping concentration of channel (1/m^3)
u0=500e-4;                      % mobility (m^2/Vs)
Vbi= VT*log((Na*Nd)/ni.^2) %built in potential of source/drain and channel junction (V)
FPp=VT*log(Na/ni); %fermi potential of bulk(i.e. ptype substrate)(V)
Vfb1= - (VT*log(Na/ni)); %mid band gap metal flat band voltage (V)
Nf=5e16;%    oxide trap charge density (1/m^3)
Cox=eox/tox; %    Oxide capacitance per unit area (F/m^2)
OIC=(q* Nf)/Cox;  %oxide charges (C)
Vfb=Vfb1-OIC;  %flatband voltage (V)
I= esi*tox*tsi;
J= 2*eox;
M= eox*3*tsi;
N= esi*16*tox;
lamda= sqrt((I/J)*(1+(M/N)));      % Natural length (m)

%   plotting family of curves
c=1;
forVd=0:0.01:1
if (Vd==0.02 || Vd==0.3 || Vd==1)
e=1;
for Vg=0:0.1:1

%threshold voltage calculation

Qth=(2e11+(0.9e10/L))*1e4;         %  threshold voltage sheet charge carrier density (1/m^3)
   Ai3=(q*Na*((esi*tox*tsi)+(0.75*eox*(tsi.^2))))/(2*eox*esi);
   Xt1=VT*log(Qth/(ni*tsi));
   Xt2=L/lamda;
Zt=exp(Xt2)-1;
   At=(exp(4*Xt2)-(2*exp(2*Xt2))+1)/(Zt.^4);
Bt=((2*exp(Xt2/2))*(1+exp(Xt2)))/(Zt.^2);
```

```
    Ct=((2*exp(3*Xt2))-(4*exp(Xt2*2))+(2*exp(Xt2)))/(Zt.^4);

    Vth=Vfb+Ai3+((At*Xt1)-(Bt*sqrt(Vbi-Xt1)*sqrt(Vbi+Vd-Xt1))-(Ct*((2*Vbi)+Vd)));
%threshold voltage short channel

dVth=((At-1)*Xt1)-(Bt*sqrt(Vbi-Xt1)*sqrt(Vbi+Vd-Xt1))-(Ct*(2*Vbi+Vd));
% threshold voltage roll-off

%Vthcaln ends

% subthreshold region calculation

    Xs1=(exp((2*L)/lamda))-1;
    A3=Vg-Vfb-Ai3;
    Xs2=Vbi-A3;
    Xs3=(exp(L/lamda))-1;
Xs=(Vd*Xs1)/(((Xs2*Xs3)-Vd).^2);
xs=((Xs2*Xs3)+(Vd*(exp(L/lamda))))/((Xs2*Xs3)-Vd);
    a=xs.^(-0.5);
    b=xs.^(-1.5);
    c=exp((3*L)/(2*lamda));
    d=exp(L/(2*lamda));
    Xss1=0.5*Xs*(a-b);
    Xss2=(-0.5)*Vd*Xs*((b*c)+(a*d));
    K1=1/((exp((2*L)/lamda))-1);
    K2=c-d;
    Ps=(xs.^(-0.5))+(xs.^0.5);
    Xss3=1+K1*((K2*(((Vbi-A3)*Xss1)-Ps))+Xss2) ;
n =1/Xss3;
ss=Vt*log(10)*n;

%subthreshold slope calc ends

% Channel length modulation calculation
u =1;
O= lamda/(L);
A= u-sqrt(O);
P= 2*Vths;
R= (Vg/Vths).^2;
Vgeff= P+((Vg-P)*tanh(R));
S=(1.5*Vd)/Vgeff;
Vdeff= Vd*tanh(S*S);
Fclm= 1+((O.^A)*(Vdeff/(Vgeff-Vths)));

% Channel length modulation calculation ends

%  drain current calculation

%series resistance parameter calculation

rsd=180;
```

```
r= (4*W*ueff*Cox*rsd*(Vg-Vth))/L;
Rsd=1/(1+r);

% calculation ends

%DIBL parameter calculation

D=0.4;
neta= (esi*D)/(Cox*L);
nw= ((Vg-Vths)/(n*VT))+((neta*Vd)/VT);
A1= exp(nw);

% calculation ends

B= 1-exp(-Vd/VT);

%   subthreshold current equation

Isub(e)=((u0*2*W*eox*(Vt*Vt)*(exp(nw))*A1*B)/(L*tox))*Fclm;

%    strong inversion drain equation

D1= (ni*ni*esi)/(2*K*T*Na);
E= (q*tox)/eox;
F= sqrt(D1);
G=2*Vt;
H=(eox*tsi)/(2*esi*tox);
Cs= (Vg+dVth-Vfb);
Cd= (Vg+dVth-Vfb-Vd);
qis= H*lambertw(E*F*exp(Cs/G));
qid= H*lambertw(E*F*exp(Cd/G));

U=(u0*2*W*2*esi)/(L*tsi);
U1=G*G;
U2= (esi*tox)/(eox*tsi);

Idsi(e)= U*U1*((qis-qid)+(U2*((qis.^2)-(qid.^2))))*Fclm*Rsd;
x=1.2*Vd;
m=1.9-sqrt(x);

%  total drain current
Id(e)=(Isub(e)*Idsi(e))/(((Isub(e).^m)+(Idsi(e).^m)).^(1/m));
e=e+1;
end
 Vg=0:0.1:1
  Plot (Vg,Id);
%semilogy(Vg,Id)
end
 c=c+1;
end
```

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