PERFORMANCE ANALYSIS OF EFFECT OF ELECTRIC FIELD ON SINGLE-WALL CARBON NANOTUBES AS VLSI INTERCONNECTS

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VLSI Design

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DECLARATION

I hereby declare that the work which is being presented in this dissertation entitled, "PERFORMANCE ANALYSIS OF EFFECT OF ELECTRIC FIELD ON SINGLE-WALL CARBON NANOTUBES AS VLSI INTERCONNECTS" in partial fulfillment of the requirement for the award of degree of Master of Technology (VLSI DESIGN) submitted in Electronics and Communication Engineering Department at Thapar University, Patiala is an authentic record of my study carried out as under the guidance of Mr. Karamjit Singh (Assistant Professor), ECED and refers other researcher's work which are duly listed in the reference section.

Date: 13 July, 2014

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It is certified that the above statement made by the student is correct to the best of my knowledge and belief.

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ABSTRACT

For more than 30 years, the rate at which performance of silicon integrated circuits (IC) has improved is astonishing. The number of functions per chip has grown exponentially, thus dramatically scaling the IC which is threatened by physical limitation of copper-based electrical wires. To alleviate this problem, the most potential candidate for future ICs is carbon-nanotube (CNT) based interconnect schemes. CNT interconnects has the advantage of having a large electron mean free path, hence low resistance than copper interconnects. As interconnect material single-wall CNT (SWCNT) having higher conductivity is more preferable to the relatively lower conductivity multi-wall CNT (MWCNT). The high resistance associated with an isolated SWCNT necessitates the use of a bundle of SWCNTs. In this dissertation an efficient circuit-compatible RLC model for metallic SWCNT bundle is presented. Using this model, the performance of SWCNT-bundle interconnects is compared to copper wires. Results show that the bundles of SWCNTs having smaller value of signal delay and power delay product (PDP) achieve significantly better performance than copper interconnects at scaled technologies. Thus, SWCNT bundles can outperform copper for long intermediate and global interconnects. Influence of electric field on single walled carbon nanotube (SWCNT) bundle interconnects is studied in order to explore the electrical properties of SWCNT bundle. Voltage dependent equivalent circuit model is presented that capture various electron–phonon scattering mechanisms as a function of electric field. To estimate the performance of SWCNT bundle interconnects, signal delay and power dissipation is calculated based on field dependent model that results in improvement in the delay and power estimation accuracy compared to field independent model. Power delay product (PDP) of interconnect decides whether it has potential of being a reliable interconnect for the given technology. It is observed that power delay product of SWCNT bundle increases with increase in electric field but decreases with technology scaling showing that in low electric field regime, SWCNT bundle is a reliable alternative interconnect for future technologies in a high performance VLSI industry.

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LIST OF SYMBOLS

VDD	Positive supply voltage
Id	Drain current
h	Planck's Constant
d	Tube diameter
s	Spacing between two interconnects
Lo	Mean free path of electron
v_f	Fermi velocity
K_B	Boltzmann's Constant
Kp	PMOS process trans-conductance parameter
Kn	NMOS process trans-conductance parameter
W	Channel width
L	Channel length
μ_n	Mobility of electrons
μ_P	Mobility of holes
Cox	Oxide capacitance
Io	Bias current
V_T	Threshold voltage
V_{GS}	Gate to source voltage
V_{DS}	Drain to source voltage
λ	Channel length modulation parameter

ABBREVIATIONS

VLSI	Very Large Scale Integration
CNT	Carbon Nanotube
IC	Integrated Circuit
ITRS	International Technology Road map for semiconductors
RLC	Resistance, Inductance and Capacitance
SWCNT	Single Wall Carbon Nanotube
MWCNT	Multi Wall Carbon Nanotube
CU	Copper
SPICE	Simulation Program with Integrated Circuit Emphasis
MOSFET	Metal Oxide Semiconductor Field Effect Transistor
CMOS	Complementary Metal Oxide Semiconductor
NMOS	N-channel Metal Oxide Semiconductor
PMOS	P-channel Metal Oxide Semiconductor
MFP	Mean Free Path
PDP	Power Delay Product

CHAPTER 1

INTRODUCTION

INTERCONNECTS

A VLSI interconnect can be defined as thin film of conducting material which provides electrical connection on the silicon chip between two or more nodes formed in a circuit. Interconnects distribute clock and signal and also provide path for the ground and the power supply in an integrated circuit (IC) [1]. The current-carrying capacity along with capacitance, inductance and the parasitic resistance of the interconnect determines the performance of an IC to a large extent. Figure 1.1 shows the physical representation of interconnect geometry [2] with w denoting width, l and t denoting length and thickness respectively of the interconnect, s represents spacing between the two interconnects and h represents distance of the interconnect from the ground.

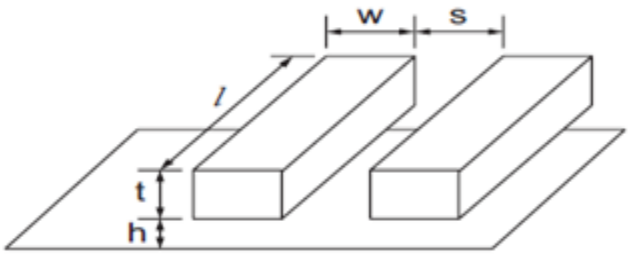

Figure 1.1: Physical representation of interconnect geometry [2].

Based on their length, interconnects can be classified as:

Local interconnects- Local interconnects are of shorter lengths ranging from 10um to 1000um and can connect nearby nodes. They usually connect emitters, collectors and bases in bipolar devices and gates, drains and sources in MOS devices. A local interconnect can also serve as gate electrode material for MOS technology. Since, local interconnects do not travel large distances , they can afford to have greater resistivity than the global interconnects [3]. But local interconnect must be able to withstand higher temperatures.

Semi-global interconnects- Semi-global interconnects are used for both long and short routes. Within a block, devices are connected through them [3]. Mid length interconnects

within a block used for communication are connected through these interconnects with typical lengths up to 300 to 400um.

Global interconnects- A global interconnect is quite long so that they are used to connect several nodes across a chip such as ground lines, clock lines, power supply etc with length varying from 400 to 1000um. They are always low resistant metals as they often travel over large distances to provide connection between different parts of the circuit and different devices [3].

The different levels of the interconnect hierarchy are shown in Figure 1.2(a) with dimensions of the local, semi-global and global interconnects shown in Figure 1.2(b) with technology scaling. Local interconnects are at the lowest level of the hierarchy used for connecting nearby nodes followed by semi-global interconnects at the next level connecting devices within functional block. Global interconnects are generally above the local interconnect level for all of the interconnect levels which are used to connect various functional blocks.

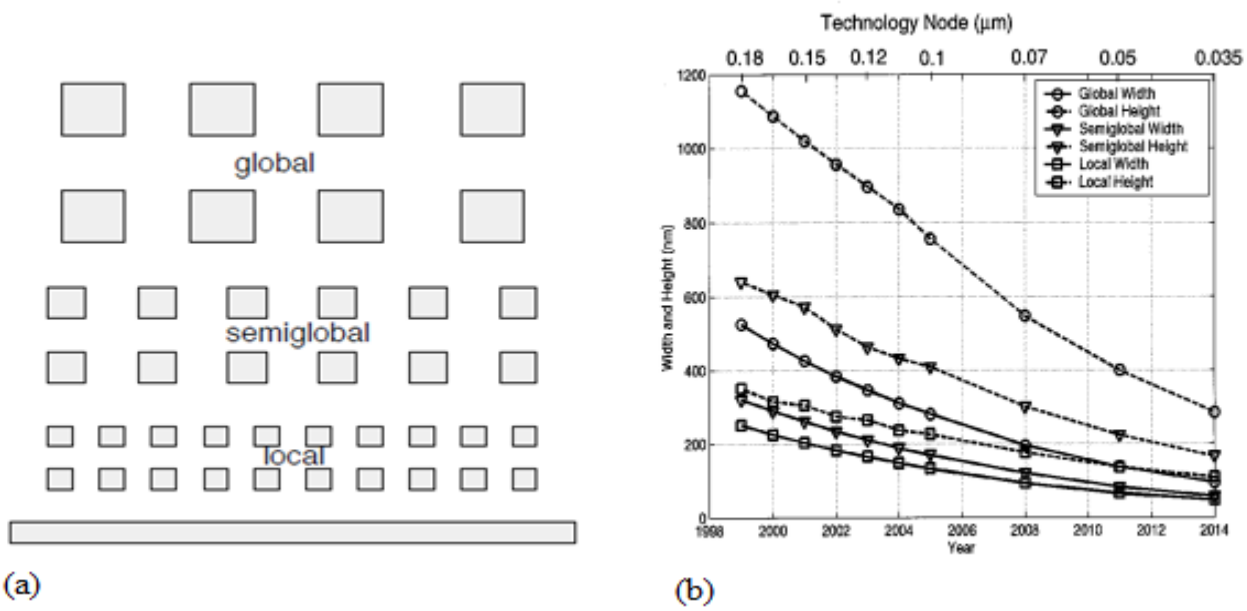

Figure 1.2: (a) A 3- tier architecture of interconnect [4] (b) ITRS '13 dictated dimensions for global, semi-global and local interconnects [5].

Due to the great enhancement in the development of information technology, it has driven the semiconductor industry to evolve at a rate which is incredible. Faster device switching

speed, increased functional density, greater number of transistors and larger chip size is the result of the growing demand in integrated circuits (ICs) for higher performance. Consequently, the communication between devices and circuit blocks which is supported by on-chip interconnects is a challenging problem and is becoming more complex [4]. Due to overall chip size remaining constant or increasing marginally with increase in number of functional modules placed on chip, the interconnects used for connection are not scaling down at the same rate with the aggressive scaling of VLSI technology. A VLSI interconnect can significantly be limit the performance of advanced systems by acting as a communication media between the functional units of a chip, thus playing an increasingly important role. In continued improvements in IC density and speed, the performance of these interconnects have really become a great bottleneck [6]. As mentioned by the International Technology Roadmap for Semiconductors (ITRS), interconnect RC delay dominates the chip performance of advanced technology nodes as compared to gate delay as shown in Figure 1.3. Considerable work has already gone into overcoming interconnect limitations to mitigate the adverse scaling trend in case of signal propagation delay (RC). The International Technology Roadmap for Semiconductors (ITRS) emphasizes specially on the need for high-

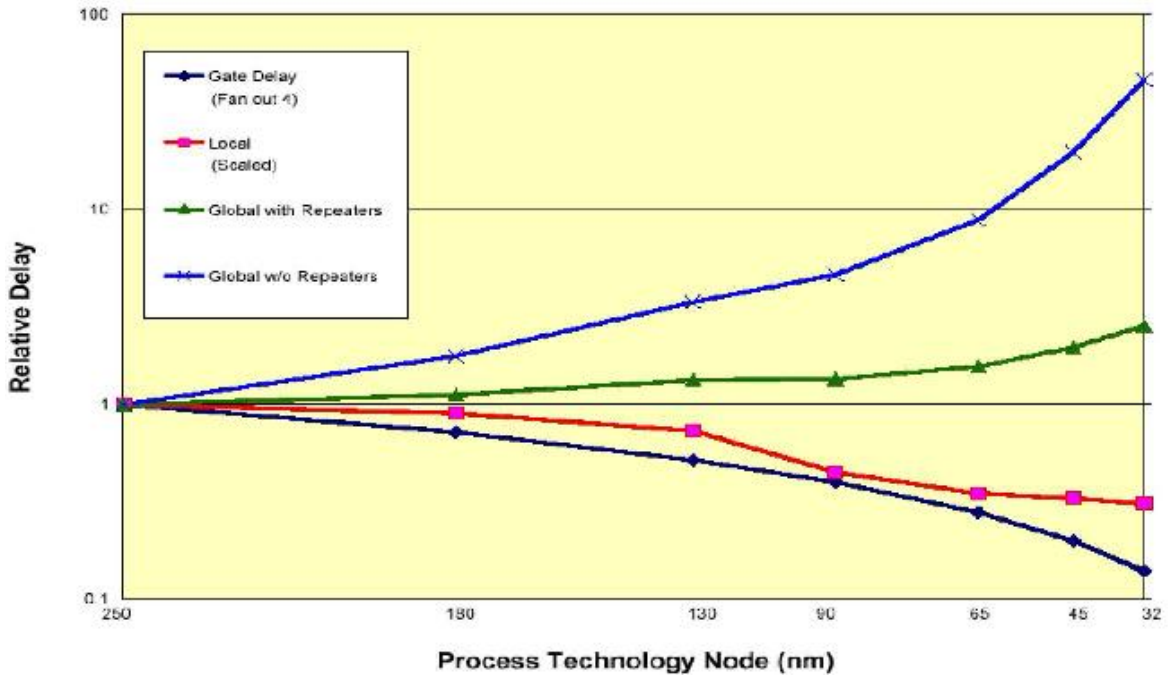

Figure 1.3: Predictions for device and wire delays (ITRS based) [5].

speed, reliable interconnects for future generations of technology. For gate lengths of nanometer size, interconnect delay is largely affected by resistive along with capacitive parasitic as per given ITRS predictions. Various alternatives were also considered before in order to decrease the RC delay. Earlier the most commonly material used for interconnects was aluminum followed by copper. The choice was usually based on its adherence on silicon dioxide and good conductivity.

1.1 PROBLEMS WITH ALUMINUM AS INTERCONNECT

Until 180nm technology node, aluminum used to be the most commonly material for interconnects due to its adherence on silicon dioxide and good conductivity. Aluminum wires were used to be responsible for large amount of resistive part of RC delay due to its high electrical resistivity. The melting point of copper (1,357 K) is higher than that of aluminum (933 K). Thus, copper having higher thermal stability than aluminum [7]. As the interconnect dimensions are scaled, aluminum interconnect material becomes highly susceptible to electromigration due to high Current densities, thus having lower reliability.

1.2 PROBLEMS WITH COPPER AS INTERCONNECT

The number of on chip interconnects are on rise with advancement in VLSI technology. The cross-sectional dimensions are being reduced rapidly to accommodate or to have more interconnects, thus resulting in dimensions of the same order as the mean free path of electrons of copper (nearly 40 nm at the room temperature). Surface scattering and grain boundary scattering are enhanced when the dimension of interconnect approaches the electron mean free path of copper [7]. Due to this, the resistivity of interconnect also increases.

i. The dimension scaling results in increase in current density. Thus, causing increase in interconnect power dissipation due to increase in current density.
ii. Thus with technology scaling increase in grain and surface boundary scattering, resistivity increases resulting increase in interconnect resistance along with length thus causing enhancement in delay [8].

iii. Due to increase in power dissipation, there is rise in heating which assists electro migration. The result of transfer of momentum from electrons, moving in the applied electric field to the lattice ions which form the interconnect material causing the formation of voids and hillocks is generally considered to be as electromigration. Failure usually results either from hillocks that results in short circuits to close by neighboring lines or voids that grow over entire line width and results in breaking of line [9].

For future generation of VLSI integrated chips, the limitations of copper interconnect dependent on scaling are going to be more and more severe. The alternative solution is the carbon nanotube interconnects to alleviate this problem for interconnects belonging to future generation chips.

1.3 CARBON-NANOTUBES

Carbon nanotubes (CNTs) being allotropes of carbon have a cylindrical nanostructure. These nanotubes are constructed with length to diameter ratio, much larger than for any other material of up to 132,000,000:1. Nanotubes derive their name from hollow, long structure with walls formed by the one atom thick sheet of carbon, which is called graphene [10]. These sheets are rolled at discrete and specific angles known as chirality. These carbon molecules of cylindrical form have unusual properties which can be valued for electronics, optics, nanotechnology and other fields of technology and material science. In particular, carbon nanotubes find applications in on chip interconnections as metal interconnects due to their extraordinary mechanical, electrical and thermal conductivity properties.CNT having lower resistivity has the advantage over copper [11]. This is due to large electron mean free path of several micrometer long as compared to mean free path of copper (Cu) of a few tens of nm. Furthermore, even at elevated temperatures a CNT wire can have a current density of the order of 10^{10} A/cm^2 without any damage [12]. Depending on the direction in which these CNTs are rolled up, they demonstrate their various properties [13].

1.3.1 Properties of carbon nanotubes

i. **Thermal Conductivity:** All carbon nanotubes are very good thermal conductors along the nanotube. Also, a SWCNT has thermal conductivity of about 5800

W·m−1·K−1 more than that of copper having 385 W·m−1·K−1 at room temperature as shown in Table 1.1.

ii. **Strength:** Carbon nanotubes are one of the stiffest, strongest and flexible materials in terms of elastic modulus and tensile strength respectively. This strength results due to the formation of covalent sp2 bonds between individual carbon atoms which are much stronger than the sp3 bonds formed in Alkenes & Diamond [13].

iii. **Kinetic Property:** In multi walled carbon nanotubes, there are multiple concentric nanotubes nested within one another which exhibit a great property of telescoping by which without friction an inner core nanotube can slide within its outer shell of the nanotube resulting in an atomically linear or a rotational bearing thus helping in precise positioning of atoms for creating useful machines.

iv. **Electrical Properties:** Carbon nanotubes have very high current carrying capacity as compared to copper shown in Table 1.1 because of the unique electronic structure and symmetry exhibited by graphene, thus structure of carbon nanotube strongly affecting the electrical properties.

Table 1.1 Comparison of properties of CNT and copper [13].

Properties	CNT	Copper
Mean free path(nm)	>1000	40
Max Current density(A/cm^2)	$>1\times10^{10}$	$\sim1\times10^{6}$
Thermal conductivity(W/mK)	5800	385

1.3.2 Classification of Carbon Nanotubes

1.3.2.1 Based on structure

Single-walled CNT (SWCNT):

Single walled CNT's structure can be viewed as a seamless cylinder formed by wrapping a one atom thick sheet of graphite which is called graphene as shown in Figure 1.4. Most of these single walled carbon nanotubes (SWCNT) usually have diameter nearly equal to 1 nm, but with tube length that can be millions of times longer than the diameter. Single-walled carbon nanotubes are one of the important types of carbon nanotubes because the various

electric properties exhibited by them are not shared by the variants such as multi-walled carbon nanotubes (MWCNT) [14].

Multi-Walled CNT (MWCNT):

Multi-walled carbon nanotubes (MWCNT) consist of concentric tubes or rolled layers of graphene as shown in Figure 1.5. A multi-walled carbon nanotube structure results when several SWCNTs of varying diameters are concentrically nested inside one another [14]. MWCNTs are usually metallic in nature and also have multiple shells. MWCNT may have very low resistance if all shells present in MWCNT are conducting due to being are properly connected to metal or polysilicon contact.

Figure 1.4: single wall CNT [14].

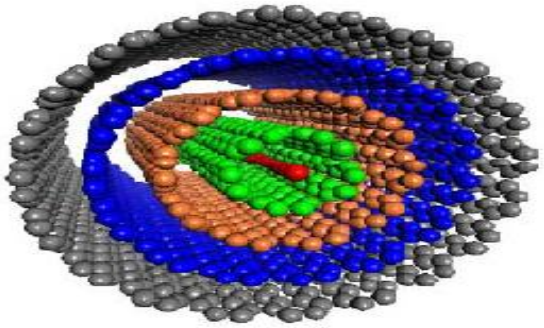

Figure 1.5: multi wall CNT [14].

Comparison of SWCNT with MWCNT interconnects:

Copper can be replaced by both SWCNT and MWCNT for global or semi global interconnects at scaled technologies. MWCNT has relatively lower conductivity as compared to SWCNT having much higher conductivity, thus being the preferred interconnect material. The reason for the difference in the conductivity of the two types of carbon nanotubes is the much smaller mean free path of MWCNT of a few nm than compared to SWCNT having mean free path of about 1um.

Also another reason that contributes to the higher resistance of multi walled CNTs is that the number of MWCNTs incorporated within the given cross section of the interconnect line are quite less due to their large diameter. Therefore, the reduced number of CNTs causes resistance to increase despite the fact that MWCNT has more number of conduction channels per nanotube [14]. But also it is a challenging job to grow a complete metallic SWCNT

bundle. MWCNT is out performed by a highly metallic SWCNT, especially at scaled technology.

1.3.2.2 Based on chirality

A CNT which can be super imposed on its own mirror image is classified as achiral CNT whereas a nanotube which cannot be super imposed is classified as chiral CNT. Also, achiral CNT is further can be classified as zigzag CNT or armchair CNT .This classification depends mainly on the geometry i.e. the circular cross-section of the nanotube as shown in Figure 1.6. The chiral vector (*n, m*) are the pair of indices which represents the way a graphene sheet is rolled. The number of unit vectors in the crystal lattice of honeycomb structure along the two directions of graphene is represented by the two indices *n* and *m*. A CNT is known as **armchair** CNT if in case (*n, m*) = (*l, l*) where *l* can be any integer. If in case *m* = 0 and *n* = *l*, then CNT formed is known as a **zigzag** CNT. If *m* = *l* and *n* = 2*l*, then CNT formed is known as a **chiral** CNT [15].

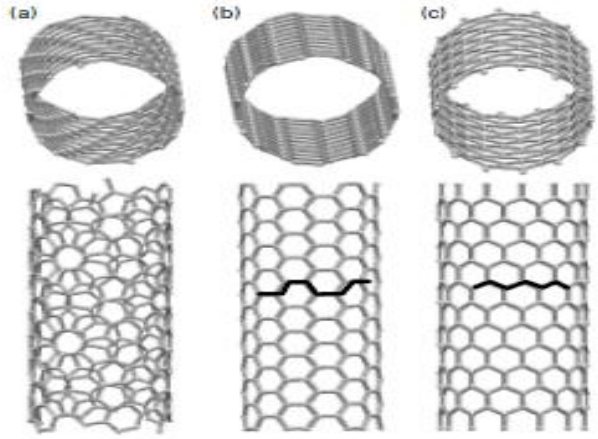

Figure1.6: The three types of CNT: (a) chiral CNT, (b) armchair CNT (c) zigzag CNT.
The armchair and zigzag character is shown by highlighting the cross-sections of the latter two illustrations by the bold lines [15].

1.3.2.3 Based on conductivity

In CNT, the results of quantization are tubes that can be either semiconductors or one-dimensional metals. One-dimensional metal tube is formed by choosing the tube axis

pointing in one of the given metallic directions resulting in a tube having fermi velocity comparable to that of a typical metal. The allowed states result in a conic section by choosing the tube axis to point in a different direction as shown in Figure 1.7. The resulting structure is a one dimensional semiconducting CNT which has a band gap between the empty electron states and the filled hole states of about 0.9eV/d [nm], where d is diameter of the tube [16]. Metallic carbon nanotubes are preferred as they are attractive materials to form interconnect due to their high mechanical and thermal stability having a thermal conductivity as high as 5800 W/mK whereas the semiconducting CNTs are not preferred as an interconnect as they do not contribute to current conduction .

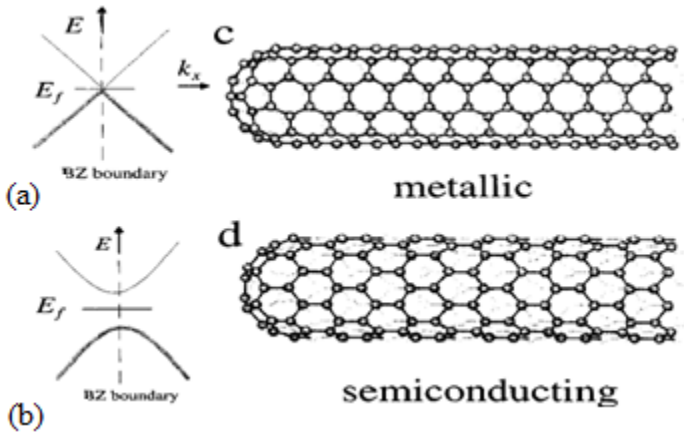

Figure 1.7: Depending on the direction in which the tube is rolled up, the result can be either (a) a metal or (b) a semiconductor CNT [16].

CHAPTER 2

LITERATURE REVIEW

Many papers on the recent researches and developments in the field of carbon nanotube as interconnects are studied. A succinct review based on the study of these papers is as follows:

Naushad Alam et al., 2009[14]

This paper investigates the prospects of using bundle of CNTs as VLSI interconnects for future applications with respect to the density of CNTs in a bundle and the average diameter of CNTs in a bundle. It is shown that with increase in average diameter, the resistance of a bundle decreases. But this can be valid only when the number of CNTs or tubes in a bundle remains constant. As the resistive impedances are much higher than inductive impedances for any length of interconnects therefore inductances can be ignored in the analysis done to evaluate performance. Because of the high value of intrinsic resistance independent of length associated with CNT, the CNT bundle interconnect at local level has a bit higher resistance as compared to its counterpart i.e. copper. The resistances of global and intermediate interconnects of CNT bundle are smaller than that of copper as copper interconnects have dimensions of the same order as MFP of electron around 40nm. Therefore, for global and Intermediate Interconnects CNT bundle interconnect is a prospective alternative to the copper interconnect.

Navin Srivastava et al., 2009[23]

This paper presents a comprehensive study of applicability of single wall carbon nanotubes (SWCNTs) as VLSI interconnects in integrated circuits at nano scale level. It is shown that with temperature there is linear increase in resistance in the bias dependent SWCNT

interconnect. Millimeter long SWCNT global interconnects offer 30%–40% improvement in the delay as compared to copper for performance critical applications. Also the overall temperature of the interconnect is affected by self heating in individual vias. The imperfect contact resistances, density of metallic SWCNTs are the factors that limit the SWCNT bundle performance.

Sankar Sarkar et al., 2011[24]

This paper analyzes how the constituent tube diameter controls the delay and power dissipation in SWCNT-bundle interconnects. SWCNT interconnect inductance and resistance increases with increase in tube diameter. It is shown that even in case of high-speed applications; an SWCNT has almost negligible inductive effect. On the other hand, interconnect capacitance decreases with increase in tube diameter. The desirable effect of reducing interconnects power dissipation and delay is indicated by decrease in capacitance with tube diameter. Increase in interconnect resistance results or has the effect of causing an increase in power dissipation and propagation delay. Much of this depends on which is the dominating one of the two. Power dissipation and delay can be independent of change in diameter if these two effects can balance each other. Hence there is always a tradeoff between power and delay dependence on tube diameter.

Navin Srivastava et al., 2005[25]

The work in this paper is to perform an analysis of the performance of CNT bundle as VLSI interconnects. An equivalent circuit is developed and analyzed in order to identify the parameters in a CNT bundle interconnect. It is shown that the CNTs lying at the edges of the interconnect bundle mainly contributes to the electrostatic capacitance of the bundle which appears as a load on the interconnect but not due to inner CNTs of the interconnect bundle. Using this model, the performance of CNT interconnect bundle is also compared to copper interconnect. At the local level of the interconnect, CNT bundles having imperfect contacts cannot give much performance improvement. It is also shown that local interconnect performance can be improved with a small decrease in density of CNT. In the case of global and long intermediate interconnect, significant improvement is shown by CNT bundle

interconnects since the additional resistance arising due to imperfect nanotube metal contacts doesn't increase with length. Thus for global and long intermediate interconnects, the CNT bundles can easily outperform copper and CNT bundles can be engineered so as to compete with copper at local level by reducing the resistance resulting from imperfect nanotube metal contacts.

Jonathan W. Ward et al., 2012[28]

The high resistance of the CNTs has hindered the replacement of copper with carbon nanotubes (CNTs) as future interconnects. In this paper, various methods to reduce sheet resistance of CNT interconnect are presented. It is shown that sheet resistance can be decreased up to 60% by functionalization with the electron accepting molecules. This is because decrease of the resistance through hole doping is possible when strong electron accepting molecules bind to surface of CNTs. Further resistance can be reduced by alignment of CNTs within the interconnect. Aligned CNT interconnect reduces the number of the CNT to CNT junctions thus resulting in decrease of resistance in contrast to the nonaligned interconnects. Also in addition to this, interconnects which are single wall CNTs show much lower resistance than the interconnects which are multi wall CNTs. This is because in MWCNTs, due to larger diameter the reduction in number of CNTs which can be incorporated within the interconnect bundle results in a higher resistance, despite having large number of the conduction channels per nanotube. The reduction in sheet resistance of CNT interconnect with functionalization and alignment and by scaling the aspect ratio of CNT interconnect appropriately, the desired *RC* delay improvement can be achieved.

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Hong Li et al., 2009[29]

In this paper high frequency effects in carbon nanotube interconnect and its implication for the performance and design analysis of on-chip inductors of high quality are presented. The analysis in this paper has shown that the skin effect in CNT bundle interconnects can be significantly reduced in comparison to that present in conventional conductors as there is presence of large kinetic inductance in each CNT. The MWCNT interconnects with large diameter could be very promising for future interconnect applications at high frequency

including inductor design, since it remains challenging to fabricate ideal densely packed SWCNT bundles separated by Van der Waal's gap with 100% metallic nanotubes. It is also shown that without using any *Q* factor enhancement techniques, CNT based bundle interconnect achieves more than three times higher *Q* factor than the copper based interconnect. The analysis of high performance on chip interconnect design explores this preferable high frequency property of CNT bundle interconnects.

Arthur Nieuwoudt et al., 2006 [30]

In this paper, the modeling of SWCNT bundle resistance for applications of on chip interconnect is presented. The impact of diameter on ohmic and contact resistance is analysed. The results indicate that significant errors as high as 120% can be produced by neglecting the diameter dependent nature of contact and ohmic resistances. Therefore, modeling the SWCNT nanotube diameter dependent contact and ohmic resistance is crucial. The relative resistance of SWCNT bundles and standard copper interconnect technology is largely affected by both the probability that a given nanotube is metallic and the diameter of the individual nanotubes. It is illustrated that SWCNT bundles can achieve one order of magnitude reduction in resistance as compared to copper interconnects depending on individual nanotube diameter and bundle geometry by using the resistance model. Moreover, an optimum nanotube diameter exists for local interconnect applications in order to minimize resistance of carbon nanotube bundle.

Pierre Gautreau et al., 2012[31]

In this paper, the affect of hot phonons on Joule heating is studied. There is a direct influence on the Joule heating with increase in scattering rate of hot phonons in SWCNT. It is shown that the scattering rate of absorption is lower than the scattering rate of an emission mechanism. The main reason of Joule heating is increase in emission which is directly translated to energy transfer to the lattice of the SWCNT interconnect. At room temperature, the applied electric field is responsible for hot phonon contribution to Joule heating, while this contribution becomes independent when the applied electric field has higher values. The electrons usually drift further away from the sub band's bottom, where the scattering changes

at a much smaller rate at higher temperatures. It is shown that the Joule heating of SWCNTs due to scattering of hot phonons exhibit non-linear behavior with respect to time. It is recommended to couple a substrate with SWCNT to allow for cooling mechanisms in order to operate at temperatures higher than room temperature.

Eric pop et al., 2006 [33]

This paper proposes an analytical model for the SWCNT thermal conductivity including temperature, length and bias dependence.The second order three phonon scattering between one optical mode and two acoustic modes causes a decrease in thermal conductivity at the upper end of temperature range. Electrical transport in the low-bias region of the SWCNT is limited by electron scattering with acoustic phonons at room temperature and the finite resistance of contacts. Self-heating can be ignored in the low bias region as it is not significant in this region. The electrical resistance of the SWCNT under high-bias is large of an order of ~300 kΩ due to electron scattering with high-energy optical phonons and is also limited by Joule self heating. This behavior enables our extraction of SWCNT thermal properties at upper temperature range directly from electrical characteristics at applied high bias.

Amir Hosseini et al., 2010[34]

In this paper, a complete model to capture both self-heating and heat transfer phenomena through electrical transport in metallic SWCNT interconnects as a function of bias voltage ,temperature, , diameter and length is presented. In the case of applied bias conditions, the electron–phonon scattering results due to the electric field that is generated along the SWCNT which accelerate electrons thus causing increase in their kinetic energy. Effective mean free path is equal to scattering length of optical phonons under high-field conditions with field of a few volts per micrometer. At practical operating temperatures i.e. hundreds of degrees above the room temperature, the SWCNT resistance is relatively independent of the temperature but varies linearly with the voltage bias. At low temperatures (≤ 300 K) under the low-field bias, the scattering resistance is dominated by acoustic phonon scattering. The

SWCNT substrate interface determines the dominant heat dissipation through the substrate. The thermally-aware model presented in this paper achieves improvement in the delay estimation of almost 51.3%. Thus carbon-nanotube (CNT) interconnects are a reliable candidate in comparison to copper interconnects for future high performance VLSI industry.

Wen Chao Chen et al., 2009[36]

In this paper, metallic single wall carbon nanotube (SWCNT) interconnect array are characterized electro thermally to evaluate performance of the above mentioned interconnects. It is assumed that there is negligible heat exchange between two neighboring SWCNTS to determine the transient heat conduction in single wall CNT by a time dependent heat conduction equation with the appropriate conditions implemented on boundary. Thus, a single SWCNT in the array biased by at a high voltage can be used to obtain the temperature distribution longitudinally. Due to self-heating effect caused by electron scattering, the temperature along the SWCNT increases until it reaches to thermal equilibrium when the SWCNT is biased by a voltage signal. It is found that for a long SWCNT, there is small Joule heating rate with the maximum rise in temperature T_{max}. Thus the scattering resistance of SWCNTs is directly affected with rise in temperature as a result of self heating in the design of local interconnect using SWCNT so time delay caused by self heating must be taken into account. Therefore while designing local SWCNT interconnect arrays at a high biasing voltage, the thermal impact on signal integrity must be taken into account.

Zhen Yao et al., 2000[37]

Due to scattering of electrons the conductance drops dramatically as the bias voltage is increased. In this paper, scattering mechanism is considered at high field and current-voltage characteristics are then explained. The transport studies of high energy electrons are enabled a when a bias voltage is applied between two contacts of low resistance thus establishing an electric field across the nanotube which causes the electrons to accelerate, therefore the contact resistance is considered to be low as in case of high resistance of the contact the

entire voltage will drop along contacts. The scattering between electrons and photons which contributes to the resistivity results in a scattering rate which is directly proportional to temperature.

Tarek Ragab et al., 2009 [39]

Joule heating in single-wall carbon nanotubes using a quantum approach is presented in this paper. The modeling is based on the transfer of energy between the electrons and both optical and acoustic phonons. The scattering with impurities does not involve transfer of energy from the electron to the lattice and scattering is assumed to be elastic due to the small mass of the electrons in comparison with mass of impurities. The dependence of electric field on the amount of energy generated due to Joule heating is also determined. The Joule heating power generated comes to a constant value at an electric field of almost 2 KV/cm, after which there is no significant effect on amount of power generated by increasing the electric field. Also, the behavior of Joule heating with changes in thermal environment is also studied. It is found that Joule heating in CNT is much less than what is predicted by the Joule law (P=IV), thus making it a perfect candidate to replace copper as VLSI interconnect material at future technologies.

Eric Pop et al., 2007 [40]

This work represents a study of thermal and electrical transport in metallic SWCNTs, over temperatures approximately (100–800K) and a wide range of applied voltages up to electrical breakdown, relevant for interconnect applications$L > 1um$. The necessary high temperature required for breakdown is provided at high applied bias by Joule self-heating. A temperature-dependent model is considered for electrical transport which is coupled with the heat conduction equation along the interconnect nanotube to account for Joule self-heating. It is found that the breakdown voltage V_{bd} usually scales linearly with length of the nanotubes for metallic SWCNTs which have low contact resistance and length greater than 1 um, approximately as 5 V/um. It is shown that the contribution of electrons which is less than 15% of the total thermal conductivity of given metallic nanotubes at room temperature, decreases at higher temperatures or at high bias. Significant self-heating can be avoided if the

thermal interface surrounding SWCNT is optimized, for interconnect applications in case of metallic SWCNTs.

CHAPTER 3

SWCNT AS VLSI INTERCONNECT

In this chapter, the behavior of single wall CNT and copper interconnect is analyzed by developing equivalent circuit for both so as to evaluate various impedance parameters such as resistance, inductance and capacitance by means of their analytical expressions. Such an equivalent circuit developed for single wall CNT and copper is then helpful or used in simulation and analysis of interconnect performance. The copper interconnects resistivity in current and future technologies is increasing at a very fast rate under combined effects of highly resistive diffusion barrier layer, surface scattering and grain boundary scattering. The large value of parasitic resistance in copper interconnects not only results in degradation of electrical performance with increase in interconnect delay but also causes major reliability issues, with increasing current density and decreasing thermal conductivity as demands from interconnects [17]. Due to high thermal conductivity, high current carrying capability and long mean free path (MFP), Carbon Nanotube are a very good alternative material for imminent nanoscale technologies, which can improve the electrical performance of an interconnect and also eliminate the electromigration reliability problem that degrades performance of nanoscale copper interconnects. SWCNTs are important type of CNTs as they have electrical properties which are not shared by the other type of CNTs i.e. MWCNTs. The main reason for considering SWCNT is high value of scattering resistance of MWCNTs as they have larger diameter which reduces the number of CNTs that can be placed within interconnect lines. So, despite the fact that MWCNT has greater number of conduction channels as compared to SWCNT, the reduction in number of CNTs per cross section results in much higher resistance, thus out performing MWCNT by a highly metallic SWCNT at scaled technologies [18]. The electronic structure of graphene and its symmetry contribute to the remarkable properties of SWCNTs. In most directions of k-space, SWCNT has a bandgap but along specific directions there is a vanishing bandgap which is called as zero bandgap semiconductors. There is quantization of momentum of electrons which are moving around the circumference of the tube when wrapped to form a nanotube [19], thus resulting in either a semiconductor or one-dimensional metal depending on whether the tube is wrapped in

preferred direction for conduction or not. Metallic SWCNTs usually have Fermi velocity v_f = 8×10^5 m/s as compared to the typical metals.

3.1 ANALYSIS OF SINGLE-WALL CNT

Equivalent Circuit Model for an Isolated Single Wall Carbon Nanotube (SWCNT):

The equivalent circuit model for an isolated single wall carbon nanotube is shown Figure 3.1.

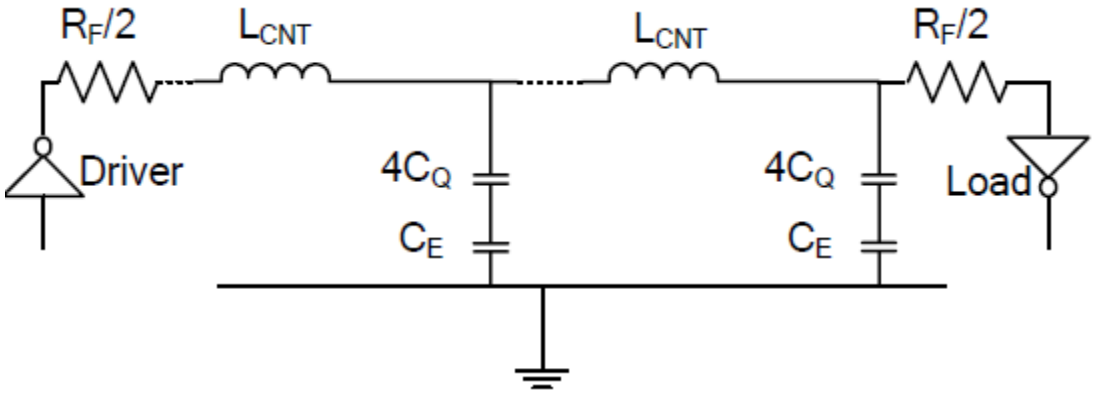

Figure 3.1: Equivalent circuit model for an isolated SWCNT [20].

The model and its different components are discussed in detail in following subsections:

3.1.1 Resistance of an Isolated SWCNT

i. **Fundamental resistance**: There are four parallel conducting channels in SWCNT (N=4) due to sub lattice and spin degeneracy of electrons. The resistance of an isolated SWCNT is $h/4e^2$ assuming perfect contacts. The resistance has a fairly large value of 6.45 KΩ when the values of the physical constants are substituted [20]. In the equivalent circuit this fundamental resistance (R_f) is divided equally between contacts present at the two ends of the nanotube.

$$R_f = \frac{h}{4e^2} \tag{3.1}$$

ii. **Scattering resistance:** For lengths which are less than the electron mean free path (λ_m) of SWCNT, the tube resistance of SWCNT equals to the fundamental resistance. But enhancement of scattering when the tube length (L) is larger than mean free path, gives rise to an additional resistance [21]. This scattering resistance increases with increase in SWCNT length above mean free path and is

$$R_S = \frac{h}{4e^2}\left(\frac{\mathrm{L}}{\lambda_m}\right) \tag{3.2}$$

iii. **Contact resistance:** It is very complex to make metal-CNT contact at the two ends of a SWCNT tube. The contacts are quite far from being perfect in most of the cases. This contact imperfection results in a very large resistance which appears in series with R_S with value of the order of 7 to100 KΩ [20].

The total resistance of the isolated SWCNT is given as

$$R_{total} = R_f + R_S + R_C \tag{3.3}$$

3.1.2 Capacitance of an Isolated SWCNT

The capacitance of a SWCNT arises from two sources-

i. **Electrostatic capacitance:** It is calculated by treating the SWCNT as a thin wire having diameter '*d*' which is placed at a distance '*y*' above the ground plane [22] as shown in Figure 3.2.

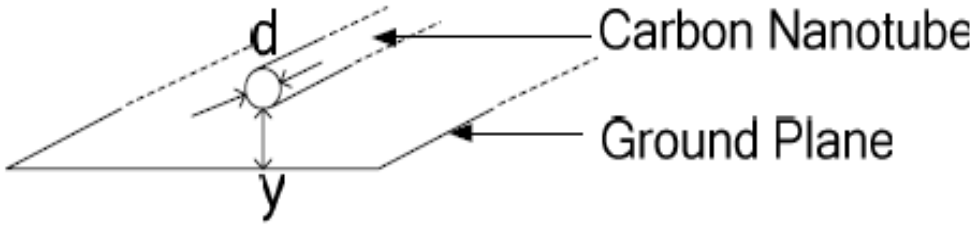

Figure 3.2: Carbon nanotube with diameter 'd', distance 'y' above ground [22].

The charge stored by the SWCNT ground plane system results in the electrostatic capacitance (C_E). Also when a charge δQ is added to a conductor, it can be considered as the change in electrostatic potential energy and is thus given as

$$C_E = \frac{2\pi\epsilon}{ln\left[\frac{y}{d}\right]} \tag{3.4}$$

ii. **Quantum capacitance:** When nanotube carries Current, the quantum electrostatic energy stored in the nanotube results in the quantum capacitance (C_Q).When the charge δQ occupies quantum energy states available above Fermi level due to the presence of low density of states at the Fermi level, thus the effective capacitance can be modeled by considering the additional quantum energy which is required to add charge δQ to the available higher energy states [22] and can be expressed as

$$C_Q = \frac{2e^2}{hv_f} \tag{3.5}$$

where $\mathbf{v_f}$ is Fermi velocity

The total effective quantum capacitance due to four parallel conducting channels is $4C_Q$ as the number four denotes that SWCNT has four conducting channels. The two capacitances of SWCNT appear in series in the isolated SWCNT equivalent circuit (Figure 3.1) because current flow through both C_E and $4C_Q$ carry same charge.

3.1.3 Inductance of an Isolated SWCNT

The energy associated with motion of electrons responsible for carrying Current (*I*) through a conductor models the inductance of a conductor.

i. **Magnetic inductance**: The magnetic field generated by the Current has energy stored in it which is given by (1/2) $L_M I^2$ where L_M denotes the magnetic inductance. So, the total magnetic energy resulting from current flowing in a wire results in magnetic inductance (L_M) which is expressed as [23].

$$L_M = \frac{\mu}{2\pi} \ln \left(\frac{y}{d}\right) \tag{3.6}$$

ii. **Kinetic inductance:** The excess electrons in a conductor can only be added at the available quantum states above Fermi energy level due to low density of states at the E_F and therefore these electrons have higher kinetic energy. This energy stored in moving electrons can be modeled as (1/2) $L_K I^2$, where L_K denotes kinetic inductance. Thus each conducting channel of the SWCNT has its own kinetic inductance (L_K) that arises from kinetic energy stored in each channel [23]. Thus the effective kinetic inductance resulting from four parallel conducting channels in a SWCNT is $L_K/4$.

$$L_K = \frac{h}{\{2e^2(v_f)\}} \tag{3.7}$$

3.2 SWCNT BUNDLE

Due to high resistance (nearly equal to 6.45 KΩ) associated with an isolated SWCNT, these interconnects cannot outperform copper interconnects at scaled technologies which necessitates the use of a bundle of SWCNTs. But, a bundle of SWCNTs may consist of metallic as well as semiconducting nanotubes due to lack of control on chirality. Metallic

SWCNTs are responsible for conduction in an interconnect whereas semiconducting nanotubes do not contribute to any current conduction.

A SWCNT bundle has a large number of isolated SWCNTs in parallel connection. These electrically parallel SWCNTs are responsible for reduction in resistance present between the two ends of the bundle. Therefore, a bundle of isolated SWCNT forms a better interconnect as compared to its isolated counterparts [24]. Practically, not all SWCNTs present in a bundle are metallic. Non-metallic SWCNTs are not responsible for current conduction and their presence can be taken into consideration as "sparsely" populated bundles as shown in Figure 3.3.

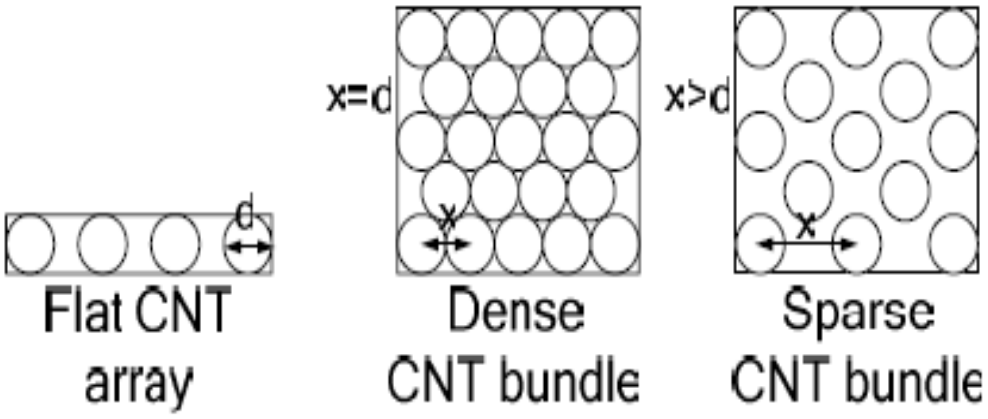

Figure 3.3: Flat CNT array and varying density of metallic CNTs within CNT bundle [25].

In the bundle the number of CNTs are calculated by the expressions shown as below, where n_w is the number of "columns", n_h is the number of "rows" in interconnect bundle , n_{CNT} is the total number of CNTs in the bundle [25] and is given as-

$$n_w = \left\{\frac{w-d}{x}\right\}; \quad n_h = \left\{\frac{h-d}{(\sqrt{3}/2)x}\right\} + 1$$

$$n_{CNT} = n_w n_h - (n_h/2) \quad \text{if } n_h \text{ is even}$$

$$= n_w n_h - \frac{n_h - 1}{2} \quad \text{if } n_h \text{ is odd} \qquad (3.8)$$

Equivalent Circuit for a Bundle of SWCNTs is given as:

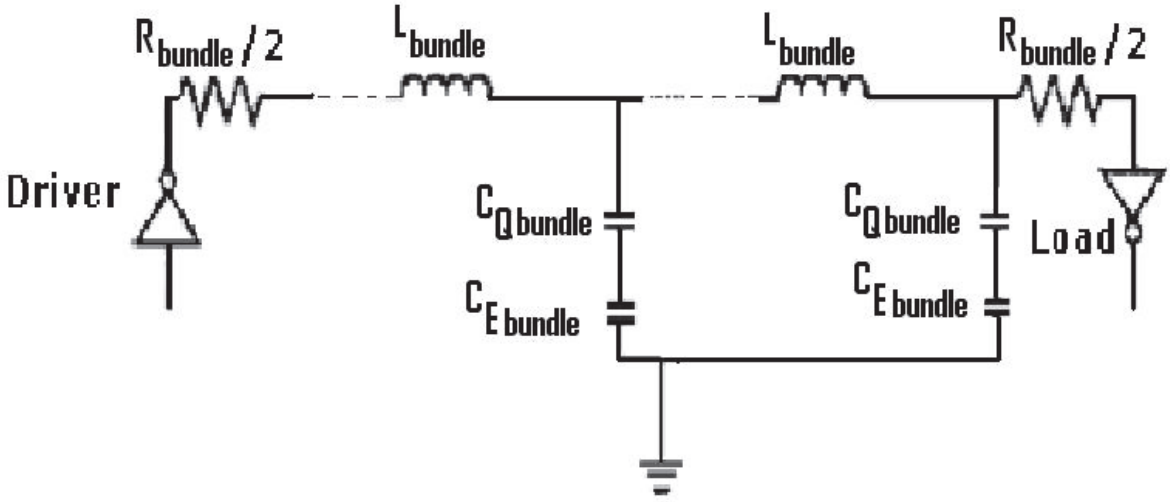

Figure 3.4: Equivalent Circuit model for a Bundle of SWCNTs [26].

3.2.1 Resistance of a SWCNT bundle

The parallel combination of resistance of isolated SWCNT gives the SWCNT bundle resistance where n_{CNT} is the total number of SWCNTs that forms the bundle and $R_{isolated}$ is resistance of each isolated SWCNT [26].

$$R_{bundle} = \frac{R_{isolated}}{n_{CNT}} \tag{3.9}$$

3.2.2 Capacitance of a SWCNT-bundle

The effective quantum capacitance of the bundle is give by summation of all the individual quantum capacitances as in a SWCNT bundle the quantum capacitances of all the SWCNTs appear in parallel. This is shown in equation 3.10, where n_{CNT} is the total number of SWCNTs that forms the bundle and C_Q^{bundle} is the quantum capacitance of a given isolated SWCNT.

$$C_Q{}^{bundle} = C_Q{}^{CNT}.n_{CNT} \tag{3.10}$$

The effective capacitance (C_{bundle}) of the series combination of a electrostatic capacitance and quantum [26] is given by

$$C_{bundle} = \frac{({C_Q}^{bundle} . {C_E}^{bundle})}{({C_Q}^{bundle} + {C_E}^{bundle})} \quad (3.11)$$

3.2.3 Inductance of a SWCNT-bundle

The parallel combination of all the inductances that correspond to each SWCNT forming the bundle gives the effective value of inductance of SWCNT bundle, which is

$$L_{bundle} = \frac{\left(L_M + \frac{L_K}{4}\right)}{n_{CNT}} \quad (3.12)$$

where L_K and L_M are the kinetic and magnetic inductance of an isolated SWCNT [26].

3.3 ANALYSIS OF COPPER INTERCONNECTS

It is well known that the increase in resistivity of copper with shrinking dimensions due to grain-boundary and surface scattering results in degradation of interconnect performance. In the following section, an RLC model for copper interconnects is presented, in a manner similar to that of SWCNT interconnects [27]. The typical layout of the copper interconnects is shown in Figure 3.5.

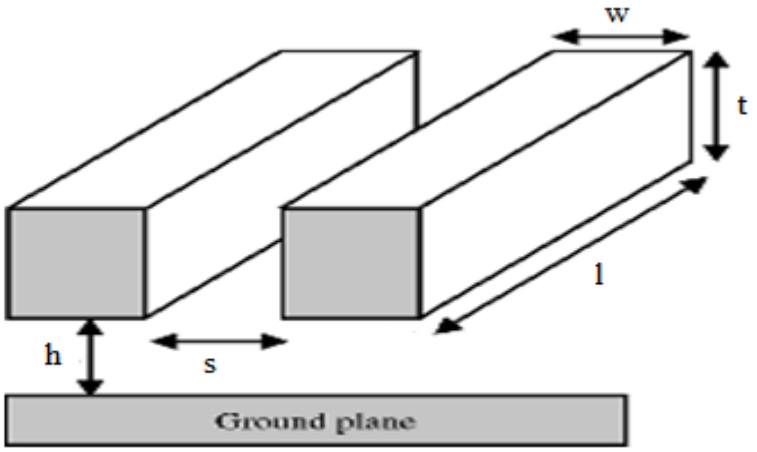

Figure 3.5: Layout of parallel copper interconnects showing the interconnect dimensions [27].

3.1.1 Resistance of copper

The resistance per unit length with rectangular cross-sections of copper interconnects [27] is calculated using expression

$$r = \frac{\rho l}{wt}$$

(3.13)

where the effects due to grain boundary scattering and surface scattering are taken into account by resistivity (ρ).

3.3.2 Capacitance of copper

The total effective capacitance of the copper interconnect [27] is given by

$$C_{total} = C_g \tag{3.14}$$

where C_g is the fringe and area flux to the underlying plane [9].

$$C_g = \in [\frac{w}{h} + 2.04 (\frac{s}{s+0.54h})^{1.77}.(\frac{t}{t+4.53h})^{0.07}] \tag{3.15}$$

where $\in$ is given as which is the dielectric permittivity

$$\in = \in_r \times 8.864 \times 10^{-12} \tag{3.16}$$

where $\in_r$ is the relative permittivity and is technology dependent.

3.3.3 Inductance of copper

The inductance with a rectangular cross section area [27] of copper wire can be expressed as following:

$$L_S = \frac{\mu_0 l}{2\pi}[\ln(\frac{2l}{w+t}) + \frac{1}{2} + 0.22(\frac{w+t}{l})] \tag{3.17}$$

where μ_0 is the permeability and given as $\mu_0 = 4\pi \times 10^{-7}$

3.4 VARIATION OF IMPEDANCE PARAMETERS OF SWCNT BUNDLE

The various impedance parameters of SWCNT such as resistance,capacitance and inductance are calculated using the above model for SWCNT and the calculated values are illlustrated with the help of the graphs.

3.4.1 Variation of resistance with tube diameter for different interconnect lengths

Figure 3.6 shows the dependence of resistance on tube diameter. It can be seen that a bundle composed of tubes of larger diameters when used as interconnect will have larger resistance. This is because when the tube diameter is increased, the number of tubes that form a bundle

reduces for a given cross-section and thus the tubes in parallel connection reduces resulting in an over all increase in the resistance of the bundle. Also at longer lengths, value of resistance is large as line resistance is directly perportional to length above the mean free path value of SWCNT.

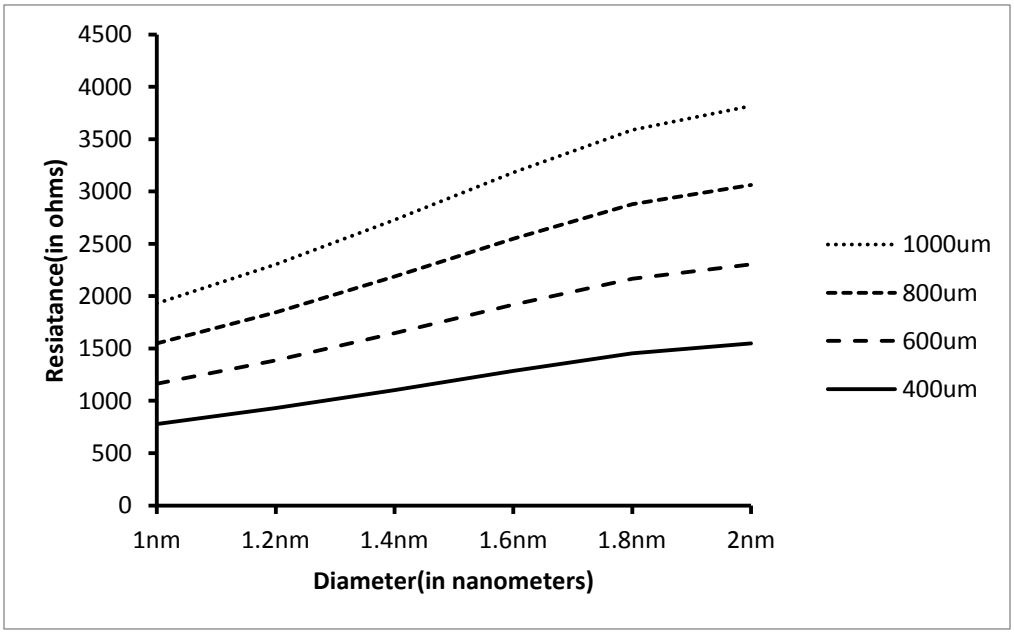

Figure 3.6:Variation of resistance with tube diameter for different interconnect lengths at 22nm technology.

3.4.2 Variation of capacitance with tube diameter for different interconnect lengths

Figure 3.7 shows the variation of SWCNT interconnect capacitance with tube diameter. The decrease in capacitance with tube diameter is due to reduction in the number of nanotubes per cross section with increase in diameter resulting in decrease in the value of n i.e. tubes that are in parallel connection to form the bundle.

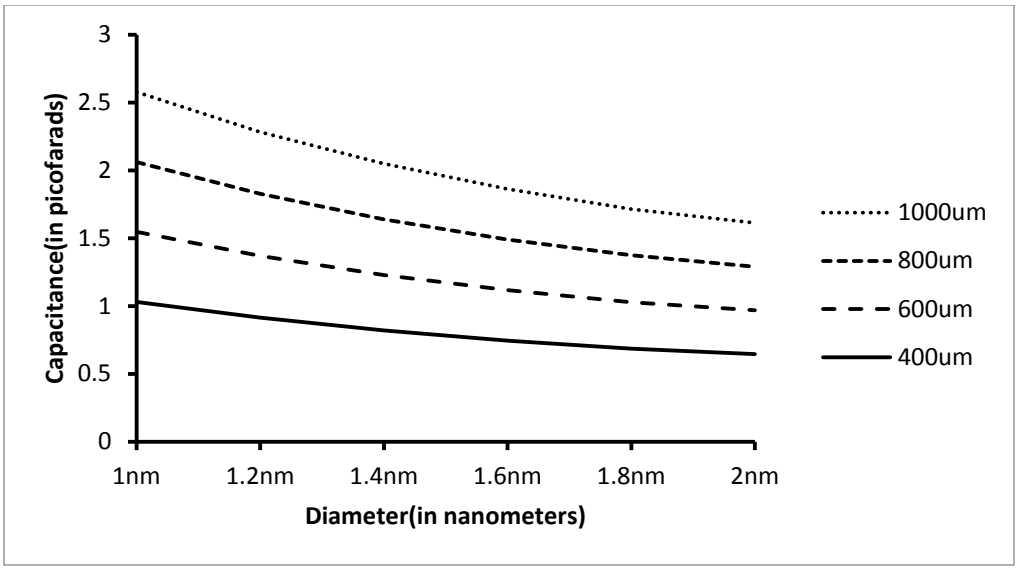

Figure 3.7:Variation of capacitance with tube diameter for different interconnect lengths at 22nm technology.

The increase in interconnect resistance with increase in tube diameter has the effect of increasing propagation delay whereas decrease in capacitance indicates the desirable effect of reducing interconnect delay. So between these two competing effects delay will depend on the factor which dominates.

3.4.3 Variation of inductance with tube diameter for different interconnect lengths

Figure 3.8 shows the dependence of inductance on tube diameter. It can be seen that when used as interconnect, a bundle with nano tubes of larger diameters will have large inductance. This is due to reduction in the nanotubes per cross section that are in parallel connection causing decrease in the value of n which is inversely proportional to inductance shown in equation 3.12 thus resulting an increase in the value of inductance.

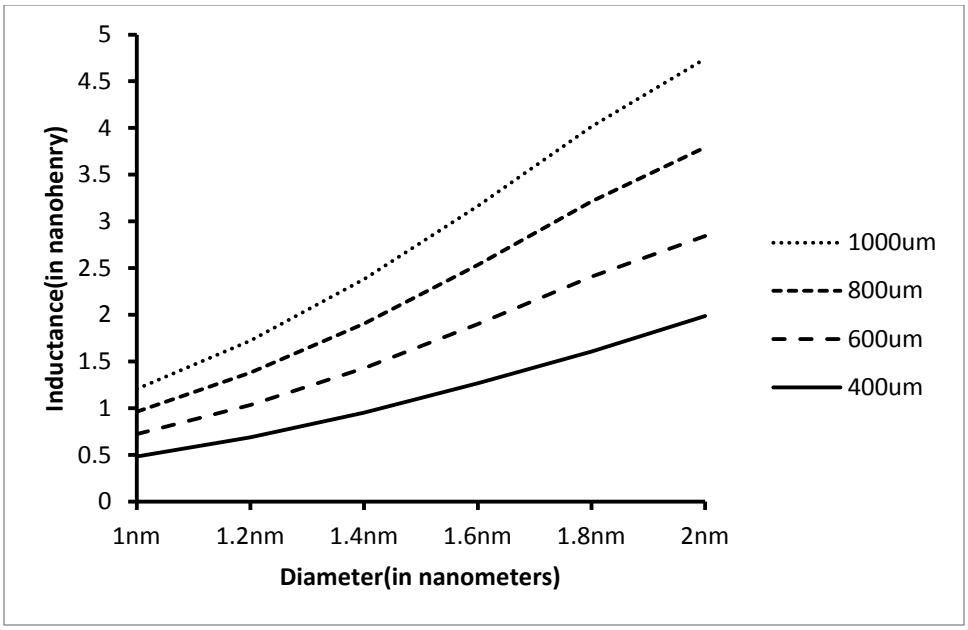

Figure 3.8:Variation of inductance with tube diameter for different interconnect lengths at 22nm technology.

The inductive impedances are very much lower than the resistive impedances at any length of interconnects, therefore inductance can be ignored in the performance analysis of SWCNT.

3.5 VARIATION OF IMPEDANCE PARAMETERS OF COPPER

The copper (Cu) interconnect considered for analysis has a rectangular cross section therefore has no diameter dependence. In this section, variation of resistance,capacitance and inductance of copper is shown with the help of the tables with respect to technology at different interconnect lengths.

3.5.1 Variation of resistance with technology at different interconnect lengths

Table 3.1 shows variation of resistance with technology. As technology scaling is performed, the value of resistance for copper interconnect increases due to increse in electromigration, surface and grain boundary scattering causing a sharp rise in the resistivity of copper interconnects resulting in large value of the resistance. Also with increse in length resistance also increses due to linear dependence of resistance of copper on length.

Table 3.1:Variation of resistance (in kiloohms) with technology at different interconnect lengths.

Technology (in nm)	Length of Copper interconnect (in um)			
	400um	600um	800um	1000um
45nm	0.8464	1.2950	1.6927	2.1159
32nm	2.0370	3.0556	4.0741	5.0926
22nm	5.4690	8.2030	10.937	13.672
16nm	16.266	2.4399	32.532	40.665

3.5.2 Variation of capacitance with technology at different interconnect lengths

Table 3.2:Variation of capacitance (in femtofarads) with technology at different interconnect lengthts.

Technology (in nm)	Length of Copper interconnect (in um)			
	400um	600um	800um	1000um
45nm	8.3400	12.570	16.690	20.860
32nm	6.7070	10.150	13.530	16.910
22nm	5.9110	8.8601	11.810	14.770
16nm	4.4840	7.2620	9.6830	12.100

With technology scaling, decrease in the value of capacitance for copper at different interconnect lengths (as shown in Table 3.2) is desirable as it may result in smaller propagation delay depending on the value resistance. As capacitance is directly proportional to length, decrease in length results in decrease in capcitance for lengths used for interconnect applications.

3.5.3 Variation of inductance with technology at different interconnect lengths

The inductance values for different technologies are calculated from equation formulated for copper model. It is observed that value of inductance increases as one moves towards higher technology as shown in Table 3.3. Like resistance and capacitance,

inductance of copper also shares a linear relationship with length resulting in increase in the value of inductance with increase in length.

Table 3.3:Variation of inductance (in nanohenries) with technology at different interconnect lengths.

Technology (in nm)	Length of Copper interconnect (in um)			
	400um	600um	800um	1000um
45nm	0.6840	1.0740	1.4780	1.8930
32nm	0.7070	1.1090	1.5240	1.9500
22nm	0.7390	1.1580	1.5890	2.0310
16nm	0.7730	1.2080	1.6570	2.1160

3.6 COMPARISON OF IMPEDANCE PARAMETERS OF SWCNT BUNDLE AND COPPER

In this section, the impedance parameters of SWCNT and copper interconnect are compared. The resistances, capacitances and inductances of the global interconnects at different technology nodes are evaluated in Matlab considering the geometries suggested by the above described models.

3.6.1 Comparison of resistance of SWCNT bundle and copper interconnects

Figure 3.9 plot resistances of SWCNT bundle and copper interconnects. It is clear from the results that the resistance of SWCNT bundle is smaller that of copper interconnect and also the rate at which copper resistance increases with technology scaling is much greater than that of SWCNT resistance. This is because with technology scaling, the dimensions of copper interconnect are of the order of mean free path which results in enhancement of surface and grain boundary scattering, electromigration thus causing sharp rise in the resistivity of copper interconnects. Also copper interconnect resistance increases linearly with increase in length, but in the case of SWCNT bundle it is only the scattering resistance

that increases linearly with length. The additional resistance due to the imperfect metal-nanotube contact in SWCNT bundle does not increase with length.

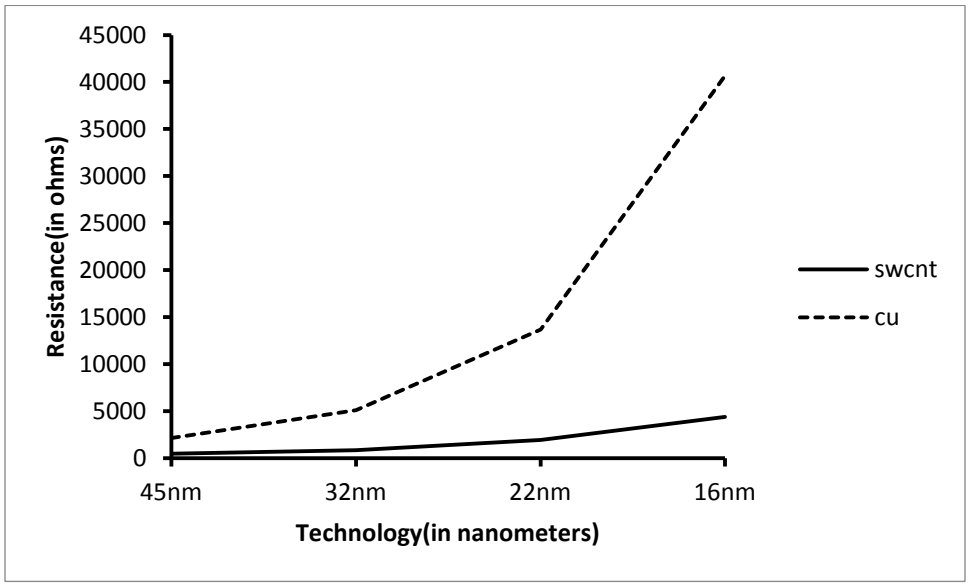

Figure 3.9: Variation of resistance of SWCNT bundle and copper interconnect with technology scaling for interconnect length of 1000um.

3.6.2 Comparison of capacitance and inductance of SWCNT bundle and copper interconnect

Figure 3.10 plot the measured capacitances of SWCNT bundle and copper interconnects. It is observed that the capacitances of SWCNT bundle are marginally higher than that of the copper counterpart over all the technology generations. But SWCNT capacitance reduces greatly with technology scaling whereas there is no much decrease in the capacitance of copper interconnect.

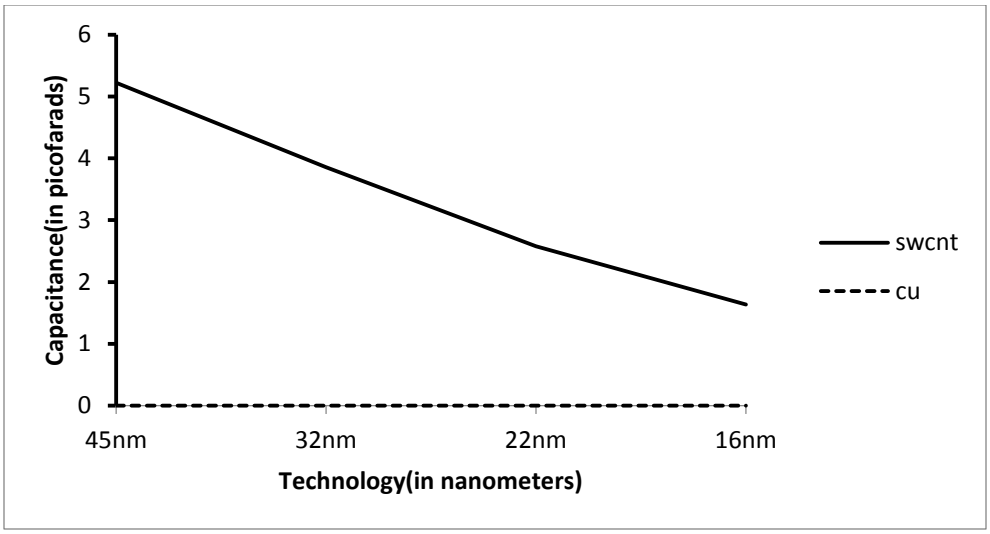

Figure 3.10: Variation of capacitance of SWCNT bundle and copper interconnects with technology scaling for interconnect length of 1000um.

Figure 3.11 plot the measured inductances of SWCNT bundle and copper interconnect. It is observed that the SWCNT bundle has lower value of inductances than copper interconnect for technology nodes till 22nm which is preferable for better performance of SWCNT interconnects. But as we move from 22nm to 16nm technology node, the value of inductance for SWCNT bundle increases. Considering the fact that these inductive impedances are quite smaller in comparison to the resistive impedances calculated for these interconnect lengths, the inductance values plotted have no much effect on the performance of the interconnect.

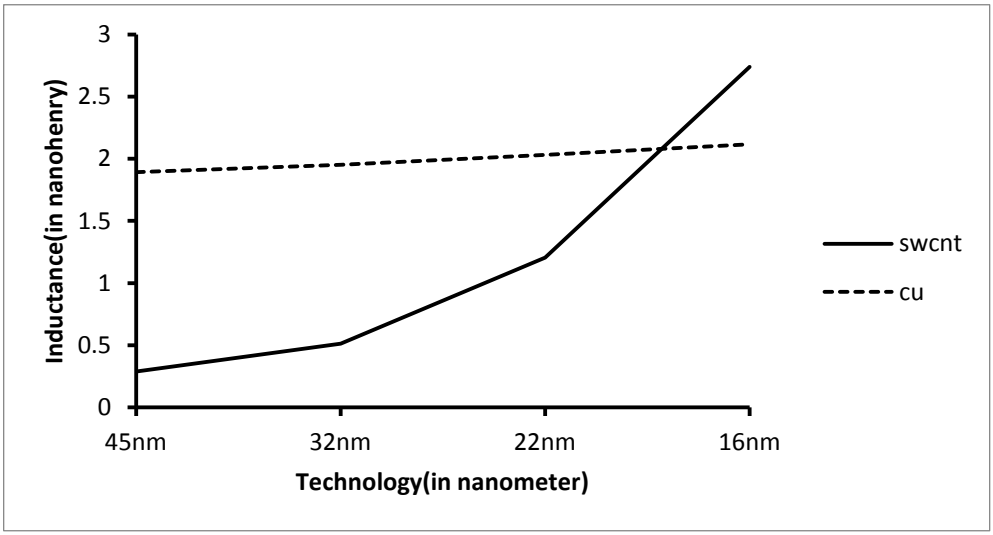

Figure 3.11: Variation of inductance of SWCNT bundle and copper interconnects with technology scaling for interconnect length of 1000um.

CHAPTER 4

EFFECT OF ELECTRIC FIELD ON SWCNT

Introduction

Employing SWCNTs as interconnects to route high speed signals in a VLSI integrated circuit is one of the main applications employed for promoting carbon nanotubes because of their ballistic transport over relatively long lengths and having high current carrying capability. SWCNT interconnects with their small dimensions and ability to operate at wide range of bias conditions are well suited for these VLSI interconnect applications. But much still needs to be explored about the electrical properties of these interconnect, before such VLSI applications are implemented into the electronic devices [29]. Because of the diversity and imbalanced utilization of interconnects at different sections of an integrated circuit, electric field can vary significantly from one area to another across interconnects. Thus, posing greater challenges in the modeling of high performance integrated circuits. In this light, impedance parameters that cause variations in the current through these interconnects are identified by examining bias dependent model that have impact on the effective mean free path by causing electron phonon scattering in the nanotube [30]. In this chapter, focus is on applicability and electrical transport of metallic SWCNTs under different electric field conditions. A novel circuit compatible voltage dependent model of SWCNT is presented in this chapter. In metallic SWCNTs, the bias dependent electrical resistance is affected strongly by dependence of electron phonon scattering in case of lengths in microns relevant to interconnect applications [31]. Consequently, all relevant electron-phonon scattering mechanisms affecting resistance and mean free path are thoroughly discussed in this chapter. A wide range of voltages which are of practical interest are covered by this proposed model. The signal delay of SWCNT interconnects and power dissipation are affected by these voltage variations and hence, will significantly determine the performance of the SWCNT based VLSI integrated circuits.

4.1 MODELING OF SWCNT INTERCONNECTS

Voltage dependent circuit model for metallic SWCNT bundle

The equivalent voltage dependent circuit model for a metallic single wall carbon nanotube bundle comprising of resistance, inductance and capacitance is shown schematically in Figure 4.1.

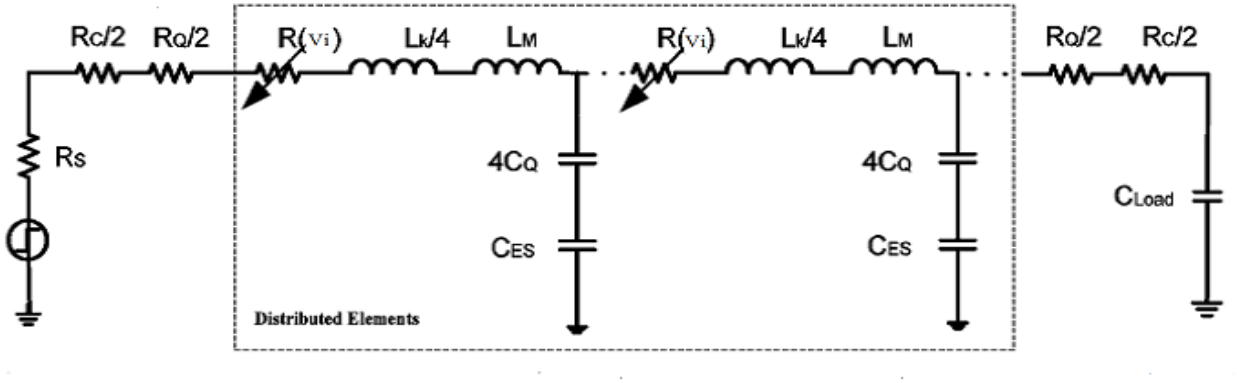

Figure 4.1: Equivalent electrical circuit model of a metallic SWCNT [32].

4.1.1 Electrical Resistance of a single walled CNT

Electrical resistance (R) of metallic SWCNT can be modeled by the fundamental or intrinsic quantum resistance (R_f), resistance due to contacts (Rc) and ohmic resistance due to the electron phonon scattering (Rs), which form a series combination in the described model [33]. These all three components are discussed in detail below.

i. **Intrinsic quantum resistance**: Due to sub lattice and spin degeneracy of electrons there are 2N conducting channels which are in parallel in SWCNT Assuming perfect contacts , the intrinsic quantum resistance of an SWCNT is

$$R_f = \frac{h}{2Ne^2} \tag{4.1}$$

This resistance (R_f) is divided equally between the two contacts at the ends of the carbon nanotube in the equivalent circuit.

Many subbands of SWCNTs with large diameters usually extend to Fermi level and create channels to contribute to electrical conductance for electrons at room temperature. The number of channels available for conductance in SWCNT [34] is expressed as

$$N=\sum_{all\ subbands} \frac{1}{\exp\left(\frac{|Ev|}{K_B T}\right)} \quad (4.2)$$

This above expression is approximated at room temperature as a function of diameter.

$$N(d) \approx 2 \quad \text{for } d < d_T$$
$$\approx ad + b \quad \text{for } d > d_T \quad (4.3)$$

where $d_T \approx 4.33$ nm, $a \approx 0.1836/(nm)$ and $b \approx 1.275$.

ii. **Contact resistance**: Contact resistance arises due to imperfection of the metal-SWCNT contact and mainly depends on the metal used to make this contact and its value is almost independent of the SWCNT diameter. The value of this resistance is 24 KΩ in case of using palladium [34].

iii. **Scattering resistance**: The scattering resistance (R_S) depends on effective electron mean free path which is a function of SWCNT diameter (d) and bias voltage (V). The electron phonon scattering is the main source of scattering. The different mechanisms of electron–phonon scattering that occurs in SWCNT bundle are acoustic and optical scattering [34] as shown in Figure 4.2. Therefore, $\lambda_{m,eff}$ is expressed as

$$\lambda_{m,eff} = (\lambda_{ac}^{-1} + \lambda_{oz}^{-1}) \quad (4.4)$$

where λ_{ac} , λ_{oz} denotes the acoustic MFP and the effective optical MFP respectively.

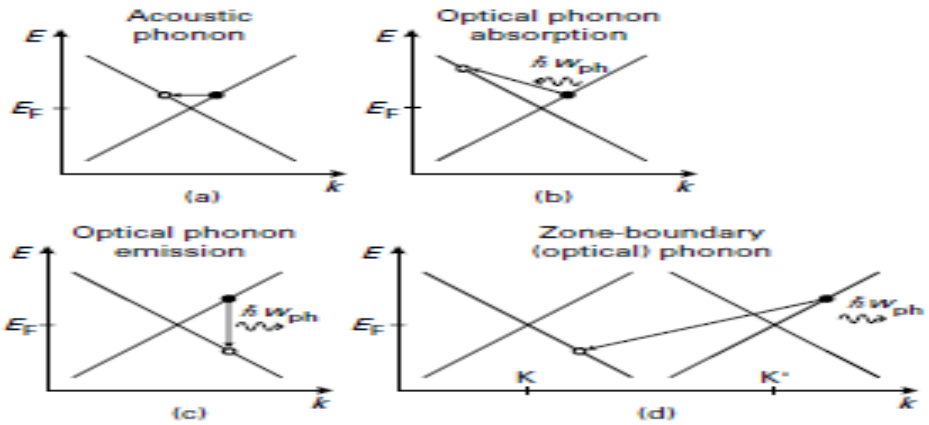

Figure 4.2: Idealized diagrams of electron– phonon scattering present in metallic SWCNTs. (a) Acoustic phonon scattering. (b) and (c) shows optical phonon absorption and emission processes of scattering respectively. (d) Phonon zone boundary scattering [35].

Ohmic resistance at low -bias conditions results in acoustic phonon scattering in SWCNTs . At room temperature, λ_{ac} is found to be directly dependable on diameter [34]. Therefore, λ_{ac} is given as

$$\lambda_{ac}(d) = \frac{\lambda_{ac,300}}{d_0} d \tag{4.5}$$

where for diameter $d_0 = 1.8$ nm, $\lambda_{ac,300} \approx 1600$ nm is the acoustic MFP at 300 K. The number of optical phonons N_{Op} strongly determines the optical phonon scattering mechanisms. Also, the number of optical phonons is given by Bose–Einstein distribution [35], and is

$$N_{Op} = \left[\frac{1}{exp(h\Omega - K_B T) - 1}\right] \tag{4.6}$$

N_{Op} is a strongly dependent on the phonon energy where $h\Omega$ denotes the optical phonon critical energy and K_B denotes Boltzmann's constant. Thus, the modes related with this critical energy are responsible for scattering of above optical phonons by the electrons. The acceleration of electrons due to the electric field (E =V/ L) generated along SWCNT in case of high-bias result in increase in their kinetic energy. A phonon of energy $h\Omega$ (in case of optical phonon, $h\Omega$ = 0.2 eV and in case of zone-boundary phonon, $h\Omega$ = 0.16 eV) will be emitted when the energy of electron reaches the critical level of optical phonon energy. Also, scattering results when an electron acquires energy by absorbing another optical phonon [36]. Therefore, λoz is given as

$$\lambda_{oz} = (\lambda_{oz,fld}{}^{-1} + \lambda_{oz,abs}{}^{-1})^{-1} \tag{4.7}$$

where $\lambda_{oz,fld}$ and $\lambda_{oz,abs}$ are the emission scattering lengths due to electrons obtaining sufficient energy due to the electric field and by absorbing an optical phonon respectively [36]. $\lambda_{oz,fld}$ can be written as

$$\lambda_{oz,fld} = \frac{(h\Omega - K_B T)L}{eV} + \frac{\lambda_{oz,300}\ d}{d_0} \tag{4.8}$$

where K_B is the Boltzmann's constant and $K_B T$ is the thermal energy. The first term in the above equation gives the distance needed to be travelled by electrons before gaining enough

amount of energy to emit a phonon and the second term represents the distance that an electron travels between the event of gaining sufficient energy and emitting a phonon. For diameter d_0, the spontaneous effective emission length, $\lambda_{oz,300}$ is 15 nm at 300 K. The scattering effect that results due to electron absorbing an optical or zone-boundary phonon is given by $\lambda_{oz,abs}$ [36] and can be expressed as

$$\lambda_{oz,abs} = \frac{\lambda_{oz,300}}{d_0} \frac{d}{N_{oz}(300)} \frac{N_{oz}(300)+1}{} \tag{4.9}$$

i) SWCNT low field scattering resistance: At low bias, the total resistance of single-wall CNT of a certain diameter [35] can be expressed as

$$R_{S,lf}(d,V) = R_C + \frac{h}{2Ne^2}\left[1 + \frac{L}{\lambda_{m,eff}(d,V)}\right] \tag{4.10}$$

In the low-field limit, acoustic phonon scattering dominates $\lambda_{m,eff}$. But there is an enhanced decline in the effective low field mean free path at room temperature as scattering due to optical phonon is no longer negligible at 300 K. The effective mean free path is largely determined by the field dependent first term of optical scattering as mentioned in equation 8 because of which $\lambda_{OZ,abs}$ has a flat profile at low bias. It is the absorption process of optical phonon that actually confers a very strong diameter dependence on λ_{OZ} in case of SWCNT bundle [35]. Under ambient conditions i.e. in air, at room temperature, the above mentioned resistance $Rs_{,lf}$ at low-field is desirable.

ii) SWCNT high field scattering resistance: The effective mean free path under high field conditions of a few volts per micrometers, is almost equal to scattering length or mean free path due to optical phonons. With high bias, SWCNT scattering resistance varies linearly with electric field strength at room temperature. An effective mean free path consisting of the field dependent term for $\lambda_{OZ,fld}$ in equation 8 which is significant at high fields and acoustic phonon scattering dependent length which is important at low fields, is constructed to derive the expression for the electric field dependent resistance of nanotube at room temperature[37].Thus,

$$R_{S,hf}(d,V) = R_{lf} + \frac{|\text{Vbias}|}{I_0} \tag{4.11}$$

where $R_{s,hf}$ denotes the high bias scattering resistance and I_0 is the current that even if V_{bias} is increased, it does not increase beyond I_0. So, it is also known as the saturation current. I_0 is almost equal to 25μA for a SWCNT of length 1μm [37]. Let the resistance of SWCNT be R_{SWCNT}. Thus to form a bundle a parallel connection of SWCNT interconnect is considered due to large amount of resistance of single wall CNT and the bundle resistance is given as

$$R_{bundle} = \frac{R_{SWCNT}}{n} \tag{4.12}$$

4.1.2 Kinetic inductance

In a conductor, the electrons have a higher kinetic energy due to the excess electrons being added only at quantum states which are available above E_F as there is low density of energy states at Fermi level (E_F). $(1/2)L_K I^2$ is the given amount of kinetic energy that is stored in these electrons where L_K denotes the kinetic inductance .Thus, due to kinetic energy stored a kinetic inductance (L_K) arises in each conducting channel of the SWCNT [38] and is given as

$$L_K = \frac{h}{4Ne^2 v_f} \tag{4.13}$$

where $v_f = 8\times 10^5$ m/s denotes the Fermi velocity and the total number of conducting channels is given as 2N. Also, $L_K >> L_M$ therefore L_M is not considered as it does not have significant impact in the above model for interconnect delay and power calculation. Furthermore, due to parallel connection between the various SWCNTs in the bundle, the total kinetic inductance for a bundle is

$$L_{K,total} = \frac{L_K}{n} \tag{4.14}$$

4.1.3 Quantum capacitance

The quantum capacitance (C_Q) gives the amount stored as electrostatic energy in each conducting channel of a nanotube carrying Current. The charge δQ is added at the quantum states available above the Fermi level due to presence of low density of states at Fermi level. The electrostatic capacitance can be modeled by considering an effective quantum

capacitance resulting from the additional quantum energy required [38], which is expressed as

$$C_Q = \frac{4Ne^2}{hv_f} \tag{4.15}$$

The total quantum capacitance for a bundle because of the parallel connection is given as

$$C_{Q,total} = n.C_Q \tag{4.16}$$

4.2 MEAN FREE PATH AND ELECTRICAL RESISTANCE

The scattering of electrons caused by phonons is usually a function of electric field or applied voltage. The bias conditions often used are divided into the low-field and high-field conditions, with a region of transition in between. In this paper, our simulation results are for low bias region. This is because at low bias, the tube is generally in thermal equilibrium with its surroundings and thus essentially isothermal. Therefore in these conditions, the effect of Joule self-heating is less owing to lower power densities in the nanotube ($p = IV/L$ with lower voltage and longer length) whereas high applied bias results in noticeable self-heating which is the main reason for in-air breakdown. This breakdown occurs as the result of heat generation due to self heating when temperature reaches its peak value at the middle of the tube [39].

The effective mean free path in SWCNT bundle is determined by electron–phonon scattering mechanism and not by electron–electron scattering mechanism which is almost negligible. Thus, the effective mean free path results from the mean free path due to acoustic and optical scattering phenomena [40] given as

$$\lambda_{m,eff} = (\lambda_{ac}{}^{-1} + \lambda_{oz,fld}{}^{-1} + \lambda_{oz,abs}{}^{-1})^{-1} \tag{4.17}$$

As the electric field increases in the low bias region, the effective mean free path decreases due to increase in electron phonon scattering as shown in Figure 4.3. In this bias regime, $\lambda_{m,eff}$ mainly comprises of the acoustic phonon scattering length which yield the resulting mean free path but optical phonon scattering also has a significant impact on the mean free path in this region especially for longer nanotubes used as VLSI interconnects at room temperature [40]. Since at these given biases, electrons are accelerated under the electric field

and thus gain sufficient energy to emit optical phonons which are responsible for scattering and thus reducing the optical mean free path.

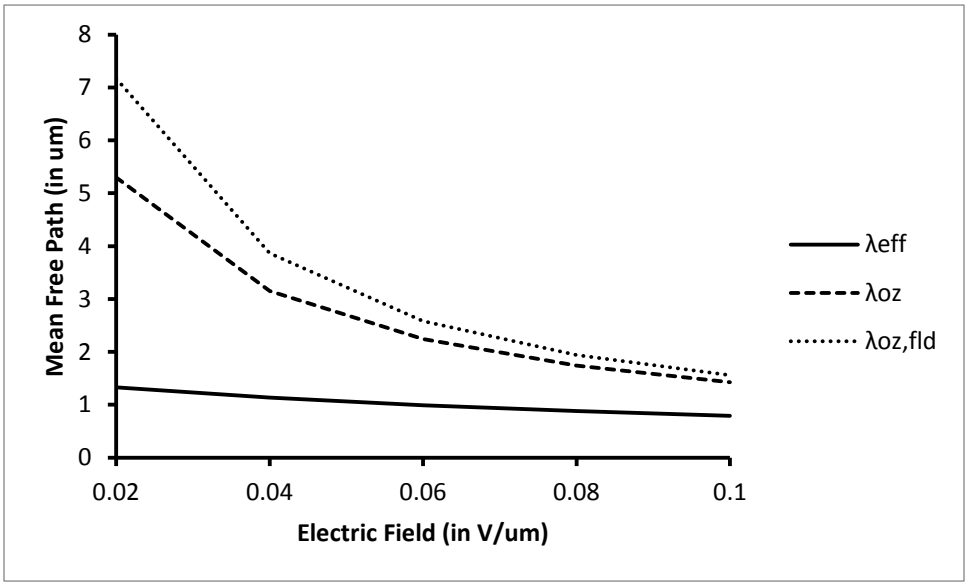

Figure 4.3: Variation of mean free path of SWCNT interconnects for length 1000um and diameter 2nm as a function of electric field.

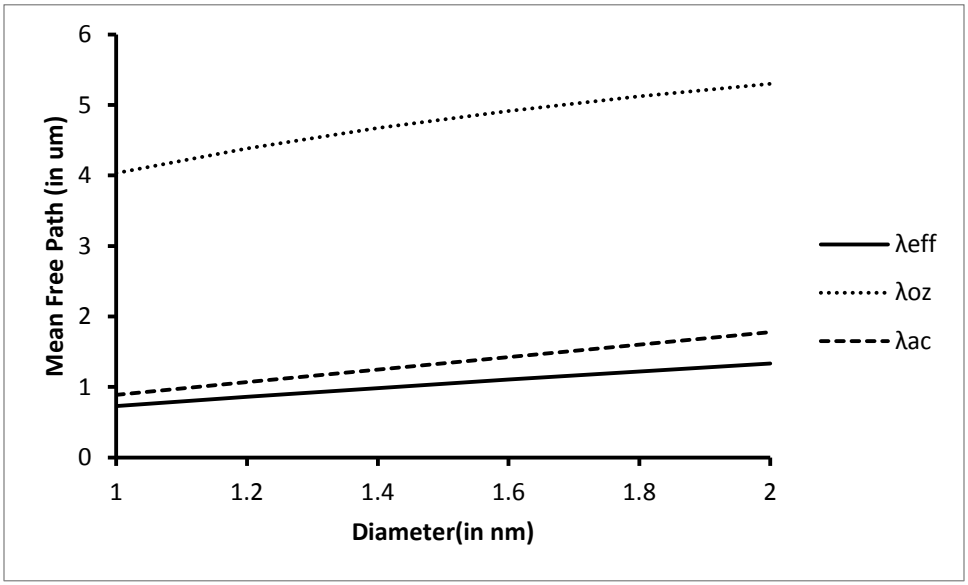

Figure 4.4: Variation of mean free path of SWCNT interconnects for length 1000um and electric field 0.02V/um as a function of diameter.

Figure 4.4 shows dependence of optical, acoustic and effective mean free path on diameter. As diameter increases both acoustic and optical phonon scattering decreases resulting an

increase in the effective mean free path. This is because both acoustic and optical mean free path share a linear relationship with diameter as described in equation 4.5, 4.8, 4.9 of voltage dependent circuit modeling.

The voltage dependent resistance is obtained by analyzing effective mean free path. Since resistance has an inverse relation with effective mean free path as presented in equation 4.10. So, as applied bias increases effective mean free path decreases due to increase in electron–phonon scattering thus, resulting an increase in electrical resistance of SWCNT. As the number of SWCNTs in a bundle are independent of electric field so bundle resistance also increases with increase in resistance of individual SWCNT with voltage bias as shown in Figure 4.5.

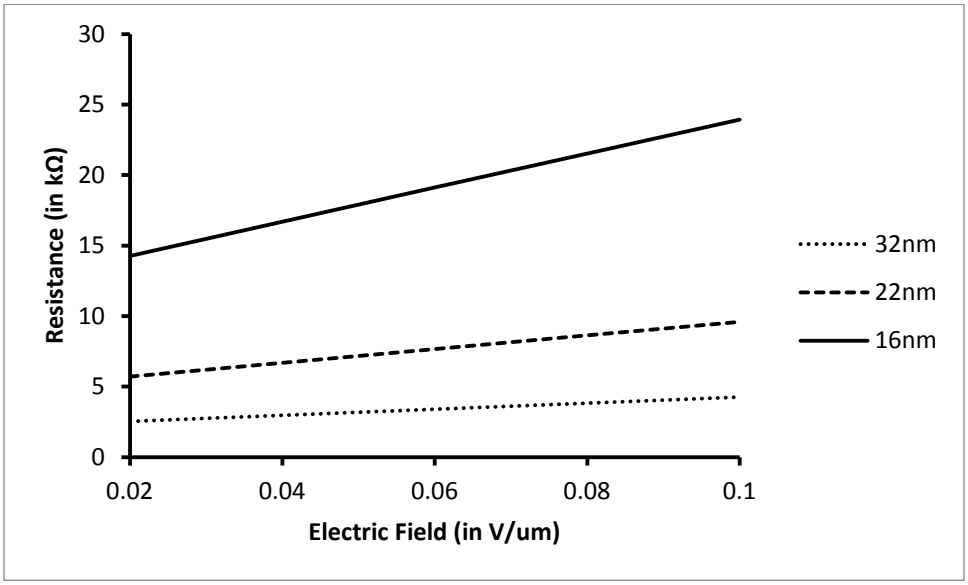

Figure 4.5: Variation of resistance of SWCNT bundle interconnects for length 1000um and diameter 2nm as a function of electric field.

Electrical resistance variation with diameter for different technologies is shown in Figure 4.6. The acoustic and optical scattering mean free paths are proven to be directly dependent on diameter. So, with increase in diameter there is less scattering causing electrical resistance to decrease in case of SWCNT. But in case of SWCNT bundle, with increase in diameter of individual SWCNT, the number of SWCNTs per cross section decreases resulting less number of SWCNTs in parallel connection thus causing net increase in bundle resistance with increase in diameter.

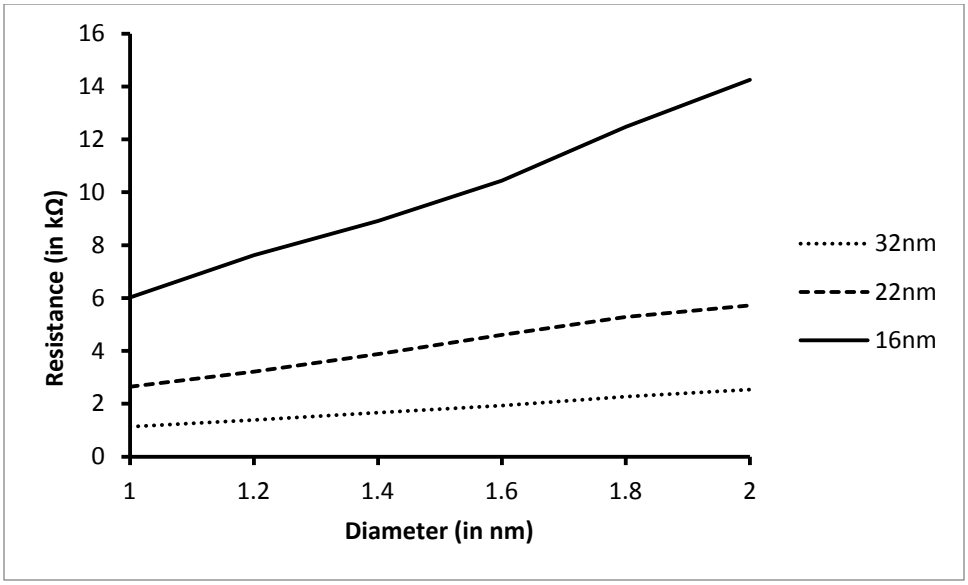

Figure 4.6: Variation of resistance of SWCNT bundle interconnects for length 1000um and electric field of 0.02V/um as a function of diameter.

CHAPTER 5

RESULTS AND DISCUSSION

Introduction

Using the calculated impedance parameters, delay and power is simulated for SWCNT bundle and copper interconnects with the help of lumped and distributed models using tanner tool and thus performance analysis is performed by comparing SWCNT bundle and copper interconnect delay and power at varying diameter, frequency and aspect ratio [42]. Thus optimum number of repeaters for each technology are obtained with optimum aspect ratio to minimize the PDP (power delay product) of SWCNT bundle used as VLSI interconnect. The electrical resistance calculated from electric field dependent model is used to achieve improvement in the delay and power estimation accuracy compared to bias independent equivalent circuit model. The resultant graphs are plotted showing variation of delay and power with electric field at different tube diameters. The technology parameters used for simulation are given in Table 5.1.

5.1 Technology and Simulation parameters of global interconnects (ITRS based) [5].

Technology	32nm	22nm	16nm
V_{dd}	0.9v	0.8V	0.7v
Width (W)	48nm	32 nm	21nm
A/R (aspect ratio)	3	3	3
Thickness (H)	144nm	96nm	63nm
Separation (s)	48nm	32nm	21nm
Oxide thickness(tox)	110.4nm	79.6nm	52.5nm
ε_{OX}(relative)	2.25	2.05	1.75
ρ(Copper)	3.52 μΩcm	4.2μΩcm	5.38 μΩcm

Contact Resistance (R_c)	24KΩ	24KΩ	24KΩ

5.1 INTERCONNECT DELAY MODEL

To calculate delay across an interconnect, it is represented in terms of an electrical model comprising of impedance parameters i.e. resistance, capacitance and inductance. This RLC network model gives approximation of the actual behaviour of the interconnect line. There are two types of interconnect models which are described below.

Lumped RLC model:

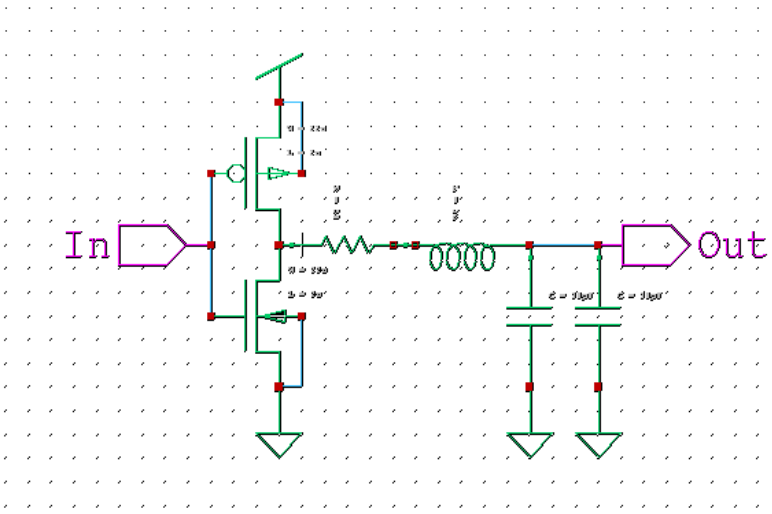

Figure 5.1: Lumped RLC model for interconnect to calculate delay and power.

As shown in Figure 5.1, input is applied through an CMOS inverter and output is obtained across a load capacitance with interconnect line represented by an RLC network. Here R, L, C values calculated for the SWCNT bundle and copper interconnect with the help of equations implemented in matlab are used to evaluate delay and power dissipation for the interconnect. The load capacitance with value 1pF is used and the operating frequency of input square waveform varies from 20Mhz to 0.5Ghz. Model files for nmos and pmos for different technologies are available to perform simulation in TSPICE. Delay is calculated through waveform editor and the power is calculated from .out file. Delay and power are calculated for different aspect ratio (W/L) of nmos and pmos then the optimum AR is chosen at which minimum PDP is obtained.

Distributed RLC Model:

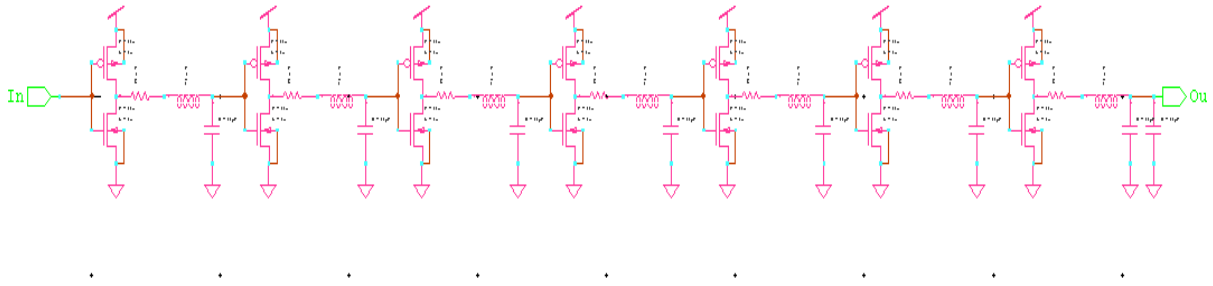

Figure 5.2: Distributed RLC model for interconnect to calculate delay and power.

The problem in lumped RLC model is that for high value of impedance parameters, the output does not have full voltage swing. The accuracy of the lumped RLC model can be improved by representing interconnects (especially for global interconnects) with a distributed RLC model in which impedance is distributed and repeaters are inserted between these impedance stages thus providing full voltage swing and better accuracy [21]. Hence for an interconnect optimum number of repeaters are calculated which gives the minimum PDP (power delay product).

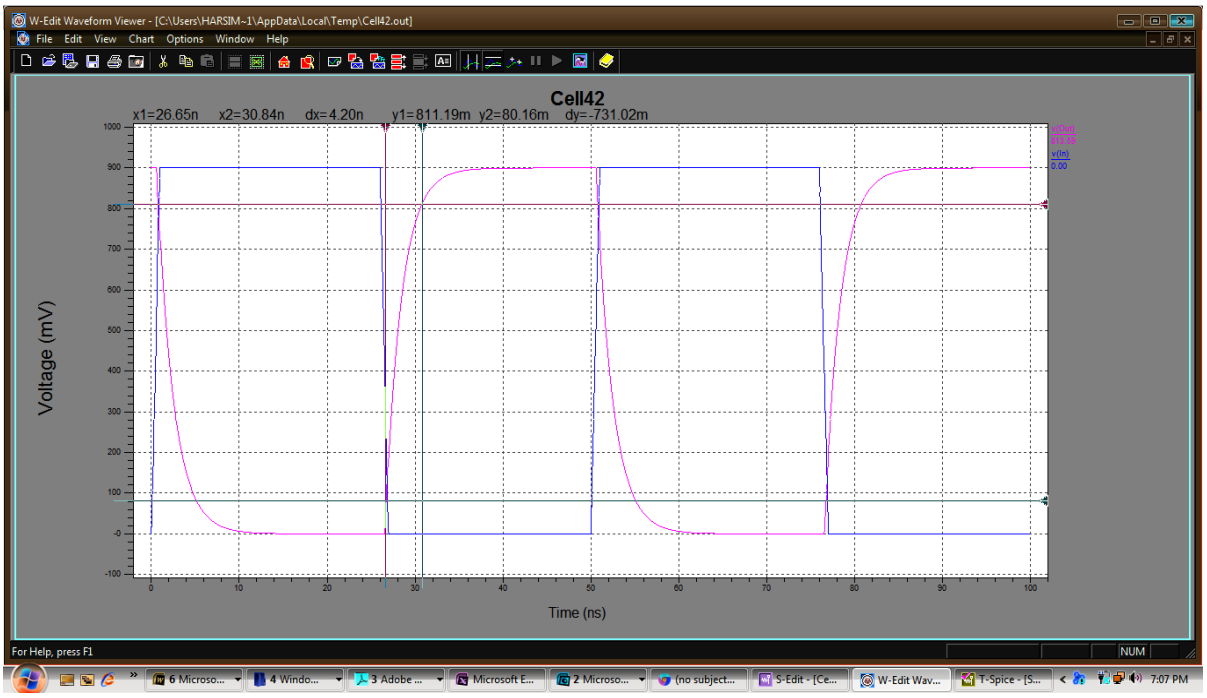

Figure 5.3: Snapshot of the input and output waveform in waveform editor for calculation of delay.

5.2 PERFORMANCE COMPARISON OF SWCNT AND COPPER INTERCONNECTS WITH BIAS INDEPENDENT MODEL

The performance of SWCNT bundle interconnects is compared to that of copper interconnects so as to determine their applicability in a VLSI design for future technology generations. In the case of global interconnects, in spite of imperfect metal-nanotube contacts densely packed SWCNT bundle interconnects show significant improvement in performance as compared to copper interconnects.

5.2.1 Variation of delay for SWCNT bundle and Copper interconnect with repeaters

Figures 5.4 and 5.5 show variation of delay for SWCNT bundle and copper interconnects with number of repeaters at different technologies for 1000um interconnect length. It is observed that the signal delay decreases when number of repeaters inserted are increased. This is because as the number of repeaters increase, long length interconnects are divided into small segments resulting in reduction of impedance parameters and the voltage signal degraded by these impedance parameters is restored by repeaters by achieving full voltage swing.

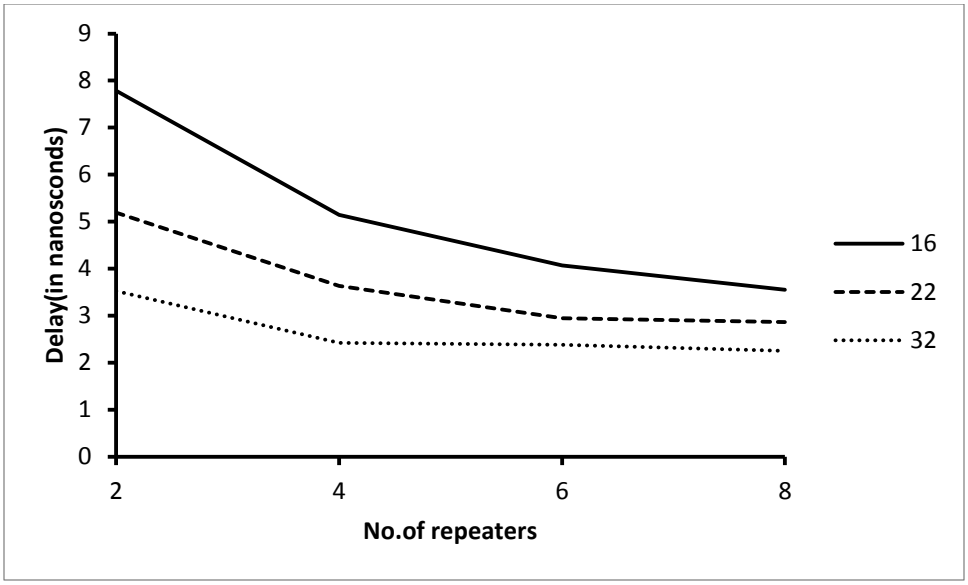

Figure 5.4: Variation of delay for SWCNT bundle interconnect with number of repeaters at different technologies for 1nm tube diameter and 1000um interconnect length.

With technology scaling, value of line resistance for both SWCNT bundle and copper interconnect increases whereas value of capacitance decreases. It can be seen from above graphs that as technology scaling is performed, signal delay increases due to resistance being more dominant factor than capacitance in determining delay of an interconnect.

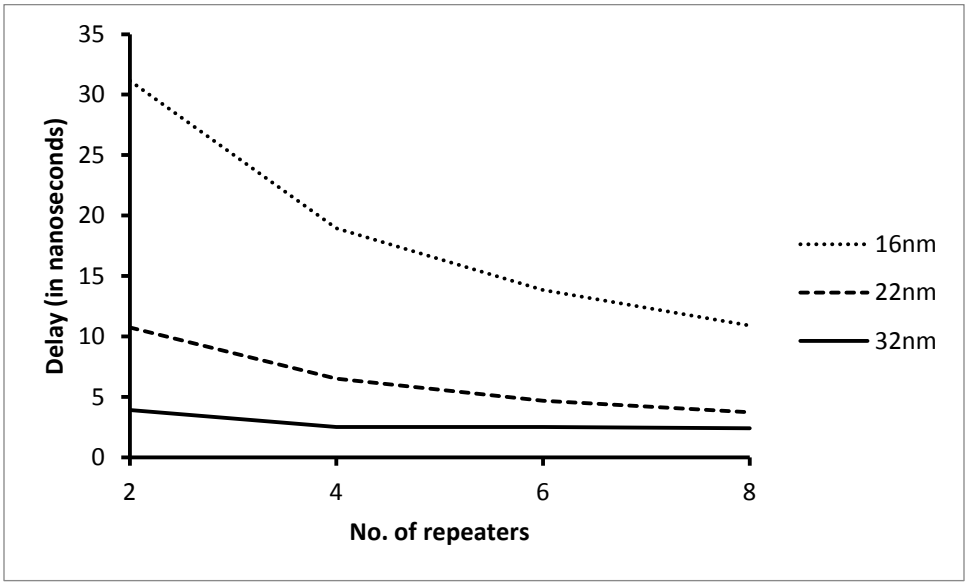

Figure 5.5: Variation of delay for copper interconnect with number of repeaters at different technologies for 1000um interconnect length.

5.2.2 Variation of power for SWCNT bundle and Copper interconnect with repeater

Table 5.2:Variation of power(in microwatts) of SWCNT bundle with number of repeaters at different technologies for 1000um interconnect length.

Technology (in nm)	Number of repeaters			
	2	4	6	8
32nm	81.415	81.860	82.520	83.104
22nm	48.290	48.600	49.080	50.027
16nm	29.600	30.329	31.236	32.269

Table 5.2 and 5.3 above shows variation of power of SWCNT bundle and copper interconnects with number of repeaters at different technologies for 1000um interconnect length. It is observed that with increase in number of repeaters, power increases as the number of repeaters inserted closely have large amount of short-circuit current and parasitic capacitance associated with them which results in an increased power dissipation.

Table 5.3:Variation of power(in microwatts) of copper interconnects with number of repeaters at different technologies for 1000um interconnect length.

Technology (in nm)	Number of repeaters			
	2	4	6	8
32nm	19.396	20.240	20.980	21.750
22nm	15.130	15.944	16.588	17.277
16nm	9.4600	13.210	15.000	16.433

Also as technology scaling is performed, the value of capacitance decreases for both SWCNT bundle and copper interconnect which results in decrease in power dissipation as there is a linear relation between capacitance and power dissipation ($P=CV^2f$) of an interconnect.

5.2.3 Variation of PDP (power delay product) for SWCNT bundle and Copper interconnect with repeaters

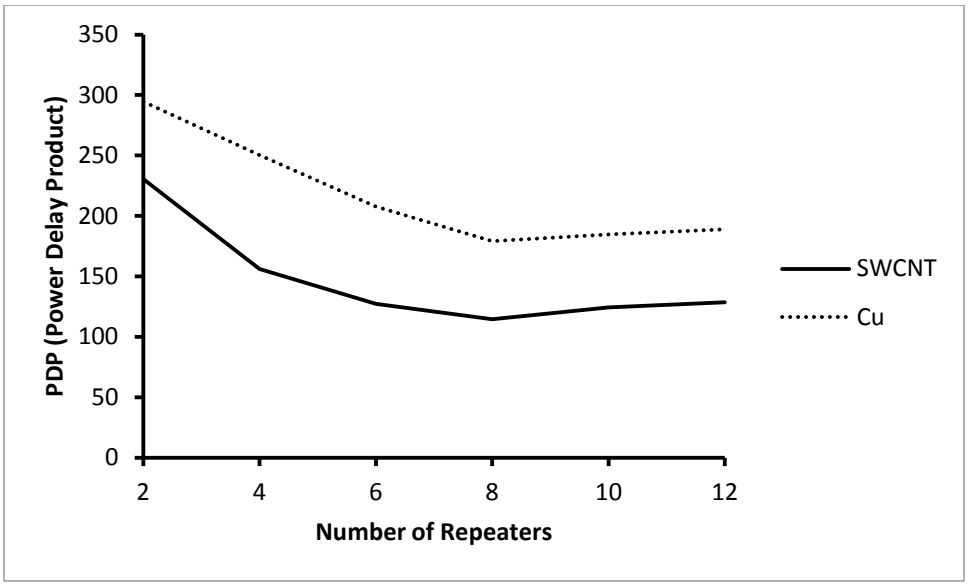

Figure 5.6:Variation of PDP (power delay product) of SWCNT bundle and copper interconnects with number of repeaters.

Figure 5.6 shows variation of PDP (power delay product) with the number of repeaters at 32nm technology for SWCNT bundle and copper interconnects of 1000um length. With increase in number of repeaters inserted, delay decreases and power increases. But after certain number of repeaters, the delay due to repeater itself becomes significant, thus degrading the performance. The optimum number of repeaters are chosen by the minimum value of PDP achievable at particular technology as the power delay product value determines the performance of an interconnect. The graph in Figure 5.6 shows that after eight repeaters, the value of PDP tends to rise for both SWCNT bundle and copper interconnects. So, eight is the optimum number of repeaters used for efficient performance of SWCNT bundle and copper interconnects at 32nm technology.

5.2.4 Variation of delay for SWCNT bundle and Copper interconnect with frequency

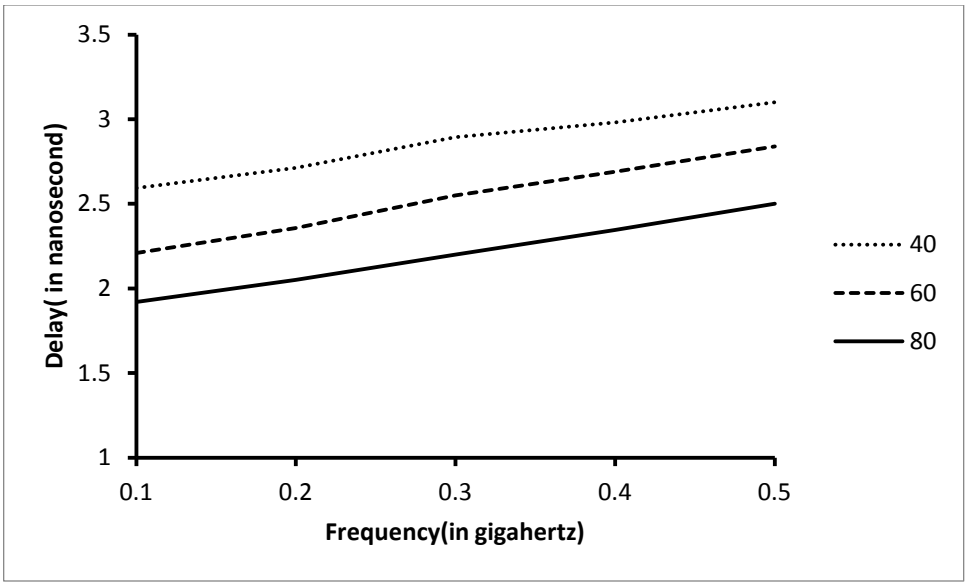

Figure 5.7:Variation of delay of SWCNT bundle of length 1000um with frequency for different aspect ratios at diameter 1nm.

Figure 5.7 and 5.8 shows variation of delay of SWCNT bundle and copper interconnect with frequency for different aspect ratios at 22nm technology with interconnect length of 1000um. It is observed that delay increases with increase in frequency for both SWCNT bundle and copper interconnect. This is because at higher frequency, the parasitic capacitances of the inverter comes into picture thus reducing the gain and increasing signal delay. Also with increase in the aspect ratio value, delay of both SWCNT bundle and copper interconnect decreases as at higher aspesct ratio due to larger size, the current conduction increases resulting decrease in delay. It can also be viewed that for any given value of frequency and aspect ratio, the signal delay for SWCNT bundle interconnects is less as compared to that for copper interconnects.

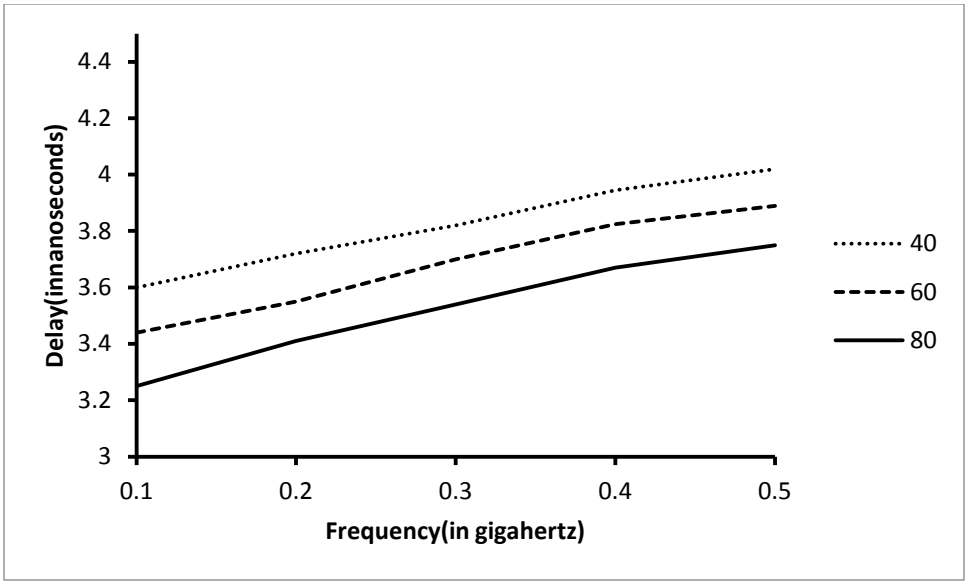

Figure 5.8: Variation of delay of copper interconnect of length 1000um with frequency for different aspect ratios.

5.2.5 Variation of power for SWCNT bundle and Copper interconnect with frequency

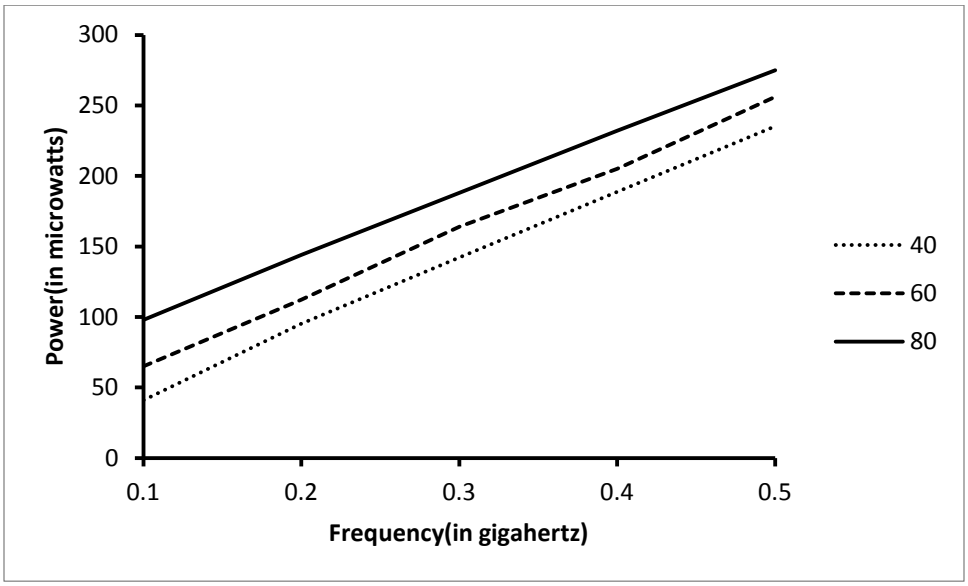

Figure 5.9: Variation of power of SWCNT bundle of diameter 1nm and length 1000um with frequency for different aspect ratios .

Figure 5.9 and 5.10 shows variation of power of SWCNT bundle and copper interconnect with frequency for different aspect ratios at 22nm technology with 1000um interconnect length. It is observed that as the aspect ratio value increases power dissipation for both SWCNT and copper interconnect increses. This is because at higher aspesct ratio due to

larger size, transistor conducts more resulting in more power dissipation. Also, as frequency increases there is more charging and discharging of load capacitor due to higher switching resulting in increase in power dissipiation for both SWCNT bundle and copper interconnect.

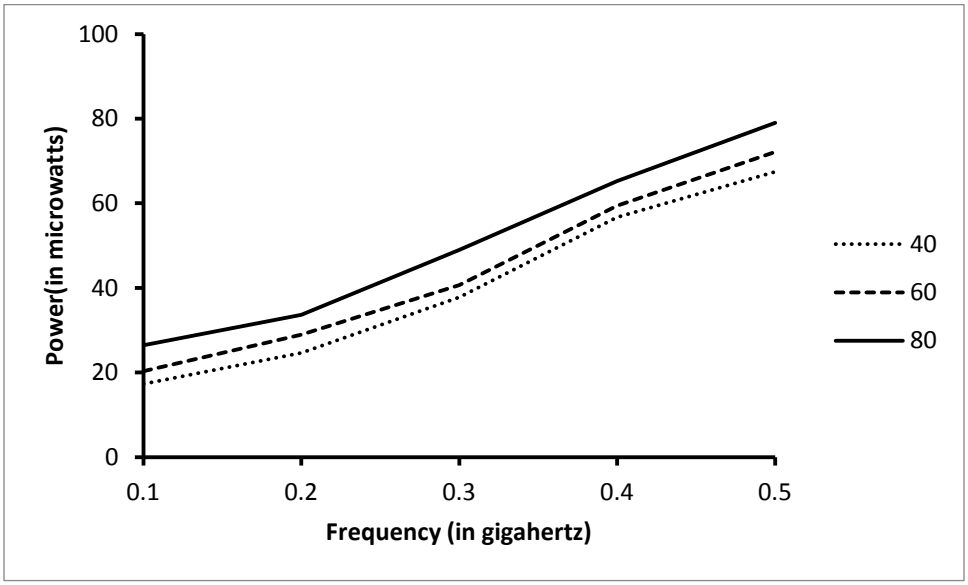

Figure 5.10: Variation of power of copper interconnect of length 1000um with frequency for different aspect ratios.

5.2.6 Comparison of delay and power for SWCNT bundle and Copper interconnect

Figures 5.11 shows variation of delay ratio of SWCNT bundle and copper interconnect for 1000um length with tube diameter at different technologies.The delay ratio in the graph is less than 1 showing that SWCNT bundle interconnects have smaller delay than copper interconnects at the below mentioned technologies. Also, the delay ratio decreases as technology scaling is performed proving that as one moves to higher future technologies the delay due to SWCNT is far less as compared to that of copper interconnect.With increase in diameter, the delay ratio increases so SWCNT nanotube with smaller diameter is preferable for better performance. In Figure 5.12, it is observed that the power ratio decrases as technology scaling is performed showing that as one goes towards higher technology the difference in the power dissipiated by SWCNT bundle and copper interconnect decreases, making SWCNT bundle a preferable candidate as VLSI interconnect at these technologies. With increase in diameter the power ratio decreases which is favorable. So an optimum tube diameter has to be choosed at which the PDP is minimum. Thus, SWCNT bundle is a favourable VLSI interconnect as compared to copper at the below mentioned technologies.

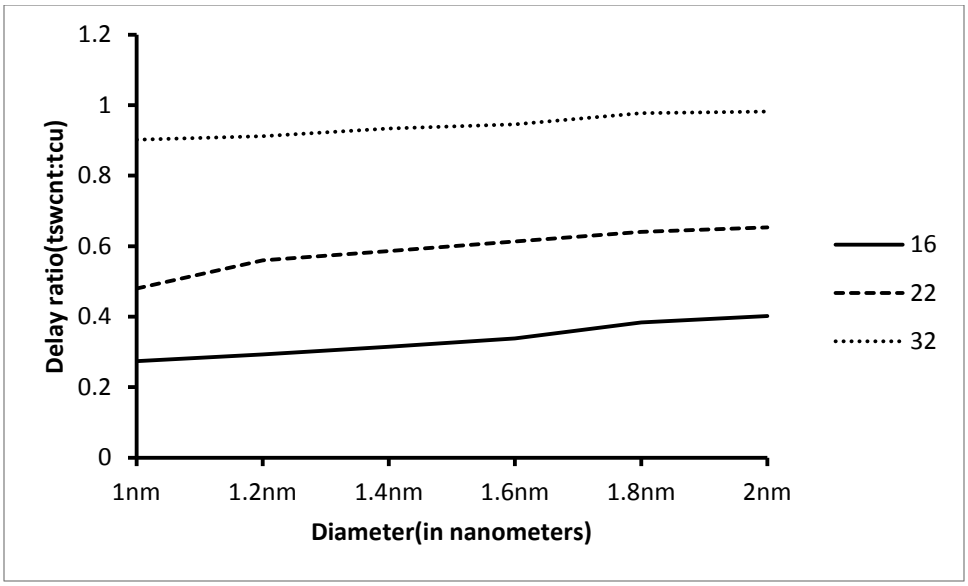

Figure 5.11:Variation of delay ratio of SWCNT bundle and copper interconnect for 1000um length with tube diameter at different technologies.

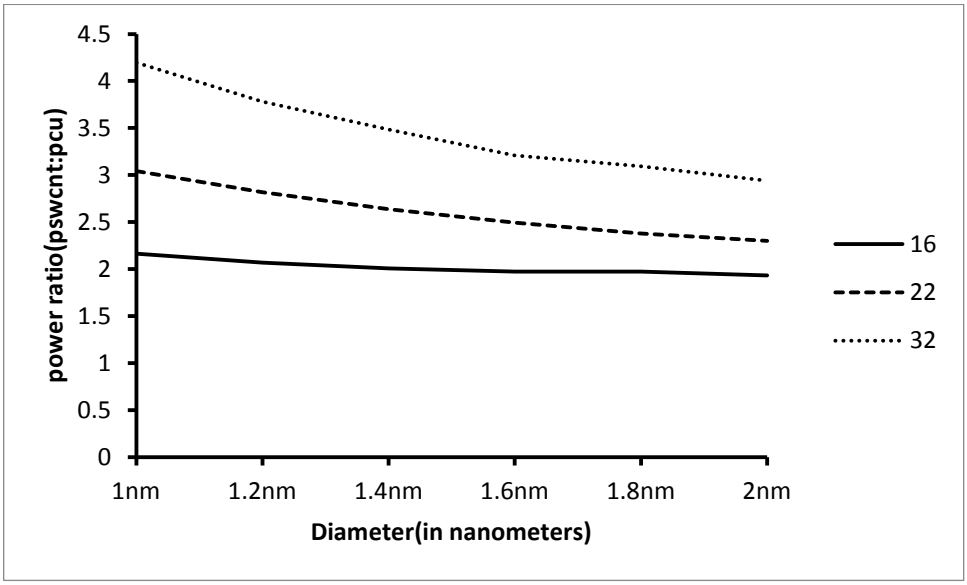

Figure 5.12:Variation of power ratio of SWCNT bundle and copper interconnect for 1000um length with tube diameter at different technologies.

5.3 PERFORMANCE ANALYSIS OF SWCNT BUNDLE INTERCONNECTS WITH BIAS DEPENDENT MODEL

Signal delay and power dissipation has significant impact on performance of SWCNT bundle interconnects. In this section signal delay, power dissipation and power delay product of SWCNT bundle interconnects is determined considering the bias

dependent equivalent circuit model. Repeaters are inserted (as shown in Figure 5.13) in the interconnect line to solve the latency problem of SWCNT bundle interconnects.

Figure 5.13: Optimum number of repeaters inserted to drive SWCNT bundle interconnects [15].

The signal delay decreases when number of repeaters inserted are increased as the voltage signal which is degraded by impedance parameters can be restored by these repeaters by achieving full voltage swing.

5.3.1Variation of delay of SWCNT bundle interconnect with repeaters and electric field

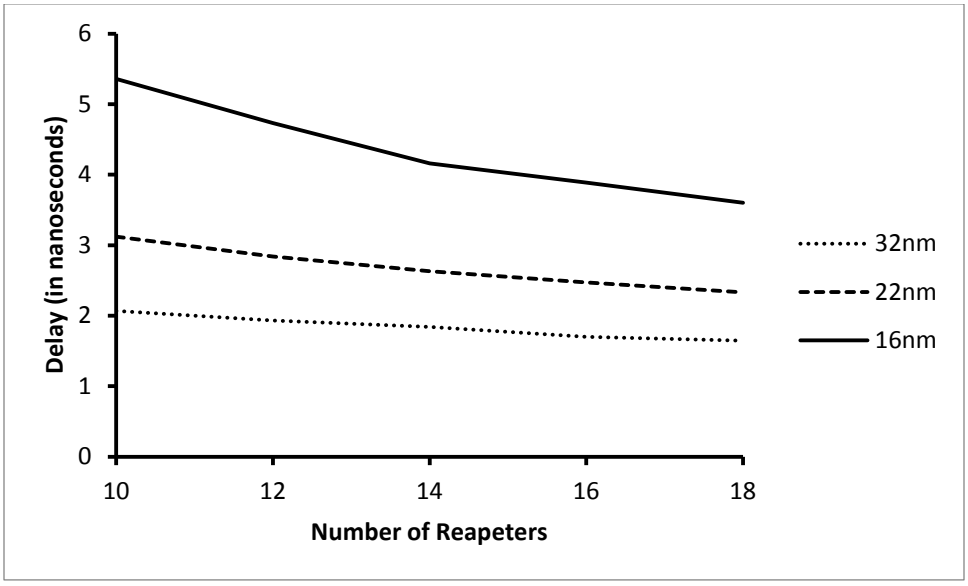

Figure 5.14: Variation of signal delay with number of repeaters at different technologies for length 1000um, diameter 2 nm and electric field 0.02V/um.

Figure 5.14 shows variation of signal delay with number of repeaters at different technologies for length 1000um, diameter 2 nm and electric field 0.02V/um. It is observed that with increase in the number of repeaters, there is decrease in the delay as more the repeaters more is the number of segments in which the interconnect is divided thus each segment having its impedance parameters divided by factor (N+1) where N is the number of

repeaters. So as value of N increases the value of impedance parameters for each segment decreases, thus making it more convenient for the repeaters to restore signal to full voltage. Also as technology scaling is performed, value of electrical resistance increases causing an increase in the delay of the SWCNT bundle interconnect.

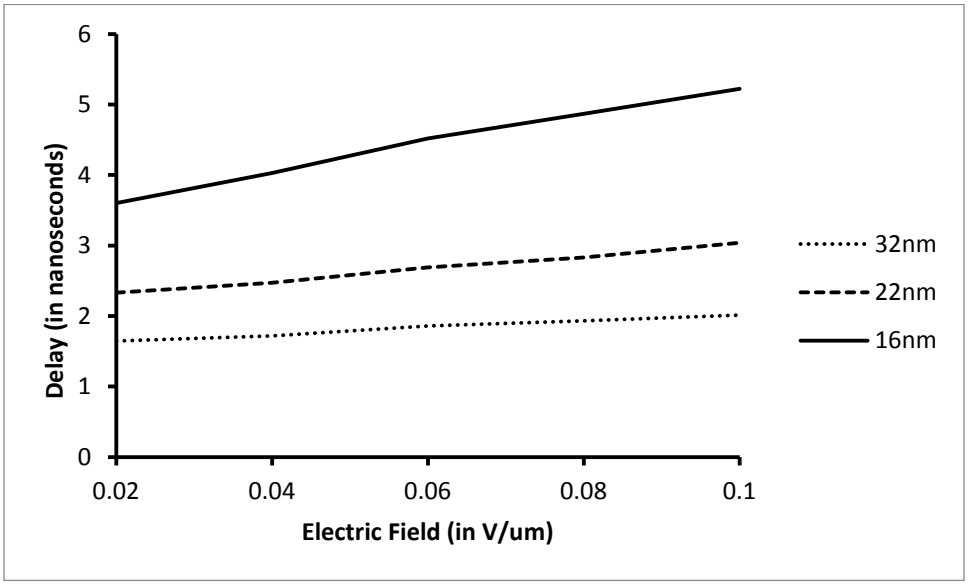

Figure 5.15: Variation of signal delay with electric field at different technologies for length 1000um and diameter 2nm.

The electric field variations have a significant impact on the delay of the signal propagating through the SWCNT bundle interconnects and hence the performance of the SWCNT bundle based integrated circuits will also be affected. On increasing electric-field across the SWCNT bundle interconnect signal delay increases as shown in Figure 5.15. This is because increase in electric–field causes increase in electron phonon scattering by accelerating electrons, thus resulting in sufficient energy gain up of electrons to emit phonons. Hence, increasing electrical resistance by decreasing effective mean free path which results in increase in signal delay. For a given value of the electric field, the electrical resistance increases with technology scaling causing further increase in signal delay.

5.3.2 Variation of power of SWCNT bundle interconnect with repeaters and electric field

Table 5.4: Variation of power (in microwatts) with number of repeaters at different technologies for length 1000 um, diameter 2 nm and electric field 0.02 V/um.

Technology (in nm)	Number of repeaters				
	10	12	14	16	18
32nm	59.180	59.765	60.562	60.985	61.603
22nm	38.455	39.000	39.502	40.059	40.646
16nm	28.621	29.592	30.547	31.625	32.739

The optimum number of repeaters used to reduce delay have a large amount of switching current associated with them due to full voltage swing achieved. Also as the number of these repeaters which are inserted closely increases, the large amount of parasitic capacitance and short-circuit current associated with them also increases. All these factors result in an increased power dissipation as shown in Table 5.4. Also with technology scaling, value of interconnect capacitance decreases resulting decrease in power as there is linear relation between power and capacitance.

Table 5.5: Variation of power (in microwatts) with electric field at different technologies for length 1000um and diameter 2nm.

Technology (in nm)	Electric field (V / um)				
	0.02	0.04	0.06	0.08	0.1
32nm	61.603	61.735	61.741	61.924	62.025
22nm	40.646	40.656	40.751	40.956	41.079
16nm	22.739	22.888	23.057	23.298	23.447

Table 5.5 shows variation of power dissipation with variation in electric field for different

technologies for length 1000um and diameter 2nm. With increase in electric field, power dissipation for every technology increases due to direct dependence of power density on electric field (P=IV/L) for the given range of applied bias. Thus due to decrease in power dissipation with decrease in electric field, it is favorable to work in low bias regime for SWCNT bundle used for interconnect applications. Also for a given value of electric field, power dissipation reduces as technology scaling is performed showing SWCNT bundle as suitable candidate for interconnect applications with higher technology at low bias.

5.3.3 Variation of PDP of SWCNT bundle interconnect with electric field

Power delay product (PDP) of an interconnect decides whether it has potential of being a reliable interconnect for the given technology. The power delay product of SWCNT bundle increases with increase in bias at different technologies (as shown in Figure 5.16) since both power and signal delay increases with increase in electric field across SWCNT bundle interconnect. Also, as technology scales, the PDP product decreases showing SWCNT bundle interconnect performs better at scaled technologies in the low bias regime for the above electrical model.

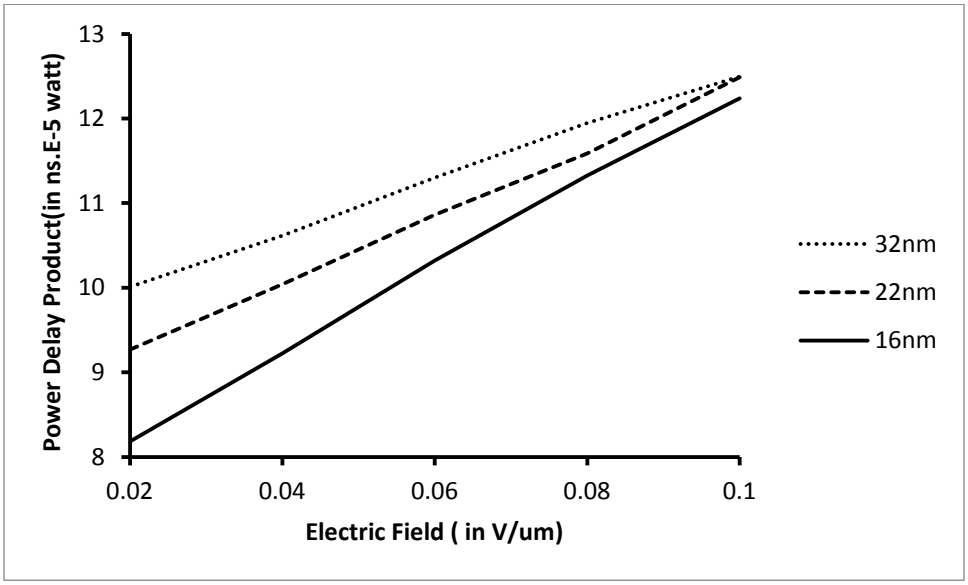

Figure 5.16: Variation of power delay product with electric field at different technologies for length 1000um and diameter 2nm.

CHAPTER 6

CONCLUSION

In this dissertation, applicability of SWCNT bundle as VLSI interconnect for nanoscale technologies is studied. For future generation of VLSI integrated chips, the limitations of copper interconnect dependent on scaling are going to be more and more severe. The alternate solution is the carbon nanotube interconnects to alleviate this problem. The behavior of single wall CNT and copper interconnect is analyzed by developing equivalent circuit model for both so as to evaluate various impedance parameters by means of their analytical expressions. Such an equivalent circuit model developed for single wall CNT and copper interconnect is used in simulation and analysis of interconnect performance. SWCNT bundle shows significant improvement in signal delay as compared to copper with technology scaling. SWCNT bundle has higher power dissipation as compared to copper but as technology scaling is performed, power dissipation due to SWCNT bundle decreases at a fast rate as compared to that of copper interconnect. The PDP (power delay product) of copper interconnects is much higher than SWCNT interconnects. Hence, SWCNT bundle is a prospective alternative to copper interconnects at future technologies. The effect of electric field on the delay of signal propagating along single wall CNT-based interconnects and its performance analysis is necessary to have more accurate results of delay and power. This work represents a study of electrical transport in SWCNT bundle interconnects, relevant for practical interconnect applications over a wide range of applied biases. The signal delay and power calculations show that increase in electric field across SWCNT bundle interconnect increases delay and power due to increased electron–phonon scattering. But, as technology scaling is performed, there is decrease in power delay product (PDP) with decrease in voltage bias across interconnect showing SWCNT bundle as a favorable future VLSI interconnect under low bias conditions at scaled technologies.

LIST OF PUBLICATIONS

[1] Harsimran Kaur, Karamjit Singh, "Performance Analysis of SWCNTs and their Comparison with Copper Interconnects for Nanoscale Technologies," International Conference on Electronics, Communication and Information Technology, October 2013.

[2] Harsimran Kaur, Karamjit Singh, "Effect of Electric Field on Metallic SWCNT Interconnects for Nanoscale Technologies," *Journal of Semiconductors* (communicated).

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APPENDIX

A.1 PTM level 54 model

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+tnom = 27	toxe = 1.1e-009	toxp = 8e-010	toxm = 1.1e-009
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+lw = 0	ww = 0	lwn = 1	wwn = 1
+lwl = 0	wwl = 0	xpart = 0	toxref = 1.1e-009
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