

Pipelined Analog to Digital Converter – Study and Design

A thesis submitted in the partial fulfillment for the
Degree of

**Master of Technology
in
VLSI Design & CAD**

Submitted by

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July 2011

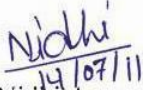
DECLARATION

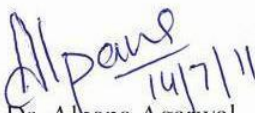
I hereby declare that the thesis report entitled “**Pipelined Analog to Digital Converter - Study and Design**” is an authentic record of my own work carried out as requirement for the award of Master of Technology in VLSI Design & CAD at Thapar University, Patiala under the guidance of Ms. Nidhi Agarwal, Project Faculty and Dr. Alpana Agarwal, Associate Professor, ECED during July, 2010 to July, 2011.

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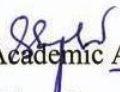
It is certified that the above statement is correct to the best of my knowledge and belief.


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ABSTRACT

Pipelined ADC offers attractive combination of high-speed, high-accuracy and low power consumption which makes it the most powerful and efficient data converter among others. However, the speed and the accuracy of pipelined ADC is limited by errors, such as capacitor mismatch, finite gain error, systematic offset and amplifier non-linearity.

With the advancement of Deep Sub-micron (DSM) technology, the low power supply became the trend of circuit designing. However, signal dynamic range decreases due to the reduction in the supply voltage which gives challenge to circuit designers to restore the dynamic range along with the reduction of noise and signal distortion. This work is divided in two parts: First, study of Pipelined Analog to Digital Converter to study the accuracy and various errors in pipelined ADC. Second, is its design for accuracy with low power. A resolution of 8-bit and 30 MSamples/sec sampling rate is chosen targeting the applications in Wireless Local Area Network (WLAN) and Wide Area Network (WAN).

Because of its simplicity, 1-bit/stage pipelined ADC architecture was chosen. Various building block of 1-bit/stage were designed. Single stage is designed from these building blocks, simulated in Cadence Analog Design Environment and results obtained were within $\frac{1}{2}$ LSB of required output. Cascading of two pipelined stages was done, simulated and observed results are also within $\frac{1}{2}$ LSB. It was observed that after cascading of more than 3-4 stages, residue voltage become more than 1LSB at some of the input voltages which causes wrong bit at the output. This thesis work could not extend after 3-4 stages due to lack of time in debugging the above issue.

The design was simulated in UMC 0.18 μ m Mixed Mode CMOS 1P6M process with power supply of 1.8V in Cadence Analog Design environment.

ACKNOWLEDGEMENT

First of all, I would like to express my gratitude to **Dr. Alpana Agarwal, Associate Professor**, Electronics and Communication Engineering Department, Thapar University, Patiala for her patient guidance and support throughout this work. I am truly very fortunate to have the opportunity to work with her. I found her guidance to be extremely valuable.

I am also thankful to **Ms. Nidhi Agarwal, Project Faculty**, Electronics and Communication Engineering Department for her time to time help in sorting out various technical issues faced while designing the pipelined ADC.

I am also thankful to **Dr. A. K. Chatterjee, Professor and Head**, Electronics and Communication Engineering Department. I found their guidance to be extremely valuable.

I also want to thank entire faculty, staff of Electronics and Communication Engineering Department, and then friends who devoted their valuable time and helped me in all possible ways towards successful completion of this work. I thank all those who have contributed directly or indirectly to this work.

I would like to thank my parents for their years of unyielding love and sacrifices. I would like to thank my wife for her constant support and encouragement. She is the real inspiration in pursuing my M.Tech study.

Lastly, I would like to thank all my class mates for their love and regard that they have given to me.

Anil Singh

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ABBREVATIONS

ADC	Analog to Digital Converter
DAC	Digital to Analog Converter
SNR	Signal to Noise Ratio
LSB	Least Significant Bit
DNL	Differential Non-linearity Error
INL	Integral Non-linearity Error
SNDR	Signal to Noise and Distortion Ratio
$\Sigma - \Delta$	Sigma-Delta
SAR	Successive-Approximation
S/H	Sample and Hold
PSRR	Power Supply Rejection Ratio
UGB	Unity Gain Bandwidth
ICMR	Input Common Mode Range
NMOS	n-type MOSFET
PMOS	p-type MOSFET
PM	Phase Margin
DSM	Deep Sub-Micron
WLAN	Wireless Local Area Network
WAN	Wide Area Network
MDAC	Multiply Digital-to-Analog Converter
UMC	United Microelectronics Corporation
DSP	Digital Signal Processing
OPAMP	Operational Amplifier

Chapter 1

Introduction

1.1 Background and Motivation

Most of real world signals are analog in nature, they are continuous-time and continuous-valued signals. Compared to analog signals, digital signals have the following advantages:

- a) These are immune to electrical noise.
- b) These can be manipulated easily (DSP processing).
- c) These easy to store.
- d) These are easy to copy and transfer.

Thus there is a trend to move signal processing from the analog domain to the digital one such as digital signal processing. Besides above advantages it allows for a higher level of accuracy, provides savings in power consumption and silicon area, increases robustness, speeds up the design process, brings flexibility and programmability and increases the possibilities for design reuse.

Because of above benefits of working in digital domain, there is a need to convert the analog real world signals to digital discrete-time, discrete-value signals. Analog to digital converters (ADC) convert the analog signals in digital domain for DSP processors to process and digital to analog converters (DAC) does the reverse.

Analog to digital conversion is the process where analog signals are mapped onto digital code representations. Although the analog input signal can be represented in several domains (for example voltage, current, charge), it is assumed that the input is in the voltage domain in this thesis work. Also, the digital codes are assumed to be in the binary domain.

The analog input signal $V_{in}(t)$ is defined for each moment in time, and we suppose that it can take any value within a certain range:

$$-A_{\max} \leq V_{in}(t) \leq +A_{\max} \quad \text{where } A_{\max} \text{ is the maximum amplitude of signal}$$

To represent this signal in a limited amount of digital data, the input signal is sampled

on fixed time intervals and quantized in the amplitude domain. The sample frequency f_s of the converter determines the time interval between two consecutive sample moments, according to

$$f_s = \frac{1}{T_s}$$

Suppose that the digital output code at each sample moment consists of N bits, and the codes are equally distributed over the allowed input range. Then, the distance between each pair of successive codes is given by

$$V_{LSB} = \frac{A_{\max}}{2^N}$$

1.2 ADC Specifications

Using or designing ADC involves a proper understanding of their specifications. These give the information to the user about features and limits. The specifications can be divided in

- a) General specifications
- b) Static specifications
- c) Dynamic specifications

Each category will be illustrated in the following sections.

1.2.1 General Specifications

The most important general features of an ADC are the following:

Type of Analog Signal

The analog input signal of an ADC can be single ended, pseudo-differential or differential. Single ended signals are referred to an analog ground; pseudo-differential signals are symmetric with respect to a generic fixed voltage; differential signals are the difference between the inputs regardless of the common-mode voltage. The differential mode is the most used because of its good features. Like, for the same input signal swing it has twice the input range, higher common-mode rejection and a higher SNR.

Resolution

The resolution (N) is the number of bits that an ADC uses to represent its input.

Dynamic Range

The dynamic range is the ratio between the maximum input voltage and the noise level. The dynamic range determines the maximum SNR achievable.

1.2.2 Static Specifications

The main static parameters of an ADC are the following:

Analog Resolution

The analog resolution is the smallest analog input variation which produces a variation of 1 LSB in the output code and it is given by $\frac{V_{ref}}{2^N}$ where V_{ref} is the input range and N is resolution.

Analog Input Range

The analog input range is the peak-to-peak input signal (voltage or current) which generates, as output, a full-scale response.

Offset

The offset is the difference between the ideal and real input signal value to get a null output signal (it can be expressed as Volt, Amperes, LSB). The offset shifts all the quantization steps by the same quantity.

Gain Error

The gain error is the error on the slope of the straight line interpolating the transfer curve, which differs from a straight line of slope 1 (ideal data converter).

Power Consumption

The power consumption is the power consumed of the ADC during normal operations.

Temperature Range

The temperature range is the range of temperatures in which the ADC can operate, while maintaining a proper functionality.

Differential Non-linearity (DNL) Error

The output of an ideal converter switches from one code to the next for an equal input voltage step which is called code widths. DNL measures the difference in LSB of the code widths of two consecutive codes. It is shown in Figure 1.1 [1]

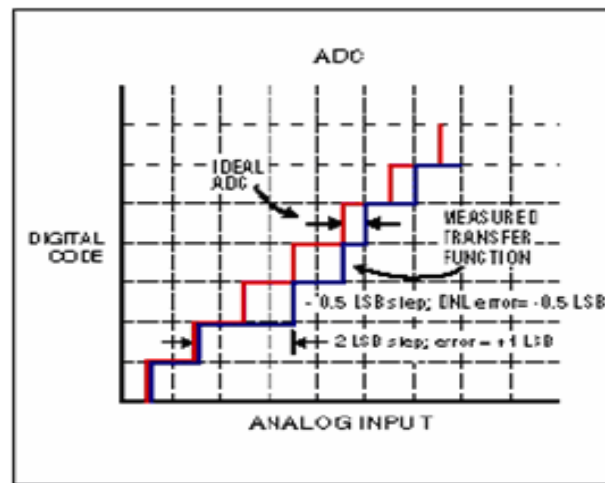


Figure 1.1: DNL Error [1]

Integral Non-linearity (INL) Error

INL on the other hand is defined as the deviation of the actual transfer function from a straight line after both offset and gain errors have been removed. INL is specified by its value of maximum deviation from ideal converter transfer function. Another method to define INL is endpoints line on best-fit line.

A good INL always indicates good DNL that is why the latter is not always included in the key parameter list. A DNL of less than ± 1 LSB guarantees a monotonic transfer function with no missing codes. It is shown in Figure 1.2 [1]

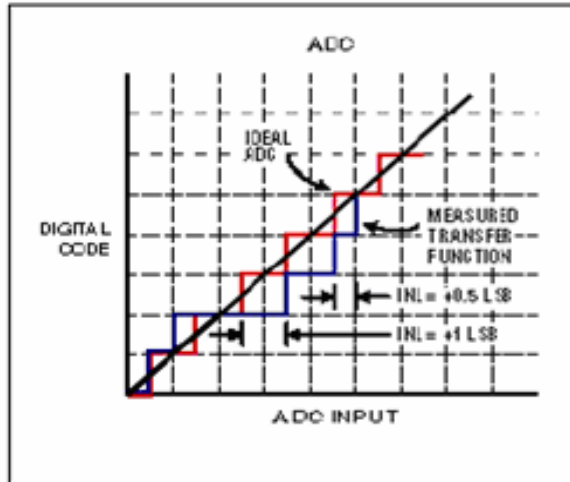


Figure 1.2: INL Error [1]

1.2.3 Dynamic Specifications

Analog Input Bandwidth

The analog input bandwidth specification is the frequency at which the output code is -3dB with respect to its low-frequency value.

Signal to Noise Ratio (SNR)

The SNR is the ratio between the power of the signal (normally sinusoidal) and the power of quantization noise and circuit noise. It is given in dB by

$$SNR = 6.02 N + 1.76$$

Signal to Noise and Distortion Ratio (SNDR)

The SNDR is almost equal to the SNR but in the power of noise, harmonic distortion is included. Mathematically, it is described as

$$SNDR_{dB} = 20 \log \left(\frac{A_{signal}}{A_{noise}} \right)$$

Where A_{signal} depicts the output signal level and A_{noise} describes the noise level.

1.3 Types of ADCs

High speed ADCs plays an important role in many digital signal-processing systems. Recently, the demands of consumer products such as video system, portable personal communication device, and LCD drivers are growing rapidly. In these applications, high speed medium-to-high resolution analog-to-digital converters are required.

In addition, the personal computing, communication, and various portable equipments, such as PDA and mobile phones, have become more popular. In order to increase the battery lifetime and reducing heat dissipation, the power reduction of integrated circuits is also becoming a major issue in these battery-based applications, especially the portable devices. From the other point of view, the growing market of portable applications, the process applications and the process technology scaling are driving the supply voltage of digital integrated circuit down to 1V, even lower. With the evolution of process, the power consumption of digital integrated circuit decreases as the supply voltage scales down. But the reduction of supply voltage makes analog integrated circuits design more challenging as it becomes more prone to noise and its leakage current increases.

For low speed, instantaneous or burst mode applications, successive approximation register ADCs are the best candidates. For high-resolution applications such as FM stereo, computer audio, stereo compact disc (CD), digital-audio-tape (DAT), and DVD audio, sigma-delta ADCs are popular, as a resolution from 12 to 24 bit could be achieved. For those applications that require both high speed and a moderately high resolution (>8 bits), pipelined ADCs are the best-suited candidates. High-speed and medium-resolution analog-to-digital converters (ADCs) are the vital elements in a wide variety of commercial applications including high-speed data conversion in communication systems, image signal processing and ultrasound front ends. In such applications, the reduction of power consumption associated with high-speed sampling and quantization is one key design issue in enhancing portability and battery operation. This trend is shown below in Figure 1.3 [1].

Today, markets that require “high speed” ADCs include many types of instrumentation applications (digital oscilloscopes, spectrum analyzers, and medical imaging).

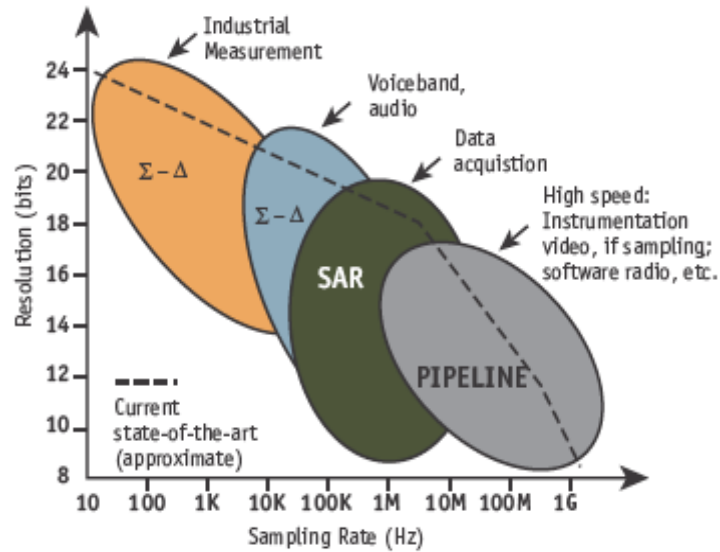


Figure 1.3: ADC architectures, applications, resolution, and sampling rates [1].

Also requiring high-speed converters are video, radar, communications (IF sampling, software radio, base stations, set-top boxes etc.), and consumer electronics (digital cameras, display electronics, DVD, enhanced-definition TV, and high-definition TV).

Among many types of CMOS ADC architectures, the pipelined ADC has the attractive feature of maintaining high accuracy at high conversion rate with low complexity and power consumption. Designing of pipelined ADC is pushed towards higher speed, higher accuracy and lower power dissipation by the rapid growth of process. These features make pipelined ADC more suitable for many applications than other ADCs.

Recently, the demand of consumer products such as video system, portable personal communication devices (WLAN transceiver) and LCD drivers is growing rapidly. In these applications, high speed medium-to-high resolution ADC is required. Taking above points, Pipelined ADC is chosen as a thesis work in this report, targeting WLAN and WAN applications with resolution of 8 bit and 30MS/s sampling rate. Table 1.1 shows the typical applications of Pipelined ADCs.

Table 1.1: Typical applications of pipelined ADCs

Resolution (Number of bits)	Application
8	Flat-panel displays, Lab instrumentation, HDTV, Medical imaging (low-end portable), WLAN and WAN, Radar
10	Flat-panel display, HDTV, Medical imaging (low-end portable), Cellular base-stations (power amp linearization), High-data-rate radios, Cable head-ends (for digitizing cable modem uplinks)
12	Cellular base-stations, Test equipment for ATE and comm., Cable head ends, Professional HDTV cameras, Medical imaging
14	Cellular base stations, particularly 3G multicarrier systems, ATE, High-end instrumentation, Military and aerospace

1.4 Thesis Organization

This thesis work is organized into five chapters. The remainder of this thesis work is organized as follows:

Chapter 2 describes 1-bit /stage pipelined ADC architecture. It discusses the design operation and related issues along with its Switch-Capacitor implementation.

Chapter 3 gives the brief introduction to BSIM3v3 behavior.

In Chapter 4, various building blocks of 1-bit/stage pipelined ADC are described. Various associated non-idealities and their impact on the performance of pipelined ADC are discussed in this chapter. Some solutions to these problems have also been suggested.

In Chapter 5, various layout techniques are discussed in order to design good designs. Layout of various building blocks is described in this chapter.

Chapter 6 concludes the work and throws light on the future scope of work.

Chapter 2

Pipelined ADC Architecture

2.1 Overview

A brief description of pipelined ADC architecture is presented in this chapter. Figure 2.1 shows the structure of a typical pipelined ADC with 1-bit per stage. Choice of resolution per stage is very important, and it can be referred in [2] for more details. It includes several cascaded stages. Each stage (shown in Figure 2.2) consists of a sample and hold (S/H) block, a sub-ADC (usually low resolution flash type ADCs), a sub digital-to-analog converter (sub-DAC), a sub-tractor and an inter-stage gain amplifier. Also, there is a bias generator for generating different potentials to be used in different blocks in pipeline - ADC and a clock generator circuitry, which generates 2 phase non-overlapping clocks to be used in pipelined ADC from external clock (clk_{in}).

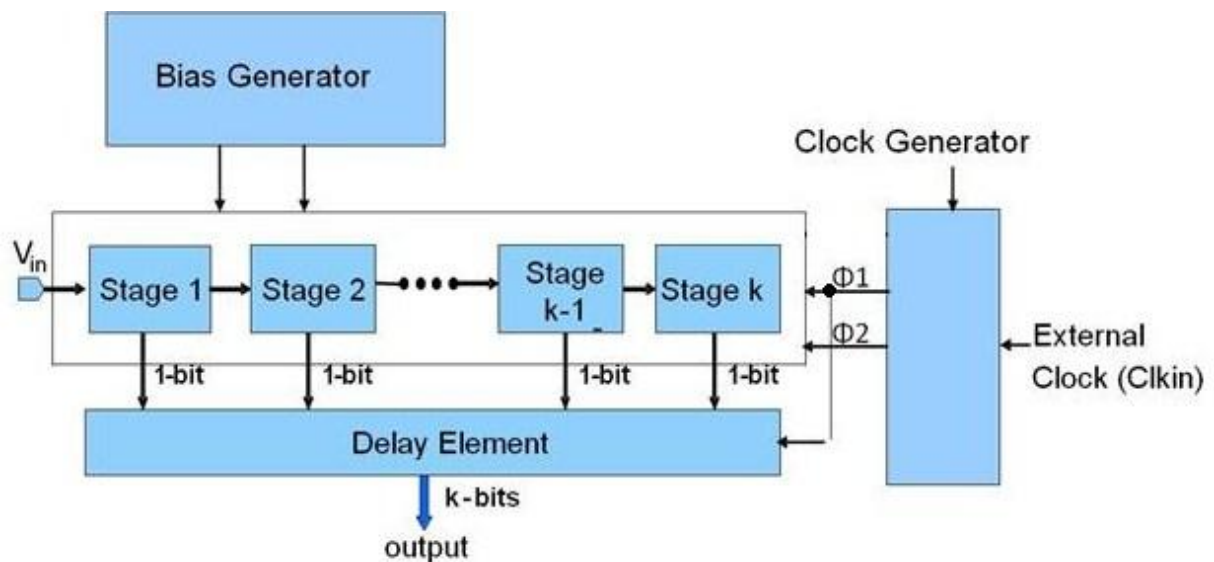


Figure 2.1: Structure of a typical k-bit pipelined ADC

Each stage (stage 1 to stage k-1, k=8 for 8-bit ADC) is shown in the Figure 2.2 except the last stage which is described in section 4.3.

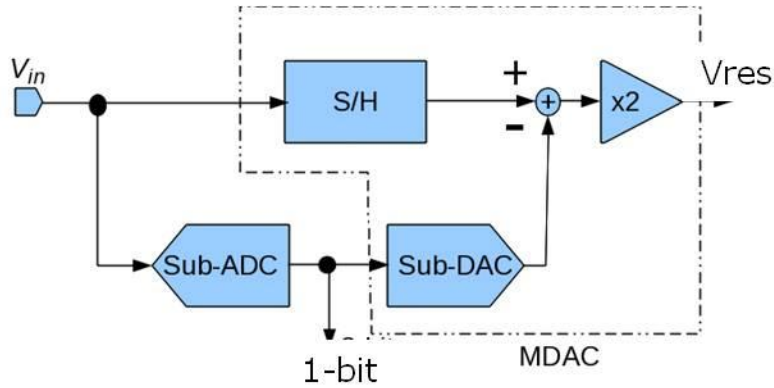


Figure 2.2: One stage in pipelined ADC

Each stage includes a sub-ADC and a MDAC block. MDAC is generally called Multiplying Digital to Analog Converter (MDAC) which includes a sub-DAC block, a sampler, a sub-tractor and multiply-by-2 amplifier. Output residue voltage generated by each block (V_{res}) is given to the next stage which acts as input for next stage.

The operation of each stage is as follows. The sampled input signal is first quantized by the sub-ADC to produce the output digital code for this stage. Then the output digital code is converted back to an analog signal by the sub-DAC. This quantized analog signal is subtracted from the original sampled input signal, resulting in a residue that is amplified to the full scale through inter-stage amplifier and then passed onto the next stage. This procedure is repeated till the last stage.

While the overall resolution of the pipelined ADC is the sum of the number of bits resolved in each stage, the most important feature of a pipelined ADC is the throughput behavior. For a pipeline with n -stages, the very first signal will take n -clock cycles to go through the entire n -stages. Of course, it will have the latency of n -clock cycles. The next signal will have the latency of $n-1$ clock cycles and so on. After n clock cycles, we will have a complete digital output in every clock cycle. Delay element is used to store the output bit generated by sub-ADC until all the bits are available.

Pipeline architecture ADCs rely on a two-phase, non-overlapping clock signal, which is generated from the external clock by the clock generator that is discussed in section 2.2.3. Φ_1 and Φ_2 are the two non-overlapping clocks as shown in the Figure 2.3 with $\Phi_1 \cdot \Phi_2 = 0$ every time.

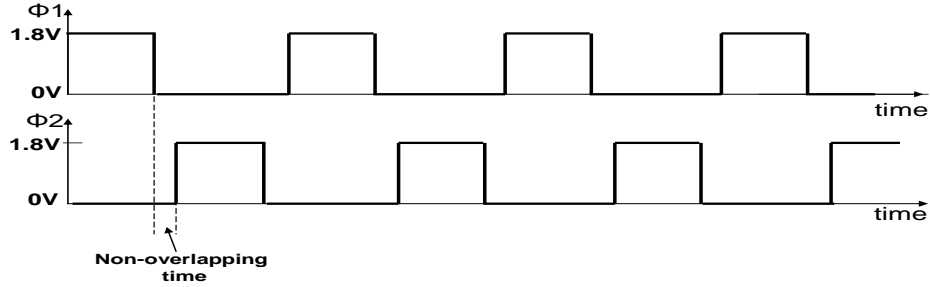


Figure 2.3: Two non-overlapping clock signals Φ_1 and Φ_2 used in pipelined ADC

Figure 2.3 shows an example of non-overlapping clock signals. This allows for all stages in the pipeline to operate concurrently. The operation of the stages is explained below. The clock has two phases: Φ_1 and Φ_2 . During Φ_1 phase, each stage samples the input signal, generates a digital output which is passed to delay element (consisting of latches) and an analog signal (the residue) during Φ_2 which is applied at the input of the next stage. Therefore while stage 3 is sampling the output voltage of stage 2 (V_{res2}) during Φ_1 phase, stage 2 will be sampling output voltage of stage 1 (V_{res1}) and stage 1 will be sampling the input voltage V_{in} at the stage 1 at the same time. Similarly amplifying operation will be performed during Φ_2 phase by each stage. So for 8-bit ADC, 8 clock cycles are necessary for the signal to propagate up to the output of the last stage. The digital outputs of the stages are delayed by latches a number of clock cycles to make up for the latency on the analog signal

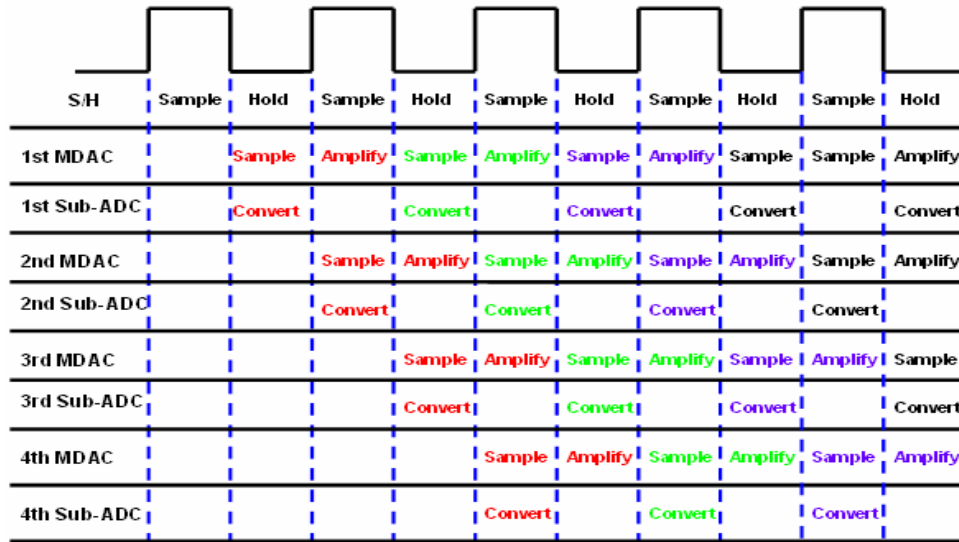


Figure 2.4: Controlling clocks for each stage [3]

logic 0 or logic 1 depending on whether V_{in} is less than V_{ref} or greater than V_{ref} respectively where V_{ref} is the reference voltage of comparator. C1P also acts as a select line for MUX2 as well as gives output bit to delay element (as shown in Figure 2.1). Based on C1P value, one of the inputs (V_{ref-} , V_{ref+}) is resulted at the output V_{dac} of MUX2. If $C1P = 0V$ (i.e. logic 0), $V_{dac} = V_{ref-}$ and when $C1P = VDD$ (i.e. logic 1), $V_{dac} = V_{ref+}$.

All the switches shown are of NMOS type for simplicity here. MOSFET switches are discussed in detail in the section 4.1.4. It is not necessary that all the switches be of NMOS type. Generally CMOS transmission gate switches are preferred due to their low resistance and wide signal swing.

In the sampling mode (Φ_1 high), M1 and M2 are closed and M4, M5 are open. Input signal V_{in} is sampled on both capacitors C_s and C_f . In this mode, M3 is also on so that right plate of capacitor is connected to common mode voltage V_{cm} as shown in Figure 2.6 due to virtual short property of OPAMP. Please note that MOS transistors which are open in this phase are not shown here. Comparator compares the input voltage V_{in} with V_{ref} and gives output C1P and MUX2 gives output V_{dac} based on the value of C1P as discussed above. This C1P is the output bit of the stage and stored in delay element. Output of sub-DAC, V_{dac} is stored in the parasitic capacitor C_p at that node for Φ_2 phase. Note that C_L shown at the output of OPAMP X1 is the parasitic load capacitor due to various parasitic capacitors present at that node.

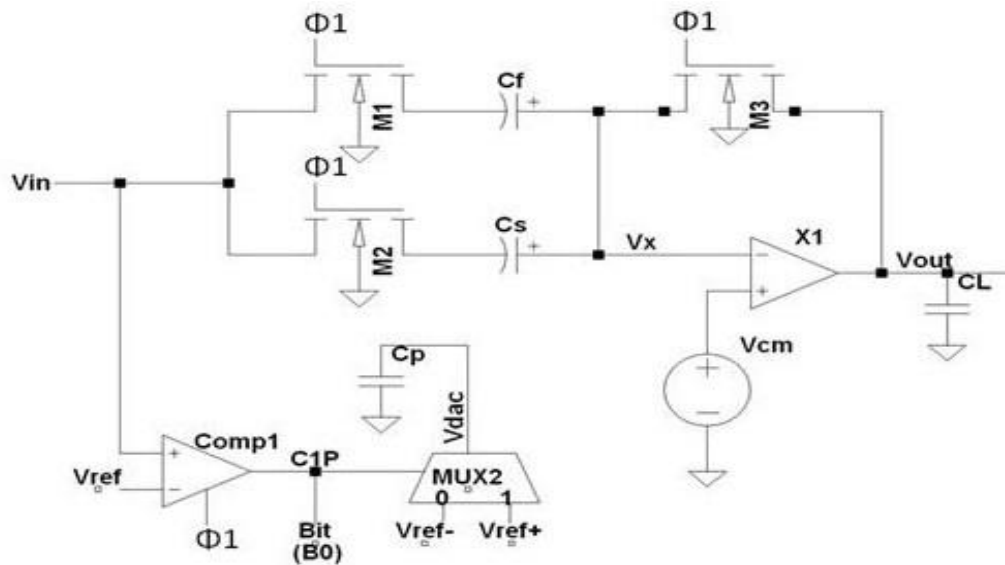


Figure 2.6: 1-bit/stage implementation in sampling phase (Φ_1 high)

In the amplifying mode (Φ_2 high), upon looking into Figure 2.5, M1, M2 and M3 are open and M4, M5 are closed. So bottom plate of capacitor C_f is connected to the output of OPAMP X1 and output of multiplexer (V_{dac}) is connected to bottom plate of capacitor C_s as shown in Figure 2.7. M6 is also ON during this phase. M6, capacitor C_h and OPAMP X2 in unity gain configuration work as sample and hold amplifier. Output of X1 is stored in C_h during this phase, therefore in CL (i.e. V_{out}).

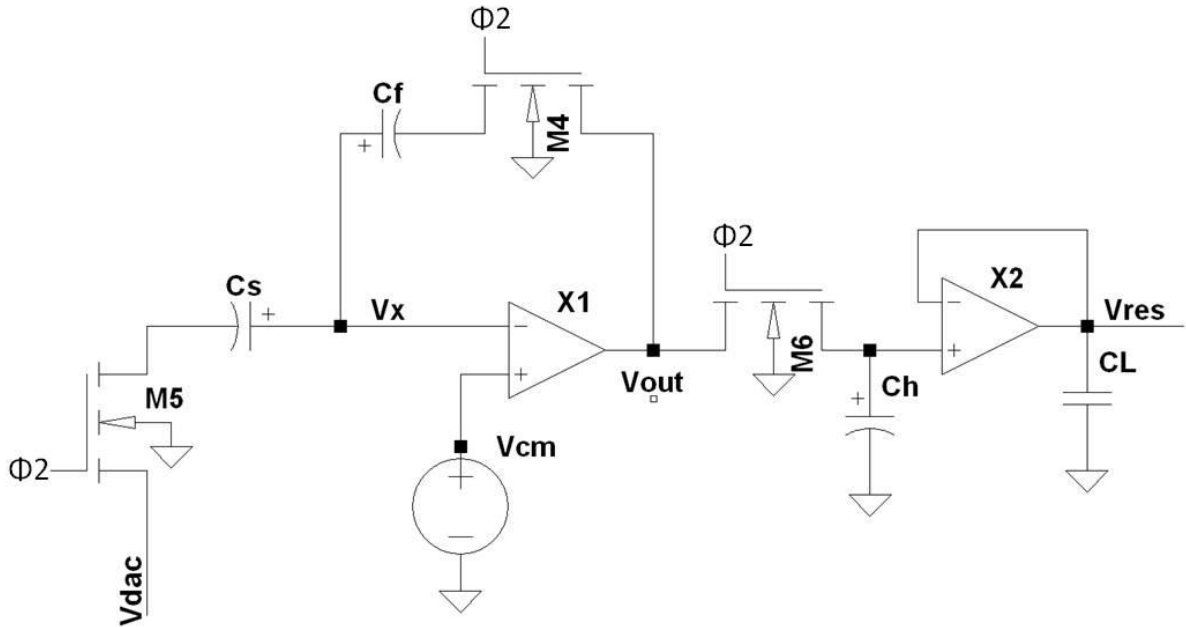


Figure 2.7: 1-bit/stage implementation amplifying phase (Φ_2 high)

When again Φ_1 phase will come, the value stored in C_h will work as input for next stage. Sample and hold amplifier is used to stabilize the output V_{out} and hence the input of next stage. If S/H amplifier (consists of M6, C_h and X2) is not used then output of OPAMP X1 will decrease as NMOS in the output stage of OPAMP is always ON, decreasing the output node. Therefore it is necessary to stabilize the output of MDAC, V_{out} . This point is discussed in detail in chapter 4.

The operation of 1-bit/stage circuit can also be described mathematically by the following equations.

During Φ_1 (refer Figure 2.6), C_s and C_f are charged to $V_{cm} - V_{in}$. So in this phase, charge stored in both capacitors is given by

$$Q_s = (V_{cm} - V_{in})(C_s + C_f) \quad (2.1)$$

In the equation (2.1), V_{cm} is dc bias voltage require to keep input MOS transistor of OPAMP in saturation. It is generally in the mid of ICMR of OPAMP. Here, OPAMP is assumed to be ideal with very high gain so inverting terminal is virtually connected to non-inverting terminal of OPAMP. V_{in} is the input signal that varies in between V_{ref-} and V_{ref+} .

In Φ_2 phase (refer Figure 2.7), charge stored in both the capacitors is given by

$$Q_a = (V_{cm} - V_{dac})C_s + (V_{cm} - V_{out})C_f \quad (2.2)$$

where V_{dac} is the output voltage from sub-DAC. Applying charge conservation at inverting terminal of OPAMP, we get

$$Q_s = Q_a$$

Solving equations (2.1) and (2.2) for V_{out} , we get

$$V_{out} = \left(1 + \frac{C_f}{C_s}\right)V_{in} - \left(\frac{C_f}{C_s}\right)V_{dac} \quad (2.3)$$

If $C_s = C_f$, then we get

$$V_{out} = 2V_{in} - V_{dac} \quad (2.4)$$

Thus, when $V_{in} < V_{ref}$,

$$V_{dac} = V_{ref-} \text{ and } V_{out} = 2V_{in} - (V_{ref-}) \quad (2.5)$$

When $V_{in} > V_{ref}$,

$$V_{dac} = V_{ref+} \text{ and } V_{out} = 2V_{in} - (V_{ref+}) \quad (2.6)$$

where V_{ref} is the threshold voltage of comparator comp1 as shown in Figure 2.5.

For $V_{in} = V_{ref}$, V_{out} can be followed by either equation (2.5) or (2.6) depending upon the offset voltage of comparator.

Chapter 3

Introduction to BSIM3v3 Behavior

3.1 General Information

In this chapter, behavior of MOSFET models used in thesis work is discussed. In older the CMOS processes greater than 2 μm , generally hand calculations and simulation results were comparable. The older MOS devices followed the “square-law” models which were analytical and matched SPICE (Simulation Program with Integrated Circuit Emphasis) Level 1 and 2 models. These models yield simulation results that match hand-calculations and give us the feedback that “I know what I am doing”. Reasonable hand calculation accuracy can be achieved in a process with L_{min} between 2 μm and 5 μm . However, if hand calculations, based on Level 1 models are used in DSM (deep submicron) process, the error is generally well above 100%.

As the dimensions of a MOSFET continue to scale down, a square-law model becomes less accurate. Modern MOS transistors have nonlinear, non-ideal behavior so using paper-pencil analysis is almost impossible so simulation is necessary to accurately predict the detailed circuit behavior. Even equations exists for gain, transfer characteristics, they are too time consuming to apply by hand for bigger circuits thus becomes impractical. The simulators accept the model of reality provided by designer and give us accurate results so it is very important to have models that are closer to silicon. Circuit designer needs to have a good intuitive understanding of circuit operation and should be able to predict the expected outcome before simulations instead of relying on simulation results because simulators are also prone to errors: garbage in, garbage out.

In today’s small dimension MOS transistor, BSIM (Berkeley Short Channel IGFET Model) is more accurate, silicon proven and widely accepted in the industry. There are many versions of BSIM models that grew with time. BSIM versions 1, 2, 3v3 and 4 are implemented as SPICE level 13, 39, 49 and 54 respectively. In the present work BSIM3v3 (Level 49) models have been used since technology is 0.18 μm . It is good for circuit simulations except it does not model gate leakage, which is supported in BSIM4 along with

other very thin gate effects.

Before starting design using such models, it is very essential to understand the behavior of models to know what the models are actually doing. It helps in design and analysis of MOS based circuits.

Following is the brief introduction to BSIM3v3 behavior. It includes short-channel effects such as mobility degradation, threshold voltage (V_t) variation, channel length modulation (CLM) effect and drain-induced barrier lowering (DIBL) [4].

3.2 Mobility Degradation

In scaled MOSFETs, the mobility of a carrier is severely reduced when gate-source voltage (V_{gs}) is high. With the large V_{gs} , a high vertical electric field draws the carriers in the channel closer to the surface of the silicon, resulting in reduction of the carrier mobility. This is shown in Figure 3.1.

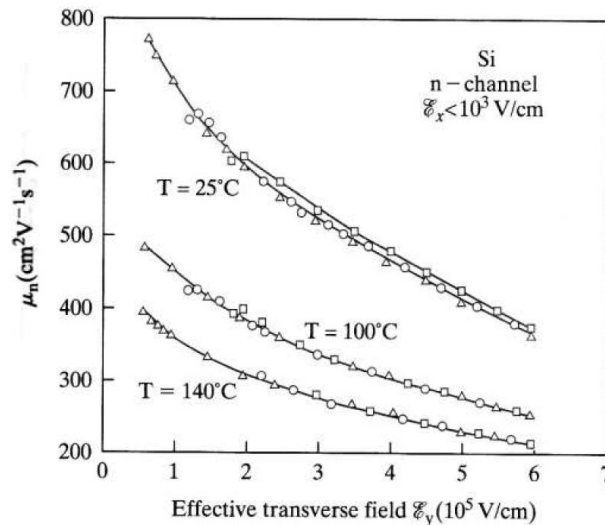


Figure 3.1: Electron mobility versus vertical electric field [4]

Since current flowing through MOSFET is dependent upon mobility which is now variable so current flowing through MOS also changes and hence its transconductance (g_m). It is shown in Figure 3.2 using UMC 0.18 μm CMOS 1P6M process with BSIM3v3 and Spectre (from Cadence) simulator.

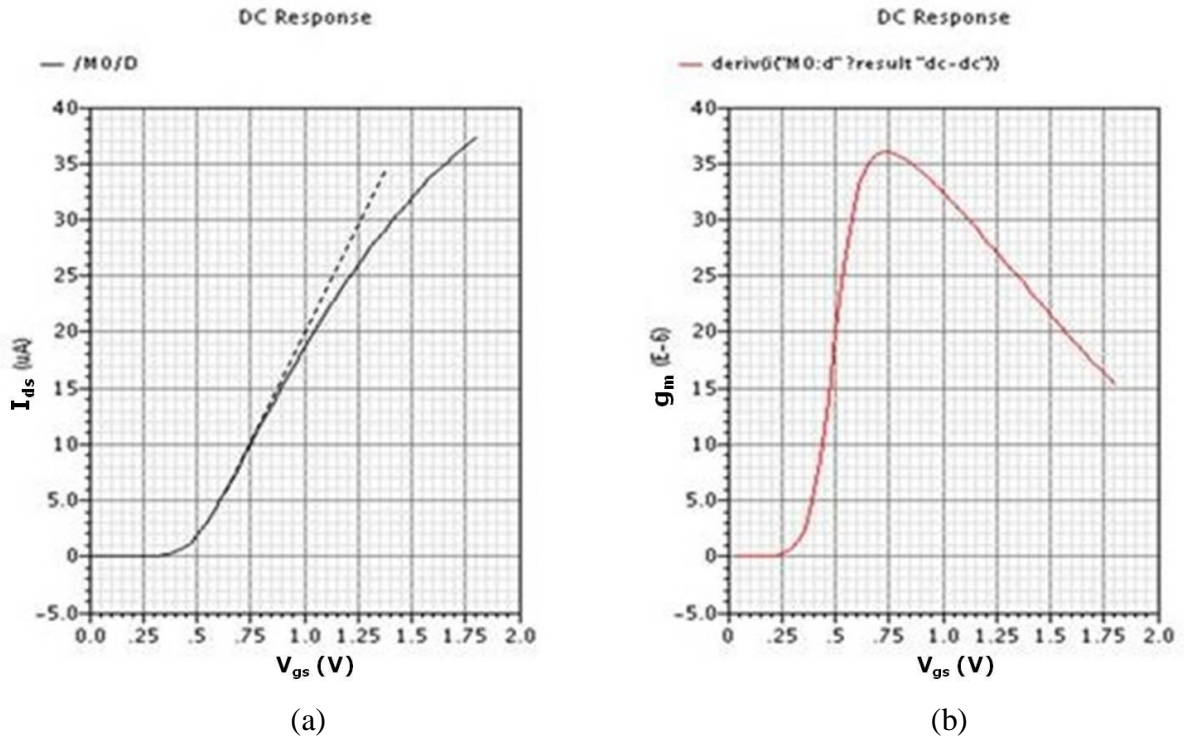


Figure 3.2: (a) I_{ds} vs. V_{gs} (b) g_m vs. V_{gs}

Figure 3.2 shows the variation in I_{ds} (current in NMOS) and g_m with variation in gate-source voltage, V_{gs} . Here, drain-source voltage, V_{ds} , applied is 0.5V for minimum W/L i.e. $0.24 \mu m / 0.18 \mu m$. It is clear from the Figure.3.2 (a) that I_{ds} deviates from its linear behavior (shown by dotted curve in a) at high V_{gs} due to vertical field mobility degradation at high V_{gs} [4]. Due to this g_m also decrease at high V_{gs} after reaching a maximum as shown in Figure 3.2 (b). Therefore while designing analog circuits where gain is important, high V_{gs} should not be used since g_m gives gain.

3.3 Output Resistance variation with V_{ds}

Output resistance (r_{out}) of a short-channel MOSFET working in the saturation region varies a lot with V_{ds} . This is depicted in Figure 3.3. When V_{ds} is relatively small, a variation of r_{out} is mainly caused by the channel length modulation. As V_{ds} increases, the depletion region of drain extends to the source and potential barrier between source and channel reduces due to DIBL. This lowers the threshold voltage of MOSFET (V_t) and therefore increases I_{ds} . In

short-channel MOSFETs, DIBL becomes more significant and V_t of a MOSFET, working in the saturation region is smaller than that of a MOSFET working in the linear region.

As V_{ds} further increases, r_{out} starts to decrease rapidly because of impact ionization [4]. In short-channel MOSFETs with small L , when V_{ds} is large, high lateral electric field accelerates the carriers in the channel. The accelerated carriers, which are also called as hot carriers, hit the silicon atoms, creating new electron-hole pairs. These newly generated electron and hole pairs increase the drain and substrate currents and reduce the output resistance (r_{out}) of MOSFET.

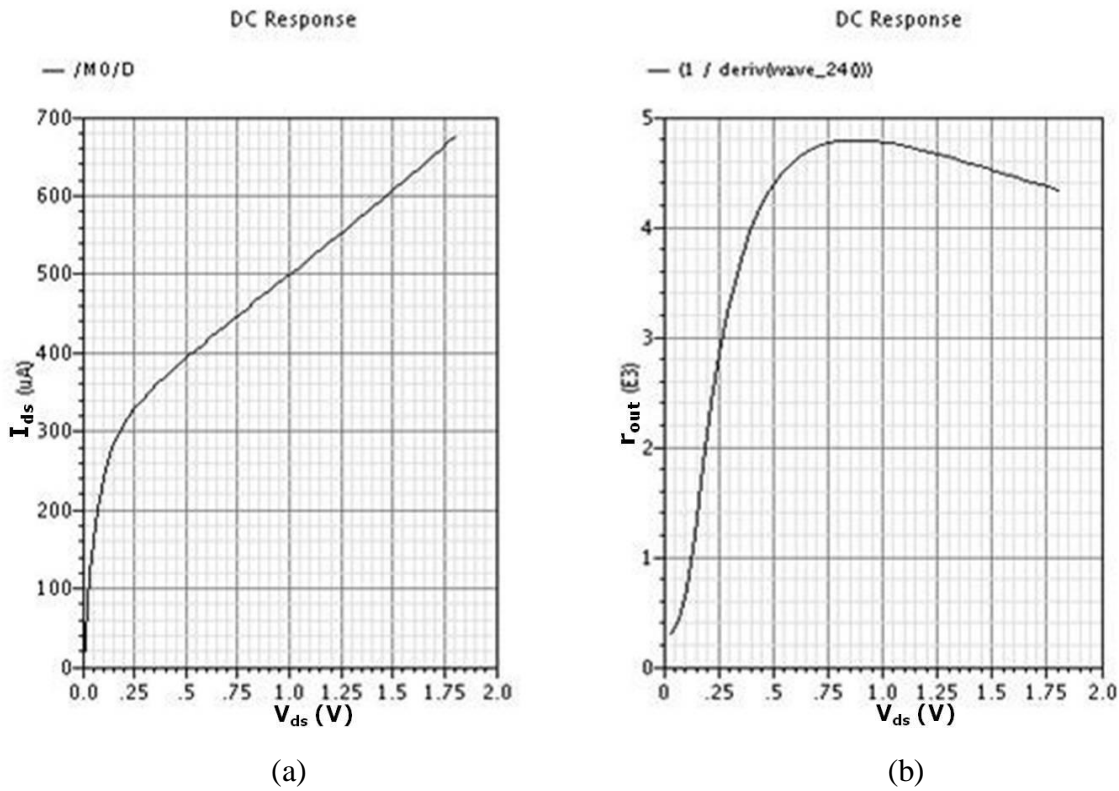


Figure 3.3: (a) I_{ds} vs. V_{ds} (b) r_{out} vs. V_{ds}

Above simulations are done at $V_{gs} = 0.6$ V and $W/L = 24 \mu\text{m} / 0.18 \mu\text{m}$. Width is taken 100 times the minimum width possible in $0.18 \mu\text{m}$ technology ($W_{min} = 0.24 \mu\text{m}$) in order to avoid the narrow width effects. It is clear from Figure 3.3 (a) that I_{ds} rises with V_{ds} reflecting CLM effect at low V_{ds} (after MOS is in saturation) and then DIBL effect. Output resistance r_{out} shown in Figure 3.3 (b) increase due to these two factors and reaches maximum. After this as V_{ds} increases further, r_{out} decreases due to impact ionization. Therefore, while

designing analog circuits where gain is important, V_{ds} of MOSFET should not be large since high gain requires high g_m and r_{out} .

Selecting the channel Length: As we know, r_{out} increases with increasing channel length (L) so to have high gain we should have high L (as r_{out} is proportional to L) but it decreases the speed of MOS transistor because of increase in intrinsic delay of MOSFET with L . Also layout area increases, which is a real-estate; therefore, using small L is usually desirable. Following are the simulations results for I_{ds} , V_s , V_{ds} , and r_{out} vs. V_{ds} using BSIM3v3 for NMOS of $W = 24 \mu\text{m}$ for $V_{gs} = 0.6\text{V}$ and various L ($L = 0.18 \mu\text{m}$, $0.36 \mu\text{m}$, $0.54 \mu\text{m}$).

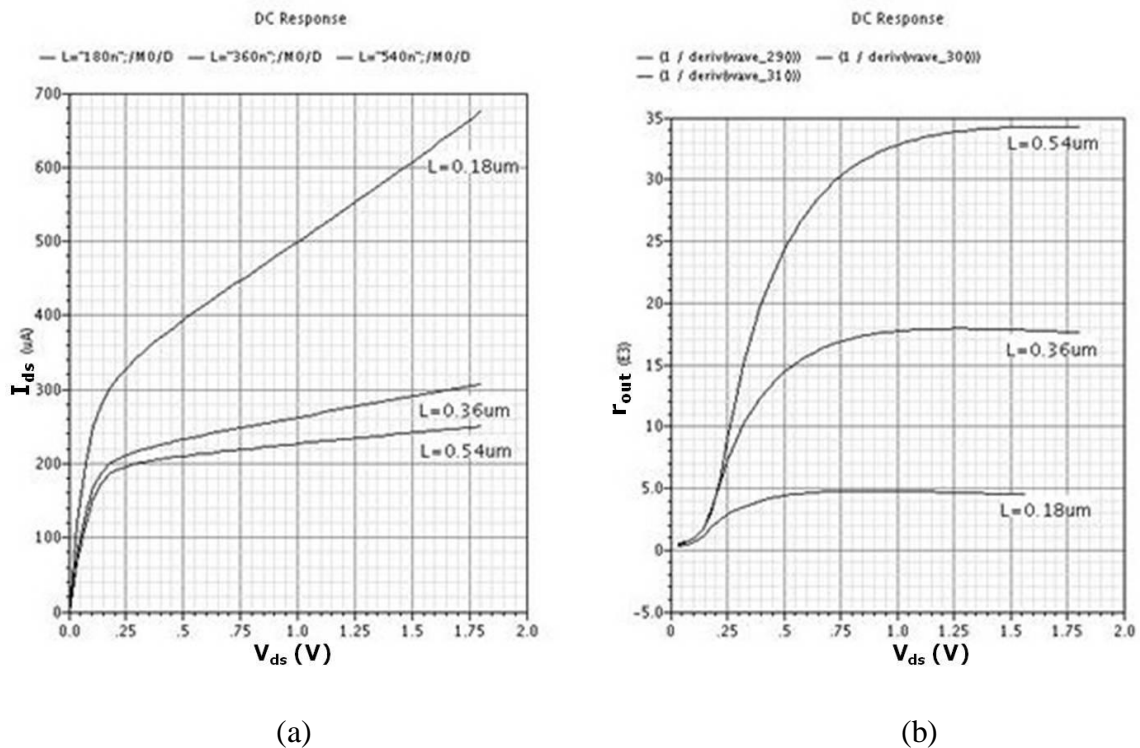


Figure 3.4: (a) I_{ds} vs. V_{ds} (b) r_{out} vs V_{ds} for different L (with same W)

It is clear from Figure 3.4 (b) that increasing L increases r_{out} and hence gain can be increased but this results in a decrease in speed. So choosing L of $0.36 \mu\text{m}$ is a reasonable tradeoff between gain, speed and area.

Selecting Overdrive Voltage ($V_{gs}-V_t$): While starting the analog designs, appropriate overdrive voltage ($V_{gs}-V_t$) is chosen. More is the overdrive voltage, more is V_{ds} required to

keep MOSFET in saturation and hence signal swing decreases along with decrease in r_{out} as described above. Also selecting high V_{gs} does not give us high gain. Thus it should be less. Threshold voltage of MOSFET changes with process and with temperature, so $(V_{gs}-V_t)$ should be as 100mV to provide some margins for these shifts.

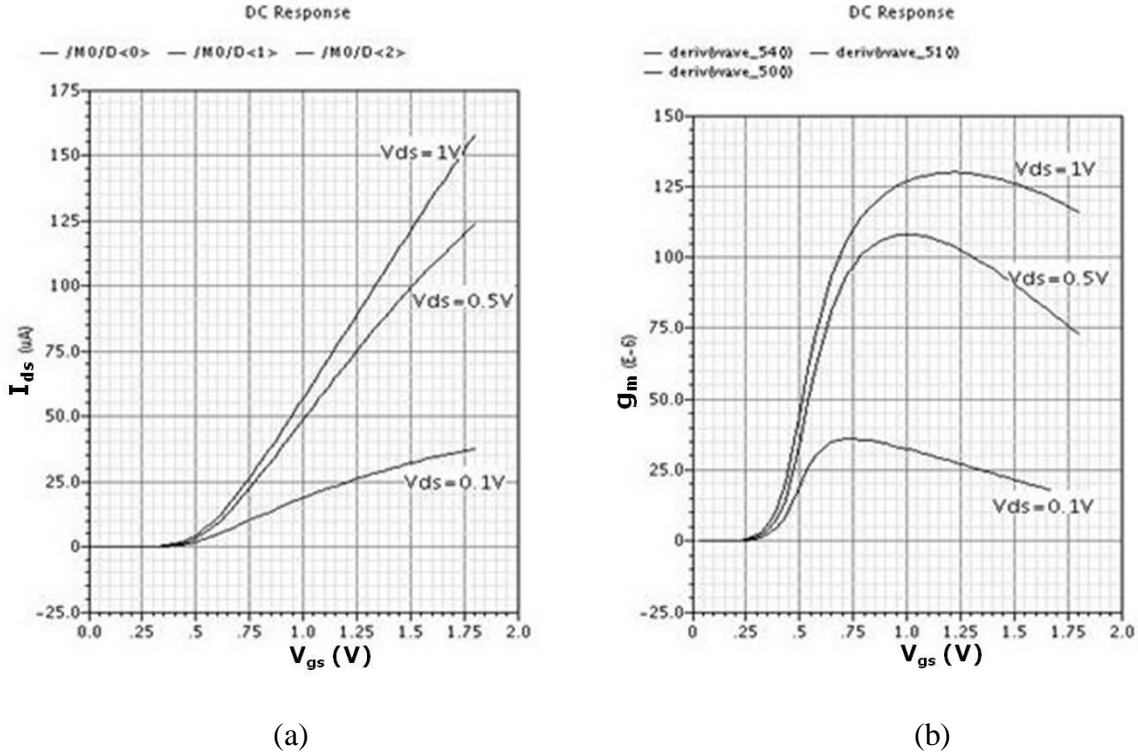


Figure 3.5: (a) I_{ds} vs. V_{gs} (b) r_{out} vs. V_{gs} for different V_{ds}

Simulations shown in Figure 3.5 are done at $W/L = 0.24 \mu m / 0.18 \mu m$ for different V_{ds} . From Figure 3.5, it is clear that at low V_{ds} ($=0.1V$) carrier mobility decrease with increase in vertical field at high V_{gs} . This is mostly the case when MOS transistor is in linear region. At high V_{ds} ($=1V$), we find the linear behavior in I_{ds} Vs. V_{gs} curve due to velocity saturation which occurs due to high lateral fields along the channel [4].

One interesting observation is changing W and L while keeping W/L ratio same. It has been observed that at minimum L , there is strong short channel effects such as DIBL (current increase at high V_{ds} due to decrease in V_t) as shown in Figure 3.6 (a). The W/L ratio was taken equal to 11.11 and $V_{gs}=0.6V$. Ratio was chosen after taking the W almost about ten times the W_{min} and taking the L equal to L_{min} (i.e. $W/L=2 \mu m / 0.18 \mu m = 11.11$). W and L increases by same factor to keep the ratio same. From Figure 3.6, it is observed that current at

$W/L = 2 \mu\text{m} / 0.18 \mu\text{m}$ is lesser than current at $W/L = 4 \mu\text{m} / 0.36 \mu\text{m}$ at low V_{ds} but crosses at high V_{ds} due to short channel effects. As both W and L increases (after $L = 0.18 \mu\text{m}$) same kind of curves are obtained but with high I_{ds} .

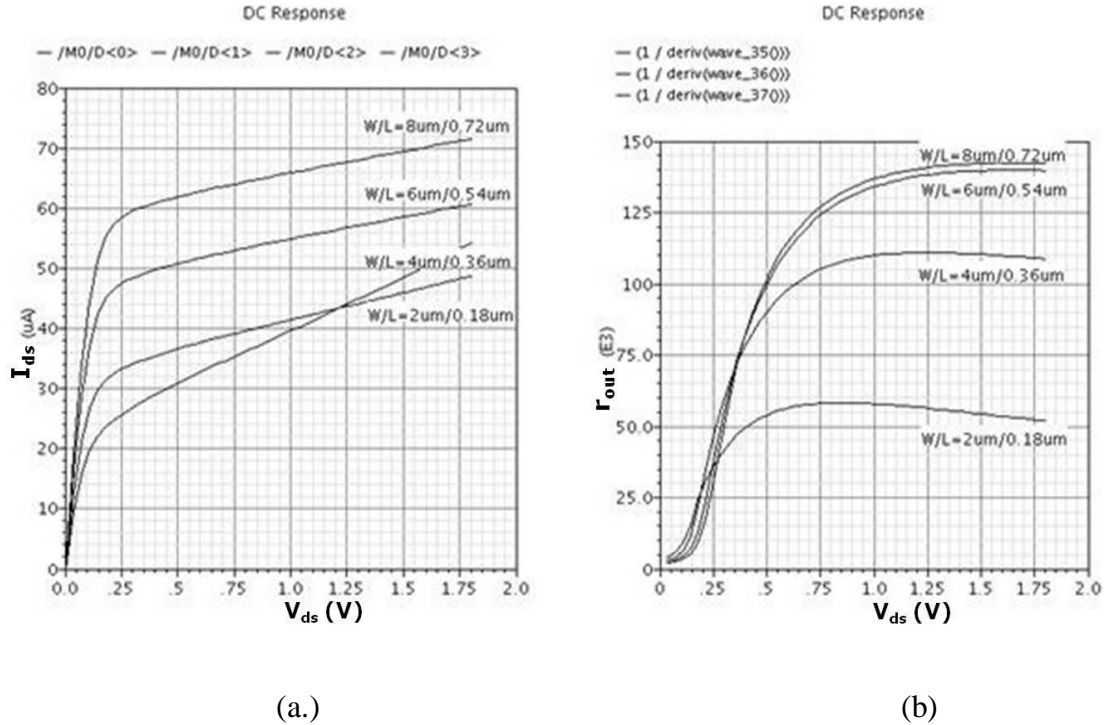


Figure 3.6: (a) I_{ds} vs. V_{ds} (b) r_{out} Vs. V_{ds} for same W/L ratio

In Figure 3.6 (b), we have less r_{out} for $W/L = 2 \mu\text{m} / 0.18\mu\text{m}$ but r_{out} then increases with increase in L for $W/L = 4 \mu\text{m} / 0.36 \mu\text{m}$ and almost same for $6 \mu\text{m} / 0.54 \mu\text{m}$ and $8\mu\text{m}/0.72\mu\text{m}$. This also tells how to choose minimum L .

Thus, it is very important to understand the model's behavior before starting the analog designs. Then only one will be able to design efficient designs.

3.4 Technology parameters and CAD tools

Following are the technology parameters for designing and CAD tools used in the present work for the design and verification.

Technology Parameters:

Foundry Specification : UMC 0.18 μm twin-tub CMOS 1P6M process

Supply Voltage range : 0V-1.8V

SPICE MOS Model : BSIM3v3 (Level 49)

CAD tools:

Schematic Entry : Cadence Schematic Entry Analog Design Environment

Simulator : Cadence Spectre and Synopsis HSPICE

Layout : Cadence Virtuoso

Layout Verification : Cadence Assura DRC/LVS

Extraction : Cadence Assura XRC Extraction tool.

Chapter 4

Design of Pipelined ADC

This chapter describes the design of pipelined ADC with architecture chosen in chapter 2 and shown in Figure 2.5. It is designed in 0.18 μm UMC CMOS technology with 1P6M process with 1.8V supply voltage. Various CAD tools used in the design and verifications are discussed in section 3.4. Design of various building blocks of 1-bit pipelined ADC stage and cascading of stages are described here.

4.1 1-bit MDAC Architecture

MDAC is called Multiplying Digital to Analog converter which includes a sub-DAC block, a sampler, a subtractor and multiply-by-2 amplifier, as shown in Figure 2.2 and Figure 2.5. OPAMP is the key part of the MDAC and worthy of most attention when designing a pipelined ADC. The main requirements on OPAMP design are high gain, large bandwidth, large slew rate, large signal swing, low noise, low power consumption and low power supply voltage. Besides these, high power supply noise rejection ratio (PSRR), high common mode noise rejection ratio (CMRR), small offset and small size are also desirable. Unfortunately, these factors cannot be improved together and many trade-offs exist among them. For example, an increase in bandwidth almost always necessitates an increase in power consumption. So a good OPAMP design is the optimization of these factors according to the design specification. But no real circuit can be ideal; due to various non-idealities in MDAC, performance of ADC is impacted. Targeting mainly WLAN applications, pipelined ADC specifications taken are [3]

- 1) Resolution(N): 8-bit
- 2) Sampling rate: 30MS/s

While designing, sampling rate is chosen 40MS/s instead of 30MS/s in order to take care of various non-idealities like process and temperature variations.

Let us first take the OPAMP. OPAMP in MDAC is the core circuit component. It must be designed very carefully. In OPAMP design we need to know

- 1) Capacitor sizes that can be determined from kT/C under certain percentage of quantization noise where $k = 1.38 \times 10^{-23}$ J/K is called Boltzmann constant, T is the temperature in Kelvin (K) and C is the capacitance in Faraday (F).
- 2) To know LSB, we need to know the full scale (FS) range that should be as high as possible.
- 3) FS range depends upon either maximum linear output swing that can be achieved by output stage of OPAMP or ICMR *e.g.* if in 1.8V supply designs, output swing is from 0.2V to 1.6V and ICMR is from 0.6V to 1.6V then FS will be decided by ICMR.

Capacitor sizes will help in deciding the load value of OPAMP and proper settling of OPAMP in a given time. It should be decided first.

Let FS=1V and N=8 so LSB is given by

$$\text{LSB} = \frac{FS}{2^N} = 3.9 \text{ mV} \quad (4.1)$$

Root mean square (RMS) value of noise, $V_{\text{noise,RMS}}$ is given by

$$V_{\text{noise,RMS}} = 10\% \text{ of LSB} = 0.39 \text{ mV}$$

Since
$$V_{\text{noise,RMS}} = \sqrt{\frac{kT}{C}}$$

So
$$C = \frac{kT}{V_{\text{noise,RMS}}^2} \cong 0.028 \text{ pF} \quad (4.2)$$

C_s and C_f values are chosen four times the above calculated in order to avoid mismatch due to process and to suppress the noise, thus $C_s=C_f = 0.1 \text{ pF}$.

It should be noted that here FS range is taken 1 V in the above calculations. While designing OPAMP if FS range changes, then we need to calculate the capacitor values again for the OPAMP to perform correctly. Calculation of FS range is described in section 4.1.2.

There are two capacitors C_s and C_f , sample the input during sampling phase (Φ_1) (Figure 2.6) and during amplification phase (Φ_2), C_s is connected to sub-DAC output V_{dac} and C_f is connected in feedback to the output of OPAMP (Figure 2.7).

One must remember that left side of both capacitors are bottom plates connected to the input signal during Φ_1 phase (shown curved plates) and top plates are connected to the input of OPAMP. Since bottom plates of capacitors has significant parasitic capacitors

between it and ground therefore it is always connected to less sensitive input side (e.g. input signal) rather than to the critical amplifier input side [6].

UMC 0.18 μm CMOS technology comes with a Metal/Metal Capacitor (MMC) module, also referred to as Metal Insulator Metal (MIM) capacitor module with Metal6 as top plate and Metal5 as bottom plate. It has a layer called MMC below Metal6 whose area (width x length) defines the capacitor value. UMC's MIM capacitor model's name is MIMCAPS_MM.

Minimum possible width of MMC layer = 1.28 μm

Minimum possible length of MMC layer = 1.28 μm

Therefore, minimum capacitor = (1.28 μm *1.28 μm) * C_{ox} = 2.0224 fF

Its diagrammatic layout is shown below.

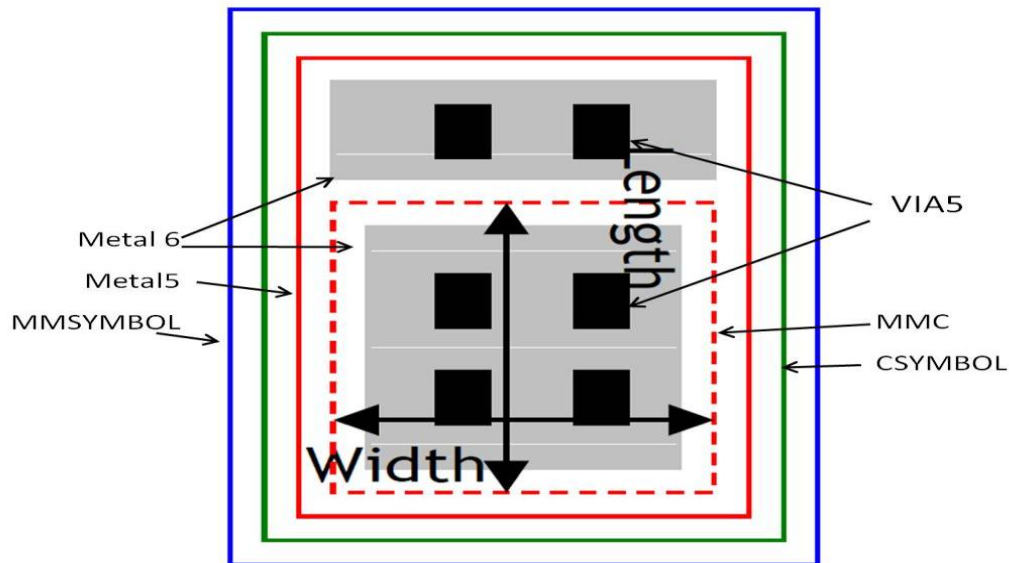


Figure 4.1: Diagrammatic layout of MIMCAP_MM capacitor along with various layers [5].

Next we will consider the non-ideal OPAMP and its impact on ADC performance.

4.1.1 Non-ideal OPAMP

Let us firstly take the real OPAMP. OPAMP is one of most important block in pipelined ADC. Various non-idealities of OPAMP are discussed here.

1) OPAMP having finite open loop gain A_0

Using ideal OPAMP, residue voltage of a stage is given by equation 4.3

$$V_{\text{out}} = 2V_{\text{in}} - V_{\text{dac}} \quad (4.3)$$

Let us assume that OPAMP has finite open loop gain A_0 and C_p is the input parasitic capacitance of an. OPAMP. During sampling phase Φ_1 (see Figure 2.6), total charge stored on capacitors C_s and C_f is given by

$$Q_s = (V_x - V_{\text{in}})(C_s + C_f) \quad (4.4)$$

During amplification phase Φ_2 (shown below for simplicity), total charge stored is given by

$$Q_a = (V_x - V_{\text{dac}})C_s + (V_x - V_{\text{out}})C_f + V_x C_p \quad (4.5)$$

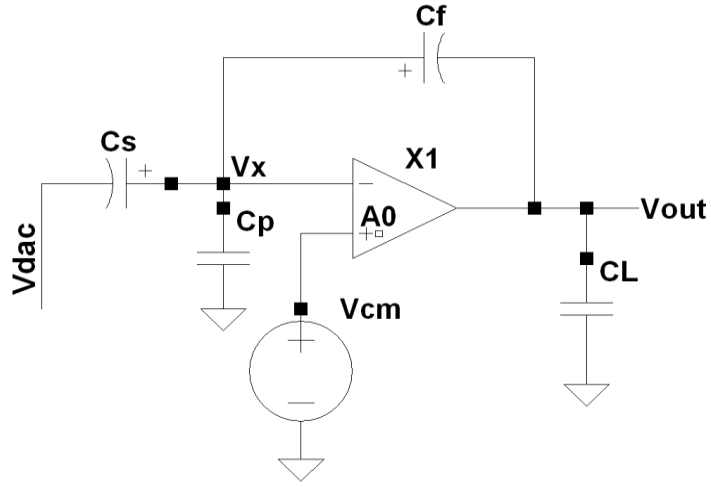


Figure 4.2: OPAMP with gain A_0 in Φ_2 phase

Where V_x is the voltage at the inverting input of the OPAMP and V_{dac} is the output voltage from sub-DAC. Applying charge conservation principle at inverting terminal of OPAMP, we get

$$Q_s = Q_a$$

Solving the equations (4.4) and (4.5) for V_{out} , we get

$$V_{\text{out}} = \left(1 + \frac{C_f}{C_s}\right)V_{\text{in}} - \left(\frac{C_f}{C_s}\right)V_{\text{dac}} + \frac{C_s + C_f + C_p}{C_f} V_x \quad (4.6)$$

Where term $\frac{C_f}{C_s + C_f + C_p}$ is known as feedback factor β and defined as how much of the output voltage of an OPAMP is fed back to OPAMP input.

$$\beta = \frac{C_f}{C_s + C_f + C_p} \quad (4.7)$$

Inverting input voltage V_x can be expressed as

$$V_x = - \frac{V_{out}}{A_0} \quad (4.8)$$

Solving equation (4.8) with equations (4.6) and (4.7) gives

$$V_{out} = \left(1 + \frac{C_f}{C_s}\right) V_{in} - \left(\frac{C_f}{C_s}\right) V_{dac} - \frac{V_{out}}{\beta A_0}$$

Solving for V_{out} , we get

$$V_{out} = \frac{\left(1 + \frac{C_f}{C_s}\right) V_{in} - \left(\frac{C_f}{C_s}\right) V_{dac}}{1 + \frac{1}{\beta A_0}} \quad (4.9)$$

Solving this equation (4.9) using first order Taylor expansion, we get

$$V_{out} \approx \left(1 + \frac{C_f}{C_s}\right) V_{in} - \left(\frac{C_f}{C_s}\right) V_{dac} \left(1 - \frac{1}{\beta A_0}\right) \quad (4.10)$$

Comparing it with ideal case of equation (2.3), we have a fractional error of $\cong \frac{1}{\beta A_0}$.

Therefore it requires a high value of open loop gain A_0 so that $\frac{1}{\beta A_0}$ factor is very less and we get output voltage V_{out} close to ideal value. For 8-bit, 40MS/s pipelined ADC there is a need to calculate the required gain and UGB of OPAMP as these decide the accuracy and speed of whole ADC. First stage is required to be designed very accurately/stringently as it generate the residue for next 7 stages.

For a N -bit ADC with a B -bit/stage architecture, the first stage gain error should be less than 1/2 LSB of the full range of the second stage ($= \frac{FS}{2^{N-B}}$) to prevent any missing codes. Therefore open loop gain of OPAMP should be [7]

$$A_0 > \frac{2 * 2^{N-B}}{\beta} \quad (4.11)$$

This is the minimum requirement on gain. Here, in this case, $B=1$ and $N=8$ so A_0 is 512 or 54dB for $\beta=1/2$. In practice, the DC gain should be much larger than this value, since errors caused by other sources such as capacitor mismatches, change in feedback factor due to input parasitic capacitance of OPAMP are not included in above equation (4.11). Also, to take care of process and temperature variations minimum open loop gain is taken as 70dB. In Φ_2 phase, OPAMP comes in closed loop with feedback factor of β , given by equation (4.7), so it should have phase margin (PM) of 55 to 60 degrees in unity gain feedback configuration.

2) OPAMP having finite Unity Gain Bandwidth (UGB):

The finite UGB of an OPAMP is another important non-ideality. It is important first to calculate the effective load seen by OPAMP. Consider a general case as shown in Figure 4.3 with OPAMP having output load capacitance C_L that OPAMP must drive. It includes mainly the gate cap of next stage plus wiring cap of interconnection along with the various diffusion capacitances present at that node of the driver itself. C_c is the compensation capacitance that is added to maintain the sufficient phase margin. At the input side, C_p represents parasitic capacitance due to input transistors of OPAMP and diffusion capacitance of switches.

Feedback network is due to capacitances C_s , C_f and C_p resulting in feedback factor given by equation (4.7).

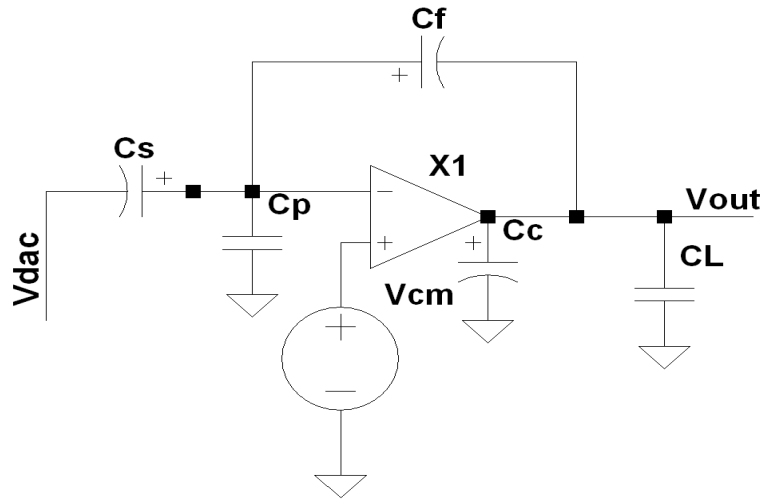


Figure 4.3: OPAMP in closed loop configuration in Φ_2 phase

Effective load capacitance seen by OPAMP X1 is given by [8]

$$\begin{aligned}
 C_{\text{load}} &= C_c \parallel C_L + (\text{series combination of } C_f \text{ with } C_s \parallel C_p) \\
 &= C_c + C_L + \frac{C_f(C_s + C_p)}{C_s + C_f + C_p} \quad (4.12) \\
 &= C_c + C_L + \beta(C_s + C_p)
 \end{aligned}$$

The speed of ADC is mainly limited by settling time of OPAMP which is dependent upon UGB of OPAMP.

In sampling phase since $\beta=1$, closed loop bandwidth is equal to UGB of OPAMP and settling time is given by

$$\tau(\text{sample}) = \frac{1}{2\pi \cdot \text{UGB}}$$

During amplification phase, β is given by equation (4.7), so closed loop bandwidth is now closely equal to $\beta \cdot \text{UGB}$ which results in longer settling time as compared to that during sampling phase. Settling time is now given by

$$\tau = \frac{1}{2\pi \beta \cdot \text{UGB}} \quad (4.13)$$

Where UGB is given by

$$\text{UGB} = \frac{g_m}{C_{\text{load}}} \quad (4.14)$$

Here, g_m is the transconductance of OPAMP input stage MOS and C_{load} is given by equation (4.12).

If a single-pole amplifier model is assumed, the output voltage of the gain amplifier is given by [7]:

$$V_{\text{out}}(t) = \left(1 + \frac{C_f}{C_s}\right) V_{\text{in}} - \left(\frac{C_f}{C_s}\right) V_{\text{dac}} (1 - e^{-\frac{t}{\tau}}) \quad (4.15)$$

Where τ is given by equation (4.8).

For pipeline ADCs, the allowed settling time is a little less than $\frac{1}{2}$ of a clock period. Then the minimum value for UGB of the amplifier should be [7]

$$\text{UGB} = \frac{N \cdot \ln(2)}{\beta \cdot \pi} \cdot f_s \quad (4.16)$$

where β is feedback factor and f_s is the sampling frequency.

So, if sampling frequency is 40 MHz, OPAMP is required with UGB of 141 MHz for $\beta = 1/2$. In order to take care of β change and other variations UGB is taken 3 times of the minimum required UGB which comes out to be 420MHz.

Note on feedback factor β : Feedback factor β is given by equation (4.7). If input parasitic capacitance $C_p = 0$ then for $C_s = C_f$, $\beta = \frac{1}{2}$ and OPAMP gives the required gain of 2 in Φ_2 phase. But due to input parasitic capacitance C_p , closed loop gain of the OPAMP changes from required gain of 2 due to change in β so it is important to have lesser input parasitic capacitance along with high A_0 . This requires careful sizing of input MOS transistors in OPAMP.

Timing requirements: Sampling frequency is known so clock period of internal clock phases Φ_1 and Φ_2 . need to be calculated for proper functioning of ADC. Since, sampling frequency f_s is 40MHz, so total time period of sampling clock $t_s = 25\text{ns}$.

From Figure 2.5, it can be seen that in Φ_1 phase input signal is sampled in capacitors and quantized by Sub-ADC. In Φ_2 phase, OPAMP X1 and X2 need to settle to $\frac{1}{2}$ LSB of required output. So out of total 25ns, Φ_2 phase require most of the time. We have divided total time period of 25ns as $\Phi_1 = 7\text{ns}$, $\Phi_2 = 13\text{ns}$ with non-overlap time of 0.5ns and rise time, fall time of both clocks with 1ns. Having larger Φ_2 time also relaxes the OPAMP specifications.

From this, it is clear that comparator must settle to final value within 7ns and amplification phase must settle to its final value (within $\frac{1}{2}$ LSB of required output) within 13ns.

4.1.2 Choosing OPAMP architecture:

Many good OPAMPs have been developed for different pipelined ADCs. Among them, the telescopic OPAMP and the folded cascode OPAMP are the most commonly used for their high gain and large bandwidth at given power consumption. While both OPAMP designs employ cascoded transistors to boost the OPAMP gain, they have many differences. The telescopic OPAMP has the advantages of higher speed and lower power consumption. But the folded cascode OPAMP has large output signal swing and large input common mode range. Another good OPAMP architecture is a two-stage OPAMP design using miller compensation. Although this two-stage OPAMP is usually slower than single stage designs, it can provide higher gain and large output signal swing, therefore is popular in low voltage pipelined ADC designs.

Besides cascode and cascade (multi-stage OPAMP), another way to increase OPAMP gain is gain-boosting technique which employs feedback scheme to enhance the output impedance of an OPAMP [9, 10]. This technique allows increase of gain without sacrificing UGB. If highest bandwidth is of interest, the G_m boost technique [9] which employs a wide band low gain preamplifier to boost the input equivalent G_m and so bandwidth without increasing input parasitic capacitance can be used.

Since in this work, although feedback factor (ratio of feedback capacitor to total

capacitor at the summing node) is $\frac{1}{2}$ and therefore required gain is 2 but we also require high UGB with phase margin of about 60 degree, so telescopic OPAMP has been chosen for its fast settling time and high UGB. This higher speed is obtained at the cost of lower ICMR. Figure 4.4 shows the circuit diagram of telescopic OPAMP used in this thesis work with VB1 and VB2 are bias voltages to bias the MOSFETs M3-M6 in saturation. R and C make the compensation network to tune the phase margin. R can be implemented by MOS working in linear region and C is MIMCAPS_MM capacitor available in UMC and described in section 4.1.

In Figure 4.4, M0-M4, M9 and M11 are NMOS transistors and M5-M8 and M10 are PMOS transistors. VB1, VB2 chosen in the design are 1.2V and 0.6V, respectively. Proper sizing of NMOSs M3-M4 and PMOSs M5-M6 is necessary so as to bias them in saturation. Choosing higher value of VB1 and VB2 decreases the ICMR as it will require higher V_{ds} to bias the transistors in saturation.

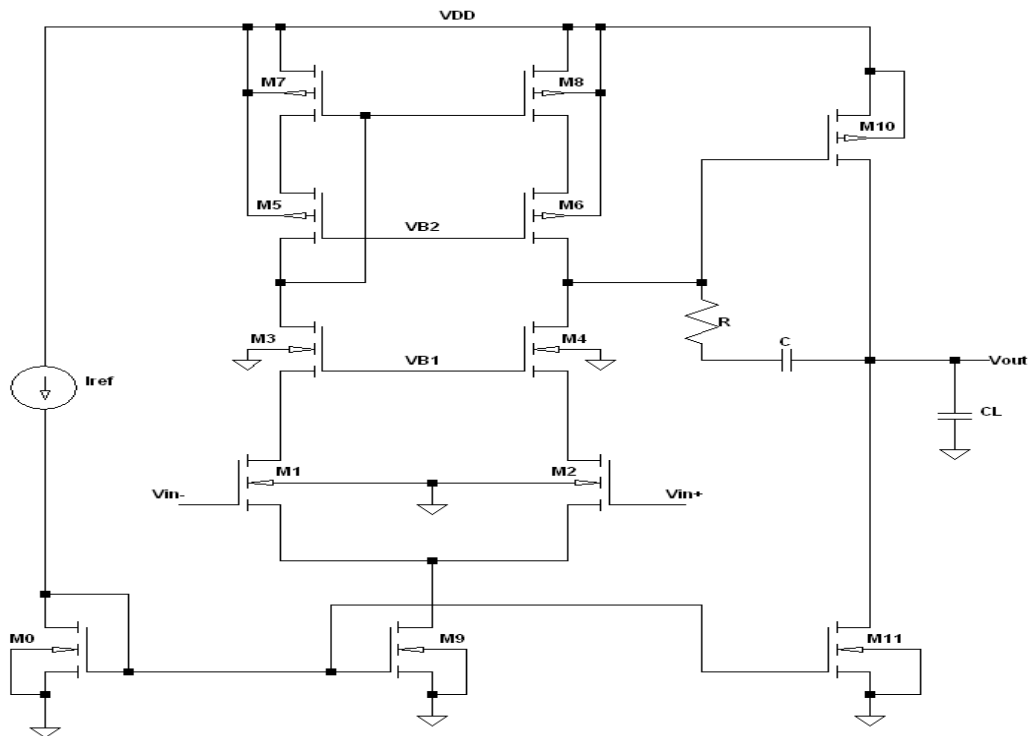


Figure 4.4: Telescopic OPAMP (X1 in Figure 2.5)

I_{ref} is the current flowing through MOSFET M0 with M0 and M9 implementing the current mirror structure. Due to cascading in first stage high gain can be achieved but it

causes low ICMR which is one of the drawbacks of the telescopic OPAMP. C_L is the load capacitance of OPAMP whose value can be determined from equation (4.12). While designing the OPAMP, sizes of input MOSFETs M1 and M2 should not be large otherwise it will contribute significant input parasitic capacitance C_p (shown in Figure 4.3) and will change the value of feedback factor β and hence the inter-stage gain. Figure 4.5 shows the simulation results of Telescopic OPAMP, shown in Figure 4.4. It shows the gain of 82.27 dB and UGB of 612.5 MHz with phase margin of 58.9 degree for load capacitance of 0.4pF (taking $C_s=C_f=0.1\text{pF}$). It has a settling time of 7.7ns.

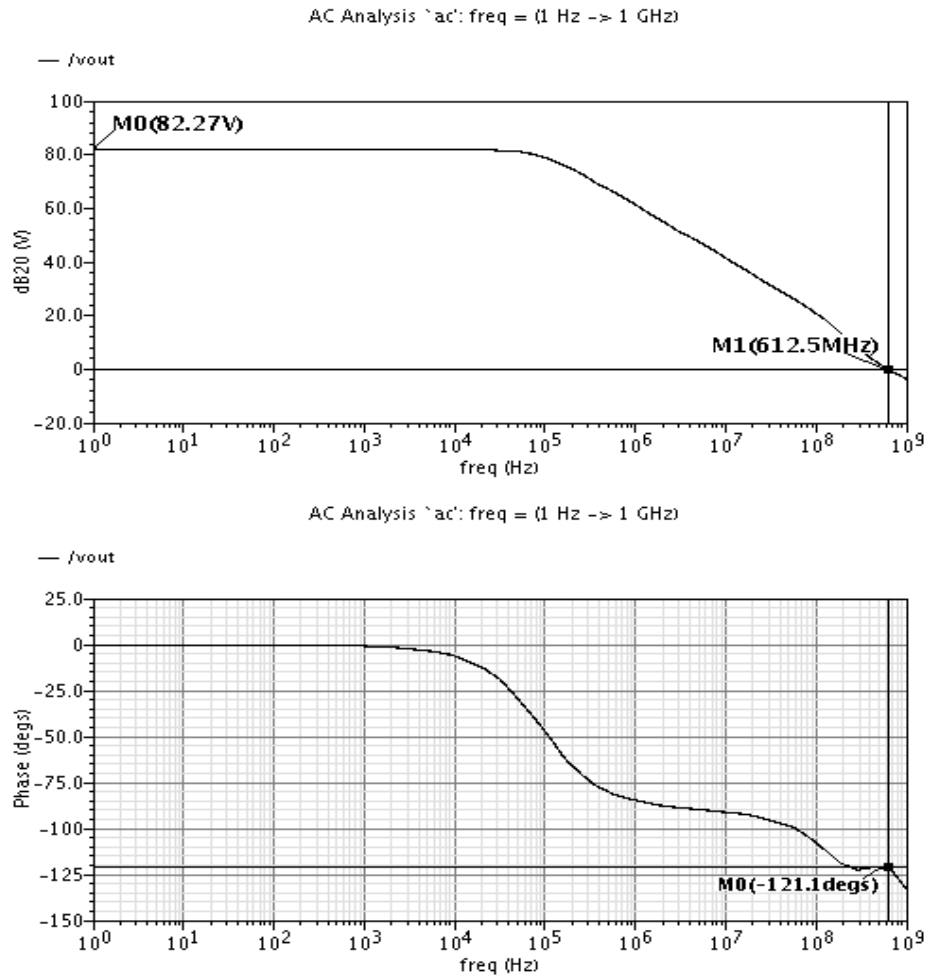


Figure 4.5: Simulation response of Telescopic OPAMP shown in Figure 4.4

Achieved results are summarized in Table number 4.1.

Table 4.1: Specifications of telescopic OPAMP

Specifications	Required	Achieved
Gain (A_0)	70dB	82.27dB
UGB	420 MHz	612.5 MHz
Phase Margin (PM)	60 degree	59 degree
Output Swing	High	0.3V-1.6V

As shown in Figure 2.5, ADC also requires another OPAMP X2 for S/H amplifier. It is used in unity gain feedback condition so it should have high UGB with high ICMR, PM of 55-60 degree and at least gain of 60 dB. Its circuit diagram is shown in Figure 4.6. M0-M2, M5 and M7 are NMOSs and M3-M4 and M5 are PMOSs. R and C make the compensating network to tune the phase margin. C_L is the load capacitance of the OPAMP which is mainly the gate capacitance of input MOSs of driving comparator comp1, input capacitance of M1 MOSFET of this OPAMP due to negative feedback and other parasitic capacitances present at output node of X2.

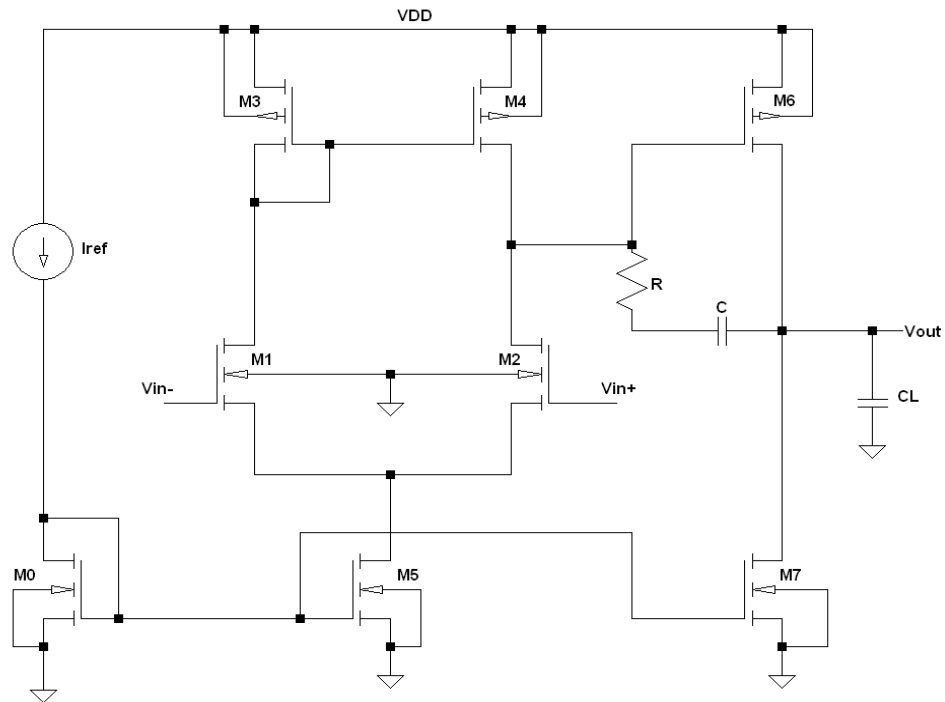


Figure 4.6: Simple two-stage OPAMP (X2 in Figure 2.5)

I_{ref} is the current flowing through MOSFET M0 with M0 and M5 implementing the current mirror structure. PMOSs M3 and M4 acts as a active load for input MOSFETs M1 and M2. First stage decides the ICMR so sizes of MOSFETs in this stage should be determined carefully to achieve high ICMR with high gain. Output swing is determined by output stage, it also require careful sizing of M6 and M7 in order to achieve high output swing at the output of OPAMP X2. Figure 4.7 shows the simulation results of simple two-stage OPAMP X2 (shown in Figure 2.5). It shows the gain of 63.3 dB and UGB of 431 MHz with phase margin of 54.9 degree for load capacitance of 0.3pF.

Simple two-stage OPAMP is chosen with the specifications given in the table number 4.2. Achieved results are also summarized in table number 4.2.

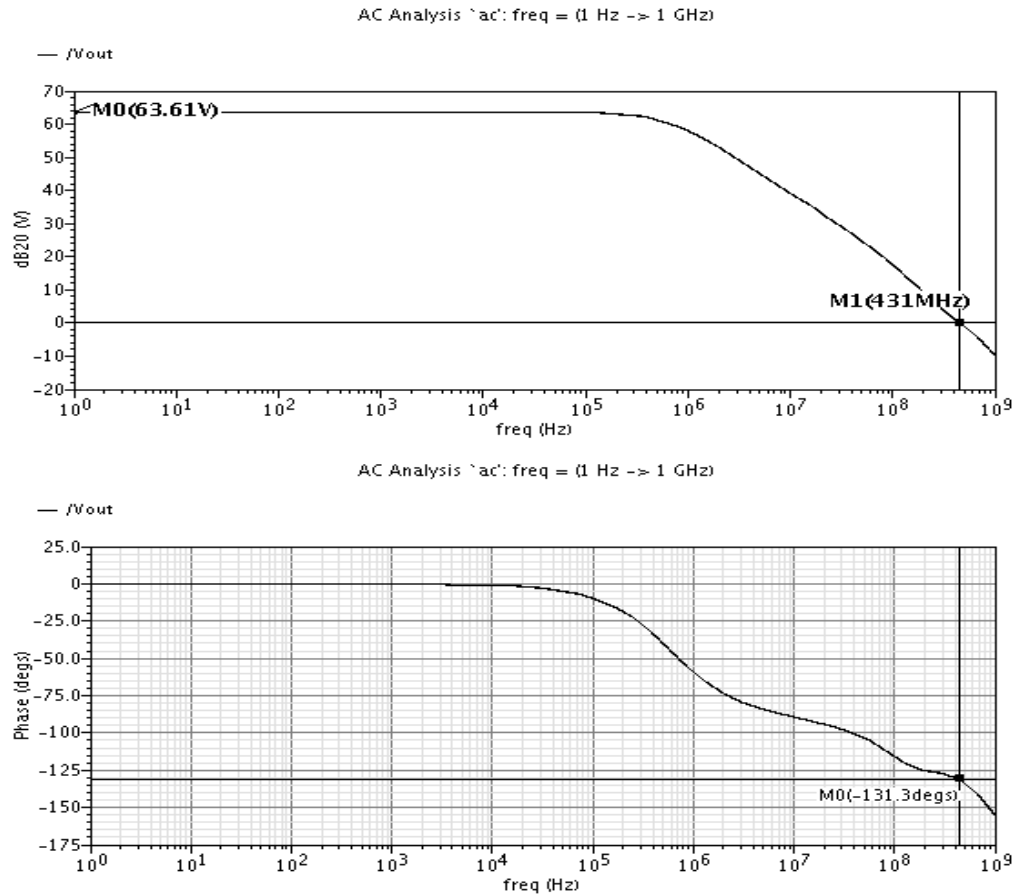


Figure 4.7: Simulation results of simple two-stage OPAMP shown in Figure 4.6

From both the Tables 4.1 and 4.2, it is clear that output swing of X1 is more than the ICMR of X2 so FS range of Pipelined ADC is decided by ICMR of OPAMP X2 used in S/H

Table 4.2: Specifications of simple two-stage OPAMP

Specifications	Required	Achieved
Gain (A_0)	60 dB	63.6 dB
UGB	420 MHz	431 MHz
Phase Margin (PM)	55-60 degree	54 degree
ICMR	High	0.6V-1.6V
Output Swing	High	0.2V-1.6V

configuration. Thus $V_{ref-} = 0.6v$ AND $V_{ref+}=1.6V$ with $FS = (V_{ref+} - V_{ref-}) = 1V$ is chosen.

Achieved phase margin is somewhat less than the required but since UGB is high it will settle to the required output voltage within the specified time. OPAMP X2 is used in unity gain configuration so gain should be high so that gain error is less and output equals the input.

4.1.3 Sub-ADC

Comparators form the core of all A/D converters, as they carry out the essential function of quantization. Hence, their characteristics, especially speed, offset, area and power consumption, affect the overall performance of the ADC. It is basically used to compare the input signal with a reference and generate a binary output. For applications in high-speed, high-resolution ADCs, the comparator needs to amplify a small difference between the input and the reference to a rail-to-rail swing in a very small amount of time.

The required high-gain can also be achieved with the help of positive feedback. This is done by using a latch with back-to-back connected inverters in positive feedback. As soon as clock goes high, the switch releases the latch to regenerate any imbalance seen by it. If an initial voltage difference, ΔV_0 , is applied at the beginning of the latch phase, the settling behavior of the latch can be described as [8]

$$\Delta V = \Delta V_0 \cdot e^{-\frac{(A-1)t}{\tau}} \quad (4.17)$$

where ΔV is the differential output voltage and A is the low frequency gain of each inverter.

The time constant τ can be written as

$$\tau = \frac{C_L}{GM} \quad (4.18)$$

Where GM is the transconductance of each inverter (i.e. $g_{m_n}+g_{m_p}$) and C_L is the load capacitance seen at the output.

The time required by the latch to generate a voltage difference ΔV_{logic} that can be recognized by the digital logic can be expressed as

$$T_{LATCH} = \tau \ln\left(\frac{\Delta V_{logic}}{\Delta V_0}\right) \quad (4.19)$$

Combining the equations (4.18) and (4.19), we get

$$T_{LATCH} = \frac{C_L}{GM} \ln\left(\frac{\Delta V_{logic}}{\Delta V_0}\right) \quad (4.20)$$

Another important aspect of comparators that has a significant impact on the ADC accuracy is input-referred offset. The offset of a comparator directly creates DNL errors and hence should be made as small as possible.

The offset voltage of comparator is require be smaller than $0.5*LSB=0.5*3.9mV=1.95mV$. The resolution of a comparator can be defined as

$$\Delta V_{min} = \frac{V_{max}-V_{min}}{A_v} \quad (4.21)$$

where A_v is the DC gain of comparator.

Once again, we require ΔV_{min} to be smaller than $0.5*LSB$. Thus, the minimum DC gain is

$$\begin{aligned} A_v &= \frac{V_{max}-V_{min}}{\Delta V_{min}} \\ &= (VDD-VSS)/0.5*LSB \\ &= (1.8-0)/1.95mV=923 \end{aligned}$$

Pulse width of Φ_1 is taken as 7ns so the response time of the comparator must be smaller than clock pulse width Φ_1 . This requires high speed comparators so positive feedback dynamic latch based comparator is chosen for this purpose. Response time of the comparator is taken as less than 5 ns as a design specification. Keeping sampling clock pulse width lesser allows remaining of clock to be used for OPAMP based operations. This way, it will relax OPAMP specifications as it will have more time to work with.

Before designing comparator it is desired to calculate the reference voltage V_{ref} . It is threshold voltage of comparator with the following

$$\begin{aligned} V_{in} < V_{ref}, & \quad V_{out} = 0V \\ V_{in} > V_{ref}, & \quad V_{out} = VDD. \end{aligned}$$

For $V_{in}=V_{ref}$, V_{out} equals to either 0V or VDD depends upon the offset of comparator.

V_{ref} is the mid voltage between the input voltage swings and given by

$$V_{ref} = \frac{(V_{ref+})+(V_{ref-})}{2} \quad (4.22)$$

In pipelined ADC, input signal V_{in} varies between V_{ref-} to V_{ref+} , also called FS range. From section 4.1.2, we have $V_{ref+} = 1.6V$ and $V_{ref-} = 0.6V$ thus $V_{ref} = 1.1V$. If these extreme values change, V_{ref} need to be calculated accordingly.

Architecture and Design

A high speed high gain and low offset comparator is required with low power dissipation. So, a dynamic comparator has been chosen to implement sub-ADC which has the above merits and is shown in Figure 4.8 [11].

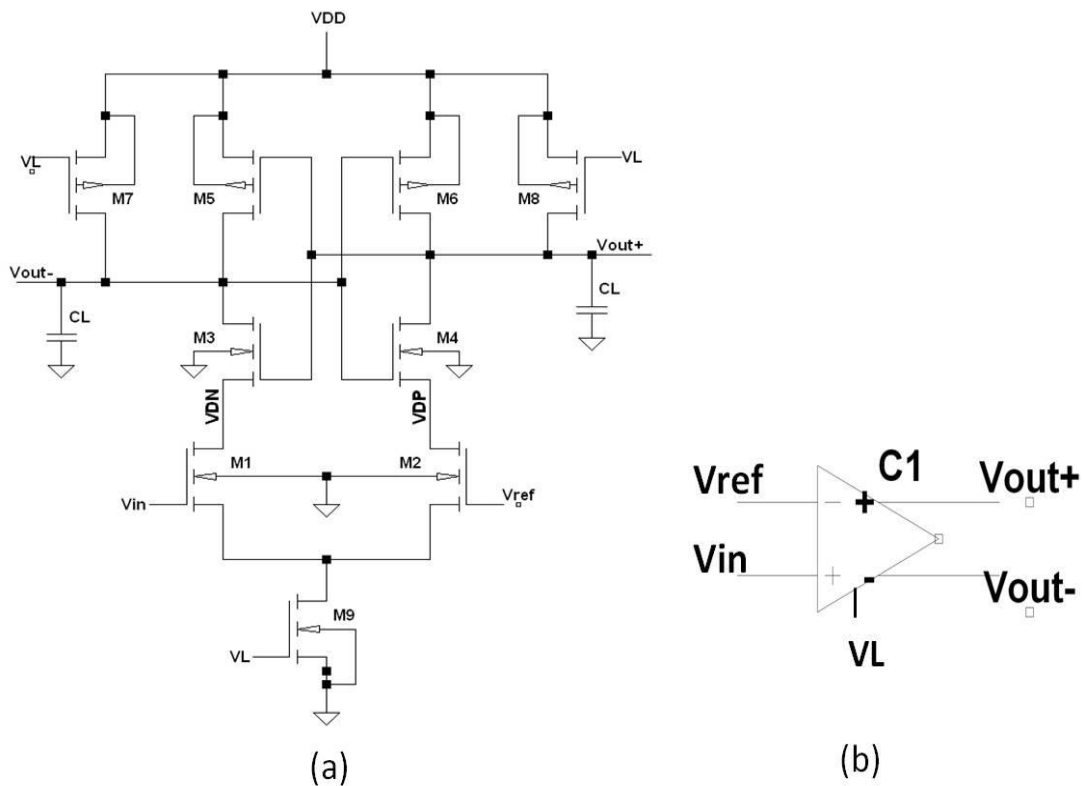


Figure 4.8: (a) Dynamic comparator (b) its symbol

The circuit is operated in two phases, one with reset or pre charge phase and an evaluation phase. During the first part of clock cycle, when clock VL is low (0V), the output

nodes of the cross-coupled inverters (M3-M6) are reset to VDD, using the reset PMOS transistors M7 and M8. This is called pre-charge phase since output is pre-charged to VDD. The second part of clock cycle is the actual sense and evaluation phase. When the clock signal goes high, reset transistors are switched OFF and the tail transistor (M9) of the differential pair (M1, M2) is turned on. VDN and VDP decrease because the parasitic capacitances at these nodes are discharged by the current flowing in M1/M2. When VDN/VDP become smaller than $V_{DD}-V_{tn}$, transistors M3/M4 turn ON and their drain current start discharging the parasitic capacitances C_L of the output nodes. Then both output voltages decrease.

Let us assume input voltage V_{in} is larger than reference voltage V_{ref} . In this case, the drain current of M3 is larger than the one flowing in M4, thus decreasing V_{out-} faster than V_{out+} . This, in turn, it makes the V_{gs} of M3 increase faster than V_{gs} of M4 transistor, which further enlarges the difference between the currents in these transistors and there is a positive feedback mechanism. When V_{out-} becomes lower than $V_{DD}-V_{tn}$ transistor M6 turns ON as $V_{gs6} \geq V_{tp}$ (threshold voltage of PMOS transistor) and accelerating the regeneration process and making V_{out+} return to VDD.

Simultaneously, V_{sg5} becomes less than threshold voltage of M5 transistor, turning it OFF. Thus, after regeneration is completed, V_{out+} is at VDD and V_{out-} is at 0V. In this situation, there is no supply current flowing which reduces the power dissipation.

The transistors should be sized to minimize the regeneration time (time output voltages take to reach the digital levels). It is given by equation (4.20), from it is observed that:

- a) Increasing the length of transistors decrease their transconductance (g_m) and enlarges their C_{gs} . Thus, all devices should have minimum length.
- b) For a given current, the g_m is proportional to $(W)^{1/2}$.
- c) Parasitic capacitances of transistor are proportional to width of transistors.

According to [11], having width ratio of PMOS/NMOS one in inverter gives best regeneration. Therefore, the PMOS: NMOS ratio is smaller than normal inverter PMOS: NMOS ratio. In cross-coupled comparator both NMOS and PMOS provide positive feedback. It should be noted that if loading capacitance is larger, increasing the size of NMOS will increase the g_m so regeneration is faster but if loading capacitance is small than

that of gate capacitance of inverter then it dominates. So, increasing the width of NMOS does not help much as load capacitance also increases. Next stage of comparator is 2-input MUX which offer less loading capacitance to comparator. Thus, for a certain load capacitor, T_{LATCH} can be minimized by properly choosing the sizes of transistors. Another way to increase the speed (or decreasing the regeneration time) is to increase the current and thus increase the width of M9. Thus, there is a tradeoff between power and speed.

Power consumption is a big issue in today's applications. To reduce the power consumption, load capacitance and current must be minimized. Assuming that load capacitance is already minimized by proper sizing and careful layout, the current can only be reduced by minimizing tail current transistor M9. As current has direct relationship with speed, there is tradeoff between power consumption and speed. Fortunately, power consumption of a clocked comparator is typically much less than normal OPAMP based comparator because positive feedback saturates the back-to-back inverters and shuts off the current when evaluation is finished.

During $V_L='0'$, both the output of dynamic comparator V_{out+}/V_{out-} are VDD called reset or pre-charge phase so a latch is required at the output of dynamic comparator to hold the previous state in this phase. NAND SR latch is used here at the output of dynamic comparator, generating C1P signal as shown below in Figure 4.9.

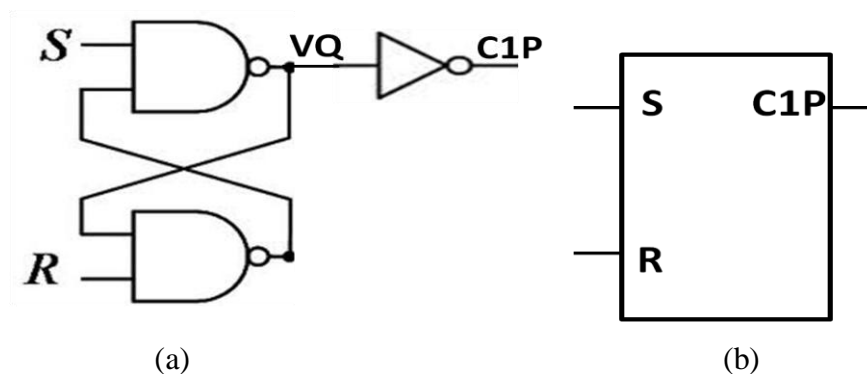


Figure 4.9: (a) S-R Latch (b) its symbol

Due to positive feedback, dynamic comparator has very high gain. The output quickly settles either to VDD or VSS so it has very less delay. From simulations in Spectre, the total delay of dynamic comparator with latch (measured from 50% rise of VL to 50% of C1P) is achieved to be equal to 3.6ns which is less than Φ_1 clock pulse width. It is observed from

simulations that systematic offset of dynamic comparator is $73 \mu\text{V}$ which is very less than 1LSB ($=3.9\text{mV}$).

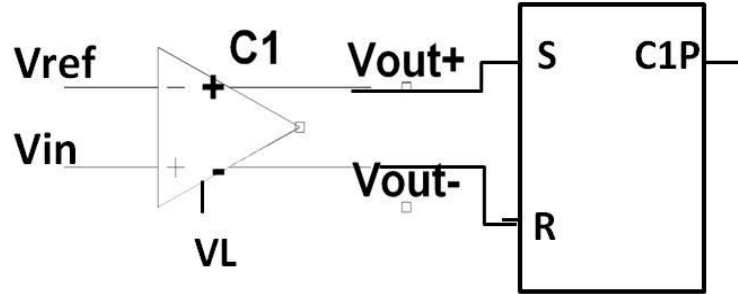


Figure 4.10: Internal blocks of comparator comp1 (shown in Figure 2.5)

From simulations, it is observed that peak current flowing through M9 when VL is high, is $150\mu\text{A}$ so peak instantaneous power dissipation ($P = VI$) is $0.27\mu\text{W}$ which is reasonable in high speed operations.

It should be noted that VL shown in Figure 4.8 and 4.10 is connected to sampling phase clock Φ_1 at the top level. NOR based SR latch can also be used in place of NAND based SR latch but later has higher speed at lesser area so NAND based SR latch is used here. Inverter at the output of latch is designed as symmetric inverter so as to have equal rise and fall times. Symmetric VTC (voltage transfer characteristic) is obtained for width ratio of PMOS: NOMOS of $1.14 \mu\text{m}:0.24 \mu\text{m}$ for $L=0.18 \mu\text{m}$ with the help of simulations.

Operation of comparator with latch (shown in Figure 4.10) is summarized in the Table 4.3. For $VL=1$, when $V_{in} < V_{ref}$, $V_{out+} = 0$ and $V_{out-} = 1$ and when $V_{in} > V_{ref}$, $V_{out+} = 1$ and $V_{out-} = 0$. When $VL=0$, it is pre-charge phase and $V_{out+} = V_{out-} = 1$. In this case SR latch hold the previous value at VQ node (as shown in Figure 4.9) and C1P is inverted value of VQ. Inverter is used at the output of latch so that for $V_{in} < V_{ref}$, output of comparator, comp1 is 0 and $V_{in} > V_{ref}$ we have 1 at the output of comp1. Without it, we will have inverted outputs. Top row of table is not defined since both V_{out+} and V_{out-} can not be 0 at the same time. For $V_{in} = V_{ref}$, output voltage of comparator is decided by the offset of comparator. From simulations, it is found that output (V_{out+}) changes from 0V to VDD for V_{in} greater than V_{ref} by $73 \mu\text{V}$. Since it is less than 1 LSB, it will not impact the performance of whole ADC.

Table 4.3: Operation of comparator with latch

VL	V _{in}	V _{out+}	V _{out-}	C1P
-	-	0	0	-
1	<V _{ref}	0	1	0
1	>V _{ref}	1	0	1
0	X	1	1	Inversion of previous value stored in SR latch

Simulations results of comparator with latch:

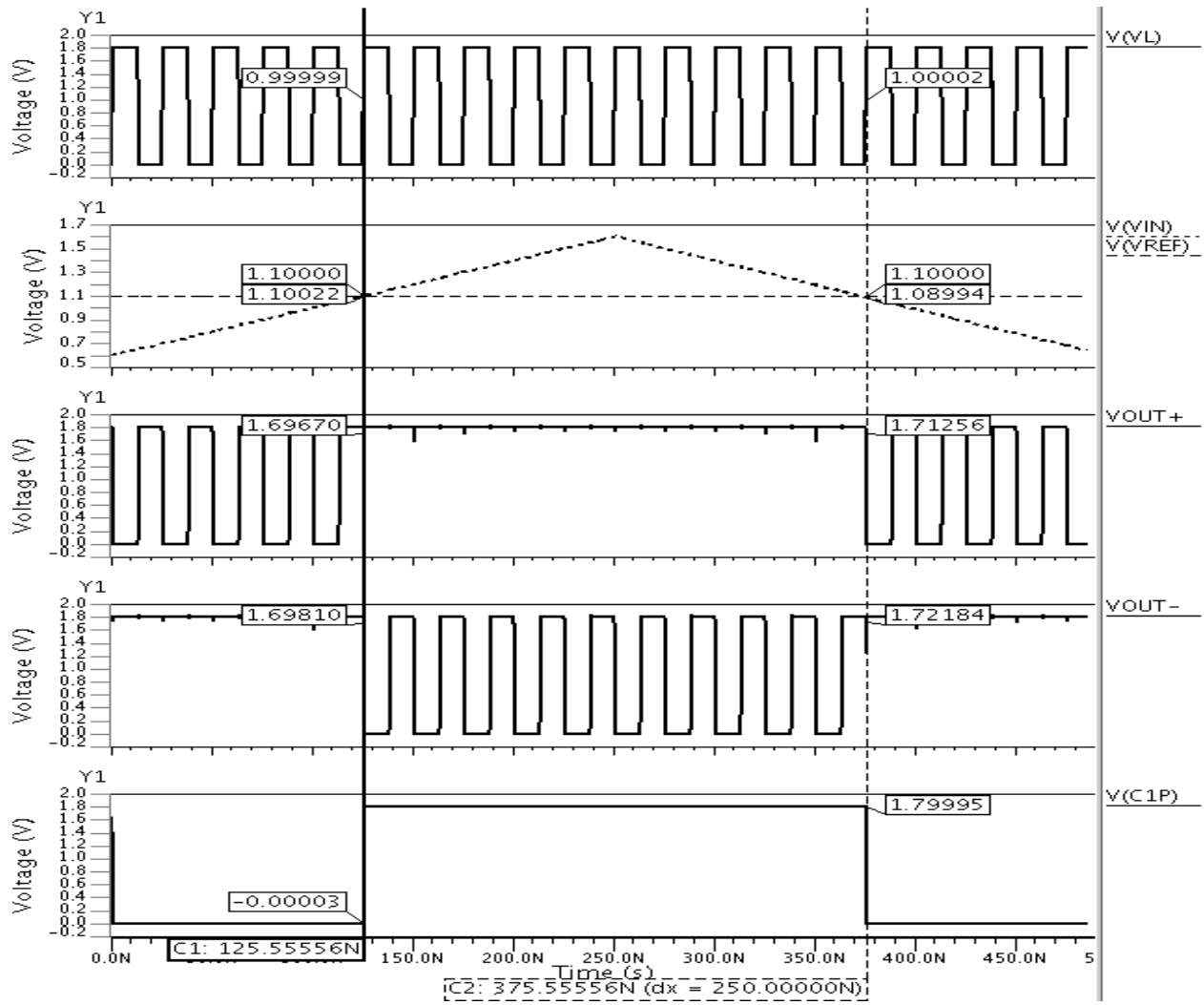


Figure 4.11: Simulation results of Comparator with latch

Figure 4.11 shows the simulations results of comparator comp1 of Figure 4.10. VL is the clock Φ_1 , V_{ref} is equal to 1.1V as calculated from equation 4.22. V_{in} is here given ramp so that input is considered as discrete values. Figure 4.11 shows the proper functioning of dynamic comparator with latch (comp1) with output of dynamic comparator V_{out+} / V_{out-} is VDD (1.8V) when VL = 0V. For $V_{in} < V_{ref}$, C1P = '0' and for $V_{in} > V_{ref}$, C1P = '1'.

4.1.4 MOSFET as Switch

Switch is generally implemented using MOS technology by one MOS (NMOS or PMOS) transistor or a pair of complementary transistors (CMOS).

A small switch resistance is required so that RC offered by switch is small and it quickly charge/discharge the output. Here, R is the switch resistance and C is the load capacitor. On-Resistance R of MOS is variable depending on the region it is working. Speed is generally measured by the time output takes to reach within a certain band of final output value. This error band is mostly 0.1% of final value in ADCs [12]. Thus, speed consideration is accompanied by accuracy specification. Figure 4.12 is showing this point, output reaches 0.1% ($\Delta V=0.1\%$) of final value after t_s time after which V_{ds} of NMOS switch is assumed to be zero and it is in linear region.

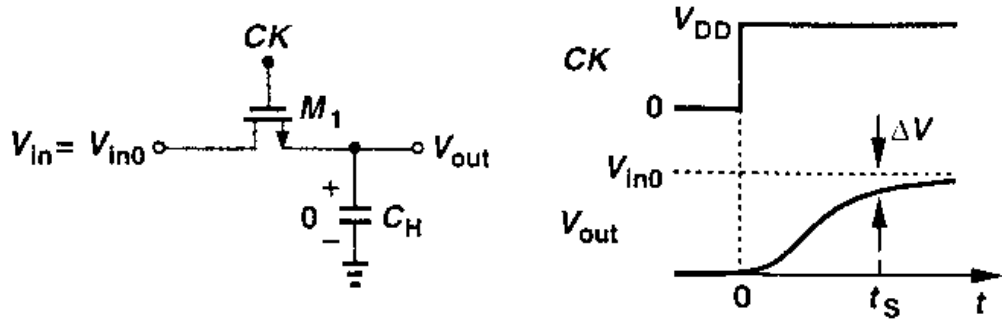


Figure 4.12: Speed consideration of a sampling circuit [12]

On-resistance of NMOS is given by

$$R_{on} = \frac{1}{\mu_n C_{ox} \frac{W}{L} (V_{DD} - V_{in} - V_{tn})} \quad (4.23)$$

where μ_n is the electron mobility, C_{ox} is the oxide capacitance, V_{tn} is the threshold voltage of NMOS.

Thus, on-resistance can be decreased by increasing the W/L ratio but care must be taken while increasing the size of MOS switch as it also increase the diffusion capacitor which increases the load capacitor and also increases the loading on the clock generator circuit and circuits connected to the gate.

It is clear that on-resistance depends upon input signal level, V_{in} , giving a larger RC for more positive inputs (for NMOS) and less positive inputs (for PMOS). Thus, using both MOSFETs in parallel reduces the dependency of on-resistance of switch on input signal. It is called CMOS switch but such a combination require complementary clocks at the gates as shown in Figure 4.13.

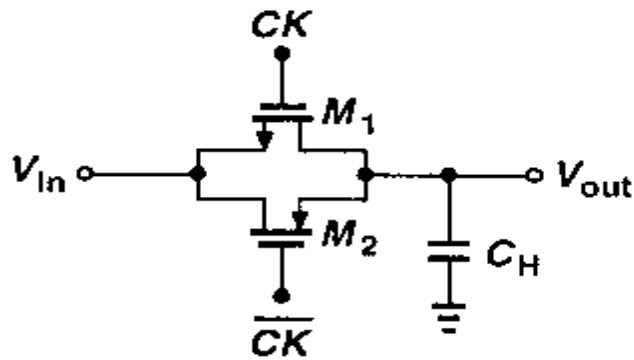


Figure 4.13: CMOS transmission gate switch [12]

M1 is NMOS and M2 is PMOS with their bodies connected to VSS and VDD respectively. This will raise the threshold voltage of MOS transistor due to body effect. It should be noted here that in order to remove the body effect, body of MOSFETs cannot be connected to source as source and drain junctions are interchangeable.

Also in high speed designs, delay between CK and \overline{CK} should be as small as possible so that both switches turn off simultaneously. Otherwise output will keep sampling the input for this remaining turn-on time with large input dependent RC and we will get distortions in the output. So generating \overline{CK} from CK can be critical in some cases [12].

One of the major problems coming from the use of CMOS switches is the so-called

charge injection (and clock feedthrough). These are discussed below.

Charge Injection:

When MOS is ON i.e $V_{gs} \geq V_t$ and it is in linear region, total charge in the channel is given by

$$Q_{ch} = W \cdot L_{eff} \cdot C_{ox} \cdot (V_{gs} - V_t) \tag{4.24}$$

$$Q_{ch} = W \cdot L_{eff} \cdot C_{ox} \cdot (VDD - V_{in} - V_t) \tag{4.25}$$

Where V_t is the threshold voltage of MOS transistor and L_{eff} is effective channel length.

When MOSFET turns OFF, Q_{ch} exits through source and drain terminals; this phenomenon is called Charge Injection. This is shown in figure 4.14 (a).

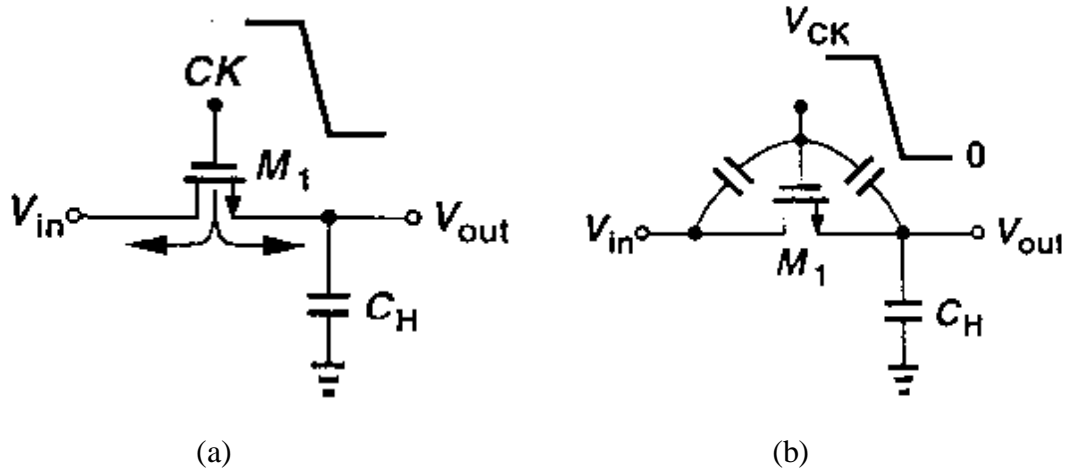


Figure 4.14: (a) Charge Injection (b) Clock Feedthrough [12]

Charge injected to the left is absorbed by source but charge injected to the right is deposited on C_H changing the values of sampled signal. As a worst case estimate, we can assume whole of the channel charge is injected on C_H , changing the output voltage V_{out} by

$$\begin{aligned} V_{out} &= V_{in} - \frac{Q_{ch}}{C_H} \\ &= V_{in} - \frac{W \cdot L_{eff} \cdot C_{ox} \cdot (VDD - V_{in} - V_t)}{C_H} \end{aligned} \tag{4.26}$$

Clock Feedthrough:

In addition to the charge injection, we have to remember the charge in the overlap

capacitance. This charge is given by

$$Q_{ov} = W \cdot DL \cdot C_{ox} \cdot V_{gs} \quad (4.27)$$

where DL is the overlap length of gate over source/drain diffusions in MOSFET. Due to this overlap capacitance clock transition is coupled to V_{out} , changing the V_{out} value. This is shown in Figure 4.10 (b). Note that both Charge Injection and Clock Feedthrough are dependent upon the sizes of MOS switches. If we increase the sizes to reduce the RC Of switch, we also increase the above effects. So sizes must be taken carefully.

The injection of charge and the one called Clock Feedthrough can result in a considerable error. This is particularly problematic for high resolution data converters where the accuracy required is high.

For 1V signal swing and 8 bits of resolution, the quantization step is as low as 3.9 mV. It is therefore necessary to reduce the charge injection drastically. Unfortunately, it is quite difficult to fully cancel this source of error. The commonly used techniques are based on compensation strategies which are only capable of alleviating the problem. The most popular methods can be classified as:

- use of dummy switch
- use of CMOS transmission gate switch
- use of fully differential solutions

Use of CMOS switches to reduce the charge injection effects is most commonly used method as it offers the low RC and wide signal swing but at the cost of increase in area to implement the opposite phase clocks.

Simulator is mainly used to get the proper sizes of PMOS and NMOS switches. But this cancelation occurs only for one input level as it is clear from below equation.

$$\Delta q_1 = \Delta q_2$$

$$W_1 \cdot L_1 \cdot C_{ox} \cdot (CK - V_{in} - V_{tn}) = W_2 \cdot L_2 \cdot C_{ox} \cdot (V_{in} - V_{tp}) \quad (4.28)$$

where V_{tn} and V_{tp} is threshold voltage of NMOS and PMOS respectively. Note this way of reducing the charge injection does not provide complete cancelation against Clock

Feedthrough since CGDO/CGSO of NMOS and PMOS are not equal [12].

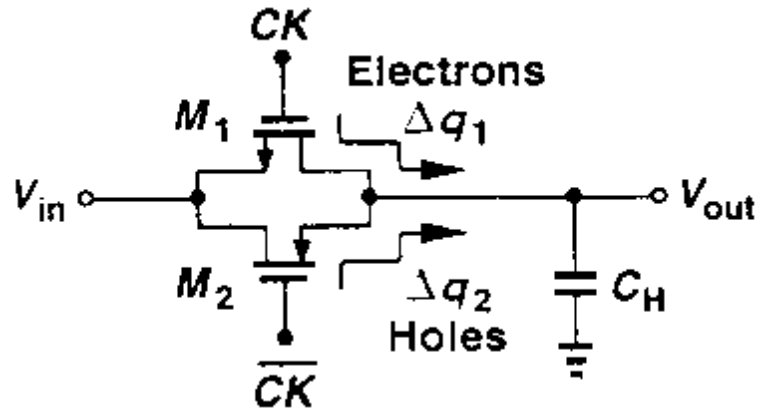


Figure 4.15: Use of CMOS switch to reduce charge injection [12]

Figure 4.16 shows how the fully differential technique can be used to compensate charge injection. The switching off of the two reset transistors across capacitors produce an injection of charge in the two op-amp inputs. However, this injection corresponds to a common mode signal that is rejected by the circuit operation. Clock coupling is then cancelled within the limits of the matching accuracy between the two processing paths.

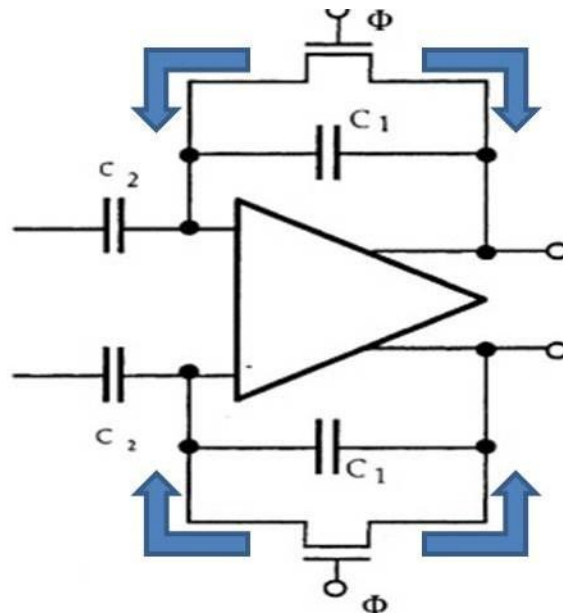


Figure 4.16: Use of differential technique to reduce charge injection [12]

Care must also be taken while drawing the layout of MOS switches. Proper care must be taken to protect the critical nodes from charge coupling from the nearby transition nodes. Shielding is needed to protect the nodes. Constant voltage lines can be used as a shield in between the critical nodes and high transition metal lines and maintains somewhat larger distance in between these lines wherever shielding is not possible.

4.1.5 2-Input Multiplexer

The block of a 2-input multiplexer (MUX2) shown in Figure 2.5. It is used to pass one value from either V_{ref-} or V_{ref+} depending upon C1P. If C1P='0' then $V_{dac}=V_{ref-}$ and $V_{dac}=V_{ref+}$ otherwise. Its circuit diagram is shown in Figure 4.17.

CMOS transmission gates are used to implement MUX2. As we know, CMOS transmission gate is a good passer of both logic '1' and logic '0'. Also, it offers less resistance hence it has been used to implement MUX2. Proper size of transistors should be used so that we have less RC and at the same time less gate parasitic capacitance and diffusion capacitances.

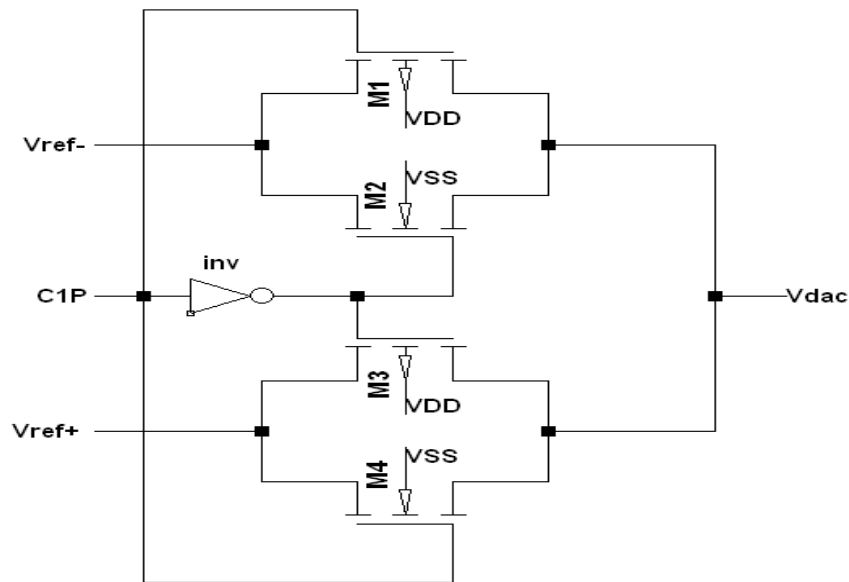


Figure 4.17: 2-input MUX implementation

M1, M3 are PMOS transistors and M2, M4 are NMOS transistors. When C1P = 0, M1 and M2 are ON, $V_{dac} = V_{ref-}$ and when C1P=1, M3 and M4 are ON and $V_{dac} = V_{ref+}$. Inverter *inv* is the symmetric inverter with equal rise and fall time.

4.2 Cascading 1-bit Pipelined ADC Stages

After 1-bit stage we cascade them to build the whole ADC as shown in Figure 2.1, output of 1st stage act as input to 2nd stage and so on (except last stage) as shown in Figure 4.18 the cascading of two 1-bit stages with left one in Φ_2 and another one in Φ_1 phase.

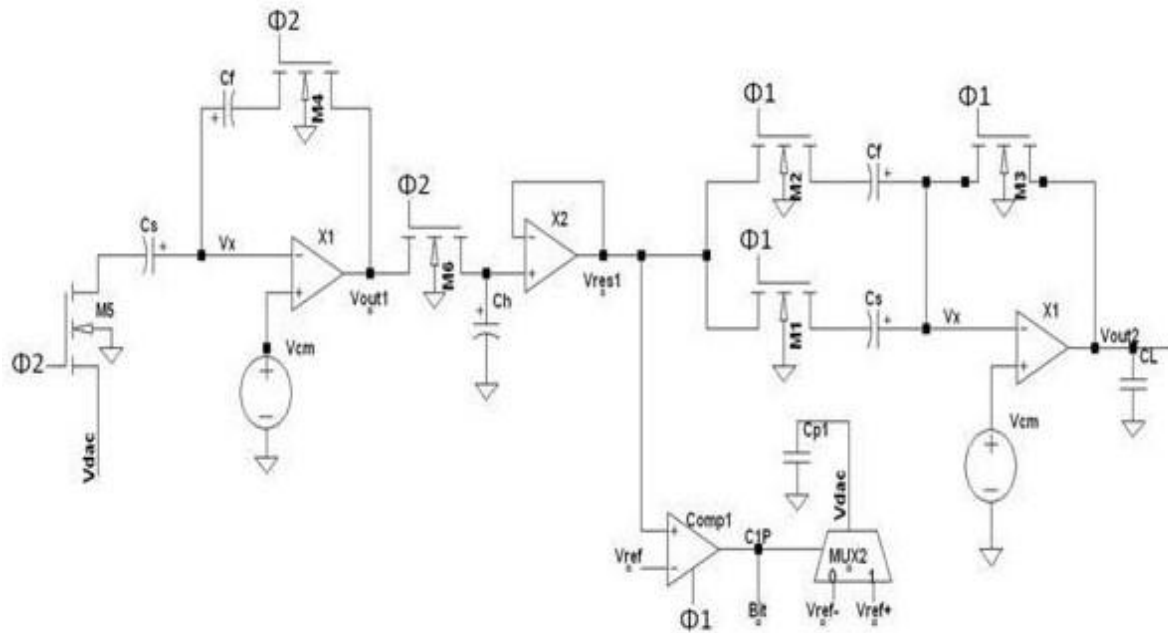


Figure 4.18: Cascading two 1-bit stages

Output voltage of X1 is stored in C_h in Φ_2 phase and is used as input for next stage in Φ_1 phase. It must be noted that sample and hold amplifier is used here to stabilize the output V_{out1} and hence the input of next stage. If Sample and Hold amplifier (M6, Ch and X2) is not used, then the output of OPAMP X1 will decrease as NMOS in the output stage of OPAMP X1 is always ON, decreasing the output node. Therefore, it is necessary to stabilize the output of MDAC.

Accuracy and speed of whole ADC depends upon the accuracy of X1 and X2 OPAMP, so they must be designed carefully. Simple two stage OPAMP with NMOS as input stage is used in X2. It also should have high UGB with 55-60 degree PM so that output quickly settles to the required value. From simulations in Spectre, it is found that the linear output swing of X1 as 0.2V-1.6V and ICMR of X2 as 0.6V to 1.6V. The worst case signal swing is ICMR of X2 which decides the FS range and hence V_{ref-} and V_{ref+} values.

4.3 Last 1-bit Pipelined ADC Stage

Looking back in Figure 2.1, we note that last 8th stage does not require MDAC, it only requires comparator (comp1) to generate the last bit which is then passed to delay logic. Its block diagram is shown in Figure 4.10 with V_{in} connected to the output of 7th stage i.e V_{res7} and C1P generated is the last 8th bit.

4.4 Delay Element

From Figure 2.1, the purpose of using delay element is to arrange the delay to save the 8 digital code output set for the same sampled signal [3]. The delay element is constructed by the D-type flip flops (DFF). Figure 4.19 shows the circuit structure of the whole 8-stage register arrays. Negative edge triggered D Flip-Flop is used here whose circuit diagram is shown in Figure 4.20. Since comparator is generating the output at the rising clock of Φ_1 , negative edge triggered flip-flop is used in the delay element so that it stores the right value.

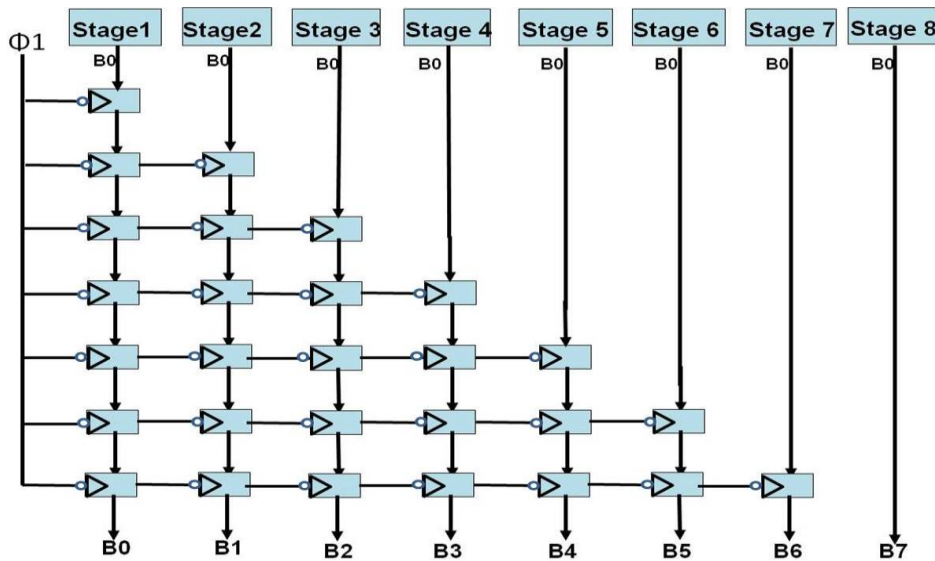


Figure 4.19: Delay element

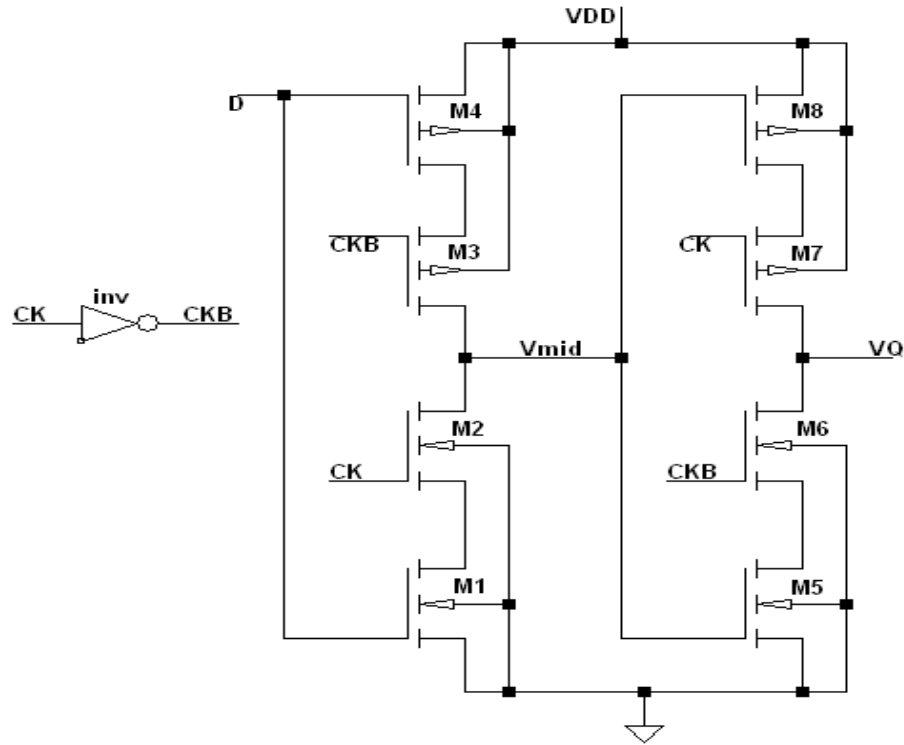


Figure 4.20: Master-Slave type D flip-flop

Figure 4.20 shows the Master-Slave type D flip-flop with master consists of MOSFETs M1-M4 and slave consists of MOSFETs M5-M8. Output of comp1 (C1P) is connected to D input of D flip-flop and Φ_1 is connected to CK. During Φ_1 (i.e. CK=1) is high, M1-M4 are ON, master is transparent to input and output of comp1 (C1P) get stored in V_{mid} as shown in Figure 4.20. When Φ_1 changes from high to low, M5-M8 are ON but M1-M4 are OFF so master is opaque but slave is transparent and stored value at V_{mid} is available at the output of flip-flop, V_Q . Inverter (inv in Figure 4.20) is the symmetric inverter with the dimensions as already discussed. It is used to generate the invert of clock for proper functioning of D flip-flop.

Table 4.4 shows the results from simulation of cascading pipelined stages for different applied inputs. $V_{ref^-} = 0.6V$, $V_{ref^+} = 1.6V$ and $1LSB = 3.9mV$. Here V_{res} (ideal) is given by equation 2.4 and residue voltage (V_{res}) of previous stage works as an input for next stage. Results are measured at 50 % of Φ_2 during its fall from high to low.

Table 4.4: Simulation results of various stages in pipelined ADC

V_{in} (V)	V_{res1} (V)		V_{res2} (V)		V_{res3} (V)		V_{res4} (V)	
	Ideal	Obtained	Ideal	Obtained	Ideal	Obtained	Ideal	Obtained
0.6	0.6	0.59893	0.6	0.59812	0.6	0.59798	0.6	0.59791
0.8	1	0.99934	1.4	1.4002	1.2	1.19141	0.8	0.775
1.0	1.4	1.39850	1.2	1.1981	0.8	0.79327	1	1.00612
1.2	0.8	0.79977	1.0	1.0016	1.4	1.3998	1.2	1.1908
1.4	1.2	1.1995	0.8	0.79886	1	0.99607	1.4	1.39451
1.6	1.6	1.5992	1.6	1.5986	1.6	1.5985	1.6	1.5978

From Table 4.4, it is clear that obtained results (ideal-obtained) are within 1/2LSB for some of inputs. For certain inputs residue is becoming more than 1 LSB e.g V_{res4} for $V_{in} = 0.8V$. Required residue voltage V_{res4} is 0.8V for $V_{in} = 0.8V$ but 0.775V is obtained at the output which is more than 1 LSB. Upto stage 2 residue voltage is within margin of 1/2 LSB but after stage 2, it increase and go beyond 1 LSB for some of inputs as shown in Table 4.4 which results in wrong bits at the output. From simulations it has been seen that for $V_{in} = 0.6V$ and $1.6V$ all the 8 bits of pipelined ADC are giving correct results with all 0s and all 1s respectively.

Chapter 5

Layouts

This chapter describes the layout designs of various blocks in pipelined ADC whose circuit diagram is shown in chapter 4. UMC 0.18 μm CMOS technology with 1P6M process technology file is used in drawing all the layouts. CAD tool used in the layout is Virtuoso layout editor from Cadence and Assura verification tool is used for DRC/LVS and Assura XRC for parasitic extractions. Layout of various building blocks of 1-bit pipelined ADC stage are shown here.

5.1 CMOS Switch

Layout of MOSFET switch used in pipelined ADC is shown in Figure 5.1. Its circuit diagram is shown in Figure 4.15. It is CMOS based transmission gate switch with inverter to generate the control signals for NMOS and PMOS.

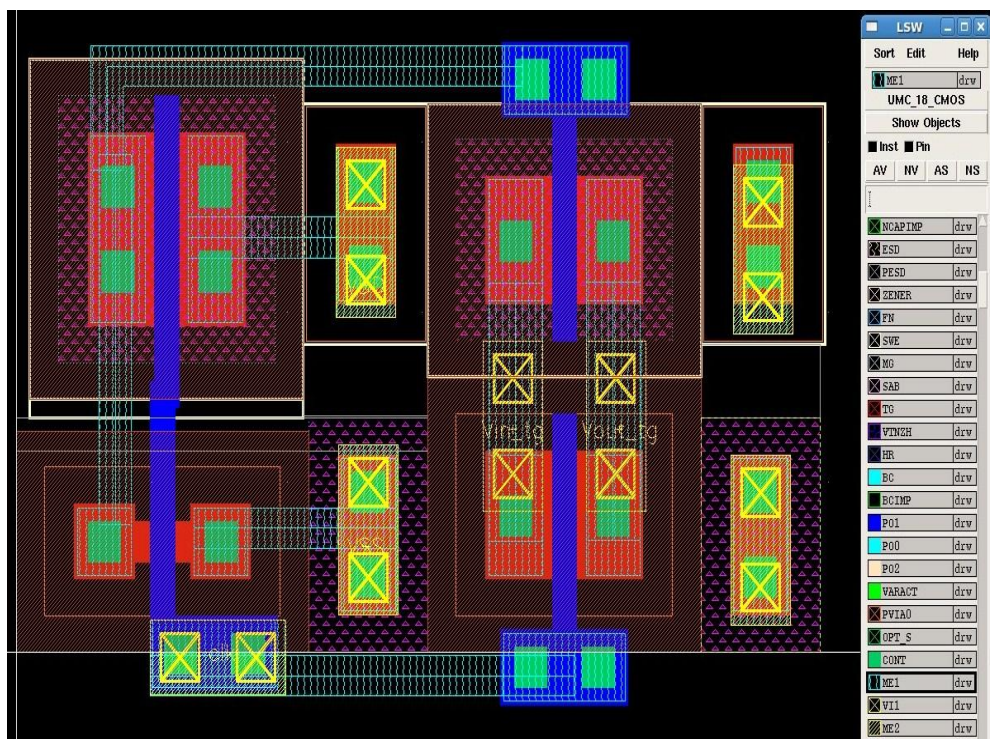


Figure 5.1: Layout of CMOS based switch

A switch is critical element in analog circuit designs as it is controlled by digital clock and used to transfer analog signal from one node to another. This kind of operation: analog function with digital control is on the border between analog world and digital world and can become a source of undesired coupling that should be avoided. These points should be kept in mind while drawing the layout of MOSFET base switch. In the Figure 5.1 analog world is surrounded by substrate and well contacts to suppress the noise that may come from digital world. Possible noise is intercepted by the substrate and well and driven toward low impedance point that biases the substrate and the well.

5.2 Dynamic Comparator with Latch

Layout of dynamic comparator with SR latch and inverter used in pipelined ADC is shown in Figure 5.2. Circuit diagram of dynamic comparator is shown in Figure 4.8 and Figure 4.10 shows the block diagram of dynamic comparator with SR latch and inverter.

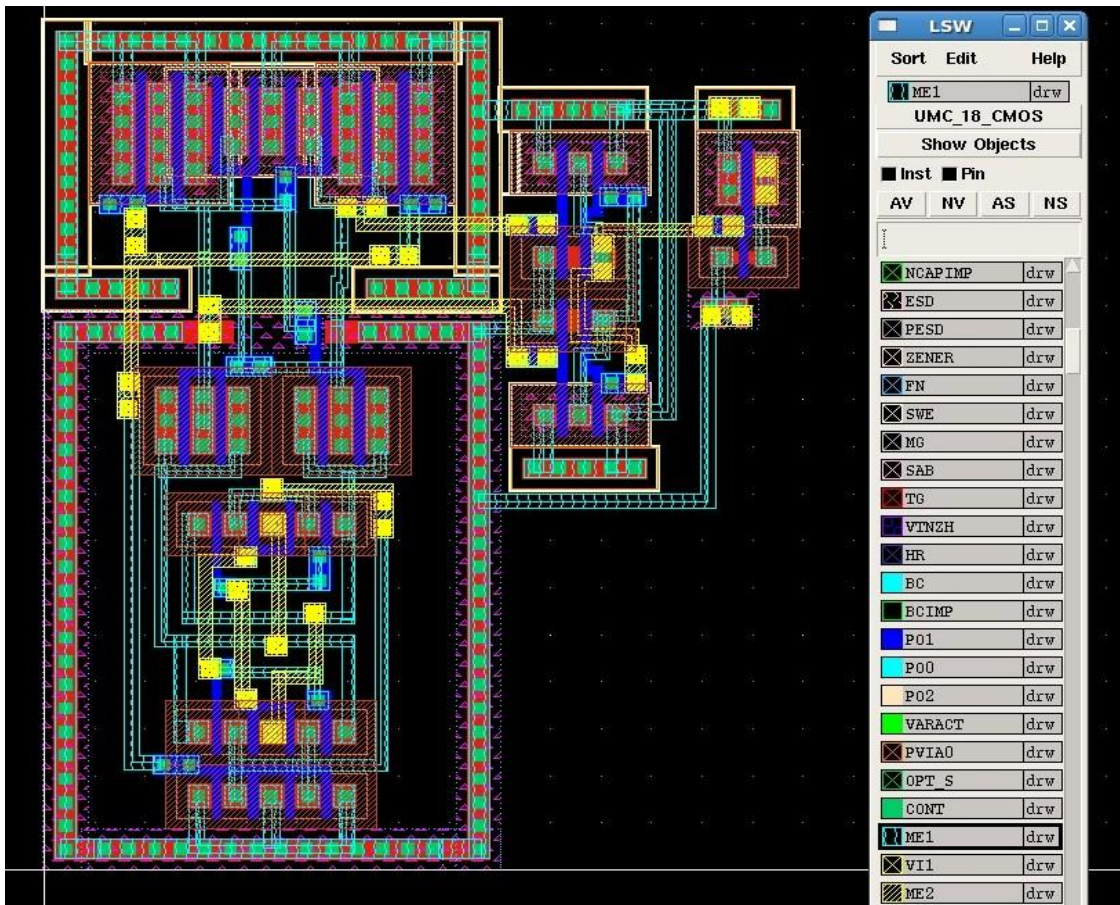


Figure 5.2: Layout of dynamic comparator with latch

Various layout design techniques are used in order to take care of process variation which is very essential for proper operation of dynamic comparator like common-centroid technique and inter-digitization. Figure 4.10 shows M1 and M2 as the input transistors which contribute the offset at the output due to process variation. So common centroid technique with inter digitization is applied to them. It also reduces the area and parasitic capacitance at various nodes. In the layout we have one part of M1 on one side and one part of M2 on other side. This compensates the boundary-dependent etching effect at the two endings.

Due to positive feedback in dynamic comparator, it has a very gain so it becomes very susceptible to noise that can cause a wrong functioning. In order to take care of this guard rings are used to around the NMOS and PMOS transistors. N-well guard ring is placed around the PMOS transistors and connected to highest positive supply voltage VDD and substrate contacts connected to VSS are placed around the NMOS transistors.

5.3 2-Input Multiplexer

Layout of 2-input Multiplexer used in pipelined ADC is shown in Figure 5.4. Its circuit diagram is shown in Figure 4.17.

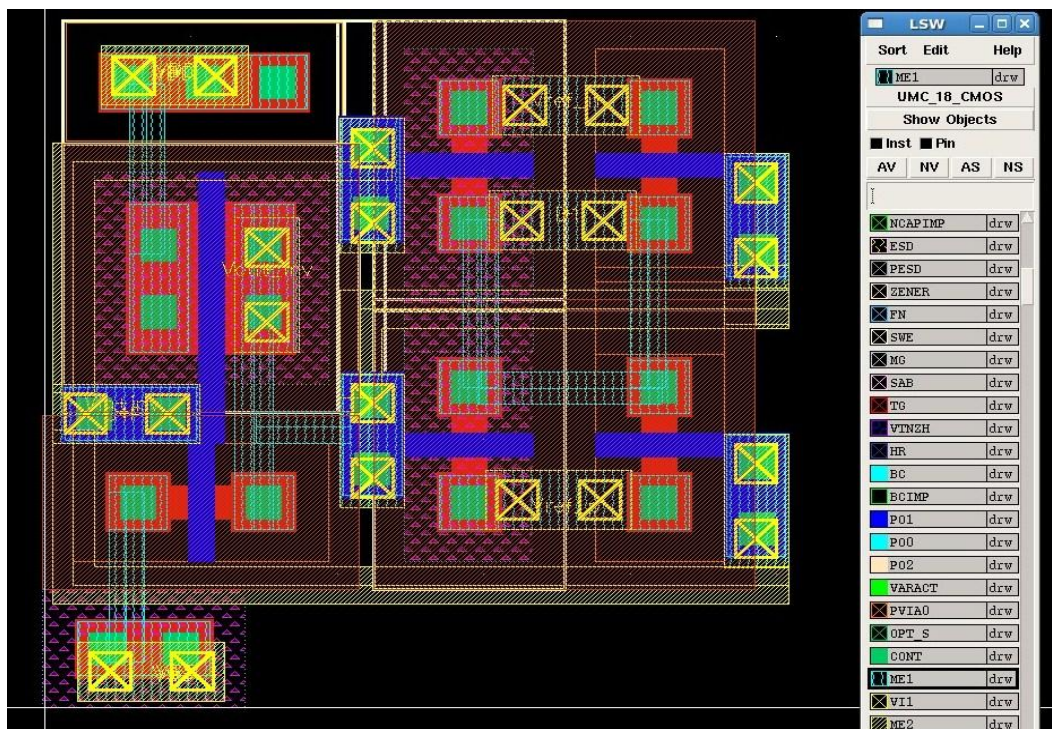


Figure 5.3: Layout of 2-input multiplexer

Layout of inverter is also shown in Figure 5.3 at the left side to generate the control signals of MOSFETs at the right side. N-well and substrate contacts are also shown in Figure 5.3 at the top and bottom of inverter.

5.4 Telescopic OPAMP

Layout of Telescopic OPAMP used in pipelined ADC is shown in Figure 5.4. Circuit diagram of telescopic OPAMP is shown in Figure 4.4.

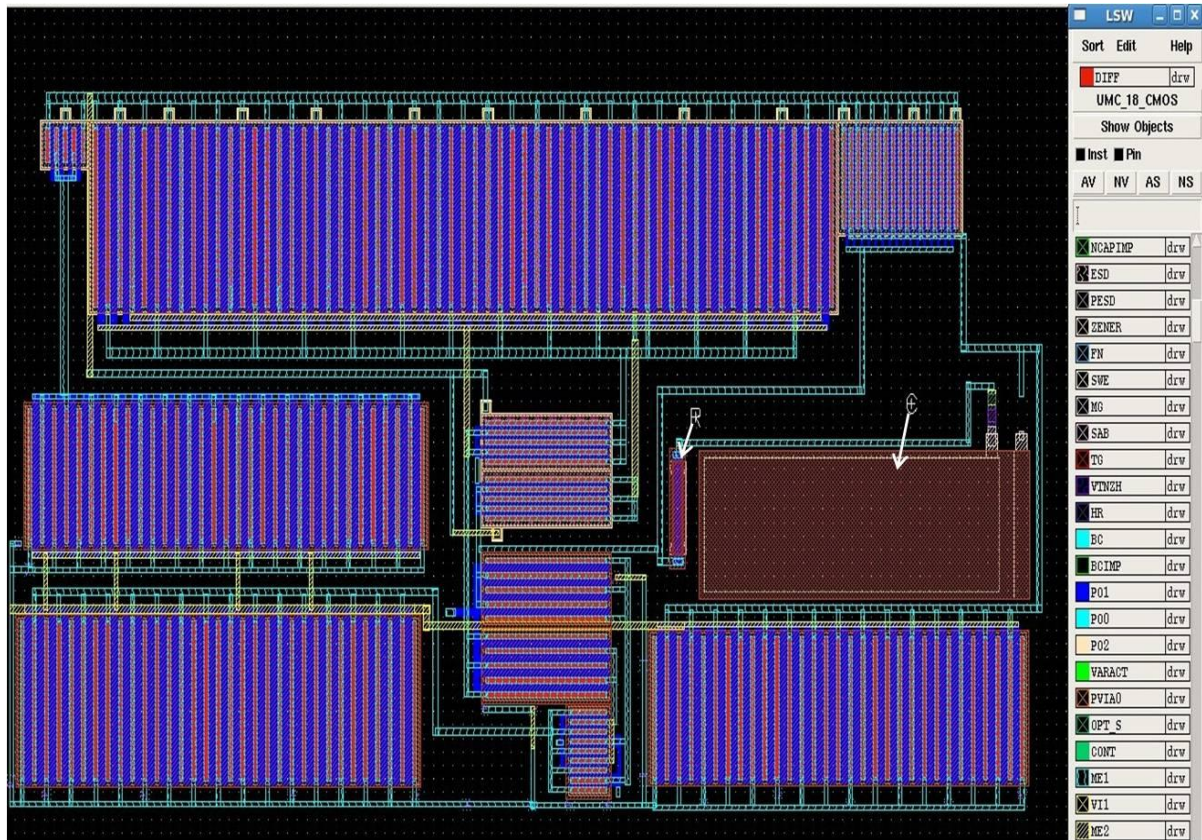


Figure 5.4: Layout of Telescopic OPAMP

Various layout design techniques are used in order to take care of process variation which is very essential for proper operation of OPAMP like inter-digitization. Figure 4.4 shows M1 and M2 as the input transistors which contribute the offset at the output due to process variation so inter-digitization is applied to them. It also reduces the area and parasitic capacitance at various nodes. The layout of compensating network R and C used in Figure

4.4 is also shown in the Figure 5.4.

5.5 Simple Two-Stage OPAMP

Layout of simple two-stage OPAMP used in pipelined ADC in sample and hold stage is shown in Figure 5.5. Its circuit diagram is shown in Figure 4.6.

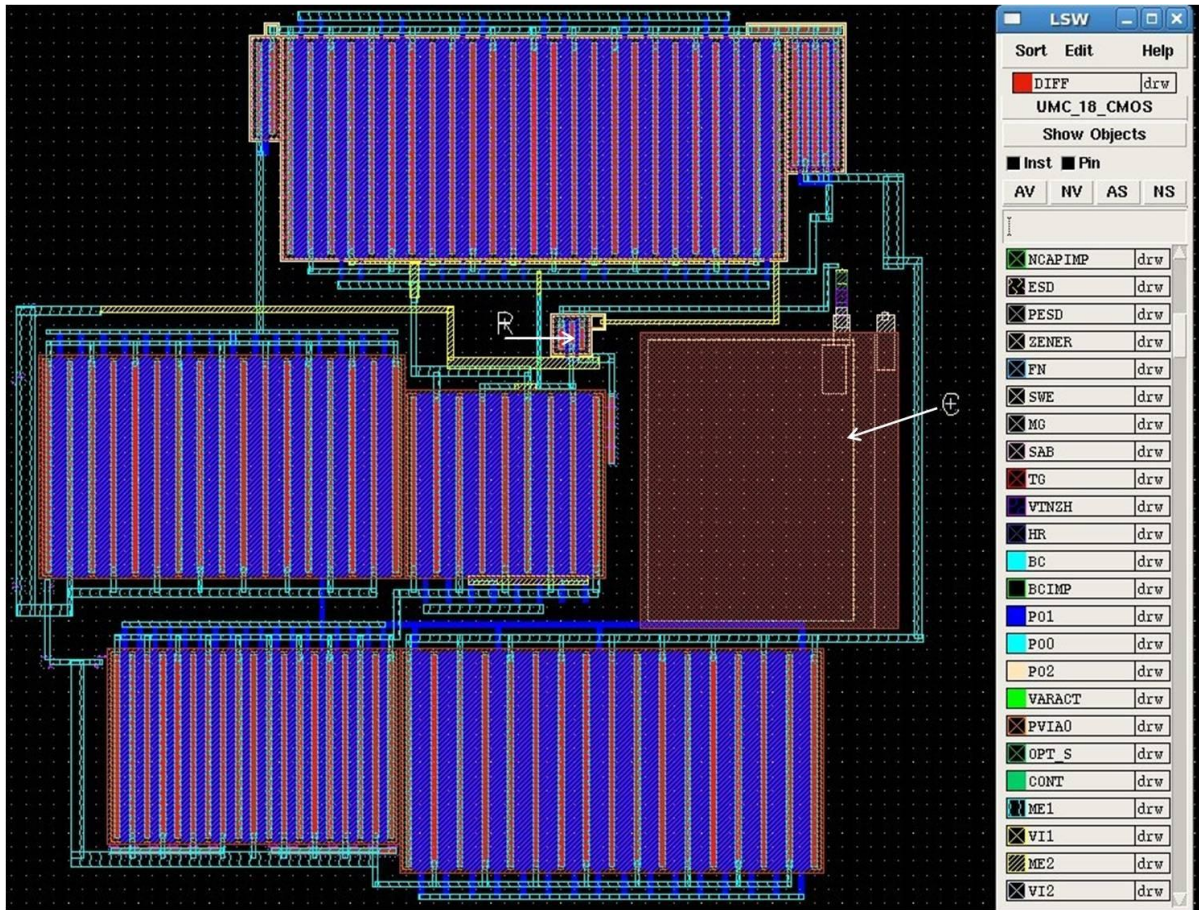


Figure 5.5: Layout of simple two-stage OPAMP

Layout design techniques applied are similar to that used in telescopic OPAMP like inter-digitization. Figure 4.6 shows M1 and M2 as the input transistors which contribute the offset at the output due to process variation. So here also inter digitization is applied to them as applied to telescopic OPAMP. It also reduces the area and parasitic capacitance at various nodes. The layout of compensating network R and C used in Figure 4.6 is also shown in the Figure 5.5.

5.6 Single Stage of Pipelined ADC

Layout of single stage of pipelined ADC is shown in Figure 5.6. Its circuit diagram is shown in Figure 4.18.

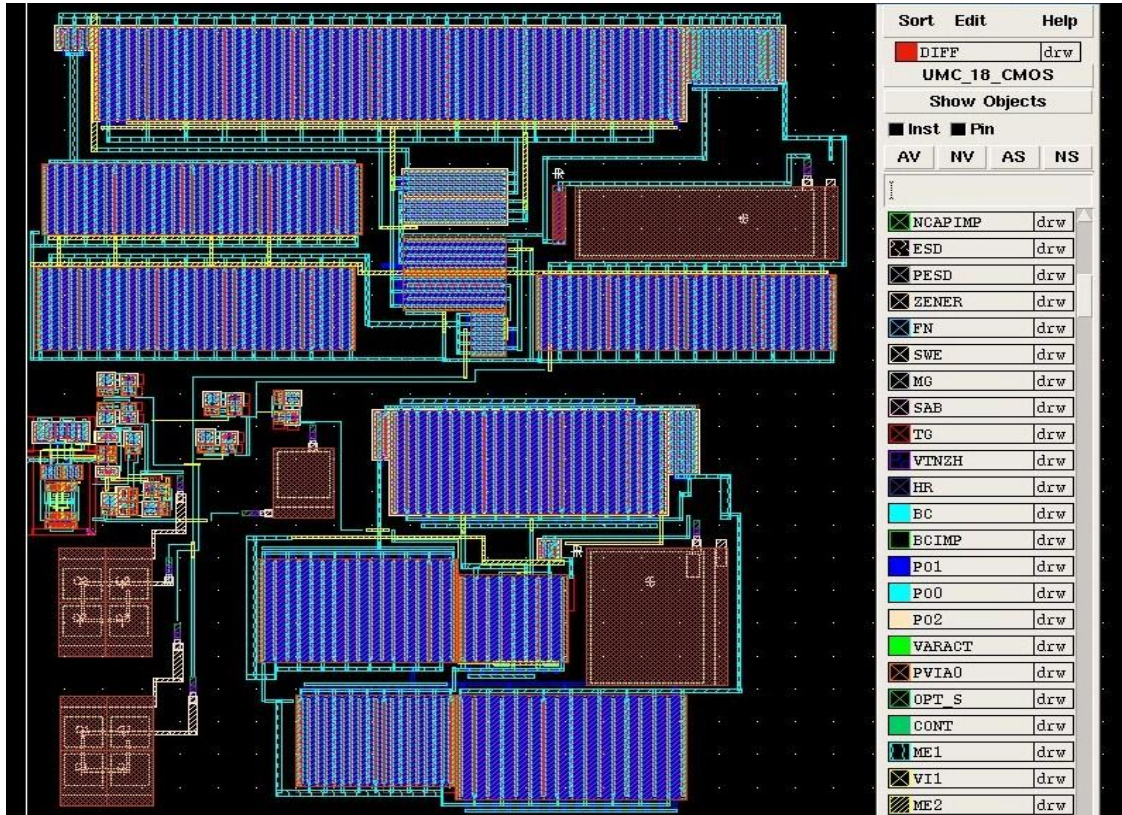


Figure 5.6: Layout of single stage of Pipelined ADC

Here layout blocks of all the building blocks of single stage Pipelined ADC are connected together as shown in Figure 5.6. Proper floor planning is required in order to save the area and metal routing. Layout of sampling capacitors C_s and C_f are shown in the left bottom.

Common-centroid technique is used while drawing the layout of capacitors in order to avoid the process variation. In order to reduce the IR drop long metal wires should have proper widths. It is very important as proper biasing is required at various nodes in the OPAMP. After RC Extraction, post layout simulation is required in order to ensure the proper working of OPAMP.

5.7 Master-Slave type D Flip-Flop

Layout of D flip-flop used in pipelined ADC is shown in Figure 5.7. Its circuit diagram is shown in Figure 4.20.

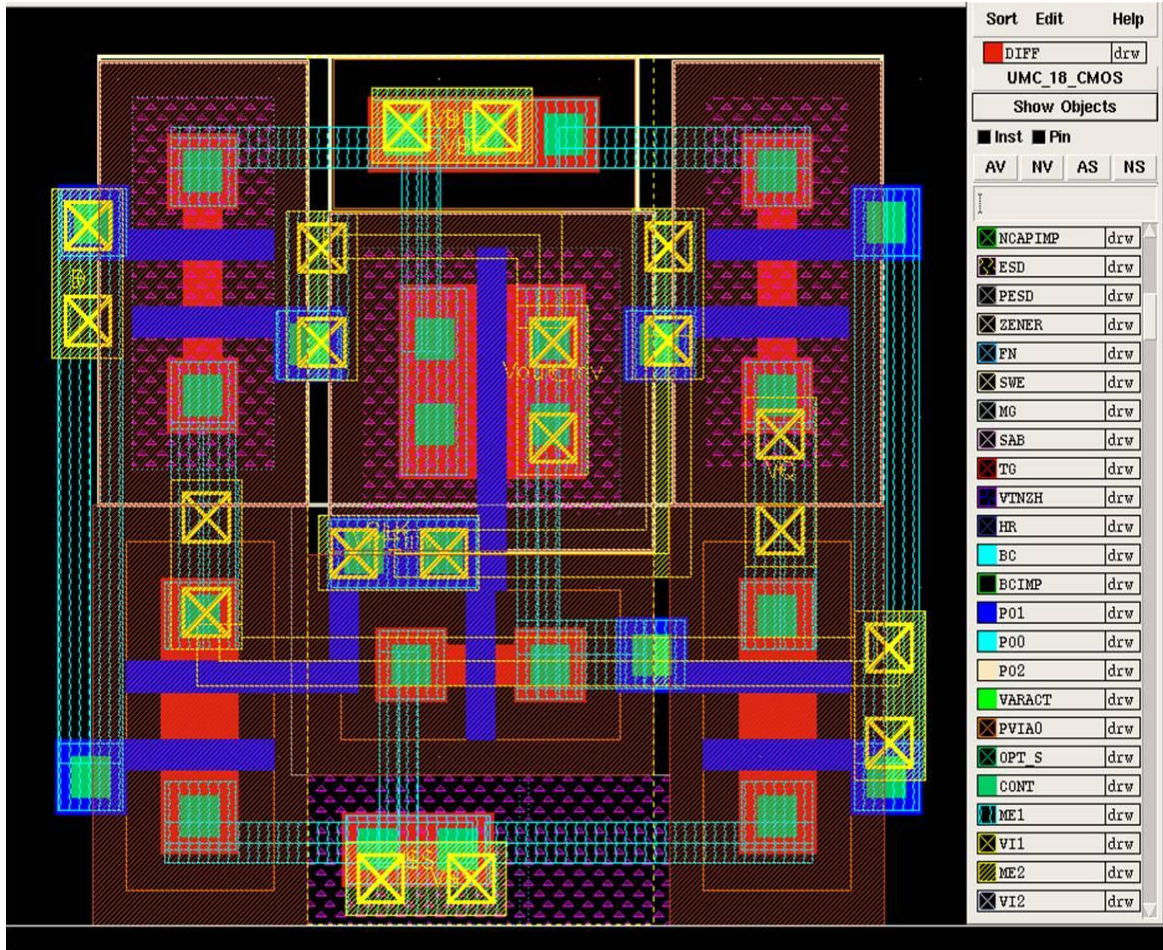


Figure 5.7: Layout of Master-Slave type D Flip-Flop

Chapter 6

Conclusion and Future Scope:

With an increasing trend to a system-on-chip, an ADC has to be implemented in a low-voltage DSM technology in order to achieve low manufacturing cost while being able to integrate with other digital circuits. In the present work, the study and design of a low-voltage 8-bit 30MS/s pipelined ADC in UMC 0.18 μm CMOS process with a 1.8 V supply voltage was presented. Various building blocks of a pipelined ADC stage are studied and designed in Cadence Analog Design Environment.

Large number of bits/stage pipelined ADC architecture also available in various literatures but 1-bit/stage pipelined ADC architecture is chosen because of its simplicity. When a small number of bits/stage is used for a single stage, power dissipation per stage is small because of a large feedback factor. The power dissipation per stage of large number of bits/stage is large because of small feedback factor. Also using large number of bits/stage requires OPAMP with high gain and high UGB than that required in small number of bits/stage. Using small number of bits/stage are more sensitive to component mismatch as compared to large number of bits/stage so in low micron technology it is very challenging to design ADC with small number of bits/stage.

Also the speed and the accuracy of pipelined ADC is limited by errors: capacitor mismatch, finite gain error, systematic offset error and amplifier non-linearity which were studied in detail in this thesis work.

Dynamic comparator is chosen and designed because of its higher speed and low power dissipation but it suffers from large offset. High speed telescopic OPAMP is used to achieve high gain and high UGB. Also simple two-stage OPAMP is designed to use it as a S/H amplifier in each stage. Comparator and OPAMP are the main building blocks of pipelined ADC. Also various non-idealities in pipelined ADC stage are discussed in detail.

Single 1-bit/stage stage is designed, simulated and results obtained are within $\frac{1}{2}$ LSB of required output. Cascading of two pipelined stages is done; simulated and observed results are also within $\frac{1}{2}$ LSB. It has been observed that after cascading of more than 3-4 stages,

residue voltage become more than 1LSB at some of the input voltages which need to debug. This thesis work could not extend after 3-4 stages due to lack of time in debugging the above issue.

In the future, this thesis work can be extended to design the complete 8-bit 30 MS/s pipelined ADC. As 1-bit/stage is more susceptible to process variation and component mismatch, other pipelined ADC architecture should be studied who takes care of these issues like 1.5 bit/stage.

Also in this thesis work, whole stage is designed single-ended; it should be designed fully differentially in order to take care of non-idealities. Fully differential circuits remove the signals such as noise common to both the inputs but at the cost of more area and power. For fully differential stage, fully differentially OPAMPs and comparator will be needed. OPAMPs designed in this thesis work can be easily converted to fully differentially ones. But it requires common mode feedback (CMFB) circuitry to implement the fully differential OPAMPs. Also dynamic comparator used in this thesis work can be modified to implement the fully differential dynamic comparator. Large number of literatures are available who discuss the fully differentially implementation of pipelined ADC.

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