MODELING AND ANALYSIS OF TEMPERATURE DEPENDENCE OF MULTIWALL CARBON NANOTUBES FOR VLSI INTERCONNECTS

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CERTIFICATE

Certified that the thesis entitled **"MODELING AND ANALYSIS OF TEMPERATURE DEPENDENCE OF MULTIWALL CARBON NANOTUBES FOR VLSI INTERCONNECTS"** being submitted by **Mr. Karmjit Singh** to the **Department of Electronics and Communication Engineering, Thapar University, Patiala** in fulfillment of the requirements for the award of degree of **"Doctor of Philosophy"** is a record of bonafide research work carried out by him. He has worked under my guidance and supervision and fulfilled the requirements for the submission of this thesis which has reached the requisite standard. The matter presented in this thesis does not incorporate any material previously published or written by any other person except where, due references are made in the text.

The results obtained in this thesis have not been submitted in part or full to any other institute or university for the award of degree or diploma.

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"*Life without thankfulness is devoid of love and passion. Hope without thankfulness is lacking in fine perception. Faith without thankfulness lacks strength and fortitude. Every virtue divorced from thankfulness is maimed and limps along the spiritual road.*"

— John Henry Jowett

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ABSTRACT

For nano-scaled technology nodes, the density of active devices increases for Very Large Scale Integration (VLSI) chip design. The large number of long interconnects are to be required to interface millions of active devices in an Integrated Circuit (IC). The impedance parameters of interconnects increase linearly as interconnects length increases, therefore the performance of an interconnect becomes more important compared to device performance at deep submicron technology. The present research, explores the possibilities to replace the traditional copper interconnects because its deficiencies like grain boundary, surface boundary and electromigration at nano-scaled technology nodes. Due to large electrical and thermal conductivity of Carbon Nanotubes (CNTs), CNT have been considered as alternative for long VLSI interconnects. CNTs are hollow tubes made from a sheet of carbon grapheme by rolling it up. These cylindrical shaped carbon molecules have attractive thermal and electrical properties which make it more suitable in the field of electronics, nanotechnology, optics, material science and other fields of technology. CNTs are classified as Single Walled Carbon Nonotube (SWCNT) and Multi Walled Carbon Nanotube (MWCNT) on the basis of its structure. SWCNTs are hollow tube rolled up from graphene sheets with similar diameter and SWCNT bundle consists of many such SWCNT tubes. Multi-Walled CNT (MWCNT) consists more than two rolled up hollow tubes having different diameters ranging from few nanometers to tens of nanometers. Both types of CNTs have same current carrying capacity but MWCNTs are easier to fabricate compared to SWCNTs because of its better control on the growth process. Such advantages of MWCNT attract most of the researcher towards the analytical modeling and performance analysis of MWCNT based interconnects for nanoscaled technology nodes.

The high performance VLSI integrated circuit design at nanoscaled technology nodes has large variations in their performance under variable thermal environment conditions for its different applications. Therefore, it is required to include the influence of thermal variations to estimate the accurate performance of an integrated circuit (IC). The works presented in thesis, proposed to estimate the influence of temperature on the performance of MWCNT bundle interconnects for global length. Temperature dependent equivalent circuit model is presented to evaluate the impedance parameters of MWCNT bundle interconnect which includes the various electron–phonon scattering mechanisms as a function of temperature.

The impact of acoustic and optical and zone boundary scattering on electron-phonon scattering mechanism is analyzed resented along with mathematical equations. These mathematical expressions are incorporated the influence of temperature on Mean Free Path (MFP) of MWCNT. Further, effective MFP used to estimate the temperature dependent impedance parameters of an individual shell of MWCNT. All the individual shells of MWCNT bundle have been considered as parallel shells for temperature dependent equivalent model of MWCNT bundle. By using the temperature dependent impedance equivalent circuit model of MWCNT bundle, the impedance parameters have been calculated for global interconnects at 32nm, 22nm and 16nm technology nodes for temperature range of 200K to 450K. For increasing temperature, MFP of shells decreases because of increasing collision rate with in MWCNT. The increase in collision rate is due to electron-phonon acoustics and optical and zone boundary scattering mechanism. The decreased MFP with increasing temperature, influence the resistance for MWCNT shells. Therefore, this change in resistance has considerable effect on the performance in terms of delay, power and PDP for the MWCNT bundle interconnects at nano-scaled technology nodes for global interconnects lengths.

Based on proposed temperature dependent impedance model, the impedance parameters of MWCNT interconnect is calculated for global interconnects at three different technology nodes (32nm, 22nm and 16nm). All interconnects technology parameters are calculated using the data obtained from ITRS 2013 version. The results show that the resistance of MWCNT bundle increases with increasing temperature from 200K-450K for all the global interconnects length under consideration at 32nm, 22nm and 16nm technology nodes. To estimate the performance of MWCNT bundle interconnects, signal delay, power dissipation and Power Delay Product (PDP) is simulated based on temperature dependent model that results in, improvement in the delay, power and PDP estimation accuracy compared to temperature independent model. The results revealed that delay and Power Delay Product of MWCNT bundle interconnects increases with increasing temperature from 200K to 450K for global level interconnects at three different technology nodes i.e. 32nm, 22nm and 16nm. Further, the temperature dependent analytical delay model has been presented for MWCNT interconnects and analytical results are compared with the simulated results. The results show that the analytical results are in similar trend with the simulated results. The trend of both results shows that the delay is increases with rise in temperature for three technology nodes i.e. 32nm, 22nm and 16nm. Therefore, it is concluded from the results that for high

performance IC design, under variable thermal environments need to be considered the impact of temperature to estimate accurate performance. A similar analysis is performed for SWCNT bundle interconnects and copper interconnects and compared with MWCNT bundle interconnects. Comparative results revealed that delay, power and Power Delay Product (PDP) is increased with rise in temperature ranging from 200K to 450K for MWCNT bundle, SWCNT bundle and copper interconnects. It has also been observed that MWCNT bundle interconnects gives better performance in terms of delay, power and PDP as compared to SWCNT bundle interconnects for global levelinterconnects at 32nm, 22nm and 16nm technology nodes under thermal variable conditions.

ACRONYMS AND ABBREVIATIONS

Abbreviation	Description
AR	Aspect Ratio
CMOS	Complementary Metal Oxide Semiconductor
CNTs	Carbon Nanotubes
Cu	Copper
DIL	Driver Interconnects Load
EDA	Electronic Design Automation
EM	Electromigration
FET	Field Effect Transistor
GHz	Giga Hertz
GNR	Graphene Nanoribbon
IC	Integrated Circuits
ITRS	International Technology Roadmap for Semiconductor
MFP	Mean Free Path
MWCNT	Multi Walled Carbon Nanotube
PDP	Power Delay Product
RC	Resistance Capacitance
RLC	Resistance-Inductance-Capacitance
SPICE	Simulation Program with Integrated Circuit Emphasis
SWCNT	Single Walled Carbon Nanotube

PTM	Predictive Technology Model
VLSI	Very Large Scale Integration

GLOSSARY OF SYMBOLS

Symbol	Description
C_q	Quantum Capacitance
C_e	Electrostatic Capacitance
D_{inner}	Diameter of innermost shell of MWCNT
D_i	Diameter of i^{th} shell of MWCNT bundle
d	Tube Diameter of SWCNT
E	Electron charge
$h\omega$	Optical-phonon energy
H	Height of SWCNT bundle
k_B	Boltzmann's constant
L	Length of Interconnect
L_K	Kinetic inductances of an individual SWCNT
L_M	Magnetic inductances of an individual SWCNT
$N_{\frac{chan}{shell}}$	Number of conducting channel per shell
n_{Bundle}	Total number of shells in a SWCNT bundle.
$n_{H(Bundle}$	Number of rows in SWCNT bundle
$n_{W(Bundle}$	Number of column in SWCNT bundle
$N_{chan/bundle}$	Number of channel per MWCNT bundle
R_{shel}	Resistance of MWCNT shell
R_s	Scattering Resistance
R_c	Contact Resistance
R_q	Quantum Resistance
T_0	Room temperature (300K)
T	Temperature in K

W	Width of SWCNT bundle
x	Centre to centre distance of adjacent tubes in SWCNT bundle
Y	Distance between center of MWCNT bundle and ground
H	Planck's constant
μ	Mobility of electron
$\rho(T)$	Temperature dependent resistivity of copper interconnect
λ_{eff}	Effective MFP
λ_{AC}	Acoustic MFP
λ_{OZB}	Optical and zone boundary MFP
$\lambda_{ozB,fld}$	MFP is due to the electric-field acceleration
$\lambda_{OZB,abs}$	MFP due to absorption of an optical or zone-boundary phonon
v_f	Fermi velocity
δ	Spacing between two adajecent shells of MWCNT (van der Waals distance)

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Published/Accepted Papers in Journals

1. **Karmjit Singh**, Balwinder Raj, "Performance analysis of temperature dependent Multi-walled Carbon Nanotubes as Global Interconnects at different technology nodes," *Journal of Computational Electronics, Springer,* Volume 14, Issue 2, pp 469-476, June 2015. **(SCI indexed-Impact Factor- 1.520).**

2. **Karmjit Singh**, Balwinder Raj, "Influence of Temperature on MWCNT bundle, SWCNT bundle and Copper interconnects for Nanoscaled Technology nodes," *Journal of Materials Science: Materials in Electronics. Springer,* Volume 26, Issue 8, pp 6134-6142, August 2015. **(SCI indexed-Impact Factor-1.569)**.

3. **Karmjit Singh**, Balwinder Raj, "Temperature Dependent Modeling and Performance Evaluation of Multi-Walled CNT and Single-Walled CNT as Global Interconnects," *Journal of Electronic Materials, Springer,* DOI :10.1007/s11664-015-4040-x ***(*SCI indexed-Impact Factor-1.798).**
4. **Karmjit Singh**, Balwinder Raj, "Comparison of Temperature Dependent Performance and Analysis of SWCNT bundle and Copper as VLSI Interconnects," *Research Cell: An International Journal of Engineering Sciences,* **(Accepted).**

Accepted Paper in International Conference

5. **Karmjit Singh**, Balwinder Raj, "Thermally Aware Modeling and Performance for MWCNT Bundle as VLSI Interconnects for High Performance Integrated Circuits," ***IEEE-4th Global Conference on Consumer Electronics (IEEE-GCCE 2015)*** Osaka, Japan **(Accepted).**

1 INTRODUCTION

1.1. Preamble

Interconnects are the conducting wires used in Integrated Circuits (IC) to establish the electrical links between different nodes of the electrical circuit[1, 2]. Different materials have been used as interconnects in ICs. Due to shortcomings of any existing material at certain technology node, traditional materials are replaced by other new materials. The performance of an IC is mainly depends upon the current carrying capacity and impedance parameters such as resistance, inductance and capacitance of the interconnect material [3-5]. As technology scaled down, the feature size and supply voltages of ICs are also scaled down to maintain electric field constant. Therefore, interconnect dimensions required to be scaled down with advanced technology nodes [3, 6-11]. With advancement of technology nodes, a large number of functionalities are to be incorporated in Very Large Scale Integration (VLSI) chips. Thus, the requirement of long interconnects is exponentially increasing which connect millions of active devices in an IC. [9, 12-17] The schematic of Driver Interconnects Load (D-I-L) is shown in Fig. 1.1.

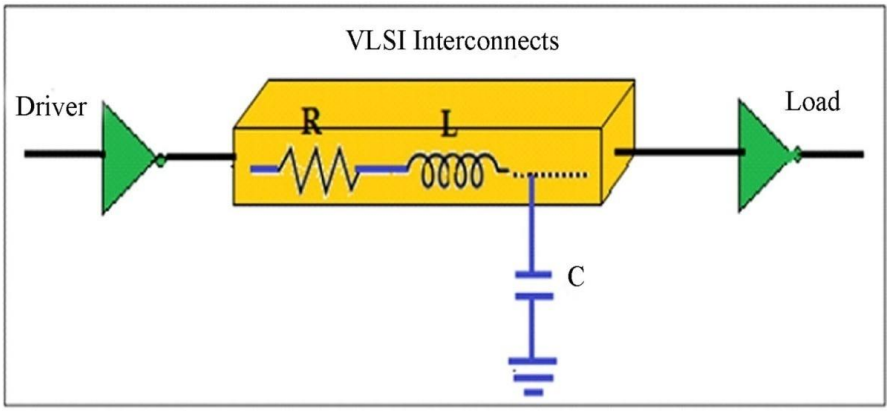


Figure 1.1: Schematic structure of VLSI interconnects [15].

In D-I-L, an interconnect is driven through CMOS inverter and loaded with a load (normally a capacitive) as shown in Figure 1.1. To estimate the performance of interconnects 'VLSI interconnects" is replaced with its equivalent R-L-C circuits model. These impedance parameters of interconnects are depend on the cross sectional dimensions and properties of the material used as "VLSI Interconnects".[18-22].

On the basis of interconnects length and cross-sectional dimensions, interconnects of ICs can be classified into three types as shown in Fig. 1.2. The cross-sectional view shows device layers and interconnects layers of Integrated Circuits (IC) [15].

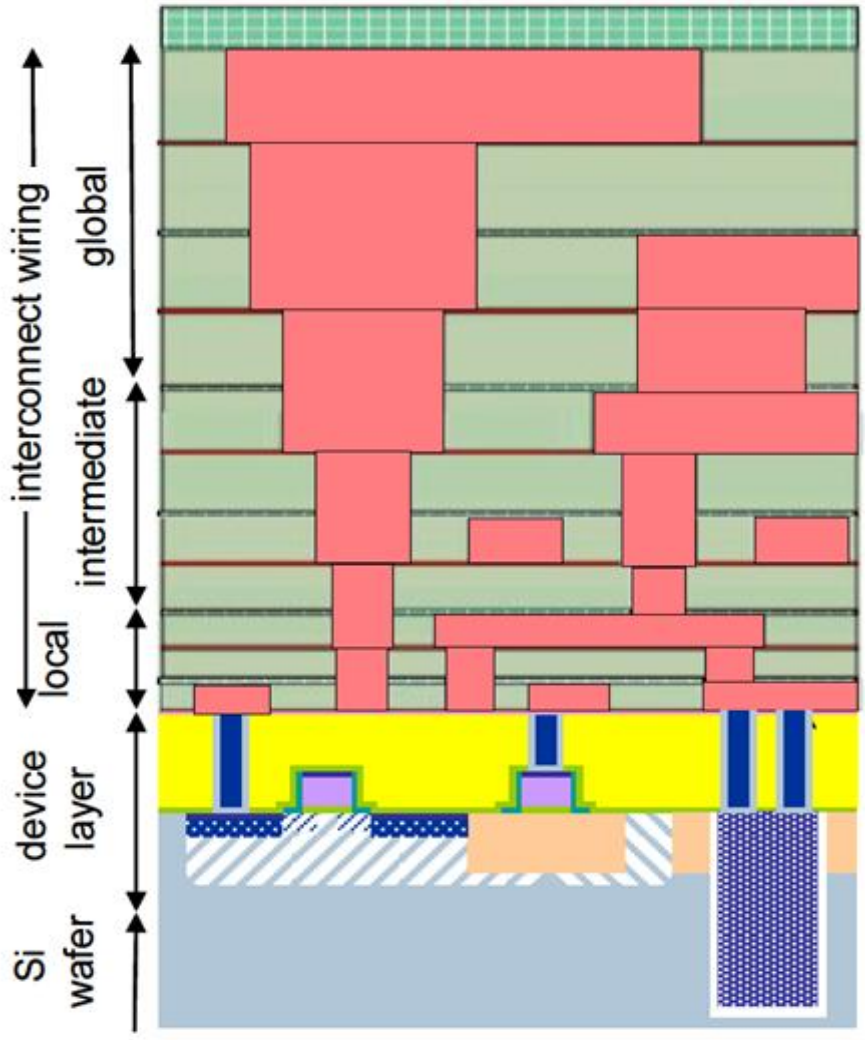


Figure 1.2: A cross sectional view of different types of interconnects for an Integrated chip (IC) [15].

Local interconnects: Local interconnects as shown in Fig. 1.2, are used to deal with small interconnects length ranging from few micrometers to tens of micrometers and can be used to connect nearby nodes. They usually connect device level terminals of CMOS technology i.e. gates, sources and drains of CMOS devices. The local interconnects can also be used as gate

electrode material for CMOS technology (vias). Since, local interconnect deals with short length wires, they can afford the high resistivity materials as interconnects compared to global interconnects. In local interconnects, maximum part of the total propagation delay is contributed by the devices of the integrated circuits. But local interconnects should be capable to resist for higher temperature applications [23-25].

Intermediate interconnects: Interconnects, which deals with both short and long interconnects length are known as intermediate interconnects. It is also known as semi-global interconnects as well. The different devices within a block, are connected through these interconnects. Intermediate interconnects lengths, within two or more blocks used for communication are also connected through these interconnects with typical lengths up to 400um [26, 27].

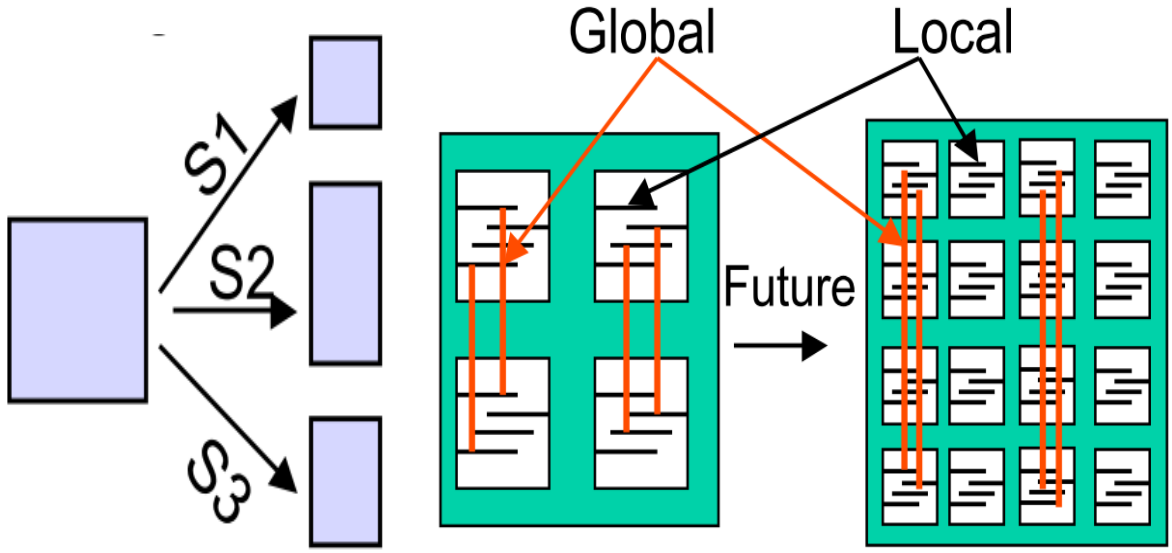
Global interconnects*:* The long interconnects length (> 400μm) used as ground, clock and power lines are known as global interconnects. For global interconnects length, the propagation delay and power dissipation are the key factors to understand the performance of interconnect. Therefore, these should always be of low resistant metallic materials as they often travel over large distances to provide connection between different parts of the circuit and different devices [15, 27].

The cross-sectional view of three different levels of interconnects are shown in Fig. 1.2 with dimensions of the local, semi-global and global interconnects. The cross-sectional view shows that with technology scaling down, local interconnects are used to connect the nearby nodes at the lowest level of the hierarchy followed by intermediate level interconnects used to connect the devices within the blocks, Global interconnects are generally used for long interconnects lengths to connects various functional blocks, power supply, clocks and grounds [15, 25].

1.2. Importance of Scaling

Scaling process in VLSI circuits design, related to systematic reduction of device dimensions as permitted by technology while geometric ratios remains preserved. The designing of high performance and high density VLSI chip design, needs the high packing density of CMOS based devices. Therefore, the size of these devices needs to be kept small to meet the required area considerations. The channel length and width of CMOS transistor are scaled down as the technology nodes scaled down. As the device dimensions are scaled down, the dimensions of interconnects are also needed to be scaled down [15, 16]. The interconnects cross sectional and length scaling is shown in Figures 1.3(a) and (b) respectively. It is shown in Figure 1.3(a)

that interconnects can be scaled down with different scaling factor *S1*, *S2* and *S3*. Similarly, wire lengths are also needs to be scaled, for future IC design. To estimate the performance of an integrated circuits, the effect of scaling on interconnects are required to be considered. The effects of scaling on local interconnects is negligible small as most of the performance estimation parameters are device dependent. Due to large impedance parasitic of long interconnects, the performance of interconnects dominates over the total performance of an IC. For long interconnects, if the device dimensions are scaled with a scaling factor *1/S* then, the propagation delay will be increased by $S^2.S_C^2$ where S_C^2 is scaling factor for size of chip.[3, 4, 28]



(a) **(b)**

Figures 1.3: (a) Interconnects wire cross sectional (b) wire length scaling respectively of an IC [15, 16].

1.3. Significance of Repeaters for long Interconnects

Interconnects can be categories into three types on the basis of their lengths as describes in section 1.1. The local interconnects are used as small interconnects wires (for device level terminals or vias), the impedance parasitic of interconnects are small compared to the impedance parasitic of driver transistor. The impedance parameters of interconnects increases linearly as interconnects length increases. Thus, the propagation delay of interconnects also increases with increase in length. The impedance parameters of the long interconnect becomes larger as compare to driver transistor. Therefore, repeaters are introduced to

decrease the overall delay of long interconnects [3, 29-32]. The repeaters divide the long interconnects into subsections/ segments and each subsection/segment is driven by CMOS inverter[33], known as repeaters as shown in Figure 1.4 [29]. The propagation delay (RC time constant) used to estimate the performance of VLSI circuits and it increases sharply as interconnect dimensions are scaled down with advanced technology nodes and affect the speed of VLSI circuits. Therefore, to improve the performance in terms of propagation delay and speed of the circuit, optimum number repeaters and optimum sized repeaters can be used. [3, 29-31, 33-41]

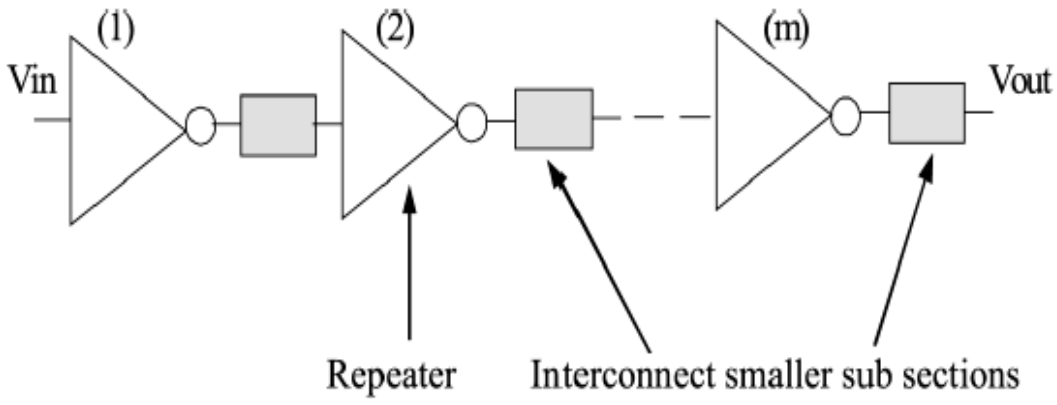


Figure 1.4: A lumped interconnect divided into different subsections as distributed model with optimum 'm' number of repeaters [29].

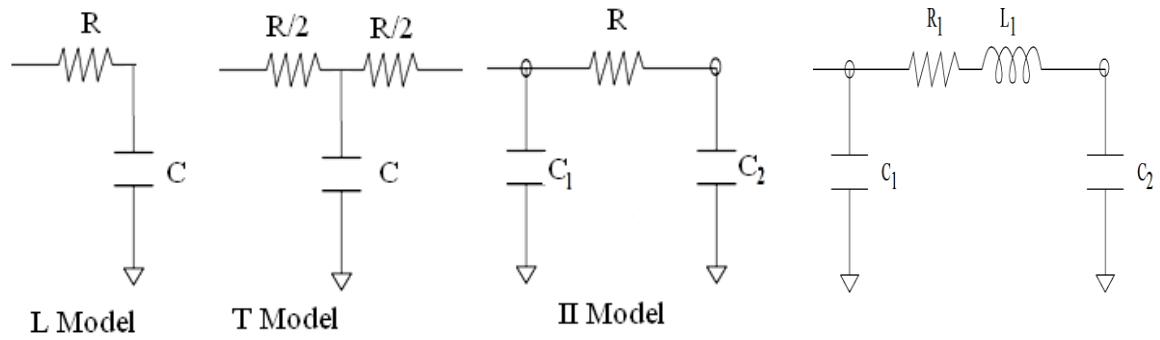
1.4. Interconnect Models

Interconnect wires of integrated circuits are acting as transmission line. Therefore, interconnect equivalent circuit model is used to estimate their performance. Interconnect models are the function of their impedance parameters in order to analyze the parasitic effects in the interconnects[42]. The interconnect models may be simple or complex depending upon the way they arranged, various effects that are being included and the accuracy required from the model.

1.4.1. Lumped Model

The equivalent lumped model for an interconnect, consists of impedance parameters like resistance, capacitance and inductance are concentrated into ideal electrical components; resistors, capacitors, and inductors[43]. The different configurations of RC interconnect

lumped models are shown in Figure 1.5(a). These models are categories as; L-model, T-model and Π-model depending upon the shape and the way they are connected.



(a) **(b)**

Figure 1.5: (a) Different configurations of RC interconnect lumped models (b) RLC interconnects lumped model [8].

In recent researches, an RLC equivalent circuit models are preferred over simple RC models and their equivalent Π-model is shown in Figure 1.5(b). An RLC lumped model, which not only consists of resistive and capacitive part but also included the inductive part as well. The performance of RLC circuit models are 30% to 35% better than RC models. [35-37, 44]

1.4.2. Distributed Model

The distributed RLC model can be approximated by a lumped multi-stage RLC network can be depicted as Figure 1.6. When a lumped interconnects model divided into different subsections/segments, referred as distribution models as shown in Figure 1.6 [8, 45]. Repeaters are generally inserted to drive a smaller subsection of distributed equivalent circuit model. The distributed circuit model, increase the drive capacity and reduce the overall delay of given long interconnects lengths [36]. The optimum number of repeaters and size of a repeater are chosen for simulation at different technology nodes [46-52].

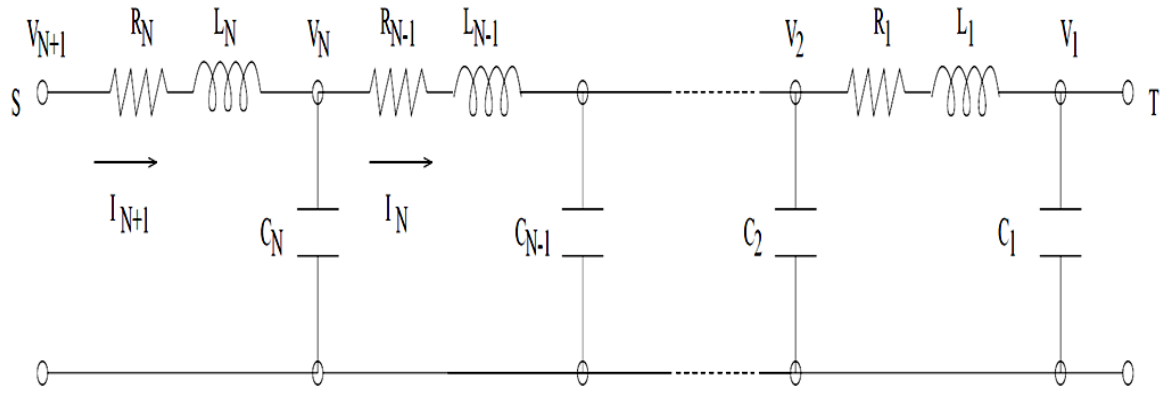


Figure 1.6: Distributed RLC Model (with N Segments)[8].

1.5. Aluminum as Interconnects

In earlier technology nodes, the aluminum was used as interconnect material due to its excellent characteristics such as good conductivity, good ohmic contact with silicon and adheres on silicon dioxide. As technology scaled down to micro-scaled level, interconnects current density increases and causes electromigration[23, 53]. Electromigration referred as the transfer of energy between the conducting electrons and the diffusing metal atoms, transport of material thus takes place by the gradual movement of ions. As the technology node further scaled down, the effect of electromigration increases. Moreover, the aluminum has the resistivity in the order of 2.7 μΩ–cm which is very higher than the resistivity of copper (1.7 μΩ–cm) [54]. Therefore, at micro-scaled technology nodes, there is need of high current density but due to its large resistivity and electromigration, high current density cannot be achieved. Due to these disadvantages, copper was used as an alternative interconnects material at micro-scaled technology nodes [5, 6, 55-57].

1.6. Copper as Interconnects

Aluminum was replaced with copper as an alternative material for interconnects, due to the shortcomings of aluminum at micro-scaled technology nodes. The copper has high current density, low resistivity and more immune to electromigration compared to aluminum. Copper also has higher electrical conductivity and melting point (1357K) compared to aluminum (933K) making it thermally more stable.[58] Comparative analysis of some properties of copper and other conducting materials and given in table 1.1.

Table 1.1: Comparison of different properties of conducting materials[23].

Properties/ Materials	Copper (Cu)	Aluminum (Al)	Gold (Au)	Silver (Ag)	Tungsten (W)
Resistivity (μΩ-cm)	1.7	2.7	2.35	1.6	5.65
Melting Point(K)	1357	933	1264	1062	3387
Corrosion in Air	Poor	Good	Excellent	Poor	Good
Adhesion to SiO_2	Poor	Good	Poor	Poor	Poor

Some other properties of copper shown in table 1.1 which make more suitable alternative compared to aluminum at micro-scaled technology nodes for VLSI interconnects.

However, as technology is scaled down to nano-scaled technology nodes (< 45nm), the resistance of copper interconnects increased rapidly because the small Mean Free Path (MFP). The MFP is the average distance travelled by an electron before its collision. The average MFP of copper is approximately equal to 45nm.[44, 59-61] The MFP of electrons is depending upon the combined effects of enhanced grain boundary scattering, surface scattering and electromigration. Grain boundary is the interface between two crystallites in a polycrystalline material. Due to grain boundaries introduce electron scattering which leads to reduce the mobility of electron and hence, it tends to increase the thermal and electrical resistivity. As technology scaled down to nano-scaled level (<45nm), the MFP of electron of copper becomes comparable to the cross-section dimensions of interconnects. Hence, there is more reflection of a electron at the surfaces cause the scattering. The scattered electrons emit or absorb phonon, introduce impurities in the copper [53, 62-64]. So, the total collisions rate with the surfaces scattering will suddenly increased and hence increase the resistance of copper at nano-scaled technology nodes, impose the serious challenges for interconnects delay and systems reliability.[56, 57, 62-68]

Therefore, sudden rise in resistance has a considerable effect on the overall performance and reliability particularly for long interconnects of VLSI circuits design. In the recent times Carbon Nanotubes (CNT) based interconnects at global interconnect level, has been considered as a proper alternative to the conventional copper interconnects. [66, 69-71]

1.7. Carbon Nanotubes as Interconnects

Carbon nanotubes (CNTs) have emerged as a promising material for future VLSI technology. CNTs are known as allotrope of carbon and made by rolling up a sheet of carbon known as graphene into a cylinder. These cylindrical shaped carbon molecules have attractive thermal and electrical properties which make it more suitable in the field of electronics, nanotechnology, optics, material science and other fields of technology. In particular, CNTs have applications in field of VLSI interconnects due their extraordinary properties. CNTs have longer MFP (1000nm) and high current density ($>10^{10}$) as compared to copper [70-75]. A comparison of different properties of CNTs and copper is given in table 1.2.

Table 1.2: Comparison of different electrical and thermal properties of Copper, SWCNT, MWCNT and Graphene [23, 26].

Properties\Material	**Cu**	**SWCNT**	**MWCNT**	**Graphene**
Maximum current density(A/cm2)	10^6	10^{10}	10^{10}	10^9
Thermal Conductivity(10^3 .W/mK)	0.385	1.75-5.8	3	3-5
Mean free Path(nm)	40	$>10^3$	$2.5X10^4$	$1X10^3$
Melting Point (K)	1357	3800(graphite)		
Temperature coefficient of resistance (10^{-3}/K)	4	<1.1	-1.37	-1.47
Mechanical Strength	Poor	Fair	Fair	Fair
Process of Fabrication	Easy	Difficult	Difficult	Difficult

1.8. Classification of CNT

Carbon nanotubes are classified into different types according to their structure, chiralty and conductivity.

1.8.1 Structure based Classification:

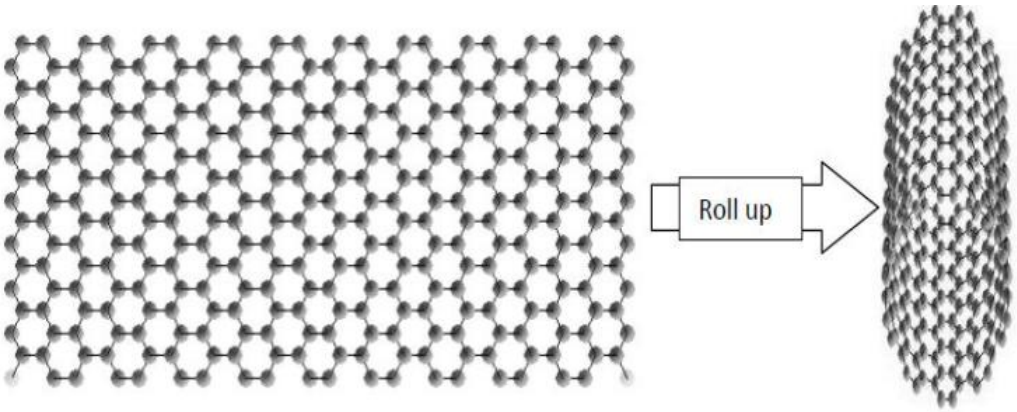
As per its structures, CNTs are classified into two types:

- Single-Walled Carbon Nanotubes
- Multi-Walled Carbon Nanotubes

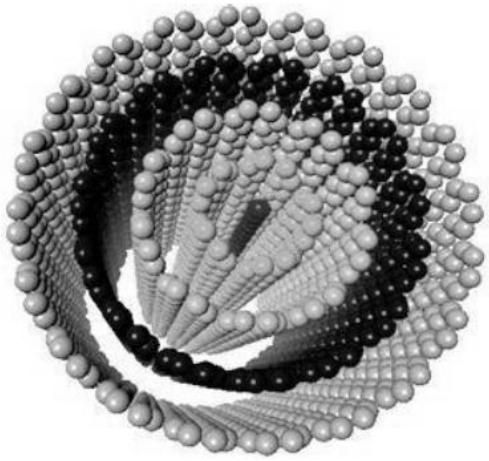
Single-Walled CNT' (SWCNT) consists of one rolled up graphene sheet of similar diameter as shown in Figure 1.7(a). In case of SWCNT bundle, all SWCNTs are considered to have similar diameter and same number of conducting channels. Thus the effective resistance and kinetic inductance per tube are divided by the number of SWCNTs and the quantum capacitance per tube is multiplied by the number of SWCNTs in a bundle [63, 76-79].

Multi-Walled CNT (MWCNT) consists more than two rolled up graphene sheets with diameters ranging from few nanometer to tens of nanometer. An MWCNT bundle has many concentric shells of different diameter, which can be seen as several shells in parallel as shown in Figure 1.7(b). It may appear similar to an SWCNT bundle which consists many CNT in parallel but with different diameters for each shell of MWCNT bundle. In case of SWCNT bundle, all nanotubes are considered to have similar diameter and same number of

conducting channels. In case of MWCNT bundle, it has shells with different diameters hence every shell consists of different number of conducting channels and MFP, resulting in different impedance parameters. Due to this, the parameters of each shell of MWCNT bundle cannot be combined in a simple way as in the case of SWCNT bundles.[18, 19, 24, 27, 65, 80-85]



(a)



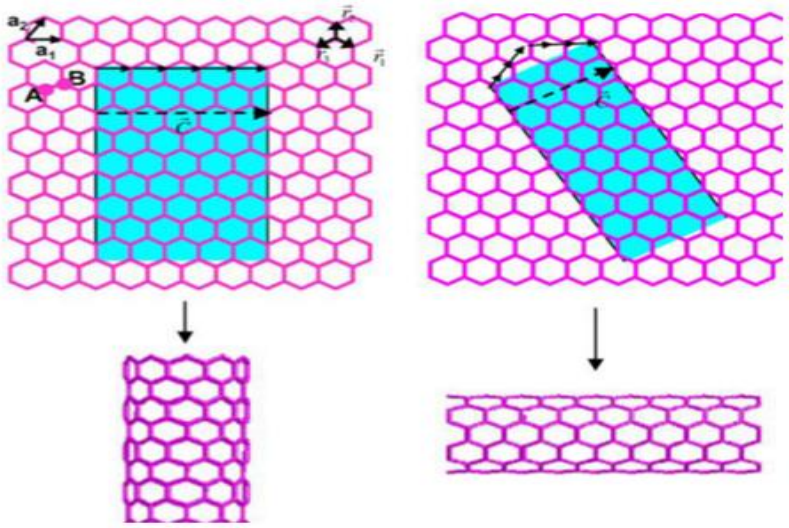
(b)

Figure 1.7: (a) Structure of SWCNT (b) Structure of MWCNT.[65]

1.8.2. Based on Chirality and Conductivity

CNTs can be classified into two types on the basis of chiral indices (n,m): armchair and zigzag. When the any one chiral indices (*n* or *m=0*) equals to zero, resultant structure is known as zigzag and shown in Figure 1.8(a) and for armchair chiral indices should be same i.e. *m=n* and shown in Figure 1.8(b). Depending upon the direction of CNT in which they are rolled up, decide the conductivity, either metallic or semiconductor. When $n - m = 3i$ (where *i*

is an integer), the armchair structures are always metallic and zigzag structures are either metallic or semiconducting depends upon the chiral indices. For VLSI interconnects only metallic CNTs structure can be used because of their high electrical and thermal properties. [24, 27, 76, 86-89]



(a) (b)

Figure1.8: (a) Zigzag semiconducting configuration (b) Armchair metallic configuration of CNT [90].

As MWCNT bundle have large diameter compared to SWCNT, MWCNT bundle consists of large number of conducting channels and long MFP. SWCNT and MWCNT have same current carrying capacity but MWCNTs are easier to fabricate as compared to SWCNTs because of its better control on the growth process. Due to these advantages, most of the research has been focusing towards the modeling and performance analysis of MWCNT based interconnects for nanoscaled technology nodes.[27, 70, 80-82, 91-95]

The high performance VLSI integrated circuits at deep submicron technology have large variation in their performance under variable thermal environment conditions for its different applications in the field of automobile industry, aeronautical engineering etc.[96-98]. These thermal variations have a significant effect on the electron surface and grain boundary scattering mechanism in MWCNT. This temperature dependent scattering mechanism has significant effect on the MFP of MWCNT and influences the performance of MWCNT in terms of delay and power for VLSI interconnects. Therefore, the influence of thermal variation on the performance in terms of delay and power needs to be investigated for MWCNT bundle interconnects. The purpose of the thesis is to propose the temperature dependent equivalent circuit model of MWCNT bundle interconnects for global interconnects

length at nano-scaled technology nodes. The theoretical model is then needs to be simulated through a CMOS inverter to comprehend influence of temperature variation on the performance in terms of delay and power of MWCNT bundle interconnect at 32nm, 22nm and 16nm technology nodes for global interconnects. To perform the comparative analysis, the influence of temperature on SWCNT bundle and copper interconnects are also presents for global interconnects and results are compared with MWCNT bundle interconnects.[52, 81, 82, 88, 90, 99-108]

1.9. Organization of Thesis

The **Chapter 1** is introductory and serves the purpose of familiarizing the basic concept needed in the subsequent chapters. It starts with the general overview of interconnects. The disadvantages of tradition copper interconnects, need of CNTs as interconnects and introduction to structures of SWCNT and MWCNTs bundle as interconnects are discussed in this chapter. Impact of temperature on the performance of CNTs and copper interconnects is also discussed. Finally, the chapter wise thesis organization has been given.

Chapter 2, gives a complete review of related literatures to provide background information on the issues to be considered in the thesis and to highlight the significance of the present study. It presents the preliminaries of VLSI interconnects, copper interconnects, need of CNT as interconnects, benefits of SWCNT and MWCNT as interconnects and thermally aware modeling of SWCNT and copper interconnects. The deficiencies of copper interconnects at nano-scaled technology nodes presented in the literature are highlighted for study. Then literature defining the need of carbon nanotubes as interconnects. It comprising the existing results to witness the SWCNT as alternative materials for local level interconnects. Further, literature presents the study related to MWCNT as global level interconnects. The results presents in the literature shows that there is overall improvement in delay and area for MWCNT bundle compared to SWCNT bundle as global interconnects and predicted as suitable material for future interconnects. Finally, the literature defines the thermally aware modeling for copper and SWCNT interconnects. The literature suggested that the rise in temperature has a comparable impact on the performance of interconnects. Therefore, high performance ICs design at moderate to high temperature needs to include the impact of temperature to understand the actual performance of material. Critically analyzing the literature, some gaps were formulated. On the basis of gaps found in the literature, objectives and methodology for the current work has been decided.

Chapter 3, explores the impact of temperature on scattering mechanism of the carbon nanotubes. With the help of extensive mathematical computations, the dependency of temperature on MFP of an individual shell of MWCNT has been obtained so that the impact of temperature on the impedance parameters can directly be obtained. An equivalent temperature dependent RLC model is presented for MWCNT bundle for global interconnects length. Further, temperature dependent equivalent impedance models are presented for both SWCNT bundle and copper interconnects.

Chapter 4, presents the temperature dependent performance analysis for MWCNT bundle interconnects. By using the proposed mathematical expressions, temperature dependent effective MFP of each shell of MWCNT is calculated for temperature range of 200K to 450K. On the basis of proposed temperature dependent impedance model, the impedance parameters of each shell of MWCNT are calculated for global interconnects length at 32nm, 22nm and 16nm technology nodes. The equivalent impedance parameters of MWCNT bundle are obtained by considering all the parameters of individual shells in parallel. Further, the calculated impedance parameters for MWCNT interconnects have been simulated for three different technology nodes to evaluate the performance in terms of delay, power and PDP.

In **Chapter 5**, the temperature dependent analytical delay model is presented for MWCNT interconnects and results are compared with the simulated results obtained from chapter 4. The results presented in the chapter shows that the analytical results are aligned with the simulated results. The trend of both results shows that the delay is increases with rise in temperature for all the technology nodes i.e 32nm, 22nm and 16nm.

In **Chapter 6**, temperature dependent impedance parameters for SWCNT bundle and copper interconnect is calculated using the equivalent models presented in the chapter 3. Further, these temperature dependent impedances are simulated using SPICE simulation tools. The study of comparative analysis of MWCNT bundle interconnects with SWCNT bundle and copper interconnects is presented. The results show that performance of proposed temperature dependent impedance model for MWCNT bundle interconnects is better than SWCNT bundle and copper interconnects for all technology nodes under consideration.
Finally, the conclusion of the thesis along with the possible future scope in the area of work is discussed in **Chapter 7**.

2 LITERATURE REVIEW

This chapter gives a complete review of related literatures to provide background information on the issues to be considered in the thesis and to highlight the significance of the present study. It presents the delay models of VLSI interconnects, copper interconnects, need of CNT as interconnects, benefits of SWCNT and MWCNT as interconnects and thermally aware modeling of SWCNT and copper interconnects

2.1. Introduction

The scaling of technology nodes, influences the performance of interconnect wires used in VLSI circuits. The increased die size and high chip density requires long interconnect wires for integrated circuits. With reduced feature size of the devices at advanced technology nodes, the dimensions of interconnects needs to be reduced as well [90, 109]. To analyze the accurate performance of interconnects, different delay model are presented in the literature. The repeaters of different sizes and shapes are proposed in the literature to mitigate the effect of impedance parameters which helps to minimize interconnects delay for long interconnects [29-31, 35]. For long interconnects, the characteristics of interconnects material play an important role particularly in deep submicron technology nodes. Performance of copper interconnects material at advanced technology nodes gets degraded and Carbon Nanotubes (CNT) is proposed as alternative for deep submicron technology nodes. Different works in the literature are presented to understand the performance of carbon nanotubes makes it more suitable candidate for intermediate and global interconnects. The performance of different types of CNT (SWCNT and MWCNT) based interconnect has been compared with copper for different interconnects lengths at different technology nodes. To understand the accurate performance of interconnects; thermal conditions are needs to be included during the analysis in deep submicron technology nodes. Temperature dependent analytical models for copper and SWCNT and their performances in terms of delay and power are presented in the

literature. The work presented in the literature is focused on the performance of MWCNT, SWCNT and copper as interconnects and influence of temperature on the performance of SWCNTs and copper as interconnects.[61, 64, 110, 111]

2.2 Interconnects Delay Models

The concept of transmission-lines plays an important role to analyze interconnects delay and performance of the systems for advanced technology nodes for VLSI circuits. Several delay models have been suggested in the literature to find analytical expressions and estimate the delay and shapes of output waveforms of interconnects.

H. B. Bakoglu, *et al*. [3], presented the effect of cross-section dimensions on the performance in terms of delay for copper interconnects. The impact of scaled down dimensions is discussed in details and results are presented for local and long interconnects. The effects of scaling on local interconnects is shown as negligible small but for long interconnects, the propagation delay increases. The results presented in the papers show that for long interconnects, if the dimensions are scaled with a scaling factor *1/S* than the propagation delay will be increased by $S^2.S_C^2$ where S_C^2 is scaling factor for size of chip. Further, paper also presented the importance of repeaters to convert a lumped interconnects model into distribution interconnects model which helps to improve the overall delay of the lumped copper interconnects model. The analytical models for different shapes of repeaters for multilayer distributed interconnect model presented for copper interconnects. It is concluded that performance in terms of delay and power of copper interconnects is better for distributed model as compared to lumped model. CMOS based optimum repeaters of difference sizes and shapes also presented in the paper.

Sakurai *et al*.[7], suggested the estimation of the delay and voltage wave form for distributed RC line. A closed form formula for RC line is derived using boundary conditions. The equations to find voltage slope, transition time, and crosstalk due to coupling capacitance of two lines are also proposed. The formulas for proposed for coupling capacitances are simple and estimated the errors less than 15% for the practical range of parameters. By using these equations, the optimum width can be calculated to minimize a bus RC delay. The trend for future RC delay is also analyzed. It is predicted that RC delays can effectively be reduced for unscaled interconnection. Expressions presented for a crosstalk and coupling capacitance can be used to estimate the leakage of signals in two conducting wires for in VLSI designs.

Kahng *et al.* [8], presented a good and simple approximation of an interconnect line and studied various combinations of first and second moments, from which they incorporated inductance effects while assuming step input when developing their first delay analytical model of RLC interconnects. The developed solutions showed that their proposed analytical delay model estimates are within 25% of the SPICE delays while Elmore delay estimates can vary as much as 50% from the SPICE-computed delays. Also, they found that when a π-model is used, RLC model achieves accuracy better than 3% in delay calculations, which the L-model achieves in 100 segments. For this reason, π-model is often used in SPICE simulations instead of large number of segments as a rational approximation of distributed RC. Sakurai made the first attempt to model the interconnect line by a π-circuit, however the driving transistor was replaced by a simple resistor.

A. Deutsch *et.al [9]*. ,presented the analytical model to evaluate the performance of local, intermediate and long interconnects with technology dependent dimensions. Analytical models are proposed to predicted capacitive coupling, inductive coupling for intermediate interconnects. For global interconnects, the mathematical equations are presented to evaluate the impedance parameters like resistance, inductance and capacitance. Further, the performance in terms of delay, crosstalk, is evaluated using the proposed models for local, and global interconnects at different technology nodes.

Dartu, *et. al.* [12], presented a time varying Thevenin equivalent model used to estimate gate delays of the devices. It proposed to replace the gate with an equivalent circuit model consisting of a linear resister and voltage source. The values assigned to these equivalent components can be determined using empirical factors, leading to a reduction inaccuracy. An RC load can be used as output in case the output load is not purely capacitive. Mostly, RC models are highly inaccurate because there basic functioning is based on assumptions for the transistor operation and simple load models can be used to represent the interconnect wires.

Rajeevan Chandel, *et al*.[29, 40], reported that the main factors to determine the performance of VLSI chip are delay and power. The repeater are inserted to reduce the propagation delay of interconnects. The voltage-scaled repeaters are proposed to separate two sub-section of distributed interconnect model that helps in minimizing delay and power dissipation in case of long/global interconnects lengths. Long length interconnects have larger value of impedance parameter and thus show large propagation delay and power dissipation in propagating signal across the length of interconnect. The analytical results are

simulated for delay for different technology nodes. It has been concluded that by using optimum voltage scaled repeaters, the number of repeaters and thereby, there is decrease in silicon area and therefore lesser heating of the chip.[112, 113]

Adler V. and E.G. Friedman, [31], presented comparative analysis for analytical and simulation results with different types and shapes of repeaters for long interconnects. The repeater design methodology is presented to estimate the delay and power of interconnects with a CMOS inverter as driving transistor and resistive-capacitive (RC) load. Different models have been presented to estimate the optimum number of repeaters and size of an optimum repeater. The results presented a range of error (from 16%-1%) for simulation and analytical models for different RC loads at long interconnect.

Ismail and E. G. Friedman [36], presented a closed form expressions to find the delay of CMOS gate driven, distribution systems for an interconnects. It proposed to include the inductive effect while evaluating the performance in terms of delay for an RLC distribution line. The traditional RC models without considering the effect of inductance can cause a large error up to 35%. The analytical solutions are presented for inserting of repeaters into interconnects line which provides more accurate results compared to numerical solutions. In accuracy in the results with repeaters will increase upto 30% for RC model as compared to RLC models. For deep submicron technology nodes, the interconnects parasitic are the dominate factor over gate parasitic. Therefore, incorporating inductance into an interconnects impedance models for delay estimations will be more important for deep submicron technology nodes. [114].

P.J. Burke *et. al [3],* proposed the revolutionary work on delay modeling of SWCNT is based on Luttinger liquid theory, for its equivalent circuit as transmission line. Since then, sufficient number models for the SWCNT bundle interconnects have been reported in literature. In case of MWCNT interconnects, early research proposed that only few outermost shells of bundle can contributes to current. Bur recently, it has been proposed that with an end contact method, all the shells of MWCNT bundle can efficiently be contacted to the electrode so that all shells of bundle can contributes to current.

M. S. Satro *et. al [51]*, proposed, a single conductor equivalent model for the MWCNT bundle to estimated the analytical delay and wave shape, which was later extended to the SWCNT bundle interconnects. The mathematical model is presented to convert the

equivalent circuit model of MWCNT bundle into a single conductor transmission line. The optimum number of repeaters and optimum size of repeater is proposed in the paper. In literature [51], it is also proposed that MWCNT bundle interconnects are more suitable for intermediate and global interconnects.

2.3. CNT as VLSI interconnects

The traditional copper interconnects used as VLSI interconnects has some severe challenges for interconnects delay and power in deep submicron technology nodes. Therefore, for long interconnects, carbon nanotubes (CNTs) are considered as an alternative for VLSI integrated circuits due its extraordinary thermal and electrical properties at deep submicron technology nodes. Several research papers in the literature have been suggested, CNT as alternative material for VLSI interconnects.

Li *et al*. [26], presented the comparative analysis of resistance, inductance and capacitance of CNT and copper and CNT interconnects. A comparative analysis in terms of delay ratio is presented for CNT and copper interconnects at semi-global and global level interconnects and proposed that the delay ratio of CNT to copper interconnect is more than unity for local level interconnects, but there is sharp decrease in the ratio as the length increases toward the semi-global and global level. In addition to this, the paper also discussed the key issues like small form factor and skin effects, related to passive device and chip packaging at deep submicron technology nodes.

Kyung-Hoae Koo*, et. al*. [44], Proposed that CNT interconnects and optical interconnects has potential to replaced the traditional copper interconnects for global interconnects and CNT interconnects can be the alternative option for local interconnects. The performance comparison of CNT and copper in terms of latency, bandwidth and power dissipation at deep submicron technology levels suggested that CNT can outperform the copper. The performance advantage of CNT bundle can be further extended by reducing the aspect ratio and electromigration. Therefore, lower wire capacitance can also be achieved in CNT. This trend is studied for scaled down technology nodes and found the improved performance in favor of CNT. Further, the work is also extended for optical interconnects for long wires.

Naushad Alam *et al*.*[65]*, investigated the applicability of SWCNT bundle as VLSI interconnects for future VLSI applications. It presented the effect of bundle density and tube diameter of an SWCNT bundle interconnects. It is shown that as tube diameter increases, the

resistance of an SWCNT bundle decreases (if number of SWCNTs in a bundle remains constant). The intrinsic resistance of an isolated tube is very high, hence the SWCNT bundle interconnect for local interconnects has higher resistance compared to copper interconnects. The resistances of intermediate and global level interconnects of SWCNT bundle are smaller compared to copper interconnects at deep submicron technology nodes. At deep submicron technology nodes (<45nm), the MFP of copper is around 40nm which is less than the cross section dimensions of technology node. Therefore, for intermediate and global interconnects SWCNT bundle interconnects can outperform the copper interconnect.

A. Naeemi *et al*. [72], presented the physical models for SWCNT and copper interconnects at different nano-scaled technology nodes are presented. At nano scaled technologies, copper interconnects suffered from many severe problems like surface scattering and grain boundary scattering, which increase the resistance of copper interconnects and reduces its speed. Most of the global interconnects lengths used as clock, power supply and ground lines required high current density, introduced electromigration. Where in CNT, show ballistic flow of electrons with long MFP in microns compared to copper (45nm). A single walled carbon nanotube has high parasitic parameters; hence SWCNT bundle structures are proposed as suitable structures for VLSI interconnects. Further, the performance in terms of delay of SWCNT and copper as interconnects are compared. It is concluded that the SWCNT interconnects provided the ultimate performance and compared them with minimum-size copper interconnects implemented at various technology nodes. It is also concluded that CNTs are always better candidate for VLSI interconnects for nano-scaled technology nodes.

Srivastava *et al*.[76], presented the applicability of SWCNT interconnects for nano-scaled technology nodes. The analytical model presented to evaluate the impedance parameters of SWCNT interconnects which included the physical parameter and contact resistance for different interconnects length. A comparative analysis is presented in terms of power and delay to understand the performance of SWCNT bundle and copper interconnects for local, semi-global and global interconnects at 32nm and 22nm technology nodes. It is concluded that there is 30%-40% improvement in terms of delay for SWCNT bundle interconnects compared to copper interconnects for global interconnects. The performance of SWCNT bundle interconnects also compared with copper interconnects for local interconnects. It is concluded in the paper that SWCNT bundle gives the better performance for local, intermediate and global interconnects particularly at nano-scaled technology nodes.

Steinhogl, W *et al*. [93], discussed the impact of small structures on copper interconnects. The analytical models are presented for copper interconnects which show that the resistivity of copper interconnects increase when its dimensions are scaled down. The impact of cross-section dimensions on the resistivity of copper, the affects of grain boundary scattering and surface boundary scattering mechanism, had been discussed in detail. The comparison of resistivity for different technology nodes from 100nm to 32nm is presented It is also observed as cross sectional dimensions are 45nm or below, the resistance of copper interconnects sharply increased and influenced the performance in terms as delay of copper as interconnect.

Mayank Rai and S. Sarkar [94], studied and presented the influence of tube diameter of SWCNT bundle on delay and power and compare the results with copper interconnects. SWCNT bundle interconnects has high current density compared to copper and hence it can conquer electromigration. Due to this SWCNT bundle is more suitable for 32nm technology and below. In SWCNT bundle interconnect, with increase in nanotube diameter the inductance and resistance increases. It is shown that for high-speed applications inductive an effect has a negligible role to analyze the performance for an SWCNT bundle interconnects. But at the same time, as the diameter of naotube increases, the capacitance of SWCNT bundle interconnects decreases. With increase in nanotube diameter, the increased resistance leads to increase the power dissipation and propagation delay where the reduced capacitance leads to reduce the propagation delay and power dissipation. Therefore it is proposed there is need to choose optimum tube diameter for optimum delay and dissipation.

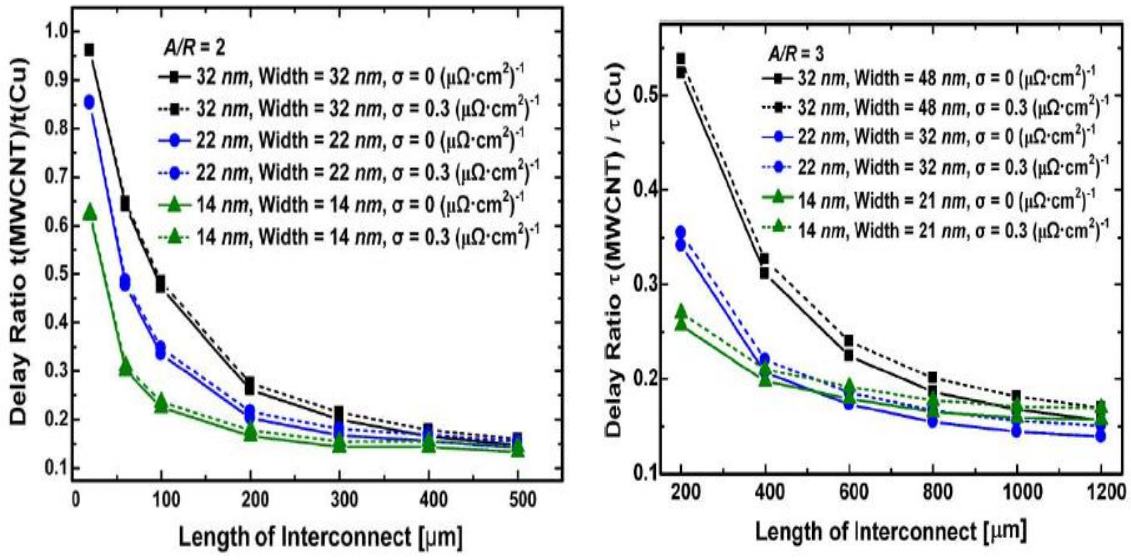
Massoud *et al*. [115], analyzed the performance of the CNT interconnects at local, intermediate and global level. The simulated results are presented for CNT interconnects for different technology nodes and compared with the copper interconnects for intermediate and global interconnects. It is concluded in the paper that CNT interconnects are more suitable candidates as compared to copper, for intermediate and global interconnects at submicron technology nodes.

2.4. MWCNT bundle as Interconnects

MWCNT bundle have of large diameter and large number of conducting channels and long MFP. Although. SWCNT and MWCNT have same current carrying capacity but MWCNTs are easier to fabricate as compared to SWCNTs because of its better control on the growth process. These advantages make it more suitable candidate for future VLSI interconnects as

compared to SWCNT and hence most of the research has been focusing to analyze the performance of MWCNT based interconnects for nanoscaled technology nodes.

H. Li *et al* [27], presented MWCNT bundle interconnect as an alternative material for future VLSI integrated circuits design. MWCNT has large diameter and long MFP for its each shell which increased the conductivity of the bundle. A complete equivalent distributed RLC model of MWCNT interconnects has been presented. The performance of MWCNT interconnects estimated on the basis of proposed equivalent model and compared with copper and SWCNT interconnects, for different interconnect lengths at 32nm, 22nm and 14nm technology nodes.



(a) **(b)**

Figures 2.1: (a) and (b) Comparative analysis in terms of delay ratio for MWCNT and copper interconnects for different interconnects lengths at different technology nodes for intermediate (A/R=2) and global (A/R=3) interconnects respectively[27].

It is shown in the results that for intermediate and global interconnects, the delay in case MWCNT bundle interconnects is less as compared to copper interconnects as shown in Figures 2.1(a) and (b). In both the cases (for AR=2 and 3), there is improvements in the delay ratio of MWCNT/copper for increasing interconnects length. At intermediate interconnects (or 500-μm) and global interconnects (>1000-μm), the delay ratio is less than 0.2 in favor of MWCNT interconnects at 14nm technology node. It is also shown that MWCNT bundles can outperform SWCNT interconnects for long interconnect length at deep submicron technology nodes. Moreover, MWCNTs are easier to fabricate as compared to SWCNT because of less

concern about chiralty control. Therefore, MWCNT interconnects can be attractive alternative for interconnects for VLSI design at nano scaled technology nodes.,

Srivastav Ashok *et al.* [63], investigated the performance one dimension fluid model of MWCNT bundle interconnects and compared with the traditional copper interconnects in very-large-scale integration (VLSI) circuits for global interconnects at different set of frequencies. The theoretical model is verified using SPICE simulation tool through a CMOS inverter pair and interconnects length. The result show that delay and power dissipation for CNTs interconnects is small as compared to copper interconnects for 22 nm and lower technology nodes. The study suggested that copper interconnects can be replaced with the MWCNT interconnects for nano-scaled CMOS technologies nodes.

B.K. Kaushik *et al*.[80], analyzed various the performance of different configurations for mixed-MWCNTs bundle with similar and different numbers of shells. It is observed that the proposed mixed structures are offered 15% lesser delay as compared to MWCNT and copper interconnects. Further, the crosstalk is reduced by 29.59%, for the mixed MWCNT bundle as bundle with SWCNT bundle and copper interconnects for different interconnects at different technology nodes. A comparison between resistances of MWCNT and copper interconnects for different technology nodes and SWCNT bundle with different chirality is shown. It is shown in the results that at semi-global and global levels interconnects, the MWCNT bundle interconnects can outperform in terms of propagation delay compared to copper interconnects and it improves its performance with scaled down technology and long interconnects lengths.

Hong Li *et al*. [116], presented the influence of high frequency signal on the performance of CNT due to existence of high on-chip inductance. It is shown in the paper that the influence of the skin effect at high frequency on CNT is lesser compared to copper and hence CNT as interconnects may be more suitable for high frequency application. Further, it is proposed that there is reduced skin effect in MWCNT bundle compared to SWCNT, make it more suitable candidate for high frequency IC design. Therefore, with large-diameter and large interconnects length MWCNT interconnects may become a strong alternatives for future high frequency interconnects applications.

H. Li *et al.* [117], proposed applicability of MWCNTs as an interconnect candidate in future VLSI design. The performance of MWCNTs interconnect simulated and compared with copper interconnects as well as SWCNTs. From the comparison, MWCNT interconnects

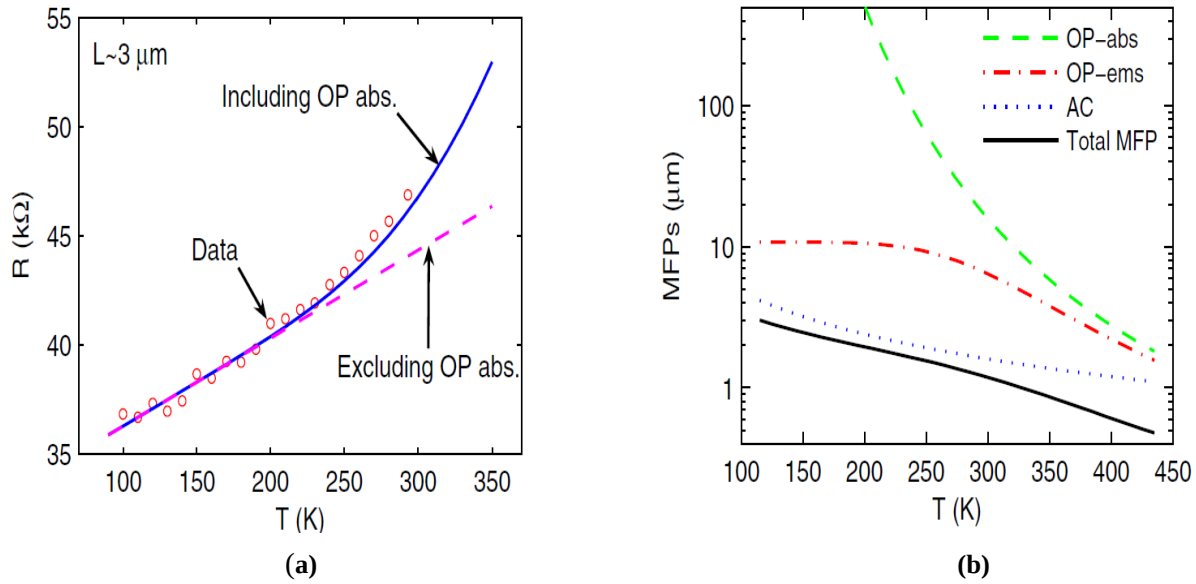
show significant improvement in signal delay as compared to copper wires. It was also predicted that better improvement can be achieved for technology scaling.

2.5. Influence of Temperature on SWCNT and Copper interconnects

The influence of temperature variations has large impact on the performance of high performance VLSI integrated circuits. The temperature variations have a significant effect on the electron surface and grain boundary scattering mechanism in SWCNT and copper interconnects. This temperature dependent scattering mechanism influences the performance of interconnects in terms of delay and power for VLSI interconnects. Therefore, the influence of thermal variation on the performance in terms of delay and power needs to be investigated for interconnects. A few research papers in the literature have been included the impact of temperature in proposed models and presented the results upto local interconnects.

Amir Hosseini *et al* [52], presented thermally-aware model for single-walled carbon-nanotube (SWCNT) based interconnects. The model presented the temperature-dependent electrical impedance model by considering different scattering mechanisms and the expressions for its temperature dependent impedance parameters for an individual shell of SWCNT. The simulation results in the paper revealed that, SWCNT-based interconnects compared to copper, offered more than 5 times reduction in delay at interconnects length of about 10–20 nm (local interconnects) for 27– 127ºC temperature range. It is also concluded that SWCNT can easily replace conventional copper and also proves to provide high performance in terms of delay for VLSI interconnects.

Pop. Eric *et al*. [103-105], presented the electrical and thermal transport phenomenon in metallic SWCNTs on insulating substrates, under a wide range of temperature and bias conditions. Various temperature dependent factors are considered while developing the temperature dependent impedance model for SWCNT. The results presented in the paper show that the rise in temperature from 200K-450K influences the MFP and resistance of SWCNT as shown in Figures 2.2(a) and (b) respectively. It concluded from the results that as temperature increase from 200K to 450K, the total MFP of SWCNT is decreasing and hence resistance is increasing for local interconnects.



(a) **(b)**

Figures 2.2: (a) and (b). Temperature dependent resistance and MFP for 3µm interconnect length at 32nm technology node [102].

It is shown in the paper that the temperature dependent total MFP of SWCNT is depending upon the various phonon scattering phenomenon (acoustic and optical and zone boundary scattering). It is revealed from the results that SWCNT bundle interconnects have significant potential to replace traditional copper interconnects for moderate to high temperature application at 32nm technology nodes and below.

Azad Naeemi *et. al.*[106], introduced metallic SWCNT bundle interconnects as an emerging material for VLSI interconnects IC. The effect of temperature on impedance parameters of SWCNT and copper is analyzed. The delay analyzed for 22nm technology node and it is reported less for SWCNT, which considering it a suitable candidate for excellent thermal strength at elevated temperatures.

Andrea G. Chiarillo, *et al.*[118, 119], presented the influence of temperature on the performance of SWCNT and copper interconnects. An accurate electrical equivalent circuit model has been presented which included the effect of temperature and size for copper interconnects and SWCNT interconnects. Further, the simulation results show that with rise in temperature the delay is increased of copper and SWCNT interconnects.

Pierre Gautreau *et al.*[120], presented, the affect of hot phonons on Joule heating is studied. It is shown in the paper that Joule heating is directly influenced with increased in scattering rate of hot phonons in SWCNT. It is shown that the absorption scattering rate is lower than

the emission scattering rate of an emission mechanism. The Joule heating is increased in emission which is directly translated to energy transfer to the lattice of the SWCNT interconnect. The applied electric field is responsible to Joule heating for hot phonon contribution, while at higher electric field this contribution becomes independent of applied electric field. The electrons usually drift further away from the sub band's bottom, where the scattering changes at a much smaller rate at higher temperatures. It is shown that the Joule heating of SWCNTs due to scattering of hot phonons exhibit non-linear behavior with respect to time.

Wen Chao Chen, *et al*.[121],presented electro-thermal effect of metallic SWCNT. The impact of temperature is analyzed for low and high bias with temperature variation for SWCNT. The effect of temperature is investigated and concluded that the thermal effect can influence the signal propagating through SWCNT as interconnects in terms of propagation delay. It is also concluded that the influence of temperature must be taken into consideration while designing high performance ICs.

2.6. Gaps in Present Study

From literature survey, it is concluded that the resistance of copper interconnects increases sharply as the cross-section dimensions of technology nodes scaled down than its MFP (<45nm). In deep submicron technology nodes (<45nm), the combine effect of grain boundary scattering and surface scattering reduces the conductivity of copper.

Recent studies suggested that the CNT based interconnects has a potential to become an alternative for future interconnects. In the literature, few studies have been investigated the influence of temperature on impedance parameters for SWCNT interconnects. The simulated work reported in literature for temperature dependent SWCNT interconnects is restricted up-to local interconnects only where as SWCNTs interconnects can also outperform the traditional copper interconnects for long interconnects as well. Therefore, temperature dependent work for SWCNT and copper interconnects needs to be extended for long interconnects to evaluate the performance of SWCNT and copper interconnects in terms of delay and power.

Further, it is also concluded in the literature that MWCNT bundle interconnects can perform better than its counterparts i.e. SWCNT bundle and copper interconnects for global length interconnects. MWCNTs bundle interconnects cannot only outperform SWCNTs bundle

interconnects in terms of its performance, but also it is easier to fabricate with less concern about chirality and density control. Therefore, it is essential to propose the temperature dependent impedance model to evaluate the performance of MWCNT bundle interconnects in terms of delay and power at global interconnects. In addition, a temperature dependent comparative analysis is required to understand the performance in terms of delay and power for MWCNT bundle, SWCNT bundle and copper interconnects for nano-scaled technology nodes at global level interconnects.

2.7. Objectives of Proposed Work

Based on the initial studies, literature survey (as reported) and the understanding established the following objectives are included in the study:

1. Development of temperature dependent equations of RLC for MWCNT interconnects.
2. Analysis of effect of temperature on delay in MWCNT interconnects.
3. Analysis of effect of temperature on power dissipation in MWCNT interconnects.
4. Comparison of the results obtained from the above analysis with results for Copper-interconnects and SWCNT-interconnects.

2.8. Research Methodology

The methodology for the work to be done for the proposed PhD proposal will have the following constituent components.

- Development of a temperature dependent modal for Copper interconnects.
- Development of a temperature dependent model for MWCNTs interconnects.
- The accuracy of the approach will be ascertained by comparison with SPICE simulation results.
- Comparison of temperature dependence of MWCNT, Copper and SWCNT interconnects.
- Analysis and conclusion.

3 TEMPERATURE DEPENDENT EQUIVALENT CIRCUIT MODEL OF MWCNT BUNDLE

This chapter explores the impact of temperature on scattering mechanism of Multi-Walled Carbon Nanotubes (MWCNT). With the help of extensive mathematical computations, the temperature dependent equivalent circuit model is presented for MWCNT bundle, SWCNT bundle and copper interconnects

3.1 Introduction

The primarily demands for Very Large Scale Integration (VLSI) industry are to design the high performance, faster and small in size integrated circuits. However, few important issues like high current densities and variable thermal operating conditions reduce the reliability of an Integrated Circuit (IC). The thermal variations are one of the most important factor under considerations for VLSI industry with scaled down technology and high packing densities of the integrated circuits. Due to large variations of the process parameters for deep submicron technology nodes, thermal environment conditions can seriously limit IC operations and responsible for most of the IC failures. So, temperature dependent electronic circuits need to be analyzed thoroughly. To understand the influence of temperature variations and the reliability of industrialized process is necessary for the successful working of any electronic circuit. [21, 79, 122]

High performance VLSI circuits have great inconsistency to operate under variable thermal environment conditions ranging from 200K to 450K [123]. These large thermal variable conditions have a considerable effect on the performance of interconnect in terms of propagation delay and power dissipation of signal passing through it. Hence, the performance of an interconnect material can be understood by analyzing different temperature dependent parameters of the interconnect material which can affect its performance. This chapter presents the mathematical equations for temperature dependent impedance parameters like resistance for MWCNT bundle interconnect those changes due to

variation in the temperature above room temperature. Several factors which need to be included those occur in MWCNT, when temperature is above room temperature under thermal variation conditions[52]. These temperature variations affect the electron surface and grain boundary scattering mechanism in MWCNT bundle interconnects. The scattering mechanism in MWCNT consists of two types of scattering: 1) electron-electron scattering mechanism and 2) electron-phonon scattering mechanism. The electron-phonon scattering mechanism plays a vital role, where electron-electron scattering has negligible effect for the scattering in MWCNT. The temperature dependent scattering mechanism variation has significant effect on the MFP of MWCNT and hence influences the impedance parameters of MWCNT[108]. This change in impedance parameters affects the performance in terms of delay, power and PDP of MWCNT bundle interconnects. The purpose of this chapter is to examine the effect of temperature on the scattering mechanism and presents the temperature dependent impedance model for global interconnects of MWCNT bundle interconnects.[52, 104, 122, 124-127]

3.2. Temperature Dependent Equivalent Electrical Circuit model for MWCNT

MWCNT bundle with several shells like SWCNTs concentrically nested with varying diameter inside one to another, as shown in Figure 3.1. The different shells of the MWCNT bundle have different diameters and vary from few nanometers to hundreds of nanometers depending on the technology nodes. The diameters of the outermost shell and innermost shell of MWCNT bundle are D_{outer} and D_{inner}, respectively. The center of MWCNT bundle is separated from the ground plane with a distance *Y*. The spacing between two adjacent shells MWCNT bundle may vary from *0.3nm to 0.4nm* for different configurations. The small adjacent distance leads towards to increase inter-shell capacitance which may effects the average power consumption of interconnects, whereas the large inter-shell distance increases the overall resistance of the bundle and effects the propagation delay. The work presents in the thesis has considered the distance of adjacent shells is equal to $\delta \approx 0.34nm$ (van der Waals distance). [27]

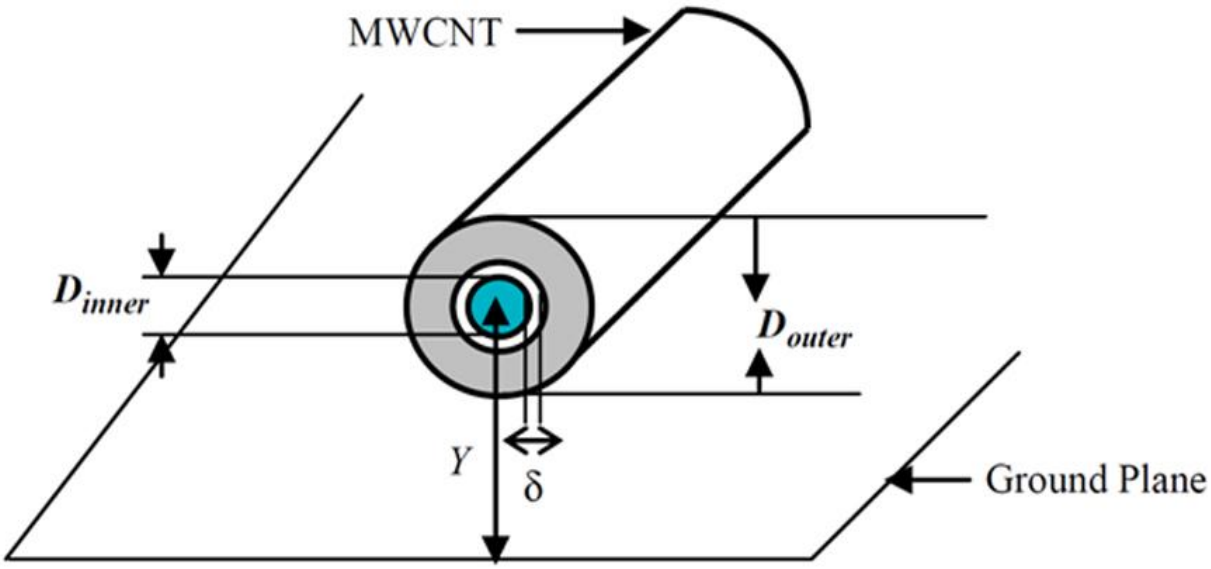


Figure 3.1: Structure of MWCNT bundle on a ground plane [19].

3.2.1. Number of Shells and Channels

The number of shells in a bundle are counted from outermost shell to innermost shell as *1, 2,.,i...n*. The number of shells for MWCNT bundle depends upon the outermost diameter of bundle and diameter ratio of the bundle. The diameter ratio is defined as the ratio between the diameters of outermost shell to innermost shell of MWCNT bundle and given as D_{inner}/D_{outer}. *[27]*. The diameter ratio may vary for different MWCNT bundles and may have range between *0.35* and *0.8*.

The outermost shell of MWCNT bundle is technology dependent parameter and diameter ratio (D_{inner}/D_{outer}) considered for this work is *0.5*. Therefore, total *n* number of shells in a bundle can be calculated as

$$n = 1 + \text{int}\left[\left(\frac{D_{outer} - D_{inner}}{2\delta}\right)\right] \qquad (3.1),$$

where int {.} represents the integer part which is to be considered for evaluation. These shells of a bundle are numbered from outermost shell to innermost shell as *1, 2,..i..n*. Each shell of MWCNT bundle have different diameter, hence the diameter of any i^{th} shell of a bundle can be calculated as[27]

$$D_i = D_{outer} - 2\delta(i-1), \quad for 1 \le i \le n \tag{3.2}$$

Each shell of MWCNT bundle consists of different number of conducting channels and these conducting channels are diameter dependent. The conducting channels for a shell having diameter less than 3nm are approximately considered equal to *2* and shells having diameters more than 3nm are diameter dependent. Therefore, conducting channels of any i^{th} shell of MWCNT bundle can be given as [27]

$$N_{\frac{chan}{i^{th}shell}} \approx 2, \qquad for\ D_i < 3nm \tag{3.3),}$$

$$N_{\frac{chan}{i^{th}\ shell}} \approx a.D_i + b, \quad for \quad D_i > 3nm \tag{3.4}$$

Where D_i is the diameter of i^{th} shell, a=6.12x 10^{-4} 1/(nmK) and $b=1.275$.Hence, each shell of a MWCNT bundle have different conducting channels[27]. Therefore, the total number of conducting channels $(N_{chan/bundle})$ of MWCNT bundle is the sum of the conducting channels ($N_{\frac{chan}{shell}}$) of all the individual shells and given by

$$N_{chan/bundle} = \sum_{i=1}^{n} N_{chan} / i^{th} shell \tag{3.5}$$

3.2.2. Temperature dependent RLC Circuit Model for an Individual Shell of MWCNT bundle

Based on different interconnect impedance parameters of an individual shell such as resistance, capacitance and inductance, the temperature dependent equivalent impedance model for an individual shell of MWCNT is shown in Figure 3.2.

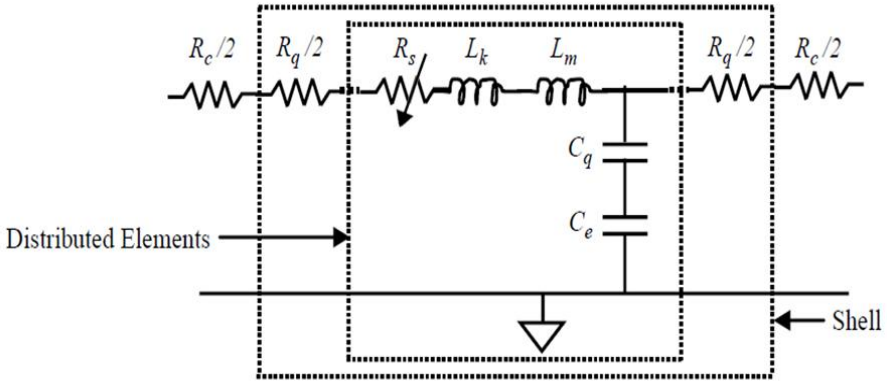


Figure 3.2: Temperature dependent RLC model of i^{th} shell of MWCNT [27].

3.2.3. Temperature Dependent Resistance (R_{shell}) of i^{th} shell

The equivalent resistance of an individual i^{th} shell of MWCNT bundle can be categorized into three resistive components: electron-phonon scattering dependent resistance (R_s) (considered in case when the length of interconnects is more than its MFP, quantum resistance (R_q) and imperfect metal contact resistance (R_c). The imperfect metal contact resistance (R_c) is because of the metal used for contacting with MWCNT and ranging from few ohms to hundred of kilo-ohm for different fabricating processes [27, 52]. It is almost independent from the diameter of the shell and temperature. Therefore the value for the metal contact resistance (R_c) is almost constant and assumed equal to $2k\Omega$ for each shell of MWCNT bundle as suggested in [128]. Hence the temperature dependent resistance for an individual shell is given by

$$R_{shell} = R_c + R_q + R_s.L$$

$$R_{shell} = 2k\Omega + \frac{h}{2e^2N} + \frac{h}{2e^2N}.\frac{L}{\lambda eff\,(T)} \qquad (3.6),$$

where $h/2e^2 =$ 12.9kΩ, N, L and $\lambda_{eff}(T)$ are the number of conducting channels in a shell, interconnect length and temperature dependent effective MFP of an individual shell respectively. It is revealed from Eq. (3.6) that there is an important role of temperature dependent effective MFP in determining the value of resistance of an individual shell of MWCNT bundle. [27, 52]

The effective MFP of an individual shell depends upon the temperature dependent scattering mechanism of MWCNT. The temperature dependent scattering mechanism consists of two

types of scattering i.e. electron-electron scattering and electron-phonon scattering. The impact of electron-electron scattering is negligible small and main contributor to the effective MFP is electron-phonon scattering mechanism for MWCNT interconnects. The electron-phonon scattering mechanism is further divided into two types: acoustic scattering mechanism and optical and zone boundary scattering mechanism for MWCNT as shown in Figure 3.3. Figures 3.3(a), (b), and (c) represent the acoustic phonon scattering mechanism, optical phonon emission process and Zone boundary scattering mechanism, respectively[52, 103-105, 108, 129]

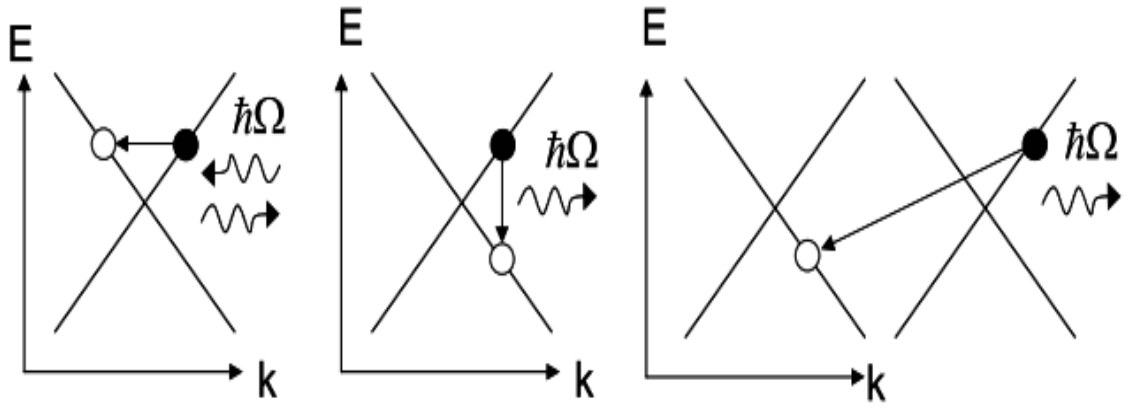


Figure 3.3: (a) Acoustic phonon scattering mechanism (b) Optical phonon emission process and (c) Zone boundary scattering mechanism[108].

Therefore, scattering dependent effective MFP (λ_{eff}) can be given as[52]

$$\lambda_{eff} = \left[\frac{\lambda_{AC}.\lambda_{OZB}}{\lambda_{AC} + \lambda_{OZB}} \right] \quad (3.7),$$

where λ_{AC} is acoustic MFP which is due to acoustic scattering mechanism and λ_{OZB} is optical and zone boundary MFP due to optical and zone-boundary scattering mechanism. For low to moderate temperature i.e. less than room temperature, the acoustic MFP (λ_{AC}) play a key role to influence the effective MFP (λ_{eff}) for MWCNT [52, 108]. Hence, the resistance of MWCNT at low to moderate temperature, generally depends upon the acoustic phonon scattering MFP (λ_{AC}) .The acoustic MFP (λ_{AC}) is directly depending upon the temperature and diameter of MWCNT and can be given as

$$\lambda_{AC}(T) = 890 \frac{T_0 D_i}{T} \quad (3.8),$$

Where T_0 is room temperature (300K), D_i is diameter and T is temperature in Kelvin for corresponding shell of MWCNT [105]. It is observed from the Eq. (3.8) that with rise in temperature, the acoustic MFP (λ_{AC}) reduces and hence decreases the total MFP. At moderate to high temperature (above 300K), the MFP (λ_{OZB}) due to optical and zone boundary scattering mechanism also play a considerable role for effective MFP (λ_{eff}). The optical and zone boundary scattering mechanism can occur in two ways: electron-phonon emission and absorption as shown in Figures 3.3(b) and (c)[52, 105, 108]. In case of high bias condition, the electrons get accelerated due to generated electric field along the MWCNT and increase their kinetic energy.[52, 102] When the electron energy reaches the optical phonon energy level, a phonon will be emitted with energy $\hbar\omega$ ($\hbar\omega \sim 0.16eV$ in case of zone-boundary phonon and $\hbar\omega \sim 0.2\ eV$ in case of optical phonon) [52, 108] . Optical or zone-boundary scattering can take place when an electron acquires the required energy by absorbing another optical or zone-boundary phonon. Therefore, optical and zone boundary MFP (λ_{OZB}) can be written as

$$\lambda_{ozB} = \left[\frac{\lambda_{ozB,\,fld} \cdot \lambda_{ozB,abs}}{\lambda_{ozB,\,fld} + \lambda_{ozB,abs}} \right] \tag{3.9},$$

where $\lambda_{ozB,fld}$ MFP is due to the electric-field acceleration based scattering and can be represented as

$$\lambda_{OZB,\,fld} = \frac{(\hbar\omega - k_B T)}{eV} L + \frac{\lambda_{ozB,300} D_i}{D_o} \frac{N_{ozB}(300)+1}{N_{ozB}(T)+1} \tag{3.10},$$

where $k_B T$ is the thermal energy (k_B is the Boltzmann's constant). The first term correspond to the distance that the electron must travel to reach the phonon emission threshold energy, and the second term represents the distance that the electron travels after gaining the energy before emitting the phonon. $\lambda_{OZB300} \sim 15nm$ is the measured spontaneous effective emission length for diameter D_0 at 300 K [52, 102-105]. MWCNTs with larger diameters have their sub-bands extended to Fermi level that plays important role for its conductance by creating the conducting channels for the flow of electrons [52]. The optical or zone boundary phonon occupied states are defined as the density of states for the final electron state after scattering and is given by

$$N_{OZB}(T) = \frac{1}{[\exp(\frac{\hbar\omega}{k_B T}) - 1]} \tag{3.11}$$

$\lambda_{OZB,abs}$ represents the scattering effect due to absorption of an optical or zone-boundary phonon and can be written as

$$\lambda_{ozB,abs} = \frac{\lambda_{ozB,300} D_i}{D_o} \frac{N_{ozB}(300)+1}{N_{ozB}(T)} \tag{3.12}$$

Therefore, it is revealed from the Eqs. (3.7-3.12) that the effective MFP of individual shells of MWCNT bundle depends upon the temperature dependent, optical and zone boundary scattering phenomenon. Further, this effective MFP, influence the resistance of the individual shell.

3.2.4. Inductance of ith shell

The inductance for a conductor is the energy associated with the movement of electrons carrying current (I) through it. There are two types of inductances in MWCNT bundle i.e. the magnetic inductance and kinetic inductance per unit length [27, 52]. The magnetic inductance is due to the current flowing through MWCNT shell and stored as total magnetic energy in the shell. The magnetic inductance for an individual 'i^{th}'shell is given by

$$L_m = \left(\frac{\mu}{2\pi}\right).cosh^{-1}\left(\frac{2Y}{D_i}\right) \tag{3.13},$$

where μ is mobility of electron, Y is the distance between center of MWCNT bundle to ground level and D_i is diameter of i^{th} shell. The kinetic inductance is due to each conducting channel of MWCNT shell stored in the form of kinetic energy when shell conducts and given as[27]

$$L_{k/channel} = \frac{h}{2\times 2 v_f e^2} \tag{3.14},$$

where v_f is Fermi velocity for carbon nanotubes is usually considered as 8x 10^5 m/s, e is electron charge and h is Planck constant. An individual i^{th} shell of MWCNT consists of N_i numbers of conducting channels and connected in parallel to each other. Hence the effective kinetic inductance of an individual shell can be calculated by

$$L_{k/shell} = L_{k/channel} / N_i \tag{3.15}$$

The mutual inductance in a bundle is due to the coupling between different shells of MWCNT bundle. The shells of MWCNT bundle have large diameters and small thickness,

so each shell can be considered as ideal cylinder with zero thickness. Therefore, the mutual inductance between shells can be estimated around *2pH/μm*. This mutual inductance is negligible small as compared to kinetic inductance of shells; hence mutual inductance is ignored for this work[27].

3.2.5 Capacitance of ith shell

The capacitance in MWCNT bundle is of two types: quantum capacitance (C_q) and electrostatic capacitance (C_e). The capacitance due to quantum electrostatic charge stored in the nanotube when it carries current is known as quantum capacitance (C_q)[27]. The quantum capacitance for a shell is given by

$$C_{q/channel} = \frac{2 \times 2e^2}{h v_f} \approx 193aF/\mu m \quad (3.16),$$

$$C_{q/shell} = C_{q/channel}.N_i \quad (3.17)$$

The electrostatic capacitance (C_e) appear due to charge stored by the outermost shell of MWCNT bundle with diameter D_{outer} and placed above ground at distance *Y*, as shown in Figure 3.1. Hence, the electrostatic capacitance per unit length of shell is given by

$$C_e = \frac{2\pi\varepsilon}{\cosh^{-1}(\frac{2Y}{D_{outer}})} \quad (3.18)$$

The potentials of difference of MWCNT shells cannot be considered to be at same level, which introduces inter-shell coupling capacitance. The inter-shell capacitance (C_s) can be obtained by using the same equation which can be used for coaxial capacitance [27]and given by

$$C_s = \frac{2\pi\varepsilon}{\ln(\frac{D_{out}}{D_{in}})} = \frac{2\pi\varepsilon}{\ln[D_{out}/(D_{out}-2\delta)]} \quad (3.19),$$

where D_{in} and D_{out} are the diameters for inner and outer adjacent shells of MWCNT bundle respectively and $\delta=0.34nm$.

Another effect is tunneling, due to inter-shells conductivity of two adjacent shells in MWCNT interconnects. The inter-shell tunneling conductance per unit length is given as

$$G_t = \sigma.\pi.D_i \qquad (3.20),$$

Where σ is normalized tunneling conductivity at $\delta=0.34nm$ and D_i is shell diameter. The tunneling conductance is depending upon the diameter because there are more atoms in a larger diameter shell and thus tunneling is more likely to take place in MWCNT bundle [27, 128, 130].

3.3. Equivalent Circuit Model of MWCNT Bundle Interconnects

An individual shell of MWCNT has very high resistance hence it cannot be used as individual tube for interconnects. So, concentrically nested several MWCNTs are used in parallel to form MWCNT bundle resulting in net reduction of overall resistance. Based on the above mentioned temperature dependent parameters, temperature dependent equivalent distributed RLC circuit model for MWCNT bundle interconnects is shown in Figure 3.4. In this figure, all the individual shells are considered to be parallel shells.[27]

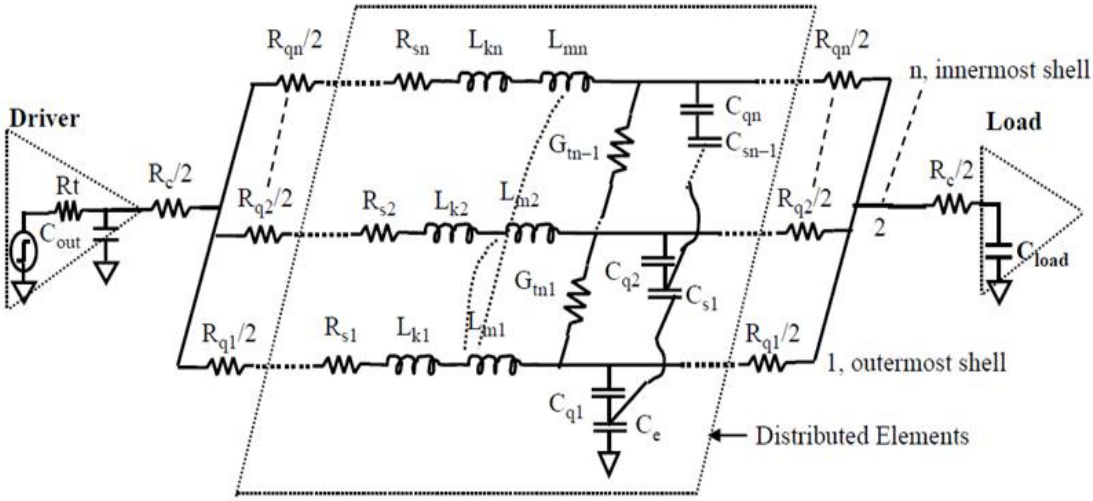


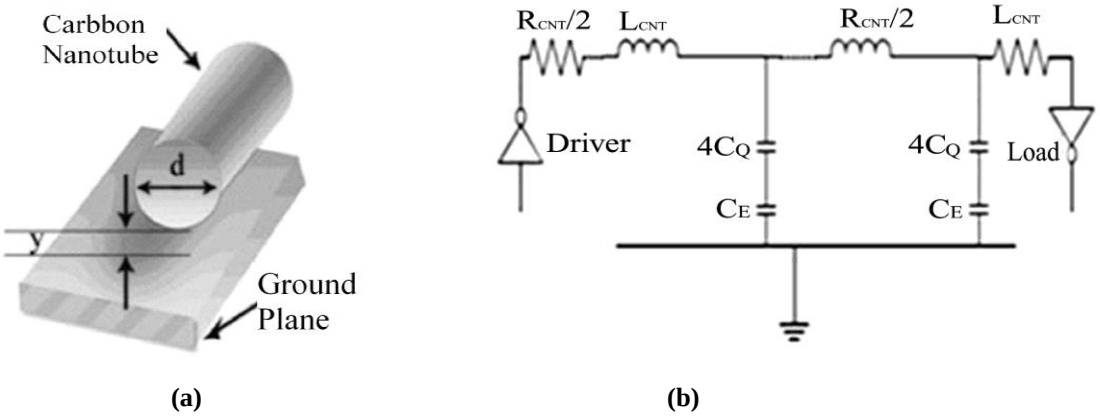
Figure 3.4: Equivalent circuit of a MWCNT interconnects [27].

3.4. Temperature dependent impedance model for SWCNT Bundle

This section of the chapter, presents the temperature dependent impedance models for SWCNT bundle and Copper interconnects.

3.4.1. Temperature dependent impedance model for an individual shell of SWCNT

A SWCNT bundle consists of many cylindrical shaped carbon nanotubes with identical diameter. An individual shell of SWCNT bundle with small diameter (in the range of 1nm to 10nm) has equivalent electrical circuit model which consists of diameter, length and temperature dependent impedance parameters such as resistance, inductance and capacitance[59]. Figure 3.5(a) shows a schematic structure for an individual shell of SWCNT on ground plane. An isolated SWCNT shell with diameter *d*, separated from ground plane with distance *y*. The equivalent RLC circuit model for an individual shell of SWCNT is shown in Figure 3.5(b). The equivalent resistance for an individual shell of SWCNT bundle can be divided into three resistive components: quantum resistance (R_Q) (6.45kΩ), the temperature dependent equivalent electron-phonon scattering based resistance (R_S) (considered when the length of SWCNT is longer than the MFP of SWCNT) and imperfect contact resistance (R_{mc}). The equivalent resistance for an individual shell of SWCNT can be obtained by using the similar way and expressions (Eqs.3.6-3.12) which are used for MWCNT as discussed in the section 3.2.3 of this chapter. The imperfect metal-CNT contact resistance (R_{mc}) leads to increase the shell resistance to its larger value as it is in series with the total shell resistance (R_{shell}) of an individual shell of SWCNT[59, 104]. The imperfect contact resistances are reported from few ohm to hundred of killo-ohms and depends upon the manufacturing process. It is almost independent from the diameter of the shell and temperature. Therefore, it is assumed to be constant and equal to ~24 KΩ [52].



(a) **(b)**

Figure 3.5: Schematic and equivalent circuit of an individual shell of SWCNT interconnects. (a) Schematic structure of individual SWCNT shell on ground plane. (b) Equivalent RLC circuit model of individual SWCNT shell [59].

An individual SWCNT shell consists of two types of inductances i.e. the magnetic inductance and kinetic inductance per unit length. The magnetic inductance is due to the magnetic field of current carrying isolated conductor with some distance from ground plane as shown in Figure 3.5(a).[59] The magnetic inductance for an individual shell of SWCNT is given by

$$L_M = \left(\frac{\mu}{2\pi}\right)\ln\left(\frac{y}{d}\right) \quad (3.21),$$

where μ is mobility of electron and y is the separation between isolated SWCNT to ground. The kinetic inductance is due to the kinetic energy stored in each conducting channel of SWCNT shell when shell conducts and given as

$$L_K = \frac{h}{4N.v_f\, e^2} \quad (3.22),$$

where v_f is Fermi velocity of electron, N is number of conducting channels in a shell, e is electron charge and h is Planck constant.

The capacitance in SWCNT is also of two types i.e. quantum capacitance (C_Q) and electrostatic capacitance (C_E) [59]. The quantum capacitance (C_Q) is due to stored quantum electrostatic charge in the nanotube when it conducts and carries current. The quantum capacitance for a shell is given by

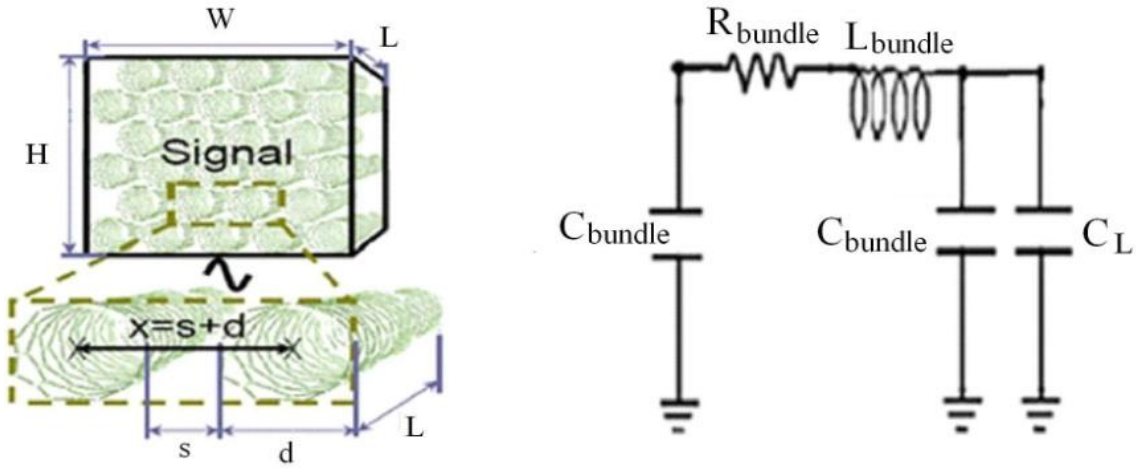
$$C_Q = \frac{4Ne^2}{hv_f} \quad (3.23)$$

The electrostatic capacitance (C_Q) of an individual SWCNT is calculated by considering the SWCNT as a thin conducing wire, with diameter d and placed at a distance y from ground plane as shown in Figure 3.5(a) [59, 94] and given as

$$C_E = \frac{2\pi\varepsilon}{\ln\left(\frac{y}{d}\right)} \quad (3.24)$$

3.4.2. Temperature Dependent Impedance Model for SWCNT Bundle Interconnects

When the parallel combination of such individual SWCNT shells with separation s, used for VLSI interconnects known as SWCNT bundle interconnects and shown in Figure 3.6(a). The equivalent electrical circuit model of SWCNT bundle to a tandem of such RLC circuits is shown in Figure 3.6(b).



(a) (b)

Figure 3.6: (a) Structure of SWCNT bundle with separation of two individual adjacent shells (b) Temperature dependent equivalent RLC model for SWCNT bundle interconnects.[59]

The temperature dependent resistance of SWCNT bundle (R_{Bundle}) with length L, temperature dependent mean free path (λ_{eff}) can be considered as all individual shells of SWCNT as parallel and given by

$$R_{(Bundle)} = \frac{R_Q + R_S.L + R_{mc}}{n_{bundle}}$$

$$R_{(Bundle)} = \frac{\frac{h}{2e^2N} + \frac{h}{2e^2N}.\frac{L}{\lambda eff\,(T)} + R_{mc}}{n_{Bundle}} \qquad (3.25),$$

Where h is Planck's constant, N is number of conducting channels and n_{Bundle} is total number of shells in a bundle.[59] The number of conducting channels in an individual shell can be calculated and given by

$$N \approx a.d + b \qquad for\ d > 3nm \qquad (3.26),$$

where d is the diameter of an individual shell, $a=6.12x\ 10^{-4}\ 1/(nmK)$ and $b=1.275$. If the diameter of an individual shell of SWCNT is less than 3nm than number of conducting channels can be calculated as [59]

$$N \approx 2, \qquad for\ d < 3nm \qquad (3.27)$$

The diameter of each shell of a SWCNT bundle is assumed to be identical and considered to be equal 1nm for the research work. Hence, the conducting channels for each shell are

considered equal to two. Therefore, the total resistance of SWCNT bundle can be re-written as

$$R_{(Bundle)} = \frac{\frac{h}{4e^2}\left(1+\frac{L}{\lambda eff(T)}\right)+R_{mc}}{n_{Bundle}} \quad (3.28),$$

where the total number of SWCNT tubes (n_{Bundle}) in a bundle, depend upon the number of rows ($n_{H(Bundle)}$) and number of columns ($n_{W(Bundle)}$) of the bundle. The total number of SWCNT bundle is also depending upon the parity of number of rows ($n_{H(Bundle)}$) of the bundle. Therefore, total tubes in a bundle for even number of rows is given as[59, 86]

$$n_{Bundle} = n_{W(Bundle)}.n_{H(Bundle)} - \frac{1}{2}n_{H(Bundle)} \quad (3.29)$$

If number of rows are odd than the total number of SWCNT tubes (n_{Bundle}) can be calculated as

$$n_{Bundle} = n_{W(Bundle)}.n_{H(Bundle)} - \frac{1}{2}(n_{H(Bundle)} - 1) \quad (3.30),$$

where number of columns ($n_{W(Bundle)}$) and number of rows ($n_{H(Bundle)}$) for a SWCNT bundle are given as

$$n_{W(Bundle)} = \left(\frac{W-d}{x}\right) \quad (3.31),$$

$$n_{H(Bundle)} = \left(\left\lfloor \frac{H-d}{\left(\frac{\sqrt{3}}{2}\right)x} \right\rfloor + 1\right) \quad (3.32),$$

where *d*, *x*, *H* and *W* are tube diameter, centre to centre separation between adjacent tubes, height and width of bundle interconnects respectively as shown in Figure 3.6.(b).

Hence the total number of SWCNT tubes (n_{Bundle}) in a bundle can be re-written as [59]

$$n_{Bundle} = \left\lfloor \frac{W-d}{x} \right\rfloor \left(\left\lfloor \frac{H-d}{\left(\frac{\sqrt{3}}{2}\right)x} \right\rfloor + 1\right) - \frac{1}{2}\left(\left\lfloor \frac{H-d}{\left(\frac{\sqrt{3}}{2}\right)x} \right\rfloor + 1\right) \quad (3.33)$$

If the number of rows in the bundle is even and

$$n_{Bundle} = \left[\frac{W-d}{x}\right]\left(\left\lfloor\frac{H-d}{\left(\frac{\sqrt{3}}{2}\right)x}\right\rfloor+1\right)-\frac{1}{2}\left(\left\lfloor\frac{H-d}{\left(\frac{\sqrt{3}}{2}\right)x}\right\rfloor\right) \tag{3.34}$$

If number of rows are odd.

The inductance of SWCNT bundle is also considered as parallel combination of inductance offered by individual SWCNT and given by

$$L_{(Bundle)} = \left(\frac{L_M + L_K}{4n_{Bundle}}\right) \tag{3.35},$$

where L_M and L_K are the magnetic and kinetic inductances of an individual SWCNT and are calculated by using Eqs.(3.21) and (3.22)[59].

The total capacitance of SWCNT bundle is the parallel combination of bundle electrostatic capacitance $C_E^{(Bundle)}$ and bundle quantum capacitance C_Q^{Bundle} of SWCNT and can be given by Eqs. (3.37) and (3.38) [59]

$$C_{(Bundle)} = \left(\frac{C_E^{Bundle}.C_Q^{Bundle}}{C_E^{Bundle}+{}^{Bundle}_{Q}}\right) \tag{3.36},$$

$$C_E^{(Bundle)} = 2\left(\frac{2\pi\varepsilon_{ox}\varepsilon_0}{\ln(S/d)}\right)+\left(\frac{W-d-2}{2}\right)\left(\frac{2\pi\varepsilon_{ox}\varepsilon_0}{\ln(\frac{S+W}{d})}\right) + 3\left(\frac{2\pi\varepsilon_{ox}\varepsilon_0}{\ln(S/d)}\right)\left(\frac{n_{H(bundle)}-2}{5}\right) \tag{3.37},$$

$$C_Q^{Bundle} = \left(\frac{2\times 2e^2}{hv_f}\right)n_{CNT} \tag{3.38},$$

where v_f is Fermi velocity and S is distance between adjoining bundles.

3.5. Temperature dependent impedance model for copper Interconnect

The temperature dependent copper interconnects model is presented in this section. The schematic structure used to evaluate equivalent temperature dependent impedance parameters such as resistance, inductance and capacitance for a copper interconnect is shown in Figure 3.7.

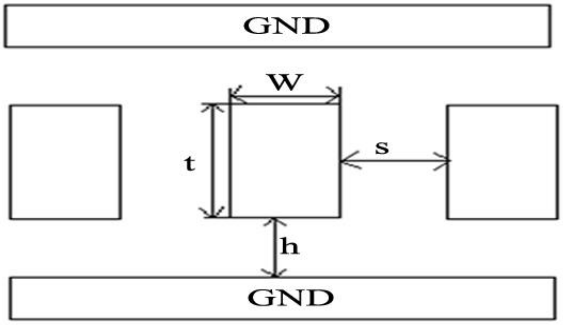


Figure 3.7: Interconnect geometry for copper [59].

3.5.1. Resistance

The resistivity of copper plays an important role to calculate the resistance for rectangular cross-sections interconnects as shown in Figure 3.7. Therefore, the temperature dependent resistance per unit length of copper interconnect strongly depends upon the resistivity as given below [104, 105]

$$R_{Cu} = \frac{\rho(T)L}{W.t} = \frac{\rho_s + \rho_d}{W.t} L \quad (3.39),$$

where, $\rho(T)$ is temperature dependent resistivity of copper interconnect. The resistivity $\rho(T)$ divided into two parts and given as temperature dependent part of resistivity which is related to phonon surface scattering (ρ_s) and temperature independent part is related to defect (ρ_d) and given as[104, 105, 119]

$$\rho(T) = \rho_s(T) + \rho_d \quad (3.40)$$

$$\rho(T) = \rho_0 \left[1 + 0.00401\left(T - T_0\right)\right] \quad (3.41),$$

where ρ_0 is technology dependent resistivity of copper at 300K and value for different technology nodes is given in table 4.1 and $T_0 = 300K$.

3.5.2. Inductance

The inductance of copper interconnects with a rectangular cross-section area can be expressed as [105]

$$L_{Cu} = \frac{\mu_0 L}{2\pi}\left[\ln\left(\frac{2L}{W+t}\right) + \frac{1}{2} + \frac{0.22(W+t)}{L}\right] \quad (3.42)$$

Where μ_0 is the permeability and its value is given as $4\pi \times 10^{-7}$H/m.

3.5.3. Capacitance

The capacitance C_g of the copper interconnect is the capacitance of area and fringe flux to the underlying plane and expressed as

$$C_g = \varepsilon \left[\frac{W}{h} + 2.22 \left(\frac{s}{s+0.7h} \right)^{3.19} + 1.17 \left(\frac{s}{s+1.51h} \right)^{0.76} . \left(\frac{t}{t+4.53h} \right)^{0.12} \right] \quad (3.43)$$

Where C_g is capacitance of per unit length, *W, h, t* are width, height and thickness copper interconnects and s is separation between two interconnects as per interconnects geometry shown in Figure 3.7. ε is dielectric constant for copper interconnect and it is technology dependent.[102-105]

3.6. Chapter Summery and Contribution

This chapter presented the impact of temperature on scattering mechanism of the carbon nanotubes. With the help of extensive mathematical computations, the dependency of temperature on MFP of an individual shell of MWCNT has been obtained so that the impact of temperature on the impedance parameters can directly be obtained. An equivalent temperature dependent RLC model is also presented for global length of MWCNT bundle interconnects. Further, temperature dependent equivalent impedance models are presented for both SWCNT bundle and copper interconnects.

A temperature dependent RLC model is proposed for MWCNT bundle interconnects. The proposed model for MWCNT bundle included the temperature dependent scattering mechanism. The proposed mathematical equations are incorporated the influence of temperature on MFP for MWCNT. Further, the effects of temperature dependent MFP are used to predict the impedance parameters of an individual shell of MWCNT. Based on this approach, a single RLC structure of an individual shell of MWCNT has been proposed and further this model is used to develop the temperature dependent equivalent RLC model for MWCNT bundle. All the individual shells of MWCNT interconnect have been considered as parallel shells for temperature dependent equivalent model for MWCNT bundle. Furthermore, to perform a comparative analysis, temperature dependent equivalent impedance models are presented for both SWCNT bundle and copper interconnects.

4 TEMPERATURE DEPENDENT PERFORMANCE ANALYSIS FOR MWCNT BUNDLE

This chapter presented the temperature dependent, simulated results for MWCNT bundle interconnects for global interconnects length at 32nm, 22nm and 16nm technology nodes

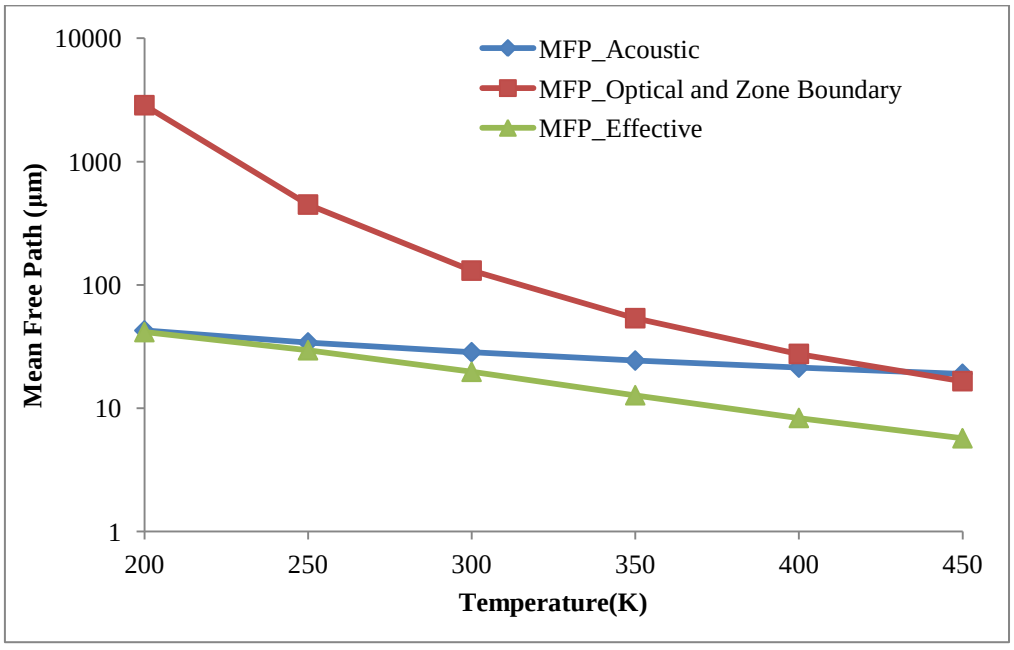
4.1 Introduction

The temperature dependent equivalent circuit model of MWCNT bundle interconnects is presented in chapter 3. The mathematical model suggested that the effective MFP of MWCNT dependents upon the thermal conditions of the Integrated Circuit (IC). This chapter presents temperature dependent performance analysis for MWCNT bundle interconnects. The temperature dependent performance of MWCNT bundle interconnects, in terms of effective MFP, resistance, delay, power and Power Delay Product (PDP) is presented for global interconnects length at 32nm, 22nm and 16nm technology nodes. By using the proposed mathematical expressions, temperature dependent effective MFP of each shell of MWCNT bundle is calculated for temperature range of 200K to 450K. On the basis on proposed temperature dependent impedance model, the resistances of each shell of MWCNT bundle are calculated for global interconnects length at 32nm, 22nm and 16nm technology nodes. The equivalent impedance parameters of MWCNT bundle are obtained by considering all the parameters of individual shells in parallel. Further, the calculated impedance parameters for MWCNT interconnects have been simulated for three different technology nodes to evaluate the performance in terms of delay, power and PDP.

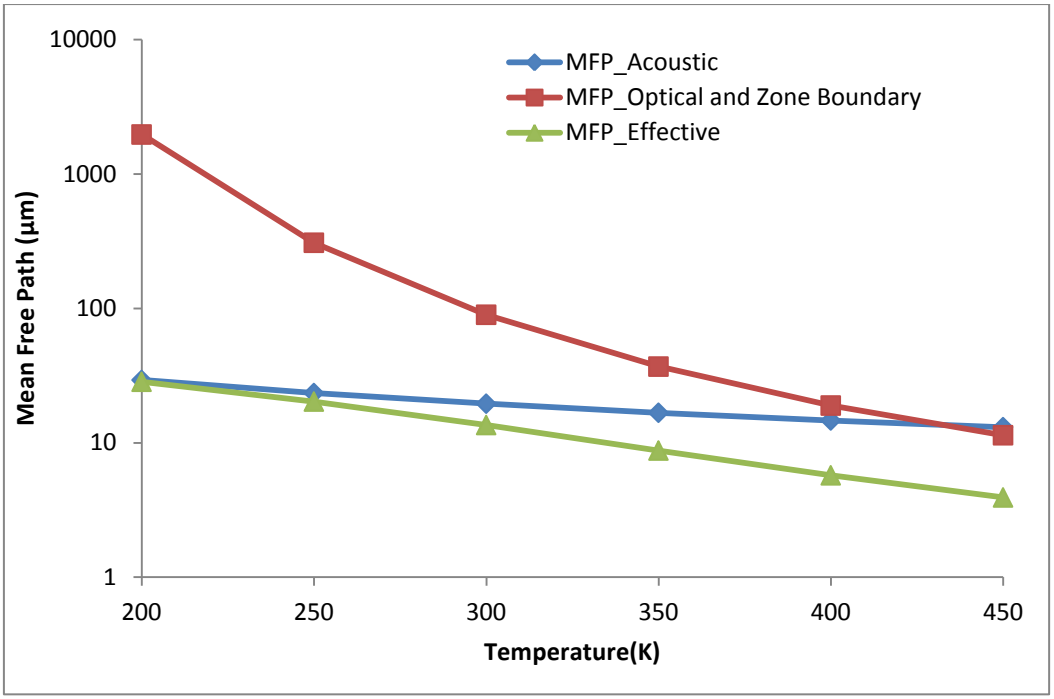
4.2 Temperature dependent impedance analysis for metallic MWCNT

The temperature dependent mathematical model presented in chapter 3 shows the effect of electron-phonon scattering mechanism on the effective MFP of an individual shell of

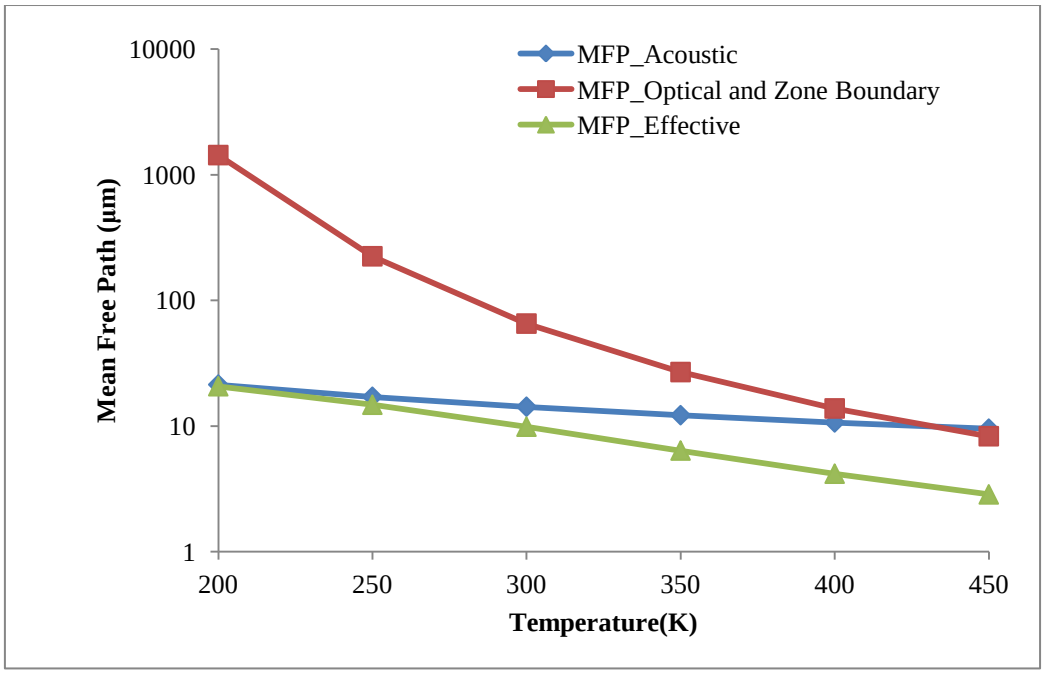
MWCNT bundle under variable temperature range. The temperature dependent scattering mechanism consists of two types of scattering i.e. electron-electron scattering and electron-phonon scattering. The impact of electron-electron scattering is negligible small and main contributor to the effective MFP is electron-phonon scattering mechanism for MWCNT. The electron-phonon scattering mechanism is further divided into two types: acoustic scattering mechanism and optical zone boundary scattering mechanism for MWCNT. The acoustic scattering mechanism dominates for lower temperature range in MWCNT shells for global interconnects and calculated using Eq. 3.8. It is observed from Eq. 3.8 that as temperature increases the acoustic MFP reduces. For moderate to high temperature range optical and zone boundary MFP also play a non-negligible role and calculated using Eqs. 3.9- 3.12. Further, the temperature dependent effective MFP calculated using Eq. 3.7. The effective MFP is calculated for 1mm interconnects length at three different technology nodes i.e. 32nm, 22nm and 16nm. The script for these calculations is written using MATLAB. It is observed from Eqs. 3.7- 3.12 that each shell of MWCNT bundle have different the effective MFP for all the technology nodes. The effective MFPs for all the individual shells are calculated for each technology node under consideration (32nm, 22nm and 16nm). As there are *n* number of shells in an MWCNT bundle (see Eq. 3.1) and therefore *n* number of effective MFPs will also be there for each technology node. Thus, for simplicity the effective MFP for outermost shell of each technology nodes i.e. 32nm, 22nm and 16nm is shown in Figure 4.1.



(a)



(b)



(c)

Figure 4.1: (a), (b) and (c) Temperature dependent acoustic, Optical and Zone boundary and effective MFPs for 32nm, 22nm and 16nm technology nodes respectively

Figure 4.1(a), (b) and (c) show the temperature dependent acoustic, optical and zone boundary and effective MFPs of outermost shell for 32nm, 22nm and 16nm respectively. It is shown in the results that the effective MFP decreases with rise in temperature for all three

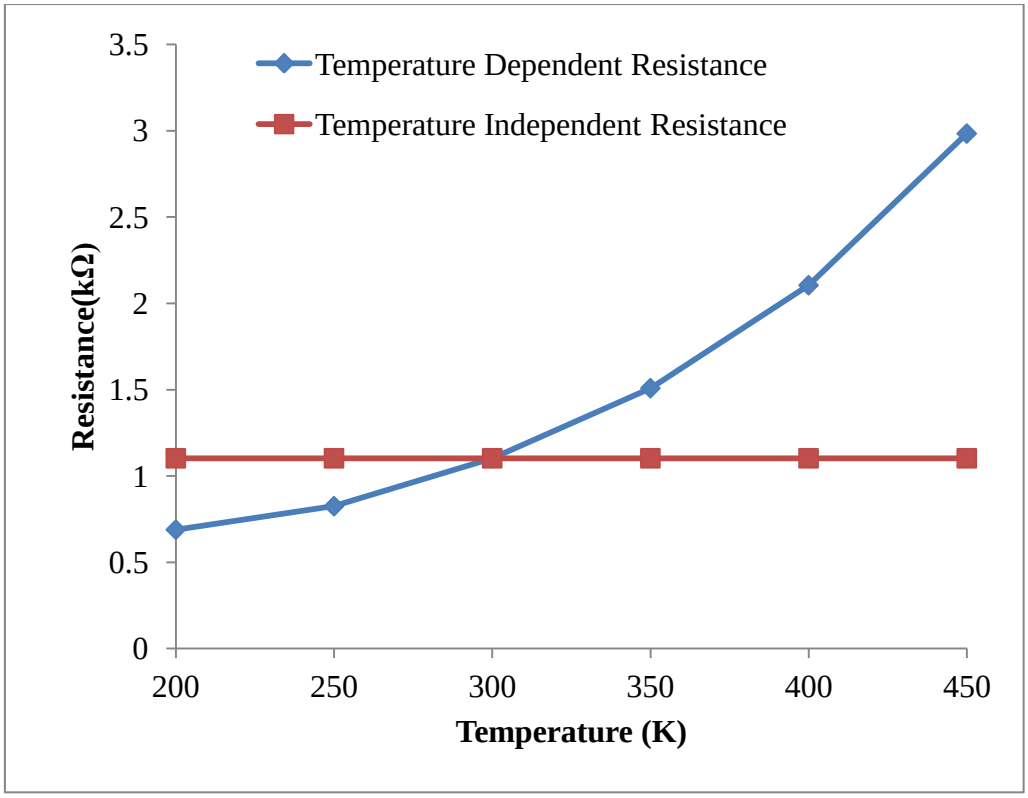
technology nodes. It is revealed from the results shown in Figure 4.1 that for temperature ranging 200K to 300K (low temperature to moderate), acoustic MFP dominates to the effective MFP but as temperature increasing from 300K to 450K (moderate to high temperature), optical and zone boundary MFP also contributes along with acoustic MFP to calculate the effective MFP. The effective MFP sharply decreases at moderate to high temperature as compare to lower side of the temperature range i.e. 200K-300K.

Therefore, it is needed to analyze the influence of temperature dependent effective MFP on the impedance parameters of MWCNT interconnects particularly for higher side of the temperature range. This change in the impedance parameters change the current density and hence affects the performance of the MWCNT interconnects in terms of delay, power and Power Delay Product (PDP). With the calculated effective MFP, the resistance of each shell of MWCNT is calculated using Eq. 3.6. The conducting channels of an individual shell and number of shells in MWCNT bundle at 32nm, 22nm and 16nm technology nodes for 1mm interconnect length (global interconnects) are calculated using Eqs. 3.1 to 3.4. Further, number of conducting channels in a bundle is calculated using Eq. 3.5. All the shells of MWCNT bundle are considered to be metallic shells. The equivalent resistance of the bundle is obtained by considering the resistances of all shells in parallel as shown in Figure 3.4 in chapter 3.

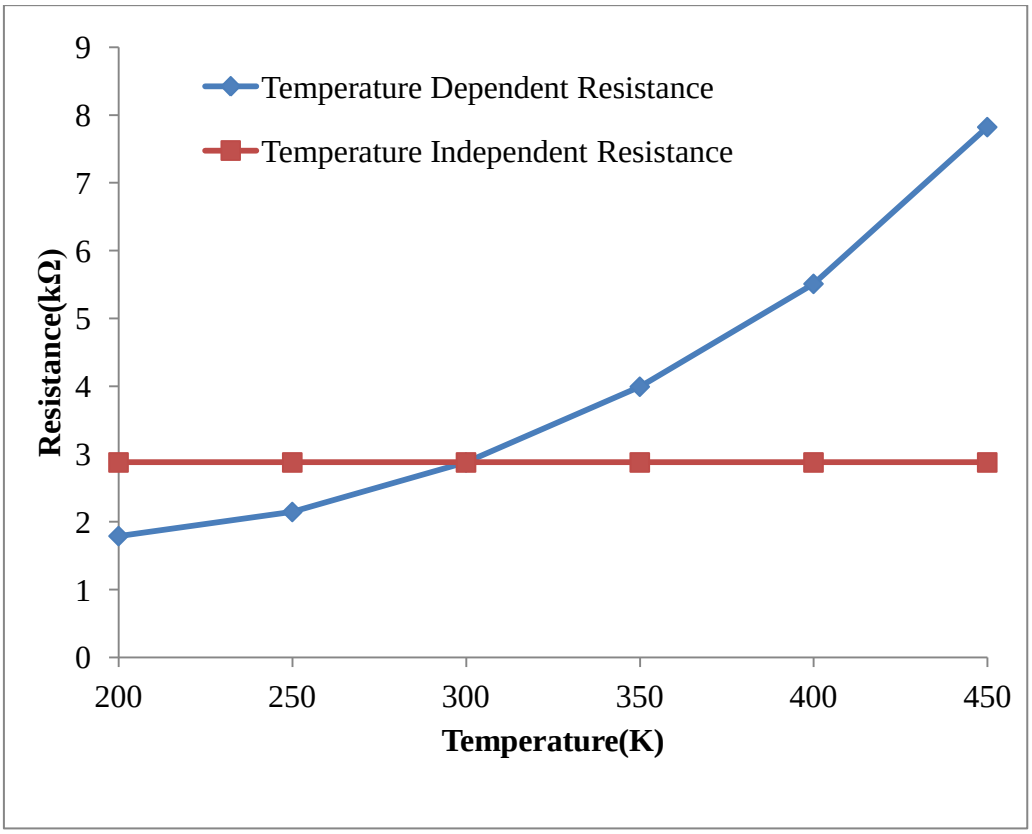
Table 4.1 ITRS 2013 based Simulation parameters for global level interconnects [16]

Technology Node	**32nm**	**22nm**	**16nm**
Width W(nm)	40	28	18
Thickness H (nm)	120	84	54
Aspect Ratio(A/R)	3	3	3
Oxide thickness t_{ox}(nm)	93.6	65.5	40
V_{DD} (volts)	0.9	0.8	0.7
Dielectric constant,	2.77	2.59	2.31
$D_{ratio}(D_{min}/D_{max})$	0.5	0.5	0.5
ρ_o for Cu(μΩ.cm)	3.66	4.2	5.31

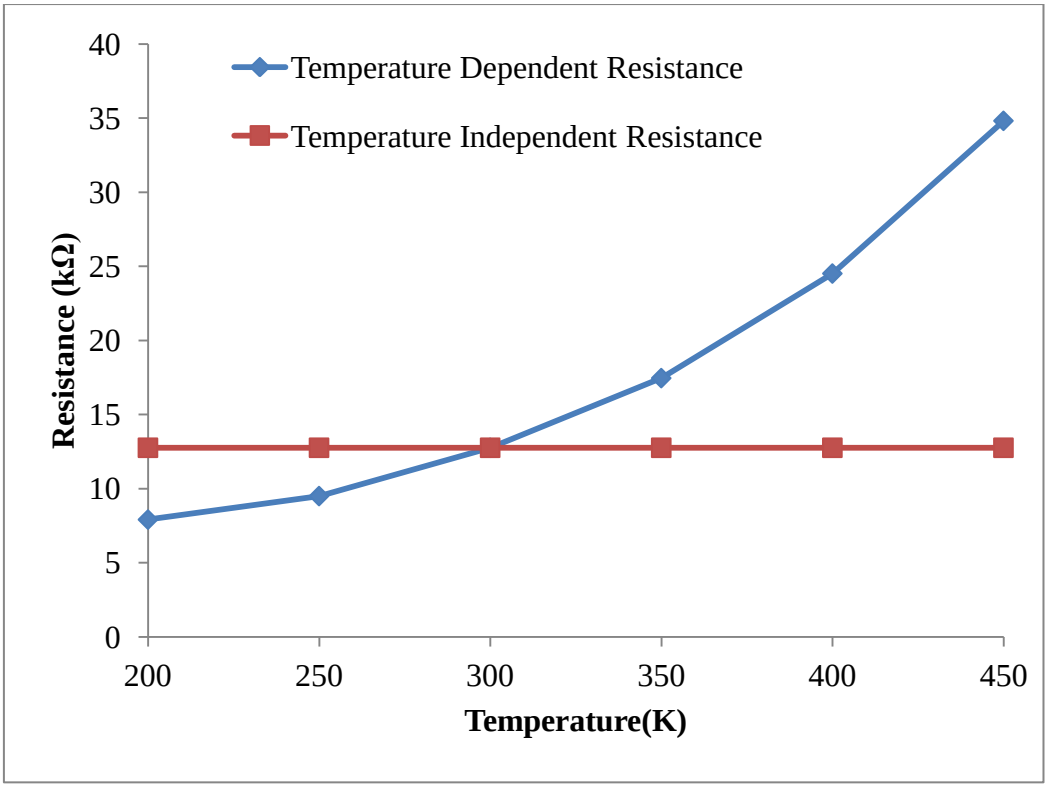
All interconnect parameters used for calculations are obtained from ITRS 2013, as summarized in table 4.1.


Temperature Dependent Resistance
Temperature Independent Resistance
Resistance(kΩ)
3.5
3
2.5
2
1.5
1
0.5
0
200
250
300
350
400
450
Temperature (K)

(a)


Temperature Dependent Resistance
Temperature Independent Resistance
Resistance(kΩ)
9
8
7
6
5
4
3
2
1
0
200
250
300
350
400
450
Temperature(K)

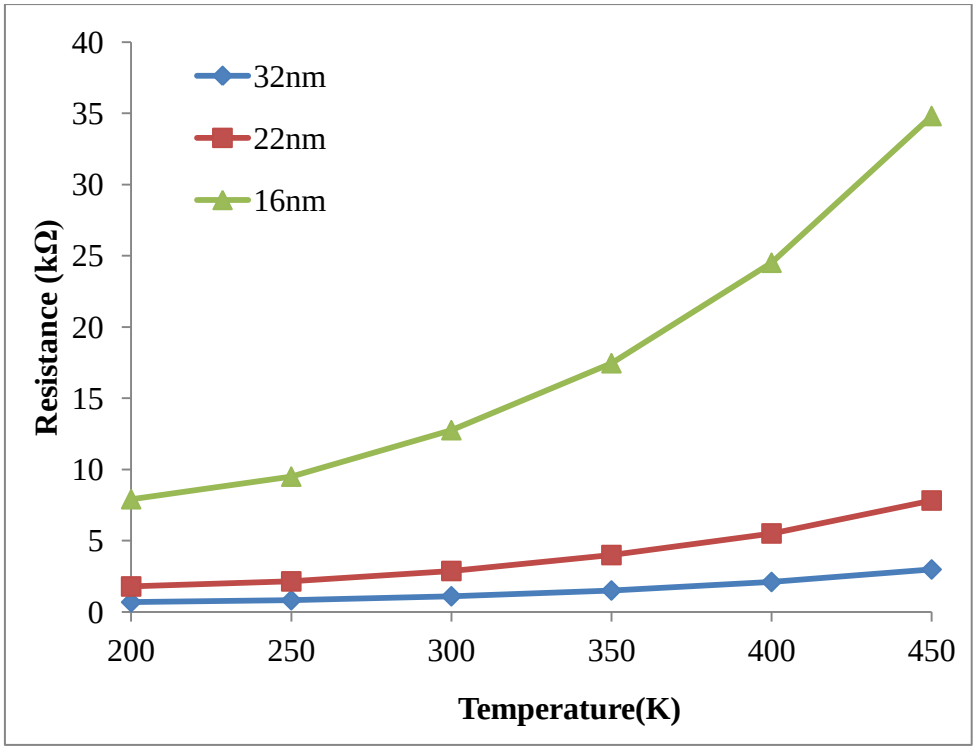
(b)



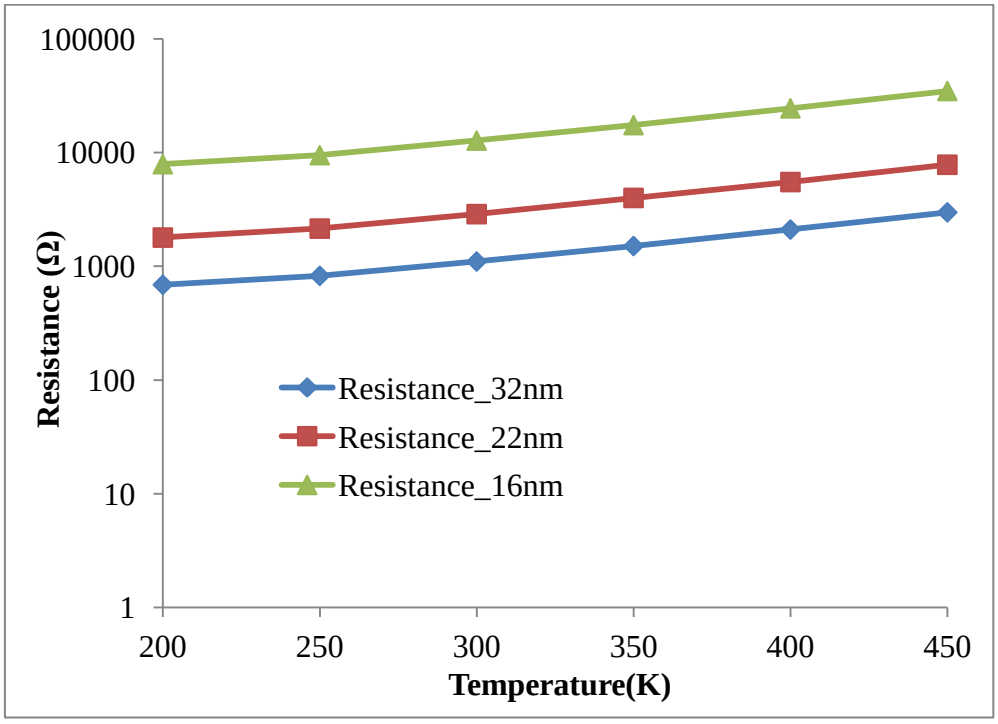
(c)

Figures 4.2: (a), (b) and (c) Temperature dependent and independent resistances of MWCNT bundle interconnects based on 1mm interconnects length at 32nm, 22nm and 16nm technology nodes respectively.

Figures 4.2(a), (b) and (c) show the calculated values of temperature dependent and independent resistances of MWCNT bundle interconnects for 1mm interconnects length at 32nm, 22nm and 16nm technology nodes respectively. With rise in temperature, a non-negligible impact of temperature on resistance can be observed from the results for each technology node under consideration as shown in Figure 4.2. It is also revealed from the results that with rise in temperature ranging from 300K to 450K, the resistance for all three technology nodes is sharply increasing and it is due to reduction in the effective MFP for each shell of MWCNT. Hence, it is concluded from the results that to analyze the accurate performance of MWCNT bundle under variable thermal environment, there is need to consider the impact of temperature for MWCNT interconnects.



(a)



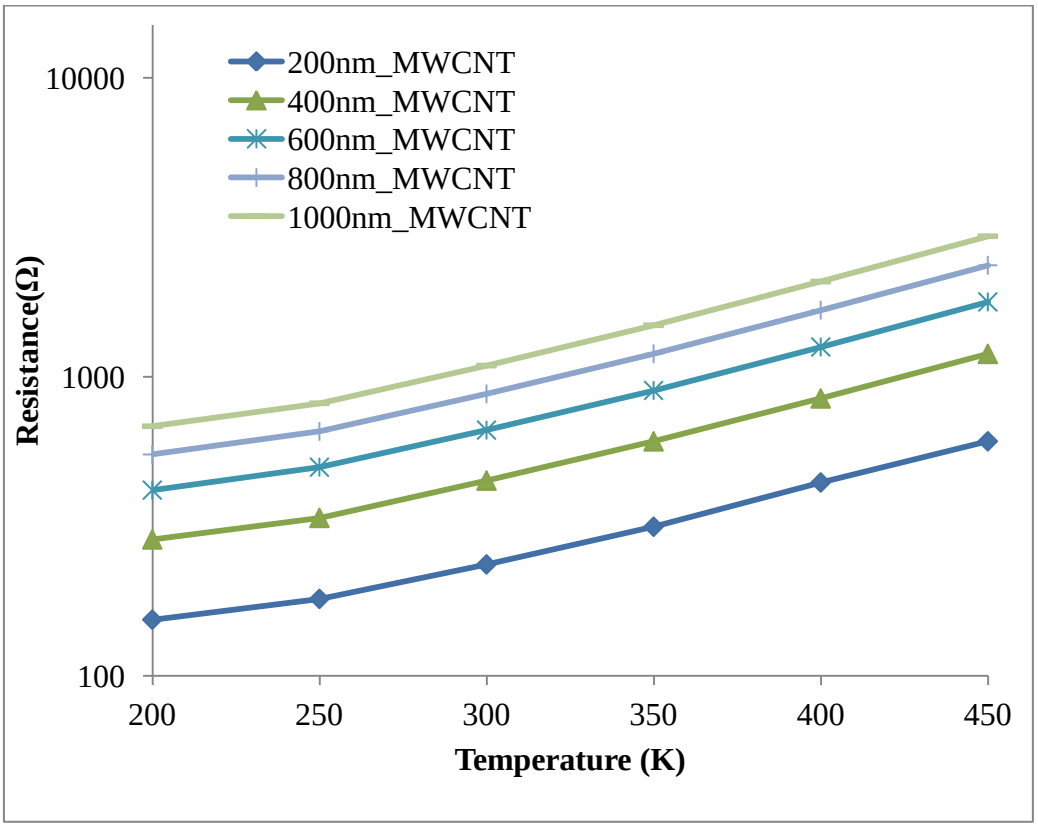
(b)

Figure 4.3: Temperature dependent resistance of MWCNT bundle interconnects for 32nm, 22nm and 16nm technology nodes for global interconnects (1mm interconnect length). (a) The resistance shown on linear scale. (b) The resistance shown on logarithm scale.

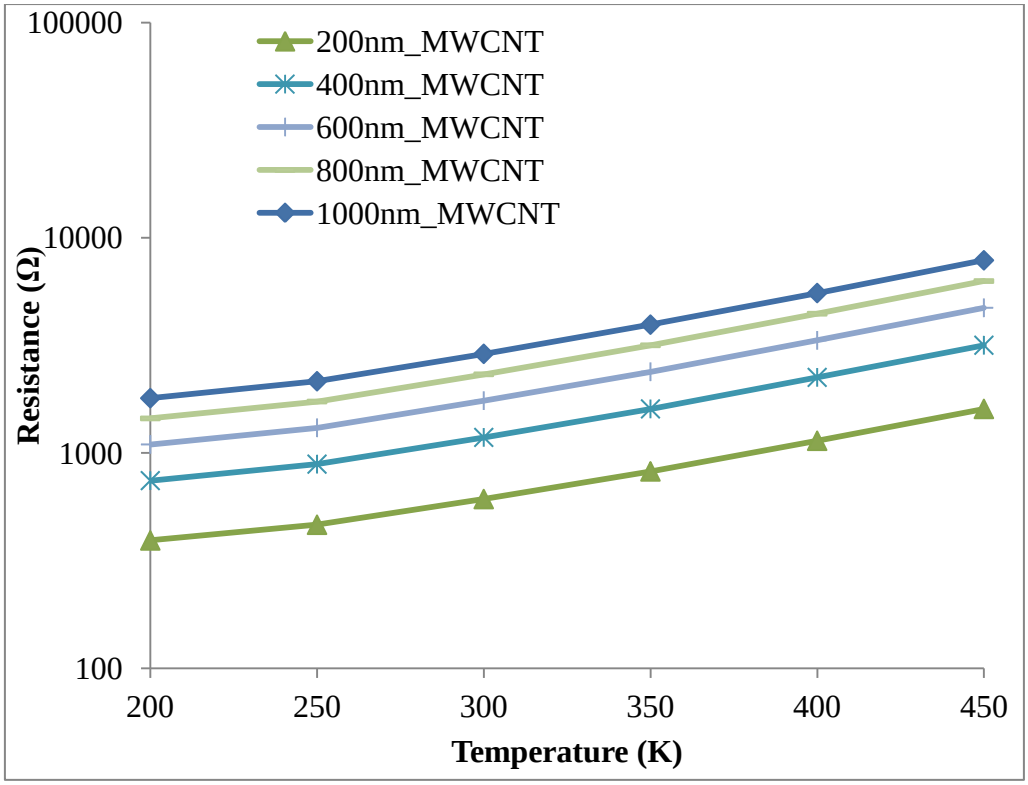
Figure 4.3 shows the calculated values of resistances of MWCNT bundle as a function of temperature for 1mm length at 32nm, 22nm and 16nm technology nodes. It is observed that with rise in temperature ranging from 200K to 450K, the resistance of MWCNT bundle increases. This is due to decrease in effective MFP and the increase in the collision rates within MWCNT with rise in temperature (see Eqs. 3.7 to 3.12).

Further, the impact of variable temperature on MWCNT bundle interconnects is also analyzes for the variable interconnects length from 200µm to 1000µm. Temperature dependent resistance for different interconnects lengths (200µm to 1000µm) at 32nm, 22nm and 16nm technology nodes is shown in Figure 4.4.

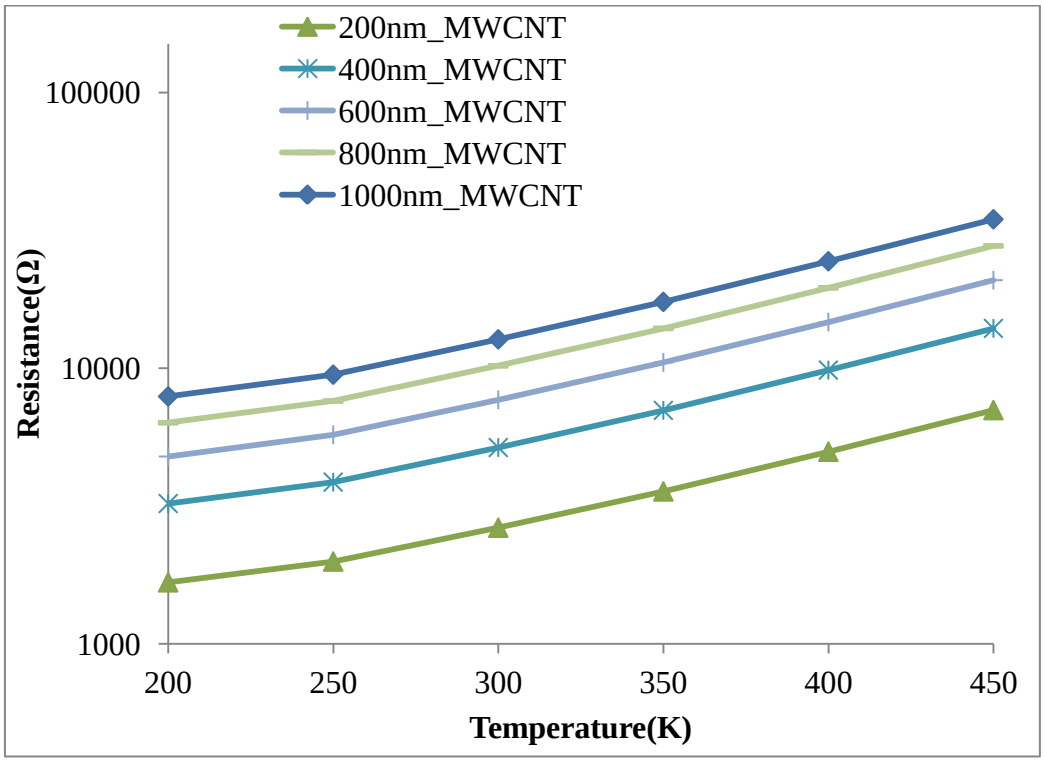
It is revealed from the results that with rise in temperature (from 200K to 450K), the resistance is increasing for all the interconnect lengths, varying from 200µm to 1000µm at all the technology nodes under consideration (32nm, 22nm and 16nm). Hence, there is a need to include the influence of temperature on variable interconnect lengths in deep sub-micron technology nodes.



(a)

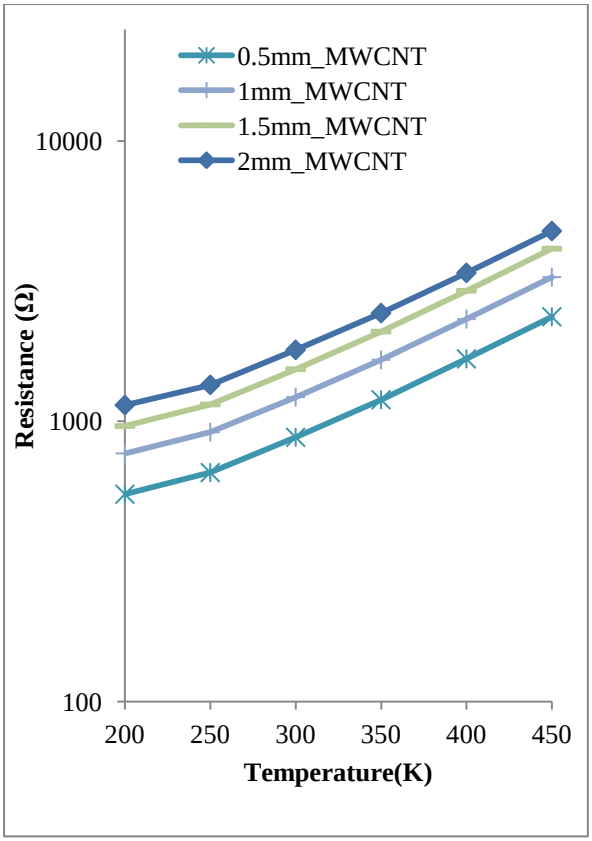


(b)

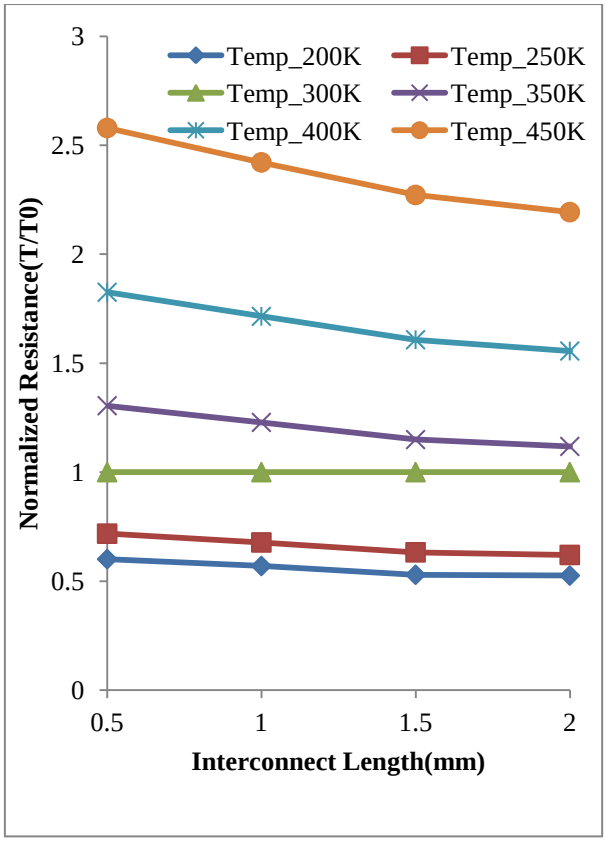


(c)

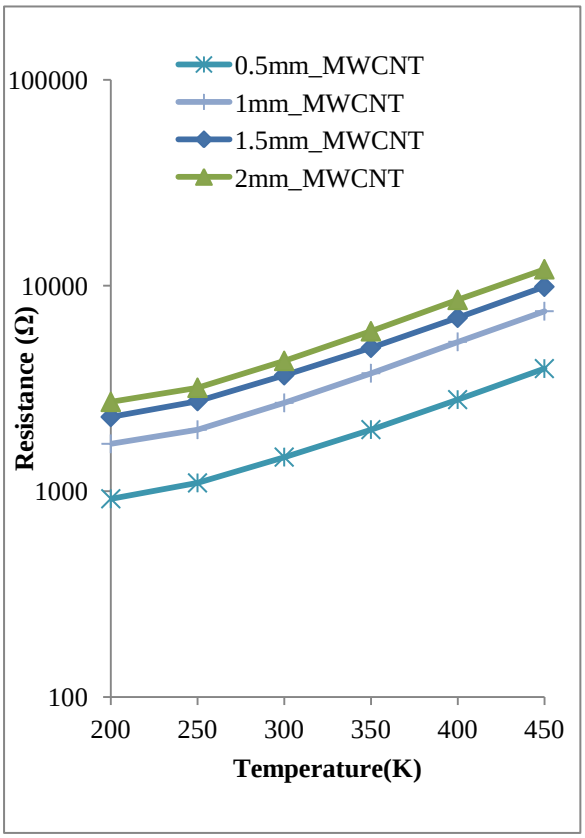
Figures 4.4: (a), (b) and (c) Temperature dependent resistance of MWCNT bundle interconnects for 32nm, 22nm and 16nm technology nodes respectively for interconnects length 200µm to 1000µm. The resistances are shown on logarithm scale.


0.5mm_MWCNT
1mm_MWCNT
1.5mm_MWCNT
2mm_MWCNT
10000
1000
100
Resistance (Ω)
200
250
300
350
400
450
Temperature(K)

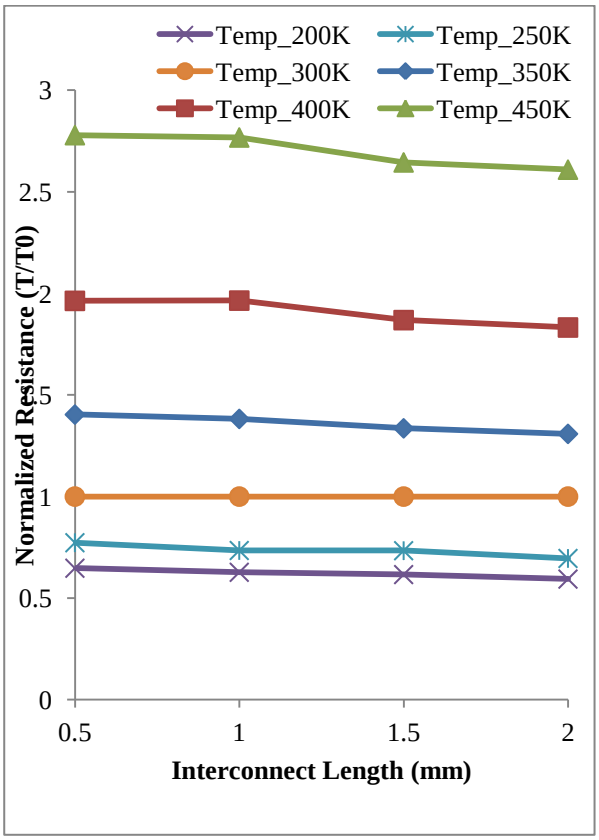
(a)


Temp_200K
Temp_250K
Temp_300K
Temp_350K
Temp_400K
Temp_450K
3
2.5
2
1.5
1
0.5
0
Normalized Resistance(T/T0)
0.5
1
1.5
2
Interconnect Length(mm)

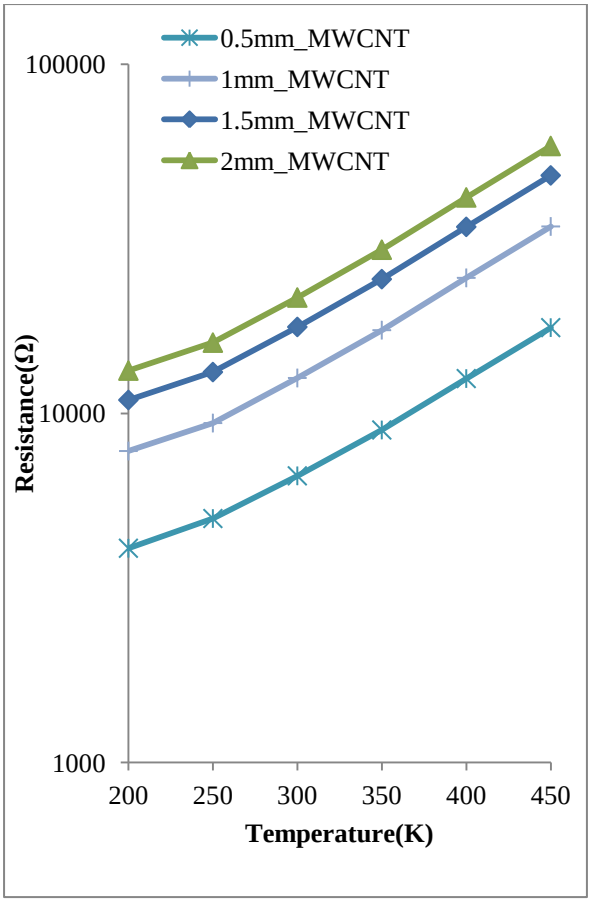
(b)

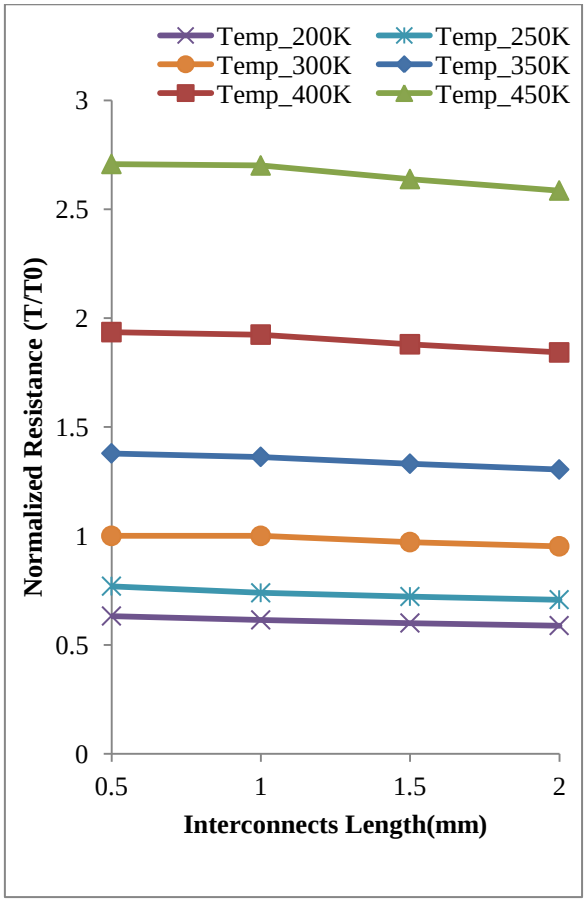

0.5mm_MWCNT
1mm_MWCNT
1.5mm_MWCNT
2mm_MWCNT
100000
10000
1000
100
Resistance (Ω)
200
250
300
350
400
450
Temperature(K)

(c)


Temp_200K
Temp_250K
Temp_300K
Temp_350K
Temp_400K
Temp_450K
3
2.5
2
1.5
1
0.5
0
Normalized Resistance (T/T0)
0.5
1
1.5
2
Interconnect Length (mm)

(d)





(e) **(f)**

Figure 4.5: Temperature dependent resistance of MWCNT bundle interconnects at 32nm, 22nm and 16nm technology nodes for long interconnects lengths from 0.5mm to 2mm. Figures 4.5 (a) and (b) Temperature dependent resistance for variable interconnects length (0.5mm to 2mm) on logarithm scale and the normalized resistance (R_T/R_{T0}) at 32nm Technology node respectively. Figures 4.5 (c) and (d) shows the similar effect for 22nm and figure 4.5(e) and (f) for 16nm respectively.

Furthermore, the impact of variable temperature on MWCNT bundle interconnects is extended up-to 2mm to understand the impact of temperature on long interconnects. Figure 4.5 shows the temperature dependent resistance of MWCNT bundle interconnects at 32nm, 22nm and 16nm technology nodes for interconnects length from 0.5mm to 2mm. Figures 4.5(a) and (b) Show the temperature dependent resistance for variable interconnects length (0.5mm to 2mm) on logarithm scale and the normalized resistance (R_T/R_{T0}) respectively at 32nm technology node.

It is revealed from the Figure 4.5(a) that there is increase in resistance with rise in temperature from 200K to 450K for long interconnects lengths from 0.5mm to 2mm. Figure 4.5(b) show the normalized resistance which is the ratio of resistance at any temperature *T* to

the resistance at room temperature (T_0=300K). It is observed from results that the normalize resistance is decreasing as interconnects length increasing, which specify that for longer interconnects, the performance of MWCNT bundle interconnects in terms of resistance is better than smaller interconnects. It is also revealed from the results that the normalized resistance is decreasing more rapidly at moderate to high temperature range (from 300K to 450K) compared lower to moderate temperature range (less than 300K). Therefore, it concluded that for higher temperature, the resistance is affected by the impact of temperature, more severely and need to be addressed for accurate analysis of MWCNT bundle interconnects. A similar effect is also observed from Figure 4.5(c) and (d) for 22nm technology node and Figure 4.5(d) and (e) for 16nm technology node respectively.

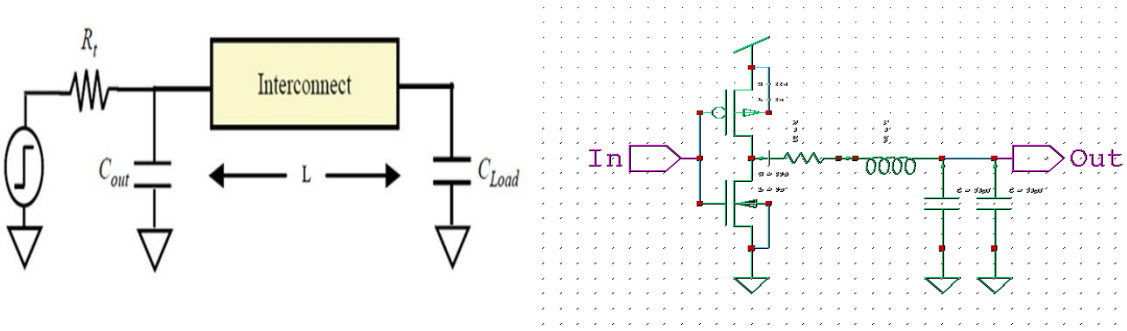
Calculations for inductance and capacitance of MWCNT bundle are obtained using Eqs 3.13 to 3.19. The equations show that the inductances and capacitances of MWCNT bundle interconnects are independence from temperature dependent effective MFP of MWCNT bundle interconnect and therefore the effect of rise in temperature on inductance and capacitance is negligible small compared to resistance and hence it is ignored in this research work.

4.3. Performance Analysis MWCNT bundle interconnects in terms of propagation delay, power dissipation and Power Delay Product (PDP)

Propagation delay and power dissipation of the signal conveyed in the VLSI technology are the key factors which determines the performance of an IC. Delay should always be low to obtain high speed signal propagation along with low power dissipation for high performance integrated circuits. Therefore, an optimum Power Delay Product (PDP) needs to be analyzed to understand the performance of an IC.

In this section the performance of MWCNT bundle interconnects is estimated in terms of delay, power and Power Delay Product (PDP) for different technology modes i.e. 32nm, 22nm and16nm at global interconnects length. A schematic structure used as simulation setup for interconnects is shown in Figure 4.6. An interconnect with length L driven by a CMOS gate driver and loaded with a capacitance C_{load} is shown in Figure 4.6(a) [131, 132] The 'interconnect' replaced by temperature dependent an equivalent RLC circuit model for MWCNT bundle interconnects. R_t and C_{out} are equivalent output resistance and capacitance of the gate driver, respectively, and C_{load} is the input capacitance of the load gate. Actual

lumped interconnects circuit model used to calculate propagation delay and power dissipation shown in Figure 4.6(b). A pulse signal is to be considered as input signal with same rise and fall time durations.[133]



(a) **(b)**

Figure 4.6: (a) Schematic of circuit of interconnects used for evaluation [95]. (b) Actual lumped RLC model used for interconnect to simulate delay and power.

The temperature dependent impedance parameters obtained from section 4.1 for MWCNT bundle interconnect using the equivalent model are simulated by using Tanner EDA tool to evaluate the performance in terms of delay, power and PDP for actual distributed RLC model for interconnects as shown in Figure 4.7.[127, 135, 136]

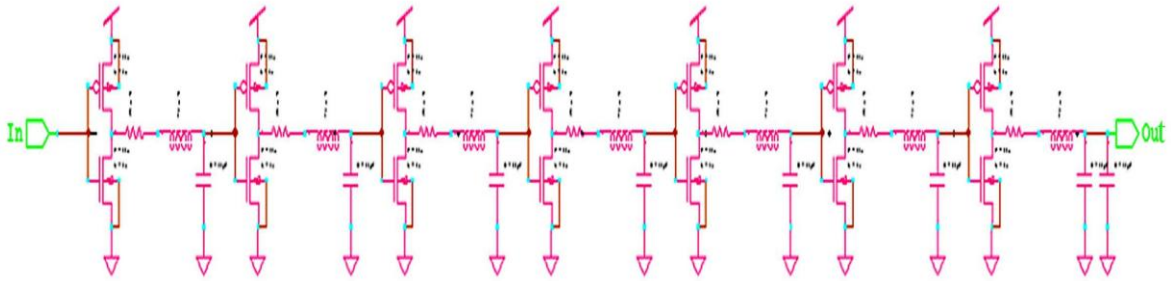


Figure 4.7: A distributed model with optimum 'm' number of repeaters.

A lumped interconnects model divided into different subsections/segments with *m* number of repeaters and referred as distribution models. Repeaters are generally inserted to drive interconnect with smaller sub sections, which increase the drive capacity and reduce the overall delay of the given length. The optimum number of repeaters and size of a repeater for simulation are chosen for different technology nodes as mentioned in table 2. The model files used for simulations are obtained from predictive technology model (PTM). The other interconnect parameters used for simulation model are also summarized in table 1.

Table 4.2: Simulation parameters for different technology nodes [137]

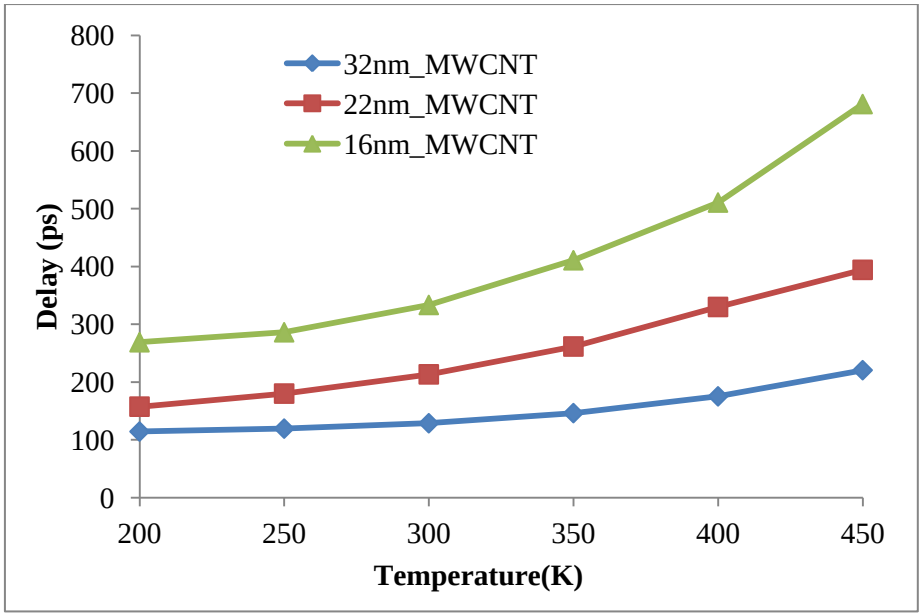
Technology Node	32nm	22nm	16nm
Frequency (GHz)	1	1	1
Repeater size (*W/L*)	50	50	60
Load Capacitance (fF)	10	10	10
No. of Repeaters	12	12	10
Model file(PTM)	54	54	54

The temperature dependent performance in terms of delay is simulated for MWCNT bundle interconnects for global interconnect length at three different technology viz. 32nm, 22nm, 16nm for variable temperature ranging from 200K to 450K and shown in Figure 4.8.

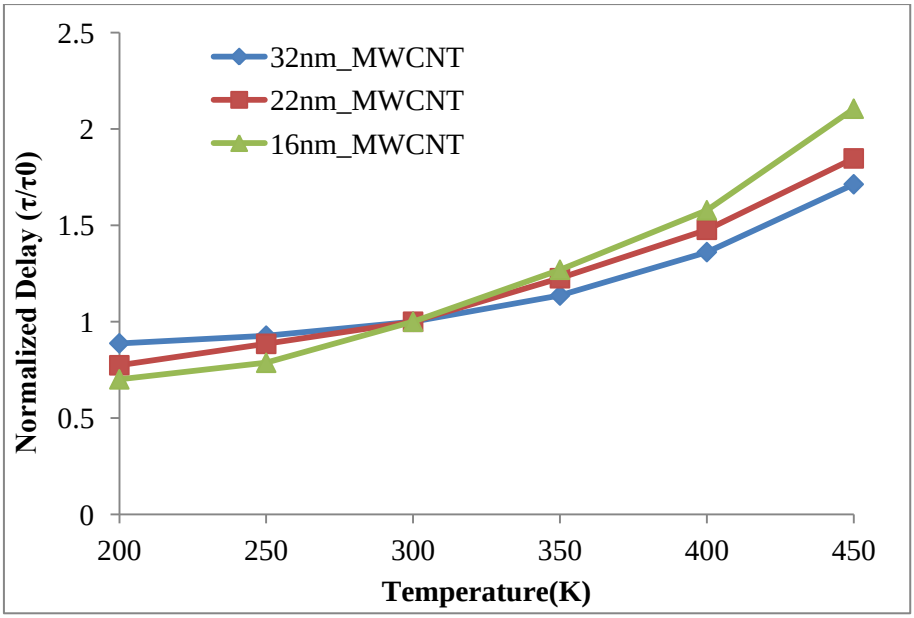
Figure 4.8(a) shows the propagation delay of MWCNT bundle interconnects as a function of temperature for 1mm interconnects length at 32nm, 22nm and 16nm technology nodes. It is observed from the results that the delay increases with rise in temperature for MWCNT bundle interconnects for all three technology nodes. This increase in delay is because of reduction in MFPs of the tubes (see Eqs.3.7-3.12). Normalized delay ratio (delay at temperature *(T)* to delay at 300K i.e. (τ/τ_0)) for three different technology nodes is given in table 4.3 and shown in Figure 4.8(b).

Table 4.3: Normalized delay ratio for MWCNT interconnects at three different technology nodes

Technology node →	**Normalized delay ratio for MWCNT**		
	32nm	**22nm**	**16nm**
Temp. (K)	**Delay(ps)**	**Delay(ps)**	**Delay(ps)**
200	0.88825	0.774225	0.701278
250	0.927883	0.885391	0.787342
300	1	1	1
350	1.136152	1.225973	1.269944
400	1.361517	1.477385	1.57885
450	1.713553	1.847632	2.105751



(a)



(b)

Figure 4.8: (a) Temperature dependent performance in terms of delay for MWCNT bundle interconnects for 1mm interconnect length at three different technology viz. 32nm, 22nm, 16nm for variable temperature ranging from 200K to 450K.. (b) Normalized delay (τ/τ_0) for MWCNT bundle.

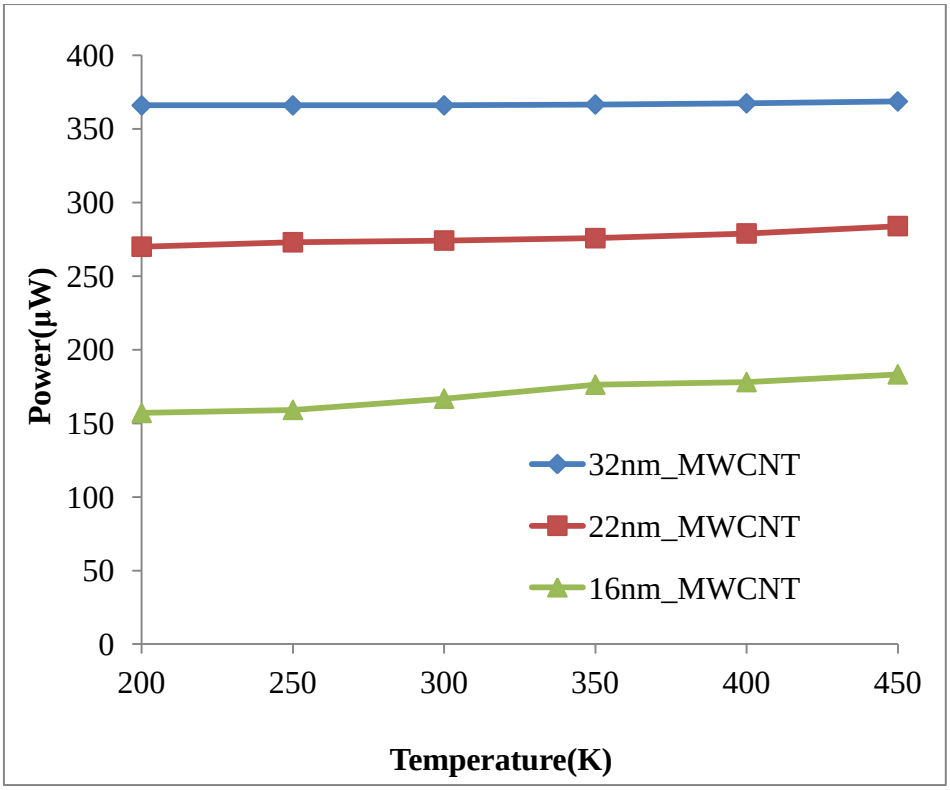
Figure 4.8 (b) shows the normalized delay ratio for MWCNT bundle based on 1mm interconnects length for temperature range from 200K-450K at 32nm, 22nm and 16nm technology nodes. It revealed from the results shown Figure 4.8 (b) that the normalized ratio is increasing sharply as the temperature increasing from 300K to 450K as compared to 200K

to 300K. It is also observed that at higher side of temperature (350K-450K), the normalized delay ratios are 1.136-1.71, 1.23-1.85 and 1.3-2.1 for 32nm, 22nm and 16nm technology nodes respectively. Further, the normalized delay ratio at 450K is 1.71, 1.847 and 2.1 for 32nm, 22nm and 16nm technology nodes respectively, indicates that for scaled down technology nodes i.e. from 32nm to 16nm, the normalized delay ratio is increasing more rapidly.

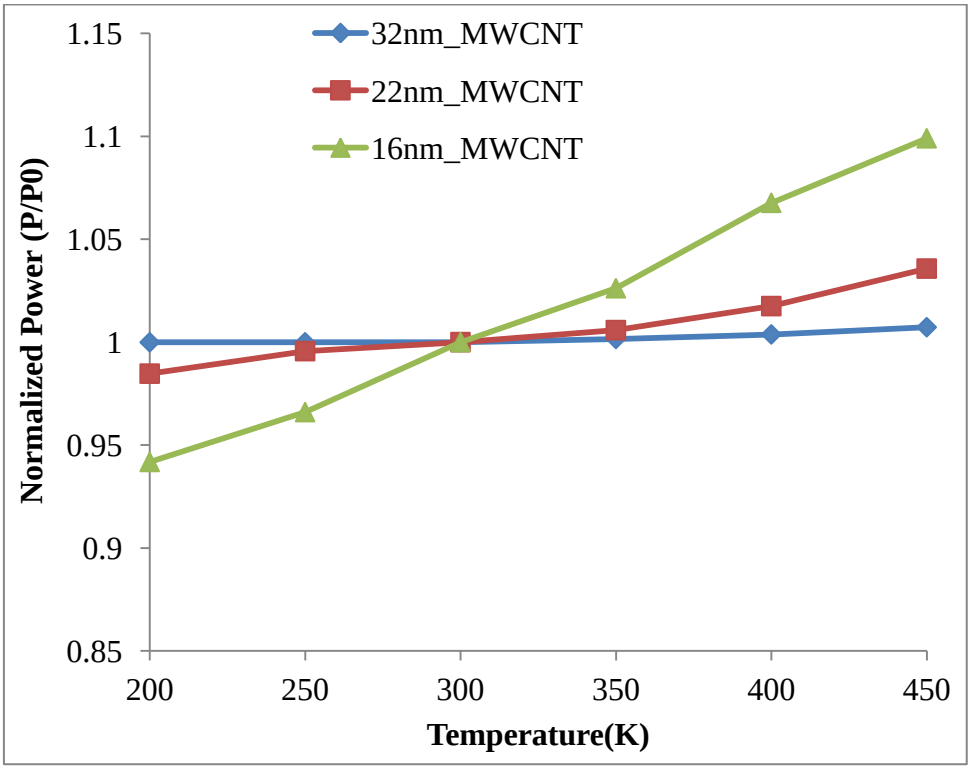
Figure 4.9(a), shows the temperature dependent power dissipation for MWCNT bundle interconnects at 32nm, 22nm and 16nm technology nodes for 1mm interconnects length. It is shown in Figure 4.9(a) that the power dissipation increases with rise in temperature for MWCNT bundle interconnects at all three technology nodes. Normalized power dissipation ratio (P/P_0) for three different technology nodes is given in table 4.4 and shown Figure 4.9(b). It revealed from the results shown Figure 4.9(b) that the normalized power ratio is increasing more rapidly at moderate to high temperature (300K to 450K) compared to low to moderate temperature (200K-300K). It is also observed from the results that the power dissipation ratio at 16nm for temperature range 300K to 450K higher than the other two technology nodes (22nm and 32nm). Therefore with scaled down technology nodes, the extent of change in power ratio is more at modern to high temperature range for VLSI integrated circuits

Table: 4.4: Normalized power ratio for temperature ranging from200K-450K at 32nm, 22nm and 16nm technology nodes

Technology node →	**Normalized power dissipation for MWCNT at different technology nodes**		
	32nm	**22nm**	**16nm**
Temp. (K)	**Power in µW**	**Power in µW**	**Power in µW**
200	0.999918	0.984683	0.94178
250	0.999918	0.995624	0.965997
300	1	1	1
350	1.001557	1.005835	1.026185
400	1.003743	1.017505	1.067694
450	1.00724	1.03574	1.099053



(a)



(b)

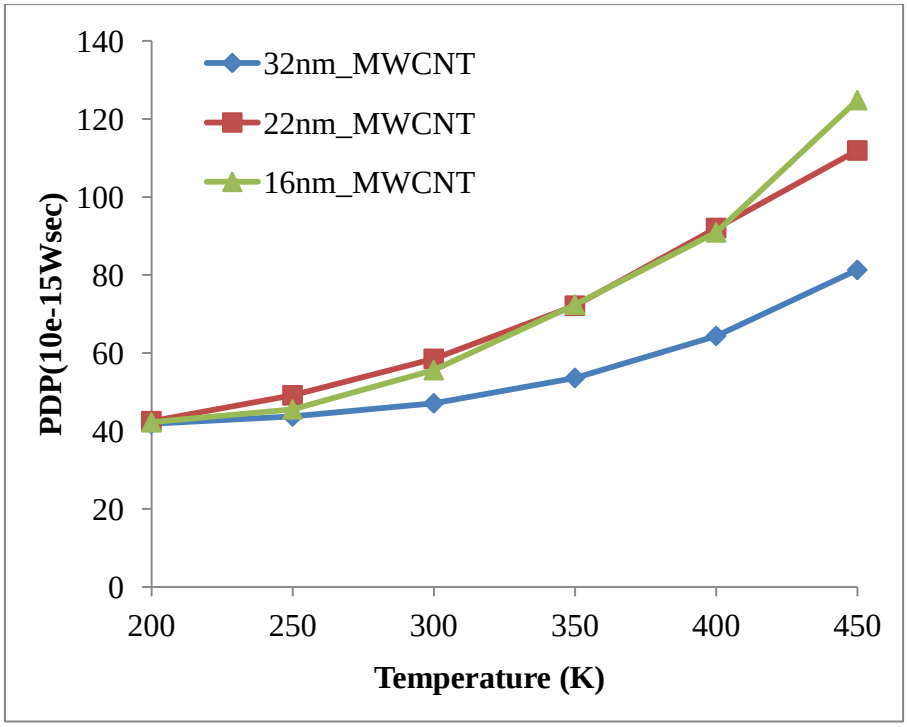
Figure 4.9: (a) Temperature dependent performance in terms of power dissipation for MWCNT bundle interconnects based on 1mm interconnect length at 32nm, 22nm, 16nm for variable temperature ranging from 200K to 450K. (b) Normalized power dissipation *(P/P$_0$)* for MWCNT bundle.

Figure 4.10(a), shows the temperature dependent Power Delay Product (PDP) of MWCNT bundle interconnects for 1mm interconnects length at 32nm, 22nm and 16nm technology nodes. It is revealed from the results that Power Delay Product (PDP) for MWCNT bundle interconnects is increasing with rise in temperature ranging from 200K to 450K for all technology nodes under consideration. Although, PDP is increasing for all the technology nodes but the degree of change in PDP for 16nm is higher compared to 22nm and 32nm technology nodes and the change in PDP for 22nm is high than 32nm technology node. Normalized Power Delay Product (PDP) ratio for three different technology nodes is given in table 4.5 and shown Figure 4.10(b).

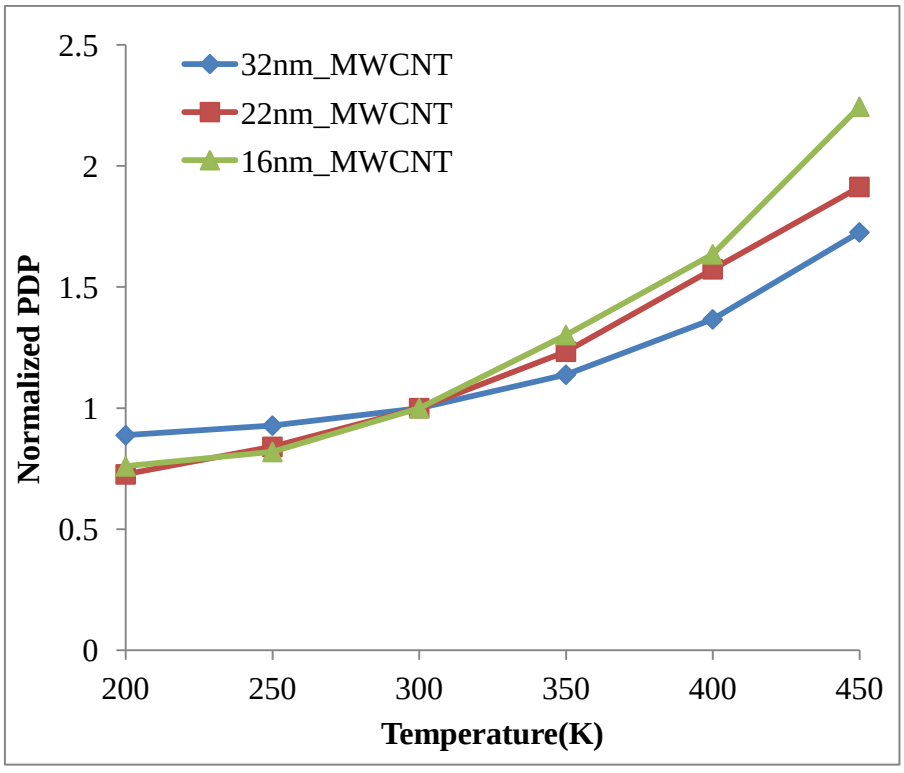
Table: 4.5: Normalized PDP ratio for temperature ranging from200K-450K at 32nm, 22nm and 16nm technology nodes

Technology node →	**Normalized PDP for MWCNT at different technology nodes**		
	32nm	**22nm**	**16nm**
Temp	**PDP**	**PDP**	**PDP**
200	0.888191	0.726624	0.759558
250	0.927822	0.840188	0.819132
300	1	1	1
350	1.137939	1.233126	1.302111
400	1.366634	1.573722	1.635298
450	1.725986	1.913666	2.245095

It revealed from the results shown Figure 4.10(b) that the normalized PDP ratio increases more rapidly for temperature above 300K compared to below 300K. The normalized PDP ratio for temperature ranging from 350K to 450K increases from 1.38 to 1.726, 1.23 to1.91 and 1.3 to 2.245 for technology nodes 32nm, 22nm and 16nm respectively. Therefore, it is also observed from the results that the PDP ratio for 16nm is higher than 22nm and 32nm technology nodes for temperature ranging from 350K to 450K. Therefore as technology scaled down, the amount of PDP is increasing at moderate to high temperature range (300K-450K) for VLSI integrated circuits design.



(a)



(b)

Figure 4.10: (a) Temperature dependent performance in terms of Power Delay Product (PDP) for MWCNT bundle interconnects for 1mm interconnect length at 32nm, 22nm, 16nm technology nodes for variable temperature ranging from 200K to 450K. (b) Normalized PDP for MWCNT bundle interconnects.

4.4. Chapter Summery and Contribution

In this chapter, temperature dependent performance analysis for MWCNT bundle interconnects is presented. By using the proposed mathematical expressions as discussed in chapter 3, temperature dependent effective MFP of each shell of MWCNT is calculated for temperature range of 200K to 450K at 32nm, 22nm and 16nm technology nodes. On the basis on proposed temperature dependent impedance model, the impedance parameters of each shell of MWCNT are calculated for different interconnects lengths at 32nm, 22nm and 16nm technology nodes. The equivalent impedance parameters of MWCNT bundle are obtained by considering all the parameters of individual shells in parallel. The calculations are obtained by writing the script in MATLAB. All interconnects technology parameters are calculated using the data obtained from ITRS 2013 version. It is observed that with rise in temperature (from 200K to 450K), the resistance increases due to decrease in MFP for MWCNT. MFP decreases because of there is increase in the collision rates within MWCNT as temperature rises. Hence, this change in resistance has considerable effect on the performance in terms of delay, power and PDP for the MWCNT bundle interconnects at nano-scaled technology nodes for global interconnects length.

The performance of MWCNT interconnect is estimated in terms of delay, power and Power Delay Product for 32nm, 22nm and 16nm technology nodes at global interconnects length. The calculated impedance parameters for MWCNT bundle interconnects using the equivalent models have been simulated to evaluate the performance in terms of delay and power by using the SPICE simulation tool for distributed RLC model for interconnects. The distributed RLC model can be approximated from a lumped model by with multi-stage RLC ladder network. Repeaters are inserted to separate different stages of RLC ladder network. The simulation results are obtained using optimum number of repeaters and optimum size repeater and number of repeaters. Other simulation parameters and model file is obtained from Predictive Technology Model (PTM).

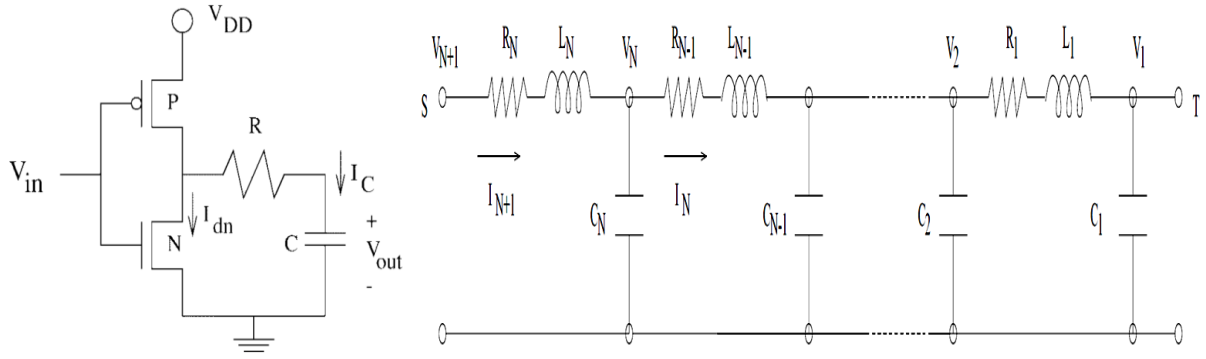
It is observed from the simulated results that with rise in temperature (200K-450K), the delay power and PDP increased for MWCNT bundle interconnects for all three technology nodes (32nm,22nm and 16nm) and it is due to the shrinking of MFPs. It is revealed from the results that the temperature variations have a considerable impact on the performance of MWCNT bundle interconnects. Therefore, during the performance estimation of MWCNT bundle based interconnects, the influence of temperature is needs to be taken care for accurate performance estimation.

5 ANALYTICAL DELAY MODEL FOR MWCNT INTERCONNECTS

In this chapter the temperature dependent analytical delay model is presented for MWCNT interconnects and results are compared with the simulated results obtained from chapter 4. The results presented in the chapter show that the analytical results are aligned with the simulated results. The trend of both results shows that the delay is increases with rise in temperature for all the technology nodes i.e 32nm, 22nm and 16nm.

5.1 Introduction

The feature size of integrated circuits for advanced technology nodes decreases, interconnects wires contributes more towards total delay compared to gate delays as the total logic-stage delay having two components; gate delay and interconnect delay[8]. Earlier, the gate delay was dominating component and estimated by considering the entire interconnect tree at the gate output as a simple lumped resistance-capacitance model as shown in Figure 5.1(a)[31].



(a) **(b)**

Figure 5.1(a) RC lumped model with CMOS driver [31] (b) Distributed RLC Model [8]

Now, as the technology scaled down, impedance parasitic of interconnects increased and becomes larger interconnect trees, the lumped capacitance approximation technique

introduces the errors in the delay and rise time calculations [138]. Accuracy to estimate gate delay and rise time closely depends upon the parasitic of interconnects and load at the output of a gate. The equivalent impedance parasitic of interconnects is to be considered as transmission lines in deep submicron technology nodes. Therefore, to estimate the accurate performance of VLSI interconnects, highly accurate RLC distributed models are to be required as shown in Figure 5.2(b). Resistance-capacitance (RC) is the basic model used to estimate the performance in terms of delay. Elmore delay model [13] is an example of RC model used to calculate the delay for RC loads only. Elmore delay model provides highly inaccurate results for high frequency input signals because it increases the inductive impedance [13]. For micro scaled technology nodes, aluminum and copper were used as interconnects material which can easily be converted into its equivalent single line transmission model. The models presented by H. B. Bakoglu, *et al*. [3], Sakurai *et al*.[7, 139] and Adler V. and E.G. Friedman, [31] were based on RC models and useful to estimate the delay for copper interconnects with optimum repeaters. A. Deutsch *et.al. [9]* and Ismail and E. G. Friedman [20, 36], proposed RLC delay models which included the impact of inductance along with RC models. The improvement is proposed in these models after inclusion of inductive effects. [92, 140]

At nano-scaled technology nodes, copper has certain deficiencies like electromigration, surface and grain boundary scattering, Carbon Nanotubes (CNT) have been considered as an alternative material for VLSI interconnects. Due to the structural complexity and different parasitic of CNTs, existing delay models are not efficient enough to estimate the accurate delay for CNT [92].

The revolutionary work on delay modeling of SWCNT is based on Luttinger liquid theory proposed by P.J. Burke [84], for its equivalent circuit as transmission line. Since then, sufficient number models have been reported for the SWCNT bundle and MWCNT bundle interconnects in literature [91, 99, 141]. Boltzmann transport theory model was other alternative used to model the SWCNT interconnect [142]. In case of MWCNT interconnects, early research proposed that only few outermost shells of bundle can contributes to current. Bur recently, it has been proposed that with an end contact method, all the shells of MWCNT bundle can efficiently be contacted to the electrode so that all shells of bundle can contributes to current. Later, some models have been proposed to evaluate the performance and equivalent circuit modeling of the MWCNT interconnects [99]. A single conductor

equivalent model for the MWCNT bundle was proposed, which was later extended to the SWCNT bundle interconnects [51, 143]. In literature [51], it is proposed that MWCNT bundle interconnects are more suitable for intermediate and global interconnects. So to estimate the optimum delay repeater based distributed RLC circuit models are to be considered. [123, 143-146]

In this chapter, closed-from empirical equations are discussed for the estimation of the delay, optimum number of repeaters and optimum repeater size, for MWCNT bundle interconnects[51,99]. By using the analytical model, the performance in terms of delay is estimated for global interconnects at 32nm, 22nm and 16nm technology nodes for variable temperature ranging from 200K- 450K. Further, a comparative analysis is performed with the results obtained from analytical models and simulated results.[99]

5.2. Equivalent Single Conductor model for MWCNT bundle

Multi-Walled CNT (MWCNT) bundle consists more than two rolled up graphene sheets concentrically inserted with diameters ranging from few nanometers to tens of nanometer. An MWCNT bundle has many concentric shells of different diameter, which can be seen as several shells in parallel. Each shell has its equivalent RLC model, and therefore for a MWCNT bundle, all shells have their RLC equivalent circuit models and connects in parallel as shown in Figure 5.2.[84]

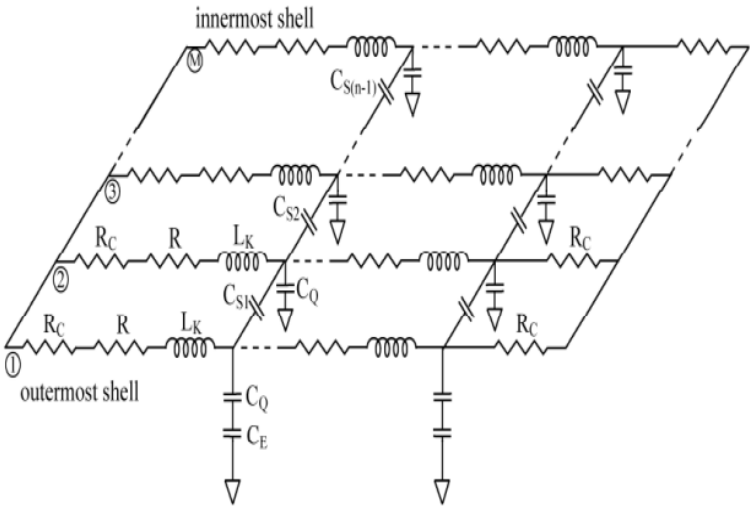


Figure 5.2 Equivalent circuit of a metallic MWNT interconnects [84].

To estimate the analytical delay, this equivalent model for MWCNT bundle needs to be converted into single conductor model. The transmission line equations for single conductor model can be given as[99]

$$\frac{\partial V(z,t)}{\partial z} + L\frac{\partial I(z,t)}{\partial t} + RI(z,t) = 0 \tag{5.1}$$

$$\frac{\partial I(z,t)}{\partial z} + C\frac{\partial V(z,t)}{\partial t} = 0 \tag{5.2}$$

Each MWCNT bundle consists of several shell, therefore, total *n* number of shells in a bundle can be calculated by using Eq. 3.1 as discussed in chapter 3. These shells of a bundle are numbered from outermost shell to innermost shell as *1, 2,..i..n*. Each shell of MWCNT bundle have different diameter, hence the diameter of any i^{th} shell of a bundle can be calculated using Eq. 3.2. Each shell of MWCNT bundle consists of different number of conducting channels and these conducting channels are diameter dependent as discussed in chapter 3. The conducting channels for a shell having diameter less than 3nm are approximately considered equal to *2* and shells having diameters more than 3nm are diameter dependent. Therefore, conducting channels of any i^{th} shell of MWCNT bundle can be given as

$$N_i \approx a.D_i + b, \quad for \quad D_i > 3nm \tag{5.3}$$

Where D_i is the diameter of i^{th} shell, a=6.12x 10^{-4} 1/(nmK) and $b=1.275$.n. Therefore, each shell of a MWCNT bundle has different conducting channels.

The work presents in the thesis analyzes the temperature dependent performance for MWCNT bundle. The equivalent temperature dependent resistance of an individual i^{th} shell of MWCNT bundle can be categorized into three resistive components: electron-phonon scattering dependent resistance (R_s) (considered in case when the length of interconnects is more than its MFP, quantum resistance (R_q) and imperfect metal contact resistance (R_c). The imperfect metal contact resistance (R_c) is because of the metal used for contacting with MWCNT and ranging from few ohms to hundred of kilo-ohm for different fabricating processes. It is almost independent from the diameter of the shell and temperature. Therefore the value for the metal contact resistance (R_c) is almost constant and assumed equal to *2kΩ*

for each shell of MWCNT bundle as suggested in [128]. Therefore, the temperature dependent resistance for an individual shell is given by

$$R_{shell} = R_c + R_q + R_s.L$$
$$R_{shell} = 2k\Omega + \frac{h}{2e^2 N_i} + \frac{h}{2e^2 N_i}.\frac{L}{\lambda eff\,(T)} \tag{5.4}$$

where $h/2e^2$= 12.9kΩ, N_i, L and $\lambda_{eff}(T)$ are the number of conducting channels in a shell, interconnect length and temperature dependent effective MFP of an individual shell respectively. It is revealed from Eq. (5.4) that there is an important role of temperature dependent effective MFP in determining the value of resistance of an individual shell of MWCNT bundle. The temperature dependent effective MFP depends upon the scattering mechanism and discussed in details in section 3.2 of chapter 3. The temperature dependent mathematical equations for individual resistance, capacitance and inductance are also discussed in detail in chapter section 3.2 of chapter 3.

The quantum resistance for each conduction channel is given by

$$R_{qt} = \frac{h}{2e^2} = 12.9k\Omega \tag{5.5}$$

The resistance of MWCNT for the calculation of equivalent single conductor model can be separated into two parts as lumped and scattered resistance and shown as [99]

$$R_{lump,bundle} = \left(\sum_{i=1}^{n} R_{lump,i}^{-1}\right)^{-1} = \left(\sum_{i=1}^{n}\left(\frac{R_{qt}}{2N_i} + R_{c,i}\right)^{-1}\right)^{-1} \tag{5.6},$$

$$R_{s,bundle} = \left(\sum_{i=1}^{n} R_{s,i}^{-1}\right)^{-1} = \left(\sum_{i=1}^{n} \frac{N_i \lambda_{eff,i}}{R_{qt}}\right)^{-1} = \frac{R_{qt}}{\sum_{i=1}^{n} N_i \lambda_{eff,i}} \tag{5.7},$$

Where $R_{s,i}$, $R_{c,i}$ $\lambda_{eff,i}$ are the temperature dependent scattering resistance, contact resistance and MFP of i^{th} shell respectively. $R_{c,i}$ considered to equal to 2kΩ for each shell and N_i is number of conducting channels in i^{th} shell.

The per unit length capacitance of equivalent single conductor of MWCNT can be given as [99]

$$C_{bundle} = (C_{ES}^{-1} + C_{QTM}^{-1})^{-1} \quad (5.8),$$

where C_{ES} and C_{QTM} are electrostatic and quantum capacitances respectively. The quantum capacitance can be calculated from the quantum capacitance of each shell and the mutual capacitance of adjacent shells in MWCNT. C_{QTM} can be calculated using recursive approach and given as [99]

$$c_{rec,1} = C_{QTM}^{(1)} \quad (5.9),$$

$$c_{rec,i} = \left(\frac{1}{c_{rec,i-1}} + \frac{1}{c_m^{i-1,i}} \right)^{-1} + C_{QTM}^{(i)}, \quad i = 1,2,3...n \quad (5.10),$$

$$C_{QTM} = c_{rec.} n \quad (5.11),$$

Where

$$C_m^{i,i+1} = \frac{2\pi\varepsilon_0}{In(D_{i+1}/D_i)}, \quad i = 1,2,3...n-1 \quad (5.12),$$

$$C_{QTM}^{(i)} = 2N_i C_q \quad 1 \le i \le n \quad (5.13)$$

$$C_q = \frac{2e^2}{h v_f} \quad (5.14)$$

Similarly the total inductance per unit length for single conductance equivalent of MWCNT bundle can be calculated as given below [99]

$$L_{bundle} = (L_{Mag} + L_{Ki}) \quad (5.15),$$

where L_{Mag} and L_{Ki} are magnetic and kinetic inductance respectively. The magnetic inductance is very small value as compare to kinetic inductance, so it can be neglected. The kinetic inductance can be calculated from the kinetic inductance of each shell and the mutual inductance of adjacent shells in MWCNT. L_{Ki} can be calculated as given below [99]

$$L_{rec,1} = L_{Ki}^{(1)} \quad (5.16),$$

$$L_{rec,i} = \left(\frac{1}{l_{rec,i-1} + L_m^{i-1,i}} + \frac{1}{L_{Ki}^{(i)}} \right)^{-1}, \quad i = 1,2,3.....n \quad (5.17),$$

$$L_{Ki} = L_{rec.} n \tag{5.18},$$

Where

$$L_m^{i,i+1} = \frac{\mu_0}{2\pi} In(D_{i+1} / D_i), \quad i = 1,2,3...n-1 \tag{5.19},$$

$$L_{Ki}^{(i)} = \frac{L_{Ki}}{2N_i} \quad 1 \le i \le n \tag{5.20},$$

$$L_k = \frac{h}{2v_f e^2} \approx 16.1 mH / m \tag{5.21}$$

The Eqs (5.1-5.21) can be used to convert MWCNT bundle into single conductor equivalent circuit model. Now, by considering single conductor equivalent RLC model for MWCNT, delay needs to be estimated using driver- interconnects- load (D-I-L) structure with CMOS as driver inverter and a load [141]. By using a closed form expression, estimate the delay of this D-I-L structure, proposed for interconnects in [99] and given by

$$t_d = \frac{\left(\exp^{-2.9\zeta^{1.35}} + 1.48\zeta\right)}{\omega_n} \tag{5.22}$$

where

$$\zeta = \frac{R_{bundle}}{2}\sqrt{\frac{C_{bundle}}{L_{bundle}}}\frac{R_T + C_T + R_T C_T (1 + C_{d0} / C_{g0}) + 0.5}{\sqrt{1 + C_T}} \tag{5.23}$$

and

$$\omega_n = \frac{1}{\sqrt{L_{bundle}.L(C_{total} + sC_{g0})}} \tag{5.24}$$

$$R_T = \frac{R_{d0}}{sR_{bundle}} \tag{5.25}$$

$$C_T = \frac{sC_{g0}}{C_{total}} \tag{5.26}$$

$$R_{bundle} = R_{S,bundle} L + R_{lump,bundle} \tag{5.27}$$

$$C_{total} = C_{bundle} L \tag{5.28}$$

Where R_{bundle}, L_{bundle} and C_{bundle} are the resistance, inductance and capacitance of single conductor equivalent model for MWCNT bundle interconnects respectively and L is length of interconnect. C_{d0},, R_{d0}, and C_{g0} are output capacitance, output resistance of CMOS driver and input capacitance of load, respectively. The aspect ratio of driver is s and R_{lump} is lumped resistance of MWCNT interconnects. [99]

5.3. Repeater Insertion

This delay model can be used to calculate the delay for lumped model for MWCNT bundle. As the work presented in the thesis is to estimate the performance MWCNT bundle at global interconnects. Therefore, to estimate the accurate delay, a distributed circuit model is to be analysis. When a lumped model is divided into subsections/segmented and each segment is driven by a CMOS inverter as shown in Figure 5.3, resultant structure is known as distributed circuit model.[39, 41, 147]

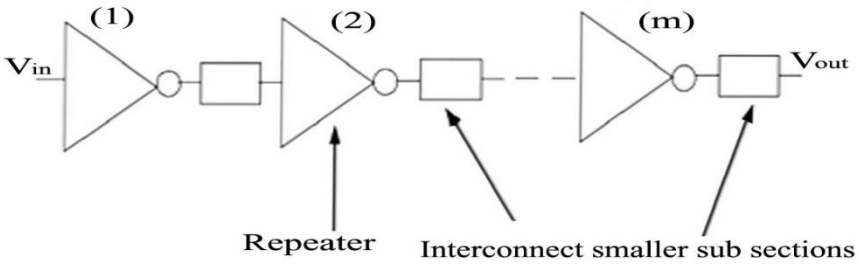


Figure 5.3 Schematic diagram for distribution model with *m* segments [29].

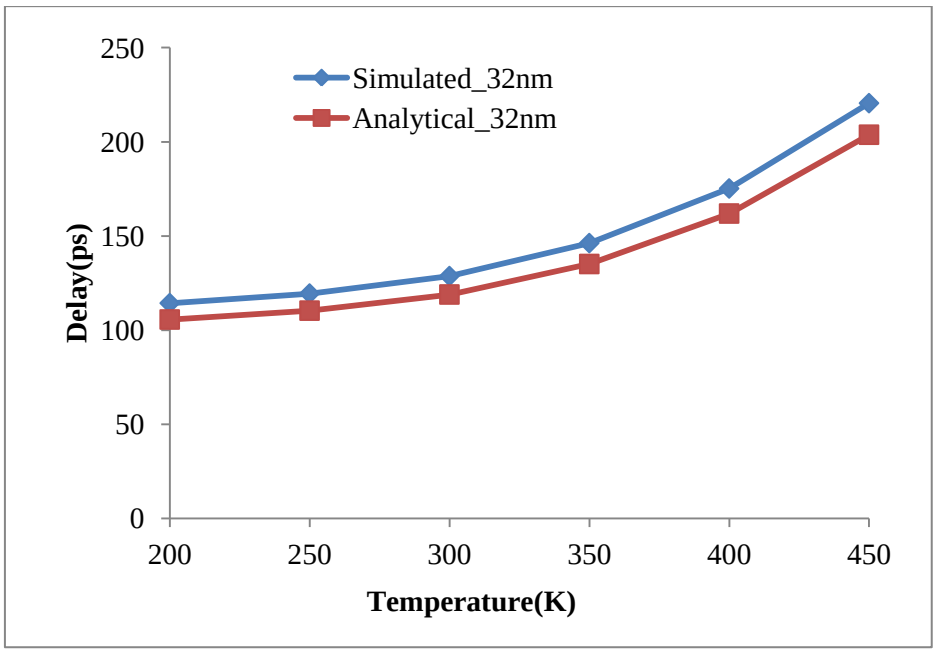
Therefore to estimate the accurate delay for distribution model, the optimum number of repeaters and optimum size of the repeater required to be estimated and given by [99]

$$S_{optimum} = \sqrt{\frac{R_{do}C_{total}}{R_{bundle}C_{g0}} \frac{1}{[1+0.18(T_{L/R})^3]^{0.26}}} \tag{5.29}$$

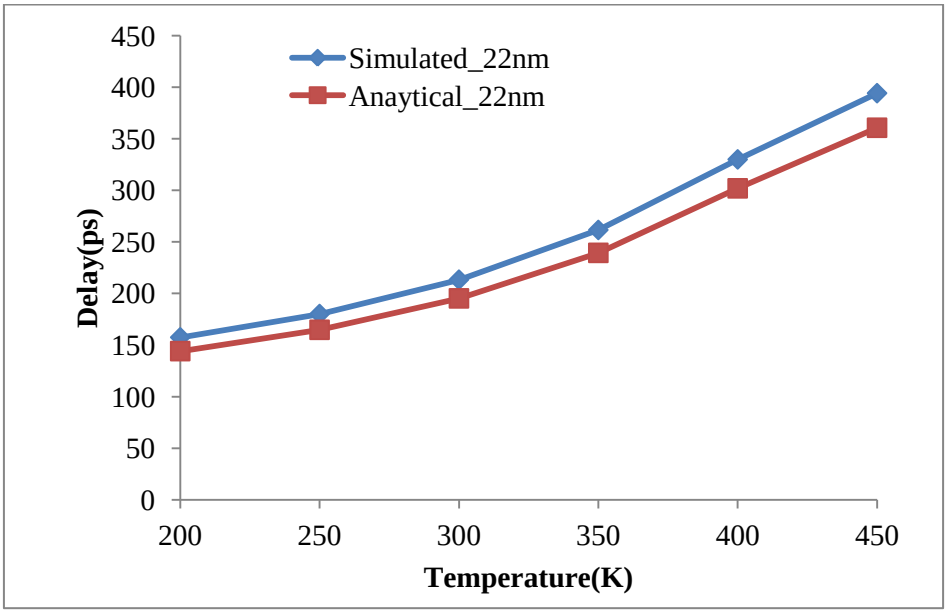
$$N_{optimum} = Int.\left\{\sqrt{\frac{R_{bundle}C_{total}}{2R_{d0}(C_{d0}+C_{g0})}} \frac{1}{[1+\beta(T_{L/R})^3]^{0.28}}\right\} - 1 \tag{5.30}$$

$$T_{L/R} = \sqrt{\frac{L_{bundle}}{R_{s,bundle}[R_{dO}(C_{d0}+C_{g0})]}} \tag{5.31}$$

Based on above mentioned analytical model, the delay is estimated for MWCNT interconnects for 1mm interconnects length at 32nm, 22nm and 16nm technology nodes for variable temperature range 200K-450K. Eqs. 5.3-5.21 are used to estimate the resistance, inductance and capacitance for single conductor equivalent model at 32nm, 22nm and 16nm technology nodes. Eqs. 3.1-3.20 are used to find the temperature dependent impedance parameters for 200K-450K for 1mm interconnects length.



(a)



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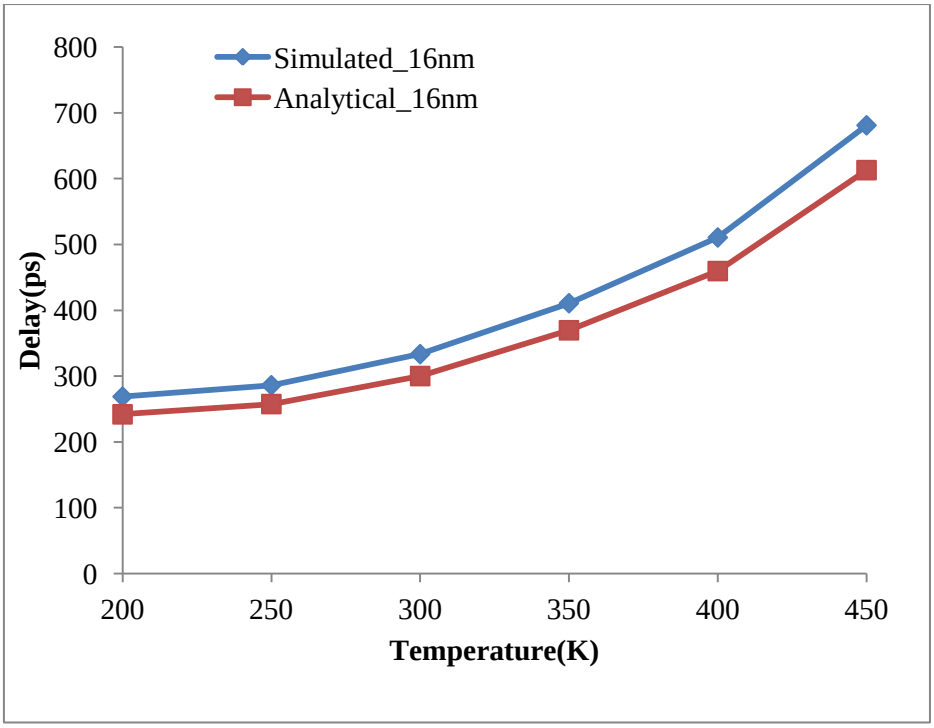

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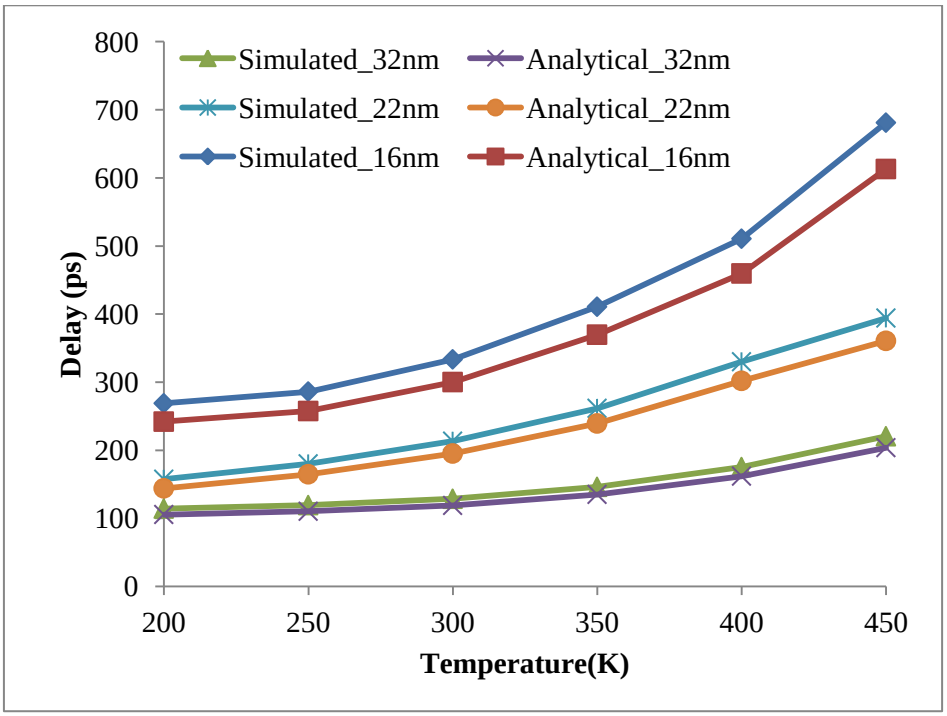


(d)

Figure 5.4: (a), (b) and (c) Comparative analysis of analytical and simulated results for 1mm interconnects length at 32nm, 22nm and 16nm technology nodes for temperature range 200K-450K respectively. (d) Comparative analysis of analytical and simulated results for 1mm interconnects length at all three different technology nodes for temperature range 200K-450K.

The simulation parameters used for calculations are obtained from ITRS 2013, to calculate the parasitic of MWCNT as summarized in Table 4.1 in chapter 4. The optimum number of repeaters and size of repeaters are obtained using Eqs. 5.29-5.31. Further, the optimum delay is calculated using Eqs. 5.22-5.28. For all these calculations, script is written in MATLAB. The comparison of analytical delay calculated from above procedure and simulation delay estimated in chapter 4 is shown in Figure 5.4.

Figure 5.4(a), (b) and (c) Comparative analysis of analytical and simulated results for 1mm interconnects length at 32nm, 22nm and 16nm technology nodes for temperature range 200K-450K respectively. (d) Comparative analysis of analytical and simulated results for 1mm interconnects length at three different technology nodes for temperature range 200K-450K. It is revealed from the results that the delay for analytical and simulated results is increasing with rise in temperature from 200K-450K. Further, the results presented show that the analytical results are aligned with the simulated results. The trend of both results shows that the delay is increasing with rise in temperature for all three technology nodes under consideration.

5.4. Chapter Summary and Contribution

The chapter presented the temperature dependent analytical delay model for MWCNT interconnects and results are compared with the simulated results obtained from chapter 4. The mathematical equations are presented to convert the MWCNT bundle into single conductor equivalent model. The analytical model is presented to estimate the analytical delay of MWCNT interconnects. Further, the method to calculate optimum number of repeater and their size for distributed circuit model is presented. Finally, the analytical and simulated results are obtained for MWCNT bundle interconnects for 1mm interconnects length at 32nm, 22nm and 16nm technology nodes for different temperature ranging from 200K-450K. The results presented in the chapter show that the analytical results are aligned with the simulated results. The trend of both results shows that the delay is increases with rise in temperature for all the technology nodes i.e 32nm, 22nm and 16nm.

6

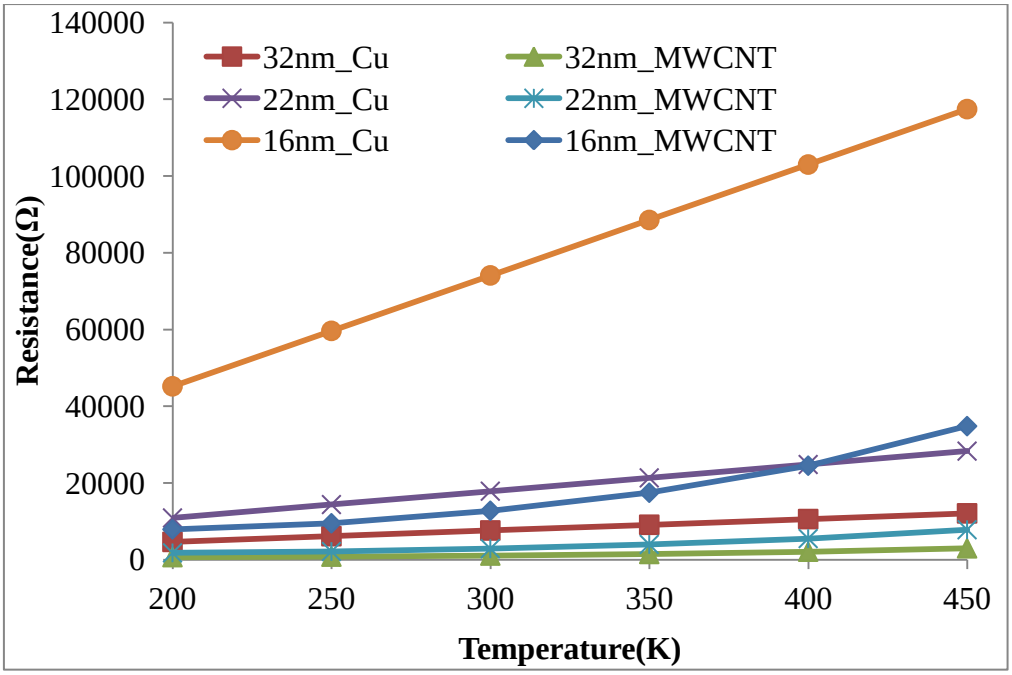
TEMPERATURE DEPENDENT COMPARATIVE ANALYSIS OF MWCNT, SWCNT AND COPPER INTERCONNECTS

6.1. Introduction

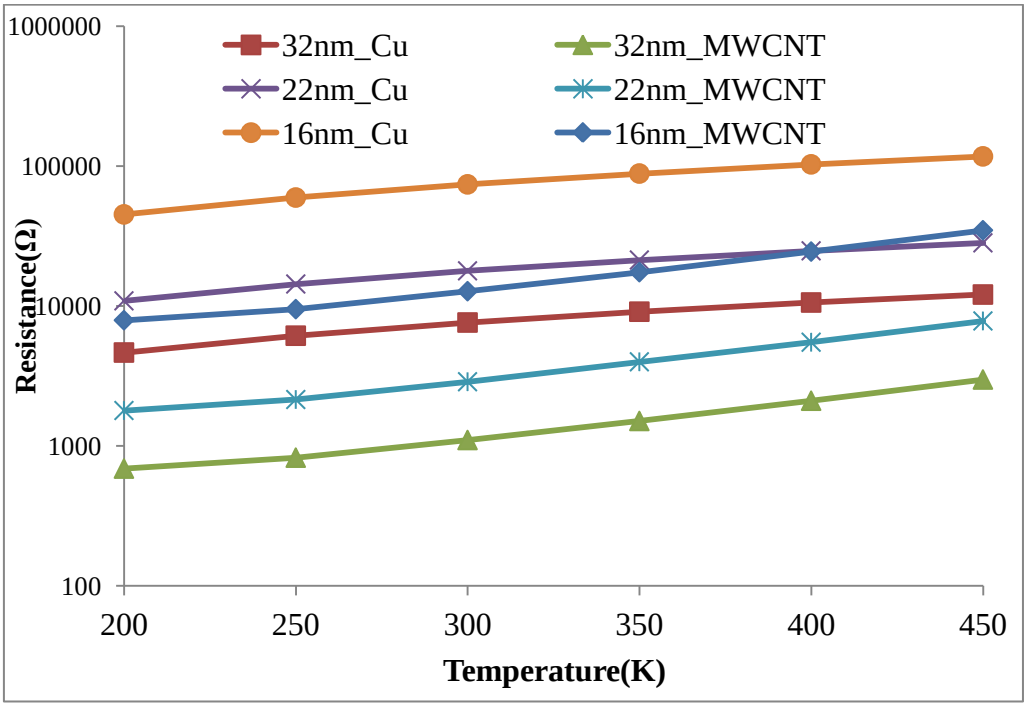
This chapter presents the temperature dependent comparative results and its analysis in terms of propagation delay, power dissipation and Power Delay Product (PDP) for MWCNT bundle, SWCNT bundle and copper interconnects at 32nm, 22nm and 16nm technology nodes for global interconnects. The chapter 3 presents the temperature dependent equivalent RLC impedance models for MWCNT bundle, SWCNT bundle and copper interconnects. In chapter 4, the influence of temperature on the performance of in terms of resistance, propagation delay, power dissipation and Power Delay Product (PDP) for MWCNT bundle is presented for different global interconnects lengths at three different technology nodes viz. 32nm, 22nm and 16nm.

6.2. Temperature Dependent Performance Analysis of MWCNT bundle and Copper interconnects

For the comparative analysis, the temperature dependent impedance parameters for copper are obtained by using the mathematical models presented in chapter 3 (using Eqs. 3.39-3.43). All the simulation parameters used for calculation are obtained from ITRS 2013 edition as summarized in table 4.1. The MATLAB is used to write the script for these calculations. The comparison of temperature dependent resistance for MWCNT bundle and copper interconnects is shown in Figure 6.1.



(a)



(b)

Figure 6.1: Temperature dependent resistance of MWCNT bundle and copper interconnect for 32nm, 22nm and 16nm technology nodes for global interconnects (1mm interconnect length). (a) The resistance shown on linear scale. (b) The resistance shown on logarithm scale.

Figures.6.1(a) and (b) show the calculated resistances of MWCNT bundle and copper interconnects as a function of temperature for 1mm length at 32nm, 22nm and 16nm

technology nodes on linear and logarithmic scale respectively. It is observed that with rise in temperature ranging from 200K to 450K, the resistance of MWCNT bundle interconnects increases which is due to decrease in the MFP. The MFP decreases due to the increase in the collision rates within MWCNT with rise in temperature (from Eqs. 3.6 to 3.12). A similar type of effect observed in copper interconnects (see Eqs. 3.39 to 3.43). It is also revealed from the results that the resistance offered by copper interconnects is several times higher than MWCNT bundle interconnect for temperature ranging from 200K to 450K at 32nm, 22nm and 16nm technology nodes for global interconnects.

6.2.1. Comparative analysis of MWCNT and Copper interconnects in terms of Delay, Power and PDP

Further, the performance in terms of delay, power and PDP of MWCNT bundle interconnects is estimated and compared with the copper interconnect for variable temperature range (200K-450K). A schematics structure used as simulation setup for interconnects is shown in Figure 6.2. A pulse signal with equal rise and fall time is applied as input to interconnects. The 'interconnect' can be replaced by an equivalent temperature dependent circuit models for MWCNT bundle and copper interconnect.

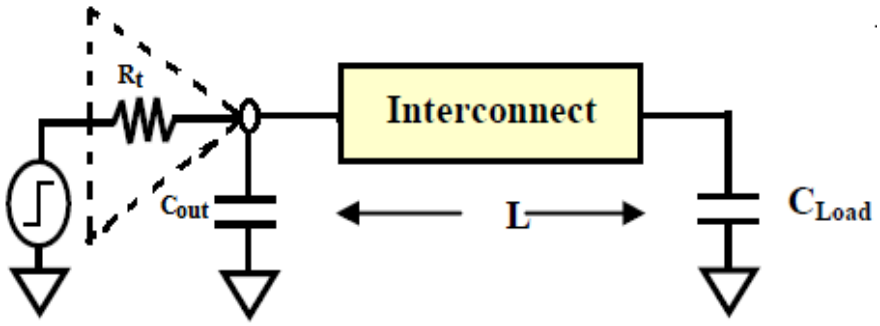


Figure 6.2: Schematic of circuit used for evaluation [95].

The calculated impedance parameters for MWCNT bundle and copper interconnect using the equivalent models has been simulated to evaluate the performance in terms of delay, power and PDP for distributed RLC model for interconnects by using the SPICE simulation tools as shown in Figure 6.3 [127].

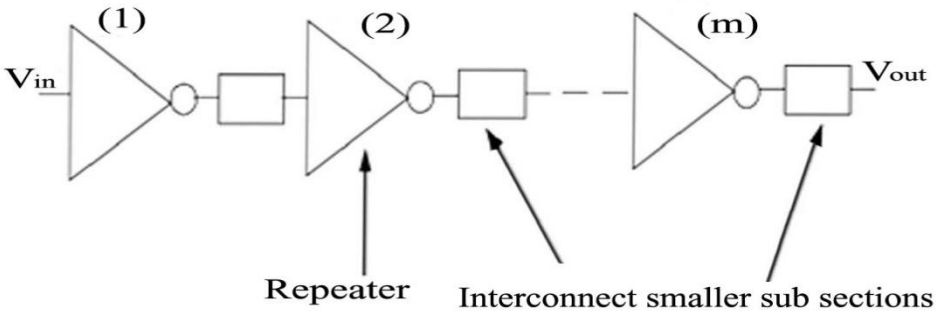


Figure 6.3: 'm' number of repeaters driving an interconnect divided into subsections as distributed model.[29]

Repeaters are normally inserted to increase the drive capability and reduce the delay [38, 131, 138]. The ITRS interconnect parameters used for simulation model are also summarized in table 4.1. The optimum number of repeaters, size of repeater, frequency and PTM model file chosen for different technology nodes as mentioned in table 6.1.

Table 6.1: Simulation parameters for different technology nodes [16, 137]

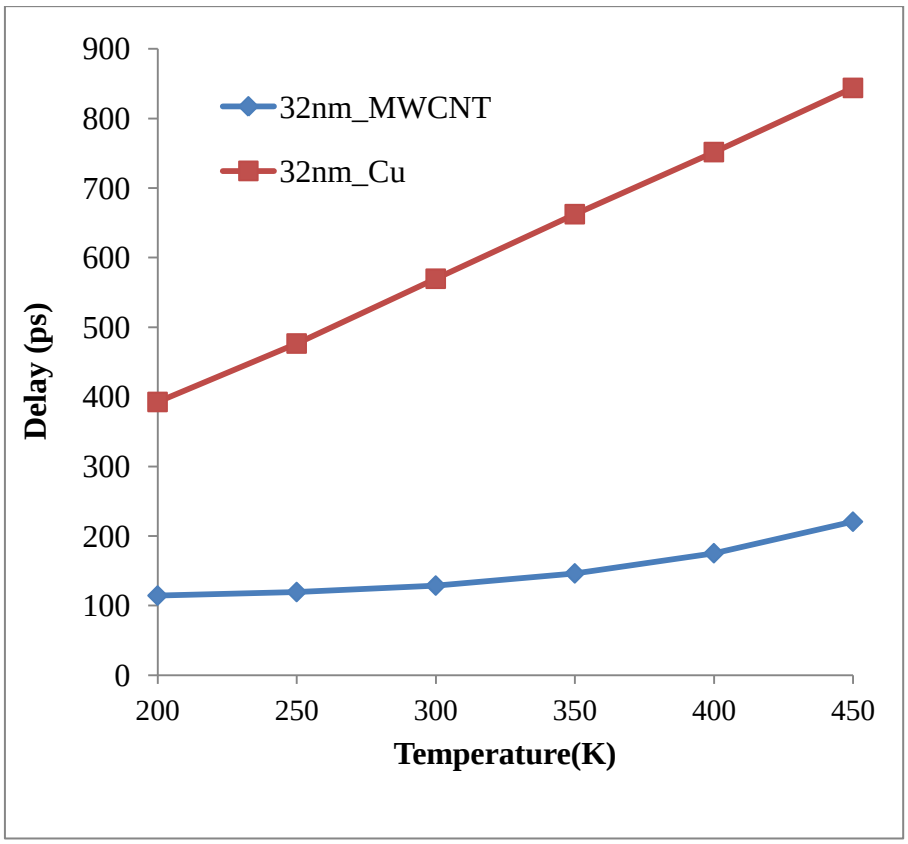
Technology Node	32nm	22nm	16nm
Frequency (GHz)	1	1	1
Repeater size (W/L)	50	50	60
Load Capacitance (fF)	10	10	10
No. of Repeaters	12	12	10
Model file(PTM)	54	54	54

The comparison of temperature dependent delay between MWCNT bundle and copper interconnects for 1mm length at three different technology nodes viz. 32nm, 22nm and 16nm is shown in Figure 6.4.

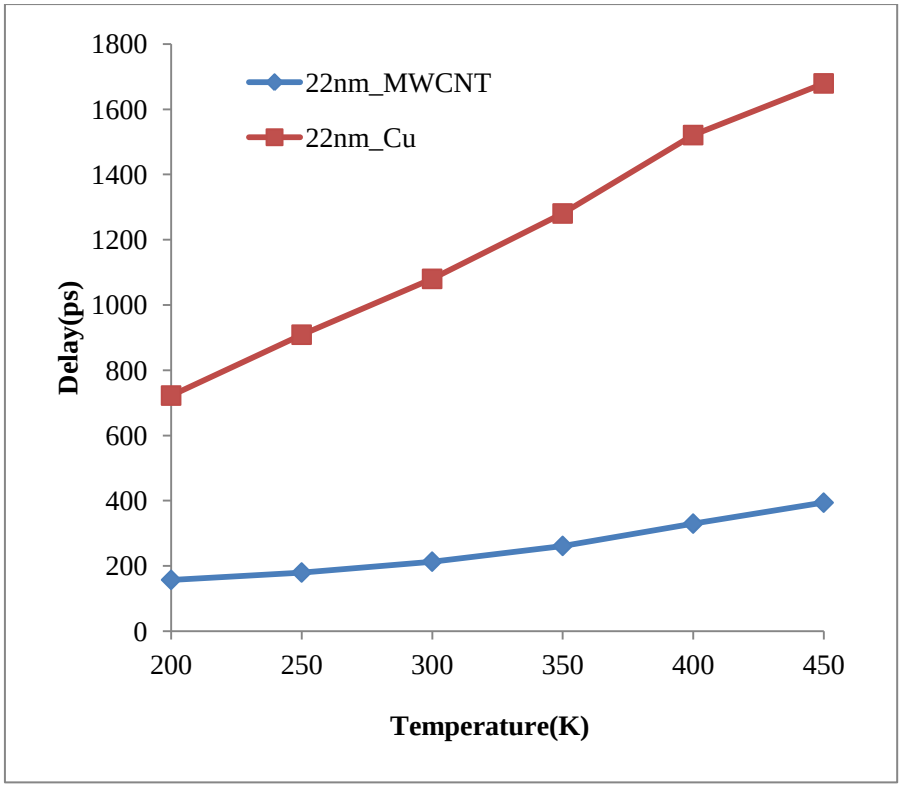
Figures 6.4(a), (b) and (c) show comparison of performance of MWCNT and copper interconnect in terms of delay for 1mm interconnect length at 32nm, 22nm and 16nm technology nodes respectively for a temperature range 200K to 450K. It is observed that the delay increases with increasing temperature for both MWCNT bundle and copper interconnects which is due to shrinking of MFPs. It is also revealed that the delay of MWCNT bundle interconnects is smaller as compare to copper interconnects and there is improvement in delay performance in MWCNT bundle interconnects for global

interconnects length compared to copper interconnects with increasing temperature from 200K to 450K at three technology nodes under consideration.

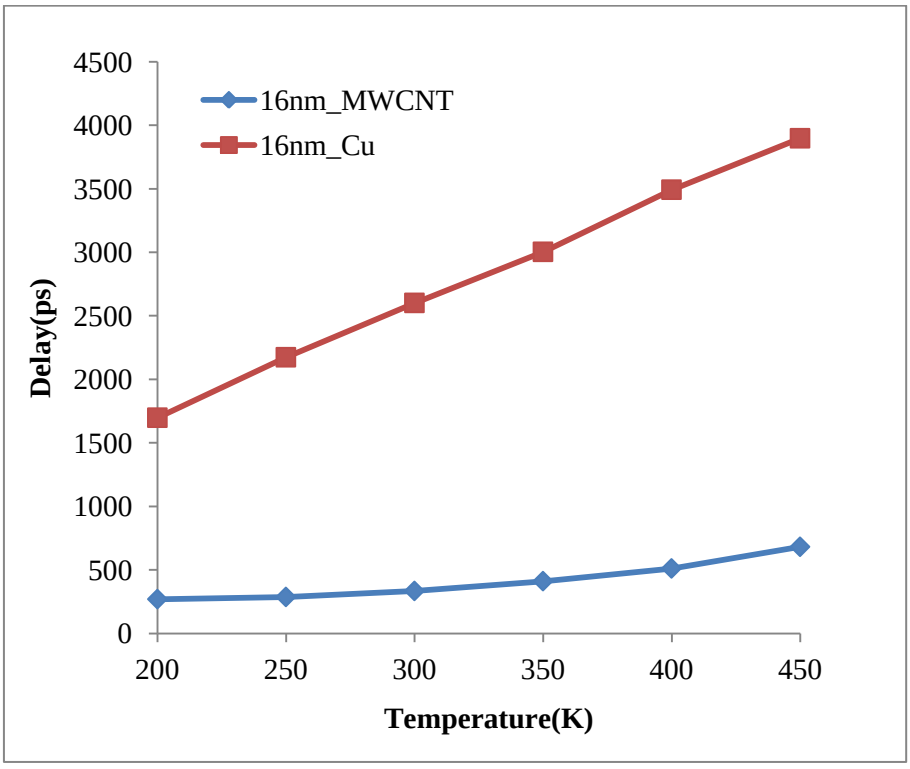
Figure 6.4(d) shows the relative delay ratio which is ratio of delay of MWCNT to copper interconnects for temperature range 200K to 450K at different technology nodes (32nm, 22nm and 16nm). It is revealed from the results that the delay ratio for the technology nodes (32nm, 22nm and 16nm) is less than unity, which suggested that MWCNT bundle offered lower delay as compare to copper interconnects. The similar trend is observed for whole temperature range i.e. 200K-450K. Further, as technology scaled down, the delay ratio is in decreasing order, which advocating MWCNT bundle interconnects as better candidate for deep sub micron technology nodes. Therefore, it is concluded that the performance of MWCNT bundle interconnects in terms of delay, is better than that of copper interconnects for global interconnects length at deep submicron technology nodes for variable temperature, ranging from 200K to 450K.



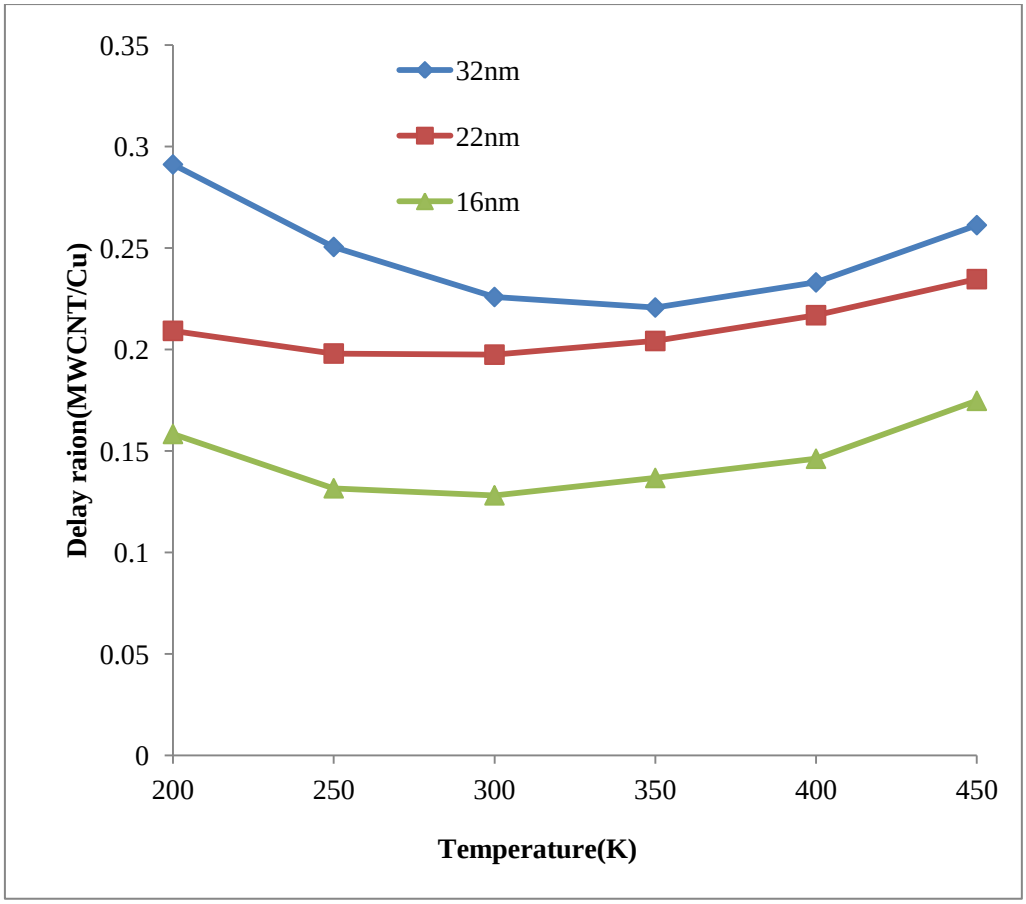
(a)


1800
1600
1400
1200
1000
800
600
400
200
0
Delay(ps)
22nm_MWCNT
22nm_Cu
200
250
300
350
400
450
Temperature(K)

(b)


4500
4000
3500
3000
2500
2000
1500
1000
500
0
Delay(ps)
16nm_MWCNT
16nm_Cu
200
250
300
350
400
450
Temperature(K)

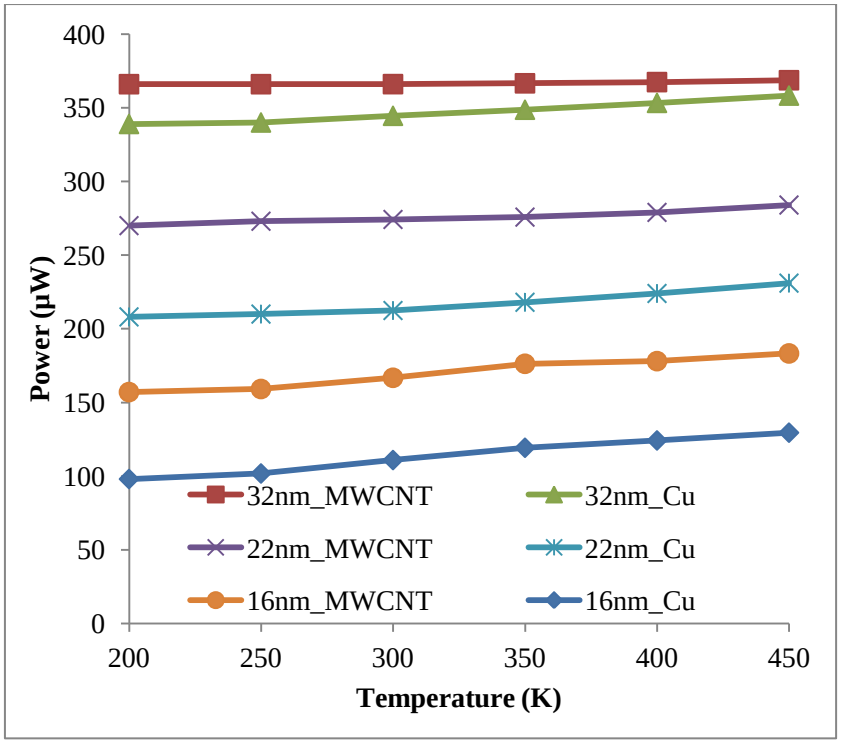
(c)



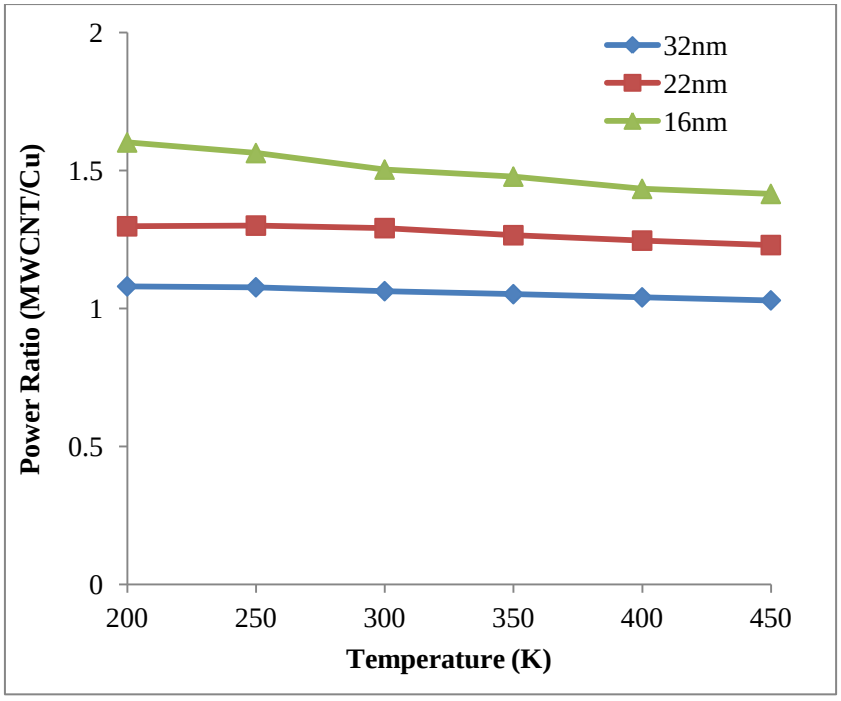
(d)

Figures 6.4: (a), (b) and (c) Performance comparison of MWCNT bundle and copper interconnects in terms of delay for 1mm interconnects length at 32nm, 22nm and 16nm technology nodes respectively. (d) Comparison of performance of MWCNT and copper interconnect in terms of delay ratio (MWCNT/Cu) for 1mm interconnects length at 32nm, technology node.

Figure 6.5(a) shows the temperature dependent performance of MWCNT bundle and copper interconnects in terms of power. The ratio of average power dissipation will be referred to as 'relative power' as shown in Figure 6.5(b). It is observed from results that the power dissipation is more in the case of MWCNT bundle interconnects compared to copper interconnects and it is because of large tube capacitance of MWCNT bundle.

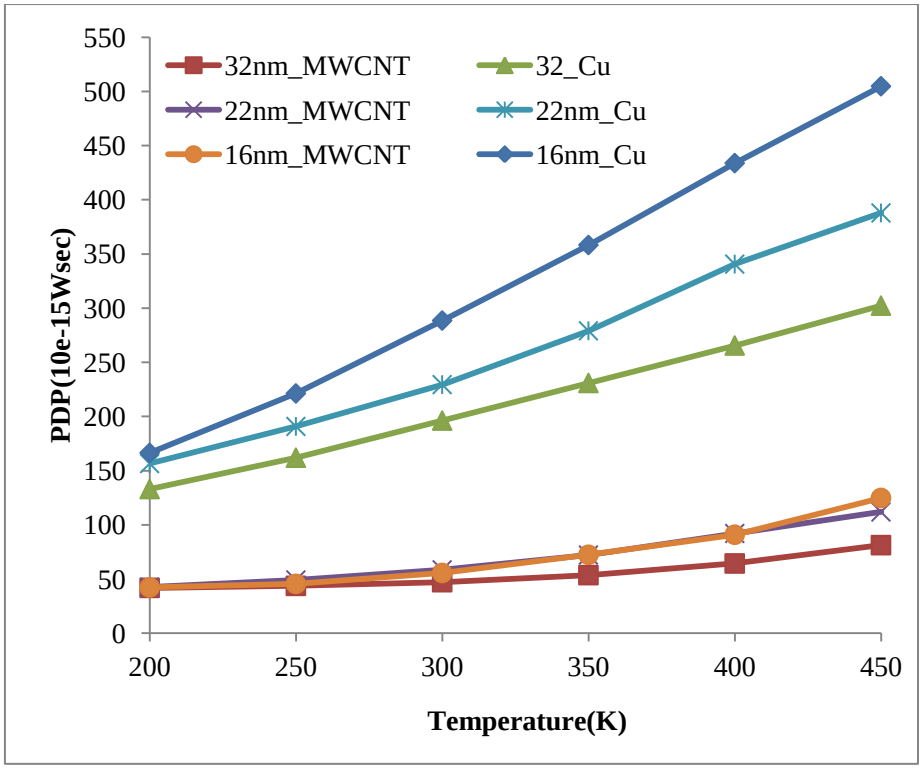


(a)

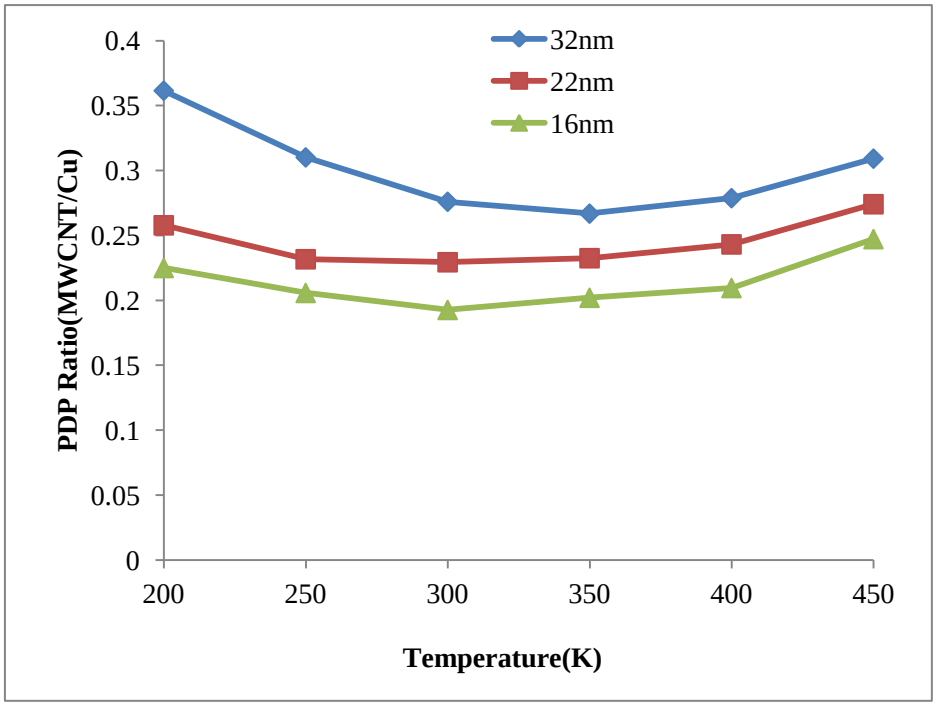


(b)

Figure 6.5: (a) Comparison of performance of MWCNT and copper interconnect in terms of power for 1mm interconnects length at 32nm, 22nm and 16nm technology nodes respectively. (b) Comparison of performance of MWCNT and copper interconnect in terms of power ratio (MWCNT/Cu).



(a)



(b)

Figure 6.6: (a) Comparison of performance of MWCNT and copper interconnect in terms of Power Delay Product (PDP) for 1mm interconnects length at 32nm, 22nm and 16nm technology nodes respectively. (b) Comparison of performance of MWCNT and copper interconnect in terms of PDP ratio (MWCNT/Cu).

Figure 6.6 shows the comparative analysis for MWCNT and copper interconnects in terms of Power Delay Product (PDP) for 1mm interconnects length at three different technology nodes viz. 32nm, 22nm and 16nm. Figure 6.6(a) shows the comparison of temperature dependent Power Delay Product (PDP) for MWCNT bundle and copper interconnect and Figure 6.6(b) shows the comparison of performance of MWCNT bundle and copper interconnect in terms of PDP ratio (MWCNT/Cu). It is observed that the rise in temperature ranging from 200K to 450K effects performance in terms of PDP in case of MWCNT and copper interconnects. A bunch of three waveforms shown in Figure 6.6(a), which represents the PDP for copper, is placing well above the other bunch of three waveforms which represent the PDP for MWCNT bundle interconnects. Therefore, the performance in terms of PDP for MWCNT bundle interconnects is better than copper for all three technology nodes (32nm, 22nm and 16nm). Further, PDP ratio for all the technology nodes under consideration is less than unity as shown in Figure 6.6(b). Furthermore, the PDP ratio is decreasing with technology scaled down nodes. Hence, it is shown in the results that the performance in terms of PDP of MWCNT bundle interconnects is several times better than the performance of copper interconnects.

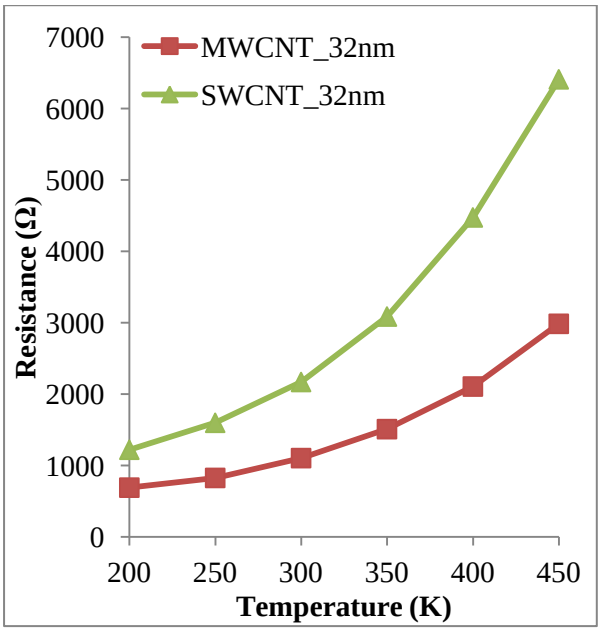
6.3. Temperature dependent performance analysis for MWCNT bundle and SWCNT bundle Interconnects

This section of chapter presents the temperature dependent analysis of MWCNT bundle and SWCNT bundle interconnects, which investigates the effect of variable temperature on the performance for global interconnects of CNT at 32nm, 22nm and 16nm technology nodes. As per discussion in section 3, the MFP is the most effective parameter of MWCNT bundle and SWCNT bundle for temperature ranging from 200K to 450K. The MFP of CNTs is affected by electron-phonon scattering mechanism at different temperatures. The affected MFP influence the impedance parameters mainly resistance of CNTs and hence the overall resistance of MWCNT bundle and SWCNT bundle interconnects exaggerated. These temperature dependent impedance parameters influence the performance of both MWCNT bundle and SWCNT bundle interconnects in terms of propagation delay, power dissipation and PDP. The temperature dependent effective MFP for an individual shell of SWCNT bundle is calculated using Eqs 3.6 to 3.12 for temperature ranging from 200K to 450K. With this effective MFP, the equivalent resistance of SWCNT bundle is obtained by considering the resistances of all shells in parallel and calculated using Eq. 3.28. The total number of

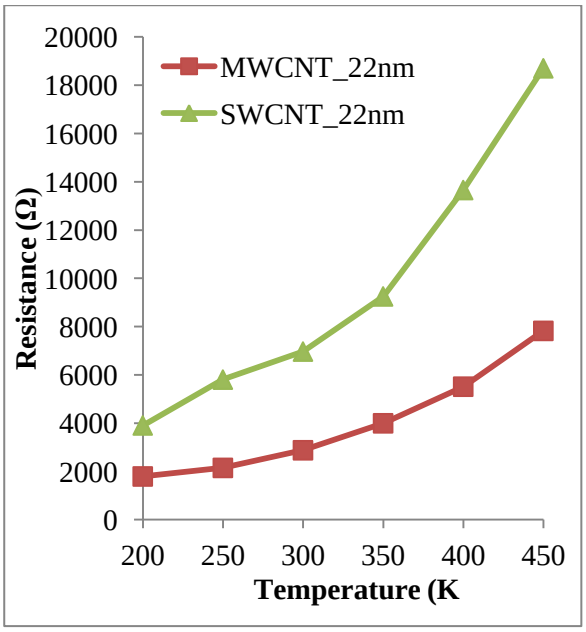
conducting SWCNTs in a bundle depends upon the technology node and calculated using Eqs. 3.29-3.34. All interconnect parameters used for calculations are obtained from ITRS 2013 based simulation parameters.

Calculations for inductance and capacitance of SWCNT bundle are obtained using Eqs. 3.35-3.38. These equations (Eqs. 3.35-3.38) show that the inductance and capacitance of SWCNT bundle interconnect is independent from effective MFP and therefore the effect of temperature on inductance and capacitance is not been considered.

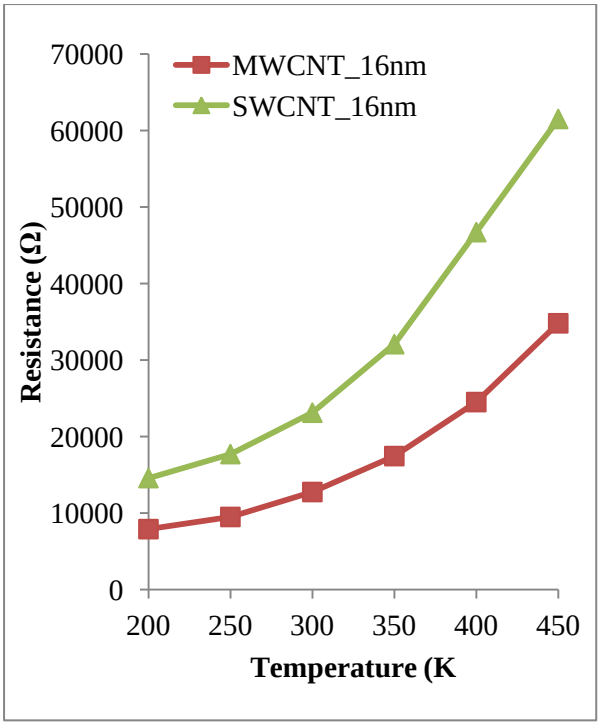
Figures 6.7(a), (b) and (c) show the comparison of temperature dependent resistances of MWCNT bundle interconnects and SWCNT bundle interconnects at 32nm, 22nm and 16nm technology nodes respectively for 1mm interconnects length. It is observed that the resistance of MWCNT and SWCNT increases with rise in temperature ranging from 200K to 450K. It is due to decrease in the effective MFP of CNTs. This decrease in MFP is due to the increase in the collision rates within MWCNT and SWCNT with rise in temperature (Eqs. 3.6 to 3.12). Figure 6.7(d) shows the comparison of temperature dependent resistance of MWCNT and SWCNT interconnects for three technology nodes (32nm, 22nm and 16nm) with logarithmic scale. It is also observed that the resistance offered by MWCNT bundle interconnect is lower than that of SWCNT bundle interconnect for different temperature ranging from 200K to 450K at 32nm, 22nm and 16nm technology nodes. Further, the influence of temperature is increases for scaled down technology nodes.



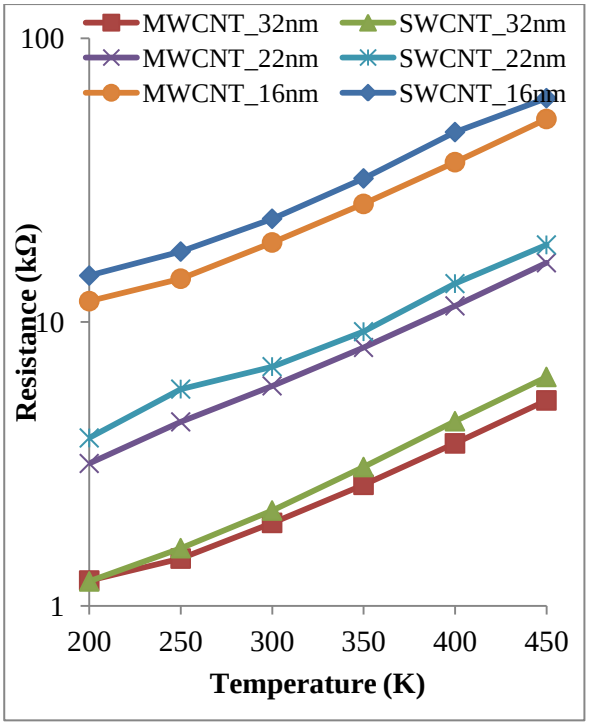
(a)



(b)



(c)



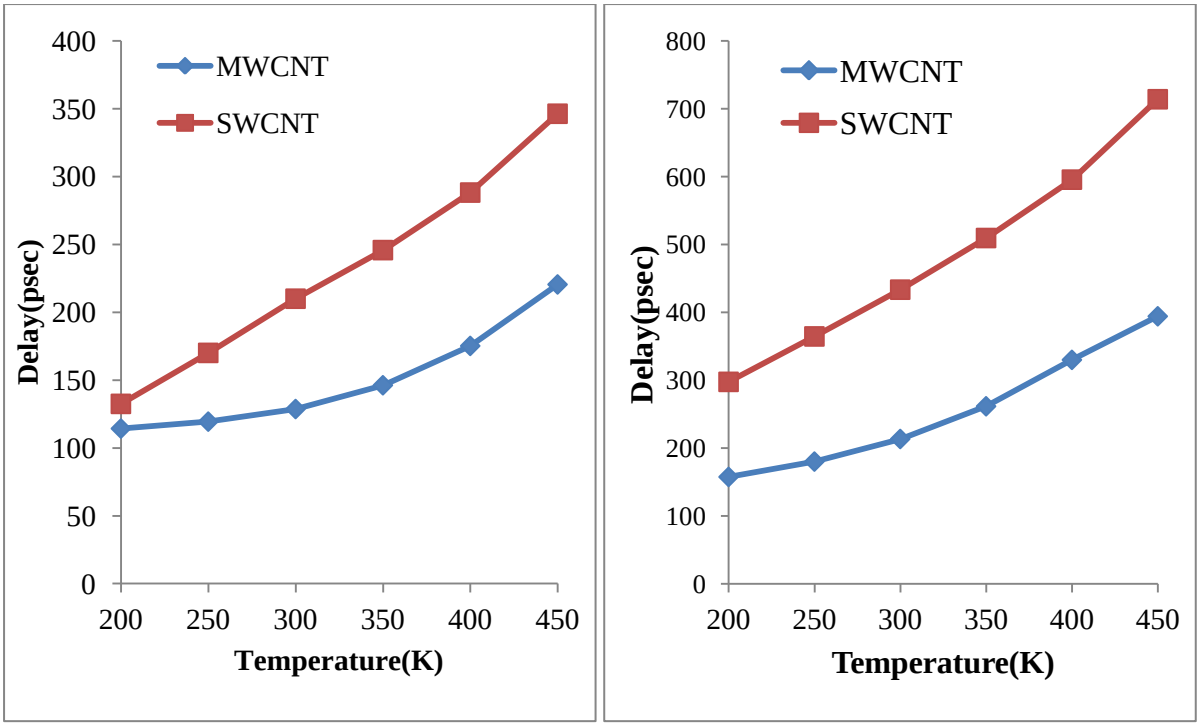
(d)

Figures 6.7: (a), (b) and (c) show temperature dependent resistance of MWCNT bundle and SWCNT interconnect for 32nm, 22nm and 16nm technology nodes for global interconnect respectively at 1mm interconnect length. (d). Resistance shows on logarithm scale for 32nm, 22nm and 16nm technology nodes.

6.3.2 Performance Analysis MWCNT and SWCNT interconnects in terms of Delay, Power and PDP

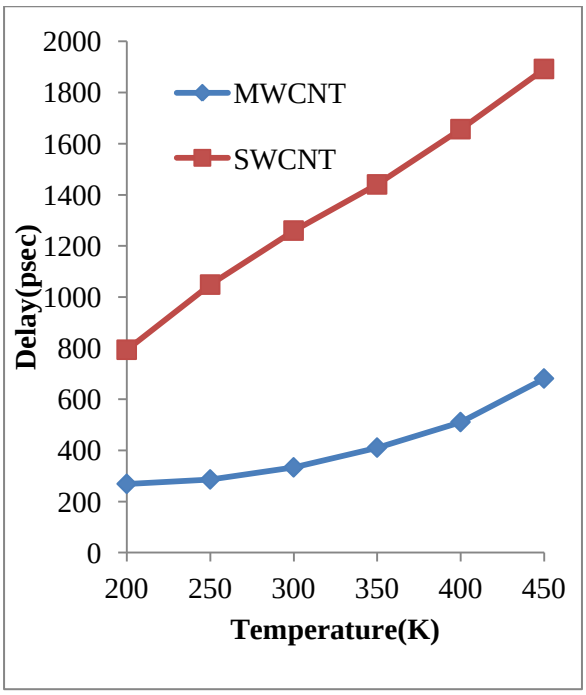
In this sub-section the performance of SWCNT bundle interconnect is estimated and compared with the MWCNT bundle interconnect for different technology modes. The calculated temperature dependent impedance parameters for MWCNT bundle and SWCNT bundle interconnects using the equivalent models is simulated using SPICE simulation tools to evaluate the performance in terms of delay, power and PDP for distributed RLC model for interconnects.

The temperature dependent performance in terms of delay is compared between MWCNT bundle and SWCNT bundle interconnects for 1mm interconnect length at three different technology viz. 32nm, 22nm, 16nm at variable temperature ranging from 200K to 450K as shown in Figure 6.8. Figures 6.8(a), (b) and (c) show the temperature dependent delay for MWCNT bundle interconnects and SWCNT bundle interconnects for 32nm, 22nm and 16nm technology nodes at 1mm interconnects length.

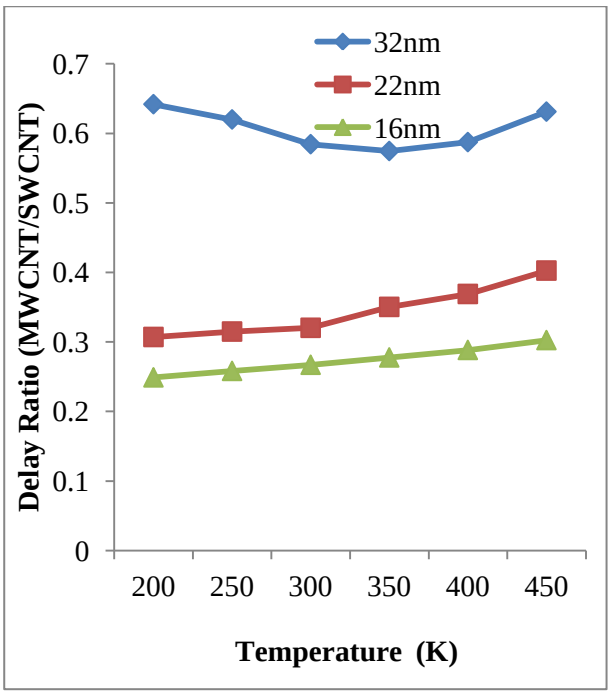


(a)

(b)



(c)



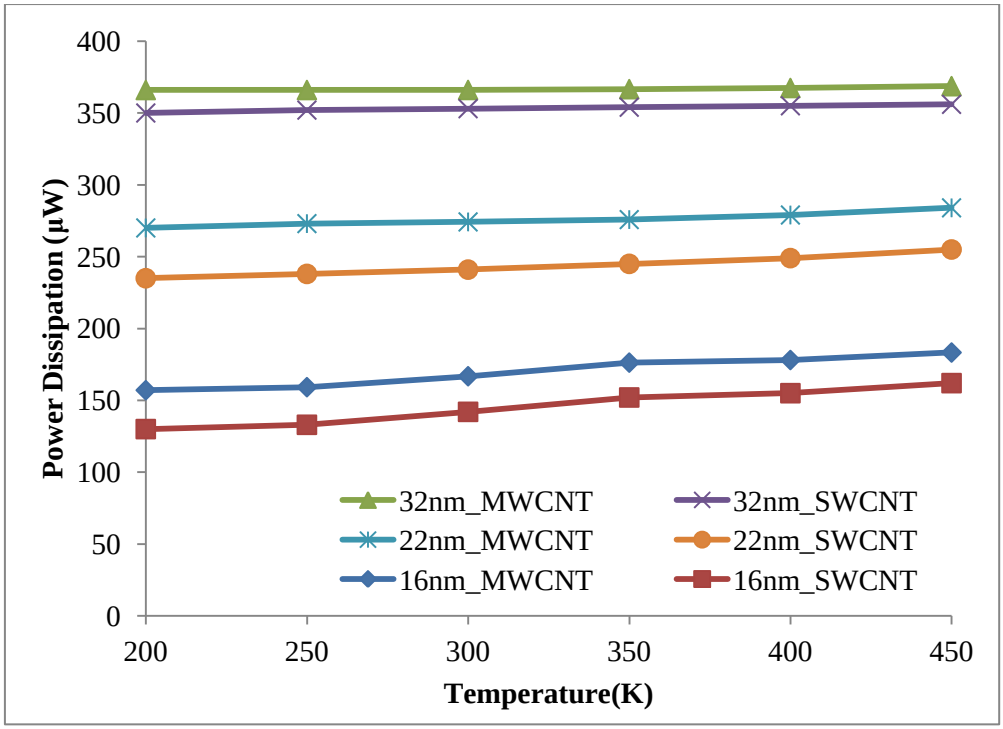
(d)

Figures 6.8: (a),(b) and (c). Comparison of performance of MWCNT bundle and SWCNT bundle interconnect in terms of delay at 1000µm interconnect length for 32nm, 22nm and 16nm technology nodes respectively. (d) Comparison of performance of MWCNT bundle and SWCNT bundle interconnect in terms of relative delay ratio (MWCNT/SWCNT).

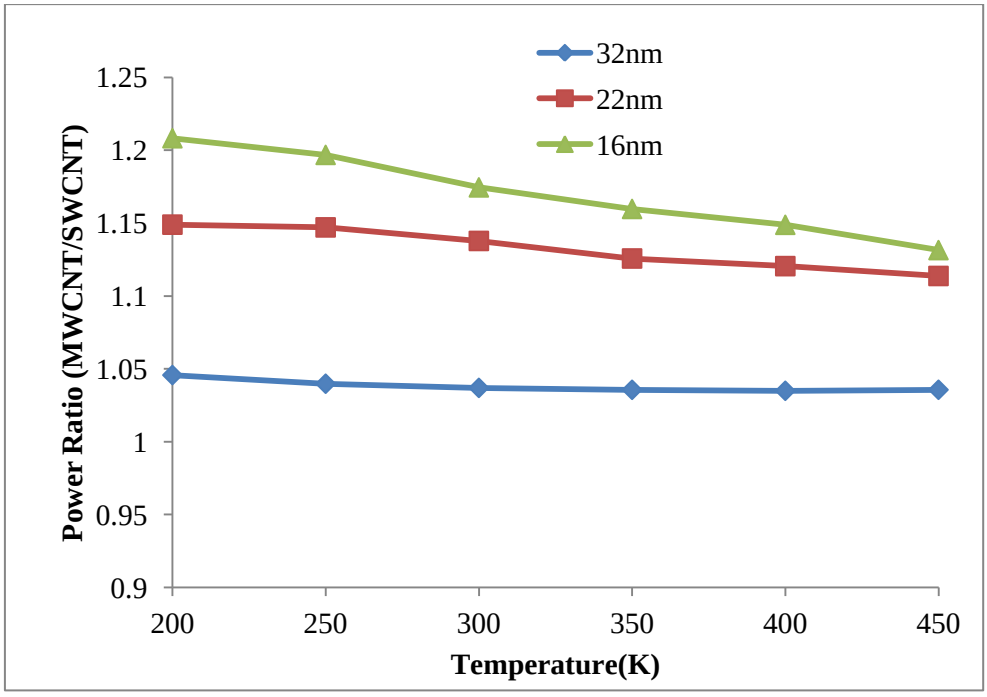
It is observed from the results that the delay increases with increasing temperature for both MWCNT bundle and SWCNT bundle interconnects for all three technology nodes. This increase in delay is because of reduction in MFPs of the tubes (see Eqs.3.7-3.12). It is also found that the delay of SWCNT bundle interconnects compared to MWCNT bundle interconnects, increased rapidly as the temperature increases from moderate to high temperature range for all three technology nodes. Therefore, it is revealed from the results that the delay offered by MWCNT bundle interconnects is smaller than that of its counterpart SWCNT bundle interconnects and there is improvement in the performance in terms of delay for MWCNT bundle interconnects as compare to SWCNT bundle interconnects with rise in temperature.

Figure 6.8(d) shows the relative delay ratio, which is delay ratio of MWCNT bundle interconnect to SWCNT bundle interconnects delay different temperature range at 32nm, 22nm and 16nm technology nodes. The relative delay ratio for all the technology nodes under consideration is less than unity which indicates that the delay offered by MWCNT bundle interconnects is smaller than the SWCNT bundle interconnects. It is also revealed from Figure 6.8(d) that the performance in terms of delay ratio of MWCNT bundle interconnects compared to SWCNT bundle interconnects, gives better results with scaled down in technology nodes viz. 32nm, 22nm and 16nm for temperature ranging from 200K to 450K. So the performance in terms of delay for MWCNT bundle interconnects is better than the performance of SWCNT bundle interconnects for advanced technology nodes at global interconnects length for moderate to high temperature range.

Figure 6.9 shows the temperature dependent performance of MWCNT bundle and SWCNT bundle interconnects in terms of power dissipation. Figure 6.9(a) show the comparison of performance in terms of power dissipation for MWCNT bundle and SWCNT bundle interconnect for 1000µm interconnect length at 32nm, 22nm and 16nm technology nodes. The ratio of average power of MWCNT bundle to SWCNT bundle interconnects is referred to as ‘relative power ratio’ as shown in Figure 6.9(b). It is found that the power dissipation for MWCNT bundle is slightly higher compared to SWCNT bundle interconnects and it is due to higher tube capacitance in case of MWCNT bundle. As technology nodes scaled down (from 32nm to 16nm) under variable temperature, the power dissipation ratio improved in favour of MWCNT bundle interconnects particularly at 16nm technology. The results show that the power dissipation ratio is almost constant for 32nm technology nodes, where it reduces from 1.3 to 1.1 for 16nm technology node for temperature ranging 200K to 450K.



(a)



(b)

Figure 6.9: (a) Comparison of performance of MWCNT bundle and SWCNT bundle interconnect in terms of power for 1000µm interconnect length at 32nm, 22nm and 16nm technology nodes. (b) Comparison of performance of MWCNT bundle and SWCNT bundle interconnect in terms of relative power ratio (MWCNT/SWCNT).

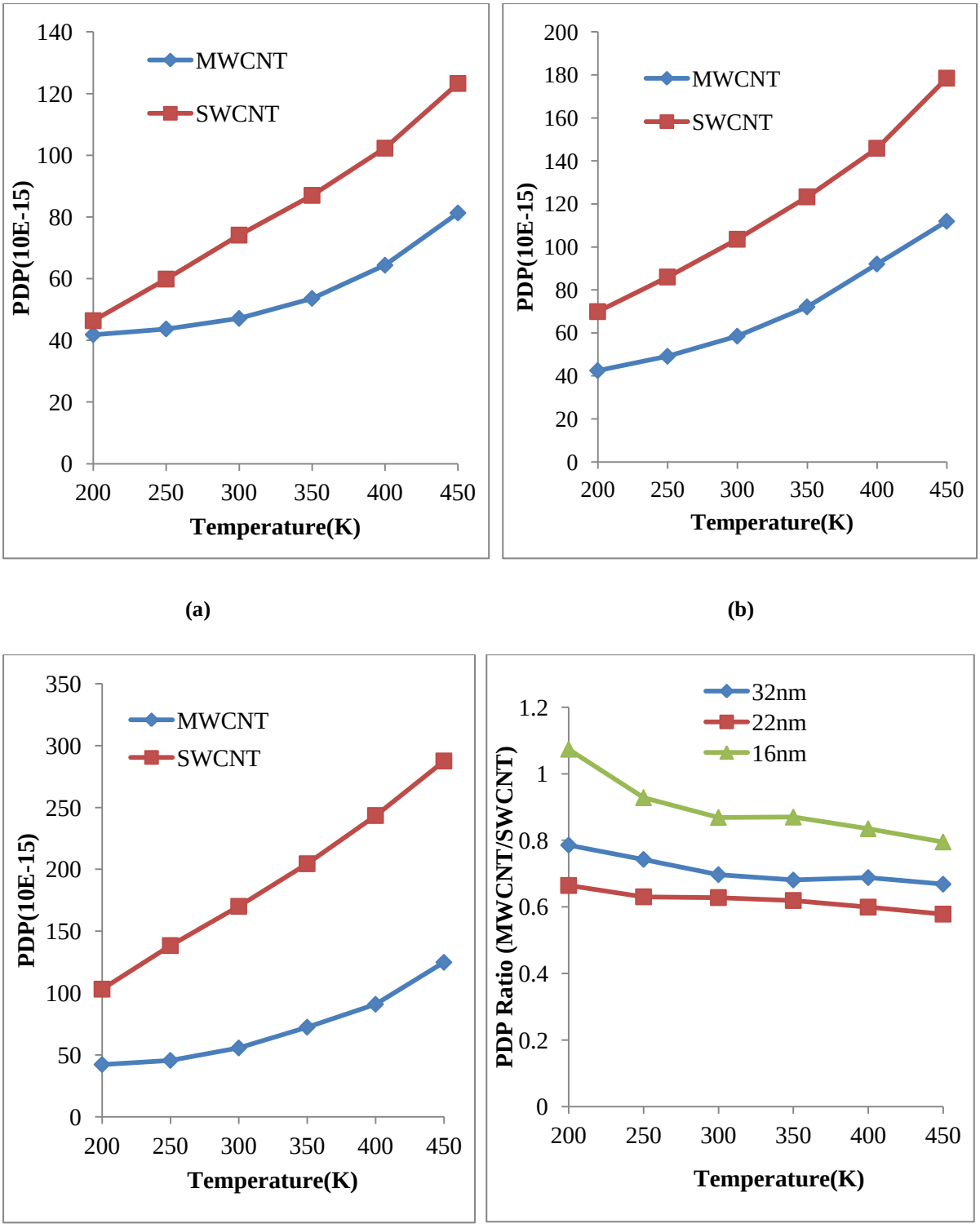


Figure 6.10: (a), (b), and (c) Comparison of performance of MWCNT bundle and SWCNT bundle interconnects in terms of Power Delay Product (PDP) for 1mm interconnect length at 32nm, 22nm and 16nm technology nodes respectively. (b) Comparison of performance of MWCNT bundle and SWCNT bundle interconnects in terms of relative PDP ratio (MWCNT/SWCNT).

Figure 6.10 shows the performance comparison of Power Delay Product (PDP) for MWCNT bundle and SWCNT bundle interconnects for temperature ranging from 200K to 450K for 1mm interconnects length at three technology nodes (32nm, 22nm and 16nm). Figures 6.10(a), (b) and (c) show the comparative results for MWCNT bundle interconnects and SWCNT bundle interconnects in terms of Power Delay Product (PDP) for 32nm, 22nm and 16nm technology nodes respectively. It is revealed from the results that with increase in temperature, the performance in terms of PDP for of MWCNT bundle and SWCNT bundle interconnects increases for all three technology nodes (32nm, 22nm and 16nm). It is also observed from the results that the PDP for MWCNT bundle interconnects is smaller as compare to SWCNT bundle interconnects at 32nm, 22nm and 16nm technology nodes for variable temperature ranging from 200K to 450K. The gap between SWCNT bundle and MWCNT bundle increases more rapidly with rise in temperature for all three technology nodes. Hence, it is concluded that for higher range of temperatures the performance of MWCNT bundle interconnects outperforms compared to the performance of SWCNT bundled interconnects.

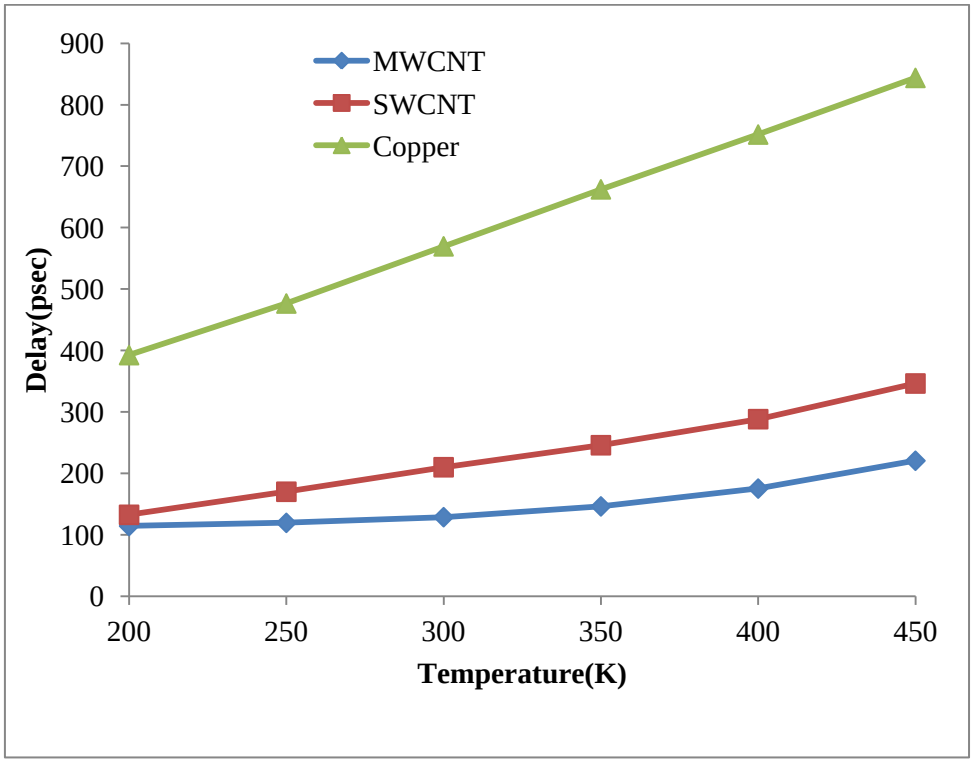
The comparative performance analysis in terms of relative PDP ratio (MWCNT/SWCNT) between MWCNT bundle and SWCNT buddle interconnects presented in Figure 6.10(d) for 32nm, 22nm and16nm technology nodes. The results show that the relative PDP ratio is always less then unity which means the PDP of MWCNT bundle is lesser than PDP of SWCNT bundle for variable temperature range (200K to 450K) at 32nm, 22nm and 16nm technology nodes. It is also revealed from the results that PDP ratio is decreasing with rise in temperature; hence PDP ratio is improving in favors of MWCNT bundle interconnects at moderate to high temperature range..

6.4. Temperature Dependent Performance Analysis of MWCNT bundle, SWCNT bundle and Copper Interconnects

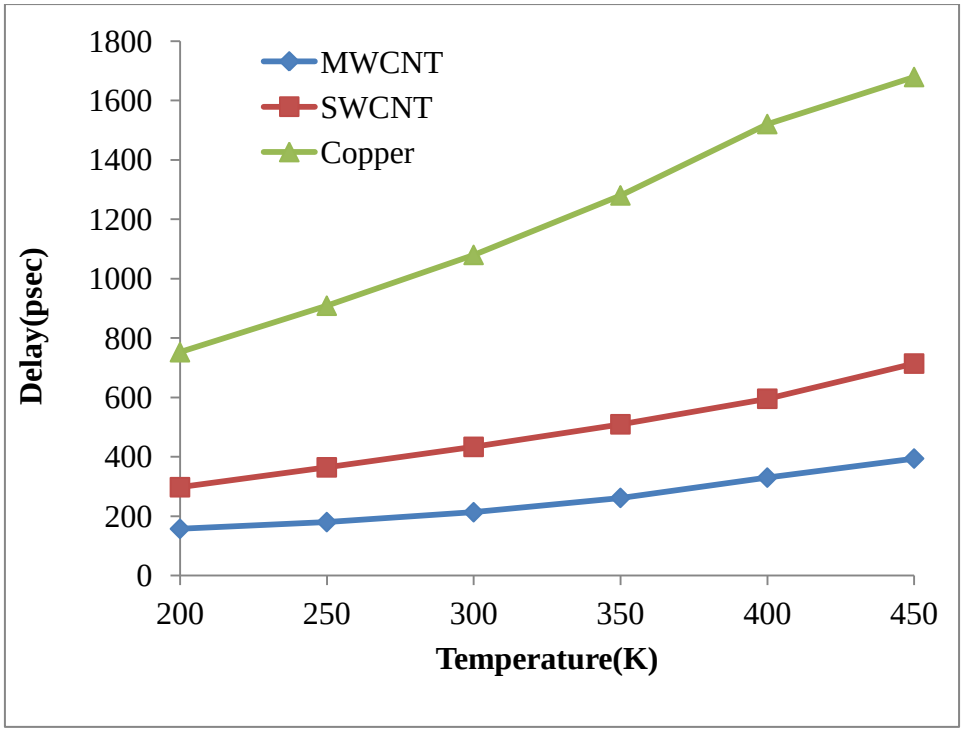
This sub section of this chapter presents the comparative results and its analysis for temperature dependent propagation delay, power dissipation and PDP for MWCNT bundle, SWCNT bundle and copper interconnects at different technology nodes viz. 32nm, 22nm and 16nm for global interconnects. The temperature dependent impedance parameters for MWCNT bundle (using Eqs.3.1-3.20), SWCNT bundle (using Eqs.3.21-3.38) and copper (using Eqs.3.39-3.43) interconnects have already been calculated in section 6.2 and section 6.3 using ITRS 2013 based simulation parameters for global interconnects. The calculated

impedance parameters for MWCNT bundle, SWCNT bundle and copper interconnect using the equivalent models have been simulated to evaluate the performance in terms of delay, power and PDP by using the SPICE simulation tools.

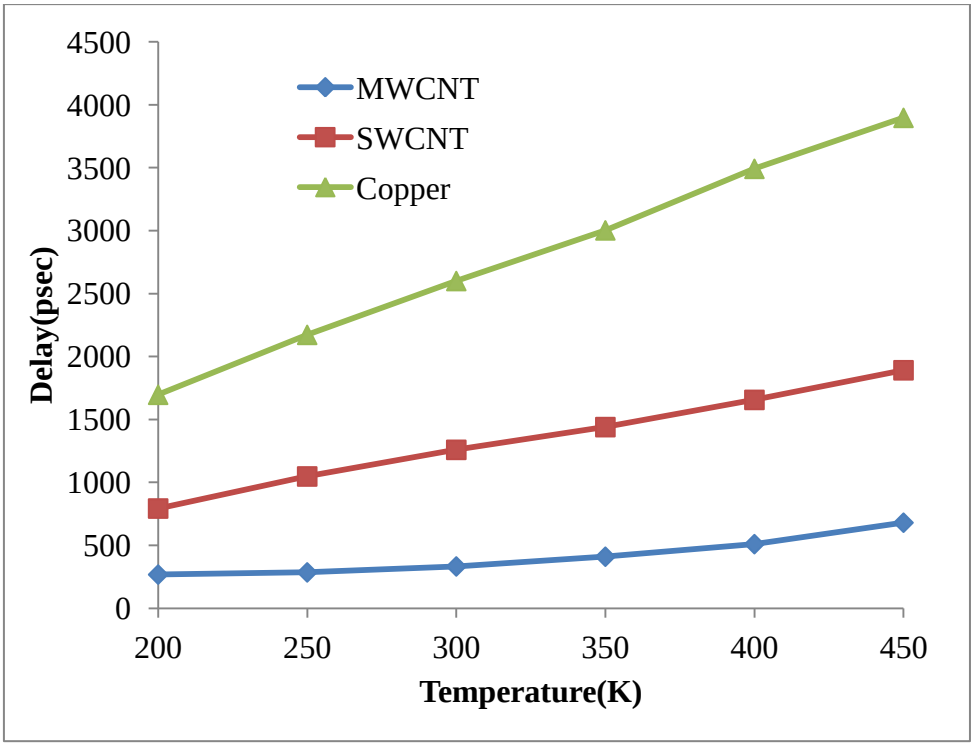
Figures 6.11(a), (b) and (c) show the comparison of performance in terms of delay for MWCNT bundle, SWCNT bundle and copper interconnect for 1mm interconnect length at 32nm, 22nm and 16nm technology nodes respectively for a temperature ranging from 200K to 450K. It can be observed from the results that as temperature increased from 200K to 450K, the delay increases for MWCNT bundle, SWCNT bundle and copper interconnect. It is also found that the delay offered by MWCNT interconnects is smaller than the delay offered by both SWCNT bundle and copper interconnects. It is shown in results that with rise in temperature, there is improvement in delay performance in the case of MWCNT interconnects at global length than its counterpart i.e. SWCNT bundle and copper interconnects. It is also revealed from results that as the technology nodes scaled down, the gap between SWCNT bundle and MWCNT bundle has been increased. The results revealed that the performance of MWCNT is better than that of SWCNT bundle and copper interconnects at variable temperature ranging from 200K to 450K for 32nm, 22nm and 16nm technology nodes.



(a)



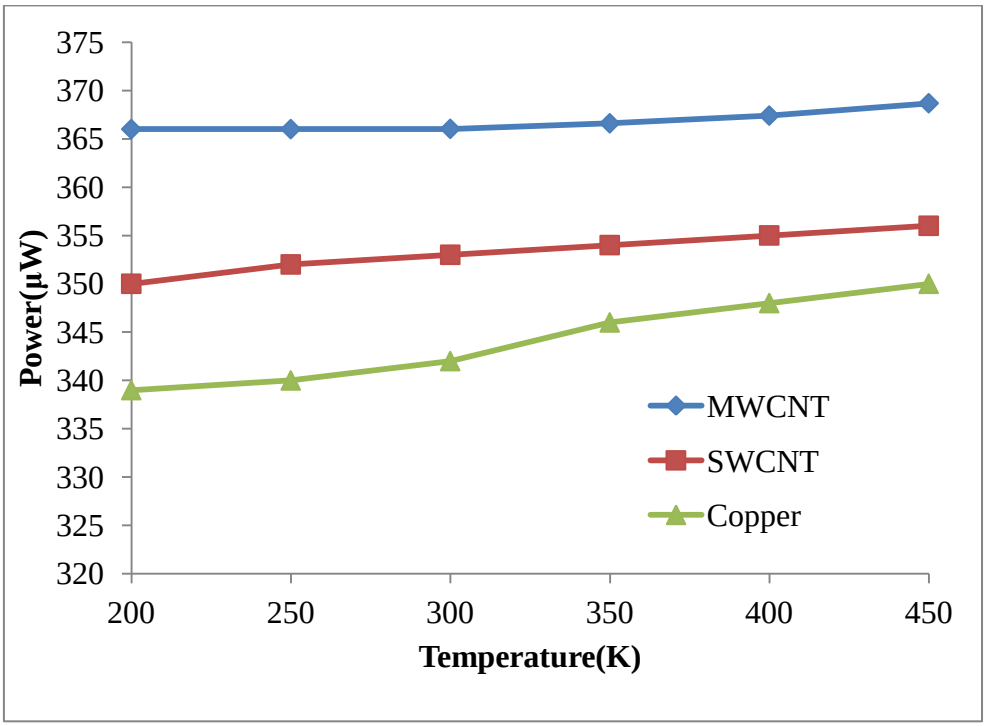
(b)



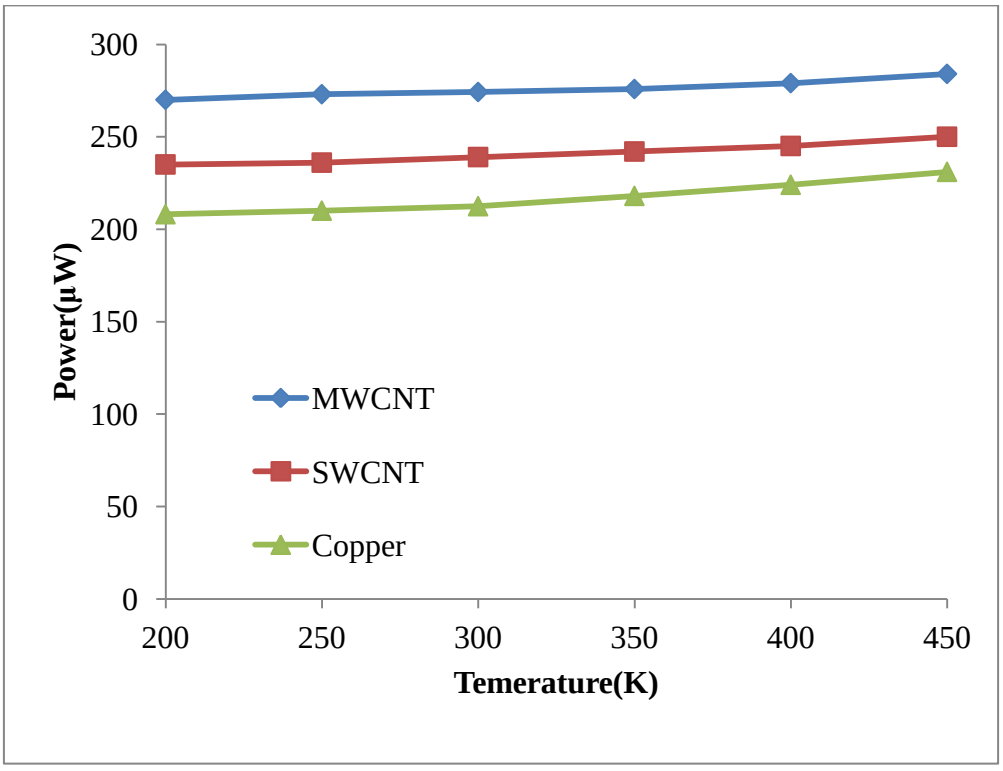
(c)

Figures 6.11: (a), (b) and (c) Comparison of performance in terms of delay of MWCNT bundle, SWCNT bundle and copper interconnects based on 1mm interconnects length at 32nm, 22nm and 16nm technology nodes respectively.

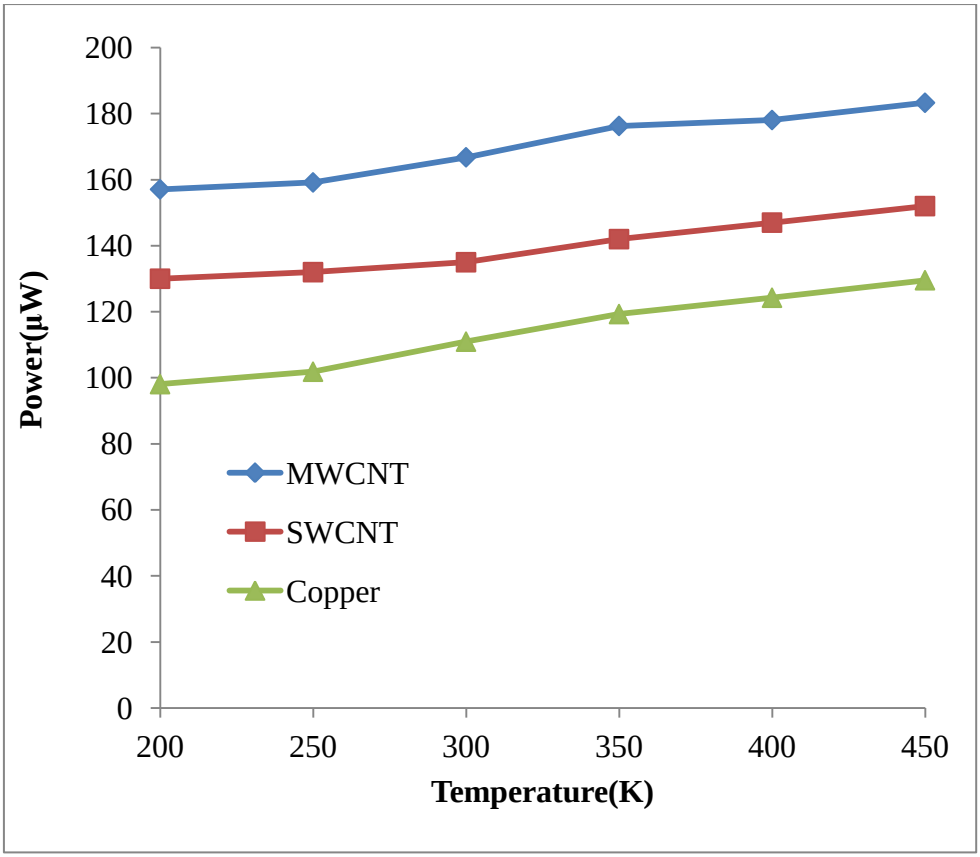
Figures 6.12(a), (b) and (c) show the temperature dependent performance in terms of power dissipation for MWCNT bundle, SWCNT bundle and copper interconnects at 32nm, 22nm and 16nm technology nodes respectively.



(a)



(b)

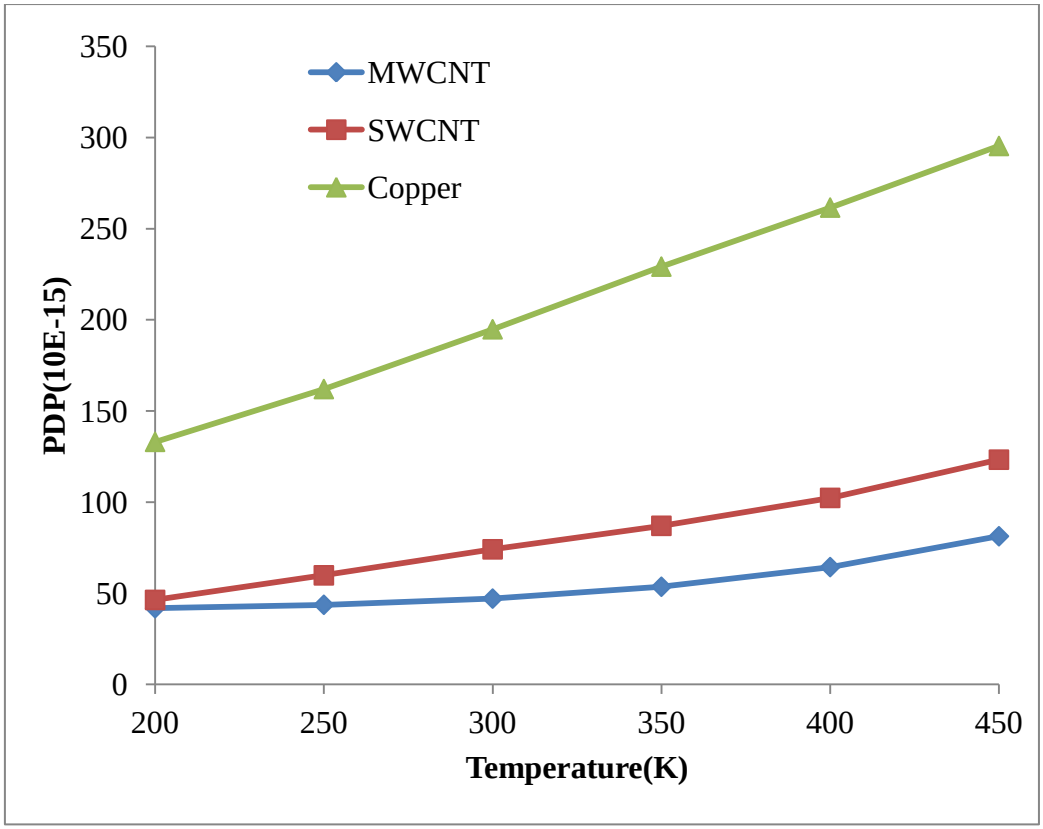


(c)

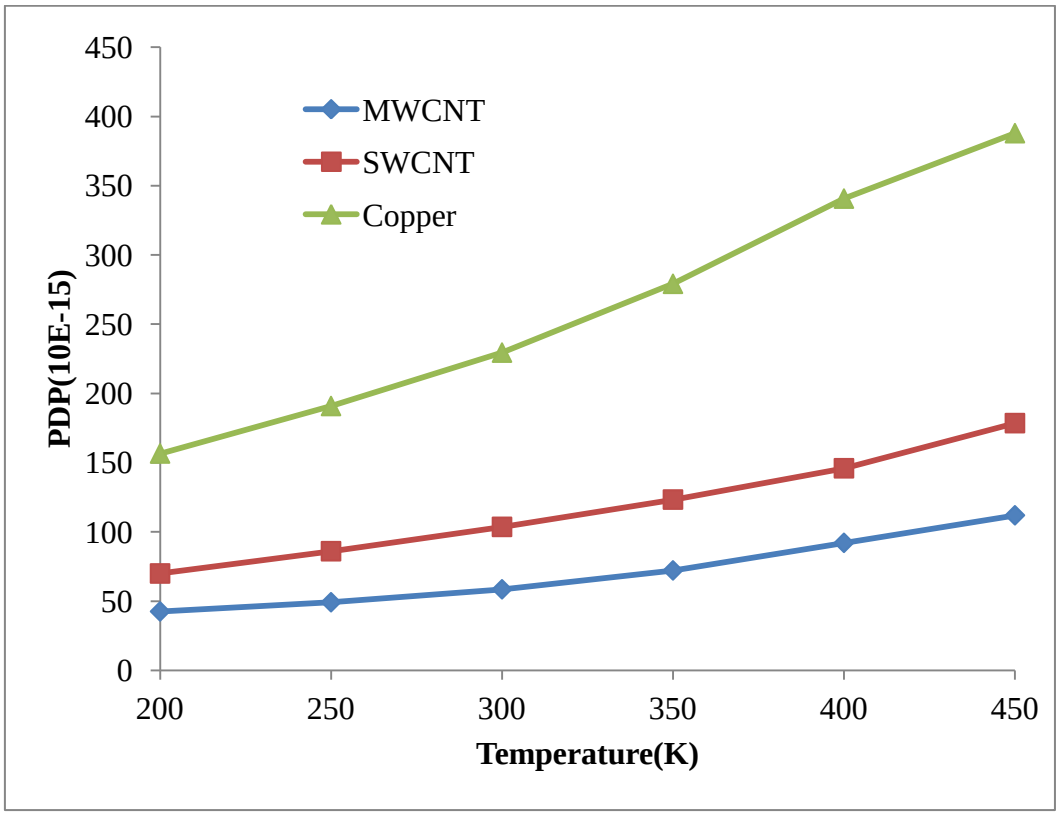
Figures 6.12: (a), (b) and (c) Comparison of performance of MWCNT bundle, SWCNT bundle and copper interconnect in terms of power dissipation for 1mm interconnect length at 32nm, 22nm and 16nm technology nodes respectively.

It is revealed from the results that the power dissipation is more for MWCNT bundle interconnects compared to SWCNT bundle and copper interconnects for temperature ranging from 200K to 450K at 32nm, 22nm and 16nm technology nodes and this is because of high tube capacitance in case of MWCNT bundle compared to SWCNT bundle and copper interconnects. It is also found from the results that the power dissipation increases as temperature increases from 200K to 450K for three technology nodes under consideration. Further, it is also revealed from the results that the power dissipation for all three materials is decreasing for scaled down technology nodes i.e. 32nm to 16nm.

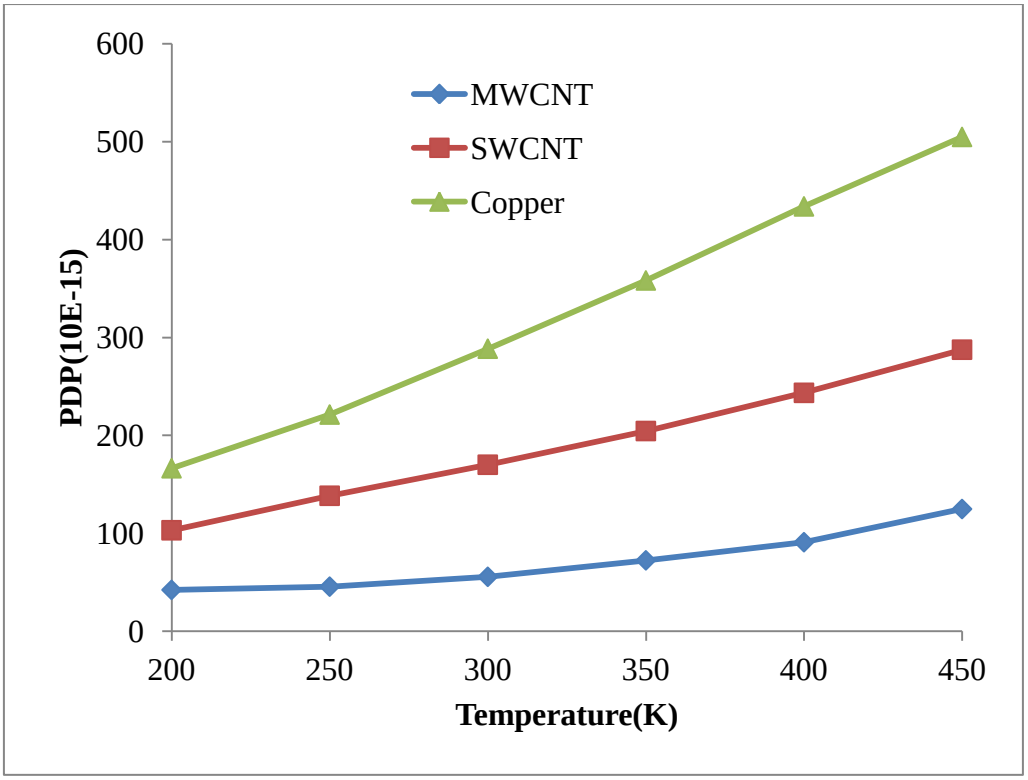
Figures 6.13(a), (b) and (c) show the performance comparison of MWCNT bundle, SWCNT bundle and copper interconnects in terms of Power Delay Product (PDP) for 32nm, 22nm and 16nm respectively at temperature range 200K to 450K for 1mm interconnects length.


350
300
250
200
150
100
50
0
PDP(10E-15)
MWCNT
SWCNT
Copper
200
250
300
350
400
450
Temperature(K)

(a)


450
400
350
300
250
200
150
100
50
0
PDP(10E-15)
MWCNT
SWCNT
Copper
200
250
300
350
400
450
Temperature(K)

(b)



(c)

Figure 6.13: (a), (b) and (c) Comparison of performance in terms of PDP for MWCNT bundle, SWCNT bundle and copper interconnect for 1mm interconnects length at 32nm, 22nm and 16nm technology nodes respectively.

It is observed that with rise in temperature ranging from 200K to 450K influence the performance in terms of PDP for MWCNT bundle, SWCNT bundle and copper interconnects. The rising temperature increases the PDP for all three types of interconnects at three different technology nodes (32nm, 22nm and 16nm). It is also revealed that for deep submicron technology nodes, the performance in terms of PDP further improved in favor of MWCNT bundle compared to SWCNT bundle and copper interconnects. It is also observed that the performance in terms of PDP of MWCNT bundle interconnects is several times better than the performance of copper interconnects.

6.5 Chapter Summary and Contribution

This chapter presented the comparison of the results obtained from MWCNT bundle interconnects with results for copper interconnects and SWCNT interconnects. The temperature dependent impedance parameters for SWCNT bundle and copper interconnects are calculated using their equivalent models presented in chapter 3, for same length and technology nodes considered for MWCNT bundle interconnects. All interconnects

technology parameters are calculated using the data obtained from ITRS 2013 version. These temperature dependent impedance parameters are simulated using SPICE simulation tool. A distributed RLC model with optimum number of repeaters is used as simulation setup. The simulation results are obtained using optimum number of repeaters. A comparative analysis in terms of delay, power and PDP of MWCNT bundle interconnects and copper interconnects is presented in section 6.2 of this chapter. It revealed from the results that the performance in terms of delay and PDP of MWCNT is many time better as compare to copper interconnects. Similarly, a comparison of MWCNT bundle interconnects and SWCNT bundle is presented in section 6.3. It is concluded from the results that MWCNT bundle interconnects are more suitable candidate as compare to SWCNT bundle for long interconnects at deep submicron technology nodes under thermal variations. Finally, a comparative analysis is presented for MWCNT bundle, SWCNT bundle and copper interconnects for global interconnects length at variable temperature from 200K-450K. It is concluded from the results that performance of proposed temperature dependent impedance model for MWCNT bundle interconnects is better than SWCNT bundle and copper interconnects at three technology nodes (32nm, 22nm and 16nm) for global interconnects length at temperature ranging from 200K-450K..

7 CONCLUSION AND FUTURE SCOPE

The analytical and simulation studies reported in this thesis are utilized to draw a set of conclusions. In this chapter, conclusion and future scope of work is presented in the following sections.

7.1. Conclusion

The work presents in the thesis, estimated the influence of temperature on MWCNT bundle interconnects for global interconnect length at 32nm, 22nm and 16nm technology nodes. In the initial stage, a thorough study of the copper interconnects and CNT interconnects presented in the literature, has been carried out. The deficiencies of copper interconnect at nano-scaled technology nodes and advantages of CNT as long interconnects documented in the literature, are highlighted so that some improvement in the performance could be established. The impact of temperature on the performance of traditional copper interconnects and SWCNT bundle interconnects is deeply analyzed, as presented in the literature. In the literature, the temperature dependent models proposed for SWCNT interconnects and presented the simulated results for local level interconnects only. Therefore, the temperature dependent performance for SWCNT bundle and copper interconnects is needs to be analyzed for long interconnects as well.

A temperature dependent RLC model is proposed for MWCNT bundle interconnects. The proposed model for MWCNT bundle included the temperature dependent scattering mechanism. The proposed mathematical equations are incorporated the influence of temperature on MFP for MWCNT. Further, the effects of temperature dependent MFP are used to predict the impedance parameters of an individual shell of MWCNT. Based on this approach, a single RLC structure of an individual shell of MWCNT has been proposed and further this model is used to develop the temperature dependent equivalent RLC model for

MWCNT bundle. All the individual shells of MWCNT interconnect have been considered as parallel shells for temperature dependent equivalent model for MWCNT bundle. Finally from the developed model, the temperature dependent impedance parameters are calculated for 32nm, 22nm and 16nm technology nodes respectively for temperature range of 200K to 450K at global interconnects length (1mm). The calculations are obtained by writing the script in MATLAB. All interconnects technology parameters are calculated using the data obtained from ITRS 2013 version. It is observed that with rise in temperature (from 200K to 450K), the resistance increases due to decrease in MFP for MWCNT shells. With rise in temperature, MFP decreases because there is increase in the collision rates within MWCNT. Hence, this change in resistance has considerable effect on the performance in terms of delay and power for the MWCNT bundle interconnects at nano-scaled technology nodes for global interconnects lengths.

Further, the effect of temperature on delay, power and PDP has been analyzed in MWCNT bundle interconnects for different technology nodes. The performance of MWCNT interconnect is estimated in terms of delay, power and PDP for 32nm, 22nm and 16nm technology nodes at global interconnects length. The calculated impedance parameters of MWCNT bundle interconnects using the equivalent models have been simulated to evaluate the performance in terms of delay and power by using the SPICE simulation tool for distributed RLC model for interconnects. The distributed RLC model can be approximated from a lumped model by divide with multi-stage RLC ladder network. Repeaters are inserted to separate different stages of RLC ladder network. The simulation results are obtained using optimum size and number of repeaters. Other simulation parameters and model file is obtained from Predictive Technology Model (PTM).

It is observed from the simulated results that with rise in temperature (200K-450K), the delay, power and PDP increased for MWCNT bundle interconnects for all three technology nodes (32nm, 22nm and 16nm) and it is due to the shrinking of MFPs. The impact of temperature on delay of MWCNT bundle is observed that for higher side of temperature range (350K-450K), the normalized delay ratios (τ/τ_0) are increasing from 1.136 to 1.71, 1.23 to1.85 and 1.3 to 2.1 for 32nm, 22nm and 16nm technology nodes respectively which specifying that the increasing temperature affects the delay performance in a worst manner for high temperature. Further, the normalized delay ratio at 450K is 1.71, 1.847 and 2.1 for 32nm, 22nm and 16nm technology nodes respectively, indicates that for scaled down technology nodes i.e. from 32nm to 16nm, the normalized delay ratio is increasing more rapidly. Further, it revealed from the results in terms of normalized PDP ratio that PDP ratio

increases more rapidly for temperature above 300K compared to below 300K. The normalized PDP ratio for temperature ranging from 350K to 450K increases from 1.38 to 1.726, 1.23 to1.91 and 1.3 to 2.245 for technology nodes 32nm, 22nm and 16nm respectively. It is also observed from the results that the PDP ratio for 16nm is higher than 22nm and 32nm technology nodes for temperature ranging from 350K to 450K. Therefore as technology scaled down, the amount of PDP is increasing at moderate to high temperature range (300K-450K) for VLSI integrated circuits design. Therefore, it is also concluded from the results that the temperature variations have considerable impact on the performance of MWCNT bundle interconnects.

The temperature dependent analytical delay model is presented for MWCNT interconnects and analytical results are compared with the simulated results. It is revealed from the results that the analytical results are in similar trend with the simulated results. The trend of both results shows that the delay is increases with rise in temperature for three technology nodes i.e 32nm, 22nm and 16nm. Therefore, it is concluded from the results that for high performance IC design, under variable thermal environments need to be considered the impact of temperature to get accurate performance.

In addition with this, a comparison of results obtained from MWCNT bundle interconnects with results for copper interconnects and SWCNT interconnects. The temperature dependent impedance parameters for SWCNT bundle and copper interconnects are calculated using their equivalent models for same length and technology nodes considered for MWCNT bundle. These temperature dependent impedance parameters are simulated using SPICE simulation tool. A comparative analysis in terms of delay, power and PDP is presented for MWCNT bundle interconnects with SWCNT bundle and copper interconnects for 32nm, 22nm and 16nm technology nodes. It is revealed from the results that performance of proposed temperature dependent impedance model for MWCNT bundle interconnects is better than SWCNT bundle and copper interconnects for global interconnects length at 32nm, 22nm and 16nm technology nodes.

Finally, it is concluded that:

MWCNT bundle interconnect is the better alternative to replace the traditional copper interconnects for semi-global and global level interconnects in high speed VLSI circuit design and to estimate the accurate performance of MWCNT based interconnects, the influence of temperature needs to be incorporated for high performance application under thermal variable environment.

7.2 Future Scope of Work

In this thesis, the deficits of copper interconnect and SWCNT interconnects have been dealt efficiently and MWCNT bundle interconnects proposed as future interconnects. Further, to estimate the influence of temperature on the performance of MWCNT bundle interconnects, a temperature dependent RLC circuit model is presented and performance of MWCNT estimated for global interconnects length at 32nm, 22nm and 16nm technology nodes. A comparative analysis is performed with SWCNT and copper interconnects. It is concluded, that MWCNT performs better than SWCNT and copper and can be used as interconnect at semi-global and global lengths in high speed VLSI applications at 32nm, 22nm and 16nm technology nodes. The performance of VLSI circuit design could further be enhanced by exploring the other fields of the proposed area. Henceforth, following are the ideas which can be explored in future:

- In deep submicron technology nodes, interconnects density increases causes more coupling between neighboring wires. Thus there is a dire need to analyze temperature dependent cross talk for MWCNT bundle interconnects for nano-scaled technology nodes at global interconnects length.

- With advanced technology nodes, there is need to focus on low power IC design. Therefore, temperature dependent analysis for sub-threshold needs to be addressed for MWCNT interconnects.

- The fabrications CNT based interconnects have certain real challenges for its growing process. Therefore, Issues related for fabrication process of MWCNT is needs to be taken care of in future work.

- In recent studies, mixed CNT interconnects (SWCNT and MWCNT) are also proposed for VLSI applications. Therefore, temperature dependent accurate analysis of Mixed CNT based interconnects need to be estimated.

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