HIGH PERFORMANCE TERNARY LOGIC DESIGN WITH CNTFETS FOR FUTURE NANOELECTRONICS

A Thesis Report Submitted In partial fulfilment of the Requirement for the Degree of

MASTER OF TECHNOLOGY

in

VLSI DESIGN

Submitted By

Mohd Javed

Roll No. 602362020

Under Supervision of

Dr. Bharat Garg

(Associate Professor, ECED)

Dr. Ankit Soni

(Assistant Professor, ECED)

THAPAR INSTITUTE
OF ENGINEERING & TECHNOLOGY
(Deemed to be University)

ELECTRONICS AND COMMUNICATION ENGINEERING DEPARTMENT
THAPAR INSTITUTE OF ENGINEERING AND TECHNOLOGY
(A DEEMED TO BE UNIVERSITY), PATIALA, PUNJAB

CERTIFICATE

This is to certify that "MOHD JAVED" final year Student of Master of Technology in VLSI DESIGN has submitted Thesis Report entitled "**High Performance Ternary Logic Design with CNTFETs for Future Nano Electronics**" in Partial fulfilment for the award of Master of Technology Degree of Thapar University, Patiala Punjab in session 2023-25. It has been found to be satisfactory and hereby approved for the submission.

Dr. Bharat Garg
(Associate Prof. TIET)
(Supervisor)

Ankit

Dr. Ankit Soni
(Assistant Prof. TIET)
(Co-Supervisor)

DECLARATION

I hereby declare that the project work entitled **"High Performance Ternary Logic Design with CNTFETs for Future Nano electronics"** submitted to Thapar University Patiala, Punjab, in partial fulfilment of the requirements for the degree of **Master of Technology in VLSI**, is a record of original work carried out by me under the guidance of **Dr. Bharat Garg** and **Dr. Ankit Soni** the research work presented in this report is original and has been submitted for the award of any other degree or diploma at Thapar University Patiala Punjab. All the sources of information used have been acknowledged appropriately. I also declare that the work complies with the ethical standards of academic research and has been completed in accordance with the institutional guidelines.

Name: Mohd Javed
Registration Number: 602362020
Course: M.Tech VLSI Design
Department: ECE
Date: 30/06/2025

Dr. Bharat Garg
(Associate Prof. TIET)
(Supervisor)

Ankit

Dr. Ankit Soni
(Assistant Prof.TIET)
(CO-Supervisor)

ABSTRACT

A viable substitute for conventional binary systems is ternary logic which provides higher data density, simpler circuitry, and possibly lower power consumption. In this work, we investigate the use of Carbon Nanotube Field-Effect Transistors (CNTFETs) for the implementation of ternary logic. Because of their superior electrical properties—such as high carrier mobility, excellent scalability, and low power dissipation—CNTFETs have become a promising candidate for next-generation Nano electronic devices. In this work ternary logic circuits of NAND and NOR and standard ternary inverter are develop and simulated while considering the CNTFET as a device. By choosing the right threshold voltages for the various states (0, 1, 2), the use of CNTFETs in ternary logic design provides improved tenability in addition to making circuits smaller and more energy-efficient. The simulation results further demonstrate the higher energy efficient.

This work proposed new circuits of standard ternary logic gates, including the ternary inverter, ternary NAND, and ternary NOR, using CNTFET device. The proposed and existing circuits of these gates are simulated with 32nm CNTFET technology node using Synopsys HSPICE. The simulation results confirm the correct ternary behavior, where the ternary inverter follows $V_{out} = 2 - V_{in}$, the ternary NAND produces a high output unless both inputs are high, and the ternary NOR generates a low output when either input is high. Compared to existing designs, the proposed CNTFET-based ternary circuits demonstrate improved performance in terms of reduced power consumption, lower transistor count, and enhanced switching characteristics**.** These results validate the feasibility of CNTFET-based ternary circuits, paving the way for efficient ternary arithmetic circuit design for low-power VLSI applications.

ACKNOWLEDGMENT

I would like to express my sincere gratitude to all those who supported me throughout the course of this project. First and foremost, I extend my heartfelt thanks to my guide, **Dr. Bharat Garg** and **Dr. Ankit Soni** for their invaluable guidance, constant support, and encouragement during this work. Their expertise and insight have been instrumental in shaping the direction of this research. I would also like to thank the faculty and staff of DECE of Thapar University Patiala, Punjab. For providing the necessary resources and facilities, which made the completion of this project possible. A special mention goes to my friends and colleagues for their continuous motivation and insightful discussions that helped refine this work. Finally, I am forever grateful to my family for their unwavering support, patience, and encouragement throughout my academic journey.

Mohd Javed

602362020

M.Tech. (VLSI DESIGN)

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ABREVIATIONS

CMOS	COMPLEMENTARY METAL–OXIDE–SEMICONDUCTOR
MOSFET	METAL–OXIDE–SEMICONDUCTOR FIELD-EFFECT TRANSISTOR
W	WIDTH
L	LENGTH
NMOS	N-CHANNEL METAL-OXIDE-SEMICONDUCTOR
PMOS	P-CHANNEL METAL-OXIDE-SEMICONDUCTOR
MVL	MULTI VALUED LOGIC
CNTFET	CARBON NANO TUBE FIELD EFFECT TRANSISTOR
NCNTFET	N-TYPE CARBON NANO TUBE FIELD EFFECT TRANSISTOR
PCNTFET	P-TYPE CARBON NANO TUBE FIELD EFFECT TRANSISTOR
$\mathbf{V_T}$	THRESHOLD VOLTAGE
STI	STANDARD TERNARY INVERTER
PTI	POSITIVE TERNARY INVERTER
NTI	NEGATIVE TERNARY INVERTER
TI	TERNARY INVERTER
T-NAND	TERNARY NAND GATE LOGIC
T-NOR	TERNARY NOR GATE LOGIC
PISO	PARALLEL IN SERIAL OUT
SISO	SERIAL IN SERIAL OUT
T-HA	TERNARY HALF ADDER

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Chapter 1

INTRODUCTION

1.1 INTRODUCTION

According to Moore’s law the number of transistors that can be integrated onto a single chip roughly doubles every two years. This consistent advancement fostered the belief that the dominance of complementary metal-oxide semiconductor (CMOS) technology would continue for the foreseeable future. Would be almost finished by 2018. Many semiconductor producers have thus started investigating and testing different materials, techniques of fabrication, and design systems to get over these constraints [1].

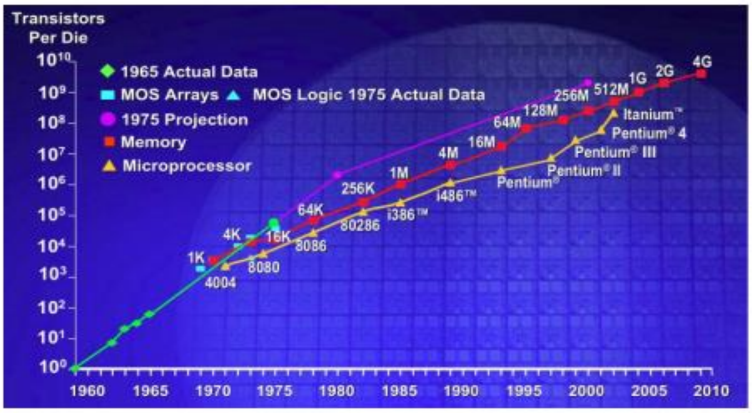

Figure 1: Graph showing illustration of Moore’s Law [3].

Given that it allows the integration of more features inside a system-on-chip while preserving the same die size, the ongoing rise in transistor count is quite exciting. Table 1 [3]. Shows the technological nodes together with the matching physical gate lengths between 2007 and 2014. Year-wise Technology Node and Corresponding Physical Gate Lengths

A. 2007**:** Technology node of 45 nm had a physical gate length of approximately 32 to 29 nm**.**
B. 2009**:** For the 32 nm node, the actual gate length reduced to around 27 to 24 nm**.**
C. 2011–2012: The 22 nm technology featured a physical gate length close to 22 or 20 nm**.**
D. 2013–2014: With the transition to 16 nm, the physical gate lengths further decreased to about 18 to 16 nm [3].

Conventional CMOS technology suffers with rising leakage current as devices are downscaled to allow faster switching speeds and higher gate counts. Different materials, including graphene, silicon nanowires, and carbon nanotubes, have been suggested to solve these problems. This work examines digital circuit simulations using (CNTFETs). Specifically, the project compares the performance of simulating CNTFETs using a ternary logic design against conventional binary designs [4].

2.2 Ternary Logic

Later validation of the ternary logic design's performance and correctness comes arithmetic circuit implementation. Operating on binary logic, digital computation historically uses two discrete values—0 and 1, or true and false—within the Boolean domain. By letting variables take on more than two values—either finite, as in ternary logic, or infinite, as seen in fuzzy logic—Multiple-Valued Logic (MVL) stretches this idea [6].

Three-valued logic, sometimes known as ternary logic, has attracted a lot of interest for possible advantages over binary logic in digital circuit design. Its benefits include lower chip area use, less interconnect complexity, and better energy economy. Especially in serial and serial-parallel architectures, these qualities can result in more effective arithmetic operations. With an eye toward ternary inverters [7]. This paper investigates the implementation of basic ternary logic gates and operators.

Because they offer three separate and steady logic states, ternary logic circuits are especially appealing and help increase the freedom of digital system design. The, voltage levels in binary systems 0V and V_{DD} reflect logic values of 0 and 1, respectively. Logic values 0, 1, and 2 in ternary systems translate, respectively, to 0V, $V_{DD}/2$, and V_{DD} [21]. More compact circuit layouts and simplified interconnections made possible by this multi-level approach help to lower power consumption and signal delays by themselves. Furthermore, ternary systems' maximize communication channels' use. Using ternary logic enables fast transfer of data both serially and in parallel [22]. Suppose that Xi and Xj are two literals that are capable of accepting any value from the set {0, 1, 2}, which implies that Xi and Xj are equal to {0, 1, 2} then

$$Xi + Xj = max\{Xi, Xj\} \quad (1)$$

$$Xi . Xj = min\{Xi, Xj\} \quad (2)$$

$$\overline{Xi} = 2 - \mathrm{Xi} \qquad (3)$$

In Eq. (1) of ternary logic the sign ′+′ represents the arithmetic OR operation and ′.′ represents the logical AND operation in Eq. (2) and ′-′ represents the arithmetic subtraction and ’¬’represents the complement of Xi in Eq. (3) [23]. This work uses ternary logic elements, including ternary inverters (TI) ternary (T-NAND) and ternary NOR (T-NOR). Apart from the resistive load inverter, three further kinds of inverters are used to assess and contrast performance. A reference circuit for verifying functionality and evaluating the performance of the suggested ternary gate design approaches is the ternary half adder (T-HA). These instances show useful ternary logic applications in digital circuit design [8].

2.3 Carbon Nano Tube FET

A carbon nanotube field-effect transistor (CNFET) functions similarly to a conventional MOSFET, as both regulate the current flow between the source and drain through a voltage applied between the gate and source terminals. While the CNFET employs a semiconducting carbon nanotube (CNT) as the channel material connecting the source and drain beneath the gate, it remains a four-terminal device, just like a MOSFET [9][10].

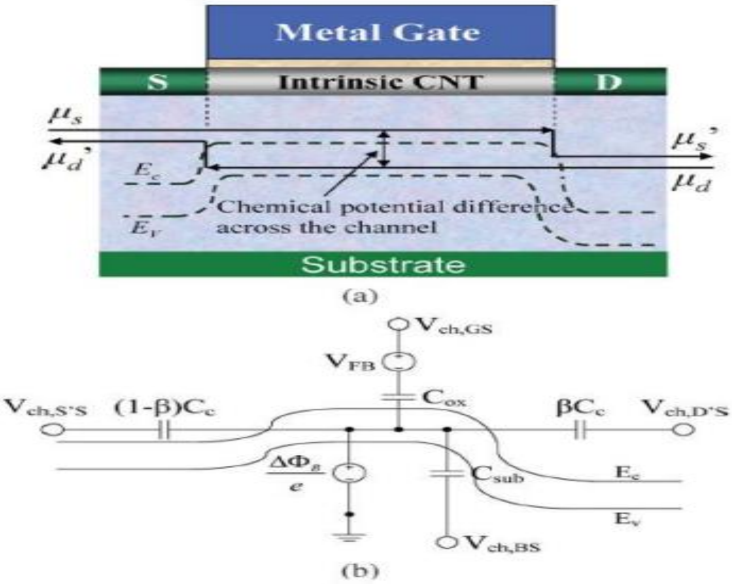

Figure 2: CNFET (a) Structure, (b) Electrostatic Capacitor Model. [10]

Carbon nanotubes (CNTs) have incredibly small diameters, usually only a few nanometers, which allows the creation of field-effect transistors (FETs) with very short gate lengths. The accompanying diagram shows electrostatic capacitance model and the structure of a CNTFET. We typically divide CNFETs into two primary types based on their operational characteristics:

(1) SB-CNTFET, or Schottky Barrier CNTFET

(2) CNTFET that resembles a MOSFET.

SB-CNTFET A single carbon nanotube is positioned on top of a conductive substrate, which serves as the gate in an SB-CNFET. A dielectric material separates the ends of the nanotube from the gate, and the ends are attached to metallic contacts that act as the source and drain. Generally speaking, the gate length is around 300 nm, which is substantially longer than that of conventional bulk FETs. Strong capacitive coupling across the channel is the result of the CNT's full gate length span. The majority charge carrier’s tunnel through Schottky barriers created at the metal-CNT contacts to power this kind of CNFET. The contact resistance produced by these tunneling barriers is the main factor affecting the on-current and overall performance [11].

MOSFET-like CNTFETs, on the other hand, use partially gated CNT channels, which leads to a weaker capacitive coupling. By altering the thickness of the potential barriers at these terminals, this design lessens the gate's capacity to modulate Charge carriers flow from the source to the drain in these devices, which are also referred to as bulk-switched transistors CNTFETs, depend on the availability of charge carriers within the channel potential and gate modulation of that potential. By adding a lot of impurities to either the source or the drain to limit the movement of one type of charge carrier—either electrons or holes—they behave in a way that only allows one type of charge to flow. Consequently, a non-tunneling mechanism in the channel controls conductivity, typically leading to n-type behavior. We can also create P-type devices by adding negative charge traps to the gate dielectric, which lowers the potential barrier for hole transport [12].

MOSFET-like CNTFETs have several benefits over SB-CNFETs. For example, the thinner potential barriers at the source and drain enable enhanced transistor conductivity and increased current capacity. Furthermore, the metal-nanotube contact interface does not largely control the current flow, improving device performance and dependability. Below are energy band diagrams that show the operational differences between MOSFET-like CNFETs and SB-CNFETs [13].

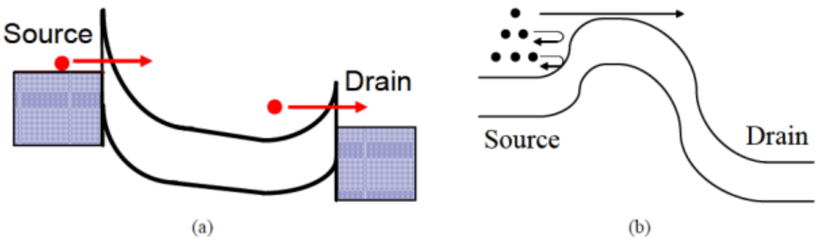

Figure 3: Energy Band Diagram for (a) SB-FET (b) MOSFET-like FET. [13]

Despite the discovery of CNTs in 1998 and the development of numerous synthesis and fabrication techniques since then, there haven't been many notable developments in their use in VLSI circuit design. Reliable instruments for assessing CNTs' performance are necessary if they are to genuinely become a breakthrough in electronics. This requirement has motivated scientists to investigate CNTs by means of theoretical modelling and performance analysis, emphasizing their distinct features.

Researchers can gain a deeper understanding of CNT behaviour by examining them from a modelling standpoint. This allows for the integration of CNTs into a wider variety of applications. In addition to forecasting circuit and device performance, a good device model should consider how performance changes as geometric parameters change [14][15]. A strong CNT-based device model must have the following essential components:

(1) Precise evaluation for conditions with small and large signals
(2) Excellent scalability for a range of device sizes
(3) Effective simulation with a manageable computation time

Chapter 2

LITERATURE REVIEW

2.1LITERATURE REVIEW

This chapter explores the study of the research work that have been already done by the researchers in direction of CNTFET and the ternary logic. At first, research papers that are related to the title are studied and their objectives and research gaps have been noted.

Trapti Sharma and Deepa Sharma (Sharma & Sharma, 2023) [1] Highlight the benefits offered by multi-valued logic. over ternary logic and benefits of the CNTFET over MOSFET and they implemented shift register like SISO and PISO with the 32 nm node file of CNTFET and the proposed design were ternary SISO achieved by the connecting multiple D-flip flops. PISO register minimize the delay concern and ternary d-flip flops design operates in three modes proposed for efficient data shifting and loading and the another design was d-flip flops design the design of D-flip flops was the master slave configuration using mux based ternary latches which improves upon NAND/NOR based design. Monte Carlo simulations validate the proposed design. The proposed design demonstrates up to 90% savings in both power usage and power-delay product. Configurations in PISO demonstrate the potential of ternary logic in optimizing digital circuit's performance all simulations achieved by the synopsis H-SPICE (Hewlett Program with Integrated Circuit Emphasis) tool.

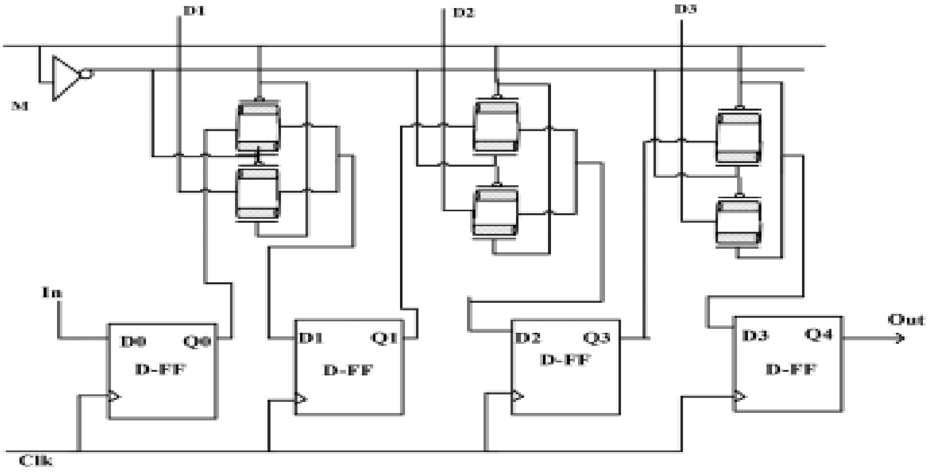

Figure 4: Ternary PISO Shift Registers Model [1]

TABLE 1: Simulations results of PISO [1].

Power (W)	Delay (sec)	PDP (J)	Power (W)
Mean (μ)	1.917 x10^{-8}	3.12x10^{-15}	1.676 x10^{-7}
Standard deviation (σ)	1.179 x10^{-8}	7.536x10^{-16}	6.392 x10^{-8}
Variability (σ/μ)	0.615 x10^{-8}	2.346 x10^{-1}	3.813 x10^{-1}
Mean (μ)	8.948 x10^{-11}	10.29 x10^{-18}	1.151 x10^{-7}
Standard deviation (σ)	1.453 x10^{-11}	2.169 x10^{-19}	1.493 x10^{-8}
Variability (σ/μ)	0.163 x10^{-8}	0.2106 x10^{-2}	1.297 x10^{-1}
Mean (μ)	3.144 x10^{-11}	10.067 x10^{-18}	3.20 x10^{-7}
Standard deviation (σ)	4.885 x10^{-12}	15.319 x10^{-20}	3.136 x10^{-8}
Variability (σ/μ):	1.553 x10^{-1}	1.553 x10^{-1}	0.9793 x10^{-1}

These results indicate that the proposed design exhibits the lowest standard deviation in the power-delay product (PDP) trade-off metric compared to other recent studies.

Trapti Sharma and Laxmi Kumbre (Sharma & Kumre, 2020) [2] they focus on a low-power ternary arithmetic logic unit (ALU) design with CNTFET. Utilizing the geometry dependent threshold voltage inherent to architecture facilitates energy efficient multi-valued logic operation. Ternary logic is another method of reducing the number of circuits required to compute multiple functions in a single block. They achieve this by recognizing certain symmetrical patterns in the operations of adder and subtractor modules, enabling them to be optimized. This helps keep arithmetic, logical and other operations in the hardware easy while implementing different functions at ALU. In simulations using the Stanford 32nm CNFET model, power and energy are shown to decrease by 62% and 58%, respectively compared to conventional designs. Which can be seen, for example in full adder/subtractor module. In addition, based on the 2-trit multiplier performance at both architecture and circuit levels is improve which makes this design a more efficient & compact ALU solution.

Vikash Prasad, Anirban Banerjee and Debaprasad Das (Prasad et al., n.d.) [3] They discuss the limitations of conventional binary logic and suggest a more efficient alternative called Multiple-Valued Logic (MVL) with fewer complexities and lower power consumption. Multi- threshold design in ternary logic, then propose CNTFET based ternary circuits to reduce the power dissipation and propagation delay. Finally, they designed p-type and n-type models for ternary logic gates using up-down staggered dual gate design where the size of these devices adjusted by varying number of nanotubes, not width. The paper presents simple, positive and negative polarity ternary inverters together with fully functional Ternary-AND gates as well as the first actual OR gate behaving very

Good in simulations. Results show that a ternary 1-bit multiplier is implemented using multiplexer-based method as well with reduced delay and power consumption comparing to previously designed multipliers. The paper concludes with the virtues of ternary logic based on CNTFET and its promising applications in digital domain scopes. The design shows ∼ 2000× less delay and 104× less power as compared to that of existing designs.

(Sharma & Kumre, 2021) [4] They first discuss the limitations associated with scaling in semiconductor based devices and then propose that instead of dual valued logic (DVL) multi-valued logic e.g. ternary logics are used both to facilitate high speed compact realization, efficient utilization of on-chip resources while minimizing power consumption also referred as very large scale integration system ab VLSI performance helpful for better data density. CNTFET is an excellent compare to conventional CMOS technology over other implementations of ternary logic. The paper presents an unbalanced ternary logic giving basic operations such as inverters and shifts which are required for use of flip-flops, counters .Synchronous counters, which feed the clock signal into all flip-flops at roughly the same time and place. Have a disadvantage that if they do not reach after resetting right away; then it will continue WAIT until CLR ≤ BACK. This aims to design D type Flip Flops having efficient Voltage Dividers which help in creating Low Power Counters. CNTFET have possibility that multi threshold thus gives better performance and efficiency for ternary logic design. Designs use D-flip-flops combined with the shifting operators for state transitions to achieve a very low power and energy efficiency for the D-flip-flop to provide more control as well as an asynchronous down-counter which is ternary-based implemented. The synchronous counter design also uses a separate clocking input for each flip-flop, which helps increase speed and improve performance. The results demonstrate significant improvement in power consumption, delay and overall efficiency for the proposed design as compared to traditional designs.

(Mohammad et al., 2021)[5] The article review multi-valued logic (MVL) and ternary as it is a new approaches to save the energy consumption, reducing amounts of interconnections in highly-dense

ICs. Ternary logic efficiently increases the number of data that can be stored due to complementing Moore's law, and it is more compatible with digital systems than CMOS which has some problems in quantum tunneling through leakage or gate oxide. The comparative study results confirm the fact that CNTFET is a good replacement of CMOS with low delay and power consumption pros. The paper proposed designs such as ternary D-latch, The Ternary Dynamic D-Latch and Master-Slave flip flop with the N-CNTFET for effective performance. Improved power, and delay efficiency with apropriatory multi-port register file architecture using dynamic DFFs. The designs contained in this paper are planned to be used for further optimization of ternary microprocessors in future work.

(Surwadkar, 2020) [6] This paper presents an in-depth analysis of CNTFET technology and its advantages over conventional CMOS technology for digital applications, focusing on a comparison between a single-walled 32nm CNTFET and 45nm, 32nm, and 22nm CMOS technologies using HSPICE simulations. The study evaluates key electrical parameters of CNTFET and CMOS inverters, revealing that the CNTFET inverter outperforms CMOS inverters in terms of switching speed and output current, with an ideal voltage transfer characteristic (VTC) and a lower switching threshold. The short-circuit current for the CNTFET inverter is significantly higher, exceeding three times that of the 32nm and 45nm CMOS technologies and nearly nine times that of the 22nm CMOS technology. However, the paper also identifies challenges related to short-circuit current transients in CNTFET inverters that need to be addressed for reliable operation at the nanoscale. Despite these challenges, the study concludes that CNTFET technology holds significant potential for future digital applications, especially as device dimensions continue to shrink, though further research is needed to mitigate short-circuit current issues. Increasing the number of carbon nanotubes in the device structure may enhance performance and reliability, suggesting CNTFET as a promising alternative to CMOS for digital electronics.

(Farhana et al., 2014) [7] The paper explores the emerging technology of CNTFET as a promising alternative to conventional CMOS technology, driven by CMOS's limitations in size and the advantages of CNTFETs, including nanoscale dimensions, high stability, and low power consumption. It proposes a novel CNTFET-based inverter design utilizing an optimal chiral vector and simulates the circuit using the PSPICE platform. The performance of the proposed CNTFET inverter is highlighted by a maximum voltage gain of 45 dB from the n-CNTFET component, along with high and low noise margins of 400 mV and 309 mV, respectively, indicating strong resistance to signal interference. The research underscores the importance of noise margin characteristics for maintaining stable operation in noisy environments, ensuring reliable digital circuit performance. The findings suggest that CNTFETs are viable for integrated logic devices and circuits, providing a foundation for future advancements in low-power, high-performance electronic systems**.**

(Dokania et al., 2018) [8] The growing demand for ultralow-power circuit design, driven by mobile devices, emphasizes the importance of techniques like voltage scaling and clock gating to reduce power consumption, with performance being secondary in such applications. Lowering supply voltage (VDD) and operating in the subthreshold region significantly enhance energy efficiency. The design of 1-bit full adder cells, critical for arithmetic operations, focuses on achieving output levels close to voltage rails while minimizing power. This study investigates the Minimum Energy Point (MEP), finding optimal energy efficiency at a supply voltage of 0.15 V through proper MOSFET sizing. Existing 1-bit full adder designs show inadequate output levels and poor performance. A proposed 10T full adder circuit improves propagation delay (1.81×), average power (3.39×), leakage power (2.25×), and energy consumption (6.12×), while demonstrating higher noise immunity and improved output signal levels. Simulations, incorporating realistic conditions and variability analysis, confirm the proposed design's suitability for energy-constrained applications like medical devices, outperforming existing designs in ultralow-power metrics.

(Nagendrababu & Pamuleti, 2017) [9] Researchers are exploring advanced alternatives to enhance semiconductor performance, focusing on high-mobility materials like semiconductors, FinFETs, and one-dimensional structures such as carbon nanotubes (CNTs). Show great promise for future technologies by improving MOSFET performance, driving interest in. CNTFETs share structural similarities with MOSFETs, featuring a drain, gate, source, and substrate, while leveraging the unique properties of CNTs, such as tuneable threshold voltage based on diameter and ballistic transport enabled by their long mean free path. Simulation studies using HSPICE demonstrate that CNTFET-based digital logic and arithmetic circuits, including full adders, subtractors, multipliers, and ALUs, outperform CMOS counterparts in terms of power consumption, delay, and energy efficiency, particularly at 32 nm technology. Comparative analysis highlights the advantages of CNTFETs for low-power, high-speed applications, making them a viable and efficient alternative to CMOS technology in digital circuit design.

Chapter 3

RESEARCH GAPS

3.1 RESEARCH GAPS

(1) Limited Exploration of CNTFET-Based Ternary Logic Designs

While CNTFETs offer promising characteristics for multi-valued logic, existing studies on CNTFET-based ternary logic circuits—particularly universal gates and STIs—are limited in scope and often lack practical implementation details.

(2) Lack of Optimized Standard Ternary Inverter (STI) Designs

Current STI designs do not adequately balance performance parameters such as power, delay, and power-delay product (PDP), leaving room for optimized or novel architectures.

(3) Insufficient Comparative Performance Analysis

Most existing works focus on either power or delay individually, but comprehensive evaluations that include power, delay, and PDP simultaneously are scarce, hindering a balanced assessment of design efficiency.

(4) Outdated or Incomplete Benchmarking Against State-of-the-Art

Many studies do not provide detailed comparisons with the most recent state-of-the-art designs, which limits understanding of where improvements are truly being made.

(5) Lack of Universal Gate Designs Tailored for Ternary Logic with CNTFETs

There is a notable absence of efficient universal gate structures specifically optimized for ternary logic in CNTFET-based technologies, which constrains the design space for more complex ternary logic circuits.

Chapter 4

RESEARCH OBJECTIVE

4.1RESEARCH OBJECTIVE

The primary objective of this research is to explore and advance the design of ternary logic circuits using CNTFET-based universal gates and standard ternary inverters (STIs). To achieve this, the following goals will be pursued:

(1) Comprehensive Literature Review

Conduct an in-depth survey of existing research on ternary logic systems, CNTFET (Carbon Nanotube Field Effect Transistor) technology, universal gates, and STI designs to establish a strong theoretical foundation.

(2) Implementation and Evaluation of State-of-the-Art Designs

Reproduce and critically evaluate existing ternary logic designs using CNTFETs to understand their operational efficiency, area, power consumption, and delay characteristics.

(3) Proposal of New Gate Designs and Inverter

Develop and propose novel architectures for standard ternary inverters and CNTFET-based universal logic gates aimed at improving performance parameters such as power efficiency, speed, and device count.

(4) Comparative Analysis

Perform a detailed comparative analysis between the proposed designs and existing state-of-the-art solutions using relevant performance metrics, highlighting the advantages and limitations of each approach.

Chapter 5

RESEARCH METHODOLOGY

5.1 RESEARCH METHODOLY

In this section research methodology has been explained and here blue color indicating the problem definition and yellow color is indicating the research gap, objectives, finding related software tools and green color simulations, performance metrics, validation and comparison with existing technologies.

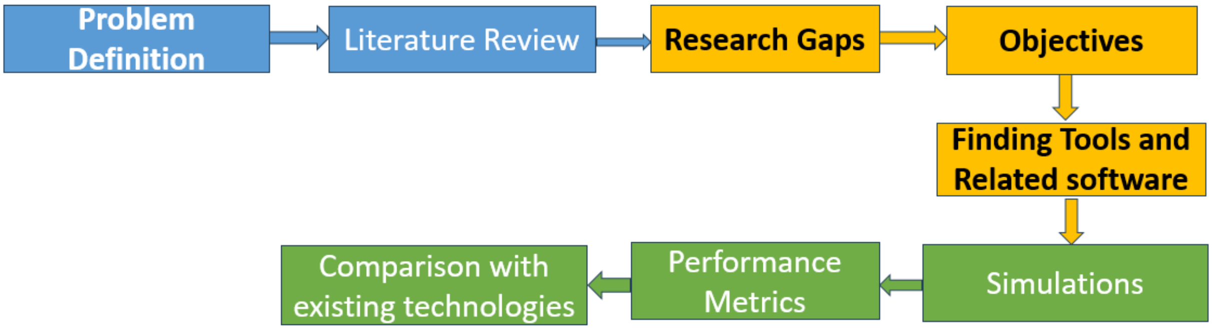

Figure 5: Research Methodology

1. Problem Definition:

Begin by identifying the current limitations in existing technologies, particularly in binary logic and CMOS circuits, focusing on performance, power, or scalability issues.

2. Literature Review:

Conduct a detailed review of published research to understand existing solutions and identify what has already been done.

3. Research Gap: Identifying the research gap based on the literature survey.

4. Objective: Define clear objectives aimed at solving the identified problem, focusing on improving performance or efficiency.

5. Circuit Designing:

Design innovative circuits that address real-world issues and have not been previously developed, using emerging technologies like CNTFETs or ternary logic.

6. Simulations:

Simulate the designed circuits using tools like HSPICE to verify functionality and predict performance.

7. Performance Metrics:

Analyse key metrics such as power, delay, power delay product. No of transistors chirality etc.

9. Comparison with Existing Technology:

Compare the proposed design with conventional binary and MOSFET-based circuits to evaluate improvements in performance and efficiency.

Chapter 6

WORK DONE

This section will outline the work accomplished to achieve the research objective. It begins with the implementation of existing designs and the analysis of their matrices. Furthermore, new inverters and universal gates are proposed, comparing them with state-of-the-art designs using the HSPICE tool.

6.1 TERNARY INVERTERS USING CNTFET

In ternary logic, there are three types of inverters: the Positive Ternary Inverter (PTI), the Negative Ternary Inverter (NTI), and the Standard Ternary Inverter (STI). The table presents the corresponding truth table for these ternary inverters. [21].

Table 2: Ternary Inverters Logic Table

Input	NTI	PTI	STI
0	2	2	2
1	0	2	1
2	0	0	0

Output values for input levels of 0, 1, and 2 are shown in Table I. These are the three inverter output options that consistently fluctuate between high and low. STI provides output at all three levels. However, only two levels are reflected by PTI and NTI.

6.2 EXISTING DESIGNS OF STANDARD TERNARY INVERTER USING CNTFET

Figure 6 displays the CNTFET-based STI design [22]. Six CNTFET devices comprise the STI. In the specified circuit, the carbon nanotubes T1, T2, and T3 exhibit chiralities of (19, 0), (10, 0), and (13, 0), respectively. The diameters of these nanotubes are as follows: T1 has a diameter of 1.487 nm, T2 has a diameter of 0.783 nm, and T3 has a diameter of 1.018 nm. Using Equation (2), the corresponding threshold voltages can be determined: 0.289 V for T1, 0.559 V for T2, and 0.428 V for T3. For transistors T5, T6, and T4, the threshold voltages are –0.559 V, –0.428 V, and –0.289 V, respectively. An output of 0.9 V (logic level 2) results from an input below 300 mV when the supply voltage is set to 0.9 V and the input voltage varies between its low and high states. In this state, T1 and T2 are OFF, while T5 and T6 are ON. When the input exceeds 300 mV, T5 remains ON and T6 turns OFF; T1 switches ON while T2 stays OFF

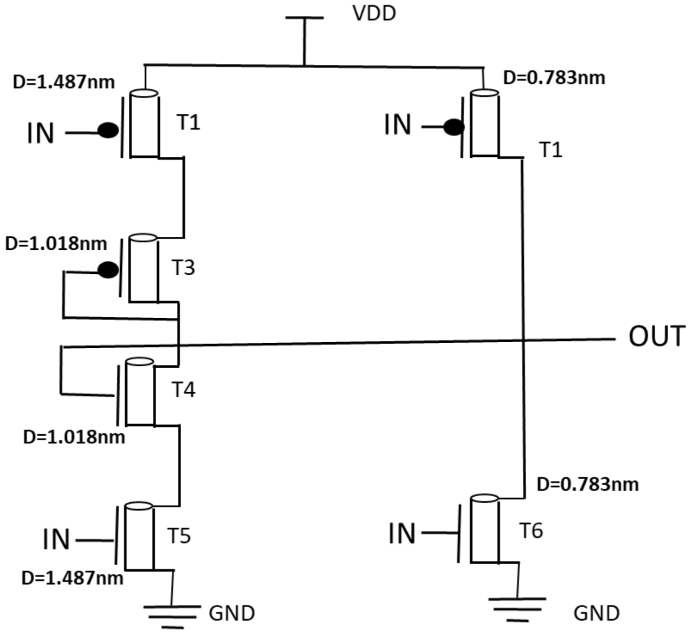

Figure 6: Standard Ternary Inverter [22].

In the specified circuit, the carbon nanotubes T1, T2, and T3 exhibit chiralities of (19, 0), (10, 0), and (13, 0), respectively. The diameters of these nanotubes are as follows: T1 has a diameter of 1.487 nm, T2 has a diameter of 0.783 nm, and T3 has a diameter of 1.018 nm. Using Equation (2), the corresponding threshold voltages can be determined: 0.289 V for T1, 0.559 V for T2, and 0.428 V for T3. For transistors T5, T6, and T4, the threshold voltages are –0.559 V, –0.428 V, and –0.289 V, respectively. An output of 0.9 V (logic level 2) results from an input below 300 mV when the supply voltage is set to 0.9 V and the input voltage varies between its low and high states.In this state, T1 and T2 are OFF, while T5 and T6 are ON. When the input exceeds 300 mV, T5 remains ON and T6 turns OFF; T1 switches ON while T2 stays OFF. Due to their threshold voltages, T3 and T4 cause a 0.45 V drop, setting the output to half the supply voltage (0.45 V), representing logic level 1 as shown in Table I. When the input surpasses 0.6 V, T5 and T6 turn OFF, and T2, along with a voltage source, pulls the output to 0 V. A similar transition occurs when the input decreases from high to low.

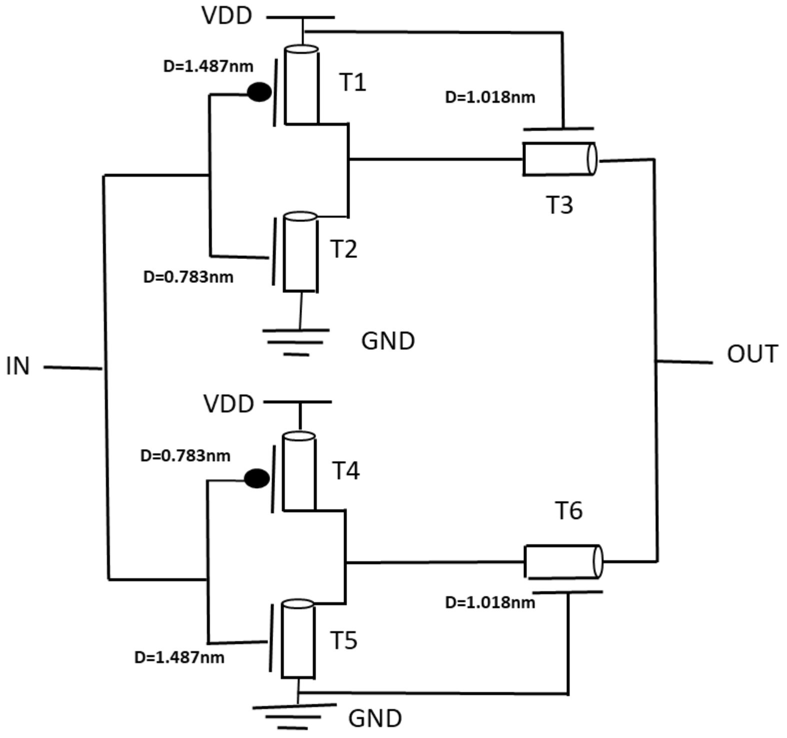

Figure 7: Standard Ternary Inverter [23].

The STI circuit shown in Figure 6 is made up of both PTI and NTI .[22] After the outputs of PTI and NTI, there are two transistors: the N-CNTFET and P-CNTFET, which share the same geometry. Due to their connection to VDD and ground, the transistors connected to PTI and NTI remain active at all times. The sum of NTI and PTI will be the power that comes out of STI. In this way, it gives off the average power. It is shown in Fig. 2 that the STI circuit is faster than the circuit shown above.

6.3 PROPOSED DESIGN OF STANDARD TERNARY INVERTER USING CNTFET

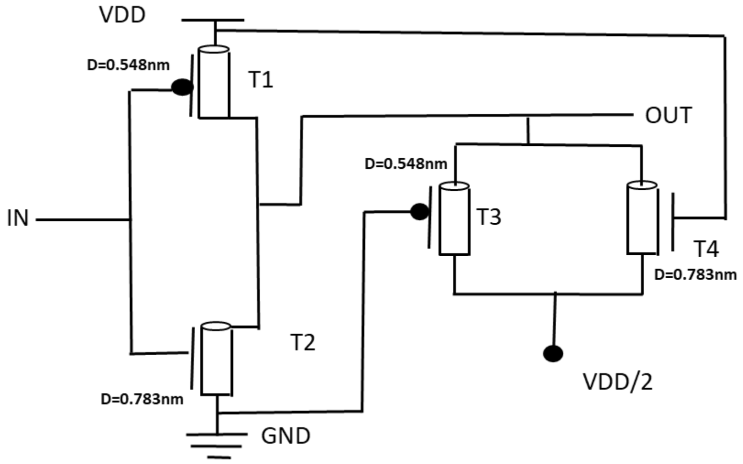

Figure 8: The circuit diagram of proposed STI

The above Fig 6. Shows the proposed standard ternary inverter it utilizes CNTFET and it operates with three levels logic ‘0’ (0V), logic 1 = (VDD/2=0.45V) and logic ‘2’= (VDD=0.9V). The electrical properties like threshold voltages required for multi valued logic implementation are determined by CNTFETs which have diameter of 1.482 nm calculated from equation 1 and chirality for T1, T3 is (7,0) with diameter 0.548nm and chirality of the transistors T2, T4 is (10,0) with diameter 0.783nm. The T1 and T2 transistors function as pull up and pull down switches to control the output levels, and the T3 and T4 transistors provide the voltage divider used for intermediate logic level stabilization in ternary logic. The circuit functions according to the following logic: when T1 is OFF, T2 is ONN, and output pulled to logic 2 (0.9V) when the input is 0V; T1 and T2 are partially conducting when the input is 0.45V. And the output is stabilized at logic 1 (0.45v) by the voltage divider (T3-T4); and T1 turns ON, T2 turns OFF, and the output is pulled to Logic 0 (0V) when the input is 0.9V.

6.4 TERNARY UNIVERSAL GATES USING CNTFET

Exploring the realm of universal ternary gates opens up new possibilities in digital design. This section delves into the intricate structures of TNAND and TNOR gates, highlighting their potential to transform digital circuit architecture. The main objective is to lay the groundwork for understanding the importance of universal gates and to evaluate their performance across multiple parameters, which will be discussed in further detail. In any design context, consistency and similarity contribute to strength, enhanced performance, and simplified fault identification. Universal gates serve a crucial purpose in digital logic design, enabling the implementation of any logical function [24]. Universal ternary gates possess the capability to realize the functionality of any logic function or equation, providing them exceptionally adaptable components in the field of digital circuit design. The universality of TNAND/TNOR gates allows for the acceptance of all ternary values .For example, a standard ternary inverter can be constructed by linking the inputs of TNANDs, and it can realize a ternary OR gate by interconnecting its inputs via the ternary inverter. In a similar manner, a TNOR gate can be utilized to create a NOT gate (STI) by linking its inputs together. By cascading and mixing these gates, it is possible to create complex logic functions for a variety of applications. Equations (6) and (7) [25]. Present the logical expression as shown. The logical illustration for ternary universal gates is presented in Table 5.

$$\text{YTNAND} = \overline{min\{lnA, lnB\}} \qquad (4)$$

$$\text{YTNOR} = \overline{max\{lnA, lnB\}} \qquad (5)$$

Table 3: Ternary Universal Gates Logic Table

INA	INB	Y-TNOR	Y-TNAND
0	0	2	2
0	1	1	2
0	2	0	2
1	0	1	2
1	1	1	1
1	2	0	1
2	0	0	2
2	1	0	1
2	2	0	0

In The above logical table InA, InB are the two ternary inputs and YTNAND is the output for ternary NAND gate and YTNOR is the output for ternary NOR gate.

6.5 EXISTING TERNARY NAND AND NOR GATE DESIGNS USING CNTFET

Investigating the following figure shows existing ternary NAND gate and NOR designs. The logical formulas for the ternary NAND and NOR gates are shown in equations (7) and (8).

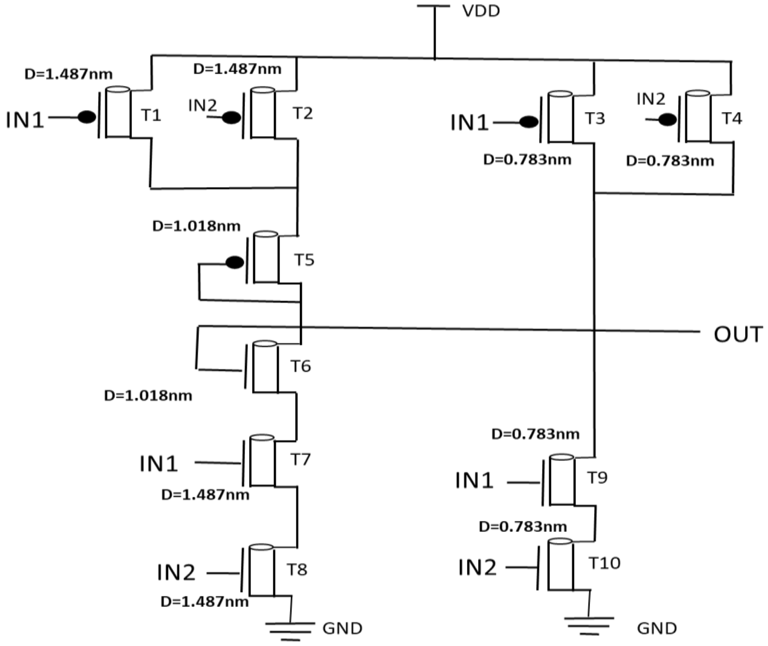

Figure. 9. Ternary NAND gate design [22].

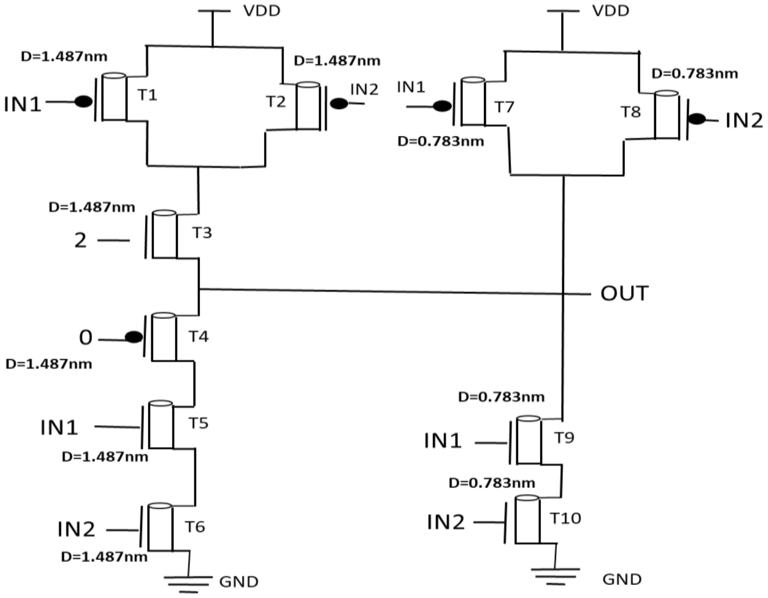

Figure. 10. Ternary NOR gate design [22].

Figure 10 and figure 11. Shows the two input NAND and NOR gate designs [15]. Comprising ten CNTFETs, each of these two gates combines three different chirali- ties. Their transistor threshold voltages vary only somewhat; functionally, they are almost exactly like traditional binary CMOS gates. Calculated with Equation (2), the matching threshold voltages using transistor diameters of 1.487 nm, 0.683 nm, and 1.018 nm are 0.289 V, 0.559 V, and 0.428 V Respectively. These values align with those seen in the Standard Ternary Inverter (STI) circuit shown in Figure 6. Using HSPICE simulations as shown in Table 5 the accuracy of these gate designs were verified.

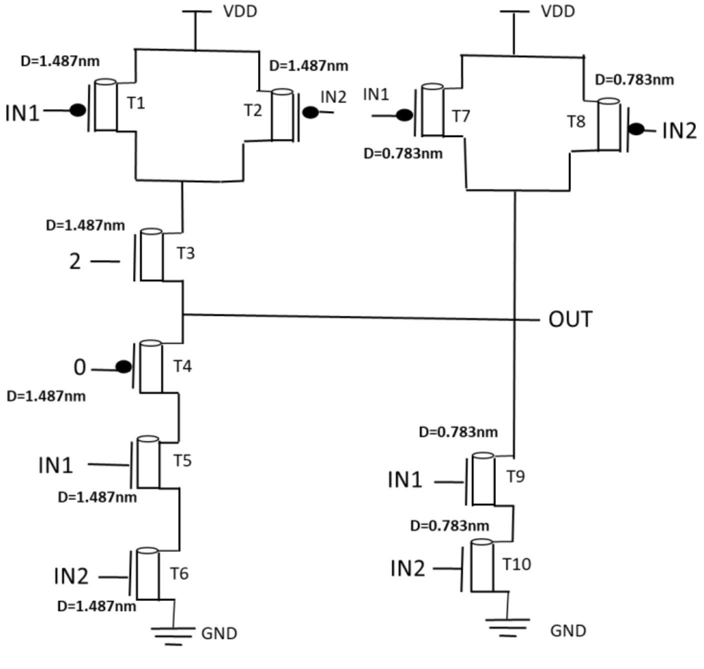

Figure. 11. Existing Ternary NAND gate design [24].

Figure 11. Shows the two-input ternary NAND gate design [22]. This design comprises a total of ten transistors, in which five transistors are PCNTFET and five transistors are NCNTFET with the chiralities of (19,0) and (10,0), and their diameters are 1.487nm and 0.783nm from the equation (1). The correctness of these designs was verified in HSPICE, according to Table 5.

The below design in figure 12 also comprises ten transistors with chiralities of transistors T1, T3, T7, T8 considered (19,0) and a diameter of 1.487nm from equation (1) [25]. T6 chirality is (13,0) with a diameter of 1.018nm and transistors T2,T4,T5,T9,T10 chiralities are (8,0) and diameter is 0.626nm and desing correctness has been verified in HSPICE according to table 5. This design also comprises ten transistors with chiralities of transistors T1, T3, T7, T8 considered (19,0) and a diameter of 1.487nm from equation (1) [25]. T6 chirality is (13,0) with a diameter of 1.018nm and transistors T2,T4,T5,T9,T10 chiralities are (8,0) and diameter is 0.626nm and desing correctness has been verified in HSPICE according to Table 5.

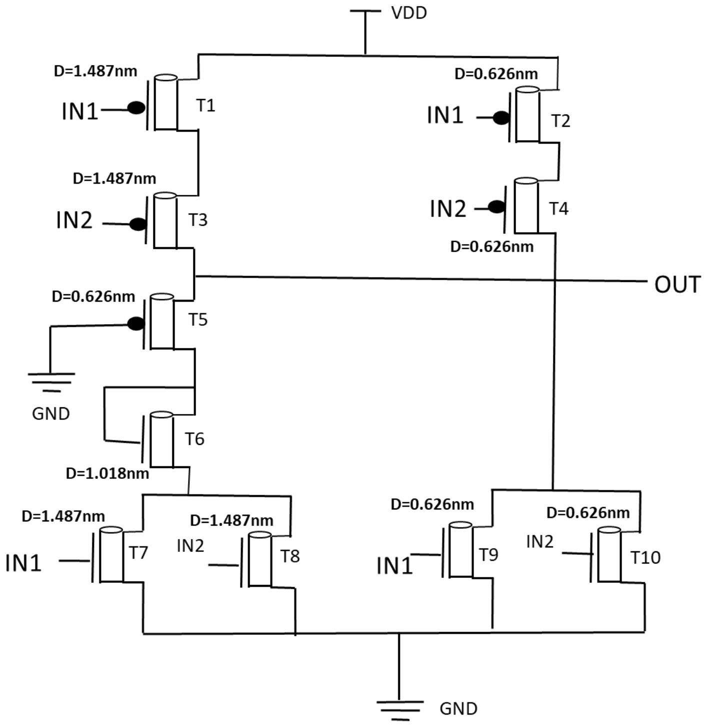

Figure. 12. Existing Ternary NOR gate design [25].

This design also comprises ten transistors with chiralities of transistors T1, T3, T7, T8 considered (19,0) and a diameter of 1.487nm from equation (1) [25]. T6 chirality is (13,0) with a diameter of

1.018nm and transistors T2,T4,T5,T9,T10 chiralities are (8,0) and diameter is 0.626nm and desing correctness has been verified in HSPICE according to Table 5.

6.6 PROPPOSED STANDARD TERNARY NAND GATE USING CNTFET

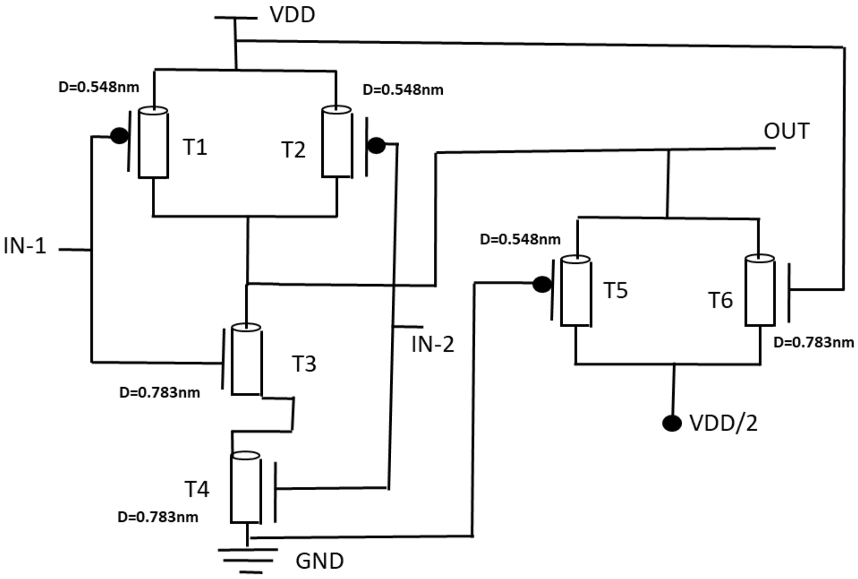

Figure 13. Proposed Ternary NAND gate

Figure 13 shows the standard ternary NAND gate design which is based on CNTFETs with ternary logic. It works with three different logic levels logic'0' (0V), logic 1 = (VDD/2=0.45V) and logic"2" = (VDD=0.9V). There is voltage divider (T5, T6) a pull up network (T1, T2), and a pull down network (T3, T4), in the circuit to control the three output values, the process work according to the truth table 5. It says if at least one input is logic 0, the result is logic '2'. Using the voltage divider, the circuit keeps the output logic 1 for the input pairs (1,1), (1,2) and (2,1). The pull down network fully starts when both the inputs are (logic 2), the output stays high (logic 1 or 2). CNTFETs with chirality (7,0) for transistors T1, T2, T5 and the diameter of these transistors is 0.548 nm and the chirality for transistor T3, T4, and T6 is (10,0) with the diameter of 0.783 nm are used because they have better performance, use less power and fewer leakage current than existing TNAND designs.

6.7 PROPPOSED STANDARD TERNARY NOR GATE USING CNTFET

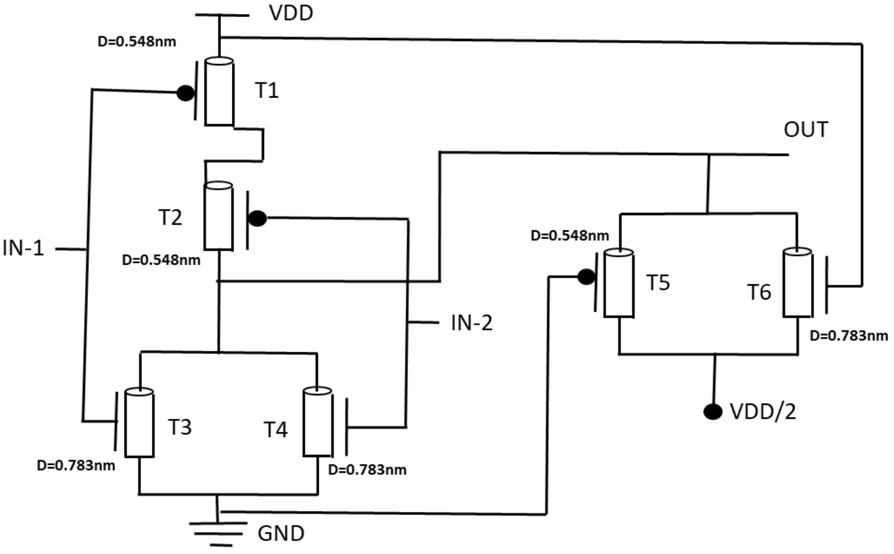

Figure 14 Proposed Ternary NOR gate

The above figure 14 shows the Ternary NOR circuit implemented using CNTFETs. Three distinct voltage levels are used by the circuit logic”0” (0V), logic 1 = (VDD/2=0.45V) and logic”2” = (VDD=0.9V). And this circuit consist of six transistors T1- T6. Transistors T1, T2 are the pull up networks and T3-T4 are the pull down network transistors T1-T4 are used CNTFETs with chirality (7,0) for transistors T1, T2, T5 and the diameter of these transistors is 0.548 nm and the chirality for transistor T3, T4, and T6 is (10,0) with the diameter of 0.783 nm are used in the circuit to control input driven logic transitions. Using pull up and pull down networks. Transistors T5 and T6 provide a voltage divider to regulate the intermediate voltage level. The circuit operation according to the truth table 5 when the input pair is (0, 0) than in the pull down network every transistor stays off the output is pulled to Logic 2 (VDD) by the conductivity of pull up transistors T1 and T2 (Y=2) in the output. If one if the input is one like (1, 0) or the opposite is true the output voltage decreased by conductivity of some of the transistors in the pull down network. The output at logic 1 (VDD/2) is stabilize by

The voltage divider effect (Y=1 in the output). When in any input is 2 the output pulled to 0V (logic 0) when at least one pull down transistor goes on. (Y=0 in the output). When both the inputs are 2 the output pushed to logic 0 (0V) since pull down route is completely engaged (Y=0 in the output).

Chapter 7

PERFORMANCE ANALYSIS AND SIMULATION RESULTS

7.1 Simulation Environment

Synopsys created the popular electronic design automation (EDA) SPICE (Simulation Program with Integrated Circuit Emphasis) is a widely used tool for simulating electronic circuits. HSPICE, one of its sophisticated variations, is especially well-suited for modelling and evaluating devices like MOSFETs, JFETs, CNFETs, and other state-of-the-art transistor models. Researchers selected HSPICE for this study over more straightforward tools like LTSPICE because lower-tier versions of HSPICE cannot accurately handle carbon nanotube (CNT) models. More simulation accuracy is offered by HSPICE, which has demonstrated success in modelling CNFETs through models created and verified by Stanford University researchers [16][17].

The physical and electrical properties of the device must be incorporated into a format that simulation tools can understand, specifically through a netlist to design a FET model using CNTs. An electronic circuit's constituent parts and their connections are described in text form in a netlist. The inclusion of references to sub-circuits, library files, and device models enables a structured and hierarchical design approach.

This work uses the Stanford 32nm CNFET model, which comes with the files CNFET.lib and PARAMETERS.lib. The operational parameters and characteristics of CNFETs are defined by these libraries, which closely resemble realistic electrical and physical behaviours. Both N-type and P-type CNFETs are necessary for the design of digital circuits. Their modelling takes into account several important factors, such as the gate's length and width, the dielectric constant of the gate material, power supply voltage, and CNT characteristics like diameter, length, and chirality. To guarantee accuracy and consistency in simulation, these values are present in the CNFET library files.[18] Synopsys created the popular electronic design automation (EDA) tool SPICE for general-purpose circuit simulation. HSPICE, one of its sophisticated variations, is especially well-suited for modelling and evaluating devices like MOSFETs, JFETs, CNFETs, and other state-of-the-art transistor models. Researchers selected HSPICE for this study over more straightforward tools like LTSPICE because lower-tier versions of HSPICE cannot accurately handle carbon nanotube (CNT) models. More simulation accuracy is offered by HSPICE, which has demonstrated success in modelling CNFETs through models created and verified by Stanford University researchers. The physical and electrical properties of the device must be incorporated into a format that simulation tools can understand, specifically through a netlist, to design a FET model using CNTs. An electronic circuit's constituent parts and their connections are described in text form in a net list. The inclusion of references to sub-circuits, library files, and device models enables a structured and hierarchical design approach. This work uses the Stanford 32nm CNFET model, which comes with the files CNFET.lib and PARAMETERS.lib. The operational parameters and characteristics of CNFETs are defined by these libraries, which closely resemble realistic electrical and physical behaviours. Both N-type and P-type CNFETs are necessary for the design of digital circuits. Their modelling takes into account several important factors, such as the gate's length and width, the dielectric constant of the gate material, power supply voltage, and CNT characteristics like diameter, length, and chirality. To guarantee accuracy and consistency in simulation, these values are present in the CNFET library files [19][20].

7.2 Device parameters of the model

The characteristics of the FET are determined by its device parameters, which are specified in advance in this model.

Table 4: Device Parameter

Device Parameter	**Description**	**Default Value**
Lch	Physical Channel Length (Channel)	32 nm
Lss	The length of doped CNT source side extension region	32 nm
Ldd	The length of doped CNT drain side extension region	32 nm
Efi	Fermi level of Doped CNT (Efo)	0.6eV
Kgate	Dielectric constant of high-k dielectric material (Kox)	16
Tox	Thickness of high-k top gate dielectric material	4 nm
Csub	The coupling capacitance between the channel and the substrate	20 pF/m
Ccsd	Coupling capacitance between gate and source/drain regions	0 pF/m
Pitch	Distance between the 2 adjacent CNTs in the same device	20nm
Wgate	Width of the metal gate (sub_pitch)	6.4 nm
(n1,n2)	Chirality of Semiconducting CNT	(19, 0)
tubes	Number of tubes in a device	3

7.3 Transient Analysis of Proposed Ternary Inverter

The given waveform illustrates the input-output behavior of a ternary inverter implemented using CNTFET technology at the 32nm node in Synopsys HSPICE. The input voltage (Vin) transitions through three distinct levels: 0V (Logic 0), ~400mV (Logic 1), and ~800mV (Logic 2)**.** Correspondingly, the output voltage (Vout) follows the expected ternary inversion**:** when Vin = 0V**,** Vout is high (~600mV, Logic 2); when Vin = ~400mV, Vout remains the same (~400mV, Logic 1); and when Vin = ~800mV, Vout is low (~200mV, Logic 0**).** This confirms the correct ternary inversion behavior following the equation Vout=2-VIN. The transitions between states are smooth, demonstrating good switching characteristics and verifying the proper operation of the standard ternary inverter (STI) for ternary logic applications.

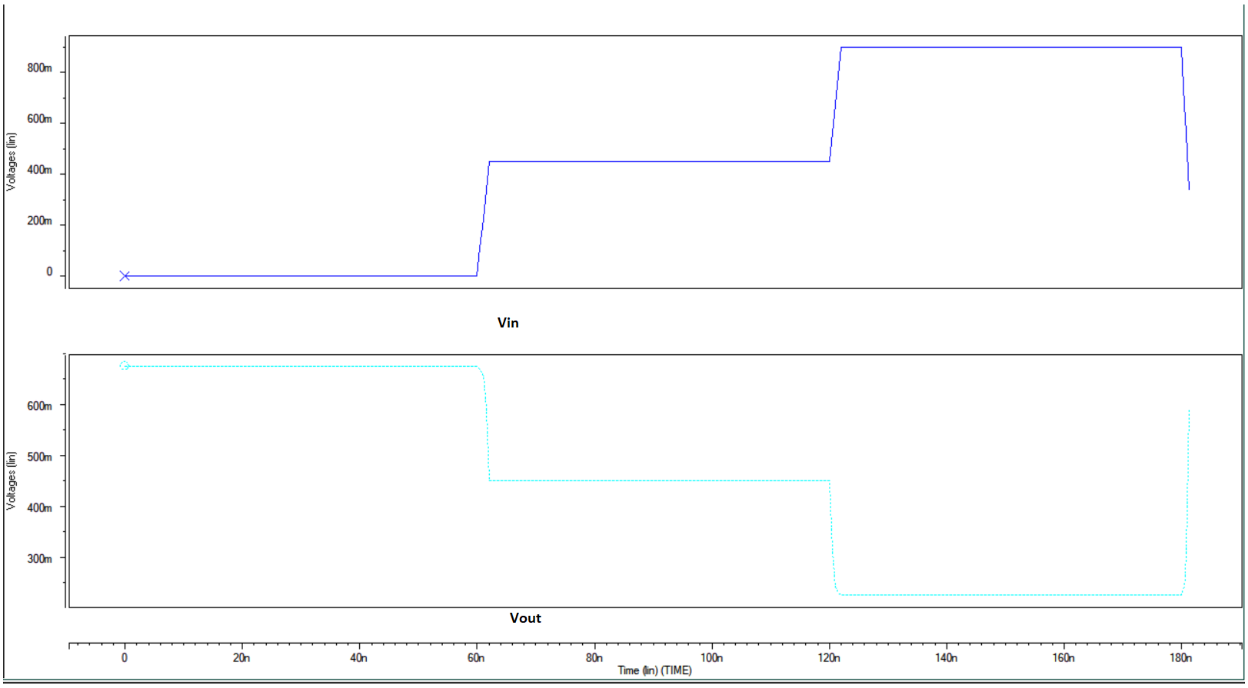

Figure 15: Transient Analysis of Proposed Standard Ternary Inverter.

7.4 Transient Analysis of Proposed Standard Ternary NAND circuit

The given waveform represents the input-output behaviour of a standard ternary NAND (T-NAND) gate implemented using CNTFET technology at the 32nm node in Synopsys HSPICE. The first two plots show the input voltages Vin1 and Vin2, which transition through three logic levels: 0V (Logic 0), ~400mV (Logic 1), and ~800mV (Logic 2). The third plot shows the corresponding output voltage Vout, which follows the ternary NAND operation: Vout = NOT (Vin1 ⊗ Vin2), where ⊗ represents the ternary AND operation. Specifically, the output remains high (~600mV, Logic 2) unless both inputs are at Logic 2, where the output transitions to a lower voltage (~200mV, Logic 0). The transitions between states confirm correct ternary NAND functionality, with smooth switching and expected ternary logic behaviour, verifying the proper operation of the T-NAND gate for ternary logic.

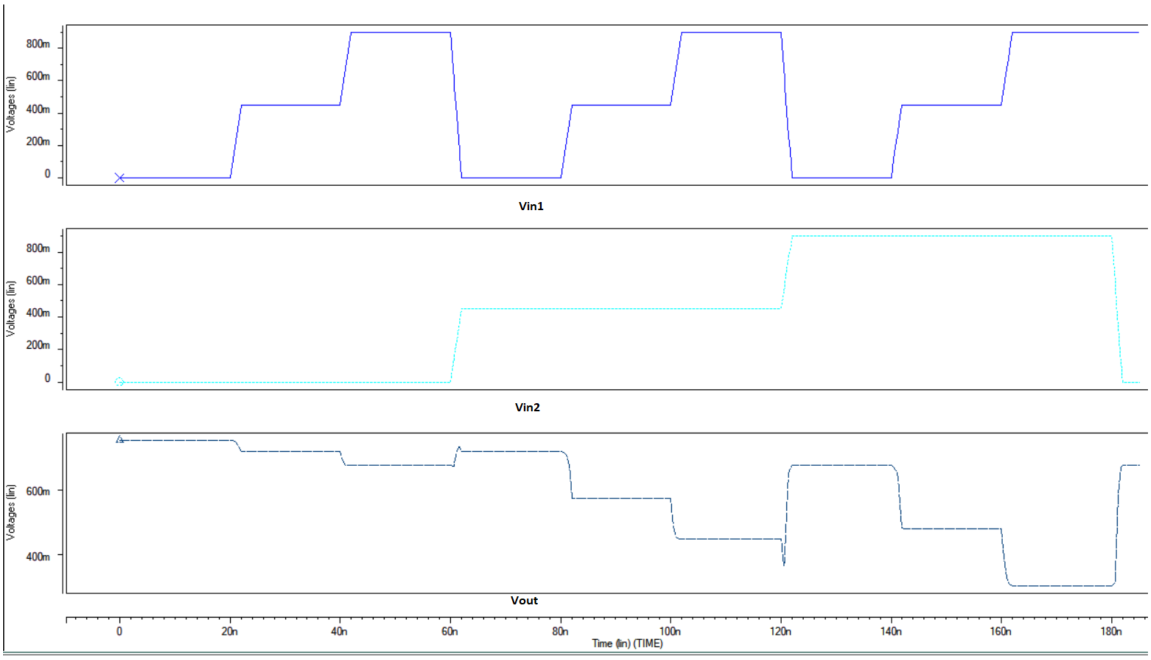

Figure 16: Transient Analysis Proposed Standard Ternary NAND gate.

7.5 Transient Analysis of Proposed Standard Ternary NOR circuit

The given waveform represents the input-output behavior of a standard ternary NOR (T-NOR) gate implemented using CNTFET technology at the 32nm node in Synopsys HSPICE. The first two plots show the input voltages Vin1 and Vin2, which transition through the three ternary logic levels: 0V **(**Logic 0), ~400mV (Logic 1), and ~800mV (Logic 2)**.** The third plot displays the corresponding output voltage Vout, which follows the ternary NOR operation: Vout = NOT (max(Vin1, Vin2))**.** This means that when either Vin1 or Vin2 is at Logic 2 (~800mV), Vout is at Logic 0 (~200mV); when both inputs are at Logic 0, Vout reaches its highest level (~600mV, Logic 2**)**. The waveform confirms correct ternary NOR functionality, demonstrating smooth transitions and proper ternary logic behavior, verifying that the T-NOR gate operates correctly for ternary logic applications.

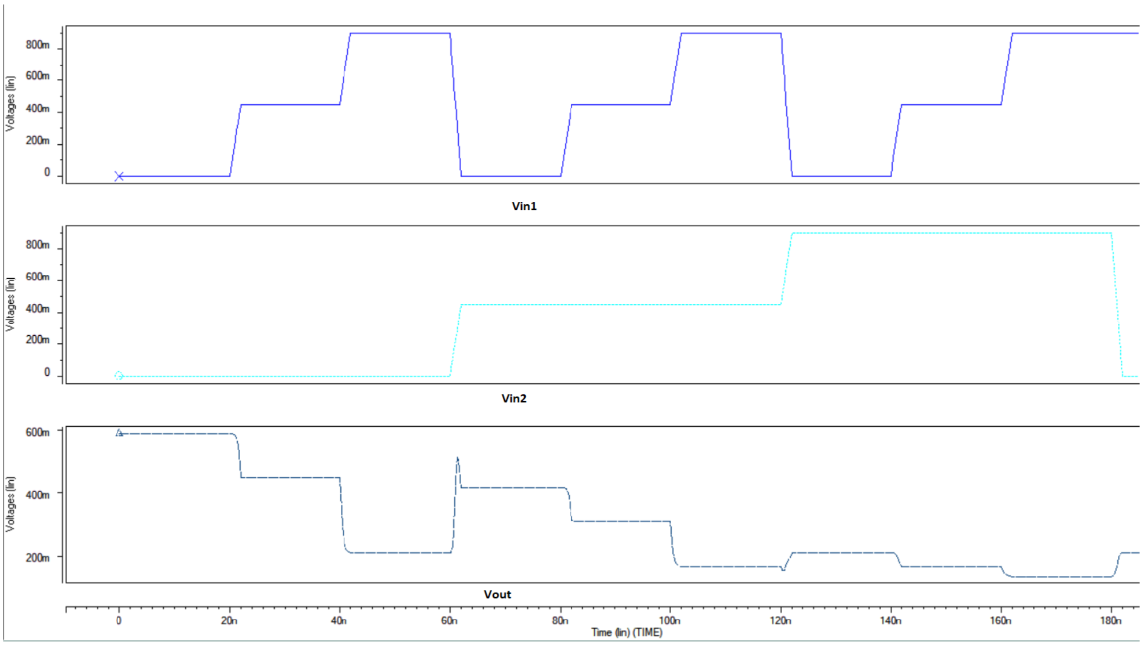

Figure 17: Transient Analysis Proposed Standard Ternary NOR gate.

7.6 RESULT ANALYSIS

This section examines the delay, power consumption, and power-delay product (PDP) of essential ternary logic circuits. The analysis focuses on the ternary inverter, ternary NAND, and ternary NOR gates.

CIRCUIT PERFORMANCE METRICS

The evaluation is based on three primary parameters:

1. **Delay (s):** The propagation delay represents the time taken for the circuit output to transition after an input change.
2. **Power Consumption (W):** The average power dissipated by the circuit during its operation.
3. **Power-Delay Product (PDP) (J):** A key metric that indicates the trade-off between speed and power efficiency. It is given by: PDP=Power × Delay

A lower PDP value signifies a more efficient circuit in terms of power consumption and speed. Performance Metrics of Ternary Logic Gates and Ternary Inverters

Table 5: Performance Metrics of Standard Ternary Inverters

Designs	Avg. power (nW)	Delay (Ps)	PDP (aJ)	Transistors	Chiralities
Proposed	269.65	87.63	23.629	4	7,10
[22]	166.61	774.92	129.10	6	19,13,10
[23]	93.171	993.73	92.58	6	19,10,13

As seen above all designs of STI designs. The proposed design is clearly best among all designs because it consumes less power and has lowest delay and lowest PDP. Hence indicating highest energy efficient. Design [22] might be considered if higher power is acceptable for modest speed gain over [23]. Design [23] is worst in all metrics highest power, longest delay, worst PDP. Design [23] is worst in all metrics highest power, longest delay, worst PDP.

Table 6: Performance Metrics of Ternary NAND gates

Designs	Avg. Power (nW)	Delay (Ps)	PDP (aJ)	Transistors	Chiralities
Proposed	86.31	6032.6	520.6	6	7,10
[22]	175.99	6503.6	1144.5	10	19,13,10
[24]	567.77	79322	45036	10	19,10

As seen above all designs of NAND gate. The Proposed design clearly the best among all designs because it consumes less power and has lowest delay among above all designs of NAND gate designs.

Table 7: Performance Metrics of Ternary NOR gates

Designs	Avg. power (nW)	Delay (ps)	PDP (aJ)	Transistors	Chiralities
Proposed	32.010	76.367	2.44	6	7,10
[22]	176.25	3098.8	546.16	10	19,13,10
[25]	368.86	578.9	213.58	10	19,8,13

As seen above all designs of NOR gate. The Proposed design is clearly the best among all designs because it consumes less power and has lowest delay and lowest PDP hence indicating highest energy efficient.

Chapter 8

SUMMARY OF RESEARCH WORK

The primary goal of this research was to explore the properties of carbon nanotubes (CNTs), design a digital circuit using an HSPICE-compatible model, and evaluate its performance based on simulation results. This research focuses on the design and simulation of standard ternary inverters (STI) and universal gates (TNAND, TNOR) using CNTFET technology in Synopsys HSPICE. The performance of these circuits was analyzed based on propagation delay, power dissipation, and power-delay product (PDP). The results demonstrate that CNTFET-based ternary logic provides significant advantages over Existing Ternary STI and TNAND TNOR circuits, including lower power consumption, improved efficiency, and scalability for future computing applications**.** The ternary inverter exhibited the lowest delay, while the ternary NOR and NAND showed better power efficiency despite higher power dissipation. These findings highlight the potential of CNTFET-based ternary logic for low-power and high-performance digital circuits, paving the way for next-generation multi-valued logic systems.

8.1 CONCLUSIVE REMARK

The study started with stressing the increasing need for developments in semiconductor technology. Of the several new technologies under investigation, carbon nanotubes (CNTs) stood out as one of the most intriguing prospects. We went to great lengths about the special qualities of CNTs and their manufacturing methods. Additionally, we investigated the construction of a simulation-compatible model for HSPICE and the equivalent circuit’s representation of field-effect transistors (FETs) made from CNTs. Important properties and parameters of CNTs were established and included in the simulation model. We then designed and simulated a digital circuits in HSPICE using this CNT-based model. We compared the proposed models of CNTFET and with existing CNTFET Models. Comparatively to propose CNTFETs revealed better power, delay and power delay product. Under high-capacitive loads, CNTFETs exhibit reduced load-driving capacity due to their very small gate dimensions. Not with standing this restriction proposed CNTFETs circuits showed noticeably better power-delay product performance. The results generally confirm that ternary logic circuits are well-suited for the implementation of CNTFET technology. Its notable power efficiency and design scalability point to great possibilities for use in the next low-power, high-performance computers.

8.2 SCOPE FOR FUTURE WORK

This work aimed to investigate the properties of CNFETs and assess their performance in relation to Existing Ternary STI and Universal Gates, enabling more research and useful applications of CNTFETs in the real world. The results give researchers important new perspectives on how carbon nanotubes built digital circuits behave, so providing a basis for future performance prediction once large-scale CNFET construction becomes practical.

The present model applied in this work is based on a simplified band structure for MOSFET-like CNFETs, so restricting its use to low-power digital systems. Including a more realistic and thorough band structure will make CNFET applicable in both low- and high-power domains. This work aims to improve current natural flow models by taking into account parasitic effects from interconnects and other circuit components, thereby more accurately reflecting real-world conditions.

Analyzing performance variations resulting from changes in environmental elements such as temperature and pressure could be additional improvements to the model. Such thorough research would help create better CNFET building techniques and enable higher-performance circuit designs in future technologies.Here future scope of CNTFET and ternary logic research includes:

1. **Device Improvement**: Optimizing CNT synthesis, contact engineering, and enhancing reliability for better CNTFET performance.
2. **Advanced Circuit Design**: Developing low-power ternary gates, memory, and arithmetic units using CNTFETs.
3. **High-Density Computing**: Leveraging ternary logic with CNTFETs for ultra-dense, power-efficient circuits in processors and memory.
4. **Emerging Applications**: Exploring CNTFET-based ternary circuits in AI, neuromorphic computing, IoT, and wearable devices.
5. **EDA Tool Development**: Creating simulation models and design libraries for ternary logic.
6. **Scalability and Integration**: Addressing large-scale manufacturing challenges and integrating CNTFETs with existing CMOS technologies.
7. **Eco-Friendly Electronics**: Using CNTFETs for sustainable and energy-efficient device designs.

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APPENDIX:

This section provides the SPICE netlist of the proposed ternary inverter and NAND, NOR gates.

Ternary Inverter Using CNTFET

```
.TITLE 'CNTFET TERNARY INVERTER'

****************************************************
.options POST
.options AUTOSTOP
.options INGOLD=2     DCON=1
.options GSHUNT=1e-12 RMIN=1e-15
.options ABSTOL=1e-5  ABSVDC=1e-4
.options RELTOL=1e-2  RELVDC=1e-2
.options NUMDGT=4     PIVOT=13

.param   TEMP=27
****************************************************


****************************************************
*Include relevant model files
****************************************************
.lib 'CNFET.lib' CNFET
****************************************************
.param supply=0.9
.param vd='supply'

****************************************************
*Beginning of circuit and device definitions
****************************************************

*Some CNFET parameters:
.param Ccsd=0      CoupleRatio=0
.param m_cnt=1     Efo=0.6
.param Wg=0        Cb=40e-12
.param Lg=32e-9    Lgef=100e-9
.param Vfn=0       Vfp=0
.param m=19        n=0
.param Hox=4e-9    Kox=16

vdd 2 0 0.9
vdd1 4 0 0.45

vpulse 1 0 pwl(0n 0v 60n 0v 62n 0.45v 120n 0.45v 122n 0.9v 180n 0.9v 182n 0v)

* Main Circuits
************************************************************************

* pFET
```

```
X1 3 1 2 2 PCNFET Lch=Lg  Lgeff='Lgef' Lss=32e-9  Ldd=32e-9
+ Kgate='Kox' Tox='Hox' Csub='Cb' Vfbp='Vfp' Dout=0  Sout=0  Pitch=20e-9  n1=m  n2=n  tubes=3

X2 3 0 4 2 PCNFET Lch=Lg  Lgeff='Lgef' Lss=32e-9  Ldd=32e-9
+ Kgate='Kox' Tox='Hox' Csub='Cb' Vfbp='Vfp' Dout=0  Sout=0  Pitch=20e-9  n1=m  n2=n  tubes=3

* nFET
X3 3 1 0 0 NCNFET Lch=Lg  Lgeff='Lgef' Lss=32e-9  Ldd=32e-9
+ Kgate='Kox' Tox='Hox' Csub='Cb' Vfbn='Vfn' Dout=0  Sout=0  Pitch=20e-9  n1=m  n2=n  tubes=3

X4 3 2 4 0 NCNFET Lch=Lg  Lgeff='Lgef' Lss=32e-9  Ldd=32e-9
+ Kgate='Kox' Tox='Hox' Csub='Cb' Vfbn='Vfn' Dout=0  Sout=0  Pitch=20e-9  n1=m  n2=n  tubes=3

********************************************************************************
* Measurements
********************************************************************************
.options runlvl=0
.tran 20n 185n
.dc vpulse 0 0.9v 0.01
.measure tran tplh trig v(1) val=0.45v fall=1 targ v(3) val=0.45v rise=1
.measure tran tphl trig v(1) val=0.45v rise=1 targ v(3) val=0.45v fall=1
.measure tran tpd param='((tphl+tplh)/2)
.measure TRAN max_pwr MAX p(vdd) from=0n to=100n
.measure TRAN avg_pwr AVG p(vdd) from=0n to=100n
.op
.end
```

Ternary NAND Using CNTFET

```
.TITLE 'CNTFET TERNARY NAND'
*********************************************************
.options POST
.options AUTOSTOP
.options INGOLD=2     DCON=1
.options GSHUNT=1e-12 RMIN=1e-15
.options ABSTOL=1e-5  ABSVDC=1e-4
.options RELTOL=1e-2  RELVDC=1e-2
.options NUMDGT=4     PIVOT=13

.param   TEMP=27
*********************************************************


*********************************************************
*Include relevant model files
*********************************************************
.lib 'CNFET.lib' CNFET
*********************************************************
.param supply=0.9
.param vd='supply'

*********************************************************
*Beginning of circuit and device definitions
*********************************************************
```

```
*Some CNFET parameters:
.param Ccsd=0      CoupleRatio=0
.param m_cnt=1     Efo=0.6
.param Wg=0        Cb=40e-12
.param Lg=32e-9    Lgef=100e-9
.param Vfn=0       Vfp=0
.param m=19        n=0
.param Hox=4e-9    Kox=16

vdd 2 0 0.9
vdd1 6 0 0.45

vpulse  1 0 pwl(0n 0v 20n 0v 22n 0.45v 40n 0.45v 42n 0.9v 60n 0.9v 62n 0v 80n 0v 82n 0.45v 100n 0.45v
102n 0.9v 120n 0.9v 122n 0v 140n 0v 142n 0.45v 160n 0.45v 162n 0.9v 180n 0.9v 182n)
vpulse1 5 0 pwl(0n 0v 60n 0v 62n 0.45v 120n 0.45v 122n 0.9v 180n 0.9v 182n 0v)

* Main Circuits
************************************************************************

X1 3 1 2 2 PCNFET Lch=Lg  Lgeff='Lgef' Lss=32e-9  Ldd=32e-9
+ Kgate='Kox' Tox='Hox' Csub='Cb' Vfbp='Vfp' Dout=0  Sout=0  Pitch=20e-9  n1=m  n2=n  tubes=3

X2 3 5 2 2 PCNFET Lch=Lg  Lgeff='Lgef' Lss=32e-9  Ldd=32e-9
+ Kgate='Kox' Tox='Hox' Csub='Cb' Vfbp='Vfp' Dout=0  Sout=0  Pitch=20e-9  n1=m  n2=n  tubes=3

X3 3 1 4 0 NCNFET Lch=Lg  Lgeff='Lgef' Lss=32e-9  Ldd=32e-9
+ Kgate='Kox' Tox='Hox' Csub='Cb' Vfbn='Vfn' Dout=0  Sout=0  Pitch=20e-9  n1=m  n2=n  tubes=3

X4 4 5 0 0 NCNFET Lch=Lg  Lgeff='Lgef' Lss=32e-9  Ldd=32e-9
+ Kgate='Kox' Tox='Hox' Csub='Cb' Vfbn='Vfn' Dout=0  Sout=0  Pitch=20e-9  n1=m  n2=n  tubes=3

X5 3 0 6 2 PCNFET Lch=Lg  Lgeff='Lgef' Lss=32e-9  Ldd=32e-9
+ Kgate='Kox' Tox='Hox' Csub='Cb' Vfbp='Vfp' Dout=0  Sout=0  Pitch=20e-9  n1=m  n2=n  tubes=3

X6 3 2 6 0 NCNFET Lch=Lg  Lgeff='Lgef' Lss=32e-9  Ldd=32e-9
+ Kgate='Kox' Tox='Hox' Csub='Cb' Vfbn='Vfn' Dout=0  Sout=0  Pitch=20e-9  n1=m  n2=n  tubes=3

************************************************************************
* Measurements
************************************************************************
.options runlvl=0
.tran 20n 185n
.dc vpulse 0v 0.9v 0.2
.measure tran tplh trig v(1) val=0.45v fall=1 targ v(3) val=0.45v rise=1
.measure tran tphl trig v(1) val=0.45v rise=1 targ v(3) val=0.45v fall=1
.measure tran tpd param='((tphl+tplh)/2)
.measure TRAN max_pwr MAX p(vdd) from=0n to=185n
.measure TRAN avg_pwr AVG p(vdd) from=0n to=185n
.op
.end
```

Ternary NOR Using CNTFET

```
.TITLE 'CNTFET TERNARY NOR'
****************************************************
.options POST
.options AUTOSTOP
.options INGOLD=2     DCON=1
.options GSHUNT=1e-12 RMIN=1e-15
.options ABSTOL=1e-5  ABSVDC=1e-4
.options RELTOL=1e-2  RELVDC=1e-2
.options NUMDGT=4     PIVOT=13

.param   TEMP=27
****************************************************


****************************************************
*Include relevant model files
****************************************************
.lib 'CNFET.lib' CNFET
****************************************************
.param supply=0.9
.param vd='supply'

****************************************************
*Beginning of circuit and device definitions
****************************************************

*Some CNFET parameters:
.param Ccsd=0      CoupleRatio=0
.param m_cnt=1     Efo=0.6
.param Wg=0        Cb=40e-12
.param Lg=32e-9    Lgef=100e-9
.param Vfn=0       Vfp=0
.param m=19        n=0
.param Hox=4e-9    Kox=16

vdd 2 0 0.9
vdd1 6 0 0.45

vpulse  1 0 pwl(0n 0v 20n 0v 22n 0.45v 40n 0.45v 42n 0.9v 60n 0.9v 62n 0v 80n 0v 82n 0.45v 100n 0.45v
102n 0.9v 120n 0.9v 122n 0v 140n 0v 142n 0.45v 160n 0.45v 162n 0.9v 180n 0.9v 182n)
vpulse1 4 0 pwl(0n 0v 60n 0v 62n 0.45v 120n 0.45v 122n 0.9v 180n 0.9v 182n 0v)

* Main Circuits
*************************************************************************

X1 3 1 2 2 PCNFET Lch=Lg  Lgeff='Lgef' Lss=32e-9  Ldd=32e-9
+ Kgate='Kox' Tox='Hox' Csub='Cb' Vfbp='Vfp' Dout=0  Sout=0  Pitch=20e-9  n1=m  n2=n  tubes=3

X2 5 4 3 2 PCNFET Lch=Lg  Lgeff='Lgef' Lss=32e-9  Ldd=32e-9
+ Kgate='Kox' Tox='Hox' Csub='Cb' Vfbp='Vfp' Dout=0  Sout=0  Pitch=20e-9  n1=m  n2=n  tubes=3

X3 5 1 0 0 NCNFET Lch=Lg  Lgeff='Lgef' Lss=32e-9  Ldd=32e-9
+ Kgate='Kox' Tox='Hox' Csub='Cb' Vfbn='Vfn' Dout=0  Sout=0  Pitch=20e-9  n1=m  n2=n  tubes=3
```

```
X4 5 4 0 0 NCNFET Lch=Lg  Lgeff='Lgef' Lss=32e-9  Ldd=32e-9
+ Kgate='Kox' Tox='Hox' Csub='Cb' Vfbn='Vfn' Dout=0  Sout=0  Pitch=20e-9  n1=m  n2=n  tubes=3

X5 6 0 5 2 PCNFET Lch=Lg  Lgeff='Lgef' Lss=32e-9  Ldd=32e-9
+ Kgate='Kox' Tox='Hox' Csub='Cb' Vfbp='Vfp' Dout=0  Sout=0  Pitch=20e-9  n1=m  n2=n  tubes=3

X6 5 2 6 0 NCNFET Lch=Lg  Lgeff='Lgef' Lss=32e-9  Ldd=32e-9
+ Kgate='Kox' Tox='Hox' Csub='Cb' Vfbn='Vfn' Dout=0  Sout=0  Pitch=20e-9  n1=m  n2=n  tubes=3

***********************************************************************
* Measurements
***********************************************************************
.options runlvl=0
.tran 20n 185n
.dc vpulse 0v 0.9v 0.2
.measure tran tplh trig v(1) val=0.45v fall=1 targ v(3) val=0.45v rise=1
.measure tran tphl trig v(1) val=0.45v rise=1 targ v(3) val=0.45v fall=1
.measure tran tpd param='((tphl+tplh)/2)
.measure TRAN max_pwr MAX p(vdd) from=0n to=185n
.measure TRAN avg_pwr AVG p(vdd) from=0n to=185n
.op
.end
```

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