DESIGN AND ANALYSIS OF CMOS ANALOG COMPARATORS

Thesis Submitted towards the Partial Fulfillment of

Requirement For the Award of the Degree of

Master of Engineering

IN

Electronics and Communication

By

JYOTI KEDIA

(8024110)

Under the guidance of

Mrs. ALPANA AGARWAL

Department of Electronics & Communication Engineering

Thapar Institute Of Engineering & Technology

(Deemed University), Patiala

Certificate

This is to certify that the Thesis report entitled **" Design and analysis of CMOS Analog Comparators "** which is being submitted herewith by Ms. Jyoti kedia (Roll No. 8024110) towards the partial fulfillment for the award of the degree of **Master of Engineering (Electronics & Communication)** of Thapar Institute of Engineering & Technology (Deemed University), Patiala is a bonafide work carried by her under my supervision and guidance during the session 2003-2004.

It is further certified that the research work embodied in this thesis has not been submitted to any other University/Institute for the award of any degree/diploma.

02/06/04
Mrs. Alpana Agarwal
Asstt. Prof.
ECED
TIET, Patiala
(Supervisor)

Counter Signed by:

Dr. R.S. Kaler 2/6/04
Prof. and HOD,
ECED,
TIET, Patiala

Dr. D.S. Bawa
Dean of Academic Affairs
TIET, Patiala

ACKNOWLEDGEMENT

It is my great pleasure to express my sincere gratitude to Asstt. Prof. Alpana Agarwal for her guidance and invaluable advice imparted throughout the project work. I look upon her with great respect for her profound knowledge and relentless pursuit for perfection. Her ever-encouraging attitude has been immensely valuable.

I shall be failing in my duties if I do not express my deep sense of gratitude towards Dr. R.S. Kaler, Prof. & Head of the Deptt. of Electronics & Communication Engineering Technology (Deemed University), Patiala who has been a constant source of inspiration for me throughout the thesis semester.

I would also like to thank Mr. Sanjay Batish and Mrs. Sushma Jain for extending all their support in the VLSI Laboratory.

Last, but not the least, I express my cordial thanks to all my friends for being there whenever I needed them and for their support and motivation. I am also grateful to my family members whose guidance and encouragement has led me up to this stage of my career.

Kedia

Date: 02·06·04

(Jyoti Kedia)

Table of Contents

ABSTRACT

A comparator is the basic component mainly used in analog-to-digital converters. Ideally, it generates an output logic signal as an instant response to the sign of an analog input (voltage or current). Obviously, a real circuit doesn't achieve the ideal function. The most important limits are the finite sensitivity, the offset and the finite speed. All these limitations affect the performance of systems where comparators are used, especially when it is required to achieve high-speed (or a high conversion rate) and high resolution.

The open loop, two-stage comparator makes an excellent high gain realization. The characterization of the two stages, open loop comparator illustrates the performance capabilities. The performance of the open loop comparator can be improved by the use of hysterisis to remove the influence of a noisy input signal. Hysterisis can be introduced in internal as well as external circuits of the comparator. All of these use positive feedback. Autozeroing can be used in comparators to reduce the input offset voltage. It is seen that self-biased comparators were always stable in the autozeroing techniques.

In many comparator applications, the signal is discrete rather than continuous. So in this case it is possible to use regenerative circuits as comparators. These are comparatively fast. It also uses positive feedback. Unfortunately, the transient response of regenerative circuits is characterized by a positive exponential. Therefore, if input signal is small a long time will be required for the signal to reach the region of the exponential response where the slope is steep. A solution to this is to cascade the latch with a preamplifier. This is what we called a high-speed amplifier. The function of the preamplifier is to quickly build up the input to the latch so that slow rate of rise of the exponential response can be avoided. This has resulted in a comparator capable of operating with slew rate up to 2.28 V/ns and greater. A comparator configuration using differential two-stage open loop comparator as the input stage is realized for high-speed applications.

The comparators that can drive large capacitance at the output are the self-biased comparators. The configuration is completely complementary i.e. each n-type device operates in push-pull fashion with a corresponding p-type device. It is self-biased through negative feedback. These two differences result in several performance enhancements desirable in comparator applications. The self-biased comparator architecture is the two folded cascode differential amplifiers acting as load for each other. The self-biasing of the amplifier creates the negative feedback loop that stabilizes the bias voltages. The comparator designed has minimum delay. Gain can be decreased to further reduce the delay.

The physical mask layout of any circuit to be manufactured using a particular process must confirm to a set of geometric constraints or rules, which are generally called layout design rules. Using the analog layout techniques of matching transistors and stacked layout one can develop the layout of any analog circuit. A layout of self-biased comparator is developed which works satisfactorily.

LIST OF FIGURES

LIST OF TABLES

INTRODUCTION

1.1 WHAT IS A COMPARATOR?

The electrical function of a comparator is to generate an output voltage with value high or low depending on whether the sign of the input is positive or negative. We can have two different types of input: voltage or current. In the former case the input voltage is measured with respect to a given reference level. Therefore, the comparator determines whether the amplitude of the input is higher or not than a reference. When the current is the input variable the comparator determines whether the input current is flowing in or out of the input terminal.

A logical signal denotes the output. The amplitude of electrical representation of the high or the low state should match the convention used in the associated digital logic to clearly distinguish between logic1and a logic 0.

When a comparator is used in a sampled data system a clock controls the action of the circuit. The comparator provides the output with a given periodicity synchronous with the clock. Therefore, a given time interval is available to achieve the result. Often, the fast variation of the input signal and the defined speed of the circuit used determine the need to separate the two functions inherent to the comparison process: to " catch" the value of the input signal and to generate the logic output. A sampled data system favours this disjunction: the clock period can be divided into two or more phases: one completes the sampling of input and other transforms the result into the logic signal. The latter non-linear operation can take advantage of the use of a latch. A latch effects a regenerative amplification of the input and, thanks to its positive feedback, preserves the achieved output.

In various types of analog signal processing and analog to digital conversion the most important part in the circuit is comparator. The comparator is a circuit that compares an analog signal with another analog signal or reference and outputs a binary signal based on the comparison. Here analog is one that can have any of a continuum of amplitude values at a given point in time. In the strictest sense a binary signal can have only one of the two values at a given point of time, but in real world, where there is a transition region between the two binary states. It is important for the comparator to pass quickly through the transition region.

The comparator is widely used in the process of converting analog signals to digital signals. In A/D conversion process, it is first necessary to sample the input. This sampled signal is then applied to a combination of comparators to determine the digital equivalent of the analog signal. In its simplest form comparator can be considered as a 1-bit analog to digital converter.

We will see that comparators can be divided into open loop and regenerative comparators. The open loop comparators are basically opamps without compensation. Regenerative comparators use positive feedback, similar to flip-flops, to accomplish the comparison of the magnitude between two signals. A third type of comparator that emerges is a combination of open loop and regenerative comparators. This combination results in comparators that are extremely fast. Very high-speed comparators exploit just the initial part of the gain stages time response. Successive stages and a latch take care of further signal amplification.

1.2 CHARACTERISTICS OF A COMPARATOR

We shall characterize the comparator by the following aspects:

- Resolving capability
- Speed or propagation time delay
- Slew rate
- Input offset voltage
- Power consumption
- Settling time
- Hysterisis

- Latching Compatibility
- Trip point

A comparator was defined as a circuit that has a binary output whose value is based on a comparison of two analog inputs. As shown in the Figure1.1, the output of the comparator is high (V_{OH}) when the difference between the noninverting and inverting inputs is positive, and low (V_{OL}) when this difference is negative. The ideal aspect of the model is the way in which the output makes a transition between V_{OL} and V_{OH}. The output changes state for an input change of ΔV, where ΔV approaches zero. This implies a gain of infinity, as shown

$$\text{Gain} = \text{Av} = \lim_{\Delta V \to 0} \frac{V_{OH} - V_{OL}}{\Delta V}$$

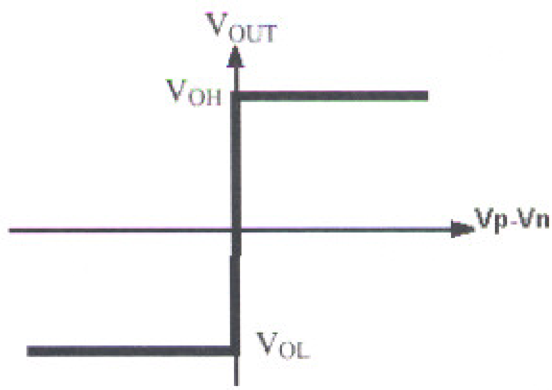


Figure 1.1: Ideal transfer curve

Practically, as shown in the Figure-1.2 we have

$$\text{Gain} = \text{Av} = \frac{V_{OH} - V_{OL}}{V_{IH} - V_{IL}}$$

Where V_{IH} and V_{IL} represent the input-voltage difference V_P-V_N needed to just saturate the output at its upper and lower limit, respectively. This input change is called the ***resolution*** of the comparator. Gain is very important characteristics describing comparator operation, for it defines the minimum amount of input change (resolution) necessary to make the output swing between the two binary states.

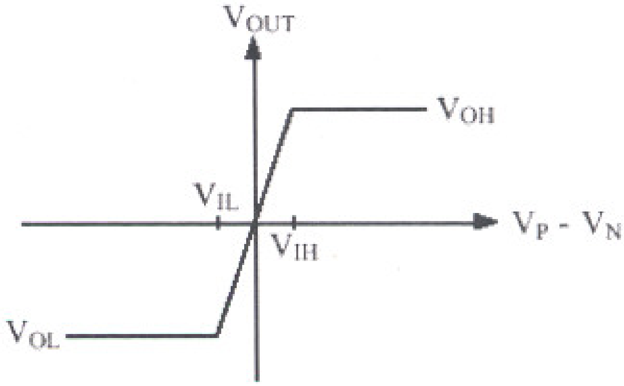


Figure 1.2: Transfer curve of a comparator with finite gain.

The second non-ideal effect seen in comparator is ***input offset voltage*** in Figure-1.3 the output changes as the input difference crosses zero. If the output did not change until the input difference reached a value V_{os}, then this difference would be defined as the offset voltage. We can also say that it is the voltage that must be applied to the input to obtain the crossing point between low and high logic level. This would not be a problem if the offset could be predicted but it varies randomly from circuit to circuit [20]. Because the input to the comparator is usually differential, the input common mode range is also important. The ICMR for a comparator would be that range of input common mode voltage over which the comparator functions normally.

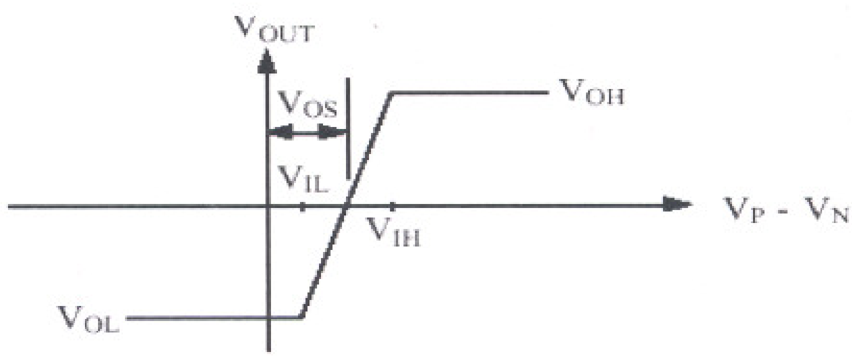


Figure1.3: Transfer curve of a comparator including input offset voltage

The characteristic delay between input excitation and output transition is the time response of the comparator. Figure-1.4 shows the response of a comparator to an input as a function of time. As we can see there is a delay between the input excitation and output response. This time difference is called the ***propagation delay time*** of the comparator. It is very important parameter since it is often the speed limitation in the conversion rate of an A/D converter. The propagation delay time in comparator generally varies as a function of the amplitude of the input. A larger input will result in a smaller delay time. There is an upper limit at which a further increase in the input voltage will no longer affect the delay. This mode of operation is called slewing or ***slew rate***. The next important characteristic is ***settling time*** [18]. This is the time that the output voltage requires, under given operating conditions, to achieve the expected output voltage within a given accuracy. The settling time is measured from the end of the slewing period. It critically depends on the phase margin: a poor phase margin leads to a ringing response that augments the settling period.

If the propagation delay time is determined by the slew rate of the comparator, then this time can be given by

$$t_P = \Delta T = \frac{\Delta V}{SR} = \frac{V_{OH} - V_{OL}}{2 * SR}$$

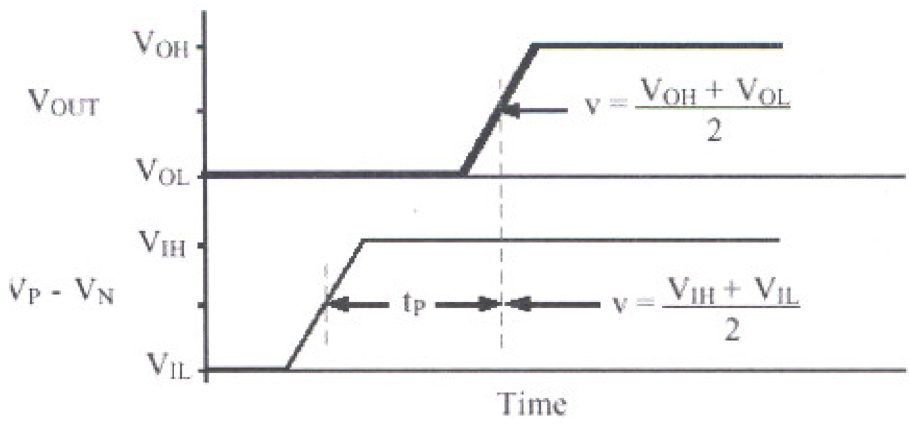


Figure1.4: Propagation delay time of a noninverting comparator

In the case where the propagation delay time is determined by the slew rate, the most important factor to decrease the propagation time is increasing the sinking or sourcing capability of the comparator.

Power consumption [18] is the power consumed under stand by conditions. Moreover, the power consumed depends upon the speed specifications. Low power operation is a very important quality factor: more and more electronic systems are powered by batteries. Therefore a key design task is to achieve the minimum power consumption for a given required speed.

The comparison threshold for the input signals changing from low to high can be different from the threshold to signals changing in the opposite direction. The difference between the two thresholds is the ***Hysterisis.*** The effect can be a limit or a benefit, depending upon the applications. For continuous time applications the crossing of a noisy input signal through the reference may produce many transitions high and low of the output voltage. A hysterisis larger than the noise level avoids the effects and results are beneficial.

The characteristics discussed above are of the continuous time comparators. They are applied to clocked comparators using latch as well but some that characterize only the clocked comparators are need to be discussed.

Latching compatibility: The output of the gain stage should properly drive the latch. Therefore, depending on the specific scheme used it is necessary to provide the effective voltage levels at the input of the latch. The clock operation leads, in addition to the static ***power consumption***, to a dynamic contribution. It depends, like in digital circuits, on the clock frequency and the capacitances that the preamplifier and the latch are required to charge and discharge. ***Amplifier response time*** is the minimum time interval required to achieve the proper logic output as a response to a minimum input step. The latch needs a given signal at its inputs to ensure the logic output. The preamplifier stage achieves this level in a time that depends on the input step amplitude: the step response time of a gain stage is a ramp during the slewing that turns into an exponential in the linear region.

1.3 OBJECTIVE OF THE WORK

In today's world everything is digitized but nature is analog. So we do need to convert the analog into digital, in which comparator is the most important. Therefore, the various design issues related to the speed, gain, power dissipation, propagation delay and resolution are of paramount importance. We need to investigate different types of comparator circuits and evaluate their properties in order to find their suitability for A/D applications. The objective of our work is to design the different comparators and evaluate their performance. The design procedures are simulated and performance evaluation is done by comparing the different comparators in terms of characteristics required.

1.4 ORGANISATION OF THE THESIS

Chapter 1 introduces the project and describes the objective of the project-work, along with the organization of the thesis.

Chapter 2 presents the literature survey discussing the different comparator circuits. It also describes the salient features of different comparators configurations that satisfy the requirements for comparators.

Chapter 3 deals with the design of Two-stage comparator. The design procedure is discussed here with the specifications. Finally, an example with given specifications is taken for the design

.

Chapter 4 discusses the design of Clocked comparator using basic latch. The design procedure is discussed here with the specifications. An example with given specifications is taken for the design

Chapter 5 describes the design of Self-Biased comparator. The design procedure is discussed here with the specifications. Finally, an example with given specifications is taken for the design

Chapter 6 deals with the tanner tools being used.

Chapter 7 gives the layout techniques and layout design rules for analog circuits. At the end of this chapter, the layout of self-biased comparator is described.

Chapter 8 illustrates the results and discusses the same.

Chapter 9 finally gives the conclusions and the scope for future work. After this chapter, a list of important references used to comprehend the theoretical concepts related to the thesis work, is included.

Appendix includes

"Design Of Clocked Comparator Using Basic Latch", Jyoti kedia, Alpana Agarwal and Chandra Shekhar* Thapar Institute of Engineering and Technology, PATIALA. *Central Electronics Engineering Research Institute, PILANI, presented in National conference on VLSI design and Technology, Bhartiya Vidyapeeth College of engineering, New Delhi, held on 15-16 April 2004.

"*Comparative analysis of CMOS analog comparators*", Jyoti kedia, Alpana Agarwal Thapar Institute of Engineering and Technology, Patiala, communicated in Thapar Institute of Engineering and Technology, Patiala.

"*Design of Self-biased comparator*", Jyoti kedia, Alpana Agarwal and Chandra Shekhar*, Thapar Institute of Engineering and Technology, PATIALA *Central Electronics Engineering Research Institute, PILANI, communicated in International conference VDAT 2004.

ANALOG-COMPARATOR ARCHITECTURES

2.1 TWO-STAGE OPEN LOOP COMPARATOR

As we can see from the previous requirements for a comparator reveal that it requires a differential input and sufficient gain to be able to achieve the desired resolution. The best implementation is the two-stage opamp [20] as shown in Figure 2.1. A simplification occurs because the comparator will generally be used in open loop mode and it's not necessary to compensate that. It is preferred so that it has largest bandwidth possible, which will give a faster response.

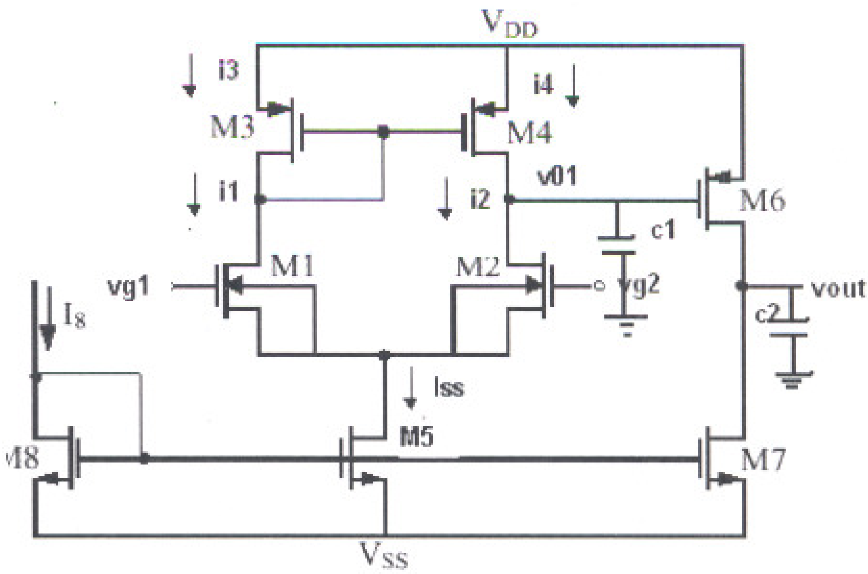


Figure 2.1: Two-stage open loop comparator

2.1.1 INITIAL OPERATING STATES FOR THE TWO-STAGE, OPEN LOOP COMPARATOR

In order to analyze the propagation delay of a slewing, two-stage, open loop comparator, it is necessary to first find the initial operating states of the output voltages of the first and voltages of the first and second stages. The capacitance at the outputs of the first and second stages is $C_1$and C_2, respectively. Consider the two-stage comparator of Figure 2.1.

First we will choose one of the input gates equal to a dc voltage and find the output voltages of the first and second stages when the other input gate is above and below the dc voltage on the first gate. We need to consider two cases for each of the previous possibilities. These cases are when the currents in M1 and M2 are different but neither is zero and when one of the input transistors has a current of Iss and the other current is zero.

Let us first assume that v_{g2} is equal to a dc voltage, V_{g2}, and that $v_{g1} > V_{g2}$ with $i_1 < Iss$ and $i_2 > 0$. In this case, as long as M4 remains in saturation, $i_4 = i_3 = i_1$, which is greater than i_2. Consequently, v_{01} increases because of the difference current flowing into C_1. As v_{01} continues to increase, M4 will become active and $i_4 < i_3$. When the voltage across source drain of M4 decreases to the point where $i_4 = i_2$, the output voltage of the first stage, v_{01} stabilizes. This value of the voltage is

$$V_{dd} - V_{sd4\,(sat)} < v_{01} < V_{dd}, \qquad v_{g1} > V_{g2},\ i_1 < Iss \text{ and } i_2 > 0 \qquad \text{----[1]}$$

Under the conditions of above equation, the value of $v_{sg6} < | V_{tp} |$ and M6 will be off and the output voltage will be

$$V_{out} = V_{ss},\ v_{g1} > V_{g2},\ i_1 < Iss \text{ and } i_2 > 0 \qquad \text{---[2]}$$

If $v_{g1} >> V_{g2}$ then $i_1 = Iss$ and $i_2 = 0$ and v_{01} will be at V_{dd} and v_{out} is still at V_{ss}.Next, assume that v_{g2} is still equal to V_{g2}, and that $v_{g1} < V_{g2}$ with $i_1 > 0$ and $i_2 <Iss$. In this case, $i_4 = i_3 = i_1$, which is less than i_2. Consequently, v_{01} decreases. As v_{01} continues to increase, M2 will become active. When the voltage across source drain of M2

decreases to the point where $i_1 = i_2 = Iss/2$, the output voltage of the first stage, v_{01} stabilizes. At this point,

$$V_{g2} - V_{gs2} < v01 < V_{g2} - V_{gs2} + V_{ds2\,(sat)},\ i_1 > 0,\quad i_2 < Iss \qquad - [3]$$

under this condition the output voltage vout will be near $V_{dd.}$ If $v_{g1} << V_{g2}$, the previous results are still valid until the source voltage of M1 or M2 causes M5 to leave the saturated region. When that happens, Iss decreases and v_{01} approaches Vss and Vout can be determined.

If the gate of M1 is equal to a dc voltage of V_{g1}, we can now get the initial states of the outputs of the first and second stages by repeating the above process. First let us assume that $v_{g1} = V_{g1}$ and $v_{g2} > V_{g1}$ with $i_2 < Iss$ and $i_1 > 0$. As a result , $i_1 < i_2$ gives $i_4 < i_2$ as long as M4 is saturated. Therefore, v_{01} decreases because of difference current flowing out of C1. As v_{01} decreases, M2 will become active and i_2 will decrease to the point where $i_1 = i_2 = Iss/2$. Therefore, v_{01} stabilizes.
The output voltage, vout will be near V_{dd}. If $v_{g2} >> V_{g1}$, the previous results are still valid until the source voltage of M1 and M2 causes M5 to leave the saturated region. When this happens, Iss decreases and v_{01} can approach Vss and vout can be determined.

Next, assume that v_{g1} is still equal to V_{g1}, but now $v_{g2} < V_{g1}$ with $i_1 < Iss$ and $i_2 > 0$. As a result, $i_1 > i_2$, which gives $i_4 > i_2$, causing v_{01} to increase. As long as M4 is saturated, $i_4 > i_2$. When M4 enters the active region, i_4 will decreases until $i_4 = i_2$ at which point v_{01} stabilizes. If $v_{g2} << V_{g1}$, then $i_1 = Iss$ and $i_2 = 0$ and v_{01} will be at V_{dd} and v_{out} is still at V_{ss}.

2.1.2 PROPAGATION DELAY TIME OF SLEWING, TWO-STAGE, OPEN-LOOP COMPARATOR

In most applications, the two stage, open loop comparator [20] is overdriven to the point where the propagation delay time is determined by the slewing performance of the comparator. In this case, the propagation delay time is found by

$$i_i = Ci\ dv_i/dt_i = Ci\ \Delta v_i/\Delta t_i$$

Where Ci is the capacitance if the i^{th} stage. The propagation delay is found by summing the delays of each stage.

The term Δv_i is generally equal to half the output swing of the i_{th} stage. In some cases, the threshold or the *trip point* of the next stage determines its value. The trip point of an amplifier is defined as the value of the input voltage that causes the output to be midway between its limits.

2.2 OTHER OPEN LOOP COMPARATOR

There are many other types of comparators besides the two-stage comparator of the previous section. In this section we will examine comparators with push-pull outputs, the folded–cascode comparator, and comparators capable of driving very large capacitive loads.

2.2.1 PUSH- PULL OUTPUT COMPARATOR

We noted in the two-stage comparator of the previous section that the propagation delay time was due to both the transition of the first stage output and the second stage output. If we replace the current-mirror load in the first stage with MOS diodes (gate- drain connected MOSFETs), then the signal at the output of the first stage will be reduced in magnitude. This type of the comparator is called a *clamped* comparator and is shown in the Figure 2.2.

There are several interesting features of this circuit. First, the gain has reduced because the current – mirror load of the first stage has been replaced by the MOS diodes. Second, we note that the output is push pull. The maximum sinking and sourcing current at the output would be I_5 times any current gain in M3 – M8 (M4 – M6). The gain equivalent to a two stage can be achieved by cascading the output. The large output resistance leads to a single

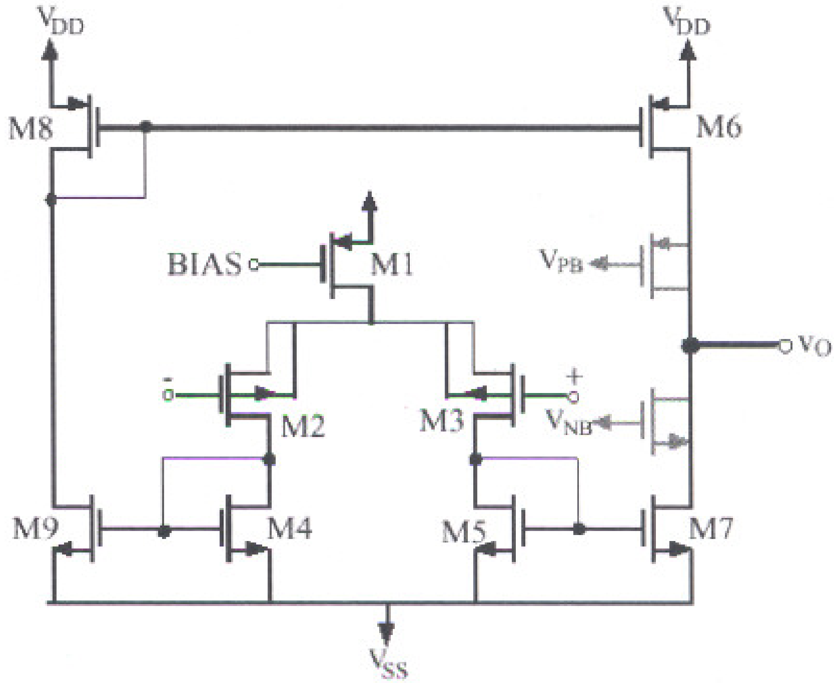


Figure 2.2: Clamped push-pull output comparator

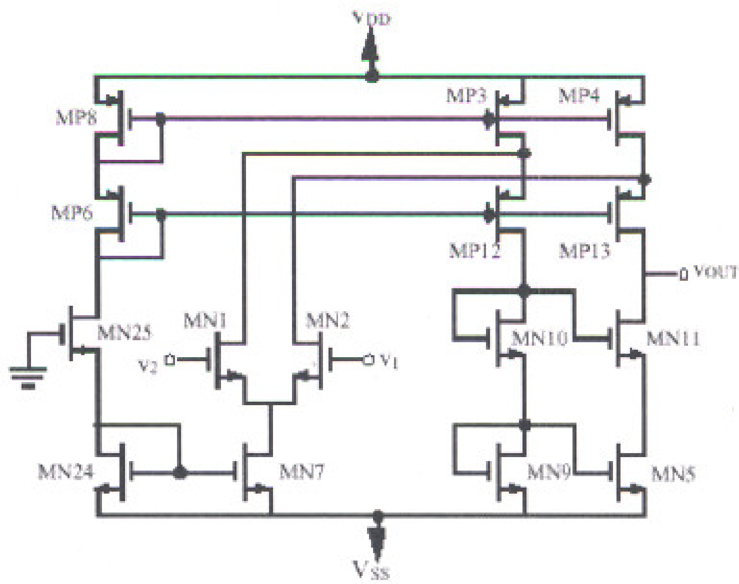


Figure 2.3: Comparator with folded cascode output

pole response. This pole is at lower frequencies than that of the two stages; therefore the linear response will be slower with the same amount of overdrive. However, because the comparator is push- pull, it will be able to source and sink large currents into the output capacitance. If the comparator is slewing, then the clamped comparator with a cascoded output stage can compete with the two stages, open loop comparator.

The folded–cascode op-amp [13,18] can also make a satisfactory comparator. Its performance will be same as that discussed above for cascoded one. The primary difference would be a better-input common mode voltage range because the MOS diodes are not used to load the first stage as shown in Figure 2.3. From a linear speed viewpoint, the comparators with cascoded output stage are slow. In general these types of comparators should not be used if the response is to be linear. They do have satisfactory performance as a comparator if the response is slewing.

2.2.2 COMPARATORS THAT CAN DRIVE LARGE CAPACITIVE LOADS

If a comparator has a large capacitive load the chances are that it is slew rate limited. Under these conditions, we will show several methods capable of driving large capacitance values. The first method is simply to add several push-pull inverters in cascade with the output of a two stage, open loop comparator as shown in Figure 2.4.

The inverters, M8- M9 and M10- M11, allow C-II to be large without sacrificing the speed. The principle is well understood in high-speed digital buffers. If a large capacitance were connected to the drains of M6-M7, the slew rate would be poor because the current sinking and sourcing is not too large. The M8-M9 inverter allows the current capability to be increased without sacrificing the slew rate.

The W/L value of M8 and M9 must be large enough to increase the current sinking and sourcing capability without loading M6 and M7. Similarly, the inverters allow the current sinking and sourcing capability to be further increased without loading M8- M9. It can be shown that, if the W/L increases by a factor of 2.72, the minimum propagation delay time is achieved.

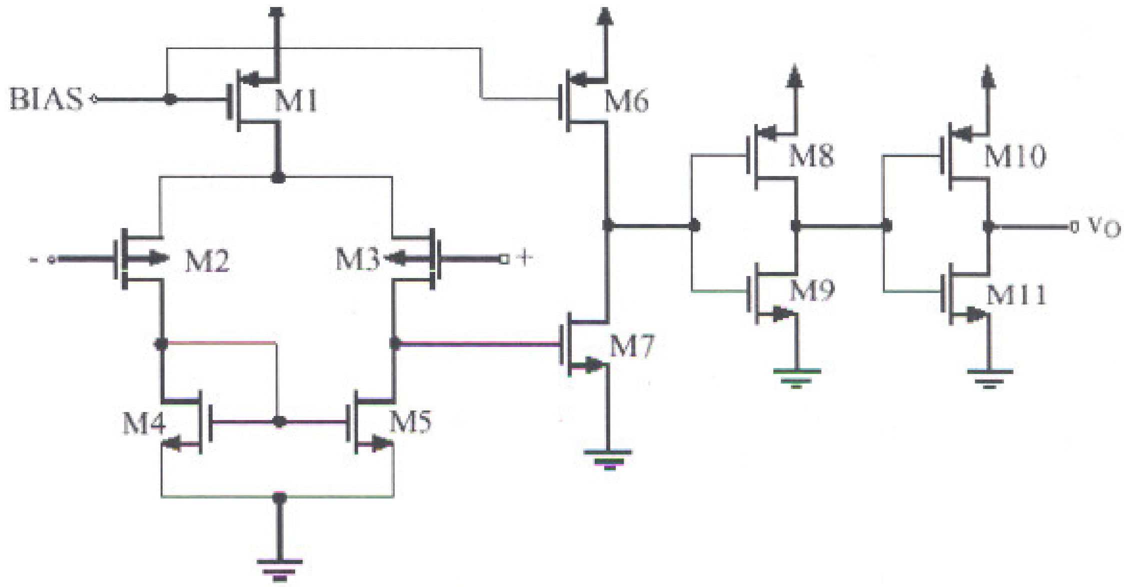


Figure 2.4: Increasing the capacitive drive of a two stage, open loop comparator

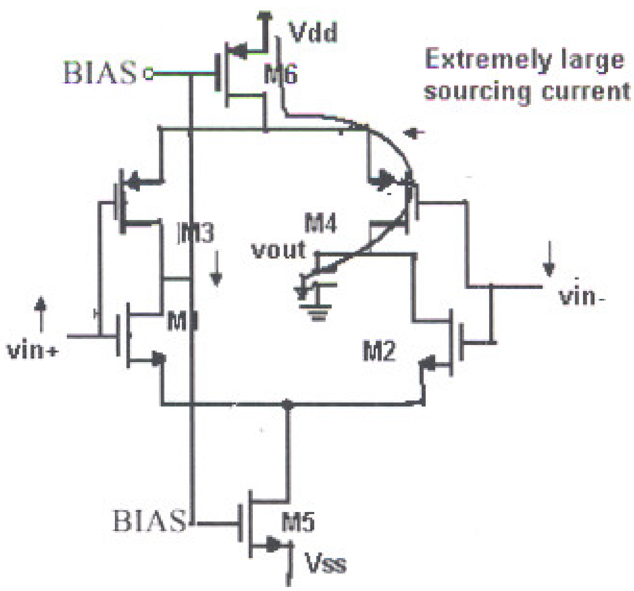


Figure 2.5: Self biased differential amplifier

One of the circuits that have the ability to sink and source large amounts of current is called self-biased differential amplifier as shown in the Figure 2.5. This amplifier consist two differential amplifier each serving as loads for each other. The tail currents of the differential amplifiers become adaptive by connecting the gates of M6 and M7 to the drains of M1 and M3 as shown in Figure 2.5. When the positive input voltage, V_{in+} is increased, the drains of M1 and M3 fall and turn on M6 to a large current, which is sourced to output capacitance connected to the drains of M2 and M4 through M4.

During this condition, the current in M5 is zero. When V_{in+} is decreased, M5 turns on and a large current is sunk through the output capacitance via M2. Thus, this circuit has the ability to source and sink large currents without a large quiescent current. A disadvantage of the circuit is that the delay time from V_{in+} to the output is slower than from V_{in-} to the output.

2.3 IMPROVING THE PERFORMANCE OF OPEN LOOP COMPARATORS

There are two areas in which the performance of an open loop, high gain comparator can be improved with little extra effort. These areas are the input offset voltage and a single transition of the comparator in a noisy environment. The latter problem can be solved by the introduction of hysterisis [13,20] using a bistable circuit. These two techniques will be examined in the following.

2.3.1 AUTOZEROING TECHNIQUES

Input-offset voltage can be a particularly difficult problem in comparator design. In precision applications, such as high-resolution A/D converters, large input–offset voltages cannot be tolerated. While systematic offset can nearly be eliminated with the proper design, random offsets still remain and are unpredictable. Fortunately, there are techniques in MOS to remove a large portion of the input offset using offset cancellation techniques because of nearly infinite input resistance of MOS transistors. This characteristic allows long-term storage of voltages on transistor's gate. As a result, offset voltages can be measured, stored on capacitors, and summed with the input so as to cancel the offset. Figure 2.6 shows an offset cancellation algorithm. A known polarity is given to the offset voltage for convenience. Figure 2.6(b) shows the comparator connected in unity gain configuration so that the input offset is available at the output.

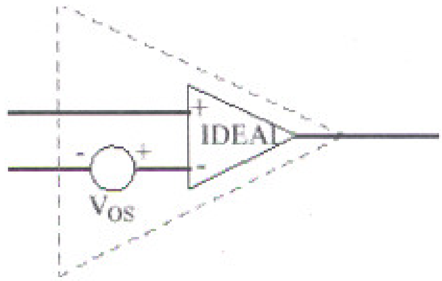


Figure 2.6(a): Simple model of comparator including offset

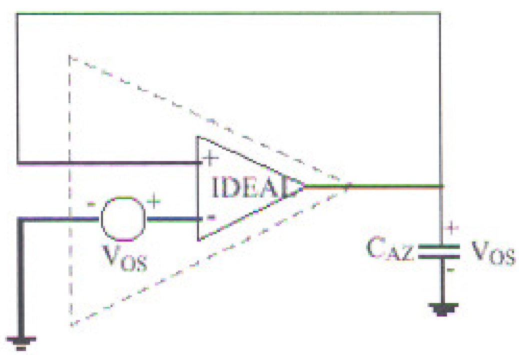


Figure 2.6(b): Comparator in unity gain configuration storing the offset on auto zero capacitor C_{AZ} during the first half of auto zero cycle.

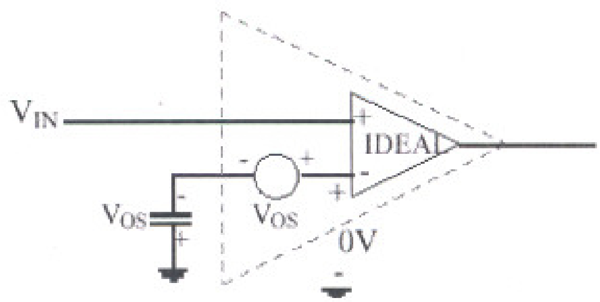


Figure 2.6(c): Comparator in open loop configuration with offset cancellation achieved at the non-inverting input during the second half of the autozero cycle

In order for this circuit to work properly, it is necessary that the comparator be stable in unity gain configuration. This implies that only self compensated high-gain amplifiers would be suitable for autozeroing. In the final operation of the auto zero algorithm C_{AZ} is placed at the input of the comparator in series with V_{OS}. The voltage across C_{AZ} adds to V_{OS}, resulting in zero volts at the noninverting input of the comparator. Since there is no path to discharge the autozero capacitor, the voltage across it remains indefinitely (in ideal case). In reality there are leakage paths in shunt with C_{AZ} that can discharge it over a period of time. The solution to this problem is to repeat the auto zero cycle periodically.

A practical implementation of a differential input, autozeroed comparator is shown in Figure 2.7. The comparator is modeled with an offset voltage source as before. Figure shows that during the first stage of the cycle when Φ_1 is high, the offset is stored across C_{AZ}. In the second phase of the autozero cycle when Φ_2 is high, the offset is cancelled by the addition of V_{OS} on C_{AZ}. It is during this portion of the cycle that the circuit acts as a comparator.

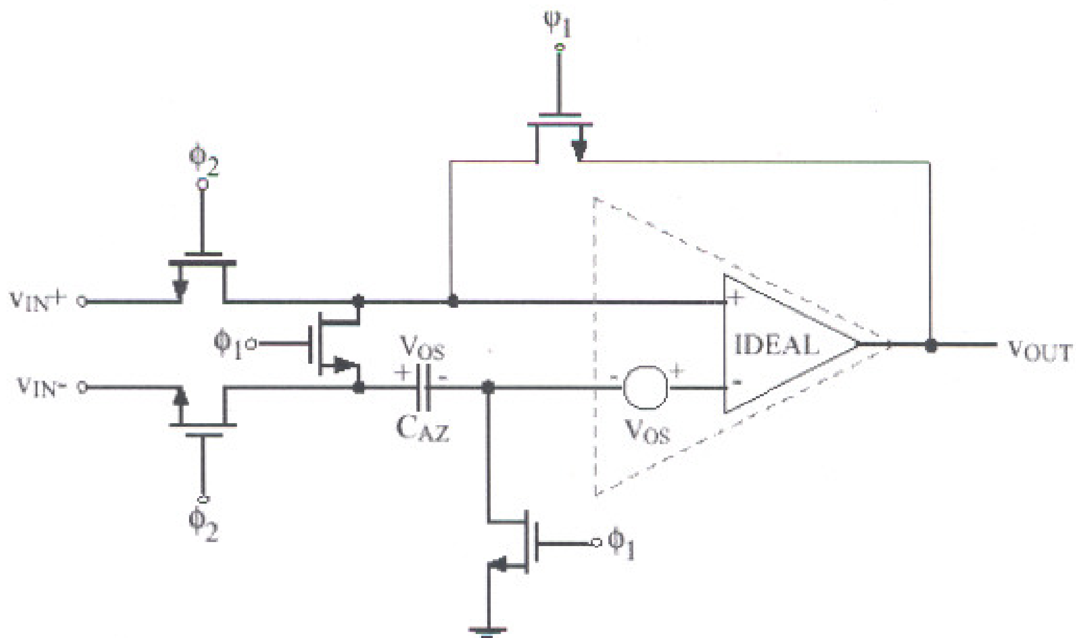


Figure 2.7: Differential circuit implementation of an autozero comparator.

The switch implementations of the autozeroed comparator can be single channel MOSFETs or complementary MOSFETs. It is important to use non-overlapping clocks to drive the switches so that any given switch turns off before another turns on. These techniques are very effective in removing the offset in large amounts but the offset cancellation is not perfect. Charge injection resulting from the clock feed through can by itself introduce an offset. This too can be cancelled, but it is usually the cause of the lower limit of the offset voltage being greater than zero.

2.3.2 COMPARATORS USING HYSTERISIS

Often a comparator is placed in a very noisy environment in which it must detect signal transition at the threshold point. If the comparator is fast enough and the amplitude of the noise is great enough, the output will also be noisy. In this situation, a modification on the transfer characteristic of the comparator is desired. Specifically, hysterisis is needed in comparator.

Hysterisis is the quality of comparator in which the input threshold changes as a function of the input (or output) level. In particular, when the input passes the threshold, the output changes and the input threshold is subsequently reduced so that the input must return beyond the previous threshold before the comparator's output changes the state again. Note that as the input starts negative and goes positive, the output does not change until it reaches the positive trip point, V_{TRP+}. Once the output goes high, the effective trip point is changed. When the input returns in the negative direction, the output does not switch until it reaches the negative trip point, V_{TRP-}.The advantage of the hysterisis in a noisy environment can clearly be seen from Figure.2.8. In this, a noisy signal is shown as the input to a comparator without hysterisis. The intent is to have the comparator output follow the low-frequency signal. Because of the noise variations near the threshold points, the comparator output is too noisy. The response of the comparator can be improved by adding hysterisis equal to or greater than the amount of the largest expected noise amplitude. The response of such a comparator is shown in Figure 2.8(b).

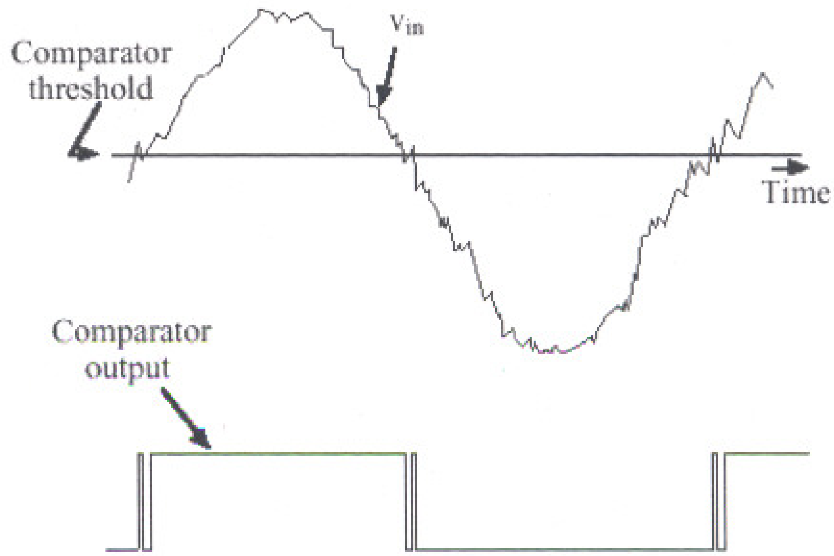


Figure 2.8(a): Comparator response to noisy input

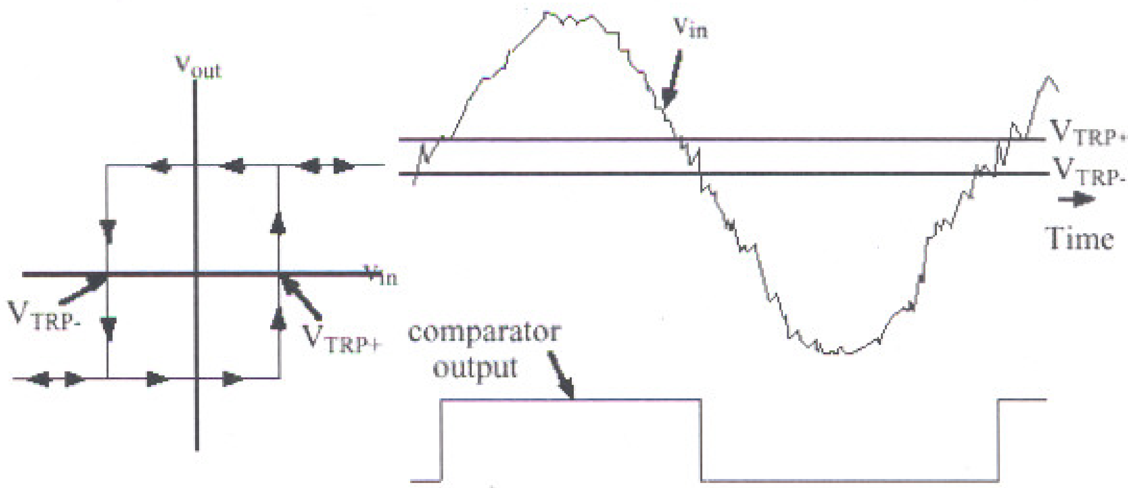


Figure 2.8(b): Comparator response to a noisy input when the hysterisis is added

There are many ways to introduce hysterisis in a comparator. All of them use some form of positive feedback. The methods can be categorized into external and internal methods. External hysterisis uses external positive feedback to implement hysterisis and can be accomplished after the comparator is built. Internal hysterisis is implemented into the comparator and doesn't require external feedback.

EXTERNAL HYSTREISIS

Figure 2.9 shows a noninverting bistable circuit using positive feedback to accomplish the hysterisis. This bistable characteristic is counterclockwise. We assume that the maximum and minimum output voltages of the comparator are V_{OH} and V_{OL}, respectively. The trip points can be found as follows. Let us assume that V_{IN} is much less than V_{OL}. As V_{IN} is increased, the upper point, V_{TRP+}, is found as

$$0 = \left(\frac{R_1}{R_1 + R_2}\right)V_{OL} + \left(\frac{R_2}{R_1 + R_2}\right)V_{TRP}^{+}$$

So we get the upper trip point

$$V_{TRP}^{+} = \frac{R_1}{R_2}V_{OL}$$

V_{OL} is negative so upper trip point is positive.

The lower trip point V_{TRP-} can be found by assuming that V_{IN} is much greater than the voltage at the positive input to the comparator. In this case, the output voltage will be V_{OH}. As V_{IN} is decreased, the lower point, V_{TRP-}, is found as

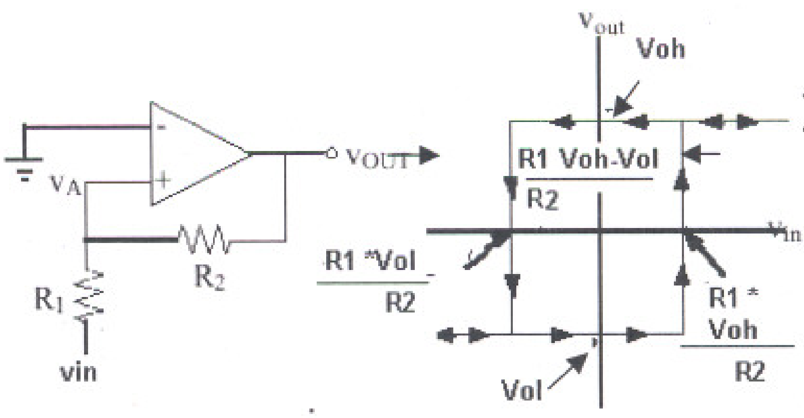


Figure 2.9: Noninverting bistable circuit using external positive feedback

$$0=\left(\frac{R_1}{R_1+R_2}\right)V_{OH}+\left(\frac{R_2}{R_1+R_2}\right)V_{TRP}^-$$

So we get the lower trip point

$$V_{TRP}^- = \frac{R_1}{R_2}V_{OH}$$

The width of the bistable characteristic is given as

$$\Delta V_{IN} = V_{TRP}^+ - V_{TRP}^- = \left(\frac{R_1}{R_2}\right)(V_{OH}-V_{OL})$$

Next Figure 2.10 shows the clock wise stable using external positive feedback. Assuming that the input is much less than the voltage at the positive input of the comparator allows defining the output state at V_{OH}. The upper trip point can be found by setting the input equal to the voltage at the positive input of the comparator. The result is

$$V_{IN} = V_{TRP}^+ = \left(\frac{R_1}{R_1+R_2}\right)V_{OH}$$

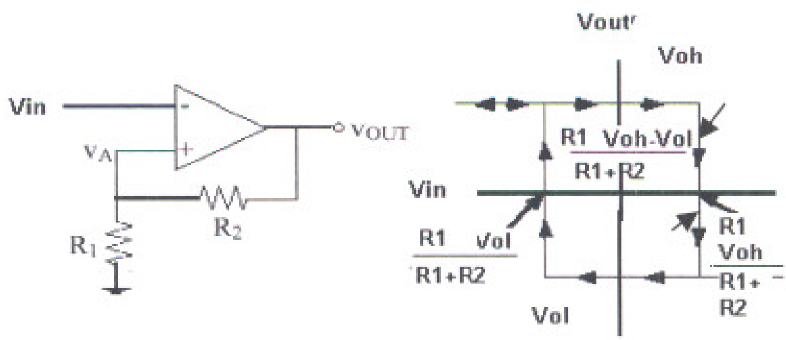


Figure 2.10: Inverting bistable circuit using external positive feedback

Next assuming that the input is much greater than the voltage at the positive input of the comparator allows defining the output state at V_{OL}. The lower trip point can be found by setting the input equal to the voltage at the positive input of the comparator. The result is

$$V_{IN} = V_{TRP}^{-} = \left(\frac{R_1}{R_1 + R_2}\right) V_{OL}$$

INTERNAL HYSTERISIS

The hysterisis can also be accomplished by using internal positive feedback. As we can see from the Figure 2.11 that there are two paths of feedback. The first is current series feedback through the common source node of transistors M1 and M2. This feedback path is negative. The second path is voltage shunt feedback through the gate drain connection of transistors M6 and M7. This path of feedback is positive.

If the positive feedback factor is less than the negative feedback factor, then the overall feedback factor will be negative and no hysterisis will result. If the positive feedback factor becomes greater, the overall feedback factor will be positive which will give rise to hysterisis.

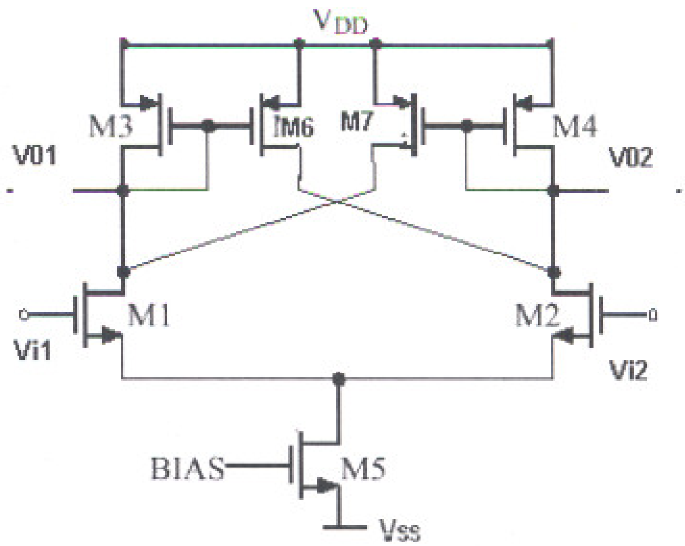


Figure 2.11: Implementation of hysterisis using the internal positive feedback in the input stage of a high gain, open loop comparator

Assume that plus minus supplies are used and that the gate of M1 is tied to ground. With the input of M2 much less than zero, M1 is on and M2 is off, thus turning on M3 and M6 and turning off M4 and M7. All of i_5 flows through M1 and

M3, so v_{02} is high. The resulting circuit is shown in the Figure 2.12. Note that M2 is shown even though it is off. At this point, M6 is attempting to source some amount of current. As v_{IN} increases toward the threshold point some of the tail current begins to flow through M2. This continues until the point where the current through M2 equals the current through M6. Just beyond this point the comparator switches state.

Knowing current in both M1 and M2, it is easy to calculate their respective V_{GS} voltages. Since the gate of M1 is ground, the difference in their gate source voltages will yield positive trip point as

$$V_{TRP+} = v_{GS2} - v_{GS1}$$

Once the threshold is reached, the comparator changes state so that majority of the tail current now flows through M2 and M4. As a result, M7 is turned on, thus turning off M3, M6 and M1. As in the previous case, as the input decreases the circuit reaches a point at which the current where the current in M1 increases until it equals the current in M7. The input voltage at this point is the negative trip point V_{trp-}. The equivalent circuit in this state is shown in Figure 2.13.

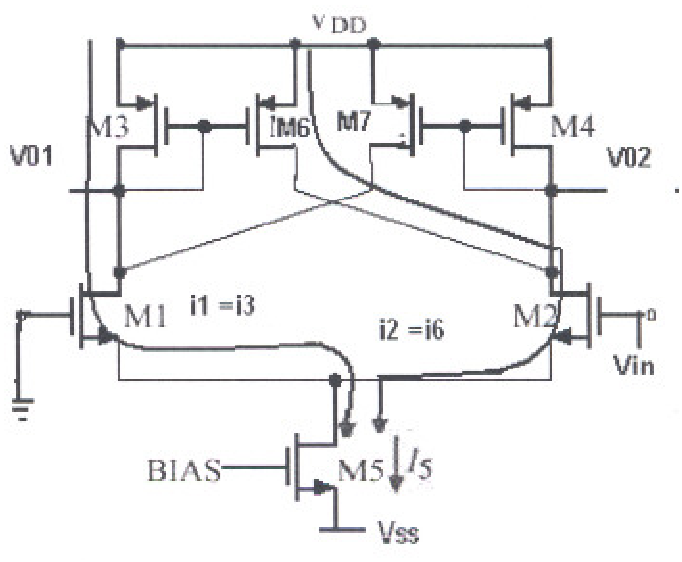


Figure 2.12: Comparator of Figure1.15 whereV_{in} is very negative and increasing toward V_{TRP+}

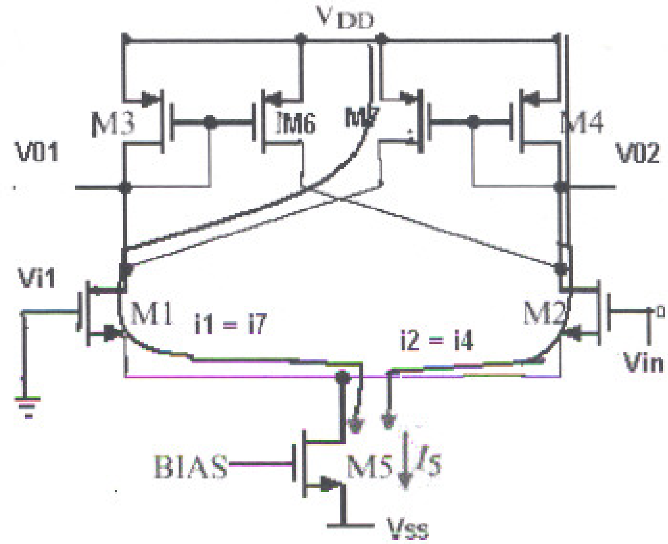


Figure 2.13: Comparator of Figure1.15whereV_{in} is very positive and decreasing toward V_{TRP}.

2.4 DISCRETE TIME COMPARATOR

In many applications the comparator only functions over a portion of a time period. Such circuits are driven by a clock and will have a portion of time or phase when the comparator is functioning as a comparator and a phase when the comparator is not being used. In this circumstance, other forms of comparator can be used that are efficient and have a small propagation delay time. We can see two such comparators in this section. They are switched capacitor comparator and the regenerative comparator.

2.4.1 SWITCHED CAPACITOR COMPARATORS

The switched capacitor comparator [23] uses a combination of switched capacitors and open loop comparators. The advantage of the switched capacitor comparator are that differential signals can be compared using single ended circuits and switched capacitor comparator naturally lends itself to autozeroing the dc offset voltage of the open loop comparator. Figure 2.14 shows typical switched capacitor comparator. The voltage applied to the circuit are normally sampled and held so that capital variables are used. When the Φ_1 switches are closed in Figure 2.14 the comparator C autozeros voltage of the comparator to ground. We recall that the comparator must be stable in unity gain operation for this circuit to work properly. It can be shown that the voltage across C_1 and C_p at the end of the Φ_1 phase period is

$$Vc\ (\Phi_1) = V_1 - Vos$$

$$\text{and} \qquad Vcp\ (\Phi_1) = Vos$$

Now when Φ_2 switches are closed, the equivalent circuit at the beginning at the Φ_2 phase period is shown in Figure 2.14(b). In this circuit, the voltage across each capacitor has been removed and represented by a step voltage source. Solving by the principle of superposition we get

$$V_{out}\ (\Phi_2) = A\ (V_1 - V_2)$$

Therefore, the difference between the voltages V_1 and V_2 is amplified by the gain of the comparator. The gain of the comparator used for the switched capacitor comparator must be large enough to satisfy the resolution requirements. In many cases, the resolution is large, so that a very simple single stage amplifier is sufficient

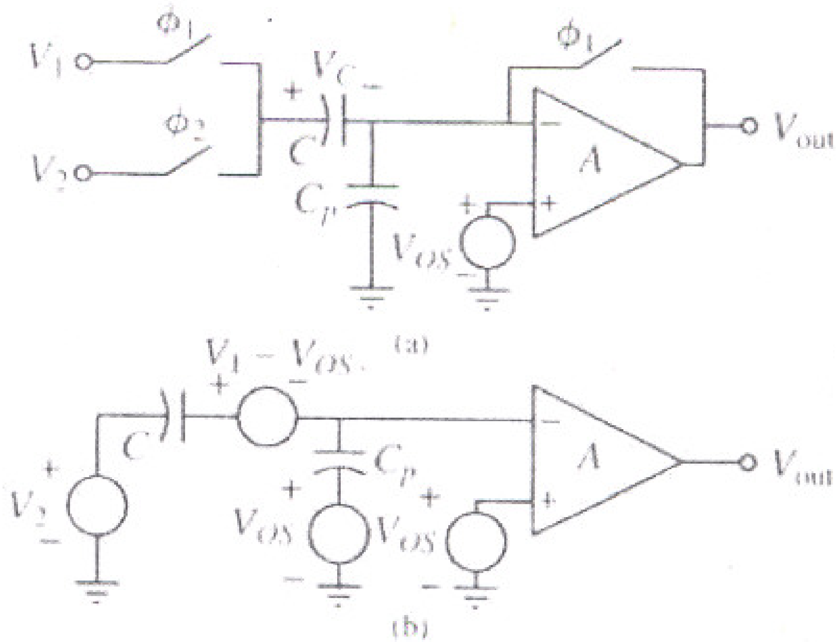


Figure 2.14: A switched capacitor comparator and its equivalent circuit when $\varnothing_2$ switches are closed

for the comparator. The speed of the comparator depends on how long it takes the circuit to settle to its steady stage after the switches have been closed for a given period. During the Φ_1 phase, the response of the circuit in Figure 2.14 is very fast. The time constants of the circuit are associated with the product of the switch on resistance and the capacitor C and the dynamics of the comparator in unity gain configuration. Both of these time constants can be small. During Φ_2, the open loop response of the comparator will determine the speed.

A differential switched capacitor comparator is shown in Figure 2.15. The input is sampled on the two identical capacitors, C, during the Φ_1 phase period. The dc offsets of the differential-in, differential-out comparator are also autozeroed during this period. During the Φ_2 phase period, the voltages sampled across the capacitor are applied to the comparator input. As the Φ_1 switches open at the end of the Φ_1 phase period, the charge injection will be reduced because the signal is a differential voltage and the charge injection is a common- mode voltage.

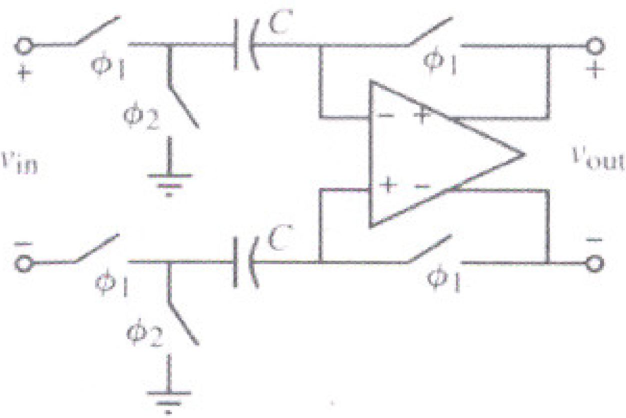


Figure 2.15: Differential switched capacitor comparator

2.4.2 REGENERATIVE COMPARATORS

Regenerative comparators [10,18,21] use positive feedback to accomplish the comparison of two signals. The regenerative comparator is also called a *latch*. The simplest form of a latch is shown in Figure 2.16.And consists of two cross-coupled MOSFETs.The current sources and sinks are used to identify the dc currents in the transistor. Normally, the latch has two modes of operation. The first mode disables the positive feedback and applies the input signal to the terminals designated as V_{01} and V_{02}.

The initial voltages applied during this mode will be designated as $V_{01'}$ and $V_{02'}$. The second mode enables the latch and depending on the relative values of $V_{01'}$ and $V_{02'}$, one of the outputs will go high and the other will go low. A two-phase clock is used to determine the modes of operation. It is

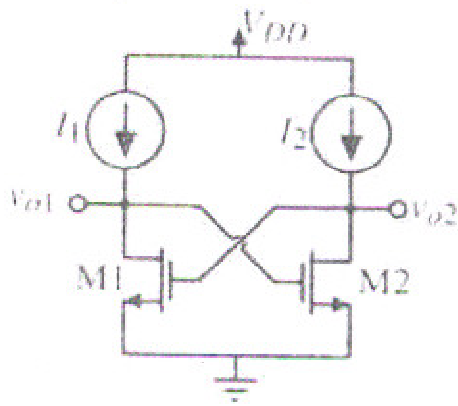


Figure2.16: NMOS latch

important to characterize the time it takes for the latch to go from its initial state to the final state during the enabled mode of operation.

A practical latch comparator is as shown in Figure 2.17. M7 and M8 are the latch transistors and are PMOS in this case. M9 and M10 are used to reset the latch by setting the source-drain voltages of M7 and M8 to zero. The input to latch is applied to the gates of M1A and M1b. The transistors M1A, M2A, M1B and M2B are operating in triode region. The values of the inputs will cause the resistance seen by the sources of M3 and M4 to ground to vary. When the latch is enabled the drains of M3 and M4 are connected to the latch outputs. M3 and M4 form a parallel positive feedback path for latch. For example, the signal at the gate of M7 can go through M7 or can go through M3 (M5 is a closed switch). The gain of the M3 and M4 feedback paths depends on the values of resistor, R_1 or R_2 respectively. If the resistor is small the gain is large and that side of the latch will go high.

When the reset/latch goes high, the latch goes into the regenerative mode. The drain currents of M5 and M6 are steered to obtain a final state determined by the mismatch between the R_1 and R_2 resistances. A simpler form of the regenerative comparator [11,18,25] is shown in Figure 2.18.Assume that the strobe signal is low. The section M5-M6-M7 of the circuit doesn't operate

.

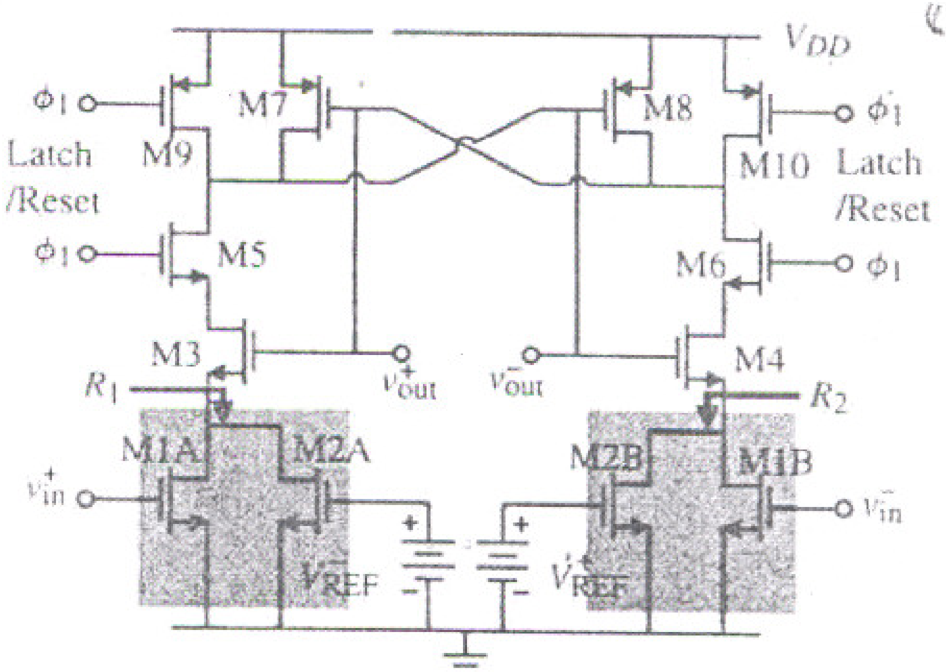


Figure 2.17:Comparator using a latch with built in threshold

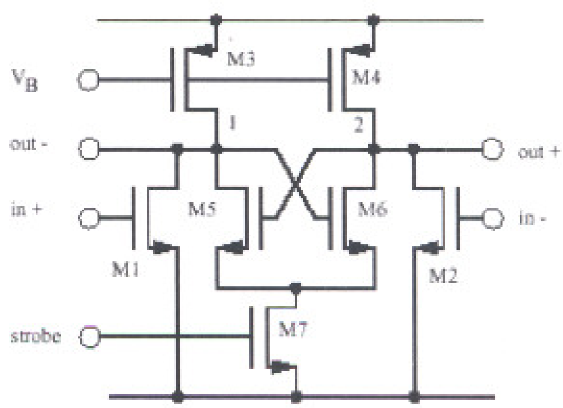


Figure 2.18: Simple low-power latch comparator

and the transistor pairs M1-M3 and M2-M4 form two inverters with active load. The voltage of node 1 and 2 are close to V_{DD} if the input voltages induce currents in M1 and M2 lower than the one drained by M3 and M4. When the common mode input exceeds a given level the currents in M1 and M2 become large and the voltage of node 1 and 2 drop down to ground.

Lets assume that the common mode input is below the above-mentioned level and that the two inputs differ by a given extent. When the strobe control goes up the transistors M5 and M6 become active and they start the regeneration operation. Since the voltages of node 1 and 2 are pretty high the action of M5 and M6 will be significant. However, one of the voltages is more effective than the other and become more and more dominant with respect to another.

If the input voltages are such that the node 1 and 2 are at a low level, at the limit, below the threshold of M5 and M6, when the strobe control is active the cross coupled pair M5 and M6 doesn't react properly or, at the limit remain in

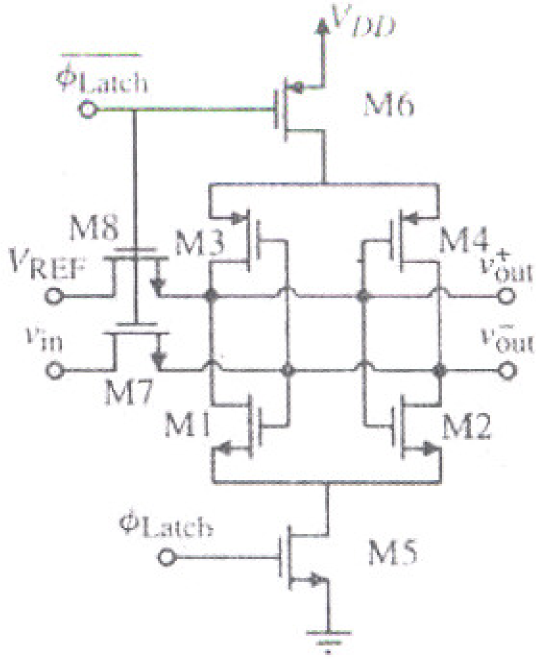


Figure 2.19: Dynamic latch

sub-threshold region of operation. Therefore the given circuit works properly for a given range of common mode input.

A latch using opposite type transistors can replace the current sinks and sources of Figure 2.16 resulting in dynamic latch [22] as shown in Figure 2.19. Here a reference voltage V_{REF}, is compared with an input voltage, V_{IN} during the time when Φ_{Latch} is high. This form of the latch has the advantage of lower power dissipation because no current is flowing when the latch is in reset mode (Φ_{Latch} is low). The input voltage offset of the latch is important because it will limit the resolution of the comparator.

2.5 HIGH SPEED COMPARATORS

A high-speed comparator [5,20] should have a propagation delay time as small as possible. In order to achieve this goal, we will have to separate the comparator in number of cascaded stages. If the input is slightly larger than $V_{IN\ (min)}$, then the function of the stages is to amplify the input with as little delay per stage as possible. We know the signal swings in initial stages will be small. As the signal swing begins to approach the desired range, the amplifiers will be limited by their slew rate. Thus, for the initial stages, the important parameter is to have a high bandwidth so that there is a little delay in amplifying the signal and passing it on to the next stage. However, at the end of the cascade of amplifiers, it is more important to have high slew rate capability so that the voltage across the inter stage capacitors and the load capacitor rises or falls quick enough. Therefore, the stages at the beginning should be designed differently than the stages at the end of amplifier chain.

The basic principle behind the high-speed comparator is to use a preamplifier to build up the input change to a sufficiently large value and then apply it to the latch. This combines the best aspects of circuits with negative exponential response (the preamplifier) with circuits with positive exponential response

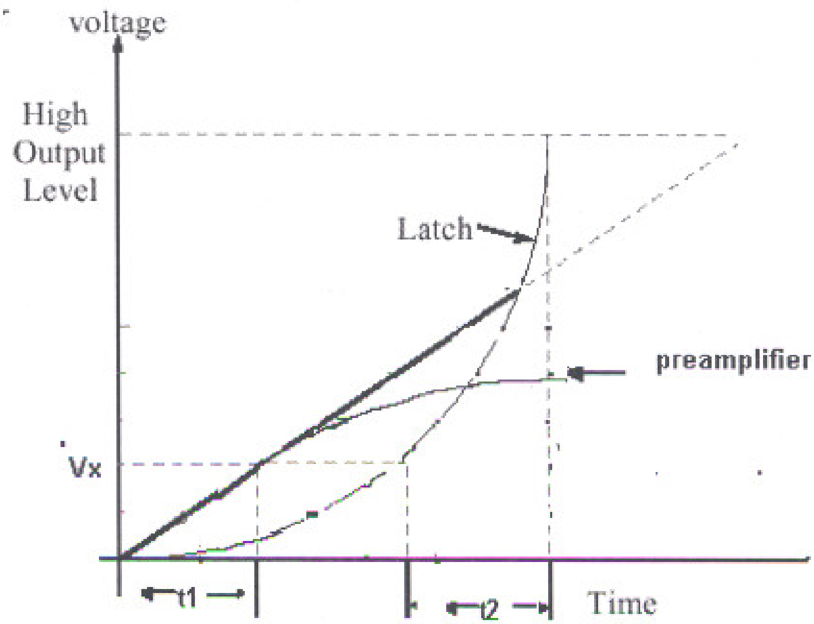


Figure 2.20: Preamplifier and latch step response

(the latch). This is illustrated in the Figure 2.20. In this figure, the gain of the preamplifier times the input voltage is not sufficient to reach the desired output level. Rather, during time t_1 the preamplifier amplifies the input voltage to a value of V_x. The voltage V_x is applied to the latch input, which then goes to desire output voltage in time t_2. Thus, the total response time is t_1+t_2. If the comparator consisted only of the preamplifier, the gain would have to be larger and the delay to make the transition from V_{OL} to V_{OH} would be longer than t_1+t_2. On the other hand, the latch would require more time than t_1+t_2 if the input was small. So we can see that the larger the input to latch the shorter the time for the output to reach its maximum value.

The design of the preamplifier must be done in such a manner that the desired latch input voltage, V_x, is achieved in minimum time. Since the preamplifier is working in linear region, this means that the bandwidth must be as large as possible. We know that the gain bandwidth of an amplifier is normally constant. Therefore, a single amplifier has a limited capability. If a number of low gain, wide bandwidth amplifiers are cascaded, the delay time t_1, can be minimized.

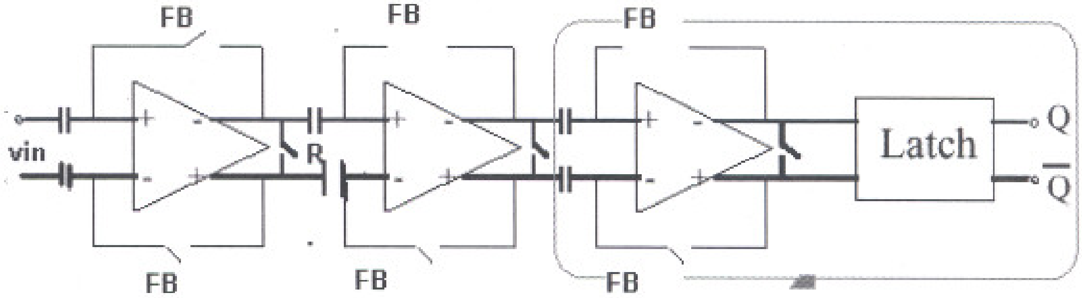


Figure 2.21: Fully differential, three stage comparator and latch

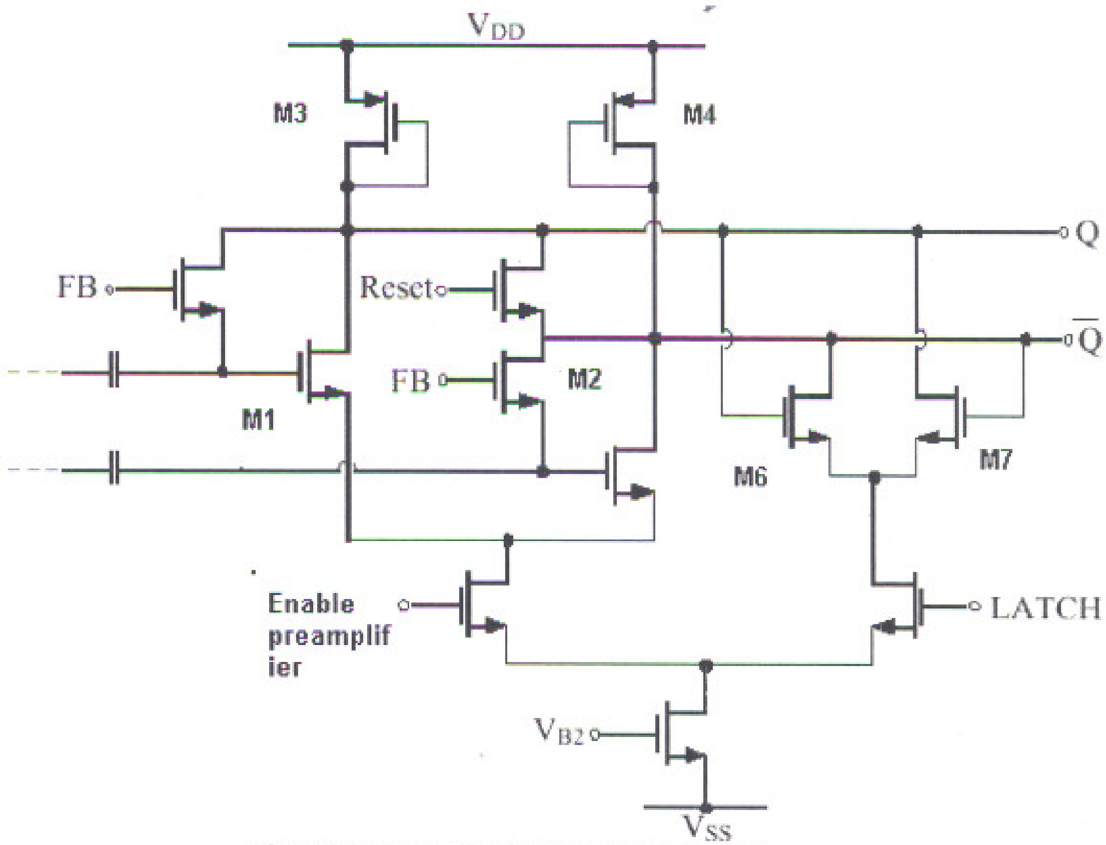


Figure 2.22: Example of a preamplifier and latch

A high-speed comparator using three cascaded low gain amplifiers as the preamplifier and a latch at the output as shown in Figure 2.21. When the FB and reset switches are closed, the capacitors designated as Cv are auto zeroed for each amplifier. Unfortunately, each amplifier must be autozeroed by itself. More switches would be required to autozero all three amplifiers at the same time. The input is applied through the capacitors C1 and C2. The low gain amplifiers must compromise between a high bandwidth and sufficient gain. A simple preamplifier is shown in Figure 2.22. The connection with latch is shown.

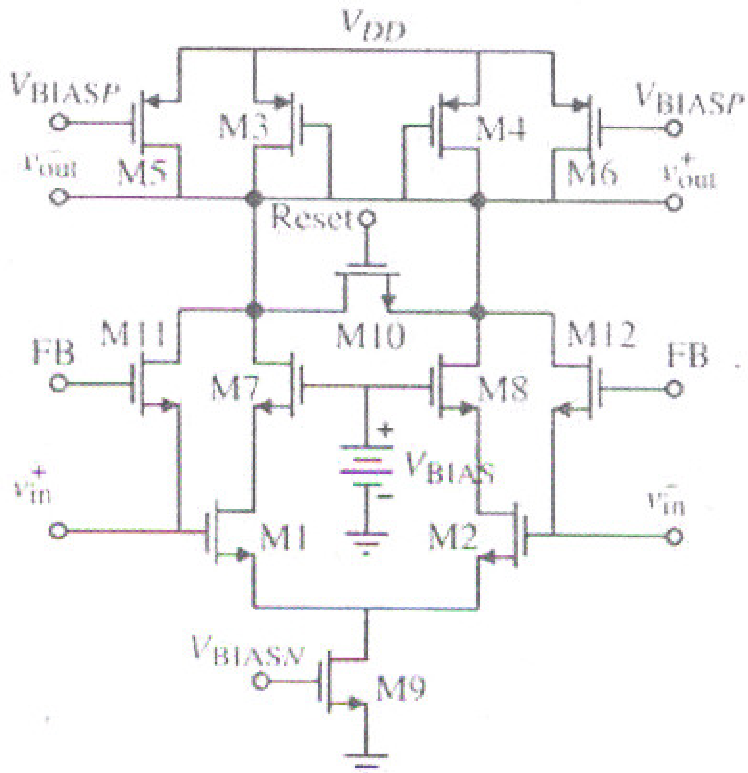


Figure 2.23: An improved preamplifier

There are several problems with the preamplifier. One is that gain is very small even for large differences of W/L values. Another is that there is no isolation between the latch outputs and inputs to the preamplifier. Rapid changes in the output of the latch can propagate through the drain gate capacitances of M1 and M2 and appear at the inputs of the latch. Figure 2.23 shows a preamplifier that solves these two problems.

Transistors M5 and M6 are used to increase the currents in M1 and M2 so that the gain is enhanced by the square root of the difference of currents in M3 and M4. Transistors M7 and M8 isolate the input from rapid changes in the latch output. The use of a preamplifier before the latch also has the advantage of reducing the input offset voltage of the latch by the gain of the preamplifier. The input offset voltage of the comparator will now becomes that of the preamplifier, which can be auto zeroed, in small values of input-offset voltage resulting.

When a comparator must drive a significant amount of output capacitance in very short times, the latch is generally not sufficient. In this it is better to follow the latch by circuits that can quickly generate large amounts of current. The first stage is a low gain, high bandwidth preamplifier that drives a latch. The latch outputs are used to drive a self-biased differential amplifier. The output of the self-biased differential amplifier drives a push-pull output driver.

TWO STAGE OPEN LOOP COMPARATOR

As we can see from the requirements for a comparator reveal that it requires a differential input and sufficient gain to be able to achieve the desired resolution. The best implementation is the two-stage opamp [18,20]. A simplification occurs because the comparator will generally be used in open loop mode and it's not necessary to compensate that. It is preferred so that it has largest bandwidth possible, which will give a faster response.

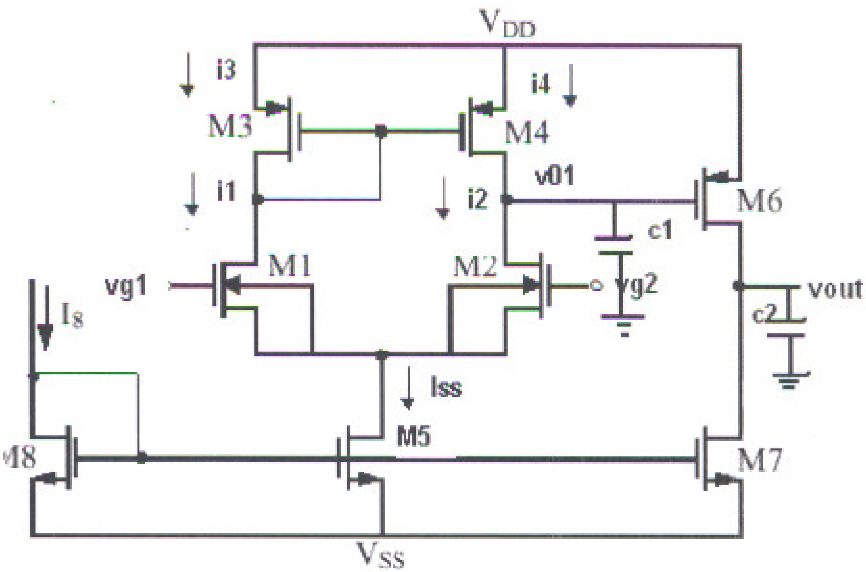


Figure 3.1: Two-stage open loop comparator used to find initial stages

3.1 BUILDING BLOCKS OF TWO STAGE OPEN LOOP COMPARATOR

3.1.1 DIFFERENTIAL STAGE

A differential pair is widely used as the input stage of the op-amplifier. It is made of two transistors with their source in common, fed by current source. The transistors may either be n-channel (as shown in Figure 3.2) or p-channel, and they are matched to each other. If the two transistors are in saturation region, we can write

$$I_1 = \frac{\mu C_{ox}}{2}\left(\frac{W}{L}\right)_1 (V_{GS1} - V_{Th})^2$$

$$I_2 = \frac{\mu C_{ox}}{2}\left(\frac{W}{L}\right)_2 (V_{GS1} - V_{Th})^2$$

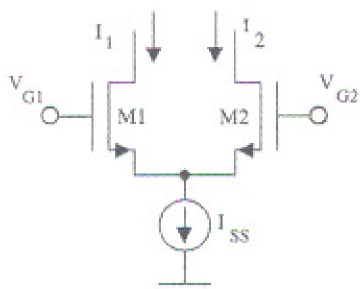


Figure 3.2 N- channel Differential pair

where $(W/L)_1$ and $(W/L)_2$ are nominally equal, the transistors being matched. Moreover, in the above equations the output conductance has been neglected. The input signals can be expressed as

$$V_{GS1} = V_{GS0} + V_{in}/2$$

$$V_{GS1} = V_{GS0} - V_{in}/2$$

Where V_{GS0} is the common mode component and V_{in} is a differential signal. Since the bias current can be expressed as

$$I_{SS} = I_1 + I_2 = \mu C_{OX}\left(\frac{W}{L}\right)_1 (V_{GS1} - V_{Th})^2$$

Therefore, in the differential stage, like in the case of the inverter with active load, the transconductance gain increases with the square root of the bias current.

3.1.2 CURRENT MIRROR

It is composed of two transistors, of which one M1 is diode connected.

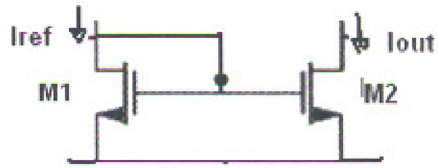


Figure 3.3: Simple current mirror

M1 receives the reference current I_{ref} and measures it by developing at its gate voltage V_{GS1}; this voltage biases the gate of M2. We assumes that both transistors operate in saturation region; therefore the currents are

$$I_{ref} = \frac{\mu C_{ox}}{2}\left(\frac{W}{L}\right)_1 (V_{GS1} - V_{Th})^2$$

$$I_{out} = \frac{\mu C_{ox}}{2}\left(\frac{W}{L}\right)_2 (V_{GS1} - V_{Th})^2$$

3.1.3 CMOS INVERTER WITH ACTIVE LOAD

The simplest form of inverter is the inverter with active load.

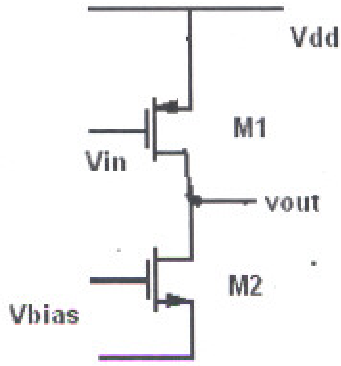


Figure 3.4: Inverter with p-channel input transistor

Here input is applied to only one transistor while the gate of complementary element is biased with a fixed voltage and operates as an active load. The biasing voltage is obtained by a transistor connected in so-called diode configuration and carrying a given current I_{Bias}.

3.2 DESIGN PROCEDURE

3.2.1 SPECIFICATIONS

- Open loop gain (A_v)
- Minimum input common mode range (V_{icm-})
- Maximum input common mode range (V_{icm+})
- Load capacitance (C_L)
- Output voltage swing (V_{OH} and V_{OL})
- Slew rate (SR)

3.2.2 DESIGN STEPS

STEP 1: Determine the value of the current in the output stage for the largest of two values

$$I_7 = I_6 = C_L\left(\frac{dV_{out}}{dt}\right) = C_L * SR$$

STEP 2: Design the transistors M6 and M7 by using the current calculated above and assuming the transistors in saturation. The equation used is

$$\frac{W_6}{L_6} = \frac{2 * I_6}{K_P * (V_{SD6}(sat))^2}$$
$$\frac{W_7}{L_7} = \frac{2 * I_7}{K_N * (V_{SD7}(sat))^2}$$

where $V_{SD6}(sat) = V_{DD} - V_{OH}$

$V_{SD7}\ (sat) = V_{OL} - V_{SS}$

STEP 3: Now we have to guess a value of C_I and will check later. This value must lie between 0.1 pf and 0.5 pf. Using this value of output capacitance of the first stage and the slew rate we can find the tail current or bias current.

$$I_5 = C_I\left(\frac{dV_{o1}}{dt}\right) = C_I * SR$$

Now calculate the value of gate to source voltage of the current mirror transistors using the specification of maximum input common mode voltage. Here we use the relation

$$V_{SG3} = V_{DD} - V_{icm+} + V_{TN}$$

STEP 4: Using the gate to source voltage calculated above we can design the transistors M3 and M4.

$$\frac{W_3}{L_3} = \frac{W_4}{L_4} = \frac{I_5}{K_P * (V_{SG3} - |V_{TP}|)^2}$$

STEP 5: Next step is to calculate the transconductance g_{m1} of transistor M1 using the gain relation of the two stages.

$$g_{m1} = \frac{A_v(0)*(g_{ds2} + g_{ds4})(g_{ds6} + g_{ds7})}{g_{m6}}$$

where

$$g_{m6} = \sqrt{\frac{2*K_P*W_6*I_6}{L_6}}$$

and $g_{dsi} = \lambda_P * I_{Di}$ (For p-type transistor)

$g_{dsi} = \lambda_N * I_{Di}$ (For n-type transistor)

STEP 6: Using the above-calculated value of transconductance of differential transistors, we can design M1 and M2 i.e. the differential pair transistors.

$$\frac{W_1}{L_1} = \frac{W_2}{L_2} = \frac{g_{m1}^2}{K_N * I_5}$$

STEP 7: Now we have to check for the output capacitance of the first stage that we have assumed. This is given by

$$C_I = C_{gd2} + C_{gd4} + C_{gs6} + C_{bd2} + C_{bd4}$$

Where

$$C_{bdx} = CJ* AD_x + CJSW* PD_x$$

$$C_{gsx} = CGSO * W_x + 0.67* C_{ox}* W_x *L_x$$

$$C_{gdx} = CGDO * W_x$$

STEP 8: If C_I is greater than that we have assumed, then we have to increase the assumed value and recalculate the current I_5 then current mirror transistors and differential pair transistors.

STEP 9: Next step is to calculate V_{DS5} (sat) using the specification of minimum input common mode voltage. The relation is given by

$$V_{DS5} = V_{icm-} - V_{GS1} - V_{SS}$$

Where
$$V_{GS1} = \sqrt{\frac{I_5 * L_1}{K_N * W_1}} + V_{TN}$$

Using the above-calculated value of V_{DS5} we can design the transistor M5.

$$\frac{W_5}{L_5} = \frac{2 * I_5}{K_N * (V_{DS5}(sat))^2}$$

If the value of V_{DS5} comes out to be less than 100mV, increase the value of W_1/L_1.

3.3 AN EXAMPLE

3.3.1 SPECIFICATIONS

- DC gain A_v (0) = 10,000 V/V
- Slew Rate (SR) = 100 V/µ
- Load Capacitance (C_L) = 5pF
- V_{icm+} = 4 V
- V_{icm-} = 1.25 V
- V_{OH} = 4.5 V
- V_{OL} = 0.5 V

3.3.2 DESIGN STEPS

STEP 1: Estimate the value of bias current in the output stage using SR.

$$I_7 = I_6 = C_L * SR = 5 * 10^{-12} * 100 * 10^6$$
$$I_7 = I_6 = 500 \mu A$$

we take the value of current 550μA, for some margin.

STEP 2: Using the value of I_6 and I_7 calculated above, we can design the output stage transistors.

$$\frac{W_6}{L_6} = \frac{2*550*10^{-6}}{2.64*10^{-5}*(0.5)^2}$$
$$\frac{W_6}{L_6} = 166.6 \cong 167$$
$$\frac{W_7}{L_7} = \frac{2*550*10^{-6}}{6.326*10^{-5}*(0.5)^2}$$
$$\frac{W_7}{L_7} = 70$$
$$K_P = 2.64*10^{-5}, K_N = 6.326*10^{-5}$$
$$V_{SD6}(sat) = 5 - 4.5 = 0.5V$$
$$V_{SD7}(sat) = 0.5 - 0 = 0.5V$$

STEP 3: Now we assume the value of output capacitance of first output stage. Let it be 0.2pF. We will check it later. So bias current of the first stage is

$$I_5 = C_I * SR = 0.2*10^{-12}*100*10^6$$
$$I_5 = 20\mu A$$

Again we take this value as 50μA for safe margin.

STEP 4: Using the bias current calculated above; design the transistor pair of current mirror circuit.

$$\frac{W_3}{L_3} = \frac{W_4}{L_4} = \frac{50*10^{-6}}{2.64*10^{-5}*(1.1-|-0.63|)^2}$$
$$\frac{W_3}{L_3} = \frac{W_4}{L_4} = 8.6 \cong 9$$

$$K_P = 2.64*10^{-5} A/V^2$$
$$V_{SG3} = 5-4.5+0.6 = 1.1V$$
$$V_{TP} = -0.63V$$

STEP 5: Design of the differential pair requires the transconductance, which can be calculated using the open loop gain specification of both stages. Therefore,

$$g_{m1} = \frac{10{,}000*(0.01+0.02)*(0.01+0.02)*550*10^{-6}*25*10^{-6}}{2202.2*10^{-6}}$$
$$g_{m1} = 56.2*10^{-6} S$$

$$g_{ds4} = \lambda_P * I_4 = 0.02*25*10^{-6},\ g_{ds2} = \lambda_N * I_2 = 0.01*25*10^{-6}$$
$$I_2 = I_4 = \frac{I_5}{2} = 25*10^{-6} A$$

$$g_{ds6} = \lambda_P * I_6 = 0.02*550*10^{-6},\ g_{ds7} = \lambda_N * I_7 = 0.01*550*10^{-6}$$
$$I_7 = I_6 = 550\mu A$$

where $$g_{m6} = \sqrt{\frac{2*K_P*W_6*I_6}{L_6}}$$

$$g_{m6} = \sqrt{2*2.64*10^{-5}*167*550*10^{-6}}$$
$$g_{m6} = 2202.2*10^{-6} S$$

STEP 6: Using the transconductance calculated above, differential pair ratios are given by

$$\frac{W_1}{L_1} = \frac{W_2}{L_2} = \frac{g_{m1}^{\ 2}}{K_N * I_5} = \frac{\left(56.2*10^{-6}\right)^2}{6.326*10^{-5}*50*10^{-6}}$$

$$\frac{W_1}{L_1} = \frac{W_2}{L_2} = 1$$

STEP 7: Assumed value of the output capacitance of first stage is to be checked. This can be done as follows:

$$AD_2 = W_2(L_1 + L_2 + L_3), \qquad PD_2 = 2*(W_2 + L_1 + L_2 + L_3)$$
$$AD_4 = W_4(L_1 + L_2 + L_3), \qquad PD_4 = 2*(W_4 + L_1 + L_2 + L_3)$$

$$AD_2 = 5*10^{-6}*(1+1+1)*10^{-6} = 15*10^{-12}\,m^2$$
$$PD_2 = 2*(5+1+1+1)*10^{-6} = 16*10^{-6}\,m$$
$$AD_4 = 9*10^{-6}*(1+1+1)*10^{-6} = 27*10^{-12}\,m^2$$
$$PD_4 = 2*(9+1+1+1)*10^{-6} = 24*10^{-6}\,m$$

$$C_{bd2} = 3.27*10^{-4}*15*10^{-12} + 1.74*10^{-10}*16*10^{-6}$$
$$C_{bd2} = 7.6\,fF$$

$$C_{bd4} = 4.75*10^{-4}*27*10^{-12} + 2.23*10^{-10}*24*10^{-6}$$
$$C_{bd4} = 18.1\,fF$$

$$C_{gd2} = 2.89*10^{-10}*5*10^{-6} = 1.45\,fF$$
$$C_{gd4} = 3.35*10^{-10}*9*10^{-6} = 3\,fF$$

$$C_{gs6} = 3.35*10^{-10}*167*10^{-6} + 0.67*0.156*10^{-4}*167*10^{-6}*10^{-6}$$
$$C_{gs6} = 57.6\,fF$$

where for p-type transistor

$$Cj = 4.75*10^{-4}\,F/m^2, \qquad Cjsw = 2.23*10^{-10}\,F/m$$

and for n-type transistor

$$Cj = 3.27*10^{-4}\,F/m^2, \qquad Cjsw = 1.74*10^{-10}\,F/m$$

and also

$$C_{OX} = \frac{\xi_{OX}}{T_{OX}} = \frac{3.97*8.85*10^{-14}}{225*10^{-10}} = 0.156*10^{-4}\,F/m$$

So

$$C_I = C_{bd2} + C_{bd4} + C_{gd2} + C_{gd4} + C_{gs6}$$
$$C_I = 7.6 + 18.1 + 1.45 + 3 + 57.6$$
$$C_I = 87.75 fF$$

As this value is smaller than that assumed, so we don't need to change the assumed value.

STEP 8: Now the only transistor left for designing is M5. Firstly, we have to calculate the drain to source voltage of M5.

$$V_{DS5}(sat) = V_{icm-} - V_{GS1} - V_{SS}$$
$$V_{DS5}(sat) = 1.25 - 1.0 = 0.25V$$

$$V_{GS1} = \sqrt{\frac{50*10^{-6}}{6.326*10^{-5}*5}} + 0.6 = 1.0V$$

M1 ratio has been increased to 5, because earlier value gave V_{DS5} less than 100mV.

So now,

$$\frac{W_5}{L_5} = \frac{2*50*10^{-6}}{6.326*10^{-5}*(0.25)^2}$$
$$\frac{W_5}{L_5} = 26$$

All channel lengths are 1µm. So, the W/L values are summarized below

MOS	M1	M2	M3	M4	M5	M6	M7
W/L	5	5	9	9	26	167	70

Table 1

DESIGN OF CLOCKED -COMPARATOR USING BASIC LATCH

4.1 INTRODUCTION

A high-speed comparator should have a propagation delay time as small as possible. The basic principle behind the high-speed comparator is to use a preamplifier to build up the input change to a sufficiently large value and then apply it to latch. This combines the best aspect of circuits with a negative exponential response (the preamplifier) with circuits with a positive exponential response (the latch).

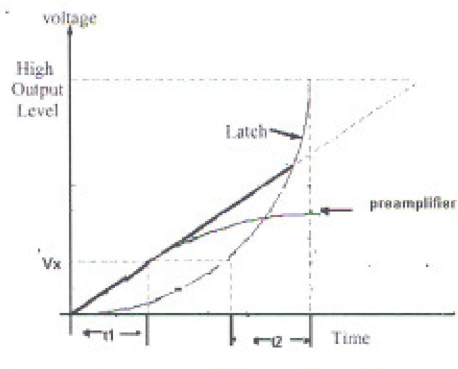


Figure. 4.1: Preamplifier and Latch Step Response

This is illustrated in Figure 4.1 [20,21], where the gain of the preamplifier times the input voltage is not sufficient to reach the desired output level. Rather during time t_1 the preamplifier amplifies the input voltage to a value V_X. The voltage V_X is then applied to latch input, which then goes to the desired output voltage in time t_2. Thus total response time is $t_1 + t_2$. If comparator consisted only of the preamplifier, the gain would have to be larger and the delay to make the transition from V_{OL} to V_{OH} would be longer. So larger the input to latch the shorter the time for the output to reach its maximum value.

4.2 COMPARATOR CIRCUIT

The proposed comparator circuit is depicted in Figure 4.2 [2]. It consists of a differential input pair (M1 and M2), a CMOS latch circuit and output buffers. The CMOS latch composed of an n-channel flip-flop (M12 and M13) with a pair of n-channel transfer gates (M8 and M9) for strobing, and a p-channel flip-flop (M6 and M7) with a pair of p-channel precharge transistors (M10 and M11).

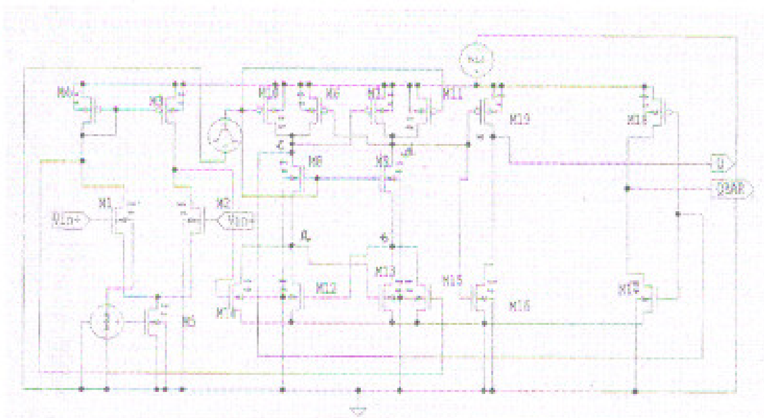


Figure 4.2 Schematic of clocked Comparator

The dynamic operation of this circuit can be divided into two parts. First, when latch is low, the p-channels M6 and M7 are isolated from n-channels, M12 and M13. After the input voltage settles on its decision, a voltage proportional to the input voltage difference is established between nodes *a* and *b* in the end of this period. This voltage difference will act as the initial imbalance for the following regeneration time interval. In the meantime, the p-channel (M6 and M7) is reset by the two-closed precharge transistors, which charge the nodes *c* and *d* to the positive power supply voltage. The closing of latch initializes the regeneration. So the transistors M8 and M9 are also closed. The n-channel flip-flop and p-channel flip-flop, regenerates the voltage difference between the nodes *a* and *b* and between the nodes *c* and *d*. the voltage difference between node *c* and *d* is soon amplified to a voltage nearly equal to power supply voltages. The proposed comparator can charge or discharge the output load with a much better slew rate as compared to Klinke [15]. The power consumption of the comparator is only 0.3 mW at 0.11 GHz clock rate, which is very low as compared to [16,17,26].

4.3 DESIGN PROCEDURE

4.3.1 SPECIFICATIONS

- DC gain (A_V)
- Input common mode range [V_{in} (min) and V_{in} (max)]
- Load capacitance (C_L)
- Total delay (ns)
- Output voltage swing
  [V_{out} (max) and V_{out} (min)]

4.3.2 DESIGN STEPS

STEP 1: First of all the total delay should be divided into three stages. Then taking that delay and output capacitance for each stage we can calculate the current. Let us see each stage's calculation. Considering the output stage as first stage the current flowing can be calculated using load capacitance, delay and output voltage swing specifications. Note that designing the output buffers is just equivalent to the design of digital inverter. So

$$I_{16} = I_{17} = C_L * \left(\frac{dv * 2}{dt}\right)$$

where dv is output voltage difference and dt is the total delay corresponding to this stage. As we have two output buffers the time is halved for the two. From the specification of output voltage swing, we can see that the minimum voltage that make the transistors M_{16} and M_{17} to remain in saturation is equal to the difference of the V_{DD} and V_{out} (max), similarly for M_{18} and M_{19} this voltage is V_{SS} and V_{out} (min). These voltages give us the drain to source voltage of both the transistors pairs. So taking this drain to source voltage and the bias current together we get

$$\left(\frac{W}{L}\right)_{16} = \frac{2 * I_{16}}{K_N * (V_{DS})^2}$$
$$\left(\frac{W}{L}\right)_{17} = \frac{2 * I_{17}}{K_N * (V_{DS})^2}$$

The corresponding p-channel transistor W/L's can be calculated using mobility ratio of p and n-channel transistors.

STEP 2: Calculate the output capacitance of second stage by taking into consider the capacitances of the transistor of first stage it has to drive. This will help in getting current that is required in second stage.

$$C_{out2} = C_{gd19} + C_{gd16}$$
$$C_{out2} = C_{GDO_P} * W_{19} + C_{GDO_N} * W_{16}$$

Looking at the circuit the second stage is a Nand gate pair. So total delay of this stage can be divided in two equal parts as in first step. We will design this stage using the equivalent of nand to inverter.

$$I_1 = I_2 = C_{out2} * \left(\frac{dv * 2}{dt}\right)$$

$$\left(\frac{W}{L}\right)_{equ} = \frac{2 * I_1}{K_N * (V_{DS})^2}$$

$$\left(\frac{W}{L}\right)_{8,9,12,13,14,15} = 2 * \left(\frac{W}{L}\right)_{equ}$$

where $(W/L)_{equ}$ is the ratio for equivalent of nand . C_{out2} is the output capacitance of second stage and V_{ds} is to be calculated in same fashion as in the previous step. The corresponding p-channel transistor W/L's can be calculated using mobility ratio of p and n-channel transistors.

STEP 3: Similarly, calculate the output capacitance of third stage by taking into consider the capacitances of the transistor of second stage it has to drive. This will help in getting bias current.

$$C_{out3} = C_{GSO} * W_{14} + 0.67 * C_{OX} * W_{eff} * L_{eff}$$

$$I_{BIAS} = 2 * C_{out3} * \left(\frac{dv}{dt}\right)$$

Next step is to calculate the transconductance g_{m1} of transistor M1 using the gain relation of the two stages.

$$g_{m1} = A_v(0) * (g_{ds2} + g_{ds4})$$

where $g_{dsi} = \lambda_P * I_{Di}$ (For p-type transistor)

$g_{dsi} = \lambda_N * I_{Di}$ (For n-type transistor)

Using the above-calculated value of transconductance of differential transistors, we can design M1 and M2 i.e the differential pair transistors.

$$\frac{W_1}{L_1} = \frac{W_2}{L_2} = \frac{g_{m1}^{\ 2}}{K_N * I_{BIAS}}$$

STEP 4: Now calculate the value of gate to source voltage of the current mirror transistors using the specification of maximum input common mode voltage. Here we use the relation

$$V_{SG3} = V_{DD} - V_{in}(max) + V_{TN}$$

Using the gate to source voltage calculated above we can design the transistors M3 and M4.

$$\frac{W_3}{L_3} = \frac{W_4}{L_4} = \frac{I_{BIAS}}{K_P * \left(V_{SG3} - |V_{TP}|\right)^2}$$

Next step is to calculate $V_{DS5}(sat)$ using the specification of minimum input common mode voltage. The relation is given by

$$V_{DS5} = V_{in}(min) - V_{GS1} - V_{SS}$$

Where $$V_{GS1} = \sqrt{\frac{I_{BIAS} * L_1}{K_N * W_1}} + V_{TN}$$

Using the above-calculated value of V_{DS5} we can design the transistor M5.

$$\frac{W_5}{L_5} = \frac{2 * I_{BIAS}}{K_N * \left(V_{DS5}(sat)\right)^2}$$

Lastly, the bias voltage is given by

$$V_{B5} = (V_{DS5} / 2) + V_{TN}$$

4.4 AN EXAMPLE

4.4.1 SPECIFICATIONS

- DC gain (A_V) = 1000 V/V

- V_{in} (min) = 1.25 V
- V_{in} (max) = 4.5 V
- Load capacitance (C_L) = 1pf
- Total delay (ns) = 20ns
- V_{out} (max) = 4.5 V
- V_{out} (min) = 0.5 V

4.4.2 DESIGN STEPS

STEP 1: Let us first divide the total propagation delay into three stages. So we can have first stage delay of 10 ns and that of regenerative latch has delay of 7 ns and that of preamplifier stage's delay is 3 ns. So now we can design the three stages. Lets start from output stage.

$$I_{16} = I_{17} = C_L * \left(\frac{dv*2}{dt}\right) = 1*10^{-12}*\left(\frac{4*2}{10*10^{-9}}\right)$$

$$I_{16} = I_{17} = 800\mu A$$

$$\left(\frac{W}{L}\right)_{16} = \frac{2*I_{16}}{K_N*(V_{DS})^2} = \frac{2*800*10^{-6}}{6.33*10^{-5}*(0.5)^2} = 101.1$$

$$\left(\frac{W}{L}\right)_{17} = \frac{2*I_{17}}{K_N*(V_{DS})^2} = \frac{2*800*10^{-6}}{6.33*10^{-5}*(0.5)^2} = 101.1$$

Now, the corresponding p-type transistors ratio can be calculated as

$$\left(\frac{W}{L}\right)_{18,19} = K*\frac{\mu_n}{\mu_p}*\left(\frac{W}{L}\right)_{16,17} = 0.989*\frac{1215.74}{361.94}*101.1$$

$$\left(\frac{W}{L}\right)_{18,19} = 335.8$$

where K is the process transconductance ratio of the n and p type transistor of an inverter. We have used it here, as the output stage is an inverter itself.

STEP 2: Now we have to calculate the output capacitance of the latch stage. This we can do by taking into consider the transistor's capacitance it has to drive. So we have

$$C_{out2} = C_{gd19} + C_{gd16}$$
$$C_{out2} = C_{GDO_P} * W_{19} + C_{GDO_N} * W_{16}$$
$$C_{out2} = 3.35*10^{-10} * 335.8*10^{-6} + 2.89*10^{-10} * 101.1*10^{-6}$$
$$C_{out2} = 0.14 pF$$

So we can design second stage using above calculated value.

$$I_1 = I_2 = C_{out2} * \left(\frac{dv*2}{dt}\right) = 0.14*10^{-12} * \frac{4*2}{7*10^{-9}}$$
$$I_1 = I_2 = 160\mu A$$

We take current as 200μA for some margin. So transistor ratios are

$$\left(\frac{W}{L}\right)_{equ} = \frac{2*I_1}{K_N*(V_{DS})^2} = \frac{2*200*10^{-6}}{6.33*10^{-5}*(0.5)^2}$$
$$\left(\frac{W}{L}\right)_{equ} \cong 26$$

$$\left(\frac{W}{L}\right)_{8,9,12,13,14,15} = 2*\left(\frac{W}{L}\right)_{equ} = 2*26$$
$$\left(\frac{W}{L}\right)_{8,9,12,13,14,15} = 52$$

The corresponding p-type transistor's ratios are given by

$$\left(\frac{W}{L}\right)_{6,7,10,11} = K*\frac{\mu_n}{\mu_p}*\left(\frac{W}{L}\right)_{equ} = 0.989*\frac{1215.74}{361.94}*26$$

$$\left(\frac{W}{L}\right)_{6,7,10,11} \cong 87$$

STEP 3: For designing the preamplifier stage we have to calculate the output voltage that it has to drive as we did in step 2.

$$C_{out3} = C_{GSO} * W_{14} + 0.67 * C_{OX} * W_{eff} * L_{eff}$$
$$C_{out3} = 2.89 * 10^{-10} * 52 * 10^{-6} + 0.67 * 0.156 * 10^{-4} * 52 * 10^{-6} * 4 * 10^{-6}$$
$$C_{out3} = 17.2 fF$$

So the bias current will be

$$I_{BIAS} = 2 * C_{out3} * \left(\frac{dv}{dt}\right) = 2 * 17.2 * 10^{-15} * \left(\frac{4}{3 * 10^{-9}}\right)$$
$$I_{BIAS} = 50 \mu A$$

We take current as 100μA for some margin.

Using the bias current calculated above; design the transistor pair of current mirror circuit.

$$\frac{W_3}{L_3} = \frac{W_4}{L_4} = \frac{100 * 10^{-6}}{2.64 * 10^{-5} * (1.12 - |-0.63|)^2}$$

$$\frac{W_3}{L_3} = \frac{W_4}{L_4} = 15.7 \cong 16$$

$$K_P = 2.64 * 10^{-5} A / V^2$$

$$V_{SG3} = 5 - 4.5 + 0.62 = 1.12V$$
$$V_{TP} = -0.63V$$

Design of the differential pair requires the transconductance, which can be calculated using the open loop gain specification of both stages.Therefore,

$$g_{m1} = \frac{10{,}00 * (0.01 + 0.02) * 50 * 10^{-6}}{2202.2 * 10^{-6}}$$
$$g_{m1} = 15 * 10^{-4}\, S$$

$$g_{ds4} = \lambda_P * I'_4 = 0.02 * 50 * 10^{-6}, g_{ds2} = \lambda_N * I'_2 = 0.01 * 50 * 10^{-6}$$
$$I'_2 = I'_4 = \frac{I_{BIAS}}{2} = 50 * 10^{-6}\, A$$

Using the transconductance calculated above, differential pair ratios are given by

$$\frac{W_1}{L_1} = \frac{W_2}{L_2} = \frac{g_{m1}{}^2}{K_N * I_5} = \frac{(15 * 10^{-4})^2}{6.326 * 10^{-5} * 2 * 50 * 10^{-6}}$$
$$\frac{W_1}{L_1} = \frac{W_2}{L_2} \cong 356$$

Now the only transistor left for designing is M5. Firstly, we have to calculate the drain to source voltage of M5.

$$V_{DS5}(sat) = V_{icm-} - V_{GS1} - V_{SS}$$
$$V_{DS5}(sat) = 1.25 - 0.686 = 0.56V$$
$$V_{GS1} = \sqrt{\frac{50 * 10^{-6}}{6.326 * 10^{-5} * 356}} + 0.62 = 0.686V$$

So now,

$$\frac{W_5}{L_5} = \frac{2 * 100 * 10^{-6}}{6.33 * 10^{-5^2} * (0.56)^2}$$
$$\frac{W_5}{L_5} = 11$$

Lastly, the bias voltage is given by

$$V_{B5} = (V_{DS5} / 2) + V_{TN}$$
$$V_{B5} = (0.56 / 2) + 0.62$$
$$V_{B5} = 0.9\ V$$

The calculated aspect ratios of transistors are summarized in the table 2.

MOS	M1	M2	M3	M4	M5	M6	M7	M8	M9	M10	M11
W/L	356	356	16	16	11	87	87	52	52	87	87

MOS	M12	M13	M14	M15	M16	M17	M18	M19
W/L	52	52	52	52	101.1	101.1	335.8	335.8

Table 2

DESIGN OF SELF-BIASED COMPARATOR

5.1 INTRODUCTION

Many techniques have been introduced in the literature for implementing high-speed CMOS comparators. The most commonly used are the latches, which are used after the preamplifier stage. If a comparator has a large capacitive load, the chances are that it is slew rate limited. The circuit that is designed here has the ability to sink and source large amounts of current in large capacitances. The circuit configuration [3] differs from those of conventional CMOS differential-amplifiers configuration in two ways:

1. The amplifier is completely complementary i.e. each n-type device operates in push-pull fashion with a corresponding p-type device.
2. The amplifier is self-biased through negative feedback.

These two differences result in several performance enhancements desirable in comparator applications.

5.2 SELF -BIASING COMPARATOR

CMOS differential amplifiers with wide input dynamic ranges have been reported [2,18]. All of these amplifiers are externally biased while none of them is fully complementary. The circuit configuration that has been designed is as shown in the Figure 5.1. As we can see that this circuit is fully complementary as well as entirely self-biased.

The operation of self-biasing comparator can be understood through its derivation [3]. Figure 5.2(a) illustrates two folded cascode differential amplifiers, one the complement of other. These amplifiers have the greater dynamic ranges than ordinary differential amplifier as a result of the larger drain-source voltage drop on input pairs. This larger voltage drop maintains the input pairs in active region even for large input voltage swings. While neither amplifier in Figure 5.2(a) is capable of covering the entire input range from negative supply to positive supply, a combination of the two amplifiers can cover this entire range. In the first step of derivation, the loads of the two amplifiers are deleted, and their outputs are connected together to produce the fully complementary, but externally biased differential amplifier of Figure 5.2(b). However the circuit of Figure 5.2(b) cannot be biased in a stable fashion.

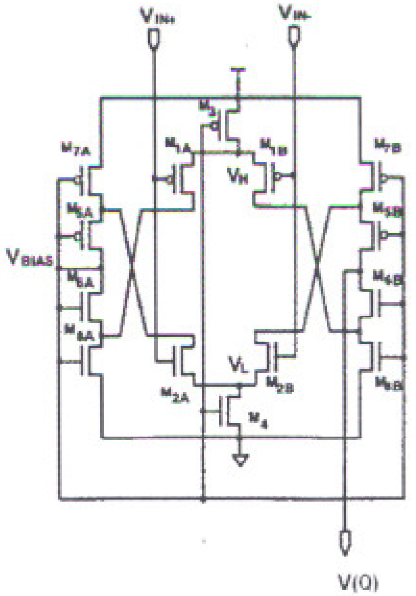


Figure. 5.1. Self-Biased Comparator

In order for the circuit to be biased in stable fashion the currents through M3 and M4 devices should be identical. Any difference in currents through these two devices result in extreme shifts in amplifier bias voltages. Achieving perfect equality of currents in these two devices using external biasing is practically impossible, so that the configuration of Figure 5.2(b) is practically impossible.

A simple modification of the circuit of Figure 5.2(b), however, results in stabilization of the bias voltages. This modification is illustrated in Figure 5.1, in which the two bias-voltages are disconnected from the external sources and instead are connected to internal amplifier node V_{BIAS}. This self-biasing of the amplifier creates the negative feedback loop that stabilizes the bias voltages.

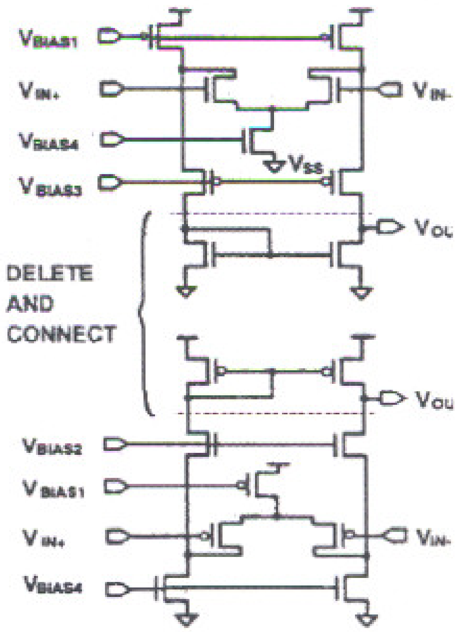


Figure. 5.2(a) Folded Cascode Differential Amplifier

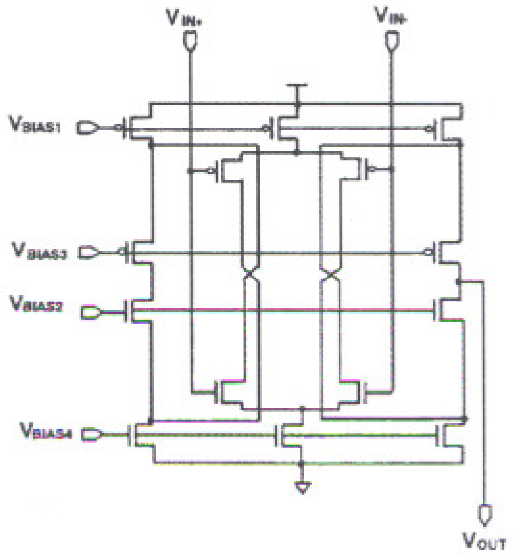


Figure. 5.2(b) Externally Biased Differential Amplifier

Any variations in the processing parameters or operating conditions that shifts the bias voltages away from their nominal values result in a shift in V_{BIAS} that corrects the bias voltages through negative feedback. The resulting self-biased amplifier is illustrated in Figure 5.1. The comparator designed takes the minimum delay as compared to [6,19,26].

5.3 DESIGN PROCEDURE

5.3.1 SPECIFICATIONS

- Unity gain bandwidth (GB)
- Input common mode range [V_{in} (min) and V_{in} (max)]
- Load capacitance (C_L)
- Slew rate (SR)
- Output voltage swing [V_{out} (max) and V_{out} (min)]

5.3.2 DESIGN STEPS

STEP 1: The first step towards design of self-biased comparator is to decide the bias currents in transistors M_3 and M_4 using the slew rate and load capacitance specifications. So we have

$$I_3 = I_4 = SR * C_L$$

STEP 1: Other bias currents I_7 and I_8 flowing through M_{7A} or M_{7B} and M_{8A} or M_{8B} should be designed in such a way that the dc current in cascode branches never goes to zero. To implement this, the values of these currents are normally between the values of I_3 or I_4 and twice their values. Now to calculate the W/L ratios of these transistor we need to calculate their drain to source voltages. From the specification of output voltage swing, we can see that the minimum voltage that make the transistors M_{7A} and M_{5A} to remain in saturation is that the drop between these two transistors is equal to the difference of the V_{DD} and V_{out} (max), similarly for M_{8A} and M_{6A} this voltage is V_{SS} and V_{out} (min) difference. These voltages if we equally divide between the two respective transistors we get the drain to source voltage of the transistors. So taking this drain to source voltage and the bias current together we get

$$I_7 = I_8 = 1.3 * I_3$$

$$\left(\frac{W}{L}\right)_{7A,7B} = \frac{2 * I_7}{K_P * (V_{ds})^2}$$

$$\left(\frac{W}{L}\right)_{8A,8B} = \frac{2 * I_8}{K_N * (V_{ds})^2}$$

Assuming that transistors are in saturation the calculated drain to source voltage can be increased to twice its value so that the transistor remain in deep saturation area.

STEP 3: The current flowing in M_{5A} or M_{5B} and M_{6A} or M_{6B} is

$$I_5 = I_6 = I_7 - (0.5 * I_3)$$
$$\left(\frac{W}{L}\right)_{5A,5B} = \frac{2 * I_5}{K_P * (V_{ds})^2}$$
$$\left(\frac{W}{L}\right)_{6A,6B} = \frac{2 * I_6}{K_N * (V_{ds})^2}$$

Where V_{ds} we have already calculated in step 2.

STEP 4: For the design of differential pair we again assume that they are in saturation. Using the unity gain bandwidth

$$g_{m1} = g_{m2} = 2 * \pi * GB * C_L$$
$$\left(\frac{W}{L}\right)_{1A,1B} = \frac{g_{m1}^{\ 2}}{K_P * I_3}$$
$$\left(\frac{W}{L}\right)_{2A,2B} = \frac{g_{m2}^{\ 2}}{K_N * I_4}$$

STEP 5: Lastly the tail transistors are designed using input common mode range specification. From [20] we have

$$V_{ds4} = V_{in}(\min) - V_{gs2A}$$

where

$$V_{gs2A} = \left(\sqrt{\frac{2 * I_4}{K_N * \left(\frac{W}{L}\right)_{2A}}} \right) + V_{TN}$$

$$\left(\frac{W}{L}\right)_4 = \frac{2 * I_4}{K_N * (V_{ds4})^2}$$

Where V_{TN} is the threshold voltage for n-type transistor. Another tail transistor M_3 can be designed using the mobility ratio of n-type and p-type transistor.

5.4 AN EXAMPLE

5.4.1 SPECIFICATIONS

- Unity gain bandwidth (GB) = 10 MHz
- V_{in} (min) = 1.0 V
- V_{in} (max) = 4.0 V
- Load capacitance (C_L) = 15pF
- Slew rate (SR) = 10 V/μV
- V_{out} (max) = 4.5 V
- V_{out} (min) = 0.5 V

5.4.2 DESIGN STEPS

STEP 1: First of all we need to calculate the bias current through the upper and lower tail transistors.

$$I_3 = I_4 = SR * C_L = 10 * 10^6 * 15 * 10^{-12}$$

$$I_3 = I_4 = 150 \mu A$$

We take the current 200μA for some margin.

STEP 2: Now the currents I_7 and I_8 will lie between above calculated current values and twice their values. So we can take

$$I_7 = I_8 = 1.3 * I_{3,4}$$
$$I_7 = I_8 = 1.3 * 200 = 260\mu A$$

$$\left(\frac{W}{L}\right)_{7A,7B} = \frac{2 * I_7}{K_P * (V_{ds})^2} = \frac{2 * 260 * 10^{-6}}{2.64 * 10^{-5} * (0.5)^2}$$
$$\left(\frac{W}{L}\right)_{7A,7B} \cong 79$$
$$\left(\frac{W}{L}\right)_{8A,8B} = \frac{2 * I_8}{K_N * (V_{ds})^2} = \frac{2 * 260 * 10^{-6}}{6.33 * 10^{-5} * (0.5)^2}$$
$$\left(\frac{W}{L}\right)_{8A,8B} = 33$$

Where the calculated V_{ds} was 0.25 V but for keeping transistors in deep saturation region we take it 0.5 V as discussed in design procedure.

STEP 3: The current flowing in M_{5A} or M_{5B} and M_{6A} or M_{6B} is

$$I_5 = I_6 = I_7 - (0.5 * I_3)$$
$$I_5 = I_6 = 260 - (0.5 * 200)$$
$$I_5 = I_6 = 160\mu A$$
$$\left(\frac{W}{L}\right)_{5A,5B} = \frac{2 * I_5}{K_P * (V_{ds})^2} = \frac{2 * 160 * 10^{-6}}{2.64 * 10^{-5} * (0.5)^2}$$
$$\left(\frac{W}{L}\right)_{5A,5B} = 49$$

$$\left(\frac{W}{L}\right)_{6A,6B} = \frac{2*I_6}{K_N*(V_{ds})^2} = \frac{2*160*10^{-6}}{6.33*10^{-5}*(0.5)^2}$$
$$\left(\frac{W}{L}\right)_{6A,6B} = 21$$

Where V_{ds} we have already calculated in step 2.

STEP 3: Now we are left with the design of differential pair transistors.

$$g_{m1} = g_{m2} = 2*\pi*GB*C_L = 2*3.14*10*10^6*15*10^{-12}$$
$$g_{m1} = g_{m2} = 9.42*10^{-4}\,S$$
$$\left(\frac{W}{L}\right)_{1A,1B} = \frac{g_{m1}^{\ 2}}{K_P*I_3} = \frac{(9.42*10^{-4})^2}{2.64*10^{-5}*200*10^{-6}}$$
$$\left(\frac{W}{L}\right)_{1A,1B} = 168$$
$$\left(\frac{W}{L}\right)_{2A,2B} = \frac{g_{m2}^{\ 2}}{K_N*I_4} = \frac{(9.42*10^{-4})^2}{6.33*10^{-5}*200*10^{-6}}$$
$$\left(\frac{W}{L}\right)_{2A,2B} = 70$$

STEP 4: Lastly the tail transistors are designed using input common mode range specification. From [1] we have

$$V_{ds4} = V_{in}(\min) - V_{gs2A}$$
$$V_{ds4} = 1 - 0.8 = 0.2V$$
$$V_{gs2A} = \left(\sqrt{\frac{I_4}{K_N*\left(W/L\right)_{2A}}}\right) + V_{TN}$$

$$V_{gs2A} = \left(\sqrt{\frac{200*10^{-6}}{6.33*10^{-5}*70}}\right) + 0.62 = 0.8V$$

$$\left(\frac{W}{L}\right)_4 = \frac{2*I_4}{K_N*(V_{ds4})^2} = \frac{2*200*10^{-6}}{6.33*10^{-5}*(0.5)^2}$$

$$\left(\frac{W}{L}\right)_4 = 26$$

For keeping the transistor in deep saturation we have increased the drain to source voltage. Using the mobility ratio we have

$$\left(\frac{W}{L}\right)_3 = 61$$

The calculated values of transistor ratios are summarized in table 3.

MOS	M1A	M1B	M2A	M2B	M3	M4	M5A	M5B
W/L	168	168	70	70	61	26	49	49

MOS	M6A	M6B	M7A	M7B	M8A	M8B
W/L	21	21	79	79	33	33

Table 3

INTRODUCTION TO TANNER TOOL

Tanner tool is a Spice Computer Analysis Programmed for Analog Integrated Circuits. Tanner tool consists of the following Engine Machines

1. S-EDIT (Schematic Edit)
2. T-EDIT (Simulation Edit)
3. W-EDIT (Waveforms Edit)
4. L-EDIT (Layout Edit)

Using these engine tools, spice programme provides facility to the user to design & simulate new ideas in Analog Integrated Circuits before going to the time consuming & costly process of chip fabrication.

6.1 SCHEMATIC EDIT TOOL (S-EDIT)

S-Edit is hierarchy of files, modules & pages. It introduces symbol & schematic modes. S-Edit provides the facility of:

1. Beginning a design.
2. Viewing, drawing & editing of objects.
3. Design connectivity.
4. Properties, net lists & simulation.
5. Instance & browse schematic & symbol mode.

BEGINNING A DESIGN: It explains the design process in detail in terms of file module operation and module.

Browser: Effective schematic design requires a working knowledge of the S-Edit design hierarchy of files & modules. S-Edit design files consist of modules. A module is a functional unit of design such as a transistor, a gate and an amplifier.

Modules contain two components:

1) **Primitives –** Geometrical objects created with drawing tools.

2) **Instances** – References to other modules in file. The instanced module is the original.

S-Edit has two viewing modes:

1) **Schematic Mode:** To create or view a schematic, we operate in schematic mode.

2) **Symbol Mode:** It represents symbol of a larger functional unit such as operational amplifier.

6.2 T-SPICE Pro Circuit ANALYSIS

Let's have an introduction to the integrated components of the T- Spice Pro circuit analysis suite.

Schematic data files (**.sdb)** describing the circuits to be analyzed in *graphical* form, for display and editing by S- Edit™ Schematic Editor.

Simulation input files (**.sp)** describing the circuits to be analyzed in *textual* form, for editing and simulation by T- Spice™ Circuit Simulator.

Simulation output files (**.out**) containing the numerical results of the circuit analyses, for manipulation and display by W- Edit™ Waveform Viewer.

6.2.1 CIRCUIT SIMULATOR (T-SPICE)

T- Spice Pro's *waveform probing* feature integrates S- Edit, T- Spice, and W-Edit to allow individual points in a circuit to be specified and analyzed. Let's discuss a few analysis:

The heart of T-Spice operation is the input file (also known as the circuit description, the net list & the input deck). This is a plain text file that contains the device statement & simulation commands, drawn from the SPICE circuit description language with which T-Spice constructs a model of the circuit to be simulated. Input files can be created and modified with any text editor.T-Spice is a tool used for simulation of the circuit. It provides the facility of

1. Design Simulation
2. Simulation Commands
3. Device Statements
4. User-Designed External Models
5. Small Signal & Noise Models

T-Spice uses Kirchoff's Current Law (KCL) to solve circuit problems. To T-Spice, a circuit is a set of devices attached to nodes. The voltage at all nodes represents the circuit state. T-Spice solves for a set of node voltage that satisfied KCL (implying that sum of currents flowing into each node is zero). In order to evaluate whether a set of node voltages is a solution, T-Spice computes and sums all the current flowing out of each device into nodes connected to it (its terminals). The relationship between the voltages at device terminals and the currents through the terminal is determined by the device model for a resistor of resistance R is

$$I = \Delta V / R$$

Where ΔV represents the voltage difference across the device.

Let's discuss a few analysis:

DC Operating Point Analysis

DC operating point analysis finds a circuit's steady- state condition, obtained (in principle) after the input voltages have been applied for an infinite amount of time. The .include command causes T- Spice to read in the contents of the model file ml2_

125 .md for the evaluation of nmos and pmos transistors. This file consists of two .model commands, describing two MOSFET models called nmos and pmos. For example:

```
.model pmos pmos
+ Level= 2 Ld=. 03000u Tox= 225. 000E- 10
+ Nsub= 6.575441E+ 16 Vto=- 0. 63025 Kp= 2.635440E- 05
+ Gamma= 0.618101 Phi=. 541111 Uo= 361.941
+ Uexp= 8.886957E- 02 Ucrit= 637449 Delta= 0. 0
+ Vmax= 63253.3 Xj= 0.112799u Lambda= 0.0
+ Nfs= 1.668437E+ 11 Neff= 0. 64354 Nss= 3.00E+ 10
+ Tpg=- 1.000 Rsh= 150 Cgso= 3.35E- 10
+ Cgdo= 3.35E- 10 Cj= 4.75E- 04 Mj=. 341
+ Cjsw= 2.23E- 10 Mjsw=. 307
```

ml2_ 125. md assigns values to various Level 2 MOSFET model parameters for both n - and p -type devices. When read by the input file, these parameters are used to evaluate Level 2 MOSFET model equations, and the results are used to construct internal tables of current and charge values. Values read or interpolated from these tables are used in the computations called for by the simulation. Two transistors, mn1 and m1p, are defined in invert1. sp . These are MOSFETs, as indicated by the key letter m, which begins their names. Following each transistor name are the names of its terminals. The required order of terminal names is: drain – gate – source – bulk. Then the model name (nmos or pmos), and physical characteristics such as length and width, are specified. The .op command performs a DC operating point calculation and writes the results to the file specified in the Simulate > Start Simulation dialog. The output file lists the DC operating point information for the circuit described by the input file.

DC Transfer Analysis

DC transfer analysis is used to study the voltage or current at one set of points in a circuit as a function of the voltage or current at another set of points. This is done by sweeping the source variables over specified ranges, and recording the output. A list of sources to be swept, and the voltage ranges across which the sweeps are to take place follow the .dc command, indicating transfer analysis. The transfer analysis will be performed as follows: vdd will be set at 2 volts and vin will be swept over its specified range; vdd will then be incremented to 2.5 volts and vin will be reswept over its range; and so on, until vdd reaches the upper limit of its range.

The .dc command ignores the values assigned to the voltage sources vdd and vin in the voltage source statements, but they must still be declared in those statements. The results for nodes in and out are reported by the .print dc command to the specified destination.

Transient Analysis

Transient analysis provides information on how circuit elements vary with time. The basic T- Spice command for transient analysis has three modes. In the default mode, the DC operating point is computed, and T- Spice uses this as the starting point for the transient simulation.

The. tran command (.tran 2n 600n) specifies the characteristics of the transient analysis to be performed: it will last for 600 nanoseconds, with time steps no larger than 2 nanoseconds.

AC Analysis

AC analysis characterizes the circuit's behavior dependence on small- signal input frequency. It involves three steps: (1) calculating the DC operating point; (2) linearizing the circuit; and (3) solving the linearized circuit for each frequency. For example, we have

vdiff in2 in1 -0.0007 AC 1 90

.ac DEC 5 1 100MEG

vdiff sets the DC voltage difference between nodes in2 and in1 to –0. 0007 volts; its AC magnitude is 1 volt and its AC phase is 90 degrees. The .ac command performs an AC analysis. Following the .ac keyword is information concerning the frequencies to be swept during the analysis. In this case, the frequency is swept logarithmically, by decades (DEC); 5 data points are to be included per decade; the starting frequency is 1 Hz and the ending frequency is 100 MHz. The .print commands write the voltage magnitude (in decibels) and phase (in degrees), respectively, for the node out to the specified file.

The. acmodel command writes the small- signal model parameters and operating point voltages and currents for all circuit devices

Noise Analysis

Real circuits, of course, are never immune from small, "random" fluctuations in voltage and current levels. In T- Spice, the influence of noise in a circuit can be simulated and reported in conjunction with AC analysis. The purpose of noise analysis is to compute the effect of the noise associated with various circuit devices on an output voltage or voltages as a function of frequency. Noise analysis is performed in conjunction with AC analysis; if the .ac command is missing, then the .noise command is ignored. With the .ac command present, the. noise command causes noise analysis to be performed at the same frequencies: starting at 1 Hz, ending at 100 MHz, 5 data points per decade. The .noise command takes two arguments: the output at which the effects of noise are to be computed, and the input at which the noise can be considered to be concentrated for the purposes of estimating the equivalent noise spectral density. The .print command is used to print results.

6.3 WAVEFORM-EDIT

The ability to visualize the complex numerical data resulting from VLSI circuit simulation is critical to testing, understanding & improving these circuits. W-Edit is a waveform viewer that provides ease of use, power & speed in a flexible environment designed for graphical data representation. The advantages of W-Edit includes:

1. Tight Integration with T-spice, Tanner EDA's circuit level simulator. W-Edit can chart data generated by T-spice directly, without modification of the

output text data files. The data can also be charted dynamically as it is produced during the simulation.

2. Charts can automatically configured for the type of data being presented.
3. A data is treated by W-Edit as a unit called a trace. Multiple traces from different output files can be viewed simultaneously in single or several windows; traces can be copied and moved between charts & windows. Trace arithmetic can be performed on existed tracing to create new ones.
4. Chart views can be panned back & forth and zoomed in & out, including specifying the exact X-Y coordinate range.
5. Properties of axes, traces, rides, charts, text & colors can be customized.

Numerical data is input to W-Edit in the form of plain or binary text files. Header & Comment information supplied by T-Spice is used for automatic chart configuration. Runtime update of results is made possible by linking W-Edit to a running simulation in T-Spice.

W-Edit saves data with chart, trace, axis & environment settings in files with the WDB (W-Edit Database).

6.4 LAY-OUT (L-EDIT)

It is a tool that represents the masks that are used to fabricate an integrated circuit. It describes a layout design in terms of files, cells & mask primitives. On the layout level, the component parameters are totally different from schematic level. So it provides the facility to the user to analyse the response of the circuit before forwarding it to the time consuming & costly process of fabrication. There are rules for designing layout diagram of a schematic circuit using which user can compare the output response with the expected one.

L- Edit: An Integrated Circuit Layout Tool

In L- Edit, layers are associated with masks used in the fabrication process. Different layers can be conveniently represented by different colors and patterns. L- Edit describes a layout design in terms of files, cells, instances, and mask primitives. You may load as many files as desired into memory. A file may be composed of any number of cells. These cells may be hierarchically related, as in a typical design, or they may be independent, as in a "library" file. Cells may contain any number or combination of mask primitives and instances of other cells.

Cells: The Basic Building Blocks

The basic building block of the integrated circuit design in L- Edit is a cell.
Design layout occurs within cells. A cell can:

- Contain part or all of the entire design.
- Be referenced in other cells as a sub- cell, or instance.
- Be made up entirely of instances of other cells.
- Contain original drawn objects, or primitives.
- Be made up entirely of primitives or a combination of primitives and instances of other cells.

Hierarchy

L- Edit supports fully hierarchical mask design. Cells may contain instances of other cells. An instance is a reference to a cell; should you edit the instanced cell, the change is reflected in all the instances of that cell. Instances simplify the process of updating a design, and also reduce data storage requirements, because an instance does not need to store all the data within the instanced cell — instead, only a reference to the instanced cell is stored, along with information on the position of the instance and on how the instance may be rotated and mirrored. There is no preset limit to the size or complexity of the hierarchy. Cells may contain instances of others cells that in turn contain instances of other cells, to an arbitrary number of levels (subject only to hardware constraints).

L- Edit does not use a "separated" hierarchy: instances and primitives may coexist in the same cell at any level in the hierarchy. Design files are self- contained. The "pointer" to a cell contained in an instance always points to a cell within the same design file. When cells are copied from one file to another, L- Edit automatically copies across any cells that are instanced by the copied cell, to maintain the self-contained nature of the destination file.

Design Rules

Manufacturing constraints can be defined in L- Edit as design rules. Layouts can be checked against these design rules.

Design Features

L- Edit is a full- custom mask editor. Manual layout can be accomplished more quickly because of L- Edit's intuitive user interface. In addition, one can construct special structures to utilize a technology without, worrying about problems caused by automatic transformations. Phototransistors, guard bars, vertical and horizontal bipolar transistors, static structures, and Schottky diodes, for example, are as easy to design in CMOS- Bulk technology as are conventional MOS transistors.

Floor plans

L- Edit is a manual floor planning tool. You have the choice of displaying instances in outline, identified only by name, or as fully fleshed- out mask geometry. When you display your design in outline, you can manipulate the arrangement of the cells in your design quickly and easily to achieve the desired floor plan.

One can manipulate instances at any level in the hierarchy, with insides hidden or displayed, using the same graphical move/ select operations or rotation/ mirror commands that you use on primitive mask geometry.

Memory Limits

In L- Edit, one can make your design files as large as one like, given available RAM and disk space.

Hard Copy

L- Edit provides the capability to print hard copy of the design. A multiage option allows very large plots to be printed to a specific scale on multiple 8 1/ 2 x 11 inch pages. An L- Edit macro is available to support large- format, high- resolution, color plotting on inkjet plotters.

Variable Grid

L- Edit's grid options support lambda- based design as well as micron- based and mil- based design.

Error Recovery

L- Edit's error- trapping mechanism catches system errors and in most cases provides a means to recover without losing or damaging data.

L- Edit Modules

- L- Edit ™: a layout editor
- L- Edit ¤ Extract ™: a layout extractor
- L- Edit ¤ DRC ™: a design rule checker

L- Edit is a full- featured, high- performance, interactive, graphical mask layout editor. L- Edit generates layouts quickly and easily, supports fully hierarchical designs, and allows an unlimited number of layers, cells, and levels of hierarchy. It includes all major drawing primitives and supports 90°, 45°, and all- angle drawing modes.

L- Edit ¤ Extract creates SPICE- compatible circuit netlists from L- Edit layouts. It can recognize active and passive devices, sub circuits, and the most common device parameters, including resistance, capacitance, device length, width, and area, and device source and drain area.

L- Edit ¤ DRC features user- programmable rules and handles minimum width, exact width, minimum space, minimum surround, non- exist, overlap, and extension rules. It can handle full chip and region- only DRC. DRC offers Error Browser and Object Browser functions for quickly and easily cycling through rule- checking errors.

ANALOG LAYOUT DESIGN

7.1 LAYOUT DESIGN RULES

The physical mask layout of any circuit to be manufactured using a particular process must confirm to a set of geometric constraints or rules, which are generally called layout design rules. These rules usually specify the minimum allowable line widths for physical objects on chip such as metal and polysilicon interconnects or diffusion areas, minimum feature dimensions, and minimum allowable separations between two such features. If a metal line width is too small, for example, it is possible for the line to break during the fabrication process or afterwards, resulting in an open circuit. If the two lines are placed too close to each other in the layout, they may form an unwanted short circuit by merging during or after the fabrication process. The main objective of design rules is to achieve, for any circuit to be manufactured with a particular process, a high overall yield and reliability while using the smallest possible silicon area.

There is usually trade off between higher yield, which is obtained through conservative geometries, and better area efficiency, which is obtained through aggressive, high-density placement of various features on the chip. The layout design rules, which are specified for a particular fabrication process normally, represent a reasonable optimum point in terms of yield and density. It must be emphasized, however, that the design rules do not represent strict boundaries, which separate "correct" designs from "incorrect" ones. A layout which violates some of the specified design rules may still result in an operational circuit with reasonable yield, whereas another layout observing all specified design rules may result in a circuit which is not functional and/or has very low yield. To summarize, we can say, in general, that observing the layout rules significantly increases the probability of fabricating a successful product with high yield.

The design rules [18] are usually described in two ways:

1. **Micron rules,** in which the layout constraints such as minimum feature sizes and minimum allowable feature separations are stated in terms of absolute dimensions in micrometers, or,
2. **Lambda rules,** which specify the layout constraints in terms of a single parameter (λ) and thus allow linear, proportional scaling of all geometrical constraints.

Lambda-based design rules were originally devised to simplify the industry-standard micron-based design rules and to allow scaling capability for various processes. It must be emphasized, however, that most of the sub-micron CMOS process design rules do not lend themselves to straightforward linear scaling. The use of lambda based design rules must therefore be handled with caution in sub-micron geometries.

The design rules define geometrical relations referring to the following four possibilities:

- Element width, $W_{min:}$ it is the minimum (or the maximum) width allowed for a given element. It avoids possibly opening or vanishing of the element. For example, we have a rule defining the minimum width of the poly gate and a rule defining the minimum size of poly-metal contacts.
- Element spacing ΔW_{min}: this is the minimum distance between two elements. This rule avoids shortening. The elements can be of the same kind (for example metal-metal) or of a different kind. For example, we have a rule defining the minimum distance between two metal lines or the minimum distance between a poly line and unrelated diffusion.
- Inner overlap $W_{in,min}$: is the minimum separation between two elements that we design one inside the other. This rule avoids the two elements detaching. For example, we have a rule defining the inner overlap of the contact over or below a metal.

➢ External extension, $W_{ex,min}$: is the minimum extension of an element overlapping another element. This kind of rule ensures that the two elements are fully overlapped. For example, we use a design rule to ensure that the poly gate always crosses the active area.

The above four categories of design rules are specified for all the possible layers used by technology. The above description of possible rules refers to the minimum spacing. However, some rules require the assigned figure to be "exact". Therefore, excepting the latter case, the designer can exceed the minimum spacing by an extent considered appropriate.

7.2 LAYOUT OF TRANSISTORS

The final step in integrated design is physical description. This consists of defining the masks to be used for processing. An MOS transistor is achieved by the simple overlap of two rectangles: one defining the active area and the other defining the polysilicon gate [2,18,21]. (Figure 7.1)

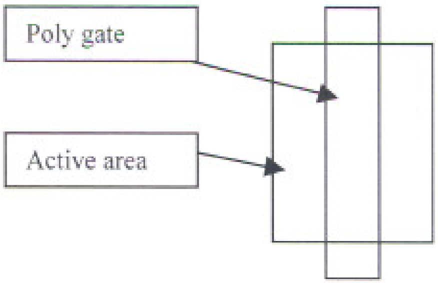


Figure 7.1: The two layers that achieve a transistor

The parts of the active area that are not protected by the gate originate the source and drain, while the part protected by the gate forms the transistor channel . To ensure that the source and drain are separated, even in presence of fabrication inaccuracies, the gate overlaps the active area to a given extent, its value being defined by the design rules of the technology used.

The physical design is not limited to the masks of the active area and polysilicon. When the transistor must be realized in the well, a suitable pattern must be defined. Moreover it is necessary to arrange the connections of source, drain and gate together with the substrate and well biasing. A typical layout of a MOS transistor (sitting in the well) is shown in Figure 7.2. It represents a pattern typical of analog circuits: the aspect ratio (W/L) of the transistor is not at a minimum, as is usually the case for analog designs.

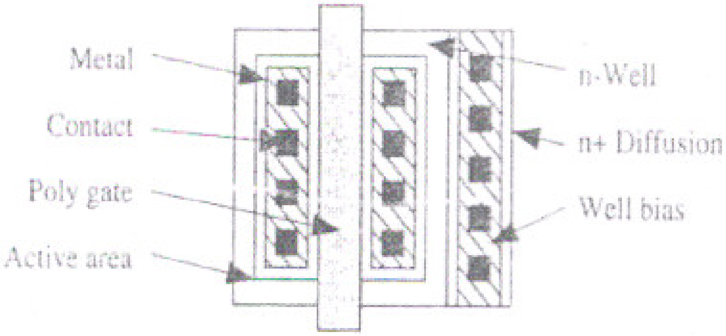


Figure 7.2: Layout of a p-channel transistor (inside an n-well)

The key points to consider when we draw transistor layouts are the following:

- Parasitic resistances at source and drain must be kept as low as possible.
- Parasitic capacitances should be minimized.
- Matching between paired elements is very important.

Concerning the first condition, we should remember that drain and source diffusions have a given sheet resistance. With only a few squares, we can achieve the hundreds of ohms of resistance: even with a current as low as few tens of μA we can have drop voltages of milivolts. Therefore, as shown in Figure 7.2, we must use multiple contacts on the top of source and drain regions to avoid parasitic transversal drop voltages. Designers prefer multiple contacts placed at a minimum distance instead of using a single large contact placed at a minimum distance instead of using a single large contact. Many contacts placed at a minimum distance instead of using a single large contact. Many contacts placed close to each other make the surface of metal connections smoother than when using only one contact; this prevents micro cracks in the metal that can be a source of failure.

Parasitic capacitances derive from the reverse source-substrate or drain substrate diodes. We have just seen that this is useful in establishing good contacts. Hence, source and drain area must be large enough to accommodate contacts and to fulfil the design rules. However, it is possible to reduce the source and drain area and, consequently, reduce the parasitic capacitances. This is achieved using the layout shown in Figure 7.3.

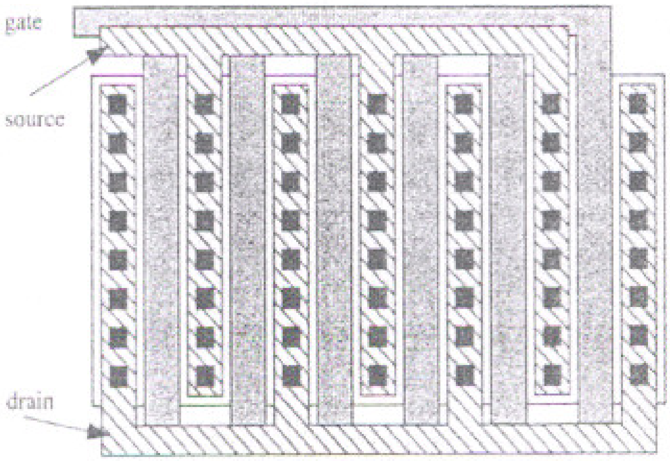
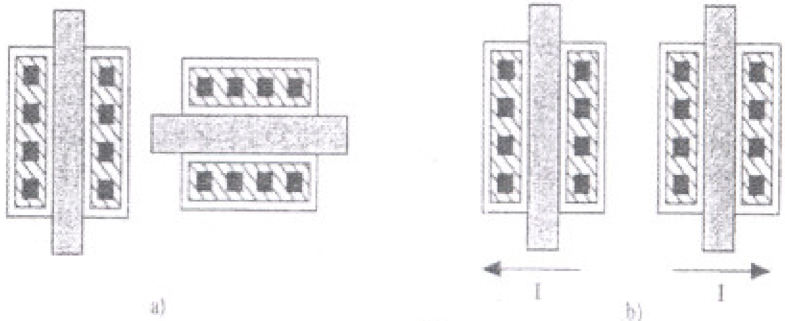


Figure 7.3: Interdigitized transistor

The transistor is split into a given number parts that are connected in parallel. We can see that most of the source and drain area is used doubly allowing the left and right parts of the transistors to be connected. It follows that the parasitic capacitances can be reduced up to a factor of 2.

Matching is very important when we have to design current mirrors and differential pairs. In general, bad matching produces high offset. Therefore, we have to use layouts that optimize matching. This is achieved by providing the best symmetrical conditions. Transistors with different orientation Figure 7.4(a) match badly. Moreover, we can suffer mismatch if the current in transistors is flowing in opposite directions Figure 7.4(b).



a) b)

Figure 7.4: Badly matching transistors: a) bad orientation b) with opposite current flow

The best methods of achieving good matching are shown in Figure 7.5. We assume that the two transistors that should match have one of the terminals (source or drain) in common so that we can use the interdigitated arrangement. Each transistor is split into four equal parts; they are interleaved in two by

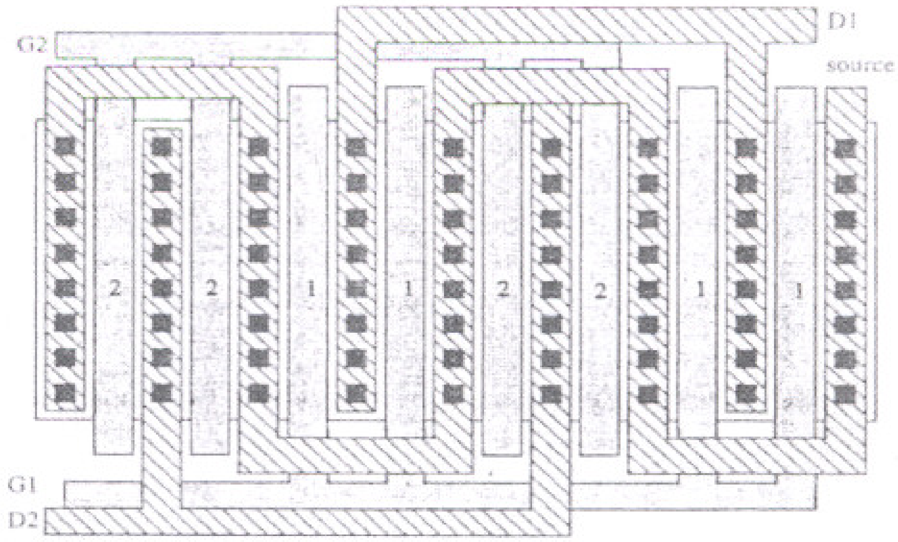


Figure 7.5: Layout of a matched transistor pair

two's so that for one pair of pieces of same transistor we have currents flowing in opposite directions. A final point concerns the biasing of substrate or of the well. This is a very important issue: we have to ensure that the biasing is as close as possible to the active devices. Any noisy signal affecting the substrate or the well should be sunk by the biasing and should not affect current itself. For this reason, any possible silicon space should be used for biasing purposes.

7.3 STACKED LAYOUT

Splitting transistor in a number of fingers favors a stack arrangement and improves the layout matching [18]. For example say in Figure 7.6 presenting the layout of a simple current mirror. The four fingers of each transistor were interleaved so that the centroid of the two transistors is one close to each other. The arrangement of the stack was AABBAABB (where A and B represent the fingers of M1 and M2 respectively). An alternative organization was ABBAABBA that lead to an identical common centroid. However, the boundary conditions are not symmetrical: two fingers of M1 establish the two boundaries while M2 have all the fingers inside the array.

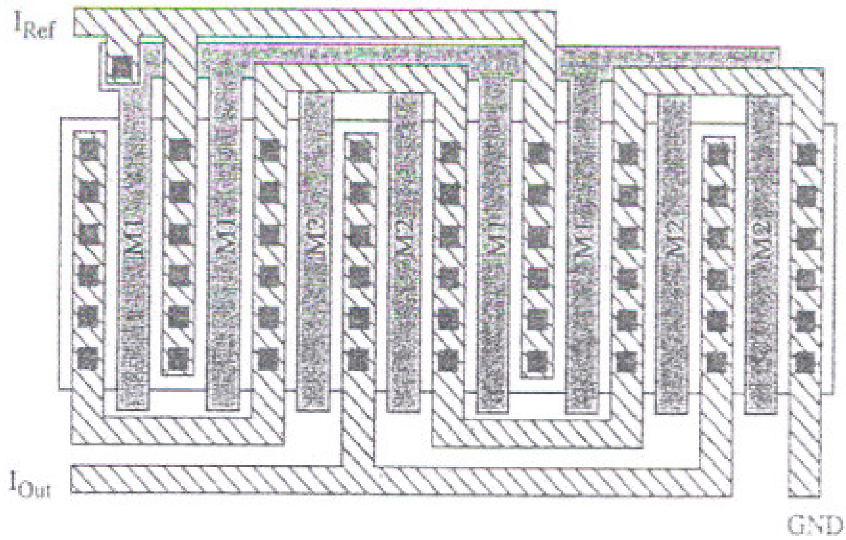


Figure 7.6: Layout of current mirror

The above layout strategy can be generalized for more complex cells. However, it is important to work on a design that favors the stacked approach. The transistors' fingers that should be laid-out on the same stack must have the same width. This is often possible: all the circuits include transistors, which sizes are not particularly critical. A small change of the widths doesn't modify the performances but permits a better layout.

7.4 LAYOUT OF SELF-BIASED COMPARATOR

Using the techniques of analog layout as described above, the layout of self-biased comparator is developed. The schematic of self-biased comparator is as shown in Figure 7.7.

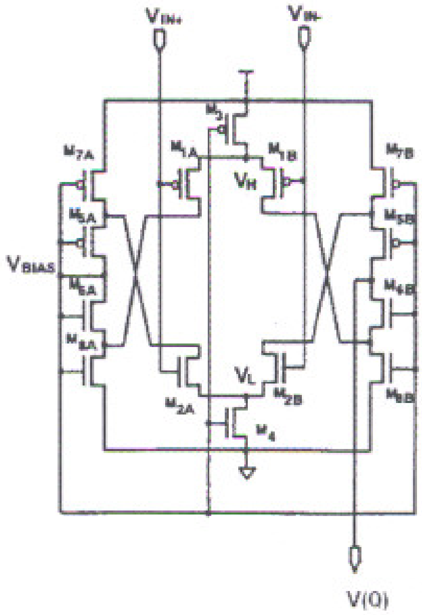


Figure 7.7: Self-biased comparator

For layout, the circuit is divided into four parts. Two parts for p-type transistors and two for n-type. The first part of p-type transistors include the p-differential pair and its corresponding tail transistor i.e. M_{1A} and M_{1B} and M_3. Another part includes the transistor M_{7A}, M_{7B} and M_{5A}, M_{5B}. Similarly, one part of n-type transistors include the n-differential pair and its corresponding tail transistor i.e. M_{2A} and M_{2B} and M_4. Another part includes the transistor M_{6A}, M_{6B} and M_{8A}, M_{8B}. The below scheme shows the possible floor planning.

EEEEE	GGHHGGHHGGHHGGHHGGHH
ABBAABBAABBAABBAABBA	IIIII JJJJJ
CDDCCDDCCD	KKKKK LLLLL
FFFFF	MNNMMNNMMN

The used letters denotes transistor fingers corresponding to

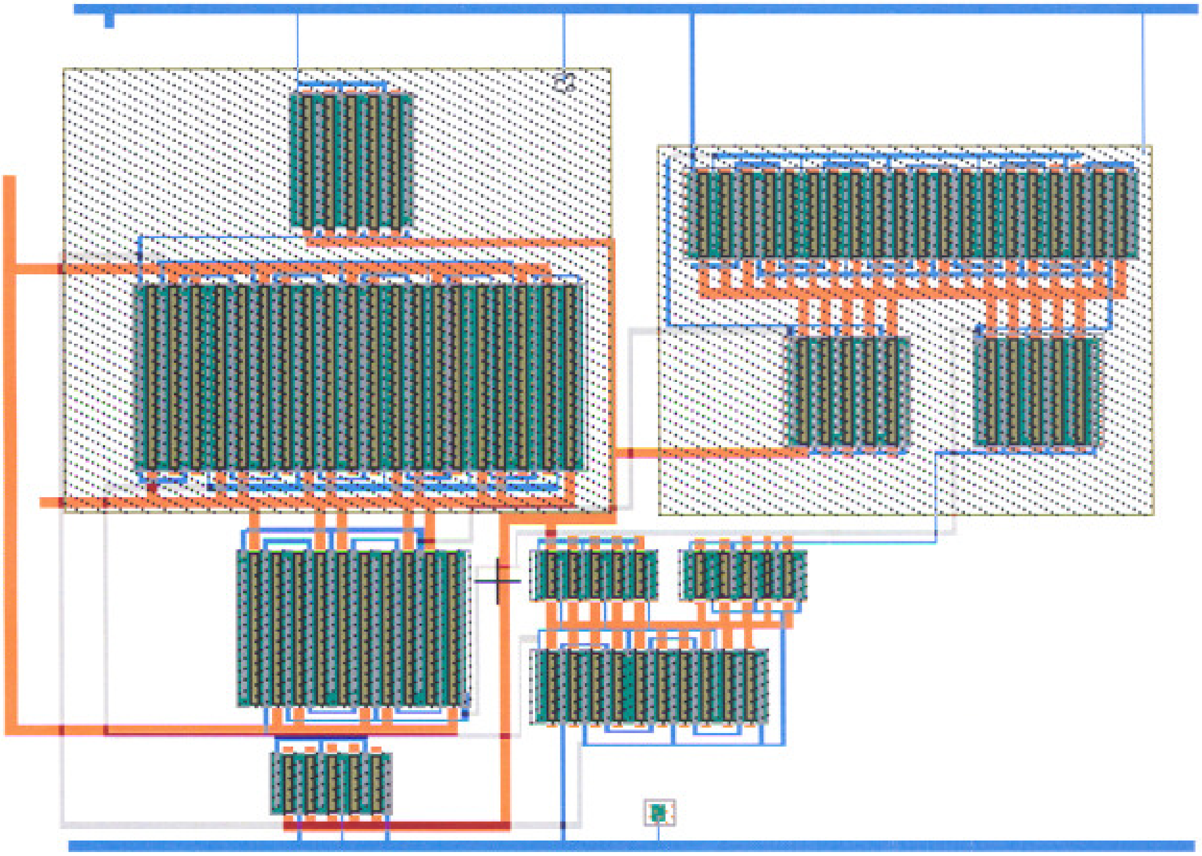
A--- M_{1A}	F--- M_4	K--- M_{6A}
B--- M_{1B}	G--- M_{7A}	L--- M_{6B}
C--- M_{2A}	H--- M_{7B}	M--- M_{8A}
D--- M_{2B}	I--- M_{5A}	N--- M_{8B}
E--- M_3	J--- M_{5B}	

The W/L ratios of transistors are

MOS	M1A	M1B	M2A	M2B	M3	M4	M5A	M5B
W/L	168	168	70	70	61	26	49	49

MOS	M6A	M6B	M7A	M7B	M8A	M8B
W/L	21	21	79	79	33	33

The length is taken 10μm. Figure 7.8 shows the obtained layout. The transistors having large W/L ratio are divided into twenty fingers like p-type differential pair. The push-pull tail transistor pair is divided into five fingers each. Two metal layers favour the interconnections. Only few metal crossings use metal 2.

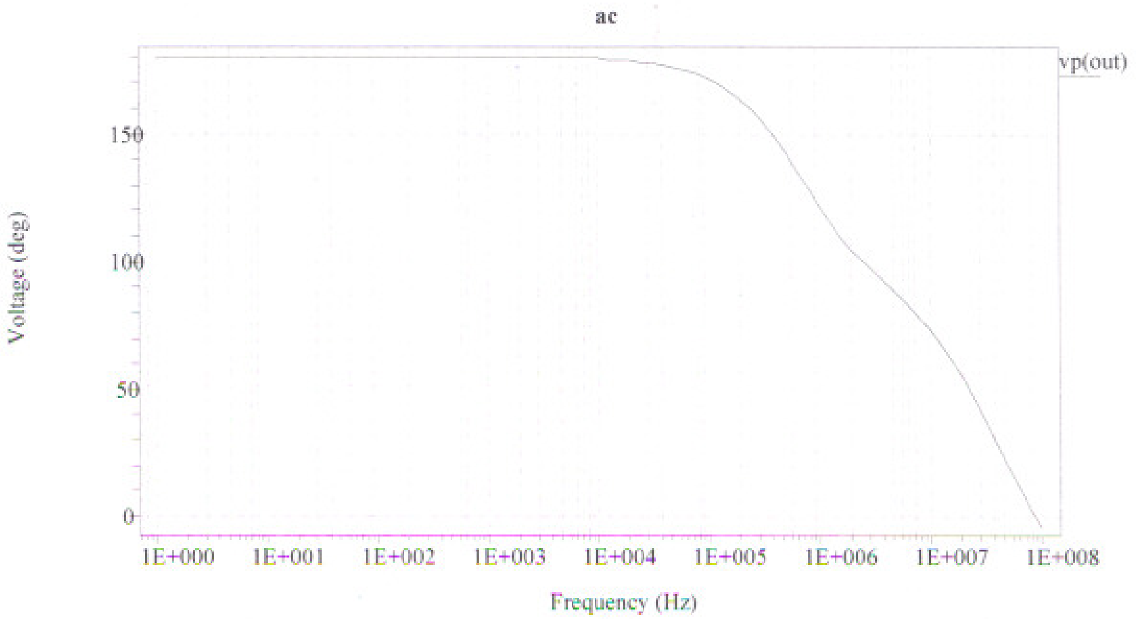


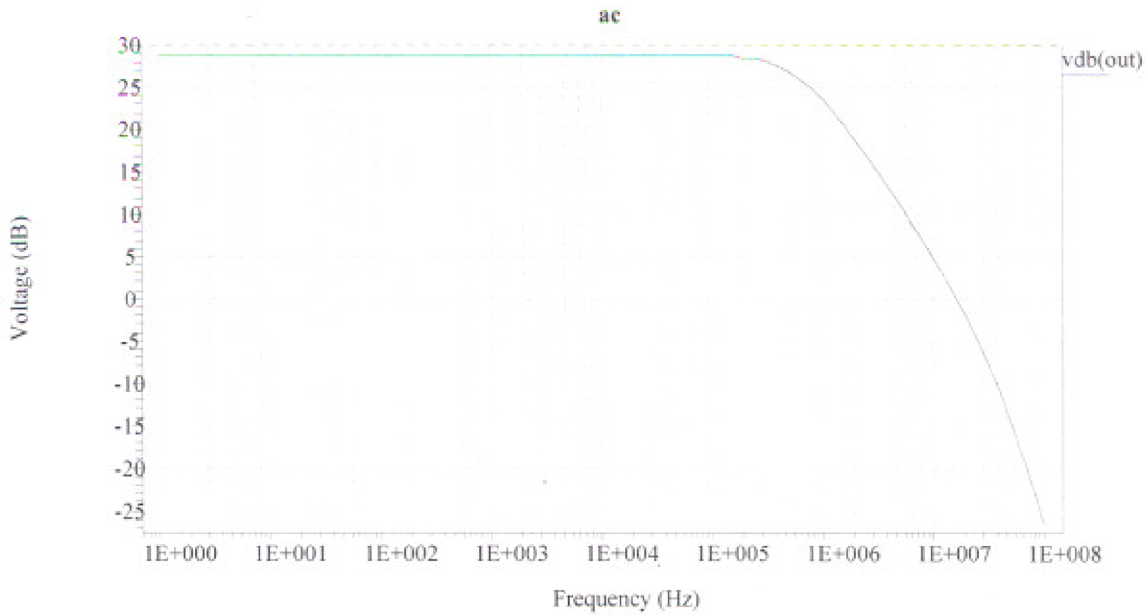
7.8 LAYOUT OF SELF BIASED COMPARATOR

RESULTS AND DISCUSSIONS

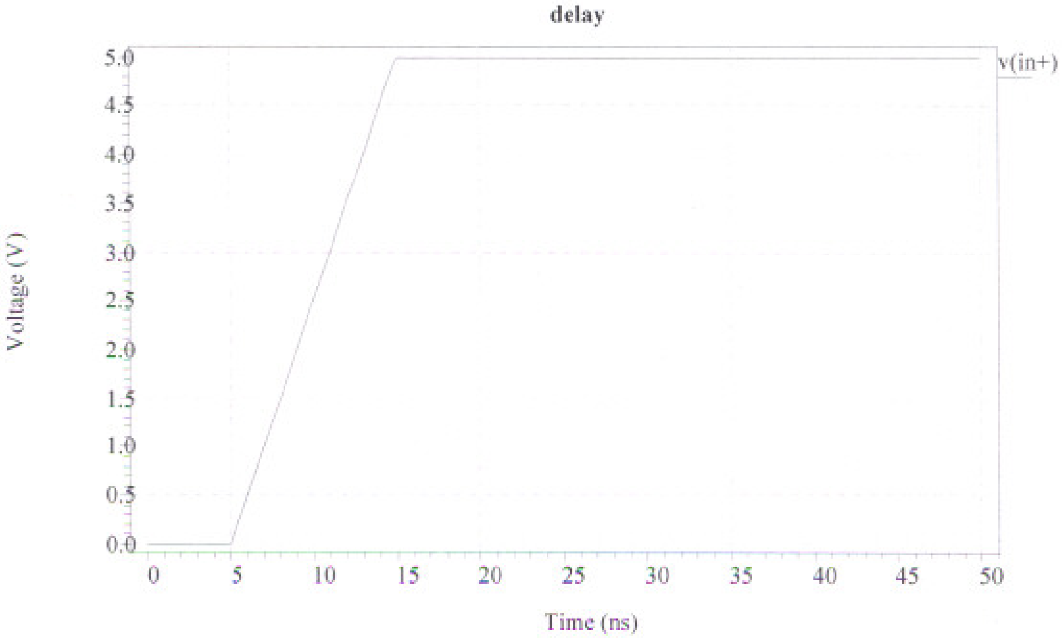
8.1 TWO STAGE OPEN LOOP COMPARATOR

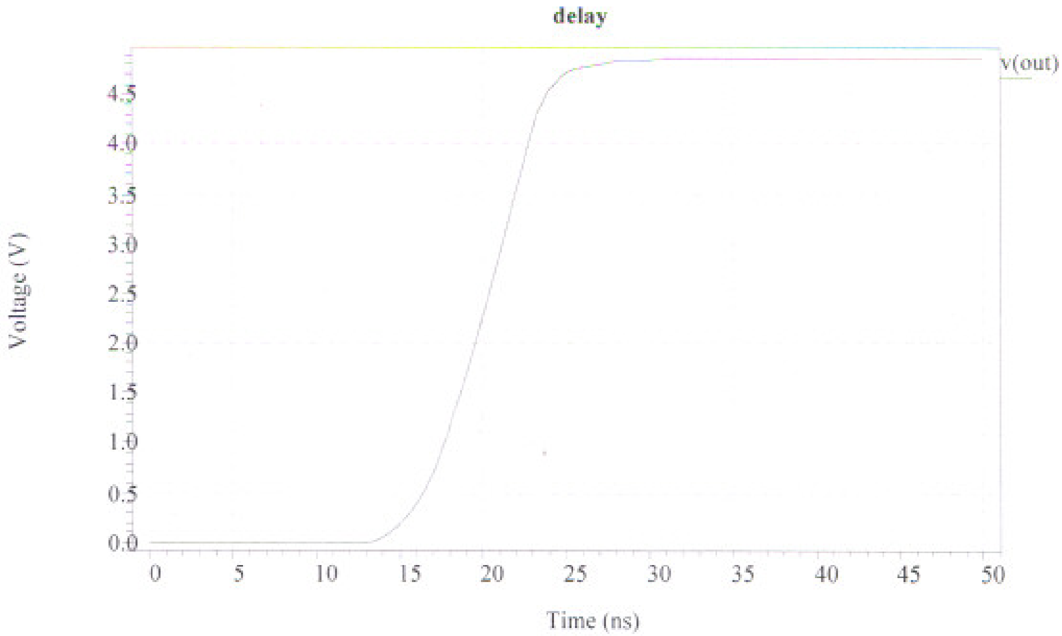
This two-stage comparator is high gain operational amplifier without compensation. The simulation results give us the gain of 32 dB with gain bandwidth (GBW) of 22.84 MHz. The matching of transistors is good i.e. 7 mV. The rising delay is approximately twice less than the falling delay. The power dissipation is quiet large i.e. 9.5 mW but average slew rate is 0.25V/ns which is very high. The minimum voltage difference that it can detect is 0.05 V. The waveforms of simulation results are as shown in following figures.



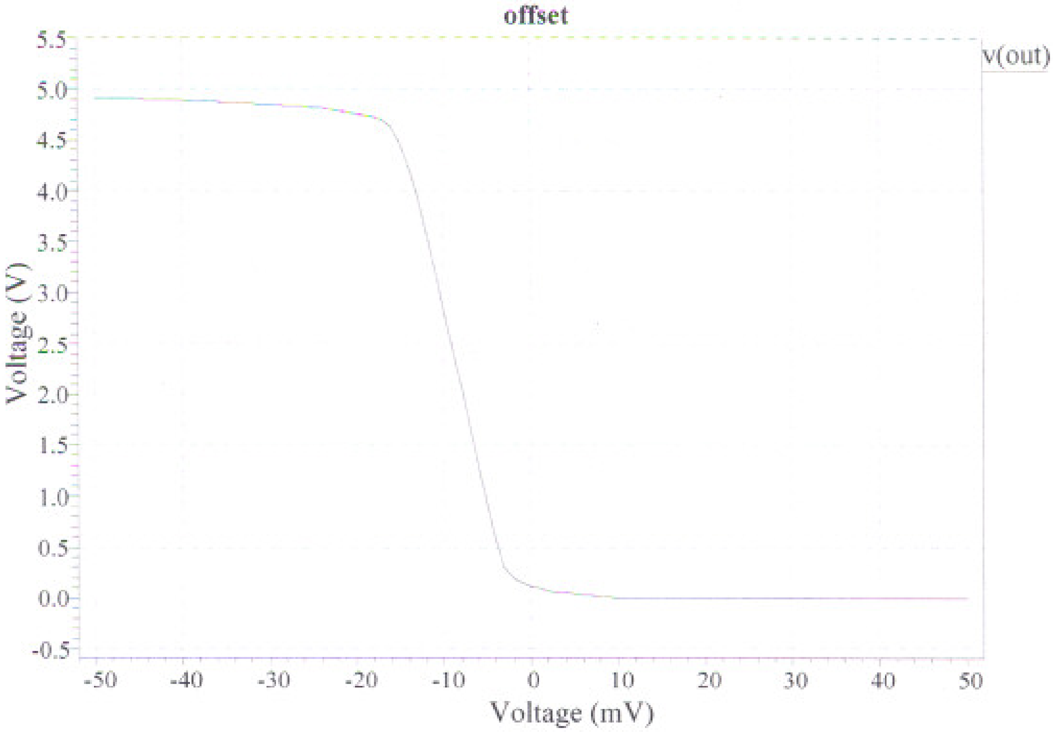


AC response of Two Stage Comparator

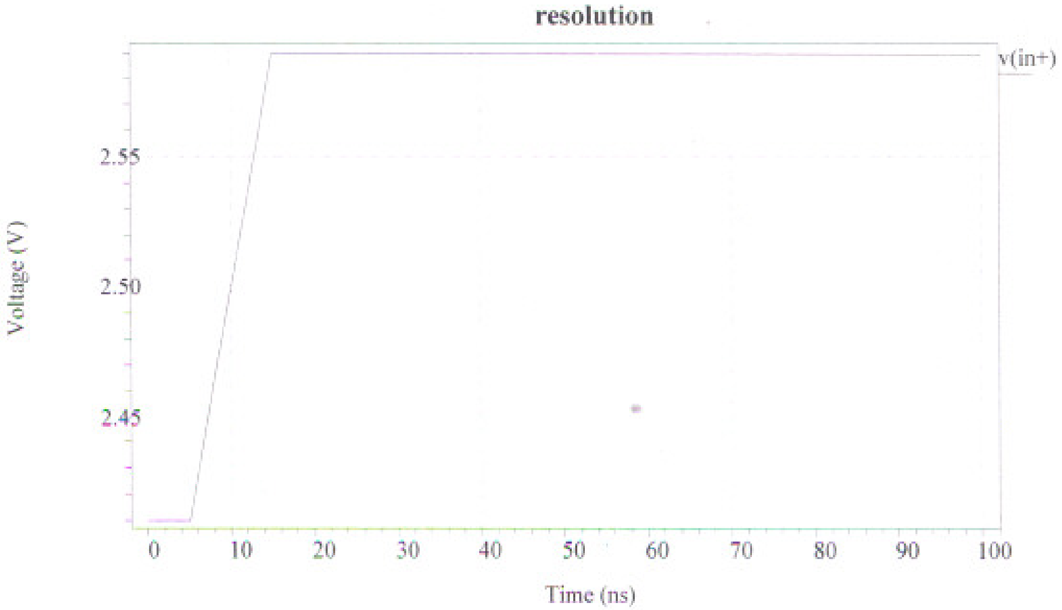


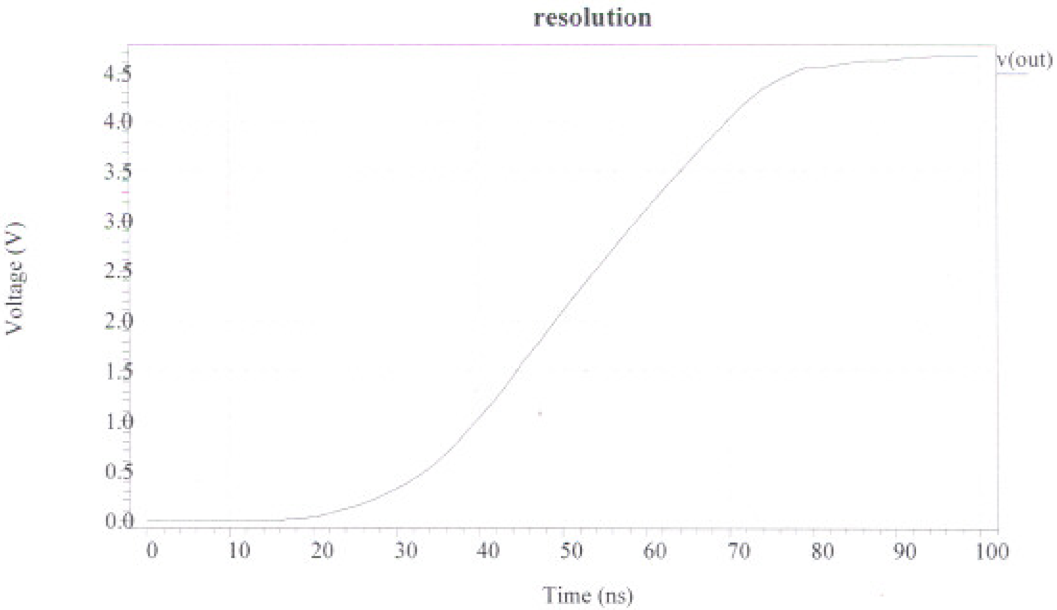


Propagation delay of two stage comparator

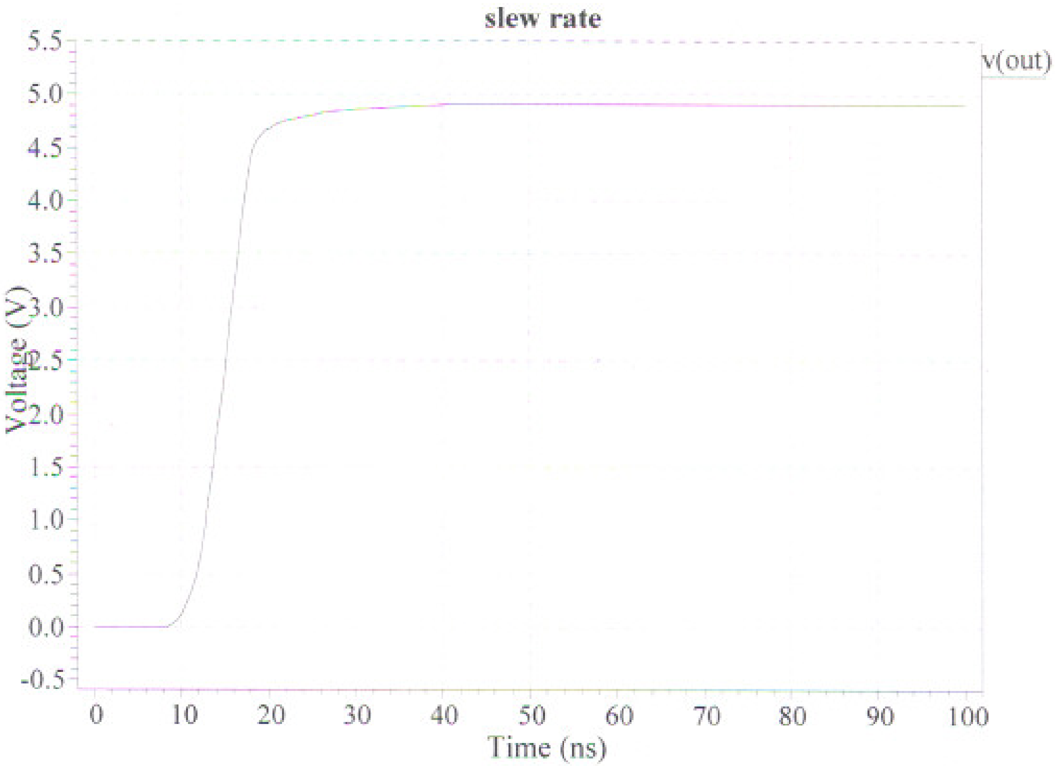


Offset of two stage comparator

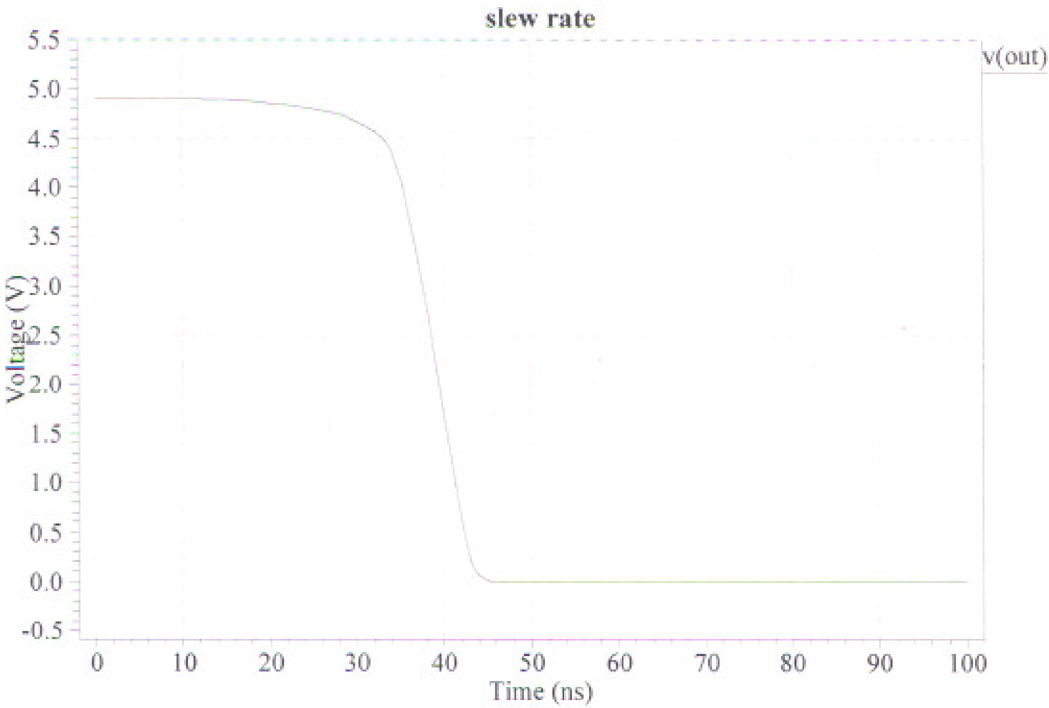




Resolution of two stage comparator



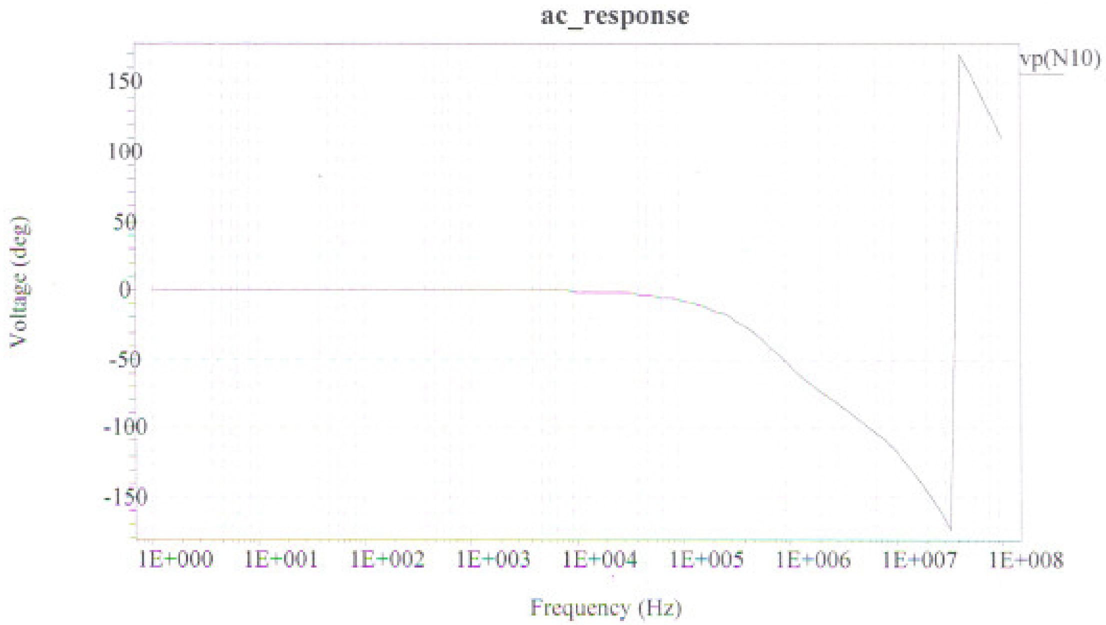
Slew rate of Two Stage comparator

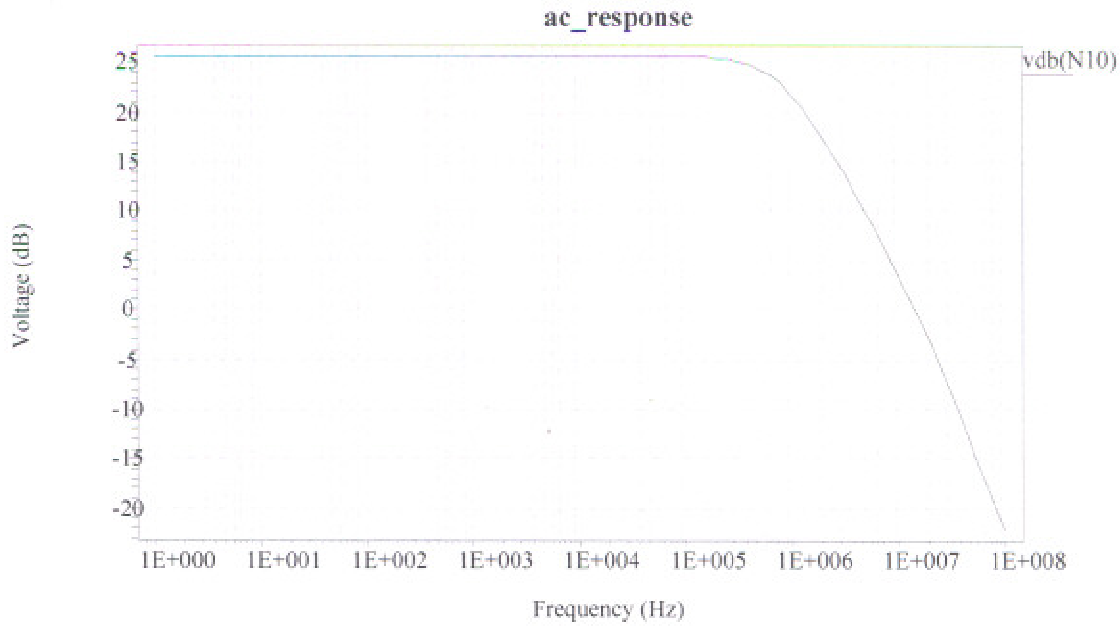


Slew rate of Two Stage comparator

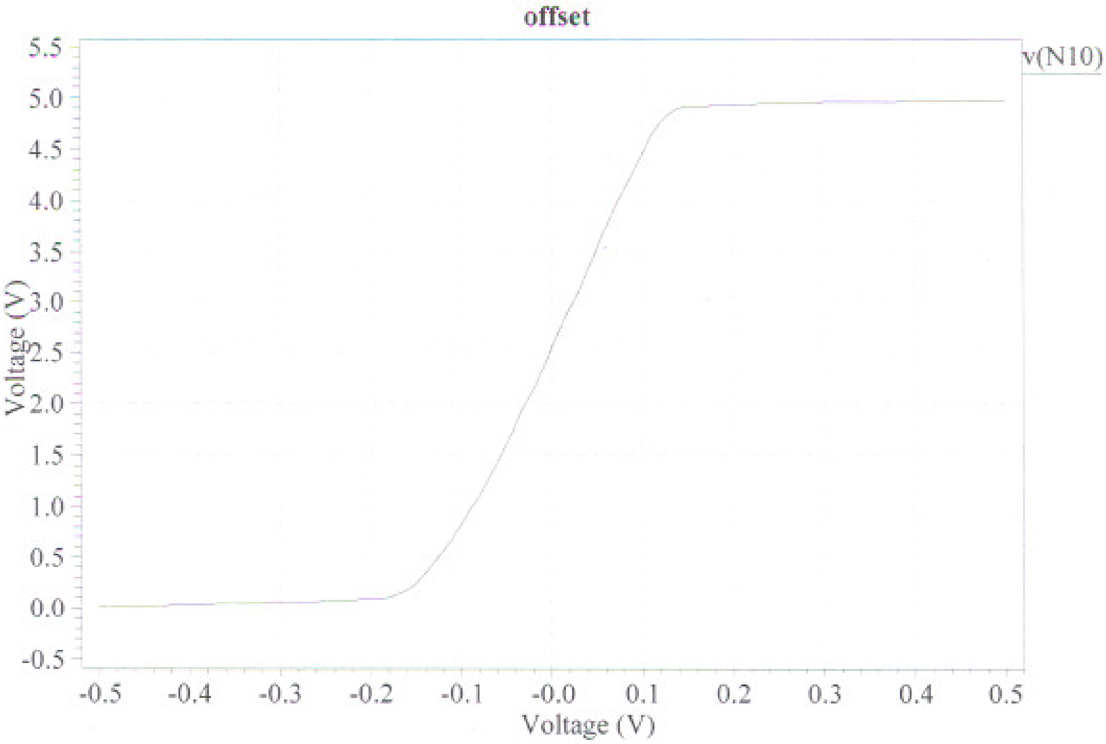
8.2 CLOCKED COMPARATOR USING BASIC LATCH

As we know from the characteristics of regenerative comparators that they are very fast with low power consumption. The simulated results have proved this. The gain of 25.7 dB with GBW 13.33 MHz is satisfactory. The main attraction of this comparator is its very high slew rate for large capacitances of 15 pF i.e. 1.74 V/ns and for load of 1 pF it is 5.8 V/ns as compared to Klinke [15]. The power consumed is just 0.3 mW at 0.11 GHz clock frequency, which is very less [16,17,26]. The resolution of this comparator is 0.02 V. The transient response of comparator shows that the preamplifier has made the input voltage difference to reach the desired value within 2 ns. The simulation results are as shown in figures followed.

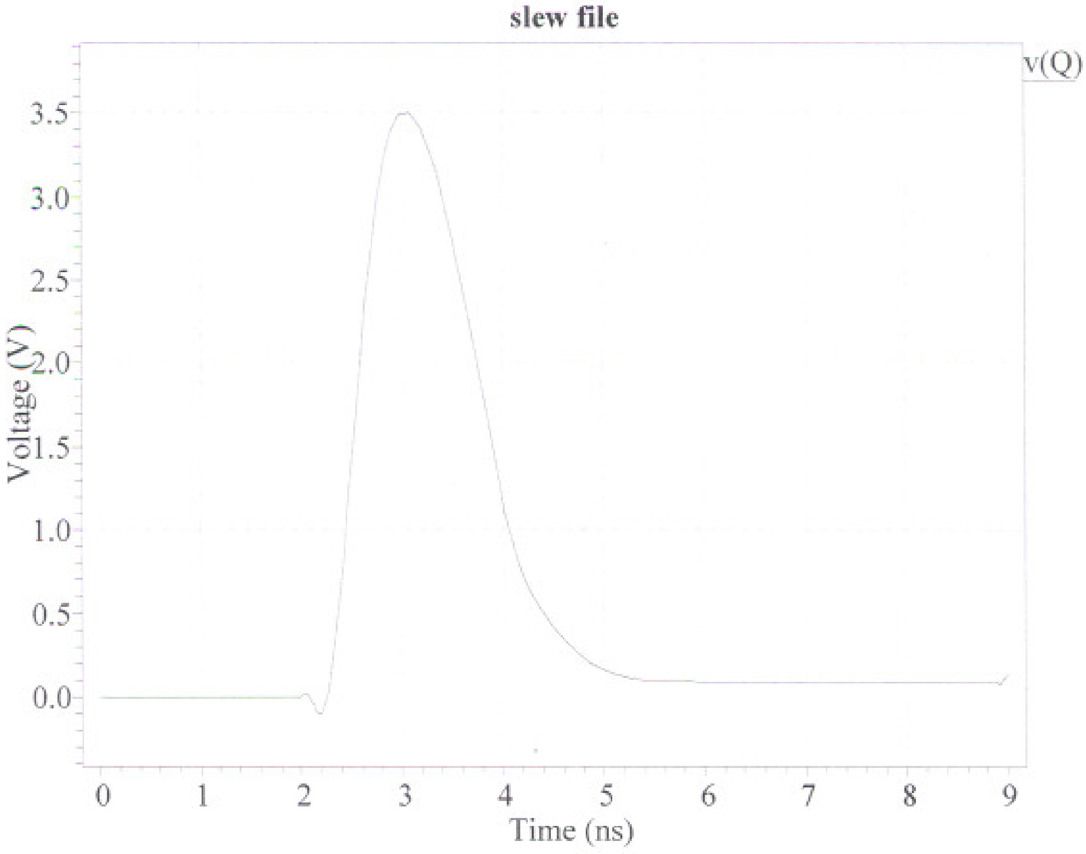




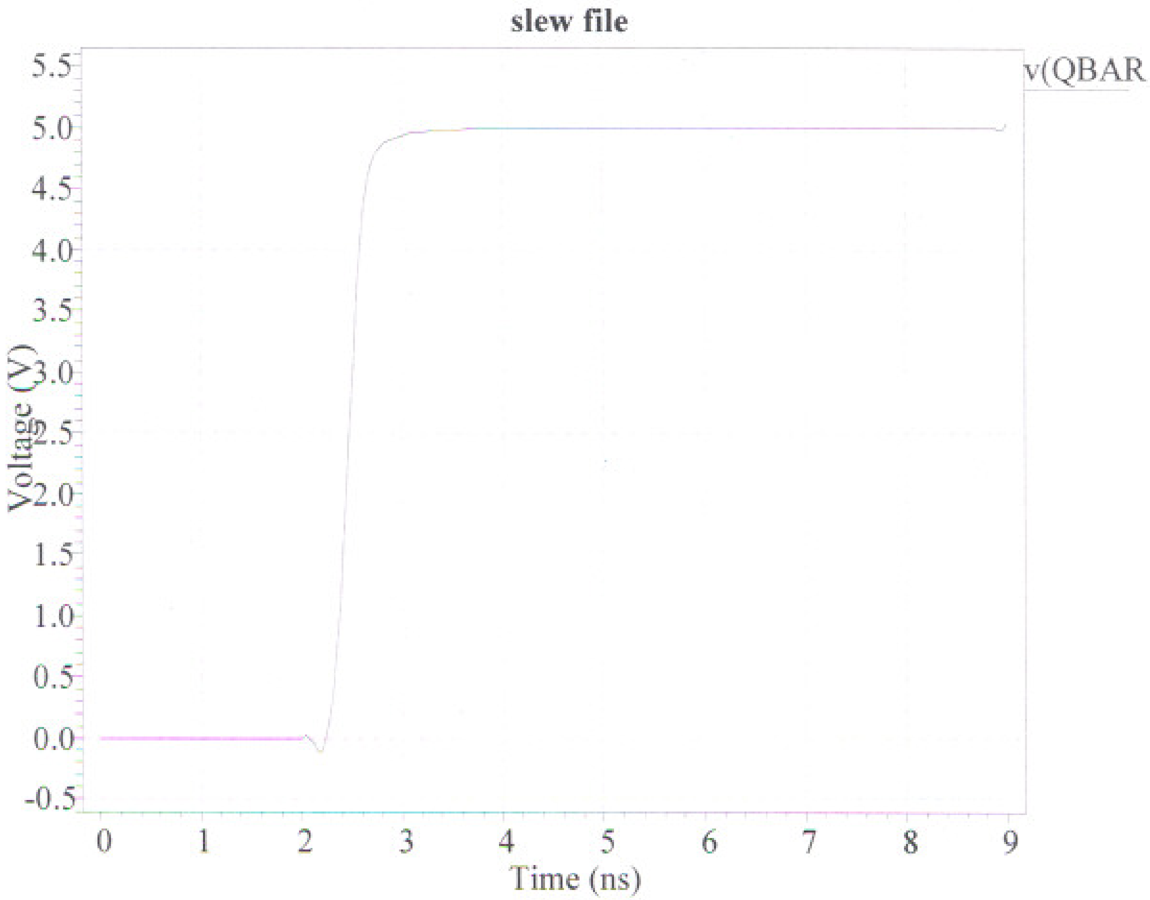
AC response of Clocked comparator



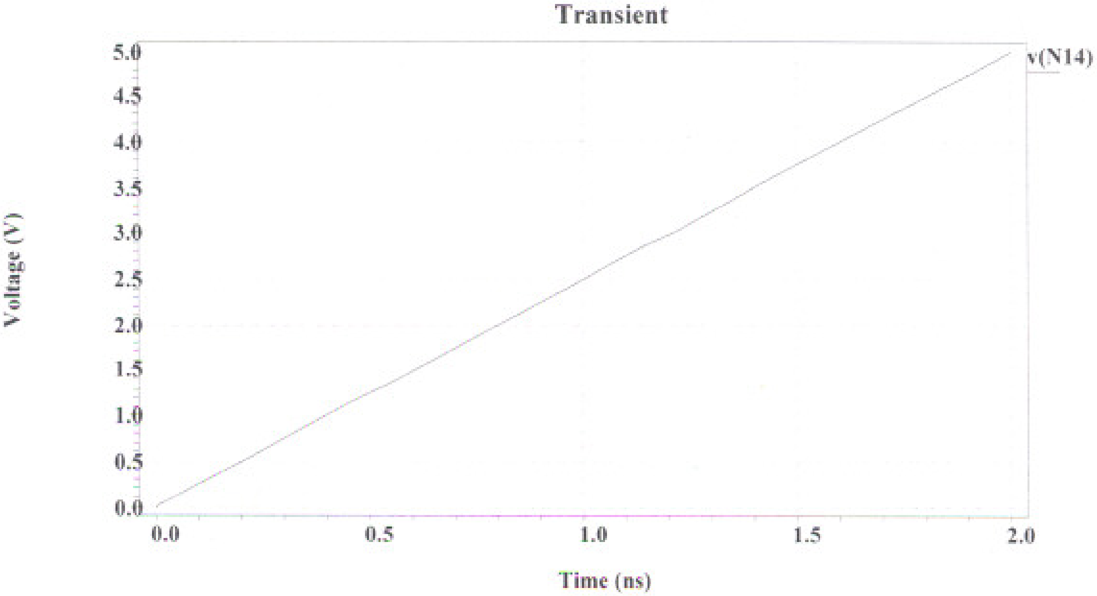
Offset of Clocked comparator

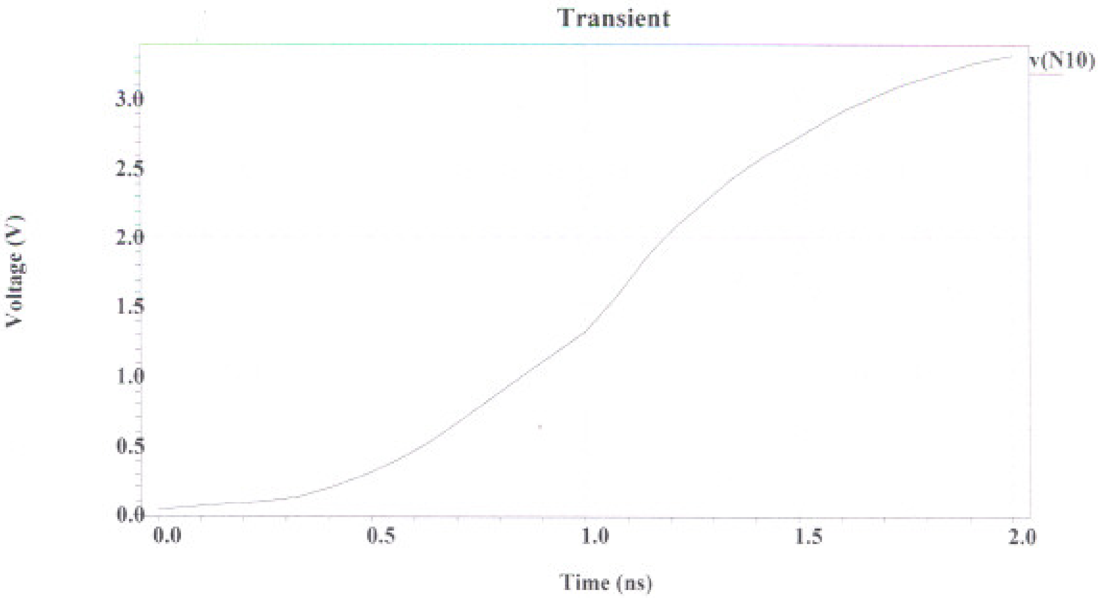


Slew rate of Clocked comparator



Slew rate of Clocked comparator

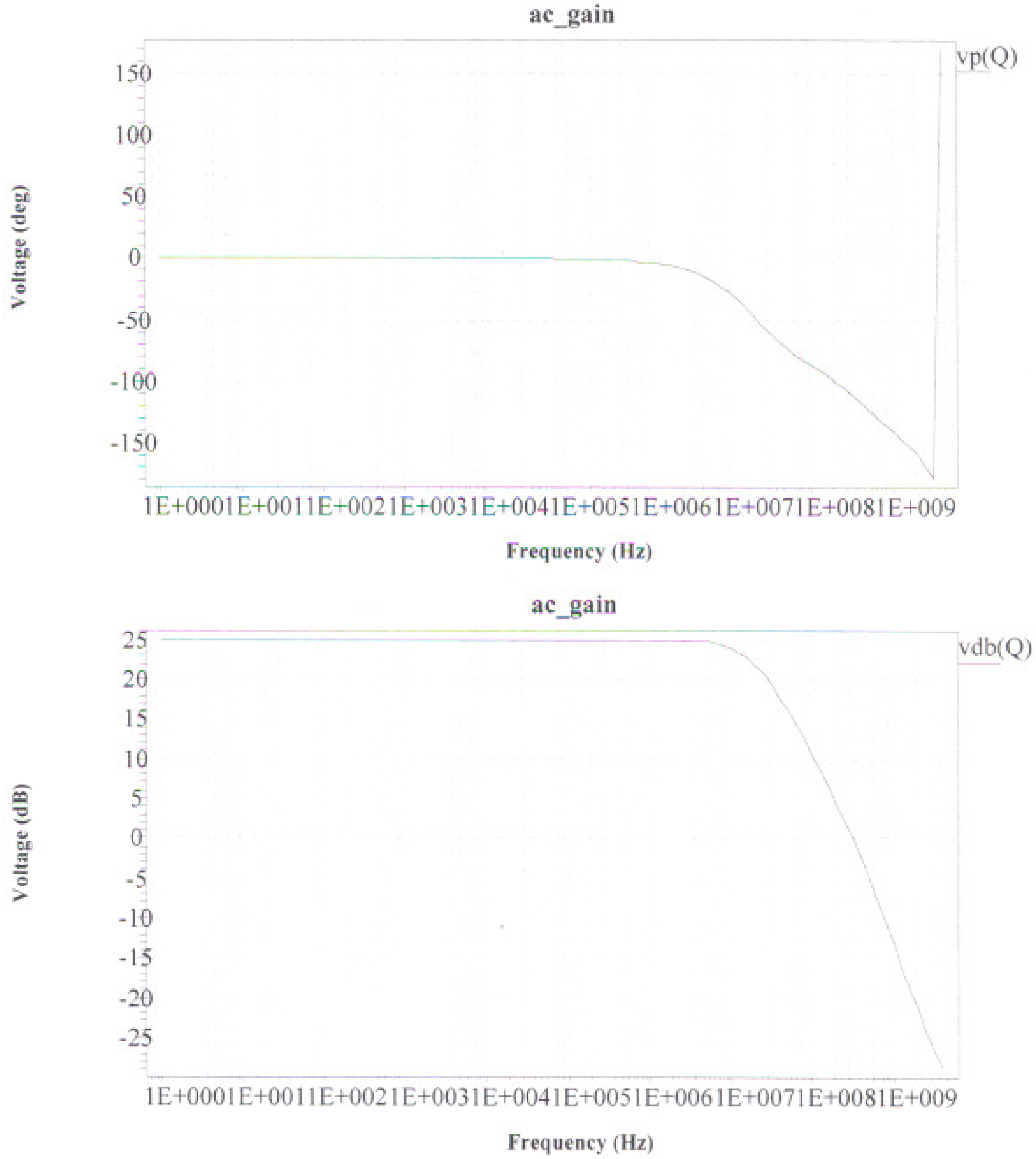




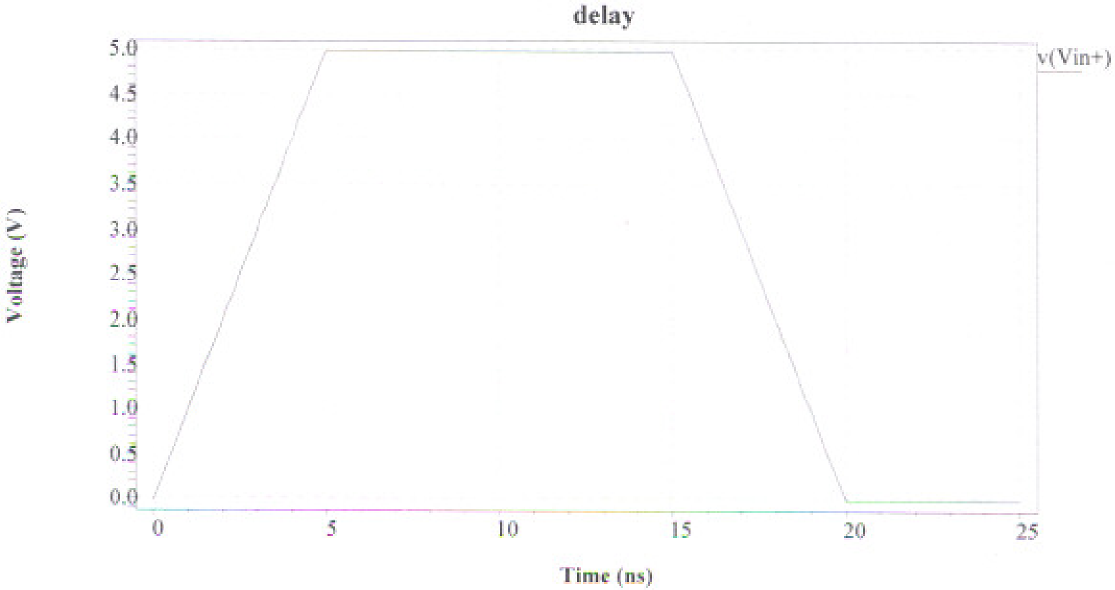
Transient response of Clocked comparator

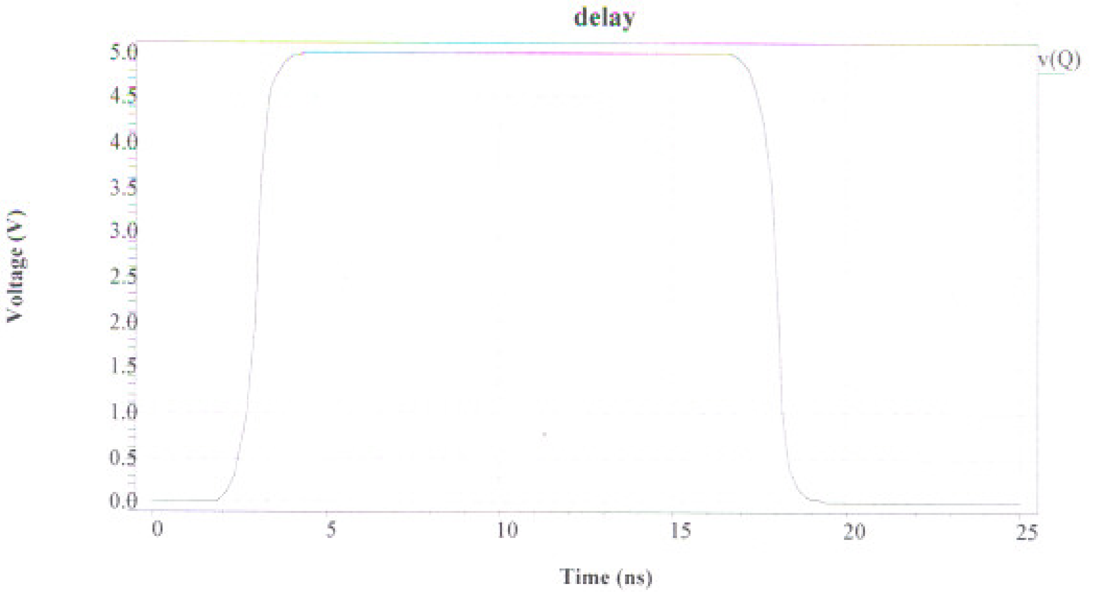
8.3 SELF-BIAS COMPARATOR

The gain achieved is same as that of clocked comparator but the unity gain bandwidth (GBW) is very high i.e. 314 MHz so it can work up to this range of frequencies. Also phase margin is 70.3 degree, which is very high so it is a very stable circuit. The best thing is it's very less delay i.e. 0.42 ns which is very less as compared to [6,19,26]. The power dissipation is quiet large i.e. 27.8 mW but average slew rate is 0.7 V/ns which is very high. The data analysis of self-biased comparator is summarized in table 4. The simulation results are as shown in figures followed.

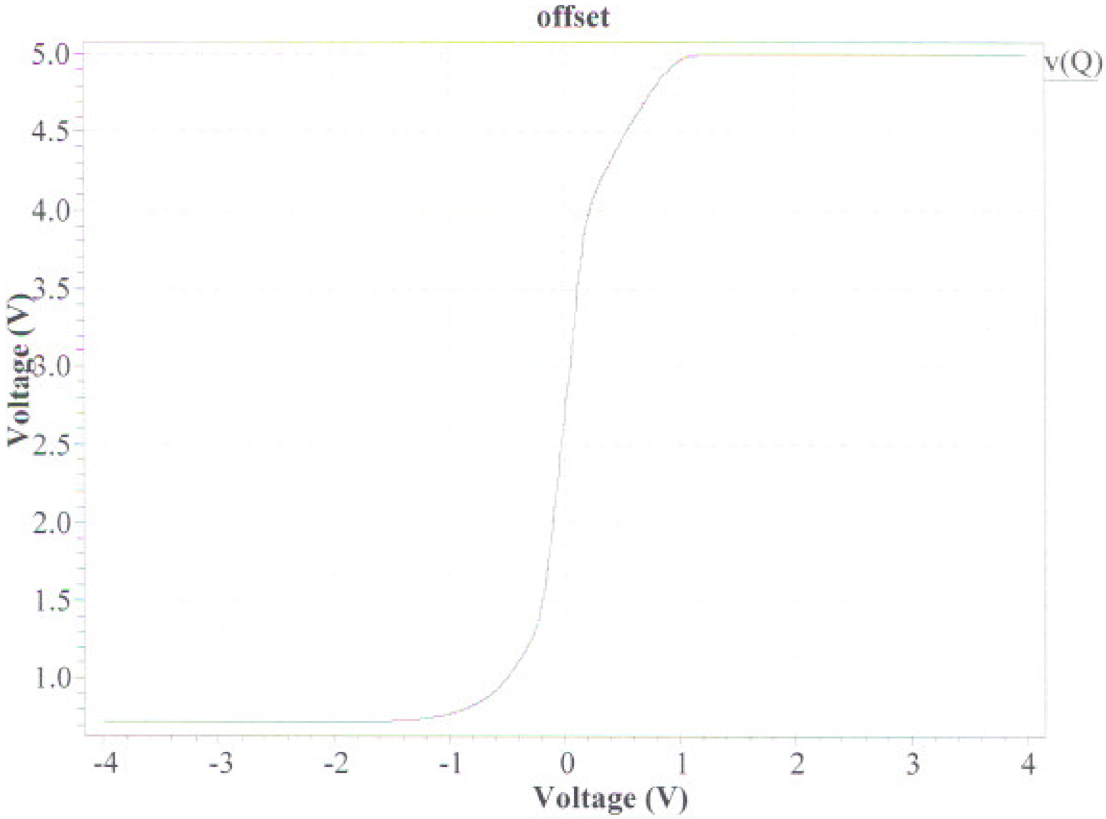


AC response of Self-Biased comparator

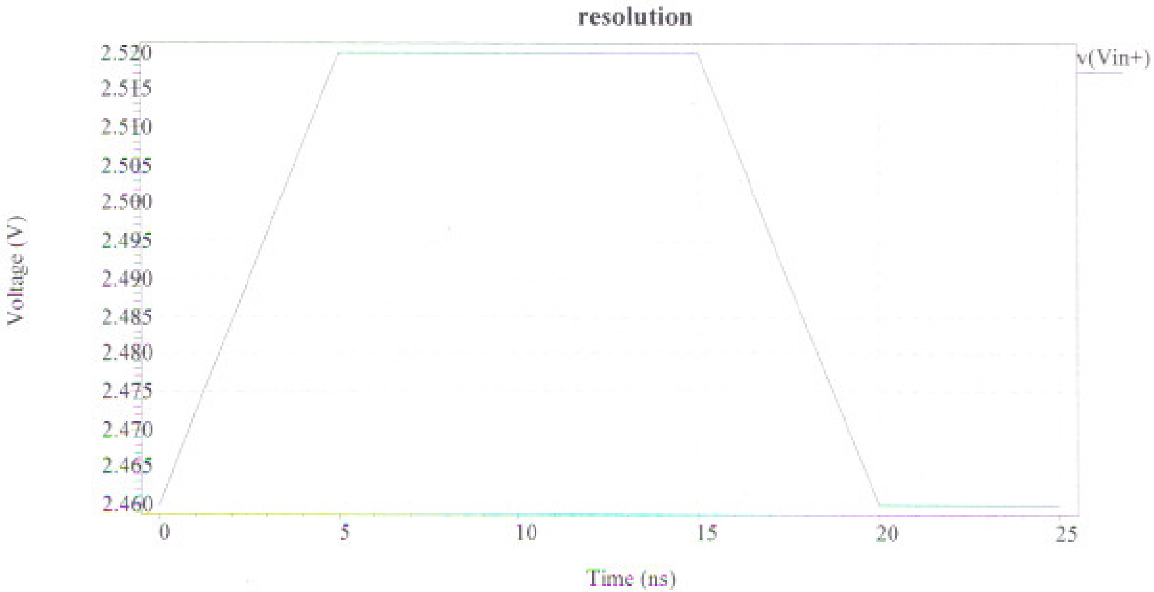


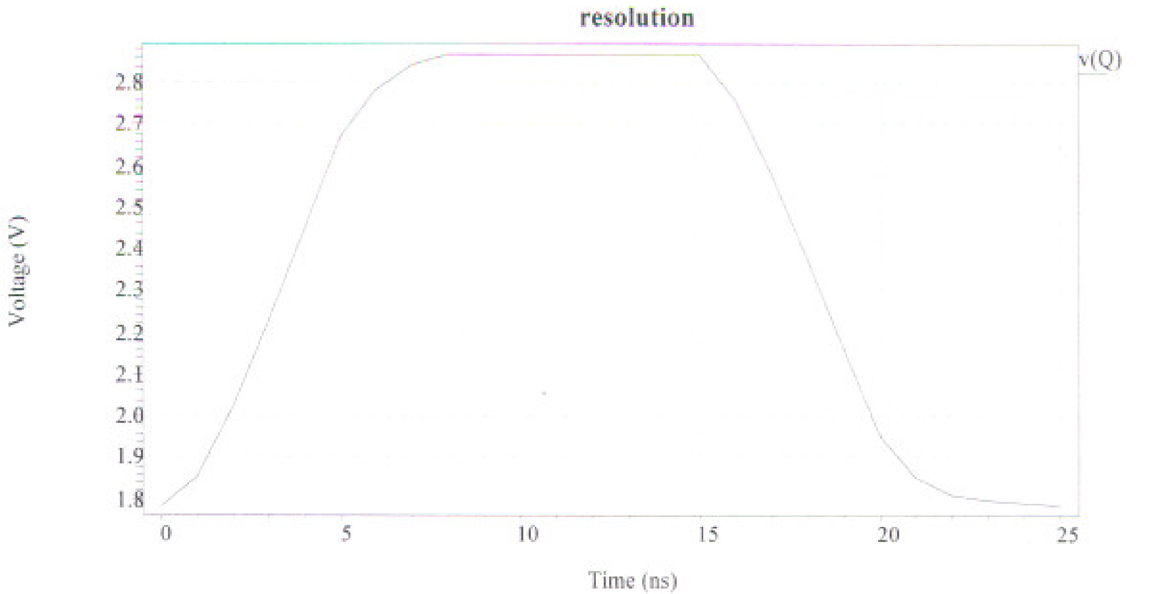


Propagation Delay of Self-Biased comparator

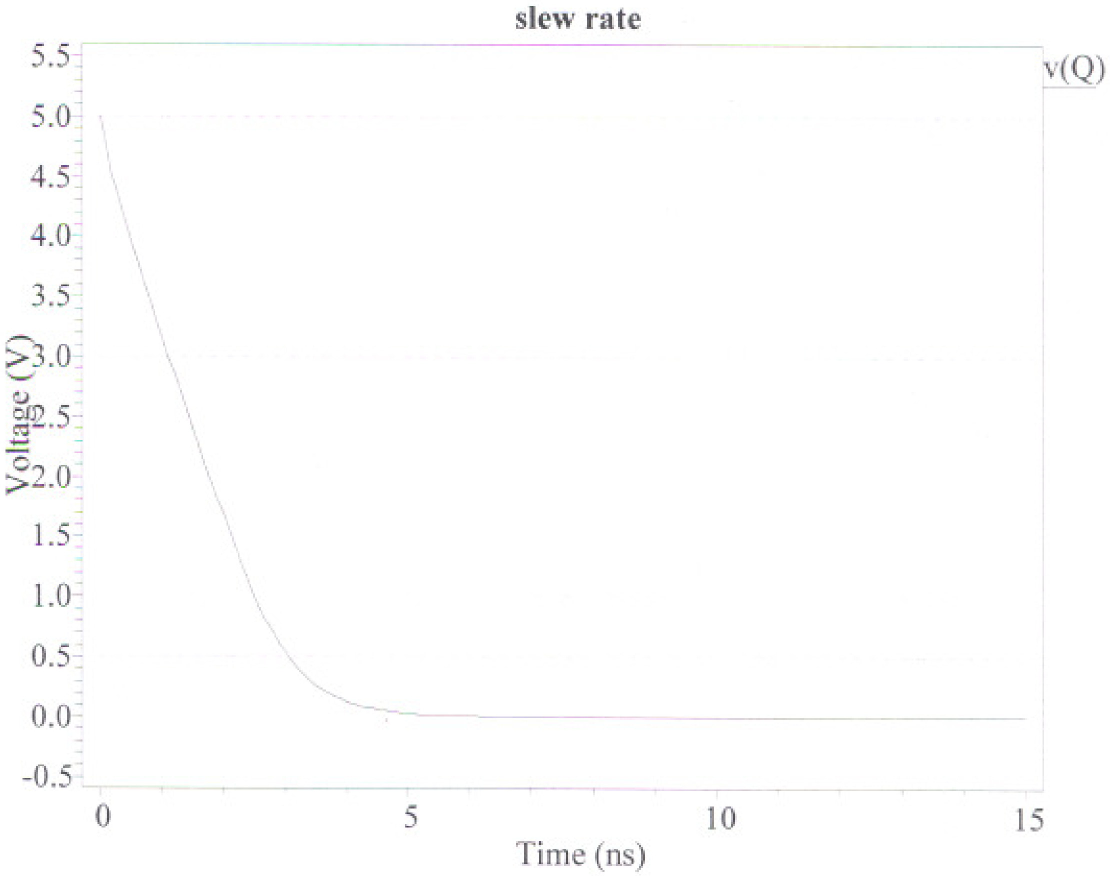


Offset of Self-Biased comparator

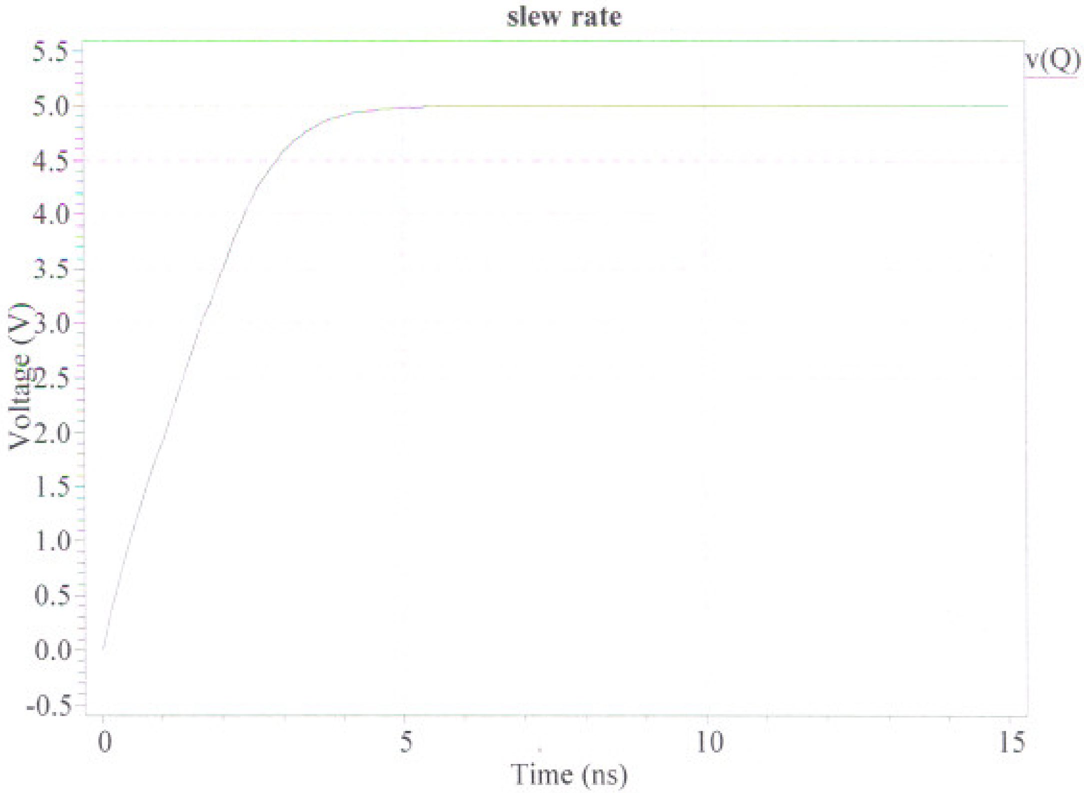




Resolution of Self-Biased comparator



Slew Rate of Self-Biased comparator



Slew Rate of Self-Biased comparator

Specifications → Parameters ↓	Set 1	Set 2	Set 3	Set 4	Set 5
Offset (V)	-0.02	-0.01	-0.06	0.01	0.02
Resolution (V)	0.2	0.04	0.01	0.02	0.03
Rising Delay (ns)	0.59	0.8	1	0.54	0.42
Falling Delay (ns)	0.68	0.9	1.27	0.58	0.46
Gain (dB)	24.77	35.5	38.88	33.02	25.34
GBW (MHZ)	256.48	246.7	621.73	533.38	314
Phase Margin (Degree)	73.4	59.3	30.57	45.6	70.3
Rising Slew Rate with 10pF load (V/μs)	72.62	28.42	132.1	132.4	112.3
Falling Slew Rate with 10pF load (V/μs)	71.4	26.4	128.9	128.9	107.4

Table 4

This data analysis is done with following specification sets:

Set 1: SR = 10 V/μs, GB = 10 MHz, C_L = 10 pF
Set 2: SR = 1 V/μs, GB = 10 MHz, C_L = 10 pF
Set 3: SR = 10 V/μs, GB = 60 MHz, C_L = 10 pF
Set 4: SR = 10 V/μs, GB = 25 MHz, C_L = 10 pF
Set 5: SR = 10 V/μs, GB = 10 MHz, C_L = 15 pF

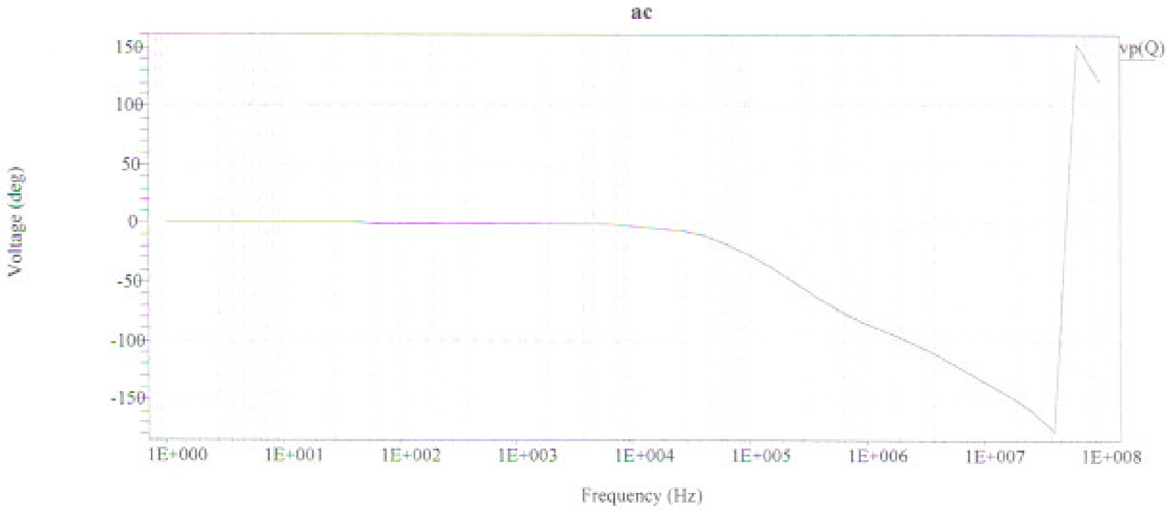
The comparison of three comparators has been summarized in table 5.

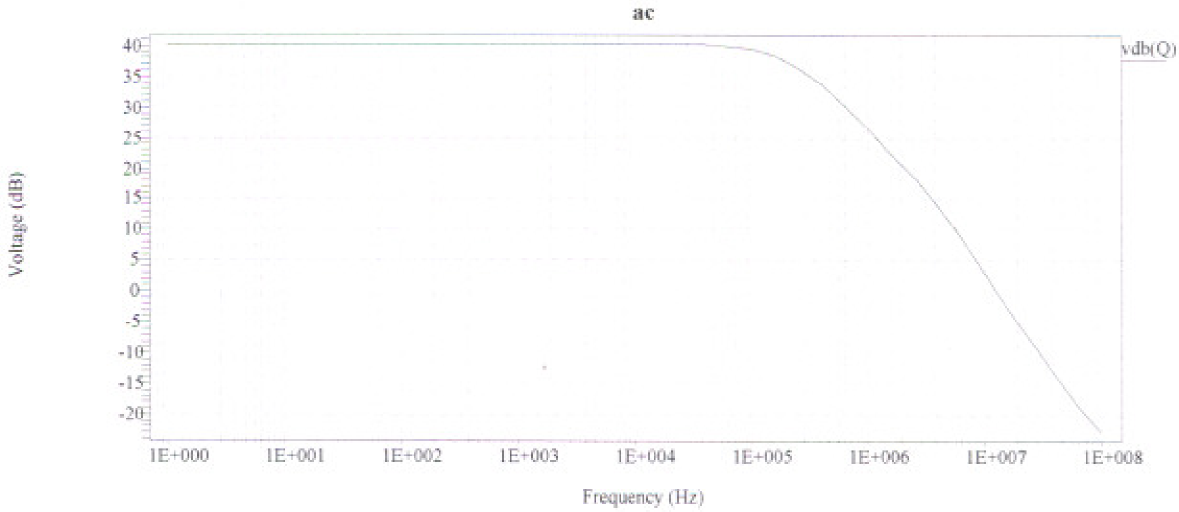
Comparator/→ ↓ Parameters	Two-stage comparator	Clocked comparator using latch	Self-biased comparator
Offset (V)	-0.007	-0.09	0.02
Resolution (V)	0.05	0.02	0.03
Rising Delay (ns)	10.3	-	0.42
Falling Delay (ns)	23.4	-	0.46
Gain (dB)	32	25.7	25.34
GBW (MHZ)	22.84	13.33	314
Phase Margin (Degree)	50	51.72	70.3
Rising Slew Rate with 1pF load (V/ns)	0.247	5.844	0.721
Falling Slew Rate with 1pF load (V/ns)	0.300	10.74	0.762
Power dissipation (mW)	9.5	0.3	27.8

Table 5

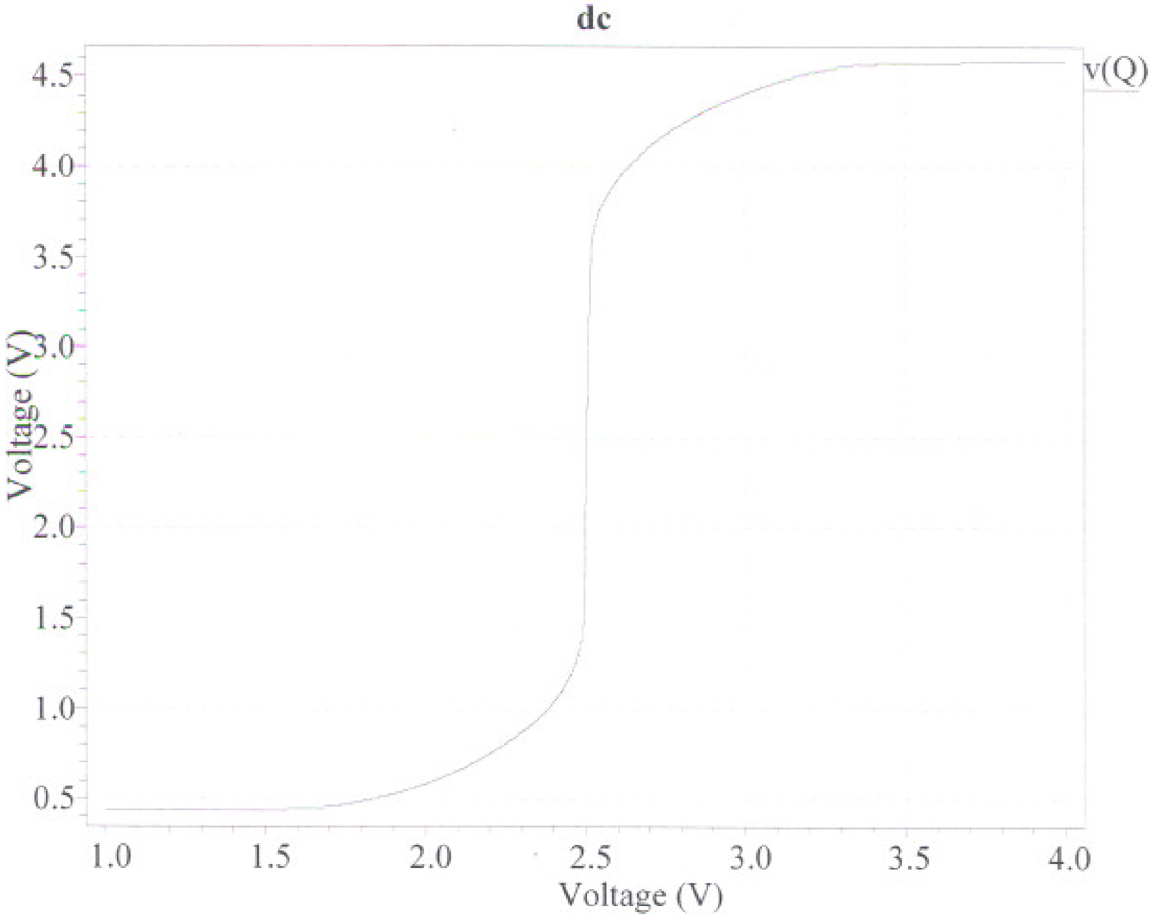
8.4 LAYOUT

The layout of self-biased comparator is developed and simulation files are extracted. The simulations of extracted files give us the gain of 40.38 dB with phase margin of 30 degree. The gain bandwidth is 21.2 MHz. As we can see gain has increased and GBW has decreased as compared to schematic simulation results. The output swing is from 0.2 V to 4.6 V. Layout resulted in very good matching giving offset of 1 mV. Slew rate has also decreased i.e. from low to high output it is 80 V/μs and from high to low output it is 116.5 V/μs.

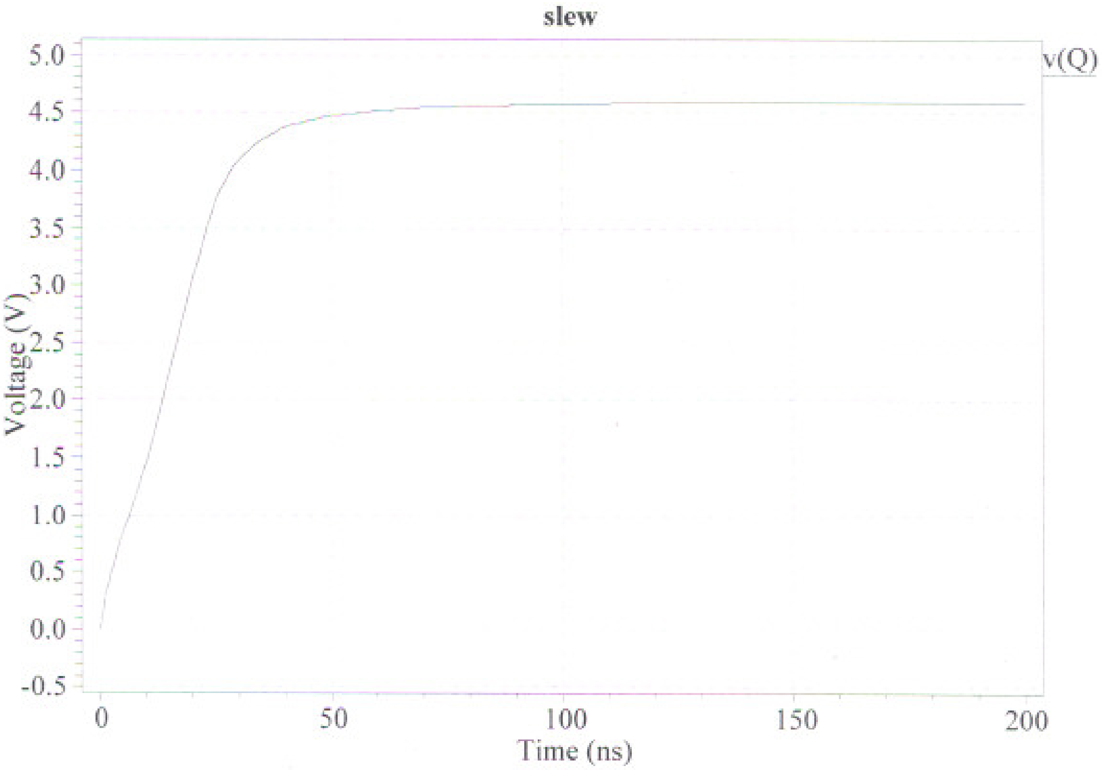

ac
vp(Q)
Voltage (deg)
150
100
50
0
-50
-100
-150
1E+000
1E+001
1E+002
1E+003
1E+004
1E+005
1E+006
1E+007
1E+008
Frequency (Hz)


ac
vdb(Q)
Voltage (dB)
40
35
30
25
20
15
10
5
0
-5
-10
-15
-20
1E+000
1E+001
1E+002
1E+003
1E+004
1E+005
1E+006
1E+007
1E+008
Frequency (Hz)

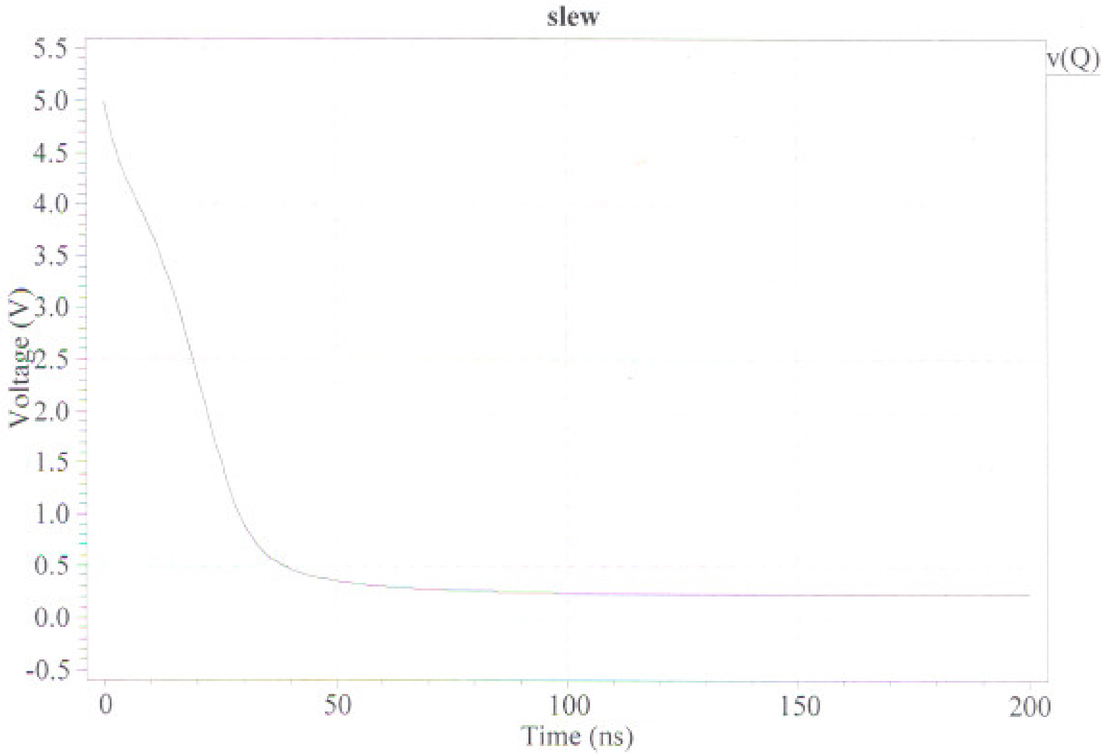
AC response


dc
v(Q)
4.5
4.0
3.5
3.0
2.5
2.0
1.5
1.0
0.5
Voltage (V)
1.0
1.5
2.0
2.5
3.0
3.5
4.0
Voltage (V)

DC response


slew
v(Q)
5.0
4.5
4.0
3.5
3.0
2.5
2.0
1.5
1.0
0.5
0.0
-0.5
Voltage (V)
0
50
100
150
200
Time (ns)

Slew rate


slew
v(Q)
5.5
5.0
4.5
4.0
3.5
3.0
2.5
2.0
1.5
1.0
0.5
0.0
-0.5
Voltage (V)
0
50
100
150
200
Time (ns)

Slew rate

9.1 CONCLUSION

The comparator design procedures have been developed for three different architectures namely: Two stage open loop comparator, Clocked comparator using basic latch and self-biased comparator. The different parameters were calculated for the three comparators, which are summarized in table 5.

We concluded that the values match directly to the characteristics defined for each comparator architecture. The open loop two stage comparator has achieved highest gain of 32 dB and the offset voltage is minimum. Whereas the clocked comparator using basic latch is fastest, which can charge, or discharge a 1 pF capacitance with slew rate of 5.8 V/ns. Also very high slew rate for large capacitances have been achieved. The power consumption of this comparator is minimum, which is only 0.3 mW. The self-biased comparator has minimum delay, which is of the order of nanoseconds i.e. 0.42 ns that is the main attraction. It has achieved maximum gain bandwidth. So it can work for highest range of frequencies. From power consumption and speed point of view the comparator using the regenerative circuit is best implementation. Whereas looking at all parameter values one can conclude that overall two-stage open loop comparator is the best implementation.

A layout has been developed for self-biased comparator. The above-mentioned parameters have also been calculated from the layout by extracting it. These parameters are satisfactory but not similar. Gain has increased but the unity gain bandwidth and slew rate has reduced as compared to the values, which we get from the schematic simulation.

9.2 FUTURE SCOPE

- Other comparator configurations can be taken for designing considering power as the main constraint.
- Layout can be further improved to remove the discrepancy.

1) Allstot D. J., "*A precision variable-supply CMOS comparator*", IEEE Journal of Solid State Circuits, vol. SC-17, no. 6, pp. 1079-1080, 1982.

2) Baker R.J, Li H.W, and Boyce D.E, " *CMOS Circuit Design, Layout , and Simulation*", Piscataway, NJ: IEEE Press, 1998, Chap, 26.

3) Bazes M., " *Two Novell Full Complementary Self Biased Differential Amplifier*", IEEE Journal of Solid State Circuits, Vol. 26, No. 2,pp. 165-168, February 1991.

4) Black W. C., "*High speed CMOS A\D conversion technique*", Ph.D. dissertation, Univ. of Calif., Berkeley, Nov. 1980.

5) Chong, C.P and Smith, K.C., " *A high resolution CMOS comparator*", Int. J Electronics, Vol. 64, pp 409-415, Mar. 1988.

6) Fisher J. A. and Koch R., "*A Highly Linear CMOS Buffer Amplifier*", IEEE Journal of Solid State Circuits, Vol. SC-22, No.3, June 1987.

7) Geiger R. L., Allen P. E. and Strader N. R., "*VLSI Design Techniques for Analog and Digital Circuits*", McGraw-Hill Publishing Company, 1990.

8) Gray P. R and Meyer, "*Analysis and design of Analog Integrated Circuits*" ,J. Wiley & Sons, New York, 1993.

9) Gray P. R., Hurst P. J., Lewis S. H. and Meyer R. G., "*Analysis and Design of Analog Integrated Circuits*", Fourth Edition, John Wiley & Sons, 2001.

10) Gregorian R., "*Introduction to CMOS OP-AMPS and Comparators*", J. Wiley and Sons, New York, 1999.

11) Heydari Payam, Mohavavelu Ravi, " *Design of Ultra High-Speed CMOS CML buffers and Latches*", Department of Electrical and Computer Engineering, University of California.

12) Hosticka B. J., " *Dynamic CMOS amplifiers*", IEEE J. Solid-State Circuits, vol. SC-15, pp. 887-894, Oct. 1980.

13) Johns D. A. and Martin K., " *Analog Integrated Circuit Design*", J. Wiley & Sons, New York, 1997.

14) Kang Sung-Mo, Leblebici Yusuf, " *CMOS Digital Integrated Circuits, Analysis and design",* Tata McGraw-Hill Edition 2003, Third Edition.

15) Klinke R., Member, IEEE, Hosticka B. J., Senior Member, IEEE and Peleiderer H. J., Senior Member, IEEE, "*A very-high Slew-rate CMOS operational Amplifier*", IEEE Journal of Solid State Circuits, Vol. 24, No.3, June 1989.

16) Kurnamoto T. et al., " *A 8-bit high speed CMOS A/D converter",* IEEE J. Solid State Circuits, Vol. SC-21, pp-976-982, Dec. 1986.

17) Laksmikumar K. R., Hadaway R. A., and Copeland M. A., " *Characterization of modeling of mismatch in MOS transistors for precision analog design",* IEEE J. Solid State Circuits, vol SC-21, pp. 1057-1066, Dec. 1966.

18) Maloberti Franco, "*Analog Design For CMOS VLSI Systems*", KLUWER academic Publisher, Boston/ Dordrecht/ London, 2001.

19) McCarroll Benjamin J., Sodini Charls D., Lee Hae-Seung, " *A High Speed CMOS Comparator For Use In An ADC*", IEEE Journal of Solid State circuits, Vol. 23, No.1, February 1988.

20) Philip Allen E., Holberg Douglas R., " *CMOS Analog Circuit Design* ", Oxford University Press, London, 2003, Second Edition.

21) Razavi B. and Wooley B. A., " *Design Techniques for high-speed, high-resolution comparators",* IEEE Journal of Solid State circuits, Vol. 27, pp.1916-1926, 1992.

22) Razavi B., " *Prospects of CMOS Technology for High-Speed Optical Communication Circuits*", IEEE J. Solid-State Circuits, vol. 37, No. 9, pp. 1135-1145, Sept. 2002.

23) Razavi Behzad, " *Design of Analog CMOS Integrated Circuits",* Tata McGraw-Hill Edition, Edition 2002.

24) Scott J. W., Lee W. L., Giancarlo C. H., and Sodini C.G., " *CMOS implementation of an immediately adaptive delta modulator"*, IEEE Journal of solid-state circuits, vol.sc-21, pp. 1088-1095, Dec 1986.

25) Wu Jieh-Tsorng and Wooley B.A., " *A 100 MHz pipelined CMOS comparator"*, IEEE Journal of Solid State Circuits, Vol. 23, pp.1379-1385, 1998.

26) Yin G.M, Eynde F. Op', and Sansen W., "*A High Speed CMOS Comparator with 8-b Resolution*", IEEE J. Solid State Circuits, Vol. 27, No.2, Feb. 1992.

27) Yukawa A., " *A CMOS 8-bit high speed A/D converter IC"*, IEEE J. Solid State Circuits, Vol. SC-20, pp-775-779, June 1985.

APPENDIX

DESIGN OF CLOCKED COMPARATOR USING BASIC LATCH

Jyoti kedia, Alpana Agarwal and Chandra Shekhar*
Thapar Institute of Engineering and Technology, PATIALA
*Central Electronics Engineering Research Institute, Pilani, India

Abstract: This paper introduces the design of a clocked high-speed CMOS comparator. The comparator consists of a differential input stage, two regenerative latch and output buffers. This circuit operating under + 5.0 / 0.0 power supply, performs comparison within a few nanoseconds. The power consumption of the comparator is only 0.3 mW at 0.11 GHz clock rate.

1. INTRODUCTION

A high-speed comparator should have a propagation delay time as small as possible. The basic principle behind the high-speed comparator is to use a preamplifier to build up the input change to a sufficiently large value and then apply it to latch. This combines the best aspect of circuits with a negative exponential response (the preamplifier) with circuits with a positive exponential response (the latch).

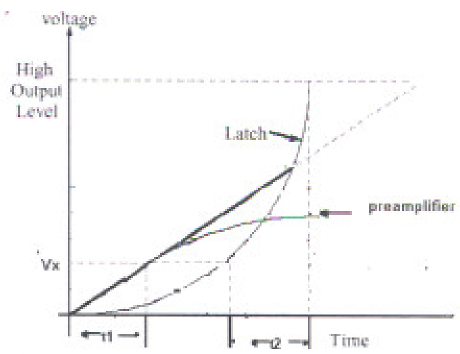


Fig. 1: Preamplifier and Latch Step Response

This is illustrated in Fig.1[1], where the gain of the preamplifier times the input voltage is not sufficient to reach the desired output level. Rather during time t_1 the preamplifier amplifies the input voltage to a value V_X.The voltage V_X is then applied to latch input, which then goes to the desired output voltage in time t_2. Thus total response time is $t_1 + t_2$. If comparator consisted only of the preamplifier, the gain would have to be larger and the delay to make the transition from V_{OL} to V_{OH} would be longer. So larger the input to latch the shorter the time for the output to reach its maximum value.

2. COMPARATOR CIRCUIT

The proposed comparator circuit is depicted in Fig.2 [2]. It consists of a differential input pair (M1 and M2), a CMOS latch circuit and output buffers. The CMOS latch composed of an n-channel flip-flop (M6 and M7) with a pair of n-channel transfer

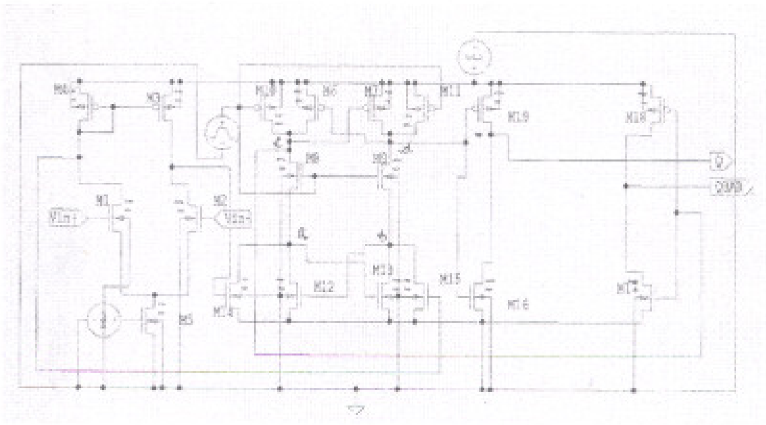


Fig.2 Schematic of Comparator

gates (M8 and M9) for strobing, and a p-channel flip-flop (M12 and M13) with a pair of p-channel precharge transistors (M10 and M11).

The dynamic operation of this circuit can be divided into two parts. First, when latch is low, the p-channels M12 and M13 are isolated from n-channels, M6 and M7. After the input voltage settles on its decision, a voltage proportional to the input voltage difference is established between nodes *a* and *b* in the end of this period. This voltage difference will act as the initial imbalance for the following regeneration time interval. In the meantime, the p-channel (M12 and M13) is reset by the two-closed precharge transistors, which charge the nodes *c* and *d* to the positive power supply voltage.

The regeneration is initialized by the closing of latch. So the transistors M8 and M9 are also closed. The n-channel flip-flop and p-channel flip-flop, regenerates the voltage difference between the nodes *a* and *b* and between the nodes *c* and *d*. the voltage difference between node *c* and *d* is soon amplified to a voltage nearly equal to power supply voltages.

3. DESIGN PROCEDURE FOR COMPARATOR

A. SPECIFICATIONS: -

- DC gain (A_V)
- Input common mode range [V_{in}(min) and V_{in}(max)]
- Load capacitance (C_L)
- Total delay (ns)
- Output voltage swing
  [V_{out} (max) and V_{out} (min)]

B. DESIGN PROCEDURE: -

1. First of all the total delay should be divided into three stages. Then taking that delay and output capacitance for each stage we can calculate the current. Let us see each stage's calculation. Considering the output stage as first stage the current flowing can be calculated using load capacitance, delay and output voltage swing

specifications. Note designing the output buffers is just equivalent to the design of digital inverter. So

$$I_{16} = I_{17} = C_L * \left(\frac{dv * 2}{dt} \right)$$

Where dv is output voltage difference and dt is the total delay corresponding to this stage. That's why time is halved for the two buffers. From the specification of output voltage swing, we can see that the minimum voltage that make the transistors M_{16} and M_{17} to remain in saturation is that the drop between these two transistors is equal to the difference of the V_{DD} and V_{out} (max), similarly for M_{18} and M_{19} this voltage is V_{SS} and V_{out} (min). These voltages give us the drain to source voltage of the transistors. So taking this drain to source voltage and the bias current together we get

$$\left(\frac{W}{L} \right)_{18} = \frac{2 * I_{16}}{K_N * (V_{DS})^2}$$

$$\left(\frac{W}{L} \right)_{19} = \frac{2 * I_{17}}{K_N * (V_{DS})^2}$$

The corresponding p-channel transistor W/L's can be calculated using mobility ratio of p and n-channel transistors.

2. Calculate the output capacitance of second stage by taking into consider the capacitances of the transistor of first stage it has to drive. This will help in getting current that is required in second stage. Looking at the circuit the second stage is a Nand gate pair. So total delay can be divided in two equally as in first step. We will design this stage using the equivalent of nand to inverter.

$$I_1 = I_2 = C_{out2} * \left(\frac{dv * 2}{dt} \right)$$

$$\left(\frac{W}{L} \right)_{equ} = \frac{2 * I_1}{K_N * (V_{DS})^2}$$

$$\left(\frac{W}{L} \right)_{6,8,10,7,9,11} = 2 * \left(\frac{W}{L} \right)_{equ}$$

where $(W/L)_{equ}$ is the ratio for equivalent of nand . C_{out2} is the output capacitance of second stage and V_{ds} is to be calculated in same fashion as in the previous step. The corresponding p-channel transistor W/L's can be calculated using mobility ratio of p and n-channel transistors.

3. Similarly, calculate the output capacitance of third stage by taking into consider the capacitances of the transistor of second stage it has to drive. This will help in getting bias current.

$$I_{BIAS} = 2 * C_{out3} * \left(\frac{dv}{dt} \right)$$

Next step is to calculate the transconductance g_{m1} of transistor M1 using the gain relation of the two stages.

$$g_{m1} = A_v(0) * (g_{ds2} + g_{ds4})$$

where $g_{dsi} = \lambda_P * I_{Di}$ (For p-type transistor)

$g_{dsi} = \lambda_N * I_{Di}$ (For n-type transistor)

Using the above-calculated value of transconductance of differential transistors, we can design M1 and M2 i.e the differential pair transistors.

$$\frac{W_1}{L_1} = \frac{W_2}{L_2} = \frac{{g_{m1}}^2}{K_N * I_{BIAS}}$$

Now calculate the value of gate to source voltage of the current mirror transistors using the specification of maximum input common mode voltage. Here we use the relation

$$V_{SG3} = V_{DD} - V_{in}(max) + V_{TN}$$

Using the gate to source voltage calculated above we can design the transistors M3 and M4.

$$\frac{W_3}{L_3} = \frac{W_4}{L_4} = \frac{I_{BIAS}}{K_P * (V_{SG3} - |V_{TP}|)^2}$$

Next step is to calculate $V_{DS5}(sat)$ using the specification of minimum input common mode voltage. The relation is given by

$$V_{DS5} = V_{in}(min) - V_{GS1} - V_{SS}$$

Where $$V_{GS1} = \sqrt{\frac{I_{BIAS} * L_1}{K_N * W_1}} + V_{TN}$$

Using the above-calculated value of V_{DS5} we can design the transistor M5.

$$\frac{W_5}{L_5} = \frac{2 * I_{BIAS}}{K_N * (V_{DS5}(sat))^2}$$

Lastly, the bias voltage is given by

$$V_{B5} = (V_{DS5} / 2) + V_{TN}$$

4. SIMULATION RESULTS

In order to verify the procedure, the circuit was designed using that and then using T-SPICE it is simulated. Fig [3,4] shows comparator gain and slew.
The comparator maintains the gain of 25.7 dB with phase margin of 51.72 degree. It can work up to the frequencies of 13.33 MHz i.e. this is the unity gain bandwidth. It can charge or discharge a load of 10pf with slew rate of 2.828 V/ns and 2.229 V/ns respectively. The total delay is found to be 9 ns. It can resolve the voltage difference of 0.02 V. The above simulation results are with specifications total delay = 20 ns, C_L = 1pf, V_{in}(min) and V_{in}(max) = 4.5 V and 1.25 V respectively, V_{out} (max) and V_{out} (min) = 4.0 V and 0.0 V respectively, A(v) = 1000.

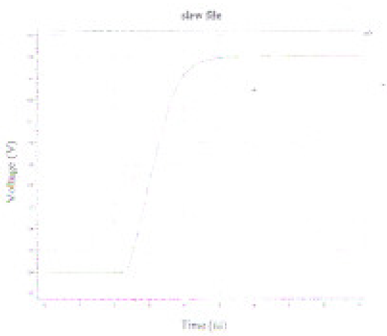


Fig.3 Slew Rate of Comparator

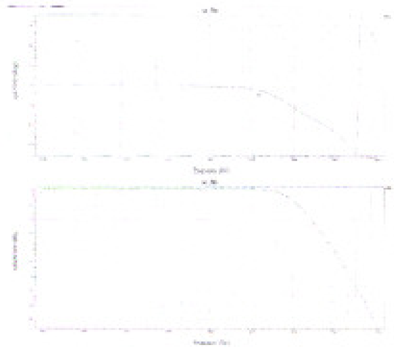


Fig.4 Ac Response of Comparator

5. CONCLUSION

A CMOS comparator design procedure has been developed for use in ADC. A dynamic latch preceded by an amplifier has been used to build a fast and precise comparator. The power consumption of the comparator is only 0.3 mW at 0.11 GHz clock rate, which is very low as compared to [5]. It can also charge or discharge with a much better slew rate than [7].

REFRENCES

[1] Allen Philip E., Holberg Douglas R., ''*CMOS Analog Circuit Design* '' Oxford University Press, London, 2003,Second Edition.

[2] Baker R.J, Li H.W, and Boyce D.E," *CMOS Circuit Design, Layout, and Simulation*". Piscataway, NJ: IEEE Press, 1998, Chap, 26.

[3] Maloberti Franco,"*Analog Design For CMOS VLSI Systems*" KLUWER academic Publisher, Boston/ Dordrecht/ London.

[4] Benjamin J. McCarroll, Charls D. Sodini, Hae-Seung Lee, " *A High Speed CMOS Comparator For Use In An ADC*," IEEE Journal of Solid State Circuits, Vol. 23, No.1, February 1988.

[5] G. M. Yin, F. Op't Eynde and W. Sansen,"A High Speed CMOS Comparator With 8-Bit Resolution", IEEE Journal of Solid State Circuits, Vol. 27, No.2, February 1992.

[6] J. A. Fisher and R. Koch, "*A Highly Linear CMOS Buffer Amplifier*," IEEE Journal of Solid State Circuits, Vol. SC-22, No.3, June 1987.
[7] R. Klinke, Member, IEEE, B. J. Hosticka, Senior Member, IEEE and H. J. Peleiderer, Senior Member, IEEE, "*A very-high Slew-rate CMOS operational Amplifier*," IEEE Journal of Solid State Circuits, Vol. 24, No.3, June 1989.

Bharati Vidyapeeth's College of Engineering

Certificate of Participation

National Conference on VLSI Design & Technology
15th 16th April, 2004

This is to certify that Mr. /Ms. /Dr. /Prof. Jyoti Kedia *of* Thapar Institute of Engineering and Technology, Patiala *has participated and presented a paper / ~~invited talk~~ on* Design of clocked Comparator using Basic Latch

Co authors: Alpana Aggarwal, Chandershekar

in the National Conference on VLSI Design & Technology held at Bharati Vidyapeeth's College of Engineering, A-4, Paschim Vihar, New Delhi-63 on 15th & 16th April, 2004

Mr. Sanjay Kumar Barwar
Co-Convener

Dr. M. K. Raina
Convener
HOD, ECE Dept.

Dr. S. S. Inamdar
Principal
BVCOE, New Delhi

COMPARATIVE ANALYSIS OF CMOS ANALOG COMPARATORS

Jyoti kedia, Alpana Agarwal
Thapar Institute of Engineering and Technology, Patiala

Abstract: This paper discusses the comparative study of three different comparators. The comparison is done on the basis of different parameters of comparator. From power consumption and speed point of view the comparator using regenerative circuit, is the best implementation.

1. INTRODUCTION

The three different comparators, which have been compared here, are:

1. Two-stage open loop comparator
2. Clocked comparator using basic latch
3. Self-biased comparator

Lets have an introduction of each of the above comparator.

As we can see from the requirements for a comparator reveal that it requires a differential input and sufficient gain to be able to achieve the desired resolution. The best implementation is the two-stage opamp [7]. A simplification occurs because the comparator will generally be used in open loop mode and it's not necessary to compensate that. It is preferred so that it has largest bandwidth possible, which will give a faster response.

A high-speed comparator should have a propagation delay time as small as possible. The basic principle behind the high-speed clocked comparator is to use a preamplifier to build up the input change to a sufficiently large value and then apply it to latch. This combines the best aspect of circuits with a negative exponential response (the preamplifier) with circuits with a positive exponential response (the latch).

The circuit of self-biased comparator that is designed here has the ability to sink and source large amounts of current in large capacitances.

The circuit configuration [2] differs from those of conventional CMOS differential-amplifiers configuration in two ways:

1. The amplifier is completely complementary i.e. each n-type device operates in push-pull fashion with a corresponding p-type device.

2. The amplifier is self-biased through negative feedback.

2. TWO STAGE OPEN LOOP COMPARATOR

Figure 1 shows the schematic of two-stage comparator. Simply the comparator is made up of three building blocks:

1. Differential stage
2. Current mirror
3. CMOS inverter with active load

A differential pair is widely used as the input stage of the op-amplifier. It is

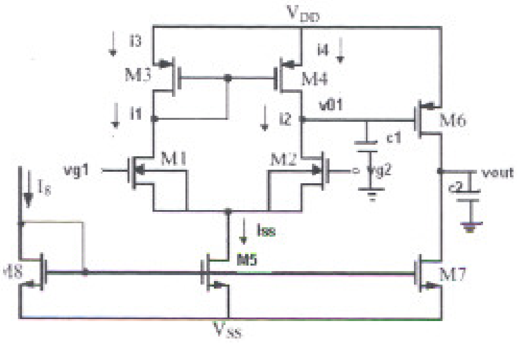


Fig. 1. Two stage Comparator

made of two transistors with their source in common, fed by current source. The transistors may either be n-channel or p-channel, and they are matched to each other.

Current mirror is composed of two transistors, of which one M1 is diode connected as shown in figure 2.

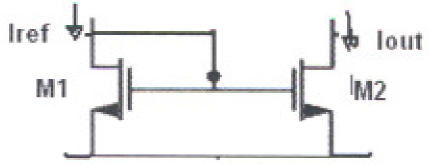


Fig 2: Simple current mirror

M1 receives the reference current I_{ref} and measures it by developing at its gate voltage V_{GS1}; this voltage biases the gate of M2.

The simplest form of inverter is the inverter with active load. Here input is applied to only one transistor while the gate of complementary element is biased with a fixed voltage and operates as an active load. The biasing voltage is obtained by a transistor connected in so-called diode configuration and carrying a given current I_{Bias}.

4. CLOCKED COMPARATOR USING BASIC LATCH

As illustrated in Figure 3 [7], where the gain of the preamplifier times the input voltage is not sufficient to reach the desired output level. Rather during time t_1 the preamplifier amplifies the input voltage to a value V_X. The voltage V_X is then applied to latch input, which then goes to the desired output voltage in time t_2. Thus total response time is $t_1 + t_2$. If comparator consisted only of the preamplifier, the gain would have to be larger and the delay to make the transition from V_{OL} to V_{OH} would be longer. So larger the input to latch the shorter the time for the output to reach its maximum value.

The proposed comparator circuit is depicted in Fig.4 [1]. It consists of a differential input pair (M1 and M2), a

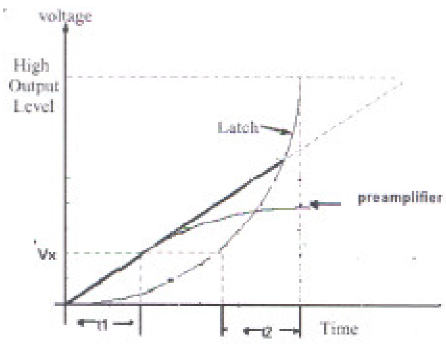


Fig 3: Preamplifier and Latch Step Response

CMOS latch circuit and output buffers. The CMOS latch composed of an n-channel flip-flop (M12 and M13) with a pair of n-channel transfer gates (M8 and M9) for strobing, and a p-channel flip-flop (M6 and M7) with a pair of p-channel precharge transistors (M10 and M11).

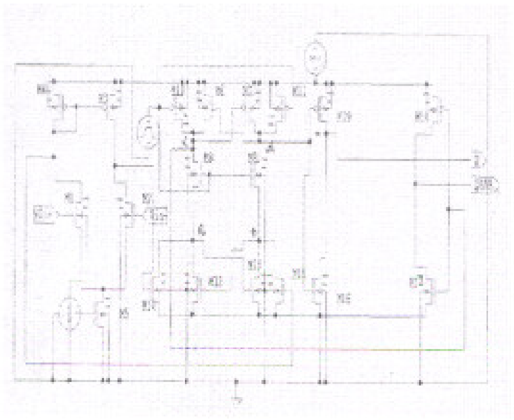


Fig.4 Schematic of Comparator

The dynamic operation of this circuit can be divided into two parts. First, when latch is low, the p-channels M6 and M7 are isolated from n-channels, M12 and M13. After the input voltage settles on its decision, a voltage proportional to the input voltage difference is established between nodes *a* and *b* in the end of this period. This voltage difference will act as the initial imbalance for the following regeneration time interval. In the meantime, the p-channel (M6 and M7) is reset by the two-closed precharge transistors, which charge the nodes *c* and *d* to the positive power supply voltage. The regeneration is initialized by the closing of latch. So the transistors M8 and M9 are also closed. The n-channel flip-flop and p-channel flip-flop, regenerates the voltage difference between the nodes *a* and *b* and between the nodes *c* and *d*. the voltage difference between node *c* and *d* is soon amplified to a voltage nearly equal to power supply voltages.

4.SELF-BIASED COMPARATOR

The operation of self-biasing comparator can be understood through its derivation [2]. Fig 6(a) illustrates two folded cascode differential amplifiers, one the complement of other. These amplifiers have the greater dynamic ranges than ordinary differential amplifier as a result of the larger drain-source voltage drop on input pairs. This larger voltage drop maintains the input pairs in active region even for large input voltage swings. While neither amplifier in Fig 6(a) is capable of covering the entire input range from negative supply to positive supply, a combination of the two amplifiers can cover this entire range.

In the first step of derivation, the loads of the two amplifiers are deleted, and their outputs are connected together to produce the fully complementary, but externally biased differential amplifier of Fig 6(b). However the circuit of Fig 6(b) cannot be biased in a stable fashion.

In order for the circuit to be biased in stable fashion the currents through M3 and M4 devices should be identical. Any difference in currents through these two devices result in extreme shifts in amplifier bias voltages. Achieving

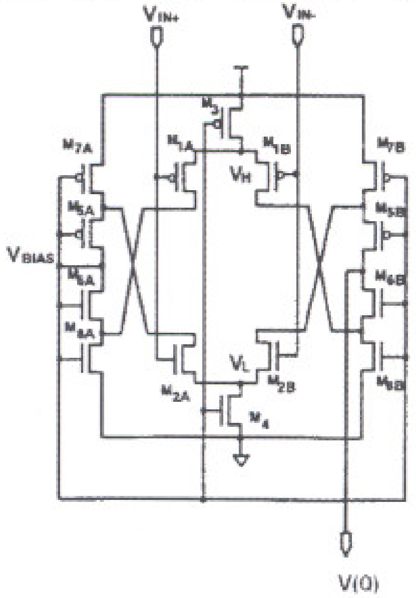


Fig. 5. Self-Biased Comparator

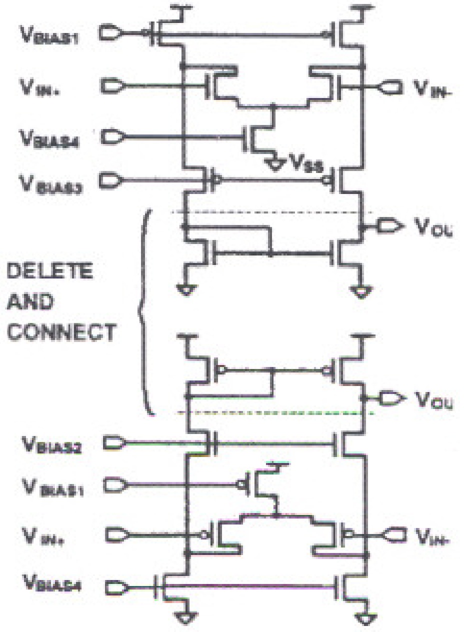


Fig. 6(a) Folded Cascode Differential Amplifier

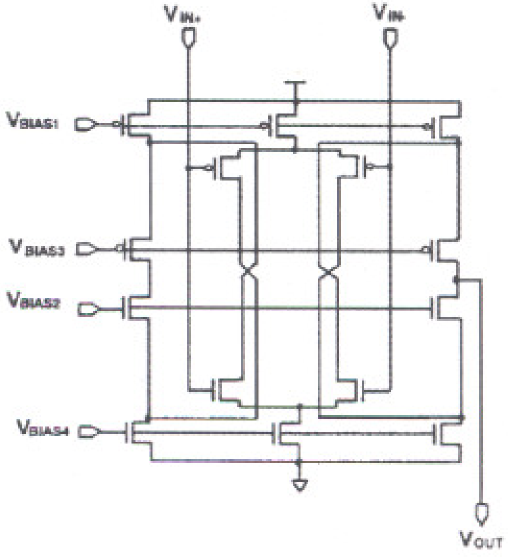


Fig. 6(b) Externally Biased Differential Amplifier

perfect equality of currents in these two devices using external biasing is practically impossible, so that the configuration of Fig 6(b) is practically impossible.

A simple modification of the circuit of Fig. 6(b), however, results in stabilization of the bias voltages. This modification is illustrated in Fig 5, in which the two bias-voltages are disconnected from the external sources and instead are connected to internal amplifier node V_{BIAS}. This self-biasing of the amplifier creates the negative feedback loop that stabilizes the bias voltages. Any variations in the processing parameters or operating conditions that shifts the bias voltages away from their nominal values result in a shift in V_{BIAS} that corrects the bias voltages through negative feedback. The resulting self-biased amplifier is illustrated in Fig. 5.

5. SIMULATION RESULTS

The comparators explained in sections 2-5 were designed and simulated in T-spice environment. The measured data of all comparator circuits have been summarized in Table 1.

6. CONCLUSION

The open loop two stage comparator has achieved highest gain of 32 dB and offset voltage is minimum. Whereas the clocked comparator using basic latch can charge, or discharge a 1-pF capacitance with slew rate of 5.8 V/ns. Also very high slew rate for large capacitances have been achieved as compared to [4]. The power consumption of this comparator is minimum, which is only 0.3 mW as compared to [8]. The self-biased comparator has minimum delay [5-7], which is of the order of nanoseconds i.e. 0.42 ns that is the main attraction. It has achieved maximum gain bandwidth. So it can work for highest range of frequencies. Looking at all parameter values one can conclude that overall two-stage open loop comparator is the best implementation.

Parameter	Two-stage	Clocked comparator	Self-biased
Offset (V)	-0.007	-0.09	0.02
Resolution (V)	0.05	0.02	0.03
Rising Delay (ns)	10.3	-	0.42
Falling Delay (ns)	23.4	-	0.46
Gain (dB)	32	25.7	25.3
GB (MHZ)	22.84	13.33	314
Phase Margin (Degree)	50	51.72	70.3
Rising Slew Rate with 1pF load (V/ns)	0.247	5.844	0.72
Falling Slew Rate with 1pF load (V/ns)	0.300	10.74	0.76
Power dissipation (mW)	9.5	0.3	27.8

Table 1

REFRENCES

[1] Baker R.J, Li H.W, and Boyce D.E, " *CMOS Circuit Design, Layout, and Simulation*". Piscataway, NJ: IEEE Press, 1998, Chap, 26.

[2] Bazes M., "*Two Novell Full Complementary Self Biased Differential Amplifier*," IEEE Journal of Solid State Circuits, Vol. 26, No. 2,pp. 165-168,February 1991.

[3] Fisher J. A. and Koch R., "*A Highly Linear CMOS Buffer Amplifier*," IEEE Journal of Solid State Circuits, Vol. SC-22, No.3, June 1987.

[4] Klinke R., Member, IEEE, B. J. Hosticka, Senior Member, IEEE and Peleiderer H. J., Senior Member, IEEE, "*A very-high Slew-rate CMOS operational Amplifier*," IEEE Journal of Solid State Circuits, Vol. 24, No.3, June 1989.

[5] Maloberti Franco, "*Analog Design For CMOS VLSI Systems*" KLUWER academic Publisher, Boston/ Dordrecht/ London.

[6] McCarroll Benjamin J., Sodini Charls D., Lee Hae-Seung, " *A High Speed CMOS Comparator For Use In An ADC*," IEEE Journal of Solid State Circuits, Vol. 23, No.1, February 1988.

[7] Philip E.Allen, Holberg Douglas R., "*CMOS Analog Circuit Design* " Oxford University Press, London, 2003,Second Edition.

[8] Yin G. M., F. Op't Eynde and Sansen W., "*A High Speed CMOS Comparator With 8-Bit Resolution*", IEEE Journal of Solid State Circuits, Vol. 27, No.2, February 1992.

DESIGN OF
SELF-BIASED COMPARATOR

Jyoti kedia, Alpana Aggarwal and Chandra Shekhar*
Thapar Institute of Engineering and Technology, PATIALA
*Central Electronics Engineering Research Institute, Pilani, India

Abstract - This paper discusses the design of self-biased CMOS analog comparator. On the basis of simulation results the performance analysis has been done. The negative feedback in self-biased comparator increases the comparison speed. The maximum delay of 0.8 ns has been achieved. The circuit is capable of driving large capacitance of 15 pf can be charged or discharged within few nano-seconds.

1. INTRODUCTION

Many techniques have been introduced in the literature for implementing high-speed CMOS comparators. The most commonly used are the latches, which are used after the preamplifier stage. If a comparator has a large capacitive load, the chances are that it is slew rate limited. The circuit that is designed here has the ability to sink and source large amounts of current in large capacitances.
The circuit configuration [4] differs from those of conventional CMOS differential-amplifiers configuration in two ways:

1. The amplifier is completely complementary i.e. each n-type device operates in push-pull fashion with a corresponding p-type device.

2. The amplifier is self-biased through negative feedback.

These two differences result in several performance enhancements desirable in comparator applications.

2. SELF -BIASING COMPARATOR

CMOS differential amplifiers with wide input dynamic ranges have been reported [2,3,7]. All of these amplifiers are externally biased while none of them is fully complementary. The circuit configuration that has been designed is as shown in the Fig 1. As we can see that this circuit is fully complementary as well as entirely self-biased.
The operation of self-biasing comparator can be understood through its derivation [4]. Fig 2(a) illustrates two folded cascode differential amplifiers, one the complement of other. These amplifiers have the greater dynamic ranges than ordinary differential amplifier as a result of the larger drain-source voltage drop on input pairs. This larger voltage drop maintains the input pairs in active region even for large input voltage swings. While neither amplifier in Fig 2(a) is capable of covering the entire input range from negative supply to positive supply, a combination of the two amplifiers can cover this entire range.
In the first step of derivation, the loads of the two amplifiers are deleted, and their outputs are connected together to produce the fully complementary, but externally biased differential amplifier of Fig 2(b). However the circuit of Fig 2(b) cannot be biased in a stable fashion.

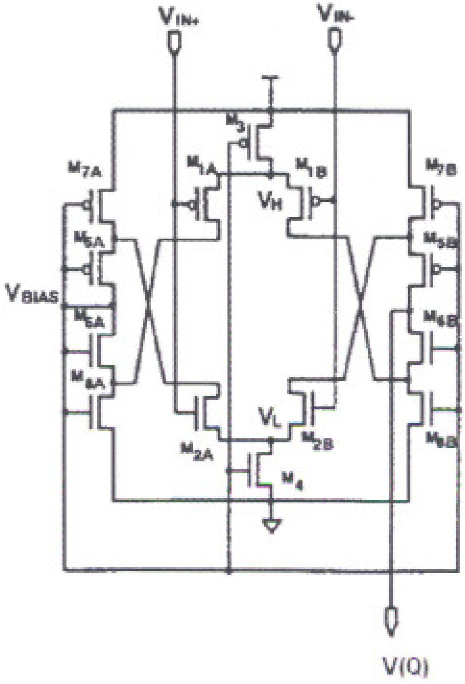


Fig. 1. Self-Biased Comparator

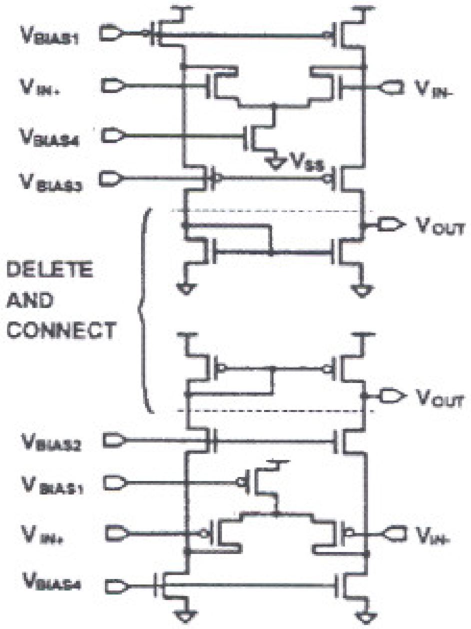


Fig. 2(a) Folded Cascode Differential Amplifier

In order for the circuit to be biased in stable fashion the currents through M3 and M4 devices should be identical. Any difference in currents through these two devices result in extreme shifts in amplifier bias voltages. Achieving perfect equality of currents in these two devices using external biasing is practically impossible, so that the configuration of Fig 2(b) is practically impossible.

A simple modification of the circuit of Fig. 2(b), however, results in stabilization of the bias voltages. This modification is illustrated in Fig 1, in which the two bias-voltages are disconnected from the external sources and instead are connected to internal amplifier node V_{BIAS}. This self-biasing of the amplifier creates the negative feedback loop that stabilizes the bias voltages. Any variations in the processing parameters or operating conditions that shifts the bias voltages away from their nominal values result in a shift in V_{BIAS} that corrects the bias voltages through negative feedback. The resulting self-biased amplifier is illustrated in Fig. 1.

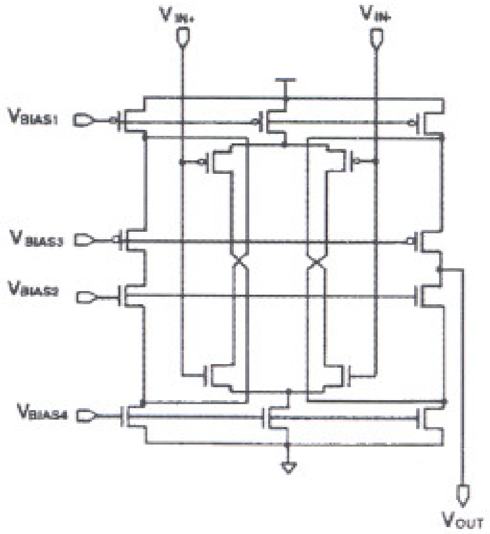


Fig. 2(b) Externally Biased Differential Amplifier

3. DESIGN PROCEDURE FOR SELF-BIASEDCOMPARATOR

A. SPECIFICATIONS

- Unity gain bandwidth (GB)
- Input common mode range [V_{in} (min) and V_{in} (max)]
- Load capacitance (C_L)
- Slew rate (SR)
- Output voltage swing [V_{out} (max) and V_{out} (min)]

B. DESIGN PROCEDURE

1. The first step towards design of self-biased comparator is to decide the bias currents in transistors M_3 and M_4 using the slew rate and load capacitance specifications. So we have

$$I_3 = I_4 = SR * C_L$$

2. Other bias currents I_7 and I_8 flowing through M_{7A} or M_{7B} and M_{8A} or M_{8B} should be designed in such a way that the dc current in cascode branches never goes to zero. To implement this, the values of these currents are normally between the values of I_3 or I_4 and twice their values. Now to calculate the W/L ratios of these transistor we need to calculate their drain to source voltages. From the specification of output voltage swing, we can se that the minimum voltage that make the transistors M_{7A} and M_{5A} to remain in saturation is that the droop between these two transistors is equal to the difference of the V_{DD} and V_{out} (max), similarly for M_{8A} and M_{6A} this voltage is V_{SS} and V_{out} (min). These voltages if we equally divide between the two respective transistors we get the drain to source voltage of the transistors. So taking this drain to source voltage and the bias current together we get

$$I_7 = I_8 = 1.3 * I_3$$

$$\left(\frac{W}{L}\right)_{7A,7B} = \frac{2 * I_7}{K_P * (V_{ds})^2}$$

$$\left(\frac{W}{L}\right)_{8A,8B} = \frac{2 * I_8}{K_N * (V_{ds})^2}$$

Assuming that transistors are in saturation the calculated drain to source voltage can be increased to twice its value so that the transistor remain in deep saturation area.

3. The current flowing in M_{5A} or M_{5B} and M_{6A} or M_{6B} is

$$I_5 = I_6 = I_7 - (0.5 * I_3)$$

$$\left(\frac{W}{L}\right)_{5A,5B} = \frac{2 * I_5}{K_P * (V_{ds})^2}$$

$$\left(\frac{W}{L}\right)_{6A,6B} = \frac{2 * I_6}{K_N * (V_{ds})^2}$$

Where V_{ds} we have already calculated in step 2.

4. For the design of differential pair we again assume that they are in saturation. Using the unity gain bandwidth

$$g_{m1} = g_{m2} = 2 * \pi * GB * C_L$$

$$\left(\frac{W}{L}\right)_{1A,1B} = \frac{g_{m1}^{\ 2}}{K_P * I_3}$$

$$\left(\frac{W}{L}\right)_{2A,2B} = \frac{g_{m2}^{\ 2}}{K_N * I_4}$$

5. Lastly the tail transistors are designed using input common mode range specification. From [1] we have

$$V_{ds4} = V_{IN}(\min) - V_{gs2A}$$

where

$$V_{gs2A} = \left(\sqrt{\frac{2 * I_4}{K_N * \left(W/L\right)_{2A}}} \right) + V_{TN}$$

$$\left(\frac{W}{L}\right)_4 = \frac{2 * I_4}{K_N * (V_{ds4})^2}$$

where V_{TN} is the threshold voltage for n-type transistor. Another tail transistor M_3 can be designed using the mobility ratio of n-type and p-type transistor.

4. SIMULATION RESULTS

In order to verify the procedure, the circuit was designed using that and then using T-SPICE it is simulated. Fig [3-7] shows comparator delay, gain, slew and resolution.

The comparator maintains the gain of 35.5 dB with phase margin of 59.3 degree. It can work up to the frequencies of 246.7 MHz i.e. this is the unity gain bandwidth. It can charge or discharge a load of 10 pf with slew rate of 28.42 V/μs and 26.4 V/μs respectively. The propagation delay is found to be 0.8 ns. It can resolve the voltage difference of 0.025 V. These all values are for specification of SR 1 V/μs, GB 10 MHz and C_L 10 pf.

5. CONCLUSION

The comparator designed takes the minimum delay as compared to [5-7]. Gain can be decreased to further reduce the delay. This comparator can charge or discharge the large capacitances within few nanoseconds. The design example as shown in the figures proves that it is possible to implement a CMOS comparator with maximum delay less than 1ns.

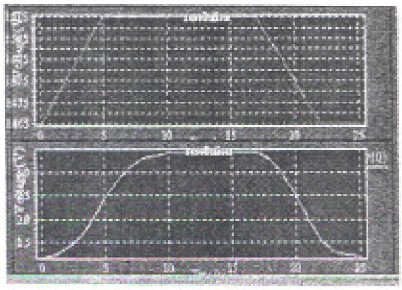


Fig.3 Resolution of Comparator

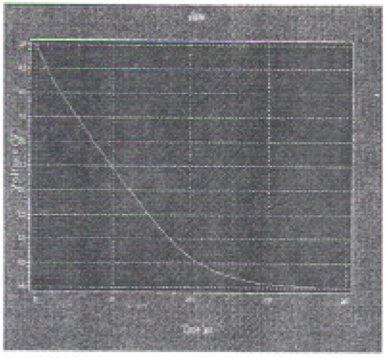


Fig. 4 Slew Rate from high to low

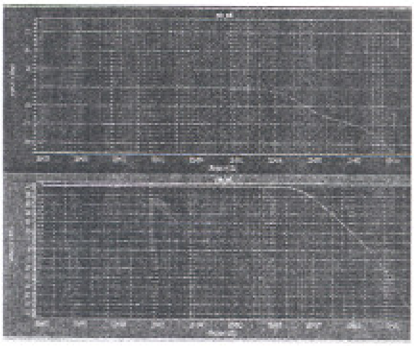


Fig.5 Unity Gain Bandwidth

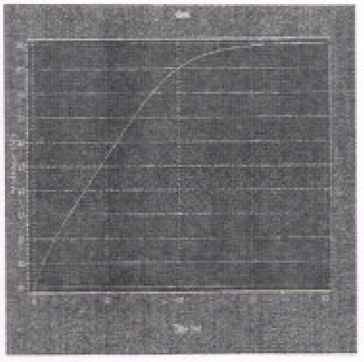


Fig.6 Slew Rate from low to high

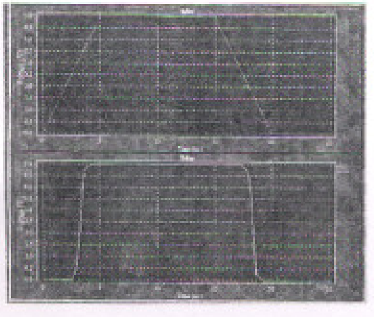


Fig. 7 Propagation Delay of Comparator

ACKNOWLEDGEMENT

The authors would like to acknowledge the financial support from MoCIT by way of SMDP-VLSI project. We are also thankful to Dr. S.C Saxena Director, Thapar Institute of Engineering and Technology, Patiala for his constant encouragement.

REFRENCES

[1] Allen Philip E., Holberg Douglas R., "*CMOS Analog Circuit Design* " Oxford University Press, London, 2003,Second Edition.

[2] Baker R.J, Li H.W, and Boyce D.E," *CMOS Circuit Design, Layout, and Sim ulation*. Piscataway, NJ: IEEE Press, 1998, Chap, 26.

[3] Maloberti Franco,"*Analog Design For CMOS VLSI Systems*" KLUWER academic Publisher, Boston/ Dordrecht/ London.

[4] M. Bazes,"*Two Novell Full Complementary Self Biased Differential Amplifier*," IEEE Journal of Solid State Circuits, Vol. 26, No. 2,pp. 165-168,February 1991.

[5] Benjamin J. McCarroll, Charls D. Sodini, Hae-Seung Lee, " *A High Speed CMOS Comparator For Use In An ADC*," IEEE Journal of Solid State Circuits, Vol. 23, No.1, February 1988.

[6] G. M. Yin, F. Op't Eynde and W. Sansen,"A High Speed CMOS Comparator With 8-Bit Resolution", IEEE Journal of Solid State Circuits, Vol. 27, No.2, February 1992.

[7] J. A. Fisher and R. Koch, "*A Highly Linear CMOS Buffer Amplifier*," IEEE Journal of Solid State Circuits, Vol. SC-22, No.3, June 1987.

$$\left(\frac{W}{L}\right)_{equ} = \frac{2 * I_1}{K_N * (V_{DS})^2}$$

$$\left(\frac{W}{L}\right)_{8,9,12,13,14,15} = 2 * \left(\frac{W}{L}\right)_{equ}$$

where $(W/L)_{equ}$ is the ratio for equivalent of nand . C_{out2} is the output capacitance of second stage and V_{ds} is to be calculated in same fashion as in the previous step. The corresponding p-channel transistor W/L's can be calculated using mobility ratio of p and n-channel transistors.

STEP 3: Similarly, calculate the output capacitance of third stage by taking into consider the capacitances of the transistor of second stage it has to drive. This will help in getting bias current.

$$C_{out3} = C_{GSO} * W_{14} + 0.67 * C_{OX} * W_{eff} * L_{eff}$$

$$I_{BIAS} = 2 * C_{out3} * \left(\frac{dv}{dt}\right)$$

Next step is to calculate the transconductance g_{m1} of transistor M1 using the gain relation of the two stages.

$$g_{m1} = A_v(0) * (g_{ds2} + g_{ds4})$$

where $g_{dsi} = \lambda_P * I_{Di}$ (For p-type transistor)

$g_{dsi} = \lambda_N * I_{Di}$ (For n-type transistor)

Using the above-calculated value of transconductance of differential transistors, we can design M1 and M2 i.e the differential pair transistors.

$$\frac{W_1}{L_1} = \frac{W_2}{L_2} = \frac{g_{m1}^{\;2}}{K_N * I_{BIAS}}$$

STEP 4: Now calculate the value of gate to source voltage of the current mirror transistors using the specification of maximum input common mode voltage. Here we use the relation

$$V_{SG3} = V_{DD} - V_{in}(max) + V_{TN}$$

Using the gate to source voltage calculated above we can design the transistors M3 and M4.

$$\frac{W_3}{L_3} = \frac{W_4}{L_4} = \frac{I_{BIAS}}{K_P * (V_{SG3} - |V_{TP}|)^2}$$

Next step is to calculate $V_{DS5}(sat)$ using the specification of minimum input common mode voltage. The relation is given by

$$V_{DS5} = V_{in}(min) - V_{GS1} - V_{SS}$$

Where $$V_{GS1} = \sqrt{\frac{I_{BIAS} * L_1}{K_N * W_1}} + V_{TN}$$

Using the above-calculated value of V_{DS5} we can design the transistor M5.

$$\frac{W_5}{L_5} = \frac{2 * I_{BIAS}}{K_N * (V_{DS5}(sat))^2}$$

Lastly, the bias voltage is given by

$$V_{B5} = (V_{DS5} / 2) + V_{TN}$$

4.4 AN EXAMPLE

4.4.1 SPECIFICATIONS

- DC gain (A_V) = 1000 V/V

- V_{in} (min) = 1.25 V
- V_{in} (max) = 4.5 V
- Load capacitance (C_L) = 1pf
- Total delay (ns) = 20ns
- V_{out} (max) = 4.5 V
- V_{out} (min) = 0.5 V

4.4.2 DESIGN STEPS

STEP 1: Let us first divide the total propagation delay into three stages. So we can have first stage delay of 10 ns and that of regenerative latch has delay of 7 ns and that of preamplifier stage's delay is 3 ns. So now we can design the three stages. Lets start from output stage.

$$I_{16} = I_{17} = C_L * \left(\frac{dv * 2}{dt}\right) = 1 * 10^{-12} * \left(\frac{4 * 2}{10 * 10^{-9}}\right)$$

$$I_{16} = I_{17} = 800 \mu A$$

$$\left(\frac{W}{L}\right)_{16} = \frac{2 * I_{16}}{K_N * (V_{DS})^2} = \frac{2 * 800 * 10^{-6}}{6.33 * 10^{-5} * (0.5)^2} = 101.1$$

$$\left(\frac{W}{L}\right)_{17} = \frac{2 * I_{17}}{K_N * (V_{DS})^2} = \frac{2 * 800 * 10^{-6}}{6.33 * 10^{-5} * (0.5)^2} = 101.1$$

Now, the corresponding p-type transistors ratio can be calculated as

$$\left(\frac{W}{L}\right)_{18,19} = K * \frac{\mu_n}{\mu_p} * \left(\frac{W}{L}\right)_{16,17} = 0.989 * \frac{1215.74}{361.94} * 101.1$$

$$\left(\frac{W}{L}\right)_{18,19} = 335.8$$

where K is the process transconductance ratio of the n and p type transistor of an inverter. We have used it here, as the output stage is an inverter itself.

STEP 2: Now we have to calculate the output capacitance of the latch stage. This we can do by taking into consider the transistor's capacitance it has to drive. So we have

$$C_{out2} = C_{gd19} + C_{gd16}$$
$$C_{out2} = C_{GDO_P} * W_{19} + C_{GDO_N} * W_{16}$$
$$C_{out2} = 3.35*10^{-10}*335.8*10^{-6} + 2.89*10^{-10}*101.1*10^{-6}$$
$$C_{out2} = 0.14pF$$

So we can design second stage using above calculated value.

$$I_1 = I_2 = C_{out2} * \left(\frac{dv*2}{dt}\right) = 0.14*10^{-12}*\frac{4*2}{7*10^{-9}}$$
$$I_1 = I_2 = 160\mu A$$

We take current as 200µA for some margin. So transistor ratios are

$$\left(\frac{W}{L}\right)_{equ} = \frac{2*I_1}{K_N*(V_{DS})^2} = \frac{2*200*10^{-6}}{6.33*10^{-5}*(0.5)^2}$$
$$\left(\frac{W}{L}\right)_{equ} \cong 26$$

$$\left(\frac{W}{L}\right)_{8,9,12,13,14,15} = 2*\left(\frac{W}{L}\right)_{equ} = 2*26$$
$$\left(\frac{W}{L}\right)_{8,9,12,13,14,15} = 52$$

The corresponding p-type transistor's ratios are given by

$$\left(\frac{W}{L}\right)_{6,7,10,11} = K*\frac{\mu_n}{\mu_p}*\left(\frac{W}{L}\right)_{equ} = 0.989*\frac{1215.74}{361.94}*26$$

$$\left(\frac{W}{L}\right)_{6,7,10,11} \cong 87$$

STEP 3: For designing the preamplifier stage we have to calculate the output voltage that it has to drive as we did in step 2.

$$C_{out3} = C_{GSO} * W_{14} + 0.67 * C_{OX} * W_{eff} * L_{eff}$$
$$C_{out3} = 2.89 * 10^{-10} * 52 * 10^{-6} + 0.67 * 0.156 * 10^{-4} * 52 * 10^{-6} * 4 * 10^{-6}$$
$$C_{out3} = 17.2 fF$$

So the bias current will be

$$I_{BIAS} = 2 * C_{out3} * \left(\frac{dv}{dt}\right) = 2 * 17.2 * 10^{-15} * \left(\frac{4}{3 * 10^{-9}}\right)$$
$$I_{BIAS} = 50 \mu A$$

We take current as 100μA for some margin.

Using the bias current calculated above; design the transistor pair of current mirror circuit.

$$\frac{W_3}{L_3} = \frac{W_4}{L_4} = \frac{100 * 10^{-6}}{2.64 * 10^{-5} * (1.12 - |-0.63|)^2}$$

$$\frac{W_3}{L_3} = \frac{W_4}{L_4} = 15.7 \cong 16$$

$$K_P = 2.64 * 10^{-5} A / V^2$$

$$V_{SG3} = 5 - 4.5 + 0.62 = 1.12V$$
$$V_{TP} = -0.63V$$

Design of the differential pair requires the transconductance, which can be calculated using the open loop gain specification of both stages.Therefore,

$$g_{m1} = \frac{10{,}00*(0.01+0.02)*50*10^{-6}}{2202.2*10^{-6}}$$
$$g_{m1} = 15*10^{-4}\,S$$

$$g_{ds4} = \lambda_P * I'_4 = 0.02*50*10^{-6}, g_{ds2} = \lambda_N * I'_2 = 0.01*50*10^{-6}$$
$$I'_2 = I'_4 = \frac{I_{BIAS}}{2} = 50*10^{-6}\,A$$

Using the transconductance calculated above, differential pair ratios are given by

$$\frac{W_1}{L_1} = \frac{W_2}{L_2} = \frac{g_{m1}{}^2}{K_N * I_5} = \frac{(15*10^{-4})^2}{6.326*10^{-5}*2*50*10^{-6}}$$
$$\frac{W_1}{L_1} = \frac{W_2}{L_2} \cong 356$$

Now the only transistor left for designing is M5. Firstly, we have to calculate the drain to source voltage of M5.

$$V_{DS5}(sat) = V_{icm-} - V_{GS1} - V_{SS}$$
$$V_{DS5}(sat) = 1.25 - 0.686 = 0.56V$$
$$V_{GS1} = \sqrt{\frac{50*10^{-6}}{6.326*10^{-5}*356}} + 0.62 = 0.686V$$

So now,

$$\frac{W_5}{L_5} = \frac{2*100*10^{-6}}{6.33*10^{-5^2}*(0.56)^2}$$
$$\frac{W_5}{L_5} = 11$$

Lastly, the bias voltage is given by

$$V_{B5} = (V_{DS5} / 2) + V_{TN}$$
$$V_{B5} = (0.56 / 2) + 0.62$$
$$V_{B5} = 0.9\ V$$

The calculated aspect ratios of transistors are summarized in the table 2.

MOS	M1	M2	M3	M4	M5	M6	M7	M8	M9	M10	M11
W/L	356	356	16	16	11	87	87	52	52	87	87

MOS	M12	M13	M14	M15	M16	M17	M18	M19
W/L	52	52	52	52	101.1	101.1	335.8	335.8

Table 2

DESIGN OF SELF-BIASED COMPARATOR

5.1 INTRODUCTION

Many techniques have been introduced in the literature for implementing high-speed CMOS comparators. The most commonly used are the latches, which are used after the preamplifier stage. If a comparator has a large capacitive load, the chances are that it is slew rate limited. The circuit that is designed here has the ability to sink and source large amounts of current in large capacitances. The circuit configuration [3] differs from those of conventional CMOS differential-amplifiers configuration in two ways:

1. The amplifier is completely complementary i.e. each n-type device operates in push-pull fashion with a corresponding p-type device.
2. The amplifier is self-biased through negative feedback.

These two differences result in several performance enhancements desirable in comparator applications.

5.2 SELF -BIASING COMPARATOR

CMOS differential amplifiers with wide input dynamic ranges have been reported [2,18]. All of these amplifiers are externally biased while none of them is fully complementary. The circuit configuration that has been designed is as shown in the Figure 5.1. As we can see that this circuit is fully complementary as well as entirely self-biased.

The operation of self-biasing comparator can be understood through its derivation [3]. Figure 5.2(a) illustrates two folded cascode differential amplifiers, one the complement of other. These amplifiers have the greater dynamic ranges than ordinary differential amplifier as a result of the larger drain-source voltage drop on input pairs. This larger voltage drop maintains the input pairs in active region even for large input voltage swings. While neither amplifier in Figure 5.2(a) is capable of covering the entire input range from negative supply to positive supply, a combination of the two amplifiers can cover this entire range. In the first step of derivation, the loads of the two amplifiers are deleted, and their outputs are connected together to produce the fully complementary, but externally biased differential amplifier of Figure 5.2(b). However the circuit of Figure 5.2(b) cannot be biased in a stable fashion.

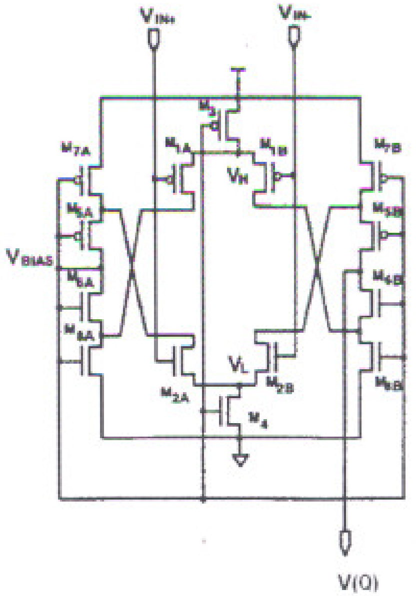


Figure. 5.1. Self-Biased Comparator

In order for the circuit to be biased in stable fashion the currents through M3 and M4 devices should be identical. Any difference in currents through these two devices result in extreme shifts in amplifier bias voltages. Achieving perfect equality of currents in these two devices using external biasing is practically impossible, so that the configuration of Figure 5.2(b) is practically impossible.

A simple modification of the circuit of Figure 5.2(b), however, results in stabilization of the bias voltages. This modification is illustrated in Figure 5.1, in which the two bias-voltages are disconnected from the external sources and instead are connected to internal amplifier node V_{BIAS}. This self-biasing of the amplifier creates the negative feedback loop that stabilizes the bias voltages.

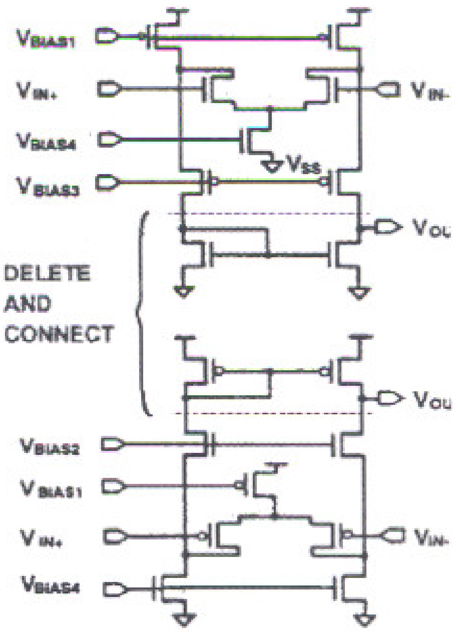


Figure. 5.2(a) Folded Cascode Differential Amplifier

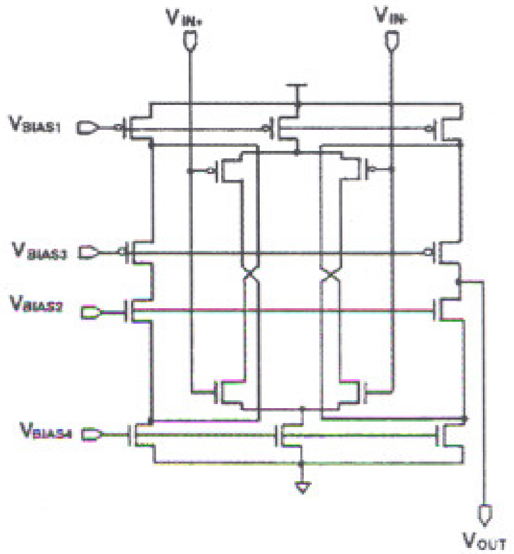


Figure. 5.2(b) Externally Biased Differential Amplifier

Any variations in the processing parameters or operating conditions that shifts the bias voltages away from their nominal values result in a shift in V_{BIAS} that corrects the bias voltages through negative feedback. The resulting self-biased amplifier is illustrated in Figure 5.1. The comparator designed takes the minimum delay as compared to [6,19,26].

5.3 DESIGN PROCEDURE

5.3.1 SPECIFICATIONS

- Unity gain bandwidth (GB)
- Input common mode range [V_{in} (min) and V_{in} (max)]
- Load capacitance (C_L)
- Slew rate (SR)
- Output voltage swing [V_{out} (max) and V_{out} (min)]

5.3.2 DESIGN STEPS

STEP 1: The first step towards design of self-biased comparator is to decide the bias currents in transistors M_3 and M_4 using the slew rate and load capacitance specifications. So we have

$$I_3 = I_4 = SR * C_L$$

STEP 1: Other bias currents I_7 and I_8 flowing through M_{7A} or M_{7B} and M_{8A} or M_{8B} should be designed in such a way that the dc current in cascode branches never goes to zero. To implement this, the values of these currents are normally between the values of I_3 or I_4 and twice their values. Now to calculate the W/L ratios of these transistor we need to calculate their drain to source voltages. From the specification of output voltage swing, we can see that the minimum voltage that make the transistors M_{7A} and M_{5A} to remain in saturation is that the drop between these two transistors is equal to the difference of the V_{DD} and V_{out} (max), similarly for M_{8A} and M_{6A} this voltage is V_{SS} and V_{out} (min) difference. These voltages if we equally divide between the two respective transistors we get the drain to source voltage of the transistors. So taking this drain to source voltage and the bias current together we get

$$I_7 = I_8 = 1.3 * I_3$$

$$\left(\frac{W}{L}\right)_{7A,7B} = \frac{2 * I_7}{K_P * (V_{ds})^2}$$

$$\left(\frac{W}{L}\right)_{8A,8B} = \frac{2 * I_8}{K_N * (V_{ds})^2}$$

Assuming that transistors are in saturation the calculated drain to source voltage can be increased to twice its value so that the transistor remain in deep saturation area.

STEP 3: The current flowing in M_{5A} or M_{5B} and M_{6A} or M_{6B} is

$$I_5 = I_6 = I_7 - (0.5 * I_3)$$
$$\left(\frac{W}{L}\right)_{5A,5B} = \frac{2 * I_5}{K_P * (V_{ds})^2}$$
$$\left(\frac{W}{L}\right)_{6A,6B} = \frac{2 * I_6}{K_N * (V_{ds})^2}$$

Where V_{ds} we have already calculated in step 2.

STEP 4: For the design of differential pair we again assume that they are in saturation. Using the unity gain bandwidth

$$g_{m1} = g_{m2} = 2 * \pi * GB * C_L$$
$$\left(\frac{W}{L}\right)_{1A,1B} = \frac{g_{m1}^{\ 2}}{K_P * I_3}$$
$$\left(\frac{W}{L}\right)_{2A,2B} = \frac{g_{m2}^{\ 2}}{K_N * I_4}$$

STEP 5: Lastly the tail transistors are designed using input common mode range specification. From [20] we have

$$V_{ds4} = V_{in}(\min) - V_{gs2A}$$

where

$$V_{gs2A} = \left(\sqrt{\frac{2 * I_4}{K_N * \left(W/L\right)_{2A}}} \right) + V_{TN}$$

$$\left(\frac{W}{L}\right)_4 = \frac{2 * I_4}{K_N * (V_{ds4})^2}$$

Where V_{TN} is the threshold voltage for n-type transistor. Another tail transistor M_3 can be designed using the mobility ratio of n-type and p-type transistor.

5.4 AN EXAMPLE

5.4.1 SPECIFICATIONS

- Unity gain bandwidth (GB) = 10 MHz
- V_{in} (min) = 1.0 V
- V_{in} (max) = 4.0 V
- Load capacitance (C_L) = 15pF
- Slew rate (SR) = 10 V/μV
- V_{out} (max) = 4.5 V
- V_{out} (min) = 0.5 V

5.4.2 DESIGN STEPS

STEP 1: First of all we need to calculate the bias current through the upper and lower tail transistors.

$$I_3 = I_4 = SR * C_L = 10 * 10^6 * 15 * 10^{-12}$$
$$I_3 = I_4 = 150\mu A$$

We take the current 200μA for some margin.

STEP 2: Now the currents I_7 and I_8 will lie between above calculated current values and twice their values. So we can take

$$I_7 = I_8 = 1.3 * I_{3,4}$$
$$I_7 = I_8 = 1.3 * 200 = 260\mu A$$

$$\left(\frac{W}{L}\right)_{7A,7B} = \frac{2 * I_7}{K_P * (V_{ds})^2} = \frac{2 * 260 * 10^{-6}}{2.64 * 10^{-5} * (0.5)^2}$$
$$\left(\frac{W}{L}\right)_{7A,7B} \cong 79$$
$$\left(\frac{W}{L}\right)_{8A,8B} = \frac{2 * I_8}{K_N * (V_{ds})^2} = \frac{2 * 260 * 10^{-6}}{6.33 * 10^{-5} * (0.5)^2}$$
$$\left(\frac{W}{L}\right)_{8A,8B} = 33$$

Where the calculated V_{ds} was 0.25 V but for keeping transistors in deep saturation region we take it 0.5 V as discussed in design procedure.

STEP 3: The current flowing in M_{5A} or M_{5B} and M_{6A} or M_{6B} is

$$I_5 = I_6 = I_7 - (0.5 * I_3)$$
$$I_5 = I_6 = 260 - (0.5 * 200)$$
$$I_5 = I_6 = 160\mu A$$
$$\left(\frac{W}{L}\right)_{5A,5B} = \frac{2 * I_5}{K_P * (V_{ds})^2} = \frac{2 * 160 * 10^{-6}}{2.64 * 10^{-5} * (0.5)^2}$$
$$\left(\frac{W}{L}\right)_{5A,5B} = 49$$

$$\left(\frac{W}{L}\right)_{6A,6B} = \frac{2 * I_6}{K_N * (V_{ds})^2} = \frac{2 * 160 * 10^{-6}}{6.33 * 10^{-5} * (0.5)^2}$$

$$\left(\frac{W}{L}\right)_{6A,6B} = 21$$

Where V_{ds} we have already calculated in step 2.

STEP 3: Now we are left with the design of differential pair transistors.

$$g_{m1} = g_{m2} = 2 * \pi * GB * C_L = 2 * 3.14 * 10 * 10^6 * 15 * 10^{-12}$$

$$g_{m1} = g_{m2} = 9.42 * 10^{-4} S$$

$$\left(\frac{W}{L}\right)_{1A,1B} = \frac{g_{m1}{}^2}{K_P * I_3} = \frac{(9.42 * 10^{-4})^2}{2.64 * 10^{-5} * 200 * 10^{-6}}$$

$$\left(\frac{W}{L}\right)_{1A,1B} = 168$$

$$\left(\frac{W}{L}\right)_{2A,2B} = \frac{g_{m2}{}^2}{K_N * I_4} = \frac{(9.42 * 10^{-4})^2}{6.33 * 10^{-5} * 200 * 10^{-6}}$$

$$\left(\frac{W}{L}\right)_{2A,2B} = 70$$

STEP 4: Lastly the tail transistors are designed using input common mode range specification. From [1] we have

$$V_{ds4} = V_{in}(\min) - V_{gs2A}$$

$$V_{ds4} = 1 - 0.8 = 0.2V$$

$$V_{gs2A} = \left(\sqrt{\frac{I_4}{K_N * \left(W/L\right)_{2A}}}\right) + V_{TN}$$

$$V_{gs2A} = \left(\sqrt{\frac{200*10^{-6}}{6.33*10^{-5}*70}} \right) + 0.62 = 0.8V$$

$$\left(\frac{W}{L} \right)_4 = \frac{2*I_4}{K_N*(V_{ds4})^2} = \frac{2*200*10^{-6}}{6.33*10^{-5}*(0.5)^2}$$

$$\left(\frac{W}{L} \right)_4 = 26$$

For keeping the transistor in deep saturation we have increased the drain to source voltage. Using the mobility ratio we have

$$\left(\frac{W}{L} \right)_3 = 61$$

The calculated values of transistor ratios are summarized in table 3.

MOS	M1A	M1B	M2A	M2B	M3	M4	M5A	M5B
W/L	168	168	70	70	61	26	49	49

MOS	M6A	M6B	M7A	M7B	M8A	M8B
W/L	21	21	79	79	33	33

Table 3

INTRODUCTION TO TANNER TOOL

Tanner tool is a Spice Computer Analysis Programmed for Analog Integrated Circuits. Tanner tool consists of the following Engine Machines

1. S-EDIT (Schematic Edit)
2. T-EDIT (Simulation Edit)
3. W-EDIT (Waveforms Edit)
4. L-EDIT (Layout Edit)

Using these engine tools, spice programme provides facility to the user to design & simulate new ideas in Analog Integrated Circuits before going to the time consuming & costly process of chip fabrication.

6.1 SCHEMATIC EDIT TOOL (S-EDIT)

S-Edit is hierarchy of files, modules & pages. It introduces symbol & schematic modes. S-Edit provides the facility of:

1. Beginning a design.
2. Viewing, drawing & editing of objects.
3. Design connectivity.
4. Properties, net lists & simulation.
5. Instance & browse schematic & symbol mode.

BEGINNING A DESIGN: It explains the design process in detail in terms of file module operation and module.

Browser: Effective schematic design requires a working knowledge of the S-Edit design hierarchy of files & modules. S-Edit design files consist of modules. A module is a functional unit of design such as a transistor, a gate and an amplifier.

Modules contain two components:

1) **Primitives –** Geometrical objects created with drawing tools.
2) **Instances** – References to other modules in file. The instanced module is the original.

S-Edit has two viewing modes:

1) **Schematic Mode:** To create or view a schematic, we operate in schematic mode.
2) **Symbol Mode:** It represents symbol of a larger functional unit such as operational amplifier.

6.2 T-SPICE Pro Circuit ANALYSIS

Let's have an introduction to the integrated components of the T- Spice Pro circuit analysis suite.

Schematic data files (**.sdb**) describing the circuits to be analyzed in *graphical* form, for display and editing by S- Edit™ Schematic Editor.

Simulation input files (**.sp**) describing the circuits to be analyzed in *textual* form, for editing and simulation by T- Spice™ Circuit Simulator.

Simulation output files (**.out**) containing the numerical results of the circuit analyses, for manipulation and display by W- Edit™ Waveform Viewer.

6.2.1 CIRCUIT SIMULATOR (T-SPICE)

T- Spice Pro's *waveform probing* feature integrates S- Edit, T- Spice, and W-Edit to allow individual points in a circuit to be specified and analyzed. Let's discuss a few analysis:

The heart of T-Spice operation is the input file (also known as the circuit description, the net list & the input deck). This is a plain text file that contains the device statement & simulation commands, drawn from the SPICE circuit description language with which T-Spice constructs a model of the circuit to be simulated. Input files can be created and modified with any text editor.T-Spice is a tool used for simulation of the circuit. It provides the facility of

1. Design Simulation
2. Simulation Commands
3. Device Statements
4. User-Designed External Models
5. Small Signal & Noise Models

T-Spice uses Kirchoff's Current Law (KCL) to solve circuit problems. To T-Spice, a circuit is a set of devices attached to nodes. The voltage at all nodes represents the circuit state. T-Spice solves for a set of node voltage that satisfied KCL (implying that sum of currents flowing into each node is zero). In order to evaluate whether a set of node voltages is a solution, T-Spice computes and sums all the current flowing out of each device into nodes connected to it (its terminals). The relationship between the voltages at device terminals and the currents through the terminal is determined by the device model for a resistor of resistance R is

$$I = \Delta V / R$$

Where ΔV represents the voltage difference across the device.

Let's discuss a few analysis:

DC Operating Point Analysis

DC operating point analysis finds a circuit's steady- state condition, obtained (in principle) after the input voltages have been applied for an infinite amount of time. The .include command causes T- Spice to read in the contents of the model file ml2_

125 .md for the evaluation of nmos and pmos transistors. This file consists of two .model commands, describing two MOSFET models called nmos and pmos. For example:

.model pmos pmos

+ Level= 2 Ld=. 03000u Tox= 225. 000E- 10

+ Nsub= 6.575441E+ 16 Vto=- 0. 63025 Kp= 2.635440E- 05

+ Gamma= 0.618101 Phi=. 541111 Uo= 361.941

+ Uexp= 8.886957E- 02 Ucrit= 637449 Delta= 0. 0

+ Vmax= 63253.3 Xj= 0.112799u Lambda= 0.0

+ Nfs= 1.668437E+ 11 Neff= 0. 64354 Nss= 3.00E+ 10

+ Tpg=- 1.000 Rsh= 150 Cgso= 3.35E- 10

+ Cgdo= 3.35E- 10 Cj= 4.75E- 04 Mj=. 341

+ Cjsw= 2.23E- 10 Mjsw=. 307

ml2_ 125. md assigns values to various Level 2 MOSFET model parameters for both n - and p -type devices. When read by the input file, these parameters are used to evaluate Level 2 MOSFET model equations, and the results are used to construct internal tables of current and charge values. Values read or interpolated from these tables are used in the computations called for by the simulation. Two transistors, mn1 and m1p, are defined in invert1. sp . These are MOSFETs, as indicated by the key letter m, which begins their names. Following each transistor name are the names of its terminals. The required order of terminal names is: drain – gate – source – bulk. Then the model name (nmos or pmos), and physical characteristics such as length and width, are specified. The .op command performs a DC operating point calculation and writes the results to the file specified in the Simulate > Start Simulation dialog. The output file lists the DC operating point information for the circuit described by the input file.

DC Transfer Analysis

DC transfer analysis is used to study the voltage or current at one set of points in a circuit as a function of the voltage or current at another set of points. This is done by sweeping the source variables over specified ranges, and recording the output. A list of sources to be swept, and the voltage ranges across which the sweeps are to take place follow the .dc command, indicating transfer analysis. The transfer analysis will be performed as follows: vdd will be set at 2 volts and vin will be swept over its specified range; vdd will then be incremented to 2.5 volts and vin will be reswept over its range; and so on, until vdd reaches the upper limit of its range.

The .dc command ignores the values assigned to the voltage sources vdd and vin in the voltage source statements, but they must still be declared in those statements. The results for nodes in and out are reported by the .print dc command to the specified destination.

Transient Analysis

Transient analysis provides information on how circuit elements vary with time. The basic T- Spice command for transient analysis has three modes. In the default mode, the DC operating point is computed, and T- Spice uses this as the starting point for the transient simulation.

The. tran command (.tran 2n 600n) specifies the characteristics of the transient analysis to be performed: it will last for 600 nanoseconds, with time steps no larger than 2 nanoseconds.

AC Analysis

AC analysis characterizes the circuit's behavior dependence on small- signal input frequency. It involves three steps: (1) calculating the DC operating point; (2) linearizing the circuit; and (3) solving the linearized circuit for each frequency. For example, we have

vdiff in2 in1 -0.0007 AC 1 90

.ac DEC 5 1 100MEG

vdiff sets the DC voltage difference between nodes in2 and in1 to –0. 0007 volts; its AC magnitude is 1 volt and its AC phase is 90 degrees. The .ac command performs an AC analysis. Following the .ac keyword is information concerning the frequencies to be swept during the analysis. In this case, the frequency is swept logarithmically, by decades (DEC); 5 data points are to be included per decade; the starting frequency is 1 Hz and the ending frequency is 100 MHz. The .print commands write the voltage magnitude (in decibels) and phase (in degrees), respectively, for the node out to the specified file.

The. acmodel command writes the small- signal model parameters and operating point voltages and currents for all circuit devices

Noise Analysis

Real circuits, of course, are never immune from small, "random" fluctuations in voltage and current levels. In T- Spice, the influence of noise in a circuit can be simulated and reported in conjunction with AC analysis. The purpose of noise analysis is to compute the effect of the noise associated with various circuit devices on an output voltage or voltages as a function of frequency. Noise analysis is performed in conjunction with AC analysis; if the .ac command is missing, then the .noise command is ignored. With the .ac command present, the. noise command causes noise analysis to be performed at the same frequencies: starting at 1 Hz, ending at 100 MHz, 5 data points per decade. The .noise command takes two arguments: the output at which the effects of noise are to be computed, and the input at which the noise can be considered to be concentrated for the purposes of estimating the equivalent noise spectral density. The .print command is used to print results.

6.3 WAVEFORM-EDIT

The ability to visualize the complex numerical data resulting from VLSI circuit simulation is critical to testing, understanding & improving these circuits. W-Edit is a waveform viewer that provides ease of use, power & speed in a flexible environment designed for graphical data representation. The advantages of W-Edit includes:

1. Tight Integration with T-spice, Tanner EDA's circuit level simulator. W-Edit can chart data generated by T-spice directly, without modification of the

output text data files. The data can also be charted dynamically as it is produced during the simulation.

2. Charts can automatically configured for the type of data being presented.
3. A data is treated by W-Edit as a unit called a trace. Multiple traces from different output files can be viewed simultaneously in single or several windows; traces can be copied and moved between charts & windows. Trace arithmetic can be performed on existed tracing to create new ones.
4. Chart views can be panned back & forth and zoomed in & out, including specifying the exact X-Y coordinate range.
5. Properties of axes, traces, rides, charts, text & colors can be customized.

Numerical data is input to W-Edit in the form of plain or binary text files. Header & Comment information supplied by T-Spice is used for automatic chart configuration. Runtime update of results is made possible by linking W-Edit to a running simulation in T-Spice.

W-Edit saves data with chart, trace, axis & environment settings in files with the WDB (W-Edit Database).

6.4 LAY-OUT (L-EDIT)

It is a tool that represents the masks that are used to fabricate an integrated circuit. It describes a layout design in terms of files, cells & mask primitives. On the layout level, the component parameters are totally different from schematic level. So it provides the facility to the user to analyse the response of the circuit before forwarding it to the time consuming & costly process of fabrication. There are rules for designing layout diagram of a schematic circuit using which user can compare the output response with the expected one.

L- Edit: An Integrated Circuit Layout Tool

In L- Edit, layers are associated with masks used in the fabrication process. Different layers can be conveniently represented by different colors and patterns. L- Edit describes a layout design in terms of files, cells, instances, and mask primitives. You may load as many files as desired into memory. A file may be composed of any number of cells. These cells may be hierarchically related, as in a typical design, or they may be independent, as in a "library" file. Cells may contain any number or combination of mask primitives and instances of other cells.

Cells: The Basic Building Blocks

The basic building block of the integrated circuit design in L- Edit is a cell.
Design layout occurs within cells. A cell can:

- Contain part or all of the entire design.
- Be referenced in other cells as a sub- cell, or instance.
- Be made up entirely of instances of other cells.
- Contain original drawn objects, or primitives.
- Be made up entirely of primitives or a combination of primitives and instances of other cells.

Hierarchy

L- Edit supports fully hierarchical mask design. Cells may contain instances of other cells. An instance is a reference to a cell; should you edit the instanced cell, the change is reflected in all the instances of that cell. Instances simplify the process of updating a design, and also reduce data storage requirements, because an instance does not need to store all the data within the instanced cell — instead, only a reference to the instanced cell is stored, along with information on the position of the instance and on how the instance may be rotated and mirrored. There is no preset limit to the size or complexity of the hierarchy. Cells may contain instances of others cells that in turn contain instances of other cells, to an arbitrary number of levels (subject only to hardware constraints).

L- Edit does not use a "separated" hierarchy: instances and primitives may coexist in the same cell at any level in the hierarchy. Design files are self- contained. The "pointer" to a cell contained in an instance always points to a cell within the same design file. When cells are copied from one file to another, L- Edit automatically copies across any cells that are instanced by the copied cell, to maintain the self-contained nature of the destination file.

Design Rules

Manufacturing constraints can be defined in L- Edit as design rules. Layouts can be checked against these design rules.

Design Features

L- Edit is a full- custom mask editor. Manual layout can be accomplished more quickly because of L- Edit's intuitive user interface. In addition, one can construct special structures to utilize a technology without, worrying about problems caused by automatic transformations. Phototransistors, guard bars, vertical and horizontal bipolar transistors, static structures, and Schottky diodes, for example, are as easy to design in CMOS- Bulk technology as are conventional MOS transistors.

Floor plans

L- Edit is a manual floor planning tool. You have the choice of displaying instances in outline, identified only by name, or as fully fleshed- out mask geometry. When you display your design in outline, you can manipulate the arrangement of the cells in your design quickly and easily to achieve the desired floor plan.

One can manipulate instances at any level in the hierarchy, with insides hidden or displayed, using the same graphical move/ select operations or rotation/ mirror commands that you use on primitive mask geometry.

Memory Limits

In L- Edit, one can make your design files as large as one like, given available RAM and disk space.

Hard Copy

L- Edit provides the capability to print hard copy of the design. A multiage option allows very large plots to be printed to a specific scale on multiple 8 1/ 2 x 11 inch pages. An L- Edit macro is available to support large- format, high- resolution, color plotting on inkjet plotters.

Variable Grid

L- Edit's grid options support lambda- based design as well as micron- based and mil- based design.

Error Recovery

L- Edit's error- trapping mechanism catches system errors and in most cases provides a means to recover without losing or damaging data.

L- Edit Modules

- L- Edit ™: a layout editor
- L- Edit ¤ Extract ™: a layout extractor
- L- Edit ¤ DRC ™: a design rule checker

L- Edit is a full- featured, high- performance, interactive, graphical mask layout editor. L- Edit generates layouts quickly and easily, supports fully hierarchical designs, and allows an unlimited number of layers, cells, and levels of hierarchy. It includes all major drawing primitives and supports 90°, 45°, and all- angle drawing modes.

L- Edit ¤ Extract creates SPICE- compatible circuit netlists from L- Edit layouts. It can recognize active and passive devices, sub circuits, and the most common device parameters, including resistance, capacitance, device length, width, and area, and device source and drain area.

L- Edit ¤ DRC features user- programmable rules and handles minimum width, exact width, minimum space, minimum surround, non- exist, overlap, and extension rules. It can handle full chip and region- only DRC. DRC offers Error Browser and Object Browser functions for quickly and easily cycling through rule- checking errors.

ANALOG LAYOUT DESIGN

7.1 LAYOUT DESIGN RULES

The physical mask layout of any circuit to be manufactured using a particular process must confirm to a set of geometric constraints or rules, which are generally called layout design rules. These rules usually specify the minimum allowable line widths for physical objects on chip such as metal and polysilicon interconnects or diffusion areas, minimum feature dimensions, and minimum allowable separations between two such features. If a metal line width is too small, for example, it is possible for the line to break during the fabrication process or afterwards, resulting in an open circuit. If the two lines are placed too close to each other in the layout, they may form an unwanted short circuit by merging during or after the fabrication process. The main objective of design rules is to achieve, for any circuit to be manufactured with a particular process, a high overall yield and reliability while using the smallest possible silicon area.

There is usually trade off between higher yield, which is obtained through conservative geometries, and better area efficiency, which is obtained through aggressive, high-density placement of various features on the chip. The layout design rules, which are specified for a particular fabrication process normally, represent a reasonable optimum point in terms of yield and density. It must be emphasized, however, that the design rules do not represent strict boundaries, which separate "correct" designs from "incorrect" ones. A layout which violates some of the specified design rules may still result in an operational circuit with reasonable yield, whereas another layout observing all specified design rules may result in a circuit which is not functional and/or has very low yield. To summarize, we can say, in general, that observing the layout rules significantly increases the probability of fabricating a successful product with high yield.

The design rules [18] are usually described in two ways:

1. **Micron rules,** in which the layout constraints such as minimum feature sizes and minimum allowable feature separations are stated in terms of absolute dimensions in micrometers, or,
2. **Lambda rules,** which specify the layout constraints in terms of a single parameter (λ) and thus allow linear, proportional scaling of all geometrical constraints.

Lambda-based design rules were originally devised to simplify the industry-standard micron-based design rules and to allow scaling capability for various processes. It must be emphasized, however, that most of the sub-micron CMOS process design rules do not lend themselves to straightforward linear scaling. The use of lambda based design rules must therefore be handled with caution in sub-micron geometries.

The design rules define geometrical relations referring to the following four possibilities:

- Element width, W_{min}: it is the minimum (or the maximum) width allowed for a given element. It avoids possibly opening or vanishing of the element. For example, we have a rule defining the minimum width of the poly gate and a rule defining the minimum size of poly-metal contacts.
- Element spacing ΔW_{min}: this is the minimum distance between two elements. This rule avoids shortening. The elements can be of the same kind (for example metal-metal) or of a different kind. For example, we have a rule defining the minimum distance between two metal lines or the minimum distance between a poly line and unrelated diffusion.
- Inner overlap $W_{in,min}$: is the minimum separation between two elements that we design one inside the other. This rule avoids the two elements detaching. For example, we have a rule defining the inner overlap of the contact over or below a metal.

- External extension, $W_{ex,min}$: is the minimum extension of an element overlapping another element. This kind of rule ensures that the two elements are fully overlapped. For example, we use a design rule to ensure that the poly gate always crosses the active area.

The above four categories of design rules are specified for all the possible layers used by technology. The above description of possible rules refers to the minimum spacing. However, some rules require the assigned figure to be "exact". Therefore, excepting the latter case, the designer can exceed the minimum spacing by an extent considered appropriate.

7.2 LAYOUT OF TRANSISTORS

The final step in integrated design is physical description. This consists of defining the masks to be used for processing. An MOS transistor is achieved by the simple overlap of two rectangles: one defining the active area and the other defining the polysilicon gate [2,18,21]. (Figure 7.1)

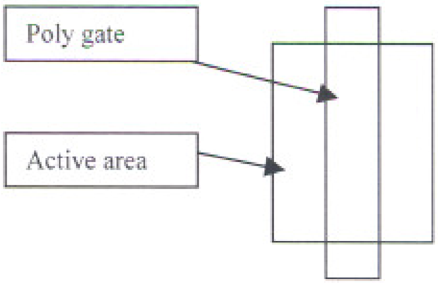


Figure 7.1: The two layers that achieve a transistor

The parts of the active area that are not protected by the gate originate the source and drain, while the part protected by the gate forms the transistor channel . To ensure that the source and drain are separated, even in presence of fabrication inaccuracies, the gate overlaps the active area to a given extent, its value being defined by the design rules of the technology used.

The physical design is not limited to the masks of the active area and polysilicon. When the transistor must be realized in the well, a suitable pattern must be defined. Moreover it is necessary to arrange the connections of source, drain and gate together with the substrate and well biasing. A typical layout of a MOS transistor (sitting in the well) is shown in Figure 7.2. It represents a pattern typical of analog circuits: the aspect ratio (W/L) of the transistor is not at a minimum, as is usually the case for analog designs.

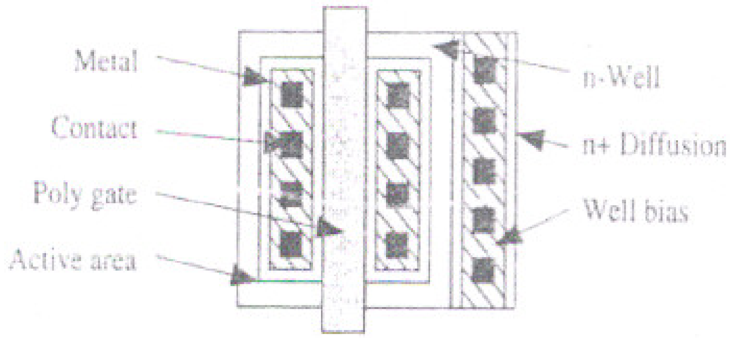


Figure 7.2: Layout of a p-channel transistor (inside an n-well)

The key points to consider when we draw transistor layouts are the following:

- Parasitic resistances at source and drain must be kept as low as possible.
- Parasitic capacitances should be minimized.
- Matching between paired elements is very important.

Concerning the first condition, we should remember that drain and source diffusions have a given sheet resistance. With only a few squares, we can achieve the hundreds of ohms of resistance: even with a current as low as few tens of μA we can have drop voltages of milivolts. Therefore, as shown in Figure 7.2, we must use multiple contacts on the top of source and drain regions to avoid parasitic transversal drop voltages. Designers prefer multiple contacts placed at a minimum distance instead of using a single large contact placed at a minimum distance instead of using a single large contact. Many contacts placed at a minimum distance instead of using a single large contact. Many contacts placed close to each other make the surface of metal connections smoother than when using only one contact; this prevents micro cracks in the metal that can be a source of failure.

Parasitic capacitances derive from the reverse source-substrate or drain substrate diodes. We have just seen that this is useful in establishing good contacts. Hence, source and drain area must be large enough to accommodate contacts and to fulfil the design rules. However, it is possible to reduce the source and drain area and, consequently, reduce the parasitic capacitances. This is achieved using the layout shown in Figure 7.3.

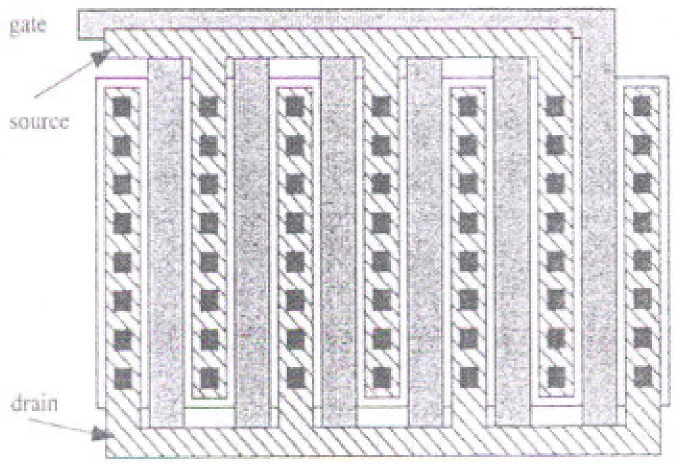


Figure 7.3: Interdigitized transistor

The transistor is split into a given number parts that are connected in parallel. We can see that most of the source and drain area is used doubly allowing the left and right parts of the transistors to be connected. It follows that the parasitic capacitances can be reduced up to a factor of 2.

Matching is very important when we have to design current mirrors and differential pairs. In general, bad matching produces high offset. Therefore, we have to use layouts that optimize matching. This is achieved by providing the best symmetrical conditions. Transistors with different orientation Figure 7.4(a) match badly. Moreover, we can suffer mismatch if the current in transistors is flowing in opposite directions Figure 7.4(b).

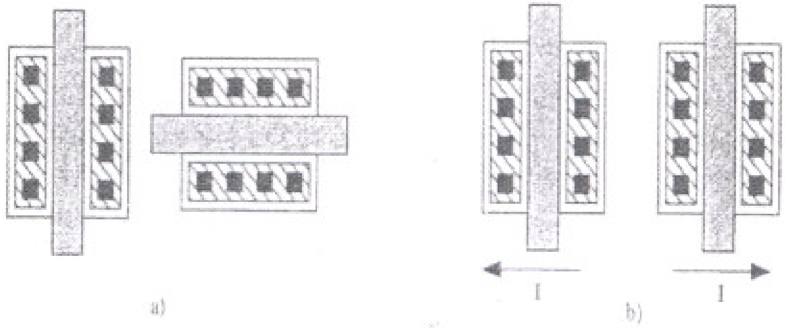


Figure 7.4: Badly matching transistors: a) bad orientation b) with opposite current flow

The best methods of achieving good matching are shown in Figure 7.5. We assume that the two transistors that should match have one of the terminals (source or drain) in common so that we can use the interdigitated arrangement. Each transistor is split into four equal parts; they are interleaved in two by

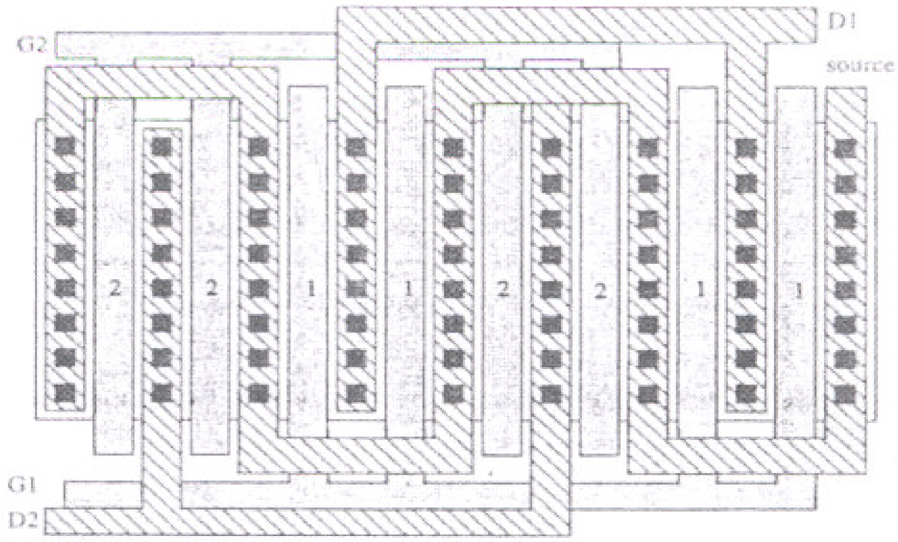


Figure 7.5: Layout of a matched transistor pair

two's so that for one pair of pieces of same transistor we have currents flowing in opposite directions. A final point concerns the biasing of substrate or of the well. This is a very important issue: we have to ensure that the biasing is as close as possible to the active devices. Any noisy signal affecting the substrate or the well should be sunk by the biasing and should not affect current itself. For this reason, any possible silicon space should be used for biasing purposes.

7.3 STACKED LAYOUT

Splitting transistor in a number of fingers favors a stack arrangement and improves the layout matching [18]. For example say in Figure 7.6 presenting the layout of a simple current mirror. The four fingers of each transistor were interleaved so that the centroid of the two transistors is one close to each other. The arrangement of the stack was AABBAABB (where A and B represent the fingers of M1 and M2 respectively). An alternative organization was ABBAABBA that lead to an identical common centroid. However, the boundary conditions are not symmetrical: two fingers of M1 establish the two boundaries while M2 have all the fingers inside the array.

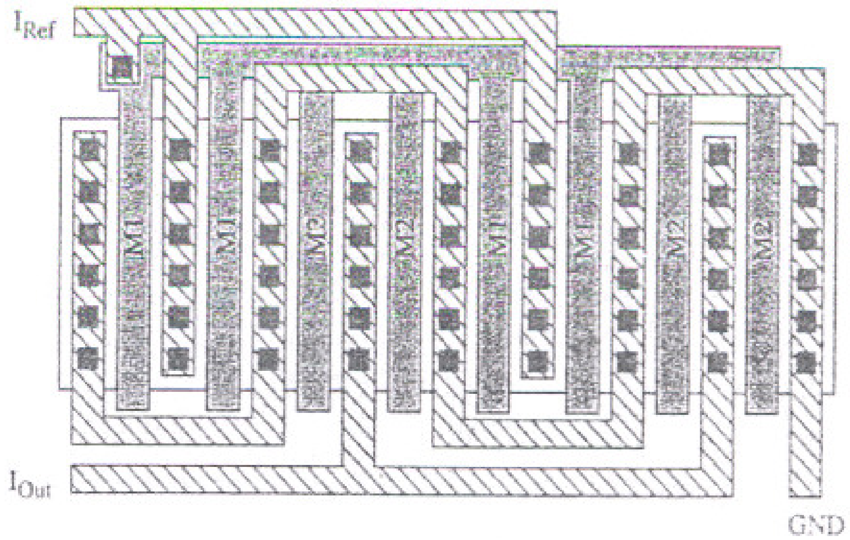


Figure 7.6: Layout of current mirror

The above layout strategy can be generalized for more complex cells. However, it is important to work on a design that favors the stacked approach. The transistors' fingers that should be laid-out on the same stack must have the same width. This is often possible: all the circuits include transistors, which sizes are not particularly critical. A small change of the widths doesn't modify the performances but permits a better layout.

7.4 LAYOUT OF SELF-BIASED COMPARATOR

Using the techniques of analog layout as described above, the layout of self-biased comparator is developed. The schematic of self-biased comparator is as shown in Figure 7.7.

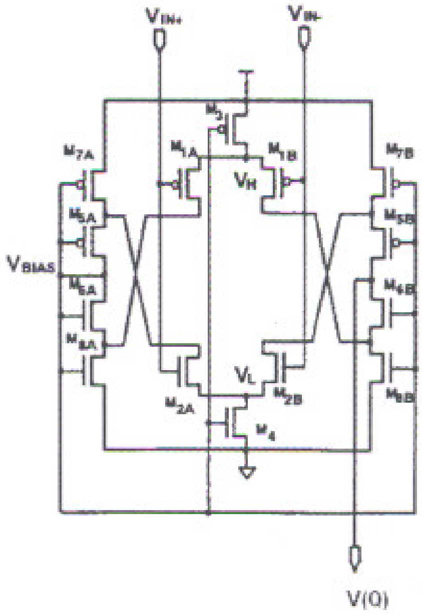


Figure 7.7: Self-biased comparator

For layout, the circuit is divided into four parts. Two parts for p-type transistors and two for n-type. The first part of p-type transistors include the p-differential pair and its corresponding tail transistor i.e. M_{1A} and M_{1B} and M_3. Another part includes the transistor M_{7A}, M_{7B} and M_{5A}, M_{5B}. Similarly, one part of n-type transistors include the n-differential pair and its corresponding tail transistor i.e. M_{2A} and M_{2B} and M_4. Another part includes the transistor M_{6A}, M_{6B} and M_{8A}, M_{8B}. The below scheme shows the possible floor planning.

EEEEE	GGHHGGHHGGHHGGHHGGHH
ABBAABBAABBAABBAABBA	IIIII JJJJJ
CDDCCDDCCD	KKKKK LLLLL
FFFFF	MNNMMNNMMN

The used letters denotes transistor fingers corresponding to

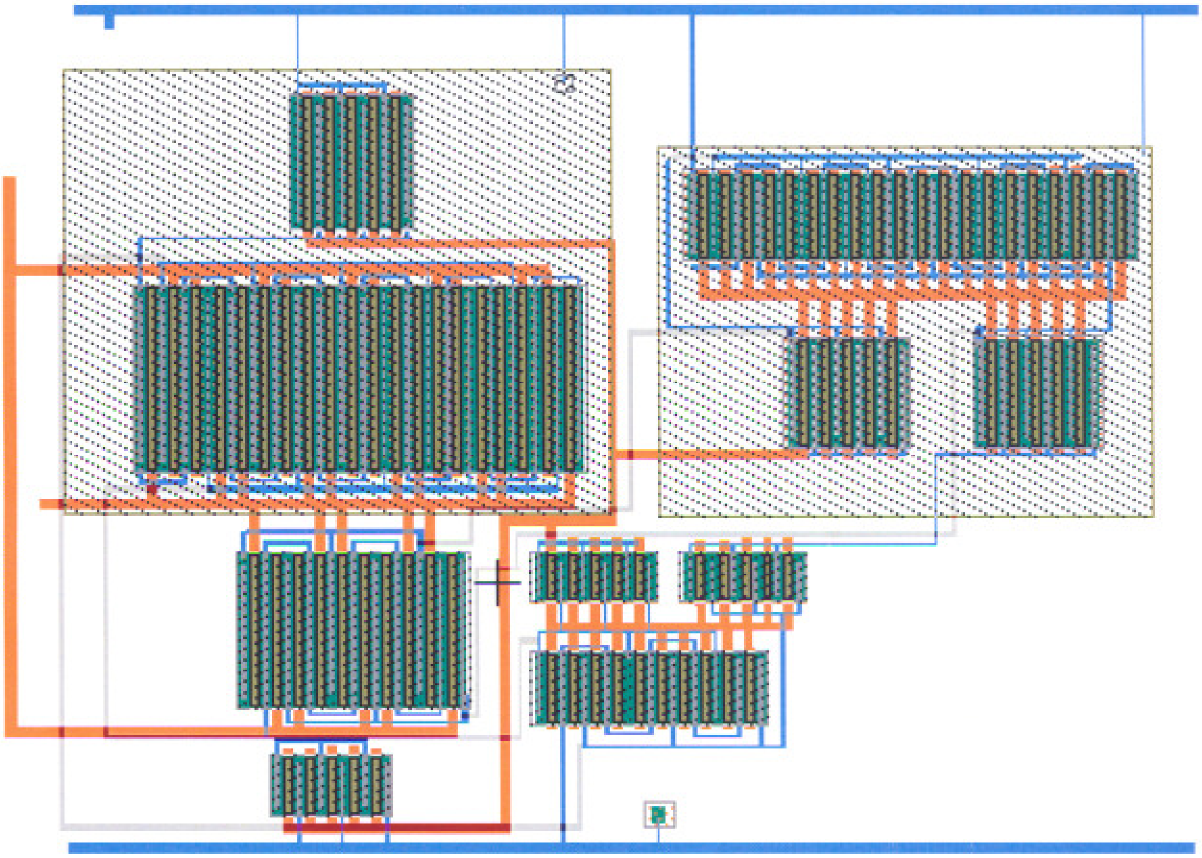
A--- M_{1A}	F--- M_4	K--- M_{6A}
B--- M_{1B}	G--- M_{7A}	L--- M_{6B}
C--- M_{2A}	H--- M_{7B}	M--- M_{8A}
D--- M_{2B}	I--- M_{5A}	N--- M_{8B}
E--- M_3	J--- M_{5B}	

The W/L ratios of transistors are

MOS	M1A	M1B	M2A	M2B	M3	M4	M5A	M5B
W/L	168	168	70	70	61	26	49	49

MOS	M6A	M6B	M7A	M7B	M8A	M8B
W/L	21	21	79	79	33	33

The length is taken 10μm. Figure 7.8 shows the obtained layout. The transistors having large W/L ratio are divided into twenty fingers like p-type differential pair. The push-pull tail transistor pair is divided into five fingers each. Two metal layers favour the interconnections. Only few metal crossings use metal 2.

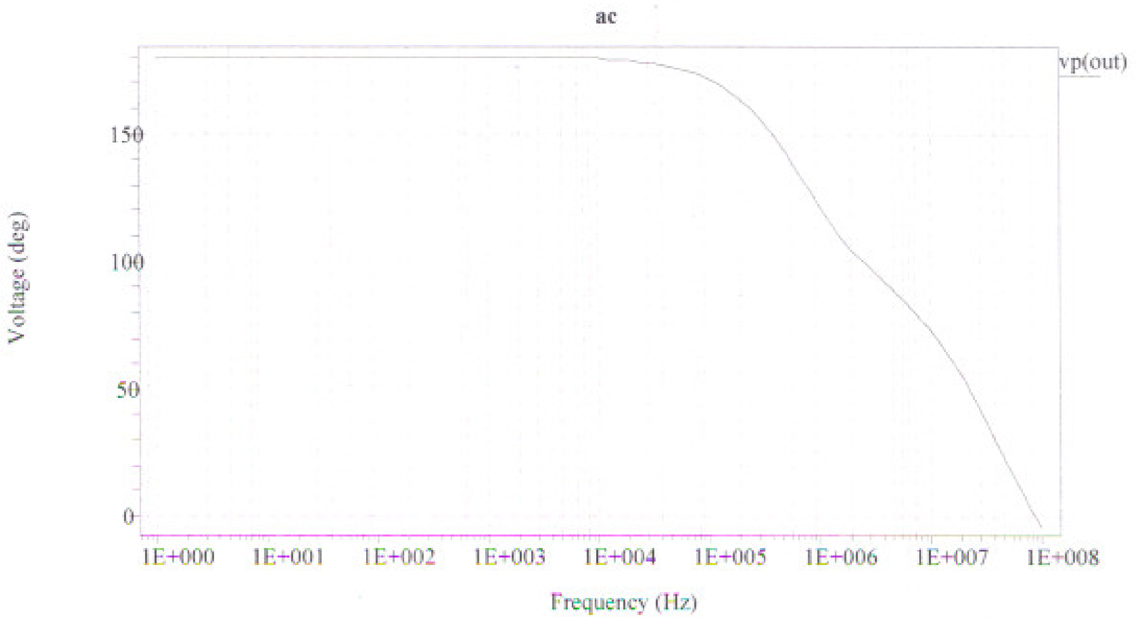


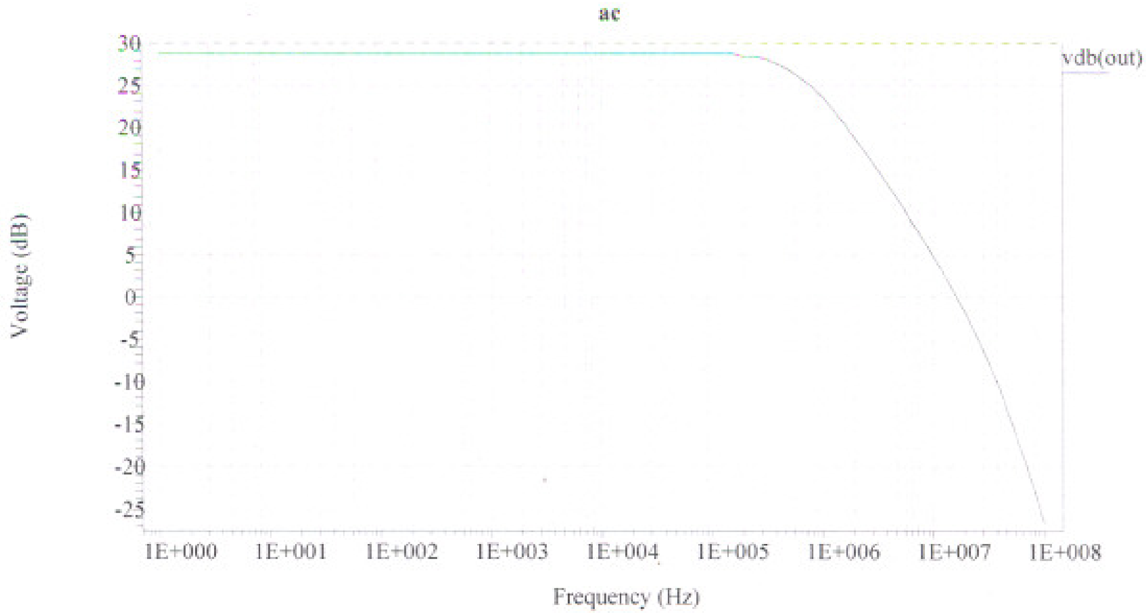
7.8 LAYOUT OF SELF BIASED COMPARATOR

RESULTS AND DISCUSSIONS

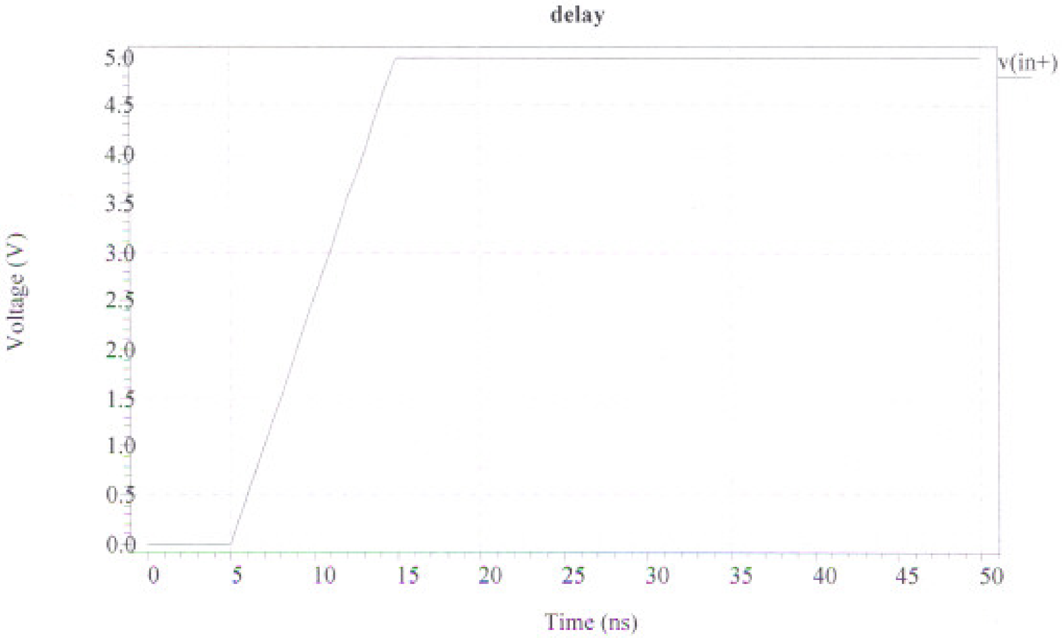
8.1 TWO STAGE OPEN LOOP COMPARATOR

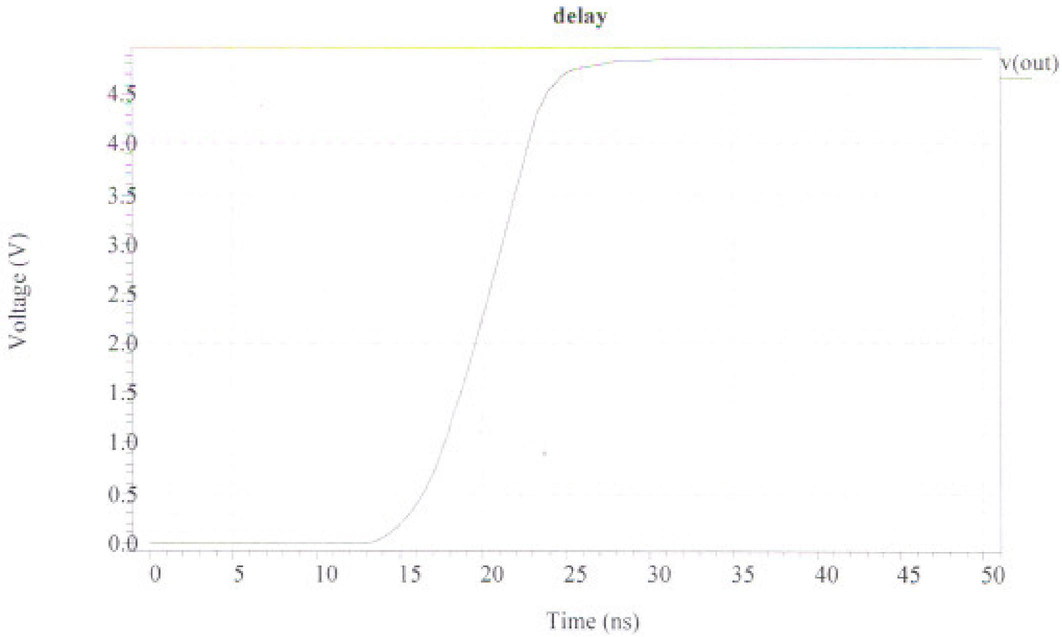
This two-stage comparator is high gain operational amplifier without compensation. The simulation results give us the gain of 32 dB with gain bandwidth (GBW) of 22.84 MHz. The matching of transistors is good i.e. 7 mV. The rising delay is approximately twice less than the falling delay. The power dissipation is quiet large i.e. 9.5 mW but average slew rate is 0.25V/ns which is very high. The minimum voltage difference that it can detect is 0.05 V. The waveforms of simulation results are as shown in following figures.



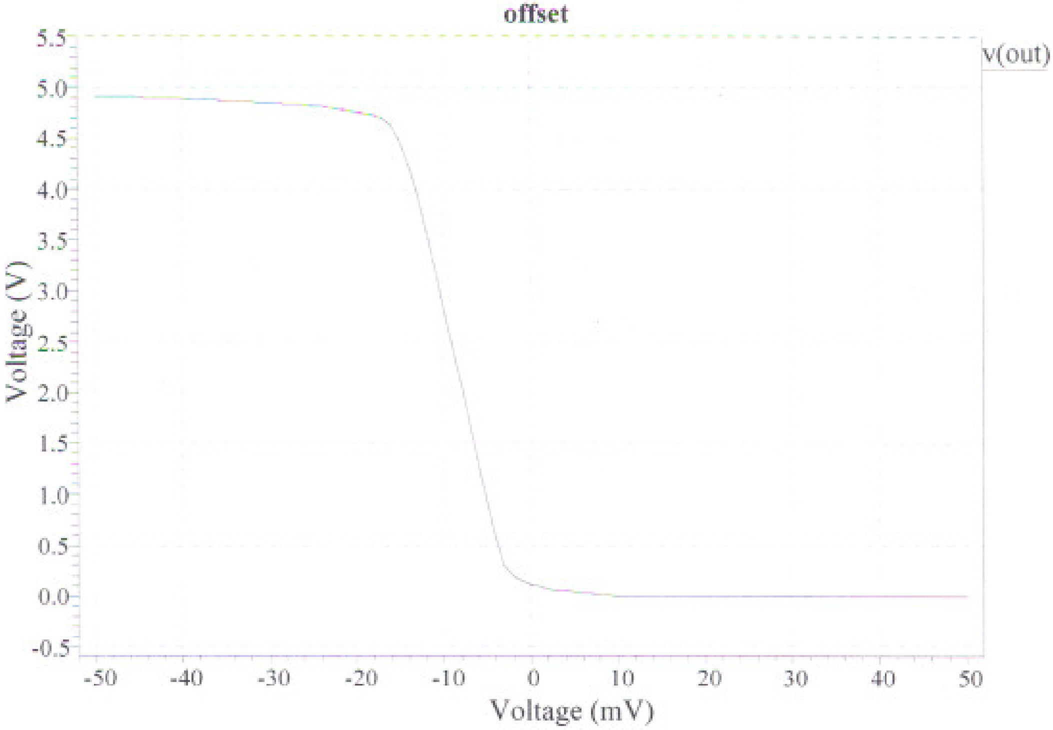


AC response of Two Stage Comparator

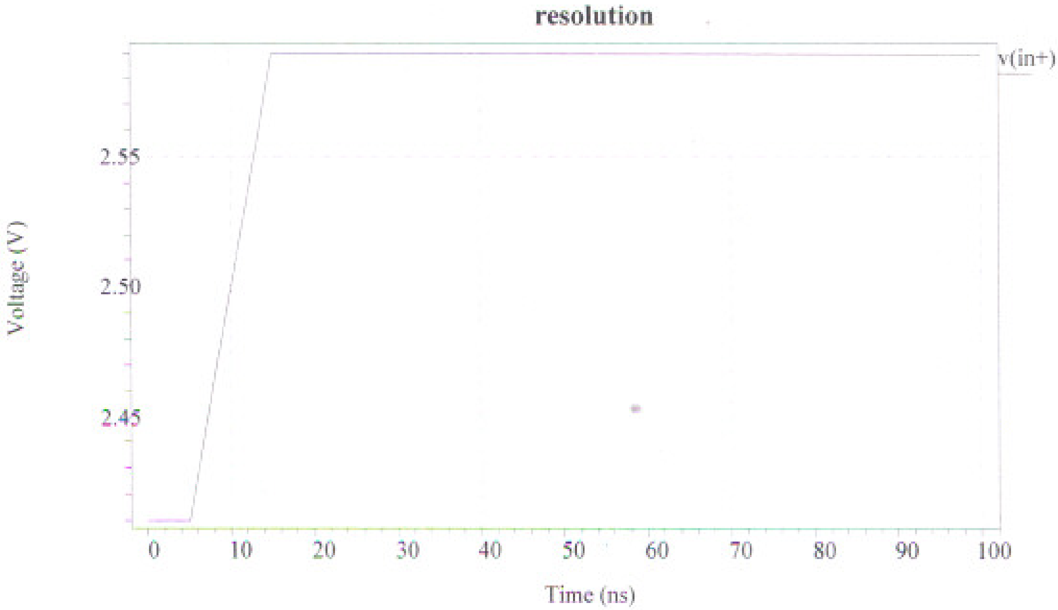


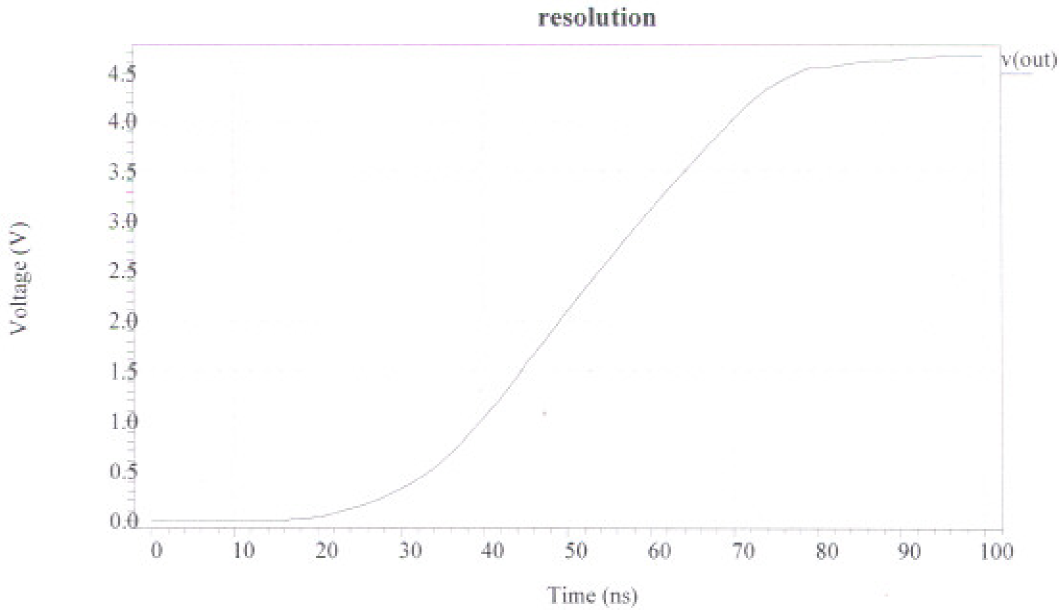


Propagation delay of two stage comparator

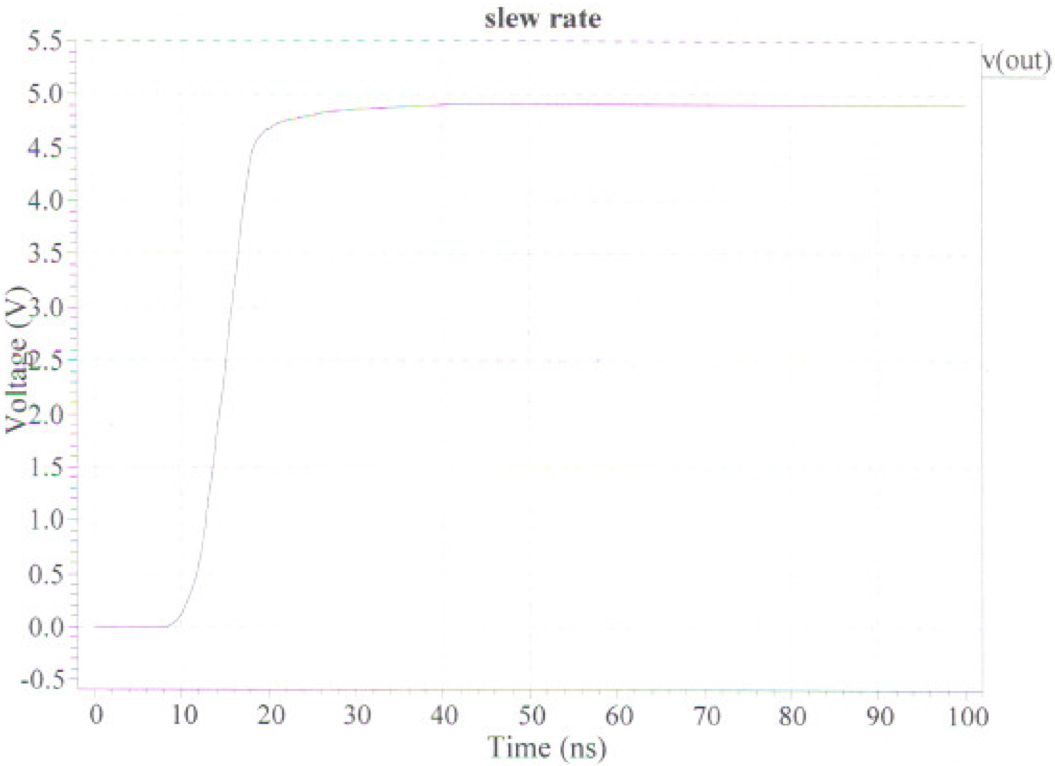


Offset of two stage comparator

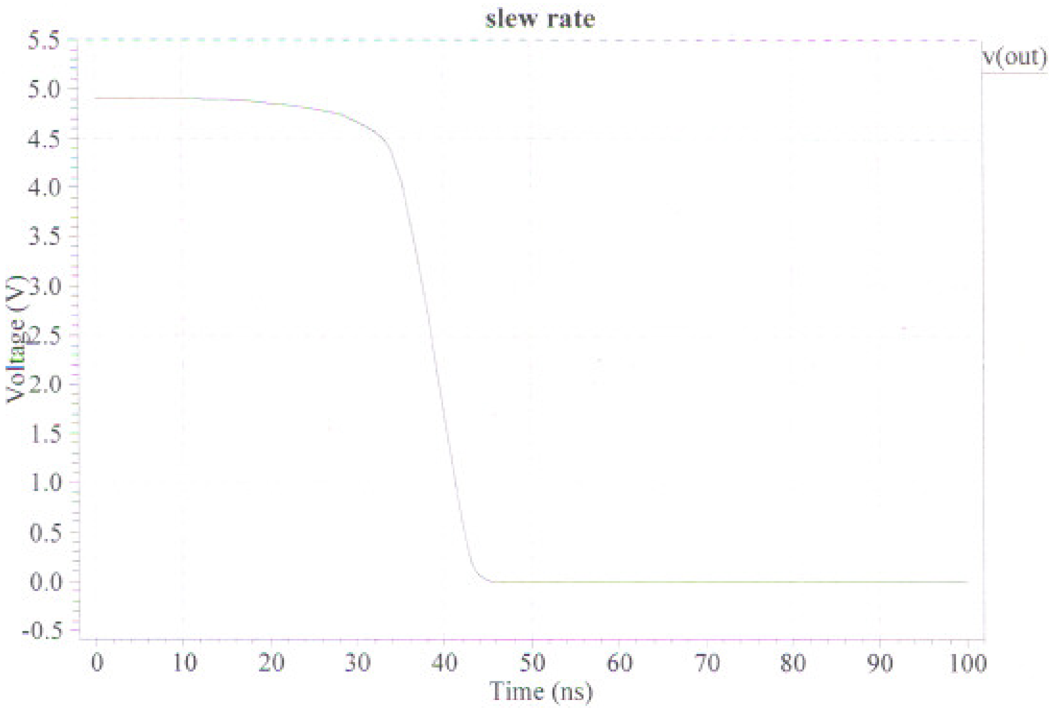




Resolution of two stage comparator



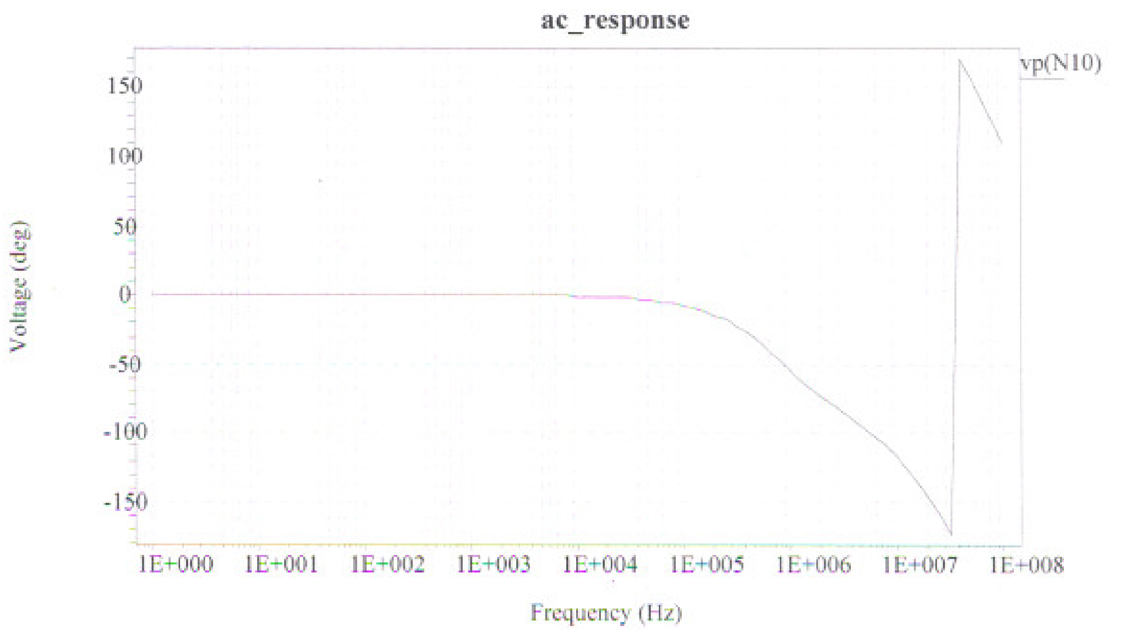
Slew rate of Two Stage comparator

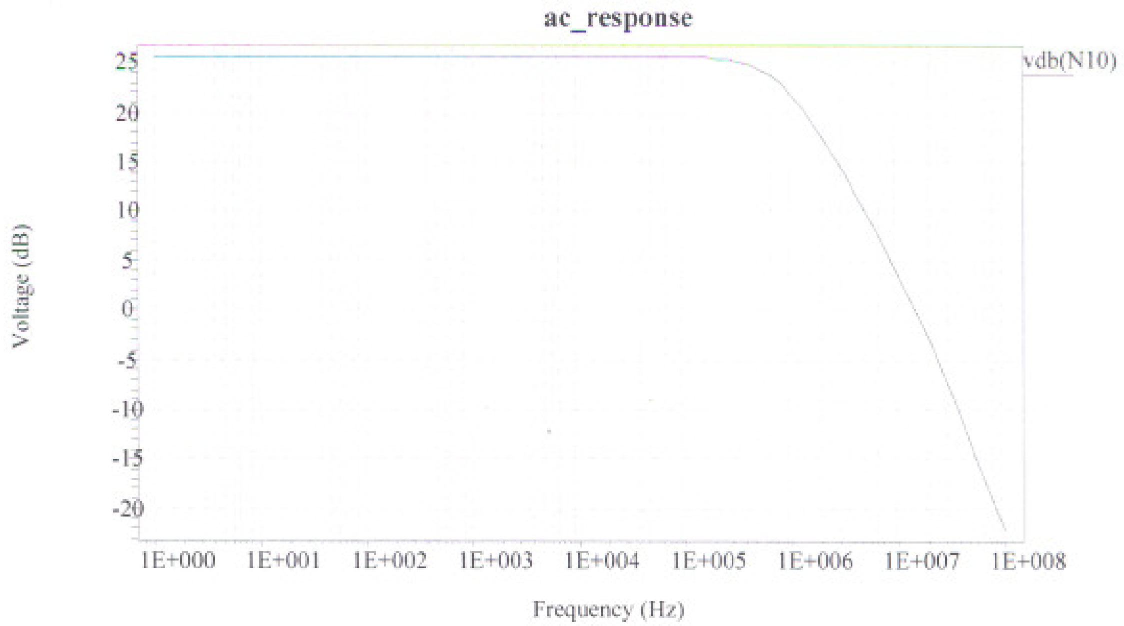


Slew rate of Two Stage comparator

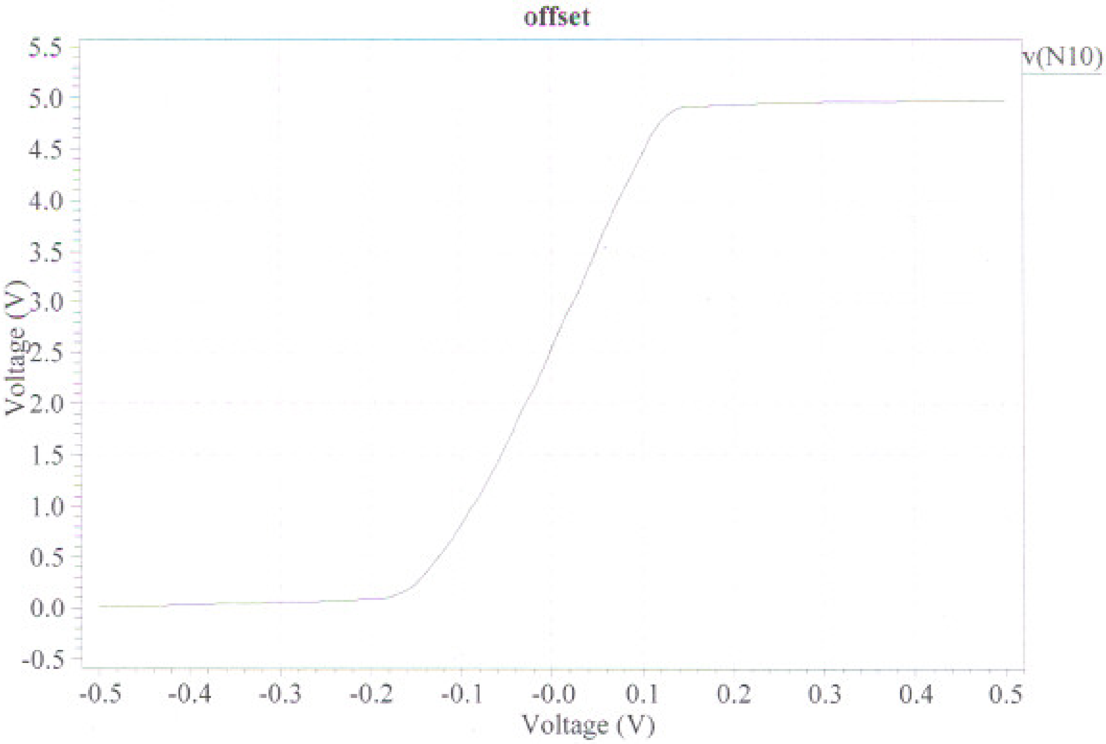
8.2 CLOCKED COMPARATOR USING BASIC LATCH

As we know from the characteristics of regenerative comparators that they are very fast with low power consumption. The simulated results have proved this. The gain of 25.7 dB with GBW 13.33 MHz is satisfactory. The main attraction of this comparator is its very high slew rate for large capacitances of 15 pF i.e. 1.74 V/ns and for load of 1 pF it is 5.8 V/ns as compared to Klinke [15]. The power consumed is just 0.3 mW at 0.11 GHz clock frequency, which is very less [16,17,26]. The resolution of this comparator is 0.02 V. The transient response of comparator shows that the preamplifier has made the input voltage difference to reach the desired value within 2 ns. The simulation results are as shown in figures followed.

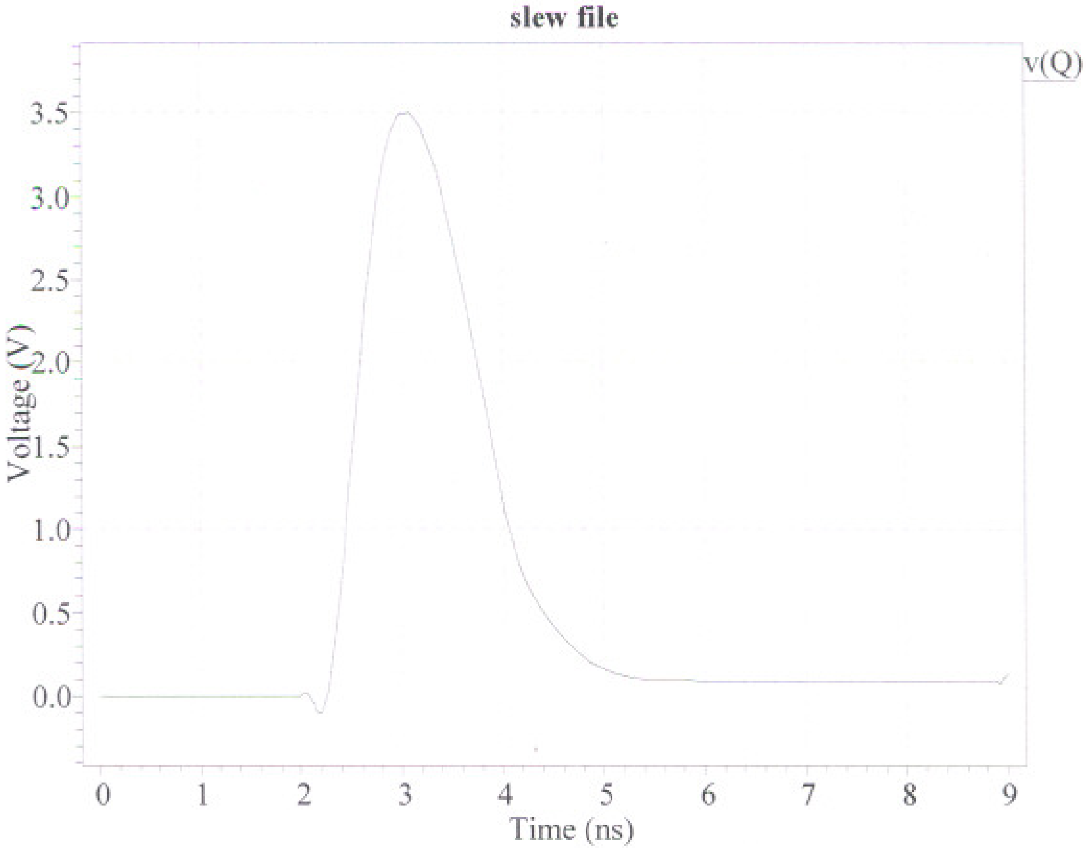




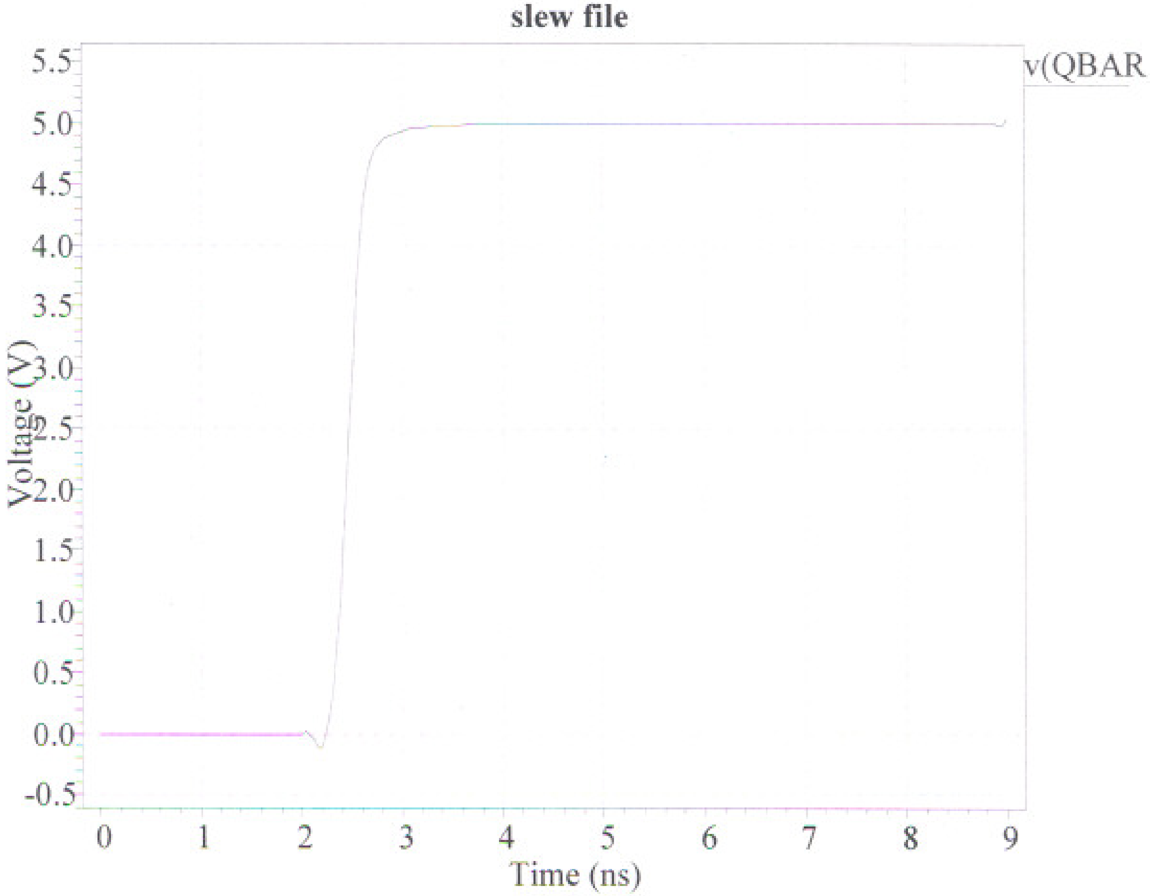
AC response of Clocked comparator



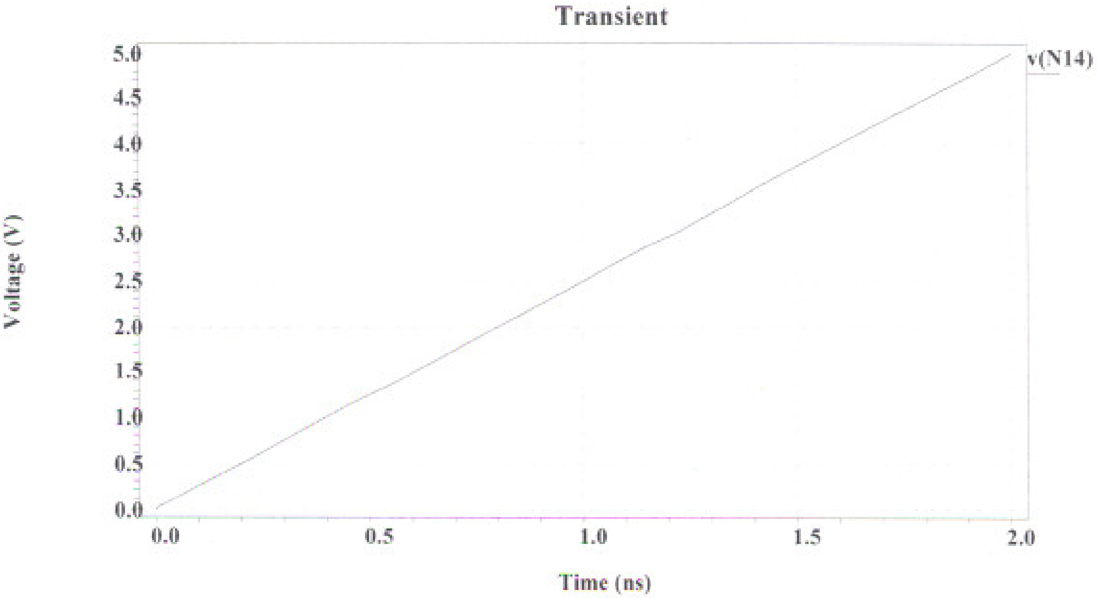
Offset of Clocked comparator

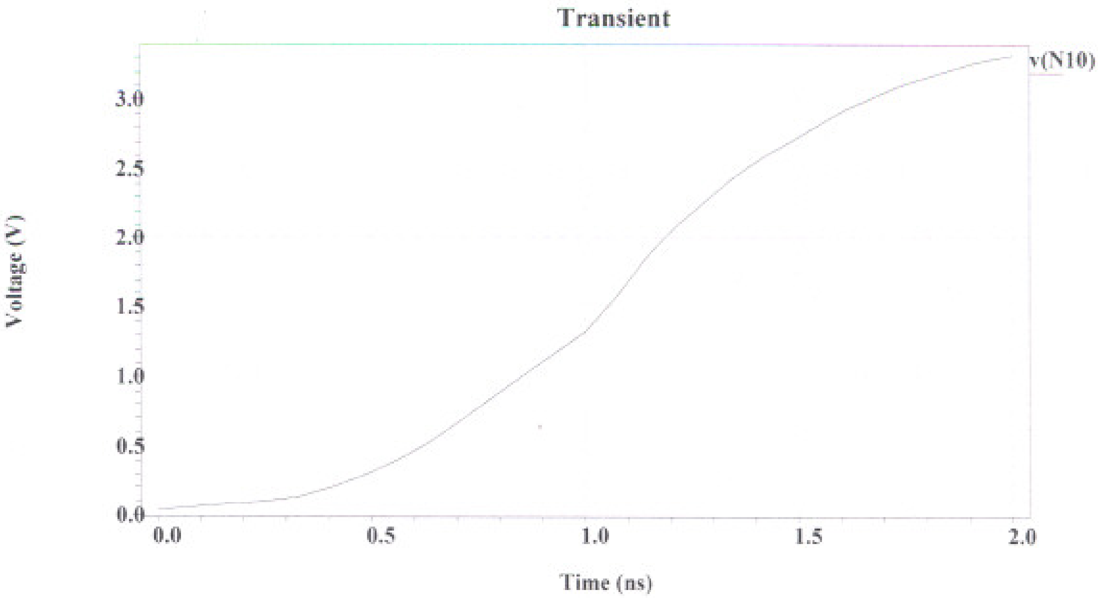


Slew rate of Clocked comparator



Slew rate of Clocked comparator

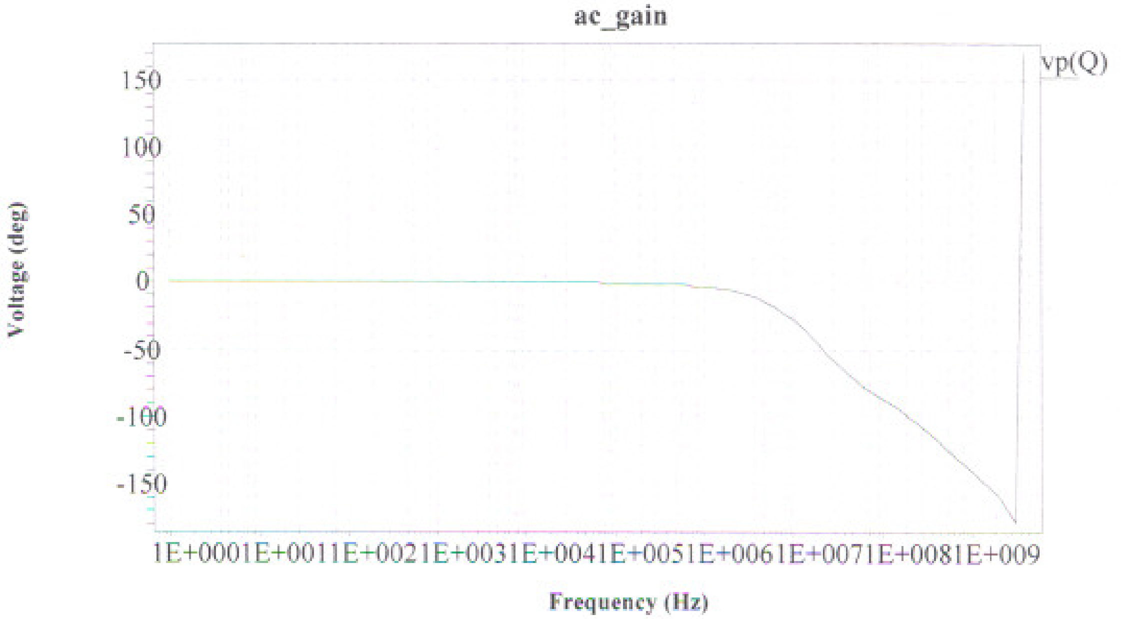


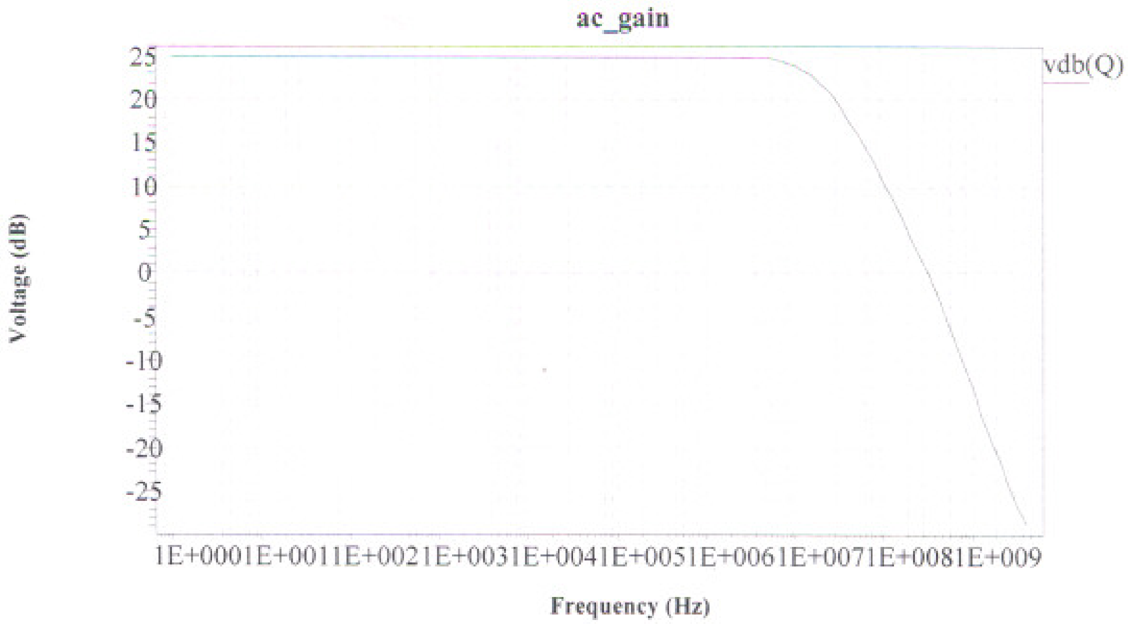


Transient response of Clocked comparator

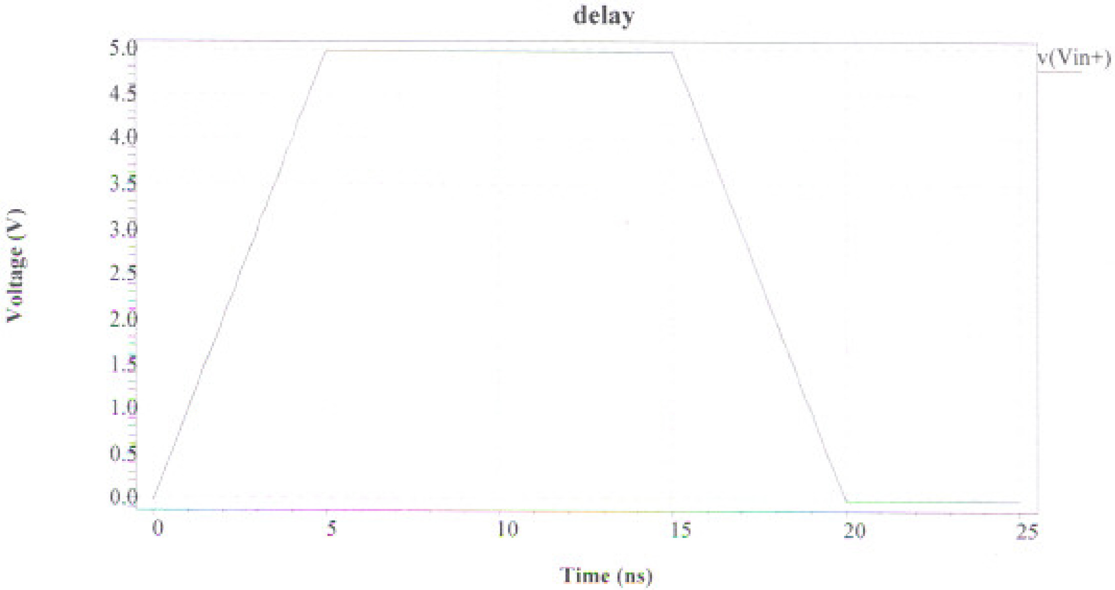
8.3 SELF-BIAS COMPARATOR

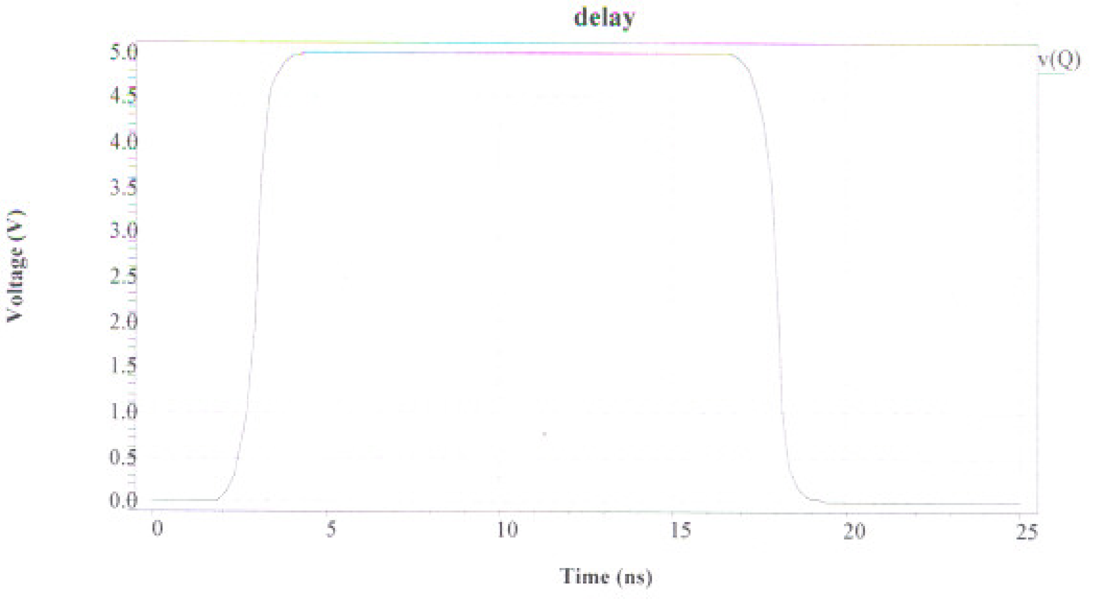
The gain achieved is same as that of clocked comparator but the unity gain bandwidth (GBW) is very high i.e. 314 MHz so it can work up to this range of frequencies. Also phase margin is 70.3 degree, which is very high so it is a very stable circuit. The best thing is it's very less delay i.e. 0.42 ns which is very less as compared to [6,19,26]. The power dissipation is quiet large i.e. 27.8 mW but average slew rate is 0.7 V/ns which is very high. The data analysis of self-biased comparator is summarized in table 4. The simulation results are as shown in figures followed.



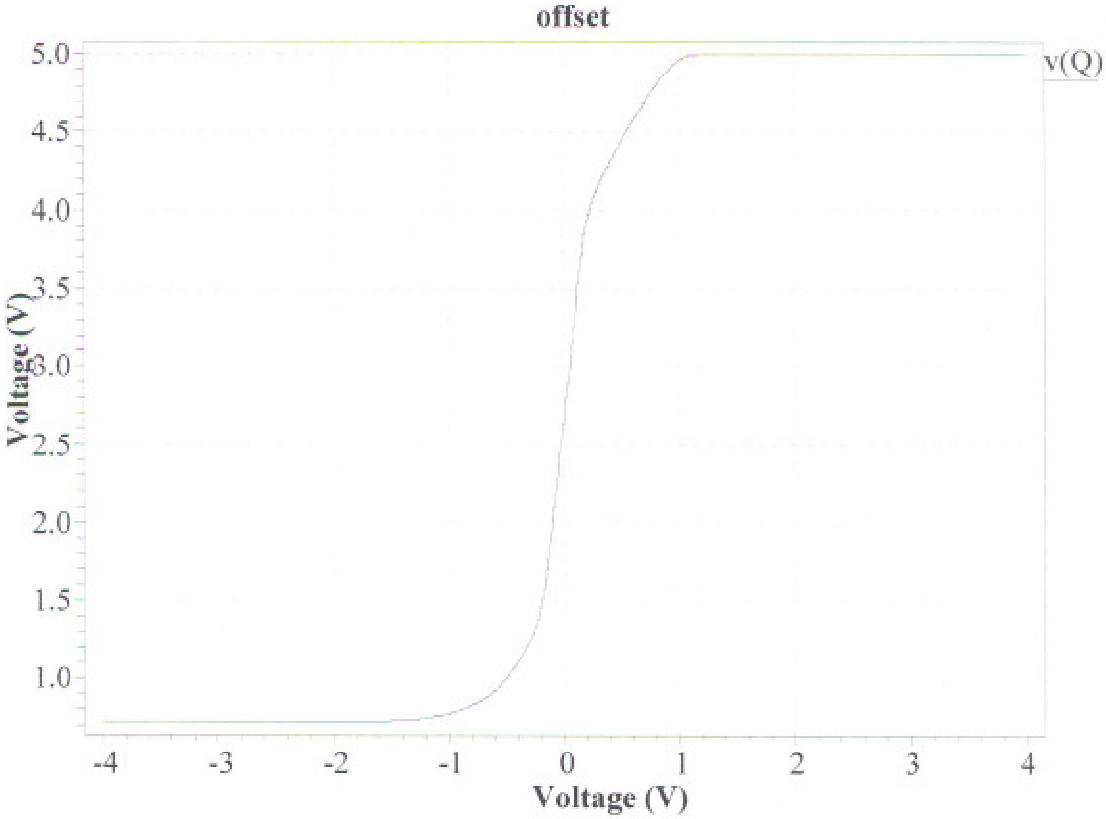


AC response of Self-Biased comparator

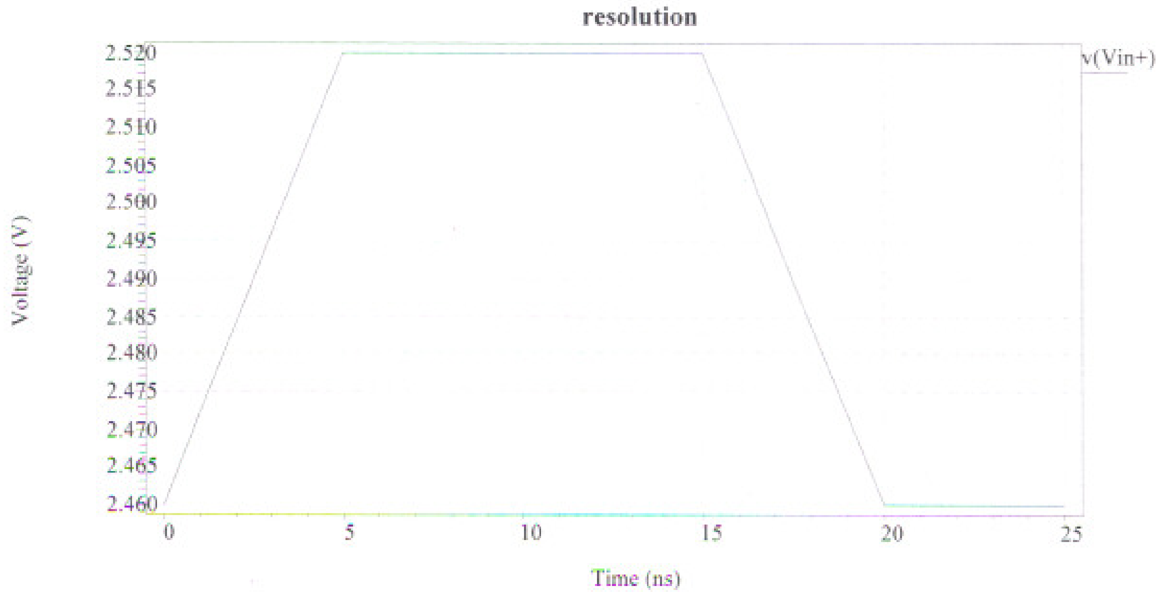


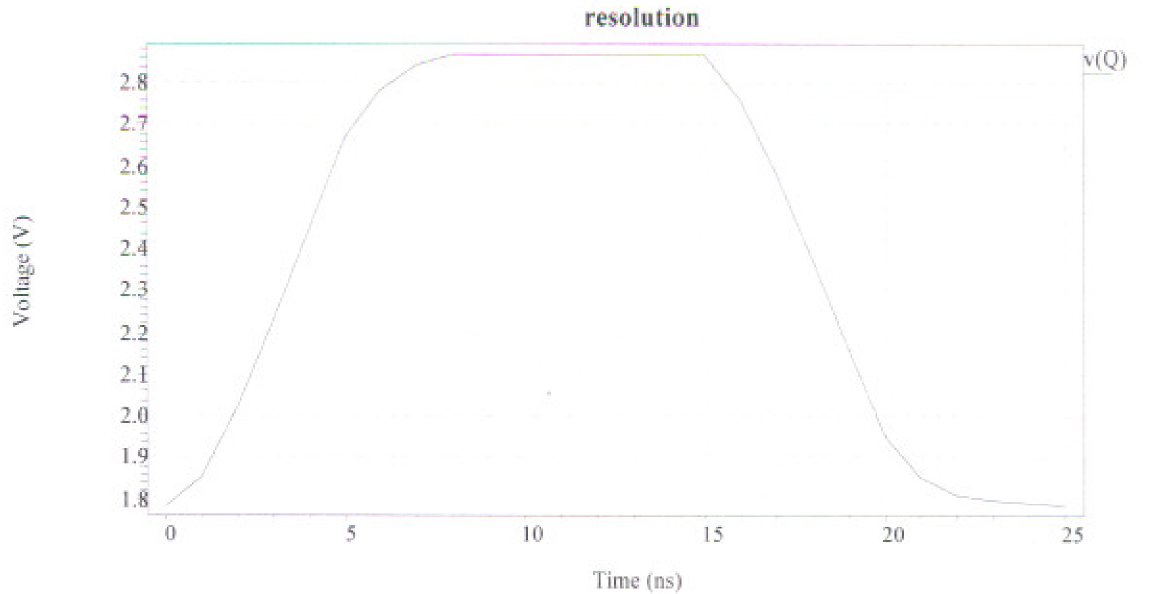


Propagation Delay of Self-Biased comparator

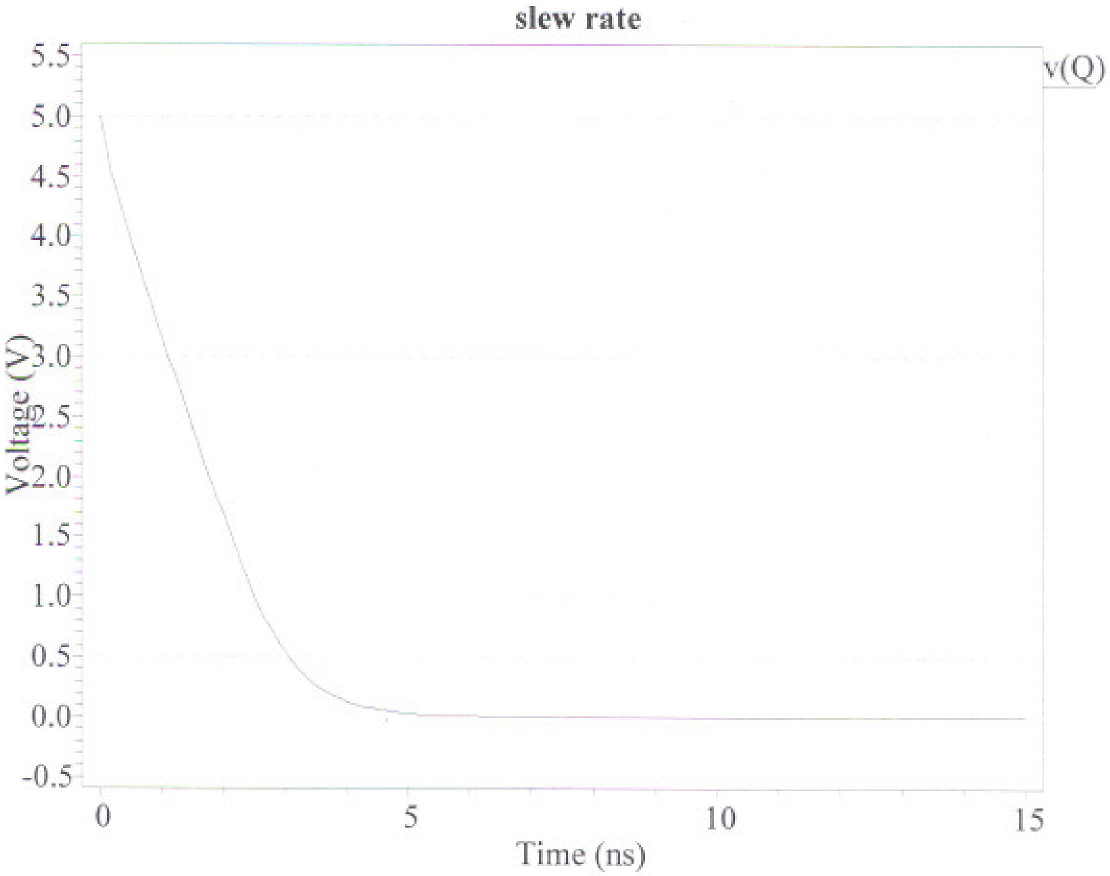


Offset of Self-Biased comparator

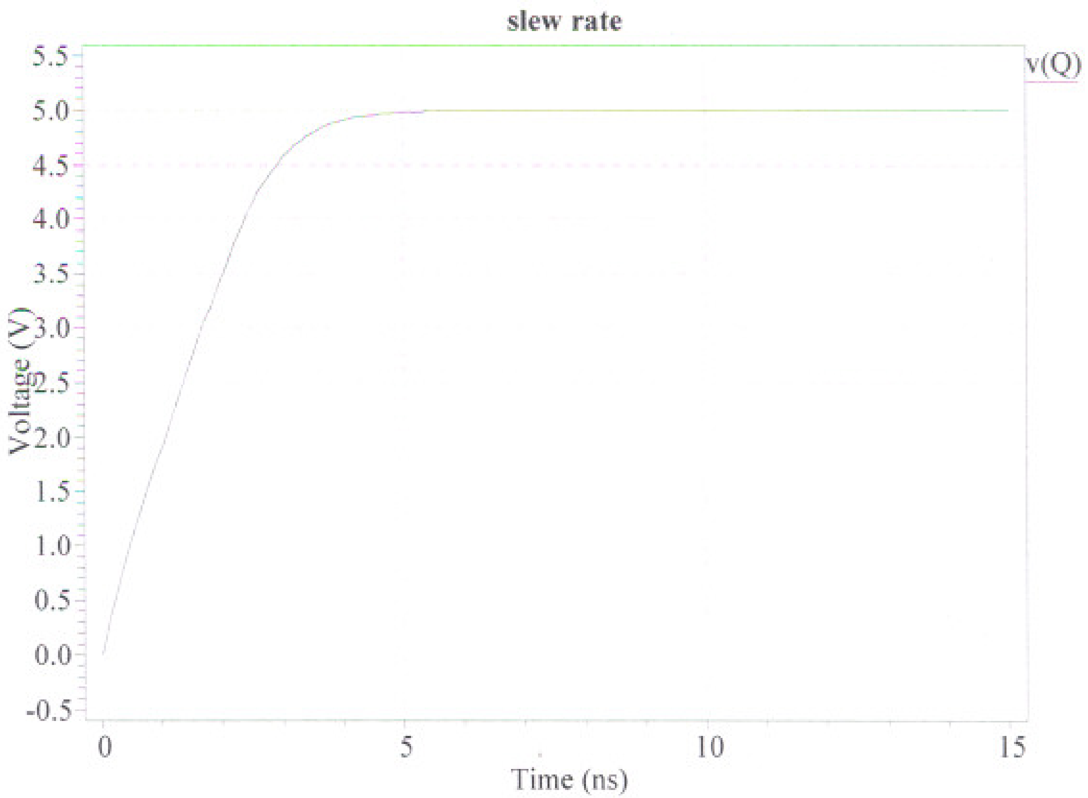




Resolution of Self-Biased comparator



Slew Rate of Self-Biased comparator



Slew Rate of Self-Biased comparator

Specifications → Parameters ↓	Set 1	Set 2	Set 3	Set 4	Set 5
Offset (V)	-0.02	-0.01	-0.06	0.01	0.02
Resolution (V)	0.2	0.04	0.01	0.02	0.03
Rising Delay (ns)	0.59	0.8	1	0.54	0.42
Falling Delay (ns)	0.68	0.9	1.27	0.58	0.46
Gain (dB)	24.77	35.5	38.88	33.02	25.34
GBW (MHZ)	256.48	246.7	621.73	533.38	314
Phase Margin (Degree)	73.4	59.3	30.57	45.6	70.3
Rising Slew Rate with 10pF load (V/µs)	72.62	28.42	132.1	132.4	112.3
Falling Slew Rate with 10pF load (V/µs)	71.4	26.4	128.9	128.9	107.4

Table 4

This data analysis is done with following specification sets:

Set 1: SR = 10 V/µs, GB = 10 MHz, C_L = 10 pF
Set 2: SR = 1 V/µs, GB = 10 MHz, C_L = 10 pF
Set 3: SR = 10 V/µs, GB = 60 MHz, C_L = 10 pF
Set 4: SR = 10 V/µs, GB = 25 MHz, C_L = 10 pF
Set 5: SR = 10 V/µs, GB = 10 MHz, C_L = 15 pF

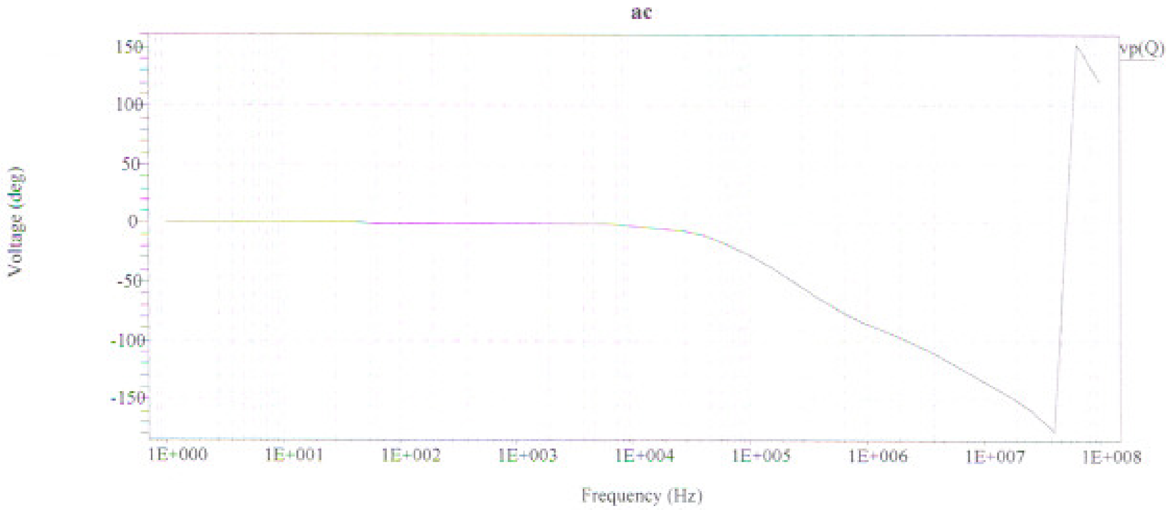
The comparison of three comparators has been summarized in table 5.

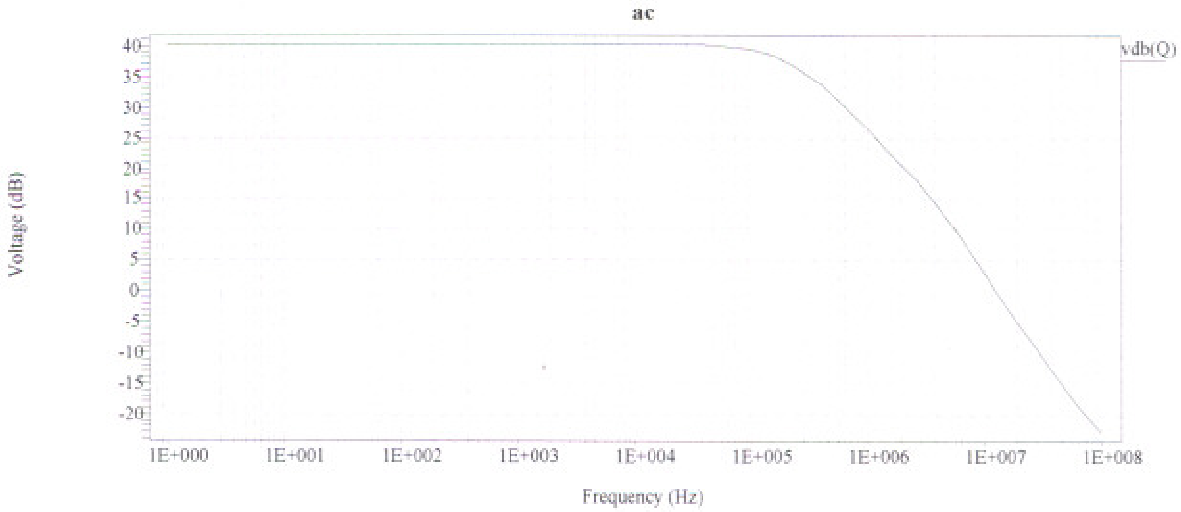
Comparator/→ ↓ Parameters	Two-stage comparator	Clocked comparator using latch	Self-biased comparator
Offset (V)	-0.007	-0.09	0.02
Resolution (V)	0.05	0.02	0.03
Rising Delay (ns)	10.3	-	0.42
Falling Delay (ns)	23.4	-	0.46
Gain (dB)	32	25.7	25.34
GBW (MHZ)	22.84	13.33	314
Phase Margin (Degree)	50	51.72	70.3
Rising Slew Rate with 1pF load (V/ns)	0.247	5.844	0.721
Falling Slew Rate with 1pF load (V/ns)	0.300	10.74	0.762
Power dissipation (mW)	9.5	0.3	27.8

Table 5

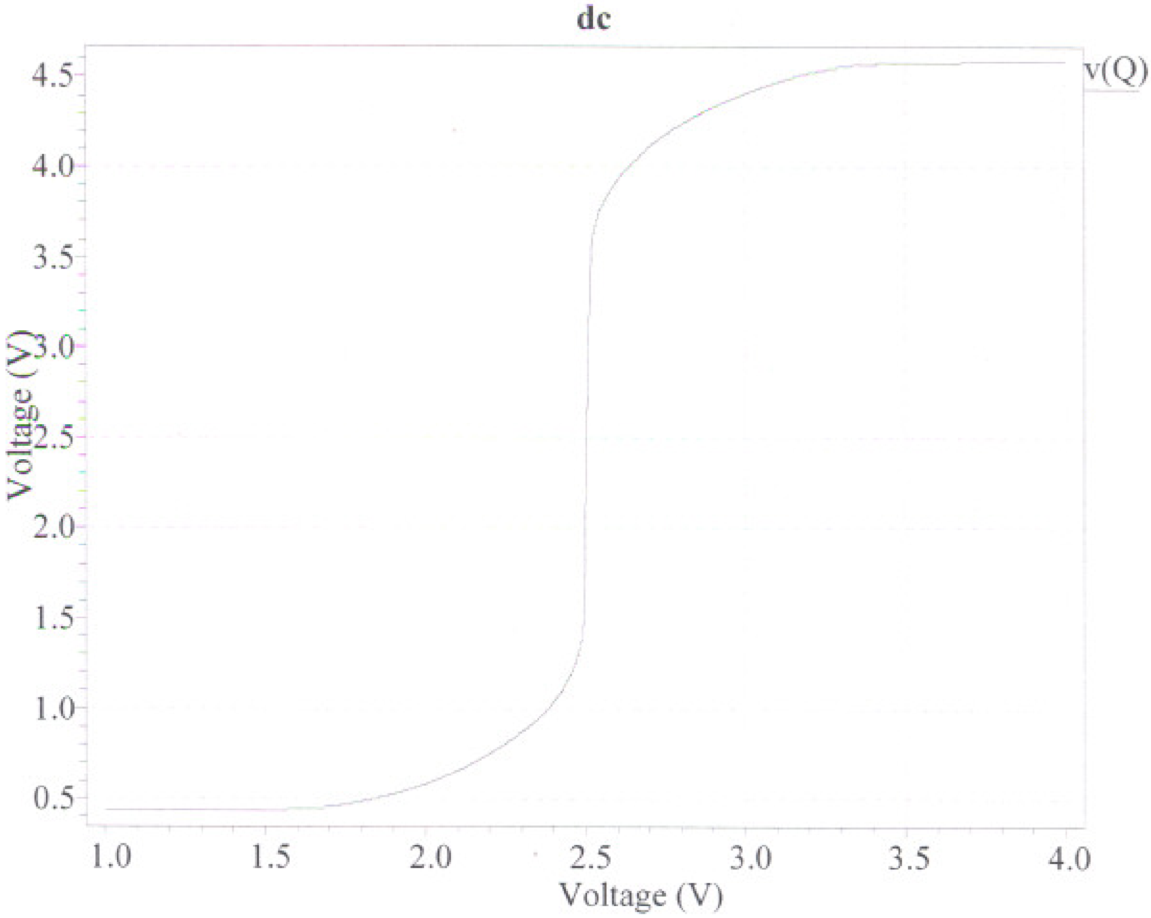
8.4 LAYOUT

The layout of self-biased comparator is developed and simulation files are extracted. The simulations of extracted files give us the gain of 40.38 dB with phase margin of 30 degree. The gain bandwidth is 21.2 MHz. As we can see gain has increased and GBW has decreased as compared to schematic simulation results. The output swing is from 0.2 V to 4.6 V. Layout resulted in very good matching giving offset of 1 mV. Slew rate has also decreased i.e. from low to high output it is 80 V/μs and from high to low output it is 116.5 V/μs.

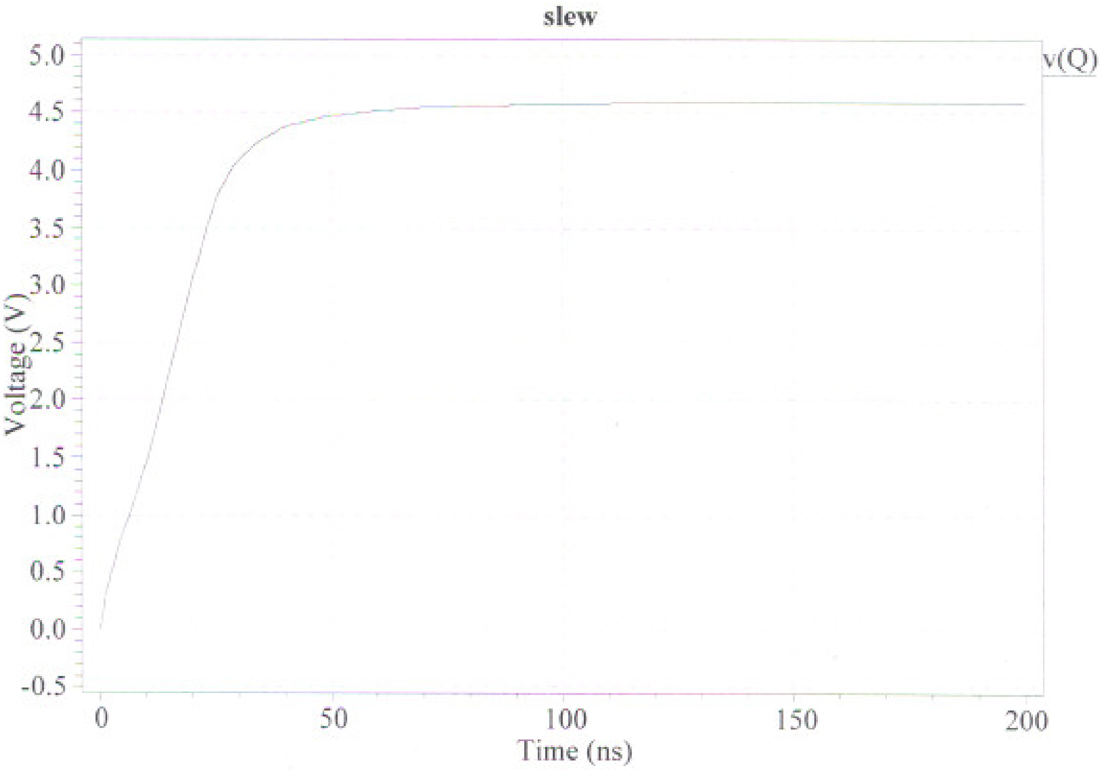

ac
vp(Q)
Voltage (deg)
150
100
50
0
-50
-100
-150
1E+000
1E+001
1E+002
1E+003
1E+004
1E+005
1E+006
1E+007
1E+008
Frequency (Hz)


ac
vdb(Q)
Voltage (dB)
40
35
30
25
20
15
10
5
0
-5
-10
-15
-20
1E+000
1E+001
1E+002
1E+003
1E+004
1E+005
1E+006
1E+007
1E+008
Frequency (Hz)

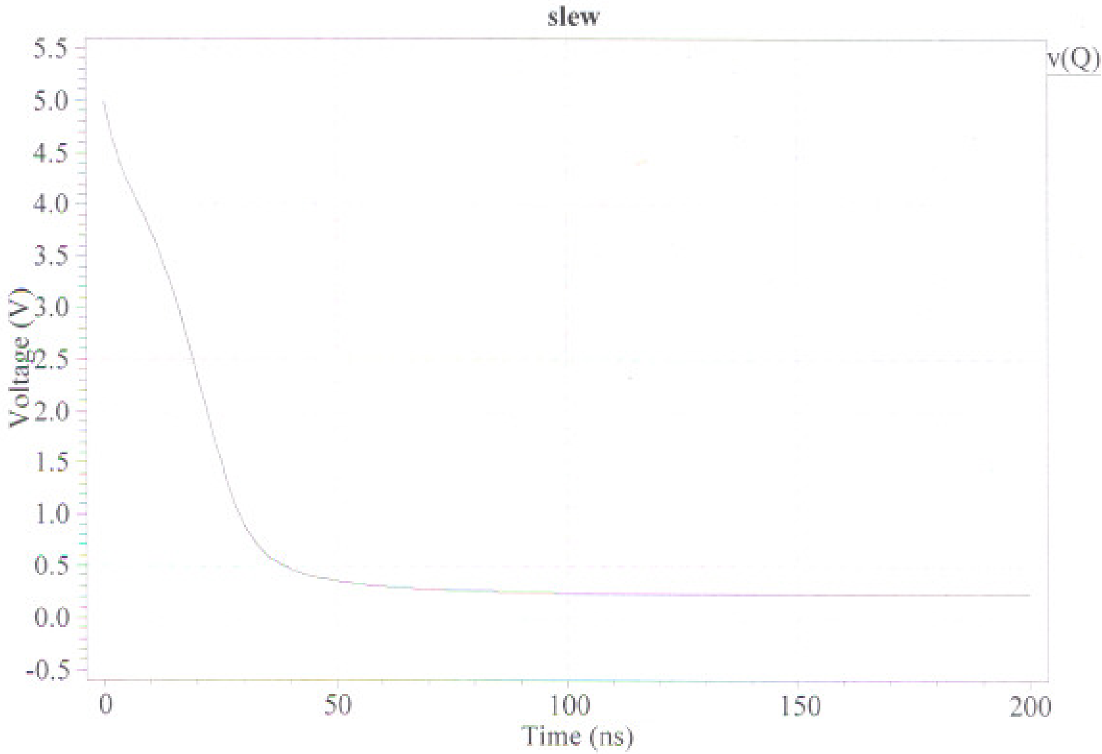
AC response


dc
v(Q)
4.5
4.0
3.5
3.0
2.5
2.0
1.5
1.0
0.5
Voltage (V)
1.0
1.5
2.0
2.5
3.0
3.5
4.0
Voltage (V)

DC response


slew
v(Q)
5.0
4.5
4.0
3.5
3.0
2.5
2.0
1.5
1.0
0.5
0.0
-0.5
Voltage (V)
0
50
100
150
200
Time (ns)

Slew rate


slew
v(Q)
Voltage (V)
5.5
5.0
4.5
4.0
3.5
3.0
2.5
2.0
1.5
1.0
0.5
0.0
-0.5
0
50
100
150
200
Time (ns)

Slew rate

9.1 CONCLUSION

The comparator design procedures have been developed for three different architectures namely: Two stage open loop comparator, Clocked comparator using basic latch and self-biased comparator. The different parameters were calculated for the three comparators, which are summarized in table 5.

We concluded that the values match directly to the characteristics defined for each comparator architecture. The open loop two stage comparator has achieved highest gain of 32 dB and the offset voltage is minimum. Whereas the clocked comparator using basic latch is fastest, which can charge, or discharge a 1 pF capacitance with slew rate of 5.8 V/ns. Also very high slew rate for large capacitances have been achieved. The power consumption of this comparator is minimum, which is only 0.3 mW. The self-biased comparator has minimum delay, which is of the order of nanoseconds i.e. 0.42 ns that is the main attraction. It has achieved maximum gain bandwidth. So it can work for highest range of frequencies. From power consumption and speed point of view the comparator using the regenerative circuit is best implementation. Whereas looking at all parameter values one can conclude that overall two-stage open loop comparator is the best implementation.

A layout has been developed for self-biased comparator. The above-mentioned parameters have also been calculated from the layout by extracting it. These parameters are satisfactory but not similar. Gain has increased but the unity gain bandwidth and slew rate has reduced as compared to the values, which we get from the schematic simulation.

9.2 FUTURE SCOPE

- Other comparator configurations can be taken for designing considering power as the main constraint.
- Layout can be further improved to remove the discrepancy.

1) Allstot D. J., "*A precision variable-supply CMOS comparator*", IEEE Journal of Solid State Circuits, vol. SC-17, no. 6, pp. 1079-1080, 1982.

2) Baker R.J, Li H.W, and Boyce D.E, " *CMOS Circuit Design, Layout , and Simulation*", Piscataway, NJ: IEEE Press, 1998, Chap, 26.

3) Bazes M., " *Two Novell Full Complementary Self Biased Differential Amplifier*", IEEE Journal of Solid State Circuits, Vol. 26, No. 2,pp. 165-168, February 1991.

4) Black W. C., "*High speed CMOS A\D conversion technique*", Ph.D. dissertation, Univ. of Calif., Berkeley, Nov. 1980.

5) Chong, C.P and Smith, K.C., " *A high resolution CMOS comparator*", Int. J Electronics, Vol. 64, pp 409-415, Mar. 1988.

6) Fisher J. A. and Koch R., "*A Highly Linear CMOS Buffer Amplifier*", IEEE Journal of Solid State Circuits, Vol. SC-22, No.3, June 1987.

7) Geiger R. L., Allen P. E. and Strader N. R., "*VLSI Design Techniques for Analog and Digital Circuits*", McGraw-Hill Publishing Company, 1990.

8) Gray P. R and Meyer, "*Analysis and design of Analog Integrated Circuits*" ,J. Wiley & Sons, New York, 1993.

9) Gray P. R., Hurst P. J., Lewis S. H. and Meyer R. G., "*Analysis and Design of Analog Integrated Circuits*", Fourth Edition, John Wiley & Sons, 2001.

10) Gregorian R., "*Introduction to CMOS OP-AMPS and Comparators*", J. Wiley and Sons, New York, 1999.

11) Heydari Payam, Mohavavelu Ravi, " *Design of Ultra High-Speed CMOS CML buffers and Latches*", Department of Electrical and Computer Engineering, University of California.

12) Hosticka B. J., " *Dynamic CMOS amplifiers*", IEEE J. Solid-State Circuits, vol. SC-15, pp. 887-894, Oct. 1980.

13) Johns D. A. and Martin K., " *Analog Integrated Circuit Design*", J. Wiley & Sons, New York, 1997.

14) Kang Sung-Mo, Leblebici Yusuf, " *CMOS Digital Integrated Circuits, Analysis and design",* Tata McGraw-Hill Edition 2003, Third Edition.

15) Klinke R., Member, IEEE, Hosticka B. J., Senior Member, IEEE and Peleiderer H. J., Senior Member, IEEE, "*A very-high Slew-rate CMOS operational Amplifier*", IEEE Journal of Solid State Circuits, Vol. 24, No.3, June 1989.

16) Kurnamoto T. et al., " *A 8-bit high speed CMOS A/D converter",* IEEE J. Solid State Circuits, Vol. SC-21, pp-976-982, Dec. 1986.

17) Laksmikumar K. R., Hadaway R. A., and Copeland M. A., " *Characterization of modeling of mismatch in MOS transistors for precision analog design",* IEEE J. Solid State Circuits, vol SC-21, pp. 1057-1066, Dec. 1966.

18) Maloberti Franco, "*Analog Design For CMOS VLSI Systems*", KLUWER academic Publisher, Boston/ Dordrecht/ London, 2001.

19) McCarroll Benjamin J., Sodini Charls D., Lee Hae-Seung, " *A High Speed CMOS Comparator For Use In An ADC*", IEEE Journal of Solid State circuits, Vol. 23, No.1, February 1988.

20) Philip Allen E., Holberg Douglas R., " *CMOS Analog Circuit Design* ", Oxford University Press, London, 2003, Second Edition.

21) Razavi B. and Wooley B. A., " *Design Techniques for high-speed, high-resolution comparators",* IEEE Journal of Solid State circuits, Vol. 27, pp.1916-1926, 1992.

22) Razavi B., " *Prospects of CMOS Technology for High-Speed Optical Communication Circuits*", IEEE J. Solid-State Circuits, vol. 37, No. 9, pp. 1135-1145, Sept. 2002.

23) Razavi Behzad, " *Design of Analog CMOS Integrated Circuits",* Tata McGraw-Hill Edition, Edition 2002.

24) Scott J. W., Lee W. L., Giancarlo C. H., and Sodini C.G., " *CMOS implementation of an immediately adaptive delta modulator",* IEEE Journal of solid-state circuits, vol.sc-21, pp. 1088-1095, Dec 1986.

25) Wu Jieh-Tsorng and Wooley B.A., " *A 100 MHz pipelined CMOS comparator",* IEEE Journal of Solid State Circuits, Vol. 23, pp.1379-1385, 1998.

26) Yin G.M, Eynde F. Op', and Sansen W., "*A High Speed CMOS Comparator with 8-b Resolution*", IEEE J. Solid State Circuits, Vol. 27, No.2, Feb. 1992.

27) Yukawa A., " *A CMOS 8-bit high speed A/D converter IC",* IEEE J. Solid State Circuits, Vol. SC-20, pp-775-779, June 1985.

APPENDIX

DESIGN OF CLOCKED COMPARATOR USING BASIC LATCH

Jyoti kedia, Alpana Agarwal and Chandra Shekhar*
Thapar Institute of Engineering and Technology, PATIALA
*Central Electronics Engineering Research Institute, Pilani, India

Abstract: This paper introduces the design of a clocked high-speed CMOS comparator. The comparator consists of a differential input stage, two regenerative latch and output buffers. This circuit operating under + 5.0 / 0.0 power supply, performs comparison within a few nanoseconds. The power consumption of the comparator is only 0.3 mW at 0.11 GHz clock rate.

1. INTRODUCTION

A high-speed comparator should have a propagation delay time as small as possible. The basic principle behind the high-speed comparator is to use a preamplifier to build up the input change to a sufficiently large value and then apply it to latch. This combines the best aspect of circuits with a negative exponential response (the preamplifier) with circuits with a positive exponential response (the latch).

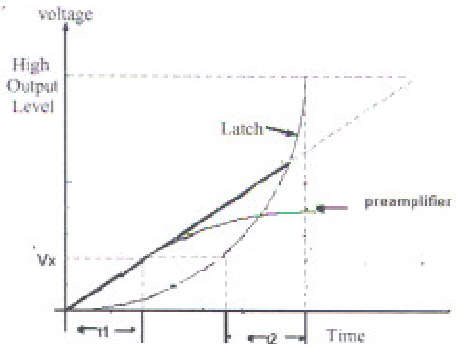


Fig. 1: Preamplifier and Latch Step Response

This is illustrated in Fig.1[1], where the gain of the preamplifier times the input voltage is not sufficient to reach the desired output level. Rather during time t_1 the preamplifier amplifies the input voltage to a value V_X.The voltage V_X is then applied to latch input, which then goes to the desired output voltage in time t_2. Thus total response time is $t_1 + t_2$. If comparator consisted only of the preamplifier, the gain would have to be larger and the delay to make the transition from V_{OL} to V_{OH} would be longer. So larger the input to latch the shorter the time for the output to reach its maximum value.

2. COMPARATOR CIRCUIT

The proposed comparator circuit is depicted in Fig.2 [2]. It consists of a differential input pair (M1 and M2), a CMOS latch circuit and output buffers. The CMOS latch composed of an n-channel flip-flop (M6 and M7) with a pair of n-channel transfer

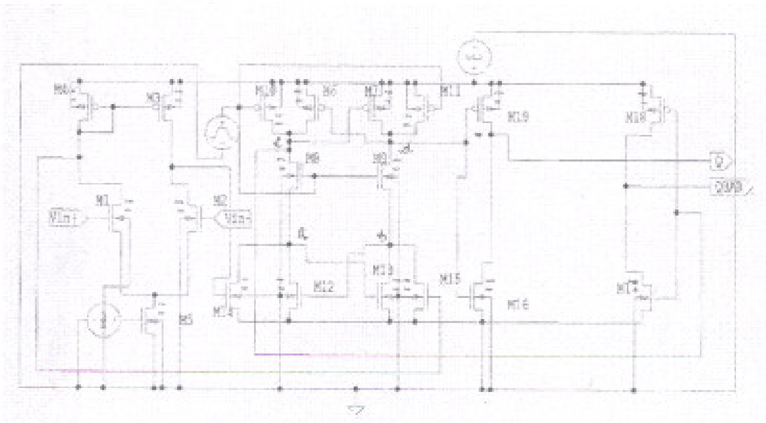


Fig.2 Schematic of Comparator

gates (M8 and M9) for strobing, and a p-channel flip-flop (M12 and M13) with a pair of p-channel precharge transistors (M10 and M11).

The dynamic operation of this circuit can be divided into two parts. First, when latch is low, the p-channels M12 and M13 are isolated from n-channels, M6 and M7. After the input voltage settles on its decision, a voltage proportional to the input voltage difference is established between nodes *a* and *b* in the end of this period. This voltage difference will act as the initial imbalance for the following regeneration time interval. In the meantime, the p-channel (M12 and M13) is reset by the two-closed precharge transistors, which charge the nodes *c* and *d* to the positive power supply voltage.

The regeneration is initialized by the closing of latch. So the transistors M8 and M9 are also closed. The n-channel flip-flop and p-channel flip-flop, regenerates the voltage difference between the nodes *a* and *b* and between the nodes *c* and *d*. the voltage difference between node *c* and *d* is soon amplified to a voltage nearly equal to power supply voltages.

3. DESIGN PROCEDURE FOR COMPARATOR

A. SPECIFICATIONS: -

- DC gain (A_V)
- Input common mode range [V_{in}(min) and V_{in}(max)]
- Load capacitance (C_L)
- Total delay (ns)
- Output voltage swing
  [V_{out} (max) and V_{out} (min)]

B. DESIGN PROCEDURE: -

1. First of all the total delay should be divided into three stages. Then taking that delay and output capacitance for each stage we can calculate the current. Let us see each stage's calculation. Considering the output stage as first stage the current flowing can be calculated using load capacitance, delay and output voltage swing

specifications. Note designing the output buffers is just equivalent to the design of digital inverter. So

$$I_{16} = I_{17} = C_L * \left(\frac{dv * 2}{dt} \right)$$

Where dv is output voltage difference and dt is the total delay corresponding to this stage. That's why time is halved for the two buffers. From the specification of output voltage swing, we can see that the minimum voltage that make the transistors M_{16} and M_{17} to remain in saturation is that the drop between these two transistors is equal to the difference of the V_{DD} and V_{out} (max), similarly for M_{18} and M_{19} this voltage is V_{SS} and V_{out} (min). These voltages give us the drain to source voltage of the transistors. So taking this drain to source voltage and the bias current together we get

$$\left(\frac{W}{L} \right)_{18} = \frac{2 * I_{16}}{K_N * (V_{DS})^2}$$

$$\left(\frac{W}{L} \right)_{19} = \frac{2 * I_{17}}{K_N * (V_{DS})^2}$$

The corresponding p-channel transistor W/L's can be calculated using mobility ratio of p and n-channel transistors.

2. Calculate the output capacitance of second stage by taking into consider the capacitances of the transistor of first stage it has to drive. This will help in getting current that is required in second stage. Looking at the circuit the second stage is a Nand gate pair. So total delay can be divided in two equally as in first step. We will design this stage using the equivalent of nand to inverter.

$$I_1 = I_2 = C_{out2} * \left(\frac{dv * 2}{dt} \right)$$

$$\left(\frac{W}{L} \right)_{equ} = \frac{2 * I_1}{K_N * (V_{DS})^2}$$

$$\left(\frac{W}{L} \right)_{6,8,10,7,9,11} = 2 * \left(\frac{W}{L} \right)_{equ}$$

where $(W/L)_{equ}$ is the ratio for equivalent of nand . C_{out2} is the output capacitance of second stage and V_{ds} is to be calculated in same fashion as in the previous step. The corresponding p-channel transistor W/L's can be calculated using mobility ratio of p and n-channel transistors.

3. Similarly, calculate the output capacitance of third stage by taking into consider the capacitances of the transistor of second stage it has to drive. This will help in getting bias current.

$$I_{BIAS} = 2 * C_{out3} * \left(\frac{dv}{dt}\right)$$

Next step is to calculate the transconductance g_{m1} of transistor M1 using the gain relation of the two stages.

$$g_{m1} = A_v(0) * (g_{ds2} + g_{ds4})$$

where $g_{dsi} = \lambda_P * I_{Di}$ (For p-type transistor)

$g_{dsi} = \lambda_N * I_{Di}$ (For n-type transistor)

Using the above-calculated value of transconductance of differential transistors, we can design M1 and M2 i.e the differential pair transistors.

$$\frac{W_1}{L_1} = \frac{W_2}{L_2} = \frac{g_{m1}^{\ 2}}{K_N * I_{BIAS}}$$

Now calculate the value of gate to source voltage of the current mirror transistors using the specification of maximum input common mode voltage. Here we use the relation

$$V_{SG3} = V_{DD} - V_{in}(max) + V_{TN}$$

Using the gate to source voltage calculated above we can design the transistors M3 and M4.

$$\frac{W_3}{L_3} = \frac{W_4}{L_4} = \frac{I_{BIAS}}{K_P * \left(V_{SG3} - |V_{TP}|\right)^2}$$

Next step is to calculate $V_{DS5}(sat)$ using the specification of minimum input common mode voltage. The relation is given by

$$V_{DS5} = V_{in}(min) - V_{GS1} - V_{SS}$$

Where $V_{GS1} = \sqrt{\dfrac{I_{BIAS} * L_1}{K_N * W_1}} + V_{TN}$

Using the above-calculated value of V_{DS5} we can design the transistor M5.

$$\frac{W_5}{L_5} = \frac{2 * I_{BIAS}}{K_N * \left(V_{DS5}(sat)\right)^2}$$

Lastly, the bias voltage is given by

$$V_{B5} = (V_{DS5} / 2) + V_{TN}$$

4. SIMULATION RESULTS

In order to verify the procedure, the circuit was designed using that and then using T-SPICE it is simulated. Fig [3,4] shows comparator gain and slew.
The comparator maintains the gain of 25.7 dB with phase margin of 51.72 degree. It can work up to the frequencies of 13.33 MHz i.e. this is the unity gain bandwidth. It can charge or discharge a load of 10pf with slew rate of 2.828 V/ns and 2.229 V/ns respectively. The total delay is found to be 9 ns. It can resolve the voltage difference of 0.02 V. The above simulation results are with specifications total delay = 20 ns, C_L = 1pf, V_{in}(min) and V_{in}(max) = 4.5 V and 1.25 V respectively, V_{out} (max) and V_{out} (min) = 4.0 V and 0.0 V respectively, A(v) = 1000.

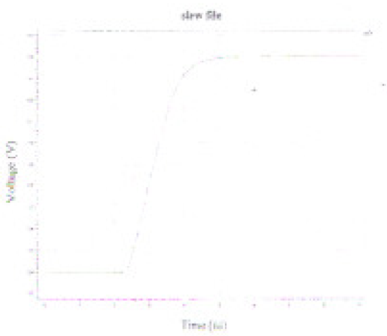


Fig.3 Slew Rate of Comparator

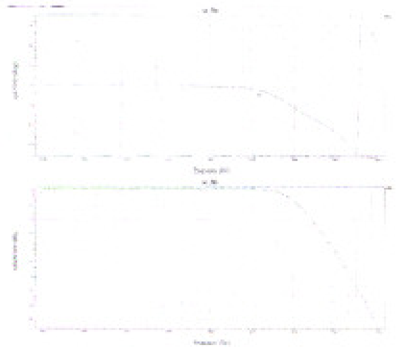


Fig.4 Ac Response of Comparator

5. CONCLUSION

A CMOS comparator design procedure has been developed for use in ADC. A dynamic latch preceded by an amplifier has been used to build a fast and precise comparator. The power consumption of the comparator is only 0.3 mW at 0.11 GHz clock rate, which is very low as compared to [5]. It can also charge or discharge with a much better slew rate than [7].

REFRENCES

[1] Allen Philip E., Holberg Douglas R., "*CMOS Analog Circuit Design* " Oxford University Press, London, 2003,Second Edition.

[2] Baker R.J, Li H.W, and Boyce D.E," *CMOS Circuit Design, Layout, and Simulation*". Piscataway, NJ: IEEE Press, 1998, Chap, 26.

[3] Maloberti Franco,"*Analog Design For CMOS VLSI Systems*" KLUWER academic Publisher, Boston/ Dordrecht/ London.

[4] Benjamin J. McCarroll, Charls D. Sodini, Hae-Seung Lee, " *A High Speed CMOS Comparator For Use In An ADC*," IEEE Journal of Solid State Circuits, Vol. 23, No.1, February 1988.

[5] G. M. Yin, F. Op't Eynde and W. Sansen,"A High Speed CMOS Comparator With 8-Bit Resolution", IEEE Journal of Solid State Circuits, Vol. 27, No.2, February 1992.

[6] J. A. Fisher and R. Koch, "*A Highly Linear CMOS Buffer Amplifier*," IEEE Journal of Solid State Circuits, Vol. SC-22, No.3, June 1987.
[7] R. Klinke, Member, IEEE, B. J. Hosticka, Senior Member, IEEE and H. J. Peleiderer, Senior Member, IEEE, "*A very-high Slew-rate CMOS operational Amplifier*," IEEE Journal of Solid State Circuits, Vol. 24, No.3, June 1989.

Bharati Vidyapeeth's College of Engineering

Certificate of Participation

National Conference on VLSI Design & Technology
15th 16th April, 2004

This is to certify that Mr. /Ms. /Dr. /Prof. Jyoti Kedia *of* Thapar Institute of Engineering and Technology, Patiala *has participated and presented a paper / ~~invited talk~~ on* Design of clocked comparator using Basic Latch

Co authors: Alpana Aggarwal, Chandershekar

in the National Conference on VLSI Design & Technology held at Bharati Vidyapeeth's College of Engineering, A-4, Paschim Vihar, New Delhi-63 on 15th & 16th April, 2004

Mr. Sanjay Kumar Barwar Co-Convener	Dr. M. K. Raina Convener HOD, ECE Dept.	Dr. S. S. Inamdar Principal BVCOE, New Delhi

COMPARATIVE ANALYSIS OF CMOS ANALOG COMPARATORS

Jyoti kedia, Alpana Agarwal
Thapar Institute of Engineering and Technology, Patiala

Abstract: This paper discusses the comparative study of three different comparators. The comparison is done on the basis of different parameters of comparator. From power consumption and speed point of view the comparator using regenerative circuit, is the best implementation.

1. INTRODUCTION

The three different comparators, which have been compared here, are:

1. Two-stage open loop comparator
2. Clocked comparator using basic latch
3. Self-biased comparator

Lets have an introduction of each of the above comparator.

As we can see from the requirements for a comparator reveal that it requires a differential input and sufficient gain to be able to achieve the desired resolution. The best implementation is the two-stage opamp [7]. A simplification occurs because the comparator will generally be used in open loop mode and it's not necessary to compensate that. It is preferred so that it has largest bandwidth possible, which will give a faster response.

A high-speed comparator should have a propagation delay time as small as possible. The basic principle behind the high-speed clocked comparator is to use a preamplifier to build up the input change to a sufficiently large value and then apply it to latch. This combines the best aspect of circuits with a negative exponential response (the preamplifier) with circuits with a positive exponential response (the latch).

The circuit of self-biased comparator that is designed here has the ability to sink and source large amounts of current in large capacitances.

The circuit configuration [2] differs from those of conventional CMOS differential-amplifiers configuration in two ways:

1. The amplifier is completely complementary i.e. each n-type device operates in push-pull fashion with a corresponding p-type device.

2. The amplifier is self-biased through negative feedback.

2. TWO STAGE OPEN LOOP COMPARATOR

Figure 1 shows the schematic of two-stage comparator. Simply the comparator is made up of three building blocks:

1. Differential stage
2. Current mirror
3. CMOS inverter with active load

A differential pair is widely used as the input stage of the op-amplifier. It is

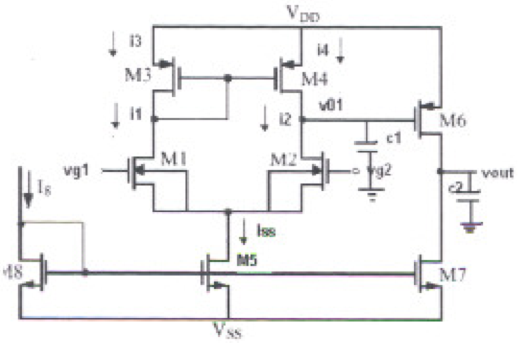


Fig. 1. Two stage Comparator

made of two transistors with their source in common, fed by current source. The transistors may either be n-channel or p-channel, and they are matched to each other.

Current mirror is composed of two transistors, of which one M1 is diode connected as shown in figure 2.

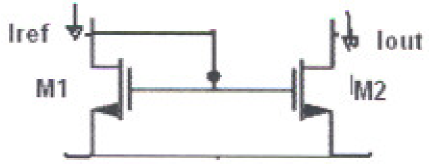


Fig 2: Simple current mirror

M1 receives the reference current I_{ref} and measures it by developing at its gate voltage V_{GS1}; this voltage biases the gate of M2.

The simplest form of inverter is the inverter with active load. Here input is applied to only one transistor while the gate of complementary element is biased with a fixed voltage and operates as an active load. The biasing voltage is obtained by a transistor connected in so-called diode configuration and carrying a given current I_{Bias}.

4. CLOCKED COMPARATOR USING BASIC LATCH

As illustrated in Figure 3 [7], where the gain of the preamplifier times the input voltage is not sufficient to reach the desired output level. Rather during time t_1 the preamplifier amplifies the input voltage to a value V_X. The voltage V_X is then applied to latch input, which then goes to the desired output voltage in time t_2. Thus total response time is $t_1 + t_2$. If comparator consisted only of the preamplifier, the gain would have to be larger and the delay to make the transition from V_{OL} to V_{OH} would be longer. So larger the input to latch the shorter the time for the output to reach its maximum value.

The proposed comparator circuit is depicted in Fig.4 [1]. It consists of a differential input pair (M1 and M2), a

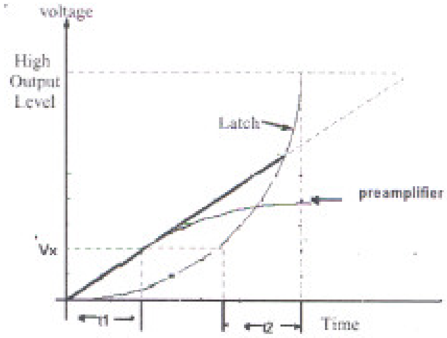


Fig 3: Preamplifier and Latch Step Response

CMOS latch circuit and output buffers. The CMOS latch composed of an n-channel flip-flop (M12 and M13) with a pair of n-channel transfer gates (M8 and M9) for strobing, and a p-channel flip-flop (M6 and M7) with a pair of p-channel precharge transistors (M10 and M11).

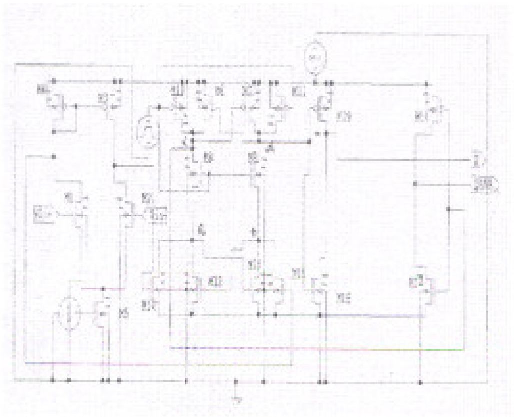


Fig.4 Schematic of Comparator

The dynamic operation of this circuit can be divided into two parts. First, when latch is low, the p-channels M6 and M7 are isolated from n-channels, M12 and M13. After the input voltage settles on its decision, a voltage proportional to the input voltage difference is established between nodes *a* and *b* in the end of this period. This voltage difference will act as the initial imbalance for the following regeneration time interval. In the meantime, the p-channel (M6 and M7) is reset by the two-closed precharge transistors, which charge the nodes *c* and *d* to the positive power supply voltage. The regeneration is initialized by the closing of latch. So the transistors M8 and M9 are also closed. The n-channel flip-flop and p-channel flip-flop, regenerates the voltage difference between the nodes *a* and *b* and between the nodes *c* and *d*. the voltage difference between node *c* and *d* is soon amplified to a voltage nearly equal to power supply voltages.

4.SELF-BIASED COMPARATOR

The operation of self-biasing comparator can be understood through its derivation [2]. Fig 6(a) illustrates two folded cascode differential amplifiers, one the complement of other. These amplifiers have the greater dynamic ranges than ordinary differential amplifier as a result of the larger drain-source voltage drop on input pairs. This larger voltage drop maintains the input pairs in active region even for large input voltage swings. While neither amplifier in Fig 6(a) is capable of covering the entire input range from negative supply to positive supply, a combination of the two amplifiers can cover this entire range.

In the first step of derivation, the loads of the two amplifiers are deleted, and their outputs are connected together to produce the fully complementary, but externally biased differential amplifier of Fig 6(b). However the circuit of Fig 6(b) cannot be biased in a stable fashion.

In order for the circuit to be biased in stable fashion the currents through M3 and M4 devices should be identical. Any difference in currents through these two devices result in extreme shifts in amplifier bias voltages. Achieving

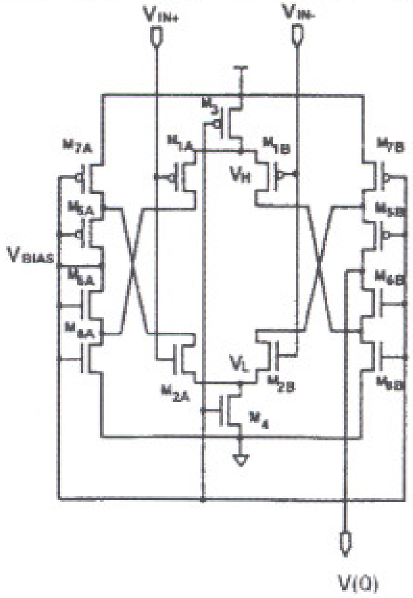


Fig. 5. Self-Biased Comparator

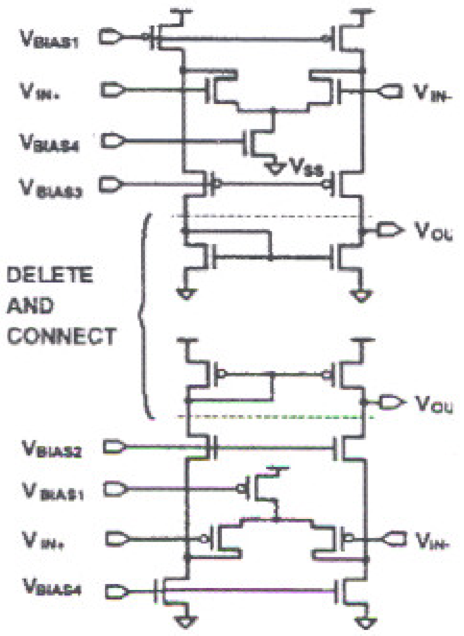


Fig. 6(a) Folded Cascode Differential Amplifier

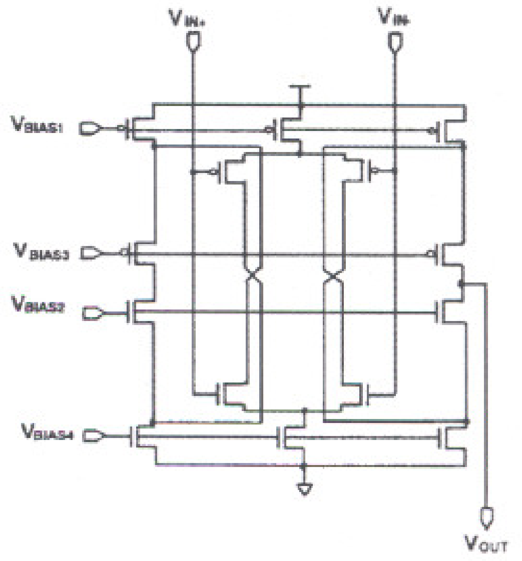


Fig. 6(b) Externally Biased Differential Amplifier

perfect equality of currents in these two devices using external biasing is practically impossible, so that the configuration of Fig 6(b) is practically impossible.

A simple modification of the circuit of Fig. 6(b), however, results in stabilization of the bias voltages. This modification is illustrated in Fig 5, in which the two bias-voltages are disconnected from the external sources and instead are connected to internal amplifier node V_{BIAS}. This self-biasing of the amplifier creates the negative feedback loop that stabilizes the bias voltages. Any variations in the processing parameters or operating conditions that shifts the bias voltages away from their nominal values result in a shift in V_{BIAS} that corrects the bias voltages through negative feedback. The resulting self-biased amplifier is illustrated in Fig. 5.

5. SIMULATION RESULTS

The comparators explained in sections 2-5 were designed and simulated in T-spice environment. The measured data of all comparator circuits have been summarized in Table 1.

6. CONCLUSION

The open loop two stage comparator has achieved highest gain of 32 dB and offset voltage is minimum. Whereas the clocked comparator using basic latch can charge, or discharge a 1-pF capacitance with slew rate of 5.8 V/ns. Also very high slew rate for large capacitances have been achieved as compared to [4]. The power consumption of this comparator is minimum, which is only 0.3 mW as compared to [8]. The self-biased comparator has minimum delay [5-7], which is of the order of nanoseconds i.e. 0.42 ns that is the main attraction. It has achieved maximum gain bandwidth. So it can work for highest range of frequencies. Looking at all parameter values one can conclude that overall two-stage open loop comparator is the best implementation.

Parameter	Two-stage	Clocked comparator	Self-biased
Offset (V)	-0.007	-0.09	0.02
Resolution (V)	0.05	0.02	0.03
Rising Delay (ns)	10.3	-	0.42
Falling Delay (ns)	23.4	-	0.46
Gain (dB)	32	25.7	25.3
GB (MHZ)	22.84	13.33	314
Phase Margin (Degree)	50	51.72	70.3
Rising Slew Rate with 1pF load (V/ns)	0.247	5.844	0.72
Falling Slew Rate with 1pF load (V/ns)	0.300	10.74	0.76
Power dissipation (mW)	9.5	0.3	27.8

Table 1

REFRENCES

[1] Baker R.J, Li H.W, and Boyce D.E, " *CMOS Circuit Design, Layout, and Simulation*". Piscataway, NJ: IEEE Press, 1998, Chap, 26.

[2] Bazes M., "*Two Novell Full Complementary Self Biased Differential Amplifier*," IEEE Journal of Solid State Circuits, Vol. 26, No. 2,pp. 165-168,February 1991.

[3] Fisher J. A. and Koch R., "*A Highly Linear CMOS Buffer Amplifier*," IEEE Journal of Solid State Circuits, Vol. SC-22, No.3, June 1987.

[4] Klinke R., Member, IEEE, B. J. Hosticka, Senior Member, IEEE and Peleiderer H. J., Senior Member, IEEE, "*A very-high Slew-rate CMOS operational Amplifier*," IEEE Journal of Solid State Circuits, Vol. 24, No.3, June 1989.

[5] Maloberti Franco, "*Analog Design For CMOS VLSI Systems*" KLUWER academic Publisher, Boston/ Dordrecht/ London.

[6] McCarroll Benjamin J., Sodini Charls D., Lee Hae-Seung, " *A High Speed CMOS Comparator For Use In An ADC*," IEEE Journal of Solid State Circuits, Vol. 23, No.1, February 1988.

[7] Philip E.Allen, Holberg Douglas R., "*CMOS Analog Circuit Design* " Oxford University Press, London, 2003,Second Edition.

[8] Yin G. M., F. Op't Eynde and Sansen W., "*A High Speed CMOS Comparator With 8-Bit Resolution*", IEEE Journal of Solid State Circuits, Vol. 27, No.2, February 1992.

DESIGN OF SELF-BIASED COMPARATOR

Jyoti kedia, Alpana Aggarwal and Chandra Shekhar*
Thapar Institute of Engineering and Technology, PATIALA
*Central Electronics Engineering Research Institute, Pilani, India

Abstract - This paper discusses the design of self-biased CMOS analog comparator. On the basis of simulation results the performance analysis has been done. The negative feedback in self-biased comparator increases the comparison speed. The maximum delay of 0.8 ns has been achieved. The circuit is capable of driving large capacitance of 15 pf can be charged or discharged within few nano-seconds.

1. INTRODUCTION

Many techniques have been introduced in the literature for implementing high-speed CMOS comparators. The most commonly used are the latches, which are used after the preamplifier stage. If a comparator has a large capacitive load, the chances are that it is slew rate limited. The circuit that is designed here has the ability to sink and source large amounts of current in large capacitances. The circuit configuration [4] differs from those of conventional CMOS differential-amplifiers configuration in two ways:

1. The amplifier is completely complementary i.e. each n-type device operates in push-pull fashion with a corresponding p-type device.

2. The amplifier is self-biased through negative feedback.

These two differences result in several performance enhancements desirable in comparator applications.

2. SELF -BIASING COMPARATOR

CMOS differential amplifiers with wide input dynamic ranges have been reported [2,3,7]. All of these amplifiers are externally biased while none of them is fully complementary. The circuit configuration that has been designed is as shown in the Fig 1. As we can see that this circuit is fully complementary as well as entirely self-biased.

The operation of self-biasing comparator can be understood through its derivation [4]. Fig 2(a) illustrates two folded cascode differential amplifiers, one the complement of other. These amplifiers have the greater dynamic ranges than ordinary differential amplifier as a result of the larger drain-source voltage drop on input pairs. This larger voltage drop maintains the input pairs in active region even for large input voltage swings. While neither amplifier in Fig 2(a) is capable of covering the entire input range from negative supply to positive supply, a combination of the two amplifiers can cover this entire range.

In the first step of derivation, the loads of the two amplifiers are deleted, and their outputs are connected together to produce the fully complementary, but externally biased differential amplifier of Fig 2(b). However the circuit of Fig 2(b) cannot be biased in a stable fashion.

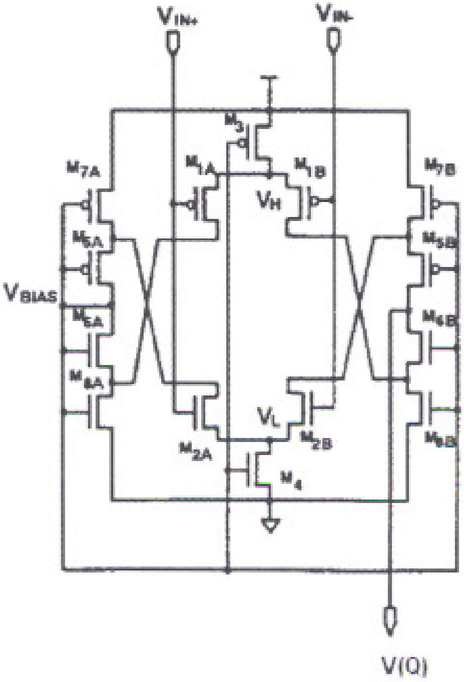


Fig. 1. Self-Biased Comparator

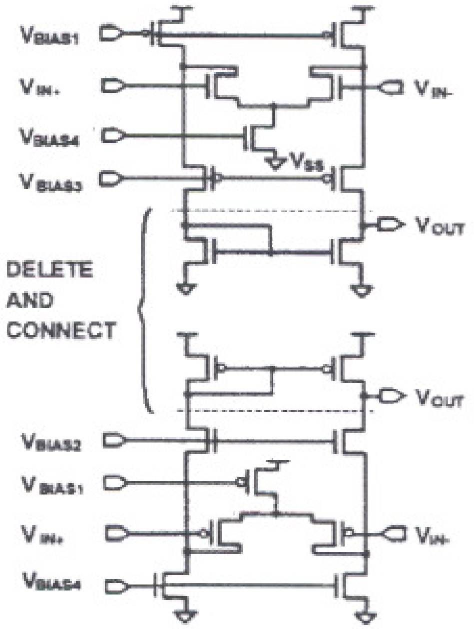


Fig. 2(a) Folded Cascode Differential Amplifier

In order for the circuit to be biased in stable fashion the currents through M3 and M4 devices should be identical. Any difference in currents through these two devices result in extreme shifts in amplifier bias voltages. Achieving perfect equality of currents in these two devices using external biasing is practically impossible, so that the configuration of Fig 2(b) is practically impossible.

A simple modification of the circuit of Fig. 2(b), however, results in stabilization of the bias voltages. This modification is illustrated in Fig 1, in which the two bias-voltages are disconnected from the external sources and instead are connected to internal amplifier node V_{BIAS}. This self-biasing of the amplifier creates the negative feedback loop that stabilizes the bias voltages. Any variations in the processing parameters or operating conditions that shifts the bias voltages away from their nominal values result in a shift in V_{BIAS} that corrects the bias voltages through negative feedback. The resulting self-biased amplifier is illustrated in Fig. 1.

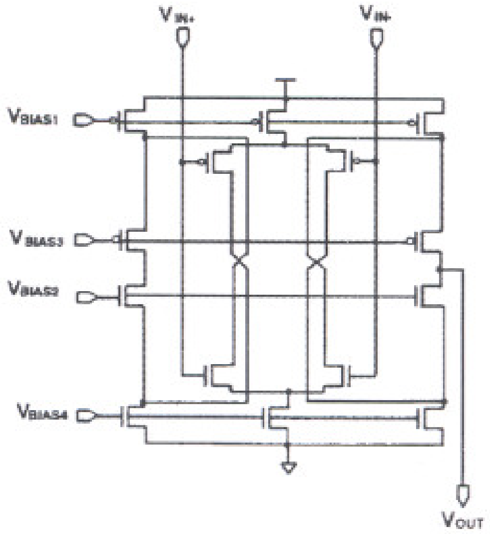


Fig. 2(b) Externally Biased Differential Amplifier

3. DESIGN PROCEDURE FOR SELF-BIASEDCOMPARATOR

A. SPECIFICATIONS

- Unity gain bandwidth (GB)
- Input common mode range [V_{in} (min) and V_{in} (max)]
- Load capacitance (C_L)
- Slew rate (SR)
- Output voltage swing [V_{out} (max) and V_{out} (min)]

B. DESIGN PROCEDURE

1. The first step towards design of self-biased comparator is to decide the bias currents in transistors M_3 and M_4 using the slew rate and load capacitance specifications. So we have

$$I_3 = I_4 = SR * C_L$$

2. Other bias currents I_7 and I_8 flowing through M_{7A} or M_{7B} and M_{8A} or M_{8B} should be designed in such a way that the dc current in cascode branches never goes to zero. To implement this, the values of these currents are normally between the values of I_3 or I_4 and twice their values. Now to calculate the W/L ratios of these transistor we need to calculate their drain to source voltages. From the specification of output voltage swing, we can se that the minimum voltage that make the transistors M_{7A} and M_{5A} to remain in saturation is that the droop between these two transistors is equal to the difference of the V_{DD} and V_{out} (max), similarly for M_{8A} and M_{6A} this voltage is V_{SS} and V_{out} (min). These voltages if we equally divide between the two respective transistors we get the drain to source voltage of the transistors. So taking this drain to source voltage and the bias current together we get

$$I_7 = I_8 = 1.3 * I_3$$

$$\left(\frac{W}{L}\right)_{7A,7B} = \frac{2 * I_7}{K_P * (V_{ds})^2}$$

$$\left(\frac{W}{L}\right)_{8A,8B} = \frac{2 * I_8}{K_N * (V_{ds})^2}$$

Assuming that transistors are in saturation the calculated drain to source voltage can be increased to twice its value so that the transistor remain in deep saturation area.

3. The current flowing in M_{5A} or M_{5B} and M_{6A} or M_{6B} is

$$I_5 = I_6 = I_7 - (0.5 * I_3)$$

$$\left(\frac{W}{L}\right)_{5A,5B} = \frac{2 * I_5}{K_P * (V_{ds})^2}$$

$$\left(\frac{W}{L}\right)_{6A,6B} = \frac{2 * I_6}{K_N * (V_{ds})^2}$$

Where V_{ds} we have already calculated in step 2.

4. For the design of differential pair we again assume that they are in saturation. Using the unity gain bandwidth

$$g_{m1} = g_{m2} = 2 * \pi * GB * C_L$$

$$\left(\frac{W}{L}\right)_{1A,1B} = \frac{g_{m1}^{\ 2}}{K_P * I_3}$$

$$\left(\frac{W}{L}\right)_{2A,2B} = \frac{g_{m2}^{\ 2}}{K_N * I_4}$$

5. Lastly the tail transistors are designed using input common mode range specification. From [1] we have

$$V_{ds4} = V_{IN}(\min) - V_{gs2A}$$

where

$$V_{gs2A} = \left(\sqrt{\frac{2 * I_4}{K_N * \left(W/L \right)_{2A}}} \right) + V_{TN}$$

$$\left(\frac{W}{L} \right)_4 = \frac{2 * I_4}{K_N * (V_{ds4})^2}$$

where V_{TN} is the threshold voltage for n-type transistor. Another tail transistor M_3 can be designed using the mobility ratio of n-type and p-type transistor.

4. SIMULATION RESULTS

In order to verify the procedure, the circuit was designed using that and then using T-SPICE it is simulated. Fig [3-7] shows comparator delay, gain, slew and resolution.

The comparator maintains the gain of 35.5 dB with phase margin of 59.3 degree. It can work up to the frequencies of 246.7 MHz i.e. this is the unity gain bandwidth. It can charge or discharge a load of 10 pf with slew rate of 28.42 V/μs and 26.4 V/μs respectively. The propagation delay is found to be 0.8 ns. It can resolve the voltage difference of 0.025 V. These all values are for specification of SR 1 V/μs, GB 10 MHz and C_L 10 pf.

5. CONCLUSION

The comparator designed takes the minimum delay as compared to [5-7]. Gain can be decreased to further reduce the delay. This comparator can charge or discharge the large capacitances within few nanoseconds. The design example as shown in the figures proves that it is possible to implement a CMOS comparator with maximum delay less than 1ns.

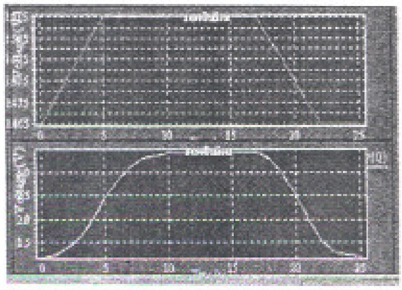


Fig.3 Resolution of Comparator

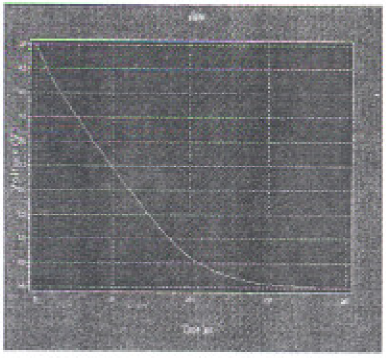


Fig. 4 Slew Rate from high to low

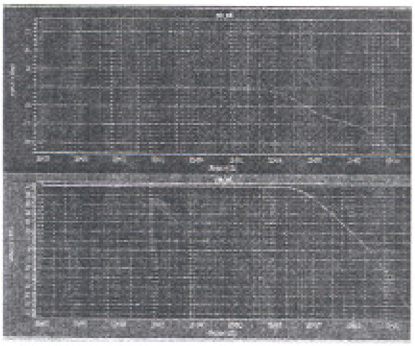


Fig.5 Unity Gain Bandwidth

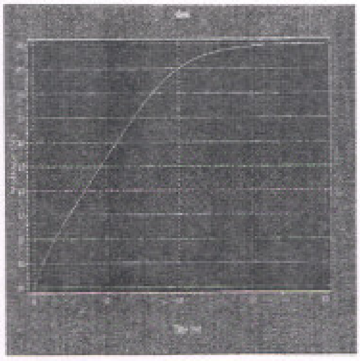


Fig.6 Slew Rate from low to high

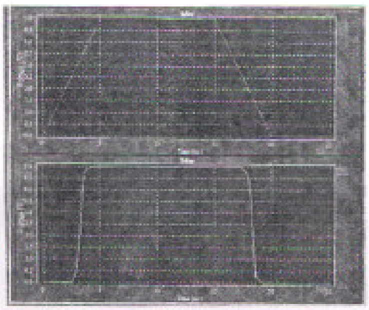


Fig. 7 Propagation Delay of Comparator

ACKNOWLEDGEMENT

The authors would like to acknowledge the financial support from MoCIT by way of SMDP-VLSI project. We are also thankful to Dr. S.C Saxena Director, Thapar Institute of Engineering and Technology, Patiala for his constant encouragement.

REFRENCES

[1] Allen Philip E., Holberg Douglas R., "*CMOS Analog Circuit Design* " Oxford University Press, London, 2003,Second Edition.

[2] Baker R.J, Li H.W, and Boyce D.E," *CMOS Circuit Design, Layout, and Sim ulation.* Piscataway, NJ: IEEE Press, 1998, Chap, 26.

[3] Maloberti Franco,"*Analog Design For CMOS VLSI Systems*" KLUWER academic Publisher, Boston/ Dordrecht/ London.

[4] M. Bazes,"*Two Novell Full Complementary Self Biased Differential Amplifier*," IEEE Journal of Solid State Circuits, Vol. 26, No. 2,pp. 165-168,February 1991.

[5] Benjamin J. McCarroll, Charls D. Sodini, Hae-Seung Lee, " *A High Speed CMOS Comparator For Use In An ADC*," IEEE Journal of Solid State Circuits, Vol. 23, No.1, February 1988.

[6] G. M. Yin, F. Op't Eynde and W. Sansen,"A High Speed CMOS Comparator With 8-Bit Resolution", IEEE Journal of Solid State Circuits, Vol. 27, No.2, February 1992.

[7] J. A. Fisher and R. Koch, "*A Highly Linear CMOS Buffer Amplifier*," IEEE Journal of Solid State Circuits, Vol. SC-22, No.3, June 1987.