Design of Two-Stage Fully-Differential Inverter-Based Self-Biased Gain-Boosted Amplifier in 0.18 µm CMOS Technology

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DECLARATION

I hereby declare that the dissertation entitled **"Design of Two-Stage Fully-Differential Inverter-Based Self-Biased Gain-Boosted Amplifier in 0.18 µm CMOS Technology"** is an authentic record of my work carried out as partial requirement for the award of degree of M.Tech (VLSI Design) at Thapar University, Patiala under the supervision of Dr. Alpana Agarwal, Associate Professor, ECED.

The matter embodied is this thesis has not been submitted for award of any other degree at this or any other university.

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ABSTRACT

This thesis work describes a two-stage fully differential gain-boosted CMOS amplifier consisting of two self-biased inverter stages. The self-biasing avoids the use of external biasing circuitry, thus reduces the die area and the power consumption. Although it relies on a class A topology, it achieves higher efficiency and comparable to the best class-AB amplifiers. In the present work regulated cascode technique has been employed for gain boosting. The miller compensation is also applied to enhance the phase margin. The circuit has been designed and simulated in 1.8 V 0.18 μm CMOS technology. The simulation results show a high DC gain of 100.7 dB, Unity Gain Bandwidth of 107.8 MHz and Phase Margin of 66.7^{o}, which makes it suitable for the pipelined ADCs.

TABLE OF CONTENTS

LIST OF ACRONYMS

CMOS	Complementary Metal Oxide Semiconductor
OP-AMP	Operational Amplifier
ADC	Analog-to-Digital Converter
FD	Fully-Differential
UGB	Unity Gain Bandwidth
DC	Direct Current
AC	Alternating Current
MOS	Metal Oxide Semiconductor
CS	Fully-Complementary Self-Bias
CSDA	Fully-Complementary Self-Biased Differential Amplifier
CMFB	Common-Mode Feedback
CM	Common-Mode
PVT	Process, Supply Voltage and Temperature
PM	Phase Margin

LIST OF FIGURES

LIST OF TABLES

CHAPTER 1

INTRODUCTION

Over the years there has been an increase in the complexity of the chips being designed [1]. This has resulted in an increased importance of the efficient implementation of both analog and digital functions using CMOS technology. Operational amplifiers or op-amps are an important building block in most of these analog and mixed circuit implementations. It is used in many circuits, which includes output buffers, sample and hold circuits and analog-to-digital converter or ADC [2]. Because of being crucial to the circuit operation, the performance of an op-amp significantly influences the system's performance.

This thesis report proposes an implementation of a two-stage fully-differential (FD) op-amp that uses an inverter as its first stage. To understand and judge whether the desired requirements are met by this circuit it is important to know the parameters that mark efficient operation of an op-amp. This chapter presents an overview of the op-amp as a device and the parameters that define its operation. The FD configuration that has been utilized in the research carried out has also been explained, alongwith the advantages offered by it and the applications that make use of it.

1.1 An Introduction to Operational Amplifiers

From its nomenclature it's evident that an operational amplifier or op-amp is an amplification device. Like other amplifier circuits it is expected to increase the amplitude of the input signal to a proportional output signal. It is required to offer this functionality without compromising on the linearity of the circuit. A feature that sets apart an op-amp from other amplification devices is that in addition to its input signal amplifying capabilities, it also allows the arithmetic or logical manipulation of the input signals. It is because of these operations, performed by it on the inputs, that it is known as an operational amplifier.

Many other reasons exist for the popularity of op-amps over other commercially available amplifiers [3]. The prime reason is being the versatility that they offer. They can be used

for the implementation of a wide variety of applications. Also, an op-amp's performance approaches that of an ideal amplifier. Unlike other amplifier circuits that amplify the environmental and other noise signals in conjunction to the applied input, an op-amp eliminates or minimizes this noise signal.

Figure 1.1 shows the symbol used for an op-amp [3]. It depicts three terminals. Out of the three terminals while two terminals (1 & 2) act as inputs the third one (3) is for output. In addition to the signal inputs the op-amp also requires dc power. This dc power is supplied to the circuit so as to result in a greater power at the output than what appears at the input. Therefore the terminals 4 and 5 are the two dc power inputs in the op-amp. While one is connected to a positive supply the other has a connection to a negative supply.

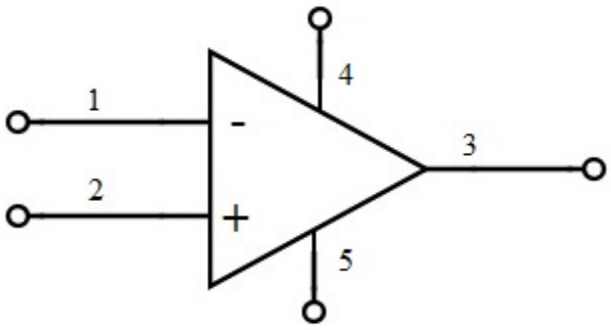


Figure 1.1 Symbol of an op-amp [3]

The figure above shows the symbol of an op-amp, however Figure 1.2 shows what lies inside of this symbolic representation. It is a generic block diagram representation of a simple two-stage op-amp [4].Vs and Vo denote the applied signal and the output voltage of the op-amp respectively. From the figure it can be observed that the following blocks make an op-amp:

i. First and foremost, an op-amp, as the name suggests, requires amplifiers. Being a two-stage op-amp implies that there are two amplifier stages (A1 and A2).

ii. A biasing circuit.

iii. A compensation network.

The roles of these blocks are more elaborately described in chapter 2.

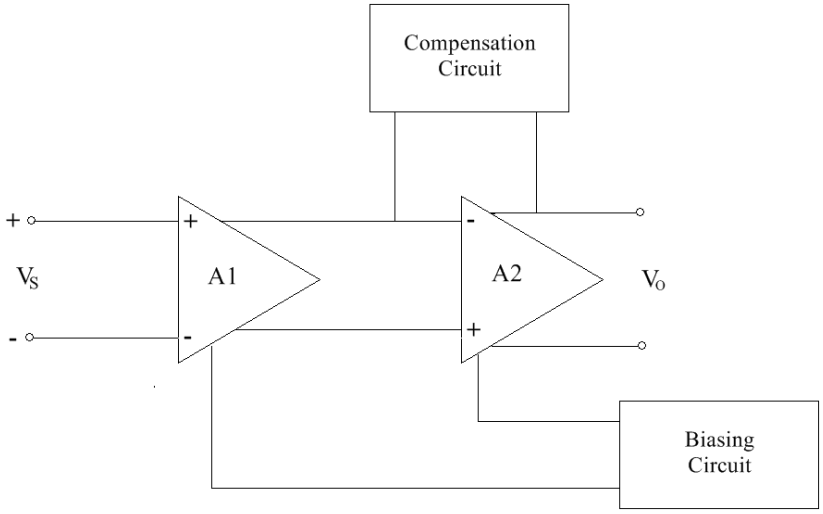


Figure 1.2 Block diagram of an op-amp [4]

The blocks in the Figure 1.2 can be replaced with the actual VLSI circuit implementations based on the application for which the amplifier is being designed.

1.2 Parameters Associated with An Op-amp

Op-amp parameters are very crucial to its designing. The performance of the amplifier is judged on the basis of these parameters. These include:

1. **Gain:** As is required for any amplifier, an op-amp is also required to exhibit very high gain. Ideally it should offer infinite gain. Practically however the value is finite [5].

2. **Input Impedance:** Ideally the input impedance of an op-amp which appears between the two input terminals is expected to be infinite. This implies that it is not possible for any current to flow into or out of the input terminals [6]. As a result, the applied input voltage is amplified to result in the output by the amplifier without drawing any current in between [3]. Practically this impedance is very high.

3. **Output Impedance:** The output terminal of the op-amp is where the output voltage signal appears. Therefore the terminal is expected to behave as an ideal voltage source that offers a voltage equal to the amplified output. This output should not fluctuate based on the current that the output load draws. This implies very clearly that the output impedance associated with the output voltage source should not have any impedance value associated with it, across which its output voltage may drop. Therefore ideally the output impedance should be zero. Practically it is a very small value [3]. The output resistance also affects the speed of charging/discharging of the output capacitor. Therefore it also decides the highest possible signal frequency [5].

4. **Common-Mode Rejection Ratio:** An op-amp works on the differential signal, i.e. the difference between the voltages that appear at the two input terminals. As a result signals that are common to both the inputs are cancelled out or rejected. This is called common-mode rejection by the op-amp. Therefore an op-amp should ideally offer zero common-mode gain. The inverse of this gain is known as the common-mode rejection and should be ideally infinite [3].

5. **Bandwidth:** The gain of a circuit is expected to remain constant for its range of operation. To achieve this it is important to know the range of frequencies over which the gain of a system is almost constant within a range (upto -3 dB). This is called the bandwidth of the circuit. For an amplifier its bandwidth and the spectrum of the signals that have to be amplified should coincide. Otherwise the different frequency components in the signal would be amplified by varying amounts, resulting in a distorted spectrum. The ideal op-amp's gain is expected to remain constant from zero frequency to infinite frequency, i.e. it has infinite bandwidth. As a result the op-amp is not used in the open-loop configuration. It is used with feedback loops. Practically the frequency response of an op-amp looks as shown in Figure 1.3 [5].

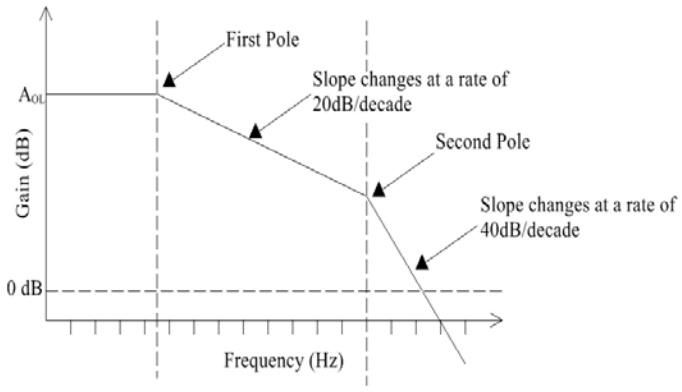


Figure 1.3 Frequency response of an op-amp [5]

Clearly the gain is not independent of the frequency and it starts to drop by 20 dB/ decade post the occurrence of the first pole. Therefore it is desirable that the first pole of the system occur at a very high frequency to improve the frequency range over which the amplifier works effectively [5].

6. **Gain Margin:** It is the margin by which the gain can still be increased up to the limit where the system becomes marginally stable at the phase cross-over frequency [7].

7. **Phase Margin:** The margin by which the phase of the circuit can be increased to bring the system at the verge of marginal stability at the gain cross-over frequency. The point at which the gain of the system is 0 dB is used as the point of measurement of the phase margin.

$$PM = 180^0 + \theta \tag{1.1}$$

where θ is the phase of the system at the 0 dB gain point. Although both the gain margin and the phase margin should be positive for a stable system, it is the phase margin which happens to be more important. This is because the phase margin also affects the transient behavior [7].

8. **Unity Gain Bandwidth (UGB):** With increasing frequencies the stray capacitances, finite carrier mobilities and other reasons, the gain of the circuit tends to decrease. Therefore an effective way to record this effect is the UGB for

the system. It is the frequency at which the gain of the circuit becomes equal to unity [5].

9. **Slew Rate:** There is a certain limit to the maximum rate of change possible at the output of the amplifier [3]. This maximum rate is known as the slew rate. It is expressed in the units of V/us. If the input signal expects the output response of the system to be faster than the slew rate the op-amp will not be able to comply. The reason for this is that for a large input step signal, certain transistors used in the op-amp circuit come out of the saturation region of operation, at times even moving into cut-off region [5]. This causes the output to follow the input at a decreased rate. Therefore slew rate is the maximum rate of change for the output.

1.3 Fully Differential Op-amp

A standard op-amp uses a single ended output, i.e. the amplified output is observed at a single output terminal. In case of a fully differential (FD) op-amp the outputs are differential, i.e. the output signal is the difference between the signals appearing at the two output terminals [8]. The difference can be observed in Figure 1.4.

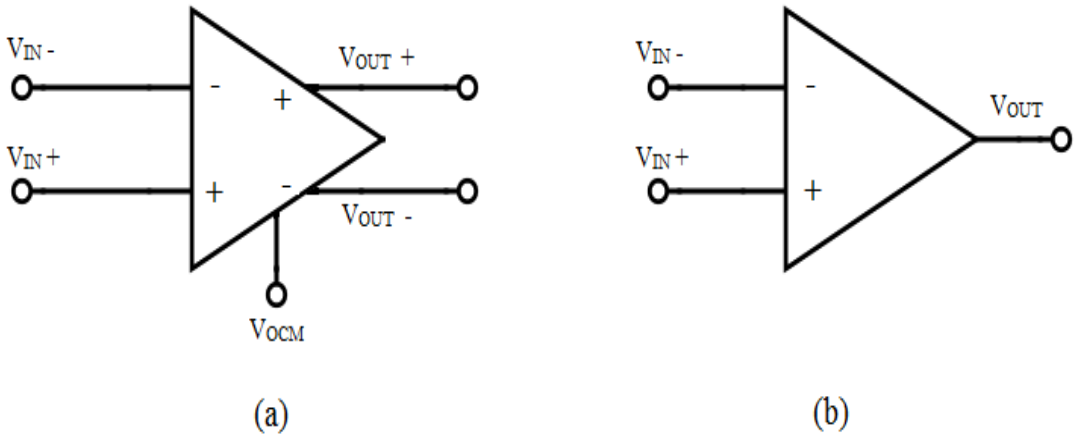


Figure 1.4 (a) Fully differential op-amp (b) Standard op-amp [8]

The output common mode voltage is denoted by V_{OCM} and can be controlled independent of the differential voltage. This is done by making use of an additional input, V_{OCM}. It is

used to control the output common-mode voltage. Therefore the output common-mode voltage is not defined by the input. Instead a V_{OCM} error amplifier ensures that the output common voltage reflects the voltage applied to the V_{OCM} pin by making a comparison between the sampled output common- mode voltage and the voltage that is applied to the pin [8].

1.4 Advantages of using Fully Differential Op-amp

There are several advantages offered by the fully-differential configuration of an op-amp. These have been listed below [8]:

1. **Improved Immunity to Noise:** Whenever the signals in a system need routing to move from one part to another, noise is, invariably, coupled into the wires used for making connections. For the case of a differential system, the wires are placed close together which makes the noise, coupled to the wires, appear as a common-mode signal. A differential amplifier always rejects the common-mode signals. As a result, the system exhibits improved immunity to noise. This has been depicted in Figure 1.5 [8].

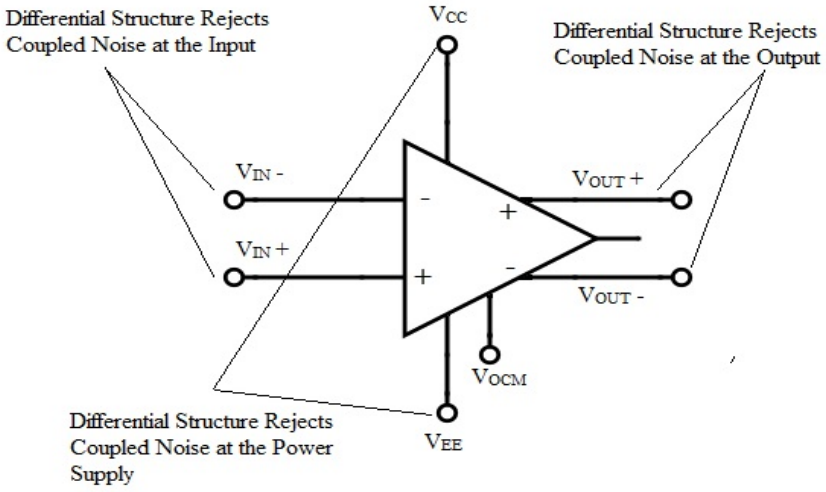


Figure 1.5 Fully-differential amplifier noise immunity [8]

V_{IN-} and V_{IN+} are the input terminals and V_{OUT+} and V_{OUT-} are the differential outputs of the FD op-amp. V_{CC} and V_{EE} are the connections to the power rails.

2. **Increased Output Voltage Swing:** A change in phase exists between the differential outputs of a FD amplifier. Because of this the differential output, which is equal to the difference of the signals appearing at the two output terminals, is doubled. Therefore, when compared to a single-ended output amplifier, a FD amplifier offers double the output voltage swing. As a result, FD amplifiers are preferred for low-voltage applications. Figure 1.6 further clarifies this.

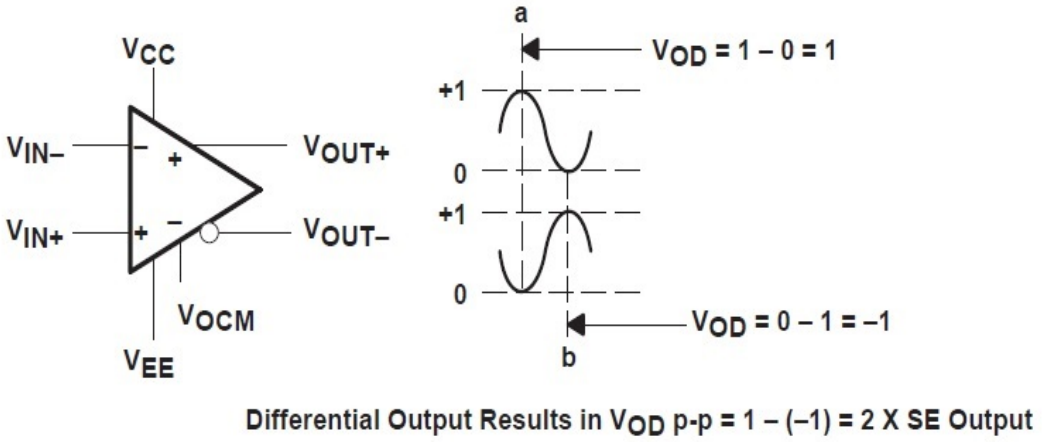


Figure 1.6 Differential output voltage swing [8]

3. **Reduced Harmonic Distortion:** Harmonic distortion is used to determine the linearity of a circuit. Lower the harmonic distortion better is the linearity offered by the system. In a FD amplifier the even order harmonics are cancelled out at the differential outputs. This can be better understood from the following mathematics.
If a generic expansion of the output signals appearing at the two terminals, i.e. V_{OUT-} and V_{OUT+} is carried out, the following results [8]:

$$V_{OUT+} = K_1 Vin + K_2 Vin^2 + K_3 Vin^3 + \ldots. \quad (1.2)$$

$$V_{OUT-} = K_1(-Vin) + K_2(-Vin)^2 + K_3(-Vin)^3 + \ldots. \quad (1.3)$$

Here, K_1, K_2, K_3..are constants. The squared and cubed terms correspond to the second and third order harmonics, respectively.

Therefore, the differential output becomes:

$$Vod = 2K_1Vin + 2K_3Vin^3 + \ldots. \quad (1.4)$$

Clearly, the even order harmonics do not appear in the differential output. Therefore, the even-order terms that remain positive in both, (1.2) and (1.3), cancel out in (1.4). This results in an odd- harmonics only output signal.

1.5 Motivation

As has already been discussed in the preceding sections, the op-amp is a very important component in most analog and mixed systems. Therefore, it is very crucial that it matches the requirements of the current trends offered by the industry. In the conventional electronics market, low-voltage operation, along with low-power dissipation is an important parameter for all devices. Op-amps are no exception to this. It is important that they also evolve to be compatible in this low-voltage low-power environment. This is the motivation behind the research carried out.

A two-stage FD operational amplifier design has been proposed. Cascading is used to avoid the output swing reduction that results in the case of cascoding. This is important because in low-voltage operation the already small swing cannot be further compromised. The cascaded connection of the two stages also ensures an improvement in the gain offered by the device.

The proposed implementation is designed to use an inverter-based first stage. This increases the transconductance of the stage-I, thereby improving the gain offered by the stage. In addition to this, the final gain offered by the circuit has been further enhanced by making use of a gain- boosting circuit.

Therefore, the proposed design is the future of op-amp technology. It improves the gain of the device while maintaining its viability as an efficient low voltage component that can be used in the present day electronics.

1.6 Organization of Thesis

This chapter served as a basic introduction to the concept of an op-amp and also the parameters that define its working. It also gives a brief description of the motivation behind this research topic.

In Chapter 2, the techniques that have been used in the proposed design have been discussed. The discussion presents an account of the occurrences of these techniques in literature.

In Chapter 3, the design methodology has been presented.

Chapter 4 presents the design and analysis of the proposed amplifier and discusses the results obtained from the PSPICE simulations for the designed circuit.

Chapter 5 concludes the report, while also mentioning the future possibilities for the applications of this circuit.

CHAPTER 2

LITERATURE SURVEY

This chapter describes the biasing schemes, the feedback techniques, gain boosting techniques and the existing FD amplifier structures that have been presented in literature in the past.

2.1 Biasing Schemes

Biasing is crucial to all types of amplifying devices. It is the biasing of the device that provides the power required by it to amplify the input signal. Various techniques exist for biasing the transistors in a circuit. Biasing of a circuit defines its steady state traits of operation in the absence of any applied signals [9]. An op-amp biased to a particular voltage implies that the output terminal rests at that voltage in the absence of a signal. Therefore, biasing is a purely DC value. With the application of an AC input signal, the output assumes values about this bias point. Therefore, it becomes important that an amplifier be so biased that the capabilities of the op-amp are not compromised and it can offer a good range to the signals applied. As a result, it becomes very important that an amplifier be properly biased before the signals that it outputs are applied to the inputs of an analog-to-digital converter, i.e. an ADC. If the signal output of the op-amp does not cover the complete input range of the ADC, the bit resolution of the ADC will be compromised.

2.1.1 Current Mirror Based Biasing

Both voltage biasing and current biasing are available options. However, current biasing has gained popularity in recent times. Current biasing is implemented using current mirrors in MOS networks. This works on the principle that, when MOS devices are in the saturation region of operation, an approximately constant current flows through them. For this constant current, a constant voltage drop is exhibited by the device [4]. A FD amplifier using the current mirror based biasing scheme has been discussed in [4].

2.1.2 Self-Biasing

Self-biasing technique not only reduces the area and power overheads but also reduces the sensitivity of the set biasing point to the process variations [10]. As the name suggests, self-biasing does not use any additional devices or biasing voltage sources for biasing purposes. Instead the scheme uses the power rails (V_{DD} and V_{SS}) only. This is the reason behind the elimination of the power and area overheads. The determination of the biasing point is done post an extensive circuit analysis. During this analysis, the transistor sizing constraints are determined.

Self-biasing technique used is a fully complementary self-biased (CS) technique. The fully-complementary part implies that the amplifier circuits are completely complementary, i.e. for every n-type device in the circuit; a complementary p-type device is used [11]. This facilitates a push-pull operation of the circuit. The derivation of a fully-complementary self-biased differential amplifier (CSDA) from the conventional CMOS amplifier configuration, better explains the concept. Figure 2.1 (a) shows two CMOS differential amplifiers [11]. As is evident from the figure, the two are complements of each other. These circuits use a current mirror as load. As the first step of derivation, these loads are eliminated from both the circuits. Following this the drains of the input-pair of one amplifier are connected to the drains of the other. This results in the fully-complementary circuit depicted in Figure 2.1 (b). However, the circuit still uses external biasing. The biasing of this circuit lacks stability. Stable biasing requires that the current flowing through the devices M3 and M4 be identical. Even a minor difference in these currents would cause the amplifier bias voltages to shift drastically. Due to the unstable biasing offered by the circuit in Figure 2.1 (b), it proves to be impractical.

To achieve perfect stability of the bias voltages, the circuit of Figure 2.1 (b) has to undergo a slight modification, resulting in the circuit of Figure 2.1 (c). The two voltage sources, being utilized for biasing purposes, are eliminated from the circuit. The bias-voltage inputs now draw their voltage from an internal node in the amplifier, V_{BIAS}. With this the conditions of self-biasing are met. This voltage, drawn from the node in the circuit, results in a negative feedback. The negative feedback, in turn, stabilizes the bias-voltages. If there happens to be a variation in the processing parameters or operating

conditions, a resultant shift will also be introduced in V_{BIAS}. This shift in the biasing voltage would lead to a correction of the bias voltages, using negative feedback.

Therefore, the figure 2.1 (c) is the CSDA.

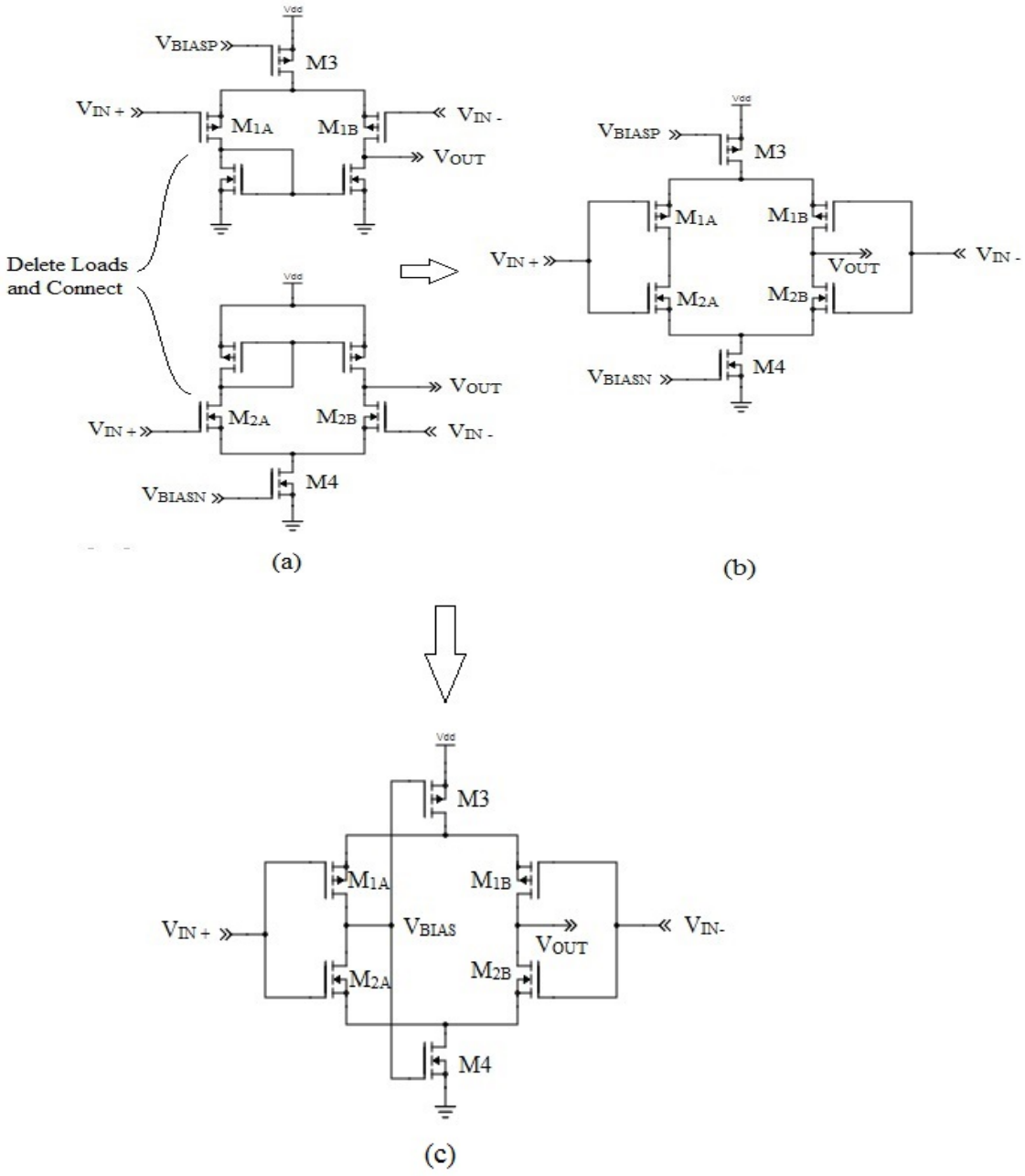


Figure 2.1 Derivation of CSDA [11]

In the CSDA configuration the transistors M3 and M4 are to operate in the linear region. Since these two transistors define the two voltages, V_H and V_L and these voltages define

the output swing of the amplifier. By setting the value of these voltages close to the supply rails, the output swing of the amplifier can be made approximately equal to the difference between the supply rail voltages. By doing so the CSDA based circuits can be easily interfaced with the conventional CMOS circuits.

Another advantage of these transistors' linear region operation is the large magnitude of the output switching currents. These currents have a much larger magnitude than the quiescent current. This is a significant advantage over the conventional CMOS circuits where the switching currents cannot go higher than the quiescent current which is set by the transistor operating in saturation region as a current source. Since CSDA based circuits are capable of generating these large current pulses, they are a suitable option for use in high-speed comparators. This is because the high speed operation in case of such devices is possible only if the capacitive loads can be charged and discharged at very fast rates while also ensuring low power dissipation.

The use of a fully-complementary configuration also has a benefit associated with it. Being fully-complementary the CSDA has a DC differential mode gain which is approximately double the gain offered by any other conventional amplifier. From figure 2.1 (a) it is clear that both the amplifiers use only two devices for amplification ($M_{1A\text{-}B}$ or $M_{2A\text{-}B}$). However, in case of CSDA the number of amplification devices double to four (both $M_{1A\text{-}B}$ and $M_{2A\text{-}B}$). For CSDA the differential mode gain (A_d) is formulated as [11]:

$$A_d = \frac{g_{m1}+g_{m2}}{g_o} \tag{2.1}$$

where g_{m1} is the transconductance of device $M_{1A\text{-}B}$ and g_{m2} is the transconductance of device $M_{2A\text{-}B}$. The amplifier's output conductance is denoted by g_o.

2.2 Common-Mode Feedback

Common-mode feedback (CMFB) is required in fully-differential circuits for the control of the common-mode output signal [12]. The basic principle of CMFB is the monitoring of the output common-mode signal ($V_o^+ + V_o^-$), and its comparison with a reference voltage, usually ground. Figure 2.2 shows the principle involved. The first step is the monitoring of the output common mode signal (V_{CMC}), next is its comparison with the

reference voltage (V_{REF}). The comparison results in a correction signal ($V_{CORRECTION}$), i.e. the difference between the common-mode signal and the reference voltage. This correction signal is then applied to the fully-differential amplifier so as to make this signal or the difference between the two voltages (V_{CMC} and V_{REF}) zero eventually.

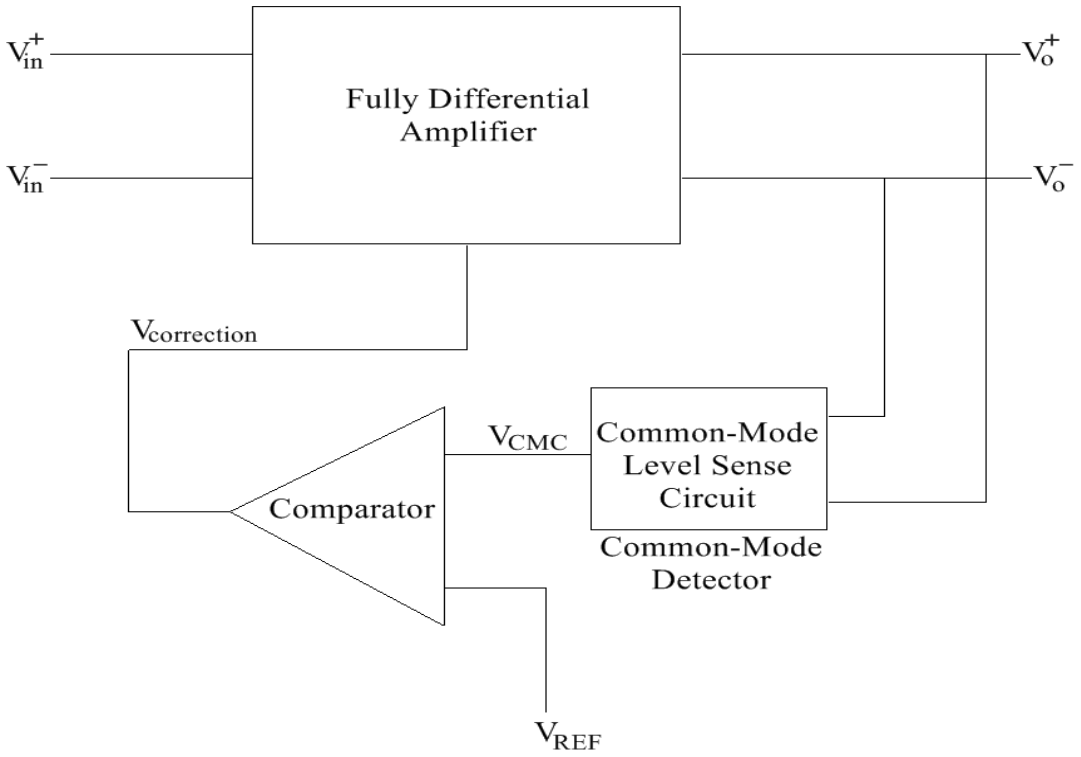


Figure 2.2 Block diagram of common-mode feedback circuit [12]

CMFB is required to meet the following objectives:

(a) Cancellation of the common-mode signals that appear at the output.

(b) Fixing the DC bias point of the amplifier circuit to achieve the maximum possible differential voltage gain.

(c) For reduction of output noise.

2.3 Frequency Compensation Techniques

Both analog and mixed signal circuits make use of negative feedback techniques [4]. But feedback systems may suffer from instability if not checked for oscillations. With the addition of every new stage in an amplifier a pole is added to the closed loop system. If this pole is located at a point with an order that is less than ten times that of the dominant pole, the phase of the amplifier circuit falls severely. Beyond the point of phase crossover, even a small amount of feedback gets added to the input, thereby saturating the output. It is also possible that even with a non-negative phase margin degradation of performance is observed. This can result from oscillations or ringing. Therefore for stable circuit operation it is very important that the circuit has a good amount of phase margin. Generally a value of 60 degrees is considered optimum for phase margin of an amplifier circuit.

Frequency compensation techniques are used to either eliminate or at least nullify the effect of poles in the circuit's frequency response. Several techniques exist for this purpose. These include pole splitting miller compensation, self compensating capacitor, feed-forward compensation that uses an additional amplifier and negative miller compensation.

Miller compensation, also known as pole splitting has been used in the research work reported in this dissertation. With the advent of multi-stage amplifiers it has become important that the circuits be compensated for stable closed-loop operation [13].A two-stage op-amp's frequency behavior is defined by the two poles of the amplifier. Miller compensation achieves a stabilized response by increasing the distance between these two poles, i.e. the dominant and the non-dominant pole. This is done by using a capacitance connected from the output to the input of the second stage of the amplifier circuit [14]. It is a large capacitance using which the dominant pole ($P_1^{'}$) is pushed closer to the origin of the complex plane (P_1) and the non-dominant pole($P_2^{'}$) is pushed further left to the origin (P_2). By doing so the non-dominant pole does not affect the frequency response till the gain becomes much less than unity. Therefore, by splitting the two poles in a two-stage op-amp far apart from each other, as shown in Figure 2.3, stable operation of the circuit is achieved.

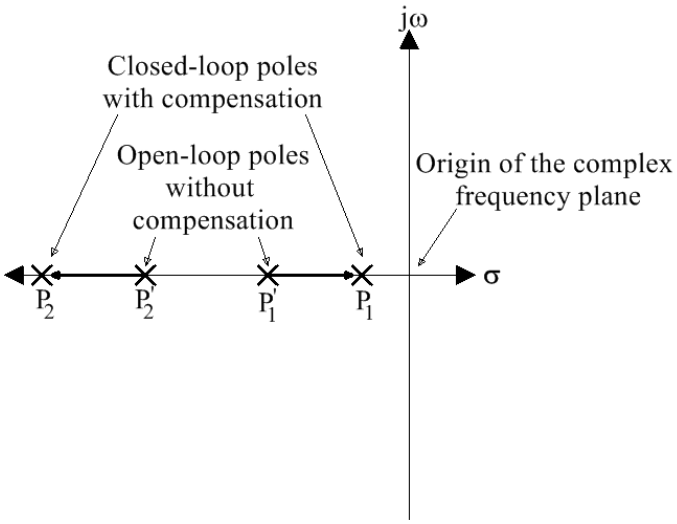


Figure 2.3 Pole-splitting in two-stage op-amp using miller compensation [14]

2.4 Gain Boosting Techniques

2.4.1J. Raman et al., 2010 [15]

This paper represents an implementation of a two-stage feed-forward amplifier. The amplifier topology makes the use of free transconductance of the folding current sources to boost the DC gain of folded cascade amplifier. The single stage differential pair converts the input voltage to a current. A current splitter extracts the part of current needed for feed-forward and for the first gain stage. There are some applications which require higher open loop gain than a basic telescopic or folded cascode amplifier. This can be achieved by using regulated cascode, but it results in a second order system that needs compensation. Miller and Ahuja compensation are two commonly used techniques. Feed-forward compensation is another approach that overcomes some of the limitations of former mentioned techniques.

2.4.2 H. Luo et al., 2013 [16]

This paper provides a cascoded sigma-delta modulator using a gain-boost class-C inverter as shown in Figure 2.4[16].The gain-boost inverter behaves as a sub-threshold amplifier and boosts its gain. The gain-boosting increases the inverter gain from 48 dB to 67 dB. It

forms a current-voltage feedback loop with the transistor at the output node. As a result output impedance and DC gain of the inverter in enhanced. The low supply voltage and low power consumption makes gain-boost class-c inverter suitable for low-power high-resolution applications.

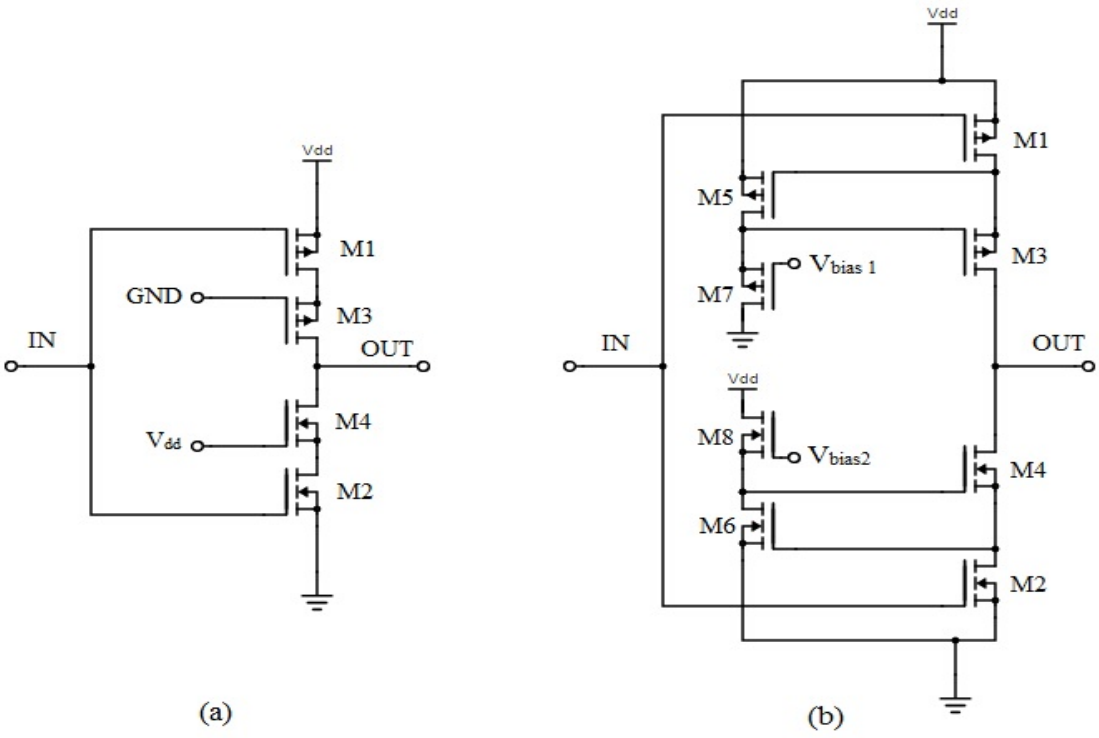


Figure 2.4 (a) Traditional cascode class-C inverter and (b) Gain-boosted class-C inverter [16]

2.4.3 N. N. Ghosh et al., 2013 [17]

This paper presents a Potential Distribution Method which guarantees that all transistors are operating in saturation region. It is a simple and quick method, which is process independent. It is also independent of device length and complex device equations. This method describes a regulated cascode technique for gain boosting.

The designing of op-amps have become very difficult with the reduced supply voltage and the continuous downscaling of transistor length in order to make low power and energy efficient circuits. And because of these sub-micron techniques there is a decrease in the gain of amplifier. Therefore increasing the gain of op-amp has become very important. But stacking of more transistors leads to a voltage headroom problem. Therefore solution

to this problem is offered by using a gain boosting technique without sacrificing the output voltage swing. In this technique an inverter stage is used with regulated cascode gain-boosting technique. A typical gain boosting technique is shown in the Figure 2.5 [17].

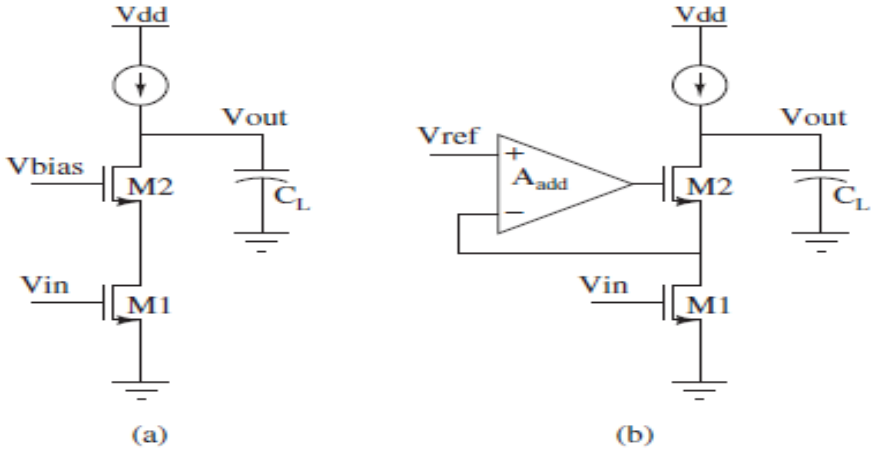


Figure 2.5Typical amplifier (a) without gain boosting (b) with gain boosting [17]

The gain of the op-amp is increased by simply increasing the cascoding effect of M2 by providing a negative feedback loop to M2 with the help of gain-boosting amplifier $A_{add.}$ The gain of the cascode stage is given as:

$$A_v = g_{m1} R_{out} \tag{2.2}$$

Where R_{out} is given by:

$$R_{out} = r_{o1} + r_{o2} + (g_{m2} + g_{mb2}) \times r_{o1} r_{o2} \tag{2.3}$$

After applying gain boosting R_{out} modifies to a new expression:

$$R_{out} = r_{o1} + r_{o2} + (g_{m2}(A_{add} + 1) + g_{mb2}) \times r_{o1} r_{o2} \tag{2.4}$$

This further simplifies to,

$$R_{out} \approx A_{add}\, g_{m2} r_{o1} r_{o2} \tag{2.5}$$

It can be seen from the above expressions that the boosting technique increases the output resistance by a factor of A_{add}, therefore increases the overall gain of the amplifier, given as:

$$A_v = g_{m1} R_{out} = A_{add}\, g_{m1} g_{m2} r_{o1} r_{o2} \tag{2.6}$$

2.5 Role of OTA in Pipelined ADC

The need for high performance digital signal processing in various fields has promoted the development of high resolution and high speed data converters. The main architecture used in high speed Analog to Digital Converters is the pipelined ADC architecture because of its higher conversion rate. The performance of op-amp limits conversion rate of ADC. Therefore the op-amps used in pipelined ADCs must have high gain and high unity gain bandwidth.

2.6 Problem Statement

After looking into the literature, the main objective of this work is to design a low-cost, low-power, low-current, high DC gain (≥ 100 dB) and high speed (UGB ≥ 100 MHz) OTA for pipelined ADC applications with less design efforts.

CHAPTER 3
DESIGN METHODOLOGY

3.1 Design and Analysis of Two Stage Inverter Based Op-Amp

A two-stage inverter-based fully differential op-amp is shown in Figure 3.1 [18]. It can be seen that two inverter stages having the similar topology are cascaded. The current sources, M11 and M14, are connected to input-stage inverter pair (M12-M13). These current sources provide the biasing and common-mode (CM) voltage to the input stage. The output stage consists of inverter pair (M22-M23) which are connected to current sources, M21 and M24, providing biasing voltage and common-mode (CM) output level to the output stage.

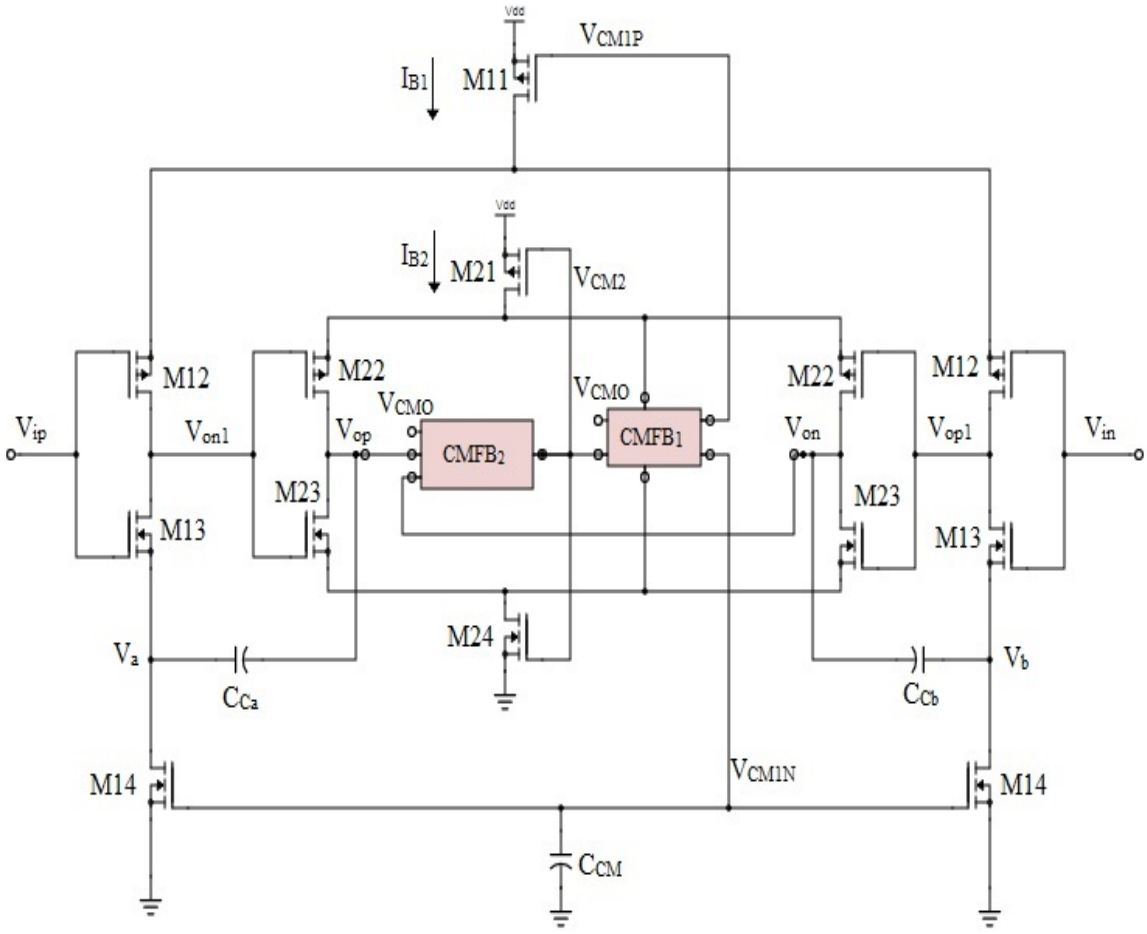
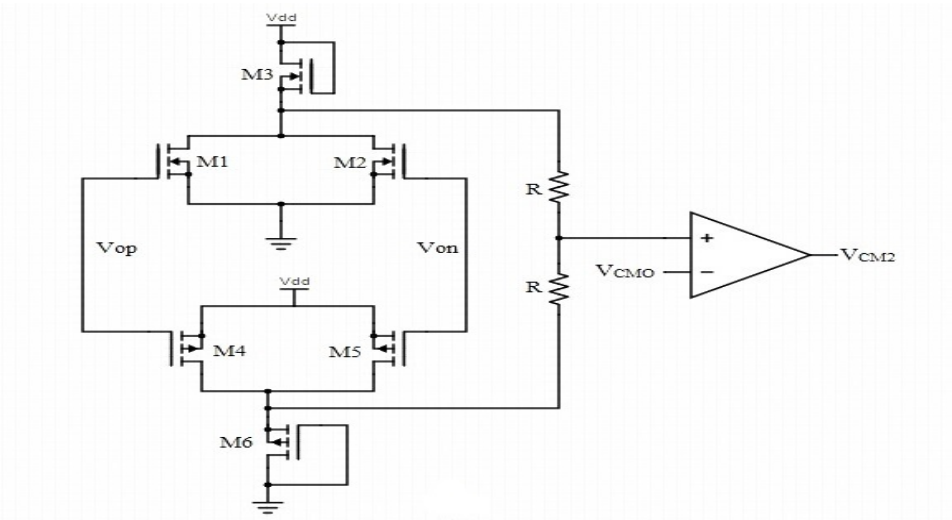


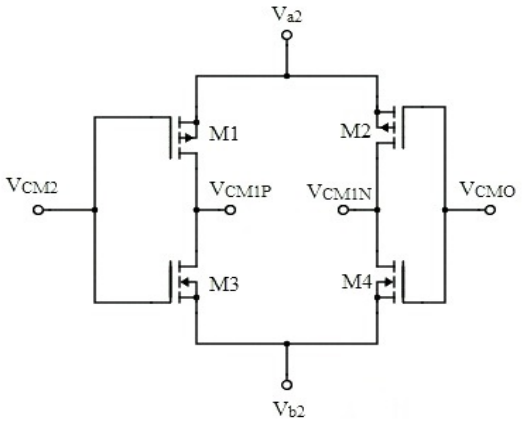
Figure 3.1 Two-stage inverter-based amplifier [18]

The two common-mode feedback blocks used in Figure 3.1 are illustrated in circuit diagrams shown in Figure 3.2 (a) and (b) [18] [19]. These continuous-time common-mode feedback circuits are used to bias the circuit and to provide the common-mode (CM) control voltages to input and output stages. The common-mode feedback circuit $CMFB_2$ in Figure 3.2 (a) generates a control voltage V_{CM2} which biases M21 and M24. The V_{CM2} is given by the expression:

$$V_{CM2} = \frac{V_{op} + V_{on}}{2} \tag{3.1}$$



(a)



(b)

Figure 3.2 Continuous-time CMFB circuits: (a) $CMFB_2$ (b) $CMFB_1$ [18] [19]

The common-mode feedback circuit $CMFB_1$ in Figure 3.2 (b) compares V_{CM2} with a constant voltage V_{CM0} and generates the voltages V_{CM1P} and V_{CM1N} to bias the input stage. The voltages generated by $CMFB_1$ and $CMFB_2$ are self-biased voltages [18].

Small Signal Analysis

In order to gain insight into the above topology of Figure 3.1 and to understand its working, a small signal analysis needs to be done. The working and topology of both stages are similar, thus, the small signal model for stage one also explains the working of stage two. The equivalent small signal model for the input stage is shown in Figure 3.3.

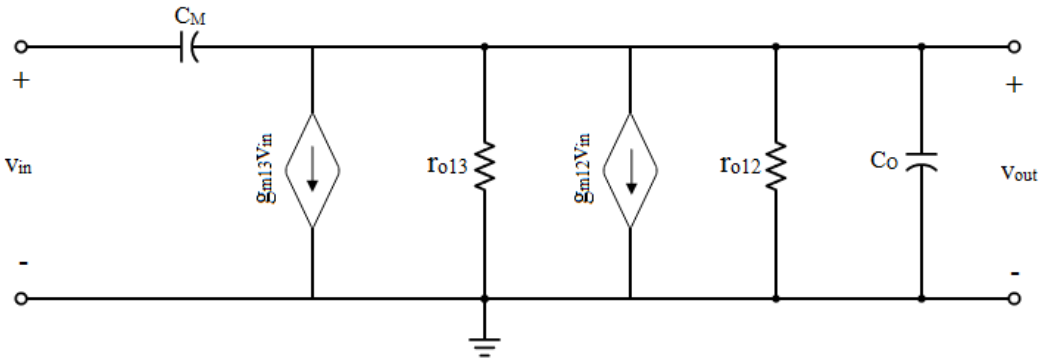


Figure 3.3 Small signal model for input stage

The transfer function of input stage is given by:

$$A_{v1} = \frac{g_{m13} + g_{m12}}{g_{ds13} + g_{ds12} + g_{m13} + g_{m12} + C_o} \tag{3.2}$$

where, $C_M = C_{gd13} + C_{gd12}$ and $C_o = C_{ds12} + C_{ds13}$

Similarly the transfer function for second stage is given by

$$A_{v2} = \frac{g_{m23} + g_{m22}}{g_{ds23} + g_{ds22} + g_{m23} + g_{m22} + C_{o2}} \tag{3.3}$$

where, $C_{o2} = C_L + C_{ds22} + C_{ds23}$

Now, the overall gain A_v is given as:

$$A_v = A_{v1} \times A_{v2} \tag{3.4}$$

$$A_v = \frac{(g_{m13} + g_{m12})(g_{m23} + g_{m22})}{(g_{ds13} + g_{ds12} + g_{m13} + g_{m12} + C_o)(g_{ds23} + g_{ds22} + g_{m23} + g_{m22} + C_{o2})}$$

Or

$$A_v \approx \frac{(g_{m13} + g_{m12})(g_{m23} + g_{m22})}{(g_{ds13} + g_{ds12})(g_{ds23} + g_{ds22})} \tag{3.5}$$

SIMULATION RESULTS

The frequency response of two-stage fully-differential inverter based op-amp is shown in the Figure 3.4. The gain of the op-amp is limited to 69.14 dB, but this can be increased by applying a gain boosting technique.

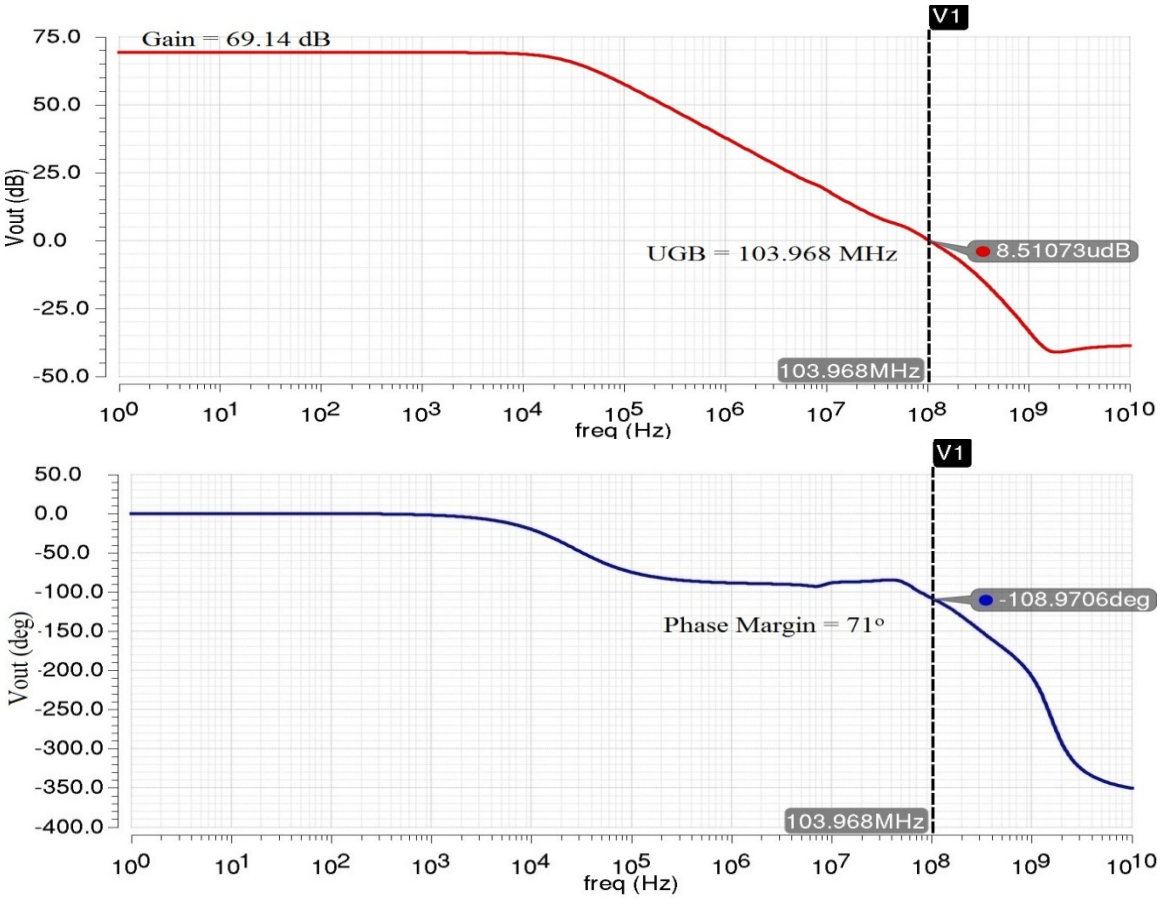


Figure 3.4 Frequency response of two stage fully differential inverter based op-amp

The Unity Gain Bandwidth is the frequency at which open loop gain becomes unity. The phase margin can be calculated from the frequency response graph shown in Figure 3.4. First determine the frequency at which open loop gain is unity, and note the phase value at this particular frequency. This value comes out to be 108.97^{o}. Then this value is subtracted from 180^{o} to obtain a difference which is called phase margin. Thus the simulated unity gain bandwidth of the op-amp is 103.96 MHz and its phase margin is 71^{o}.

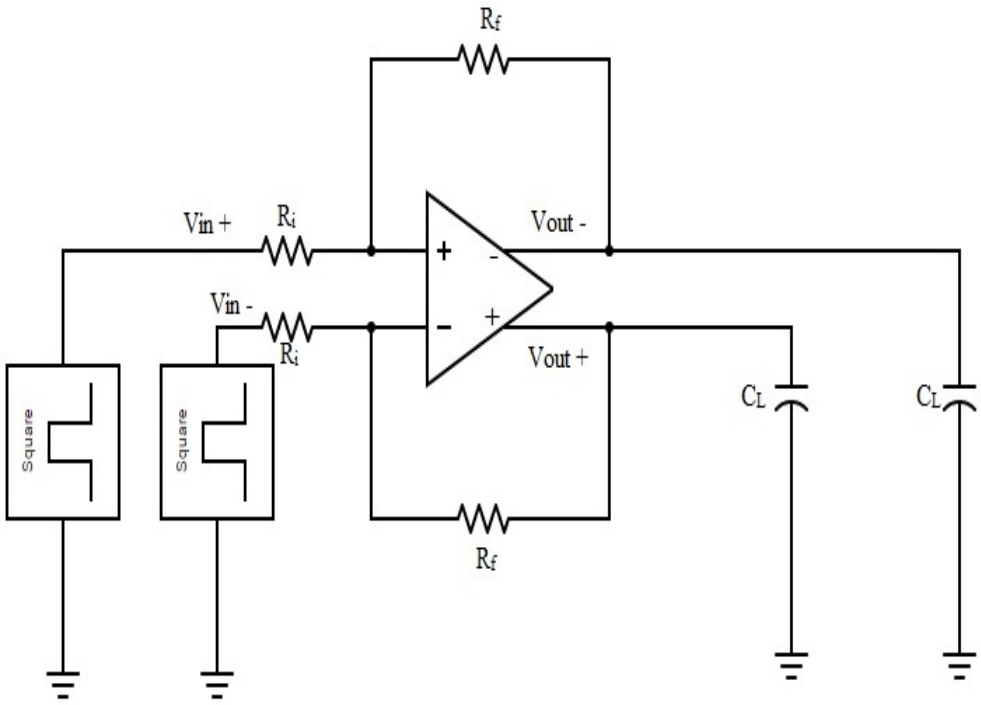


Figure 3.5 Test bench for transient response

The test bench for the transient response of op-amp is shown in the Figure 3.5 and the respective result after applying a step signal of 0.8 Vp-p is shown in the Figure 3.6. The slew rate found by calculating the slope of rising edge of the output waveform comes to be 30V/ us.

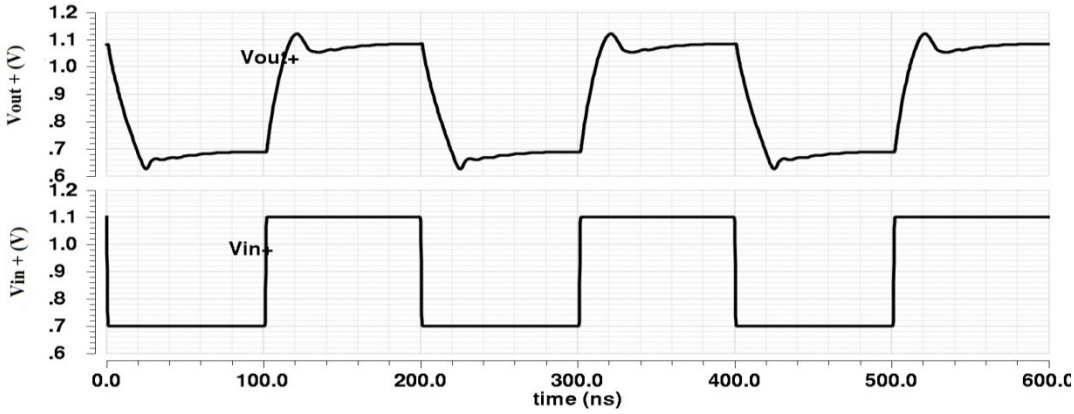


Figure 3.6 Transient step response of the op-amp

The Table 3.1 shows the simulation results for various performance parameters.

Table 3.1 Simulation Results

S.No.	Performance Parameters	Simulated Results
1	Technology (µm)	0.18
2	Power Supply (V)	1.8
3	Gain (dB)	69.14
4	Unity Gain Bandwidth (MHz)	103.9
5	Power Dissipation (mW)	0.246
6	Slew Rate (V/µs)	30
7	Phase Margin (^{o})	71
8	Load Capacitance (C_L)	4

3.2 Gain Boosting

The regulated cascode gain boosting technique is applied to circuit given in Figure 3.1. Again-boost module is added to the output inverter stage as shown in Figure 3.7. The gain-boost module, including transistors from M31 to M34, build up two current-voltage feedback loops together with transistors M23 and M24, respectively. As a result, the output impedance and the dc gain of the inverter are enhanced.

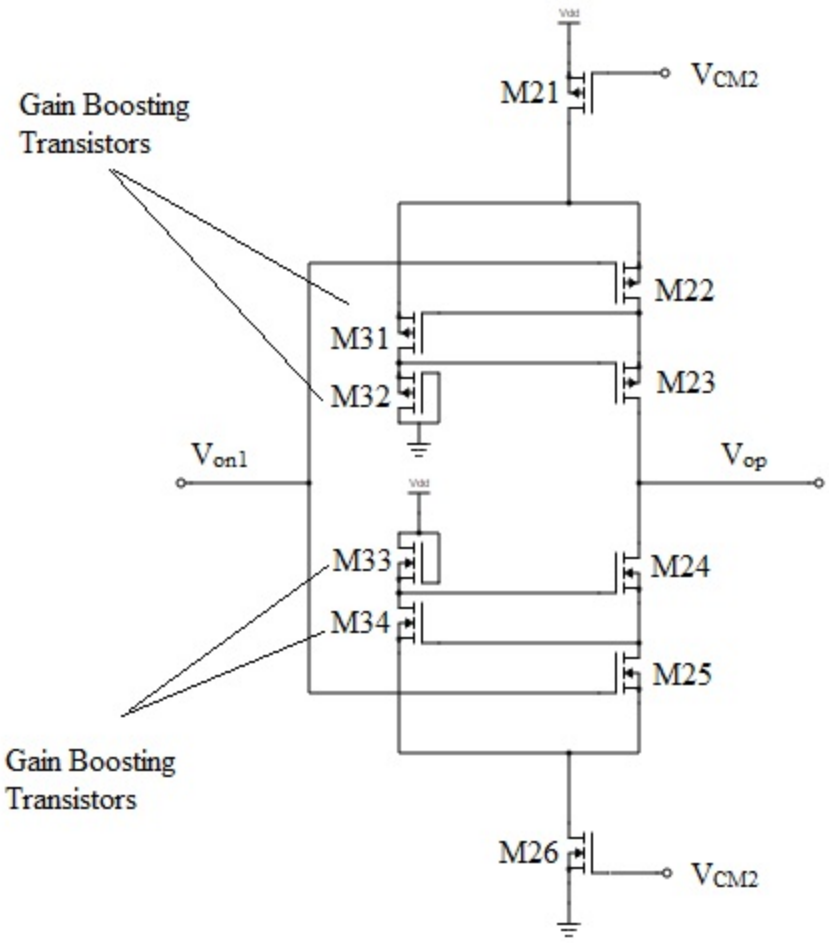


Figure 3.7 Regulated cascode gain boosting applied at output stage

SIMULATION RESULTS

Bode plot in Figure 3.8 shows the frequency response of the circuit after adding the regulated cascode feedback technique to it. The gain of the op-amp is enhanced to 100.71 dB and the unity gain bandwidth achieved is 186.53 MHz. The phase margin is reduced to 41.2^{o}, due to addition of unwanted poles and zeroes.

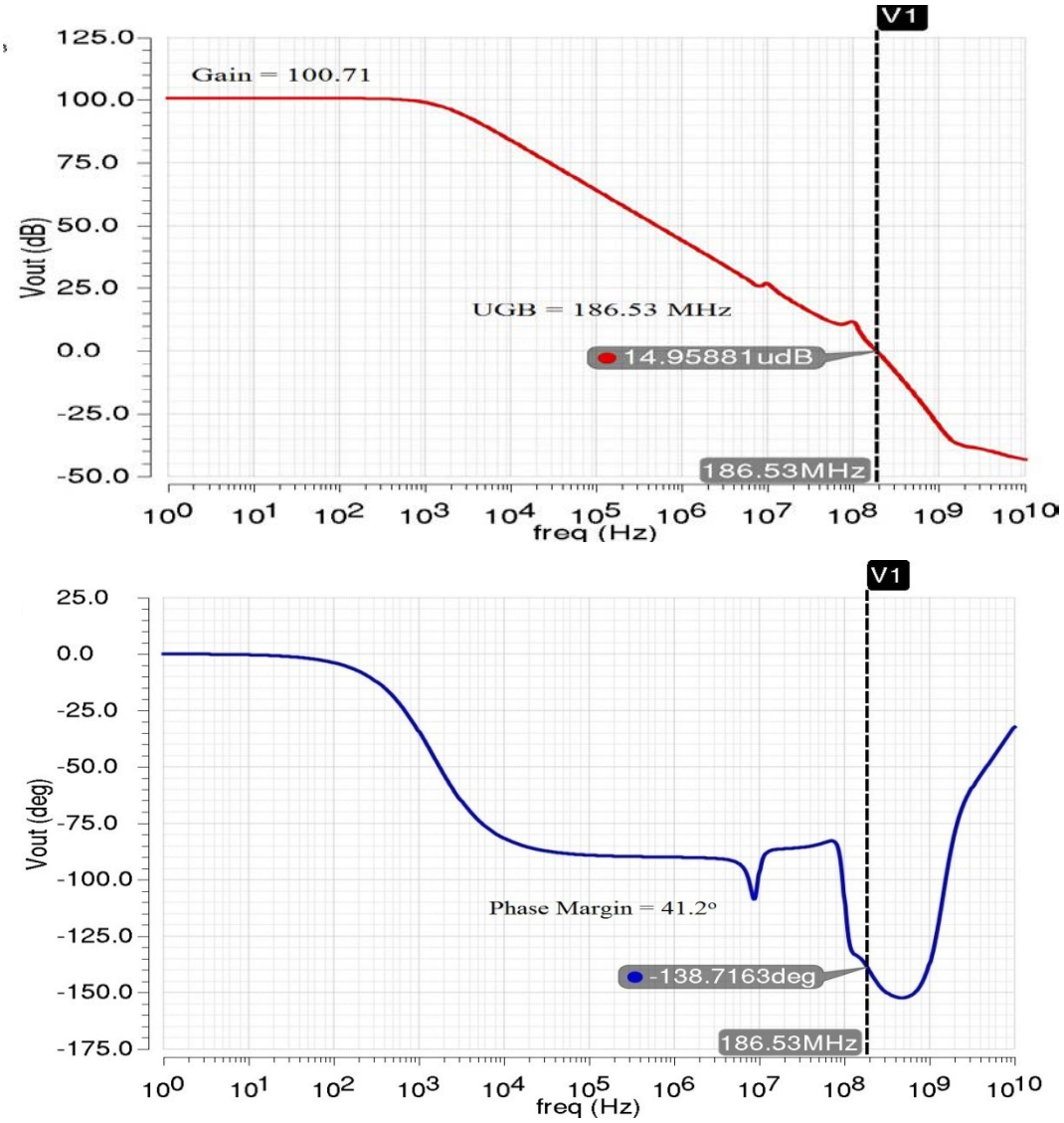


Figure 3.8 Frequency Response of Op-amp with Gain Boosting

3.3 Frequency Compensation

To remove the effect of unwanted poles and zeroes the miler compensation is applied by connecting the compensation capacitor, C_{C1}, between the nodes V_{on1} (i.e. output of first stage) and V_{op} (i.e. the output of second stage) in the circuit.

The working can be better understood by the small signal model illustrated in Figure 3.9 [14]. The addition of compensation capacitor (Cc) firstly increases the effective capacitance shunting R_1 and moves the dominant pole (p_1) towards the origin. Secondly it moves the second pole, (p_2) away from the origin because of decrease in the output

resistance. This technique increases the phase margin of the op-amp. Therefore making circuit stable as shown in the Figure 3.10.

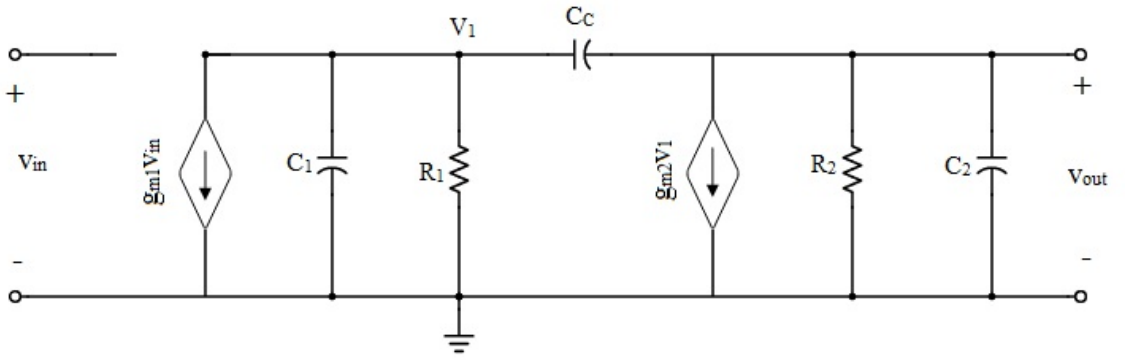


Figure 3.9 Miller compensation applied in two-stage op-amp [14]

The overall transfer function that results from the addition of Cc is given by:

$$\frac{V_o(s)}{V_{in}(s)} = \frac{g_{m1}g_{m2}R_1R_2\left(1-\frac{sC_c}{g_2}\right)}{1+s(R_1(C_1+C_c)+R_2(C_2+C_c)+g_{m2}R_1R_2\,C_c)+s^2R_1R_2\,(C_1C_2+C_cC_1+C_cC_2)} \tag{3.6}$$

Where R_1 and R_2 are the output resistances seen at the out of the first stage and the second stage respectively. Similarly C_1 and C_2 are the capacitances to the ground seen from the output of the first stage and the second stage respectively.

The location of compensated poles p_1 and $p_2$is given by:

$$p_1 = \frac{-1}{g_{m2}R_1R_2\,C_c} \tag{3.7}$$

$$p_2 = \frac{-g_{m2}C_c}{C_1C_2+C_cC_1+C_cC_2} \tag{3.8}$$

If C_2 is much greater than C_1 and C_c then equation (3.8) becomes:

$$p_2 = \frac{-g_{m2}}{C_2} \tag{3.9}$$

The right half plane zero is given by:

$$z_1 = \frac{g_{m2}}{C_c} \tag{3.10}$$

SIMULATION RESULTS

The phase plot in the Figure 3.10 shows an increase in the phase margin from 41.2^o to 66.7^o after applying the frequency compensation.

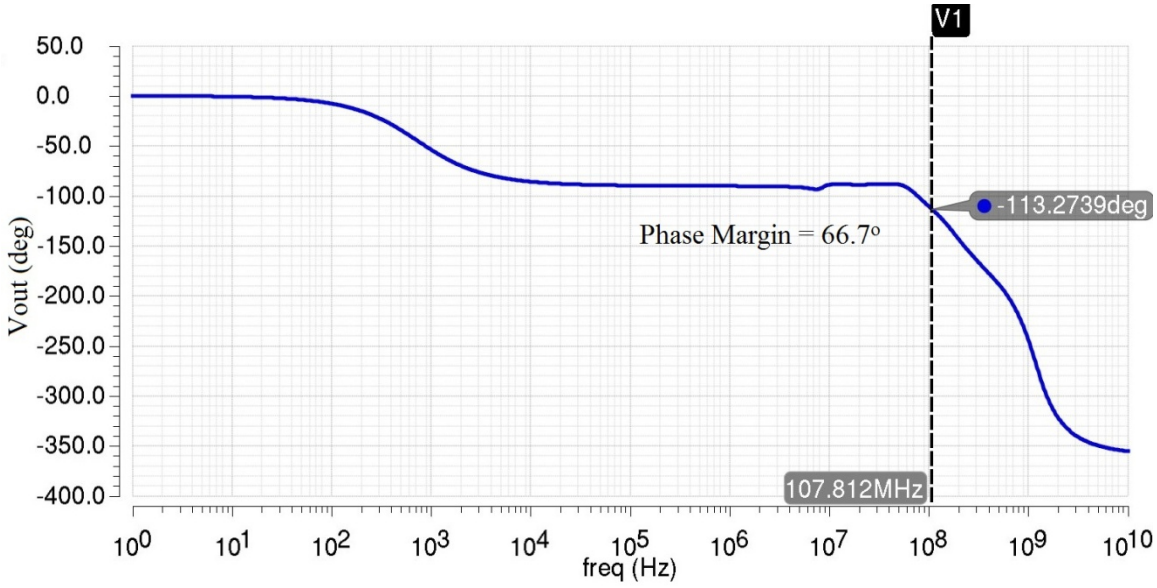


Figure 3.10 Frequency response of op-amp with frequency compensation

CHAPTER 4
DESIGN AND ANALYSIS OF THE PROPOSED AMPLIFIER

This chapter presents the design and analysis of proposed amplifier circuit. The op-amp is designed and simulated in the 0.18 µm CMOS technology. The tests are run on the circuit in order to find out the various parameters of the operational amplifier.

This chapter is divided into following sections

1. Proposed Circuit
2. Circuit Analysis
3. Schematic Simulations
4. Performance Comparison

4.1 Proposed Circuit

The proposed circuit is a two stage gain-boosted fully differential inverter based CMOS amplifier. The regulated cascode gain boosting and miller compensation are applied in this circuit as discussed in previous chapter. The circuit comprises of two self biased inverter stages, where gain boosting is applied to output stage inverter as shown in the Figure 4.1.

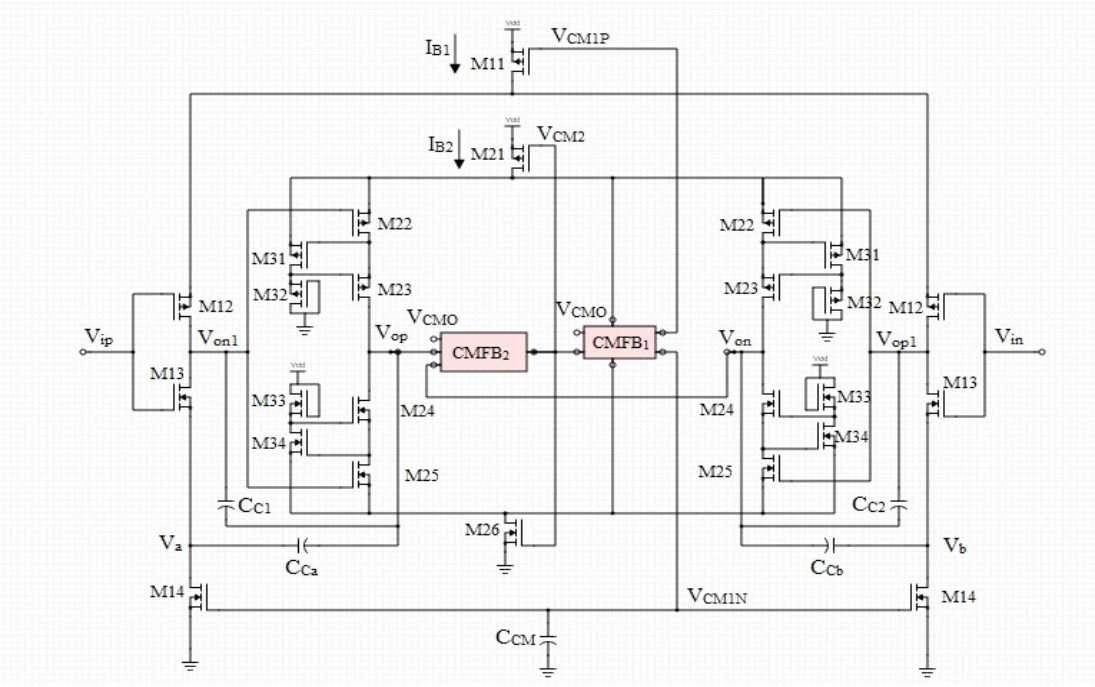


Figure 4.1 Proposed circuit of gain boosted two-stage inverter based op-amp

4.2 Circuit Analysis

In order to understand the working of proposed amplifier circuit, a small signal analysis needs to be done. The Figure 4.2 shows a small signal differential-mode half circuit of the circuit shown in the Figure 4.1. Considering the input stage first, R_{op1} and R_{on1} represents the output resistances seen at the output node of the input stage.

The gain A_{v1} of the first stage is given by:

$$A_{v1} = g_{m1} \times (R_{op1} \,||\, R_{on1}) \tag{4.1}$$

where,

$g_{m1} = g_{m12} + g_{m13}$, $R_{op1} = r_{o12}$ and $R_{on1} = r_{o13}$.

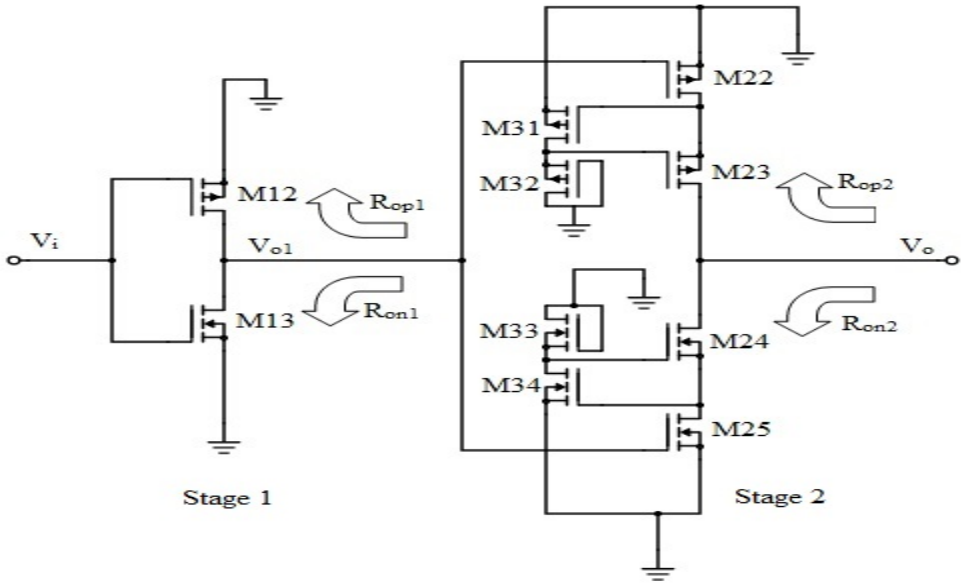


Figure 4.2 Small signal differential-mode half-circuit of the amplifier

Now, considering the output stage, the transistors M31-M32 represents a common source amplifier with diode connected pmos load having gain A_{vp}. The transistors M33-M34 represents a common source amplifier with diode connected nmos load having gain A_{vn}. The resistances R_{op2} and R_{on2} represents the output resistances seen at the output node of the output stage.

The gain A_{v2} of the second stage is given by:

$$A_{v2} = g_{m2} \times (R_{op2} \,||\, R_{on2}) \tag{4.2}$$

where, $g_{m2} = g_{m22} + g_{m25}$, $R_{op2} = A_{vp} g_{m23} r_{o23} r_{o22}$ and $R_{on2} = A_{vn} g_{m24} r_{o24} r_{o25}$.

Thus the overall gain is given by:

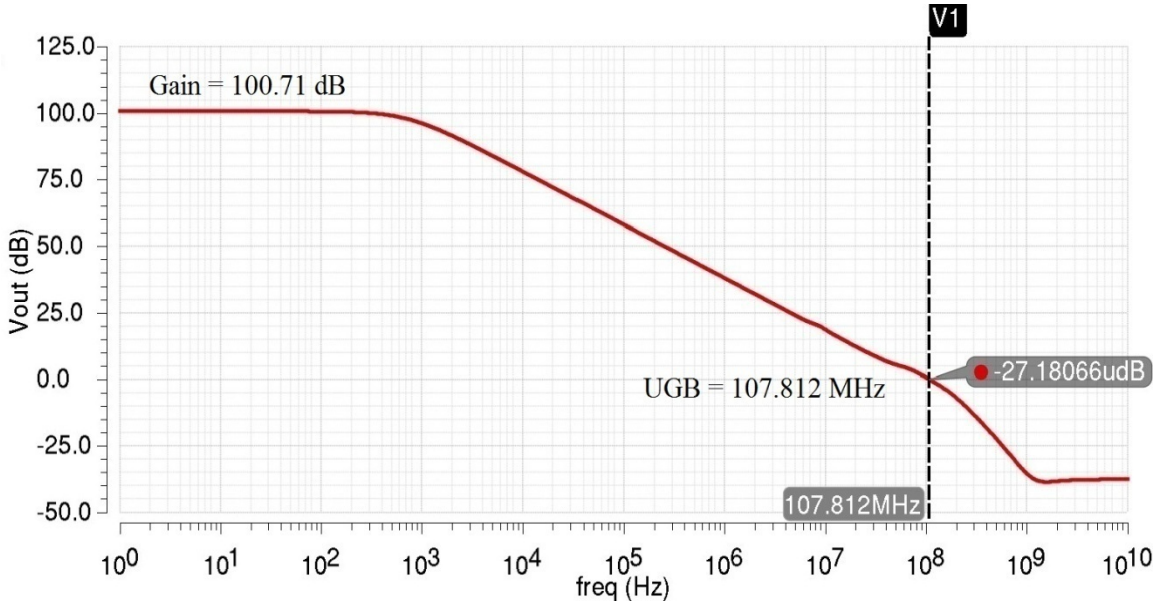
$$A_v = A_{v1} \times A_{v2} \tag{4.3}$$

$$A_v = (g_{m12} + g_{m13})(g_{m22} + g_{m25})(r_{o12} \,||\, r_{o13})(A_{vp} g_{m23} r_{o23} r_{o22} \,||\, A_{vn} g_{m24} r_{o24} r_{o25}) \tag{4.4}$$

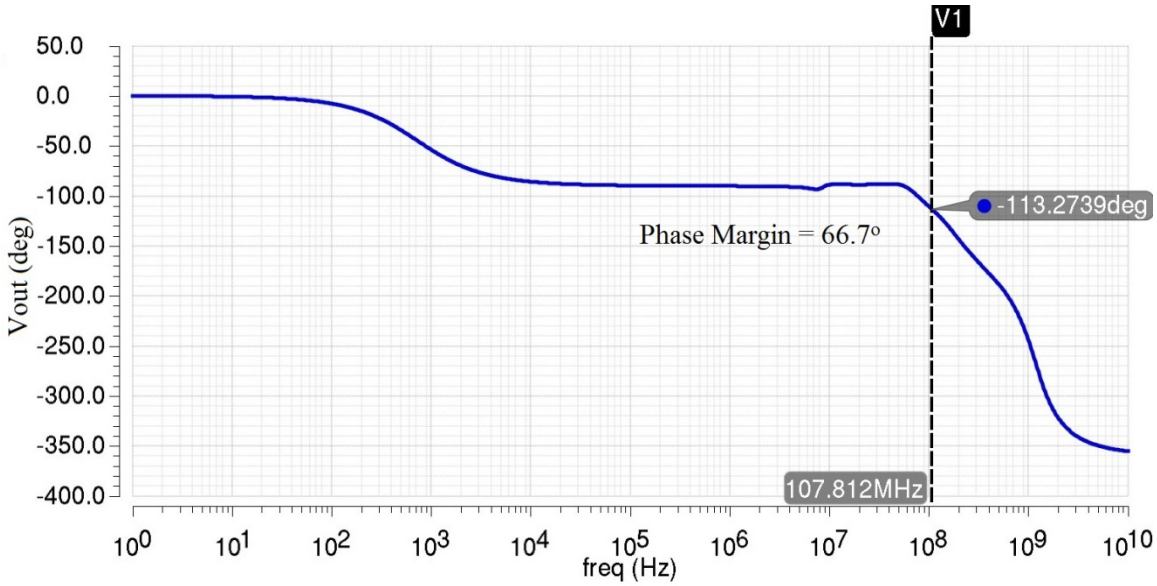
4.3 Schematic Simulations

4.3.1 AC Response

The bode plot and phase plot of the proposed op-amp in the Figure 4.3 shows a gain of 100.71 dB and unity gain bandwidth of 107.812 MHz with the phase margin of 66.7^o.



(a)

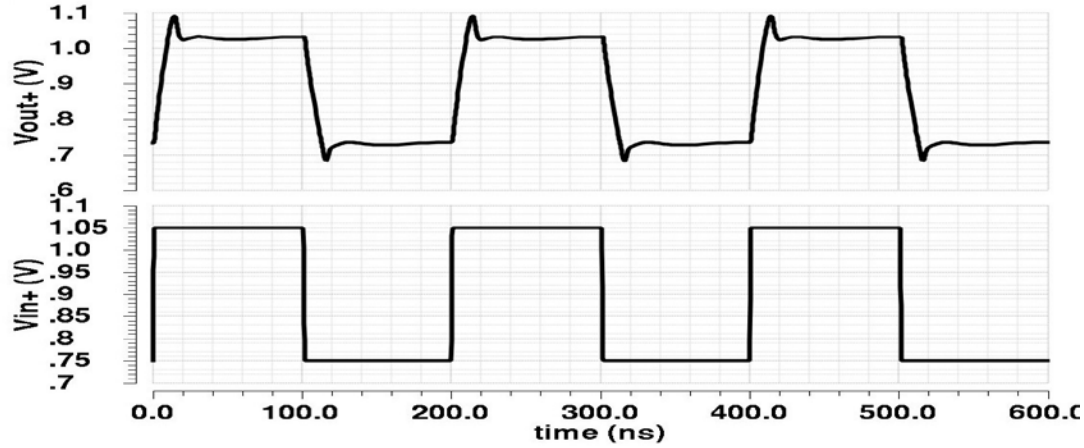


(b)

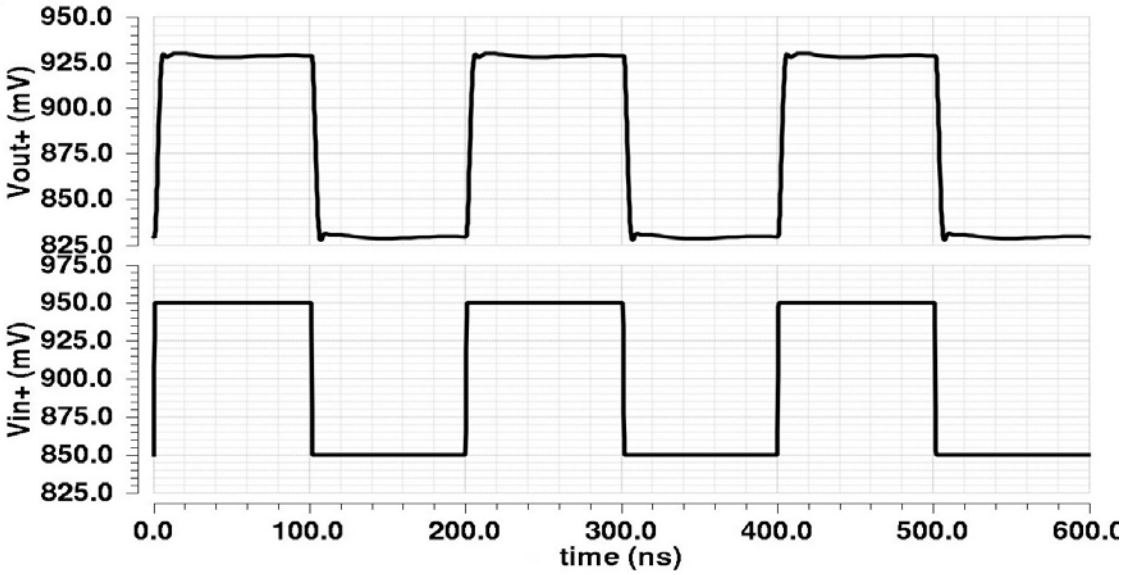
Figure 4.3 Frequency response of the proposed op-amp

4.3.2 Transient Step-Response

The transient response of the proposed op-amp is shown in the Figure 4.4. The Figure 4.4 (a) and (b) shows the step response when the large signal (0.6 Vp-p) and the small signal (0.1 Vp-p) are applied to the input respectively. The slew rate observed is 32.6 V/µs for the large signal and 26.57 V/µs for the small signal.



(a)



(b)

Figure 4.4 Step responses (a) Large signal (b) Small signal

4.3.3 Input Common-Mode Range

The Figure 4.5 shows the input common mode range equal to 1.03 Vp-p and output common mode range equal to 1 Vp-p.

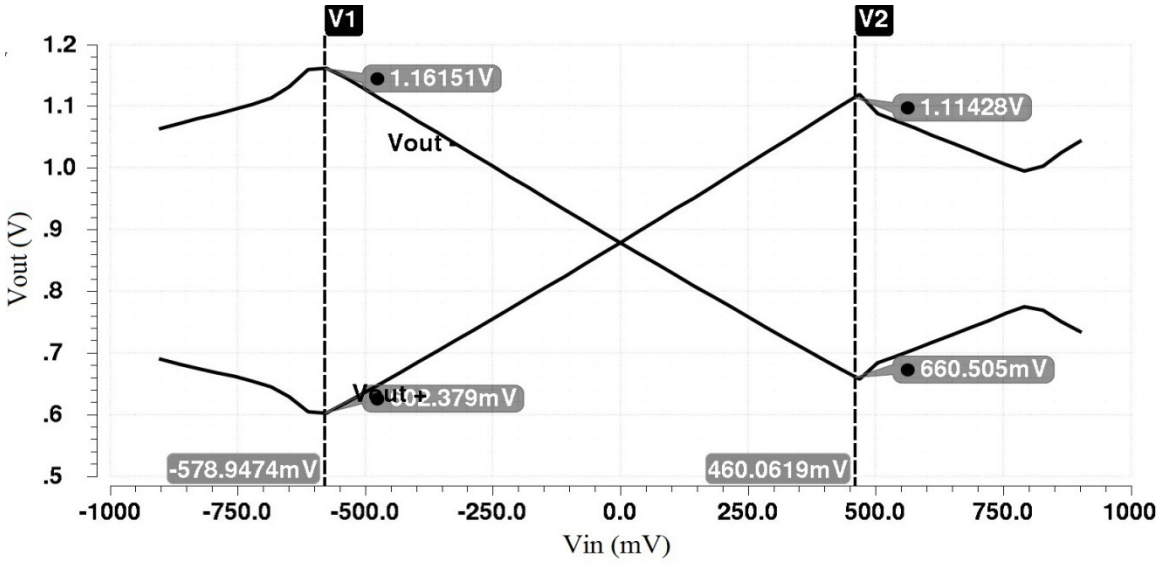


Figure 4.5 Input common mode range

4.4 Performance Comparison

Table 4.1 presents a summary of key measured parameters, as well as, a performance comparison with various single stage and multistage amplifiers available in literature.

Table 4.1 Comparison and Key Performance Summary of the Op-Amp

	[20]	[21]	[22]	[18]	**This Work**
Architecture	Conventional Fully Differential Two Stage	Recyclic Folded Cascode	Self-Cascode Structure	Self-Biased Inverter-Based	**Self-Biased Inverter-Based**
Tech (μm)	0.18	0.18	0.18	0.13	**0.18**
Power Supply (V)	1.8	1.8	1.8	1.2	**1.8**
Adc (dB)	74	60.9	96	71	**100.71**
UGB (MHz)	160	134.2	146	35	**107.8**
Power Dissipation (mW)	0.362	1.44	0.720	0.110	**0.286**
SR (V/μs)	26.7	94.1	N/A	19.5	**32.6**
Input Common Mode Range (Vp-p)	N/A	N/A	N/A	N/A	**1.03**
Output Common Mode Range (Vp-p)	N/A	N/A	N/A	N/A	**1**
PM (^{o})	N/A	70.6	70	47	**67**
C_L (pF)	1.75	5.6	15	5	**4**

CHAPTER 5
CONCLUSION AND FUTURE SCOPE

5.1 Conclusion

The research work in the thesis describes a low power two-stage gain-boosted fully differential CMOS amplifier for pipelined ADC. The regulated cascode gain-boosting technique employed in the circuit increases the gain of the amplifier. The amplifier uses self-biased inverter stages. Thus avoiding any need of biasing circuitry. Different circuit analyses are carried out using Cadence Virtuoso Analog Design Environment in 180 nm CMOS technology. These include small signal differential-mode half circuit analyses, frequency response, transient step response and slew rate. The results show that the proposed quasi class-A amplifier topology is highly efficient and its performance is comparable to class-AB amplifiers. When compared to the inverter-based self-biased op-amp without the gain boosting stage, the proposed circuit is observed to offer improved performance parameters such as the DC gain, slew rate, UGB and phase margin at a minimal power dissipation of 0.286 mW. The DC gain shows an improved value of 100.71 dB. UGB offered is 107.8 MHz. The improved PM of 67^{o} results from the compensation applied in the circuit. Therefore the circuit proposed is capable of offering low voltage, low power operation without compromising the other performance parameters. This makes it a viable and effective option to be used in pipelined ADC architecture.

5.2 Future scope

In this thesis work, a two-stage gain boosted fully differential inverter-based op-amp has been designed. Op-amp is a basic building block of a pipelined ADC. Its speed and accuracy decides the conversion rate and the power requirements of the ADC. As the proposed circuit is completely self-biased and does not require any external biasing, it dissipates much less power. Thus, in the future, the designed op-amp can be used in energy efficient pipelined analog to digital converters. Also, the proposed op-amp has a lower unity gain bandwidth (UGB) therefore another future target can be to increase its UGB in order to improve the performance of op-amp.

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