CROSS TALK ANALYSIS IN CARBON NANOTUBE BASED VLSI INTERCONNECTS

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Submitted by

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CANDIDATE'S DECLARATION

I hereby certify that the work which is being presented in the thesis entitled "CROSS-TALK ANALYSIS IN CARBON NANOTUBE BASED VLSI INTERCONNECTS" in partial fulfillment of the requirement for the award of the **Degree of Doctor of Philosophy** and submitted in the **Department of Electronics and Communication Engineering** of the Thapar University, Patiala is an authentic record of my own work carried out during a period from July 2010 to December 2013 under the supervision of late Professor Sankar Sarkar and professor Rajesh khanna.

The matter presented in this thesis has not been submitted by me for the award of any other degree of this or any other institute.

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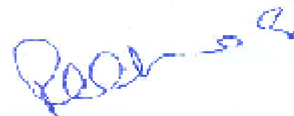

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ABSTRACT

With advanced technology nodes, large number of functionalities is integrated in a Very Large Scale Integration (VLSI) chip. Thus, the density of long interconnects is increased exponentially that connect millions of active devices on a chip, is posing a serious bottleneck in terms of substantial capacitive and inductive couplings. Hence there appears a dire need to search a potential material for future generation of VLSI interconnects that will be capable of exhibiting minimized propagation delay, power dissipation and crosstalk effects.

The present work explores the possibilities of alternative interconnect material for future VLSI interconnects. The most promising alternative for copper interconnects turns out to be Carbon Nanotube (CNT).A comparative analysis of the propagation delay, power dissipation, cross-talk induced noise voltage and its frequency spectrum in CMOS inverter driven global interconnects of SWCNT bundle and copper has been presented. The single interconnect as well as capacitively coupled interconnects are represented by the π-equivalent circuit of distributed *RLC*-model. The Driver-Interconnect-Load (DIL) model [15] of distributed *RLC* circuit is used for the mutually coupled interconnects. An Alpha power law model [129] is used for representing the transistor in the CMOS inverter (driver).

Influence of separation between adjacent tubes of various lengths and tube diameters, on delay and power dissipation in Single Walled Carbon Nanotube (SWCNT) bundle interconnect has been analyzed at 32nm and 22nm technology nodes. The main aim of this investigation is to optimize separation distance(x) between adjacent SWCNT and tube diameter (d) for better

performance. The output waveform is analytically determined using CMOS inverter driven π-equivalent RLC circuit of SWCNT bundle and copper interconnect. The results are compared with SPICE simulation results at same technology nodes. There appears good agreement between the analytical and simulation results obtained. SPICE simulation result reveals that, in terms of delay, SWCNT bundle interconnect performs better than copper interconnect if the separation between the tubes is less than a certain critical value. It has also been noted that a SWCNT bundle composed of tubes of 1nm diameter is of lower delay than copper interconnect at various interconnect lengths and higher power dissipation due to dominance of larger capacitance of SWCNT bundle.

Here an analytical model is developed to extract the transient response of victim output using CMOS inverter driven π-equivalent RLC circuit of capacitively coupled interconnects of SWCNT bundle. It is observed that at 32nm and 22nm technology nodes, for capacitively coupled interconnects, the piecewise analytical results replicate the SPICE waveforms very well.

Crosstalk induced, noise voltage waveform and its frequency spectrum in capacitively coupled and mutually coupled SWCNT bundle interconnects, at the far end of victim line, at 32nm and 22nm technology nodes respectively have been analyzed. The diameter dependent crosstalk induced noise voltage levels have also been evaluated for the same technology nodes. The waveform of victim output analytically determined and compared with SPICE simulation results. A similar analysis has been performed for copper interconnects and a comparison made between the results of these two analyses. The analytical and simulation results have shown good agreement, for both CNT and copper.

Based on these results it is found that, compared to copper, crosstalk noise voltage levels in capacitive coupled SWCNT bundles, at the far end of victim line, are significantly low. In

mutually coupled copper interconnects, width of the noise waveform is wider compared to CNT at the far end of victim line. These results have further revealed that, compared to copper interconnects, capacitively coupled interconnects of SWCNT bundle filter more noise frequency components at both 32nm and 22nm technology nodes. In addition, compared to copper, mutually coupled interconnects of SWCNT bundles suppress comparable noise components in the higher frequency range for the same technology nodes. Based on these comparative results, an improved model for extracting inter-bundle, real life, coupling capacitances between SWCNT bundles has been proposed in this present work.

An investigation of the control of crosstalk induced noise voltage (functional crosstalk noise) in capacitively coupled interconnects of SWCNT bundle, at the far-end of victim line, for fixed pitch and varying interconnect dimensions, for the proposed inter coupling capacitance model and the conventional model, at 22nm technology node, have been carried out. Results reveal that, in comparison to the latter, the former provides better reduction in crosstalk induced noise voltage. A similar analysis is performed for copper interconnects. Result reveals that, compared to SWCNT bundle interconnects, copper interconnects has higher coupled noise voltage levels.

Finally, an analysis of the effect of temperature, varying over a range from 300K to 500K, on the crosstalk induced noise voltage waveform and its frequency spectrum both in capacitively coupled interconnects of SWCNT bundle using an improved inter bundle coupling capacitive model and in the copper interconnects at the far end of victim line, at 22 nm technology node is carried out. Result shows that, as temperature rises from 300K to 500K, compared to copper interconnects, the crosstalk induced voltage levels at the far end of victim line in SWCNT bundle interconnect are significantly low. With rise in temperature, the coupled

SWCNT bundle interconnects suppresses more frequency components of the noise voltage than the conventional metal (copper) interconnects.

The result of present research emphasizes that the comparative study of crosstalk analysis in CNT and copper interconnects shall be particularly important for the deep submicron high density, high performance chips.

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LIST OF SYMBOLS

t_e	Even mode time of flight
t_o	Odd mode time of flight
L_s	Self inductance of the interconnect
C_g	Ground capacitance of the interconnect
C_C	Coupling capacitance between coupled interconnects
τ	Transition time
n	Carrier density
ω	Angular frequency
$\sigma(\omega)$	AC conductivity
σ_0	Frequency independent DC conductivity
K_f	Fermi wave vector
R_Q	Quantum contact resistance
R_S	Scattering resistance
L_K	Kinetic inductance
N_{CNT}	Number of CNT in a bundle
λ	Mean Free Path
C_Q	Quantum capacitance
d	Diameter of SWCNT
x	Center to center distance between SWCNT(Tube separation)

H	Thickness of rectangular interconnect
w	Width of rectangular interconnect
s	Space between two rectangular interconnects
y	Separation between interconnect to ground
ρ	Resistivity
S'	Center to center distance between rectangular interconnect
M	Mutual inductance
ε	Dielectric constant
μ_0	Permeability of vacuum
α	Velocity saturation index
V_{T0}	zero bias threshold voltage
K_s	Transconductance parameter of MOSFET (Saturation region)
K_l	Transconductance parameter of MOSFET (Linear region)
ζ	Temperature coefficient of resistance
$\lambda_{OP,300}$	Spontaneous optical emission length at 300 K
$\lambda (T)$	is the temperature-dependent Mean Free Path

LIST OF ABBREVIATION

DSM	Deep submicron
VLSI	Very large scale integration
IC	Integrated Circuit
ITRS	International technology roadmap for semiconductors
PTM	Predictive Technology Model
MTL	Multi-conductor Transmission Line
EM	Electromigration
CVD	Chemical vapor deposition
PE-CVD	Plasma enhanced chemical vapor deposition
HF-CVD	Hot-filament chemical vapor deposition
MOSFET	Metal oxide field effect transistor
CMOS	Complementary MOSFET
pMOS	P-channel MOSFET
nMOS	N-channel MOSFET
CNT	Carbon nanotube

SWCNT	Single walled carbon nanotube
MWCNT	Multi walled carbon nanotube
DWCNT	Double-walled carbon nanotube
s-CNT	Semiconducting CNT
m-CNT	Mixed CNT
GNR	Graphene nanoribbon

Chapter 1

INTRODUCTION AND STATEMENT OF THE PROBLEMS

1. INTRODUCTION

A VLSI interconnect is a thin film of conducting material that provides electrical connection between two or more nodes of the circuit/system formed in the silicon chip. Earlier the most commonly used material was aluminum. The choice was based on its good conductivity and adherence on silicon dioxide. Another useful property of aluminum is that it forms good ohmic contact with silicon. As device density increased with technology scaling, interconnect current density also increased. A disadvantage with aluminum is that at high current densities considerable electromigration takes place, causing increase in resistance of the wire. Later it was realized that copper a material of higher conductivity is several times more resistant to electro migration than aluminum. In comparison with aluminum, copper can withstand about five times more current density with equal reliability for IC-applications. Due to the advantages that it offers copper became the preferred interconnect material, especially for submicron and deep submicron high density, high performance chips.

As the aggressive technology scaling continues, a new problem is started. With decrease in cross-section copper interconnect resistivity increases due to surface roughness and grain boundary scattering, causing increase in propagation delay, power dissipation and electro-migration. To alleviate this problem, for interconnects of future generation chips alternative

solutions are under consideration. The most promising alternative for copper interconnects turns out to be Carbon Nanotube (CNT). CNT considered here is graphene sheet, rolled up to form cylinder, depending on its chirality, can be either metallic or semiconductor. CNT is also classified into single-walled and multi-walled nanotube. Two parallel SWCNTs (Single walled nanotubes) on ground plane are shown in Fig.1.

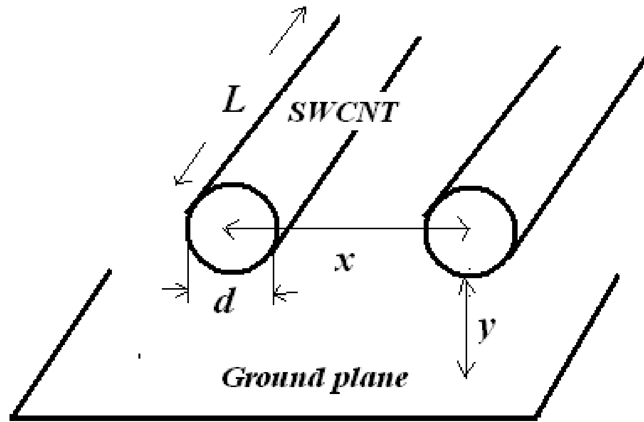


Figure 1.1 Two parallel SWCNT, of diameter '*d*', separation between tubes '*x'*, length 'L' distance from ground 'y.

This work includes a comparative analysis of the propagation delay, power dissipation, crosstalk induced noise waveform and its frequency spectrum in CMOS inverter driven global interconnects of SWCNT bundle and copper. An analytical timing model is developed to extract the transient response for the far end of victim line in capacitively coupled interconnects of SWCNT bundle. SPICE simulations have been used for verification of the validity of the analytical methods.

Several researchers have reported the crosstalk effect in coupled interconnects of CNT by representing the driving CMOS gate by a simple linear resistor [1]-[13]. However, some researchers have considered the CMOS gate instead of linear resistor [14]-[16].It is observed that

the replacement of the driver equivalent linear resistor by CMOS gate can improve both delay and crosstalk analysis.

A number of analyses have been reported in coupled CNT interconnects, assuming the value of coupling capacitance between bundles as equivalent to that of the coupling effect between metal interconnects (copper material based interconnects) of the same dimensions (e.g.[1]-[6],[59]). There is need for some more realistic estimation of coupling capacitance values. Hence, an improved model of inter bundle coupling capacitance [118], based on this idea, has been proposed in the present work. Here the effect of (a) tube diameter, (b) pitch and temperature variations on crosstalk induced noise voltages in capacitive coupled interconnects have also been investigated.

1.2 STATEMENT OF THE PROBLEMS

A detail literature survey carried out in the area of crosstalk analysis in coupled CNT interconnects for advanced technology nodes, clearly establishes that it is essential to study the crosstalk effect in CNT interconnects for future generation of VLSI design. To meet this end, the influence of the parasitics of metallic CNT as interconnect is to be considered. As this would require an analytical modeling and SPICE simulation, the problem is oriented to meet the following objectives:

- Effect of tube parameters on Carbon Nanotube (CNT) performance.
- Analysis of cross talk effect in Carbon Nanotube (CNT) interconnects.
- Analysis of pitch effect variation on coupled CNT-lines.
- Timing analysis with application of DIL (driver-interconnect-load) model to coupled CNT-lines.
- Technology dependence of crosstalk in CNT-interconnect to be analyzed.

- Comparison of the results obtained from the above analyses with results for copper (Cu) interconnects.
- Temperature dependent crosstalk analysis in CNT and copper interconnects.

1.3 ORGANIZATION OF THE THESIS

The main aim of the present research work provides a detailed investigation of the influence of tube parameters viz. tube separation(x), diameter (d) and length (L) on propagation delay and power dissipation, and comparative crosstalk analysis in coupled CNT and copper interconnects. The contributions and important developments are presented in this thesis in the following sequences.

- The present chapter 1 introduces the subject of the thesis topic. The objectives of the problems are identified.
- Chapter 2 reviews the past research works carried out on delay, power dissipation and crosstalk analysis in Carbon Nanotube (CNT) based VLSI interconnects and their control by tube parameters viz. tube separation (x), tube diameter (d) and length (L). Various aspects of crosstalk in coupled interconnects of CNT have been discussed. The role of interconnect parasitic on performances is examined.
- Chapter 3 presents the effect of tube parameters viz. tube separation (x), diameter (d) and length (L) on delay and power dissipation in single walled carbon nanotube (SWCNT) bundle interconnect. Output waveforms have been analytically determined using CMOS inverter driven π-model [16] of interconnect, for both SWCNT bundle and copper. The results are compared with SPICE simulation results at 32nm and 22nm technology nodes. There is good agreement between the analytical and simulation results obtained.

This chapter also presents a comparative study of interconnect performance in terms of delay and power dissipation between CNT and copper.

- Chapter 4 presents an analytical model of victim output in capacitive coupled interconnects using CMOS inverter driven π-equivalent *RLC* circuit. This model takes into consideration, the dependence of MOSFET behavior on input waveform. Crosstalk induced transient responses of victim output are extracted, for both SWCNT bundle and copper. The results are verified by SPICE simulations at 32nm and 22nm technology nodes. A diameter dependent crosstalk analysis at the same technology nodes has been analyzed and results discussed. This chapter also investigates, (i) a detailed comparative analysis of analytically extracted, capacitively and mutually coupled dependent transient responses and simulated transient responses, for both SWCNT bundle with an improved coupling capacitive model and copper interconnects and (ii) its frequency spectrum, at the far end of victim output.
- Chapter 5 compares, the control of crosstalk induced noise voltage (functional crosstalk noise) in capacitively coupled interconnects of SWCNT bundle using an improved inter bundle coupling capacitive model [118] and the conventional model with copper, at the far-end of victim line, for fixed pitch and varying interconnect dimensions under three different cases, at 22nm technology node. Furthermore, a comparative analysis of the effect of interconnect resistance, inductance and ground capacitance on coupled positive peaks at the far end of victim line in capacitively coupled interconnects of SWCNT bundle and copper has also been discussed.
- Chapter 6 analyzes, the effect of temperature, varying over a range from 300K to 500K, on the crosstalk induced noise voltage waveform and its frequency spectrum both in

capacitively coupled interconnects of SWCNT bundle using an improved inter bundle coupling capacitive model and in copper interconnects, at the far end of victim line, at 22 nm technology node.

- Finally, chapter 7 summarizes the work and draws conclusions on the basis of the results presented in the preceding chapters. Some suggestions for future works are also given in the thesis.

Chapter 2

CROSSTALK ANALYSIS – A REVIEW

2.1 INTRODUCTION

Crosstalk effect between coupled interconnects becomes increasingly valuable in a VLSI chip as technology advances to Giga Scale Integration (GSI) level. This is due to the fact that the interconnect density has grown and dimensions have shrunk, as the chip size increases in scaled Deep submicron (DSM) CMOS technologies. These wires do not scale in length with technology scaling and parasitic impedance parameters of these wires increase with the length of interconnects. The parasitic impedance parameters of interconnect and device depend on materials, geometry and technology. Hence, the long interconnects pose severe challenges viz. crosstalk , delay and power dissipation for high performance VLSI design.

As the aggressive technology scaling continues a new problem is surfacing. With decrease in cross-section copper interconnect, resistivity increases due to surface roughness and grain boundary scattering, causing increase in propagation delay, power dissipation and electromigration [17],[18].

On the other hand, as the integration density of interconnects increases, crosstalk effects will become a very challenging issue, directly affecting the reliability of circuit performance. Therefore, many researchers are now exploring new and high-performance interconnects in order to meet the critical requirements of future ICs. To alleviate this problem, for interconnects of future generation chips, alternative solutions are under consideration [17]-[30]. The most promising alternative for copper interconnects turns out to be Carbon Nanotube (CNT).

Crosstalk effect, propagation delay and power dissipation have become a core research problem in deep submicron technology. Therefore, a lot of work is being carried out to address these problems. The present chapter reviews in detail the various research aspects of the crosstalk analysis in mutually coupled interconnects of copper and SWCNT bundles in DSM technology nodes and other associated problems.

2.2 PROBLEMS WITH EXISTING INTERCONNECT MATERIALS

Along with a continuous reduction in the feature size of the interconnect, there has been a parallel increase in the die size. As technology scaling continues, the length of some of the chip interconnects keeps increasing. Interconnects are categorized as global, local and semi-global according to their length. While a global interconnect is very long and connected to several nodes across the chip, as for example, clock lines, ground lines etc., the local ones, of shorter lengths, connect nearby nodes while the semi-global ones, of intermediate lengths, connect intermediate nodes of blocks and their delay is mainly determined by their *RC* product..

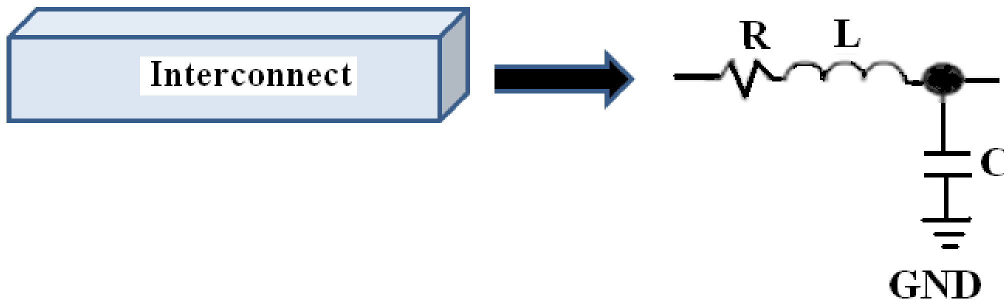


Figure 2.1 Lumped RLC-equivalent of interconnect.

A lumped *RLC* circuit is equivalent to an interconnect (Fig. 2.1). Any increase in the length of the interconnect causes *R*, *L* and *C* to increase. This in turn results in an increase in the interconnect signal propagation delay. Thus, with the scaling of technology, compared to the

delay caused by the gate, signal delay caused by the interconnect became increasingly more significant and thereby affects the circuit's reliability. As per ITRS predictions [31], for nanometer size gate lengths, the interconnect delay is mostly affected by resistive and capacitive parasitics. Since the early 1990s, in an effort to decrease the resistive part of the *RC* delay, various alternatives to aluminum have been considered.

Presently, amongst the various materials having well developed VLSI-interconnect technology, copper is the most preferred interconnect material. This is because of its far better electrical resistivity and electro migration than those of aluminum. Table 2.1 compares the resistivity and melting point of these two metals. With a melting point higher than that of aluminum, copper provides more thermal stability. The increase in resistivity of aluminum, will limit the performance of on chip interconnection in terms of delay. Therefore copper have been used as a suitable material in submicron technology nodes.

Table 2.1 Resistivities of aluminum and copper

Metal	**Bulk resistivity (μΩ.cm)**	**Melting point(K)**
Al	2.67	933
Cu	1.70	1,357

With the advancement of VLSI technology, the number of chip interconnects is on the rise. To accommodate the increasing number of interconnects the cross-sectional dimensions are reduced rapidly resulting in dimensions of the order of Mean Free Path (MFP) of electrons in copper (~ 40 nm at room temperature). As the dimension approaches that of the electron MFP grain boundary, the surface scattering is enhanced [32]-[35] and consequently interconnect resistivity is increased.

Another effect of dimension scaling is increase in current density. Thus, as technology scales, these effects on resistivity together with increase in interconnect resistance with length

enhances delay. Besides increase in delay, interconnect power dissipation increases because of the increased current density and increase in the frequency of operation. The increased heating, due to the rise in power dissipation, assists electro migration. These scaling dependent limitations of copper interconnect will become further severe for future generation VLSI chips. Hence it seems appropriate to look for an alternative material.

Considering the various advantages mentioned below, CNT appears to be a good alternative [36],[37]. The CNT possesses a resistivity much smaller than copper. This is due to the fact that, compared to the MFP of copper, which is only a few tens of a nanometer, the MFP of CNT is several micrometers long [36],[37],[118]. Moreover, a CNT wire is capable of carrying current densities of the order of 10^{14} A/m^2 or more, without carrying any damage at elevated temperature of 250^{0}C [62], has a thermal conductivity as high as 5800W/mK and high thermal and mechanical stability[38] ,[62] (Table2.2).

Table 2.2 Electrical and thermal properties
of SWCNT and copper [36]-[38],[62],[118]

Properties	**CNT**	**Cu**
Mean free path(nm) at room temperature	>1000	40
Max current density (A/cm^2)	>1x10^{10}	~1x10^6
Thermal conductivity(W/mK)	5800	385

2.3 CARBON NANOTUBE THEORY

To explain the electrical characteristics of CNTs, it is worthwhile to first explain the electrical behavior of graphene and its two dimensional analogue. Graphene sheet is a single planar sheet of sp^2 bonded carbon atoms arranged in a honeycomb pattern, as shown in Fig.2.2. Due to strong sp^2 bonding (like graphite), carbon nanotubes are much less susceptible to

electromigration (EM) problems that plague copper interconnects and can carry very high current densities [36].

A unit cell of graphene with its basis vectors is shown in Fig.2.3. This primitive unit cell contains two carbon atoms, each of which contributes one electron to the valence band. Therefore, there are two valence electrons per unit cell. So graphene has a filled valence band, thereby making it a semiconductor. However, because of symmetric effects, the valence and conduction bands meet at the edge of the Brillouin zone at the *K* point as shown in Fig.2.4, making graphene a zero band-gap semiconductor that behaves metallically [39].

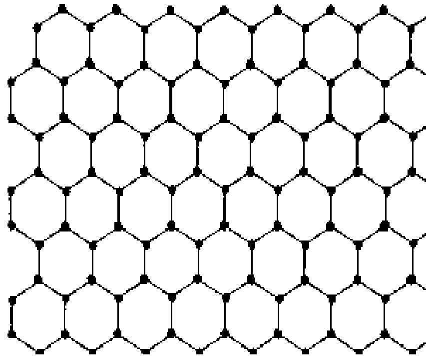


Figure 2.2 Graphene sheet .

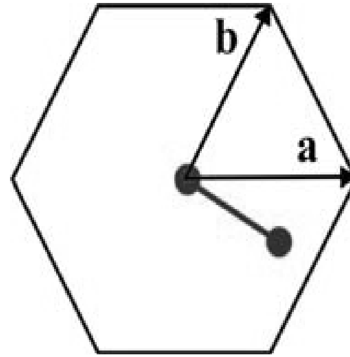


Figure 2.3 Graphene Unit Cell.

The CNTs considered here are graphene sheets, rolled up to form cylinders, each with a specific chirality, with diameters of the order of a few nanometers. CNTs are broadly classified in two categories, viz., Single walled carbon nanotubes (SWCNTs) and Multi-walled carbon nanotubes (MWCNTs). SWCNTs are those CNTs that are constituted by only one thin wall of graphene sheet. Those CNTs which consist of a multiple of concentric SWCNT like graphene tubes are termed MWCNTs.

A SWCNT is constructed from a section of a graphene sheet, as shown in Fig.2.5. In the figure, the shaded section represents that portion of the graphene sheet that can be rolled up to make the nanotube. The vector $\boldsymbol{C} = n\mathbf{a}+m\mathbf{b}$, called the chiral vector, forms the nanotube's

circumference. In this description, **a** and **b** are primitive vectors for the graphene sheet and *n* and *m* are integers [40]. When the nanotube is rolled up, the chiral vector will originate and terminate on the same carbon atom. Therefore, when the nanotube is formed, the cylinder will be completely seamless. The nanotube unit cell is enclosed in the box formed by the vectors **C** and **T.** Once the nanotube has been rolled up, it is essentially a 1-D crystal with a spacing **T** between unit cells. Theoretical calculations have demonstrated that electronic properties of CNTs are very sensitive to their geometric structure [42]-[44].

Further, although graphene is a zero-gap semiconductor, theory predicts that CNTs can be either metallic or semiconducting, with different energy gaps, depending very sensitively on the indices (*n,m*). For (*n,n*) or (*n,3j–n*), where *j* is an integer, the nanotube will be metallic. For all other (*n,m*), the nanotube will exhibit semiconducting characteristics.

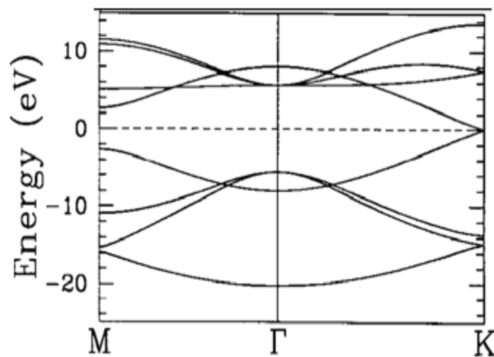


Figure2.4 Graphene band structure [41].

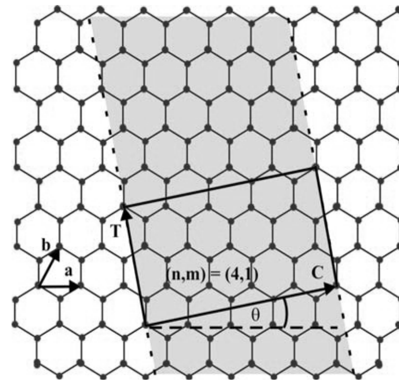


Figure 2.5 SWCNT from graphene sheet.

2.3.1 Fabrication Challenges in CNT

The process of growing on-chip CNT bundle for commercial purposes is very challenging [45]. Of the two types of CNTs viz. SWCNT and MWCNT, SWCNT has conductivity relatively much higher than that of MWCNT and hence is more preferable as

interconnect material. The difference in conductivity is because the MFP of SWCNT is much longer (about 1μm) compared to that of MWCNT (a few nm).

The process of CNT growth generally involves some catalyst particles (Fe, Ni, Co or their compound with Mo) that assist the growth process and control the tube diameter. To fill via with CNT, the catalyst particles are placed on the metal-1 at the bottom of via. CNT is then grown by chemical vapor deposition (CVD), at 450-800°C, in presence of a carbon containing gas [46]. So far, it has been easier to grow MWCNT.

Li et al. [37] proposed a bottom-up approach for growing MWCNT via on metal-1. The carbon fibers grow from the Ni catalysts deposited at predefined locations. By means of Plasma enhanced chemical vapor deposition (PE-CVD) and an applied bias voltage, the fibers are aligned perpendicular to the wafer surface. Finally SiO_2 is deposited and the wafer is planarized. The planarization process exposes the CNT ends for contact with the metal-2 layer. However, this method yields high interconnect resistance, of the order of a few hundred kilo ohms, possibly due to imperfections in the structure of the MWCNTs thus grown, cannot achieve high density growth and appears more suitable for growing single MWCNT fillings. A different approach for growing MWCNT is etching via down to metal 1 layer and growing the CNTs in these vias [46],[47]. In [47], dry etching stops at a film of the catalyst (Ni or Co). Arrays of MWCNTs are formed by hot-filament CVD (HF-CVD). The resistance achieved by this method is about 30% of that achieved by Li et al. [37]'s method. Instead of HF-CVD, Kreupl et al.[46] adopted a pure CVD approach and took care to ensure that via etching stops exactly on the catalyst layer so that highly reliable MWCNTs are grown with density varying between 100 and 10000/μm^2. This method produced tubes of resistance of nearly 10Ω.

Earlier, arc discharge and laser ablation methods were used for growing SWCNT [48],[49]. These processes involved evaporation of carbon from its solid form at temperatures as high as 3000^0C or more. Such a high temperature requirement is not desirable. Another limitation of these approaches is that the nanotubes formed were twisted around each other, making it difficult to purify and arrange the CNTs suitably for application purposes. More recently CVD with methane as carbon source and iron oxide nano particles as catalyst have been used to grow high quality SWCNT where the desired result is achieved in the temperature range 850-1000^0C.

2.3.2 SWCNT as VLSI Interconnect

Metallic SWCNTs, in their applicability as VLSI interconnects of the future [36],[37],[50], have aroused a lot of research interest. As has already been mentioned in Section 2.2, this is because, compared to copper interconnects, SWCNTs exhibit several desirable properties at highly scaled VLSI technology nodes [38],[51]-[53]. To investigate their potentiality as interconnect material, an equivalent circuit for CNT interconnects needs to be developed. For this, a one- dimensional fluid model for electron transport has generally been used [54], [55] ,[119].

However, the high resistance (greater than 6.45 KΩ) associated with an isolated SWCNT [56] necessitates the use of a bundle (rope) of CNTs conducting current in parallel to form an interconnection [36],[37]. Further, due to its lack of control on *chirality*, any bundle of SWCNTs consists of both metallic as well as semi-conducting nanotubes, in which the latter do not contribute to current conduction in the interconnect.

2.4 INTERCONNECT PERFORMANCE

The exponential growth of interconnect density, which connects millions of active devices on a chip, are posing a serious bottleneck in VLSI design. Thus there is a need to minimize delay, power dissipation and crosstalk if a high performance VLSI circuit is to be achieved. An overview of interconnect performance in terms of delay, power dissipation, crosstalk between CNT and conventional material (copper) based interconnects have been given in subsequent sub-sections.

2.4.1 Interconnect Performance in terms of Delay and Power Dissipation

Raychowdhury et al. [57], presented an efficient circuit compatible RLC model for metallic single walled carbon nanotubes (SWCNTs) and analyzed the impact of SWCNTs on the performance of ultra scaled digital VLSI design. It has been shown that CNT interconnects suffer from lack of vertical scalability but provide reliable interconnect solution for the future technology.

More importantly, interconnects dissipate more than 70% of the total power in a digital chip, a large portion of which corresponds to short local interconnects [58]. Lowering the capacitance of local interconnects, therefore, has a major impact on power-limited Giga Scale Integration (GSI) chips. For short lengths, performance of copper interconnects and nanotube interconnects with different configurations have been compared and presented [20]. It has been observed that mono- or bi-layer SWCNT interconnects above thick dielectric layers are promising candidates for short local interconnects because of their significantly smaller lateral capacitances compared to conventional copper wires even though they have larger resistances and time-of-flights. Mono-layer nanotube interconnects can have 50% smaller capacitance compared to copper wires, and can hence save significantly in terms of power as local

interconnects are the major source of power dissipation[20],[59]. Also, dynamic delay variation due to different switching patterns decreases significantly as the maximum variation in interconnect capacitance is 73% in contrast to 216% for copper interconnects.

Many researches[60]-[63] have been carried out to investigate the prospects of carbon nanotube performance in terms of power dissipation and reliability for future VLSI applications. Srivastava and Banerjee [60] addressed the critical issue of scaling limits of local interconnects, contact plugs and local vias made of metal. In this work, they analyzed the impact of small dimensions (and high resistance) of metallic local interconnects, contacts and vias on circuit performance and reliability. It has been shown that the current carrying capacity of copper vias/contacts fails to meet ITRS current density requirements beyond the 45 nm technology node.

A comprehensive evaluation of carbon nanotube bundle interconnects from all aspects critical to VLSI circuits - performance, power dissipation and thermal management and reliability perspectives have been presented in [61]. As shown in this work, CNT bundle vias can greatly reduce interconnect temperature rise and thus, when integrated with copper (Cu) interconnects, tremendously improve Cu interconnect performance (about 30%) and lifetime (by at least two orders of magnitude) due to lower temperatures. It has also been found that CNT bundles can significantly improve the performance of long global interconnects by as much as 80% with minimal additional power dissipation (for maximum metallic CNT density).

Banerjee and Srivastava [62] examined the applicability of CNTs in future VLSI interconnect applications. They compared the performance of CNT interconnect to scaled copper interconnects, in terms of power dissipation and thermal reliability aspects at different technology nodes viz. 22nm, 32,nm and 45nm. Also highlighted is the concept of *hybrid CNT/Cu*

interconnects employing CNT vias in tandem with copper interconnects. While the outstanding intrinsic properties of metallic single-walled CNTs in conjunction with encouraging performance, power and thermal/reliability analysis results of CNT bundles provide strong impetus for further investments in CNT interconnect research. Several challenges remain to be overcome in the areas of fabrication and process integration.

In the work [63], an exhaustive comparison in terms of representative performance, energy and density metrics has been carried out among the different options for global interconnects viz. carbon-nanotube (CNT) interconnects, wafer-level package (WLP) interconnects, 3D interconnects, RF microwave interconnects and optical interconnects. Outcome reveals that 3D interconnects offer an attractive option to reduce the energy dissipation and propagation delay of long on-chip wires (51% and 54% reduction in latency and energy dissipation respectively at 45nm node).

This analysis also shows that optical interconnects offer reduced latency compared to scaled Cu/Low-k technologies but they do not offer significant improvement compared to other technologies like WLP interconnects. It also follows from the analysis that CNT interconnects compare favorably to scaled Cu/Low-k interconnects in terms of latency with a 42% reduction in delay. Bamal et al.[64] analyzed and compared the performance of Interconnect Technology and Architecture Options for Deep Submicron Technology Nodes.

Koo et al. [65] and Cho et al. [66], analyzed and compared the performance of both CNT and optical options with copper(Cu)/low-κ wires of all three categories viz. local, intermediate and global, for future high-performance integrated circuits. They presented these comparisons in terms of both commonly used metrics, such as latency, energy per bit (power dissipation) and bandwidth density.

Koo et al. [65] reported that for a local wire, a CNT bundle exhibits a smaller latency than Cu for a given geometry. In addition, by leveraging the superior electromigration properties of CNT and optimizing its geometry, the latency advantage can be further amplified. For semiglobal and global wires with advance technology nodes, optical wires have the lowest latency and the highest possible bandwidth density using wavelength division multiplexing, whereas a CNT bundle has a lower latency than copper.

The work in [66], reported that for long wires (~10 mm) both carbon nanotubes and optical interconnects outperform future Cu wires with optical interconnects having lower energy per bit and latency. For short wires (~1 mm), carbon-nanotube wires outperform both Cu and optical interconnects. The power density comparison is highly switching activity (SA) dependent. Because of a fundamental difference in the nature of power dissipation (static for optics versus dynamic for CNT/Cu) and "where" this power is dissipated (end devices for optics versus medium itself for Cu/CNT), optical interconnects are more power efficient for higher SA circuits and longer lengths. However, for lower SA at low bandwidth per linear cross section length (φ_{BW}), CNT and Cu exhibit lower power density. These observation show that CNT and optical interconnects are the promising option in advanced technology nodes.

In [67] Li et al., discussed various carbon nanomaterials, along with their prospects for next-generation interconnects and passive devices. They also provide a comparative analysis of these nanomaterials vis-à-vis optical and RF interconnects, and illustrate why carbon nanomaterials constitute the ideal interconnect technology choice for next-generation ICs.

An equivalent transmission line model for CNT has been reported [68]-[71].The work in [68], proposed an equivalent transmission line model of CNT interconnect. The performance of CNT interconnects is examined based on modified model and compared with conventional

copper counterpart, at different interconnect levels. It was observed that the propagation delay of CNT interconnect is still larger than Cu interconnect at local interconnect level. However, at intermediate and global level, CNT interconnects have advantages of having even non-zero metal-nanotube contact resistances. These advantages are enlarged as the technology advanced. They also find that the pitches of bundle have significant impact on the performance of CNT interconnect. In order to achieve the best performance of CNT interconnect, the pitches of bundle should be reduced as much as possible.

A new model was presented to describe the propagation of electric signals along carbon nanotube (CNT) bundles, in the framework of the classical transmission line theory [69]. A possible implementation of a future scaled microstrip based on CNT bundle is analyzed and compared to a conventional microstrip. In this work, the equivalent transmission line (TL) is derived from a fluid-model description of the nanotube, so that all the parameters are associated in a clear and meaningful way to the physics of the considered system. Taking into account the predicted behavior of copper at nanometric scale, a performance comparison between SWCNT and Cu interconnects has been performed, in terms of study of latency.

The obtained results suggest that SWCNT interconnects at intermediate level show better or equivalent performances with respect to copper. The performances at local level may be equivalent to copper only if the fabrication process ends with a high percentage of metallic SWCNTs in the bundle and good quality terminal contacts are realized. In any case, the reduction in power dissipation and the increase of current density allowed may suggest using SWCNTs bundles even for the local level case.

First time, a new method for stability analysis of carbon nanotube (CNT) interconnects based on transmission line (TL) modeling and using the Nyquist stability criterion has been

addressed [70]. The obtained results show that with increasing the length of the CNT bundle and the diameter of each individual CNT interconnect, the relative stability increases and the system becomes more stable. A new sixth-order linear parametric expression for the transfer function of transmission line (TL) based interconnects has been presented to analyze the time-domain response of carbon nanotube (CNT) interconnects [71].This transmission line based model takes the effects of both contact and fundamental (quantum) resistances on the step response, especially the propagation delay has been studied. The obtained results show that for the length of a CNT bundle equal to 50 mm with the diameter equals to 1 nm of each individual CNT, the propagation delay changes from 0.138 to 5.58 ns for the contact resistance values ranging from 1 to 50 kΩ, i.e. a variation range of 39.43 times the minimum value. The related delay variations for the length values 200 mm, 500 mm and 1000 mm, are 31.37, 22.61 and 15.42 times the minimum value, respectively.

The propagation of electric signals has been modeled using the fluid model along SWCNT interconnects, both in the case of isolated and bundled CNTs [72]. Some preliminary results have been presented in [73]. Here, the fluid model is enhanced to account correctly for the influence of the CNT radius on its electrical behavior. The work in [74], presented the modeling of diameter dependent nanotube bundle resistance for on-chip interconnect applications. The obtained results indicate that neglecting the diameter-dependent nature of ohmic and contact resistances can produce errors as high as 120%. Using the resistance model, it is shown that SWCNT bundles can provide up to one order of magnitude reduction in resistance when compared with traditional copper interconnects depending on bundle geometry and individual nanotube diameter. Furthermore, for local interconnect applications, an optimum nanotube diameter exists to minimize the resistance of the carbon nanotube

Nieuwoudt et al.[75] evaluated the performance and reliability of nanotube bundles for future VLSI applications. The results indicate that SWCNT interconnect bundles can provide significant improvement in delay over that in traditional copper interconnect. It is also demonstrated that the magnetic inductance will have a significantly larger impact on SWCNT bundle performance than kinetic inductance for predicted SWCNT bundle geometries.

Several researchers [76]-[79], compared the performance of Multi walled carbon nanotube(MWCNT) with SWCNT and copper interconnects at deep submicron technology nodes. Naeemi et al.[76] demonstrated that a hybrid system of copper/SWNT/MWNT offers the highest performance enhancement for interconnects. The results of this paper indicate that copper wires, SWCNTs, and MWCNTs have distinct advantages and disadvantages, and a hybrid system made out of Cu/SWNT/MWNT interconnects would be the optimal multilevel interconnect network. At the global levels, it was observed that SWCNT-bundles can outperform copper wires in terms of resistance and delay only if they are densely packed, the fraction of metallic nanotubes is larger than 40%.Outcomes of this work also indicate that large diameter MWNTs are promising for global signal interconnects since they can offer substantial reduction in resistance.

Li et al. [77] presented a compact equivalent circuit model of MWCNT based interconnect and the performance of such interconnects is evaluated and compared against traditional Cu interconnects, as well as Single-Walled CNT (SWCNT)-based interconnects, at different interconnect levels (local, intermediate, and global) for future technology nodes. This work presented, a detailed investigation of MWCNT-based interconnect performance. It has been seen that at the intermediate and global levels, MWCNT interconnects can achieve smaller signal delay than that of Cu interconnects, and the improvements become more significant with

technology scaling and increasing wire lengths. At 1000-μm global or 500-μm intermediate level interconnects, the delay of MWCNT interconnects can reach as low as 15% of Cu interconnect delay. It was also shown that in order for SWCNT bundles to outperform MWCNT interconnects, dense and high metallic-fraction SWCNT bundles are necessary. On the other hand, since MWCNTs are easier to fabricate with less concern about the chirality and density control, they can be attractive for immediate use as horizontal wires in VLSI, including local, intermediate, and global level interconnects.

The current status of research on CNT and GNR interconnects, both from fabrication and modeling perspectives has been reviewed in [78]. From modeling perspective, SWCNT, DWCNT, and MWCNT interconnects can provide better delay performance than that of Cu, particularly for long global wires. However, on the fabrication front, most of the reported progress has been focused on MWCNT-based vertical interconnects (vias). Electrothermal analysis of CNT vias has shown that although CNT vias are both electrically and thermally ballistic, smaller diameter densely packed SWCNTs with good contacts are needed to have better thermal and reliability performance compared to that of the Cu vias. Moreover, taller CNT vias will have better advantages than shorter CNT vias as compared to their metal (Cu or W) counterparts. However, a thermal conductivity model for long-length CNT is still lacking. Outcomes show that single-walled, double-walled and multiwalled CNTs can provide better performance than that of Cu. However, in order to make GNR interconnects comparable with Cu or CNT interconnects, both intercalation doping and high edge-specularity must be achieved. Thermal analysis of CNTs shows significant advantages in tall vias, indicating their promising application as through silicon vias in 3-D ICs. However, it has been shown that in order for GNR interconnects to be comparable with CNT and Cu interconnects, intercalation-doped multilayer

GNRs with high edge-specularity are needed. High-frequency analysis of CNT interconnects reveals that due to the presence of large kinetic inductance, the skin effect is reduced in a CNT bundle.

This unique characteristic of CNT bundle is very important and promising for future high frequency circuit applications. CNT-based on-chip inductors could offer more than three times quality factor enhancement over Cu-based inductors without using any magnetic material or design optimization. Close et al. [79], experimentally investigated the local interconnect wires made of single MWCNTs with 30-nm diameter, geometrically suitable for the 22-nm node and beyond. Sub second delay of theses wires has been experimentally extracted and compared with an existing MWCNT interconnect model, as well as with the expected performances of scaled copper wires.

A review work has been carried out in [80] to explore optical fiber and carbon nanotube (CNT) as prospective alternatives to copper in VLSI interconnections. Although, the theoretical aspects proves CNTs and optical interconnects to be better alternative against copper on the ground of performance parameters such as power dissipation, switching delay and crosstalk. But copper would last for coming decades on integration basis.

An existing work in the literature proposed using an "equivalent dc conductivity" to calculate the inductance of CNT bundles [81]. In this method, a realistic CNT bundle consisting of discrete conductors is replaced by a single solid conductor of identical dimension with an equivalent dc conductivity. Subsequently, the inductance of the CNT bundle is extracted by employing a widely used field solver, Fast Henry [82], on that single "equivalent dc conductivity" solid conductor. However, such an approach has several fundamental issues that need to be justified.

First, the treatment of discrete conductors as a single solid conductor is not valid for all cases. While the behavior of a very large number of discrete solid conductors may approach that of a single solid conductor, a significant difference could be induced by this treatment for small number of discrete conductors, as has been shown in [83]. Second, the realistic CNTs hollow cylindrical structure cannot be captured by the approach in [81]. Most importantly, the "equivalent dc conductivity" method in [81] does not take into account the large kinetic inductance of CNTs when calculating the magnetic inductance. Without considering kinetic inductance, the impedance of CNT bundles cannot be correctly extracted in the high-frequency regime. This indicates that the inductance extraction method outlined in [81] is flawed.

Since understanding the high-frequency effects in CNT interconnects is critical to further explore their applicability in high-frequency circuit design, a correct frequency-dependent impedance extraction method for CNT interconnects is highly desirable. From an application perspective, CNT-based inductors have been proposed in several works [84], [85], although these structures cannot be easily fabricated as part of the VLSI back-end process. In [86], an SWCNT-based on-chip inductor has been analyzed based on a modified inductance extraction procedure presented in [81]. However, since the employed inductance extraction method is flawed as discussed earlier, the inductor analysis in [86] would lead to dubious quantitative results and conclusions.

Banerjee et al. [87], not only developed a frequency-dependent impedance extraction method but also present a rigorous investigation of high-frequency effects in CNT bundle structures. The analysis in this paper has illustrated for the first time that because of the presence of large kinetic inductance (due to large momentum relaxation time) in each CNT, the skin effect in CNT bundles is significantly reduced compared to that in conventional conductors.

Particularly, MWCNTs could offer significant advantages in high-frequency applications, since they exhibit much reduced skin effect in comparison to SWCNTs and are also known to offer comparable circuit performance with that of SWCNTs due to low dc resistivity. This preferable high-frequency property of CNTs is then explored in the design and analysis of high-performance on-chip inductors. This analysis quells existing misunderstandings and provides insights that could potentially open up new vistas in RF/mixed-signal and off-chip applications for CNT interconnects.

The works in [88]-[90] analyzed process variations in CNT based interconnect. Despite the fact that high performance integrated circuits have a great variance in temperature (300–450 K), only a few prior studies have investigated the effect of temperature variations on the electrical transport of CNTs [91]-[95]. These temperature variations have a significant effect on the delay of the signal propagating along CNT-based interconnects, and hence, will affect the performance of the CNT-based integrated circuits.

Hosseini and shabro [95], presented an accurate thermally-aware model for single-walled carbon-nanotube (SWCNT) based interconnects. They verified the accuracy of electro-thermal model against recently reported experimental measurements. It has been observed that the thermally aware model of SWCNT-based interconnects offer more than 5 times reduction in delay at dimensions of about 10–20 nm for 27– 127 ^{0}C temperature range.

The voltage dependency was modeled to examine the electrical equivalent circuit of CNT based interconnects [74],[96],[97]. The work in [98] analyzed the electrical properties of SWCNT bundle with respect to three important circuit operating conditions: process, temperature, and voltage (PTV) for 32 nm technology node. The equivalent circuit model for CNT based interconnect has been developed. It is found that CNT based interconnect performs

better for long interconnects as compared to Cu wire. The performance varies by more than 50% with process variation where as with voltage and temperature the delay variations are ~3% and ~13−23% from the nominal voltage and room temperature, respectively.

The transmission line (TL) based propagation equations of a large-diameter MWCNT has been formulated in the frequency domain [99]. Recently, the circuit model of an MWCNT has been presented on the basis of qualitative considerations and used to compare the performance of MWCNT and scaled copper interconnects [77]. Sarto et al. [100] presented the rigorous analytical derivation of the multi conductor TL model of an MWCNT, in any configuration, including the effects of all mutual inductances and capacitances among the shells. It has also been proposed a new equivalent single conductor (ESC) model of an MWCNT excited in common mode configuration, which is very accurate up to several tens of gigahertz and at any distance from the ground plane.

Sathyakam et al.[101] presented for the first time an accurate modelling hierarchy for mixed CNT bundle interconnects. In this work, SWCNTs and MWCNTs have been modelled as equivalent single conductor transmission lines and then combined to form a mixed CNT bundle interconnect, which is basically a multiple equivalent single conductor model. The delays from transient analysis for both models for a unit bundle have been compared with the corresponding ones for SWCNT bundles and MWCNTs that exist in the literature. It is found that mixed CNT bundle interconnects are superior to both SWCNT bundle and MWCNT interconnects in terms of delay.

Alam et al.[102], investigated the prospects of mixed bundle of Carbon Nanotubes (CNT) as low-power high-speed interconnects for future VLSI applications. The power dissipation and delay of CNT bundle interconnects are examined and compared with that of the Cu interconnects

at the 32-nm technology node. The power dissipation analysis of interconnects has been performed for the first time and it is observed that for intermediate and global interconnects, mixed bundle of CNTs consumes smaller power than its copper counterpart. This paper also analyzed the effect of CMOS and CNFET driver where it is clear from the results that CNFET driver drives interconnects more efficiently. It is concluded that mixed bundle of CNTs can replace copper interconnects in future low-power high-speed VLSI systems.

In the recent, a hierarchical modeling approach has been proposed for mixed carbon nanotube (CNT) bundle (MCB) interconnects [103]. Based on the arrangements of single-walled CNTs (SWCNT) and multi-walled CNTs (MWCNTs), three different MCB structures were proposed. It was observed that the delay and power dissipation are significantly improved for the proposed MCB structures as compared to bundled SWCNT and bundled MWCNT at different global interconnect lengths.

2.4.2 Crosstalk between coupled interconnects

With the continuous increase in signal switching speed and higher density of interconnects, these parallel running long interconnects interfere with each other and have substantial capacitive and inductive couplings. Such coupling between adjacent interconnects signal propagating down one (aggressor) affects signal propagating down the other (victim). This is commonly referred to as crosstalk. Capacitive-coupling noise has positive polarity while inductive coupling noise has negative polarity. Crosstalk affects the signal integrity and degrades the performance of the circuit. A mutually coupled interconnects is shown

in Fig.2.6.These coupling effects are dependent on the length of interconnects, distance between them, input transition time and waveform.

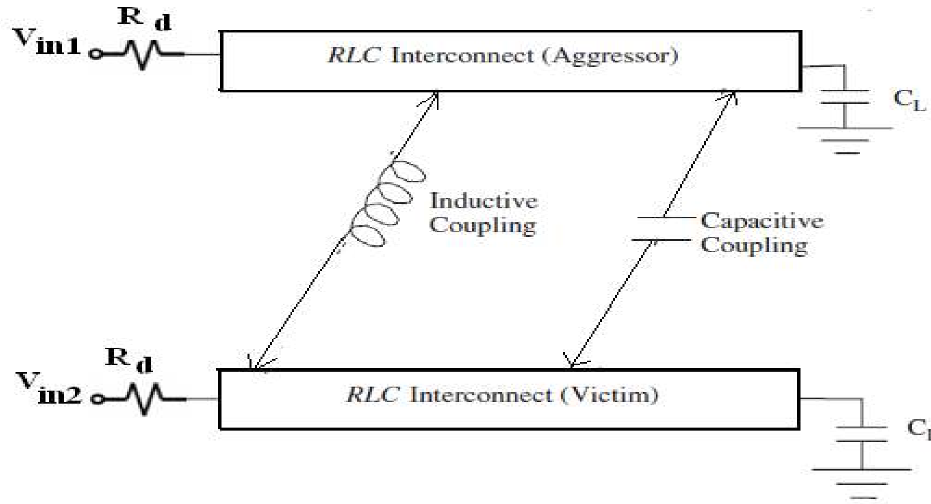


Figure 2.6 Mutually coupled interconnects. R_d and C_L are the driver resistance and load capacitance.

2.4.3 Control of Physical Parameters on Crosstalk Noise Voltage

One way to manage coupling noise is by controlling line parasitic viz. Resistance (*R*), inductance (*L*) and capacitance (*C*), which in turn can be controlled by wire sizing and spacing as well as shield line insertion.

2.4.4 Effect of Line Width on Resistance (*R*), Ground Capacitance (C_g) and Self Inductance (L_S)

For physical design tool, line width is an important parameter during wire optimization because it has a significant effect on both line resistance and ground capacitance. Line resistance increases with decrease in line width in coupled structure of interconnects (see Fig.2.1), the crosstalk noise voltage peak reduces. This is due to the fact that, with resistance, the voltage steps traveling along the line undergo attenuation and dispersion. Hence, the voltage steps arriving at the far end of the line are smaller and have larger rise times.

Ground capacitance increases with decrease in line width, which causes capacitive coupled crosstalk noise voltage peak to reduce. This is due to the fact that the difference between even and odd mode times of flight reduces. Even mode and odd mode time of flight are given in eqns. (2.1) and (2.2).

$$t_e(even) = \mathrm{L}\sqrt{L_s C_g} \quad (2.1),$$

$$t_o(odd) = \mathrm{L}\sqrt{L_s(C_g + 2C_C} \quad (2.2),$$

where L is the length, L_s is the self inductance, C_g is the ground capacitance of interconnect and C_C is the coupling capacitance between coupled interconnects.

For inductive coupling, the difference between even-mode time of flight and odd mode time of flight increases with rise in ground capacitance. Hence, contrary to capacitive coupling, inductive-coupling noise voltage peak increases with line width. So increasing line width is traditionally considered as a useful noise avoidance technique.

Unlike capacitance, inductance is only a weak function of line geometry and is primarily controlled by location of current return paths. Self inductance can be controlled by varying shield insertion and power-grid design during physical-design optimization. As self inductance increases, crosstalk noise voltage peak due to capacitive coupling increases significantly. This is due to the fact that the difference between even and odd mode time of flight increases. However, in inductive coupling, noise peak increases slightly due to reduction in difference between even and odd mode time of flight.

2.4.5 Effect of Spacing on Crosstalk Induced Noise Voltage

Spacing between two coupled interconnects is an important factor that influence the crosstalk noise voltage. As spacing increases, crosstalk noise voltage, due to both capacitive and inductive coupling reduces. This reduction in inductive noise voltage is not as significant as that

in the capacitive nose. This is due to the fact that with spacing, the coupling capacitance reduces more rapidly as compared to mutual inductance.

There are several effects of crosstalk. For example, false switching occurs when the magnitude of overshoot or undershoot is beyond the threshold voltage of a gate. The peak overshoot and undershoot generated at a noise-site can wear out a thin gate oxide layer resulting in permanent failure of the chip. In modern interconnect design, to reduce crosstalk the interconnects in adjacent metal layers are laid orthogonal to each other. But with growing interconnect density and reduced chip size, even the non-adjacent interconnects exhibit considerable coupling effects. This problem will be more and more significant as the feature size of transistor reduces with advancement of technology.

Therefore, it is important to investigate the effects of coupling in advanced technology nodes. In this section an overview on crosstalk analysis in coupled carbon nanotube(CNT) based interconnects has been reviewed. Crosstalk in copper and aluminum interconnects are extensively studied [104]-[112],[115]. However, very little work has been done in the area of crosstalk in CNT interconnect.

Previously, many researchers [104]–[112], have modeled crosstalk noise in copper based distributed capacitively and inductively coupled RLC-interconnect line by representing the driving CMOS gate by a simple resistor. Agarwal et al. [104], analytically showed that a signal traveling in a coupled line system is equivalent to the superposition of two distinct modes of propagation. These modes have different propagation constants and characteristic impedances for the interconnect lines. For one of the modes (even mode) both lines switch in the same direction, while for the other (odd mode) the lines switch in opposite directions. Like other authors, Agarwal et al. [104], assumed the driver impedance to be a linear resistance.

In estimating the crosstalk effect when an equivalent linear resistor is used to model the non-linear CMOS transistors, it leads to discrepancy in results. This can be understood by noting that a transistor in a CMOS gate operates partially in the linear region and partially in the saturation region during switching. It is only in the linear region that a transistor can be accurately approximated by a resistor, where as in the saturation region, the transistor is more accurately modeled as a current source with a parallel high resistance.

Kausik and Sarkar [14],[15], analyzed that the linearization of the transistor results in an erroneous estimation of crosstalk noise and their time of occurrence. They have developed a composite model combined with a transmission line-based coupled RLC model of interconnect to analytical purpose. Comparison of the analytical results with SPICE extracted results showed that the average error involved in estimating noise peak and their time of occurrence was less than 7%. It has also been seen that the proposed model is useful for accurate noise estimation in the presence of inductive effects, and would be extremely effective in guiding noise aware physical design optimizations.

In the current scenario, with growing importance of inductive effects, optimal repeaters are inserted effectively in *RLC*-model of long interconnects. Uniform repeater insertion is an effective technique for driving long interconnects. This technique divides the interconnect into equal sections and employs equal size repeaters to drive each sections [113],[114].Conventionally, The primary objective of uniform repeater insertion is to minimize the Power Delay Product(PDP) in long interconnect.

In recently a new criterion, the Power Delay Crosstalk Product(PDCP), was introduced by Kaushik et al.[115], as an efficient condition to insert repeaters into long coupled interconnect. It was observed that instead of PDP criterion, PDCP criterion is best suited for the

determination of optimum number of repeaters for overall minimization of delay, power and crosstalk.

Rossi et al. [1] was the first to study crosstalk in CNT interconnect. They analyzed crosstalk in CNT interconnect implemented bus architectures. Both SWCNT and MWCNT interconnects were considered. It was shown that delay and voltage noise margins in MWCNT busses were much better than SWCNT busses. The crosstalk delay is also lower in the SWCNT busses. In these busses cross delay can be improved by optimizing the spacing between the interacting interconnects. Furthermore, crosstalk induced logic error in the output device can be considerably large in case of MWCNT where as no such problem occurs in SWCNT architecture. Rossi et al. also proposed a crosstalk aware CNT bus architecture. This architecture is formed by double walled carbon nanotubes (DWCNT) in parallel. It is shown to be significantly less susceptible to cross talk produced delay and noise voltage peaks.

First time in [91], Jia et al. studied the Performance and reliability of coupled CNT interconnects in terms of temperature variations over a range from 300K – 600K and indicates that the performance and reliability degrades with an increase in CNT interconnect temperature. They proposed two modified temperature-dependent equivalent circuit models for single- and double-walled carbon nanotube (SWCNT & DWCNT) interconnects at first and the temperature effect on crosstalk in SWCNT and DWCNT interconnects were investigated.

The crosstalk-induced delay and noise of these novel interconnects are characterized numerically over a temperature range from 300 to 600K. The results obtained through simulation showed that the crosstalk-induced delay increases significantly and the noise increases slightly with rise in temperature.

The sensitivity analysis of the crosstalk effects was performed in SWCNT bundles using multi-conductor transmission line (MTL) model and equivalent single conductor (ESC)[2]. The results obtained by applying the MTL model and the simplified ESC approach are in good agreement. In any case, it should be noted that the ESC approach gives a worst case prediction of the crosstalk. Therefore, it is suitable for EMC design purposes of next generation nano interconnect.

Pu et al. [3] developed and analyzed crosstalk effects in SWCNT and DWCNT interconnects. Their analysis included coupling inductance along with coupling capacitance. The analytical crosstalk models thus developed capture crosstalk delay, glitches etc. with good accuracy. Crosstalk induced delay in SWCNT and DWCNT bundle interconnects were compared with that of copper interconnect. It is observed that for semi-global and global interconnects CNT especially DWCNT results in much reduced crosstalk induced signal delay. For suppression of crosstalk induced glitch copper interconnect is better.

In the work [4], impact of process variations on the crosstalk coupling of CNT-based buses was presented. Besides, unlike traditional SPICE-based estimation, Sun and Luo proposed a closed-form model to solve this problem. It was shown that the experimental results were able to save the long computation time of SPICE-based tools and this approach yields little loss in accuracy. Also, it provides a compound result which provides more information, promising it to be much closer to the truth in real manufacturing process.

The crosstalk induced voltage peaks produce stress in oxide layers underlying the victim interconnect. With technology scaling oxide thickness has drastically reduced. As a consequence of oxide thinning a small crosstalk produced overshoot or undershoot causes a prohibitively large electric field to generate across the oxide. With time such electric field weakens the oxide layer

and possibility of its damage increases. The possibilities of oxide damage due to crosstalk overshoot and undershoot was studied by Das and Rahaman [5], [6]. They observed that with scaling ratio of overshoot/undershoot voltages to power supply voltage does not vary with scaling in all types of interconnects. However, in case of copper interconnects overshoot and undershoot increases as interconnect length is increased. In case of CNT based interconnects on the other hand, neither scaling nor increase in length affect crosstalk induced voltage overshoot and undershoot.

In [7], Hassanet et al. presented a method to use the negative capacitance technique to minimize crosstalk effects in carbon nanotube based interconnect, which has a potential future on-chip communication medium. Obtained results demonstrated that with careful synthesis and arrangement of CNT bundles, the capacitive coupling can be suppressed significantly. They mainly focused to prove the concept and the analysis was obtained through mathematical and qualitative perspective.

A new compact coupled *RC* model for the coupled MWCNT bundles was proposed by Sheikhassadi et al. [7] and studied the crosstalk analysis between coupled MWCNT bundle interconnects. The models developed for two coupled MWCNTs and for bundles of MWCNTs were employed for simulations of the global interconnects at 14 nm technology. Results obtained through simulation were in good agreement with the rigorous distributed model considered as the reference, with an average error being less than 1% and 2.5% for the two MWCNTs and MWCNT bundles.

The equivalent circuit has been developed to perform the crosstalk analysis by Zhang et al.[9] and the main influencing factors were discussed. Results obtained by simulation, showed that the crosstalk voltage can be decreased by increasing spacing between adjacent lines, setting

the appropriate position when the length is fixed, decreasing line length and selecting the appropriate frequency.

As integration density of interconnects increases at every technology node, increased delay and crosstalk effects may become a more challenging design problem particularly for subthreshold interconnects. Nanometer subthreshold global interconnect faces subthreshold driver design challenges and problems due to increased interconnect capacitance. Pable et al.[10] examined and compared the effect of crosstalk on delay for mixed wall carbon nano tube and Cu interconnects. This work reports new aspect ratio for global interconnect to reduce the effect of crosstalk on interconnect performance under subthreshold conditions. This paper has successively reported that interconnect geometry parameters provided by ITRS for super threshold circuits will not give the optimum performance for subthreshold region. There is need to redesign the same to reduce the delay as well as crosstalk effects.

In the work [11], Lu et al. presented an efficient method based on the equivalent single conductor (ESC) model and delay extraction technique to investigate the crosstalk effects of complex multi-walled carbon nanotube (MWCNT) interconnects. Each MWCNT interconnect is first characterized by the ESC model. A decoupling algorithm is then utilized to transform the coupled interconnects into a set of individual lines. After that, based on a modified Lie formula, a delay algebraic equation was derived to obtain the time domain response of each single interconnect. The validity and efficiency of the proposed method were demonstrated by the numerical example and compared with the original multi-conductor circuit (MCC) model. It was found that a good agreement was observed between ESC model and MCC model.

In the work [12], the crosstalk analysis among MWCNTs in a complex bundle was performed in the frequency domain in the range up to 100 GHz. Numerical simulations were

performed by using both the multi-conductor transmission line (MTL) method and reduced-order equivalent models based on the equivalent single conductor (ESC) approach in order to reduce the complexity of the system. Each MWCNT of the bundle was first modeled as an ESC; Next, the parallel connected ESCs of the bundle were further represented by only one equivalent conductor. The accuracy of the proposed approximation was assessed and discussed.

It was observed that the values of the total input and output currents of the bundle and the crosstalk currents induced in the victim were in good agreement with the data obtained by the full MTL theory in the frequency range 100 MHz - 100 GHz .

Crosstalk effects in MWCNT interconnect for future ICs were investigated [13] by virtue of the equivalent single conductor model and the finite-difference time-domain solution of transmission line equations. The worst case time delay and the peak crosstalk voltage on victim wire of multi-wire MWCNT interconnect configurations were derived and compared to those of the copper (Cu) wire counterparts for the intermediate and global interconnects at the 22- and 14-nm technology nodes. The obtained results were illustrated that the crosstalk-induced time delays in the MWCNT interconnects were found to be much smaller than those in the Cu interconnects, in particular, for longer wires. Nevertheless, the MWCNT interconnects exhibited little improvement on the crosstalk-induced noises in comparison with their copper counterparts.

In the recent work [116],[117], addressed the crosstalk-related issues (signal integrity) in CNT interconnect lines. In the work [116], different analytical models of SWCNT, double-(DWCNT), and MWCNT were studied to analyze the crosstalk delay at global interconnect lengths. A capacitively coupled three-line bus architecture employing CMOS driver was used for accurate estimation of crosstalk delay. Each line in bus architecture was represented with the equivalent RLC models of single and bundled SWCNT, DWCNT, and MWCNT interconnects.

Crosstalk delay was observed at middle line (victim) when it switches in opposite direction with respect to the other two lines (aggressors). Using the data predicted by ITRS 2012, a comparative analysis on the basis of crosstalk delay was performed for bundled SWCNT/DWCNT and single MWCNT interconnects. It was observed that the overall crosstalk delay improved by 40.92% and 21.37% for single MWCNT in comparison to bundled SWCNT and bundled DWCNT interconnects, respectively.

Sathyakam et al. [117] presented a new method to reduce crosstalk of carbon nanotube (CNT)-based VLSI interconnects. For this, proper integration of semiconducting CNTs (s-CNTs) and a new contact geometry, where metallic CNTs are in the core and s-CNTs are in the periphery of the CNT bundle, was proposed. The coupling capacitance between adjacent interconnects was modeled and compared with and without s-CNTs in the CNT bundle periphery. Result through SPICE analysis and EM simulations showed that the coupling capacitance can be reduced by 82.5% and the resulting delay by 8.41%. They suggested that the crosstalk effect between neighboring wires can be reduced by using s-CNTs in the design.

2.5 CONCLUSION

From the literature it is clear that, Single-walled carbon nanotubes (SWCNT) have been proposed as a possible replacement for copper (Cu) interconnect due to their large conductivity and current carrying capabilities in deep submicron (DSM) technology nodes. Some researchers have considered another possibilities for interconnects in DSM technology nodes viz. MWCNT, mixed CNT bundle, Graphene Nanoribbon(GNR) and optical interconnects to analyze the performance of interconnect in terms of delay, power dissipation and crosstalk analysis. In addition, some work has been carried out to investigate the prospects of mixed bundle of Carbon Nanotubes (CNT) as low-power high-speed interconnects for future VLSI applications.

It is also seen from the literature that very little work has been published in crosstalk point of view in coupled CNT bundles. However, reported work in literature related with crosstalk are mostly based on the effect of length, power supply variations, input switching activity and oxide thickness in coupled SWCNT, MWCNT and mixed CNT bundles.

Despite the fact that high performance integrated circuits have a great variance in temperature, only a few prior studies have investigated the effect of temperature variations on the electrical transport of CNTs. These temperature variations have a significant effect on the delay of the signal propagating along CNT-based interconnects as well as crosstalk induced noise voltage between coupled interconnects, and hence, will affect the performance of the CNT-based integrated circuits.

However, variations in signal frequency of input and variations of tube parameter on crosstalk induced noise voltage have not been carried out fully in coupled SWCNT bundle interconnects for DSM technology nodes. Analytical study of crosstalk in coupled SWCNT bundles with accurate coupling capacitance and mutual capacitance expressions is still a topic of

research. Most investigators of SWCNT bundle interconnects assume the value of coupling capacitance and mutual inductance as equivalent to that of the coupling effect between metal interconnects of the same dimensions. However, since material properties of copper vary widely from those of CNTs, perhaps there is need for some more realistic estimation of coupling capacitance as well as mutual inductance values.

In addition, no account of temperature dependent frequency spectrum analysis of crosstalk induced noise voltage in coupled SWCNT bundle interconnects has been reported. Hence, there is need for an analytical study on this subject.

From the literature review it can be concluded that the study of temperature variations and tube parameter variations with accurate coupling capacitance and inductance model on crosstalk induced noise voltage in coupled SWCNT bundle interconnects, can be particularly useful for the future VLSI interconnect design.

Chapter 3

INFLUENCE OF TUBE PARAMETERS ON SWCNT BUNDLE INTERCONNECT PERFORMANCE

3.1 INTRODUCTION

Good VLSI-interconnect designing demands minimization of line delay and power dissipation. Delay and power dissipation are influenced by resistance, inductance and capacitance of the interconnect. These impedance parameters depend on the Single Walled Carbon Nanotube (SWCNT) parameters viz. tube separation, diameter and length. So it is important to investigate the effects of these SWCNT parameters on delay and power dissipation. This chapter deals with a study of the dependence of SWCNT bundle interconnect delay and power dissipation on the separation between adjacent tubes of the bundle for the various interconnect lengths and SWCNT diameters. Separation implies the distance between the centers of adjacent CNT cross- sections of two immediately neighboring tubes [118].

Several researchers have, on the basis of circuit simulation, reported that a SWCNT-bundle interconnect provides low-resistivity advantage over copper when the bundle length is semi-global or global [63],[118],[119]. These authors primarily focused on the influence of length and widths on bundle interconnect performance. They opined that the observed influences are due to the control of bundle length and width on equivalent circuit impedance parameters.

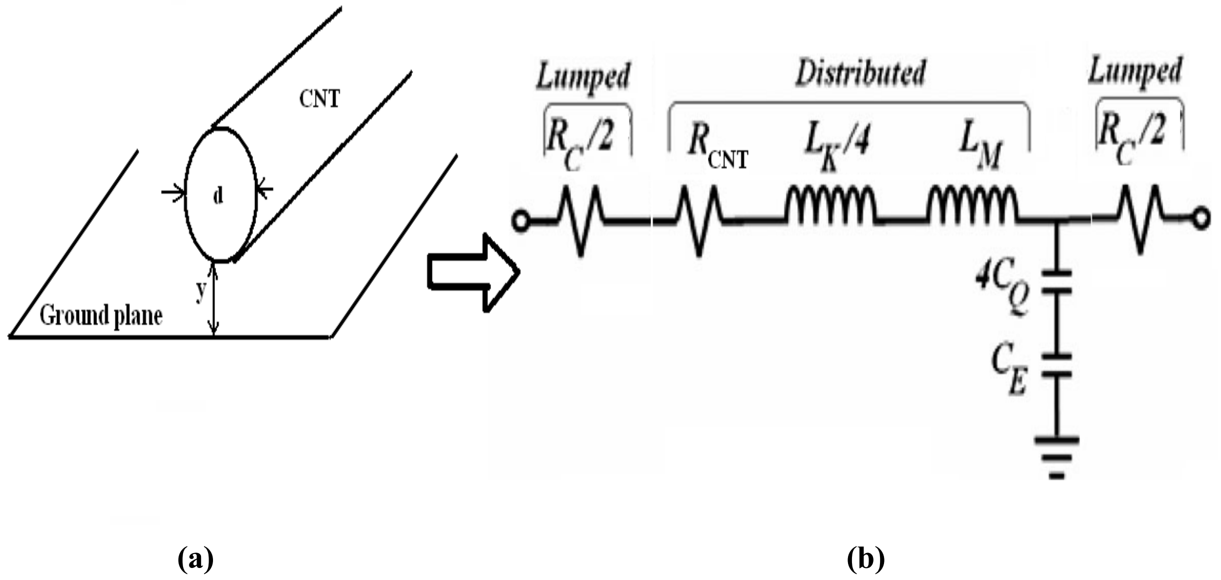
Massoud et al. [120] showed that the impedance parameters of the equivalent circuit also depend on CNT diameter in the bundle. An account of how delay and power dissipation in a SWCNT-bundle interconnect is controlled by the constituent tube diameter has been reported in [121]. Nieuwoudt et al.[122] developed a diameter-dependent *RLC* SWCNT model and predicted that optimized nanotube bundles can provide a significant delay reduction over copper wires and non-optimized MWCNT and SWCNT bundles for intermediate and global interconnect application.

Here, in this study, an alpha power law model has been used for representing transistors of CMOS-driver and output waveform and propagation delay analytically determined and compared with SPICE simulation results. There is good agreement between the analytical and simulation results obtained. The SPICE simulation results reveal that delay increases with an increase in the separation between adjacent tubes for the entire range of length values and tube diameters whereas the reverse is true for power dissipation. Finally these results have been compared with those of currently used copper interconnects at 32 nm and 22nm technology node respectively.

3.2 Equivalent Circuit and Impedance Parameters of SWCNT Interconnect.

To analyze and understand the behavior of any interconnect (CNT or else) it is essential to first develop its equivalent circuit (Fig.3.1). The development of an equivalent circuit is complete only when the various impedance parameters like resistance, capacitance and inductance are fully defined by means of analytical expressions. Such an equivalent circuit can then be used in the analysis and simulation of interconnect performance. An isolated SWCNT on

ground plane is shown in Fig.3.1a. The separation between the nanotube and the ground is 'y' and the diameter of the SWCNT is '*d*'. Assuming cylindrical coordinates, on the basis of Luttinger Liquid Theory, Burke [91] developed an electrical equivalent of the structure as shown in Fig. 3.1b.The resistances, inductances and capacitances of a bundle can be obtained from expressions available in the Literature [87],[118],[121].



(a) **(b)**

Figure 3.1 (a) SWCNT, of diameter '*d*', distance 'y' below it.**(b)** Electrical equivalent circuit of SWCNT.

According to Drude model, an AC electric conductivity [123] is given by

$$\sigma(\omega) = \left(\frac{ne^2\tau}{m^*}\right)\frac{1}{1+j\omega\tau} \quad (3.1)$$

where τ is the momentum relaxation time, n is the carrier density, ω is the angular frequency and m^* is the effective mass. For the DC case ($\omega = 0$), the conductivity expression reduces to

$$\sigma_0 = \left(\frac{ne^2\tau}{m^*}\right) \quad (3.2)$$

Eq.(3.1) can now be re-written as

$$\sigma(\omega) = \frac{\sigma_0}{1+j\omega\tau} \quad (3.3),$$

and so $\rho(\omega) = \frac{1+j\omega\tau}{\sigma_0} = \frac{1}{\sigma_0} + \frac{j\omega\tau}{\sigma_0}$ (3.4),

where σ_0 is the frequency independent DC conductivity mentioned in Eq.(3.2) above. For the 1D conductivity case, Eq.(3.3) provides conductance per unit length. Considering the 1D conductor case here, with only one conductivity channel with two spin modes and length L, the interval of neighboring states in *K* space is given as 2π/L. So the number of carriers per unit length from (-K_f to K_f) can be derived as [87]:

$$n_{1d} = 2x2\left\{\frac{K_f}{2\pi}\right\} = \frac{2K_f}{\pi} \quad (3.5),$$

where K_f is the Fermi wave vector .The first prefactor “2” represents the spin degeneracy, and the second prefactor “2” accounts for both negative and positive *K* space. So the DC conductance of the 1D conductor is given by

$$\sigma_0^{1D} = \left(\frac{n_{1D}\, e^2 \tau}{m^*}\right) = \left(\frac{2K_f e^2 \tau}{m^* \pi}\right) \quad (3.6),$$

and $\hbar K_f = m^* v$ (3.7),

so that $K_f = \frac{m^* v}{\hbar}$ (3.8).

Substituting this value of K_f in Eq.(3.6).

$\sigma_0^{1D} = \left(\frac{2ve^2\tau}{\hbar\pi}\right)$, where $\hbar$ =h/2π (3.9),

$$\sigma_0^{1D} = \left(\frac{4e^2 \tau v}{h}\right) \tag{3.10}$$

In a 1D conductor, the backscattering momentum relaxation time due to back scattering is given as $\tau_B = 2\tau$.

Therefore , Eq.(3.10) can now be re-written as

$$\sigma_0^{1D} = \left(\frac{2e^2 \tau_{\boldsymbol{B}}\, v}{h}\right) \qquad (3.11),$$

$$or\ \sigma_0^{1D} = \left(\frac{2e^2 \lambda}{h}\right), \text{ where } \lambda = \tau_{\boldsymbol{B}}\, v \tag{3.12}$$

Hence, Eq.(3.4) can now be written in the impedance per unit length form as

$$Z_{p.u.l} = \left(\frac{h}{2e^2\lambda}\right)(1 + j\omega\tau) \qquad (3.13),$$

$$Z_{p.u.l} = \left(\frac{h}{2e^2\lambda}\right) + j\omega\tau\left(\frac{h}{2e^2\lambda}\right) = \left(\frac{h}{2e^2\lambda}\right) + j\omega\left(\frac{h}{4e^2 V_f}\right) \qquad (3.14),$$

where V_f is the Fermi velocity = $8\text{x}10^5$m/s.

The first term of Eq.(3.14) is the per unit length scattering resistance (R_S)

$$R_S = \left(\frac{h}{2e^2\lambda}\right) \qquad (3.15),$$

and the second term can be modeled as the inductive impedance($j\omega L_K$),where L_K is the kinetic inductance per unit length and equal to

$$L_K = \left(\frac{h}{4e^2 V_f}\right) = 8nH/\mu m \tag{3.16}$$

The kinetic inductance is dependent on the net sum of kinetic energy of left and right moving electrons in the network, and as a result, it is a per unit length quantity[119].

In reality, besides scattering resistance, there is quantum contact resistance (R_Q).This quantum contact resistance R_Q is also equal to $\left(\frac{h}{2e^2}\right)$ for each conducting channel. This resistance is length independent whereas scattering resistance R_S, depends on both bias voltage and interconnect length. At higher bias, CNT does not show ohmic behavior. On the other hand, in the low bias regime, the CNTs show perfect ohmic behavior and are compatible with VLSI interconnect applications. The high bias resistance has much influence on the interconnect performance in the case where interconnect length is short (L≤λ). In this study here, interconnects are considered long to ignore high bias resistance [97]. There is another contact resistance (R_C) due to imperfect contact condition between CNT and other materials. This resistance can range from zero to hundreds of kilo-ohms for different growth process [124]. For the sake of proper calculation of SWCNT resistance, R_C is assumed 100 kilo-ohms. Due to spin and sub lattice degeneracy of electrons there are 4 parallel conducting channel in SWCNT (N=4). Hence, for CNT with N conducting channel and with length L, the total low bias resistance

$$R_{CNT} = \left(\frac{R_Q+R_SL}{N} + R_C\right) \quad (3.17)$$

The total kinetic inductance of SWCNT is equal to:

$$L_K^{CNT} = \left(\frac{h}{4e^2V_f}\right)\left(\frac{L}{N}\right) \quad (3.18),$$

where kinetic inductance scales down with the number of channels.

CNT has another inductance viz. magnetic inductance (L_M) given as:

$$L_M = \frac{\mu}{2\pi} \ln \frac{y}{d} \tag{3.19}$$

This is the traditional inductive component per unit length due to the electromagnetic (EM) field. In metallic SWCNT, the magnetic inductance depends on the current loop formed by the CNT and is therefore highly dependent on the geometry of the CNT interconnect and its associated ground return paths.

CNT has two capacitances of different origins. One is electrostatic capacitance and the other is quantum capacitance. The electrostatic capacitance (C_E) is due to charge stored by the CNT- ground plane system (Fig.3.1a) and is given by

$$C_E = \frac{2\pi\varepsilon}{\ln\left(\frac{y}{d}\right)} \tag{3.20}$$

This is per unit length of the nanotube. The quantum capacitance (C_Q) accounts for the quantum electrostatic energy stored in the nanotube when it carries current. Considering this energy, an effective capacitance (per unit length) may be obtained, expressed as:

$$C_Q = \frac{2e^2}{hv_f} \tag{3.21}$$

Typically, $C_Q$is 100aF/μm [119]. The effective quantum capacitance is $4C_Q$, due to the four conducting channels in SWCNT. The per unit length electrostatic coupling capacitance between the two parallel CNTs is given by [121]

$$C_C = \frac{\pi\varepsilon}{\ln\left(\frac{x}{d} + \sqrt{\left(s/d\right)^2 + 1}\right)} \tag{3.22},$$

If the diameter $d \ll x$, Eq.(3.22),reduces to

$$C_C = \frac{\pi\varepsilon}{\ln\left(\frac{2x}{d}\right)} \tag{3.23}$$

3.3 Equivalent Circuit and Impedance Parameters of SWCNT Bundle and copper Interconnect

A SWCNT bundle consists of a large number of electrically parallel, isolated CNTs as shown in Fig.3.2. The result of the parallel connection is a considerable reduction of resistance between the ends of the bundle. Therefore, a CNT bundle makes a better interconnect than the isolated counterparts. For the densely packed bundle, the inter-CNT distance (x) is equivalent to tube diameter (d=1nm) as shown in Fig.3.2.

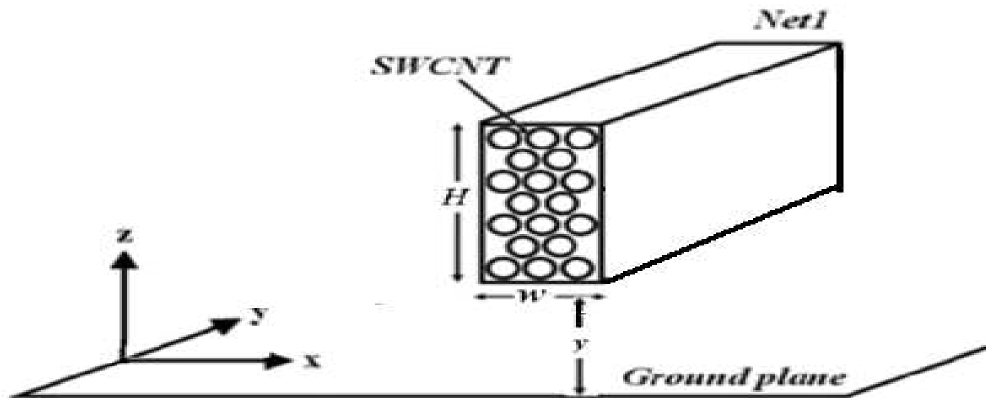


Figure 3.2 Schematic of the interconnect structure using SWCNT bundle. H is thickness, w is the width of SWCNT bundle interconnect and y is the distance between SWCNT bundle interconnect and ground plane.

A commonly used equivalent circuit of bundle SWCNT interconnect is a tandem of series *RLC* circuit segments [54], [55], [118]. The capacitance of each segment is across its output nodes. This equivalent circuit can be further reduced to a single π-*RLC* network [123] as shown in Fig.3.3. The resistances, inductances and capacitances of the π-*RLC* equivalent circuit can be obtained by appropriate use of the expressions available in [54], [118].

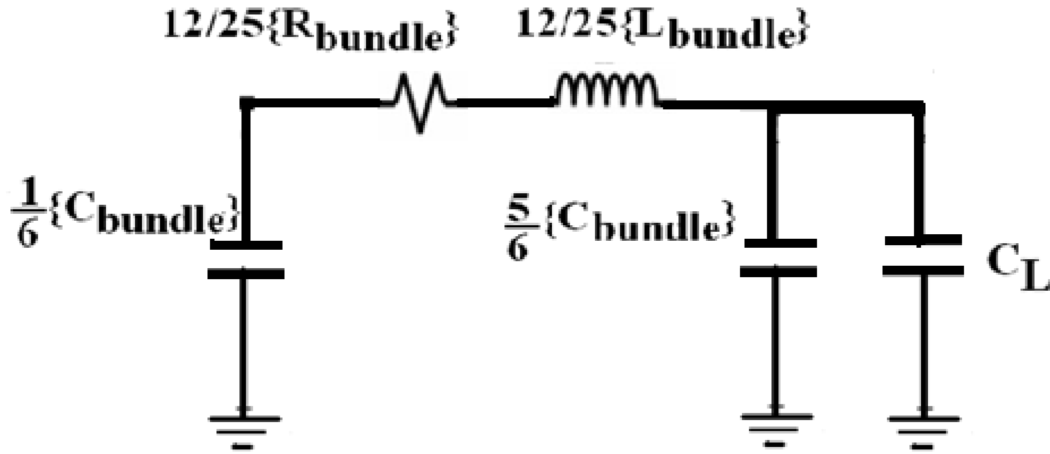


Figure 3.3 Equivalent *π-RLC* model for bundle SWCNT (length(L)> mean free path(λ)) [16].

The resistance of a CNT bundle of length L is given by Eq.(3.24) ,where N_{CNT} is the total number of CNT tubes in the bundle as shown in Fig.3.2, *d* is the tube diameter, *H* is the thickness, *w* is the width of SWCNT bundle interconnect and x is the separation between the centers of two neighbouring tubes.

$$R_{bundle} = \frac{R_{CNT}}{N_{CNT}} \quad (3.24),$$

$$N_{CNT} = n_w\left(\left\lfloor\frac{H-d}{\frac{\sqrt{3}}{2}x}\right\rfloor + 1\right) - \frac{1}{2}\left(\left\lfloor\frac{H-d}{\frac{\sqrt{3}}{2}x}\right\rfloor + 1\right) \quad (3.25),$$

if the number of rows in the bundle is even and is

$$N_{CNT} = n_w\left(\left\lfloor\frac{H-d}{\frac{\sqrt{3}}{2}x}\right\rfloor + 1\right) - \frac{1}{2}\left(\left\lfloor\frac{H-d}{\frac{\sqrt{3}}{2}x}\right\rfloor\right) \quad (3.26),$$

if number of rows is odd. Here $n_w = \left\lfloor\frac{w-d}{x}\right\rfloor$. The number of rows is given as

$$n_H = \left(\left\lfloor \frac{H-d}{\frac{\sqrt{3}}{2}x} \right\rfloor + 1 \right) \quad (3.27)$$

The total effective capacitance of bundle of SWCNT is given by Eq.(3.28), where C_E^{bundle} and C_Q^{bundle} are the total electrostatic capacitance and total quantum capacitance of SWCNT bundle and are calculated by Eqs.(3.29) and (3.30),

$$C_{bundle} = \frac{C_E^{bundle} . C_Q^{bundle}}{C_E^{bundle} + C_Q^{bundle}} \quad (3.28),$$

$$C_E^{bundle} = 2\left(\frac{2\pi\varepsilon_{OX}}{\ln\left(\frac{S}{d}\right)}\right) + \left(\frac{\left\lfloor\frac{w-d}{x}\right\rfloor - 2}{2}\right)\left(\frac{2\pi\varepsilon_{OX}}{\ln\left(\frac{S+w}{d}\right)}\right) + 3\,\frac{(n_H - 2)}{5}\left(\frac{2\pi\varepsilon_{OX}}{\ln\left(\frac{S}{d}\right)}\right) \quad (3.29),$$

$$C_Q^{bundle} = \left(\frac{2e^2}{hv_f}\right) N_{CNT} \quad (3.30),$$

where s is the separation between adjacent bundles. The inductance of a CNT bundle is given by the parallel combination of the inductances corresponding to each CNT forming the bundle, which is:

$$L_{bundle} = \left(\frac{L_M + (L_K/N)}{N_{CNT}}\right) \quad (3.31),$$

where L_M and L_K are the magnetic and kinetic inductances of an isolated CNT. These components of isolated CNT inductance are calculated by Eqs. (3.16) and (3.19).

As such, for nanotube lengths L≫ λ *(CNT)*, the kinetic inductance term is not valid [118]. Therefore, L_K is excluded from the calculations in this work. The analytical expressions used to calculate the impedance parameters of copper interconnect are recapitulated as follows

[6],[125],[126]:

$$R = \frac{\rho L}{wH} \quad (3.32),$$

$$L_S = \frac{\mu_0 L}{2\pi}\left[\ln\left(\frac{2L}{w+H}\right) + \frac{1}{2} + \frac{0.22(w+H)}{L}\right] \quad (3.33),$$

$$C_g = \varepsilon\left[\frac{w}{y} + 2.22\left(\frac{s}{s+0.7y}\right)^{3.19} + 1.17\left(\frac{s}{s+1.15y}\right)^{0.76}\left(\frac{s}{H+4.53y}\right)^{0.12}\right] \quad (3.34),$$

Here R is the resistance, L_S is the self inductance, M is the mutual inductance and C_g is the capacitance with respect to ground. Also L = length, w = width , H =thickness, ρ=resistivity, y=height above ground, s=spacing, ε=dielectric constant and μ_0=permeability of vacuum.

3.4 ANALYSIS OF EQUIVALENT IMPEDANCE PARAMETERS

3.4.1 Influence of Technology Scaling on Interconnect Resistance

Fig.3.4 exhibits the variation of resistance of long (1 mm) CNT and copper interconnects with technology scaling. These resistance values have been calculated using the data given in [77], [125] and Eqs.(3.1)-(3.32), for different technology nodes. The figure shows that in advanced technology nodes, the resistance of such long (1 mm) CNT interconnect is several times lower than that of long (1 mm) copper based interconnects. This is due to the higher dominance of deep submicron technology effects in copper compared to CNT, as has already been mentioned in chapter 2. Thus, once again the merit of preferring CNT over copper as a better interconnect material, has been highlighted here.

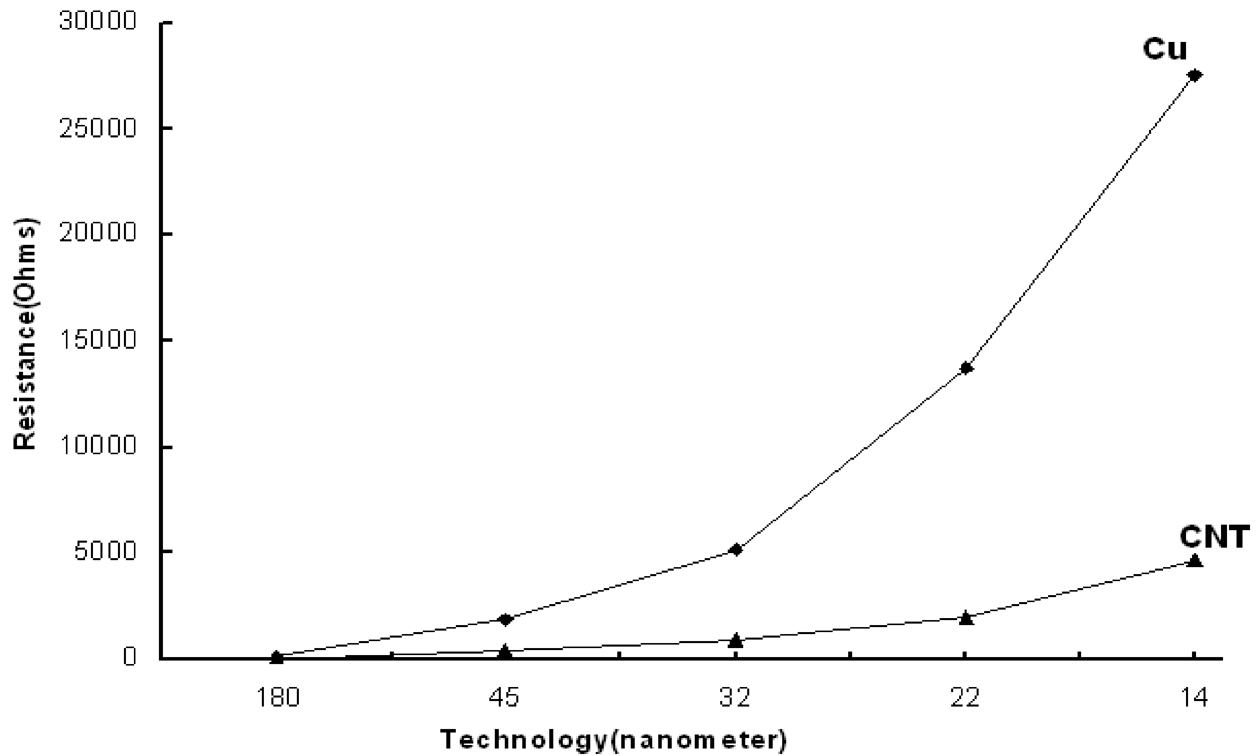


Figure 3.4 Technology node dependence of resistances of long Cu and CNT interconnects. Interconnect length: 1mm.

3.4.2 Influence of Center to Center Distance(x) between adjacent Tubes on Impedance Parameters and Number of Tubes in SWCNT bundle

The π-equivalent circuit impedance parameters of a SWCNT bundle, constituted by tubes of 1nm diameter [77],[127],[128], are now calculated as function of tube separation, tube diameter and tube length , from Eqs.(3.1)-(3.31) and the data given in Table 3.1. These have been tabulated in Tables 3.2 , 3.3 and 3.4 and their variations exhibited in Figs 3.5 and 3.6.

Table 3.1 Simulation parameters [77]

Technology :22nm			Technology:32nm	
V_{dd}=0.7V; Mean free path (SWCNT)=1000nm; Oxide thickness=39.6nm; Oxide dielectric constant=2.05; $\rho\rho_{Cu}(\mu\Omega cm) = 4.2$			V_{dd}=0.9V; Mean free path (SWCNT)=1000nm; Oxide thickness=54.4nm; Oxide dielectric constant=2.25; $\rho\rho_{Cu}(\mu\Omega cm) = 3.52$	
Bundle parameter	Local & Semi-global	Global	Local & Semi-global	Global
Width(w)	22n	32nm	32nm	48nm
Aspect Ratio of interconnect	2	3	2	3
Interconnect thickness(H)	44nm	96nm	64nm	144nm
Separation between adjacent bundles(s)	22nm	32nm	32nm	48nm
SWCNT diameter(*d*)	1nm	1nm	1nm	1nm

Table 3.2 Impedance Parameters of SWCNT bundle for global interconnect (~1mm)

32nm technology				**22nm technology**		
Center to center distance between adjacent SWCNT(*x*)	*R(Ω)*	*L(pH)*	*C(pF)*	*R(Ω)*	*L(pH)*	*C(pF)*
1nm	848.56	0.122	3.845	1952	0.259	2.576
1.5nm	1934.44	0.278	2.558	4539.15	0.602	1.714
2nm	3506.42	0.504	1.905	8208.02	1.088	1.270
2.5nm	5584	0.802	1.525	12944.66	1.716	1.011
3nm	8066.5	1.159	1.271	18607.96	2.467	0.846

Table3.3 Impedance parameters SWCNT bundle for global interconnect (~1mm)

32nm technology				**22nm technology**		
Diameter(*d*)	*R(Ω)*	*L(pH)*	*C(pF)*	*R(Ω)*	*L(pH)*	*C(pF)*
0.7nm	415.583	0.0642	5.04	952.866	0.1397	3.36
0.8nm	550.281	0.0828	4.53	1265.46	0.1764	3.03
0.9nm	691.22	0.1015	4.15	1589.42	0.2158	2.79
1.0nm	867.205	0.1219	3.84	1951.73	0.2587	2.57
1.1nm	1045.16	0.1471	3.57	2380.95	0.3086	2.4

Table 3.4 Impedance parameters of SWCNT bundle and copper (Cu) interconnect

22nm technology						
Length of interconnect (μm)	SWCNT bundle			Copper(Cu)		
	R(Ω)	*C(pF)*	*L(pH)*	*R(Ω)*	*C(pF)*	*L(pH)*
L=50	412.2	0.07	0.036	3104	0.00097	78.23
L=100	222.06	0.25	0.072	1145.8	0.0014	170.33
L=400	798.57	1.031	0.104	5468	0.0059	740
L=700	1375	1.802	0.181	8020.83	0.01	1372
L=1000	1951.73	2.57	0.259	13671.9	0.0148	2031.33
32nm technology						
Length of interconnect (μm)	SWCNT bundle			Copper(Cu)		
	R(Ω)	*C(pF)*	*L(pH)*	*R(Ω)*	*C(pF)*	*L(pH)*
L=50	110	0.32	0.011	890	0.0009	187.23
L=100	230	0.98	0.021	1421	0.0021	350.3
L=400	347.15	1.54	0.049	2037.04	0.006	706.79
L=700	681.85	3.07	0.097	4074.07	0.014	1524.49
L=1000	848.446	3.84	0.122	5092.59	0.017	1950.24

In Fig.3.5, the dependence of the impedance parameters viz., resistance, inductance and capacitance of a SWCNT bundle on the distance between the centers of adjacent tubes for four different interconnect lengths, with the parameters normalized by their respective values for a center to center separation equal to 1nm, have been illustrated in the case of 22 nm technology node. In this case, tube diameter is kept fixed by 1nm. The figure shows that a bundle, composed

of tubes of larger center to center distance, when used as interconnect, will have larger line resistance and inductance but lower capacitance. A similar variation pattern exists in the case of 32 nm technology node.

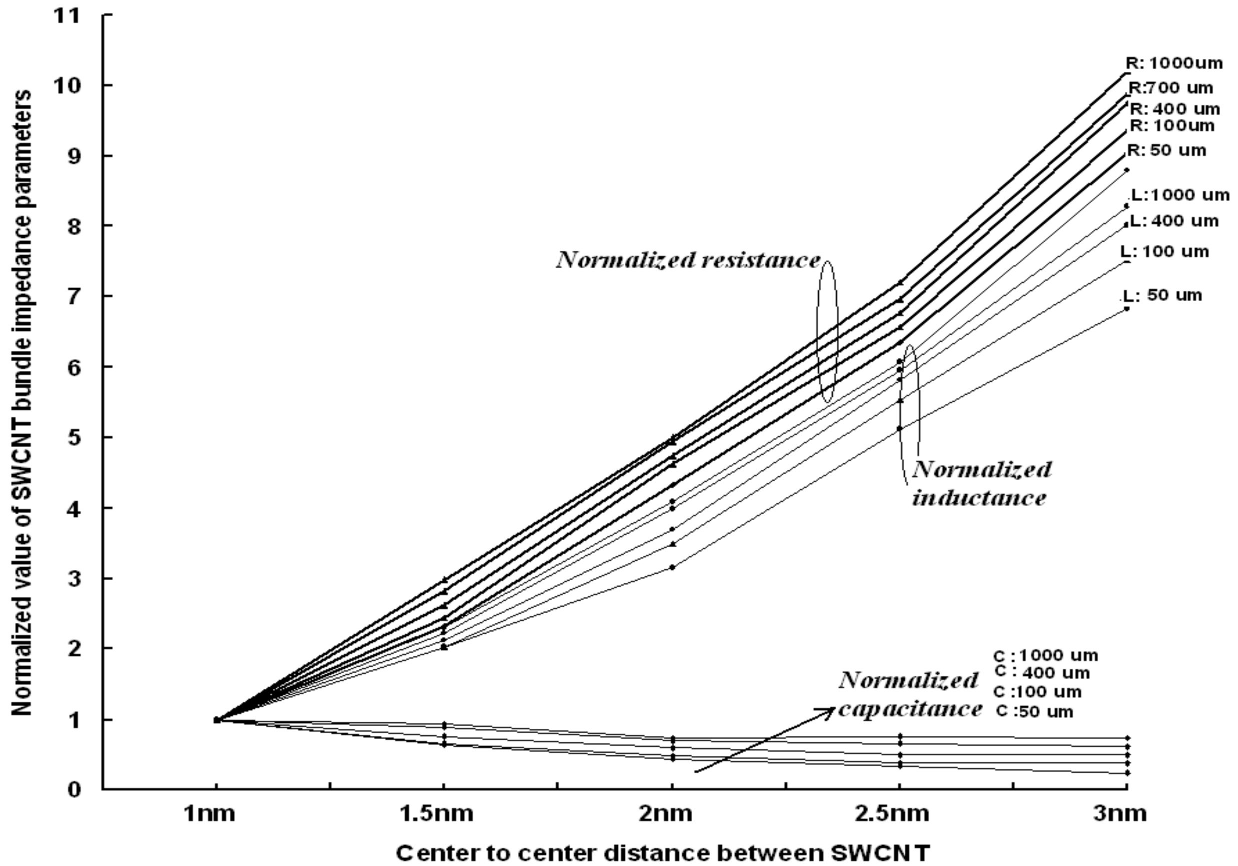


Figure 3.5 Normalized impedance parameters as functions of center to center distance (x) between SWCNT for different interconnect lengths at 22nm technology node. Tube diameter (d) =1nm.

In Fig.3.6, the dependence of SWCNT impedance parameters on tube diameter is exhibited as in the case of 22 nm technology node for 1mm long interconnect. Here the variation of the SWCNT bundle interconnect impedance parameters with center to center distance(x) of adjacent tubes for different tube diameters, where the parameters are normalized by their respective values for a center to center separation equal to 1nm , is shown. It is seen that for

increasing tube diameters, the resistance and inductance of the tube increases but the capacitance decreases. A similar variation pattern exists for the 32 nm technology node.

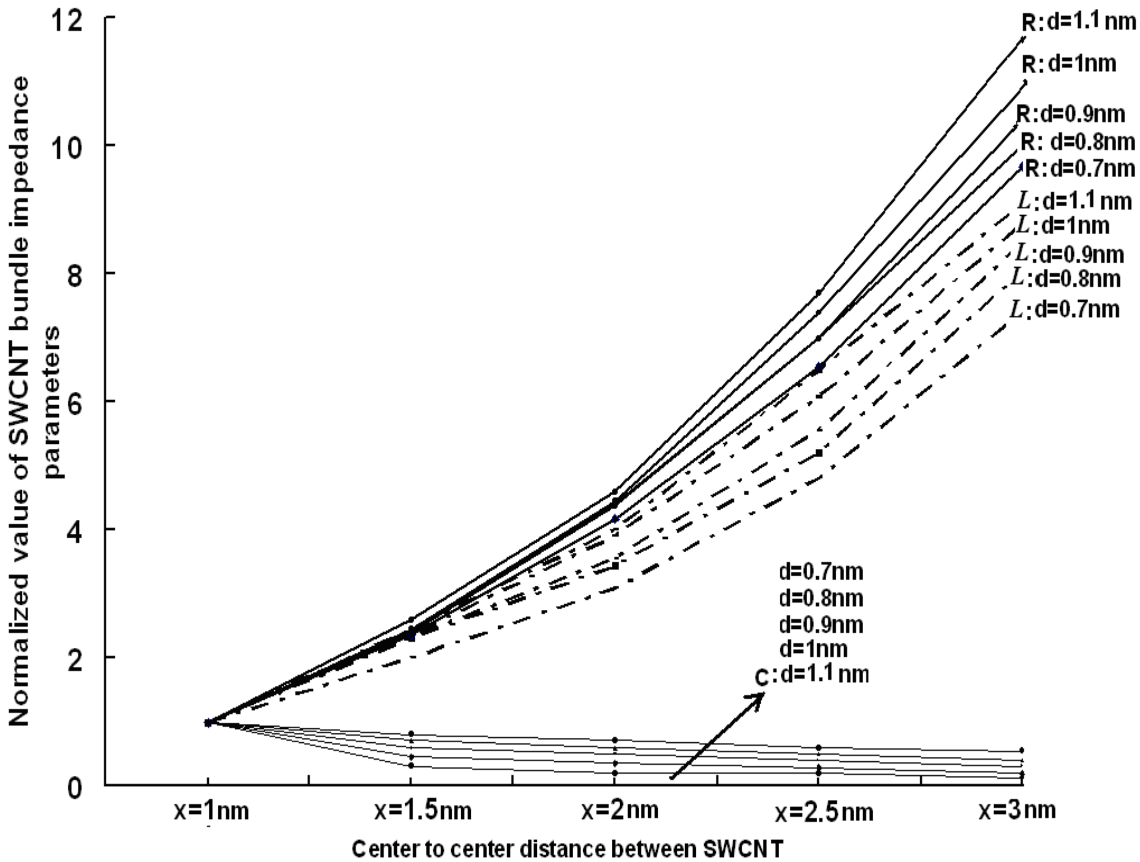


Figure 3.6 Dependence of normalized impedance parameters of center to center distance (x) between SWCNT for different tube diameters at 22nm technology node. Interconnect length=1mm.

Thus a bundle composed of tubes of smaller diameters will have larger interconnect capacitance and lower interconnect resistance. Such a decrease in capacitance and increase in resistance with tube diameters indicates that using a SWCNT bundle composed of tubes of large diameter will produce the desirable effect of reduced power dissipation and interconnect delay. The impedance parameters of a bundle interconnect also depend on the total number of CNTs (N_{CNTs}) that the bundle encloses [55], [118]. The number of N_{CNTs} have been calculated for a

local, semi-global and global SWCNT bundle interconnects and exhibited in Fig.3.7. A nonlinear relationship between N_{CNT} and tube to tube spacing in a bundle is observed for each of the three cases. As spacing between the tubes increases, N_{CNT} decreases and the rate of change falls off sharply. Such a spacing dependence of the number of isolated CNT (N_{CNT}) has a significant effect on the impedance parameters of a SWCNT bundle interconnect.

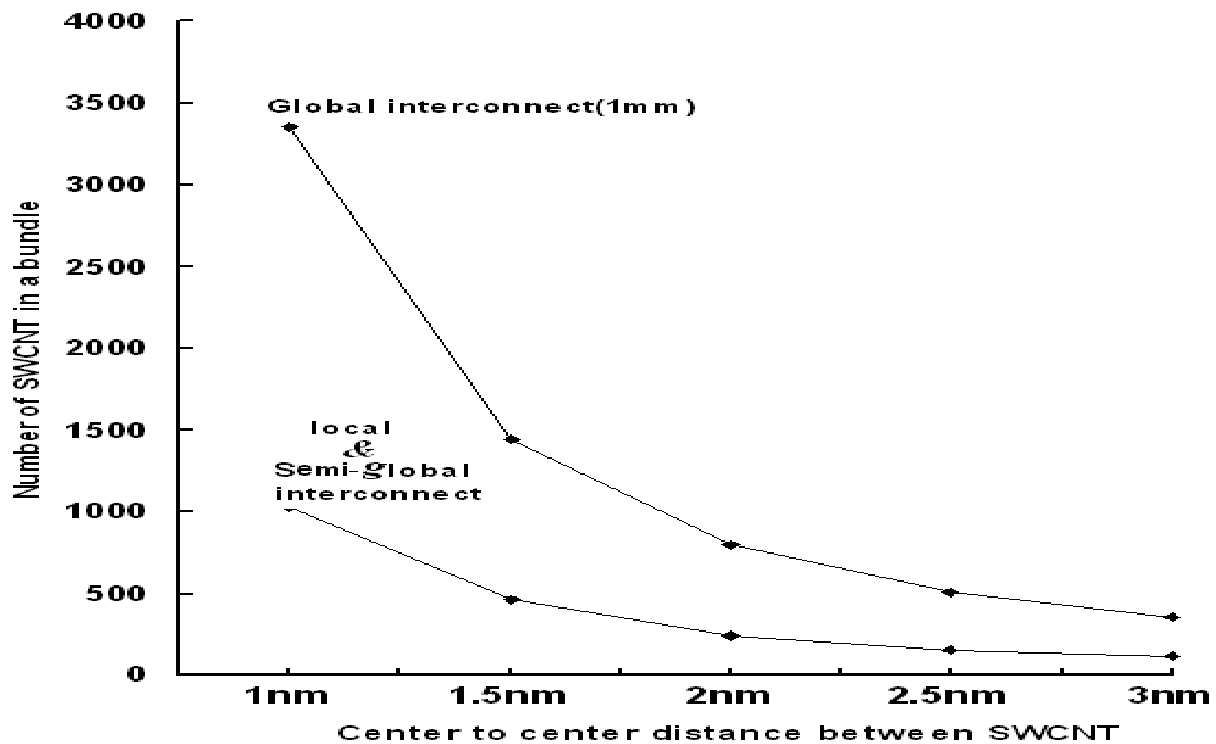


Figure 3.7 Dependence of number of SWCNT (N_{CNT}) as functions of center to center distance (x) between SWCNT. Global interconnect (~1mm): H=96nm, w=32nm and for semi global (≤1mm) and local(~50µm): H=44nm,w=22nm,Technology:22nm.

All tubes in a bundle are electrically connected in parallel. The metallic tubes are the major contributors to the current conduction process in a CNT bundle. Thus bundle resistance will rise as separation between the tubes is increased thereby causing a fall in N_{CNT}. When several inductive elements are in parallel, the resultant inductance of the combination is inversely

proportional to the number of elements. This applies to CNTs as well. As capacitances of parallel capacitors add, decrease in N_{CNT} will lead to decrease in bundle capacitance. Thus, as spacing between adjacent CNT is increased, the bundle capacitance will be decreased.

3.5 ANALYSIS OF SWCNT BUNDLE INTERCONNECT PERFORMANCE IN TERMS OF DELAY AND POWER DISSIPATION

3.5.1 Voltage Waveform at Load Terminal

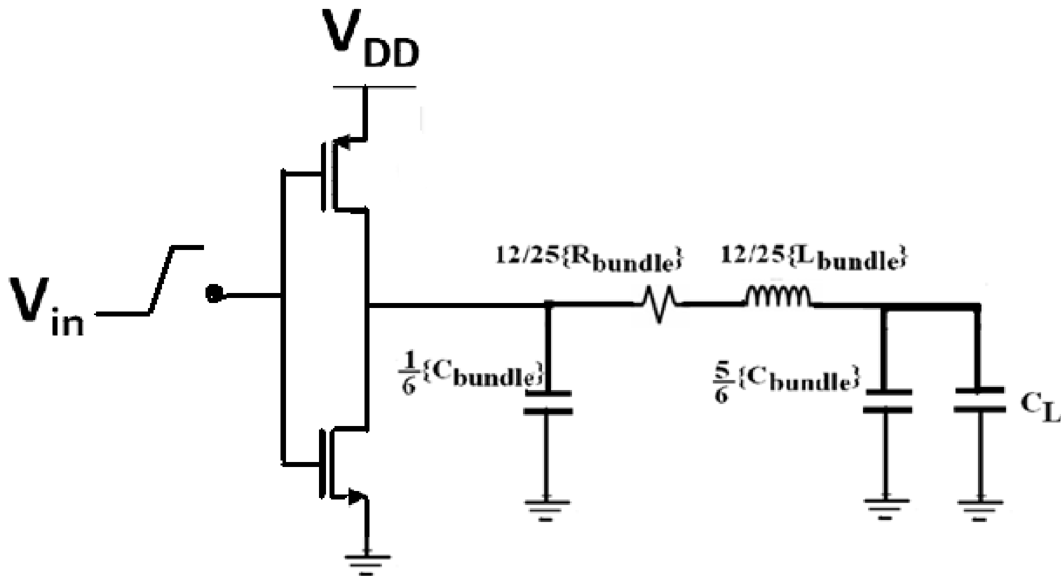


Figure 3.8 CMOS inverter driven π-equivalent *RLC* circuit of SWCNT bundle interconnect[16].

For this part of the analysis, circuits comprising of a CMOS-inverter driving an SWCNT bundle interconnect, loaded by a capacitance of 1pF, as shown in Fig.3.8, has been considered. A 0.1 GHz of input rising pulse with rise time of 1ns provides the input to the inverter. For time analysis of the output voltage across the load capacitance, transistors of the inverter are represented by the α-power law model [129]. A piece wise approach, as described in [16], is used to obtain analytical time dependent expressions for the output voltage over different ranges of the

input transition time. For simulation purposes, SWCNT bundle interconnect is represented by its π-*RLC* model. The Predictive technology model of 32nm and 22nm node [125] is used for the CMOS-driver. Simulation is also carried out for copper-interconnects of same technologies and clock speed. In this case, the circuit parameters are calculated by appropriate use of the expressions from Eqs. (3.32) – (3.34) and the data given in Table 3.1. The performances of these setups are then investigated by comparing the graphical representation of these analytical results with SPICE simulation results (Fig. 3.9).

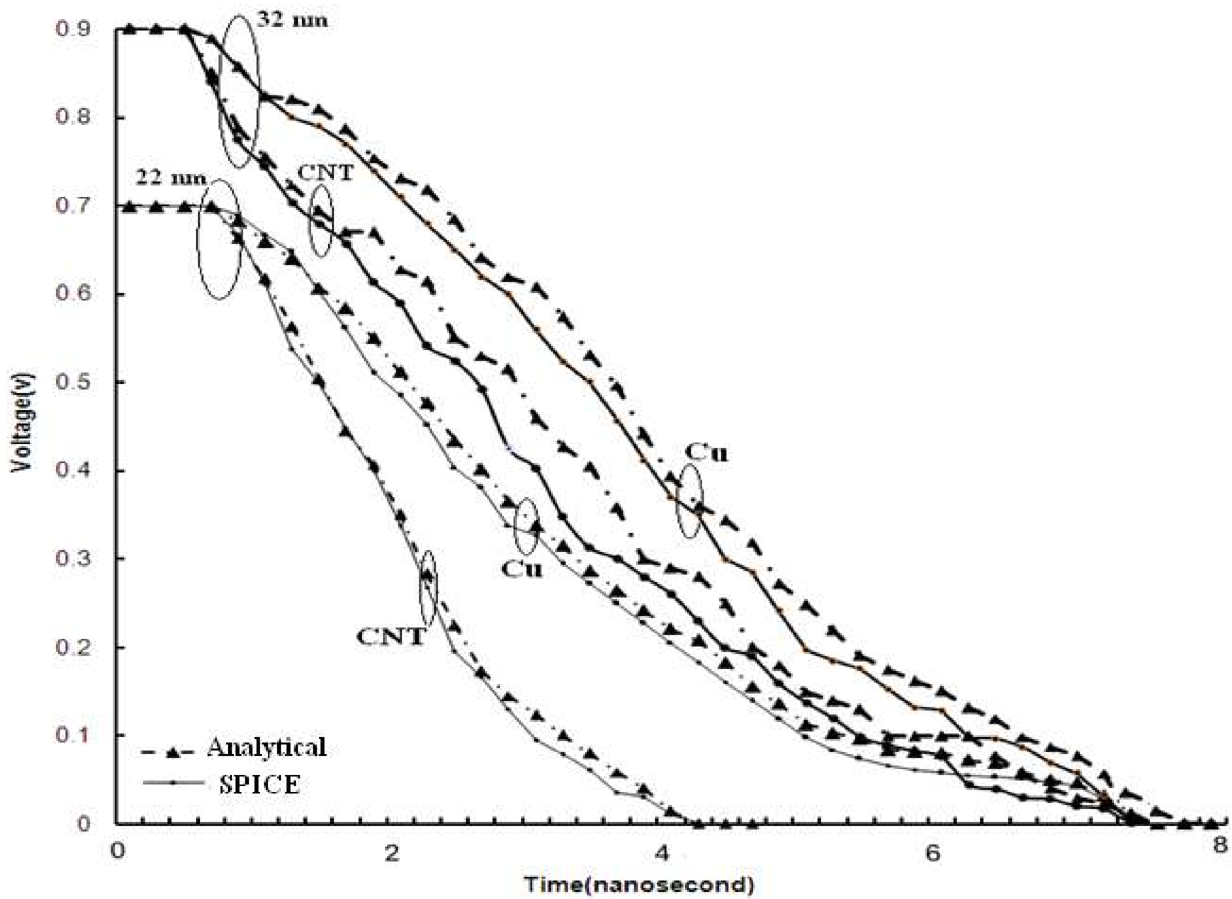


Figure 3.9 Output voltage variation with time in case of 1mm long SWCNT bundle and copper interconnects for fast input ramp.

Fig.3.9 shows the time variation of the output voltage when a low to high transition takes place at the inverter input. The extremely good agreement between the time variation of the output voltage obtained from the piecewise timing analysis and from SPICE simulation results, in both cases of SWCNT bundle interconnects and copper interconnects, is well exhibited here. The figure shows that, for 32nm and 22nm technology nodes, SWCNT bundle interconnects are faster than their copper counterparts. This advantage is due to the low resistance and inductance of CNT interconnects as compared to its copper counterpart (see Table 3.4).

3.5.2 Influence of Tube Diameter on SWCNT Bundle Performance

The impedance parameters of an interconnect is known to affect its delay and power dissipation [130],[131]. As the diameter of an isolated tube controls the impedance parameters of a CNT bundle, it is important to study the effect of the isolated tube diameter on delay and power dissipation. For this part of the analyses, circuits, as shown in Fig.3.8, are considered. For both SWCNT bundle and copper interconnects, 90% delay and average power dissipation are extracted from the SPICE simulation results at 32 and 22nm technology nodes. The size of driver transistor is set to be 40 times the minimum size of transistor. The copper interconnect delay and power dissipation are used as normalizing parameters for SWCNT bundle interconnect delay and power dissipation respectively. These normalized quantities are thus relative measures of CNT interconnect delay and power dissipation with respect to those of copper interconnect. In Fig 3.10, the relative delay as a function of isolated tube diameter is shown. It may be noted here that the variations exhibited in the figure are simply reflections of the resultant effect of diameter variations on resistance and capacitance taken together.

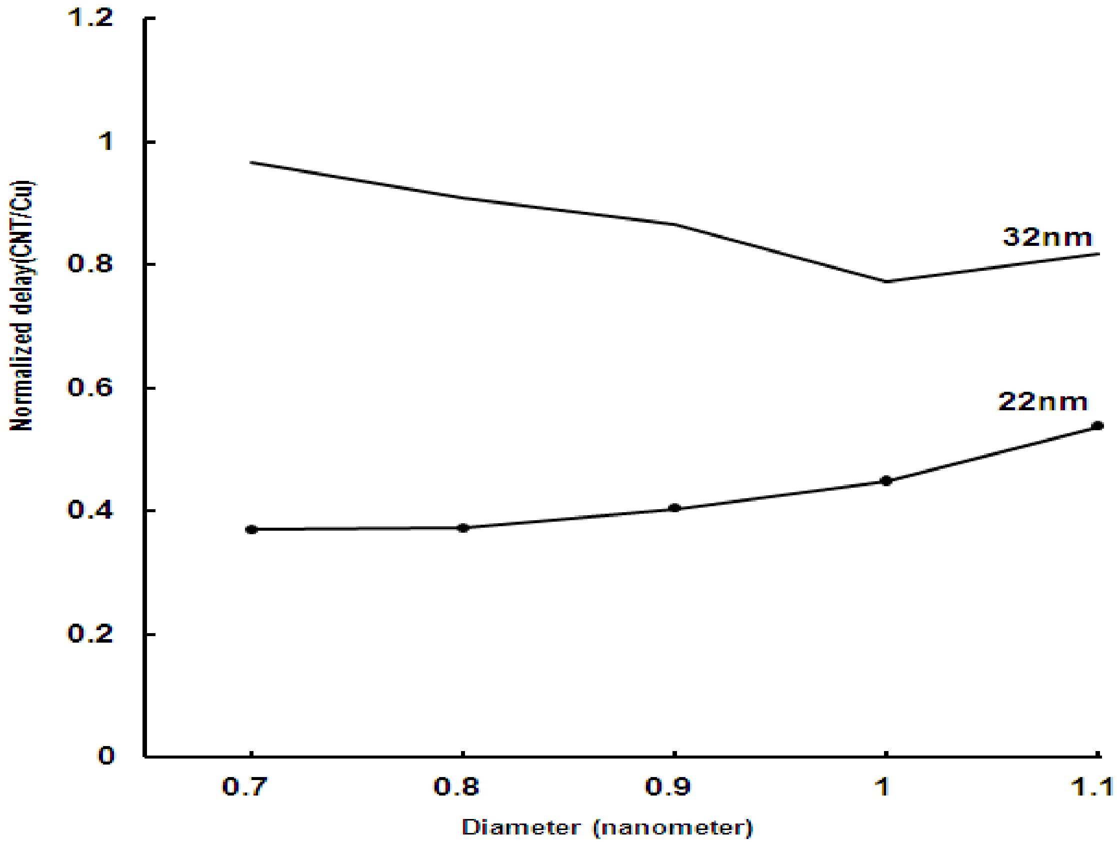


Figure 3.10 Tube diameter dependence of normalized SWCNT bundle interconnect propagation delay at 32nm and 22nm technology nodes with interconnect length=1 mm.

The normalized delay values are always far less than one implying that the CNT interconnect delay is far less than the copper interconnect delay for nearly all diameters. The relatively larger inductance of copper facilitates the lowering of this relative delay thereby placing SWCNT bundle as a more favorable candidate for future VLSI interconnects. In the figure, the gradual rise of relative delay in the case of 22 nm technology node indicates the dominance of CNT resistance over its capacitance. Further, for 32 nm technology node case, it is seen that as diameter is increased the capacitance dominates till a certain critical diameter (diameter ≈ 1 nm) is reached. Beyond this critical diameter, the resistance takes over. Thus for a good performance, if possible, this optimum tube diameter (≈ 1 nm) should be selected (as in the

32 nm technology node case). Otherwise tube diameter should be restricted (as in the 22 nm technology case).

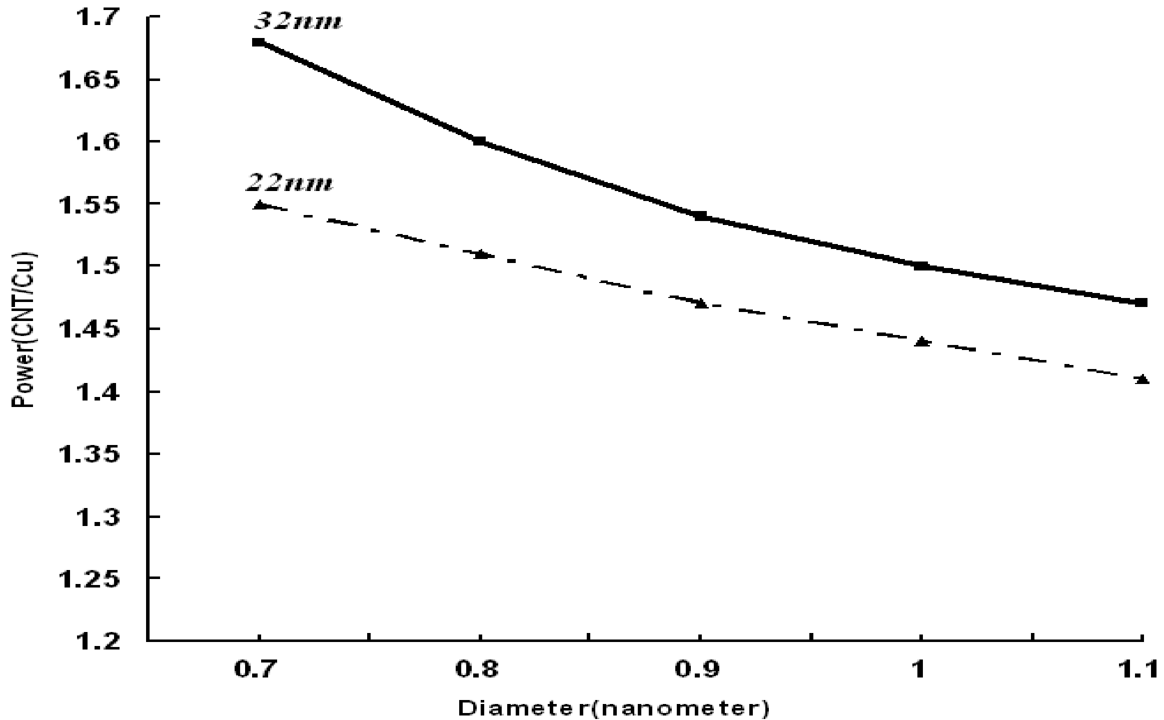


Figure 3.11 Relative power dissipations as function of tube diameter with length 1mm as parameter at 32 and 22 nm technology nodes.

In Fig. 3.11, the ratio of SWCNT and copper interconnect power dissipation, at 32 and 22 nm technology nodes, is illustrated. The pattern of variation of the relative power dissipation shows that, in general, SWCNT-interconnect dissipate more power than its copper counterpart. This is due to the higher tube capacitance values of the SWCNT-interconnect. As SWCNT interconnects have negligible inductance (see Table3.4), the decrease in CNT power dissipation with increase in tube diameter indicates that the effect of capacitance dominates over the effect of resistance. Thus it seems possible to reduce the power dissipation of SWCNT bundle interconnects by increasing the tube diameter.

3.5.3 Influence of Center To Center Distance between adjacent Tubes on SWCNT Bundle Performance

Fig.3.12 shows the variation of relative delay and power dissipation as a function of center to center distance (x) of adjacent SWCNT tubes for different interconnect lengths. For this analysis, the size of driver transistor is set to be 40 times the minimum size of transistor. These relative delay and average power dissipation values have been extracted from the SPICE simulation results at 22nm technology node. The variations are simply reflections of the combined effects of the variations of x on resistance and capacitance. The projected results show that as x increases, the delay increases rapidly but power dissipation falls nominally. An increase of relative delay indicates dominance of resistance of the CNT over its capacitance.

The SWCNT bundle has negligible inductive effect, much less compared to that of copper interconnects. As the equivalent capacitance is a slowly varying function of x (see Fig.3.5), the fall in power dissipation is not much appreciable. It may be noted from Fig. 3.12 that interconnect delay improves if the tubes are close to one another. This indicates that, compared to the sparse bundle, there will be better performance for a dense bundle. However, there is a critical x ($\approx$ 2nm) beyond which the performance of the CNT interconnect is inferior to that of the copper interconnect.

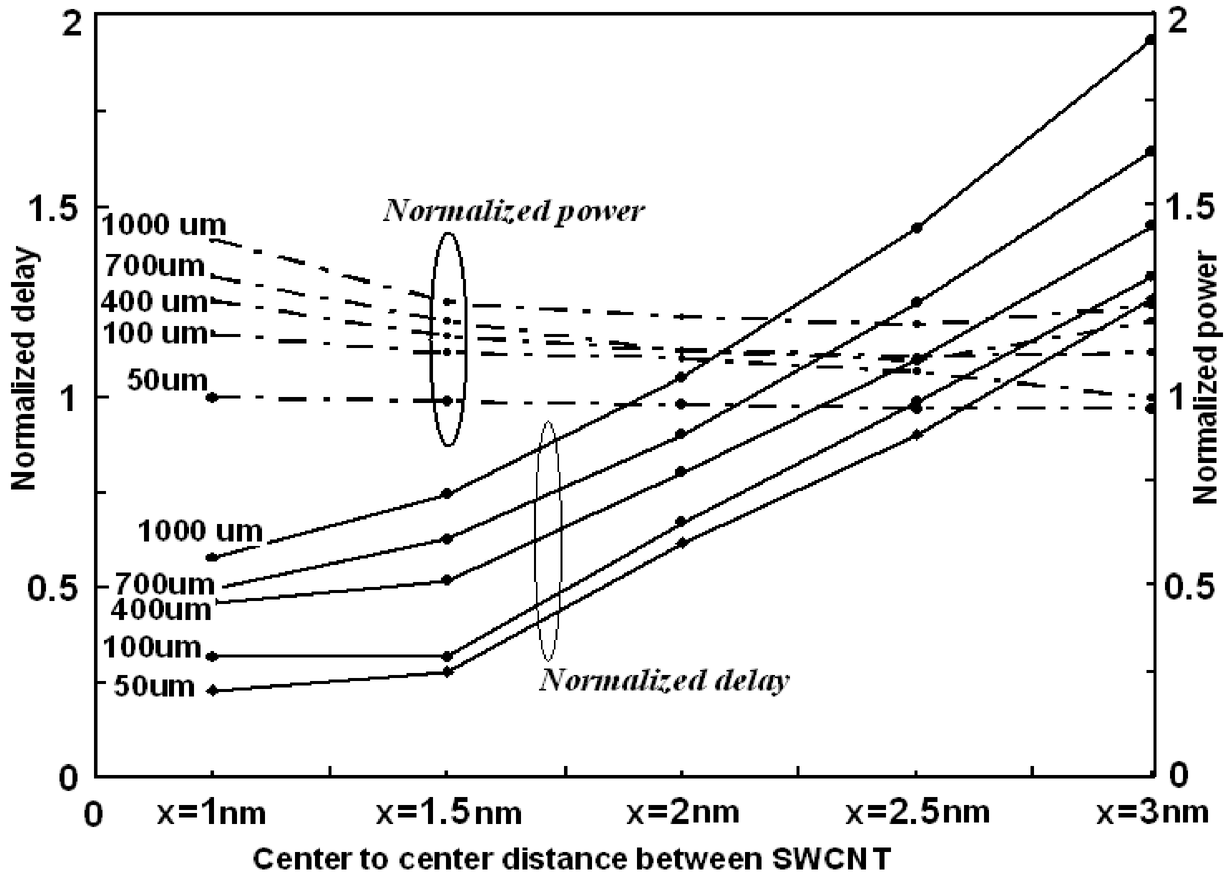


Figure 3.12 Dependence of relative delay and power dissipation on tube separation for different interconnect lengths at 22nm technology node. Tube diameter=1nm.

In Fig.3.13, the variation of relative delay and power dissipation as a function of tube separation and tube diameter, at 22nm technology node, are illustrated. The resultant effect of the variation of both the tube separation and diameter on resistance and capacitance, taken together, are reflected here. The gradual rise in relative delay indicates dominance of CNT resistance over its capacitance, with negligible effect of inductance.

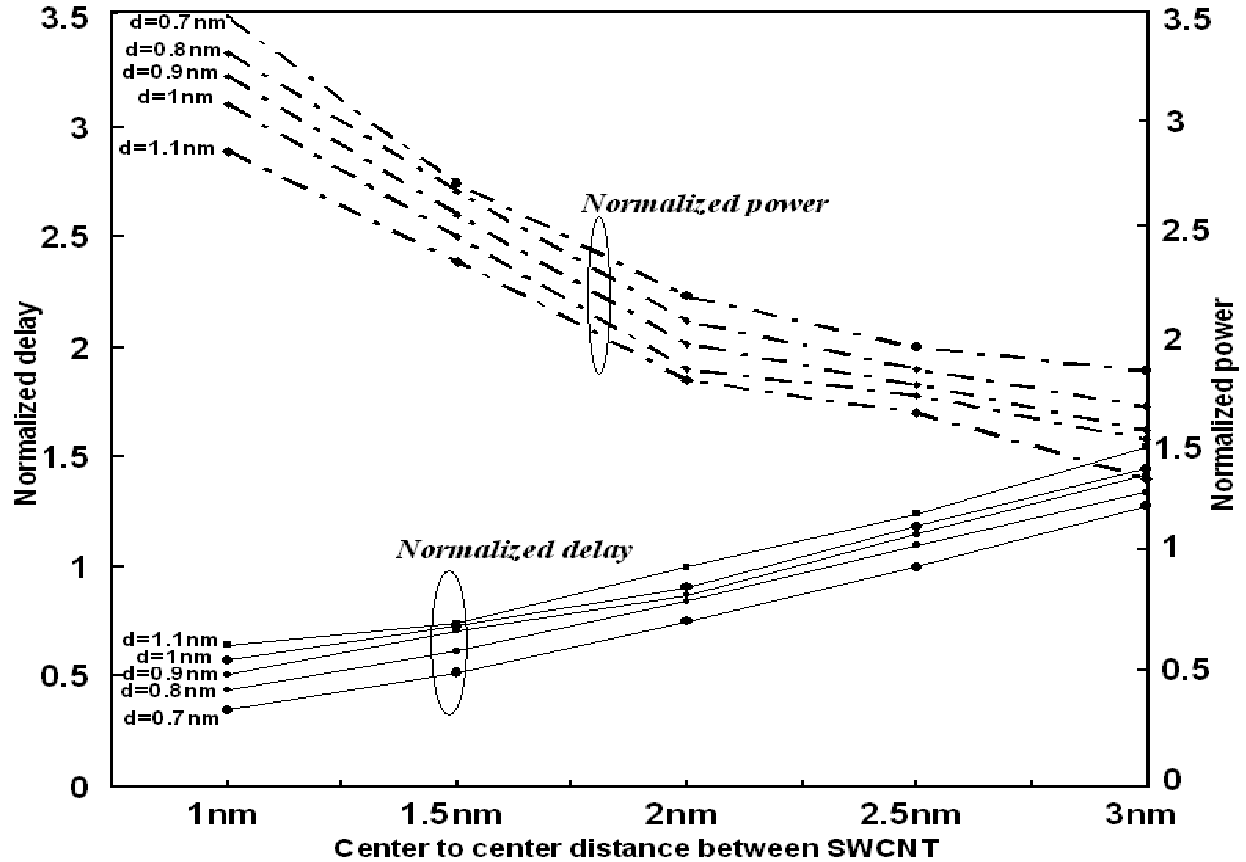


Figure 3.13 Dependence of relative delay and power dissipation on tube separation for different tube diameters at 22nm technology node. Interconnect length=1mm.

For a fixed tube separation with $x \leq$ 2nm, the smallest possible diameter (d=0.7nm) provides a 46% delay reduction on an average, compared with x >2nm. It is observed that the relative power dissipation decreases with increase in tube separation as well as tube diameter. In addition, SWCNT bundle dissipate more power than its copper counterpart. This is due to the higher value of tube capacitance as shown in Table 3.4. The results also indicate that, on an average, the variation of relative power dissipation with tube separation is about 10% more than with tube diameter. Thus for interconnect applications, it is desirable to grow SWCNT bundles of lower x and optimum diameter (if available). Else a lower diameter should be chosen, of course, with due consideration to power dissipation.

3.6 CONCLUSION

The influence of tube parameters viz. *x, d* and L on propagation delay and power dissipation using CMOS inverter driven π-equivalent circuit of SWCNT bundle interconnect at 32nm and 22nm technology nodes has been analyzed. The alpha power law model is used for representing transistors of the CMOS-inverter and the output waveform analytically determined and compared with SPICE simulation results. Good agreement between analytical and SPICE simulation results is achieved at 32nm and 22 nm technology nodes.

It has been observed that, for SWCNT bundle interconnects, delay is appreciably increased as tube separation is increased. Similarly, as tube diameter increases, delay increases appreciably. However, the effect of separation between adjacent tubes on power dissipation is much less. The variation of power dissipation with tube separation is observed 10% more on an average than of tube diameter. The results also indicate that how well the optimized tube separation and tube diameter can control the delay of SWCNT bundle and this can also be utilized to reduce the power dissipation in SWCNT interconnect.

Further, a similar analysis was carried out with the currently used copper interconnects at the same 32nm and 22nm technology nodes and the results obtained are compared with those previously obtained for SWCNT bundle interconnects. On the basis of these, it has been observed that, in terms of delay, SWCNT bundle interconnect performs better than copper interconnect if the separation between the tubes is less than a certain critical value (viz. x=2nm). It has also been noted that a SWCNT bundle composed of tubes of 1nm diameter is of lower delay than copper interconnect at various interconnect lengths and higher power dissipation due to dominance of larger capacitance of SWCNT bundle.

Chapter 4

CROSSTALK ANALYSIS IN COUPLED CARBON NANOTUBE BUNDLE INTERCONNECTS

4.1 INTRODUCTION

As discussed in Chapters 2 and 3, conductive (or metallic) Single Walled Carbon Nanotubes (SWCNTs) are envisioned as ideal interconnect devices, not only for emerging technologies at nano scale but also for today's very deep submicron (silicon-based) electronics. In scaled deep sub micron (DSM) CMOS Technology, the growing interconnect density and reduced chip size causes more capacitive and inductive coupling by parallel running interconnects, thereby affecting the reliability of the performance of the circuit. Thus issues related to crosstalk between coupled interconnects has emerged as a major challenge in the suitable designing of high performance integrated circuits. In recent times, accurate crosstalk analysis between coupled nanotubes has become a prime aspect of research for future nanoscale interconnects based on CNTs. Several researchers have investigated the various effects of crosstalk in CNT interconnects and reported their results in the literature [1]-[13].

As discussed in Chapter 2, crosstalk in coupled interconnects may induce delay, logic failure and noise on the victim line. Coupled voltage noise can, in general, be divided into two categories viz.1) functional crosstalk noise and 2) change in signal propagation delay. In functional crosstalk noise, a victim line experiences a voltage spike due to adjacent line switching. Change in signal propagation delay occurs in the coupled lines due to simultaneous

switching, either in phase or out of phase. In the present chapter, the focus is on the aspects of functional crosstalk noise voltage.

This chapter investigates crosstalk induced, noise voltage waveform and its frequency spectrum in capacitively coupled and mutually coupled SWCNT bundle interconnects, at the far end of victim line, at 32nm and 22nm technology nodes respectively. In mutually coupled interconnects, a magnetic coupling is considered in addition to capacitive coupling. The diameter dependent crosstalk induced noise voltage levels have also been analyzed for the same technology nodes. An alpha power law model has been used for representing transistors of CMOS-driver and the waveform of victim output analytically determined and compared with SPICE simulation results. A similar analysis has been performed for copper interconnects and a comparison made between the results of these two analyses. The analytical and simulation results have shown good agreement.

Based on these results it is found that, compared to copper, crosstalk noise voltage levels in capacitive coupled SWCNT bundles, at the far end of victim line, are significantly low. In mutually coupled copper interconnects, width of the noise waveform is wider compared to CNT at the far end of victim line. These results have further revealed that, compared to copper interconnects, capacitively coupled interconnects of SWCNT bundle filter more noise frequency components at both 32nm and 22nm technology nodes. In addition, compared to copper, mutually coupled interconnects of SWCNT bundles suppress comparable noise components in the higher frequency range for the same technology nodes. Based on these comparative results, an improved model for extracting inter-bundle [118], real life, coupling capacitances between SWCNT bundles has been proposed in this chapter.

Most investigators of bundle interconnects assume the value of coupling capacitance as equivalent to that of the coupling effect between metal interconnects of the same dimensions (e.g.[1]-[6],[118]). However, since material properties of copper widely vary from those of CNTs, perhaps there is need for some more realistic estimation of coupling capacitance values. The present work is an effort in that direction. Here inter bundle capacitance values are estimated using validated empirical relationships for CNT interconnects [118] and both analytical and simulated values of crosstalk-induced noise voltage of this novel interconnects obtained, with a suitable crosstalk analysis.

4.2 CROSSTALK ANALYSIS IN CAPACITIVELY COUPLED INTERCONNECTS

4.2.1 Piece Wise Transient Analysis

In this part of the study, the approach of *CRLC* π-circuit (CMOS inverter driven distributed *RLC* interconnect load) [16] of single interconnect has been used in capacitively coupled SWCNT bundle interconnects for obtaining an accurate analytical expressions for the far end of victim line (victim output). The equivalent capacitively coupled CMOS gate driven π-equivalent distributed RLC circuit is shown in Fig.4.1. Here R, L, C_1 and C_2 represent equivalent *RLC* values of the π-model [131] and C_C is the coupling capacitance. This circuit consists of two coupled interconnects where one line is switching (aggressor line) and the other is quiet (victim line). The aggressor line's CMOS driver transistor can be represented by α- Power Law model [129]. The transistor current representation, using α-Power Law model under different regions of operation, is given in Eq. (4.1).

$$I_D = \begin{Bmatrix} 0:\ cut\ off, \\ K_l(V_{GS} - V_{T0})^{\alpha/2} V_{DS}: Linear\ region, \\ K_S(V_{GS} - V_{T0})^{\alpha}: Saturation\ region, \end{Bmatrix} \quad (4.1),$$

where K_l *and* K_S are the transconductance parameters in linear and saturation regions, respectively; α is the velocity saturation index and V_{T0} is the zero bias threshold voltage.

Instead of linear resistance, CMOS driver has been used here to overcome the discrepancy in results, as has earlier been discussed in Chapter 2. During switching, a transistor in a CMOS gate operates partially in the linear region and partially in the saturation region. In the linear region, the transistor can be accurately approximated by a resistor. However, in the saturation region, the transistor is more accurately modeled as a current source with a parallel high resistance. This high resistance in series with an interconnect line over-rides the series resistance and inductance of the line. Thus interconnect appears predominantly capacitive (*RC*) when the transistor operates in the saturation region and the effect of inductance and resistance is negligible. Therefore for accurate crosstalk analysis, the equivalent linear resistor needs to be replaced by nonlinear CMOS transistors in capacitive coupled interconnects.

The output waveform at the end of victim line is efficiently approximated by piecewise linear waveforms, thereby enabling calculation of the voltage waveform at each point of the interconnect line. In order to obtain the output voltage expression analytically, the input transition period can be divided into four regions for fast input ramp condition, on the basis of MOSFET operating condition. An input ramp is categorized as fast ramp depending on the state the nMOS device attains when the input voltage reaches its final value. If the nMOS continues to operate in saturation region when the input ramp has reached its final value, the ramp is called fast.

The parasitic capacitance due to long interconnect is large. As a result the gate to drain coupling capacitance has a negligible effect on output. So, in this analysis, gate to drain coupling capacitance has been assumed to be negligible. An input, in the form of rising and falling ramp, with transition time τ, is applied to the transistor gate. For calculation purposes, the value of α has been assumed to be 1.

4.2.2 Rising Input Pulse:

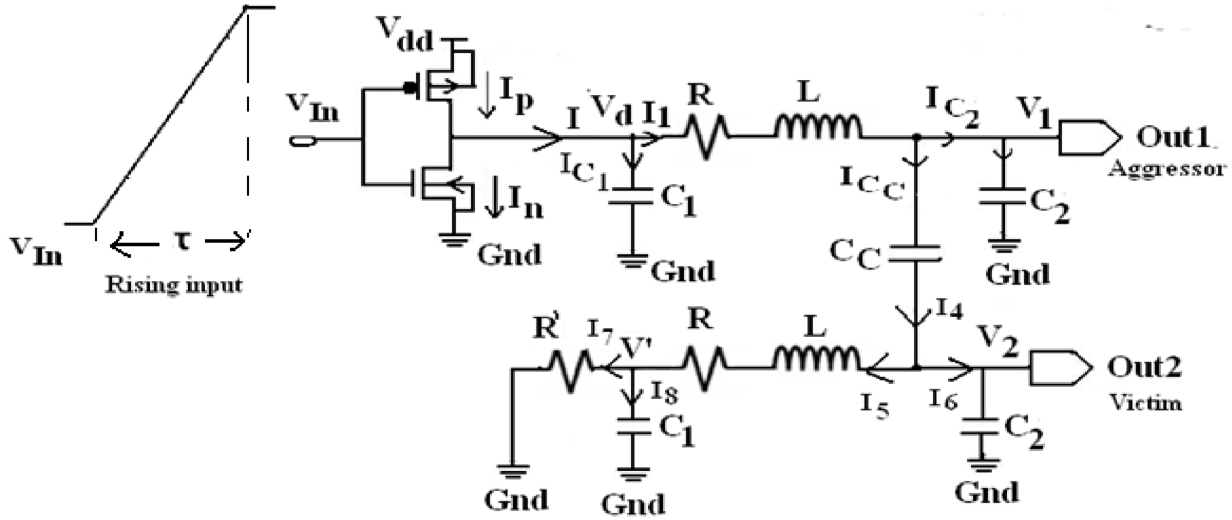


Figure 4.1 Capacitively coupled interconnects with rising input. $R = \frac{12}{15} * R_{bundle}$, $L = \frac{12}{15} * L_{bundle}$, $C_1 = \frac{1}{6} * C_{bundle}$, $C_2 = \left\{\left(\frac{5}{6} * C_{bundle}\right) + C_{load}\right\}$, $R' = driver\ resistance.$

In order to derive the differential equation that describes the operation of the circuit in Fig.4.1, the parasitic current through the pMOS transistor is considered negligible. This is a reasonable assumption since long interconnects present a high capacitance thus reducing the maximum value of the short circuit current [129].

By applying KCL at drain of nMOS in Fig.4.1, we obtain

$$I_p = I_n + I \tag{4.2}$$

Neglecting the pMOS current $(I_p = 0)$ Eq.(4.2) reduces to

$I_n + I = 0$.

By applying KCL at V_d (near-end voltage of the interconnect)

$I = I_{c1} + I_1$, where $I_1 = I_{c2} + I_{Cc}$.

Therefore $I = I_{c1} + I_1 = I_{c1} + I_{c2} + I_{Cc}$ (4.3)

$$\mathrm{I} = C_1 \frac{dV_d}{dt} + C_2 \frac{dV_1}{dt} + C_c \frac{d(V_1 - V_2)}{dt} \tag{4.4}$$

By applying KVL at V_d (near-end voltage of the interconnect)

$$V_d = V_1 + RI_1 + L\frac{dI_1}{dt} \tag{4.5}$$

Substituting the value of I_1 in Eq.(4.5).

$$V_d = V_1 + R\left(C_2 \frac{dV_1}{dt} + C_c \frac{d(V_1 - V_2)}{dt}\right) + L\frac{d}{dt}\left(C_2 \frac{dV_1}{dt} + C_c \frac{d(V_1 - V_2)}{dt}\right) \tag{4.6}$$

Substituting the value of V_d in Eq.(4.4) results in the following third-order differential equation:

$$\mathrm{I} = C_1 \frac{dV_1}{dt} + RC_1C_2 \frac{d^2V_1}{dt^2} + RC_1C_c \frac{d^2(V_1 - V_2)}{dt^2} + LC_1C_2 \frac{d^3V_1}{dt^3} + LC_1C_c \frac{d^3(V_1 - V_2)}{dt^3} + C_2 \frac{dV_1}{dt} + C_c \frac{d(V_1 - V_2)}{dt}$$

$$\mathrm{I} = \frac{d^3V_1}{dt^3}(LC_1C_2 + LC_1C_c) + \frac{d^2V_1}{dt^2}(RC_1C_2 + RC_1C_c) + \frac{dV_1}{dt}(C_1 + C_2 + C_c) - \frac{d^3V_2}{dt^3} LC_1C_c - \frac{d^2V_2}{dt^2} RC_1C_c - C_c \frac{dV_2}{dt} \tag{4.7}$$

By applying KCL at the far end of victim line

$$I_4 = I_5 + I_6 \tag{4.8}$$

$$I_4 = I_6 + I_7 + I_8 \tag{4.9}$$

$C_c \frac{d(V_2 - V_1)}{dt} = C_2 \frac{dV_2}{dt} + C_1 \frac{dV_2}{dt} + \frac{V'}{R'}$ (4.10),

$$where\ V' = -\left(RI_5 + L\frac{dI_5}{dt} + V_2\right)$$

So Eq. (4.10) becomes

$$C_c \frac{d(V_2 - V_1)}{dt} = C_2 \frac{dV_2}{dt} + C_1 \frac{dV_2}{dt} - \frac{R}{R'}\left(C_c \frac{d(V_2 - V_1)}{dt} - C_2 \frac{dV_2}{dt}\right) - \frac{L}{R'}\frac{d}{dt}\left(C_c \frac{d(V_2 - V_1)}{dt} - C_2 \frac{dV_2}{dt}\right) - \frac{V_2}{R'}$$

$$\frac{d^2V_1}{dt^2}\left(\frac{LC_c}{R'}\right) + \frac{dV_1}{dt}\left(-C_c + \frac{R}{R'}C_c\right) = \frac{d^2V_2}{dt^2}\left(-\frac{LC_c}{R'} + \frac{L}{R'}C_2\right) + \frac{dV_2}{dt}\left(-\frac{R}{R'}C_c + \frac{R}{R'}C_2 - C_c + C_2 + C_1\right) + \frac{V_2}{R'} \tag{4.11}$$

Region-I: **(0<t<t_1)**

During this interval of time, nMOS is in cutoff state ($I_n = 0$).From Eq.(4.2)

$I_n + I = 0$ $\qquad\qquad$ $where\ I_n = 0.$

Therefore current reduces to $I = 0$.

From Eq. (4.7), the differential equation describing this state of operation is given as

$$\frac{d^3V_1}{dt^3}(LC_1C_2 + LC_1C_c) + \frac{d^2V_1}{dt^2}(RC_1C_2 + RC_1C_c) + \frac{dV_1}{dt}(C_1 + C_2 + C_c) - \frac{d^3V_2}{dt^3}\ LC_1C_c - \frac{d^2V_2}{dt^2}RC_1C_c - \ C_c\frac{dV_2}{dt} = 0 \tag{4.12}$$

Here initial conditions are $v_1(0) = V_{DD}, \frac{dv_1}{dt} = 0,\ v_2(0) = 0, \frac{dv_2}{dt} = 0$. From Eqs. (4.12) and (4.11), the solution of V_2 (t) can be expressed as $V_2(t)=0$, implying that the value of $V_2(t)$ continues to be at the level of zero up to time t_1 where $V_{in} = V_{t0}$.

Region-II: **(t_1<t<τ)**

In this region of transition time, nMOS operates in saturation region. Therefore, from Eqn.(4.1):

$I_n = k_s(V_{GS} - V_{to})^\alpha$ and from Eq.(4.2), $I + I_n = 0, where\ V_{GS} = \frac{V_{DD}}{\tau}t.$ Where K_s is the transconductance parameter. From Eqs.(4.1) and (4.12), the differential equation which defines this state is

$$\frac{d^3V_1}{dt^3}(LC_1C_2 + LC_1C_c) + \frac{d^2V_1}{dt^2}(RC_1C_2 + RC_1C_c) + \frac{dV_1}{dt}(C_1 + C_2 + C_c) - \frac{d^3V_2}{dt^3}\ LC_1C_c - \frac{d^2V_2}{dt^2}RC_1C_c - C_c\frac{dV_2}{dt} = -k_s\left(\frac{V_{DD}}{\tau}t - V_{to}\right)^\alpha \quad (4.13),$$

$where\ A = LC_1C_2 + LC_1C_c\ , =\ RC_1C_2 + RC_1C_c\ ,\ D = C_1 + C_2 + C_c\ , E =\ LC_1C_c\ ,\ F = RC_1C_c\ , G = C_c$ .The value V_{dd} for different technology nodes are shown in Table 4.1.

The current term $k_s\left(\frac{V_{DD}}{\tau}t - V_{to}\right)^\alpha$ can be solved using a Taylor series expansion:

$$k_s\left(\frac{V_{DD}}{\tau}t - V_{to}\right)^\alpha = A_0 + A_1t \quad (4.14)$$

For $\alpha = 1,\ A_0 = -k_sV_{to}\ and\ A_1 = k_s\frac{V_{DD}}{\tau}$.Therefore Eq.(4.13) can be expressed as

$$\frac{d^3V_1}{dt^3}A + \frac{d^2V_1}{dt^2}B + \frac{dV_1}{dt}D - \frac{d^3V_2}{dt^3}\ E - \frac{d^2V_2}{dt^2}F - G\frac{dV_2}{dt} = -A_0 - A_1t \quad (4.15)$$

The solution of the differential equations in Eqs.(4.11) and (4.15) can be obtained using Laplace Transform and expressed in the s- domain as :

$$V_2(s) = \frac{(-A_0 s - A_1)(Ps+Q)}{s^2[\alpha' s^4 + \beta s^3 + \gamma s^2 + \delta s + \omega]} \quad (4.16),$$

where $V_2(s)$ is the Laplace Transform of V_2 (victim output).

Table 4.1 Various parameters of the transistor used in the analysis

Parameters	Technology nodes	
	32nm	22nm
I_{do}(mA)	1.6	1.45
Vdd(V)	0.9	0.7
α	1	1
V_{to}(nMOS)	0.3692	0.3558
V_{to}(pMOS)	-0.25399	-0.24123
τ (nano second)	1	1

In Eq. (4.16), $P = \frac{LC_c}{R'}$,$Q = -C_c + \frac{R}{R'}C_c$,$W = -\frac{LC_c}{R'} + \frac{L}{R'}C_2$,$T = -\frac{R}{R'}C_c + \frac{R}{R'}C_2 - C_c + C_2 + C_1$,$Z = \frac{1}{R'}$, $\alpha' = WA - PE,\ \beta = BW - PF - QE + TA, \gamma = DW + TB + ZA - PG - QF, \delta = TD + ZB - QG, \omega = ZD$.

Taking the inverse Laplace Transform of Eq.(4.16) we get the solution in the time domain as:

$$V_2(t) = Z_0 * t + Z_1 \exp(s_1 t) + Z_2 \exp(s_2 t) + Z_3 \exp(s_3 t) + Z_4 \exp(s_4 t) + Z_5 \quad (4.17),$$

$where\ Z_0 = \frac{-A_1 Q}{s_1 s_2 s_3 s_4}, Z_1 = \frac{-A_0 P s_1^2 - (A_1 P + A_0 Q) s_1 - A_1 Q}{s_1^2 (s_1 - s_2)(s_1 - s_3)(s_1 - s_4)}, Z_2 = \frac{-A_0 P s_2^2 - (A_1 P + A_0 Q) s_2 - A_1 Q}{s_2^2 (s_2 - s_1)(s_2 - s_3)(s_2 - s_4)}, Z_3 =$

$\frac{-A_0 P s_3^2 - (A_1 P + A_0 Q) s_3 - A_1 Q}{s_3^2 (s_3 - s_1)(s_3 - s_2)(s_3 - s_4)}, Z_4 = \frac{-A_0 P s_4^2 - (A_1 P + A_0 Q) s_4 - A_1 Q}{s_4^2 (s_4 - s_1)(s_4 - s_2)(s_4 - s_3)}$, $Z_5 = -(Z_1 + Z_2 + Z_3 + Z_4)$ and s_1, s_2, s_3 and s_4 are the roots of the equation: $\alpha' s^4 + \beta s^3 + \gamma s^2 + \delta s + \omega = 0$.

Region III: **(τ<t<t_2)**

Over this region, nMOS is in saturation and the input ramp has reached its final value. Therefore $I_n = k_s (V_{GS} - V_{to})^\alpha$, where $V_{GS} = V_{dd}$.From Eqs.(4.2) and (4.12),the differential equation which defines this state is:

$$\frac{d^3V_1}{dt^3}(LC_1C_2 + LC_1C_c) + \frac{d^2V_1}{dt^2}(RC_1C_2 + RC_1C_c) + \frac{dV_1}{dt}(C_1 + C_2 + C_c) - \frac{d^3V_2}{dt^3} LC_1C_c - \frac{d^2V_2}{dt^2} RC_1C_c - C_c\frac{dV_2}{dt} = -k_s(V_{dd} - V_{to})^\alpha \quad (4.18)$$

Time point t_2 is calculated by setting the drain to- source voltage equal to the drain saturation voltage of the nMOS device [129].The solution of the differential equations in Eqs.(4.11) and (4.18), can be obtained using Laplace Transform and expressed in the s-domain as :

$$V_2(s) = \frac{-k_s(V_{dd} - V_{to})^\alpha (Ps + Q)}{[\alpha' s^4 + \beta s^3 + \gamma s^2 + \delta s + \omega]} \quad (4.19)$$

where $V_2(s)$ is the Laplace Transform of V_2 (victim output).

Taking the inverse Laplace Transform of Eq.(4.19), the solution in the time domain is given as:

$$V_2(t) = -k_s(V_{dd} - V_{to})^\alpha [X_1 \exp(s_1 t) + X_2 \exp(s_2 t) + X_3 \exp(s_3 t) + X_4 \exp(s_4 t)] \quad (4.20),$$

where $X_1 = \frac{Ps_1+Q}{(s_1-s_2)(s_1-s_3)(s_1-s_4)}$, $X_2 = \frac{Ps_2+Q}{(s_2-s_1)(s_2-s_3)(s_2-s_4)}$, $X_3 = \frac{Ps_3+Q}{(s_3-s_1)(s_3-s_2)(s_3-s_4)}$,

$X_4 = \frac{Ps_4+Q}{(s_4-s_1)(s_4-s_2)(s_4-s_3)}$.

s_1, s_2, s_3 and s_4 are the roots of the equation:

$$\alpha' s^4 + \beta s^3 + \gamma s^2 + \delta s + \omega = 0$$

Region-IV: **($t>t_2$)**

This region of input transition time has the nMOS operating in its linear region and from Eq.(4.1):$I_n = k_l(V_{dd} - V_{to})^{\frac{\alpha}{2}} V_d$,$where\ V_d = V_1 + RI_1 + L\frac{dI_1}{dt}$ and $I_1 = C_2\frac{dV_1}{dt} + C_c\frac{d(V_1-V_2)}{dt}$.

Here k_l is calculated by measuring I_{D0} and V_{D0} through the device characteristic curves [129] and is given as $K_l = \frac{I_{D0}}{V_{Do}(V_{dd}-V_{to})^{\frac{\alpha}{2}}}$. The value of I_{D0} for different technology nodes are shown in Table 4.1. From Eqs.(4.2) , (4.6) and (4.12) ,the differential equation which defines this state is

$$\frac{d^3V_1}{dt^3}(LC_1C_2 + LC_1C_c) + \frac{d^2V_1}{dt^2}(RC_1C_2 + RC_1C_c) + \frac{dV_1}{dt}(C_1 + C_2 + C_c) - \frac{d^3V_2}{dt^3} LC_1C_c - \frac{d^2V_2}{dt^2} RC_1C_c - C_c\frac{dV_2}{dt} + k_l(V_{dd} - V_{to})^{\frac{\alpha}{2}} V_d = 0$$

$$\frac{d^3V_1}{dt^3}(LC_1C_2 + LC_1C_c) + \frac{d^2V_1}{dt^2}(RC_1C_2 + RC_1C_c) + \frac{dV_1}{dt}(C_1 + C_2 + C_c) - \frac{d^3V_2}{dt^3} LC_1C_c - \frac{d^2V_2}{dt^2} RC_1C_c - C_c\frac{dV_2}{dt} + k_l(V_{dd} - V_{to})^{\frac{\alpha}{2}}\left[V_1 + R\left(C_2\frac{dV_1}{dt} + C_c\frac{d(V_1-V_2)}{dt}\right) + L\frac{d}{dt}\left(C_2\frac{dV_1}{dt} + C_c\frac{d(V_1-V_2)}{dt}\right)\right] = 0 \quad (4.21)$$

The solution of the differential equations from Eqs. (4.11) and (4.21) can be obtained using Laplace Transform and expressed in the s-domain as:

$V_2(s)$

$$= \frac{PP_1V_{dd}s^5 + V_{dd}s^4(PP_2 + QP_1) + V_{dd}.s^3(PP_3 + QP_2 - P_1) + V_{dd}.s^2(QP_3 - P_2) - V_{dd}P_3s - V_{dd}P_7}{s[\alpha_1s^5 + \alpha_2s^4 + \alpha_3s^3 + \alpha_4s^2 + \alpha_5s + \alpha_6]}$$

(4.22),

where $V_2(s)$ is the Laplace Transform of V_2 (victim output) and

$P_1 = LC_1C_2 + LC_1C_c, P_2 = RC_1C_2 + RC_1C_c + k_l(V_{dd} - V_{to})^{\frac{\alpha}{2}}(LC_2 + LC_c), P_3 = C_1 + C_2 + C_c + k_l(V_{dd} - V_{to})^{\frac{\alpha}{2}}(RC_2 + RC_c), P_4 = LC_1C_c, P_5 = RC_1C_c + LC_ck_l(V_{dd} - V_{to})^{\frac{\alpha}{2}}, P_6 = C_c + RC_ck_l(V_{dd} - V_{to})^{\frac{\alpha}{2}}$, $P_7 = k_l(V_{dd} - V_{to})^{\frac{\alpha}{2}}, \alpha_1 = WP_1 - PP_4, \alpha_2 = WP_2 + TP_1 - PP_5 - QP_4, \alpha_3 = WP_3 + TP_2 - PP_6 - QP_5 + ZP_1, \alpha_4 = WP_7 + TP_3 - QP_6 + ZP_2, \alpha_5 = TP_7 + ZP_3$ and $\alpha_6 = ZP_7.$

Taking the inverse Laplace Transform of Eq.(4.22), the solution is obtained in the time domain as:

$$V_2(t) = Y_0 + Y_1\exp(s_1t) + Y_2\exp(s_2t) + Y_3\exp(s_3t) + Y_4\exp(s_4t) + Y_5\exp(s_5t) \quad (4.23),$$

where $Y_0 = \frac{s_1's_2's_3's_4's_5'}{s_1s_2s_3s_4s_5}, Y_1 = \frac{(s_1-s_1')(s_1-s_2')(s_1-s_3')(s_1-s_4')(s_1-s_5')}{s_1(s_1-s_2)(s_1-s_3)(s_1-s_4)(s_1-s_5)}, Y_2 = \frac{(s_2-s_1')(s_2-s_2')(s_2-s_3')(s_2-s_4')(s_2-s_5')}{s_2(s_2-s_1)(s_2-s_3)(s_2-s_4)(s_2-s_5)}, Y_3 = \frac{(s_3-s_1')(s_3-s_2')(s_3-s_3')(s_3-s_4')(s_3-s_5')}{s_3(s_3-s_1)(s_3-s_2)(s_3-s_4)(s_3-s_5)}, Y_4 = \frac{(s_4-s_1')(s_4-s_2')(s_4-s_3')(s_4-s_4')(s_4-s_5')}{s_4(s_4-s_1)(s_4-s_2)(s_4-s_3)(s_4-s_5)}$ and $Y_5 = \frac{(s_5-s_1')(s_5-s_2')(s_5-s_3')(s_5-s_4')(s_5-s_5')}{s_5(s_5-s_1)(s_5-s_2)(s_5-s_3)(s_5-s_4)}$.

Here s_1, s_2, s_3, s_4 and s_5 are the roots of equation:

$\alpha_1s^5 + \alpha_2s^4 + \alpha_3s^3 + \alpha_4s^2 + \alpha_5s + \alpha_6 = 0$ and s_1', s_2', s_3', s_4' and s_5' are the roots of equation:

$PP_1V_{dd}s^5 + V_{dd}s^4(PP_2 + QP_1) + V_{dd}.s^3(PP_3 + QP_2 - P_1) + V_{dd}.s^2(QP_3 - P_2) - V_{dd}P_3s - V_{dd}P_7$=0.

4.2.3 Falling Input Pulse

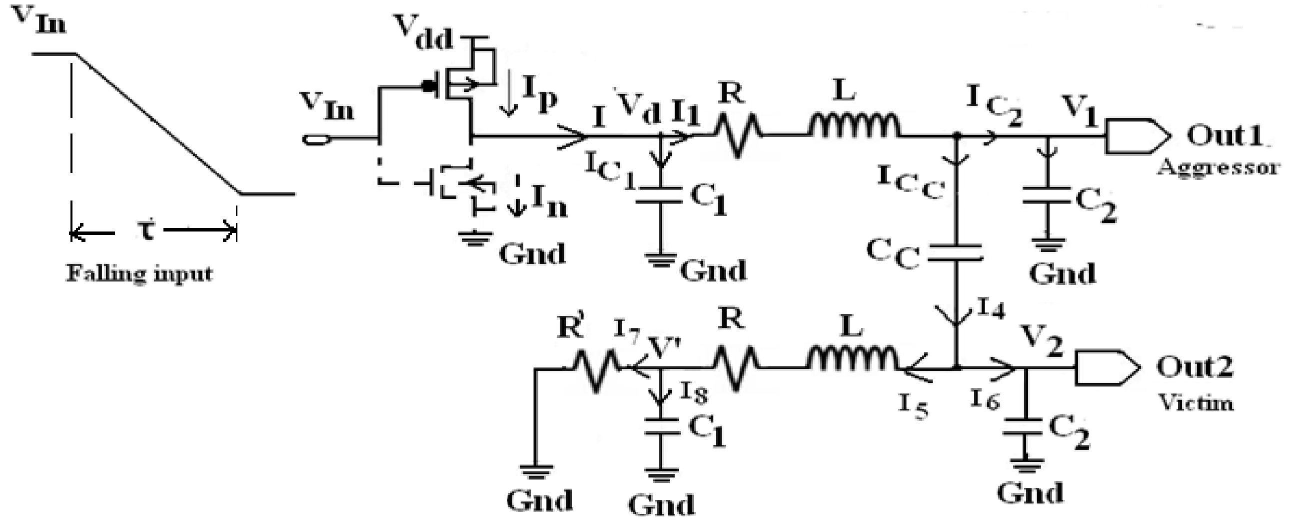


Figure 4.2 Capacitively coupled interconnects with falling input. $R = \frac{12}{15} * R_{bundle}$, $L = \frac{12}{15} * L_{bundle}$, $C_1 = \frac{1}{6} * C_{bundle}$, $C_2 = \left\{\left(\frac{5}{6} * C_{bundle}\right) + C_{load}\right\}$, $R' = driver\ resistance.$

A similar analysis, as in section 4.2.2, gives the output voltage at the far end of victim line. For this falling input pulse, following circuit as shown in Fig.4.2 is considered. In this case, the parasitic current through the nMOS transistor is considered negligible to derive the differential equation that describes the operation of the circuit in Fig.4.2 and it is assumed that

$V_{in} = V_{dd} - \frac{V_{DD}}{\tau}t$. By applying KCL at drain of pMOS

$$I_p = I_n + I \tag{4.24}$$

Neglecting the nMOS current ($I_n = 0$) Eq.(4.24) reduces to $\mathrm{I_p} = \mathrm{I}$.

***Region-I:* (0<t<t$_1$)**

During this region, the pMOS is in cutoff state and according to Eq.(4.24)

$I_p = I$ $\qquad\qquad$ $here\ I_p = 0.$

So $\quad I = 0.$

Circuit differential equation which defines this state is similar to Eq. (4.7), as discussed in 4.2.2.

$$\frac{d^3V_1}{dt^3}(LC_1C_2 + LC_1C_c) + \frac{d^2V_1}{dt^2}(RC_1C_2 + RC_1C_c) + \frac{dV_1}{dt}(C_1 + C_2 + C_c) - \frac{d^3V_2}{dt^3}\ LC_1C_c - \frac{d^2V_2}{dt^2}RC_1C_c - \ C_c\frac{dV_2}{dt} = 0 \qquad (4.25)$$

The initial conditions are $v_1(0) = 0,\ \frac{dv_1}{dt} = 0,\ v_2(0) = 0, \frac{dv_2}{dt} = 0$. From above Eqs. (4.11) and (4.25) ,the solution of $V_2(t)$ is given by $V_2(t)=0$.

***Region-II:* (t$_1$<t<τ)**

The pMOS device operates in saturation and the input signal is in transition, therefore according to Eqn.(4.1) drain current through pMOS expressed as $I_p = k_s\left(V_{dd} - \frac{V_{DD}}{\tau}t - V_{to}\right)^{\alpha}$. From Eqs. (4.7) and (4.24) , results in the following third-order differential equation:

$$\frac{d^3V_1}{dt^3}(LC_1C_2 + LC_1C_c) + \frac{d^2V_1}{dt^2}(RC_1C_2 + RC_1C_c) + \frac{dV_1}{dt}(C_1 + C_2 + C_c) - \frac{d^3V_2}{dt^3}\ LC_1C_c - \frac{d^2V_2}{dt^2}RC_1C_c - C_c\frac{dV_2}{dt} = k_s\left(V_{dd} - \frac{V_{dd}}{\tau}t - V_{to}\right)^{\alpha} \qquad (4.26)$$

The current term $k_s\left(V_{dd}-\frac{V_{dd}}{\tau}t-V_{to}\right)^{\alpha}$ can be solved using Taylor series expansion:

$$k_s\left(V_{dd}-\frac{V_{dd}}{\tau}t-V_{to}\right)^{\alpha}=A_0+A_1t \qquad (4.27)$$

For $\alpha=1,\ A_0=k_s(V_{dd}-V_{to})\ \ and\ A_1=-k_s\frac{V_{dd}}{\tau}$.Therefore, Eq.(4.26) can be expressed as:

$$\frac{d^3V_1}{dt^3}A+\frac{d^2V_1}{dt^2}B+\frac{dV_1}{dt}D-\frac{d^3V_2}{dt^3}E-\frac{d^2V_2}{dt^2}F-G\frac{dV_2}{dt}=A_0+A_1t \qquad (4.28),$$

$where\ A=LC_1C_2+LC_1C_c, B=RC_1C_2+RC_1C_c, D=C_1+C_2+C_c, E=LC_1C_c, F=RC_1C_c\ and\ G=C_c.$

The Solution of differential equation expression from Eqs.(4.11) and (4.28) in terms of s-domain using Laplace Transform of V_2(victim output), can be derived and expressed as :

$$V_2(s)=\frac{(A_0s+A_1)(Ps+Q)}{s^2[\alpha' s^4+\beta s^3+\gamma s^2+\delta s+\omega]} \qquad (4.29)$$

Taking the inverse Laplace Transform of Eq.(4.29), solution of V_2 becomes in time domain:

$$V_2(t)=Z_0*t+Z_1\exp(s_1t)+Z_2\exp(s_2t)+Z_3\exp(s_3t)+Z_4\exp(s_4t)+Z_5 \qquad (4.30),$$

where $P=\frac{LC_c}{R'}, Q=-C_c+\frac{R}{R'}C_c, W=-\frac{LC_c}{R'}+\frac{L}{R'}C_2, T=-\frac{R}{R'}C_c+\frac{R}{R'}C_2-C_c+C_2+C_1, Z=\frac{1}{R'}$,

$\alpha'=WA-PE, \beta=BW-PF-QE+TA, \gamma=DW+TB+ZA-PG-QF$

$\delta=TD+ZB-QG, \omega=ZD, Z_0=\frac{A_1Q}{s_1s_2s_3s_4}, Z_1=\frac{A_0Ps_1^2+(A_1P+A_0Q)s_1+A_1Q}{s_1^2(s_1-s_2)(s_1-s_3)(s_1-s_4)}, Z_2=\frac{A_0Ps_2^2+(A_1P+A_0Q)s_2+A_1Q}{s_2^2(s_2-s_1)(s_2-s_3)(s_2-s_4)}, Z_3=\frac{A_0Ps_3^2+(A_1P+A_0Q)s_3+A_1Q}{s_3^2(s_3-s_1)(s_3-s_2)(s_3-s_4)}, Z_4=\frac{A_0Ps_4^2+(A_1P+A_0Q)s_4+A_1Q}{s_4^2(s_4-s_1)(s_4-s_2)(s_4-s_3)}, Z_5=-(Z_1+Z_2+Z_3+Z_4).$

Here s_1, s_2, s_3 and s_4 are the roots of the expression: $\alpha' s^4+\beta s^3+\gamma s^2+\delta s+\omega=0.$

Region-III: **(τ<t<t₂)**

During this transition interval, the input has reached its final value and the pMOS transistor is still in saturation. Therefore $I_p = k_s(V_{dd} - V_{to})^{\alpha}$. From the Eqs.(4.7) and (4.24), The differential equation which defines this state is

$$\frac{d^3V_1}{dt^3}(LC_1C_2 + LC_1C_c) + \frac{d^2V_1}{dt^2}(RC_1C_2 + RC_1C_c) + \frac{dV_1}{dt}(C_1 + C_2 + C_c) - \frac{d^3V_2}{dt^3}\,LC_1C_c - \frac{d^2V_2}{dt^2}RC_1C_c - \quad C_c\frac{dV_2}{dt} = k_s(V_{dd} - V_{to})^{\alpha} \qquad (4.31)$$

The Solution of differential equation expression from Eqs.(4.11) and (4.31) in terms of s-domain using Laplace Transform of V_2(victim output), can be derived and expressed as :

$$V_2(s) = \frac{k_s(V_{dd}-V_{to})^{\alpha}(Ps+Q)}{[\alpha' s^4+\beta s^3+\gamma s^2+\delta s+\omega]} \qquad (4.31)$$

Here $P, Q, \alpha', \beta, \gamma, \delta\ and\ \omega$ are same as previous one. Taking the inverse Laplace Transform of Eq.(4.31), solution of V_2 becomes in time domain:

$$V_2(t) = k_s(V_{dd} - V_{to})^{\alpha}[X_1 \exp(s_1t) + X_2 \exp(s_2t) + X_3 \exp(s_3t) + X_4\exp(s_4t)] \qquad (4.32),$$

where $X_1 = \frac{Ps_1+Q}{(s_1-s_2)(s_1-s_3)(s_1-s_4)}, X_2 = \frac{Ps_2+Q}{(s_2-s_1)(s_2-s_3)(s_2-s_4)}, X_3 = \frac{Ps_3+Q}{(s_3-s_1)(s_3-s_2)(s_3-s_4)}, X_4 = \frac{Ps_4+Q}{(s_4-s_1)(s_4-s_2)(s_4-s_3)}$ and s_1, s_2, s_3 and s_4 are the roots of the equation:

$\alpha' s^4 + \beta s^3 + \gamma s^2 + \delta s + \omega = 0.$

Region-IV: **(t>t₂)**

During this transition of time, the pMOS transistor operates in linear region. Therefore drain current through pMOS from Eq.(4.2) becomes

$I_p = k_l(V_{dd} - V_{to})^{\frac{\alpha}{2}}(V_{dd} - V_d)$ (4.33),

where k_l is the transconductance parameter(Linear region).

From Eqs.(4.7),(4.24) and (4.33), the differential equation describing this state of operation is given as

$$\frac{d^3V_1}{dt^3}(LC_1C_2 + LC_1C_c) + \frac{d^2V_1}{dt^2}(RC_1C_2 + RC_1C_c) + \frac{dV_1}{dt}(C_1 + C_2 + C_c) - \frac{d^3V_2}{dt^3}\ LC_1C_c - \frac{d^2V_2}{dt^2}RC_1C_c - C_c\frac{dV_2}{dt} + k_l(V_{dd} - V_{to})^{\frac{\alpha}{2}}\left[V_{dd} - V_1 - R\left(C_2\frac{dV_1}{dt} + C_c\frac{d(V_1-V_2)}{dt}\right) - L\frac{d}{dt}\left(C_2\frac{dV_1}{dt} + C_c\frac{d(V_1-V_2)}{dt}\right)\right] = 0 \quad (4.34)$$

The Solution of differential equation expression from Eqs.(4.11) and (4.34) in terms of s-domain using Laplace Transform, of V_2(victim output) can be derived and expressed as :

$$V_2(s) = \frac{-(Ps^2+Qs)P_8}{s[\alpha_1 s^5+\alpha_2 s^4+\alpha_3 s^3+\alpha_4 s^2+\alpha_5 s+\alpha_6]} \quad (4.35),$$

$where\ P_1 = LC_1C_2 + LC_1C_c, P_2 = RC_1C_2 + RC_1C_c - k_l(V_{dd} - V_{to})^{\frac{\alpha}{2}}(LC_2 + LC_c), P_3 = C_1 + C_2 + C_c - k_l(V_{dd} - V_{to})^{\frac{\alpha}{2}}(RC_2 + RC_c), P_4 = LC_1C_c, P_5 = RC_1C_c - LC_ck_l(V_{dd} - V_{to})^{\frac{\alpha}{2}},$
$P_6 = C_c - RC_ck_l(V_{dd} - V_{to})^{\frac{\alpha}{2}}, P_7 = -k_l(V_{dd} - V_{to})^{\frac{\alpha}{2}}, P_8 = V_{dd}\ k_l(V_{dd} - V_{to})^{\frac{\alpha}{2}}.$

s_1, s_2, s_3, s_4, s_5 are the root of the equation:$\alpha_1 s^5 + \alpha_2 s^4 + \alpha_3 s^3 + \alpha_4 s^2 + \alpha_5 s + \alpha_6 = 0$

Here $\alpha_1 = WP_1 - PP_4, \alpha_2 = WP_2 + TP_1 - PP_5 - QP_4, \alpha_3 = WP_3 + TP_2 - PP_6 - QP_5 + ZP_1, \alpha_4 = WP_7 + TP_3 - QP_6 + ZP_2$ and $\alpha_5 = TP_7 + ZP_3, \alpha_6 = ZP_7.$

Taking the inverse Laplace Transform of Eq.(4.35), solution of V_2 becomes in time domain:

$$V_2(t) = Y_1\exp(s_1t) + Y_2\exp(s_2t) + Y_3\exp(s_3t) + Y_4\exp(s_4t) + Y_5\exp(s_5t) \quad (4.36),$$

where

$Y_1 = \frac{-(Ps_1{}^2+Qs_1)P_8}{s_1(s_1-s_2)(s_1-s_3)(s_1-s_4)(s_1-s_5)}$, $Y_2 = \frac{-(Ps_2{}^2+Qs_2)P_8}{s_2(s_2-s_1)(s_2-s_3)(s_2-s_4)(s_2-s_5)}$,

$Y_3 = \frac{-(Ps_3{}^2+Qs_3)P_8}{s_3(s_3-s_1)(s_3-s_2)(s_3-s_4)(s_3-s_5)}$, $Y_4 = \frac{-(Ps_4{}^2+Qs_4)P_8}{s_4(s_4-s_1)(s_4-s_2)(s_4-s_3)(s_4-s_5)}$ and

$Y_5 = \frac{-(Ps_5{}^2+Qs_5)P_8}{s_5(s_5-s_1)(s_5-s_2)(s_5-s_3)(s_5-s_4)}$.

4.2.4 Coupling Capacitance Model

In this analysis, semi-conducting SWCNT is excluded and metallic SWCNT is considered due to its desirable properties as discussed in chapter 2. The coupling capacitance between number of metallic CNTs forming a bundle is of no consequence. This is because, when the CNT bundle carries, it is assumed that each CNT conducting current is held at the same potential, as any other. Hence the coupling capacitance of the bundle that appears as a load on the interconnect is expected to arise mainly from the CNTs lying at the edges of the bundle that are capacitively coupled with the adjacent interconnects [62], [118].

Thus, the model for extracting the coupling capacitance between adjacent bundles of SWCNTs can now be summarized by the following equation [118].

$$C_C(between\ bundles) = 2C_{En} + \frac{n_W-2}{2}C_{Ef} + 3\frac{(n_H-2)}{5}C_{En} \quad (4.37),$$

where $C_{En} = \left(\frac{2\pi\varepsilon_{OX}}{\ln\left(\frac{S}{d}\right)}\right)$, $C_{Ef} = \left(\frac{2\pi\varepsilon_{OX}}{\ln\left(\frac{S+w}{d}\right)}\right)$ and $n_H = \left(\left\lfloor\frac{H-d}{\frac{\sqrt{3}}{2}x}\right\rfloor + 1\right)$.

Here n_H is the number of rows in the interconnect bundle and n_w is the number of "columns". C_{En} and C_{Ef} are the near and far neighbor inter bundle capacitive effects that can be easily calculated for an isolated SWCNT over a ground plane.

4.2.5 Transient Response Analysis At The Far end Of victim Line

In this Section, a comparative study of the crosstalk analysis between (i) SWCNT bundle interconnects with coupling capacitance estimated (a) conventionally (conventional model) and (b) as proposed above, in the present study (proposed model) and (ii) copper interconnects, is reported. Further, a detailed comparative investigation of the analytically extracted capacitive coupled dependent transient responses and simulated transient responses at the far end of victim output, for the proposed model of SWCNT bundle and copper interconnects has been performed and the ensuing results and inferences compared. To analyze the crosstalk voltage noise, a capacitively coupled CMOS inverter driven π-equivalent distributed *RLC* interconnects circuit, as shown in Figs. 4.1 and 4.2, has been considered. All the signal wires are driven by a CMOS driver at 32nm and 22nm technology node [125] with clock speed of 0.1 GHz, rise time=1ns, fall time=1ns and terminated with capacitive load of 0.14fF [77]. For crosstalk analysis, the victim net (i.e. the crosstalk affected net) is kept fixed at logic 0 and the aggressor net (i.e. the net that cause crosstalk on victim) is switched from logic 1→0 and 0→1 respectively. The aggressor line CMOS driver has pMOS width (W_p) double than nMOS width (W_n) while the victim line is grounded at the input through a linear region equivalent driver resistance.

For all calculation and simulation purposes for global(1mm long) interconnect of CNT and copper, all the equivalent various impedance parameters are calculated using Eqs.(3.17)-(3.34) and the data shown in Table 3.1 have been used. The values of proposed coupling capacitance are calculated using the appropriate expression available in Eq.(4.37) and shown in Table 4.2.The coupling capacitance between adjacent bundles of SWCNT for the conventional model is calculated by Eq.(4.38) [6],[125]. For the conventional and proposed model, a densely

packed SWCNT bundle with tube diameter of 1nm has been considered. Table 4.2 shows that, for both technology nodes, compared to the conventional model of coupled SWCNT bundle interconnects with proposed and the copper based coupled interconnects, the coupling capacitance (C_C) of the proposed model is much less, of the order of few a fF only.

Table 4.2 Inter coupling capacitance value between adjacent interconnects

<table>
<tr><th rowspan="2">Technology</th><th rowspan="2">Impedance parameters</th><th colspan="2">SWCNT bundle</th><th>Copper</th></tr>
<tr><td>Conventional</td><td>Proposed</td><td rowspan="2">75.17</td></tr>
<tr><td>22nm</td><td>Coupling capacitance (fF)</td><td>75.17</td><td>2.6</td></tr>
<tr><td>32nm</td><td>Coupling capacitance (fF)</td><td>82.199</td><td>3.89</td><td>82.199</td></tr>
</table>

Fig.4.3 exhibits the crosstalk-induced transient response of the victim output for the SWCNT bundle interconnects with the proposed model and the conventional model of coupling capacitance at 22nm technology node. These observations are based on the simulated results. Compared to the waveform of the proposed model based SWCNT bundle, that based on the conventional shows higher positive and negative voltage peaks. These high positive and negative voltage peaks are due to the low reactance path between the two coupled SWCNT bundles. Figs.4.4 and 4.5 illustrate the analytical piecewise and simulated crosstalk-induced transient response of the victim output for the SWCNT bundle interconnects (proposed model) and the copper interconnects at 32nm and 22nm technology node respectively. There is good agreement between the analytical and simulation results obtained for both CNT and copper at 32nm and 22nm technology nodes.

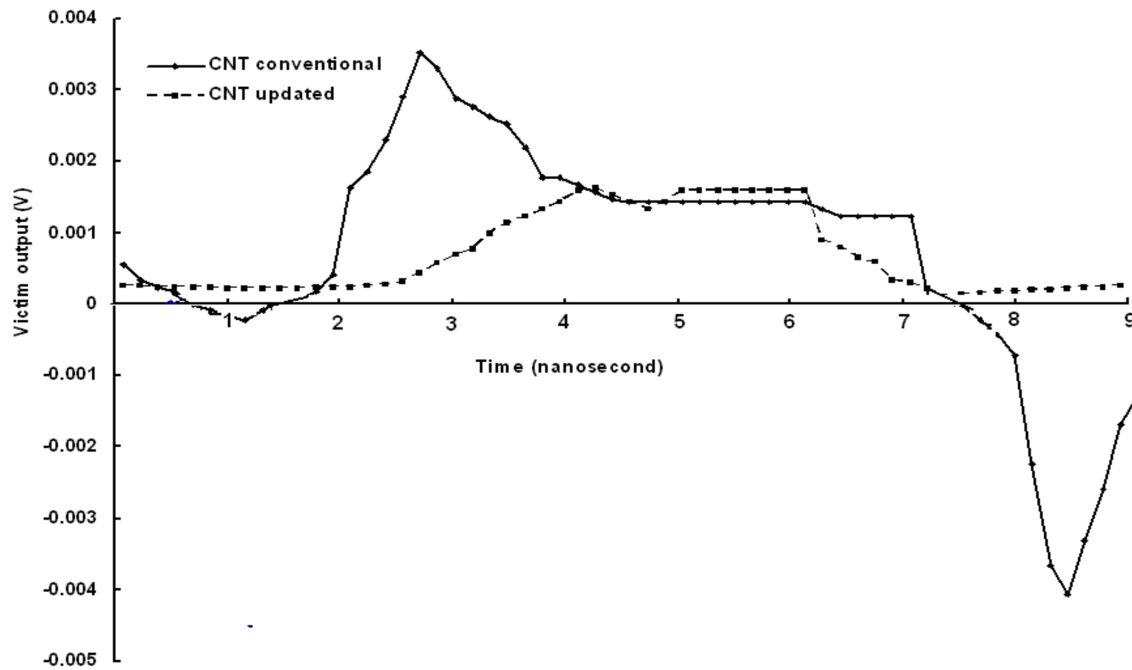


Figure 4.3 Crosstalk induced transient response of capacitively coupled interconnects for the proposed and conventional model of SWCNT bundle at the far end of victim line, at 22n technology node.

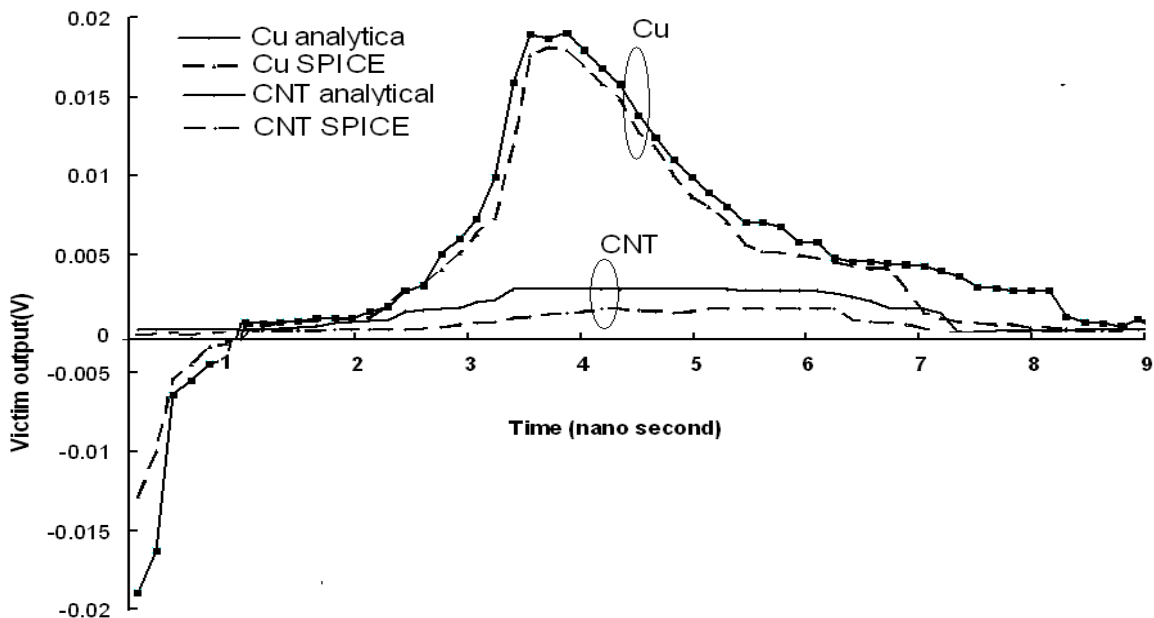


Figure 4.4 Analytical piecewise and simulated crosstalk-induced transient response of the victim output for the SWCNT bundle interconnects (proposed model) and the copper interconnects at 32nm.

Compared to the waveform of the proposed model based SWCNT bundle, that of the copper shows higher positive and negative voltage peaks in the both cases of technologies. The high voltage peaks are due to the comparatively higher self inductance (L_S), coupling capacitance (C_C) and lower ground capacitance (C_g) values of copper (see Tables 3.4 and 4.2). Due to this higher C_C value, compared to the SWCNT bundle, copper based coupled interconnects provide a lower reactance path. In addition, as self inductance is increased, the even and odd mode characteristic impedances increases, causing the positive coupled peak voltage to rise significantly [14],[15],[104]. When the ground capacitance increases, both even and odd mode characteristic impedance reduces and causes a large fall in coupled peak voltage.

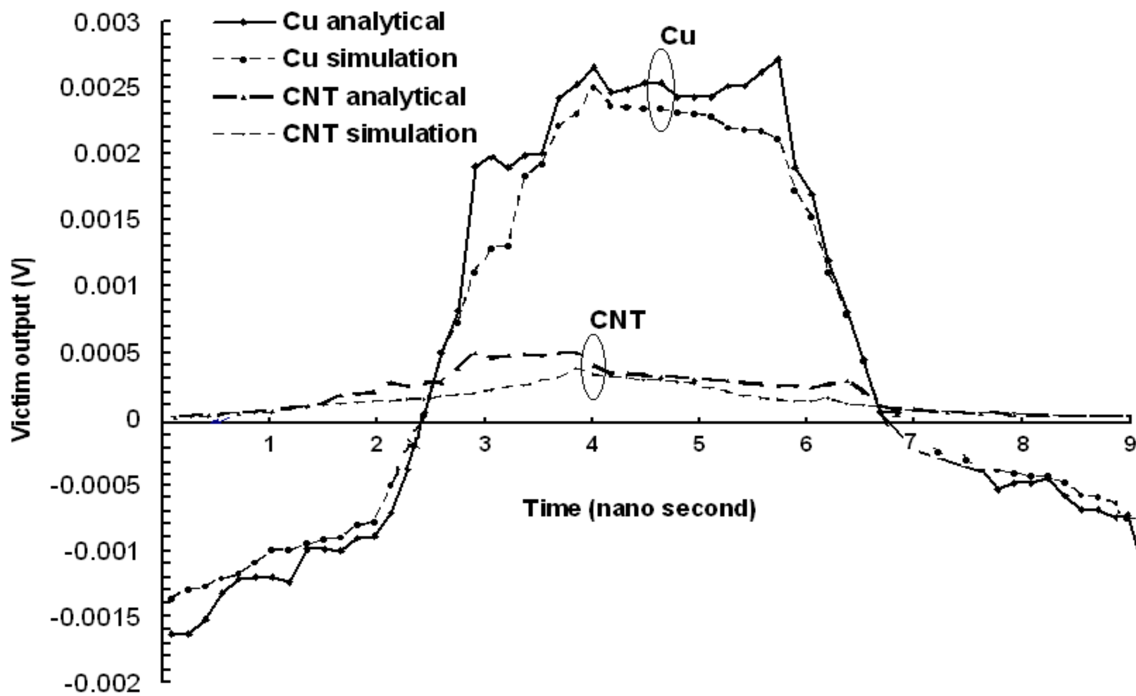


Figure 4.5 Analytical piecewise and simulated crosstalk-induced transient response of the victim output for the SWCNT bundle interconnects (proposed model) and the copper interconnects at 22nm.

4.2.6 Frequency Spectrum Analysis

Figs. 4.6 and 4.7 illustrate the frequency spectrum of the crosstalk-induced transient response waveforms of the victim output, at 32nm and 22nm technology nodes, shown in Figs. 4.4 and 4.5 respectively. The frequency components have been obtained using a script of Fast Fourier transform (FFT) technique written in C language, with transition period of the input and output waveforms divided into 64(2^6) equal parts. The amplitudes of the frequency spectrum (y axis of Figs.4.6 and 4.7) are normalized by the amplitudes of input signal frequency; the frequencies (x axis of Figs.4.6 and 4.7) are normalized by the corresponding input signal frequency. Figs. 4.6 and 4.7 show that, for the entire normalized frequency range, compared to copper interconnects, coupled interconnects of SWCNT bundle have smaller amplitude levels of noise and filter more noise frequency components of victim output. Also, both for SWCNT bundle and copper interconnects, noise frequency components are more suppressed in the smaller frequency range. It may be noted that, compared to CNT, in copper, coupling is more dominant due to low reactance path between two parallel interconnects, a higher line resistance and inductance with smaller line capacitance.

In addition, it may be also noted that as compared to the results exhibited in Fig.4.7, in Fig.4.6 the difference between CNT and copper noise frequency components are more prominent. This is due to the fact that the normalized crosstalk induced noise obtained is more at 22nm compared to 32nm technology node. Furthermore, there is a good agreement between the frequency spectrum of analytical and spice waveform for both CNT and copper at both 32nm and 22 nm technology nodes.

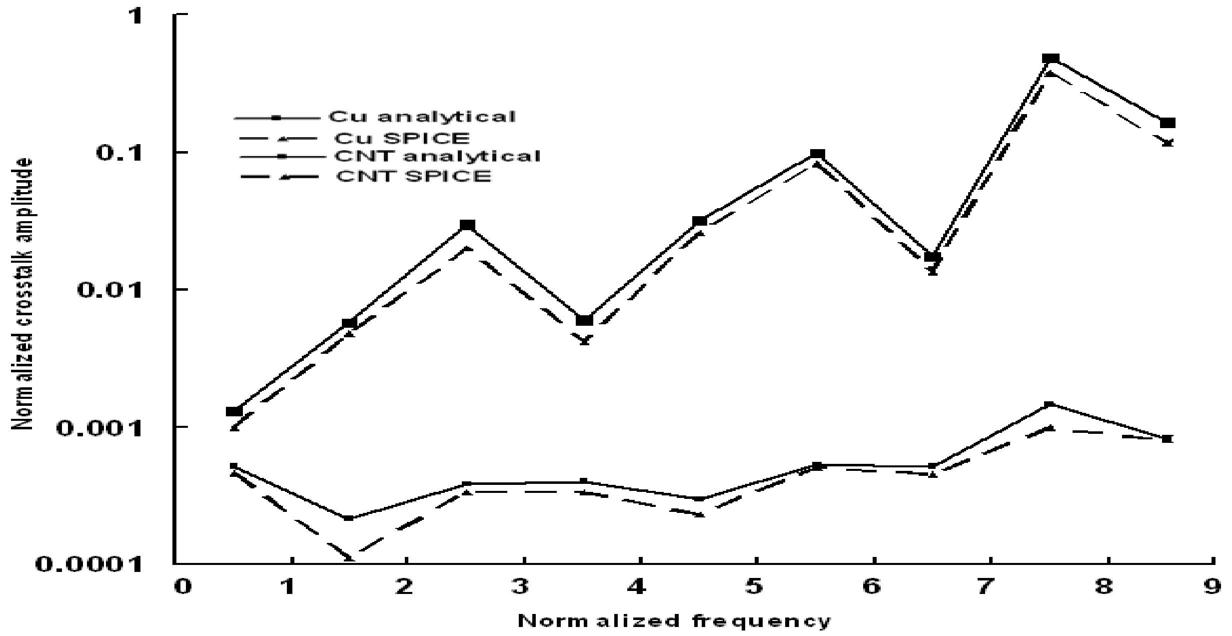


Figure 4.6 Variation of normalized crosstalk amplitude of frequency components for capacitively coupled interconnects at far end of the victim line with normalized signal frequency, at 32nm technology node.

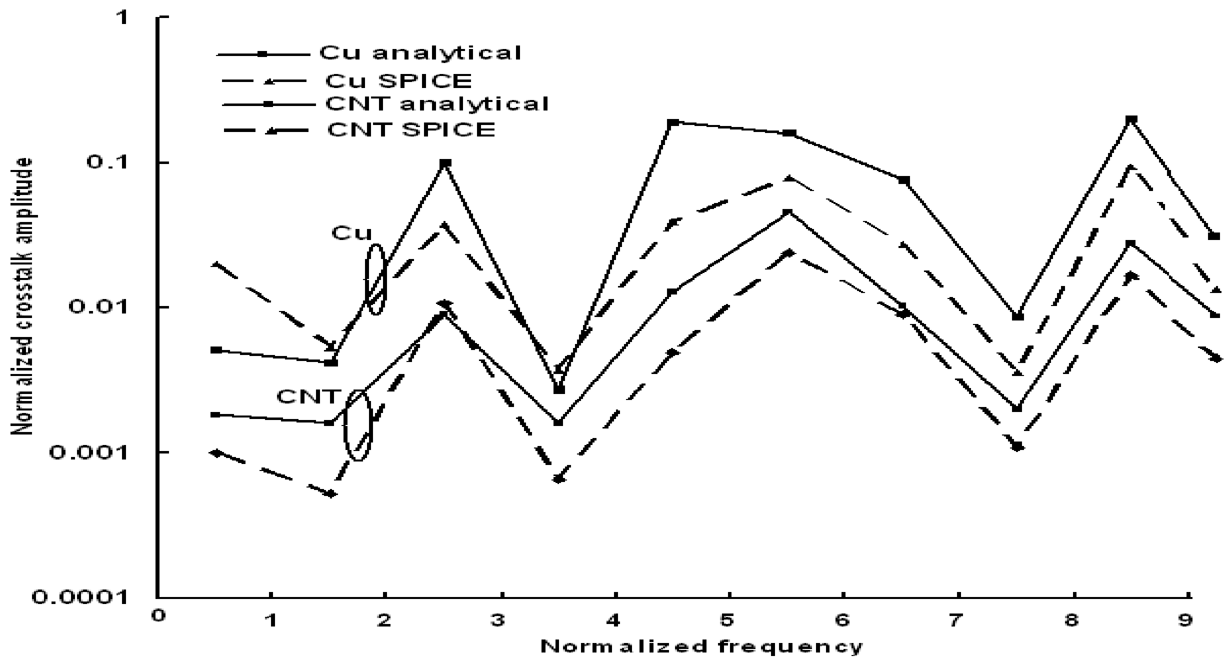


Figure 4.7 Variation of normalized crosstalk amplitude of frequency components for capacitively coupled interconnects at far end of the victim line with normalized signal frequency, at 22nm technology node.

4.2.7 Effect of SWCNT Diameter on Crosstalk Induced Noise Voltage

Fig.4.8 illustrates the dependence of normalized crosstalk noise on the tube diameter (*d*) at 32nm and 22nm technology nodes. Normalized crosstalk noise is defined as the ratio between the terminal voltages at victim output and the input voltage ($V_{victim\ out}/V_{in}$). These observations are based on the simulated results. It is observed that, for both technology nodes, the normalized crosstalk noise at the far end of victim line initially decreases with increase in tube diameter but then increases after a critical value of the tube diameter is reached. The variations are simply reflections of the combined effects of tube diameter (*d*) variations on resistance and capacitance. Initially, the gradual fall in normalized crosstalk with tube diameter indicates dominance of CNT resistance over its capacitance, with negligible effect of inductance. Further, it is seen that as diameter is increased, after a certain critical diameter, the capacitance dominates over CNT resistance. Thus for a good performance in terms of crosstalk, if possible, this optimum tube diameter should be selected.

Also as discussed in chapter 3, SWCNT bundle resistance increases with increase in tube diameter whereas the reverse is true for tube bundle capacitance. Work reported in [14],[15], [104] show that as line resistance increases, the noise peak reduces. This is due to the fact that, with increasing in resistance, the voltage steps traveling along the line undergo attenuation and dispersion. Hence, the voltage steps arriving at far end of the line are smaller and have larger time duration. It may also be noted that the normalized crosstalk noise obtained at 22 nm technology is more compared to 32nm technology node for the entire range of tube diameter. This is due to the comparatively lower values of ground capacitance (C_g) and higher values of self inductance (L_S) for the entire range of diameter variation, as is seen in Table 3.3.

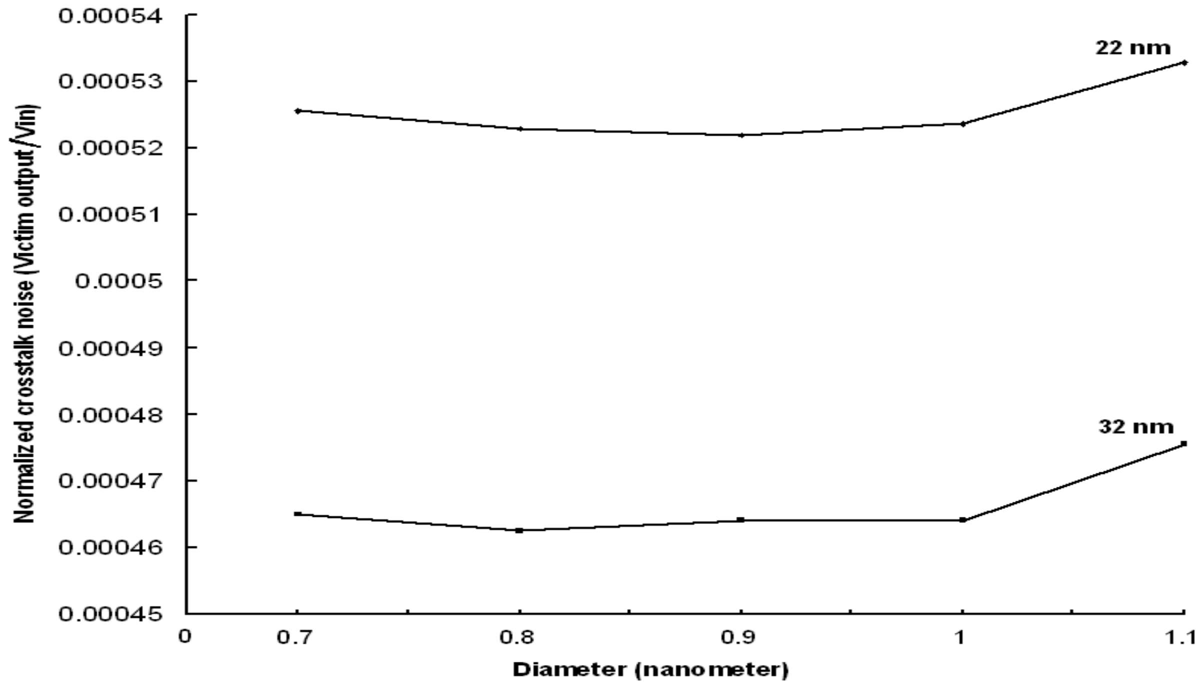


Figure 4.8 Normalized crosstalk noise as a function of tube diameter with length 1mm.

4.3 CROSSTALK ANALYSIS IN MUTUALLY COUPLED INTERCONNECT

4.3.1 Transient Response at the Far End of Victim Output

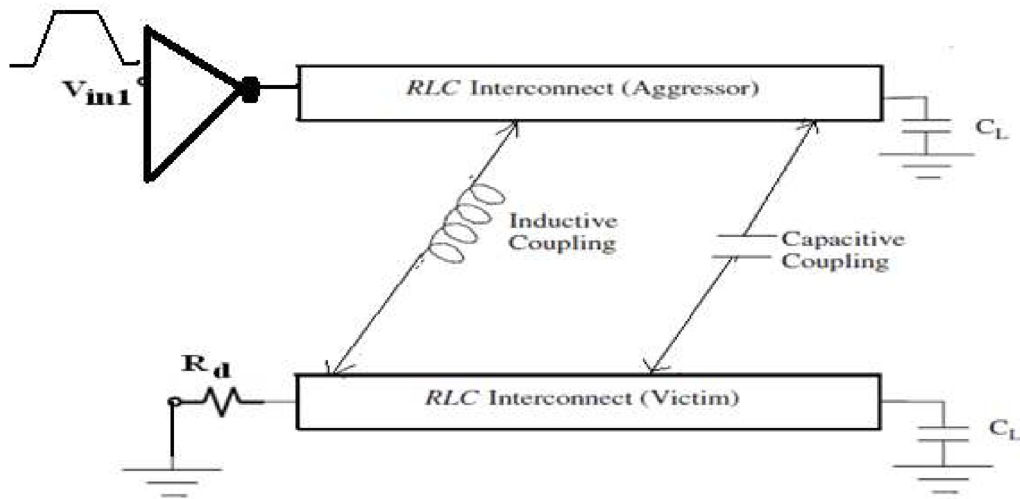


Figure 4.9 Mutually coupled interconnects. R_d and C_L are the driver resistance and load capacitance [15].

Wide wires are frequently encountered in global interconnects in upper metal layers. These wires can exhibit significant inductive effects [15]. For this part of the analysis, circuits comprising of a CMOS-inverter driven, mutually coupled, distributed interconnects of SWCNT bundle, loaded by a capacitance of 0.14pF, as shown in Fig.4.9, has been considered. A 0.1 GHz of rising pulse provides the input to the inverter with rise time and fall time of 1ns. For a transient response analysis of the output voltage across the load capacitance at the far end of victim, transistors of the inverter are represented by the α-power law model [129]. A piecewise approach, as described in [15], is used to obtain analytical time dependent expressions for the output voltage over different ranges of the input transition time. For simulation purposes, the Predictive Technology Model (PTM) of 32nm and 22nm nodes [125] is used for the CMOS-driver. For all calculation and simulation purposes for global(1mm long) interconnect of CNT and copper, the equivalent various impedance parameters are calculated using Eqs.(3.17)-(3.34) and the data shown in Table 3.3 have been used.

Similar analysis is carried out for copper-interconnects of same technologies and clock speed. For this part of the analysis, the victim net (i.e. the crosstalk affected net) is kept fixed at logic 0 and the aggressor net (i.e. the net that cause crosstalk on victim) is switched from logic 1→0 and 0→1 respectively. The mutual inductance between interconnects of SWCNT is assumed to be same as that of copper based interconnect with same dimensions and calculated using Eq.(4.39)[6],[125],[126].The value of inter coupling capacitance of SWCNT bundles is calculated using Eq. (4.37) and for copper, is calculated by Eq.(4.38)[6],[125],[126].

$$C_C = \varepsilon \begin{bmatrix} 1.14\frac{H}{s}\left(\frac{y}{y+2.06s}\right)^{0.09} + 0.74\left(\frac{w}{w+1.59s}\right)^{1.14} \\ +1.16\left(\frac{w}{w+1.87s}\right)^{0.16}\left(\frac{y}{y+0.98s}\right)^{1.18} \end{bmatrix} \quad (4.38),$$

$$M = \frac{\mu_0 L}{2\pi}\left[\ln\left(\frac{2L}{S'}\right) - 1 + \frac{S'}{L}\right] \quad (4.39),$$

Here C_C is the coupling capacitance between adjacent interconnects and M is the mutual inductance. Also L = length, w = width, S'= center to center distance between rectangular interconnect, H=thickness, y=height above ground, s=spacing between parallel interconnects, ε=dielectric constant and μ_0=permeability of vacuum.

Figs.4.10 and 4.11 exemplify the analytical piecewise and simulated crosstalk-induced transient response of the victim output for the mutually coupled SWCNT bundle interconnects and the copper interconnects at 32nm and 22nm technology nodes respectively.

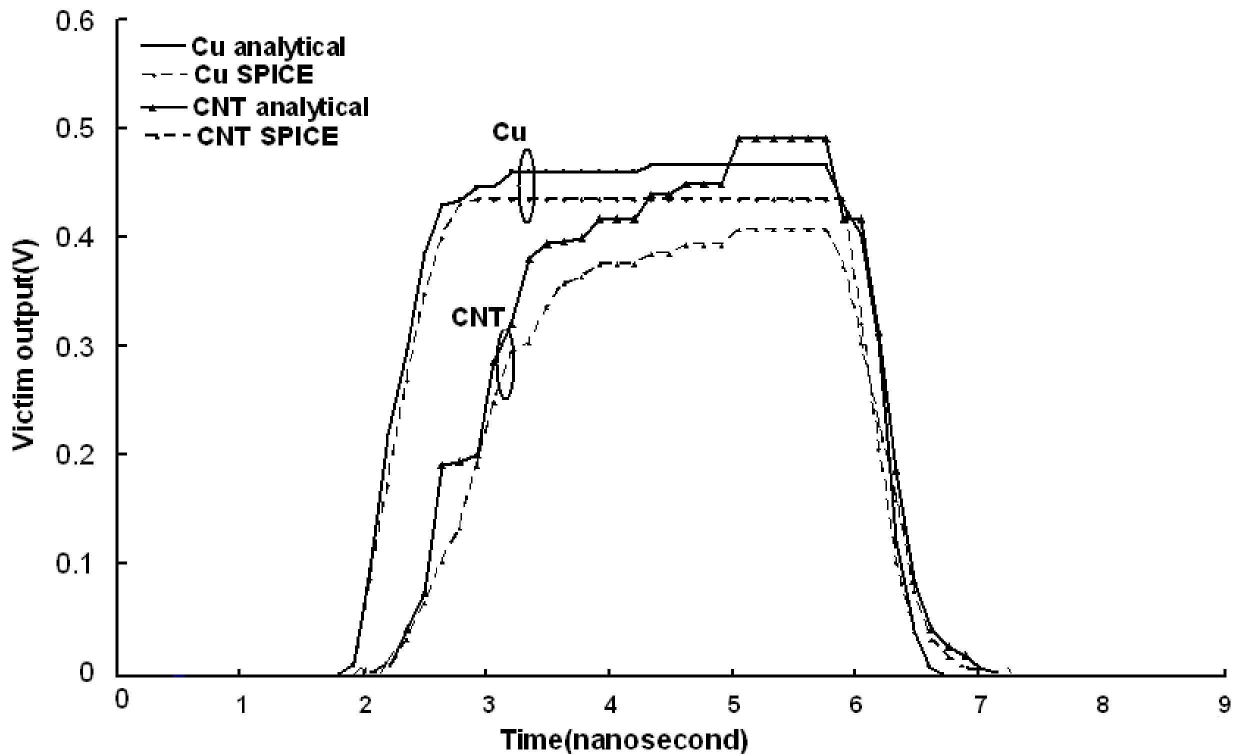


Figure 4.10 Analytical piecewise and simulated crosstalk-induced transient response of the victim output for the mutually coupled SWCNT bundle interconnects and the Copper interconnects at 32nm.

There is good agreement between the analytical and simulation results obtained for both CNT and copper at 32nm and 22nm technology nodes. It is observed that, compared to the waveform of mutually coupled SWCNT bundles, that of copper interconnects shows wider crosstalk induced pulse at the far end of victim output in terms of time duration and higher positive peaks at both technology nodes. This is due to the comparatively higher R, L_S, C_C and lower C_g values of copper (see Tables 3.4 and 4.2).

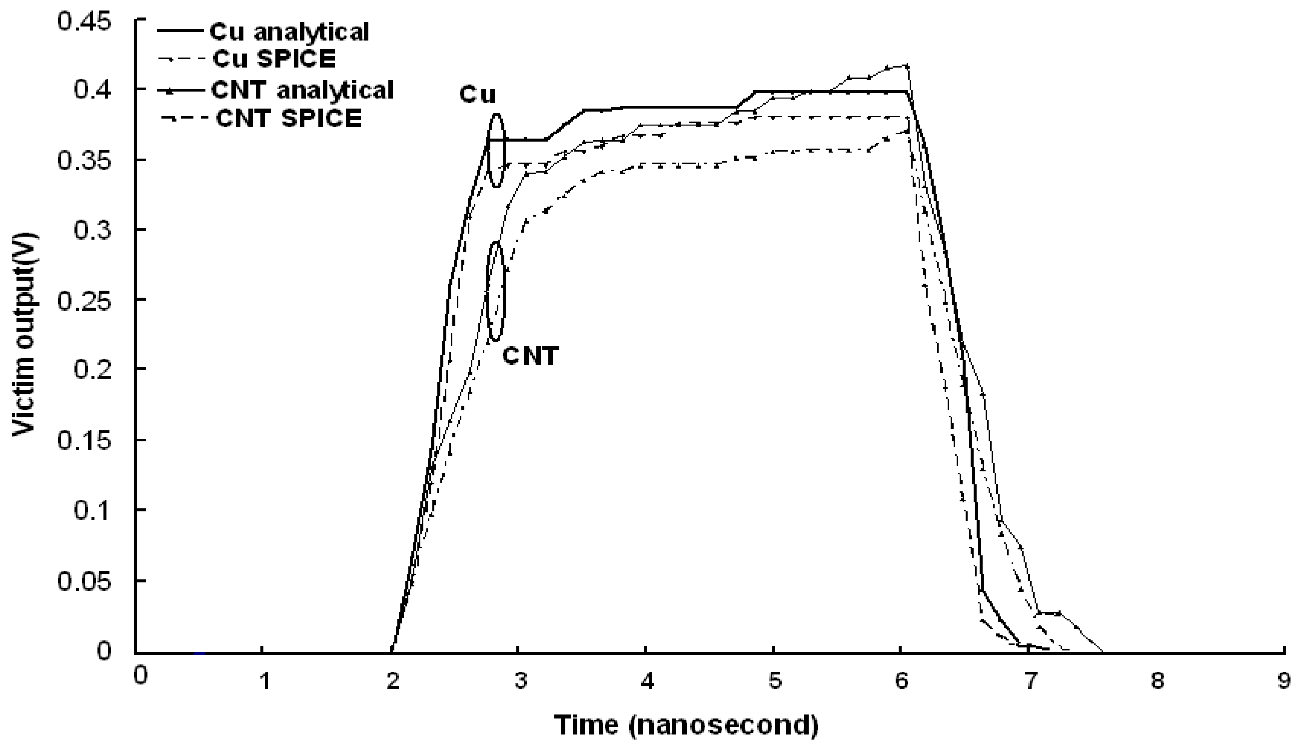


Figure 4.11 Analytical piecewise and simulated crosstalk-induced transient response of the victim output for the mutually coupled SWCNT bundle interconnects and the copper interconnects at 22nm.

4.3.2 Frequency Spectrum Analysis

Figs. 4.12 and 4.13 illustrate the frequency spectrum of the crosstalk-induced transient response waveforms of the victim output, at 32nm and 22nm technology nodes, shown in Figs. 4.10 and 4.11 respectively. The frequency components have been obtained using a script of Fast

Fourier transform (FFT) technique written in C language , with transition period of the input and output waveforms divided into 64(2^6) equal parts. The amplitudes of the frequency spectrum (y axis of Figs.4.12 and 4.13) are normalized by the amplitudes of input signal frequency; the frequencies (x axis of Figs.4.12 and 4.13) are normalized by the corresponding input signal frequency.

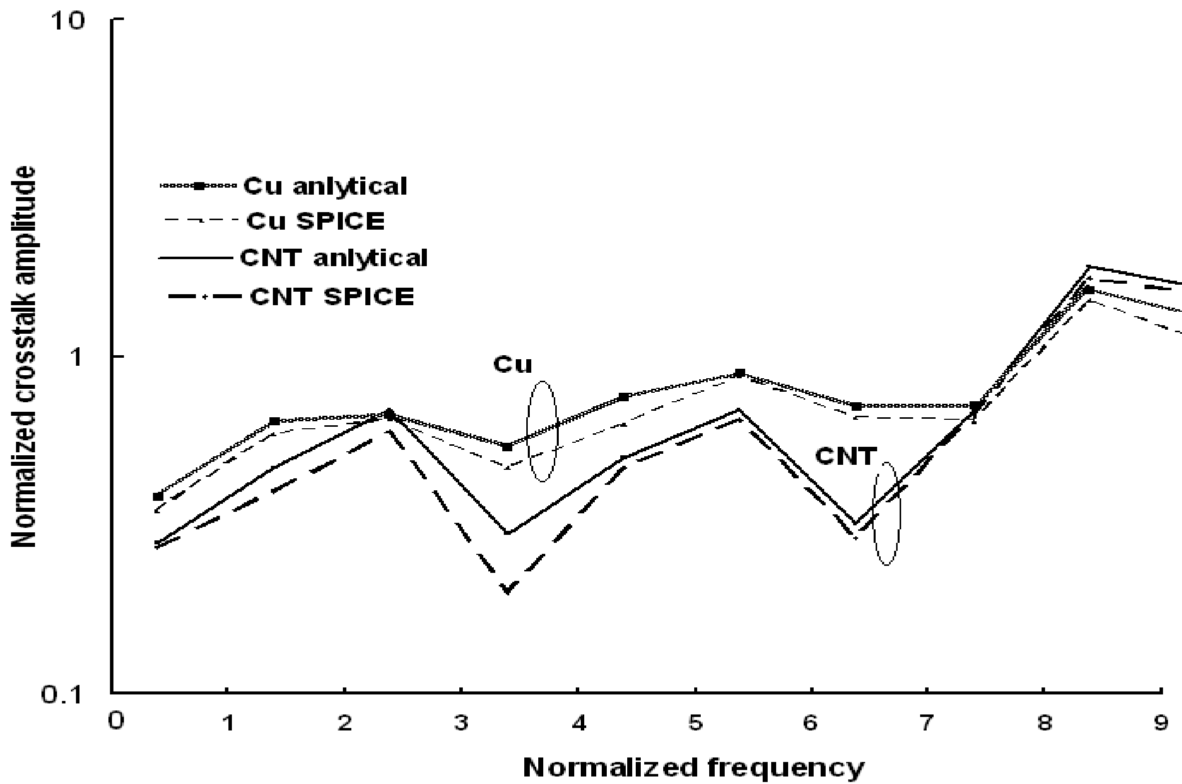


Figure 4.12 Variation of normalized crosstalk amplitude of frequency components for mutually coupled interconnects at the far end of the victim line with normalized signal frequency, at 32nm technology node.

Figs. 4.12 and 4.13 show that, for the smaller normalized frequency range, compared to copper interconnects, mutually coupled interconnects of SWCNT bundle have smaller amplitude levels of noise and filter more noise frequency components of victim output. In addition, for both technology nodes, for the higher frequency range, compared to mutually coupled interconnects of SWCNT bundle, copper interconnects have comparably suppressed frequency components. It

may also be noted that, compared to noise peaks at 32nm technology node, more noise peaks are observed at 22nm technology nodes.

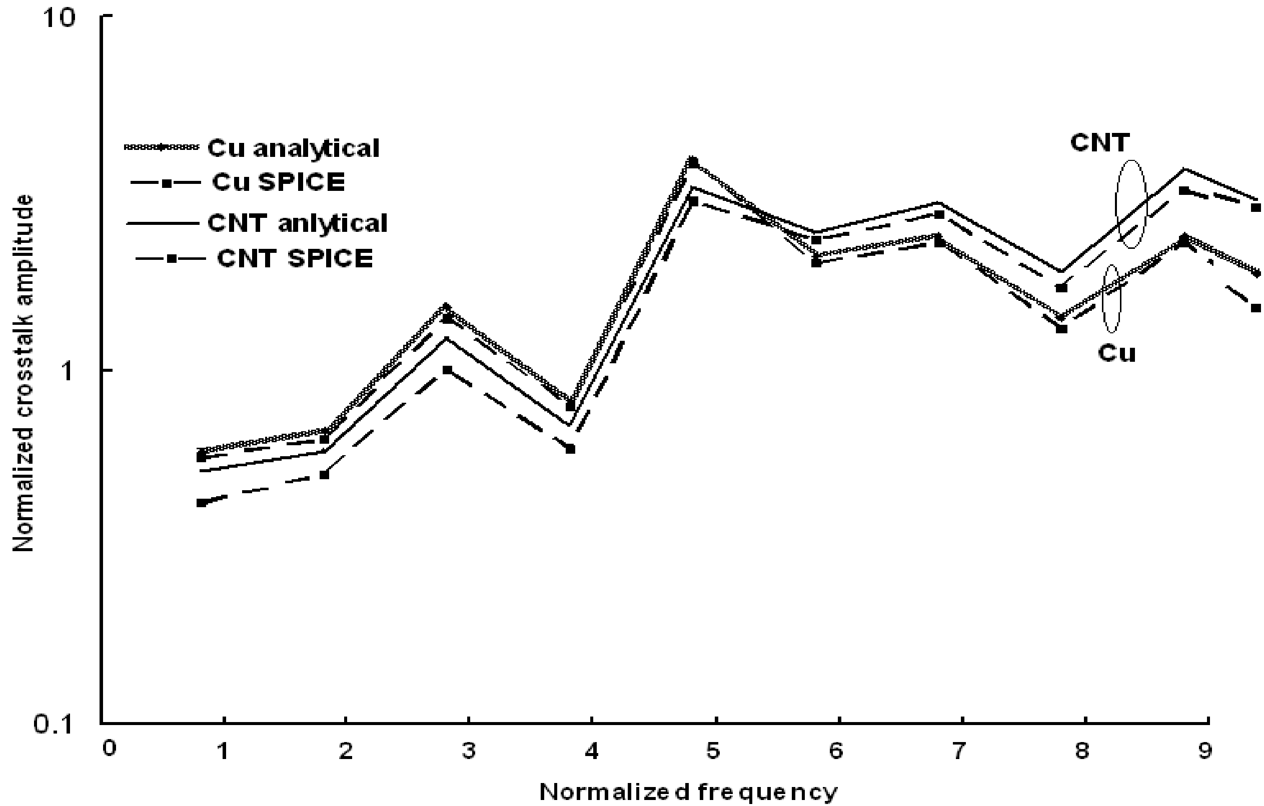


Figure 4.13 Variation of normalized crosstalk amplitude of frequency components for mutually coupled interconnects at the far end of the victim line with normalized signal frequency, at 22nm technology node.

4.4 CONCLUSION

In this chapter, (i) crosstalk induced, noise voltage waveform and its frequency spectrum, in capacitively coupled and mutually coupled interconnects of SWCNT bundle, at the far end of victim line, at 32nm and 22nm technology nodes respectively, (ii) a comparative study of crosstalk analysis between SWCNT bundle interconnects with coupling capacitance estimated (a) conventionally (conventional model) and (b) proposed model, (iii) diameter dependent

crosstalk induced noise voltage levels for the same technology nodes have been analyzed and results discussed.(iv) Further waveform of victim output have been analytically determined and compared with SPICE simulation results,(v) a similar analysis has been performed for copper interconnects and a comparison made between the results of these two analyses.

Based on these analyses it was observed that compared to the waveform of the proposed model of inter bundle capacitance based SWCNT bundle that of the conventional model shows higher positive and negative voltage peaks at the far end of victim line. Further it was observed that the piecewise analytical results replicate the SPICE waveforms very well. Results of the analyses also reveal that, compared to copper, crosstalk noise voltage levels in capacitively coupled SWCNT bundles, at the far end of victim line, are significantly low. It was seen that, for both technology nodes, the normalized crosstalk noise at the far end of victim line, initially decreases with increase in tube diameter and then increases beyond a critical value of tube diameter. These variations are simply reflections of the combined effect of the tube diameter (d) variations on tube resistance and capacitance.

In mutually coupled copper interconnects, width of noise waveform was wider compared to CNT at the far end of victim line. Further it was noted that, at both 32nm and 22nm technology nodes, compared to copper interconnects, capacitive coupled interconnects of SWCNT bundle filtered more noise frequency components. In contrast, for the same technology nodes, in mutually coupled interconnect of SWCNT bundles, compared to copper, comparable noise components in the higher frequency range were suppressed.

Chapter 5

INFLUENCE OF INTERCONNECT DIMENSIONS IN COUPLED CARBON NANOTUBE BUNDLES

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5.1 INTRODUCTION

Coupling noise (or crosstalk) between adjacent interconnects is also a primary concern for present and future generations of CMOS VLSI circuits. Coupling effects become more significant as the feature size is decreased to deep sub micrometer dimensions[15],[104],[106].One way to manage coupling noise is by controlling line parasitics, which in turn can be controlled by wire sizing and spacing.

In this chapter, we analyzes how crosstalk noise voltage (functional crosstalk noise) in capacitively coupled Single Walled Carbon Nanotube (SWCNT) bundle interconnects, at the far-end of victim line, is controlled under the influence of interconnect dimensions such as space(s) and width(w) for fixed pitch, using proposed inter coupling capacitive model. A similar analysis is performed for copper based interconnect and comparison is made with result obtained for CNT based interconnect at 22nm technology. The SPICE simulation results reveal that the crosstalk noise voltage level at the far end of victim line in CNT bundles is significantly low compared to that in conventional metal(copper) conductors in three different cases to keep the pitch ($s+w$) fixed but varying the value of interconnect spacing and width.

5.2 IMPEDANCE ANALYSIS OF CNT INTERCONNECTS

It can be seen from Eqs.(3.24),(3.28), (3.31) and (4.37), the impedance parameters of bundle SWCNT are the functions of interconnect dimensions.

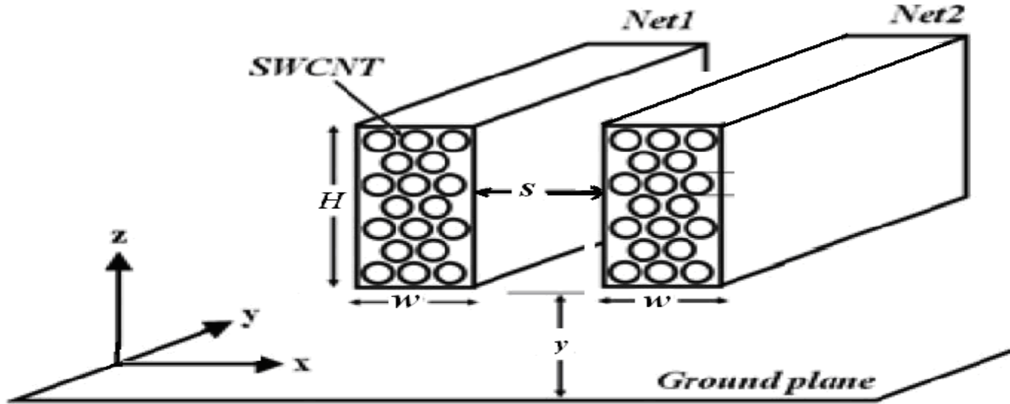

Figure 5.1 Schematic of the parallel interconnects structure using SWCNT bundle. *H* is thickness, *w* is the width of SWCNT bundle interconnect and y is the distance between SWCNT bundle interconnect and ground plane.

The parallel interconnects structure constituted with SWCNT bundles are shown in Fig.5.1. The equivalent circuit impedance parameters of CNT are calculated from Eqs. (3.15)–(3.31) and for copper from Eqns.(3.32)-(3.34) and Eq.(4.38), under three different cases viz.,case-1,case-2 and case-3.

Case-1: Space (s) between two interconnect equals to $s + w/2 = (3w)/2$=48nm and Width (w) = $w - w/2 = w/2$=16nm.

Case-2: Space (s) between two interconnect equals to 32nm and Width (w)=32nm.

Case-3: Space (s) between two interconnect equals to $s - (w/2) = w/2$=16nm and Width (w) =

$w + (w/2) = 3w/2$=48nm. In all three cases pitch ($s + w$) is kept fixed at 64nm but interconnect dimensions are varied.

Data given in Table-3.1 are used for the calculations. Fig.5.2 exemplifies how the resistance varies with interconnect length for three different dimensions. It can be seen that an interconnect of larger width in case-3, when used as interconnect will have smaller line resistance for both CNT and copper. It shows that in various length and width of interconnects the resistance of bundle SWCNT is several times lower than that of copper based interconnects. Variations in interconnect resistance has the effect on far end voltage magnitude of victim and time durations [15], [104]. Fig.5.3 shows the variation of total interconnect effective capacitance (equivalent ground capacitance) as a function of interconnect length for different adjacent interconnects dimension. Interconnect capacitance increases with decrease in space between adjacent interconnects and decreases with scaled down dimensions.

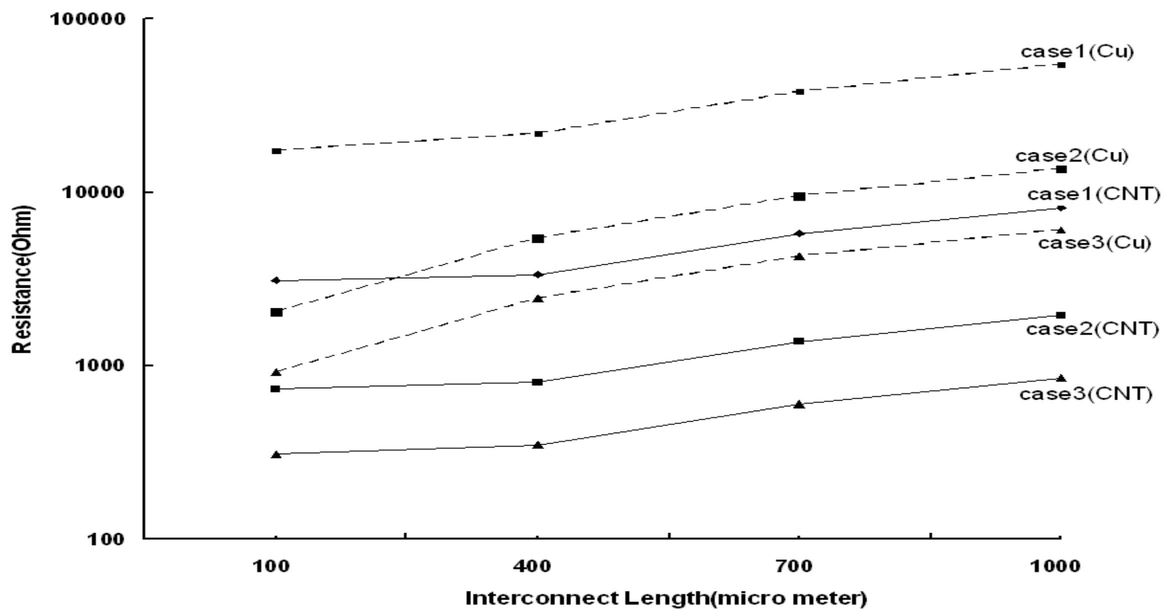

Figure 5.2 Variation of resistance as a function of interconnect length at different dimension between adjacent interconnects for 22nm technology.

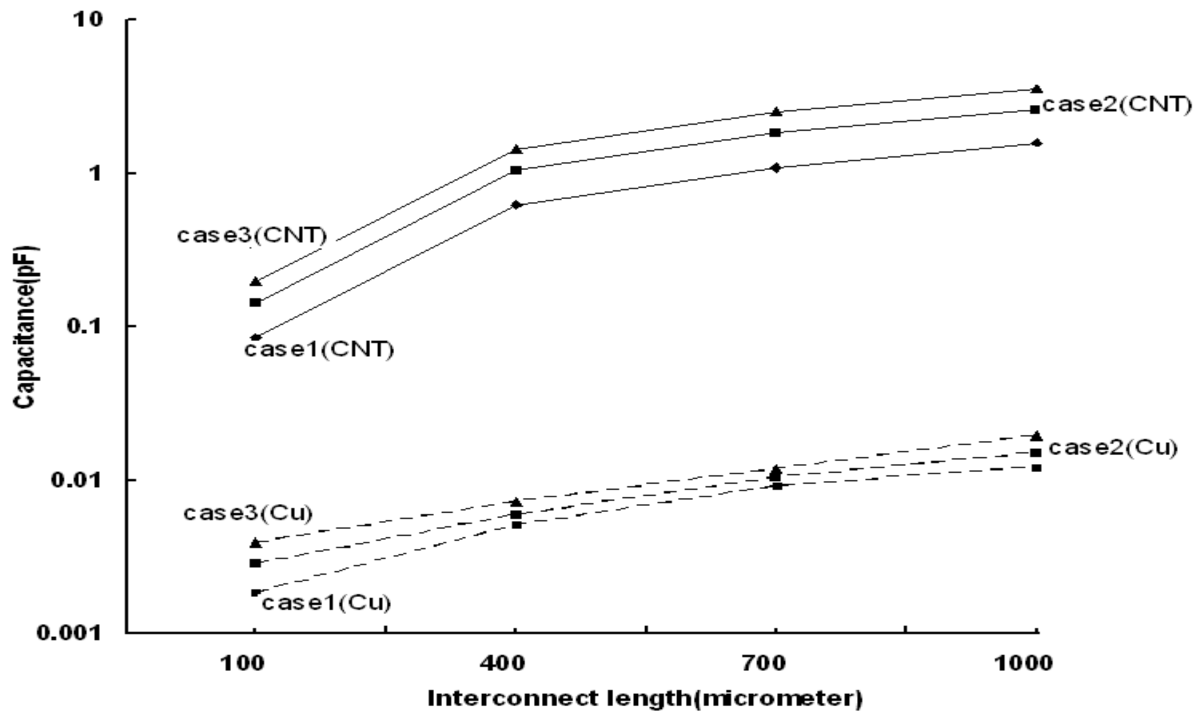

Figure 5.3 Variation of capacitance as a function of interconnect length at different dimension between adjacent interconnects for 22nm technology.

It is observed that a bundle composed of tubes has larger effective capacitance in all three cases compared to the copper based interconnect. Since, the cylindrical surface area of the CNTs at the edge of a bundle exposed to the surrounding interconnects is larger than the corresponding surface area for a copper (Cu) interconnect with straight edges [62]. Therefore SWCNT bundle has larger effective capacitance as compared to copper of equivalent dimension. Fig.5.4 illustrates the dependence of inductance on interconnect dimensions as well as length. Inductance increases with increase in space between interconnects and decreases with increase in width of interconnects in all three cases.

Kinetic inductance L_K is excluded from the calculations of SWCNT bundle for lengths L >> λ (mean free path of CNT)[118].Therefore, it has been observed that a bundle composed of

tubes has smaller inductance in all three cases as compared to copper . Results are obtained in Figs.5.2, 5.3 and 5.4 indicate that a densely packed interconnects have larger capacitance but reverse is true for inductance and resistance. In capacitively coupled interconnects, as self inductance is increased, the difference between even and odd mode time of flight increases [104]. The increase in time of flight with self inductance indicates the desirable effect on crosstalk induced noise voltage levels at far end of victim line.

Fig.5.5 shows how inter coupling capacitance between adjacent interconnects vary as a function of interconnect length for three different dimensions. Inter coupling capacitance between adjacent interconnects of SWCNT bundle is extracted from the proposed model encapsulated in Eq.(4.37). Coupling capacitance increases with decrease in space between adjacent interconnects and decreases with scaled down the width of interconnects. Coupling capacitance increases significantly with increase in length of interconnect. Results also reveal that copper based interconnect has higher value of coupling capacitance than a CNT bundle counterpart in three different cases.

These variations in coupling capacitance, using scaling of interconnect dimensions, have the effect of voltage magnitude at far end of victim line. The conventional model based inter coupling capacitance [6],[132],[133] between adjacent interconnects of SWCNT bundle has been also calculated under three different cases of interconnect dimensions. Comparison is made with result obtained from the proposed model under same cases and shown in Table 5.1, in which coupling capacitance (C_C) value of the proposed model is less compared to conventional. It is of the order of few fF.

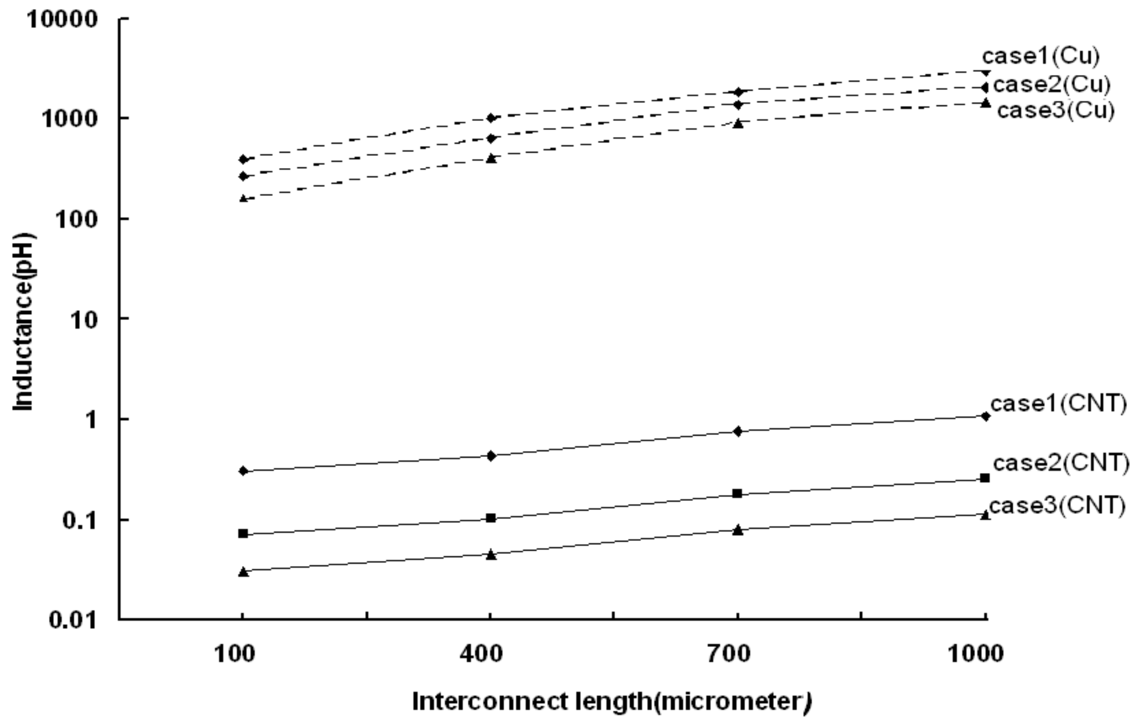

Figure5.4 Variation of Inductance as a function of interconnect length at different dimension between adjacent interconnects for 22nm technology.

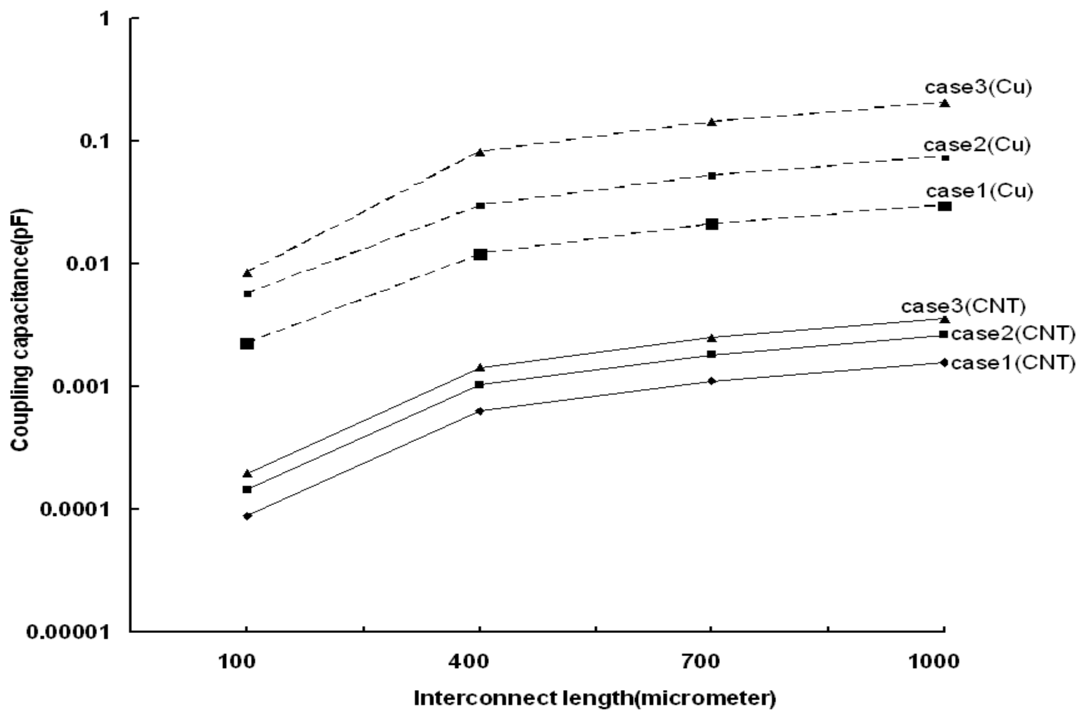

Figure 5.5 Variation of coupling capacitance as a function of interconnect length at different dimension between adjacent interconnects.

5.3 CROSSTALK ANALYSIS IN CAPACITIVELY COUPLED INTERCONNECTS OF SWCNT BUNDLE

In this sub-section, we study the effect of changing the dimension of capacitively coupled interconnects on coupled noise (functional crosstalk noise) voltage at the far-end of victim line. In order to analyze crosstalk noise voltage in terms of voltage spikes on adjacent nets, we consider capacitively coupled distributed interconnects circuit [86] as shown in Fig.5.6. All the signal wires are driven by a CMOS driver at 22nm technology [125] with clock speed of 0.1 GHz, V_{dd}=0.7V, rise time=1ns, fall time=1ns and terminated with capacitive load of 0.14fF [77]. FO4 (fanout of four) is consider in this analysis [77]. For calculation and simulation purpose for interconnect of SWCNT bundle, the data shown in Table 3.1 have been used. A densely packed SWCNT bundle of diameter 1nm is considered. Simulation is also carried out for coupled interconnects of copper with same clock speed and technology node.

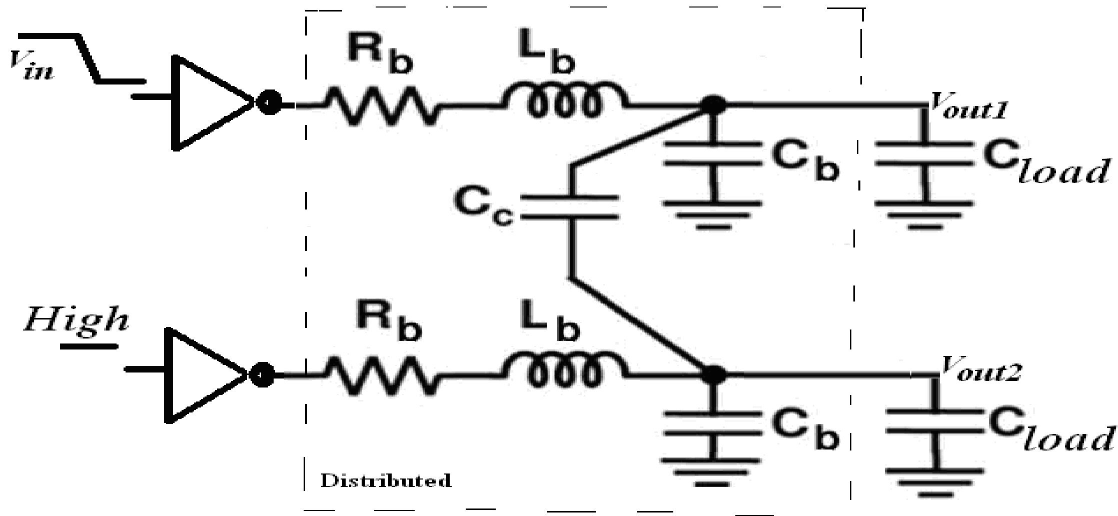

Figure 5.6 CMOS gate driven capacitively coupled interconnects [86]. R_b is the SWCNT bundle resistance, L_b is the SWCNT bundle inductance, C_b is the SWCNT bundle capacitance and C_{load} is the load capacitance.

Circuit parameters and coupling capacitance of coupled interconnect of copper are calculated by appropriate use of the expressions from Eqs.(3.32)-(3.34) and Eq.(3.38) and data obtained from Table 3.1. For overshoot and undershoot analysis, the victim net (i.e. the crosstalk affected net) is kept fixed at logic 1 and the aggressor net (i.e. the net that cause crosstalk on victim) is switched from logic 1→0. The aggressor line CMOS driver has pMOS width (W_p) double than nMOS width (W_n) while the victim line is grounded at the input through a linear region equivalent driver resistance and the size of CMOS driver nMOS is set to be 40 times the minimum size of transistor. In this analysis, the width (w) and thickness (H) of interconnect are assumed to be 32nm and 96 nm respectively, and space(s) between two interconnect is assumed to be 32nm.

A comparative study of crosstalk analysis between (i) SWCNT bundle interconnects with coupling capacitance estimated using improved model, and (ii) conventional model, is reported and shown in Table 5.1.The value of conventional model of inter coupling capacitance is calculated from Eq.(4.38) under three different cases. It can be seen that the propose model provides lower value of coupled noise voltage as compared to conventional counterpart in all three cases. Furthermore, the table also provides an account of crosstalk noise voltage corresponding to three different cases of copper coupled interconnects. Fig.5.7 illustrates the dependence of normalized crosstalk noise voltage on interconnect dimensions at the far end of victim line for different interconnect lengths.

Table 5.1 Comparison between crosstalk noise voltage using conventional Cc and Proposed Cc. Length of interconnect=1mm,C_{Load}=0.14fF,Technology:22nm

Interconnect dimensions	**Inter coupling capacitance (C_C) between adjacent SWCNT bundles**		**Crosstalk noise voltage at the far end victim in coupled SWCNT bundle interconnects**		**Crosstalk induced noise voltage (copper)**
	Conventional	Proposed model	Conventional	Proposed model	
Case-1	29.9fF	1.569fF	3.4mV	0.334mV	30.2mV
Case-2	75.173fF	2.597fF	3.01mV	0.331mV	23.63mV
Case-3	204.395fF	3.575fF	5.96mV	0.363mV	32.56mV

The normalized crosstalk noise voltage at the far end of victim line, defined as the ratio between the terminal voltage at victim output and the input voltage (V_{out2}/V_{in}). It is observed that, with increased spacing for both copper and CNT, noise voltage peaks due to capacitive coupling reduction in case-1 as compared to case-3.This is due to the fact that with increased spacing, the coupling capacitance reduces rapidly. On the other hand, case-2 has lower crosstalk noise voltage levels for different interconnect lengths as compared to case-1 due to the reduction in line width by a factor of $w/2$. Now consider case-3 where crosstalk noise voltage levels (in form of peaks) are more for different interconnect lengths as compared to case-1 and case-2 due to low reactance path. In addition, as compared to SWCNT bundle interconnect for all three cases, copper has higher coupled noise voltage levels due to larger value of coupling capacitance as shown in Fig.5.5.

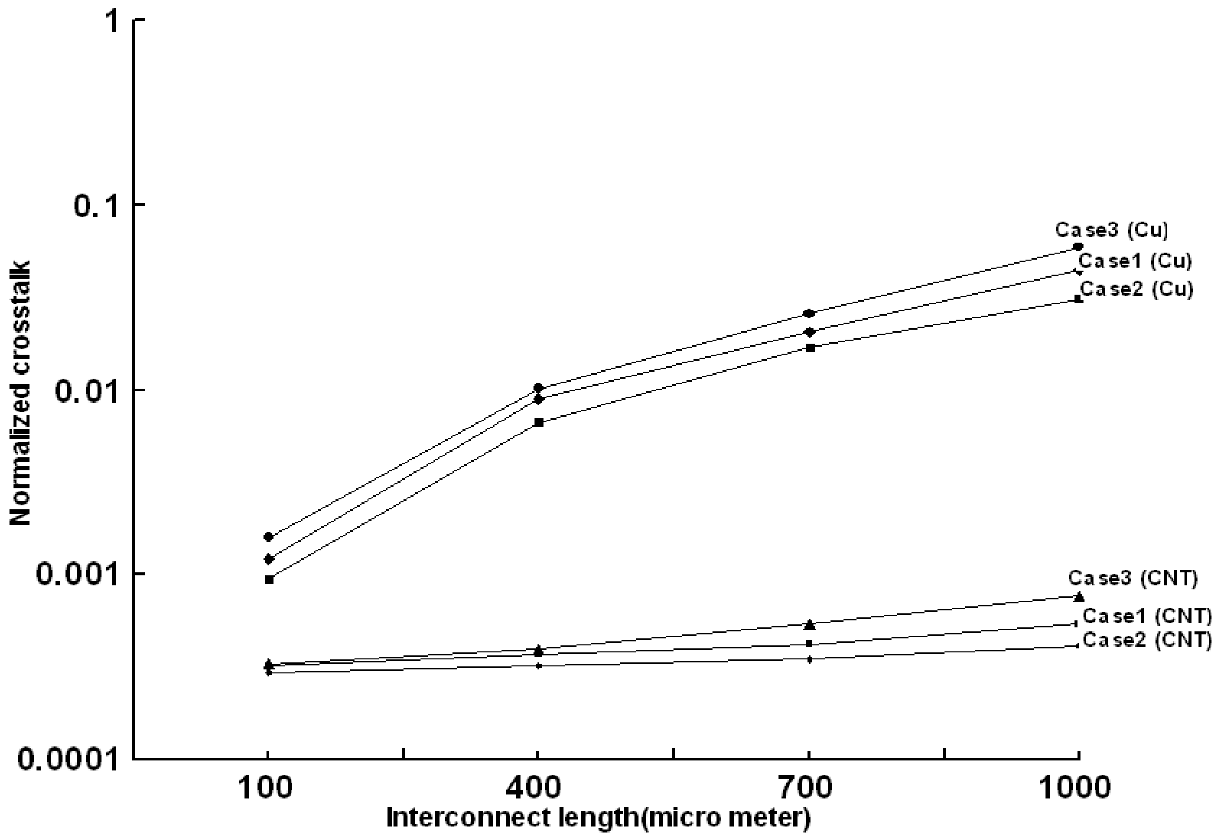

Figure 5.7 Normalized crosstalk noise voltage as a function of length for different interconnect dimensions.

Scaling of interconnect dimensions has a significant effect on both interconnect resistance, capacitance (ground capacitance) and self inductance as shown in Figs.5.8, 5.9 and 5.10. The effect of line resistance on noise peak voltages is shown in Fig.5.8 for both CNT and copper. It can be seen that positive coupled peak voltage (noise peak voltage) is a function of line resistance. Results are obtained by sweeping Interconnect resistance. Resistance is normalized by their respective values for 1mm length of interconnect.

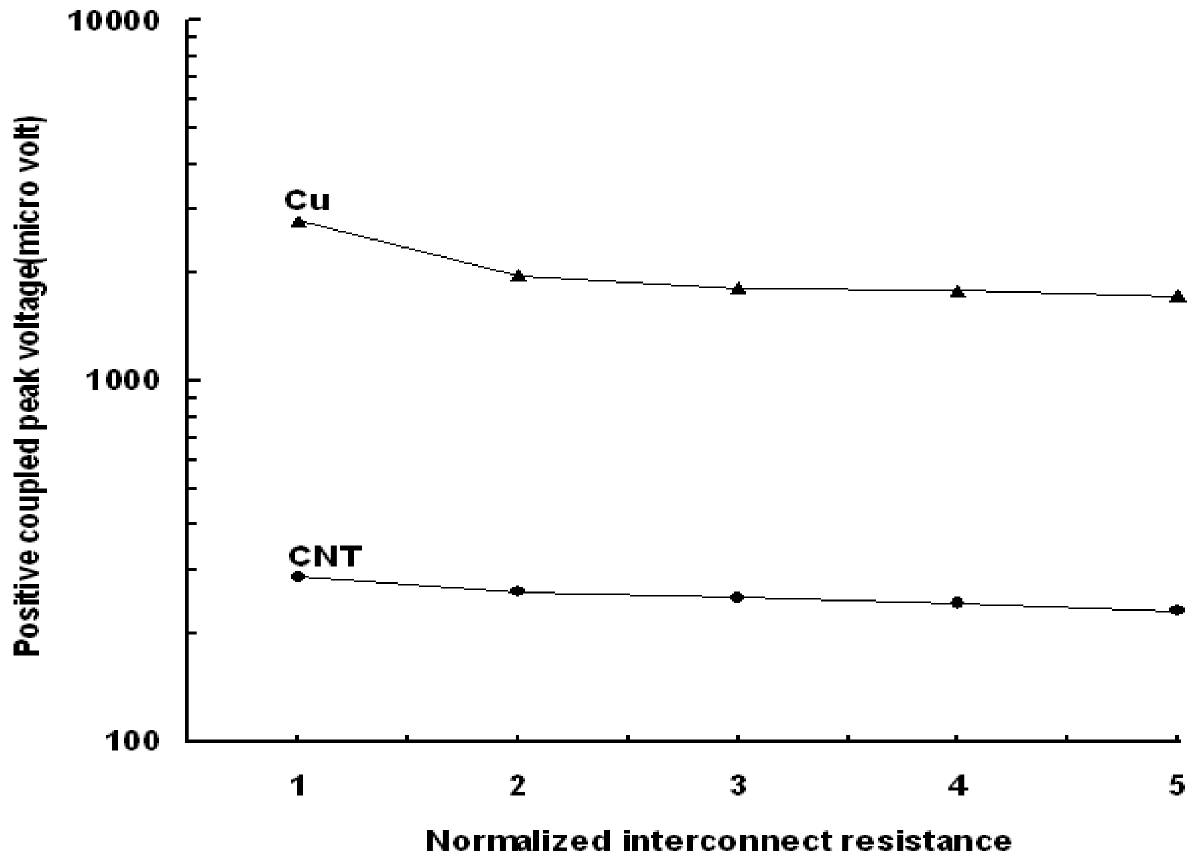

Figure 5.8 Positive coupled peak voltage as a function of normalized interconnect resistance.

The result resembles that as line resistance increases, the noise peak reduces. This is due to the fact that, with resistance, the voltage steps traveling along the line undergo attenuation and dispersion. Hence, the voltage steps arriving at far end of the line are smaller and have larger time duration. These results also illustrate that SWCNT bundle interconnects have lower positive peaks compared to copper based interconnect due to small value of coupling capacitance.

Fig.5.9 shows absolute positive coupled peak voltage as a function of self inductance at the far end of victim line. In this setup, we consider 1mm long interconnects with same width and spacing between interconnects of 32nm. Instead of using extracted self inductance values, it is varied from 1 to 5 normalized ranges. Self inductance is normalized by their respective values

for 1mm length of interconnect. It is observed that coupled peak voltage increases with an increase in self inductance. This is due to the fact that, as self inductance is increased, the even and odd mode characteristic impedances increase, causing positive coupled peak voltage to rise significantly. For capacitive coupling, characteristic impedance (Z_0) for even and odd mode of communication are given by Eqs.(5.1) and (5.2) [104]:

$$Z_{0e} = \sqrt{\frac{L_S}{C_g}} \quad (5.1),$$

$$Z_{00} = \sqrt{\frac{L_S}{C_g + 2C_C}} \quad (5.2),$$

where Z_{0e} and Z_{0o} are the characteristic impedance of even and odd mode transmission, L_S is the self inductance, C_g is the ground capacitance of interconnect and C_C is the coupling capacitance. In addition, as compared to coupled SWCNT bundle, copper coupled interconnects have higher positive coupled peaks.

Fig.5.10 shows the dependence of noise peak voltage on interconnect capacitance (ground capacitance). A similar setup is used as in Fig.5.9. For copper and SWCNT bundle, results are obtained by sweeping interconnect capacitance from 1 to 5 normalized ranges instead of extracting capacitance values from Eqs.(3.28) and (3.34) respectively. Capacitance is normalized by their respective values for 1mm length of interconnect.

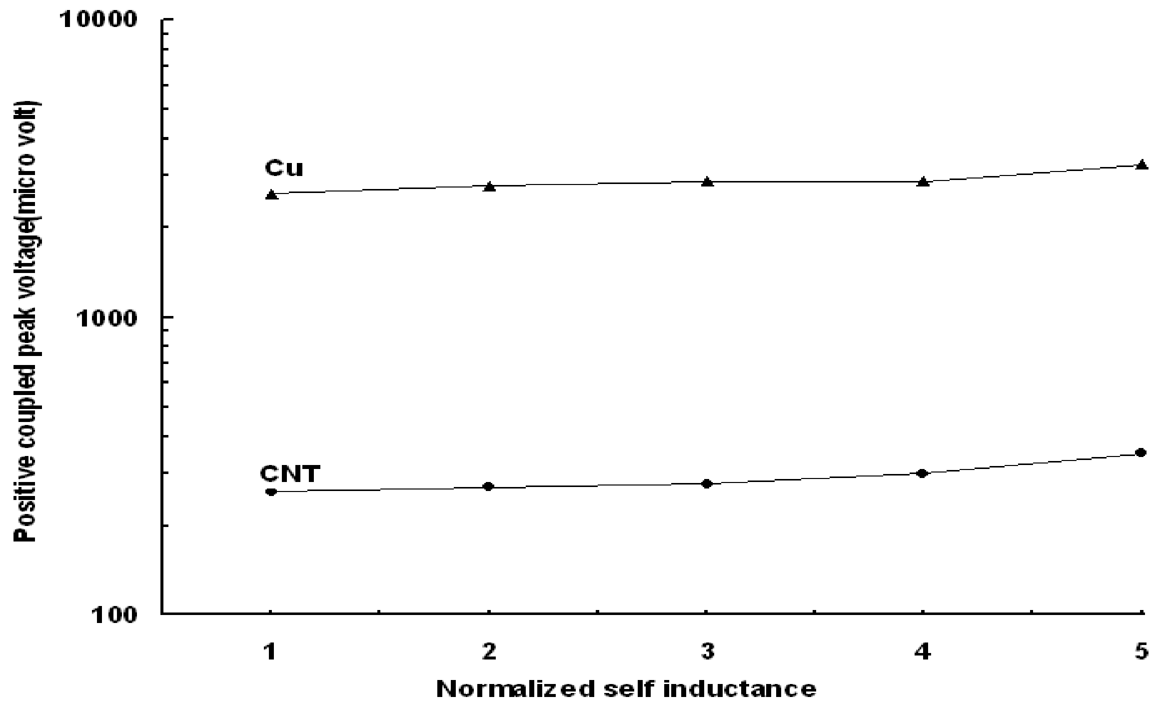

Figure 5.9 Positive coupled peak voltage as a function of normalized self inductance.

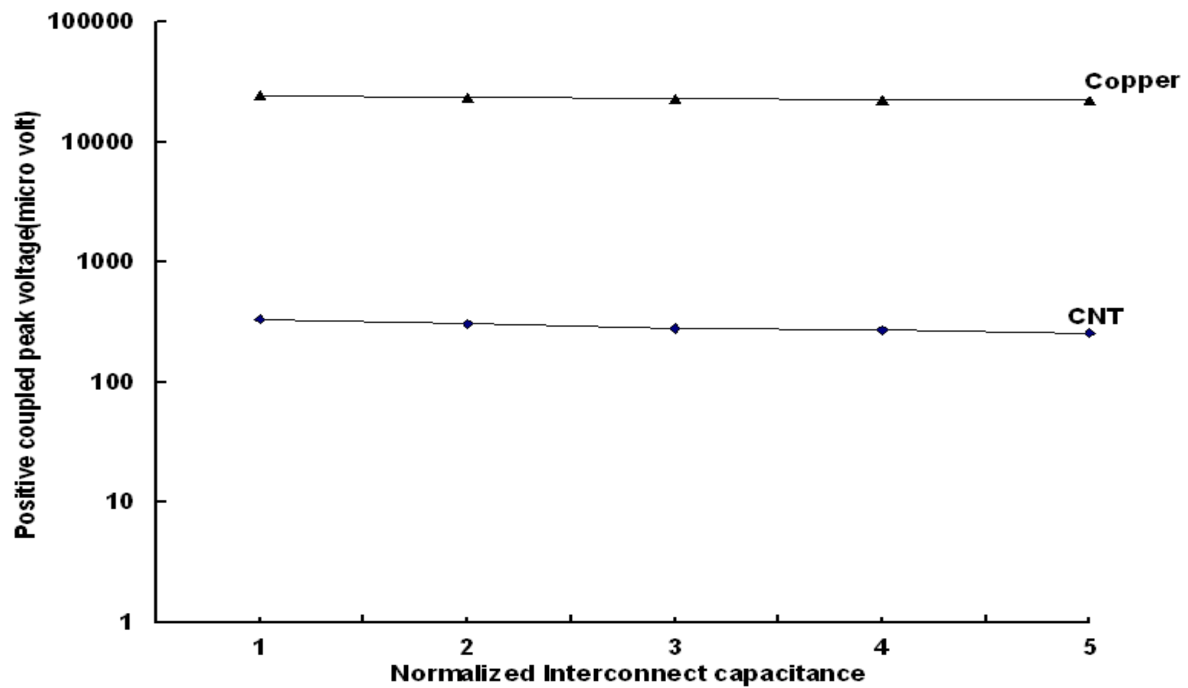

Figure 5.10 Positive coupled peak voltage as a function of normalized interconnect capacitance.

The result resembles that as interconnect capacitance increases, the noise peak in terms of voltage reduces. This is due to the fact that with increased interconnect capacitance, both even and odd mode characteristic impedances reduces. This causes fall in coupled peak voltage. It is also observed that coupled SWCNT bundle interconnects have lowered positive peaks as compared to copper based interconnects for all normalized range of capacitances due to the lower value of coupling capacitance (Fig.5.5). Thus, scaling of interconnect dimensions is to be handled carefully in design of interconnects for future VLSI applications.

5.4 CONCLUSION

The control of crosstalk induced noise voltage (functional crosstalk noise) in capacitively coupled interconnects of SWCNT bundle, at the far-end of victim line, for fixed pitch and varying interconnect dimensions under three different cases, for the proposed inter coupling capacitance model and the conventional model, at 22nm technology node, have been analyzed. It has been observed that the proposed model of coupling capacitance provides better reduction in crosstalk noise voltage compared to conventional counterpart in all three different cases.

A similar analysis performed for copper interconnects showed that, compared to coupled interconnects of SWCNT bundle, copper interconnects has higher coupled noise voltage levels due to larger coupling capacitance (see Fig.5.5).

Furthermore, a comparative analysis of the effect of interconnect resistance, self inductance and ground capacitance of interconnect on positive coupled peaks at the far end of victim line in capacitively coupled interconnects of SWCNT bundle and copper has been studied. It is observed that, with increase in line resistance or ground capacitance, while the noise voltage peak reduces for both CNT and copper, there are more noise voltage peaks in the copper.

Also as the self inductance increases, in copper interconnects the victim line gets more prone to crosstalk noise. It has also been noted that with suitably optimized interconnect dimensions in deep submicron; the coupled noise voltage at the far end of victim line can be controlled quite well.

Chapter 6

TEMPERATURE DEPENDENT CROSSTALK ANALYSIS IN COUPLED CARBON NANOTUBE BUNDLE INTERCONNECTS

6.1 INTRODUCTION

Thermal issues have now emerged as a major challenging factor in the possible usage of nanotubes for designing high performance integrated circuits, due to the present trends in device scaling. Integrated circuits often operate at temperatures much greater than room temperature. So, if SWCNTs are to be employed in integrated circuit applications, it is critical to understand how their electrical characteristics will vary at temperatures greater than room temperature. A few researchers have investigated the performance of SWCNTs within integrated circuits from a thermal point of view [93]-[95], [134],[135]. Their analyses show that the low-bias resistance of micron scale SWCNTs is affected by optical phonon absorption (a scattering mechanism, previously neglected) at temperatures above 250K. Pop et al. [136] provide extrapolated values of thermal conductivity of single nanotubes, in the high-bias regime, at temperatures ranging from 300 K to 800 K.

However, in such a regime, self heating occurs and interaction with optical phonons dominates the transport characteristics. In the present study, simulations have been performed in the low-bias regime, where CNTs show perfect ohmic behavior and are compatible with VLSI interconnect applications. In recent times, few researchers have studied the effect of crosstalk in CNT interconnects [1]-[13,[137] as discussed in chapter1 and 2. However, Several

other researchers have investigated the applicability of CNT as VLSI interconnect [17]-[30],[138]-[143].

This chapter focuses on functional crosstalk noise voltage. Here the temperature dependent, crosstalk induced, noise voltage waveform and its frequency spectrum, in capacitively coupled Single Walled Carbon Nanotube (SWCNT) bundle interconnects, at the far end of victim line, have been analyzed first time, at 22nm technology node. A similar analysis is performed for copper interconnects and a comparison is made between the results of these two analyses. The SPICE simulation results reveal that at temperature variations ranging from 300K to 500K, compared to conventional metal (copper) conductors, crosstalk noise voltage levels in CNT, at the far end of victim line, are significantly low. Simulated results further reveal that, with rise in interconnect temperatures, compared to copper interconnects, coupled interconnects of SWCNT bundle filter more noise frequency components.

In this study, an improved inter bundle capacitance values are estimated as discussed in chapter 4, using validated empirical relationships for CNT interconnects [118] and simulated values of crosstalk-induced voltage noise of this novel interconnects obtained, with a suitable crosstalk analysis, over a temperature range from 300 K to 500K.

6.2TEMPERATURE -DEPENDENT CIRCUIT PARAMETERS OF SWCNT BUNDLE AND COPPER BASED INTERCONNECT

The temperature dependence of the low bias resistance is obtained through temperature dependence of the electron scattering mean free paths (MFPs) with acoustic (AC) and optical phonons (OP) [93]-[95],[134]. The temperature dependent resistance of SWCNT is given as:

$$R_{CNT} = \left[\frac{h}{4e^2}\right]\left[\frac{\mathrm{L}+\lambda(T)}{\lambda(T)}\right] + R_C \quad if\ \mathrm{L} > \lambda \qquad (5.1),$$

where $\lambda\ (T)$ is the temperature-dependent MFP. This includes electron scattering both by OP emission and by absorption. Here $\lambda\ (T)$ is given as:

$$\lambda(T) = \left[\frac{T}{300.\lambda_{ac,300}} + \left(\lambda_{OP,300}\left(\frac{N_{OP}(300)+1}{N_{OP}(T)}\right)\right)^{-1} + (\lambda_{OPems})^{-1}\right]^{-1} \quad (5.2),$$

where $\lambda_{ac,300} \approx 1600nm$ is the AC scattering length at 300 K,

$$N_{OP}(300) = \left(e^{\frac{0.18eV}{0.026eV}} - 1\right)^{-1} \quad (5.3),$$

$$N_{OP}(T) = \left(e^{\frac{\hbar.\omega_{OP}}{K_B.T}} - 1\right)^{-1} \quad (5.4),$$

$$\lambda_{OPems}(T) = \left[\frac{1}{\lambda_{OPems}^{fd}(T)} + \frac{1}{\lambda_{OPems}^{abs}(T)}\right]^{-1} \quad (5.5),$$

$$\lambda_{OPems}^{fd}(T) = \left(\frac{\hbar.\omega_{OP}}{e.V_{dd}}.l\right) + \left(\frac{N_{OP}(300)+1}{N_{OP}(T)+1}\right).\lambda_{OP,300} \quad (5.6),$$

$$\lambda_{OPems}^{abs}(T) = \lambda_{OPabs}(T) + \left(\frac{N_{OP}(300)+1}{N_{OP}(T)+1}\right).\lambda_{OP,300} \quad (5.7),$$

and $\lambda_{OPabs}(T) = \lambda_{OP,300}\left(\frac{N_{OP}(300)+1}{N_{OP}(T)}\right)$ (5.8)

Here $\lambda_{OPems}^{abs}(T)$ is the OP emission MFP after an absorption, $\lambda_{OPems}^{fd}(T)$ is the former OP emission MFP event and $\lambda_{OP,300} \approx 15$ nm is the spontaneous optical emission length at 300 K.R_C is the contact resistance, due to imperfect contact condition between CNT and other materials, this resistance can range from zero to hundreds of kilo-ohms for different growth processes [124]. Here, for the sake of proper calculation of SWCNT resistance, R_C value is assumed to be 100 kilo-ohms.

On the basis of Luttinger Liquid Theory [119], the resistances of a bundle is given by Eq.(3.24). A densely packed bundle of metallic SWCNT has been considered as discussed in chapter 5 (Fig 5.2). For this densely packed bundle, the inter-CNT distance (x) is equivalent to tube diameter (d=1nm).The temperature dependent effective resistance of a SWCNT bundle of length L>λ is derived from Eqs.(3.24) and (5.1), and given as:

$$R_{CNT}(Bundle) = \frac{\left[\frac{h}{4e^2}\right]\left[\frac{L+\lambda(T)}{\lambda(T)}\right]+R_C}{N_{CNT}} \qquad if\ L > \lambda \tag{5.9}$$

where N_{CNT} ,the total number of SWCNT tubes in the bundle as discussed in the chapter 3.

Luttinger Liquid Theory based equivalent circuit for SWCNT [119] is well accepted and a very little of experimental validation of this equivalent circuit is available in the literature. A piece wise linear model for length and bias dependence of resistance is derived [121] from the original model of Burke [119]. The results of the piece wise linear model compares with experimental data [124].

Additionally, in order to estimate the performance of copper interconnects accurately under temperature variation, the following temperature-dependent resistance formula can be used as:

$$R(T) = R_0(1 + \zeta(T - T_0)) \tag{5.10}$$

Here ζ is the temperature coefficient of resistance measured at room temperature T_0=300K. For copper, the accepted value of this temperature coefficient is ζ=0.0039K^{-1} [144]. Resistance at room temperature is defined as $R_0 = \rho_0 \cdot (L/A)$, where ρ_0 is the resistivity of copper at room temperature. Eqs. (5.9) and (5.10) show that the effective low bias resistances of the SWCNT bundle and copper are functions of temperature.

6.3 IMPEDANCE ANALYSIS

It can be seen from Eqs. (5.9) and (5.10), the effective low bias resistance of the SWCNT bundle and copper based interconnect are functions of temperature. The other circuit parameters SWCNT bundle viz., equivalent bundle capacitance and inductance can be calculated from Eqs.(3.28) and (3.31). In case of copper; circuit parameters viz. equivalent inductance and capacitance can be calculated by appropriate use of the expressions from Eqs.(3.33) and (3.34).Data given in Table-3.1 are used for the calculations of CNT and copper parameters.

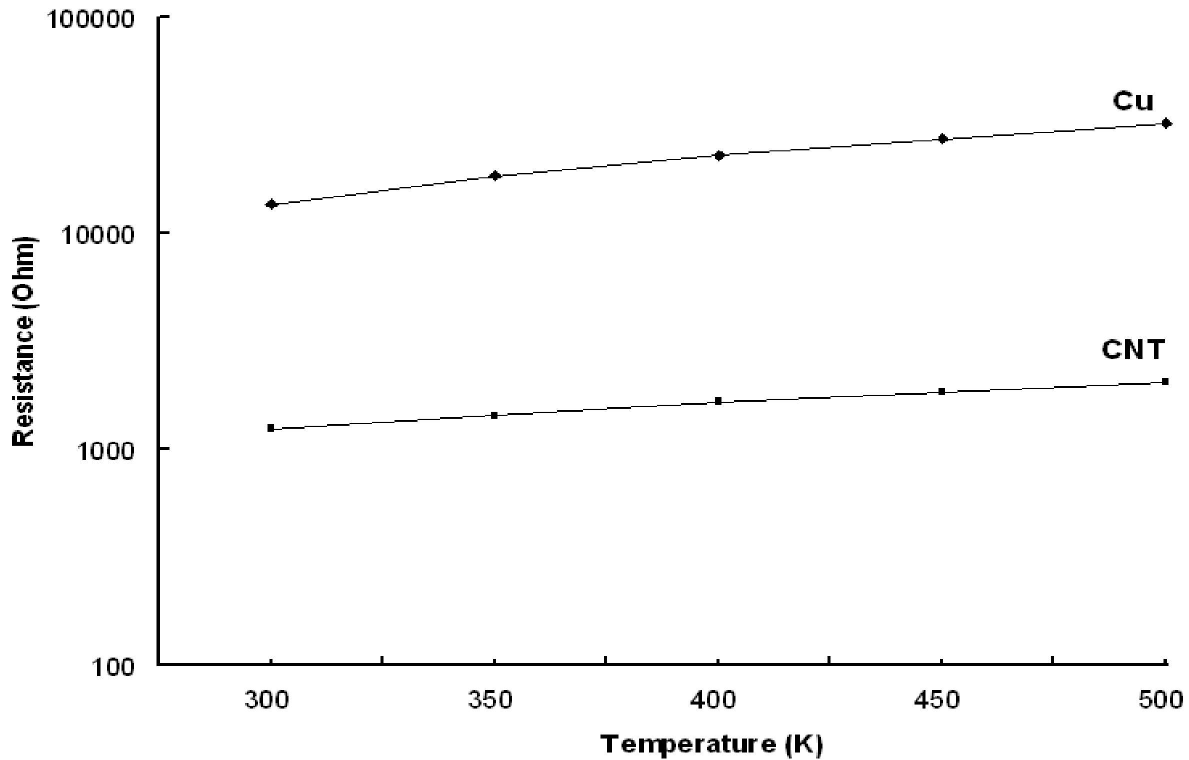

Figure 6.1 Resistance of SWCNT bundle and copper interconnects as a function of temperature.

In Fig.6.1, the variation of equivalent resistance of long (1mm) interconnects with temperature is exhibited at 22nm technology node. It is seen that, in case of such long interconnects, the low bias resistance of SWCNT bundle increases with a rise in temperature.

Pop et al.[93] have reported similar observations for SWCNT interconnect and suggested that this was due to the dominance of OP absorption above room temperature.

We further note from this Figure that, although the variation of low bias resistance of copper interconnects with temperature follows a similar pattern, this variation here is more as compared to that of SWCNT bundle. Variation of resistance with temperature, as is exhibited in Fig. 6.1, indicates the desirable effect of reducing voltage noise level and time duration of output voltage[15],[104]. It is also observed from Fig.5.1 that the value of resistance of SWCNT bundle, at any specific temperature, in the range 300 K to 500 K, is always several times lower than that of copper based interconnect. This suggests that, in the context of reducing noise voltage levels of integrated circuits, compared to copper interconnects, SWCNT interconnects are more promising.

6.4 TEMPERATURE DEPENDENT CROSSTALK ANALYSIS

In this Section, a comparative study of crosstalk analysis between (i) SWCNT bundle interconnects with coupling capacitance estimated using improved model, and (ii) copper interconnects, is reported. Further, a detailed investigation of temperature-dependent crosstalk analyses as also the frequency spectrum analyses of the temperature dependent transient responses at the far end of victim output, for the proposed model and copper interconnects was performed and the ensuing results and inferences compared. To analyze the crosstalk voltage noise, a capacitively coupled *RLC* distributed interconnects circuit has been considered as discussed in chapter 5 (Fig.5.6). All the signal wires are driven by a CMOS driver at 22nm technology node [125] with clock speed of 0.1 GHz, V_{dd}=0.7V, rise time=1ns, fall time=1ns and terminated with capacitive load of 0.14fF [77]. A densely packed metallic SWCNT bundle with tube diameter of 1nm has been considered.

For crosstalk analysis, the victim net (i.e. the crosstalk affected net) is kept fixed at logic 1 and the aggressor net (i.e. the net that cause crosstalk on victim) is switched from logic 1→0. The aggressor line CMOS inverter (driver) has pMOS width (W_p) double than nMOS width (W_n) while the victim line is grounded at the input through a linear region equivalent driver resistance. For all calculation and simulation purposes of long (1mm) interconnect of SWCNT bundle, the data shown in Table 3.3 have been used. The value of improved coupling capacitance between adjacent interconnects of SWCNT bundle as discussed in chapter 4, is calculated using appropriate expression available in Eq. (4.37).

The circuit parameters and coupling capacitance of long (1mm) interconnect of copper are calculated from Eqs.(3.32)-(3.34) and Eq.(4.38), and data obtained from Table 3.1. Simulation for coupled interconnects of copper has been carried out assuming the same technology node and clock speed.

Table 6.1 Impedance parameters of long (1mm) interconnect:
Temperature 300K, Technology=22nm

Impedance parameters	**SWCNT bundle**	**copper (Cu)**
Resistance(Ω)	1240	13671.87
Ground Capacitance(pF)	2.57	0.015
Self Inductance(pH)	0.26	2031.33
Coupling capacitance (fF) (proposed model)	2.6	75.17

6.4.1Transient Response Analysis

Figs.6.2 and 6.3 exhibit the transient response of crosstalk induced noise at the far end of victim line, for varied temperatures, both for CNT and copper and provide an insight into the temperature variation of interconnect resistance (see Fig.6.1). In this analysis, the width (*w*) and thickness (*H*) of global (1mm long) interconnect are assumed to be 32nm and 96 nm respectively, and space(*s*) between two interconnect is assumed to be 32nm.

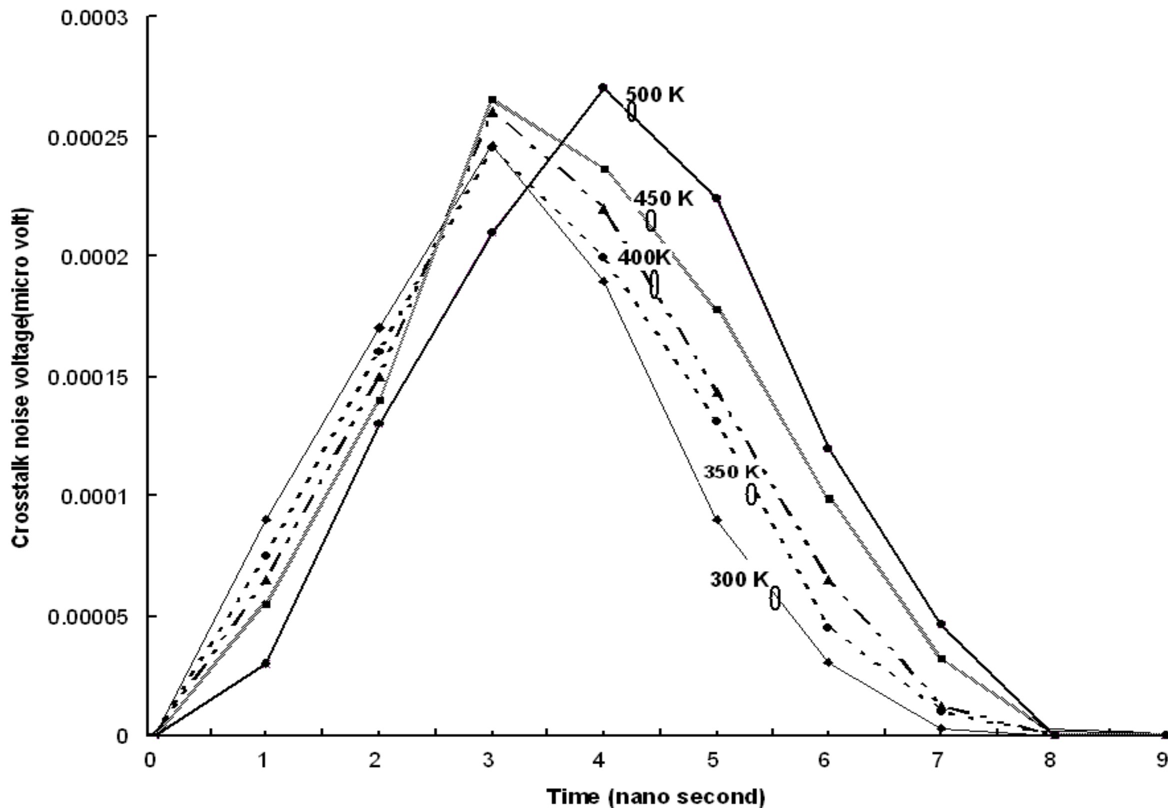

Figure 6.2 Crosstalk induced transient response of coupled interconnects for the SWCNT bundle (proposed model) at the far end of victim line, at 22n technology node for varying temperatures.

It is seen that while over a rise in temperature, ranging from 300K to 500K, the transient variation of crosstalk-induced noise voltage level increases for both CNT and copper interconnect. Compared to the waveform of the improved model based SWCNT bundle, that of

the Copper shows higher positive and negative voltage peaks. The high voltage peaks are due to the comparatively higher L_S, C_C and lower C_g values of copper (see Table 6.1).

Due to this higher C_C value, compared to the SWCNT bundle, copper based coupled interconnects provide a lower reactance path. In addition, as self inductance is increased, the even and odd mode characteristic impedances increases, causing the positive coupled peak voltage to rise significantly [15],[104]. When the ground capacitance increases, both even and odd mode characteristic impedance reduces and causes a large fall in coupled peak voltage.

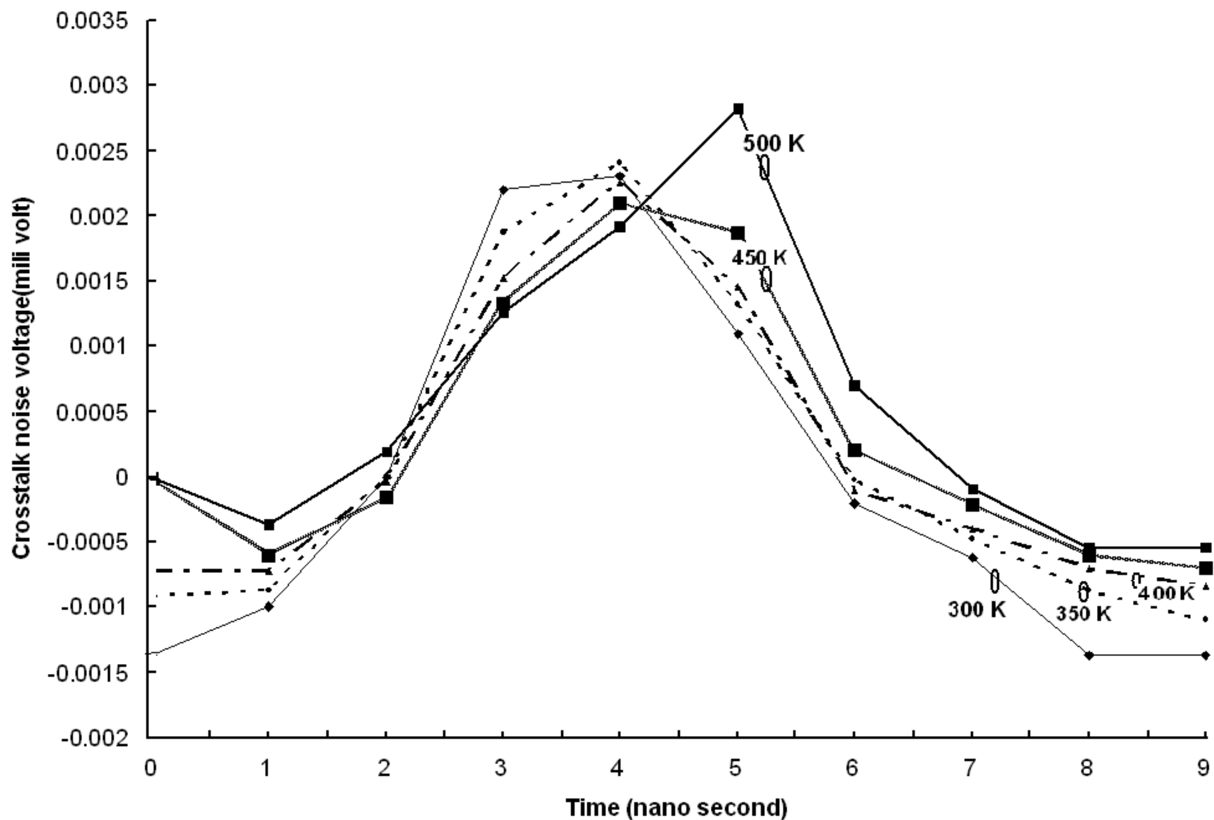

Figure 6.3 Crosstalk induced transient response of coupled interconnects for the copper at the far end of victim line, at 22n technology node for varying temperatures.

Fig.6.4 illustrates the dependence of the normalized time duration of the victim output waveform on temperature, ranging from 300K to 500K, for both CNT and copper. The time duration values have been normalized by their respective values obtained at 300K. It is observed that while the variation of the waveform time duration of the coupled SWCNT bundle interconnect with temperature is always lower than that of the copper interconnect, both monotonically increase with temperature. This is because, with increased temperature, interconnect resistance increases [15], [104], [106] and so the time duration also increases.

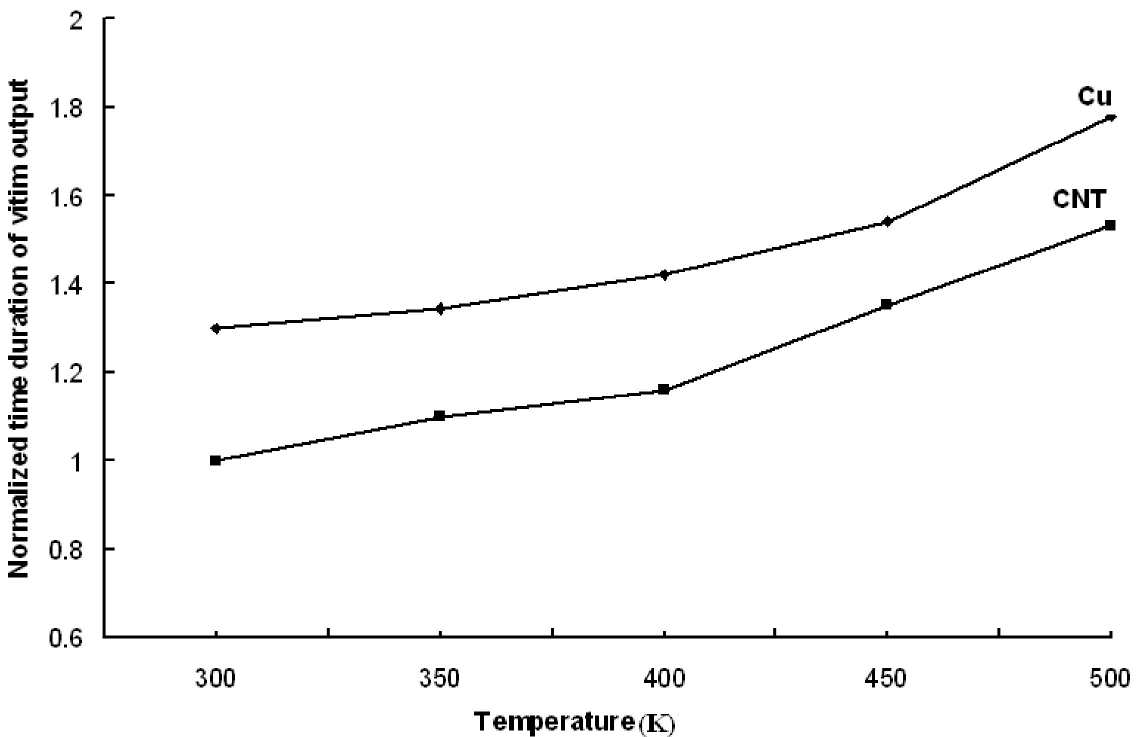

Figure 6.4 Variation of time duration with temperature at 22nm technology node.

6.4.2 Frequency Spectrum Analysis

Figs.6.5 and 6.6 depict the variation of crosstalk amplitudes with temperatures ranging from 300 K to 500 K, for varied frequencies, for SWCNT bundle and copper interconnects respectively. The frequency components have been obtained using a script of Fast Fourier transform (FFT) technique written in C language , with transition period of the input and output waveforms divided into 64(2^6) equal parts. The amplitudes of the frequency spectrum (y axis of Figs.6.5 and 6.6) are normalized by the amplitudes of input signal frequency; the frequencies (x axis of Figs.6.5 and 6.6) are normalized by the corresponding input signal frequency.

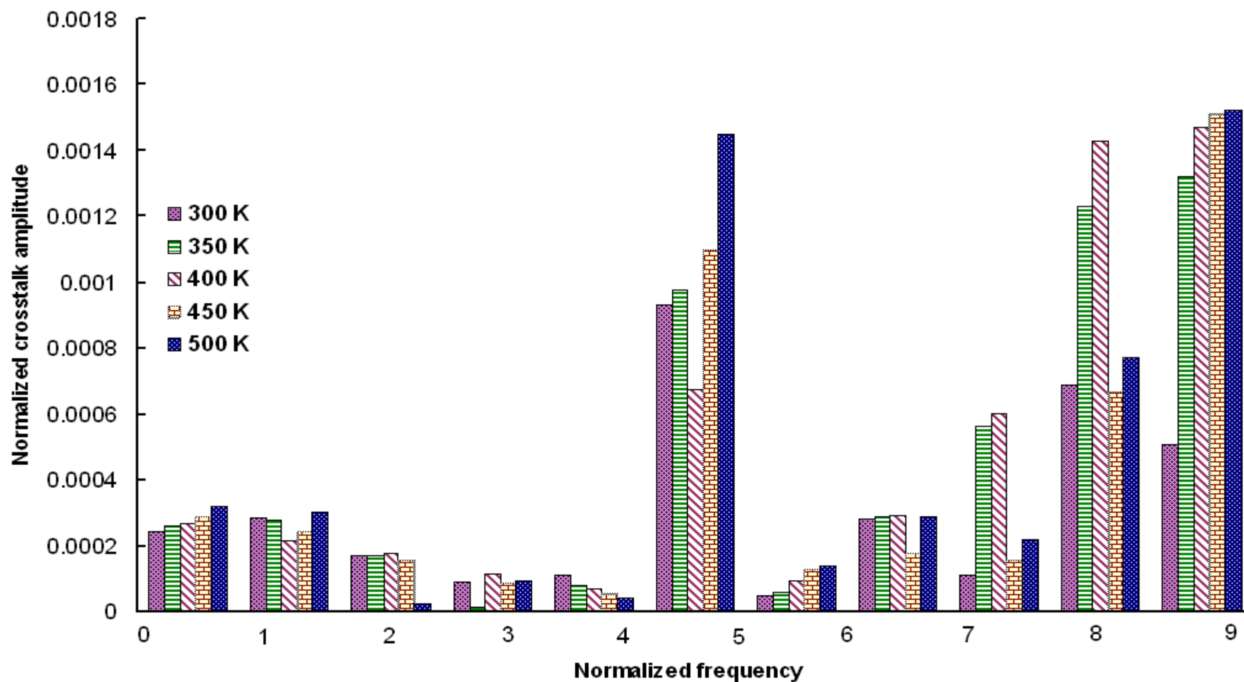

Figure 6.5 Variation of normalized crosstalk amplitude of frequency components with normalized signal frequency as a function of temperature variations for SWCNT bundle at the far end of victim line.

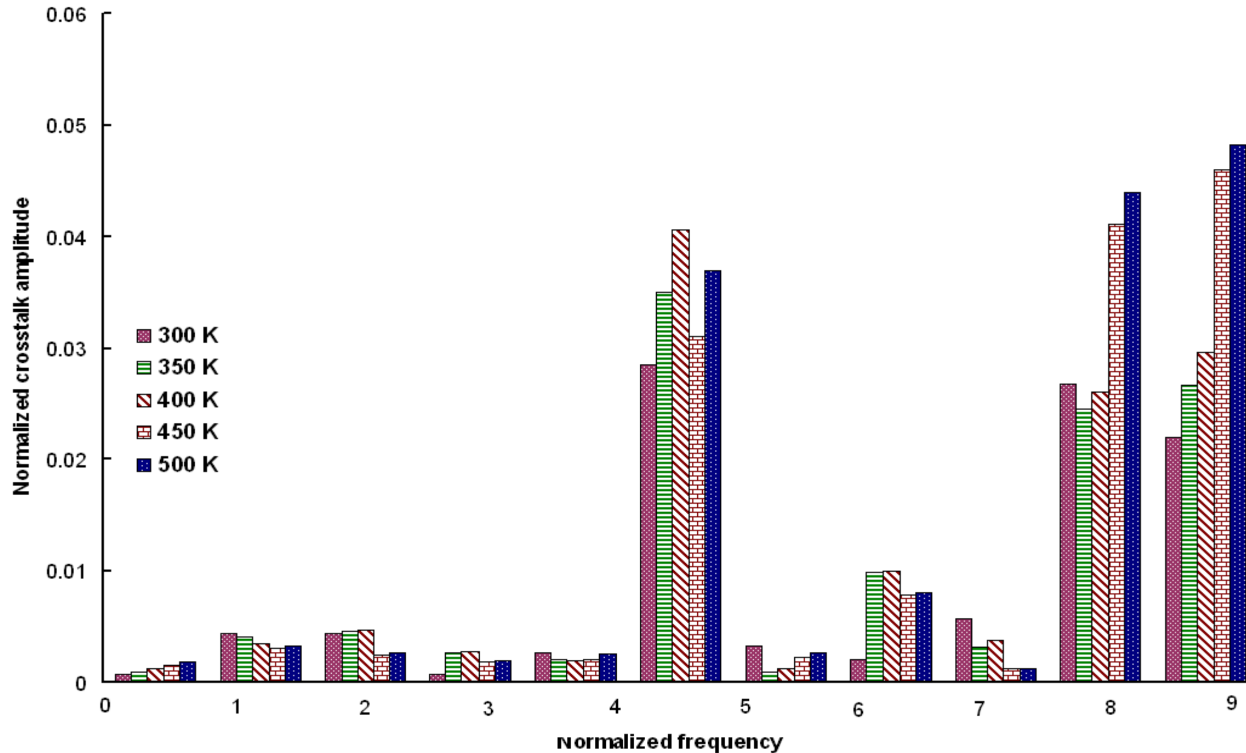

Figure 6.6 Variation of normalized crosstalk amplitude of frequency components with normalized signal frequency as a function of temperature variations for Copper at the far end of victim line.

Result shows that, for the entire normalized frequency range, compared to copper interconnects, as temperature rises, coupled interconnects of SWCNT bundle have smaller amplitude levels of noise and filter more noise frequency components of victim output. Also, both for SWCNT bundle and copper interconnects, noise frequency components are more suppressed in the smaller frequency range. Furthermore, it has been seen that, at all frequencies, the amplitude of the crosstalk noise level generally increases. It may be noted that, compared to CNT, coupling is more dominant in copper due to low reactance path between two parallel interconnects and combined influence of other impedance parameters of interconnect viz. higher resistance and inductance with smaller ground capacitance.

6.5 CONCLUSION

The effect of temperature, varying over a range from 300K to 500K, on the crosstalk induced noise voltage waveform and its frequency spectrum both in capacitively coupled interconnects of SWCNT bundle using an improved inter bundle coupling capacitive model and in copper interconnects at the far end of victim line, at 22 nm technology node has been investigated.

It is observed that, as temperature rises from 300K to 500K, the crosstalk induced voltage levels at victim far end in SWCNT bundle interconnects are found to be significantly low compared to the copper. The time duration of the coupled victim output waveform increases with rise in temperature for both Copper and SWCNT bundle interconnects but the variation is more pronounced in the Copper.

It has also been noted that, with rise in temperature, the coupled SWCNT bundle interconnects suppresses more frequency components of the noise voltage than the conventional metal (copper) interconnects. In addition, as signal frequency and temperature of the interconnect increases, the victim line gets more prone to crosstalk noise in copper interconnects than SWCNT bundle interconnect. These considerations make SWCNT bundle interconnects an attractive and promising material in modern VLSI design.

Chapter 7

CONCLUSION AND SUGGESTION FOR FUTURE WORK

7.1 INTRODUCTION

In this chapter, the entire research work presented in the thesis has been summarized and important conclusions drawn. The scope for future work has also been discussed here. Section 7.2 gives a summary of the important findings, Section7.3 lists the important contributions and Section 7.4 provides some suggestions and scope for future work in the related topic.

7.2 SUMMARY OF IMPORTANT FINDINGS

In recent times, the exponential growth of copper based interconnect density in deep submicron(DSM) technology nodes, that connect millions of active devices on a chip, is posing a serious bottleneck in terms of substantial capacitive and inductive couplings. Hence there appears a dire need to search a potential material for future generation of VLSI interconnects design that will be capable of exhibiting minimized delay, power dissipation and crosstalk effects.

The research work presented in this dissertation provides a comparative analysis of the propagation delay, power dissipation, cross-talk induced noise voltage and its frequency spectrum in CMOS inverter driven global interconnects of SWCNT bundle and copper. An

Alpha power law model [129] is used for representing the transistor in the CMOS driver. The single interconnect as well as capacitively coupled interconnects are represented by the π-equivalent circuit of distributed *RLC*-model. The Driver-Interconnect-Load (DIL) model [15] of distributed *RLC* circuit is used for the mutually coupled interconnects. The analytical results obtained using the CMOS inverter driven π-equivalent *RLC*-circuit model and DIL model matches closely with the SPICE simulation results. Further the effect of (i) tube diameter, (ii) interconnect dimensions and temperature variations on crosstalk induced noise voltages in capacitive coupled interconnects have also been investigated. Finally an improved model for the inter bundle coupling capacitance of CNT has been proposed.

7.2.1 Influence of Tube parameters on SWCNT Bundle Interconnect Performance

The performance of SWCNT bundle interconnects in terms of delay and power dissipation is influenced by resistance, inductance and capacitance. These impedance parameters depend on the Single Walled Carbon Nanotube (SWCNT) parameters viz. tube separation(x), diameter (d) and length (L). Therefore it seems pertinent to investigate the effects of these SWCNT parameters on delay and power dissipation. Other researchers have also investigated the influence of length and widths on SWCNT bundle interconnect performance [63],[118],[120] and suggested that these are due to the control of bundle length and width on equivalent circuit impedance parameters.

The present study investigates how, at 32nm and 22nm technology nodes, delay and power dissipation in a CMOS inverter driven π-equivalent circuit of SWCNT-bundle interconnect is controlled by the tube parameters x, d and L. The alpha power law model is used for representing transistors of the CMOS-inverter and the output waveform analytically

determined, for both CNT and copper, and compared with SPICE simulation results. There appears good agreement between the analytical and simulation results obtained.

Based on these results, it is observed here that, for SWCNT bundle interconnects, delay is appreciably increased as tube separation is increased. Similarly, as tube diameter increases, delay increases appreciably. In comparison, the effect of separation between adjacent tubes on the power dissipation is much less. The variation of power dissipation with tube separation is observed to be, on an average, about 10% more than it is with tube diameter. These results further indicated that a suitably optimized tube separation and tube diameter can control the SWCNT interconnect delay very well. This approach can be utilized for reducing the power dissipation in SWCNT interconnects.

Further, a similar analysis was carried out with the currently used copper interconnects at the same 32nm and 22nm technology nodes and the results obtained were compared with those previously obtained for SWCNT bundle interconnects. On the basis of these, it was observed that, in terms of delay, SWCNT bundle interconnect performs better than copper interconnect if the separation between the tubes is less than a certain critical value (viz. x=2nm). It has also been noted that a SWCNT bundle composed of tubes of 1nm diameter is of lower delay than copper interconnect at various interconnect lengths and higher power dissipation due to dominance of larger capacitance of SWCNT bundle.

7.2.2 Crosstalk Analysis in Coupled Carbon Nanotube Bundle Interconnects

In scaled DSM-CMOS Technology, the growing interconnects density and reduced chip size causes more capacitive and inductive coupling by parallel running interconnects of copper. This affects the reliability of the performance of the circuit. Several researchers have been exploring for new, high performance interconnects that will be capable of meeting the critical

requirements of future ICs [17]-[30]. In terms of reliability of performance of the circuit, the Carbon Nanotube (CNT) appears a more promising alternative than copper interconnects.

In recent times, accurate crosstalk analysis between coupled nanotubes has become a prime aspect of research for future nanoscale interconnects based on CNTs. Several researchers have investigated the crosstalk effects in coupled interconnects of CNT by representing the driving CMOS gate by a simple resistor [1]-[13]. When an equivalent linear resistor is used to model the non-linear CMOS transistors, it leads to discrepancy in the estimation of the crosstalk effect [14], [15]. Hence, for accurate crosstalk analysis in CNT interconnects, the equivalent linear resistor needs to be replaced by nonlinear CMOS transistors in capacitive coupled interconnects. This idea has been incorporated in this study.

Here an analytical model is developed to extract the transient response of victim output using CMOS inverter driven π-equivalent *RLC* circuit of capacitively coupled interconnects of both Single Walled Carbon Nanotube (SWCNT) bundle and copper. An Alpha power law model is used to represent the transistor in the CMOS inverter (driver). It is observed that at 32nm and 22nm technology nodes, for capacitive coupled interconnects, the piecewise analytical results replicate the SPICE waveforms very well.

Most investigators of CNT interconnects assume the value of coupling capacitance as equivalent to that of the coupling effect between metal interconnects (copper material based interconnects) of the same dimensions (e.g.[1]-[6],[59]). However, since material properties of copper widely vary from those of CNTs, there is need for some more realistic estimation of coupling capacitance values. An improved model of inter bundle coupling capacitance [118], based on this idea, has been proposed in the present work.

A comparative study of the crosstalk analysis between SWCNT bundle interconnects with coupling capacitance, estimated (a) conventionally (conventional model) and also (b) as proposed above (the proposed model) and also copper interconnects, at 32nm and 22nm technology nodes, has shown that, compared to the waveform of the proposed model of inter bundle capacitance based SWCNT bundle, that of the conventional model shows higher positive and negative voltage peaks at the far end of victim line.

The parasitic impedance parameters viz. resistance(R), inductance (L) and capacitance(C) of SWCNT interconnect depends on the tube diameter. A diameter dependent crosstalk analysis at 32nm and 22nm technology nodes has revealed that, for both technology nodes, the normalized crosstalk noise at the far end of victim line initially decreases with increase in tube diameter but then increases beyond a critical value of the tube diameter. These variations are simply reflections of the combined effect of the tube diameter (d) variations on tube resistance(R) and capacitance(C).

A comparative analysis of the analytically extracted, capacitively and mutually coupled dependent transient responses and simulated transient responses and its frequency spectrum, at the far end of victim output, for both SWCNT bundle using an improved coupling capacitive model and the copper interconnects has revealed that, compared to copper, crosstalk noise voltage levels in capacitively coupled SWCNT bundles, at the far end of victim line, are significantly low.

In case of mutually coupled copper interconnects, the width of noise waveform is wider compared to CNT at the far end of victim line. Also, at both 32nm and 22nm technology nodes, compared to copper interconnects, capacitive coupled interconnects of SWCNT bundle filter

more noise frequency components while in mutually coupled interconnects of SWCNT bundles, noise components in the higher frequency range are suppressed.

7.2.3 Influence of Interconnect dimensions in Coupled Carbon Nanotube Bundles

With decrease of feature sizes to deep sub micrometer dimensions, the coupling effects that accompany the exponential growth of interconnects become increasingly more significant [87],[89],[97]. One way to manage the coupling noise is by controlling the line parasitics viz. resistance(R), inductance (L) and capacitance (C). These can be controlled by wire sizing and spacing.

In this present study, an investigation of the control of crosstalk induced noise voltage (functional crosstalk noise) in capacitively coupled interconnects of SWCNT bundle, at the far-end of victim line, for fixed pitch and varying interconnect dimensions, for the proposed inter coupling capacitance model and the conventional model, at 22nm technology node, have indicated that, in comparison to the latter, the former provides better reduction in crosstalk induced noise voltage. It also showed that with suitably optimized interconnect dimensions in deep submicron, the coupled noise voltage at the far end of victim line can be controlled quite well.

A similar analysis performed for copper interconnects showed that, compared to coupled interconnects of SWCNT bundle, copper interconnects has higher coupled noise voltage levels due to larger coupling capacitance. A comparative analysis of the effect of interconnect resistance, self inductance and ground capacitance of interconnect on positive coupled peaks at the far end of victim line in capacitively coupled interconnects of SWCNT bundle and copper showed that with increase in line resistance or ground capacitance, while the noise voltage peak

reduces for both CNT and copper, there are more noise voltage peaks in the latter. Also as the self inductance increases, in copper interconnects the victim line gets more prone to crosstalk noise.

7.2.4 Temperature Dependent Crosstalk Analysis in Coupled Carbon Nanotube Bundle Interconnects

For advanced technology nodes, integrated circuits often operate at temperatures much greater than room temperature. Thus thermal issues are now emerging as a major challenging factor in the possible use of nanotubes for designing high performance integrated circuits. Thus it has become critical to understand how electrical characteristics of SWCNTs vary at temperatures greater than room temperature.

An analysis of the effect of temperature, varying over a range from 300K to 500K, on the crosstalk induced noise voltage waveform and its frequency spectrum both in capacitively coupled interconnects of SWCNT bundle using an improved inter bundle coupling capacitive model and in copper interconnects at the far end of victim line, at 22 nm technology node is conducted in this part of the study.

It is observed that, as temperature rises from 300K to 500K, compared to copper interconnects, the crosstalk induced voltage levels at the far end of victim line in SWCNT bundle interconnect are significantly low. The time duration of the coupled victim output waveform increases with rise in temperature for both copper and SWCNT bundle interconnects but the variation is more pronounced in the former. With rise in temperature, the coupled SWCNT bundle interconnects suppresses more frequency components of the noise voltage than the conventional metal (copper) interconnects. In addition, as signal frequency and temperature of

the interconnect increases, the victim line gets more prone to crosstalk noise in copper than in interconnects of SWCNT bundle.

7.3 MAIN CONTRIBUTIONS

- The present research provides a detailed investigation of the influence of tube parameters viz. tube separation, diameter and length on propagation delay and power dissipation using a CMOS driven π-equivalent circuit to SWCNT bundle interconnect at 32nm and 22nm technology nodes.
- A comparative analysis of the analytically extracted transient responses using CMOS inverter driven π-model [16] and simulated transient responses of the interconnect output, for both SWCNT bundle and copper, is carried out.
- An analytical timing model is developed to extract the transient response of the far end of victim line using CMOS inverter driven π-equivalent *RLC* circuit of capacitive coupled interconnects, for both SWCNT bundle and copper. The dependence of active device (MOSFET) behavior on input waveform is considered in this model.
- An improved model for extracting inter-bundle, real life, coupling capacitance between SWCNT bundles has been proposed.
- A comparative analysis of the analytically extracted, capacitively and mutually coupled dependent transient responses and simulated transient responses and its frequency spectrum, at the far end of victim output, for both SWCNT bundle with an improved coupling capacitive model and the copper interconnects, at 32nm and 22nm technology nodes, is studied.

- The effect of tube diameter on crosstalk induced noise voltage levels in capacitive ly coupled interconnects of SWCNT bundle at the far end of victim line, at 32nm and 22nm technology nodes, is studied.
- The effect of interconnect dimensions for fixed pitch on crosstalk induced noise voltage in capacitively coupled interconnects of SWCNT bundle for an improved inter coupling capacitive model and the conventional model with copper, at the far end of victim line, at 22nm technology node has been compared. Furthermore, the effect of interconnect resistance, inductance and ground capacitance on coupled positive peak at the far end of victim line is also observed.
- Finally, the effect of temperature, varying over a range from 300K to 500K, on the crosstalk induced noise voltage waveform and its frequency spectrum both in capacitively coupled interconnects of SWCNT bundle using an improved inter bundle coupling capacitive model and in copper interconnects at the far end of victim line, at 22 nm technology node, has been analyzed.

7.4 SUGGESTION FOR FUTURE WORK

Research and development is a continuous process. Each end of the research work is an opening to many avenues for the future work. The work just concluded has been verified by analytical modeling and simulation. It needs to be verified by fabrication.

The results obtained through the analysis presented in this thesis suggested that the effect of tube separation (x) and tube diameter (d) are advantageous to control the delay and power dissipation for long interconnects. Similar studies for ultra low power systems, working in sub threshold condition should be carried out.

Analytical study of crosstalk in coupled SWCNT bundles with accurate coupling capacitance and mutual capacitance expressions is still a topic of research. Most investigators of SWCNT bundle interconnects assume the value of coupling capacitance and mutual inductance as equivalent to that of the coupling effect between metal interconnects of the same dimensions. However, since material properties of copper widely vary from those of CNTs, perhaps there is need for some more realistic estimation of coupling capacitance as well as mutual inductance values.

Another possibilities for CNT interconnect in DSM technology nodes viz. Multi walled Carbon Nanotube (MWCNT), mixed CNT bundle and Graphene Nanoribbon (GNR) interconnect is a need to analyze the performance in terms of delay, power dissipation and crosstalk effects.

In addition, no account of temperature dependent crosstalk modeling and frequency spectrum analysis of crosstalk induced noise voltage in coupled SWCNT bundle interconnects has been reported. Therefore, similar studies should be carried out for advanced technology nodes.

REFERENCES

[1] Daniele Rossi, José Manuel Cazeaux, Cecilia Metra, and Fabrizio Lombardi, "Modeling Crosstalk Effects in CNT Bus Architectures," *IEEE Transactions on Nanotechnology* ,vol. 6, no. 2, pp.133-145, 2007.

[2] M. D'Amore, M.S. Sarto, A. Tamburrano, **"**Transient Analysis Of Crosstalk Coupling Between High-Speed Carbon Nanotube Interconnects," *in proc**.** IEEE International Symposium on Electromagnetic Compatibility,*2008,pp.1-6.

[3] Shao-Ning Pu,Wen-Yan Yin, Jun-Fa Mao and Qing H.Liu, "Crosstalk prediction of Single - and Double - walled Carbon-Nanotube (SWCNT/DWCNT) Bundle Interconnects," *IEEE Transactions on Electron Devices,vol.56.No.4, pp. 560-568,* 2009.

[4] Peng Sun, Rong Luo "Analytical Modeling for Crosstalk Noise Induced by Process Variations among CNT-based Interconnects," *in proc. IEEE International Symposium on Electromagnetic Compatibility (EMC 2009)* **,** 2009, pp.103-107.

[5] Debaprassad Das and Hafizur Rahaman, "Crosstalk analysis in carbon Nanotube interconnects And its impact on gate oxide reliability*", in proc.IEEE 2nd Asia symposium on quality electronic design*, 2010,pp.272-279.

[6] Debaprassad Das and Hafizur Rahaman. Analysis of Crosstalk in Single- and Multiwalz Carbon Nanotube Interconnects and Its Impacton Gate Oxide Reliability," *IEEE Trans. on Nanotechnology*:vol.10, no.6 ,pp.1362-1370,2011.

[7] Hassan, M.K. ,Rahaman, M.S., Chowdhury, M.H. *"Addressing crosstalk issue in on-chip carbon nanotube interconnects using negative capacitance", in proc. IEEE International Symposium on Circuits and Systems (ISCAS)*, 2011,pp. 1407 -1410.

[8] Sheikhassadi, H. , Masoumi, N. and Hakimi, A. "Crosstalk modeling in multiwalled carbon nanotubes as interconnects using the compact RC model," *in proc.15th IEEE Workshop on Signal Propagation on Interconnects (SPI),* 2011,pp.133-136.

[9] Zhang, Kailiang , Bo Tian ; Xiaosong Zhu ; Fang Wang ; Jun Wei**,** "Crosstalk analysis of carbon nanotube bundle interconnects," *in proc.IEEE 4th International Nanoelectronics Conference (INEC),*2011,pp.1-2.

[10] S.D.Pable, Mohd. Hasan and Mohd. Ajmal Kafeel, "Performance Analysis of Ultra Low-Power Mixed CNT Interconnects for Scaled Technology," *in proc. International Symposium on Electronic System Design*, 2011,pp.286-289.

[11] Jiaqing Lu , Min Tang and Junfa Mao**,** "Fast crosstalk analysis of multi-walled carbon nanotube interconnects," *in proc. IEEE Electrical Design of Advanced Packaging and Systems Symposium (EDAPS)*, 2012,pp. 131-134.

[12] Tamburrano, A. , D'Aloia, A.G. and Sarto, M.S. "Bundles of multiwall carbon nanotube interconnects: RF crosstalk analysis by equivalent circuits," *in proc. IEEE International Symposium on Electromagnetic Compatibility (EMC),* 2012, pp. 434 -439.

[13] Feng Liang, Gaofeng Wang and Hai Lin**,** "Modeling of Crosstalk Effects in Multiwall Carbon Nanotube Interconnects," *IEEE Transactions on Electromagnetic Compatibility*, vol.54 , issue.1 , pp.133 -139, 2012.

[14] R. Venkatesan, J.A. Davis, J.D. Meindl, Compact distributed RLC interconnect

models—part IV: unified models for time delay, crosstalk, and repeater insertion," *IEEE Trans. on Electron. Devices*, vol.50, pp. 1094–1102, 2003.

[15] Brajesh Kumar Kaushik and Sankar Sarkar, "Crosstalk Analysis for a CMOS-Gate-Driven Coupled Interconnects" *IEEE Transactions on Computer-Aided Design Of Integrated Circuits And Systems,* vol. 27, NO. 6, pp.1150-1154, 2008.

[16] Brajesh Kumar Kaushik, Sankar Sarkar and R.P.Agarwal, "Wave form analysis and delay prediction for a CMOS gate driven RLC interconnect load," *Integration the VLSI journal*, *vol.*40, pp.394-405,2007.

[17] W.Steinhogl, G.Schindler, G.Steinlesberger, M.Tranving, and M.Engelhardt, "Comprehensive study of the resistivity of copper wires with lateral dimensions of 100 nm and smaller," *Journal of Applied Physics*,vol.97,pp.023706(1-7), 2005.

[18] Naeemi et al., "Performance comparison between carbon nanotube and copper interconnects for giga scale integration (GSI)," *Electron Device letters*, vol. 26, no. 2, pp. 84-86, 2005.

[19] C. Schonenberger et al., "Interference and interaction in multiwalled carbon nanotubes," *Applied Physics A*, vol, 69, pp.283-295, 1999.

[20] A. Naeemi and J. D. Meindl, "Monolayer metallic interconnects: promising candidates for short local interconnects," *Electron device letters*,vol. 26, no. 8, pp. 544-546, 2005.

[21] G. Zhang, et.al., "Ultra-high-yield Growth of Vertical Single-Walled Carbon Nanotubes: Hidden Roles of Hydrogen and Oxygen," *in proc.* Nation Academy of Sciences, 2005, vol.102, no.45, pp.16141-16145.

[22] B.Q.Wei, R. Vajtai and P.M.Ajayan,"Reliability and current carrying capacity of

carbon nanotubes," *Applied Physics Letters,* vol.79,no.8,pp.1172-1174,2001.

[23] C. Dong, S. Haruehanroengra, and W Wang, "Exploring Carbon Nanotubes and NiSi Nanowires as On -Chip Interconnections," *in proc. of ISCAS,2000,* pp. 3510-3513.

[24] Gayasen, A., Vijaykrishnan, N. and Irwin, M.J., "Exploring technology alternatives for nano- scale FPGA interconnects," in p*roc. of DAC'05*, june 2005,pp. 921-926.

[25] Wu, Y., Xiang, J., Yang, C., Lu, W. *et al*.,"Single crystal metallic nanowires and metal/semiconductor nanowire heterostructures," *Nature*, vol. 430, pp. 61-65,July 2004.

[26] Morimoto, T. *et al*., "Self-aligned nickel-mono-silicide technology for high-speed deep submicrometer logic CMOS ULSI," *IEEE Trans. Electron Devices,*vol. 42, pp. 915–922, 1995.

[27] Y. Cui, L. J. Lauhon, M. S. Gudiksen, J. Wang and C. M. Lieber, "Diameter-controlled synthesis of single-crystal silicon nanowires," *Applied Physics Letter,vol.* 78, pp. 2214–2216,2001.

[28] Wu, Y. *et al.,* "Controlled growth and structures of molecular-scale silicon nanowires," *Nano Letter*,4 (3), pp. 433– 436, 2004.

[29] K. Toman, "The structure of NiSi," *Acta Crystallogr,* vol. *4*, no. 5, pp. 462–464,1951.

[30] Meyer, B. *et al.,* "Intrinsic properties of NiSi," *J. Alloys Compounds,* vol.262-263, pp.235–237, 1997.

[31] International Technology Roadmap for Semiconductors, 2007, available: www.itrs.net/Links/2007ITRS/2007.

[32] W.Steinhogl, G.Schindler, G.Steinlesberger, M.Tranving, and M.Engelhardt, "Comprehensive study of the resistivity of copper wires with lateral dimensions of

100nm and smaller," *Journal of Applied Physics*, vol.97,023706, 2005.

[33] Naeemi et al., "Performance comparison between carbon nanotube and copper interconnects for giga scale integration (GSI)," *Electron Device letters*, vol. 26, No. 2,84-86,2005.

[34] Dresselhaus, M.S., Dresselhaus, G. and Avouris, P., *Carbon Nanotubes: Synthesis, Structure,Properties and Applications*. New York: Springer- Verlag, 2001.

[35] Wu, W. and Maex, K., "Studies on size effects of copper interconnect lines," in *Proc. Solid-State and Integrated-Circuit Technology*, Shanghai, China, 2001, vol. 1, pp. 416-418.

[36] F. Kreupl, A. P. Graham , G. S. Duesberg , W. Steinhogl , M. Liebau , E. Unger , W. Hönlein, "Carbon Nanotubes in Interconnect Applications," *Microelectronic Engineering*, vol. 64, issues. 1-4, pp. 399-408, 2002.

[37] Jun Li, Qi Ye, Alan Cassell, Hou Tee Ng, Ramsey Stevens, Jie Han, and M.Meyyappan, "Bottom-up Approach for Carbon Nanotube Interconnects," *Applied Physics Letters*, vol. 82, no.15, 2491-2493, 2005.

[38] B. Q. Wei, R. Vajtai, and P. M. Ajayan, "Reliability and current carrying capacity of carbon nanotubes," *Appl. Phys. Lett*. vol.79,pp.1172-1174,2001.

[39] M. S. Dresselhaus, G. Dresselhaus, Ph. Avouris, ed. "Carbon Nanotubes: Synthesis,Structure, Properties and Applications," Berlin: Springer, 2001.

[40] S. J. Tans, M. H. Devoret, H. Dai, A. Thess, R. E. Smalley et al., "Individual Single-wall Carbon Nanotubes as Quantum Wires." *Nature*, vol.386, pp.474-77, 1997.

[41] M. S. Dresselhaus, G. Dresselhaus, A. Jorio, "Unusual Properties and Structure of Carbon Nanotubes," *Annual Reviews in Materials Research* ,vol.34 ,pp.247-78,2004.

[42] J. W. Mintmire, B. I. Dunlap, C. T. White, "Are Fullerene Tubules Metallic?" *Physical Review Letters,*vol. 68 pp. 631-34,1992.

[43] N. Hamada, S. Sawada, A. Oshiyama, "New One-dimensional Conductors: Graphitic Microtubules." *Physical Review Letters*,vol. 68 pp. 1579-81,1992.

[44] R. Saito, M. Fujita, G. Dresselhaus, M. S. Dresselhaus, "Electronic Structure of Chiral Graphene Tubules," *Applied Physics Letters* ,vol.60 ,pp.2204-6,1992.

[45] H. Dai, J. Kong, C. Zhou, N. Franklin, T. Tombler A. Cassel, S. Fan and M. Chapline, "Controlled chemical routs to nano architectures, physics and devices," *J.Phys. chem. B*, vol.103, pp. 11246-11255, 1999.

[46] F. Kreupl, A. P. Graham, M. Liebau, G. S. Duesberg, R. Seidel and E. Unger, "Microelectronic interconnects based on carbon nanotubes," available: http://arxiv.org/ftp/cond-mat/papers/0410/0410630.pdf**.**

[47] M.Nihei,M.Horibe,A Kawabata,Y.Awano, "Simulataneous formation of multiwall carbon nanotubes and their end-bonded ohmic contacts to Ti electrodes for future ULSI interconnects," *japan.J.Appl.Phys*. vol.43.no.4B, pp.1856-1859,2004.

[48] D. S. Bethune et al., "Cobalt-catalysed growth of carbon nanotubes with single-atomic-layer walls," *Nature*, vol. 363, pp. 605-607, 1993.

[49] A. Thess et al.,"Crystalline Ropes of Metallic Carbon Nanotubes," *Science*, vol. 273, pp. 483-487, 1996.

[50] M. Nihei, et al., "Low-Resistance Multi-Walled Carbon Nanotube Vias with Parallel Channel Conduction of Inner Shells," *IITC* , pp. 234-236, 2005.

[51] P. G. Collins, et al., "Current Saturation and Electrical Breakdown in Multiwalled Carbon Nanotubes," *PRL*, vol. 86, no. 14, pp 3128-3131,2001.

[52] S. Berber, et al., "Unusually High Thermal Conductivity of Carbon Nanotubes," *PRL*, vol. 84, no. 20, pp. 4613-4616, 2000.

[53] K. M. Liew, et al., "Thermal Stability of Single and Multi-walled Carbon Nanotubes," *Physical Review B*, vol. 71, pp.075424-075430, 2005.

[54] Navin Srivastav,Hong Li Franz Kreupl and kaustav Banerjee, "On the Applicability of Single Walled Carbon nanotubes as VLSI interconnects," *IEEE Transactions Nanotechnology*.vol.8, no.4,542-559, 2009.

[55] Ashok Srivastava,Yao Xu, Ashwani K. Sharma, **"**Carbon nanotubes for next generation very large scale integration interconnects," *Journal of Nanophotonics*, vol. 4,pp. 041690-041717, 2010.

[56] P. L. McEuen, et al., "Single-Walled Carbon Nanotube Electronics," *IEEE Trans. on Nanotechnology*, vol. 1, no. 1, pp. 78-85, 2002.

[57] Arijit Raychowdhury and Kaushik Roy, "Modeling and Analysis of Carbon Nanotube Interconnects and their Effectiveness for High Speed VLSI Design," *in proc.*4th *IEEE Conference on Nanotechnology*, 2004,pp.608-610.

[58] T. Sakurai, "Perspectives on power-aware electronics," *in proc. IEEE ISSCC Tech. Dig.*, 2003,pp.26–29.

[59] Azad Naeemi and James D. Meindl, "Design and Performance Modeling for Single-Walled Carbon Nanotubes as Local, Semiglobal, and Global Interconnects in Gigascale Integrated Systems," *IEEE Trans. On Electron Devices*, vol. 54, issue 1, pp.26– 37, 2007.

[60] Navin Srivastava and Kaustav Banerjee, "A Comparative Scaling Analysis of Metallic and Carbon Nanotube Interconnections for Nanometer Scale VLSI Technologies," *in*

Proc.21st International VLSI Multilevel Interconnect Conference (VMIC), Waikoloa, HI, 2004, pp. 393-398.

[61] Navin Srivastava, Rajiv V. Joshi and Kaustav Banerjee, "Carbon Nanotube Interconnects: Implications for Performance, Power Dissipation and Thermal Management,"*in proc.IEEE Conf.,*pp.251-253, 2005.

[62] Kaustav Banerjee and Navin Srivastava "Are Carbon Nanotubes the Future of VLSI Interconnections?" *in proc.DAC 2006*, San Francisco, California, USA, 2006,pp.809-814.

[63] Y Massoud and A Nieuwoudt. "Performance Analysis of Optimized Carbon Nanotube Interconnect,"*in proc. IEEE Symposium on Circuits and Systems*, *ISCAS* , 2008, pp 792-795.

[64] Mandeep Bamal, Scott List, Michele Stucchi, Anne S. Verhulst, Marleen Van Hove, Rudi Cartuyvels, Gerald Beyer and Karen Maex "Performance Comparison of Interconnect Technology and Architecture Options for Deep Submicron Technology Nodes," *in proc.IEEE conf.,* 2006, pp.202-204.

[65] Kyung-Hoae Koo, Hoyeol Cho, Pawan Kapur, and Krishna C. Saraswat, "Performance Comparisons Between CarbonNanotubes, Optical, and Cu for Future High-Performance On-Chip Interconnect Applications," *IEEE Transactions on Electron Devices*, vol. 54, no. 12, pp.33206-3215, 2007.

[66] Hoyeol Cho, Kyung-Hoae Koo, Pawan Kapur, and Krishna C. Saraswat, "Performance Comparisons Between Cu/Low-*κ*,Carbon-Nanotube, and Optics for Future On-Chip Interconnects," *IEEE Electron Device Letters*, vol. 29, no. 1,pp.122-124, 2008.

[67] Hong Li, Chuan Xu, and Kaustav Banerjee, "Carbon Nanomaterials: The Ideal Interconnect Technology for Next- Generation ICs," *IEEE Design & Test of Computers, Emerging Interconnect Technologies for Gigascale Integration*, vol. 27,no. 4, pp.20-31,2010.

[68] Hong Li, Wen-Yan Yin, and Jun-Fa Mao, "Modeling of Carbon Nanotube Interconnects andComparative Analysis with Cu Interconnects," *in Proc*. of Asia-Pacific Microwave Conference, Yokohama, 2006,pp. 1361 - 1364.

[69] Antonio Maffucci, Giovanni Miano, and Fabio Villone, "Performance Comparison Between Metallic Carbon Nanotube and Copper Nano Interconnects," *IEEE Transactions On Advanced Packaging*, vol. 31, no. 4, pp.692-699, 2008.

[70] Davood Fathi and Behjat Forouzandeh,"A Novel Approach for Stability Analysis in Carbon Nanotube Interconnects," *IEEE Electron Device Letters*, vol. 30, no. 5, pp.475-477, 2009.

[71] D. Fathi B. Forouzandeh S. Mohajerzadeh R. Sarvari, "Accurate analysis of carbon nanotube interconnects using transmission line model," *Micro & Nano Letters*, vol. 4, iss. 2, pp. 116–121, 2009.

[72] Antonio Maffucci, , Giovanni Miano, and Fabio Villone, "New Circuit Model for Carbon Nanotube Interconnects With Diameter-Dependent Parameters," *IEEE Transactions on Nanotechnology*, vol. 8, no. 3, pp.345-354,2009.

[73] A. Maffucci, G. Miano, and F. Villone, "Comparison between metallic carbon nanotube and copper nano-interconnects," *in Proc. IEEE Workshop Signal Propag. Interconnects SPI 2007*, Ruta di Camogli, Italy, 2007, pp. 29–32.

[74] Arthur Nieuwoudt, and Yehia Massoud "Evaluating the Impact of Resistance in

Carbon Nanotube Bundles for VLSI Interconnect Using Diameter-Dependent Modeling Techniques" *IEEE Transactions on Electron Devices*, vol. 53, no. 10, pp.2460-2466, 2006.

[75] Arthur Nieuwoudt Mosin Mondal and Yehia Massoud, "Predicting the Performance and Reliability of Carbon Nanotube Bundles for On-Chip Interconnect," *in proc. IEEE Conf.*, 2007, pp.708-7013.

[76] Azad Naeemi, and James D. Meindl, "Performance Modeling for Single- and Multiwall Carbon Nanotubes as Signal and Power Interconnects in Gigascale Systems," *IEEE Transactions on Electron Devices*, vol. 55, no. 10, pp. 2574-2582, 2008.

[77] Hong Li, Wen-Yan Yin, Kaustav Banerjee, and Jun-Fa Mao,"Circuit Modeling and Performance Analysis of Multi-Walled Carbon Nanotube Interconnects," *IEEE Transactions on Electron Devices*, vol. 55, no. 6, pp. 1328-1337, 2008.

[78] Hong Li, Chuan Xu, Navin Srivastava and Kaustav Banerjee,"Carbon Nanomaterials for Next-Generation Interconnects and Passives: Physics, Status, and Prospects," *IEEE Transactions on Electron Devices*, vol. 56, no. 9, pp. 1799-1820, 2009.

[79] Gael F. Close,Shinichi Yasuda, Bipul C. Paul, Shinobu Fujita and H.-S. Philip Wong"Measurement of Subnanosecond Delay Through Multiwall Carbon-Nanotube Local Interconnects in a CMOS Integrated Circuit," *IEEE Transactions on Electron Devices, vol.* 56, no. 1, pp. 43-49,2009.

[80] Brajesh Kumar Kaushik, Saurabh Goel,and Gaurav Rauthan, "Future VLSI interconnects: optical fiber or carbon nanotube – a review," *Microelectronics International*, vol. 24 issue. 2, pp.53 -63, 2007.

[81] A. Nieuwoudt and Y. Massoud, “Understanding the impact of inductance in carbon nanotube bundles for VLSI interconnect using scalable modeling techniques,” *IEEE Trans. on Nanotechnol.*, vol. 5, no. 6, pp. 758–765, 2006.

[82] M. Kamon, M. J. Tsuk, and J.White, “FastHenry: A multipole-accelerated 3-D inductance extraction program,” *IEEE Trans. Microw. Theory Tech.*, vol. 42, no. 9, pp. 1750–1758, 1994.

[83] H. Li and K. Banerjee, “High-frequency effects in carbon nanotube interconnects and implications for on-chip inductor design,” *in proc. IEDM Tech. Dig.*, 2008, pp. 525–528.

[84] P. C. P. Watts, W. L. Hsu, D. P. Randall, V. Kotzeva, and G. Z. Chen, “Fe-filled carbon nanotubes: Nano-electromagnetic inductors,” *Chem. Mater.*, vol. 14, no. 11, pp. 4505–4508, 2002.

[85] K. Tsubaki, Y. Nakajima, T. Hanajiri, and H. Yamaguchi, “Proposal of carbon nanotube inductors,” *J. Phys.: Conf. Ser.*, vol. 38, pp. 49–52, 2006.

[86] A. Nieuwoudt and Y. Massoud, “Predicting the performance of low-loss on-chip inductors realized using carbon nanotube bundles,” *IEEE Trans. Electron Devices*, vol. 55, no. 1, pp. 298–312, 2008.

[87] Hong Li and Kaustav Banerjee, “High-Frequency Analysis of Carbon Nanotube Interconnects and Implications for On-Chip Inductor Design,” *IEEE Transactions On Electron Devices*, vol. 56, no. 10, pp.2202-2214, 2009.

[88] Peng Sun, Rong Luo, “Analytical Modeling for Crosstalk Noise Induced by Process Variations among CNT-based Interconnects,” *in proc. IEEE International Symposium on Electromagnetic Compatibility*, 2009, pp. 103 - 107.

[89] Naushad Alam, A. K. Kureshi, Mohd. Hasan, and T. Arslan , "Performance Comparison and Variability Analysis of CNT Bundle and Cu Interconnects," *in proc. Multimedia, Signal Processing and Communication Technologies*, 2009. IMPACT '09, pp. 169 - 172.

[90] Arthur Nieuwoudt and Yehia Massoud, "Assessing the Implications of Process Variations on Future Carbon Nanotube Bundle Interconnect Solutions," *in proc.*8th *International Symposium on Quality Electronic Design*, ISQED 2007,pp .119 - 126.

[91] Lei Jia, Wen-Yan Yin, "Temperature Effects on Crosstalk in Carbon Nanotube Interconnects," *in proc. Asia-Pacific Microwave Conference(*APMC 2008*)*,2008, pp.1-4.

[92] Wen Chao Chen, Wen-Yan Yin, Lei Jia, and Qing Huo Liu, "Electrothermal Characterization of Single-Walled Carbon Nanotube (SWCNT) Interconnect Arrays," *IEEE Trans. on Nanotechnology*, vol. 8, no. 6, pp.718-728, Nov. 2009.

[93] E. Pop, D. Mann, J. Reifenberg, K. Goodson, H. Dai, "Electro-Thermal Transport in Metallic Single-Wall Carbon Nanotubes for Interconnect Applications," *in proc. IEEE International Electron Devices Meeting(IEDM) Technical Digest*, 2005, pp. 254–256.

[94] E. Pop, D.A. Mann, K.E. Goodson, H. Dai, "Electrical and thermal transport in metallic single-wall carbon nanotubes on insulating substrates," *Journal of Applied Physics* ,vol.101,iss.9,pp. 093710, 2007.

[95] Amir Hosseini , Vahid Shabro, "Thermally-aware modeling and performance evaluation for single-walled carbon nanotube-based interconnects for future high performance integrated circuits," *Microelectronic Engineering* ,vol.87, pp.1955–1962, 2010.

[96] K. C. Narasimhamurthy and Roy P. Paily, "Impact of Bias Voltage on Magnetic Inductance of Carbon Nanotube Interconnects,"*in proc.22nd International Conference on VLSI Design,* 2009,pp. 505 - 510.

[97] Azad Naeemi and James D. Meindl, "Impact of Electron-Phonon Scattering on the Performance of Carbon Nanotube Interconnects for GSI," *IEEE Electron Device Letters*, vol. 26, no. 7, 2005.

[98] Debaprasad Das, and Hafizur Rahaman "Timing Analysis in Carbon Nanotube Interconnects with Process, Temperature, and Voltage Variations," *in proc.IEEE International Symposium on Electronic System Design,* pp.27-32,2010.

[99] M. D'Amore, M. S. Sarto, and A. Tamburrano, "Modelling of multiwall carbon nanotube transmission lines," in proc. ICEAA 2007, Torino, Italy,2007,pp. 629 – 632.

[100] Maria Sabrina Sarto and Alessio Tamburrano, "Single-Conductor Transmission-Line Model of Multiwall Carbon Nanotubes," *IEEE Transactions on Nanotechnology*, vol. 9, no.1,pp.82-92, 2010.

[101] P.U.Sathyakam, P.S.Mallick, "Transient analysis of mixed carbon nanotube bundle interconnects," *Electronics Letters, - IET,* vol.47, iss.20, pp. 1134 -1136,2011.

[102] Naushad Alam, A. K. Kureshi, Mohd. Hasan and T. Arslan, "Carbon Nanotube Interconnects for Low-Power High-Speed Applications," *in proc. IEEE International Symposium on* Circuits and Systems, 2009 ,pp. 2273- 2276.

[103] Manoj Kumar Majumder, B. K. Kaushik and S. K. Manhas, "Analysis of Mixed CNT Bundle Interconnects: Impact on Delay and Power Dissipation," *in proc.5th international Conf. Computer and Device for Communication (CODEC2012)*, Kolkata, 2012,pp. 1-4.

[104] K. Agarwal, D. Sylvester, D. Blaauw, “Modeling and analysis of crosstalk noise in coupled RLC interconnects,” *IEEE Trans. on Computer.-Aided Des. Integrated Circuits* Syst.,vol. 25,pp. 892–901, 2006.

[105] L.Gal, “On-Chip crosstalk-The new signal integrity challenge,” *in proc. Custom-Integrated Circuits Conf.*, 1995,pp.12.1.1-12.1.4.

[106] Kevin T. Tang and Eby G. Friedman, “Peak Crosstalk Noise Estimation in CMOS VLSI Circuits,” *in proc. IEEE Conf.*, 1999,pp.1539-1542.

[107] J.A. Davis, J.D. Meindl, “Compact distributed RLC interconnect models—part I: Single line transient, time delay and overshoot expessions,” *IEEE Trans. Electron. Devices* ,vol.47, pp. 2068–2077, 2000.

[108] J.A. Davis, J.D. Meindl, “Compact distributed RLC interconnect models— part II: coupled line transient expressions and peak crosstalk in multilevel interconnect networks,” *IEEE Trans. Electron. Devices* ,vol.47, pp.2078–2087, 2000.

[109] K. Banerjee, A. Mehrotra, “Accurate analysis of on-chip inductance effects and implications for optimal repeater insertion and technology scaling,” *in Proc. of the IEEE Symposium on VLSI Circuits*, Kyoto, Japan, 2001 pp. 195–198.

[110] K. Banerjee, A. Mehrotra, “Analysis of on-chip inductance effects for distributed RLC interconnects,” *IEEE Trans .on Computer Aided Design,* vol.21,904–915, 2002.

[111] R. Venkatesan, J.A. Davis, J.D. Meindl, “Compact distributed RLC interconnect models—part III: transients in single and coupled lines with capacitive load termination,” *IEEE Trans. Electron. Devices* ,vol.50, pp.1081–1093,2003.

[112] B.K. Kaushik and S. Sarkar. “Crosstalk analysis for a CMOS gate driven inductively and capacitively coupled interconnects,” *Microelectronics Journal,* vol.39, pp.1834-

1842, 2008.

[113] H.B.Bakoglu, J.D.Mendil, “Optimal interconnection circuits for VLSI,” *IEEE Transactions on Electron Devices*, vol.32,no.5,pp.903-909,1985.

[114] H. B. Bakoglu, “Circuit, Interconnections, and packaging for VLSI,” Addison-Wesley: Reading, MA,1990.

[115] B.K.Kaushik, R.P Agarwal, S.Sarkar, R.C.Joshi and D.S.Chauhan “Repeater insertion in crosstalk-aware inductively and capacitively coupled interconnections,” *International Journal of Circuit Theory and Applications,*vol.39, pp.629-647,2011.

[116] Manoj Kumar Majumder, Nisarg D. Pandya, B. K. Kaushik, and S. K. Manhas, “Signal Integrity Analysis in Single and Bundled Carbon Nanotube Interconnects,” *Journal of Nanoscience*, article ID 407301, doi.org/10.1155/2013/407301,2013.

[117] Uma Sathyakam, P. , Karthikeyan, A. and Mallick, P.S. “Role of Semiconducting Carbon Nanotubes in Crosstalk Reduction of CNT Interconnects,” *IEEE Transactions on Nanotechnology*, vol.12 , no.5, pp. 662 – 664, 2013.

[118] N. Srivastava and K. Banerjee, “Performance analysis of carbon nanotube interconnects for VLSI applications,” *in proc. IEEE/ACM Intl. Conf. on ICCAD*,2005, pp.383-390.

[119] P. J. Burke, “Luttinger Liquid Theory as a Model of the Gigahertz Electrical Properties of Carbon Nanotubes,” *IEEE Trans. Nanotechnology*, vol. 1, no. 3,129-144, 2002.

[120] Yehia Massoud and Arthur Nieuwoudt, “Modeling and Design Challenges and Solutions for Carbon Nanotube Based Interconnect in Future High Performance Integrated Circuits,” *ACM Journal on Emerging Technologies in Computing Systems,*

vol. 2, no. 3, 2006.

[121] A.Raychowdhury and K.Roy, "Modeling of metallic carbon-nanotube interconnects for circuit simulations and a comparison with Cu interconnects for scaled technologies," *IEEE Trans. Comput.-Aided Design Integr.Circuits Syst.*,vol.25,no.1,pp.58-65,Jan.2006.

[122] Artur Nieuwoudt and Yehia Massoud, "On the Optimal Design, Performance, and reliability of Future Carbon Nanotube-Based interconnect Solutions," *IEEE Transaction on Electron devices*,vol.55,no.8,2008.

[123] N.W.Ashcroft and N.D.Mermin. Solid State Physics. Philadelphia,PA:Saunders College, 1976.

[124] Park J. Y, Rosenblatt S., Yaish .Y, Sazonova V., Ustunel H., Braig S, Arias T. A, Brouwer P. W, and McEuen P. L., "Electron-phonon scattering in metallic single-walled carbon nanotubes," *Nano Lett,*vol. 4 ,no.*3*, pp.517-520,2004.

[125] Predictive Technology Model [Online]. www.eas.asu.edu/~ptm/.

[126] Wong Shyh-Chyi, Lee Gwo-Yann, and Ma Dye-Jyun, "Modeling of Interconnect Capacitance, Delay, and Crosstalk in VLSI," *IEEE Trans. on Semiconductor Manufacturing*, vol.13, no.1.pp. 108 -111, 2000.

[127] A. Naeemi and J. D. Meindl, "Compact physical models for multiwall carbon-nanotube interconnects," *IEEE Electron Device Lett.,* vol. 27,no. 5, pp. 338–340, 2006.

[128] A. Naeemi and J. D. Meindl, "Design and performance modeling for single-walled carbon nanotubes as local, semiglobal, and global interconnects in gigascale integrated systems," *IEEE Trans. Electron Devices*, vol. 54, no. 1, pp. 26–37, 2007.

[129] T.Sakurai,A.R.Newton, “Alpha-power law MOSFET model and its applications to CMOS inverter delay and other formulas,”*IEEE J.Solid-State Circuits*,vol.25,pp.584-594,1990.

[130] R. Chandel, S Sarkar and R. P. Agarwal, “Delay and Power Management of Voltage-scaled Repeater Driven Long Interconnects,” *Int. J. Modeling and Simulation*, vol. 27, pp.333-339, 2007.

[131] M. A. El-Moursy and E. G. Friedman, “Power Characteristics of Inductive Interconnect,” *IEEE Trans. on VLSI Systems*, vol. 12, no. 12, pp. 1295- 1306,2004.

[132] Kailiang Zhang , Bo Tian , Xiaosong Zhu , Fang Wang and Jun Wei, “Crosstalk analysis of carbon nanotube bundle Interconnects,”*Nanoscale Research Letters* , vol.7,no.138, pp. 1-5, 2012.

[133] Marcello D’ Amore, Maria Sabrina Sarto, and Alessio Tamburrano, “Fast Transient Analysis of Next-Generation Interconnects Based on Carbon Nanotubes*,” IEEE Trans. on Electromagn. Compat*.,vol.52, no.2,pp. 496-503, 2010.

[134] E. Pop,David Mann,Jien Cao,Qian Wang,Kenneth Goodson and Hongjie Da. “Negative Differential Conductance and Hot Phonons in Suspended Nanotube Molecular Wires,” *Physical Review Letters*: vol.95,pp. 1-4, 2005.

[135] Choongho Yu , Li Shi , Zhen Yao , Deyu Li , and Arunava Majumdar, “Thermal Conductance and Thermopower of an Individual Single-Wall Carbon Nanotube,” *Nano Letters*,vol.5,pp.1842–1846, 2005.

[136] Eric Pop, David Mann, Qian Wang, Kenneth Goodson, and Hongjie Dai, “ThermalConductance of an Individual Single-Wall Carbon Nanotube above Room Temperature,” *Nano Letter,*vol.6,no.1,pp.96-100, 2006.

[137] Giustiniani, V. Tucci, W. Zamboni: "Carbon Nanotubes Bundled Interconnects: Design Hints Based on Frequency and Time-Domain Crosstalk Analyses", *IEEE Trans. On Electron Devices*, vol. 58, no. 8, pp. 2702-2711, DOI: 10.1109/ TED. 2011.2152846, 2011.

[138] El Shabrawy, K., Maharatna, D. K, Bagnall, and B.M. Al-Hashimi, "Modeling SWCNT band gap and effective mass variation using a Monto Carlo approach" *IEEE Transactions on Nanotechnology*, vol. 9,issue.2, pp.184-93,2009.

[139] V.Parkash and A.K . Goel, "Modeling of Electronic Transport in Metallic Carbon Nanotubes in the presence of Electron-phonon interactions," *Microwave and Optical Technology letter*,vol.54, no.11, pp.2477-2483,2012.

[140] V.Parkash and A.K . Goel, "Performance analysis of Metallic Carbon Nanotubes as Nanotechnology circuit interconnects," *Microwave and Optical Technology letter*,vol.53, no.11,pp.2505-2508,2012.

[141] Giustiniani, V. Tucci, W. Zamboni, "Modeling Issues and Performance Analysis of High Speed Interconnects Based on a Bundle of SWCNT," *IEEE Trans. On Electron Devices*, vol. 57, issue 8, pp.1978 – 1986, DOI 10.1109/ TED.2010. 2050836,2010.

[142] Kang Zhang, Qing Zhang, Cao Liu, Nicola Marzari and Francesco Stellacci, "Diameter Effect on the Sidewall Functionalization of Single- Walled Carbon Nanotubes by Addition of Dichlorocarbene,"*Advanced Functional Materials, vol.22*,issue.24, pp.5216-5223, 2012.

[143] Patrizia Lamberti and Vincenzo Tucci, "Impact of the Variability of the Process Parameters on CNT-Based Nanointerconnects Performances: A Comparison Between SWCNTs Bundles and MWCNT," *IEEE Transactions on Nanotechnology*, vol. 11,

no. 5, 2012.

[144] Giancoli, Douglas. 25. Electric Currents and Resistance: In Jocelyn Phillips (ed.), *Physics for Scientists and Engineers with Modern Physics* (4th edition ed.). Upper Saddle River, New Jersey: Prentice Hall: (2009) [1984]; 658.ISBN 0-13-149508-9.

LIST OF PUBLICATIONS

1. **Mayank Kumar Rai**, Rajesh Khanna and Sankar Sarkar "Control of tube parameters on SWCNT Bundle Interconnect Delay and Power Dissipation," *Microelectronics International,* volume 31, issue 1, pp.24–31, 2013, **(SCI Indexed Impact Factor:0.731)**.
2. **Mayank Kumar Rai**, Rajesh Khanna and Sankar Sarkar,"Crosstalk analysis in CNT bundle interconnects for VLSI application," *IEEJ Transaction on Electrical and Electronic Engineering,* (*Journal of Wiley*),accepted,2013, in press, **(SCI Indexed Impact Factor:0.343)**.
3. **Mayank Kumar Rai** and Sankar Sarkar, "Influence of distance between adjacent Tubes on SWCNT bundle interconnect delay and power dissipation," *Journal of Computational Electronics (JCEL)*, volume 12, Issue 4, pp 796-802, December 2013, (*Journal of Springer*) , **(SCI Indexed Impact Factor:1.013).**
4. Mayank Kumar Rai and Sankar Sarkar, "Influence of tube diameter on carbon nanotube interconnect delay and power output," *physica status solidi (a),* vol.208, issue.no.3,pp.735-739,2011, *Journal of Wiley* **(SCI Indexed Impact Factor:1.469)**.
5. S.Sarkar, **Mayank Kumar Rai** et.al, "Carbon Nanotube Based Interconnects for VLSI Application" *Journal of The Institution of Engineers (I): Series B, Springer,Formerly IE(I) Journal – ET,* Volume 91, January 2011.

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1. **Mayank Kumar Rai** and Sankar Sarkar, "Temperature dependant crosstalk analysis in coupled Single walled carbon nanotube (SWCNT) bundle interconnects" *International Journal of Circuit Theory and Applications,(Journal of Wiley).*

Book chapter

1. Book chapter accepted Titled "Carbon nano tube as VLSI Interconnect", in the book Titled "Carbon Nanotubes / Book 5", ISBN 978-953-307-499-3, Publisher: InTech Open Access, Austria. Authors Name: **Mayank Kumar Rai** and Sankar Sarkar.

Conferences

1. **Mayank Kumar Rai** et.al, "Delay analysis of Carbon Nanotube interconnects for VLSI Application", IEEE sponsored Int.Conf on Emerging Trends in Signal Processing and VLSI Design(SPVL2010), GNEC, Hyderabad, 11-13th June 2010.
2. **Mayank kumar rai** et. al., "Control of SWCNT- Interconnect Performance by Tube diameter", *in proc. Intl.Conf. on Circuits and Systems,* ***IEEE Tencon 2009***,24-27th Nov.2009.Singapore.
3. **Mayank kumar rai** et al., "Power Dissipation in SWCNT Interconnect" *In proc.4th Intl.Conf. on Computers and Devices for Communication* ***(CODEC09)***, 14–16th Dec,2009, organized by Institute NEV of Radio Physics & Electronics ,University of Calcutta, Kolkata, India, sponsored by *IEEE, IEEE GRSS and Electron Devices society sponsored*.