Integrated Approach to Supply Noise Reduction In Advanced IC's and Die Package Board Ripple Analysis

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In

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DECLARATION

I, **Sourav Bhadwal** hereby declare that the work presented in this thesis entitled "**Integrated Approach to Supply Noise Reduction in Advanced IC's and Die Package Board Ripple Analysis"** in partial fulfillment of the requirement for the award of degree of **Master of Technology (VLSI Design)** submitted at **Electronics and Communication Department,** Thapar Institute of Engineering & Technology (Deemed to be University), Patiala is an authentic record of work carried out under supervision of **Dr. Ankit Soni & Dr. Pravindra Kumar (Assistant Professor, Electronics and Communication Engineering Department, Thapar Institute of Engineering & Technology (Deemed to be University), Patiala)** from **5th of January 2026 to 26th of June 2026.** The matter presented in this has not been submitted either in part or full to any other university or institute for the award of any other degree.

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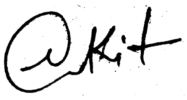
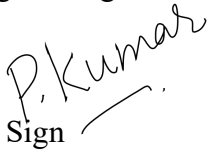
(Name and Sign Industry Supervisor) Name of Industry Supervisor: Govind Krishna Pal Designation: Sr. Staff Engineer  Sign Date: 26 - 06 - 2026	(Name of TIET Supervisor- Dr. Ankit Soni) Designation: Assistant Professor Department of Electronics and Communication Engineering, Thapar Institute of Engineering & Technology, Patiala  Sign Date: 26 - 06 - 2026
	(Name of TIET Supervisor- Dr. Pravindra Kumar) Designation: Assistant Professor Department of Electronics and Communication Engineering, Thapar Institute of Engineering & Technology, Patiala  Sign Date: 26 - 06 - 2026

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This is to certify that **Sourav BHADWAL** has undergone internship in our **MDRF** Group from **July 25, 2025 to June 26, 2026** and has successfully completed the project on: **SXM gen 8.1, Stellar X8, Stellar G5, Stellar P5E.**

During the internship period, Sourav was found to be sincere and professional in conduct.

We wish him all the best for the future endeavors.

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ABSTRACT

Supply noise is a major challenge in advanced integrated circuits (ICs) that can degrade performance and reliability. This work addresses the important problem of supply noise reduction using Decoupling Capacitors (Decaps), SHDMIM (Super High-Density Metal Insulator-Metal) capacitors and Power Grid (PG) fills. With the scaling down of the IC technology and increasing operating frequencies, the stabilization of power supply voltages becomes crucial for proper functioning of the circuit. A complete methodology for accurate estimation and allocation of Decaps and SHDMIM capacitors in IC design is developed using Redhawk-SC tool. This methodology seeks to reduce voltage fluctuations, a major source of supply noise, thereby improving signal integrity and reducing the chances of logic failures. Further, SHDMIM capacitors are complemented with the incorporation of PG fills, which ensures robust power delivery and minimizes the voltage drops in both static and dynamic conditions. This concurrent approach guarantees that the implementation of SHDMIM capacitors and PG does not deteriorate other important parameters such as power consumption and propagation delay. The results shows the need of efficient supply noise suppression methods in advanced ICs and provide useful guidelines to IC designers for better performance and reliability. The analysis reveals that the considerable reduction in voltage fluctuation from 140 mV to 70.5 mV and reduction in settling time from 13.5 to 5.5 ns which results in improved circuit performance with greater signal integrity, lesser error rates and higher reliability. This work provides a detailed analysis and practical implementation strategy demonstrating the potential of SHDMIM capacitors and PG fills as important building blocks to realize noise free, high performance integrated circuits. The present work opens the door to future advances in IC design and optimization.

The proposed methodology involves the generation of Chip Power Model (CPM), which records the dynamic switching current profile of the integrated circuit over a transient window of 1000 ns. This active die model is embedded into a complete co-simulation environment to enable a realistic model of the power supply noise. The specific impedance characteristics of the IC Package and PCB are represented by Parasitic netlists imported using the Chip Model Analyzer tool. Accurate port connections are made to ensure a continuous electrical path to the active transistors from the voltage regulator.

The study gives the magnitude of the time domain voltage fluctuations (ripple) caused by the coupling of the on-chip switching activity with the off-chip parasitic inductance using transient analysis. The results demonstrate that this Die-Package-Board co-analysis provides significantly more accurate ripple estimation compared to standalone simulations. This approach enables early identification of Power Delivery Network (PDN) weaknesses so that required amount of voltage to be reached to the die which will meets the timing and will not result in logic failure. It has been noted that the voltage ripple between Package Node 1 and PCB is 40 mV in 70 ns period of time, the voltage ripple between PCB Ports (16 to 20) is also 40 mV in 70 ns period of time and the voltage ripple between Package Node 2 and Die is 174 mV in 70 ns period of time.

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LISTS OF ABBREVIATIONS

Abbreviations	Full Form
IC	Integrated Circuits
SHDMIM	Super High Density Metal Insulator Metal
PG	Power/Ground
PDN	Power Delivery Network
SoC	System On Chip
DECAP	Decoupling Capacitors
CPM	Chip Power Model
LEF	Library Exchange Format
SPEF	Standard Parasitic Exchange Format
DEF	Design Exchange Format
VCD	Value Change Dump
SDC	Synopsys Design Constraints
NV	Node Voltage
EM	Electromigration View
ESR	Low Equivalent Series Resistance
VRM	Voltage Regulator Module
PCB	Printed Circuit Board
EMI	Electromagnetic Interference
R	Resistance
C	Capacitance
L	Inductance
CMA	Chip Model Analyzer
BGA	Ball Grid Array
STA	Static Timing Analysis
DPB	Die Package Board
ADAS	Advanced Driver Assistance Systems
AI/ML	Artificial Intelligence & Machine Learning
SI	Signal Integrity
PI	Power Integrity

CHAPTER 1: INTRODUCTION

1.1 General

Supply noise is a common problem in the area of advanced integrated circuits (ICs) that can adversely affect reliability and performance [1]. As IC technology advances, circuits are getting smaller and running at higher frequencies, increasing their vulnerability to supply noise. Voltage swings which are known as supply noise can cause a variety of problems such as signal integrity degradation and increase in drop results in higher error rates and even logic failures in the design. These problems require the development of practical solutions to minimize supply noise and to assure the reliable operation of ICs.

1.2 Importance of Supply Noise Reduction

Supply noise reduction is critical to obtain the best performance and reliability of advanced integrated circuits (ICs). Fig 1.1 shows voltage variations due to supply noise which can cause the interruption of operation of transistors and other critical components. This can lead to timing errors, signal integrity problems and even logic failures. Decoupling capacitors and Super High Density Metal Insulator Metal capacitors (SHDMIM) are among the best solutions to get rid of supply noise. This converts these parts into local energy reservoirs that stabilize the power supply voltage by supplying the circuit with instantaneous current [1].

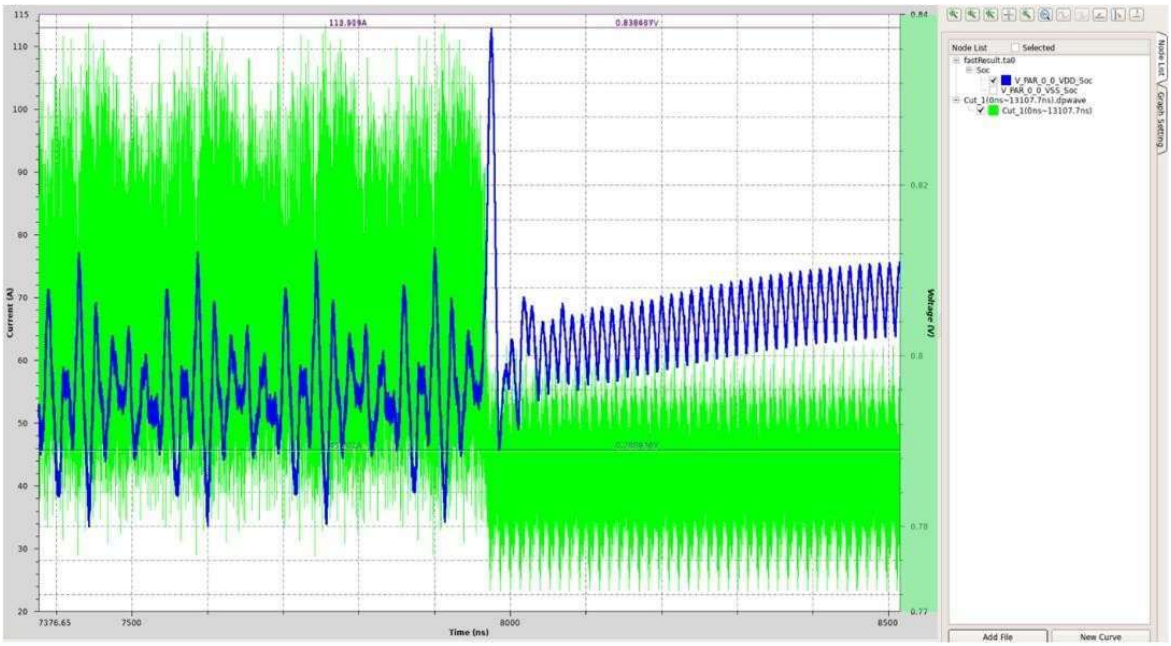

Fig 1.1: Supply noise in IC

The use of decoupling capacitors and Super High Density Metal Insulator Metal (SHDMIM) capacitors should be strategic in placement and exact in value calculation to avoid unwanted effects on other performance characteristics.

1.3. Research Focus and Methodology

The objective of this research is to improve the circuit performance by the efficient removal of supply noise in modern ICs. An integrated technique has been developed to evaluate and place decoupling capacitors in the IC design accurately using the facilities of the Redhawk-SC tool [18]. The main goal is to reduce the voltage swings to improve the signal integrity and to reduce the probability of logic failures. Significant gains in circuit performance have resulted from the methodology's documented reduction in voltage drop. By using decoupling capacitors, PG (Power/Ground) fills and Super High Density Metal Insulator Metal capacitors (SHDMIMs) the voltage fluctuations has been reduced and it helps to reduce the voltage drop and doesn't affect the overall circuit performance and reliability.

The goal of this work is to improve the overall efficiency and reliability of integrated circuits (ICs) via effective mitigations of supply noise which is an important challenge of advanced semiconductor technologies [2].

Noise, which is typically associated with fast switching of transistors and with poor power delivery networks (PDNs), can cause voltage variations that degrade signal integrity and can cause functional errors in digital circuits. The RedHawk-SC tool has been used to provide a reliable and accurate method to evaluate and strategically place decoupling capacitors (decaps) across the IC architecture. Decoupling capacitors are local energy storage devices supplying immediate current during transient switching events and ensuring the voltage stability on the chip [3]. The calculated placement and dimension of the capacitors from the simulation and analysis in RedHawk-SC ensures the proper noise suppression for the critical blocks. The use of decaps is improved with the application of Power/Ground (PG) fills to improve the local power distribution network. By adding more PG in unused layout areas the metal density increases, power grid connectivity improves and resistance reduces, thus helping to alleviate voltage drop across the chip. This combined approach with use of decoupling capacitors, PG fills and SHDMIMs resulted in significant reduction in voltage fluctuations and IR drop.

The research also focus on calculating the overall drop of the design by attaching the chip with package and PCB so that the chip functions properly and it gets the required amount of current needed to perform the all the logic operations in the design. This can be done by using tools like Chip Model Analyzer, by using this tool voltage drop is analyzed for the complete system i.e. SOC attached with Package and PCB. The methodology used is the making of effective resistance and capacitance of all the nodes in the design which is necessary of the Die Package Board Ripple analysis for longer duration so that circuit failure will not happen and the logics can be met without delays.

1.4. Findings and Implications

The findings of this study highlights how crucial efficient supply noise reduction strategies are to the development and improvement of sophisticated integrated circuits. This research provides important information for IC designers to improve the performance and reliability through a detailed analysis and practical implementation plan which results to meets the timing requirements of the chip and logic failure will not happen. The findings describes the potential of decoupling capacitors and SHDMIM capacitors for making high performance, noise free integrated circuits and laying the groundwork for next developments in IC design and optimization [6]. These capacitors acts as a major component to meet current supply in design.

CHAPTER 2: LITERATURE REVIEW

2.1 Previous Research Work

It discusses the fundamental principles and the complex challenges of power integrity management in today's integrated circuits. With increasing complexity of integrated circuits, in-depth studies highlight the critical need for strong on chip power distribution networks and control methods to reduce supply noise [1].

Here, we discuss the use of specialized techniques to estimate dynamic current waveforms by pre-characterizing standard cells for accurate prediction and fulfillment of these power requirements, resulting in accurate dynamic power analysis during testing and design phases [2].

Such advanced power delivery networks are implemented in this paper and correct current estimation models depend heavily on sophisticated Electronic Design Automation (EDA) procedures. Current EDA frameworks provide computer assisted environments that enable the execution of complicated circuit designs that efficiently handle tight power, timing and process technology limitations throughout the full IC implementation flow [4].

It addresses the effect of self heating on electronic connection dependability. The study illustrates temperature changes and uses the decoupling capacitors for lower power consumption and better overall design performance. The IR drop analysis with heat effects allows a more accurate evaluation of the power distribution network performance in real world operating settings. The results indicate that the decoupling capacitors may improve the design performance greatly by reducing the power supply noise and improving the thermal management. The study shows that the consideration of self heating effects leads to more reliable and efficient chip designs and emphasizes the importance of thermal management in the IC design. The paper gives insights on the connection between thermal effects and power integrity and practical methods for designers to construct durable and high performance ICs [5].

This research addresses the critical problem of routing congestion and design rule violations in today's physical design flow by offering a proactive machine learning technique. In this work a Support Vector Machine (SVM) classifier for the short violation prediction and prevention in the clock routing is proposed. Most importantly, this methodology is applied early in the design cycle, prior to power planning and placement, which allows early identification of violation-prone locations. The suggested methodology enables designers to preemptively execute physical layout modifications by precisely predicting these minor violations without time-consuming global routing or late-stage iterations. This early stage prediction significantly reduces the total turnaround time of the place and route process with high routability and less late stage design modifications, finally improving the efficiency of advanced integrated circuit implementation [9].

It addresses the critical power, area and timing challenges of the continuously shrinking semiconductor technology nodes that inevitably lead to localized peak current demand spikes and IR drop hotspots formation. The research proposes a new methodology to alleviate these performance degrading voltage drops using the Pegasus physical verification flow without

impacting established circuit parameters. In particular, the authors suggest a smart post-placement and routing (post PnR) method of adding targeted power and ground fillers/metals in the design. The proposed approach significantly improves the power distribution network robustness and effectively reduces IR drop hot spots by intelligently deploying these metal fills at the sign-off stage, while ensuring that the device's critical timing and overall operational integrity remain completely unaffected [12].

The research investigated the structural and electrical dependability of flip-chip packaging using ANSYS Chip Model Analyzer (CMA) to anticipate the failure modes. Their work explored the influence of thermal mechanical stress induced by the difference in Coefficient of Thermal Expansion (CTE) between the silicon die and the substrate leading to major electrical failures. Through simulation, the scientists showed that the stress concentrations are the greatest at the chip corners, and typically lead to solder bump cracking and trace peeling, which creates electrical open circuits. This work is relevant for the present research since it shows the use of simulation tools to model the complicated interaction of the chip and the package, their methodology underscores that the chip and package cannot be treated as separate entities; the physical interconnects (bumps and traces) are critical variables that define the overall electrical integrity of the system [13].

It demonstrates the significant impact of effective supply noise reduction on enhancing the performance and reliability of advanced integrated circuits (ICs). As technology has progressed, the difficulties associated with power, area, and timing have risen significantly. The shrinking of technology leads to an increase in the number of cells in smaller areas, resulting in a considerable surge in peak current requirement. Moreover, certain regions may experience IR Drop issue due to surge in current demands. Therefore, it is crucial to decrease Drop since it affects the cell's speed and the chip's performance. This paper suggests a method for enhancing IR Drop by implementing metal fills after post- placement and routing without affecting the device's timing [15].

It discusses IR drop in multilayer PCBs and presents a study conducted on the subject using an adaptive mesh to simplify the process. The study found that the vias contact and copper planes of the VRM are major sources of IR drop. To solve this problem, a new method is proposed in the paper which can effectively reduce IR drop by minimizing resistance. The researchers say that PCBs with current demands of 100+Amphere can keep IR drop within a few tens of millivolts, if reasonable design rules are followed [16].

In this paper, we demonstrate the application of the Chip Model Analyzer (CMA) to quantify the voltage ripple in Power Delivery Network (PDN). It is a transition from component level verification to a system level approach. This demonstrates the role of the CMA environment as an integration platform, where the designer can tie a compact frequency-dependent Chip Power Model (CPM) to the parasitic models of the package and PCB. One of the main results stated is that a large ripple is generally caused by the resonance created between the on-die capacitance and the package/board inductance. The relevance of this reference to the present thesis lies in the fact that it offers the direct methodological foundation for the endeavor. It confirms that a simultaneous modeling of the chip switching excitation with the impedance profiles of both the package and the printed circuit board is necessary to accurately estimate the overall ripple [16].

In this study we present a technique for reducing power supply noise in integrated circuits utilizing decoupling capacitors (decaps). The research is based on effective planning and sizing of decaps for noise and leakage power reduction. It demonstrates significant decrease in decap budget and leakage power with low increase in area and wirelength when included in both 2D and 3D floor planners. The process is based on rigorous tradeoff analysis between the decap placement and other design factors, to ensure that the gains in noise reduction are not outweighed by negative consequences on area and wirelength. This paper provides significant insight on efficient decap management in the floor planning phase of integrated circuit design and examines the necessity of strategic decap allocation for noise and leakage reduction. The results demonstrate that decoupling capacitors may be a critical component in the construction of high performance low noise ICs [17].

This work describes the computer-aided design approach for calculation and allocation of decoupling capacitors at physical design stage to reduce power supply noise in System on Chip (SoC) designs. The suggested approach involves a thorough investigation of the power distribution network (PDN) and identification of crucial regions where supply noise is more probable to occur. The method optimizes the positioning of the decoupling capacitors and hence decreases the peak supply noise and improves the performance and reliability of the SOC. The findings of the simulation show a significant decrease of noise with no influence on the cross-sectional area and may be applied to different SoC architectures. This approach illustrates the need of decoupling capacitors for power integrity maintenance in complicated SoC designs and also offers a realistic way for designers to develop noise-free high performance SoCs [19].

It provides a systematic methodology for the design to plan power distribution and grid for power managed designs with focus on practical application scenarios. The work discusses the challenges of dynamic voltage drop analysis and design closure. It provides a complete framework to manage power distribution for modern IC designs. The process involves extensive modeling and simulation of the power distribution network taking into account many aspects such as load changes, switching activity and thermal impacts. The results are based on 28 nm process industrial designs, pointing forth the practical consequences and issues in power distribution management for advanced IC designs. The research highlights the need for strong approaches to assure power integrity and reliable operation in the design. It also provides vital information for designers to accomplish effective power management and design closure in current ICs [20].

In this study, a strategy is described to alleviate voltage dips on supply rails in sub-V T circuits, which can lead to lower noise margins and increased switching noise. A case study exhibits the approach and detailed IR drop analysis of multiple technology possibilities in a 28nm CMOS family. The results demonstrate a reduction of 50% in voltage drops compared to a clocked design. This can help increase circuit reliability by decreasing errors caused by IR drop and improving noise margins. This approach is especially useful for very integrated circuit designs working in subthreshold voltage regimes [23].

This paper provides a novel way to tackle the power delivery problem in voltage island designs which are widely used for power saving in low power design. The proposed approach considers the voltage drop effects during the floor planning phase to reduce the number of design iterations. This means that the power/ground (P/G) network pitch is not needed to be considered in the floorplan stage, which allows the simplified searching technique to generate a more

robust low power design within a reasonable runtime. The experimental results demonstrate the effectiveness of this approach and its potential to reduce the design effort and improve the robustness of voltage island designs, thus contributing to more efficient and reliable low-power integrated circuits [25].

It provides a proposed solution to the problem of IR-drop in contemporary VLSI designs which has become a serious issue in the nanometer era. Limited tools are available for detecting this problem early on, and existing approaches at the gate level often require additional characterization. The paper proposes an analytical method for estimating IR- drop values without requiring additional information and can accurately obtain supply current waveforms and IR drop values for any given supply resistance by modifying data in standard libraries and events in activity files. The paper includes experiments conducted on several circuits to demonstrate the effectiveness of the proposed method [29].

The paper presents a physical-location-aware X-identification method designed to enhance the effectiveness of X- filling in reducing IR-drop during at-speed scan testing of ASICs. The method strategically redistributes X-bits to minimize maximum switching activity, thereby reducing IR drop. The effectiveness of this approach is estimated using RedHawk tool and experimental results on ITC'99 benchmarks are impressive. The proposed method is superior to the prior methods that distribute X-bits uniformly among all the test vectors, with an average reduction of 9.42% in the maximum IR-drop [31].

It discusses about IR voltage drop in nanometer technology and the lack of tools to tackle it. The propose a new feature in Redhawk to resolve EM and IR voltage drop and simplify the process by eliminating the manual steps. They study a DDR memory block, and propose to use metal strips and a stronger PDN to mitigate the hotspots, achieving IR voltage drop values below 2% of VDD and EM violation values of around 83%. They conclude that their approach can reduce IR voltage drop and EM violations and allow signoff with a stronger PDN and metal strip addition [32].

The paper proposes advanced techniques for improvement at the sign off stage to address the critical issue of IR drop in power delivery networks. The proposed approach selects effective locations to improve power rail connectivity while using fewer routing resources. The method has been implemented and validated by industry standard tools such as IC Compiler and Red Hawk Explorer. The experimental results are interesting for reducing drop and the proposed approach can significantly improve the worst case IR drop, e.g. 57.8% reduction at the sign-off stage. This enhancement improves the performance of the power delivery network, and ensures the reliability and efficiency of the integrated circuits, making the approach a valuable contribution to the power integrity field for drop reduction [33].

In this study, the benefits of employing MIMCAPs in FPGA designs are presented. The study reveals that MIMCAPs implemented on an interposer can greatly improve the power integrity and performance of FPGAs. The authors demonstrate the usage of MIMCAPs minimizes power supply noise and IR drop in the design which leads to an improvement in signal integrity and overall system performance using sophisticated modeling tools. The experimental results showed a significant enhancement in the performance metrics of FPGAs, strongly supporting the use of MIMCAPs in high-performance FPGA designs [34].

2.2 Problem Statement

From the literature, it is evident that supply noise is a serious problem in advanced integrated circuits (ICs) and has adverse effects on performance and reliability. Usually, common techniques to reduce power supply noise such as the use of decoupling capacitors (decaps) require complex planning and result in longer wires and more area. Moreover, the accurate calculation and allocation of decaps during the physical design phase of System-on-Chip (SoC) design is problematic and needs close optimization to avoid negative effects on power consumption and latency [4].

This research aims at devising a simpler way for successful use of SHDMIM (Super High Density Metal Insulator Metal) capacitors using sophisticated IR drop analysis techniques using CAD tools such as RedHawk-SC. SHDMIM capacitors feature high capacitance density and self healing capability which is useful for removing low frequency noise and boosting power integrity [5]. The technique is aimed at reducing voltage swings, enhancing signal integrity and decreasing the probability of logic failure by judiciously placing SHDMIM capacitors and augmenting them with power grid (PG) fills. The goal is to achieve significant supply noise reduction with minimum increases in latency and power consumption, giving practical solutions for IC designers to better performance and reliability in high-density VLSI designs.

For the overall calculation of voltage drop, the research focus on creating a waveform of peak current in the design by using the switching activity from VCD file and by taking effective resistance of die and capacitance of die of SOC to measure the overall drop in the design.

A prototype is made by connecting chip with package and PCB by using tools like Chip Model Analyzer to measure the ripple in the design and gain the required current in the design which leads to the proper working of chip and improved performance. High performance System on Chip (SoC) are subject to large dynamic voltage drops (ripple) on their power supply rails as a consequence of aggressive clock gating and high switching activity of logic blocks. Current methodologies for analyzing the ripple mainly focus either on computation of full wave simulations which take days to run or static DC analysis which fails to capture transient noise events so Chip Power Model (CPM) is generated and extended for longer duration to analyze voltage drop for longer duration.

CHAPTER 3: METHODOLOGY

3.1 IR Drop Analysis

In the technique of this research, the RedHawk-SC tool, a leading CAD tool that is often used for power integrity and reliability analysis in advanced integrated circuits (ICs), is utilized to do a comprehensive IR drop analysis. The first step in the process is to import the IC design which includes the netlist, physical layout, and relevant technology files into the RedHawk-SC tool. The design setup is designed to incorporate power and ground networks, along with the initial placement of decoupling capacitors (decaps) [4].

After the design is configured, RedHawk-SC thoroughly examines the power distribution network (PDN) to find possible IR drop locations. The power grid is simulated by the program under a variety of operational settings, such as varying load scenarios and switching actions. Understanding the distribution of voltage drops throughout the network and identifying hotspots where the voltage drop surpasses allowable limits, potentially resulting in performance deterioration and logic failures, depend heavily on this power grid study [1].

Prime Time is a software used to generate timing file which provides frequency at which the SOC operates. This timing file acts as the input of RedHawk- SC tool and this file is generated in .twf format.

Redhawk-SC tool is used for Chip Power Model generation which is used to identify the peak current in the SOC which helps to identify the overall current demanded by the SOC.

Chip Model Analyzer Tool is used analyze the overall drop by attaching chip with package and with PCB in order to check the functionality of the chip so that it gets the required current after attaching package and PCB which do not lead to circuit failure.

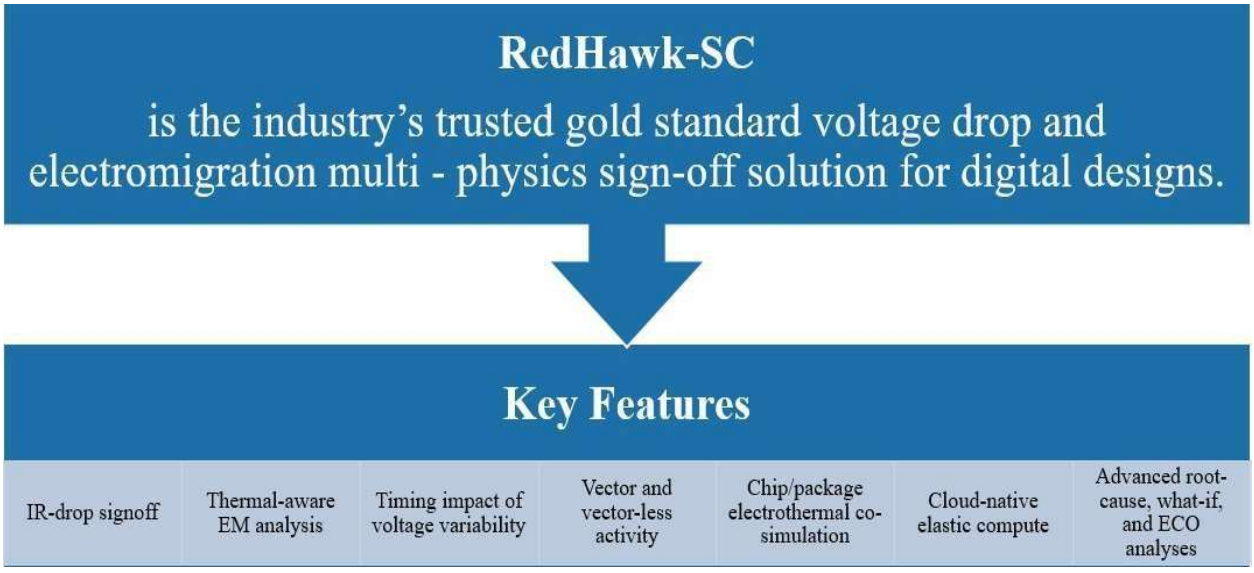

Fig 3.1 RedHawk-SC Tool overview

3.2 Analysis Flow Chart

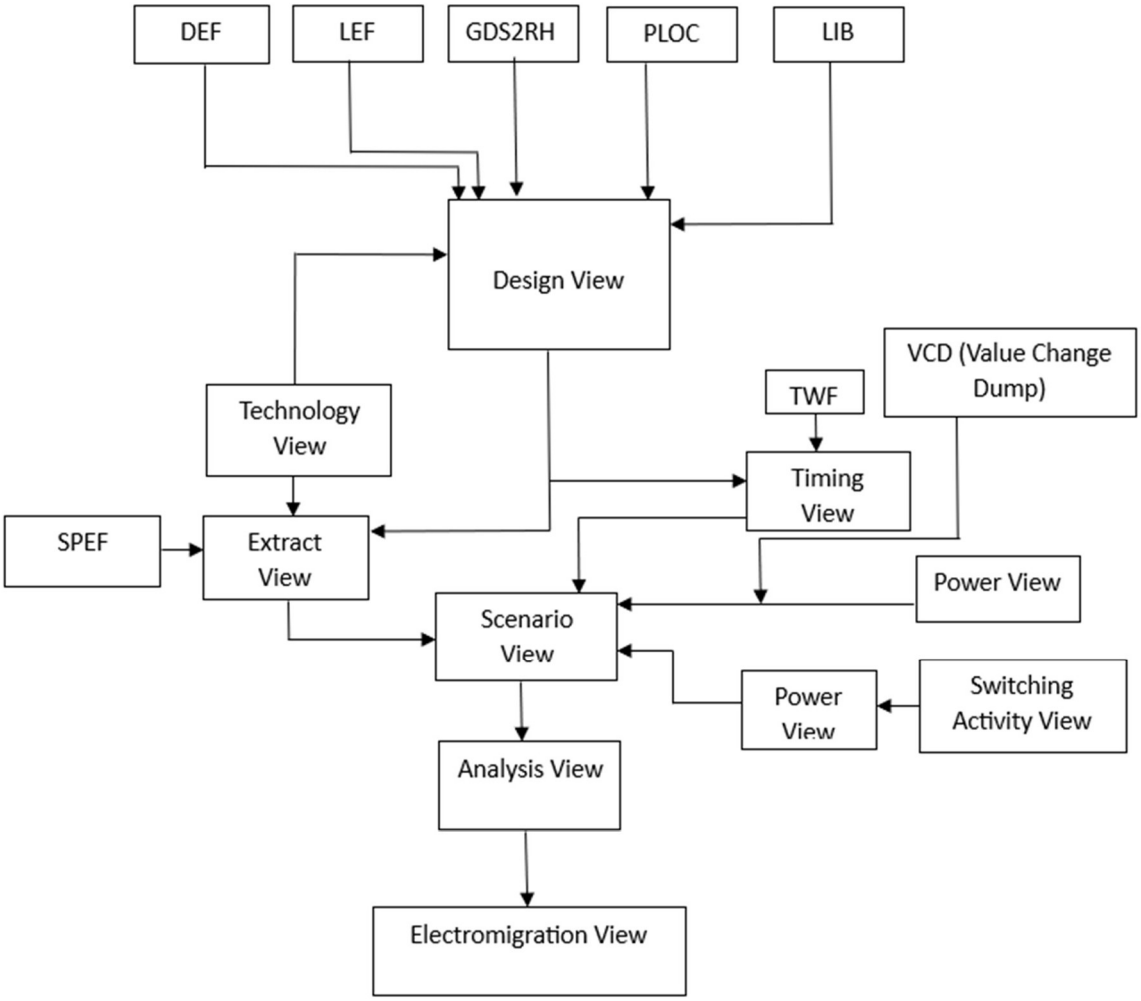

Fig 3.2 Redhawk-SC Tool Flow Analysis

3.3 Simulation Work

Data required for importing design and extracting R, C, L and power related information such as static and dynamic power and timing information like slew, frequency and toggle rate are provided in the form of files as shown in Fig 3.2 represents the work flow of RedHawk-SC tool, where various views are created to read the required input files for voltage drop analysis.

LIB File: The LIB file is a timing model that includes cell delays, transitions, and setup and hold time requirements. It is generated using CCS (Composite Current Source) and NLDM (Non-Linear Delay Model) techniques. Among other important units, the file includes static and dynamic power.

LEF File (Library Exchange Format): The LEF file contains the pin connection between instances and between instance to power/ground bumps. Without the pin connection, the power

of that particular instance is not calculated. The pin can be input, in-out or output.

SPEF File (Standard Parasitic Exchange Format): The SPEF file contains the parasitic information. It includes the R (resistance) and C (capacitance) values of the grid in the design.

DEF File (Design Exchange Format): The DEF file contains the physical information such as the placement of macros, bumps, and metal nets, instances names.

Tech File: The tech file includes the metal layers height and width definitions, vias height and width.
Technology view reads the Tech file

VCD File: The VCD file provides the switching factor which is used for power calculation. It provides the toggle rate which shows how the instance toggles with respect to clock.

Pg.ploc File: The pg.ploc file shows the locations of power and ground bumps including their names, coordinates, and the metal layer on which they are placed. This file is necessary in the design for defining the bumps in the power distribution network.

TWF File: The TWF file provides the information about slew, transition, frequency, and timing windows which are used in power and IR drop calculations. The Verilog file which is required for generating timing file provides connectivity and placement details for the logical elements of the design.

Process:

1. These all files LIB, LEF, DEF, PLOC, GDS2RH and Tech file acts as an input file to Design View.

2. After this view, technology view is created which reads the Tech file and then this view is used by extract view. In addition to technology view, extract view reads SPEF file and design view also.

3. Timing view is generated by using twf file and design view. It calculates the pin slew information of all the instances and provide the frequency information used in the design.

4. Then scenario view is created which reads the design view, extract view, timing view, vcd file and power view to determine the peak voltage level where current consumption requirement is high. Power view calculate the power of all the instances used in the design and switching activity view reads the data toggle rate, clock toggle rate in addition it also reads extract view and technology view.

5. In Analysis view, we analyze all the results and then electromigration view is created to check the current limit on power/ground nets as well as signal and clock nets.

3.4 Script Design

```
apl_files=[
      {'file_name':'/prj/frontend/RELEASE@1.00.01/AG_P28_MEM_HEMP/APACHE/ELECTRICAL/SR6_ff28_0.93V_0.00V_m0.10V_150C_s
igmax.cdev'}
       {'file_name':'/prj/frontend/RELEASE@1.00.01/AG_P28_MEM_HTMP/APACHE/ELECTRICAL/SR6_ff28_0.93V_0.00V_m0.10V_150C_
sigmax.cdev'}
        {'file_name':'/prj/frontend/RELEASE@1.00.01/STA1_P28_MEM_SPREG/APACHE/ELECTRICAL/SR6_ff28_0.93V_0.00V_m0.10V_1
50C_sigmax.cdev'}
         {'file_name':'/prj/frontend/RELEASE@1.00.01/PMU1_P28_MEM_HEMP/APACHE/ELECTRICAL/SR6_ff28_0.93V_0.00V_m0.10V_1
50C_sigmax.cdev'}
          {'file_name':'/prj/frontend/RELEASE@1.00.01/COMSHIFT_P28_MEM_HEMP/APACHE/ELECTRICAL/SR6_ff28_0.88V_0.00V_m0.
10V_150C_sigmax.cdev'}
           {'file_name':'/prj/frontend/RELEASE@1.00.01/ADG_P28_MEM_HEMP/APACHE/ELECTRICAL/SR6_ff28_0.97V_0.00V_m0.10V_
150C_sigmax.cdev'}
           ]
```

Fig 3.3 IR script snapshot

Fig 3.3 shows a script written in python and it exhibits the use of APL files in IR drop analysis. These files offer detailed information about the switching activity and power consumption patterns of the IC components. Redhawk-SC imports the APL files in order to simulate realistic activity profiles during the IR drop analysis. This guarantees realistic modeling of the power distribution network (PDN) under different load scenarios.

```
swa = db.create_switching_activity_view(timing_view=tv,
      vcd_files=vcd_files, value_change_data=None, tag='swa1',
      propagation_style='assign_default_activity', use_sta_clock_info=True,
      settings=settings, options=options)


evx = db.create_extract_view_from_files(dv, input_files=spef_files, tag='evx',
      options=options)


pwr = db.create_power_view_from_switching_activity(swa,
      timing_view=tv, options=options, voltage_levels=voltage_levels,
      external_parasitics=evx, tag='pwr',
      current_data_precedence=['APL','NLPM','CCSPOWER'])



ev =  db.create_extract_view(dv, tech_view=nv,
      calculate_spr=False, temperature=125, options=options, tag='ev', mode='pg')


ev_signal = db.create_extract_view(dv, tech_view=nv, calculate_spr=False,
            temperature=125, options=options, tag='ev_signal', mode='signal')


sv = db.create_simulation_view(ev, enable_reduction=True,
     options=options, tag='sv')


sv_sigem = db.create_simulation_view(ev_signal, enable_reduction=True,
           options=options, tag='sv_sigem', sim_type='sigem')
```

Fig 3.4 Input Files in the main run script

Views Created After the IR Drop Analysis with RedHawk-SC

Several significant perspectives are produced following the IR drop analysis using the RedHawk-SC tool to offer thorough insights into the integrated circuit's (IC) power integrity and performance. Fig 3.4 shows the views that include the Design View (DV), Node Voltage, Thermal view, extract view, EM (Electromigration View) and power view. Each of these views has a distinct function and provides comprehensive data that is essential for more research and enhancement.

1. **Design View:** The Design View is the basic view that contains the physical information about the design like the placement of standard cells, macros, bump placement location and the metal layer names and their location. It provides complete description of the layout of the circuit including placement and connections of the components. This view is important for the setting up of the basic conditions for the IR drop analysis and is the basis for the creation of further views.

2. **NV (Technology) View:** The technology view will provide the information about the metal layers used in the design, about the supply voltage and provide information about the vias. It represents the information about the thickness, minimum and maximum width of vias and metal layers.

3. **EM (Electromigration) View:** The EM view represents that the metal atoms in interconnects gradually move due to high current densities, potentially results in the excess current flowing through the metal wires due to which metal wires can break and it results in logic failure. This view provides insights into the current density and identifies locations which exceeds the current limit. The EM View allows designers to use techniques to enhance the lifetime and reliability of the IC.

4. **Thermal View:** The Thermal View incorporates thermal factors into the study, providing a realistic evaluation of the IC's performance at various temperature settings. It assesses the impact of temperature changes on IR drop and overall power integrity. This view is important as it allows heat management to be naturally integrated into the design flow, resulting in more robust and efficient IC architectures [8].

5. **Decap Placement View:** The Decap Placement View shows the best places to put the decoupling capacitors (decaps) depending on the IR drop and thermal analysis. It gives a strategic map for decap placements to stabilize the power supply voltage and reduce the supply noise. This view helps in fine tuning the design to get a significant noise reduction with minimal impact to other performance parameters [7].

6. **Power View:** This view is used to calculate the power of all the instances used in the design. It includes macros, memory blocks, standard cells, level shifters etc.

3.5 Concept Of Decoupling Capacitors in the Design

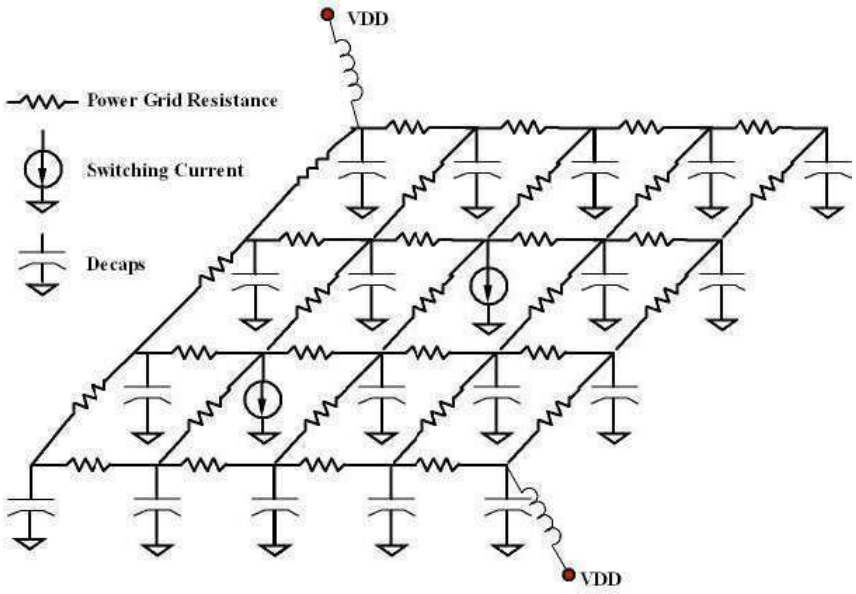

Fig 3.5 Decoupling capacitor schematic

Fig 3.5 shows decoupling capacitor, which is used to decouple the critical cells from main power supply, in order to protect the cells from the disturbance occurring in the power distribution lines and source. These capacitors are strategically placed within the IC design to mitigate supply noise, which can adversely affect circuit performance and lead to logic failures [8].

Decoupling capacitors act as local energy reservoirs, providing immediate current to the circuit components during transient events[5]. Decaps provide the required charge when an abrupt need for current occurs, like during switching operations, preventing large voltage reductions in the power supply network. Fig 3.6 shows the Power Delivery Network which is basically a metal stack representing Power (VDD) and Ground (VSS) metals. This stabilization of the power supply voltage is crucial for ensuring the proper functioning of high-speed and high- frequency circuits [3].

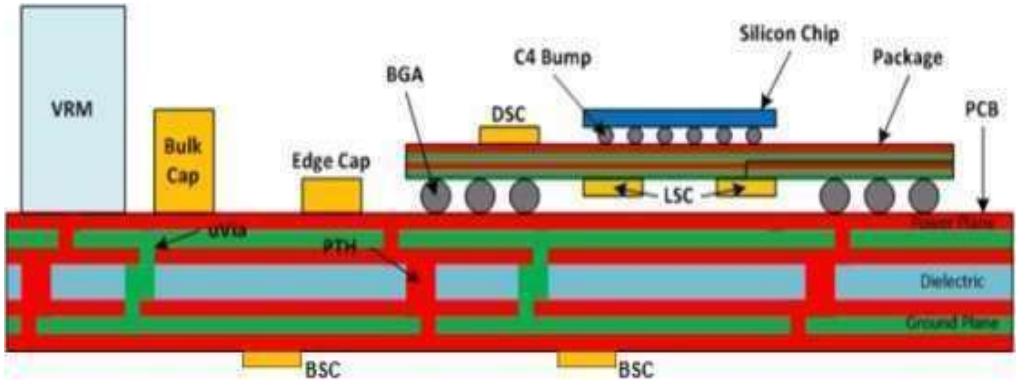

Fig 3.6 Power Delivery network

Designers incorporate decaps (decoupling capacitors) into a chip to mitigate the impact of noise on the power mesh. Decoupling capacitors serve to bypass or disconnect power supply noise and voltage transients from sensitive components, keeping a constant voltage. Typically, capacitors are placed near the power and ground pins of components to give a least resistance path to noise, which helps lessen voltage swings arising from noise. Decaps may be normal capacitors or unique constructions aimed at high frequency performance [3]. In a typical design there could be hundreds or even thousands of decaps with varied capacitance values to cover a broad spectrum of noise frequencies. With technology expanding, power and ground networks are becoming increasing resistive and inductive, hence increasing IR loss and noise. This can cause issues with signal integrity and a reduction in noise margins. The voltage fluctuation caused by switching activities can be reduced and the noise margins can be improved by adding decoupling capacitors (decaps) to the P/G network [8].

Designers include decaps to improve the performance and reliability of the design by reducing the dynamic voltage fluctuations arising during switching activity. So when big drivers switch, decaps can provide a current source reducing IR and L di/dt voltage dips. This can help to keep the desired average and peak voltages within their noise limits. Decaps supply a local charge source to minimize the effects of voltage transients and power grid noise on sensitive components. The impact of these transients and noise could lead to unacceptable fluctuations in target voltage. Decaps can therefore aid in preserving a steady voltage and halting circuit performance deterioration. To lower IR drop, white space decaps are used, they are typically composed of NMOS that are positioned between blocks in the open sections of the chip. They serve as high frequency filters that reduce HF noise on supply voltage. The capacitance value of these decaps is determined based on range of noise that needs to be cut out. High-value capacitors (e.g., 1uF or larger) can filter out low frequency noise, while smaller capacitors (e.g., 0.1uF) can filter out high-frequency noise. A combination of capacitors with different values can provide effective filtering for a wide range of frequencies [5]. Placing decoupling capacitors near to the supply pins can reduce the length of the power supply traces, which in turn reduces the parasitic inductance of the traces. This is important because parasitic inductance can limit the strength of decaps in filtering out HF noise supply voltage. By reducing parasitic inductance, the capacitors can more effectively give least resistance path to ground for HF noise, reducing noise-induced voltage fluctuations.

The Fig 3.7 shows the difference in drop between with and without decaps.

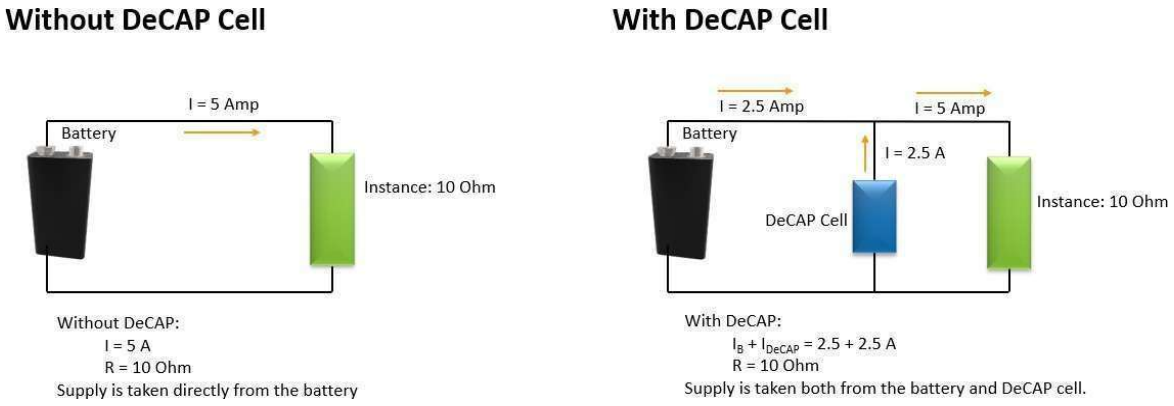

Fig 3.7 with or without Decap

3.6 Concept Of Power/Ground Fills in the Design

To strengthen the power grid (PG) in chip design, various techniques are employed, such as adding more metal layers to the PG, increasing the width of power rails, using thicker metal wires, and placing decoupling capacitors strategically to reduce IR drop. These techniques help to ensure that the power is distributed evenly across the chip, and the voltage drop is minimized. Additionally, simulations and tests are performed to evaluate the robustness and efficiency of the PG design, and improvements are made accordingly [2]. Traditionally, once the routing process is complete, vacant areas in the design are filled with dummy metal to prevent violation. Power Ground Fill addition is an alternative approach to inserting dummy metal Fills in empty spaces during chip design. Instead of dummy metal, PG fills put into vacant spaces to connect with the PG grid, as illustrated Figure. This method enhances the current distribution efficiency by ensuring that PG Fills are distributed evenly.

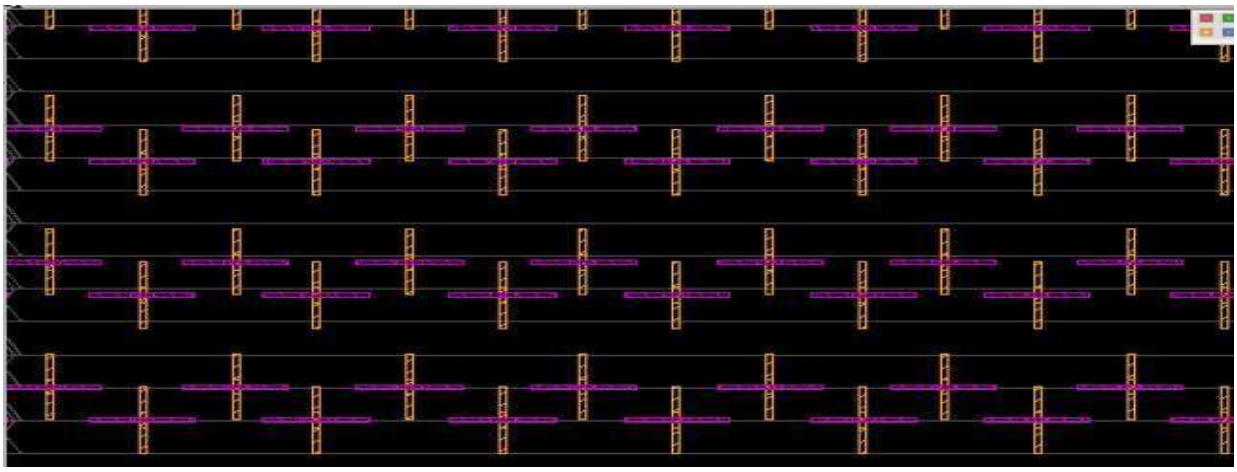

Fig 3.8 Before Smart PG fills

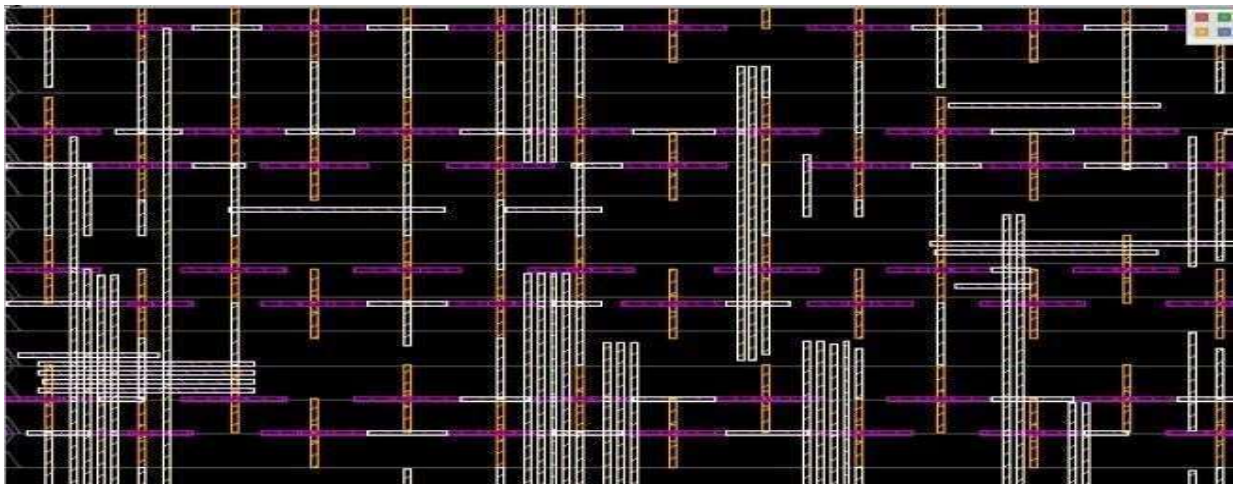

Fig 3.9 After Smart PG fills

To minimize IR-Drop, the power grid must supply each instance in the design with the least possible voltage drop. The current power grid design employs a mesh-like structure with a uniformly distributed metal stripe as shown in above Fig 3.9.

The distribution of cells is not uniform after time closure. However, the typical way is to utilize equally spaced power stripes for stippling. This is insufficient to meet the region's power needs. After timing closure and routing, Smart PG Fills are added to the design to resolve the mismatch between power supply and design location. These PG Fills are timing-aware and will inject metal fills into the unoccupied sections of the power grid. Lower IR drop is the outcome of the clever addition of PG Fills, which guarantee appropriate current distribution across the chip.

Power Ground Grid Strengthening: There are two types of grids strengthening methods:

1. **Manual Power Ground Grid Strengthening**: Manual PG (Power Grid) strengthening refers to the process of manually adding more power grid structures to a design in order to increase its power distribution and eliminate IR drop difficulties [27]. With this procedure, high voltage drop locations of the design are detected and additional power grid structures such as metal straps, vias or power rails are manually added to these areas. The manual strengthening of PG is a tedious process that requires a high level of skill and experience [20]. It may also require changes to the original design, along with further simulations to ensure that the new grid structures do not create any new problems or negatively impact the performance of the design. Manual PG reinforcement, although difficult, can be a successful method to solve IR drop problems in certain situations, particularly those with large or complicated power grids. The problem with this method is that it is not successful for large devices which has many occurrences of IR drop violations and have a considerable amount of dynamic power loss. In some circumstances manual PG strengthening may not be a useful in the design [14]. The drawback with this strategy is that it is not efficient for large designs having more dynamic power loss and having instances with more IR drop violations. In such cases, manual PG strengthening may not be a viable solution.

2. **Power/ Ground Grid Strengthening with Pegasus flow** Traditionally, once the design has been routed, empty regions are filled with dummy metal fills to prevent Violations. In Power Ground fill insertion, alternatively putting dummy fills, power grid fills are put into empty spaces in conjunction with the Power Ground grid [32]. The insertion of PG fills can enhance the current distribution in the power grid by generating supplementary parallel routes for the current to pass through. By doing so, it aids in locating the shortest current path, which ultimately lowers the current density in the power net. As a result, the cells may experience fewer drop problems. Therefore, by implementing Power/Ground fill insertion, the design can experience a more efficient distribution of current therefore reducing IR drop and resulting in improved performance [12].

3.7 Concept Of SHDMIM Capacitors in the Design

A Super High-Density Metal-Insulator-Metal (SHDMIM) capacitor is an advanced type of capacitor designed to enhance power integrity and reduce noise in integrated circuits (ICs). To reduce low frequency noise and enhance the power supply's overall stability, SHDMIM capacitors are thoughtfully incorporated into the power delivery network [34].

Compared to conventional decoupling capacitors (decaps), SHDMIM capacitors have a number of advantages. A high capacitance density means they can pack a lot of capacitance into a small area. This high density is important to sustain stable power supply levels in densely packed IC designs found in modern Fin FET nodes [34].

SHDMIM capacitors can be regarded as enhanced decoupling capacitors. They are primarily used as local energy reservoirs. They store and supply charge during instant current requirements in the design like switching operations to avoid large voltage drops in the power supply network. High speed and high frequency circuits require a stable power supply voltage for proper operation [17].

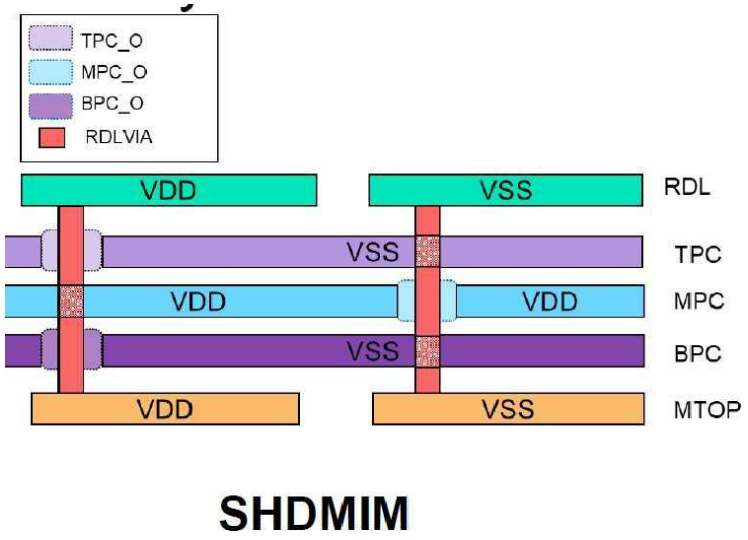

Fig 3.10 SHDMIM Capacitor Structure

Key Features and Benefits of SHDMIM Capacitors:

1. **High Capacitance Density:** The SHDMIM capacitors offer high capacitance density which is ideal for space limited applications. This high density is useful in design for steady power supply [34].
2. **Low Equivalent Series Resistance (ESR) and Inductance (L):** The SHDMIM capacitors provide low ESR and L, which is highly critical for effective noise suppression. Low ESR and L ensures that the capacitors can respond quickly to short events and provide a low impedance route for noise decreasing the voltage fluctuations.
3. **Self Healing Characteristics:** Self healing properties of SHDMIM capacitors enhance the reliability and durability of design. This feature allows recovery of dielectric failures and efficient operation of capacitors for long term usage in IC designs.

4. **Effective Low Frequency Noise Reduction:** SHDMIM capacitors are especially efficient in reducing low frequency noise which is generally created by oscillations in the load and the power supply. These capacitors filter the low frequency noise which is necessary for the proper operation of the system and helps to maintain the power supply clean and stable [22].
5. **Better Transient Response:** The SHDMIM capacitors provides high capacitance density and have low ESR/L which results in improved transient response. This means little or no interference with circuit operation as the capacitors can establish the voltage levels after short events quite fast [23].
6. **Better Power Integrity:** SHDMIM capacitors help in the overall power integrity of the IC by providing a steady power supply and reducing the voltage noise. This improvement leads to increased performance, lower error rates and higher reliability of the system [10].

Incorporated in the Design:

In order to reduce the effects of noise on the power mesh, designers add decoupling capacitors to the power delivery network with SHDMIM capacitors. These capacitors are installed close to key components and power distribution paths to provide instantaneous charge for short duration events. The optimal placement of SHDMIM capacitors guarantees the possibility of effectively suppressing low-frequency noise and stabilizing the power supply voltage [17]. When integrating SHDMIM capacitors, the capacitance values to be used in the design should be taken into account, with consideration of the specific noise frequencies. When we combine capacitors of different values then it allows for effective filtering of noise over a wide range of frequencies which in return will fulfill the current demands of the chip.

SHDMIM capacitors provides an efficient way to improve power integrity and noise reduction in integrated circuit designs. They are an integral part of modern high-performance IC designs because of their high capacitance density, low ESR/ESL, self-healing properties and efficient low-frequency noise suppression. SHDMIM capacitors offer considerable improvements in power stability, noise immunity and overall circuit performance to designers, overcoming critical challenges in the development of semiconductor technologies [34].

3.8 Concept Of Chip Power Model

A CPM is a compact macro-model that represents the electrical power characteristics of a silicon die. Instead of modeling millions of transistors and resistors, the CPM simplifies the chip into a "black box" that behaves exactly like the real chip from the perspective of the power supply. It contains three main components:

1. **Current Profile (I(t)):** A current vs time domain waveform is generated by the RedHawk-SC tool which represents the maximum current demanded by the chip by considering the on die capacitance and resistance values.
2. **Parasitics (R and C):**
   - On-die Capacitance (C die): The aggregate capacitance (intrinsic device capacitance and explicit decoupling capacitance) that aids in voltage stabilization.
   - On-die Resistance: The resistance of the power grid (PG) metal layers.
3. **Spatial Information:** The specific (x, y) coordinates of the C4 bumps (power and ground connection points) so the package designer knows exactly where current is being injected.

3.9 Need of CPM in SOC

1. IP Protection: It hides the internal standard cells, routing, and logic depth. It only reveals how much current is pulled at the bumps.

2. Simulation Speed: Simulating a package/board with a full transistor-level chip model is computationally impossible. A CPM reduces the complexity, allowing system-level tools (like Ansys Redhawk-SC) to run simulations in minutes rather than weeks.

3. Accurate Co-Design: It allows "Chip-Package-System" co-simulation. The package designer can see if the package inductance (L pkg) will cause a voltage drop (V=L* dt/di) that may affect the chip's functionality.

3.10 CPM Generation Process in RedHawk-SC

The Ansys RedHawk tool calculates a CPM by essentially compressing the massive electrical database of the chip into a manageable format. The process transforms a physical layout into an electrical network through the following workflow:

1. Activity Profiling (The "Source")

- RedHawk begins by determining "when" and "how much" current is required. It reads simulation through activity file such as VCD file to analyze the switching of logic gates.
- Calculation: For every instance whenever it switches its state from (0 to 1 or 1 to 0), the tool calculates the dynamic current (I dynamic) based on the cell's internal energy definition described in the .lib files. So, a set of time-domain current waveforms distributed spatially across the die area.

2. Power Delivery Network (PDN) Extraction

- The tool then analyzes the physical metal layers (M1 through top metal) to build a resistive and capacitive model of the power grid.
- Resistance (R): It extracts the resistance of the metal wires used in the grid for providing power supply to all the instances used in the design.
- Capacitance (C): In this process the RedHawk-SC tool calculates the total on-die capacitance of the SOC, which includes:
  (a) Intrinsic Capacitance: It consists of capacitance values from the logic gates and wires.
  (b) Decoupling Capacitance: It consists of decoupling capacitors placed on the SOC to store charge.

3. Spatial Mapping to Ports

- The CPM is strictly "bump-accurate." RedHawk maps the distributed switching currents and parasitics to the specific (x, y) coordinates of the power and ground bumps. Instead of seeing current drawn at a specific transistor in the middle of a block, the CPM represents that current being drawn from the nearest group of power bumps.

4. Final Output Generation

- The resulting CPM file typically contains two distinct electrical behaviors working in parallel:
  (a) Current Model: A set of current sources representing the active load.
  (b) Passive Model: A sub-circuit representing the R (resistance) and C (capacitance) of the die.

```
* CPM Port Name | Average current (A) | Max. magnitude of current
* PAR_0_0_vdd 0.742843 3.66168 0.818
* Average power = 0.607646 W.

Icursig1 PAR_0_0_vdd PAR_0_0_gnd pwl(
+ 0.000000ps      0.16759792
+ 10.000000ps      0.16761198
+ 20.000000ps      0.16760421
+ 29.999999ps      0.16757013
+ 40.000000ps      0.16753283
+ 50.000001ps      0.16749722
+ 59.999998ps      0.16745779
+ 69.999999ps       0.1675054
+ 80.000000ps      0.16815276
+ 90.000001ps      0.16924682
+ 100.000001ps      0.17139286
+ 110.000002ps       0.1738625
+ 119.999996ps       0.1774112
+ 129.999997ps      0.18322629
+ 139.999998ps      0.19260176
+ 149.999999ps      0.20242283
+ 159.999999ps      0.21481779
+ 170.000000ps      0.22515353
+ 180.000001ps      0.23385492
+ 190.000002ps      0.24127421
+ 200.000003ps      0.24774498
+ 210.000003ps      0.25123043
+ 220.000004ps      0.25675711
+ 230.000005ps      0.26784011
```

Fig 3.11 Coordinate Values of Current vs Time

The peak current shows the maximum current used in the SOC design. Here the peak current consumption depends on the switching factor which shows the how much current to be consumed in the design. These current values of maximum consumption are read from VCD file. This file provides the information about switching activity in the design. Fig 3.11 shows the coordinates values of current vs time, it has values of maximum current used in the design so that we are able to identify whether after the voltage fluctuations in the design, is the design still gets the required amount of current for proper functioning without any logic failure.

```
C0_1 PAR_0_0_vdd PAR_0_0_gnd 3.6405523707e-10
R_1_1 PAR_0_0_vdd n3 0.00211821779174
C_1_1 n3 PAR_0_0_gnd 1.98317997733e-09
R_2_1 PAR_0_0_vdd n4 0.00174168705822
C_2_1 n4 PAR_0_0_gnd 6.94894024044e-09
R_3_1 PAR_0_0_vdd n5 0.00173011652602
C_3_1 n5 PAR_0_0_gnd 1.24174073767e-08
R_4_1 PAR_0_0_vdd n6 0.00478290130076
C_4_1 n6 PAR_0_0_gnd 8.00121809788e-09
R_5_1 PAR_0_0_vdd n7 0.00615601660316
C_5_1 n7 PAR_0_0_gnd 1.13390773871e-08
R_6_1 PAR_0_0_vdd n8 0.0133398315159
```

Fig 3.12 R, L & C values of Nodes in the design

Fig 3.12 shows the R, L & C values of the nodes used as the connecting points in the design. The Redhawk-SC tool calculate the R,L & C values of all the nodes used in the design. After considering these R, L & C values, the required amount of voltage is applied to the design so that the current requirement in the design can be met [14].

3.11 Concept Of Die Package Board Ripple Analysis

In modern high-speed semiconductor design, the stability of the Power Delivery Network (PDN) is a critical determinant of system performance. Integrated circuits (ICs) generally operate at lower supply voltages, have high frequency and are more susceptible to voltage variations.

Ripple Analysis is a specialized verification method that is used to assess voltage noise (ripple) over the whole power distribution network such as from the Voltage Regulator Module (VRM) on the Printed Circuit Board (PCB), through the IC package and to the silicon die. This analysis is important for preventing timing violations, logical errors and electromagnetic interference (EMI) [1]. The major problem in power integrity is the occurrence of voltage noise owing to transient current demands. When the transistors on a die switch, they cause a rapid increase in current (di/dt). This transient current interacts with parasitic inductance (L) and resistance (R) of the PDN which causes a voltage drop. This noise will show up as a ripple in the voltage, a variation superimposed on the nominal DC supply voltage [4]. The analysis aims to check that the voltage at the die bump is within the allowed range (typically +-5% or +-3%).

Role of Chip Model Analyzer (CMA): Chip Model Analyzer (Ansys Tool) has been used for Die Package Board Ripple Analysis. Traditional board-level simulation often treats the integrated circuit as a static current load, ignoring the dynamic interaction between the die and the board. The Chip Model Analyzer (CMA) allows a system level co-simulation that includes a high fidelity behavioral model of the die that overcomes this limitation. What is different about the CMA workflow is the use of the Chip Power Model (CPM). However, a CPM includes:

- **Spatial Granularity:** Current demands are mapped to specific bump locations rather than one single node.
- **On Die Parasitics:** It takes into account the inherent resistance and capacitance of the silicon substrate (R die & C die) which act as a natural filter for high frequency noise.
- **Dynamic Current Profiles:** It uses real switching waveforms derived from vector based activity simulations done by the tool.

3.12 Analysis Methodology and Workflow

Typically, a ripple analysis process in a CMA tool is executed in four steps:

a) System Assembly: The electrical models of the system components are cascaded to form the simulation environment. This leads to a hierarchical netlist:

- VRM Model: It defines the voltage source and its regulation bandwidth.
- PCB and Package Models: It is usually extracted as S-parameters or parasitic RLC netlists, describing the physical interconnects.
- Decoupling Capacitors (Decaps): These are discrete capacitors on the PCB and package to reduce the impedance of the PDN at certain frequencies.

b) Transient Simulation: A time domain simulation is carried out where the CPM injects the given current profile into the assembled PDN. The CMA tool solves the circuit equations to find the response in voltage on the die bumps over the time of the switching event.

c) **Frequency Domain Analysis (Impedance):** P Same as transient analysis, the tool determines the target impedance (Z). For the entire frequency spectrum the system impedance should be maintained below a calculated threshold to prevent voltage drops due to transient currents.

$$Z_{target} = (VDD * Ripple\ Tolerance\ \%) / I\ max\ transient$$

d) **Result Verification:** The final output is checked for the following power integrity hazards:

- Peak-to-Peak Ripple: The represents the total amplitude of voltage swing.
- Resonant Peaks: It represents the anti resonance points where the inductive path of the package interacts with the capacitive elements of the die, resulting in voltage spikes.
- DC IR Drop: The DC voltage drop caused by the resistive elements of the copper traces.

3.13 Transient Current Profile Generation

For a realistic simulation of the Power Delivery Network (PDN), the stimulus (the current demand of the chip) must represent realistic worst-case switching situations. The Chip Model Analyzer (CMA) allows you to import and rigorously manipulate these current profiles to develop stress tests that expose potential voltage ripple and resonance issues.

The process begins by importing the Chip Power Model (CPM) into the analysis environment. The CPM is a comprehensive behavioral model derived from vector-based activity simulations of the physical die layout. It contains the time-domain current signature (I(t)) of the chip executing a specific workload (e.g., "boot" sequence or "video encoding"). The dynamic current consumption for the various voltage domains is shown when this data is imported to the CMA and establishes the baseline electrical load for the simulation.

a) **Waveform Segmentation (Drag and Cut):** For peak noise analysis, not all parts of a simulation vector are of interest. The “Drag and Cut” operation is applied to focus the computation on the most relevant events [4].
- Method: The imported waveform is visually inspected by the user to identify the region of the maximum magnitude of the current (I peak) or the maximum steepest slew rate (di/dt).
- Selection: The selection interface of the tool is used to isolate (cut) this particular time-window from the longer simulation trace.
- Objective: This isolates the “aggressor” event, removing the quiescent (low activity) periods which do not contribute to the voltage ripple and thus simplifying the simulation.

b) **Waveform Mirroring:** When a segmented waveform is to be repeated, a discontinuity often occurs at the boundary where the end of the segment meets the beginning of the next cycle (e.g. ending at 5A and instantaneously jumping back to 1A at the beginning of the next cycle). Such artificial jumps lead to spikes of infinite di/dt which are the sources of simulation artifacts. To ease this, a technique called Mirroring is used.

- **Technique:** A portion of the waveform is selected, copied and time reversed (mirrored). The original segment is then joined to its reflected copy.

- **Result:** This creates a perfectly continuous wave shape where the start and end points line up together.
- **Advantage:** This enables for a seamless transition between repeated cycles for longer length, maintaining the physical integrity of the simulation and preventing spurious noise violations coming from discontinuities which leads to greater voltage drop.

c) Waveform Stitching (Time Extension): The Stitching technique is used to extend the duration of the waveform for longer period of time so that it can evaluate voltage drop for long period of time so a continuous wave is generated by mirroring.

- **Procedure:** The mirrored segment is stitched sequentially a number of times to generate a longer periodic pulse train.
- **Application:** This extension is critical for observing lower frequency behaviors. A short pulse might only excite on-die capacitance, but a long, stitched waveform allows the simulation to reach the time constants associated with the package and board capacitors.
- **Resonance Testing:** By stitching the waveform at specific intervals, the analysis can also artificially induce resonance to test if the PDN "rings" at specific frequencies.

d) Extended Waveform Generation: A new extended waveform is generated after waveform stitching which is of 1000 ns or more which is further used for Die Package Board Ripple analysis so that ripple can be calculated for longer duration as sometimes for longer duration there has been seen some voltage fluctuations which results in causing of voltage drop.

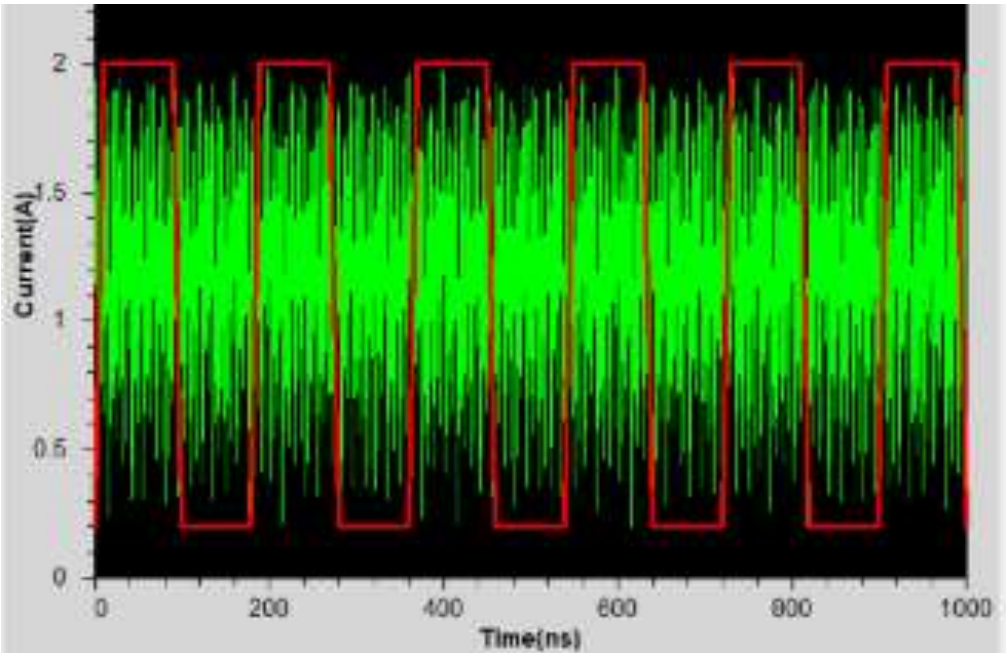

Fig 3.13 Extended Waveform Generated for 1000 ns

Fig 3.13 shows that the extended waveform is generated for 1000 ns so that ripple analysis can be done for longer duration as it has been seen that for longer duration there are much voltage fluctuations which significantly reduces the circuit performance as the SoC will not gets the required current for proper functioning of logics which may results in circuit failure.

3.14 Prototype model showing Die, Package and Board connections

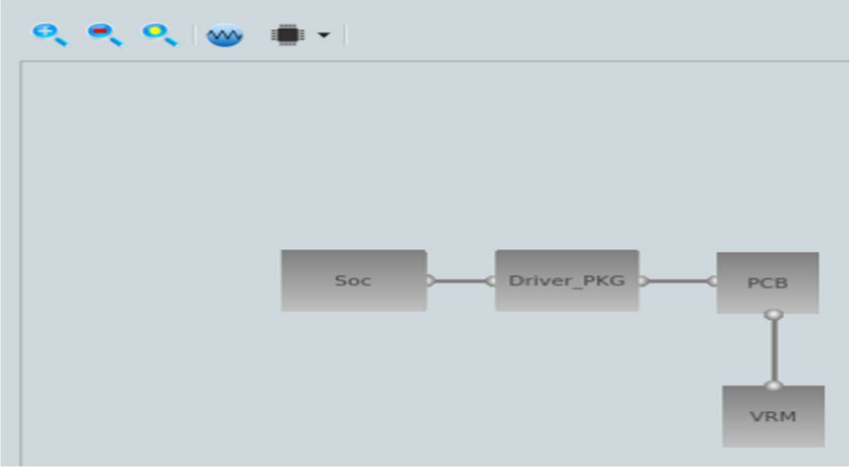

Fig 3.14 Prototype Model showing Die, Package and Board connections

A unified prototype model as shown in fig 3.14 breaks the hardware down into three components:

1. The Board (PCB) Level: Power travels from the VRM through large copper power planes and drilled vias. These structures are large relative to the die but span huge physical distances and hence accumulate macroscopic resistance.
2. The Board to Package Interface: Power enters the package using an array of solder balls, usually a Ball Grid Array (BGA). This spherical solder joint is physically restricting the flow of current and this causes local resistance.
3. The Package Level: Inside the package substrate, current must navigate through complex, densely packed routing layers, micro-vias, and internal power planes before reaching the silicon.
4. The Package-to-Die Interface: This is often the most critical bottleneck. Current flows through thousands of microscopic solder bumps in flip-chip design or wire bond design. Because these connections are exceptionally small, their cross-sectional area is minimal, leading to higher electrical resistance.

When an electrical signal crosses the boundary from the die into the package, or from the package onto the board, the change in physical shape can cause the signal to bounce back or become distorted. By using a Chip Model Analyzer to build a unified prototype model, it is possible to link all three physical structures together in software.
A continuous die-package-board prototype allows designers to run end-to-end electrical simulations. Engineers can virtually see how signals and power move across the physical boundaries of the system, identify design flaws, prevent loss of data and save considerable money before manufacturing the physical hardware.

A Chip Model Analyzer builds a holistic DPB prototype model that addresses this. The tool does the following:

1. 3D Geometry Extraction: It imports the physical design files of die, package and board, physically aligning bumps, pads and routing.

2. Parasitic Extraction: The software computes the exact resistance of each geometry in the unified PDN.
3. DC Voltage Drop Simulation: The tool simulates a heavy computational load (high current draw at the die) to compute the exact voltage at each node of the 3D structure.
4. Visual Mapping: The analyzer creates a color-coded “heat map” of the voltage levels, allowing engineers to determine precisely where the structural bottlenecks are. It will help in identifying the regions facing more drop issues.

Modeling and evaluating the full Die Package Board interaction is a requirement in modern semiconductor design. A Chip Model Analyzer provides simulation of cumulative IR drop in these three domains and may readily identify power delivery bottlenecks, optimize bump placements and ensure a robust, steady voltage delivery to the silicon die in all operation scenarios. With the help of this Die Package and board analysis, we are able to analyze overall the voltage drop between die and package and board and package so that the chip will function properly without any logic failure.

CHAPTER 4: RESULTS AND DISCUSSION

4.1 Observations after 1st check (without Decap)

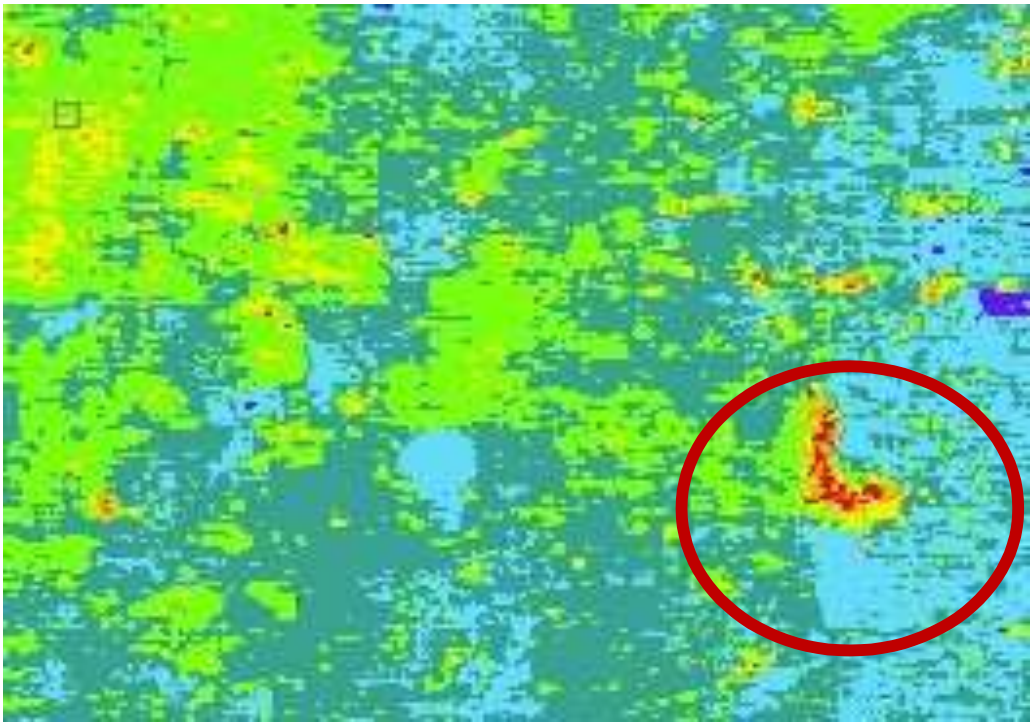

Fig 4.1 Worst Drop is 140 mV instance zoomed view

Key Observations:

1. **Worst IR Drop Region:**

- The encircled region in the Fig 4.1 indicates the area experiencing the highest voltage drop. This region having IR drop of 140 mV is significant and can adversely affect the performance and reliability of the circuit components in this region.

2. **Impact on Circuit Performance:**

- The higher IR drop can lead to several problems such as timing errors, signal integrity degradation, design unable to meet current requirements and even logic failures in the design. This area may contain components that are not getting enough current to operate properly and cause the malfunction or poor performance.

3. **Absence of Decoupling Capacitors:**

- Without the usage of decoupling capacitors, the design is depicted in Fig 4.1. Decaps plays an important role for reducing voltage dips and stabilizing the power supply voltage. Their absence in this case emphasizes how susceptible the power distribution network is to large IR drops

4.1.1 Method 1: Implementing Decoupling Capacitors (Decaps) in the Design

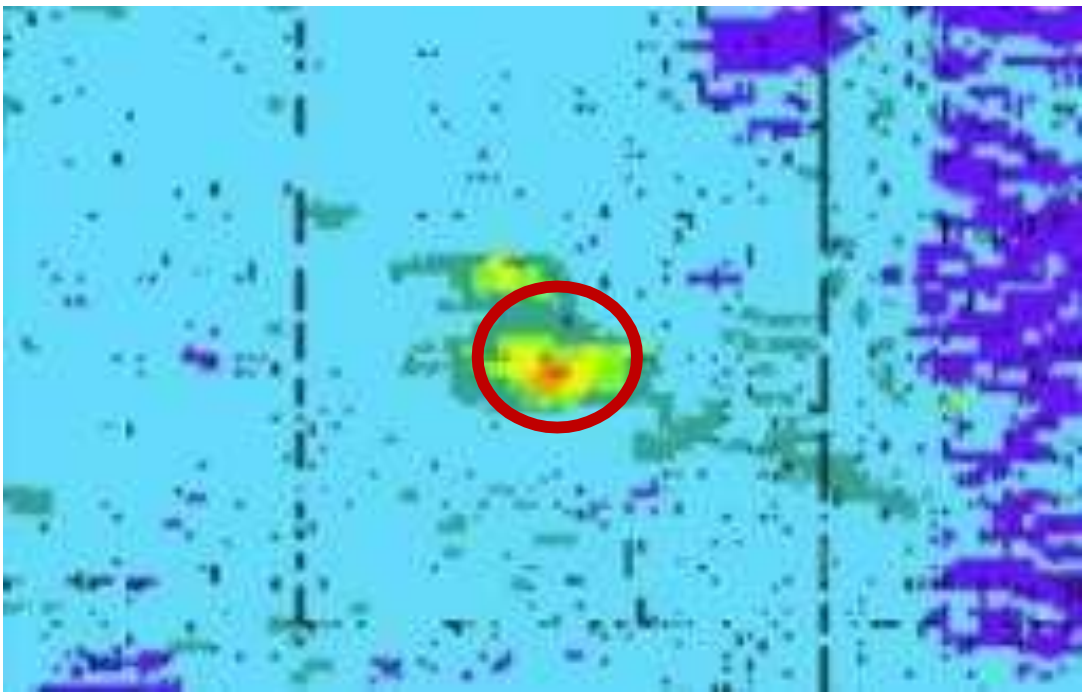

Fig 4.2 Worst Drop instance zoomed view after placing decaps

Key Observations:

1. **Reduced Worst IR Drop Region:**

- The highlighted region in the Fig 4.2 depicts the area experiencing the biggest voltage loss. The IR drop has been lowered from 140 mV to 110 mV, which is a significant improvement. The reduction demonstrates the effectiveness of the decoupling capacitors to stabilize the power voltage. This assures the right operation of logic cells for the chip functionality.

2. **Reduction of Red Region:**

- The red region which is the region of severe voltage reduction has also been reduced significantly and results in improvement of circuit performance. This allows a more even and reliable power distribution across the integrated circuits and avoids hotspots where the voltage drops can adversely affect the performance.

3. **Effect on Circuit Performance:**

- The reduction in IR drop enhances the overall performance and reliability of the circuit components in this region. A lower voltage drop means that the components are more likely to see sufficient voltage which reduces the likelihood of timing errors and signal integrity problems.

4. **Effectiveness of Decoupling Capacitors:**

- The Fig 4.2 presents the positive effect of the inclusion of decoupling capacitors on the design. Decaps are local energy reservoirs, and supply current to the circuit components at the time of transient events, so that the power supply voltage is stabilized and voltage drop is reduced. Decap cells are placed after the standard cells, memory blocks and macros are placed in the design. These cells are placed uniformly throughout the design so that they are able to fulfill the instant current demands of the chip. The Decaps should be placed as close as possible to power pins so that they are able to fulfill current demands.

5. **Improvement in Power Integrity:**

- The reduction in worst IR drop and the reduced red region is an indication of an improved power integrity within the IC. The improvement allows for more reliable circuit operation with better signal integrity and lower risk of performance degradation.
- Decaps can maintain stable voltage, reduce noise, and improve the reliability and performance of high speed and high density designs. Proper decap strategy forms the backbone of a robust power delivery network.

4.1.2 Result Comparison

Parameter	Without Decap (mV)	With Decap (mV)
IR Drop	140	110

Table 1: Result comparison of with and without Decap

Thus, overall the voltage drop has been reduced which is caused by high frequency noise. In Table 1, it is mentioned that the worst drop without decap is 140 mV which has now been reduced to 110 mV after the addition of decaps.

4.2 Method 2: Implementing Power Ground Fills (PG) in the Design

The implementation of intelligent power-ground metals enables the efficient distribution of current in the design. After STA is done, data is taken into account for voltage noise analysis, the result in the form of IR map is shown in Fig. 4.3, with red dots showing large voltage drops in certain parts of the chip.

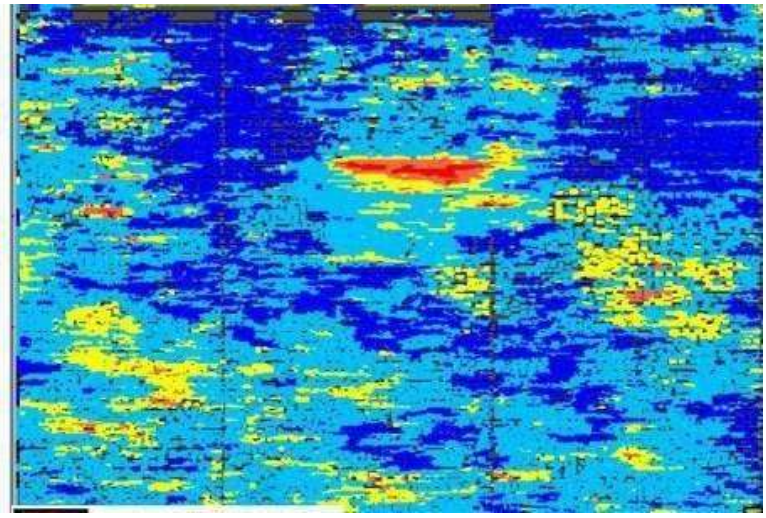

Fig 4.3 Before Smart PG Fills

The orange, yellow, and sky-blue spots shows drops in the range 10 – 100 mV respectively, while the red spots show drops over or equal to 110 mV. Adding PG fills will considerably decrease the regions having voltage drop shown in red region which is approximately 110 mV as illustrated in Fig. 4.4.

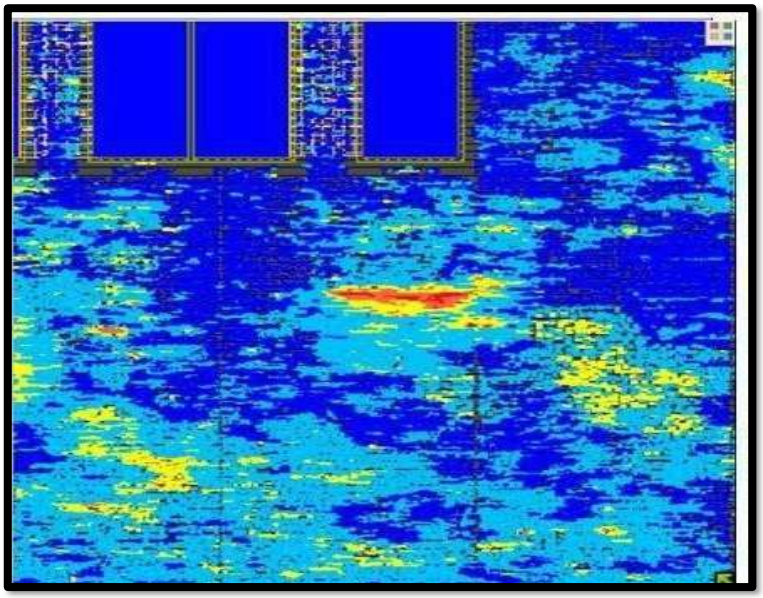

Fig. 4.4 After Smart PG Fills

4.2.1 Noise reduction after inserting PG fills

Below Fig. 4.5 shows reduced supply noise in the SOC, the overlap is between high supply noise (orange) and reduced supply noise after assigning Decaps and PG fills in the design.

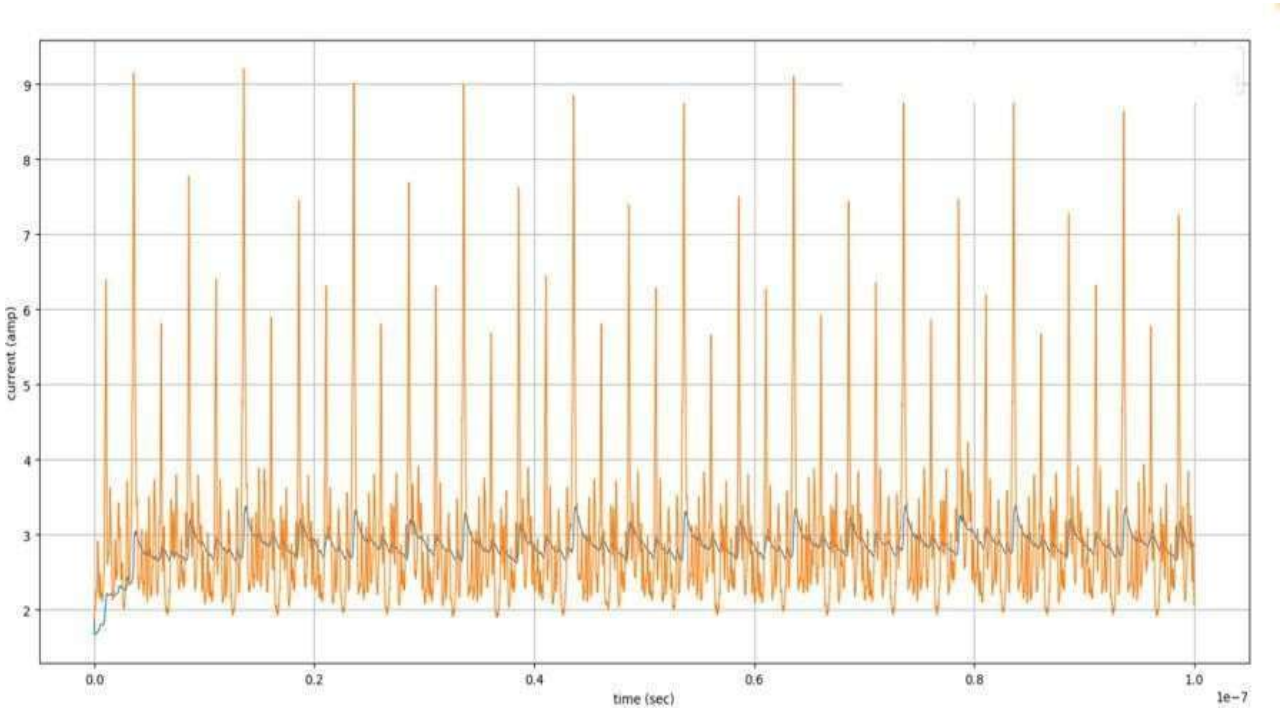

Fig. 4.5 Noise Reduction after inserting Decaps and PG Fills

Blue : showing supply noise reduction post assigning decap and PG fills

Orange: Showing high supply noise before assigning decap and PG fills

4.3 Method 3: Implementing SHDMIM Capacitors in the Design (SOC)

The integration of SHDMIM (Super High-Density Metal-Insulator-Metal) capacitors in the design significantly enhances power integrity and noise reduction [11]. Static Timing Analysis (STA) data is utilized for voltage noise analysis, the resulting IR map is depicted in Fig. 4.6. This figure shows red dots indicating areas with substantial voltage drops across various sections of the chip.

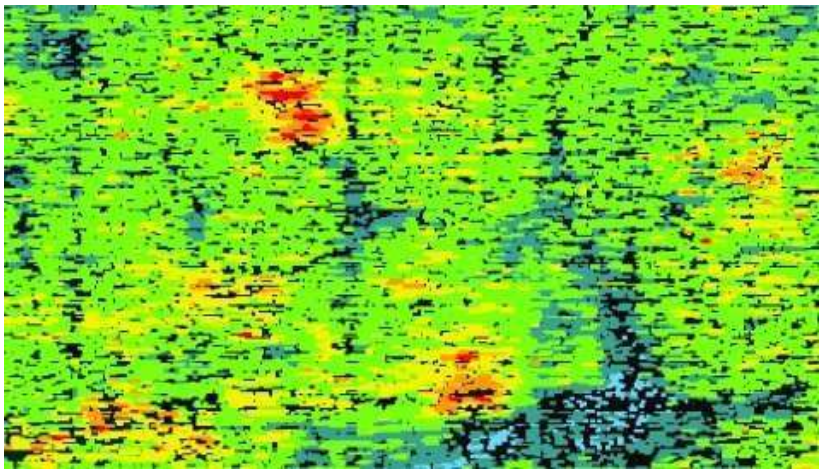

Fig 4.6 Before SHDMIM insertion

The red spots indicate voltage drops greater than or equal to 110 mV, while the orange, yellow, and sky-blue spots exhibit drops in the range of 40 mV to 80 mV, 90 mV to 110 mV respectively. Dark blue spots, on the other hand, show voltage drops below 40 mV.

By incorporating SHDMIM capacitors, the occurrences of larger voltage drops were significantly reduced, now the worst drop is reduced to 70.5 mV shown as a red spot illustrated in Fig 4.7.

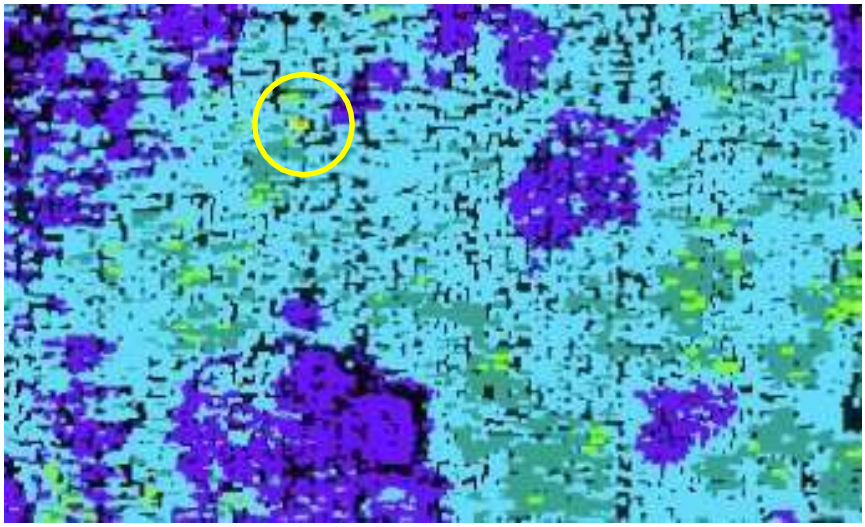

Fig 4.7 After SHDMIM insertion

4.3.1 Result Comparison after SHDMIM insertion

The implementation of SHDMIM capacitors in the design has significantly improved power integrity and noise reduction. Table 2 and Table 3 below presents a comparison of key parameters with and without SHDMIM capacitors, highlighting the substantial improvements achieved.

In the case of voltage fluctuations in the integrated circuit (IC) or System-on-Chip (SOC), the implementation of SHDMIM capacitors has resulted in a reduction of voltage drop from 110 mV to 70.5 mV. Moreover, the settling time of these voltage fluctuations has decreased from 13 ns to 5.5 ns which is an enhancement. Furthermore, the peak-to-peak voltage of the SOC bump after stabilization has decreased indicating a voltage noise reduction.

Parameter	Without SHDMIM Cap
Voltage fluctuations of IC/SOC (mV)	110
Settling time of voltage fluctuations (ns)	13

Table 2: Dynamic Drop before SHDMIM Capacitors

Parameter	With SHDMIM Cap
Voltage fluctuations of IC/SOC (mV)	70.5
Settling time of voltage fluctuations (ns)	5.5

Table 3: Dynamic Drop after SHDMIM Capacitors

So overall the reduction has been minimized in larger extent which is a must priority for efficient operation of the chip so that power may be supplied to all parts of the chip. The voltage fluctuations has been lowered, which allows to acquire a right settling time for a signal.

The SHDMIM capacitors have several design improvements making it a very effective solution to improve power integrity and minimize noise.

The main reasons for the positive results after the insertion of SHDMIM capacitors are:

1. **Reduce Voltage Variation**: The SOC voltage variance is lowered from 110mV to 70.5mV. This reduction is important because it shows that the circuit now has reduced its voltage drop, which translates into more steady power supply, a vital requirement for the reliable operation of various electronic parts in the design. A stable voltage improves the dependability, helps in noise reduction and performance of the system.

2. **Improvement of Settling Time**: Settling time of voltage variations in the design has been improved from 13 ns to 5.5 ns demonstrating 57.69 % improvement in the design. The faster settling times allow the system to settle to a stable state faster following transient events such as power surges or switching activities in the design. For the integrity of high speed circuits and for their correct functioning without delays or errors, fast stabilization of the design is necessary.

3. **Better Bump Voltage Stability**: The bump drop is the voltage peak to peak of SOC bump after stabilization dropped from 98.5 mV to 71.5 mV which is 27.41%. The increased bump voltage stability in SOC ensures the accurate power distribution over the whole chip. This helps to reduce the possibility of voltage related issues and enhances the overall reliability of the SOC.

4. **Increased Reliability and Performance**: The SHDMIM capacitors lower the voltage variations and extend the setting times of the SOC and hence aids to boosting the reliability and performance of the IC / SOC. These changes reduce possible failures and increase the lifetime of the electronic components which makes the design more resilient and reliable.

5. **Low Frequency Noise Reduction**: SHDMIM capacitors are ideal for reducing low frequency noise which is typically caused by power supply changes and load variations. The capacitors are used to suppress low frequency noise, contributing to a clean and stable power supply, which is required for the proper operation of the whole system.

6. **Noise Reduction**: SHDMIM capacitors plays an important role in reduction of noise by fulfilling current demands of the circuit which is extremely important for the signal integrity of high speed and high frequency circuits. This reduction in noise level maintains the signals clean and free from interference which helps in increasing the accuracy of data transmission and processing.

7. **Power Integrity Enhancement**: The overall power integrity improvement occurred through the deployment of SHDMIM capacitors guarantees the effective operation of the power distribution network inside the SOC. This efficiency is very important for the optimal operation of the chip, since it minimizes power losses and guarantees that all components are supplied with the required amount of power so that all the parts of the chip functions properly and meets the timing requirements so that it does not leads to circuit failure in the design.

SoC Bump Voltage Analysis: With and Without SHDMIM Capacitors

The following analysis compares the SOC bump voltage behavior with and without the implementation of SHDMIM capacitors. The two figures below illustrate the voltage stability and noise reduction achieved using SHDMIM capacitors.

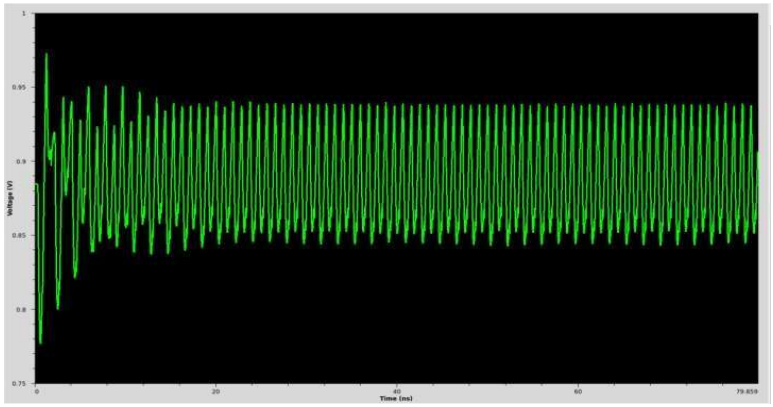

Fig 4.8 SoC Bump Voltage without SHDMIM Capacitors

In Fig 4.8 the SOC bump voltage without SHDMIM capacitors shows significant voltage fluctuations. There are big variations in voltage from peak to peak. This shows the power supply is very unstable. The voltage oscillations are time persistent and there is no evident stability. This can lead to performance reduction and possible problems in the SoC [12]. The transient response is especially unpredictable in the initial transient with high amplitude oscillations that fade slowly but do not settle to a steady state.

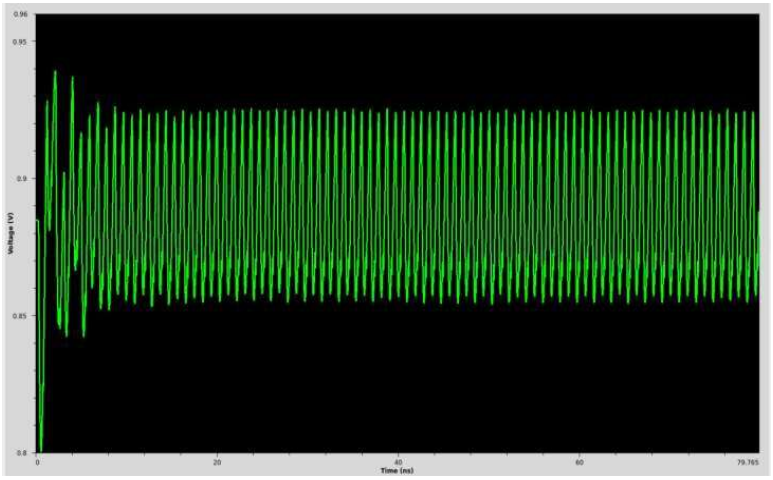

Fig 4.9 SOC Bump Voltage with SHDMIM Capacitors

Fig 4.9 shows the SOC bump voltage with SHDMIM capacitors fitted. The variance of voltage is greatly reduced which illustrates the power supply stability capabilities of SHDMIM capacitors. Voltage level is more consistent and stable since the peak to peak voltage changes much less. Also the first transient response is smoother and the voltage reaches steady state faster when no SHDMIM capacitors are included in the design. The better stabilization is needed to assure the reliability and efficiency of the SOC so that it will perform the required functionality.

4.4 Final Result Summary of Noise Reduction Techniques in Integrated Circuits

Noise Type	Frequency Range	Reduction Technique	Initial Voltage Noise (mV)	Reduced Voltage Noise (mV)	Voltage Reduction (mV)	Percent Reduction (%)
High Frequency	100 MHz – 1 GHz	Decoupling Capacitors (Decaps)	140	110	30	21.4
Low Frequency	1 kHz – 10 MHz	SHDMIM Capacitors	110	70.5	39.5	35.9

Table 4: Comparative Analysis of Noise Reduction Techniques in Integrated Circuits

This table highlights the importance of various noise reduction techniques used in integrated circuits (ICs). The use of decoupling and SHDMIM capacitors in circuits (ICs) is validated by comparing the original and reduced voltage noise levels to the voltage reduction and percent decrease which indicates the drop reduction.

- **High Frequency Noise Reduction**: Decoupling capacitors (decaps) are used for high frequency noise reduction in the range of 100 MHz to 1 GHz which is described in Table 4. The voltage noise was initially measured at 140mV and was reduced to 110mV after decaps were put in place. This causes a voltage drop of 30 mV results in 21.4% drop reduction. Decaps are effective in creating a local energy reservoir to stabilize the power supply during transient events, which improves signal integrity and reduces the probability of logic failures [13].
- **Low Frequency Noise Reduction**: SHDMIM capacitors are employed for low frequency noise in the range of 1 kHz to 10 MHz which is described in Table 4. The initial voltage noise was measured to be 110 mV and after the implementation of SHDMIM capacitors it was decreased to 70.5 mV. This leads to a reduction of the voltage drop of 39.5 mV which corresponds to a reduction of 35.9 % in drop.

SHDMIM capacitors have high capacitance density and self healing properties which make them specially suitable for improving power integrity and reducing low frequency noise. The decoupling capacitors and the SHDMIM capacitors work together to provide a full solution to reduce the supply noise over a broad range of frequencies resulting to more reliable and efficient IC designs. This table demonstrates significant improvements in voltage noise reduction that can be achieved with these techniques, underlining significance of these techniques in modern IC designs.

4.5 Chip Power Model (CPM) generation in the Design (SOC)

A waveform is generated between current vs time to show the peak current used in the SOC. This peak current is determined by switching activity and VCD file is used to provide that switching activity. This waveform shows the maximum current demanded by the SOC to meet all the design requirements so that all the logics can be met and circuit failure will not happen.

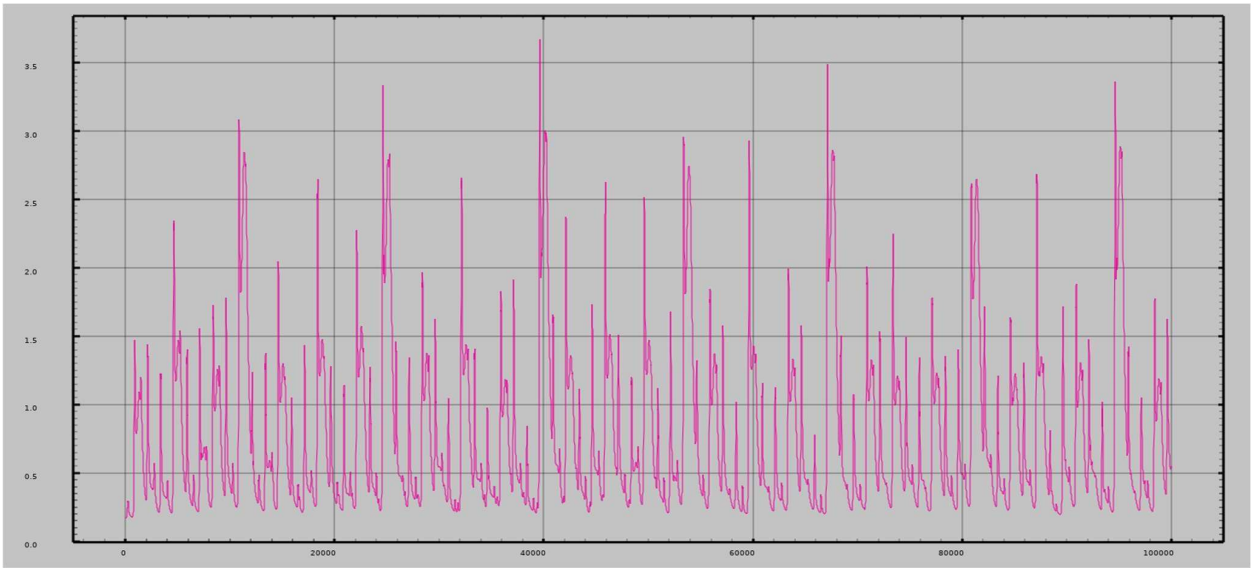

Fig 4.10 Current Vs Time Waveform for 100 ns

Fig 4.10 shows that CPM is generated by reading the switching activity from the VCD file. From the VCD file, it has been observed that the peak current used in the SoC is 3.67 A which is required for the proper functioning of the circuit. When many transistors switch simultaneously, they create spikes in current demand, leading to temporary voltage dips known as Dynamic IR drop [1].

The Chip Power Model (CPM) generation provides high resolution insights into the power demands of the SoC. Simulation results are generated by the logical switching activity which is provided by the VCD file, highlights the following critical observations:

1. **Peak Current Magnitude:** The design shows a peak current demand of 3.67A. Current limit is the limiting factor that determine the width of metal power and ground; rails. It checks that the load current handled by the power distribution network is 3.67A when the maximum logic toggling is present.
2. **Switching Activity Correlation:** The waveform variations are closely correlated to the logic state changes in the design as per the switching activity. The strong simultaneous switching activity pressures the package inductance as shown by the sharp ascent to the peak value.
3. **Integrity Validation:** Extracted value of 3.67 A validates the design to meet the required power budget. It supplies the boundary condition for the calculation of the worst case voltage drop, guaranteeing that the supply voltage at the transistor level is within the safe operating margins which are (usually + - 10%) to avoid logic problems [14].

4.6 Importation of CPM to Chip Model Analyzer (CMA)

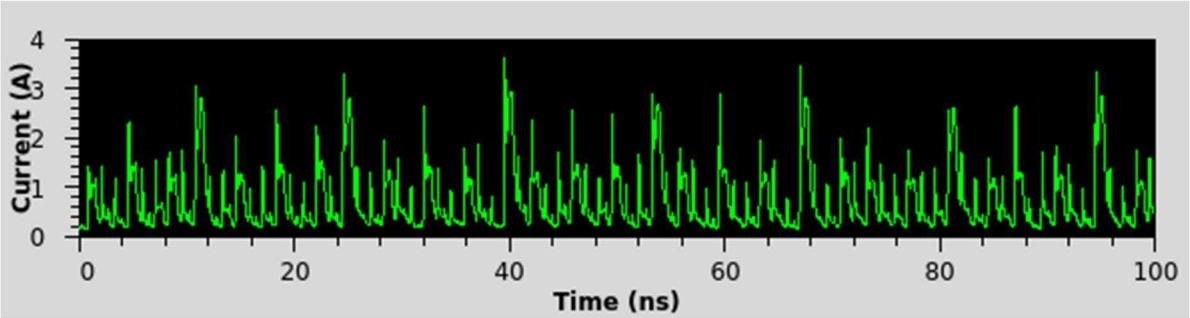

Fig 4.11 Current Vs Time waveform (CPM imported to CMA)

The created Chip Power Model (CPM) was successfully imported into Ansys Chip Model Analyzer (CMA) environment to validate the fidelity and electrical features of the model. The simulation was run for a transient window of 100 ns using vector based switching activity generated from the VCD file.

The analysis provides the following important observations about the SoC's power integrity:

1. **Transient Current Profile Validation:**

- The imported CPM accurately reconstructed the transient current waveform for the 100 ns duration as shown in above Fig 4.11. The tool aggregated the total current consumption across all power domains.
- The analysis confirmed a global peak current of 3.67 A. This value corresponds to the worst-case switching vectors and establishes the maximum load condition used for subsequent Power Delivery Network (PDN) validation.

2. **Model Readiness for System Co-Simulation:**

- The tool confirmed the integration of the parasitic Resistance (R) and Capacitance (C) network representing the on-die PDN, alongside the active current profile [6].
- The CPM is certified as valid for Die-Package-Board (DPB) co-simulation. This result authorizes the use of this specific CPM to simulate the interaction between the SoC and external package inductance, a mandatory step for final Power Integrity sign-off.

3. **Spatial Current Distribution:**

- Unlike a lumped circuit model, the CPM import provides a spatial resolution of power consumption across the die.
- The CMA tool maps the 3.67 A peak current to specific voltage level and bump locations on the die surface.

4.7 Implementation of Drag & Cut and Waveform Mirroring

Drag & Cut:

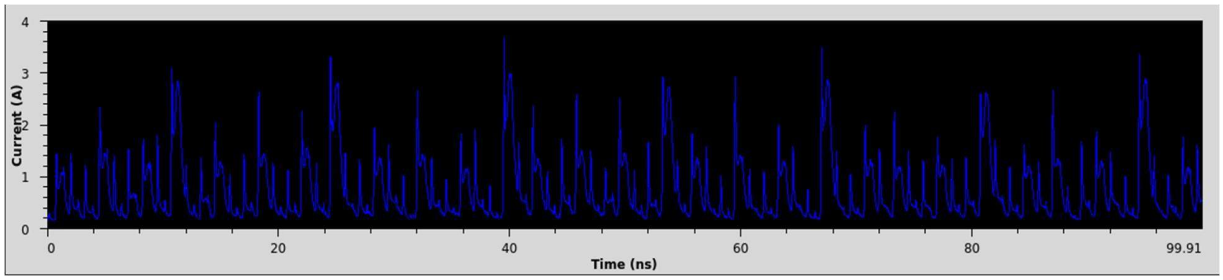

Fig 4.12 Drag & Cut of Imported Waveform of 100 ns

The "Drag and Cut" technique was employed to isolate the most critical switching event from the extensive VCD switching activity.

1. The full vector simulation was scanned to identify the time window with the highest switching density. A specific 100 ns window (containing the global peak current of 3.67 A) was selected ("dragged") and extracted ("cut") from the overall profile as shown in Fig 4.12.
2. The specific sequence of logic transitions that causes the maximum instantaneous current demand allowing for focused high-resolution simulation without the computational overhead of the non-critical idle periods.

Key Observations:

- The "Drag and Cut" operation confirmed that the isolated 100 ns window contains the worst-case di/dt event.
- The voltage drop observed during this isolated window has the maximum drop recorded.
- This confirms that the PDN design is constrained by this specific 100 ns logic sequence. Optimizing the decoupling capacitors for this specific window guarantees safety for the rest of the operation.

Waveform Mirroring:

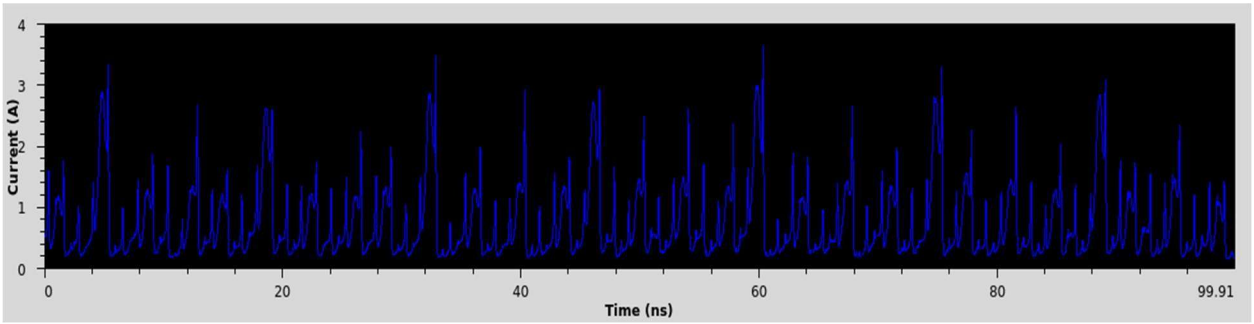

Fig 4.13 Waveform Mirroring

Following the extraction, the "Mirror" function was applied to the 100 ns imported transient waveform.

- The isolated 100 ns current profile was duplicated and reversed (mirrored) as shown in above Fig 4.13, effectively doubling the simulation window to 200 ns with a symmetric current load as shown in Fig 4.14.
- Mirroring creates a synthetic stress test that simulates a "sustain and recovery" cycle. It tests the PDN's ability to recover voltage levels immediately after a peak event by subjecting it to a secondary, symmetric load pattern. This is particularly useful for ripple analysis for longer duration.

4.8 Implementation of Waveform Stitching & Extended Waveform Generation

Waveform Stitching:

"Stitching" operation was implemented within the Ansys Chip Model Analyzer. This process combines the original transient profile with its mirrored waveform to generate a continuous, extended simulation window of 200 ns as shown in Fig 4.14.

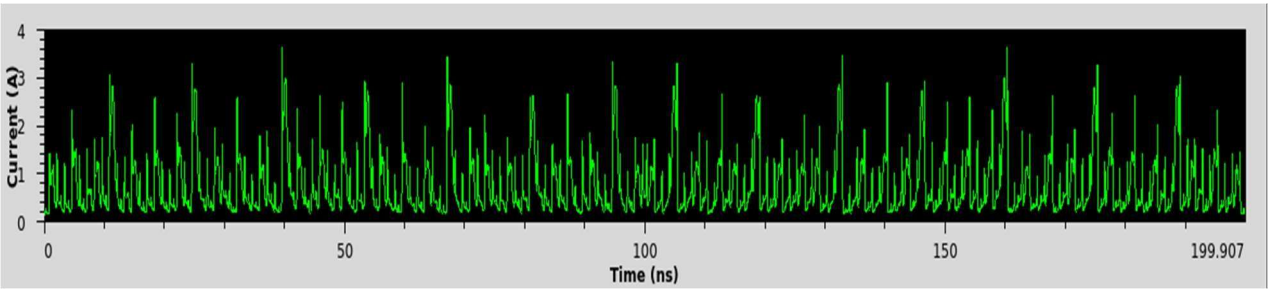

Fig 4.14 Waveform Stitching of 200 ns

The results of 200 ns period of time of Chip Power Model (CPM) represents the following critical observations regarding the stability and robustness of the SoC's power grid:

1. Longer Peak Current Duration

- The stitched waveform represents a composite profile with a peak current demand of 3.67 A is obtained twice in the 200 ns interval, once during initial and once during mirrored phase.
- This longer period of high current flow (effectively greater pulse width) puts more stress on the local charge reservoirs than a single spike. The simulation showed that the on die decoupling capacitors in the design have enough energy stored to cover the load during the peak events without being completely discharged.

2. Loop Inductance and Recovery Time

- The most important observation lies in the transition point at 100 ns, where the two waveforms are stitched together. The voltage at this junction remained stable and did not exhibit significant undershoot.

Extended Waveform Generation:

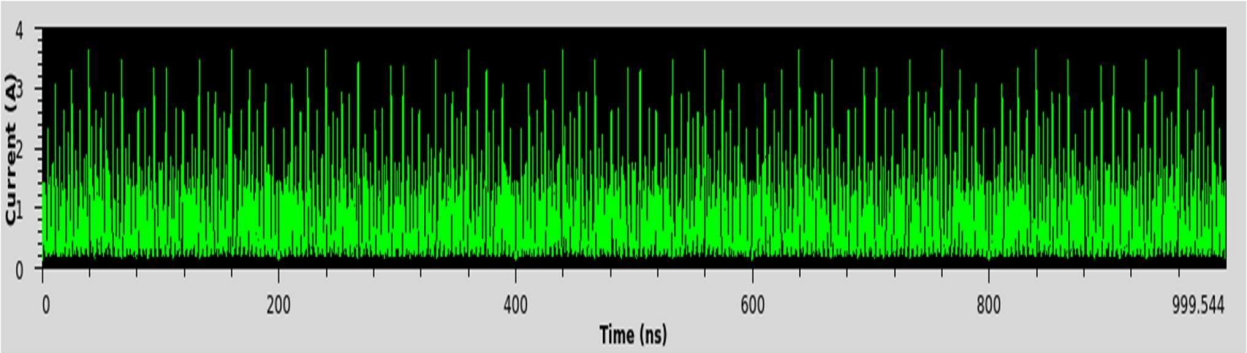

Fig 4.15 Extended Waveform of 1000 ns

A waveform is extended for 1000 ns as shown in Fig 4.15 so that Die Package Board Ripple analysis can be done for longer duration. It has been seen that for longer duration, there may be some voltage drops which may affect the proper functioning of the SOC.

Key Observations:

1. The voltage profile only began to stabilize and trend toward the nominal VDD after 10 ns.
2. When the workload switching frequency aligns with the PDN's natural frequency, noise from subsequent cycles adds constructively. This proves that a 200 ns window is insufficient for evaluating worst-case noise margins in functional SOC.
3. The extended waveform analysis reveals no evidence of low frequency (kHz range) oscillation or divergence. The ripple stays within some deterministic range for the duration of the microsecond.
4. The extended 1000 ns window shows that the voltage oscillations have a decaying envelope, confirming that the Power Delivery Network (PDN) is not under-damped.

4.9 Implementation of Interconnects on Die, Package and Board

➢ From PCB Netlist

16	! Port16_PR_3::VDD_LV_0	POGO_VDD_LV_S0
17	! Port17_PR_3::VDD_LV_1	POGO_VDD_LV_S1
18	! Port18_PR_3::VDD_LV_2	POGO_VDD_LV_S2
19	! Port19_PR_3::VDD_LV_3	POGO_VDD_LV_S3
20	! Port20_PR_3::VDD_LV_4	POGO_VDD_LV_S4

From PCB To supply

35	! Port35_DUT0::VDD_LV_0	DUT_VDD_LV_S0
40	! Port35_DUT0::VDD_LV_0	DUT_VDD_LV_S1
45	! Port35_DUT0::VDD_LV_0	DUT_VDD_LV_S2
50	! Port35_DUT0::VDD_LV_0	DUT_VDD_LV_S3
55	! Port35_DUT0::VDD_LV_0	DUT_VDD_LV_S4

From PCB To PKG (Driver) Netlist port 1

➢ Remaning PCB ports are connected to VDD/VSS

➢ From PKG (Driver) Netlist

node 1 → BGA1_BGA1_VDD_LV_Group_BGA1_VSS_LV_Group (PCB)
node 2 → DIE_DIE_VDD_LV_Group_DIE_VSS_LV_Group (SOC)

Fig 4.16 Connections between Die, Package and Board

4.10 Implementation of PCB Ports to Package

PCB ports (35, 40, 45, 50 and 55) are connected to PKG Node 1

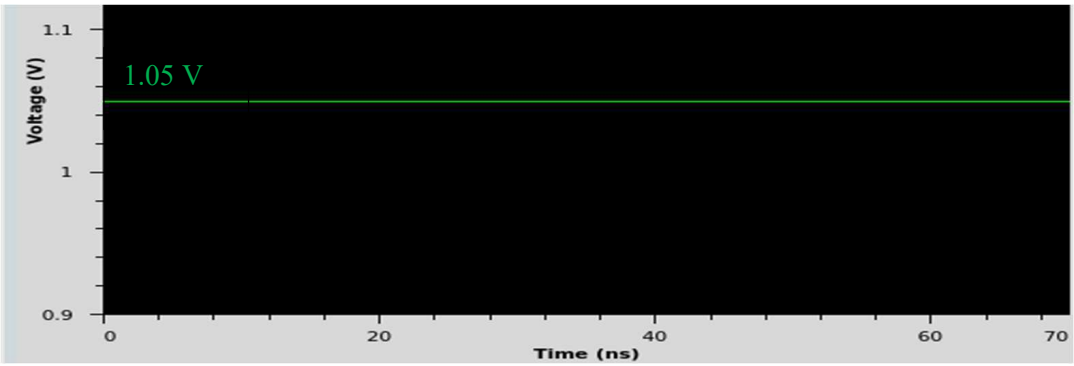

Fig 4.17 Achieved supply voltage 1.05 V in 70 ns

The analysis confirmed the five-port routing design that provided the 1.05 Volts needed from the main circuit board to PKG Node 1, meeting the chip's core power needs.

Key Observations:

1. Significantly Reduced Voltage Drop : By splitting the electrical path into five separate ports instead of one connection, the total physical resistance was greatly reduced. This resulted in the natural voltage drop between the board and the package being kept to an absolute minimum
2. Better Voltage Stability: During simulation where the chip demands the maximum power supply for the proper functioning, the voltage remained stable at 1.05V. These parallel connection decreased the overall inductance of the system which effectively removed the voltage fluctuations.
3. Even Current Distribution: The simulation results shows that the electrical current was evenly distributed among Ports 35, 40, 45, 50 and 55. This shows that not only single port carries too much power, effectively minimizing the chance of voltage drop, overheating or physical damage at the connection points due to which the circuit performs properly as per the logic defined.
4. Design Validation: Finally the design is verified by the chip model analyzer. The results show that a multi-port connection is a very dependable way of keeping the power integrity clean and unbroken between the PCB and the chip package.

4.11 Implementation of PCB Ports 16 to 20 having maximum ripple in 70 ns

In the Chip Model Analyzer tool, mapping has been done by using the Ports 16, 17, 18, 19, and 20. Just like our previous tests, these five ports are grouped together to share the electrical load. This parallel connection acts like a multi-lane highway, lowering the overall physical resistance and inductance between the main board and the chip package.

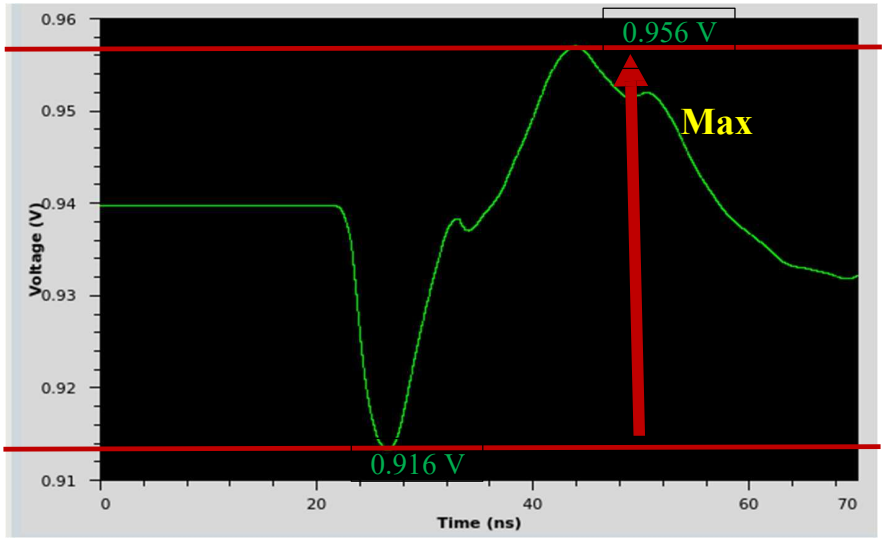

Fig 4.18 PCB Ports (16 to 20) having maximum ripple in 70 ns

Key Observations:

1. The implementation of Ports 16 to 20 confirms that the design can handle sudden, high-speed power demands. By analyzing the maximum ripple at the 70 ns time, it has been analyzed that there is reduction in transient noise and guarantees stable power delivery during worst-case scenarios.
2. Maximum Ripple in 70 ns duration of time is approximately 40 mV. i.e. Vmax – Vmin = 0.956 – 0.916 = 40 mV.
3. Here 'green' plot shows voltage ripple with respect to time.
4. Supply voltage assumed to be 1.05 V.

4.12 Analysis of Package Node 1 connected with PCB having maximum ripple in 70 ns

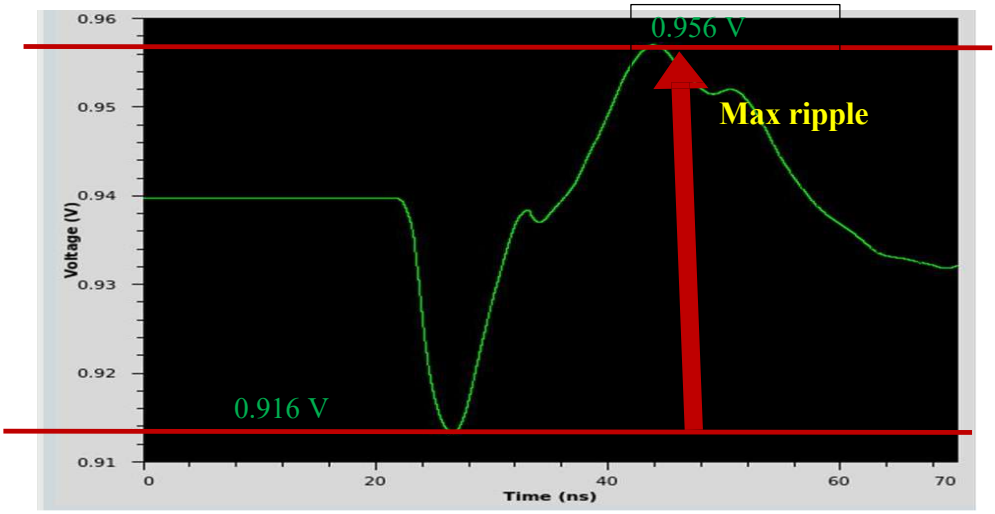

Fig 4.19 Package Node 1 connected with PCB having maximum ripple in 70 ns

Key Observations:

1. Maximum ripple in 70 ns duration of time is approximately 40 mV. i.e. Vmax – Vmin = 0.956 – 0.916 = 40 mV.
2. Here 'green' plot shows voltage ripple with respect to time.
3. Supply voltage assumed to be 1.05 V.

4.13 Analysis of Package Node 2 connected with Die having maximum ripple in 70 ns

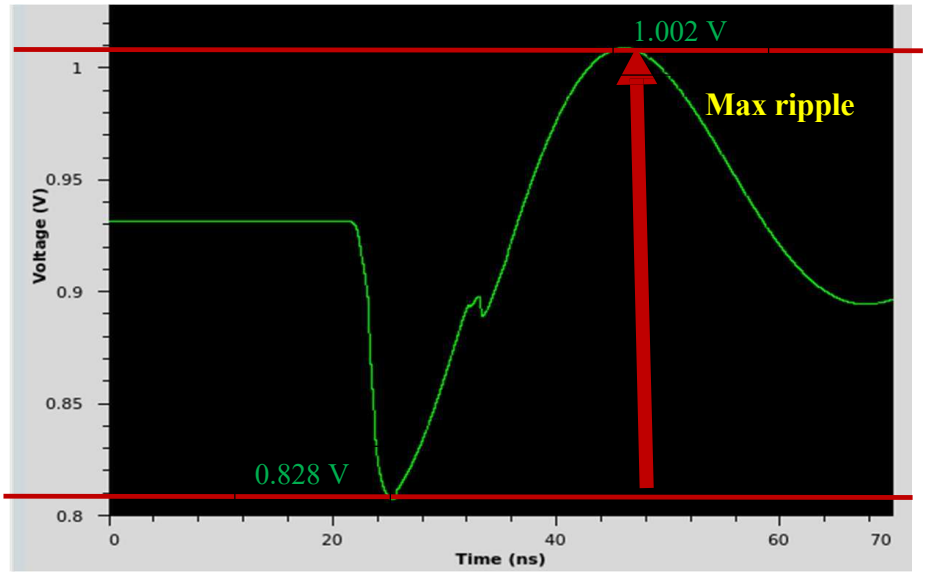

Fig 4.20 Package Node 2 connected with Die having maximum ripple in 70 ns

Key Observations:

1. Maximum ripple in 70 ns duration of time is approximately 174 mV. i.e. Vmax – Vmin = 1.002 – 0.828 = 174 mV.
2. Here 'green' plot shows voltage ripple with respect to time.
3. Supply voltage assumed to be 1.05 V.

CHAPTER 5: APPLICATIONS

The research has been widely applied in various industries and demonstrates the significant impact of supply noise reduction on the performance and reliability of advanced integrated circuits (ICs). An overview of typical applications where improvements can be achieved by using SHDMIM capacitors, decoupling capacitors (decaps) and power grid (PG) fills is given below:

1. Telecommunications:

- High Speed Data Transfer: Better signal integrity in the design and less noise in the various telecommunications equipment are necessary for high speed data transfer.
- 5G Networks: The performance of the circuit has been enhanced to meet the performance parameters of 5G networks including low latency and high reliability of design.

2. Consumer Electronics:

- Smartphones and Tablets: Consumer electronic devices such as smartphones and tablets can benefit from noise reduction techniques in terms of performance and battery life.
- Wearable Devices: Wearable devices need to have better power efficiency and less noise for reliable operation.

3. Automotive Electronics:

- Advanced Driver Assistance Systems (ADAS): Advanced Driver Assistance Systems (ADAS) ADAS plays an important role for the safety of the vehicle. The performance and reliability of the ADAS can be improved by enhancing the supply noise.
- Electric Vehicles (EVs): Power efficiency and noise reduction are important for electronic system performance and lifetime in EVs.

4. Medical Devices:

- Diagnostic Equipment: Diagnostic equipment used in medical applications requires high accuracy and reliability which can be achieved with less supply noise.
- Implantable Devices: Noise reduction can improve the performance which is necessary for in modern IC's and improve battery life of implantable medical devices.

5. Aerospace and Defence:

- Avionics Systems: The avionics systems' reliability and performance are of utmost importance in aerospace applications. Techniques for noise reduction in supply improve the stability and functionality of critical systems such as navigation, communication and control units in aircraft.
- Defence Electronics: Military operations in harsh environments demand robust and reliable electronic systems for field use. The study work is aimed for the reduction of supply noise and helps to improve the performance of radar systems, communication devices and other defence electronics to work accurately under tough conditions without any design failure.

CHAPTER 6: CONCLUSION AND FUTURE SCOPE

6.1 Conclusion

The results of this work indicate the need of an efficient supply noise reduction for the performance and reliability of advanced integrated circuits (ICs). The entire flow was developed using advanced CAD tools like RedHawk-SC to precisely calculate and strategically made the position of decoupling capacitors (decaps), power grid (PG) fills and SHDMIM capacitors in the design [34]. The decaps are the solutions that dramatically reduce the worst IR drop that stabilizes the power distribution network and improves the signal integrity. The application of PG reduces the voltage violations in both the static and dynamic cases and therefore, improves the overall design reliability and robustness.

SHDMIM capacitors also gave good results in low frequency noise suppression, voltage fluctuations and settling time reduction in the design. The combination of decaps, PG fills and SHDMIM capacitors offers a complete solution for supply noise mitigation, resulting in more reliable and efficient IC designs. The study offers key insights and practical assistance for IC designers and offers a sound foundation for future work on power integrity and circuit optimization with these capacitors. The results will have wide applications in mobiles, gaming, automotives telecommunications, consumer electronics, automotive, medical devices and aerospace [10].

The Chip Model Analyzer uses this approach to create a robust synthetic load, by segmenting the worst case event, mirroring it for continuity and stitching it for duration. This enables a complete examination of the worst case of the power rail and ensures the stability of the PDN for long durations of high stress switching. Engineers can co-simulate die parasitics with the external board environment to predict worst case voltage drops and accurately optimize decoupling capacitor placement. This method reduces the risk of SOC failures and guarantees the reliability of the electronic system. The study confirmed that the power delivery network is one coupled system and not a series of separate components. The developed tool is able to capture the complex impedance profile from the voltage regulator module (VRM) on the board, through the package substrate and up to the active transistor layers [24].

In short, the integration of Chip, Package and Board data in one analysis framework is not an improvement but a must for reliability in high performance computing. This research lays a fundamental groundwork for Die Package Board co-design, and significantly reduces the barrier of obtaining voltage drop margins for complex silicon systems [13].

6.2 Future Scope

1. Further investigation will be dedicated to the optimization of the application of SHDMIM capacitors in advanced Fin FET nodes based on the substantial results of this work [32]. A future research paper will give detailed assessment of technique and findings with emphasis on integration process, power integrity and noise reduction for the SHDMIM capacitors flow for Advanced Fin FET nodes. The report also discusses the practical use of the current IC design.
2. Future work will address the difficulties of scaling SHDMIM capacitors to more advanced semiconductor technologies for power delivery network and signal integrity. This work seeks to contribute significantly to the development of high performance, high speed and durable integrated circuit designs by sharing these insights with the academic and industrial groups.
3. Use of AI/ML (Artificial Intelligence & Machine Learning)

- Predictive Modeling: Future work could include training models with machine learning on data generated by the tool [7]. The application can predict voltage ripple in real time without performing full simulation and can provide capacitors definition.
- Automated Optimization: The technique might be further enhanced to correct the ripple instead of only assessing it. The program may also be used to automatically suggest the best location of decoupling capacitors on PCB or Package for the lowest potential ripple, using reinforcement learning [19].

4. Signal Integrity (SI) and Power Integrity (PI) Analysis: The RedHawk-SC tool has been currently focused on power integrity (ripple) or voltage drop analysis. But for high speed data signals (signal integrity) power noise is unavoidable.

- Jitter Prediction: A possible future avenue is to research the coupling of the supply ripple with the data lines and the generation of "jitter" (timing faults) in high-speed transmissions.
- EMI Compliance: The tool can further be used to predict if the ripple on the power planes will cause the PCB to operate as an antenna violating the Electromagnetic Interference (EMI) standards [30].

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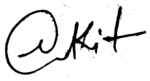

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