Realizing A Single Source Three-Phase Controllable Voltage Boosting Inverter using Single Switched-Capacitor

A dissertation report submitted in fulfilment of the requirement for the Degree

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in

Power Systems

Submitted by

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CANDIDATE'S DECLARATION

I hereby certify that the work which is being presented in the dissertation entitled "Realizing A Single Source Three-Phase Controllable Voltage Boosting Inverter using Single Switched-Capacitor." in partial fulfilment of the requirement for the award of the degree of **Master of Engineering** in **Power Systems** submitted in the Electrical and Instrumentation Engineering Department of Thapar Institute of Engineering and Technology, Patiala is an authentic record of my own work carried out under the guidance of **Dr S. K. Jain**, Professor, EIED. The matter contained in this dissertation is not submitted, neither in full nor in part for any other degree to any other institute.

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It is certify that the above statement made by the student is correct to the best of my knowledge & belief.

Place: TIET, Patiala, Punjab — **Dr S.K. Jain**

Date: 25 August 2022 — Professor

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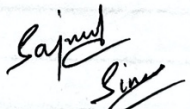

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LIST OF ABBREVIATIONS

BMS	Battery Management System
CMV	Common Mode Voltage
CSI	Current Source Inverter
ESR	Equivalent Series Resistance
EV	Electric Vehicle
PWM	Pulse Width Modulation
SCU	Switched Capacitor Unit
SPWM	Sinusoidal Pulse Width Modulation
SVM	Space Vector Modulation
SVPWM	Space Vector Pulse Width Modulation
VSI	Voltage Source Inverter
ZSI	Z-Source Inverter

ABSTRACT

The majority of the electric vehicles (EVs) today are using voltage source inverters (VSIs) as traction inverters. Due to the inherent buck character of VSI, a dc-dc converter consisting of an inductor is used to boost the voltage before the conventional three-phase bridge inverter. Hence, the system becomes bulkier and involves higher losses. To overcome the drawback, a switched-capacitor (SC) voltage boosting inverter along with its proposed carrier-based modulation strategy are presented in this study. A switched-capacitor unit (SCU) is connected to the conventional three-phase bridge inverter to obtain the increased voltage at the output. Modified sinusoidal pulse width modulation (SPWM) is used to increase the utilization of the DC source and the linear operating range of the inverter. A single carrier signal is used for comparing and switching signal generation. For modulation of the switches of SCU, new reference signals are generated from the traditional three-phase reference signals. Boosting of the inverter can be controlled by manipulating the newly generated reference signals. To yield fractional boosting, the voltage boost is obtained for a fraction of the active state duration, which thereby is resulting in less voltage drop across the capacitor. A number of SCUs can be added to a conventional VSI for The multi-fold voltage augmentation can be realized by adding number of SCUs to a conventional VSI.

The value of the switched-capacitor is designed and the simulation is performed using MATLAB/SIMULINK while the experimental verification is done for the passive load. An OPAL-RT 4510 with a digital output board is used to generate the pulses for the MOSFET inverter switches. The proposed work can be used with existing three-phase bridge inverters. The SCVSI can be used for various low to medium voltage applications i.e. electric vehicles, photovoltaics, battery energy storage systems etc.

Chapter 1
INTRODUCTION

1.1 BACKGROUND

As consumption of energy is increasing day by day, conventional energy resources are expected to exhaust very quickly. Consequently, researchers are emphasizing to find alternate sources of energy and to also use the energy efficiently [1]. This gives the rise to photovoltaic power generation, electric vehicles, battery energy storage systems etc. Among such technologies, the DC-AC converters are indispensable part of the power conversion system. It can be seen from Figure 1.1, that in the electric vehicle, a DC-AC converter is needed to transfer the power from the battery to the motor. This converter can be DC to single-phase or three-phase AC depending on the motor used in the traction system. Such traction systems employ different type of inverters. These include, voltage source inverters (VSIs), current source inverters (CSIs) and Z-source inverters (ZSIs) [2]. Each of the inverters has its own merits and demerits. Most of the traction inverters are the three-phase VSIs because of their higher efficiency and low cost. However, VSIs are inherently buck in nature. Therefore voltage boosting is required for VSIs. The CSIs can boost the output voltage but their efficiency is quiet low in comparison to the VSIs [3]. The Z-source inverters can either buck or boost the voltage as per the requirement. Also, its efficiency is better than the combination of VSI and DC-DC boost converter for low voltage gain ratio [4]. But the presence of the passive components increases its volume and cost.

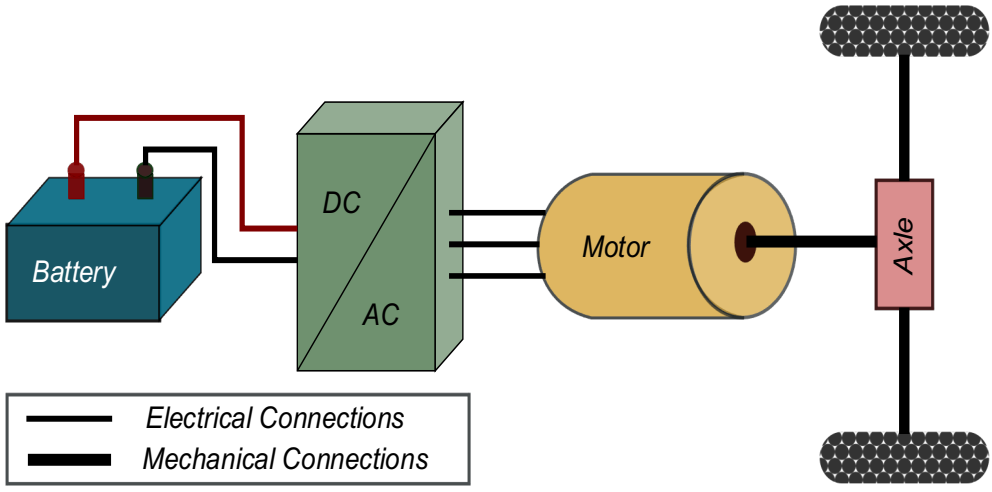

Figure 1.1: General Structure of EVs

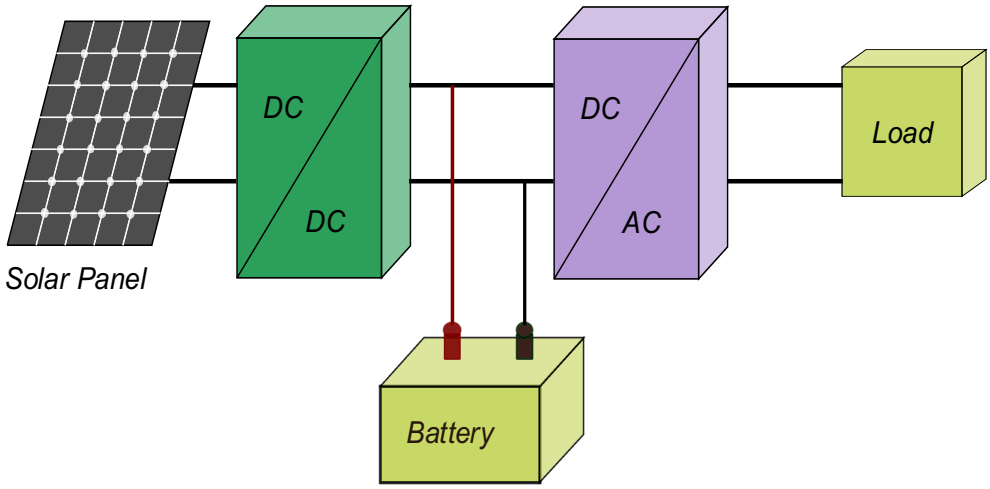

Figure 1.2: Layout for PV System

There are many typical applications such as Photovoltaic or fuel cells, which generate low voltage DC and require the boost converters before the power is fed to the grid or AC load. This typical arrangement it presented as Figure 1.2. A voltage boosting DC-DC converter is connected with the solar panel to extract maximum power through the MPPT technique at different levels of irradiance. This system further requires an inverters to fed the power to AC load. With the utilization of two converters, the system becomes large and costlier. Therefore, with an inverter capable of voltage boosting, the requirement of DC-DC boost converters can be eliminated.

With inverters being an integral part of the power conversion system, many inverter topologies such as cascaded H-bridge [5], diode clamped [6], flying capacitor [7], etc. have been presented to obtain multilevel voltage at the output. In recent times, with the advent of silicon carbide/gallium nitride wide band gap switching devices, researchers are emphasizing the use of high voltage converters to reduce the conduction losses. However, usage with the high voltage sources is still very complicated because of the reliability and cost of the Battery Management System (BMS) [8]. Also, the voltage source inverters work as buck converters. Therefore, voltage boosting at the input of the inverter is required. Most of the time, to step up the voltage before the inverter, dc-dc boost converters are used [9].

The Figure 1.3 presents the schematic of boost three-phase inverter. This method requires an inductor at the front end resulting in a large size of the power conversion system and lower efficiency. To overcome this, switched-capacitor inverters have been proposed to boost the inverter voltage [10]. Various switched-capacitor-based inverter topologies have

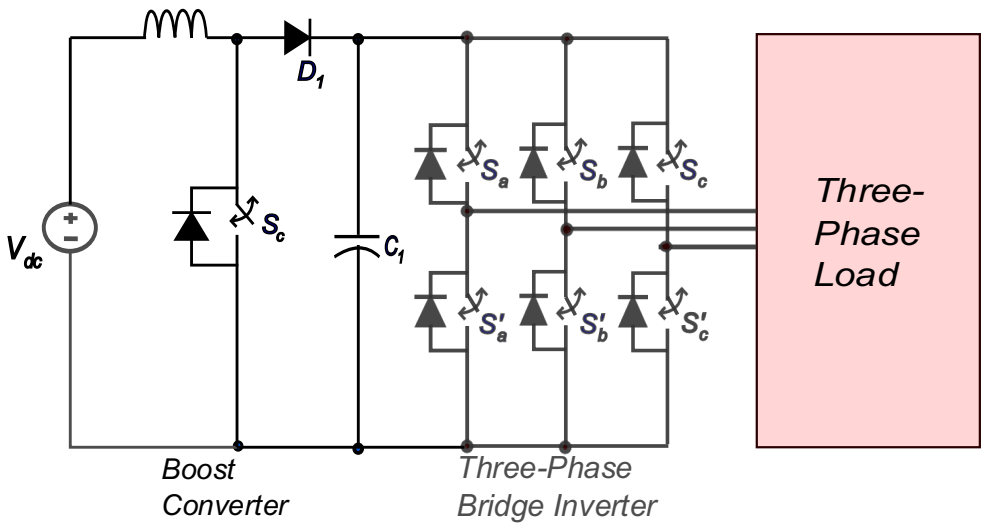

Figure 1.3: Conventional Boost Three-Phase Bridge Inverter

been proposed to date [11]. However, in switched capacitor VSIs, peak charging current is a major issue, as the capacitor is connected in parallel with the load and the source during the charging time. For three-phase inverter topologies, capacitors are used in each leg to boost the voltage. Consequently, the number of passive components and size of the power conversion unit increases

Therefore, the scope is identified to boost the three-phase VSI voltage using a single switched capacitor unit at the front end with SPWM and to reduce the capacitor charging current.

1.2 LITERATURE REVIEW

With the increase in demand for energy, it has become very important to channelise the efforts to reduce the dependence on conventional resources for energy requirements [1]. Therefore, electrification of traction systems and PV-based generation of power has gained a lot of popularity among academic and industrial researchers. Power conversion systems are very much needed for the mentioned advancements and inverters are the backbone of these systems.

1.2.1 Conventional Inverter Topologies

With DC-AC converters becoming an important part of the power conversion, there are several topologies proposed for DC-AC conversion. In the 1970s, a new topology is presented with a number of H-bridges connected in a series having separate electrical sources [5]. This topology is known as cascaded H-bridge topology.

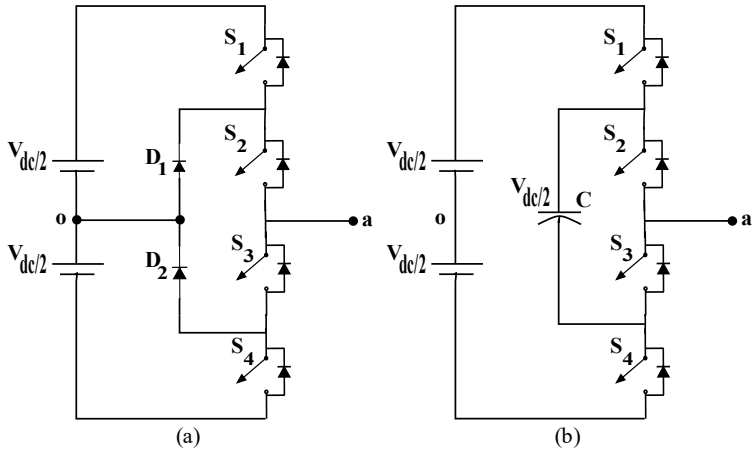

Figure 1.4: (a) NPC Multilevel Inverter (b) FC Multilevel Inverter

A new neutral point clamped PWM inverter comprising auxiliary and main switches as shown in Figure 1.4(a) was introduced in 1981 [6]. With the use of the auxiliary switches, the output voltage is clamped to the neutral point and a zero level in the output waveform is obtained resulting in the multilevel waveform at the output which significantly improves the harmonic profile of the AC output.

In [7], flying capacitor converters as shown in Figure 1.4(b) were proposed to be used as either voltage source converters or choppers. The multilevel waveform at the output can be obtained by utilizing the charging and discharging states of the capacitor. In flying capacitor converter topology, there are redundant states of operation which help to balance the capacitor voltage.

To analyse the reduction in harmonic distortion in a multilevel inverter, a generalized structure of a multilevel PWM inverter is presented in [12] with a simple PWM technique for a three-level output waveform. The specific harmonic can be eliminated by choosing the appropriate number of steps, width and height of the steps.

With the advancements in high voltage power switching devices such as SiC and GaN [13], academics and industrial researchers are steering toward the high voltage supply and high voltage inverters to reduce the size and losses of the system. But, using high voltage batteries is less reliable because of the complexity of BMS. To produce the high voltage from DC sources, a number of cells are needed to be connected in series and charge equalization becomes difficult. Therefore, boosting the voltage before the inverter and using a high voltage inverter is more beneficial [8].

The importance of boosting the input voltage of the inverter can also be understood as voltage source inverters are inherently buck in operation. The peak output voltage on the AC side is always less than the DC side voltage [14]. Therefore, for many applications like renewable energy sources, which are not high voltage sources, voltage elevation is required before the inverter.

1.2.2 Boost Inverter Topologies

To boost the conventional VSI, a topology is analysed in [9]. It has a conventional dc-dc boost converter at the front end of the inverter to step up the voltage at the input of the inverter. It produces more voltage on the ac side than the supplied dc voltage. However, the inductor at the front end makes the system bulkier.

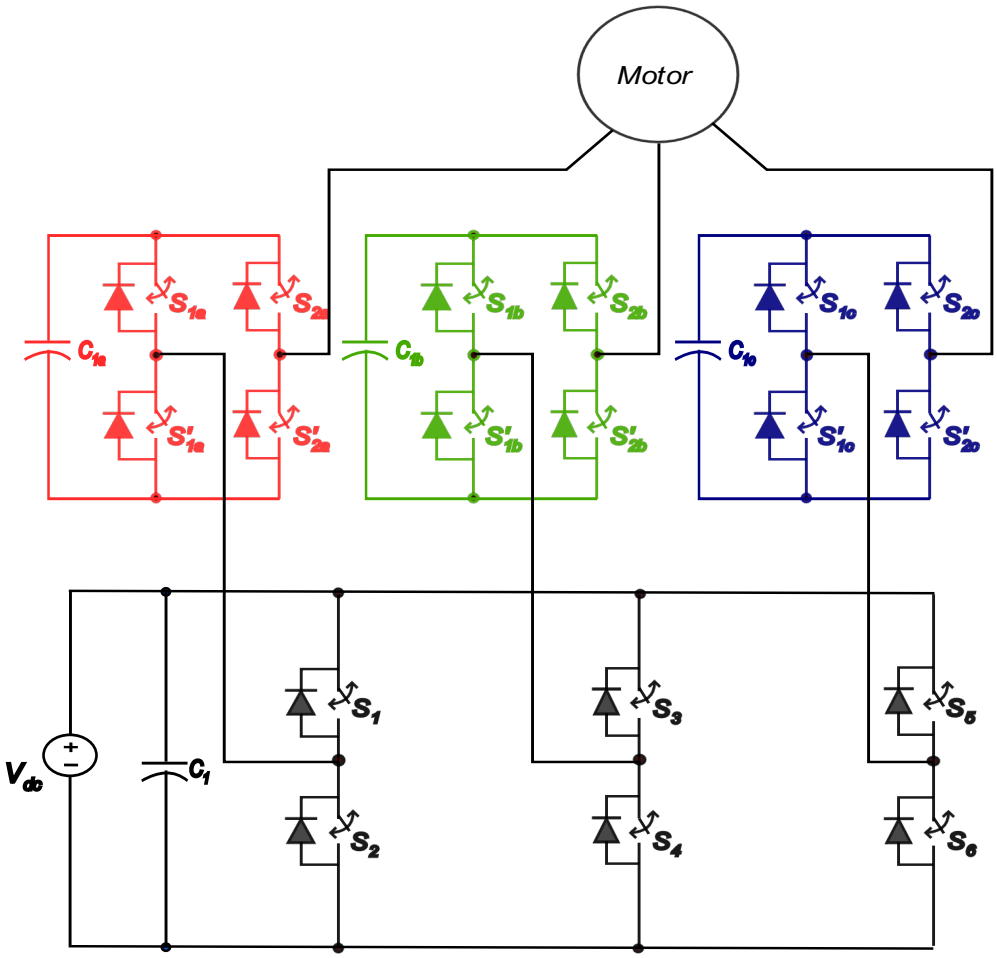

Figure 1.5: Switched capacitor inverter topology proposed in [14]

Z-source converter is proposed [15] to overcome the limitations of conventional buck and boost inverters. In this converter, shoot-through states are used in addition to active and null states of the conventional VSI. But, the addition of passive components increases the size and the cost of the system.

A novel method to build a three-phase boosting VSI is introduced by Darwish [16]. Čuk converters are connected separately in a three-phase arrangement. Boosted voltage is obtained at the output side of VSI. However, Čuk converters are inherently non-linear, which increases the complexity in control and cost of the system.

The motor's neutral point is connected to the battery in [17] to boost the inverter output voltage. The function of voltage boost-up is performed by utilizing the motor's leakage inductance rather than using an additional inductor at the front end of the inverter. Consequently, less number of components will be used.

1.2.3 Switched Capacitor Inverter Topologies

Initial work on a switched-capacitor-based inverter is produced in [10] without using an inductor. Capacitors are connected in series and parallel in an alternating manner. During parallel connections, capacitors are getting charged and during series connections, the inverter is working in a boosting mode and capacitors are getting discharged. However, there is no discussion about the charging current in the capacitor branch.

A switched-capacitor-based inverter topology is proposed in [18] as shown in Figure 1.5. Each leg of the conventional three-phase VSI is connected to an H-bridge including a capacitor. Hence, a multilevel waveform is obtained at the output. But the number of components is huge in this proposed structure resulting in complexity in controlling of devices and a high initial cost of the system.

In recent times, various switched-capacitor-based inverter topologies such as [19], and [20], have been proposed. Three-phase operation is discussed in these topologies. But, separate switched capacitors are required for separate phases. Therefore, the number of components used for three-phase operations is very large. Also, the charging current in the capacitor loop is higher in comparison to the load current.

1.2.4 Modulation Techniques

An evaluation of the carrier-based pulse width modulation is carried out in [21]. The advantages of modified sinusoidal PWM are discussed. However, using a particular Sinusoidal PWM should be application-based as each one has its own merits for a particular application.

The relationship between sinusoidal PWM and space vector PWM is analysed in [22] as both the approaches can increase the linear modulation ranges and SPWM can also imitate the SVPWM with some modifications. It is shown how equal null states (000 and 111) can be obtained with variable amplitude of injected third harmonic. It is to be noted that the time period for both the null states in a single switching cycle for modified SPWM is not the same for any constant amplitude of injected third harmonic.

1.3 RESEARCH GAPS

From the above literature review, it has been observed that boosting VSIs are characterized with number of advantages. However, there are some limitations as summarized below:

1. The conventional boosting DC-DC converter, utilizes an inductor, which results in large size of the power conversion units.
2. In three-phase topologies for switched-capacitor inverters, capacitors are used in each leg. It also uses a large number of components for balancing the switched capacitor, which make the system bulkier and costlier.
3. The capacitor comes in parallel with the load and the supply during charging. Consequently, a large current flows through the capacitor loop, which could lead to component damage and system failure.
4. Most of the recent topologies require an altogether new structure and a new system for modulation, thereby obsoleting the existing systems.

1.4 OBJECTIVES OF WORK

The following objectives are identified for the study:

1. Reduce the number of capacitors and switches in the existing three-phase structure for voltage boosting VSIs
2. Realize a modulation technique to control the peak charging current in the capacitor loop of switched-capacitor-based inverters
3. Validate the proposed work through simulation/experimentation

1.5 METHODOLOGY

It has been studied that most of the traction inverters are three-phase VSIs due to their high efficiency and low cost. However, voltage boosting or a high voltage source is required before the VSIs due to their buck characteristic. The availability of high voltage DC sources is scanty with respect to the industrial demand. Thereupon, research was focused on providing a boost to the inverter output.

Switched-capacitor method was favored for study against the conventional boosting methods using inductors due to the reduced size of the system and fewer losses. As various switched capacitor topologies are already available, hence, major issues such as a large number of components and charging current for switched-capacitor boosting in inverters have been addressed.

Few topologies that are already being used for various applications were studied with the prospect of advancement in them. Subsequently, the three-phase bridge voltage source inverter is chosen for introducing the switched capacitor unit at its front end. Because of its simple structure and existence in the market, the proposed changes can be retrofitted with ease.

To obtain a boosting pole voltage in each leg from the varying front-end voltage, the system was analytically and graphically studied with respect to the different switching states. A peculiar scheme was conceptualized that could produce the boosting at intermediate levels with a single capacitor for all three legs. For generating these switching signals, different modulation schemes were deliberated, and a modified sine pulse width modulation technique was considered, because of ease of its implementation and maximum source utilization.

Designing of the system capacitor is carried out analytically for practical implementation. Some assumptions were made to perform the calculations. It was taken care that the deviation from the actual results because of these assumptions were insignificant. The equation to design the capacitor is obtained in terms of modulation index, boosting factor, load current, carrier frequency and capacitance. The fundamental component of the output PWM line-line voltage was analytically derived based on some assumptions [14]. These derived results were also verified from Simulink results.

The simulation was performed for the proposed work (with a single SCU and two SCUs) using MATLAB/SIMULINK 2017a. Specialized technology blocks for the power system from the simscape library were used to prepare the model. The discrete solver with a fixed step size of 1 microsecond was used to run the model.

To validate the analytical and simulated results, experimental results were taken from the setup as discussed in chapter 5. The DC power is taken from the regulated power supply rated 30 V, 2A. The pulses for the modulation are obtained from the digital board of OPAL-RT 4510 output. MOSFET switches are used because of their better efficiency at higher frequencies. The results are visualized with the help of a digital storage oscilloscope (Yokogawa DL 950).

1.6 DISSERTATION STRUCTURE

This dissertation consists of six chapters, which are briefed hereunder as:

In **chapter 1**, the background and the literature review are presented. Previous research related to inverter topologies and their modulation is analysed. Research gaps and objectives of the study with applications of VSIs are also be reviewed. the methodology for the produced work is discussed. Software and hardware used for the work are listed.

In **chapter 2**, an analysis related to the circuit of the three-phase bridge inverter with a single switched capacitor unit will be done. Its detailed theory and analytical calculations are presented and verified with the simulation results.

In **chapter 3**, an analysis of the structure and working of the three-phase bridge inverter with two switched capacitor units will be done. Its operation and proposed modulation will also be discussed in detail.

In **chapter 4**, simulation is done for different boosting factors and results are discussed for the presented switched capacitor boost inverter with the proposed modulation strategy

In **chapter 5**, hardware results are shown for the presented switched capacitor boost inverter with the proposed modulation strategy

Conclusion and future scope are discussed in **chapter 6**.

Chapter 2

THREE-PHASE BRIDGE INVERTER WITH A SINGLE SCU

2.1 DESCRIPTION OF THE TOPOLOGY

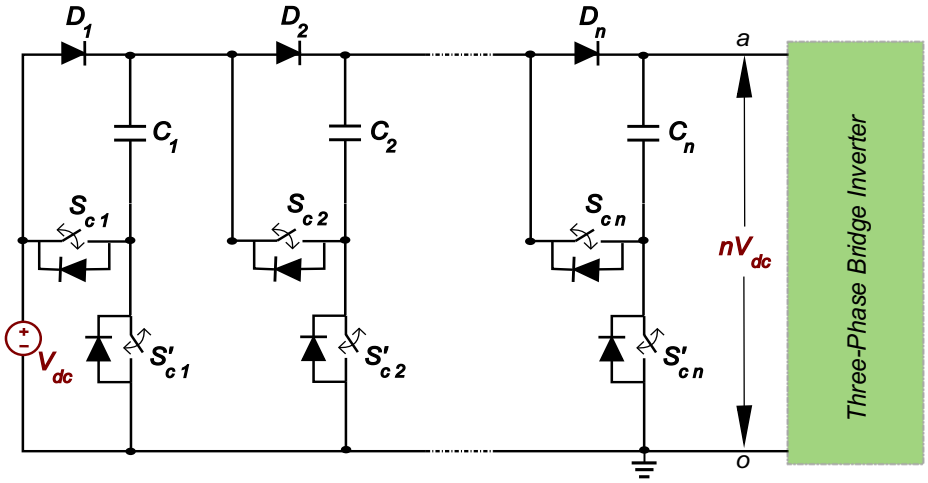

Figure 2.1: 3-ø bridge inverter with n number of switched-capacitor units at the front end

The structure of the topology and proposed modulation strategy is discussed in this chapter. The general layout of the topology is presented in Figure 2.1. Basically, n number of SCUs are introduced on the front end side with DC source in conventional three-phase bridge inverter. A single SCU comprises two switches, a diode and a capacitor. The diode is there to prevent the short-circuiting of the capacitor. Switches S_{cn} and S'_{cn} are complementary in nature. During normal operation switch, S'_{cn} will conduct, keeping the switched-capacitor in a charging state. Switch S_{cn} will conduct during boosting state in a switching cycle keeping switched capacitor in discharging state.

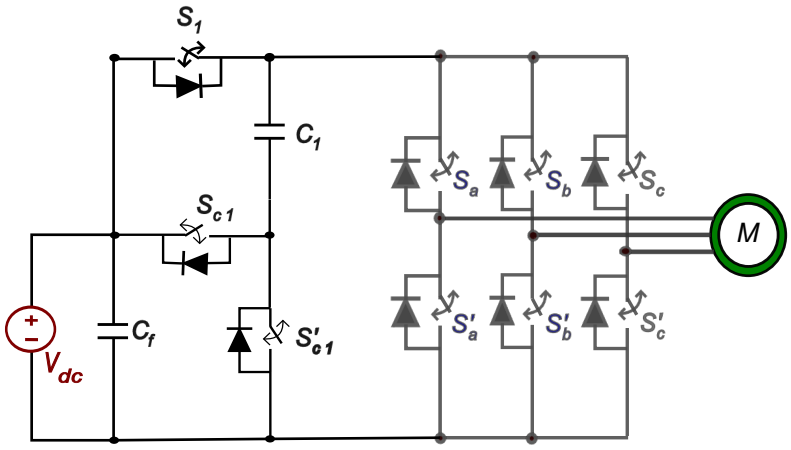

Figure 2.2: Switched capacitor unit with a switch for reverse power flow

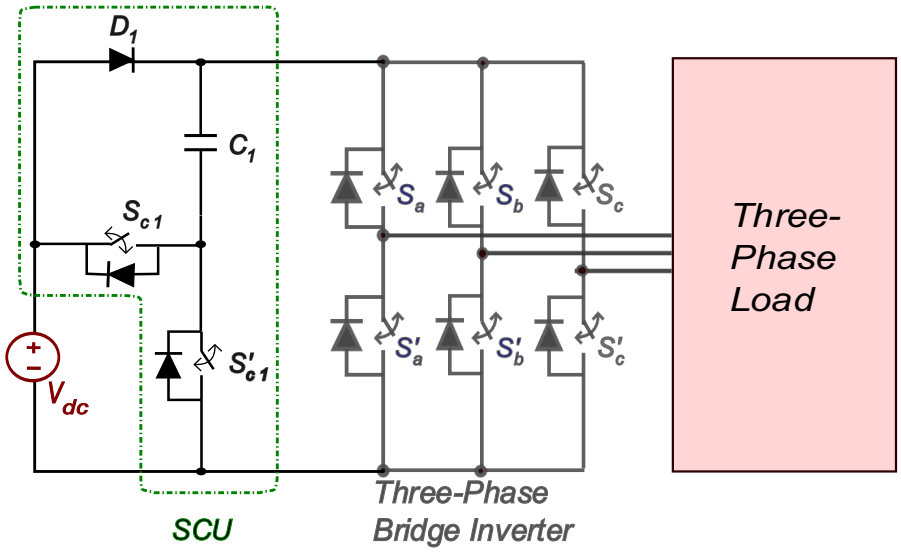

Figure 2.3: 3-ø bridge inverter with single SCU at the front end

For some cases where reverse power flow is also required such as regenerative braking, the diode in the topology can be replaced with a power switch as shown in Figure 2.2. The Converter will now work as a three-phase rectifier. Another capacitor is introduced in parallel with the DC terminal side to smooth out the ripples in output voltage.

In this chapter, a three-phase bridge with a single switched capacitor unit as shown in Figure 2.3 is used for analysis. The very difference of this structure is, that only one switched capacitor is required to boost the voltage in all three legs of the inverter. Also, the conventional three-phase bridge VSI is readily available for industrial applications. So, the given topology can be reassembled in the conventional inverters for boosting the voltage.

2.1.1 Switching States

There are 8 switching states available for traditional three-phase bridge VSI as given in Table 2.1. Out of the 8 switching states, 6 states are active states and 2 are null states. These null states are sometimes replaced with active vectors for CMV reduction [23], But for boosting the inverter voltage, these states are very important for the modulation of the topology and charging of the capacitors. It is discussed in further sections.

Table 2.1: Switching states for 3-phase bridge VSI

Sr. No.	Switching State ($S_1S_2S_3$)	State Name	Active/Null State
1.	000	A_1	Null
2.	100	A_2	Active
3.	110	A_3	Active
4.	010	A_4	Active
5.	011	A_5	Active
6.	001	A_6	Active
7.	011	A_7	Active
8.	111	A_8	Null

2.1.2 Modes of operation

Two levels of voltages that is V_{dc} and $2V_{dc}$ can be obtained at the virtual link *ao* using different modes of operation discussed as follows

Mode-I: During this mode, the voltage at virtual link *ao* is the same as the source voltage V_{dc}. Switch S_c' will conduct in this mode making the capacitor in parallel with the load and voltage source as shown in Figure 2.4. Capacitor charging will take place during this mode. Only equivalent series resistance (ESR) of capacitor and switch resistance is there in the charging loop.

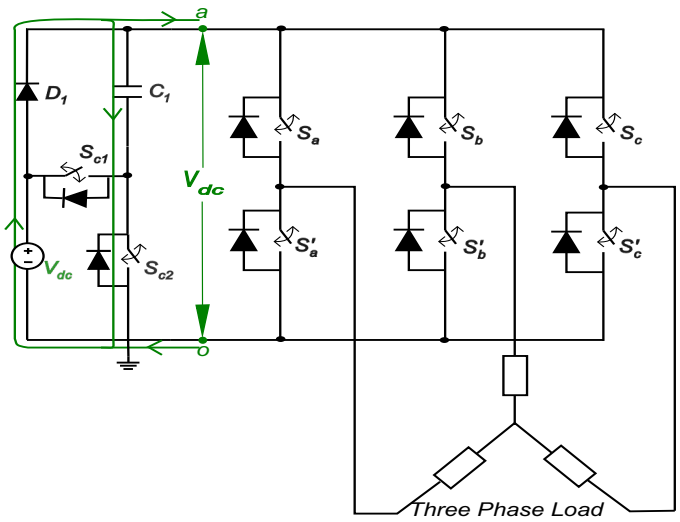

Figure 2.4: Mode of operation 1 for $V_{ao} = V_{dc}$

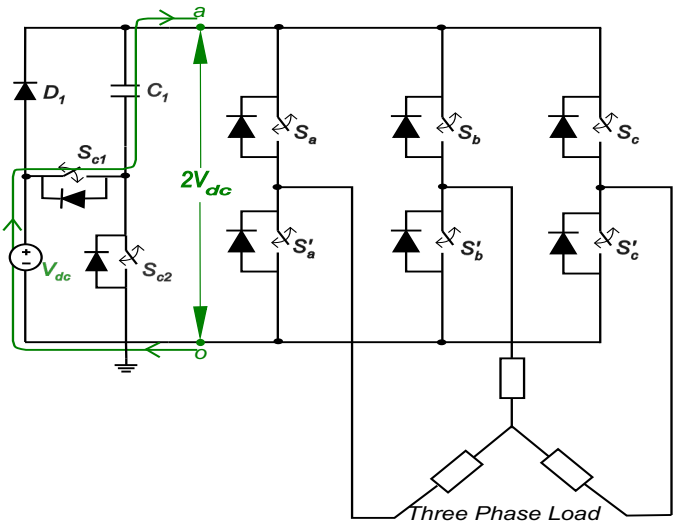

Figure 2.5: Mode of operation 1 for $V_{ao} = 2V_{dc}$

Mode-II: Switch S_c is turned on during this mode of operation. The capacitor will be in discharging mode and variable voltage V_{ao} becomes twice the source voltage as shown in Figure 2.5. This boosted voltage can be utilised with two different modulation schemes to boost the VSI output voltage as discussed in the next section.

2.1.3 Voltage equations

Switches $S_a \& S'_a, S_b \& S'_b, S_c \& S'_c$ and $S_c \& S'_c$ are complementary in nature. Therefore voltage equations for the given converter can be written in the terms of switching signals of the switches as follows:

Pole voltages:

$$V_{Ao} = (1 - A'_a)(2 - A'_c)V_{dc} \quad (2.1)$$

$$V_{Bo} = (1 - A'_b)(2 - A'_c)V_{dc} \quad (2.2)$$

$$V_{Co} = (1 - A'_c)(2 - A'_c)V_{dc} \quad (2.3)$$

Line Voltages:

Since $V_{L_1L_2} = (V_{L_1} - V_{L_2})$

Therefore,

$$V_{AB} = (A'_b - A'_a)(2 - A'_c)V_{dc} \quad (2.4)$$

$$V_{BC} = (A'_c - A'_b)(2 - A'_c)V_{dc} \quad (2.5)$$

$$V_{CA} = (A'_a - A'_c)(2 - A'_c)V_{dc} \quad (2.6)$$

Phase Voltages:

Since for three-phase bride inverter, $V_{L_1N} = \frac{[2V_{L_1} - V_{L_2} - V_{L_3}]}{3}$

Therefore,

$$V_{AN} = \frac{[(A'_b + A'_c - 2A'_a)(2 - A'_c)V_{dc}]}{3} \quad (2.7)$$

$$V_{BN} = \frac{[(A'_a + A'_c - 2A'_b)(2 - A'_c)V_{dc}]}{3} \quad (2.8)$$

$$V_{CN} = \frac{[(A'_b + A'_a - 2A'_c)(2 - A'_c)V_{dc}]}{3} \quad (2.9)$$

where A_i is the switching function of the i^{th} switch and can be defined as:

$$A_i = \begin{cases} 1 \text{ if switch } i \text{ is On} \\ 0 \text{ if switch } i \text{ is Off} \end{cases}$$

2.2 MODULATION OF TOPOLOGY

Modified (Third harmonic injected) SPWM technique is used for switching the three legs of the inverter. This technique helps in maximum utilization of the DC source [21]. It is presented in Figure 2.6. The first thing to be analysed is reference signals are changing their order after every 60 degrees. Their importance is discussed further while presenting the operation. It can be observed from the figure that the left-aligned sawtooth waveform is used as a carrier signal resulting in right-aligned switching signals. It is easy to analyse and understand the concept of switched-capacitor modulation from a one-sided aligned signal than from a centre-aligned switching signal. For this modulation, 1/5 times the amplitude of the reference sine wave has been used as amplitude for injected third harmonic and calculations have also been carried out taking the same.

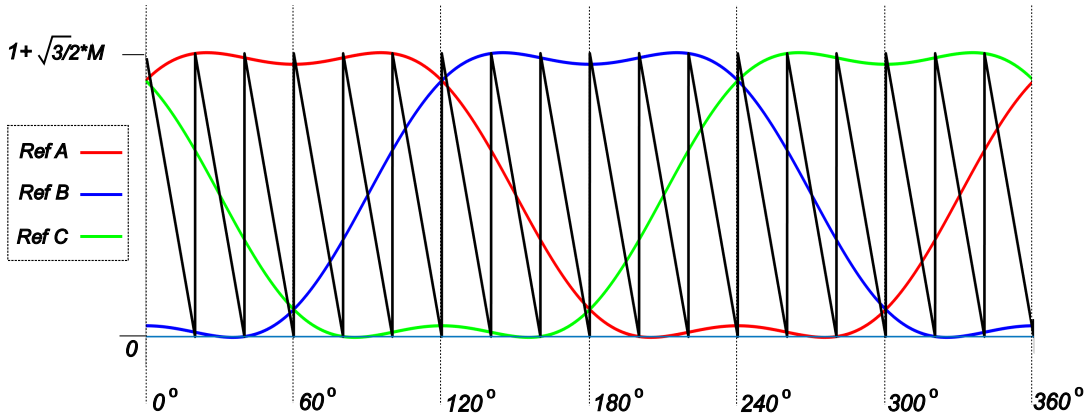

Figure 2.6: Modulation scheme for whole active state boosting

As Modified SPWM is being used, the linear operating range for the inverter will be increased and the modulation index can be expressed as

$$0 < M \leq 1.154$$

There can be 2 types of modulation for operation.

Type-I:

$$b = 1$$

Type-II:

$$0 < b \leq 1$$

Where b is the boosting factor.

Boosting factor is broadly a term used for the fraction of the switched capacitor turn-on time with respect to the total active state duration.

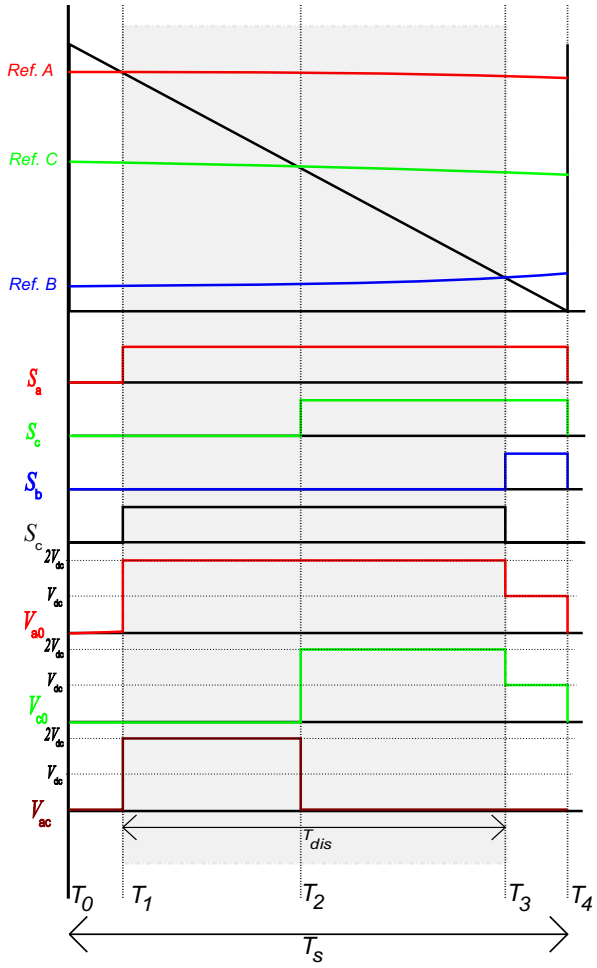

Figure 2.7: One switching cycle for whole active state boosting condition (Type-1)

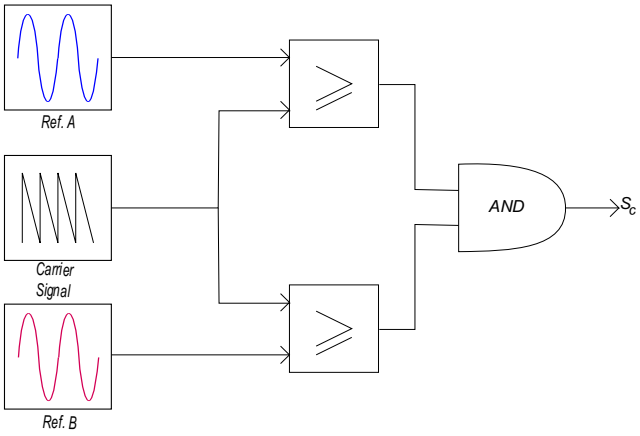

Figure 2.8: Schematic representation for type-I modulation

Type 1: If the switched-capacitor operates in discharging mode for the whole of the active state duration in a switching cycle, a three-level boosting line voltage can be obtained at the inverter output. As the switched-capacitor is getting charged only at null states, the charging time will be less than the discharging duration, resulting in a large fall in capacitor voltage V_c. High current will flow in a parallel charging loop due to only ESR of the capacitor and switch resistance in the loop.

To turn on the switched capacitor for the whole active state, a simple carrier-based modulation technique is used as shown in Figure 2.6 . It could also be observed from the figure, that when Ref_A is greater than the carrier signal and Ref_B is less than the carrier signal, the capacitor is working in series with the source and load for complete active state duration. But it should be taken care that the order of the references changes after every sixty degrees, so reference signals must be altered as per their order which is quite similar to the sector defining in space vector modulation (SVM), let us call it a segment. The modulation given in Figure 2.6 is for segment 1.

One switching cycle of type-I modulation is presented in Figure 2.7 for analysis. In this figure, from T_0 to T_1, null state A_1 and from T_3 to T_4, null state A_8 are present. From T_1 to T_3, 2 active states A_2 and A_3 are there. The switched capacitor is turned on for the whole of the active state duration and boosted line voltage V_{ac} is obtained. It is easy to modulate the switched capacitor for total active state duration without any additional reference signals as shown in Figure 2.8. For this modulation, the voltage drop across the capacitor will be large for the switching cycle, when active state duration will be maximum.

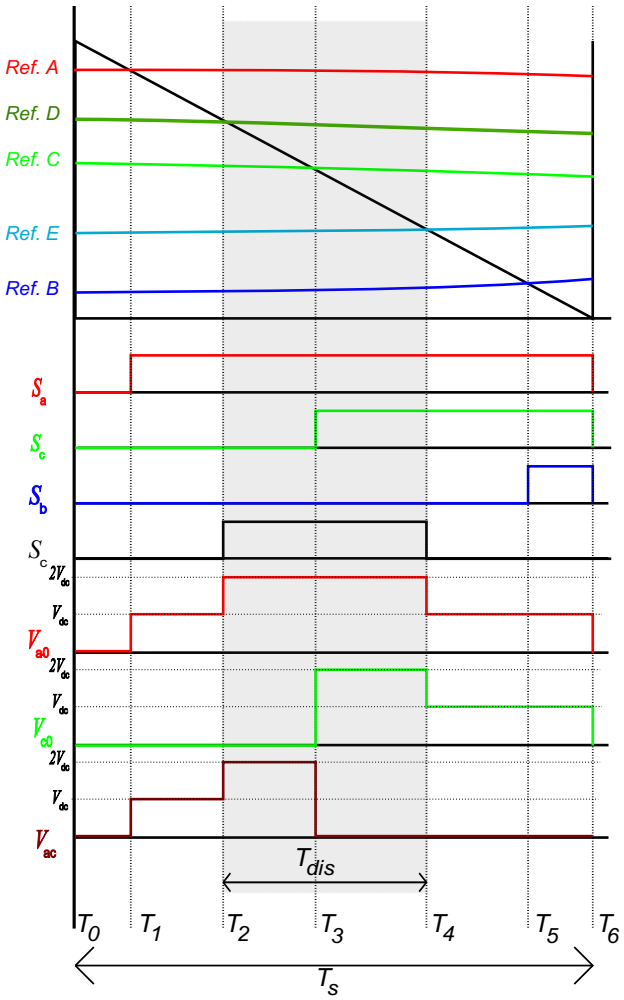

Figure 2.9: One switching cycle for fractional boosting of active state duration (Type-II)

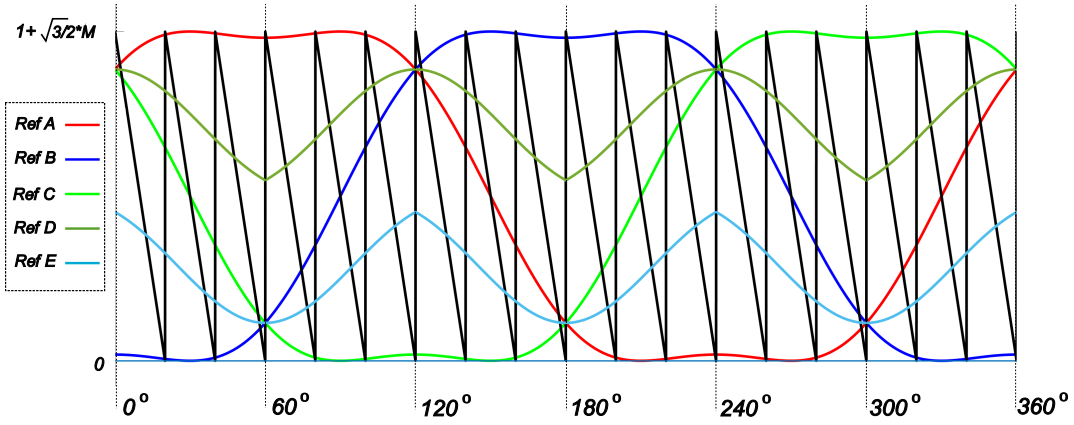

Figure 2.10: Modulation Scheme for fractional boosting of active state duration.

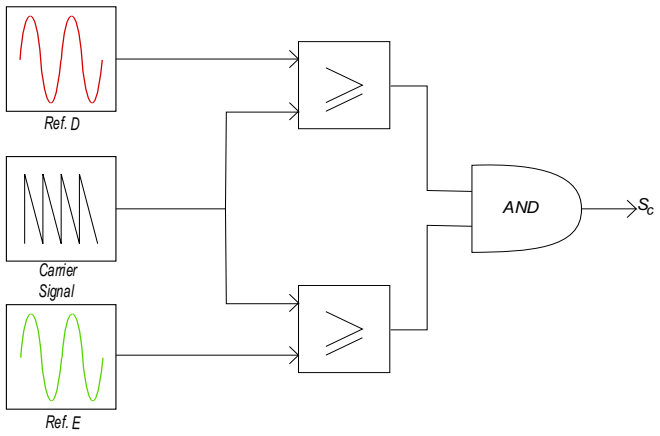

Figure 2.11: Schematic representation for type-II modulation

Type 2: In this modulation technique, the switched-capacitor is turned on for a fraction (boosting duration) of the total active state period. Signals for the single switching period are shown in Figure 2.9. It can be observed that switched capacitor is in series with the source only for part of the total active duration. Hence, the capacitor will get discharged for less time resulting in a low voltage drop in the capacitor. Although, to turn on the capacitor in between the active state for approx. small duration, new reference signals are needed as presented in Figure 2.10. How these reference signals are generated is discussed in a further sub-section. Now, instead of using Ref_A and Ref_B in segment 1 for modulation of switched-capacitor, Ref_D and Ref_E are used as shown in Figure 2.11.

Table 2.2: Segment-wise reference generation

Segment	$\boldsymbol{Reference_D}$	$\boldsymbol{Reference_E}$
1	$Ref_A * (b) + Ref_C * (1-b)$	$Ref_C * (1-b) + Ref_B * (b)$
2	$Ref_A * (b) + Ref_B * (1-b)$	$Ref_B * (1-b) + Ref_C * (b)$
3	$Ref_B * (b) + Ref_A * (1-b)$	$Ref_A * (1-b) + Ref_C * (b)$
4	$Ref_B * (b) + Ref_C * (1-b)$	$Ref_C * (1-b) + Ref_A * (b)$
5	$Ref_C * (b) + Ref_B * (1-b)$	$Ref_B * (1-b) + Ref_A * (b)$
6	$Ref_C * (b) + Ref_A * (1-b)$	$Ref_A * (1-b) + Ref_B * (b)$

2.2.1 Reference Signal Generation

As carrier frequency is very high as compared to the reference signal, it can be assumed that the reference signal is linear and almost constant for a single switching cycle. On this assumption, new reference signals can be generated to modulate the SCU for fraction of the total time period of active states in a switching cycle. Assign a variable *b* to the fraction of the total active state's time period in a cycle. As discussed earlier, reference signals are changing their order after 60 degrees, therefore, new reference signals should be formed segment-wise as stated in Table 2.2.

2.3 DESIGN OF CAPACITOR

2.3.1 Analytical Derivation

As discussed, three modified sinusoidal references shifted by 120 degrees from each other are being used for the proposed modulation of the inverter. The third harmonic is injected with an amplitude of $\frac{M}{5}$. Reference signals are shifted to the positive side by adding 1 to make the calculations easy for the generation of Ref_D and Ref_E for switched-capacitor modulation. Three reference signals are listed below:

$$Ref_A = 1 + MSin\left(\omega t + \frac{\pi}{6}\right) + \frac{M}{5}Sin\left(3\omega t + \frac{\pi}{2}\right) \tag{2.10}$$

$$Ref_B = 1 + MSin\left(\omega t - \frac{\pi}{2}\right) + \frac{M}{5}Sin\left(3\omega t + \frac{\pi}{2}\right) \tag{2.11}$$

$$Ref_C = 1 + MSin\left(\omega t + \frac{5\pi}{6}\right) + \frac{M}{5}Sin\left(3\omega t + \frac{\pi}{2}\right) \tag{2.12}$$

To find out the turn-on time for different switches in a switching cycle, the value of the reference signal for that particular switching period is required. To calculate the value of reference and turn-on time of switches, some assumptions should be made. With switching frequency being very high, it can be assumed that the reference signals for a single switching cycle are linear and almost constant [14]. Therefore, for one switching cycle, the mean value can be calculated for three reference signals as (2.13), (2.14) and (2.15). It can be analysed that time at the starting and end of the switching cycle can be written as a product of the switching cycle and the switching period.

$$\overline{Ref_{A_{(T_S)}}} = \frac{\left[1+MSin\left(\omega(n-1)T_S+\frac{\pi}{6}\right)+\frac{M}{5}Sin\left(3\omega(n-1)T_S+\frac{\pi}{2}\right)+\ 1+MSin\left(\omega(n)T_S+\frac{\pi}{6}\right)+\frac{M}{5}Sin\left(3\omega(n)T_S+\frac{\pi}{2}\right)\right]}{2} \quad (2.13)$$

$$\overline{Ref_{B_{(T_S)}}} = \frac{\left[1+MSin\left(\omega(n-1)T_S-\frac{\pi}{2}\right)+\frac{M}{5}Sin\left(3\omega(n-1)T_S+\frac{\pi}{2}\right)+\ 1+MSin\left(\omega(n)T_S-\frac{\pi}{2}\right)+\frac{M}{5}Sin\left(3\omega(n)T_S+\frac{\pi}{2}\right)\right]}{2} \quad (2.14)$$

$$\overline{Ref_{C_{(T_S)}}} = \frac{\left[1+MSin\left(\omega(n-1)T_S+\frac{5\pi}{6}\right)+\frac{M}{5}Sin\left(3\omega(n-1)T_S+\frac{\pi}{2}\right)+\ 1+MSin\left(\omega(n)T_S+\frac{5\pi}{6}\right)+\frac{M}{5}*Sin\left(3\omega(n)T_S+\frac{\pi}{2}\right)\right]}{2} \quad (2.15)$$

As reference signals are changing their order after 60 degrees (segment) but duration for active states and nulls states are similar and repeating for each segment, analysis for only 1st segment is carried out to calculate the maximum voltage drop across the capacitor. The number of switching cycles in one segment can be calculated as (2.16). Here, f_s is the switching frequency and f_r is the frequency of reference signals.

$$N_s = \frac{f_s}{6f_r} \quad (2.16)$$

We know that,

$$\omega = 2\pi f_r \ and \ T_s = \frac{1}{f_s}$$

By putting the above values in (2.13), (2.14) and (2.15), we will get averaged reference values for one switching cycle in one segment.

$$\overline{Ref_{A_{(nT_S)}}} = \frac{\left[\frac{1}{2}+MSin\left(\frac{\pi}{3N_S}(n-1)+\frac{\pi}{6}\right)+\frac{M}{5}Sin\left(\frac{\pi}{N_S}(n-1)+\frac{\pi}{2}\right)+MSin\left(\frac{\pi}{3N_S}(n)+\frac{\pi}{6}\right)+\frac{M}{5}Sin\left(\frac{\pi}{N_S}(n)+\frac{\pi}{2}\right)\right]}{2} \quad (2.17)$$

$$\overline{Ref_{B_{(nT_S)}}} = \frac{\left[\frac{1}{2}+MSin\left(\frac{\pi}{3N_S}(n-1)-\frac{\pi}{2}\right)+\frac{M}{5}Sin\left(\frac{\pi}{N_S}(n-1)+\frac{\pi}{2}\right)+MSin\left(\frac{\pi}{3N_S}(n)-\frac{\pi}{2}\right)+\frac{M}{5}Sin\left(\frac{\pi}{N_S}(n)+\frac{\pi}{2}\right)\right]}{2} \quad (2.18)$$

$$\overline{Ref_{C_{(nT_S)}}} = \frac{\left[\frac{1}{2}+MSin\left(\frac{\pi}{3N_S}(n-1)+\frac{5\pi}{6}\right)+\frac{M}{5}Sin\left(\frac{\pi}{N_S}(n-1)+\frac{\pi}{2}\right)+MSin\left(\frac{\pi}{3N_S}(n)+\frac{5\pi}{6}\right)+\frac{M}{5}Sin\left(\frac{\pi}{N_S}(n)+\frac{\pi}{2}\right)\right]}{2} \quad (2.19)$$

Now, the switching cycle with maximum duration for active state is $\frac{N_S}{2}$ or $\left(\frac{N_S}{2}+1\right)$

To find out mean value of reference signal for switching cycle with maximum active state, Put the value of $n = \frac{N_S}{2}$ if N_s is odd and $n = \left(\frac{N_S}{2}+1\right)$ if N_s is even, in equation (2.17), (2.18) and (2.19).

$$\overline{Ref_{A_{nmax}}} = \ 1 + \frac{\sqrt{3}M}{4} + \frac{\sqrt{3}M}{4}Cos\left(\frac{\pi}{3N_S}\right) - \frac{M}{4}Sin\left(\frac{\pi}{3N_S}\right) + \frac{M}{10}Sin\left(\frac{\pi}{N_S}\right) \quad (2.20)$$

$$\overline{Ref_{B_{nmax}}} = \ 1 - \frac{\sqrt{3}M}{4} - \frac{M}{4}Sin\left(\frac{\pi}{3N_S}\right) - \frac{\sqrt{3}M}{4}Cos\left(\frac{\pi}{3N_S}\right) + \frac{M}{10}Sin\left(\frac{\pi}{N_S}\right) \quad (2.21)$$

$$\overline{Ref_{C_{nmax}}} = 1 + \frac{M}{2} Sin\left(\frac{\pi}{3N_s}\right) + \frac{M}{10} Sin\left(\frac{\pi}{N_s}\right) \quad (2.22)$$

As listed in Table 2.2, equation for ref_D and Ref_E for segment 1 can be written as follows

$$Ref_D = Ref_A * b + Ref_C * (1 - b) \quad (2.23)$$

$$Ref_E = Ref_B * b + Ref_C * (1 - b) \quad (2.24)$$

By algebraic manipulation of earlier listed equations, the value of Ref_D and Ref_E for the switching cycle with maximum active duration can be calculated as:

$$\overline{Ref_{D_{nmax}}} = 1 + \frac{\sqrt{3}Mb}{4} + \frac{\sqrt{3}Mb}{4} Cos\left(\frac{\pi}{3N_s}\right) - \frac{3Mb}{4} Sin\left(\frac{\pi}{3N_s}\right) + \frac{M}{2} Sin\left(\frac{\pi}{3N_s}\right) + \frac{M}{10} Sin\left(\frac{\pi}{N_s}\right) \quad (2.25)$$

$$\overline{Ref_{E_{nmax}}} = 1 - \frac{\sqrt{3}Mb}{4} - \frac{\sqrt{3}Mb}{4} Cos\left(\frac{\pi}{3N_s}\right) - \frac{3Mb}{4} Sin\left(\frac{\pi}{3N_s}\right) + \frac{M}{2} Sin\left(\frac{\pi}{3N_s}\right) + \frac{M}{10} Sin\left(\frac{\pi}{N_s}\right) \quad (2.26)$$

The equation for carrier signal is

$$y(t) = -2f_c t + 2$$

On comparing we will get $t_{on}\ and\ t_{off}$ for switched capacitor operation in the switching cycle with maximum active state duration.

Therefore, $S_{c(on)max} = t_{dis(\max)} = t_{off} - t_{on}$

By simplifying the above equations, we get

$$t_{dis(max)} \approx \frac{\sqrt{3}Mb}{4f_c}\left[Cos\left(\frac{\pi}{3N_s} + 1\right)\right] \quad (2.27)$$

$$\Delta V_{c(\max)} = \frac{I}{C} * t_{dis(max)}$$

It is to be noted that maximum voltage drop will be occurred for the purely resistive load. Therefore, the capacitor design equations are derived for the same.

$$\Delta V_{c(\max)} \approx \frac{\sqrt{3}IMb}{4Cf_c}\left[Cos\left(\frac{\pi}{3N_s} + 1\right)\right] \quad (2.28)$$

$$C \approx \frac{\sqrt{3}IMb}{4\Delta V_{c(\max)} f_c}\left[Cos\left(\frac{\pi}{3N_s} + 1\right)\right] \quad (2.29)$$

2.3.2 Verification Of Derived Equation From Simulation Results

The derived formula is verified by comparing it with simulation results. The DC source of 400 V, a resistive load of 50 Ω, reference signals of 50 Hz frequency, carrier/switching of 4.5 kHz frequency, modulation index of 1.15, boosting factor of 0.4, and Capacitor of 6600 μF with ESR of 0.011 Ω, are taken to verify the (2.28). As mentioned earlier, the derived equation is verified for the switching cycle with maximum active duration.

Analytical results:

By taking the above-mentioned parameters and putting in (2.28), we get $\Delta V_{c(\max)}$ = 0.107 V.

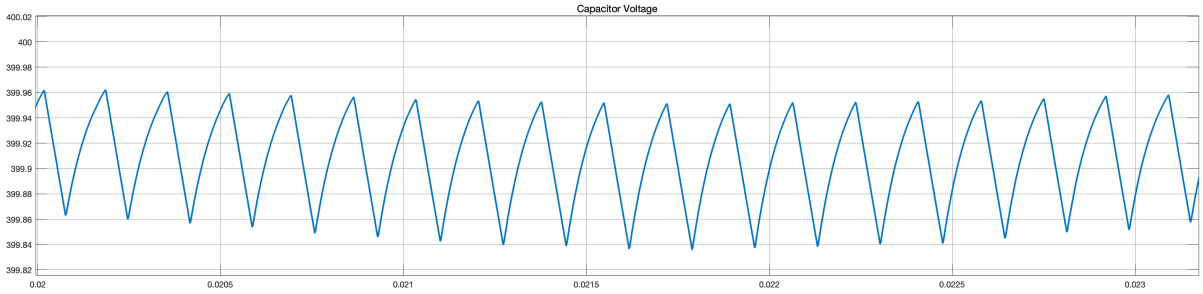

Figure 2.12: Results for verification of the derived equations for capacitor voltage drop

Simulation results:

Analysing the results presented in Figure 2.12, we get $\Delta V_{c(\max)}$ = 0.112 V

It can be observed from the difference between the results of the analytically calculated value of change in capacitor voltage and calculated from the simulation results is very less.

2.4 FUNDAMENTAL COMPONENT OF LINE VOLTAGE

2.4.1 Analytical Derivation

With the change in boosting duration (b), there is a change in the fundamental component of the output waveform accordingly. To find out the fundamental component, an average value of the PWM for each switching step should be calculated.

The average value of output for the switching cycle with maximum active duration is equal to the peak of the fundamental frequency of the output waveform [14], thereupon, the amplitude of the fundamental harmonic for line voltage V_{ab} can be calculated as follows:

$$|V_{ab(1)}| = \frac{V_{dc}\left(T_{nb(\max)}\right) + 2V_{dc}\left(t_{dis(\max)}\right)}{T_s} \quad (2.30)$$

Where, V_{dc} is DC source voltage and $\left(T_{nb(\max)}\right)$ is active state (max.) time with $V_{ao} = V_{dc}$.

$$T_{nb(\max)} = T_{active(\max)} - t_{dis(\max)} \quad (2.31)$$

$$T_{active(\max)} = (Ref_A - Ref_B)_{\max} * \frac{T_s}{A_{cr}} \quad (2.32)$$

Where A_{cr} is carrier amplitude.

From (2.31) and (2.32), we will get

$$T_{nb(\max)} = \frac{\sqrt{3}M}{4f_s}\left[Cos\left(\frac{2\pi}{m_f} + 1\right)\right](1-b) \quad (2.33)$$

where $m_f = \frac{f_s}{f_r}$

Putting value of $T_{nb(\max)}$ in (2.30), we get

$$|V_{ab(1)}| = \frac{\sqrt{3}MV_{dc}}{4}\left[cos\left(\frac{2\pi}{m_f} + 1\right)\right](1-b) \quad (2.34)$$

2.4.2 Verification Of Derived Equation From Simulation Results

The derived equation is verified by comparing it with FFT analysis in SIMULINK. The DC source of 200 V, reference signals of 50 Hz frequency, carrier signal of 4.5 kHz frequency, modulation index of 1.15, and boosting factor of 0.8, are taken to verify the (2.34)

Analytical results: By taking the above-mentioned parameters and putting in (2.34), we get $|V_{ab(1)}|$ = 348.5 V.

Simulation results: Analysing the results presented in Figure 2.13, we get $|V_{ab(1)}|$ = 348.1 V

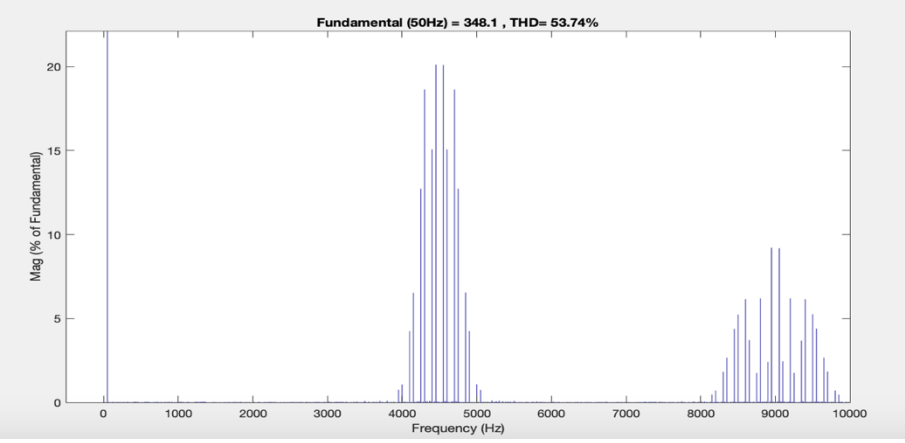

Figure 2.13: FFT results to verify the analytical derivation of fundamental component

Chapter 3

PROPOSED VOLTAGE BOOSTING VSI WITH TWO SCUs

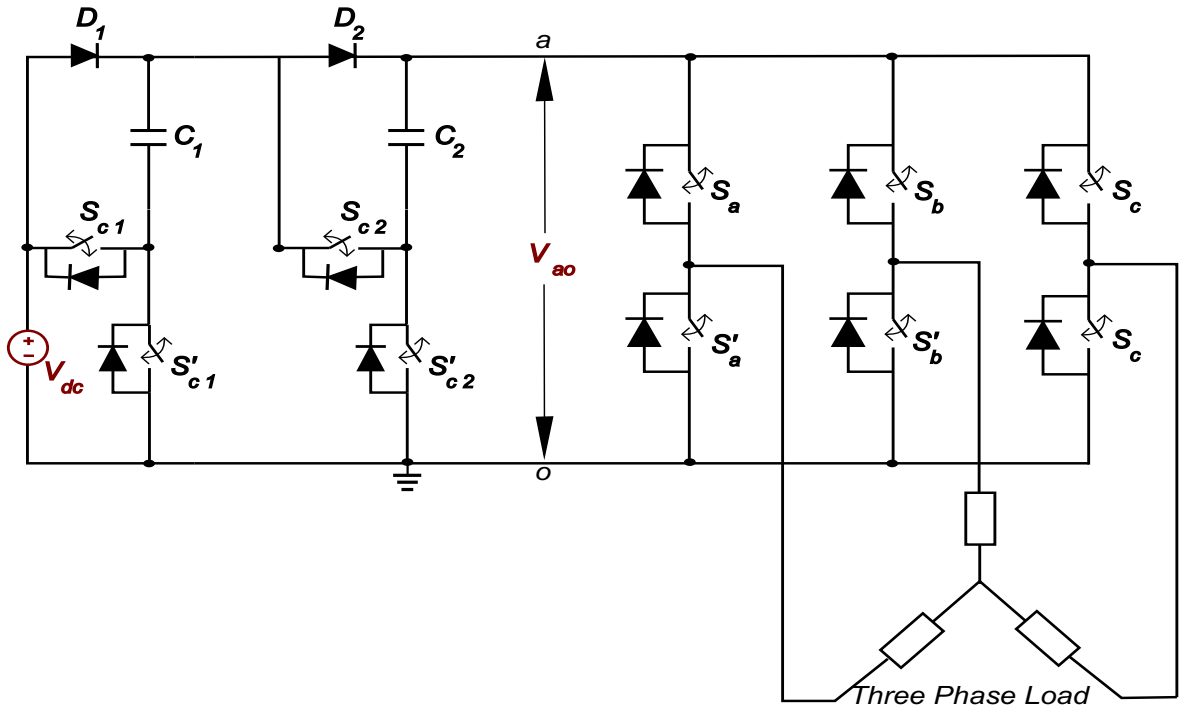

Figure 3.1: Proposed boost 3-phase VSI with 2 SCUs at front end

As discussed in chapter 2, n number of SCUs can be used at the front end of the conventional three-phase bridge VSI for voltage boosting. In this chapter, the working of the VSI with two SCUs at the front end as presented in Figure 3.1 will be discussed. With two SCUs, the peak line-line voltage obtained at the output will be equal to the thrice of the source voltage.

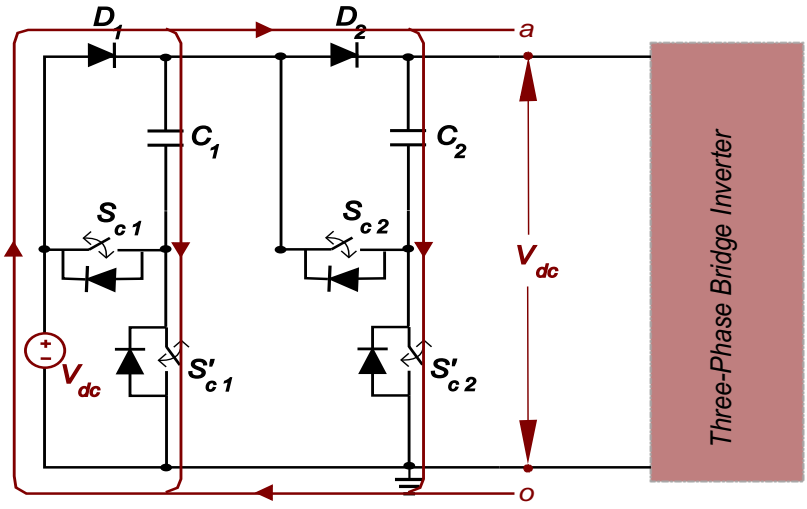

Figure 3.2: Mode of operation I ($V_{ao} = V_{dc}$)

3.1 MODES OF OPERATION

Depending on the modulation scheme, three different voltage levels that is V_{dc}, $2V_{dc}$ and $3V_{dc}$, can be obtained at the virtual link *ao*. These modes of operation are discussed as follows:

3.1.1 Mode of operation-I ($V_{ao} = V_{dc}$)

During this mode, the voltage at link *ao* is equal to the source voltage. Switches S'_{c1} and S'_{c2} are turned on keeping both SCUs in charging mode. Both the capacitor C_1 and C_2 get charged to the voltage equals to the V_{dc}. This mode of operation is shown in Figure 3.2

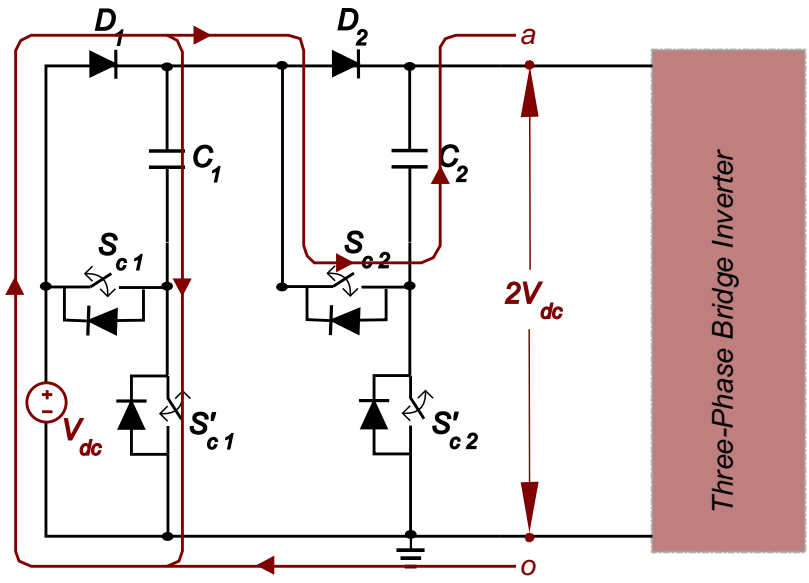

Figure 3.3: Mode of operation II ($V_{ao} = 2V_{dc}$)

3.1.2 Mode of operation-II ($V_{ao} = 2V_{dc}$)

Switches S'_{c1} and S_{c2} are turned-on during this mode of operation as shown in Figure 3.3. SCU-1 is in charging mode as capacitor and source are in parallel, which results in charging of the capacitor equals to source voltage V_{dc}. SCU-2 is in series with the source and the load, thereupon, capacitor C_2 gets discharged. The voltage obtained at link *ao* is equal to twice the source voltage.

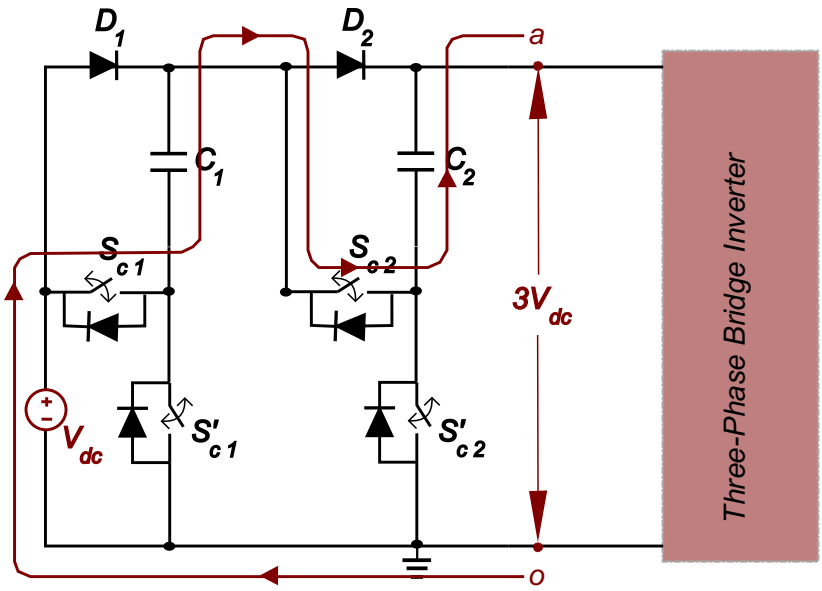

Figure 3.4: Mode of operation III ($V_{ao} = 3V_{dc}$)

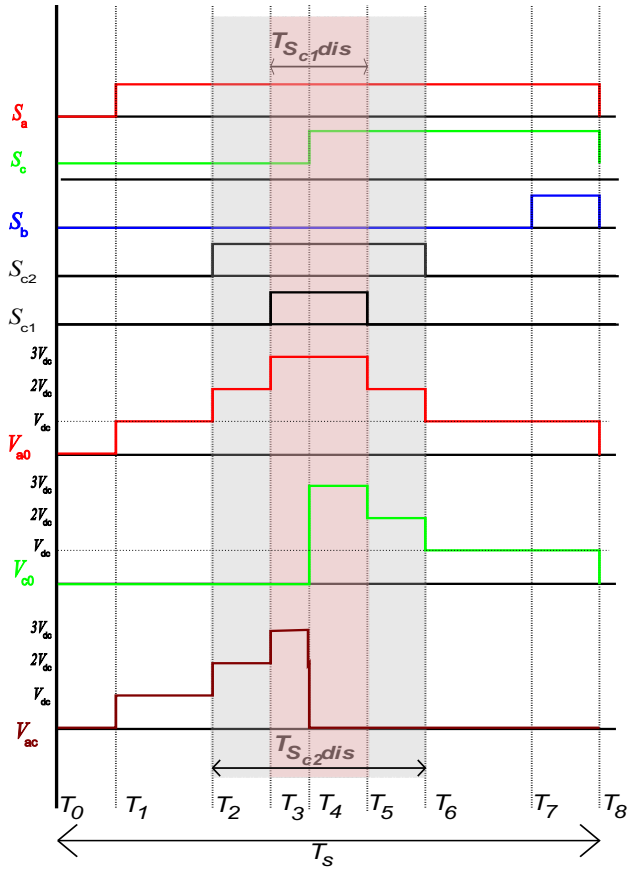

Figure 3.5: Switching signals for one cycle of carrier frequency

3.1.3 Mode of operation-III ($V_{ao} = 3V_{dc}$)

In this mode of operation, both the SCUs are in series with the source and the load, thereby, discharging both the switched-capacitors as shown in Figure 3.4. Therefore, the voltage level obtained at the link *ao* is equal to the thrice of the source voltage.

3.1.4 Voltage Equations

Switches S_a & S'_a, S_b & S'_b, S_c & S'_c, S_{c1} & S'_{c1} and S_{c2} & S'_{c2} are complementary in nature. Therefore voltage equations for the given converter can be written in the terms of switching signals of these switches as follows:

Pole Voltages:

$$V_{Ao} = (1 - A'_a)[1 + (1 - A'_{c2}) + (1 - A'_{c1})]V_{dc} \quad (3.1)$$

$$V_{Bo} = (1 - A'_b)[1 + (1 - A'_{c2}) + (1 - A'_{c1})]V_{dc} \quad (3.2)$$

$$V_{Co} = (1 - A'_c)[1 + (1 - A'_{c2}) + (1 - A'_{c1})]V_{dc} \quad (3.3)$$

Line Voltages:

$$V_{AB} = (A'_b - A'_a)[1 + (1 - A'_{c2}) + (1 - A'_{c1})]V_{dc} \quad (3.4)$$

$$V_{BC} = (A'_c - A'_b)[1 + (1 - A'_{c2}) + (1 - A'_{c1})]V_{dc} \quad (3.5)$$

$$V_{CA} = (A'_a - A'_c)[1 + (1 - A'_{c2}) + (1 - A'_{c1})]V_{dc} \quad (3.6)$$

where A_i is the switching function of the i^{th} switch and can be defined as:

$$A_i = \begin{cases} 1 \text{ if switch } i \text{ is On} \\ 0 \text{ if switch } i \text{ is Off} \end{cases}$$

3.2 MODULATION SCHEME

The modulation scheme with respect to the presented topology for a single switching cycle is shown in Figure 3.5. It can be observed that switch S_{c2} is turned on from $t = T_1$ to $t = T_2$ for fraction of the total active state and switch S_{c1} is turned on from $t = T_3$ to $t = T_5$ fraction of S_{c2} turn-on period. This fraction is named as boosting constant *b.* The obtained pole vole voltages are of three levels resulting in three-level line-line voltage at the output. To modulate the switches of SCU-1, another pair of the reference signals is needed as shown in Figure 3.6.

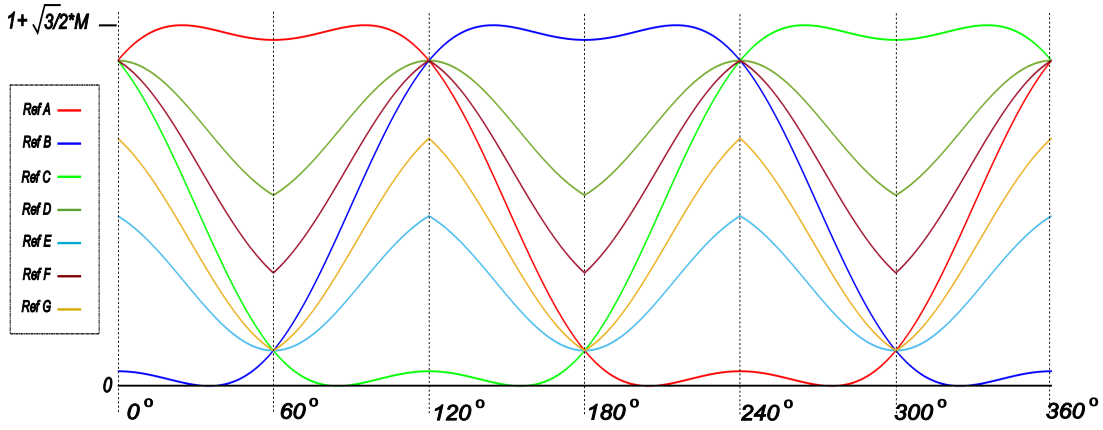

Figure 3.6: Reference signals for modulation of the proposed structure

3.2.1 Reference Signals Generation

To generate the switching signals for S_{c1} and S'_{c1}, new reference signals are required. It has already been discussed earlier that to generate the new signals, we need equations for every sixty degrees separately. The reference generation for the proposed operation with two SCUs at the front end is presented in Table 3.1

Table 3.1: Segment-wise generation of the reference signals

Segment	$Reference_F$	$Reference_G$
1	$Ref_A * (b^2) + Ref_C * (1 - b^2)$	$Ref_C * (1 - b^2) + Ref_B * (b^2)$
2	$Ref_A * (b^2) + Ref_B * (1 - b^2)$	$Ref_B * (1 - b^2) + Ref_C * (b^2)$
3	$Ref_B * (b^2) + Ref_A * (1 - b^2)$	$Ref_A * (1 - b^2) + Ref_C * (b^2)$
4	$Ref_B * (b^2) + Ref_C * (1 - b^2)$	$Ref_C * (1 - b^2) + Ref_A * (b^2)$
5	$Ref_C * (b^2) + Ref_B * (1 - b^2)$	$Ref_B * (1 - b^2) + Ref_A * (b^2)$
6	$Ref_C * (b^2) + Ref_A * (1 - b^2)$	$Ref_A * (1 - b^2) + Ref_B * (b^2)$

Chapter 4
SIMULATION RESULTS

4.1 BOOSTING WITH A SINGLE SCU

To validate the proposed work, simulation of switched-capacitor VSI with proposed modulation is done using MATLAB/SIMULINK. The simulation is performed for an inverter designed for 20 kVA full load with 0.85 power factor. The parameters used for the Simulink model are listed in Table 4.1. Simulation is done for different values of boosting factor (*b*). Steady State results have been obtained for the line-line voltage, line-neutral voltage, line-neutral current, source current and capacitor voltage.

4.1.1. For Boosting = 0%

With boosting parameter *b* equal to zero, the inverter will work as a conventional VSI. The Peak line voltage is equal to the source voltage as shown in Figure 4.1. The phase voltage and the current is presented in Figure 4.2. The capacitor loop is in parallel with the source. Therefore, the capacitor voltage drop is negligible as can be observed in Figure 4.3. The peak source current is almost equal to the peak load current suggesting that no extra current is supplied for capacitor charging.

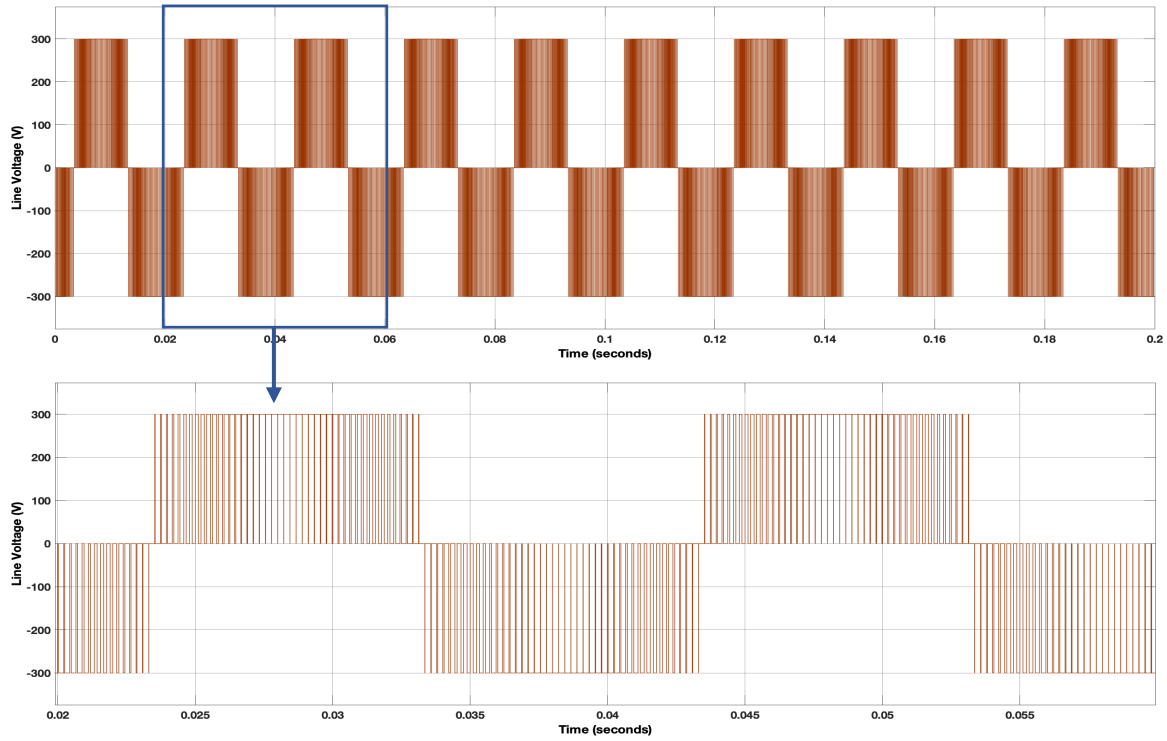

Figure 4.1: Output line-line voltage for *b* = 0

Table 4.1: Parameters Used for Simulink Model

DC Voltage Source	200 V
Capacitor	6600 µF
Load Inductor	20 mH
Load Resistance	10 Ω
Line Frequency	50 Hz
Switching Frequency	4.5 kHz
Modulation Index	1.15
ESR	0.02 Ω
Step Size	1e-06 s

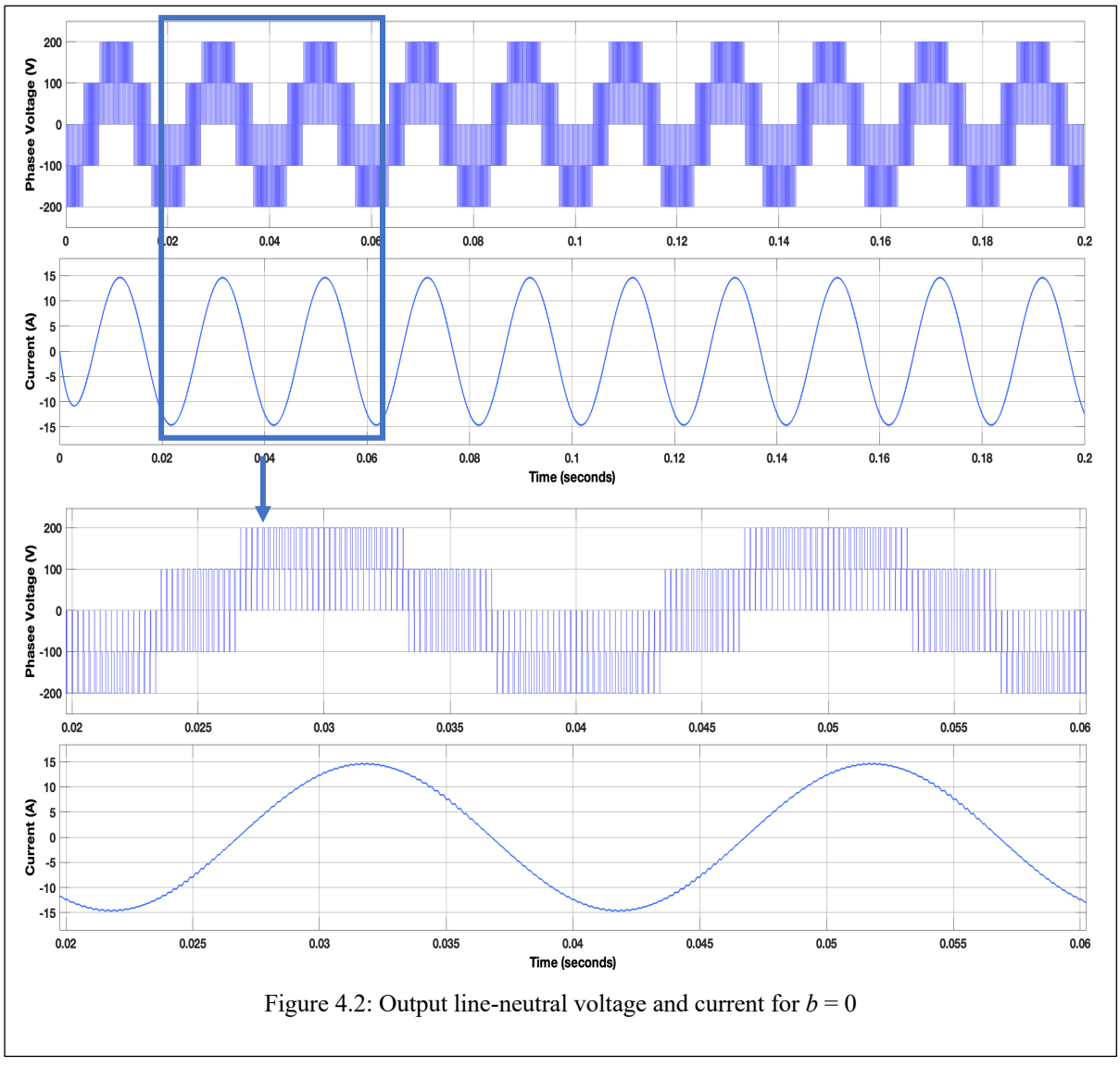

Figure 4.2: Output line-neutral voltage and current for $b = 0$

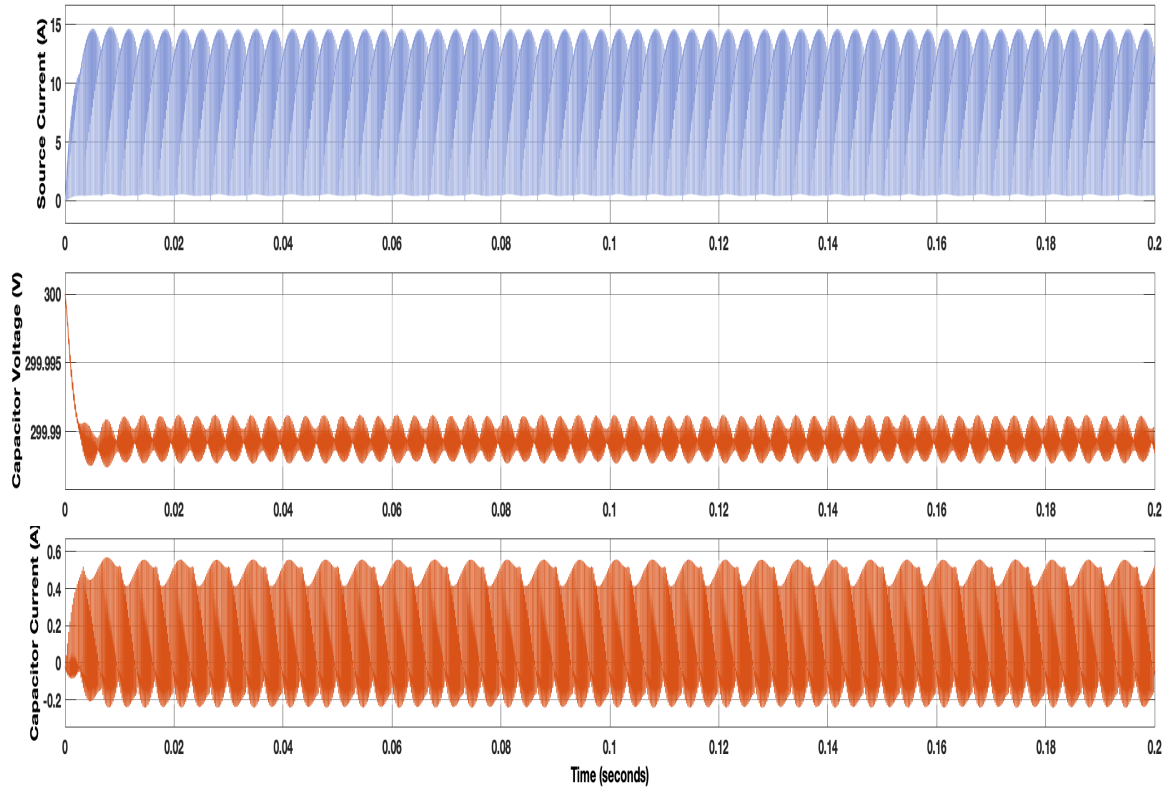

Figure 4.3: Source Current, capacitor voltage and capacitor current for $b = 0$

4.1.2. For Boosting = 25%

With boosting factor $b = 0.25$, we can observe from the Figure 4.4 that the peak line voltage is double the source voltage, but the step-up voltages are obtained for about 25% of the total active state duration. From Figure 4.5, it can be analysed that phase current is increased because of increased fundamental phase voltage. Nonetheless, discharging time of the capacitor is still less, ergo, a little drop in capacitor voltage. The charging current is less than the twice load current as shown Figure 4.6

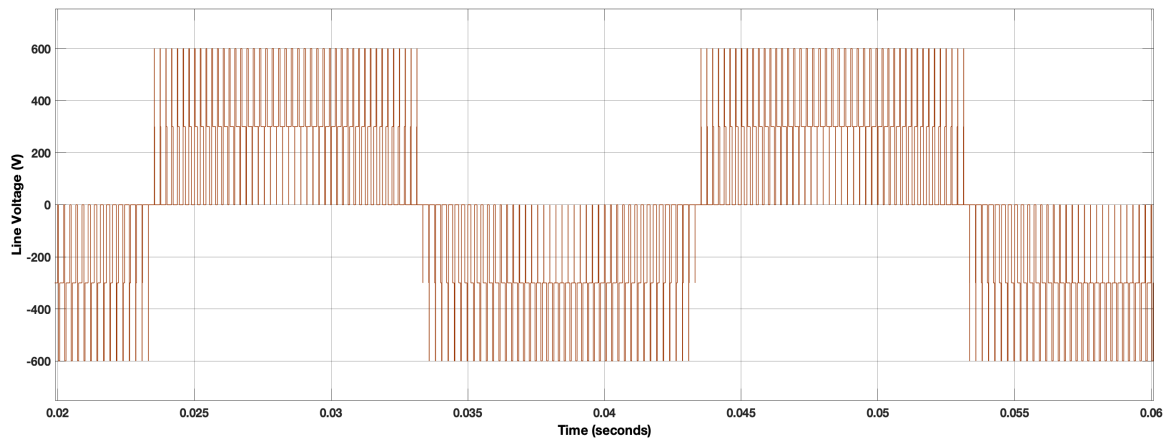

Figure 4.4: Line-line voltage for $b = 0.25$

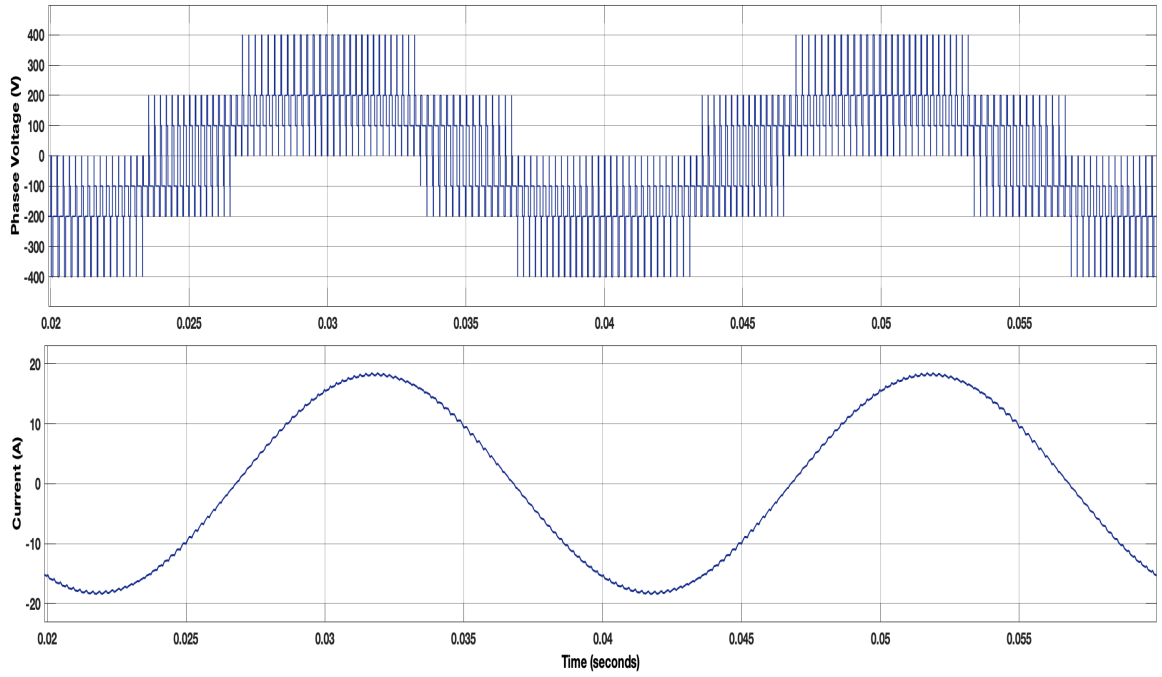

Figure 4.5: Line-neutral voltage and current for $b = 0.25$

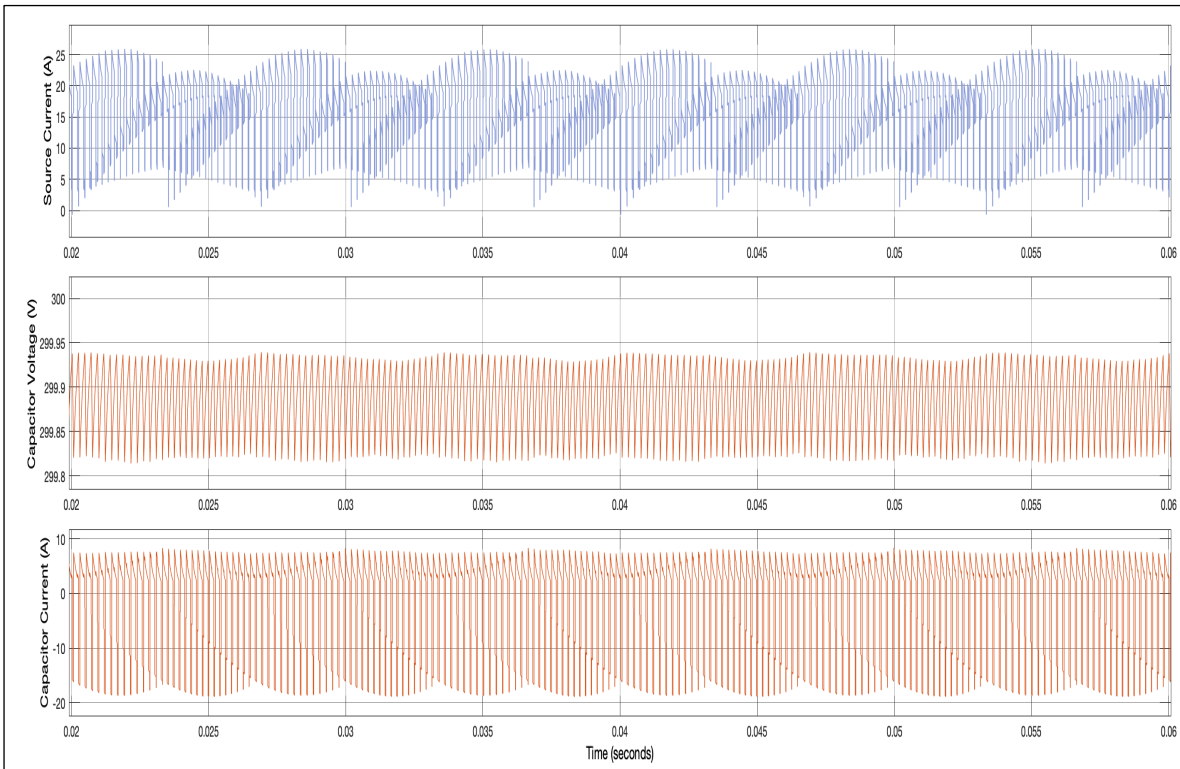

Figure 4.6: Source current, capacitor voltage and capacitor current for $b = 0.25$

4.1.3. For Boosting = 50%

For boosting factor $b = 0.5$, the line-line voltage is shown in Figure 4.7. Now with the increase in the fundamental component of output voltage, the peak current delivered to the load has also increased as shown in Figure 4.8. Hence, more current is demanded from the source to charge the capacitor as can be observed in Figure 4.9. However, the source current peaks are still around twice the maximum load current, which can be considered within limit for low current applications.

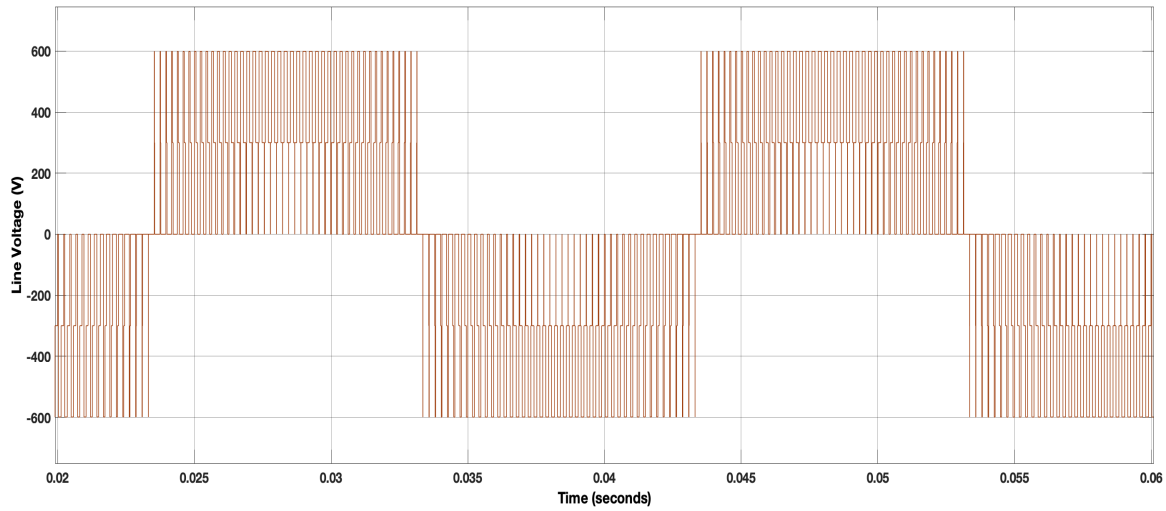

Figure 4.7: Line-line voltage for $b = 0.5$

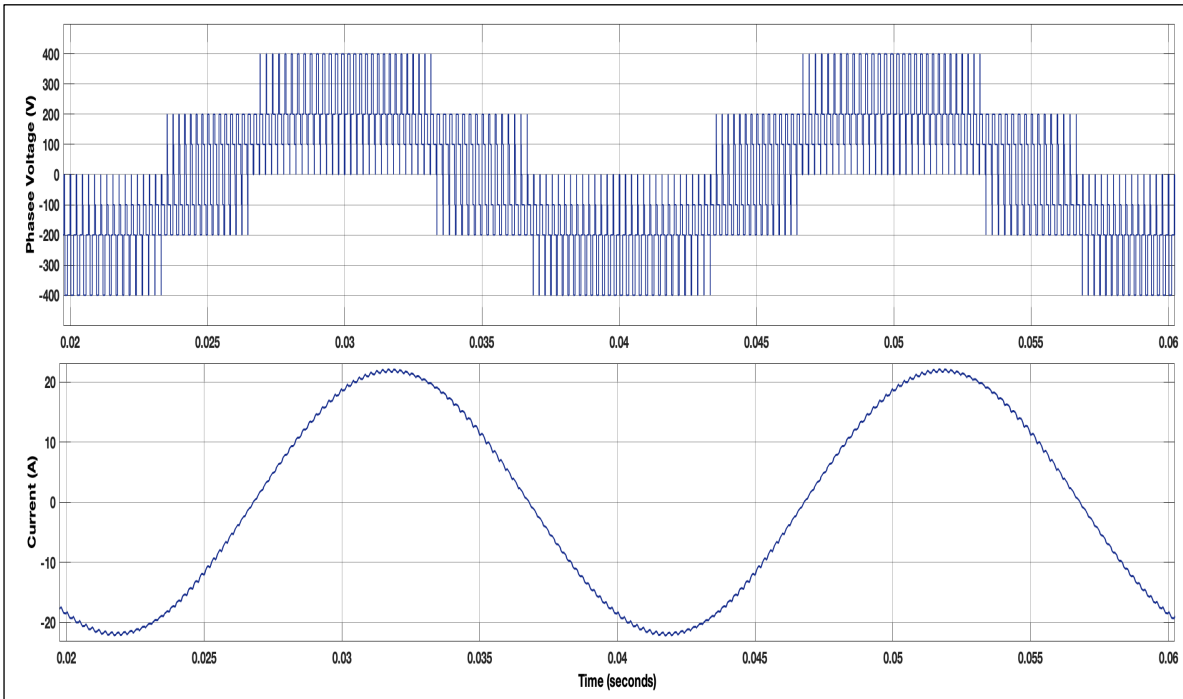

Figure 4.8: Output line-neutral voltage and current for $b = 0.5$

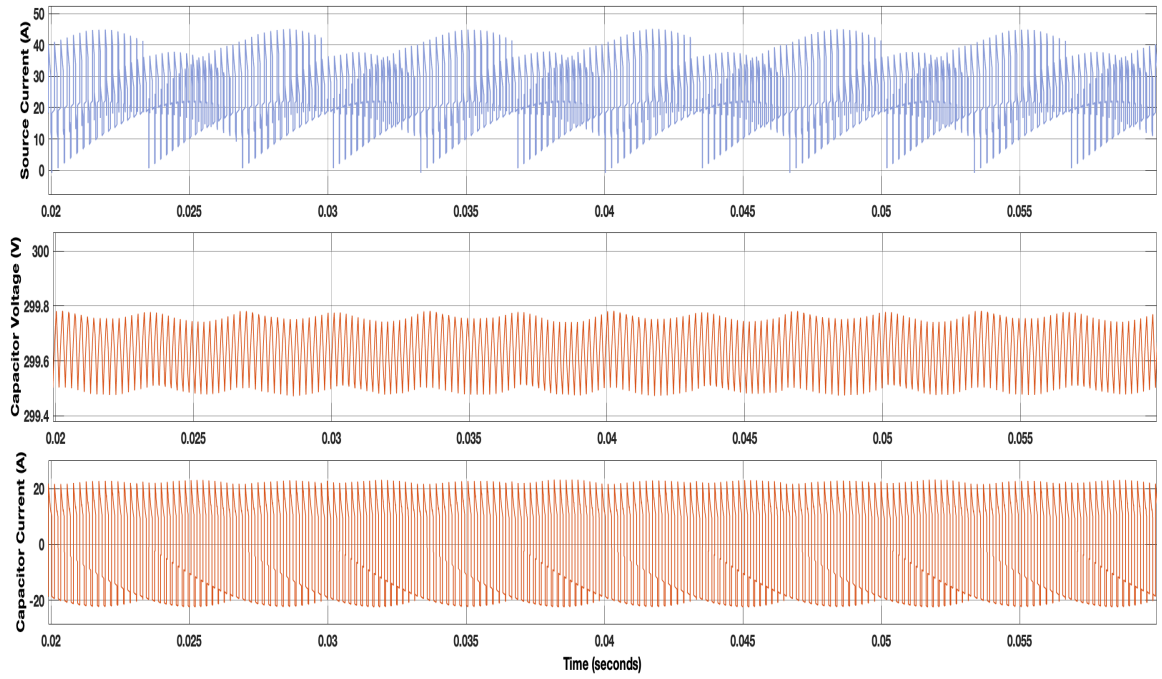

Figure 4.9: Source current, capacitor voltage and capacitor current for $b = 0.50$`

4.1.4. For Boosting = 100%

This is basically the simulation of the type-I modulation, where SC discharges for the complete active state time period in a single switching cycle. The results are presented in Figure 4.10 to Figure 4.12. It can be observed that the intermediate levels in output waveforms and line-line voltages are purely three-level. The fundamental component of the output is increased resulting in a higher load current. The voltage drop across the capacitor is significant, hence the source current peaks as shown in Figure 4.12 are very high as compared to the load current.

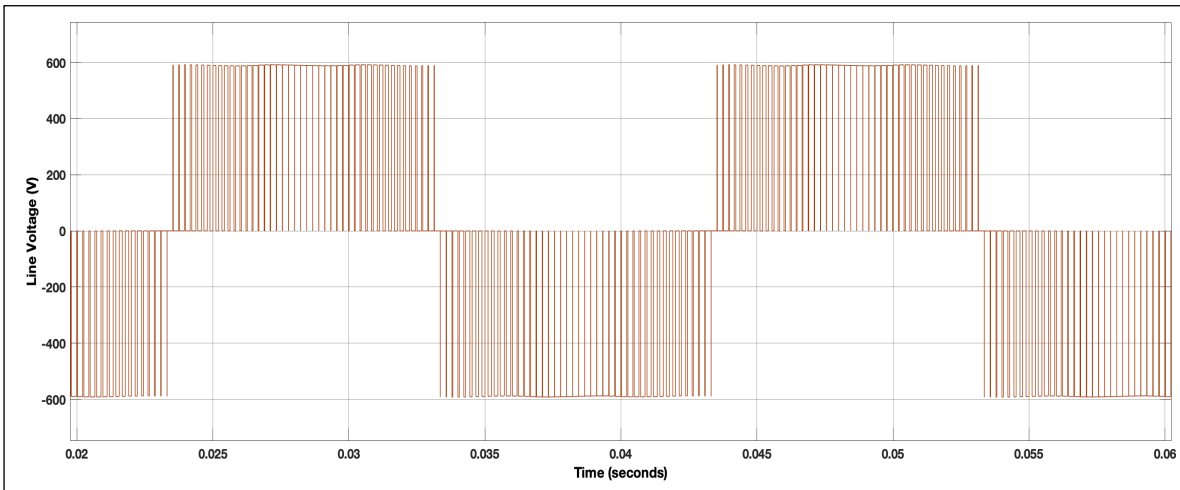

Figure 4.10: Output line-line voltage for $b = 1$

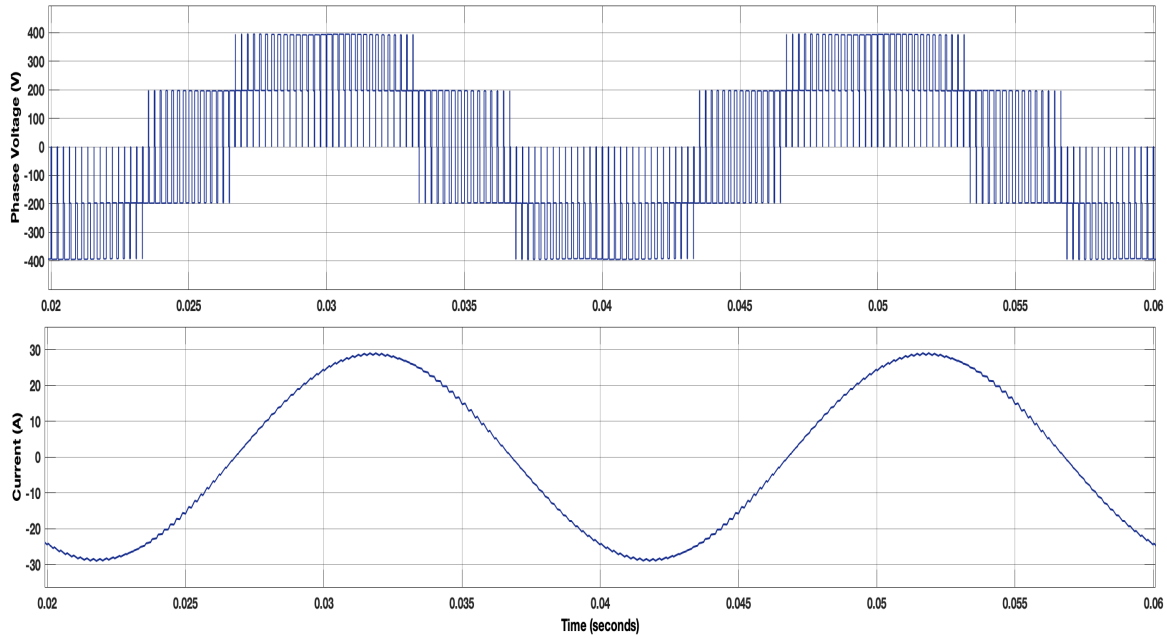

Figure 4.11: Output line-neutral voltage and current for $b = 1$

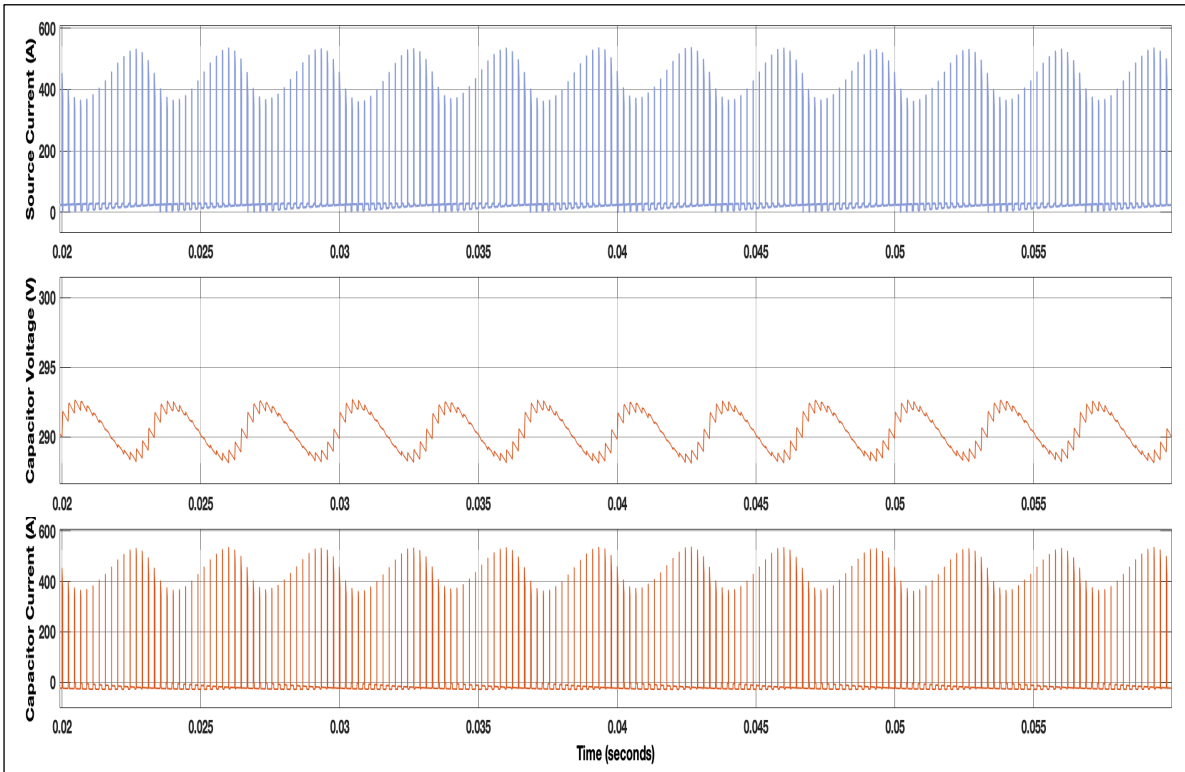

Figure 4.12: Source current, capacitor voltage and capacitor current for $b = 1$

4.2 BOOSTING WITH TWO SCUs

To obtain the results for three-phase bridge VSI with two switched capacitor units at the front end, the same parameters as shown in Table 4.1 are used except for the DC source voltage, which is now taken as V_{dc} = 200 V. The obtained peak line-line voltage is now 600 V that is thrice the source voltage. The results are taken for boosting factor b equals 0.25 and 0.50.

4.2.1. For Boosting = 25%

For boosting factor b = 0.25, results are shown in the Figures 4.13 to Figures 4.15. The peak line-line voltage is thrice the source voltage as presented in Figure 4.13, but voltage boost is obtained for less duration. The phase voltage and current can be observed from Figure 4.14. As the discharging time and current are less, the voltage drop across the capacitors will be very less as shown in Figure 4.15.

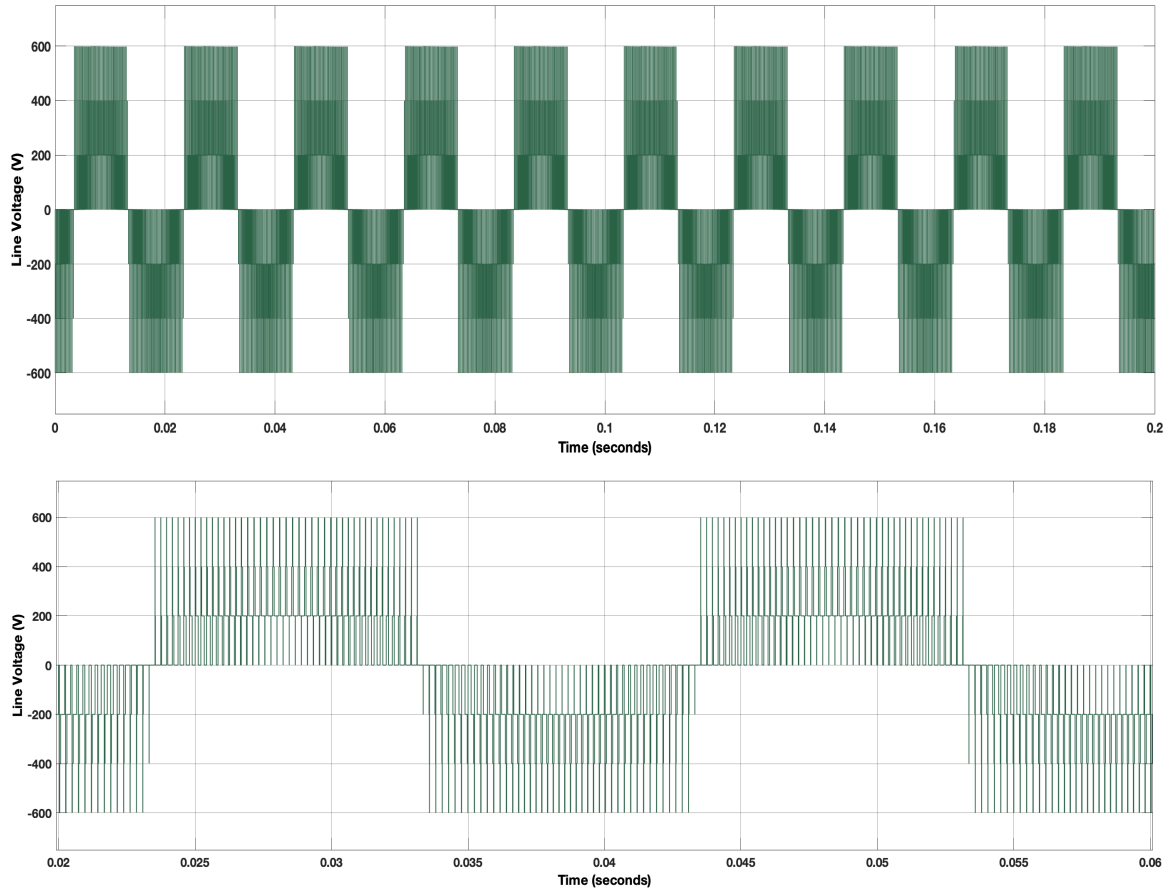

Figure 4.13: Output line-line Voltage for b = 0.25

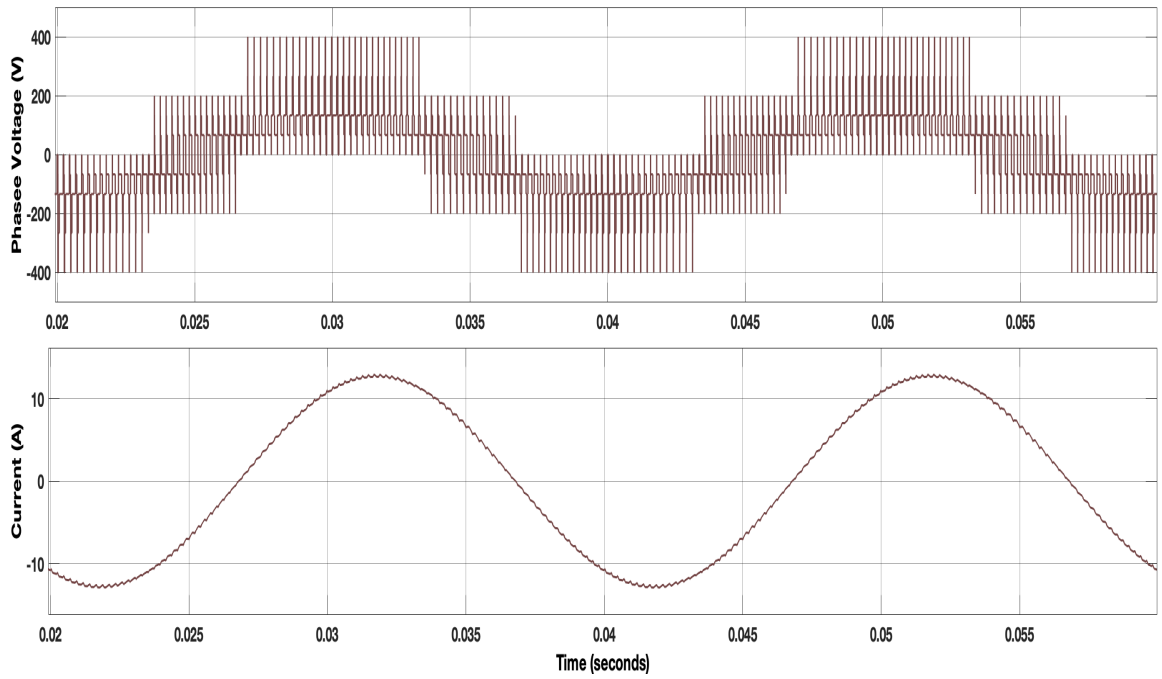

Figure 4.14: Output line-neutral phase voltage and current for b = 0.25

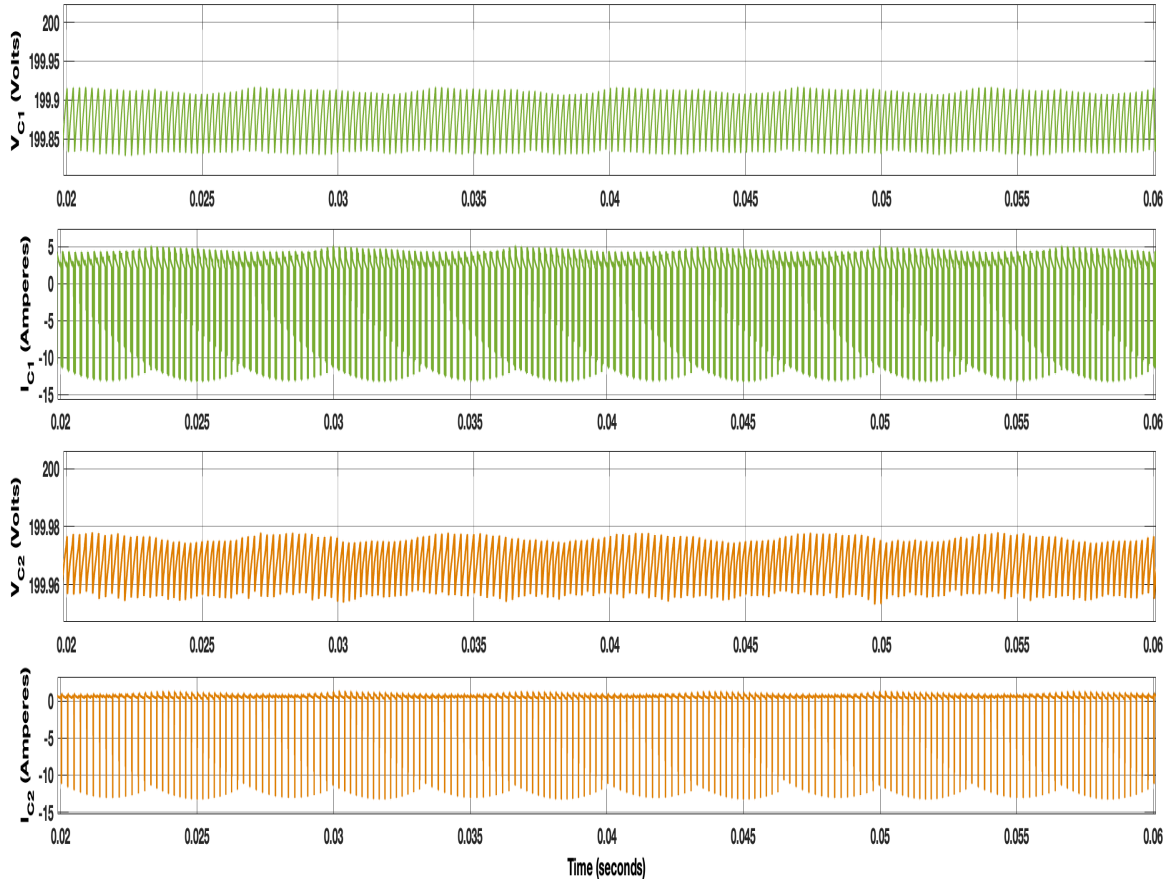

Figure 4.15: Voltage and current across capacitor 1 and capacitor 2 for b = 0.25

4.2.2. For Boosting = 50%

For boosting factor b = 0.5, The line-line voltage can be observed from Figure 4.16. The capacitor C_2 will get discharged for 50% duration of the active state period, and capacitor C_1 will get discharged for 50% duration of capacitor C_2 discharging time. The phase voltage and the current increase due to the increased duration of the boosting as shown in Figure 4.17. As the discharging current and time of the capacitor increase, the voltage drop across the capacitors increases significantly compared to 25% boosting as shown in Figure 4.18.

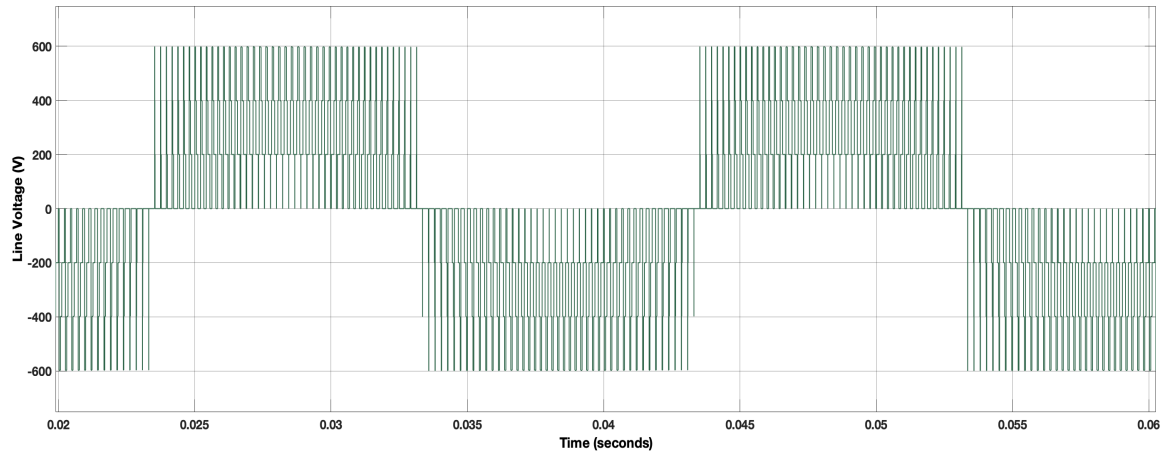

Figure 4.16: Output line-line voltage for b = 0.5

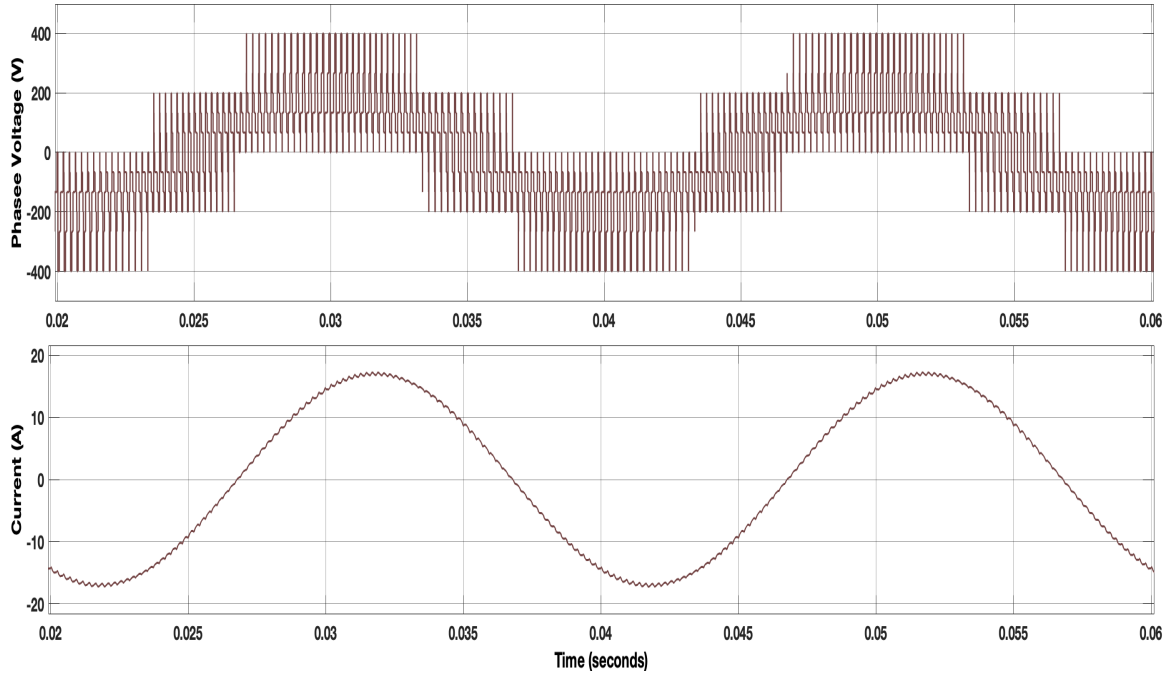

Figure 4.17: Output phase voltage and current for b = 0.5

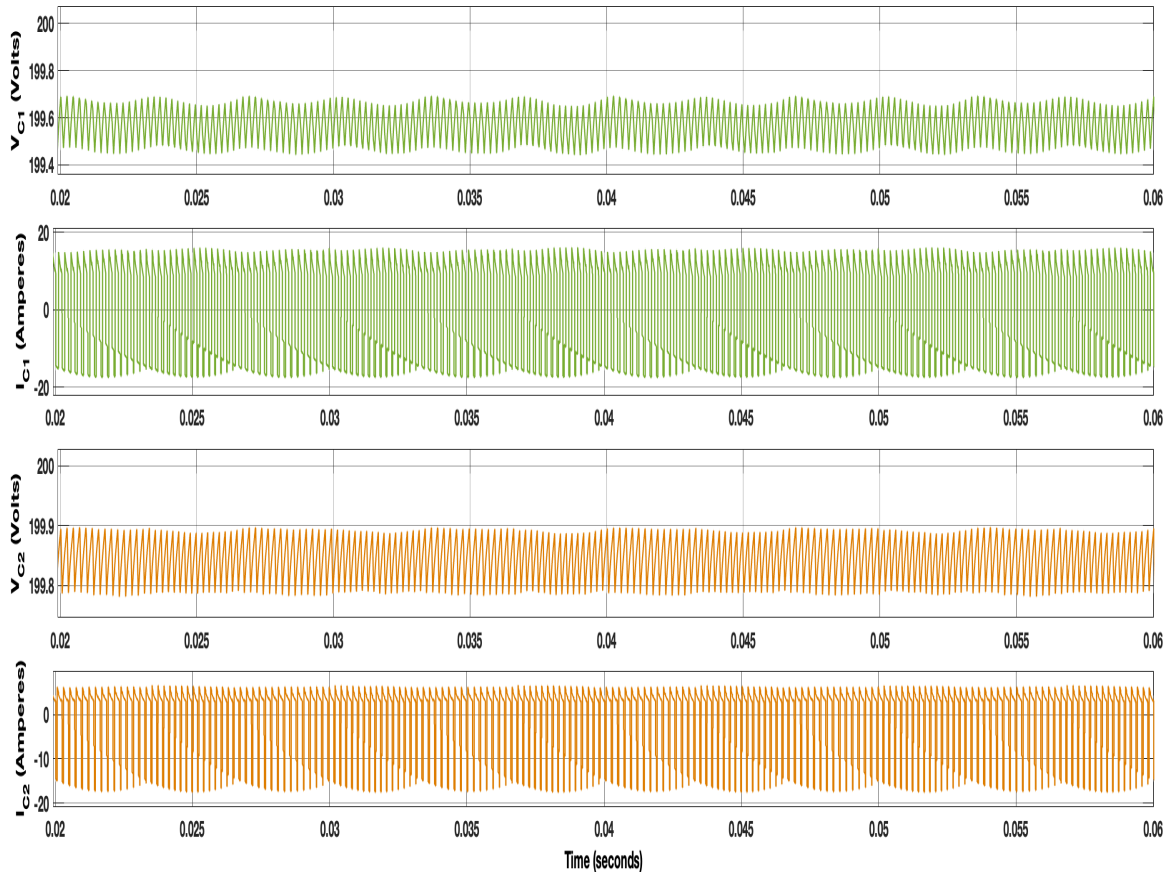

Figure 4.18: Voltage and current across capacitor 1 and capacitor 2 for $b = 0.5$

Chapter 5

EXPERIMENTAL RESULTS

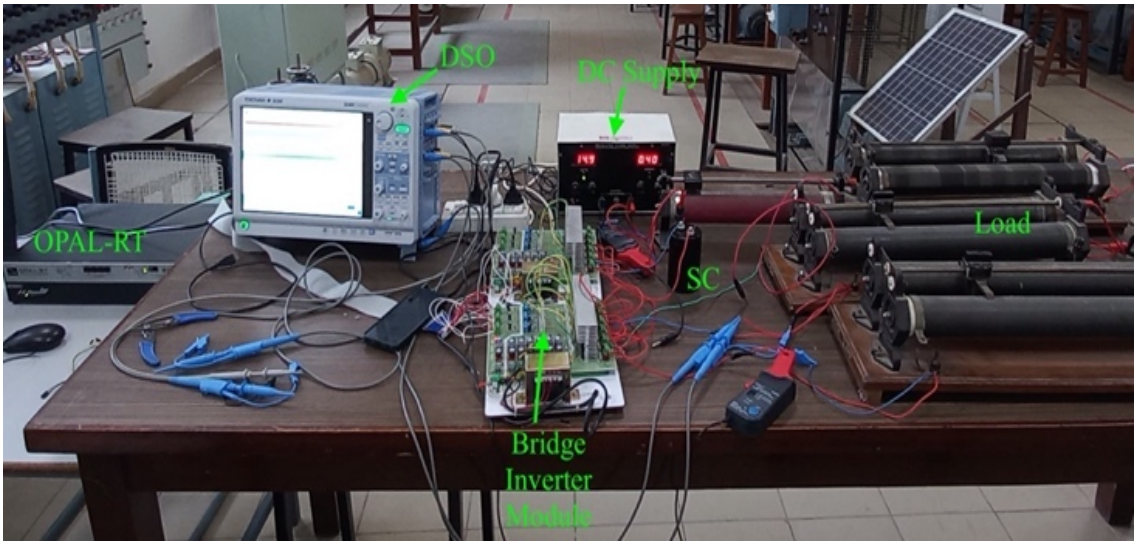

Figure 5.1: Experimental setup with a single SCU at the front end of conventional 3-phase bridge inverter

To validate the proposed work, results are obtained from the experimental setup shown in Figure 5.1. A switched capacitor unit is introduced at the front end of the conventional three-phase bridge circuit. The gate pulses are obtained from OPAL-RT 4510 through a digital I/O board. A 30V-2A regulated DC power supply is used as the source. The parameters used to obtain the results are listed in Table 5.1. Results are taken for 0%, 10% and 40% boosting.

5.1 FOR BOOSTING = 0%

The results for 0% boosting can be analysed in Figure 5.2. As expected, the inverter is working as conventional VSI. Peak line-line voltage is equal to the source voltage. The voltage drop across the capacitor is insignificant.

Table 5.1: Parameters used for experimental setup

DC Voltage Source	15 V
Capacitor	2200 µF
Load Resistance	36 Ω
Line Frequency	50 Hz
Switching Frequency	3 kHz
Modulation Index	1.15
Step Size	1e-05 s

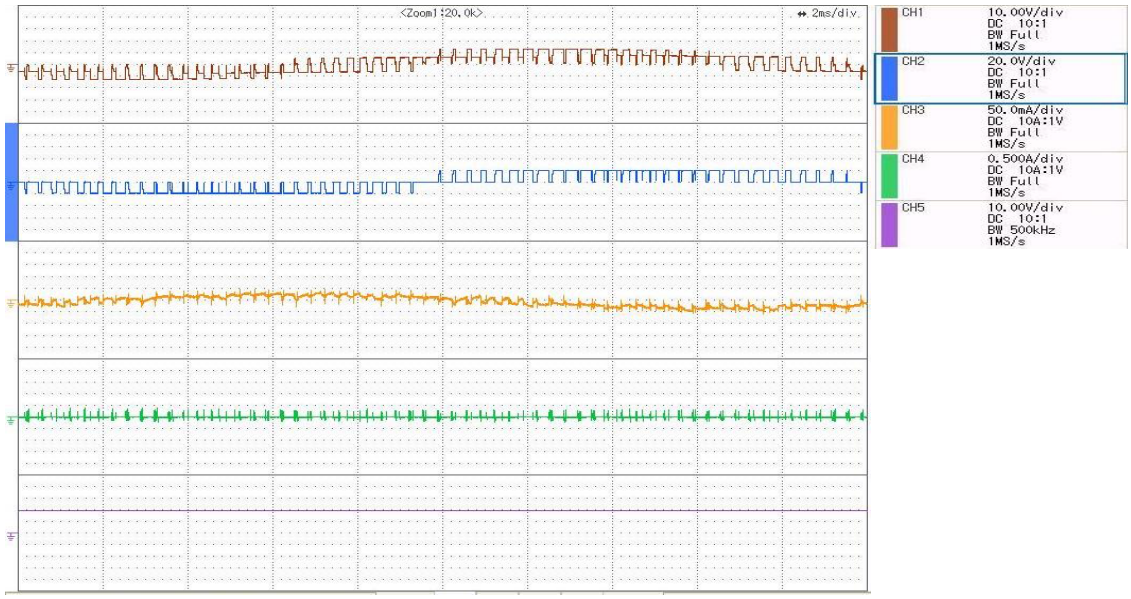

Figure 5.2: Line-neutral voltage, line-line voltage, load current, source current and capacitor voltage (Top to bottom) for boosting factor of 0.

5.2 FOR BOOSTING = 20%

In Figure 5.3 results for 20% boosting can be analysed. The waveforms are imitating the expected results. Boosting in the line-line voltage is occurring for a small duration and the current required from the source is within limits.

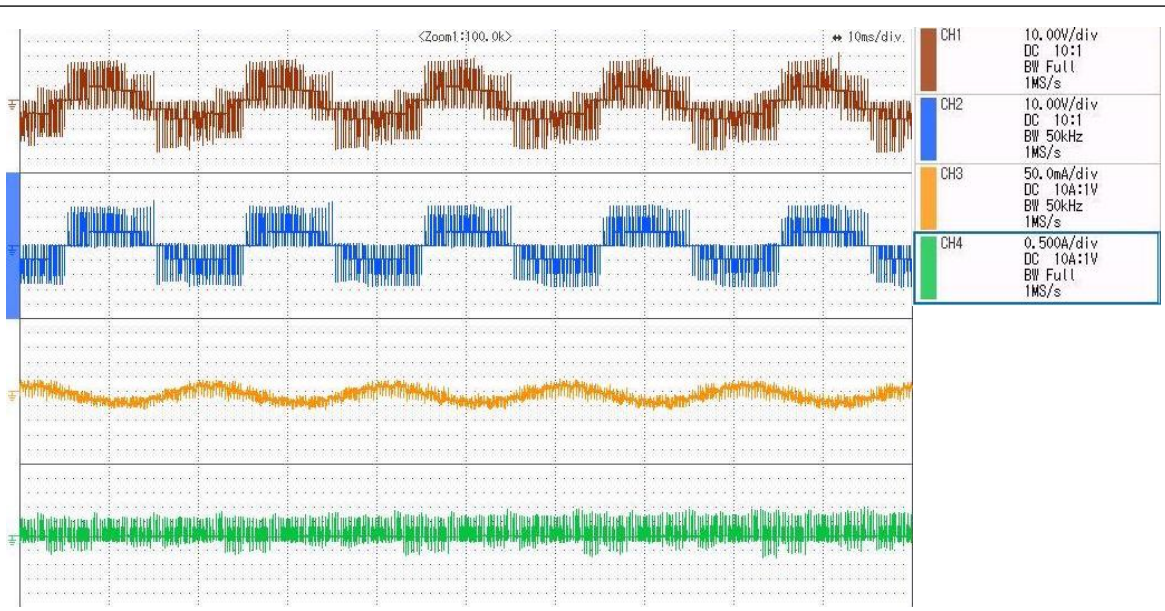

Figure 5.3: Line-neutral voltage, line-line voltage, load current and source current (Top to bottom) for boosting factor of 20%

5.3 FOR BOOSTING = 40%

The results for 40% boosting can be observed in Figure 5.4. Peak line-line voltage is 30V, which is twice the supply voltage. From the zoom-in view presented, the duration of boosting state can be analysed. It is about 40% of the total active state period in one switching cycle. The source current is within the limits.

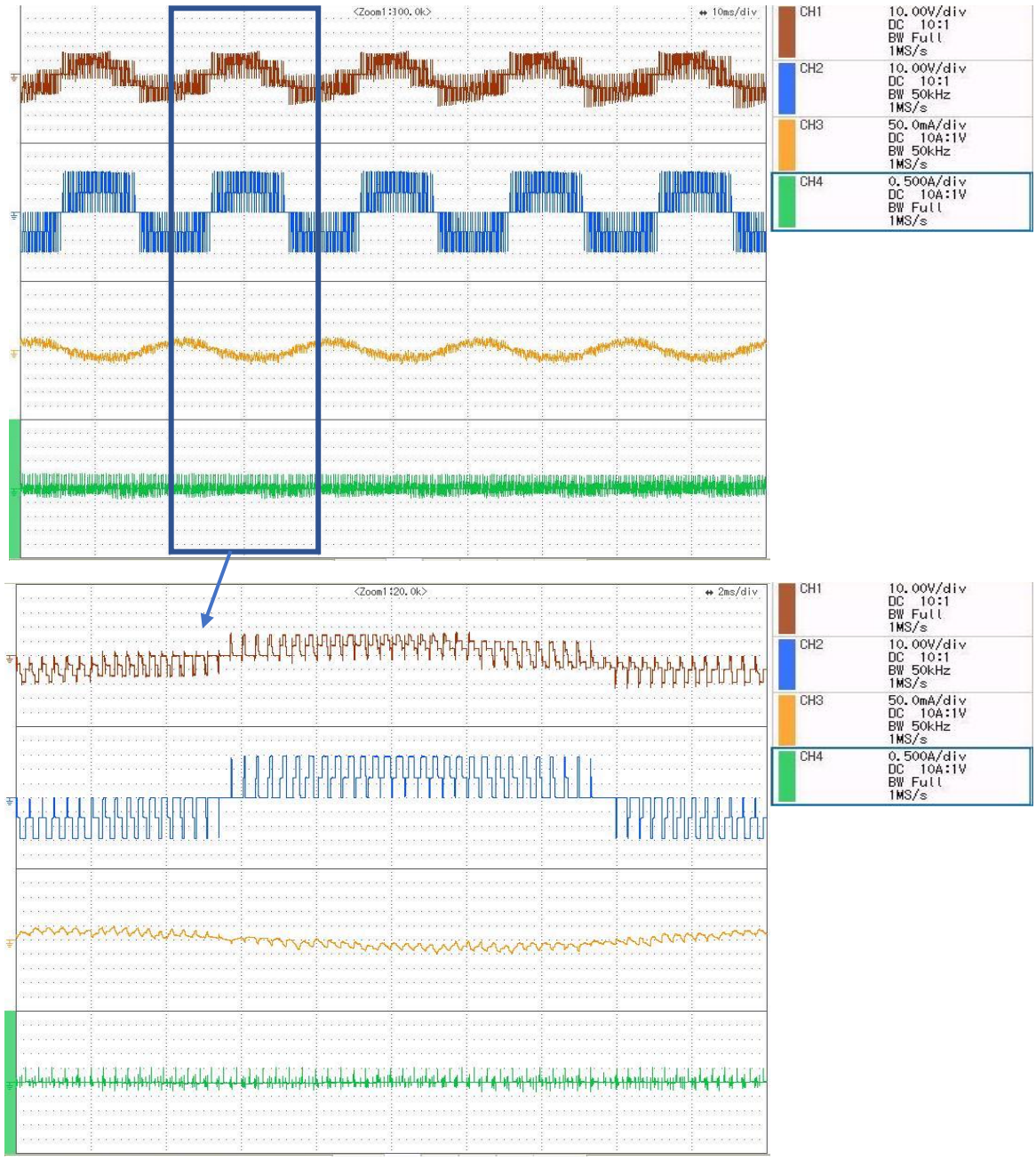

Figure 5.4: Line-neutral voltage, line-line voltage, load current and source current (Top to bottom) for boosting factor of 40%

Chapter 6
CONCLUSIONS AND FUTURE SCOPE

6.1 CONCLUSIONS

This study presents an SC-based three-phase VSI that can boost the voltage in all three legs with switched capacitor units at front end. The topology has been realized with one switched capacitor unit and two switched capacitor units. Modified SPWM (third harmonic injected) is used for the modulation of inverter, which increases the source utilization and linear operating range. The value of the switched-capacitor is designed for the proposed structure. The equation for fundamental of the output PWM line-line voltage is also presented. The Simulation/Experimentation is performed to validate the proposed structure and the modulation

The following conclusions are drawn from the study :

- The voltage boosting is provided by the single structure to all the legs of an inverter, thereby, employing the lesser number capacitors and switches as compared to other topologies.
- Boosting ratio is manipulated by changing the boosting factor without varying the modulation amplitude of original three-phase references. The voltage drop across the capacitor is maneuvered by controlling the boosting factor through fractional boosting. Thereby, the charging current in the capacitor loop is controlled for limited boosting requirements. It leads to reduction in the system size.
- The proposed topology and modulation scheme are validated through Simulation/Experimentation. Strong agreement is resulted between simulated and experimental results for passive load.
- As the presented system is yielding controllable voltage boosting, it can be used for various application such as traction inverters, photovoltaic applications.

6.2 SCOPE FOR FUTURE WORK

At the end of study, some areas has been identified where further engagement is needed for the improvement. These areas for further works are summarized as follows:

- The PIV across the switches is same as the highest boosting level required from the system. There is scope to reduce it by conceptualizing the multilevel output waveform for the proposed structure.
- The charging current is still large for the higher boosting factor. There is a scope to design and introduce a small inductor in charging loop to limit such high charging current.
- The effectiveness of the presented fractional boosting technique can be validated with other multilevel inverter topologies.

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PLAGIARISM REPORT

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