High Precision low-voltage WTA/LTA circuit and its applications

A dissertation submitted in partial fulfilment of the required for the award of degree of

MASTER OF TECHNOLOGY

In

VLSI Design

Submitted By

SAHIB SINGH

Roll No. 601361022

Under the supervision of

Dr. RISHIKESH PANDEY
Assistant Professor, ECED

Department of Electronics and Communication Engineering

THAPAR UNIVERSITY

(Established under the section 3 of UGC Act, 1956)

PATIALA – 147004 (PUNJAB)

DECLARATION

I hereby declare that the work, which is being presented in the dissertation, entitled "High Precision Low-voltage WTA/LTA circuit and its application" in partial fulfilment of the requirements for the award of degree of Master of Technology in VLSI Design submitted in of Electronics and Communication Engineering Department of Thapar University, Patiala, is an authentic record of my own work carried out under the guidance of Dr. Rishikesh Pandey, Assistant Professor, ECED and refers other researcher's which are duly listed in the reference section.

The matter presented in this dissertation has not been submitted in any other University/Institute for award of degree.

Date: 15/7/15

Sahib Singh

Roll No. 601361022

It is certified that the above statement made by the student is correct to the best of my knowledge and belief.

15/7/2015

Dr. Rishikesh Pandey
Assistant Professor, ECED,
Thapar University,

Countersigned by :

Dr Sanjay Sharma
Head of ECED,
Thapar University
Patiala–147001, (Punjab)

Dr S. S. Bhatia
Dean of Academic Affairs
Thapar University
Patiala–147001, (Punjab)

ACKNOWLEDGEMENT

First of all, I would like to express my gratitude to **Dr. Rishikesh Pandey Assistant Professor**, Electronics and Communication Engineering Department, Thapar University, Patiala for his patient guidance and support throughout this thesis work. I am truly very fortunate to have the opportunity to work with him. I found his guidance to be extremely valuable.

I am also thankful to the **Head of the Department, Dr. Sanjay Sharma** as well as **Dr. Amit Kumar Kolhi, Associate professor**, **PG Coordinator of ECED** and **Dr Anil Arora Coordinator for VLSI Design**, I would also like to thank entire faculty and staff of Electronics and Communication Engineering Department and my friends who devoted their valuable time and helped me in all possible ways towards successful completion of this work. I thank all those who have contributed directly or indirectly to this work.

Lastly, I would also like to thank my parents for their years of unyielding love and encouragement. They have always wanted the best for me and I admire their determination and sacrifice.

Sahib Singh

ABSTRACT

In this thesis**,** a novel low-voltage current mode WTA/LTA circuit is proposed for which detects maximum and minimum values from the given current inputs simultaneously. The circuit is developed using cascode current mirrors and a substractor circuit. The cascode current mirror is used to improve the output swing and substractor circuit is used to compute the difference of two input currents. The proposed circuit operates at supply voltage of 1.1V with high precision. The output current is mirrored with transfer error lower than 0.035% while input current is varying from 0 to 40uA. Simulations have been performed with SPICE level 53 (TSMC) parameters in 0.18um CMOS technology. Some of the applications of the proposed WTA/LTA circuit such as half wave rectifier, full wave rectifier and modulus circuit with their simulation results have also been presented.

Maximum and Minimum functions are fundamental operations in many nonlinear systems. Most analogue maximum and minimum continuous-time CMOS implementations have been derived from ‘Winner-take-all (WTA) and Looser take all (LTA) circuits. The thesis gives a brief review of different approaches reported by various researchers in literature. Out of these, one of the maximum and minimum circuit has been designed and simulated. The simulated results have also been presented.

TABLE OF CONTENTS

LIST OF FIGURES

LIST OF TABLES

List of symbols

I_{min}	Minimum Current
I_{max}	Maximum Current
R_{in}	Total Input Impedance
g_{mi}	Transconductance of MOSFET
V_{DD}	Supply Voltage
V_{DS}	Drain to Source Voltahe Drop
V_{th}	Threshold Voltage
V_i	Voltage at Node i
r_{oi}	Output Resistance
i_x	Input Current
Vin	Input Current
W	Width of MOSFET
L	Length of MOSFET
I_D	Minimum current through first cascode current mirror
V_{OV}	Overdrive Voltage
R_{out}	Output Impedance
i.e.	That is

ABBREVIATIONS

WTA	Winners takes all
LTA	Looser takes all
CM	Current mirror
THD	Total Harmonic Distortion
HSCCM	High Swing Cascoded Current Mirror
HWR	Half Wave Rectifier
FWR	Full Wave Rectifier

CHAPTER

INTRODUCTION

1.1 Introduction

The need for high accuracy and energy efficient devices continues to derive the need of devices which consume lesser energy and work for longer hours without being charged. In areas of neural networks and artificial intelligence, the demand of very small circuits with similar characteristics are required. Along with the reduction in size of integrated circuit they use, the functionality and flexibility needs to improve. Analog circuits have provided solution with continuous changing technology sizes and smart designs to enhance their capability. One of such circuit most widely used is winner takes all (WTA)/ loser takes all (LTA) circuit which is used to find the maximum and minimum outputs from given set of inputs. In analog design there has always remained a trade-off in between several major parameters like speed, size, functionality, resolution, supply voltage etc.

These circuits also find application in the area of fuzzy logic circuits [13, 25] for implementing nonlinear circuits. These circuits are used for high end results. This circuit can also be employed in various fields like signal processing [3, 9], cellular neural network and data compression.

One of the primary limitation in deploying this design is high precision which needs taken care off. While differentiating between the inputs that have equal magnitudes these errors occur. Another restriction is imposed by supply voltage because neural network circuits have to work in collaboration with several other circuit so energy requirement increases as whole. Moreover, the signals are of very weak signal strength which have to be located and responded back. So, keeping trade-off between constraints the design has been proposed that results in reduced supply voltage requirement of the circuit without degrading high resolution.

1.2 Motivation

The rapid growth in the field of fuzzy logic and neural network has led to the design of high precision and low supply circuits for the hardware realization for these systems. WTA/LTA circuits provide solutions to that areas, where the physical variable carrying on the information is either current or voltage and there is need to find information in form of maximum or minimum signal. Hardware implementations which take voltages as inputs are generally based on operational amplifiers that means complex circuit blocks.

More promising for VLSI are current based implementations of maximum and minimum circuits. For these applications current-mode techniques are used to design and is currently the subject of intense research activities since offering advantages in terms of power, efficiency, chip area and simplicity.

The applications are found in particular areas as fuzzy or artificial neural networks, analog signal processing areas, communications, instrumentation, *etc*.

1.3 Key Contributions

The work in the thesis can be summarized as follows.

1. Designing and simulation of proposed WTA/LTA circuit that finds maximum and minimum values simultaneously from given input currents.
2. Using high swing cascoded current mirror high precision has been achieved.
3. Half wave rectifier, full wave rectifier and modulus circuit are also investigated.

In this dissertation, a low voltage with high precision Winners takes all/ Loser takes all circuit is proposed which computes the maximum and minimum value from given current inputs. High swing cascoded current mirror has be used as the major component which not

only helps in reduction of error to improve precision but also contributes to in decreasing supply voltage requirement.

Applications of WTA/LTA circuit have also been achieved by exploiting its basic capability to find maximum and minimum. The wave rectifier has been verified by applying one input current in form of sinusoidal current and other as dc current. Output obtained from maximum and minimum output are half wave rectified. While in full wave rectifier both the input currents are applied in form of sinusoidal but in out of phase. The output is obtained from maximum output. Modulus circuit is crucial function used in

The circuit inherits advantages such as low supply voltage requirement, high precision and low error.

1.4 Organization of thesis

The organization of this dissertation is as follows:

CHAPTER 1: This chapter includes introduction, motivation for the proposed circuit, key contributions and the organization of the thesis.

CHAPTER 2: This chapter addresses the literature survey of the WTA/LTA circuits.

CHAPTER 3: This chapter presents operation of proposed WTA/LTA circuit and its applications such as half wave rectifier, full wave rectifier and modulus circuit.

CHAPTER 4: In this chapter simulation results have been given to ensure the effectiveness of the proposed circuits. Various parameters of the proposed circuits have been compared and presented with the similar circuits available in literature.

CHAPTER 5: This chapter concludes the thesis and suggests the future scope of the work.

CHAPTER

WTA AND LTA CIRCUITS

2.1 Introduction

The idea of winners takes all is taken from a living being's natural behavior, a person responds to that part of the body where the stimuli applied is maximum. This idea has been formulated in circuitry form, where a bunch of inputs are applied to circuit and only one input signal with strongest magnitude is allowed to propagate at output. In similar manner where out of several neurons only one neuron with maximum signal strength reaches human brain and gets response instantly. This method is realized by Winner takes all circuit (WTA). Whereas, the circuits that are designed by subtracting inputs from an altered reference to accomplish the required calculation to get minimum value. This primary computational move to perform these determination operations is executed by looser takes all (LTA) circuit.

The winner takes all (WTA) and loser takes all (LTA) circuits are used to generate computational functions for nonlinear circuits. Also, these circuits play a significant role in neural networks [13], fuzzy logic blocks [13, 25], signal processing applications [3, 9], rectification systems [5, 20] etc. In literature, several authors have reported various WTA/LTA circuits using voltage and current mode approaches [1-6, 7-18]. The voltage mode WTA / LTA circuit was introduced by Anderson et al. in 1992 [1]. The circuit includes a number of adaptable current mirrors with floating node, which is controlling node of the WTA circuit. The circuit has poor resolution and complex circuitry. Opris [2] proposed a multiple-input maximum/minimum circuit that has improved resolution and reduced corner errors than the circuit suggested in [1]. Minimum circuits with better resolution have presented in [3-4], in which each source follower is replaced by a flipped

voltage follower cell. Promme et al. [5] presented a CMOS based voltage-mode multiple-inputs WTA (WTA) maximum and minimum circuits with improved performance. A differential pair with improved cascode current mirror is used to choose the desired input. Voltage-mode maximum-minimum circuit presented by Soleimani et al. [6] that operates with high precision at high frequencies.

Current mode WTA/LTA circuit was introduced by Lazzaro et al. in 1989 [7], which formed foundation stone for current mode WTA/LTA circuits. Serrano et al. [8] have presented a WTA circuit with improved precision. Demosthenous et al. [9] have suggested a WTA circuit with improved operating speed and resolution by using alternatively NMOS and PMOS.

Lazzaro et al.'s [1] current mode WTA/LTA circuit is shown in Figure 2.1, which still holds relevance even after two decades. Many circuits based on this Lazzaro's circuit were proposed later on with improvements. It choose the strongest of the input currents applied and the output is sensed at the common node, but the main disadvantage of the circuit is poor resolution.

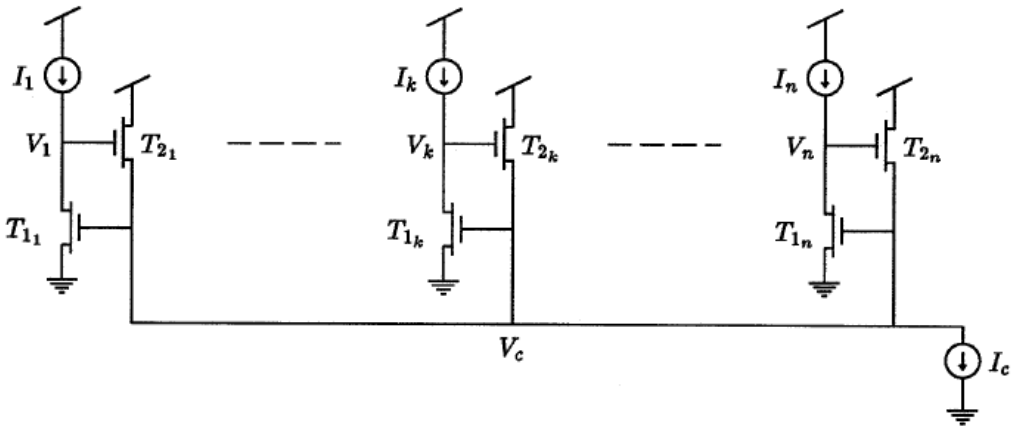

Figure 2.1 Lazzaro's current mode WTA [1]

There are several applications of WTA/LTA circuit such as star tracking system[10], neuro fuzzy controller[11] and mixed signal CMOS fuzzy logic controller [12]

h.The speed and resolution of WTA circuit suggested in [13] have been improved using inhibitory and local excitatory feedback based on input current average computation**.** Alikhani et. al. [14] have proposed WTA/ LTA circuit that can find minimum and maximum simultaneously for two inputs with good precision and accuracy. Abdulla et al. [15] suggested a multi-input fuzzy minimum and maximum circuit based of Wilson current mirror with improved characteristics of speed, accuracy and simplicity of design.

In this thesis, a novel current mode WTA/LTA circuit with high precision and high resolution is proposed. The half wave-rectifier, full wave rectifier and modulus circuit based on proposed WTA/LTA circuit are also presented.

2.2 Characteristics of WTA/LTA circuits

The basic design parameters that distinguish different WTA/LTA circuits are as follows:

- Resolution: The resolution of the WTA circuit is the minimum difference between two inputs that the circuit can resolve and sustain it over entire dynamic range for the same result.
- Speed: The speed of the device depends upon the response time of the circuit.
- Compactness : Compactness is highly desirable so that that design takes least amount of space and is insensitive to spatial distribution.
- Supply voltage requirement: It depends upon the biasing of the circuit required to operate the transistors in particular region of operation.
- Power dissipation: It relies on several factors among them some are transistor count, input/output impedance of the circuit, supply voltage and frequency of input applied.

WTA/LTA circuits are also differentiated based on their type of input supplied and output obtained. These are as follow

- Current mode WTA/LTA circuits
- Voltage mode WTA/LTA circuits

When the inputs are applied in form of current and output is also obtained in form of current then this type of circuits are known as current mode WTA/LTA circuits. On the other hand when the voltage inputs are delivered then this type of circuit are called as voltage mode WTA/LTA circuits.

There are many areas that require WTA/LTA circuit's operation such as in image processing[12] where there is need of spatial image processing, spotting most shining or high contrast objects from the picture these circuits can be employed along with transducers and sensors. Even in video processing areas these circuits are used to find part of video highest or lowest resolution. In neural networks to find and address the neuron with strongest and weakest signal strength these circuits are applied. In communication systems where demodulation is done to extract the signal from carrier signal these circuits can be used. In computations circuits to calculate modulus, difference, maximum and minimum at every instant of time these circuits are used.

3 CHAPTER

LITERATURE REVIEW

Various authors have reported maximum/minimum or WTA/LTA circuits [2-19]. A brief review based on their papers is as follows:

Lazzaro *et al.* [1] introduced basic WTA circuit to operate in weak-inversion as well as in strong inversion mode. It choose the maximum of the currents injected to its inputs. The output was sensed at the common node, which lumped interconnection parasitic. The complexity of system increased due to device mismatch resolution degraded. Another important design trade off was deceasing mismatch effect with increase in transistor size in the expense of silicon area.

Anderson *et al.* [2] suggested winner takes all consist of number of conventional current mirrors, each having with a floating node for flow of current and controlling the potential at field effect transistor. This is first voltage based WTA circuit. This circuit is basic circuit that uses properties of current mirrors to replicate the inputs and find maximum. Resolution of the circuit is not good enough but design is simple. Supply voltage requirement is high.

U. Cilingiroglu *et al*. [2] have suggested architecture of Loser Takes All Circuit, which is a charge domain application. This design is generalized version of a two input charge sensing latched refresh amplifier used in DRAMs. This design has good resolution with certain drawbacks of the circuit that the area requirement increased with square of the inputs applied and the circuit is unable to be parallelized by a simple inter connection.

Teresa Serrano *et al.* [8] presented a current mode based WTA circuit. The operation circuit depend on current transfer, comparison and replicating by current mirrors. It had

improved resolution than circuits discussed before and has n number of inputs without degrading precision unlike the earlier circuits. But delay and complexity of the circuit increases at greater rate when input current are increased.

Baturone *et al.* [3] proposed a circuit based on WTA (winner-take-all) circuits with interconnection of the simple two transistors. The design to convert a WTA into a current-mode max operator circuit only needs a simple transistor in saturation to recover maximum current from this shared voltage. The circuit is simpler than that reported [1] in achieving same precision. In addition, since only the winner cell is conducting, the power dissipation is less. The structure is connection of Wilson current mirrors which share their output diode connected transistor.

Opris [2] has proposed a multiple-input maximum/minimum circuit technique, which reduces the errors associated with previous analog circuit implementations [1] by combining a common-source voltage-mode configuration with a current-mode "winner takes all" circuit.. The architecture minimizes the "corner errors" by combining a voltage-mode common-source configuration with a current-mode circuit. The main advantages of this approach are the linear complexity with the number of inputs and the use of local feedback loops that improve the circuit's functionality at high frequencies. Two complementary half circuits are used to achieve simple architecture.

Carvajal *et al.* [3] have presented a voltage-mode maximum circuit that have a simple architecture with low supply voltage (1.5V). Unlike conventional winner-take-all [1] or source follower [2] based schemes, the circuits are characterized by reduced voltage swing at all internal nodes and by a very low output impedance, which enables them to provide high-speed and high-precision operation. All follower transistors share a common output node and a common bias source. Their complexity grows linearly with the number of inputs.

The proposed technique has advantages as following

(a) all internal nodes have small voltage swings .

(b) high speed operation.

Giacomo Indiveri [6] suggested a current mode WTA circuit that is improved version of Lazzaro's circuit [7], it exhibits local excitatory feedback and lateral excitatory coupling which has been applied to implement distributed hysteresis. These methods have been applied enhance the charaterstics like resolution , speed of the circuit and supply voltage.

Angulo *et al.* [5] purposed a circuit that exhibits linear increase of complexity with the number of inputs at the rate of only three transistors per input. In the circuit, each input follower is enhanced by local shunt feedback to increase the gain and to reduce the output impedance.

Siskos *et al* [12] presented a nonlinear filter that has its functionality based on current mode WTA circuit. The circuit is developed using current comparator, feedback network. Earlier circuits could only find maxima or minima only but the suggested circuit can also compute median of the inputs. The processing rate, accuracy and speed of the circuit is quite good. The major limitation was large area requirement due to its complex functionality.

Prommee *et al.* [4] proposed configuration based on d a CMOS based near zero-offset multiple inputs maximum and minimum circuit. The analog signal building blocks including shunt-feedback buffer, voltage-subtraction circuits and current mirrors are deployed for obtained the good performances. This achieved circuit is a simply scheme and able to work with low power supplies. The input range is obtained around ± 600 mV within ±1.5 V power supplies. Near zero-offset and low output impedance are provided by proposed circuit. The delay of output is less than 5ns.

The proposed configuration of CMOS-based multiple inputs max-circuit and min-circuit are based on Winners take it all [1] principle. Symmetry of inputs was realized and multiple inputs can be operated, but using too many transistors and complex structure [2]. The results of realization are compactness and the lowest output offset is adjustable.

The voltage follower's characteristics including near zero-offset, low delay, low THD and wide bandwidth are obtained with a simple configuration. The low delay time is achieved around 5 ns.

Peymanfar *et al.* [11] presented a new design based on a strategy in which analog advantages such as low die area, high speed and simplicity were added to the system, whose output is digital considering unchanged digital system properties. For implementing this idea, a new programmable Fuzzifier circuit based on mixed-signal input and generation of three different current membership functions including Gaussian, Trapezoidal and Triangular shapes have been proposed. To contribute antecedents in inference block, three new integrated circuits for implementing Max-Min operators are proposed.

Prommee *et al.* [10] purposed design of a voltage-modem multiple-inputs winner-take-all (WTA) maximum (max) and minimum (min) circuits. The proposed circuits are realized in a CMOS technology with low- component counts of transistors, which in turn provides low output impendence, fast response and simple structure.

Alikhani *et al.* [13] have suggested a CMOS based current mode maxima /minima circuit based on Wilson current Mirror. The proposed circuit has lower number of transistors, can detect minimum and maximum of the input currents at the same time, shows high precision.

The salient features of the proposed circuit are

- Single circuit for maximum and minimum detection.
- High speed
- High precision

Abdulla *et al.* [14] have proposed a simple current mode multiple input maximum/minimum circuit for fuzzy interface system. The circuit is based on Wilson current mirror taking analog design advantages such as low die area, high speed, and simplicity. Circuit is modular current-mode to obtain the minimum and maximum of N analog inputs. For implementing his idea, new current mode circuits are proposed which is

based on the Wilson current mirror. The proposed circuit has needs fewer transistors than the previous designs. More importantly, because the circuit has one stage structure, not only the problem of accumulation error solved but the speed of circuit operation has increased. The accuracy of circuit is mainly dominated by the input current mirror, moreover output current errors can be reduced by substituting the cascaded mirror for the basic current mirror

The circuit has following features:

- the number of transistors needed for n-input Minimum circuit is only n(n+3) and n-input maximum is only 3(n+1).
- the dynamic range of the circuit is large.
- speed of circuit is high.

Rahman et al. [15] proposed a voltage based WTA circuit capable of distinguishing input voltages with good precision of millivolts range. This precision is achieved by applying inhibitory along with local feedback approach. But the resolution of circuit decreases when the inputs are applied in layered form. Power consumption is low but circuit is complex. Use of various PMOS transistors increases the area requirement of the circuit.

Dlugosz [27] presented a current mode WTA circuit which has good resolution by avoid replication of the applied analog signal between different layers unlike in other circuits that used techniques of common collector or binary tree approaches. The technique used is in-between of the two approaches. The circuit has trade-off between minimum current input and capacitance of the circuit, as the delay increases with capacitance. As the input currents are increased the complexity of circuit increases with square of inputs applied.

Ghanavati [28] proposed different circuits for current mode WTA and LTA circuit that operate at low supply voltage requirement. Furthermore, at high frequency they operate with good resolution. The limitation for this circuit is that different circuits are required for computation of maximum and minimum from the applied inputs.

CHAPTER 4

PROPOSED WTA/ LTA CIRCUIT

4.1 **INTRODCTION**

Current mode WTA/LTA circuit was introduced by Lazzaro in 1989 [7], which formed foundation stone for current mode WTA/LTA circuits. It can choose the maximum of the input currents applied and the output is sensed at the common node, but the circuit has poor resolution and speed. Serrano et al. have presented a WTA circuit with improved precision based on circuit transformation, replication and comparison [8]. The problems of speed and resolution have been improved using inhibitory and local excitary feedback based on input current average computation [9]

A novel current mode WTA/LTA circuit with high precision and high resolution is presented. The block diagram representation is shown in Figure 4.1.The half wave-rectifier, full wave rectifier and modulus circuit based on proposed WTA/LTA circuit are also proposed. The thesis is organized as follows.

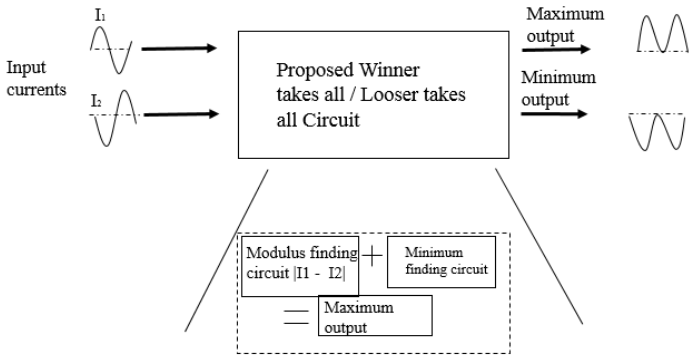

Figure 4.1: Block diagram of WTA/LTA circuit

4.2 Proposed WTA/LTA circuit

The proposed WTA/LTA circuit is shown in Figure 4.2. The circuit is developed using high swing cascode current mirror [22] (HSCCM) which generates equal current in the

transistors under node X and Y. As soon as magnitude of one of the input currents becomes higher, for example current from first input source is than second input current source, the gate potential of transistor M_{16} connected at node X becomes higher than transistor M_{17} connected at node Y, this turns on

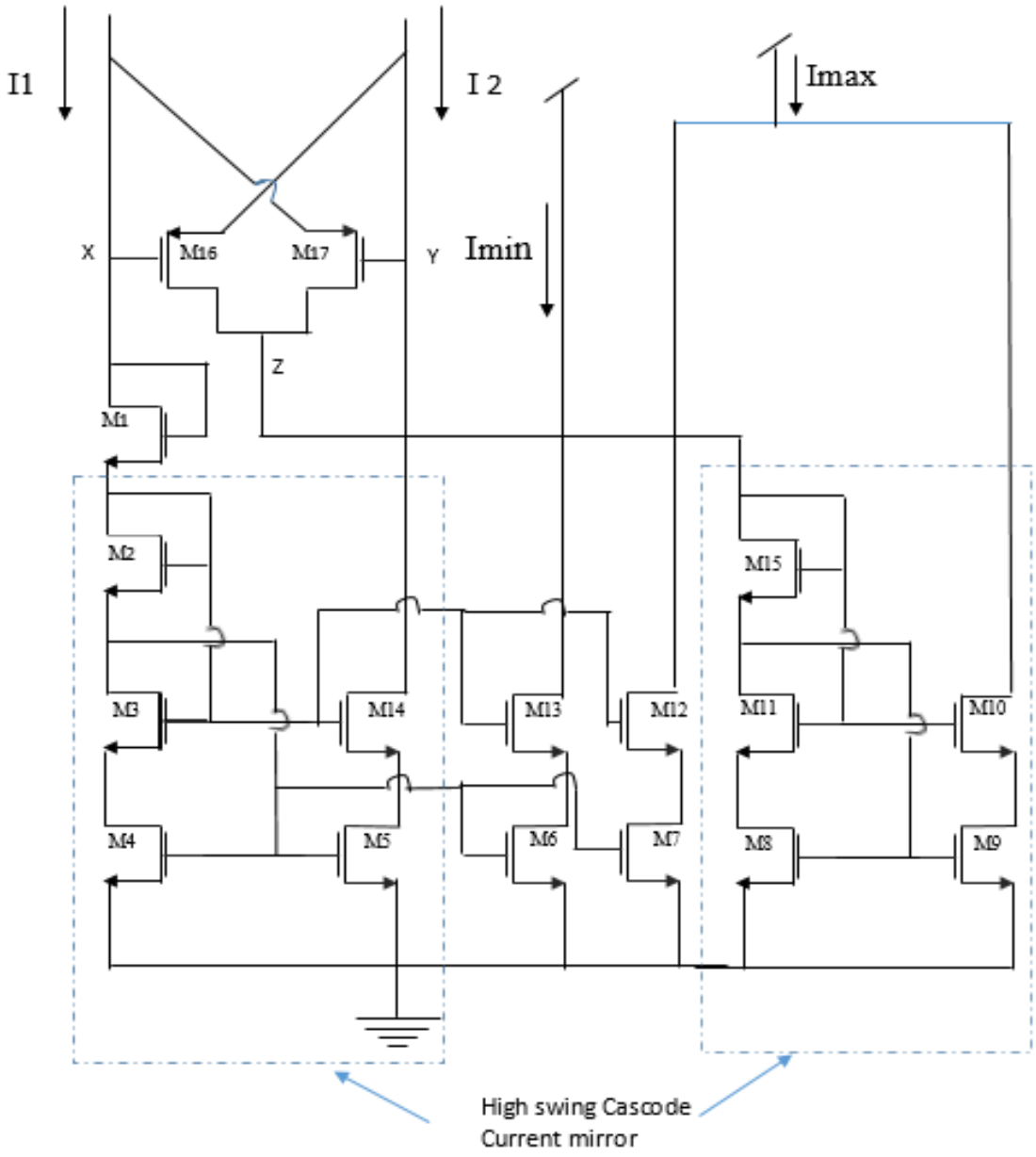

Figure 4.2: Proposed WTA/LTA circuit

transistor M_{17}, which is connected at lower gate potential because the drain terminals of both the transistors are shorted at node Z. The difference between two input currents I_1 and I_2 is reflected in transistors M_{8-} M_{11} and M_{15}. In other words, to obtain maximum of the two input currents, the absolute difference between two input currents ($|I_2 – I_1|$) is added to the minimum current value of them. Similarly, if input current at node Y is greater than input current at node X, then node voltage of Y increases in comparison with the node voltage of X. Therefore, transistor M_{17} turns off and transistor M_{16} is on. The difference of two input currents ($I_2 – I_1$) flows to the current mirror through transistor M_{17} will be added to the minimum of the input currents to obtain the maximum value of the two input currents. When both the input currents are equal then neither transistor M_{16} nor transistor M_{17} will turn on. Consequently maxima and minima output currents will be equal (i.e. $I_{min} = I_{max}$).

4.3 Circuit Analysis

WTA / LTA circuit is composed of three basic components which are high swing cascode current mirror, substractor circuit and an additional active resistor. The nature of this circuit depends on these components. The active resistor is used to balance offset.

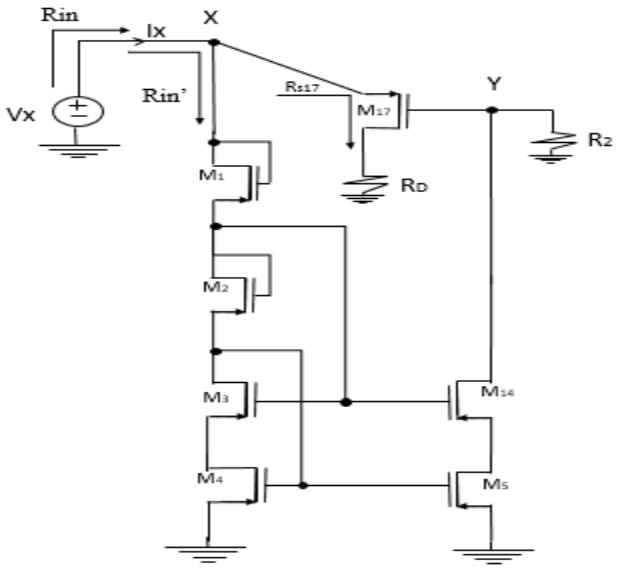

Figure 4.3: Equivalent input impedance model of the proposed WTA/LTA circuit

4.3.1 Calculation of input and output impedance of proposed circuit

Now the actual path travelled by the current when $I_1 > I_2$ through transistor M16 and then to branch. The equivalent input impedance model of the proposed circuit is shown in Figure 4.3. The total input impedance (R_{in}) and input impedance experienced at node X towards ground (R_{in}') are given as

$$R_{in} = Rin' || Rs17 \quad (1)$$

The input impedance Rin' experienced at node X towards ground is given as

$$Rin' = \frac{1}{gm1} + \frac{1}{gm2} + \frac{1}{gm4} \quad (2)$$

where g_{m1}, g_{m2} and g_{m4} are transconductances of transistors M_1 , M_2 and M_4 respectively.

The drain to source impedance of transistor M_{17} is given as

$$R_{s7} = \frac{ro17 + RD}{1 + ro17.gm17} \quad (3)$$

where ro_{17} and g_{m17} are impedance and transconductance of transistor M_{17}.

The impedance of the cascode of current mirror denoted as R_D that evaluates the difference of input currents is written as

$$R_D = \frac{1}{gm15} + \frac{1}{gm8} \quad (4)$$

where g_{m8} and g_{m15} transconductance of transistors M_{15} and M_8 respectively

Using eq. (3) and (4) the drain resistance Rs_7 is modified as

$$Rs7 = \frac{r017.gm15.gm8 + 1}{gm15.gm8(1 + ro17gm17)} \quad (5)$$

Also, using eqs. (1), (2) and (5), the total input impedance at the input terminal is expressed as

$$R_{in} = \frac{(r017.gm15.gm8 + 1) * (gm1 + gm2 + gm4)}{gm15gm8(1 + ro17gm17) * (gm1 + gm2 + gm4) + (gm1gm2gm4) * (r017.gm15.gm8 + 1)} \quad (6)$$

Assuming gm4=gm5=gm7=gm2, and gm15=gm8 eq. (6) reduces to

$$R_{in}=\frac{(r017.gm8\text{^}2+1)*(gm1+gm2+gm4)}{gm8\text{^}2(1+ro17gm17)*(gm1+gm2+gm4)+(gm1gm2gm4)*(r017.gm15\text{^}2+1)} \quad (7)$$

From eq. (7) it is observed that the total impedance depends on g_{m1}, g_{m2} g_{m4}, g_{m8} and r_{o17}

Similarly, when input current at node Y is greater than the input current at node X, the transistor M_{17} turns on and the actual path travelled by maximum current and minimum currents is shown in Figure 3.

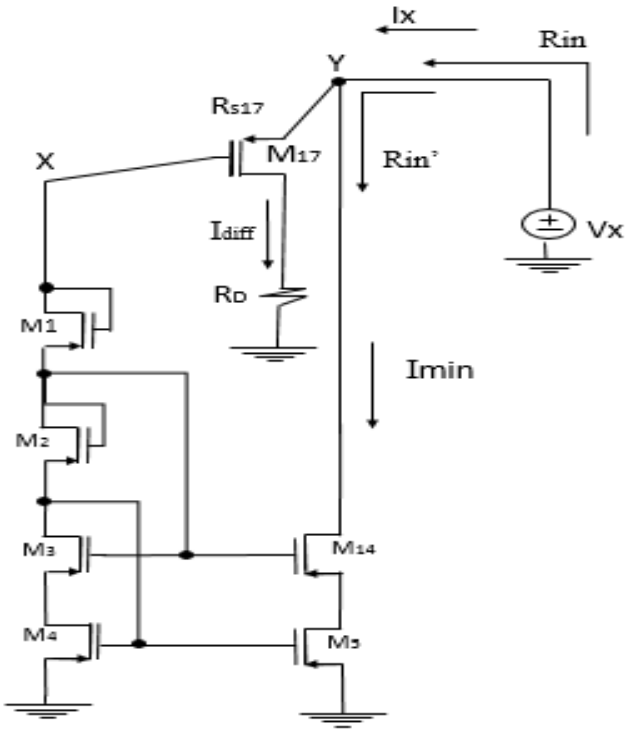

Figure 4.4: Equivalent input impedance model of the proposed WTA/LTA circuit (If $I_2 > I_1$)

The equivalent input impedance R_{in} at node Y is given as

$$R_{in}=\frac{(r014.gm14gm5(r016gm15gm8+gm15+gm8)}{gm15gm8r014gm14gm14r05*r016(gm15+gm8))} \quad (8)$$

where $r012$, $r014$ and $r16$ are drain to source resistances of transistors M_7, M_{10} and M_{12} respectively.

For the calculation of output impedance maximum output, the small signal model of the proposed WTA/LTA circuit is shown in Figure 4

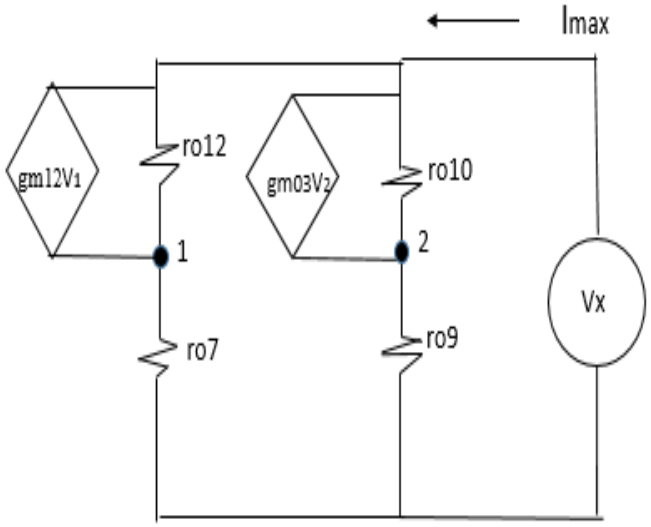

Figure 4.5: Small signal model at maximum output

The output impedance R_{out} is given as

$$R_{out=}(r07ro12gm12)||(ro10ro9gm10) \quad (9)$$

where $r07$, $r10$ and $r12$ are drain to source resistance of transistors M_7, M_{10} and M_{12} respectively, $gm10$ is transconductance of M_{10} and $gm12$ is transconductance of M_{12}.

For the calculation of output impedance at minimum output small signal model of the proposed WTA/LTA circuit is shown in Figure 5.

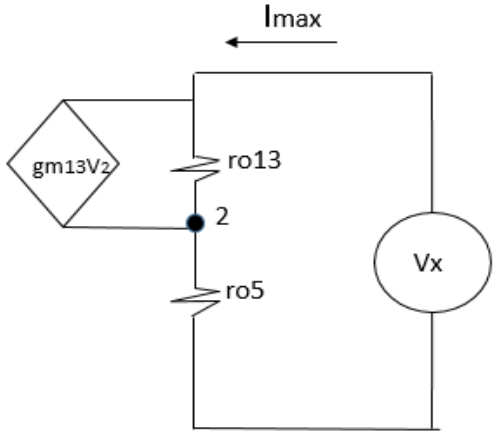

Figure 4.6: Small signal model at minimum port

The output impedance R_{out} is given as

$$\frac{Vx}{Ix} = r05 + r013 + r013.r05.gm13 \quad (10)$$

In eq. (10), the value of $r013.r05.gm13$ is chosen as

$$r05.r013.gm13 >> r05 + ro13 \quad (11)$$

Using eq.(10) and (11), eq.(10) reduces to

$$R_{outMin} = 05.r013 \,.\, gm13 \quad (12)$$

where r_6 is drain to source impedances of transistors M_5 and $ro13$ is drain to source impedances of transistors M_{13} and $gm13$ is transconductance of M_{13}.

4.3.2 Analysis of dynamic range

For the calculation of the dynamic range of the circuit we can neglect the body bias effect to reduce complexity of the circuit.

For the MOSFET to be in saturation region of operation following conditions must be satisfied.

$$V_{DS} \geq V_{GS} - Vth \quad \text{and} \quad V_{OV} > 0 \quad (13)$$

where V_{DS} is the drain to source voltage, V_{GS} is the gate to source voltage, Vth is the threshold voltage of the MOSFET and V_{OV} is the overdrive voltage($V_{OV} = V_{GS} - Vth$)

The voltage V_y at node Y is given as

$$V_Y \geq V_{ov5} + V_{ov14} \quad (14)$$

where V_{ov5} and V_{ov14} are overdrive voltages of transistors M5 and M14 respectively.

The voltage V_y can also be written as

$$V_Y \geq I_D/gm5 + I_D/gm14 \quad (15)$$

where I_D is the minimum current flowing through node Y and $gm5$ and $gm14$ are transconductances of transistors M_5 and M_{14} respectively.

The drain current I_D is given as

$$I_D \leq V_Y/(1/g_{m14} + 1/g_{m5}) \quad (16)$$

Since, the transistors M_5 and M_{14} are perfectly matched eq.(16) is modified as

Consider transistors identical, eq (20) reduces to

$$I_D \leq V_y.g_m/2 \quad (17)$$

The voltage at V_x at node X is given as

$$V_X \geq Vgs1 + Vth + Vov2 + Vov4 \quad (18)$$

where Vx is potential at node X, Vgs1 is the gate to source voltage of transisitor M1, $Vov2$ is overdrive voltage of transistor of M_2, $Vov4$ is overdrive voltage of transistor M_4 and Vth is threshold voltage.

The voltage Vx can be written as

$$V_X \geq \frac{2I_D}{gm1} + Vth + Vth + 2\,I_D/gm2 + \frac{2I_D}{gm4} \quad (19)$$

where gm1, gm2 and gm3 are transconductances of transistor M_1, M_2

and M_4 respectively.

After simplification eq. (23) reduces to

$$I_D \leq (V_X\text{-}2V_{th}) / 2(1/gm1 + 1/gm2 + 1/gm4) \quad (20)$$

For similar transistors gm1 = gm2 = gm4= gm eq.(20) is modified as

$$I_D \leq (V_X - 2V_{th}).g_m/6 \quad (21)$$

To calculate the range of the difference of two input currents ΔI generated by transistors M_{16} and M_{17}, it is considered as $I_1 > I_2$. The voltage V_Z at node Z is given as

$$V_z \geq Vov8 + Vov15 + V_{th} \quad (22)$$

where $Vov8$ and $Vov15$ are overdrive voltages of transistors M_8 and M_{15} respectively.

The voltage Vz can also be written as

$$Vz \geq 2\Delta I \left(\frac{1}{gm8} + \frac{1}{gm15}\right) + Vth \quad (23)$$

From eq.(23) the difference of two input currents is given as

$$\Delta I \leq (Vz - V_{th})/2 \left(\frac{1}{gm8} + \frac{1}{gm15}\right) \quad (24)$$

The difference of the two input currents ΔI will pass either through M_{16} or M_{17} depending upon the magnitude of two currents, so one of the transistors goes to triode region while other in saturation region. Suppose $I_1 > I_2$, then M_{16} goes to triode region and the drain to source voltage V_{YZ} of M_{16} is given as

$$V_{YZ} = V_Y - Vz \leq V_{SDsat16} \quad (25)$$

Using eqs. (15), (19) and (25) the voltage V_{YZ} is modified as

$$V_{YZ} = 2I_D(1/gm5 + 1/gm14) - 2\Delta I \left(\frac{1}{gm15} + \frac{1}{gm8}\right) - V_{th} \quad (26)$$

Using eq.(26) in eq.(25), eq.(25) is modified as

$$\{ 2I_D(1/gm5 + 1/gm14) - 2\Delta I\left(\frac{1}{gm15} + \frac{1}{gm8}\right) - V_{th}\} \leq 2\Delta I/gm16 \quad (27)$$

Assuming gm5 = gm14 = gm15 = gm8 = gm in eq. (27), the difference of two input currents ΔI is given as

$$\Delta I \geq I_D - 2V_{th}.gm \quad (28)$$

4. 4 Applications of WTA circuits

In this section, the applications of the proposed WTA/LTA circuit as half wave rectifier, full wave rectifier and modulus circuit are addressed There are several area where

this circuit can be employed. Some of the applications of the WTA/LTA circuit, have been proposed here in thesis .

4.4.1 Half Wave rectifier

Figure 4.7 shows the block diagram representation of WTA/LTA circuit as half wave rectifier(HWR), in which one of input current is applied as a sinusoidal current and other is applied as a DC current. From the figure, it can be seen that the circuit finds the maximum value in the positive half cycle and minimum value in the negative half cycle, which proves the rectification behavior of the proposed WTA/LTA circuit.

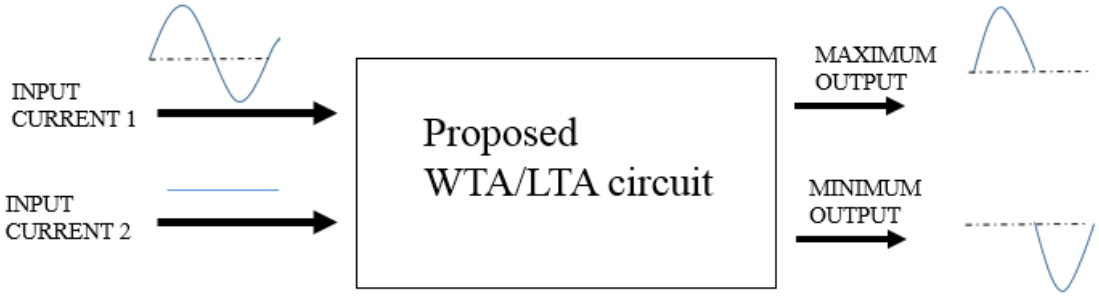

Figure 4.7: Proposed half wave rectifier based on WTA/LTA circuit

4.4.2 Full Wave rectifier

Figure 4.8 shows the block diagram representation of WTA/LTA circuit as full wave rectifier(FWR), in which both of the applied input currents are sinusoidal waveforms of equal magnitude with phase difference of 180^{o}. From the figure, it can be seen that the circuit finds the maximum value in the positive half cycle and minimum value in the negative half cycle, which proves the rectification behavior of the proposed WTA/LTA circuit.

.

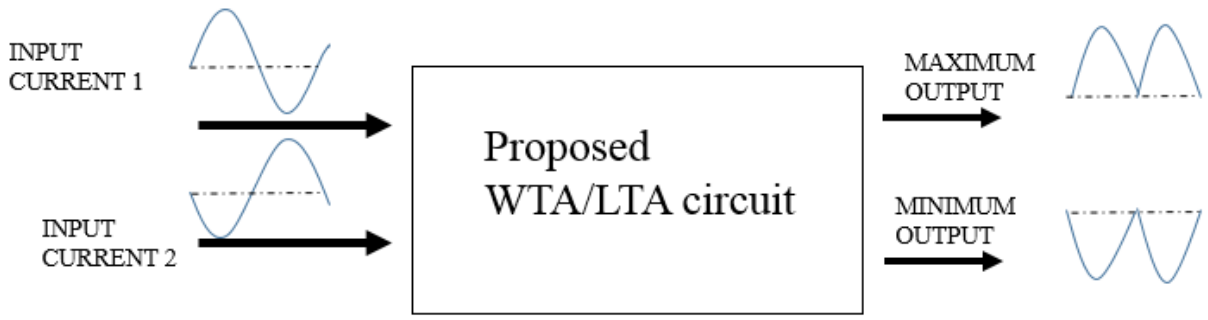

Figure 4.8: Proposed full wave rectifier based on WTA/LTA circuit

4.4.3 Modulus Circuit

The proposed WTA/LTA circuit can also be used to calculate the modulus of two input currents (i.e. $|I_1 - I_2|$) by connecting minimum output port to the ground as shown in Figure 4.9.

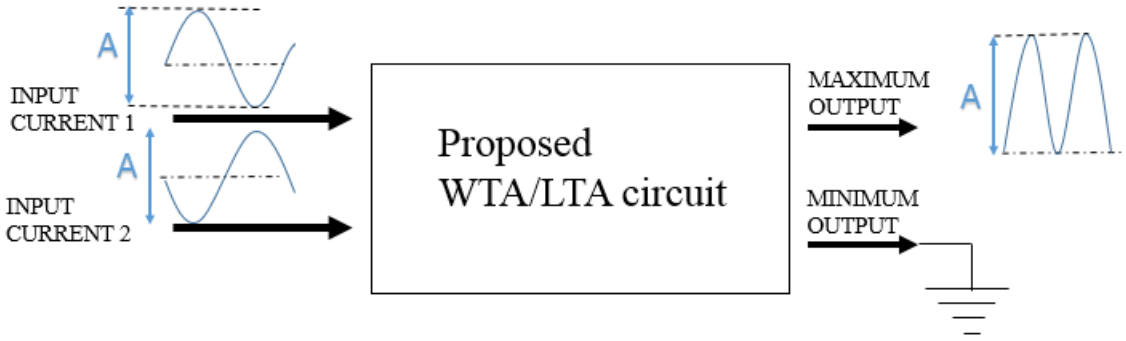

Figure 4.9: Proposed modulus circuit based on WTA/LTA circuit

5 CHAPTER

SIMULATIONS RESULTS

5.1 INTRODUCTION

The proposed WTA/LTA circuit has been simulated in 0.18um CMOS technology with SPICE level53 (TSMC) parameters. The chapter is organized as follows. Section 5.2 presents the simulation results of proposed high precision low-voltage WTA/LTA circuit. Section 5.3 includes the presents the simulated results applications of proposed WTA/LTA circuit, also it includes the table of comparison of proposed circuit with earlier proposed circuits and table of designing parameters of transistors used.

5.2 SIMULATION RESULTS OF PROPOSED WTA/LTA CIRCUIT

Figure 5.1 and 5.2 show the maxima output plots. For Figure 5.1, both the input currents are applied as sinusoidal waveforms of frequencies 50 kHz and 100 kHz

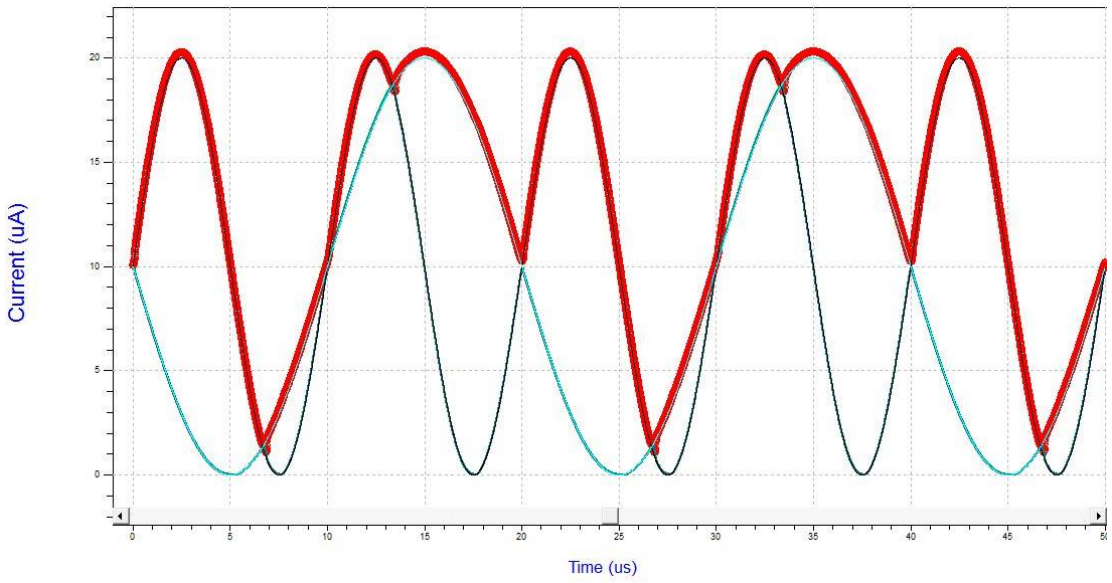

Figure 5.1: Maximum output at 100 kHz and 50 kHz sinusoidal current inputs

and for Figure 5.2 both the input currents are applied as triangular waveforms of frequencies 33.33 kHz and 66.66 kHz. It is observed that in both figures the maxima output plot follows the input current having maximum value at every instant of time.

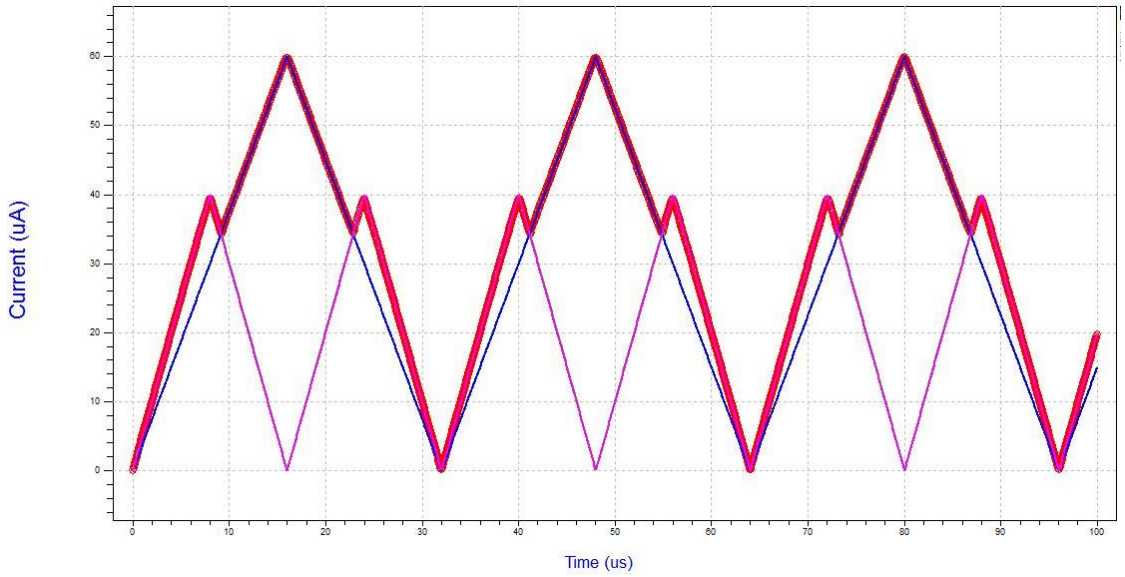

Figure 5.2: Maximum output of triangular wave at 66.66 kHz and 33.3 kHz

Figure 5.3 shows the error plot for maximum output of proposed WTA/LTA circuit for sinusoidal current inputs of frequencies 50 kHz and 100 kHz. From the plot, it is observed that the maximum error is 0.047 uA

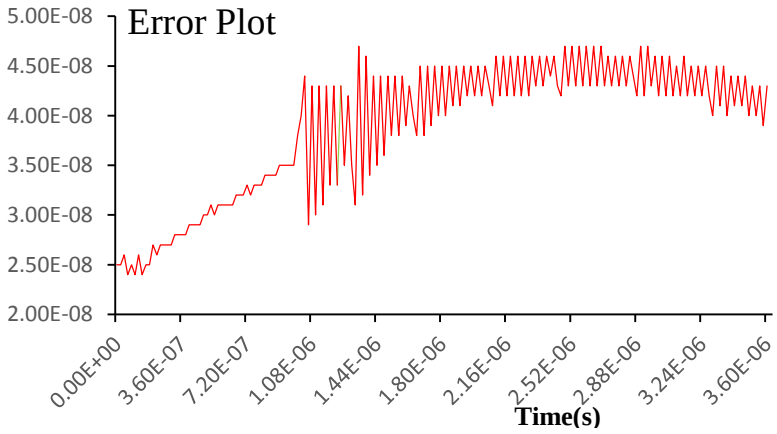

Figure 5.3: Error plot for maximum output of proposed WTA/LTA circuit

Figures 5.4 and 5.5 shows the minima output plot for sinusoidal and triangular waveforms respectively. For the plot in Figure 5.4 the input currents are applied as sinusoidal waveform of frequencies 100 kHz and 50 KHz. And for Figure 5.5 the input currents are applied as sinusoidal waveforms of frequencies 33.33kHz and 66 kHz .it is observed that the minima plot follows the input having least value at given instance time.

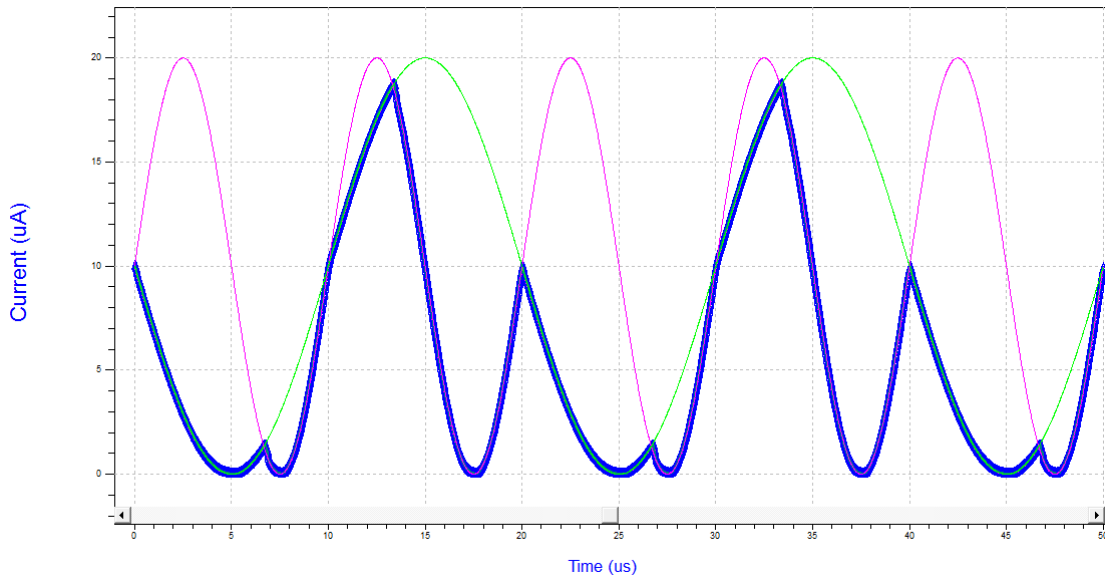

Figure 5. 4: Minimum output at 100 kHz and 50 kHz sinusoidal current inputs

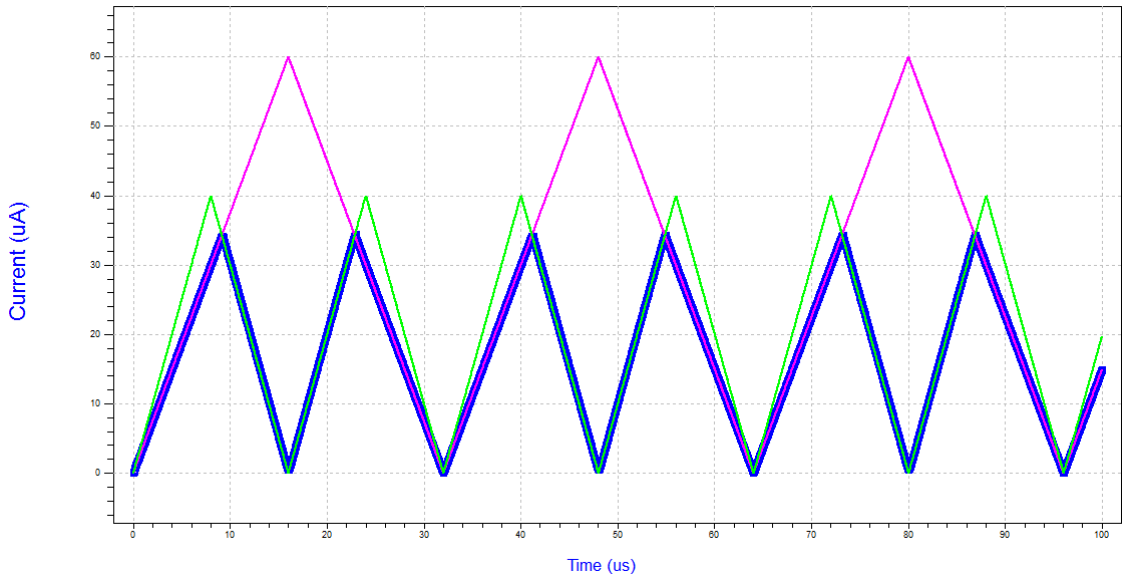

Figure 5.5: Minimum output for triangular waveforms at frequency 33.33 kHz and 66.66 kHz

Figure 5.6 shows the error plot for minimum output of proposed WTA/LTA circuit for sinusoidal current inputs of frequencies 50 kHz and 100 kHz. From the plot, it is observed that the maximum error is 0.12 uA.

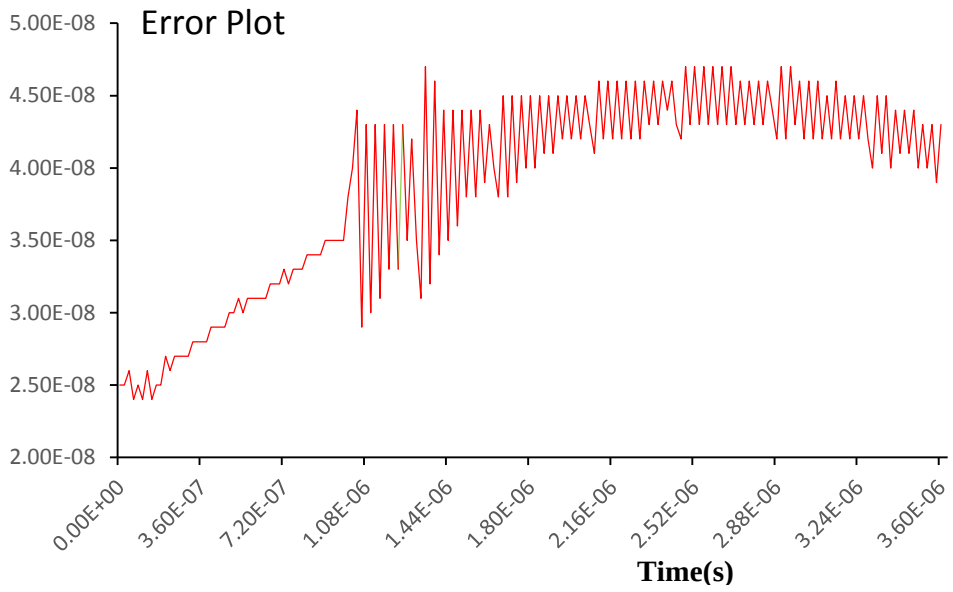

Figure 5.6: Error plot for minimum output of proposed WTA/LTA circuit

5.3 Applications

5.3.1 Half wave rectifier - Figures 5.7 and 5.8 show the rectified signals of the proposed WTA/LTA circuit as half wave rectifier. The rectified outputs of half wave rectifier are obtained by applying one of the input currents as DC of 10uA and another input current as sinusoidal waveform of 100 kHz.

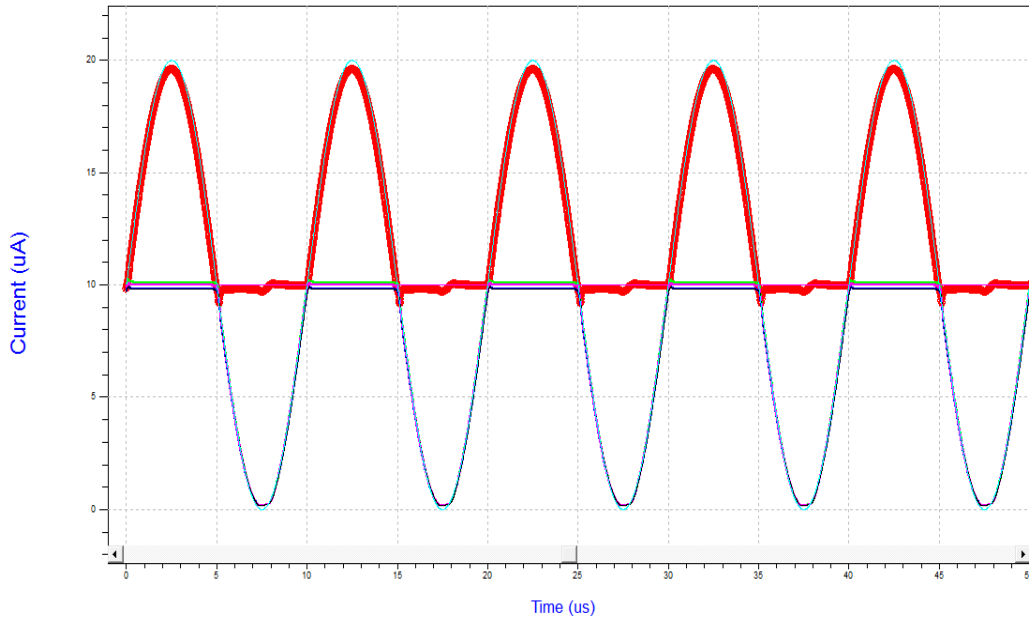

Figure 5.7 Rectified output of proposed WTA/LTA circuit as half wave rectifier (for positive cycle)

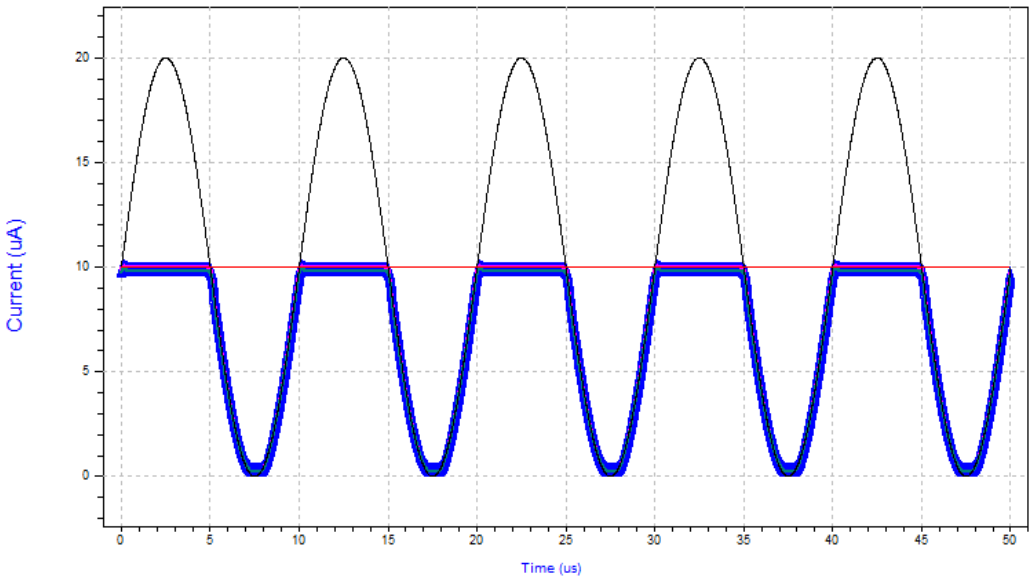

Figure 5.8: Rectified output of proposed WTA/LTA circuit as half wave rectifier (for negative cycle)

5.3.2 Full Wave rectifier

Figure 5.9 shows the rectified signal of the proposed WTA/LTA circuit as full wave rectifier. The rectified output of full wave rectifier is obtained by applying two input currents as sinusoidal waveforms of same frequencies of 100 kHz with phase difference of 180^{o}.

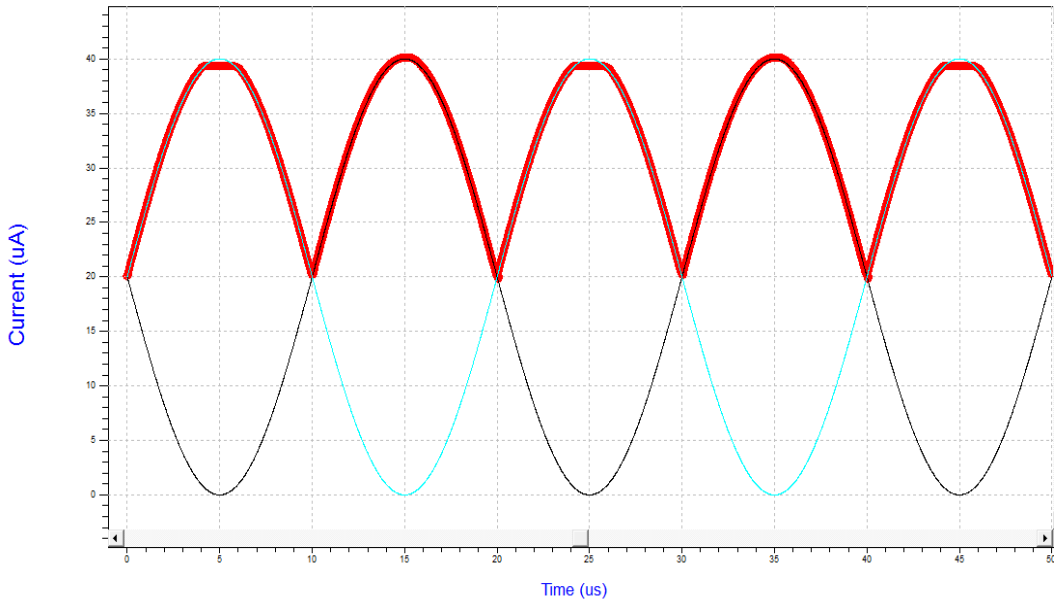

Figure 5.9: Output of proposed full wave rectifier

5.3.3 WTA/LTA as Modulus Circuit

The output is obtained by applying two different input sinusoidal waveforms of frequencies 50 kHz and 100 kHz shown in Figures 5.10 and 5.11 shows the output waveform of the modulus circuit at every instant of time when both the input currents are applied.

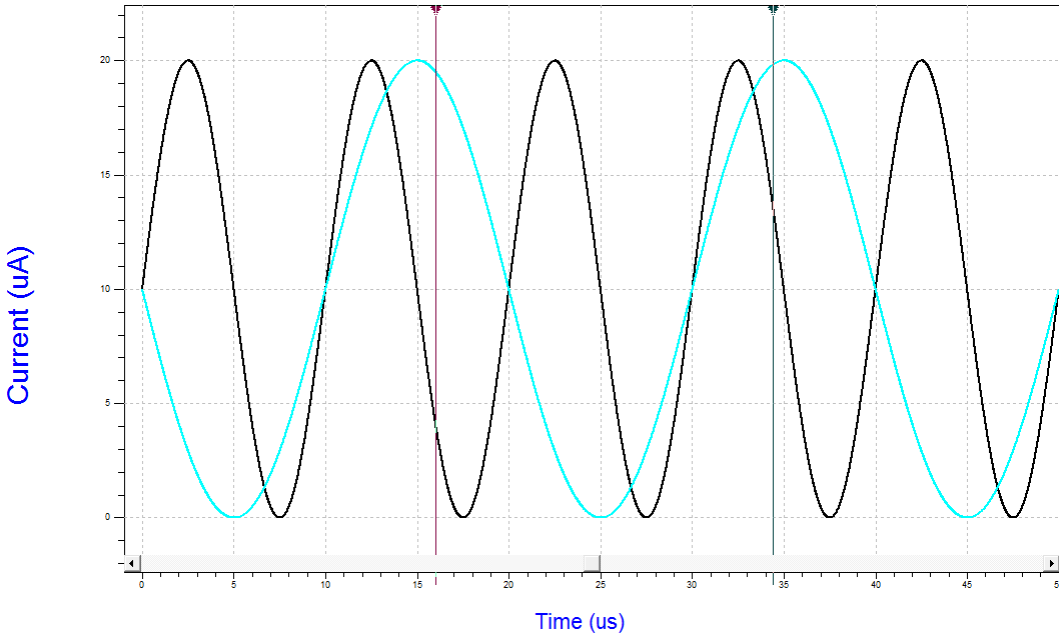

Figure 5.10 Input waveforms of proposed modulus circuit

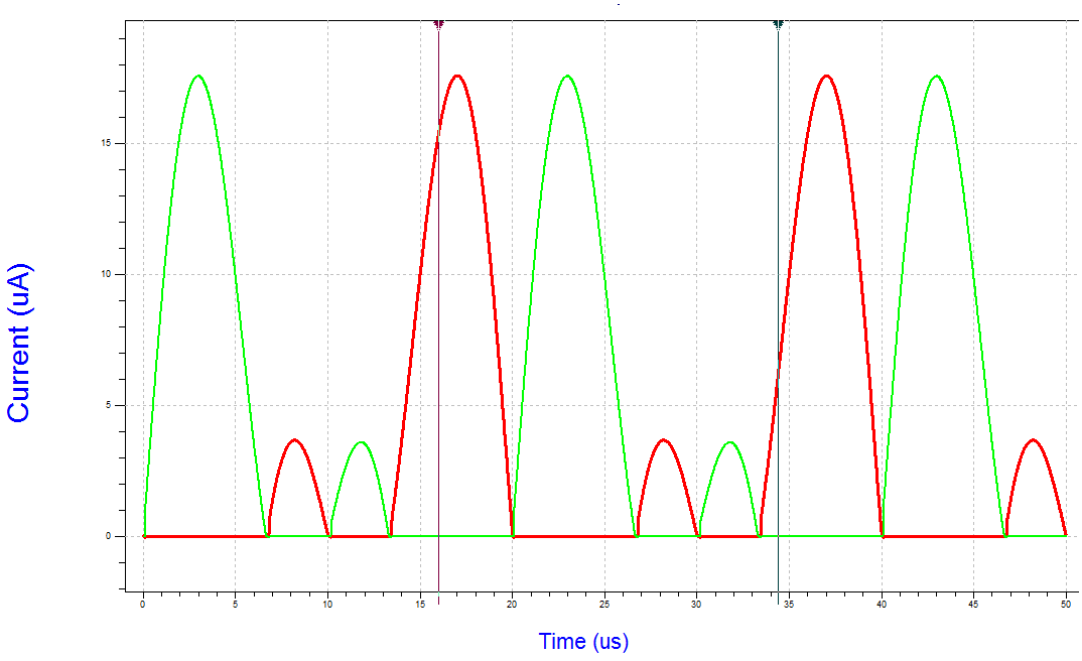

Figure 5.11: Output waveform of proposed modulus circuit

Table 5.1 shows comparison among different implementations presented earlier with the proposed WTA/LTA circuit on various parameters

Table 5.1. Comparison of proposed WTA/LTA circuit with other WTA/LTA circuits reported in literature

Name of Author	Technology	Minimum Difference	Voltage Supply	Error percentage	Operation Capability
Lazzaro et al.[7]	2.0um	2uA	5 V	2%	Maximum
Opris [2]	2.0um	N.A.	5 V	N.A.	Maximum and Minimum
Serrano et al.[8]	2.0um	N.A.	2.5 V	1.5%	Maximum
Demosthenous [16]	2.4um	N.A.	5 V	1%	Maximum
Fish et al. [9]	0.35um	60nA	3.3V	0.8%	Maximum
Mesgarzadeh [10]	0.35um	100nA	1.5V	>1%	Maximum and minimum
Alikhani et al. [13]	0.25um	600nA	2.5V	0.6%	Maximum /Minimum
Ghanavati et al. [28]	0.35μm	N.A.	1.5V	N.A.	Maximum and minimum
Proposed circuit	0.18um	47nA	1.1V	0.03%	Maximum /Minimum

From the Table 5.1, it is observed that the proposed WTA/LTA circuit has highest precision amoung the circuits discussed and lower supply voltage requirement than the WTA/LTA circuits available in literature.

The dimensions of the proposed circuit are listed in Table 5.2. Proposed WTA/LTA Circuit is simulated using TSMC 0.18um CMOS technology.

Table 5.2 Transistor sizing of proposed ciruit

TRANSISTOR NAME	WIDTH(um)	LENGTH(um)
M_1	.80	2
M_2	10	.20
M_3	.75	.70
M_4,M_5,M_6,M_7,M_8,M_9	.60	.60
M_{10},M_{11},M_{12},M_{13},M_{14}	.75	.70
M_{15}	4	.20
$M_{16,}$ M_{17}	.84	.60

CHAPTER 6

CONCLUSION AND FUTURE SCOPE

6.1 Conclusion

In this thesis the WTA/LTA circuit based on high swing cascade current and its applications have been proposed. The circuit has with several advantages of improved precision, low supply voltage requirement which makes it suitable for low voltage applications like neural network, signal processing, and communication systems, moreover error has been reduced to great extend 45nA. This circuit has been tested with various inputs at various frequencies and input current level. This circuit has been implemented on 0.18um technology at TSPICE. The result obtained has been compared with previous implementations.

6.2 Future Scope

Some suggestion and ideas that can extend this work in future.

- The circuit could be extended to multiple layered inputs by using Binary tree approach.
- Furthermore, the local feedback can be used for improving the precision of circuit.
- It is also highly desirable to avoid corner errors at high frequencies, an improvement in these errors could produce remarkable results.

REFERENCES

[1] J. Lazzaro, S. Ryckebusch, , M. A. Mahowald and C. A. Mead "Winner-take-all network of O(n) complexity, *"Advances in neural information processing systems* 1," pp. 703-711(1989)

[2] D. Janeem, W. Anderson, A. Carver Mead, Timothy Allen, M. F. Wall US 5146106 A(1992) CMOS winner-take all circuit with offset adaptation.

[3] I. E. Opris," Rail-to-Rail Multiple-Input Min/Max circuit," *IEEE Trans. on circuits on circuits and system-II, Analog and Digital Signal Processing,"* vol.45(1), pp.137-140(1998)

[4] R. Angulo, J. Ducoudray Acevedo, G. Carvajal and Lopez-Martin, "Low-voltage high-performance voltage- mode and current-mode WTA circuits based on flipped voltage followers," *IEEE Transactions on Circuits and Systems II:Express Briefs*, vol. 52, pp. 420–423, 2005.

[5] P. Prommee and K. Chattrakun, "CMOS WTA maximum and minimum circuits with their applications to analog switch and rectifiers," *Microelectronics Journal*, vol. 42, pp. 52–62, 2011.

[6] R. G. Carvajal, J. Ramırez-Angulo, A. Lopez-Martin, A. Torralba, J. Galan, A. Arlosena and F. Munoz, "The flipped voltage follower: A useful cell for low voltage low power circuit design," *IEEE Transactions Circuits Systems* I, vol. 52, pp. 1276-1291, 2005.

[7] S. KazemiNia, A. Khoei, K. Hadidi, "High Speed High Precision Voltage Mode MAX and MIN Circuits," *Journal of circuits, systems and computer*(JCSC), vol. 16(2), pp. 233-244, 2007.

[8] T. Serrano and B. Linares Barranco, "A modular current-mode high-precision winner-take-all circuit." *IEEE Transactions on Circuits and Systems II,* vol.42(2), pp. 132–134, 1998.

[9] A. Fish, D. Akselrod and O. Yadid pecht, "High Precision Image Centroid Computation via an Adaptive K-Winner-Take-all Circuit in Conjunction with a Dynamic Element Matching Algorithm for Star Tracking Applications," *Analog Integrated Circuits and Signal Processing*, vol. 39, pp. 251–266, 2003.

[10] B. Mesgarzadeh, "A CMOS Implementation of Current-Mode Min-Max Circuits and A Sample Fuzzy Application," *Fuzzy Systems,* vol. 2, pp. 941-946, *2004.*

[11] A. Peymanfar, A. Khoei, and K. Hadidi, " Design of a general propose neuro-fuzzy controller by using modified adaptive-network-based fuzzy inference system,." *International Journal of Electronic and Communications (AEU˙*), vol. 6, pp. 433–442, 2009.

[12] G. Yosefi, S. Aminifar, S. Neda and Daneshwar, "Design of a mixed-signal digital CMOS fuzzy logic controller (FLC) chip using new current mode circuits*," Communications & Signal Processing, 2007 6th International Conference on Information,* pp. 1-5, 2007.

[13] A. Alikhani , A. Ahmadi, "A novel current-mode min–max circuit" *Analog Integrated Circuits and Signal Processings*, vol. 72, pp. 343–350, 2012.

[14] K. P. Abdulla and M. F. Azeem, "A CMOS Current Mode implementation of Multiple Input Fuzzy MIN and MAX Circuits for Analog Fuzzy Processors," *International Journal of Scientific & Engineering Research,* vol 4(4), pp. 133-161, 2013.

[15] M. Rahman, K. L. Baishnab and F. A. Talukdar, "A High Speed and High Resolution VLSI Winner Take-All Circuit for Neural Networks and Fuzzy Systems," *International Symposium on Signals, Circuits and Systems,*pp. 1-4, 2009.

[16] A. Demosthenous, S. Smedley, and J. Taylor, "A CMOS analog winner take-all network for large-scale applications," *IEEE Trans. Circuits System I*, vol. 45, no. 3, pp. 300–304, 1998.

[17] R.G. Carvajal, Torralba, A. Millan, R. and Franquelo, L.G, "Automatic synthesis of analog and mixed-signal fuzzy controllers with emphasis in power consumption," *Proc. IEEE Int. Symp. Circuits and Systems ISCAS*, vol. 5, pp. 571-574, 1999.

[18] P. Prommee, K. Angkeaw, , Somdunyakanok, M and Dejhan, K, "CMOS based near zero-offset multiple inputs max–min circuits and its applications,"*Analog Integrated Circuit and Signal Processing ,vol* 61, pp. 93–105, 2009.

[19] P. H. Siqueira, M. Teresinha Arns Steiner and Sergio Scheer, "recurrent neural network with soft 'winner takes all' principle for the TSP," *Proceedings of the International Conference on Fuzzy Computation and International Conference on Neural Computation*," pp. 265-270, 2010.

[20] M. H. Moaiyeri, R. Chavoshisani, A. J. Keivan and N. Omid-ashemipour, "High-Performance Mixed-Mode Universal Min-Max Circuits for Nanotechnology," *Circuits System Signal Process*, vol. 31, pp. 465–488, 2012.

[21] S. Lin, Y. B. Kim and F. Lombardi, "A novel CNFET based ternary logic gate design, " Proc. *IEEE International Midwest Symposium on Circuits and Systems*," pp. 435–438, 2012.

[22] M. Gupta, B. Aggarwal, A. K. Gupta, "A very high performance self-biased cascode current mirror for CMOS technology," *Analog Integrated Circuit Signal Processing,* vol. 75, pp.67-74, 2013.

[23] B. Razavi, Design of Analog CMOS Integrated Circuits, second edition, Tata Mc Graw Hill, New Delhi, 2002.

[24] N. H. E. Weste, D. Harris, A. Banerjee, CMOS VLSI Design A Circuits and Systems Perspective, third edition, Dorling Kindersley India for Pearson Education South Asia, 2006

[25] R. G. Carvajal, A. R. Angulo, and J. M. Heredia," High-Speed High-Precision Min/Max Circuits in CMOS Technology," *IEE Electronic Lett*ers vol. 36, pp. 697-699, 2000.

[26] S. Vlassis, K. Doris, S. Siskos, "Analog Implementation of Erosion/Dilation, median and Order Statistics Filters", *IEEE,* 1999.

[27] R. Dlugosz and T. Talkas, "A low power current-mode binary-tree WTA / LTA circuit for Kohonen neural networks," *Mixed Design of Integrated Circuits & Systems, MIXDES '09,* 2009.

[28] B. Ghanavati and E. Taghavi Moghaddam, "Low-Voltage Current-Mode WTA/LTA Circuit," *Universal Journal of Electrical and Electronic Engineering* vol.2(4), pp. 161-164, 2014.

[29] Y. C. Hung, B. D. Liu and C. Y. Tsai "1-V bulk-driven CMOS analog programmable winner-takes-all circuit," *Analog Integrated Circuits and Signal Processing,* vol 49(1), pp. 53-61.

APPENDIX A

MODEL FILE USED FOR PMOS TRANSISTOR

LEVEL= 53 TNOM = 27 TOX = 4.1E-9

+XJ = 1E-7 NCH = 4.1589E17 VTH0 = -0.3948389

+K1 = 0.5763529 K2 = 0.0289236 K3 = 0

+K3B = 13.8420955 W0 = 1E-6 NLX = 1.337719E-7

+DVT0W = 0 DVT1W = 0 DVT2W = 0

+DVT0 = 0.5281977 DVT1 = 0.2185978 DVT2 = 0.1

+U0 = 109.9762536 UA = 1.325075E-9 UB = 1.577494E-21

+UC = -1E-10 VSAT = 1.910164E5 A0 = 1.7233027

+AGS = 0.3631032 B0 = 2.336565E-7 B1 = 5.517259E-7

+KETA = 0.0217218 A1 = 0.3935816 A2 = 0.401311

+RDSW = 252.7123939 PRWG = 0.5 PRWB = 0.0158894

+WR = 1 WINT = 0 LINT = 2.718137E-8

+XL = 0 XW = -1E-8 DWG = -4.363993E-8

+DWB = 8.876273E-10 VOFF = -0.0942201 NFACTOR = 2

+CIT = 0 CDSC = 2.4E-4 CDSCD = 0

+CDSCB = 0 ETA0 = 0.2091053 ETAB = -0.1097233

+DSUB = 1.2513945 PCLM = 2.1999615 PDIBLC1 = 1.238047E-3

+PDIBLC2 = 0.0402861 PDIBLCB = -1E-3 DROUT = 0

+PSCBE1 = 1.034924E10 PSCBE2 = 2.991339E-9 PVAG = 15

+DELTA = 0.01 RSH = 7.5 MOBMOD = 1

+PRT = 0 UTE = -1.5 KT1 = -0.11

+KT1L = 0 KT2 = 0.022 UA1 = 4.31E-9

+UB1 = -7.61E-18 UC1 = -5.6E-11 AT = 3.3E4

+WL = 0 WLN = 1 WW = 0

+WWN = 1 WWL = 0 LL = 0

+LLN = 1 LW = 0 LWN = 1

+LWL = 0 CAPMOD = 2 XPART = 0.5

+CGDO = 6.28E-10 CGSO = 6.28E-10 CGBO = 1E-12

+CJ = 1.160855E-3 PB = 0.8484374 MJ = 0.4079216

+CJSW = 2.306564E-10 PBSW = 0.842712 MJSW = 0.3673317

+CJSWG = 4.22E-10 PBSWG = 0.842712 MJSWG = 0.3673317

+CF = 0 PVTH0 = 2.619929E-3 PRDSW = 1.0634509

+PK2 = 1.940657E-3 WKETA = 0.0355444 LKETA = -3.037019E-3

+PU0 = -1.0227548 PUA = -4.36707E-11 PUB = 1E-21

+PVSAT = -50 PETA0 = 1E-4 PKETA = -5.16

MODEL PARAMETERS USED FOR NMOS TRANSISTOR

LEVEL= 53 TNOM = 27 TOX = 4.1E-9

+XJ = 1E-7 NCH = 2.3549E17 VTH0 = 0.3725327

+K1 = 0.5933684 K2 = 2.050755E-3 K3 = 1E-3

+K3B = 4.5116437 W0 = 1E-7 NLX = 1.870758E-7

+DVT0W = 0 DVT1W = 0 DVT2W = 0

+DVT0 = 1.3621338 DVT1 = 0.3845146 DVT2 = 0.0577255

+U0 = 259.5304169 UA = -1.413292E-9 UB = 2.229959E-18

+UC = 4.525942E-11 VSAT = 9.411671E4 A0 = 1.7572867

+AGS = 0.3740333 B0 = -7.087476E-9 B1 = -1E-7

+KETA = -4.331915E-3 A1 = 0 A2 = 1

+RDSW = 111.886044 PRWG = 0.5 PRWB = -0.2

+WR = 1 WINT = 0 LINT = 1.701524E-8

+XL = 0 XW = -1E-8 DWG = -1.365589E-8

+DWB = 1.045599E-8 VOFF = -0.0927546 NFACTOR = 2.4494296

+CIT = 0 CDSC = 2.4E-4 CDSCD = 0

+CDSCB = 0 ETA0 = 3.175457E-3 ETAB = 3.494694E-5

+DSUB = 0.0175288 PCLM = 0.7273497 PDIBLC1 = 0.1886574

+PDIBLC2 = 2.617136E-3 PDIBLCB = -0.1 DROUT = 0.7779462

+PSCBE1 = 3.488238E10 PSCBE2 = 6.841553E-10 PVAG = 0.0162206

+DELTA = 0.01 RSH = 6.5 MOBMOD = 1

+PRT = 0 UTE = -1.5 KT1 = -0.11

+KT1L = 0 KT2 = 0.022 UA1 = 4.31E-9

+UB1 = -7.61E-18 UC1 = -5.6E-11 AT = 3.3E4

+WL = 0 WLN = 1 WW = 0

+WWN = 1 WWL = 0 LL = 0

+LLN = 1 LW = 0 LWN = 1

+LWL = 0 CAPMOD = 2 XPART = 0.5

+CGDO = 8.53E-10 CGSO = 8.53E-10 CGBO = 1E-12

+CJ = 9.513993E-4 PB = 0.8 MJ = 0.3773625

+CJSW = 2.600853E-10 PBSW = 0.8157101 MJSW = 0.1004233

+CJSWG = 3.3E-10 PBSWG = 0.8157101 MJSWG = 0.1004233

+CF = 0 PVTH0 = -8.863347E-4 PRDSW = -3.6877287

+PK2 = 3.730349E-4 WKETA = 6.284186E-3 LKETA = -0.0106193

+PU0 = 16.6114107 PUA = 6.572846E-11 PUB = 0

+PVSAT = 1.112243E3 PETA0 = 1.002968E-4 PKETA = -2.906037E-3

LIST OF PUBLICATIONS

[1] Sahib Singh and Rishikesh Pandey, "Low voltage high WTA/LTA circuit and its application" *Analog integrated circuit signal processings (AICSP)*, communicated