A Highly Linear Floating Gate MOSFET based Source-Degenerated OTA and Its Applications in Realizing Inductor, Tunable Resistors and Filters for Signal Processing

Dissertation submitted in partial fulfilment of the requirements
for the award of degree of

Master of Technology

in

VLSI Design

Submitted By

Tanmay Dubey
Roll No. 601261030

Under guidance of

Dr. Rishikesh Pandey
Assistant Professor, ECED
Thapar University
Patiala

Electronics and Communication Engineering Department
THAPAR UNIVERSITY
(Established under the section 3 of UGC Act, 1956)
PATIALA-147004 (PUNJAB)

JULY, 2014

DECLARATION

I hereby declare that the work which is presented in the dissertation entitled, **"A Highly Linear Floating Gate MOSFET based Source-Degenerated OTA and Its Applications in Realizing Inductor, Tunable Resistors and Filters for Signal Processing"** in partial fulfilment of the requirement for the award of degree of Master of Technology in VLSI Design submitted in Electronics and Communication Engineering Department of Thapar University, Patiala, is an authentic record of my own work carried out under the supervision of Dr. Rishikesh Pandey, Assistant Professor, ECED and refers other researcher's work which are duly listed in the reference section.

The matter presented in this dissertation has not been submitted in any other University/Institute for the award of degree.

Tanmay Dubey

Date: 01/07/2014

Tanmay Dubey
Roll No: 601261030

It is certified that the above statement made by the student is correct to the best of my knowledge and belief.

01/07/2014

Dr. Rishikesh Pandey
Assistant Professor
ECED, Thapar University

Countersigned by:

Head
ECED, Thapar University
Patiala- 147004

Dean of Academic Affairs
Thapar University
Patiala- 147004

ACKNOWLEDGMENT

First of all, I would like to express my gratitude to **Dr. Rishikesh Pandey, Assistant Professor**, Electronics and Communication Engineering Department, Thapar University, Patiala for his patient guidance and support throughout my work. I am truly very fortunate to have the opportunity to work with him. I found his guidance to be extremely valuable.

I am also thankful to **Head of Department, Professor (Dr.) Sanjay Sharma** and **PG coordinator, Associate Professor (Dr.) Kulbir Singh** of Electronics and Communication Engineering Department for their encouragement and inspiration for the execution of this thesis work. I would also like to thank my friends who devoted their valuable time and helped me in all possible ways towards successful completion of this work. I thank all those who have contributed directly or indirectly to this work.

Lastly, I would like to thank my parents for their unconditional support and encouragement.

Tanmay Dubey

Roll No: 601261030

ABSTRACT

In the last few years, portable electronic devices such as mobiles, tablets, laptops etc. are become an essential part of human life. All these devices are operated with the help of battery and portability of these devices is dependent on the battery life. The battery life and hence the portability of the device can be increased by design such integrated circuits which can operate with low voltage supply. The low voltage operation can be achieved by using floating gate MOSFETs because of their great potential for low voltage design and compatibility with CMOS process technology.

This dissertation proposes a highly linear floating gate MOSFET based source-degenerated OTA designed using UMC 0.18μm process technology parameters. The low voltage operation of the proposed OTA is achieved by using floating gate MOSFETs as input transistors and the linearity of the OTA is increased by using source-degeneration linearization technique. The designed OTA operates with ±0.6V power supply and has rail-to-rail input differential voltage range. The physical layout of the proposed OTA is designed using Cadence Virtuoso XL layout editor tool using UMC 0.18μm process technology. Some applications of the proposed OTA such as active inductor, tunable resistors and filters are developed. The performance parameters of the designed OTA is compared with the existing OTAs available in literature and the comparison shows that the proposed OTA has better input differential voltage range with low power supply requirement.

TABLE OF CONTENTS

LIST OF FIGURES

LIST OF TABLES

LIST OF SYMBOLS

I_D	Drain Current
K	Transconductance Parameter
V_T	Threshold Voltage
V_{DS}	Drain-to-Source Voltage
V_{BS}	Bulk-to-Source Voltage
μ	Mobility of Carriers
W	Channel Width
L	Channel Length
C_{GD}	Parasitic Capacitance between Floating Gate and Drain
C_{GS}	Parasitic Capacitance between Floating Gate and Source
C_{GB}	Capacitance between Floating Gate and Substrate
V	Voltage
G_m	Transconductance Gain
M	MOSFET
V_{in}	Input Voltage
I_{out}	Output Current
I_B	Bias Current
R	Resistance
L_{eq}	Equivalent Inductance
C	Capacitance

LIST OF ABBRIEATIONS

MOSFET	Metal Oxide Semiconductor Field Effect Transistor
VLSI	Very Large Scale Integrated Circuit
SNR	Signal to Noise Ratio
CMOS	Complementary Metal Oxide Semiconductor
OTA	Operational Transconductance Amplifier
EPROM	Erasable Programmable Read Only Memory
EEPROM	Electrically Erasable Programmable Read Only Memory
UMC	United Microelectronics Corporation
THD	Total Harmonic Distortion
FVF	Flipped Voltage Follower
QFG	Quasi Floating Gate
NAF	Neuron Activation Function
DRC	Design Rule Check
LVS	Layout Vs. Schematic

CHAPTER

INTRODUCTION

1.1 INTRODUCTION

In the last few decades, a lot of evolution had been occurred in the technology. Firstly, the large vacuum tubes were replaced by bipolar transistors which were further replaced by small sized MOS transistors which allowed the manufacturers to place large number of transistors in a single chip. As the size of transistors reduced further, the number of transistors in a single chip was increased from few hundreds to millions of transistors per chip. But, the increased numbers of transistors in a single integrated circuit also increase the total power consumption of the circuit. So, the obligation towards the lower supply voltage and smaller power consumption has been increased. The miniaturization of the circuits has made it a necessity that they consume smallest possible amount of voltage and power. The low voltage/ low power circuits have become unavoidable as the increased number of components per chip area and decreased channel length [1]. In the last two decades, the devices such as mobiles, laptops, smart phones have become an important part of daily life, the technology is evolving at a very fast rate and with this the demand of low power low voltage circuits has also inflated. The battery operated operation of all these devices has made it urgent to produce circuits which consume smallest amount of supply voltage and current. The smaller the supply voltage or current consumption the more will be the life of the battery and so the portability of the devices.

In VLSI circuits, the digital and analog circuits can be integrated together as the number of transistors integrated on a single chip increases. This also results in the reduced production cost [2]. The digital circuits have the advantage over the analog circuits because of their smaller production cost and faster speed, but on the other side the analog circuits have their own importance as an inevitable interface between the digital and

physical world. Eventually the design of analog circuits sets the platform for the performance of the digital technology.

1.2 MOTIVATION

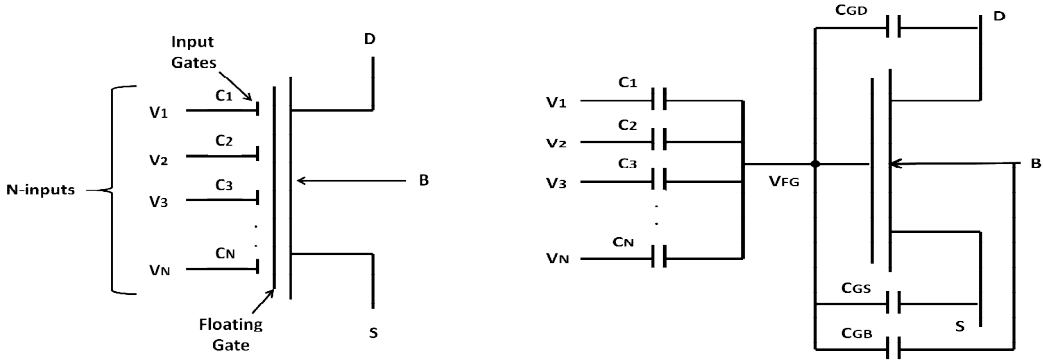
In recent years, with miniaturization of technology, the demand of low power low voltage supply has become essential [3]. For designing of analog circuits, it has become the major factor that they operate with low supply voltage and power as their digital counterparts. Analog designers face many difficulties and challenges due to the limited voltage headroom, because the threshold voltage and drain-to-source saturation voltage of CMOS technologies do not scale down at the same rate as the supply voltage or do not scale at all with low supply voltage. The power supply requirement of analog circuits can be reduced by two techniques known as technology modification and transistor implementation [4]. Using technology modification technique, the device technology dependent threshold voltage can be reduced. But, higher threshold voltage gives better noise immunity and the lower threshold voltage reduces the noise margin to result in poor signal to noise ratio (SNR). Hence, for present day CMOS technology, reduction in threshold voltage is limited to the noise floor level, below which further reduction will introduce an amount of noise sufficient to result in very complex circuits.

Some of the transistor implementation techniques available in literature are level shifters, self-cascode MOSFETs, sub-threshold MOSFETs, bulk-driven MOSFETs and floating gate MOSFETs [5-7], etc. Out of these floating gate MOSFETs present a unique advantage of programmability of threshold voltage, which can be lowered from its conventional value, thus makes it suitable for low voltage applications [8-10]. Motivated by the unique characteristics of the floating gate MOSFETs, a highly linear OTA is proposed. The OTA is a versatile building block employed as the active cell in many analog integrated circuits such as continuous-time filters [11-14], variable gain amplifiers [15-17] and current sensing circuits [18-19].

1.3 OPERATION OF FLOATING GATE MOSFET

The structure of floating gate MOSFET is similar to a conventional MOSFET. The difference between these two is the gate which is electronically isolated, creating a floating node in DC, and a number of secondary gates electrically isolated from the floating gate, above which they are deposited. There exist only capacitive connection

between inputs and floating gate [20]. The floating gate which is completely surrounded by highly resistive material serves as charge storage device. Therefore, the first application of the floating gate MOSFET was to store the digital information for very long period, in structures such as EPROMs, EEPROMs and Flash memories [21-22]. Along with this, floating gate MOSFET devices show easy addition and compression of voltage signals, as well as allow a reduction of the effective threshold voltage. The threshold voltage of a floating gate transistor can be controlled by the amount of the static charge stored in the floating gate. This property has prompted their use in low voltage low power analog circuits [23]. The symbol and equivalent circuit model of N-input floating gate MOSFET are shown in Figs. 1.1 (a) and (b) respectively. In both the figures, V_i (for i=1, 2,…, N) are the control input voltages and D, S and B are the drain, source and substrate, respectively.



(a) (b)

Fig. 1.1 Floating gate MOSFET: (a) Symbol (b) Equivalent circuit diagram [10]

The drain current I_D of n-type N-input floating gate MOSFET in saturation region is given as [24, 25]:

$$I_D = \frac{K_n}{2}\left\{\frac{\sum_{i=1}^{N} C_i V_{iS}}{C_T} + \frac{C_{GD}}{C_T}V_{DS} + \frac{C_{GB}}{C_T}V_{BS} - V_T\right\}^2 \quad (1.1)$$

where $K_n=\mu_n C_{ox}(W/L)$ is the transconductance parameter, $\sum_{i=1}^{N} C_i$ is the sum of the N-input capacitances, V_{iS} is the input voltage at the i^{th} input gate with respect to source, V_{DS} is the drain-to-source voltage, V_{BS} is the substrate-to-source voltage, V_T is the threshold voltage, C_T ($=\sum_{i=1}^{N} C_i + C_{GD} + C_{GS} + C_{GB}$) is the total capacitance seen by the floating-gate, C_{GD} is the parasitic capacitance between floating-gate and

drain, C_{GS} is the parasitic capacitance between floating-gate and source, and C_{GB} is the capacitance between floating-gate and substrate.

1.4 KEY CONTRIBUTION

The work in this dissertation can be summarized as bellow.

1. Design and simulate a highly linear floating gate based source-degenerated OTA.
2. Investigating the application of floating gate MOSFET based source-degenerated OTA as active inductor.
3. Design and simulate tunable resistors and filters as applications of proposed floating gate MOSFET based source-degenerated OTA.

In the dissertation, a highly linear floating gate MOSFET based source-degenerated OTA with rail-to-rail input voltage range is proposed. The proposed circuit is used to develop some of the applications such as active inductor, tunable resistors, and Gm-C filters. All the proposed circuits have been simulated using UMC 0.18μm CMOS process technology parameters and the simulation results are presented. The performance parameters of the circuits have also been compared with the existing OTAs available in literature. The comparison shows that the proposed OTA has wide input voltage range and low power supply voltage requirement.

1.5 ORGANIZATION OF THE THESIS

In this section, each chapter of the dissertation is discussed in brief. The second chapter gives the overview of the Operational Transconductance Amplifier. The numerous methodologies for designing the linear OTA available in literature are discussed in third chapter. In fourth chapter, floating gate MOSFET based source-degenerated OTA and its applications such as active inductor, tunable resistors and filters are proposed. The simulation results and layout of the proposed OTA are presented in fifth chapter. The sixth chapter summarizes the dissertation and suggest the future scope of the work.

CHAPTER

OPERATIONAL TRANSCONDUCTANCE AMPLIFIER

2.1 INTRODUCTION

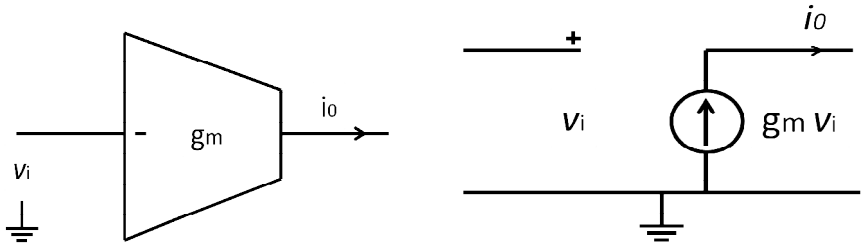
The transconductor or Operational Transconductance Amplifier (OTA) is used as a basic building block to design various analog integrated circuits such as continuous-time filters [11-14], variable gain amplifiers [15-17], current sensing circuits [18-19], etc. This chapter is organized as follows. A brief overview of operational transconductance amplifier is presented in section 2.2. Different types of OTAs based on their input-output configuration are also discussed in this section. The chapter is concluded in section 2.3.

2.2 OVERVIEW OF OPERATIONAL TRANSCONDUCTANCE AMPIFIER

The operational transconductance amplifier is different from conventional operational amplifier (Op-amp) in various aspects. One of the differences between OTA and Op-amp is the type of output. In OTA, the output is in the form of current but in Op-amp, the output is in voltage form. A simple two transistor differential amplifier is used as the input stage for both OTA and Op-amp but in OTA there is no use of capacitors and resistors as in Op-amp. OTA is generally used as open loop that is without negative feedback in linear applications. The output voltage of the OTA is controlled by the resistor connected to its output terminal. In OTA, the input differential voltage is converted to the current at the output terminal so it is also known as Voltage-to-Current convertor (V-I convertor). The OTAs are classified into four different types based on their input and output configurations as following:

2.2.1 SINGLE INPUT-SINGLE OUTPUT

In Single Input-Single Output OTA, there is only one input terminal and one output terminal. The symbolic representation and equivalent circuit diagram of this type of OTA are shown in Figs. 2.1 (a) and (b) respectively [19].



(a) (b)

Figs. 2.1 Single input-Single output OTA: (a) Symbol
(b) Equivalent circuit diagram [19]

The relation between input voltage and output current of Single input-Single output OTA is given as

$$i_0 = g_m v_i \tag{2.1}$$

where g_m is the transconductance, v_i is the input voltage and i_0 is the output current.

Fig 2.2 shows a Single Input-Single Output OTA [26]. In the circuit, two composite transistors formed by transistors M_1, M_2 and M_3, M_4 are used to design a Single Input-Single Output OTA. The input voltage V_{in} is applied on the gate terminals of transistors M_2 and M_3. The output current (I_{out}) is the difference of the drain currents I_{D1} and I_{D2} of the two composite transistors.

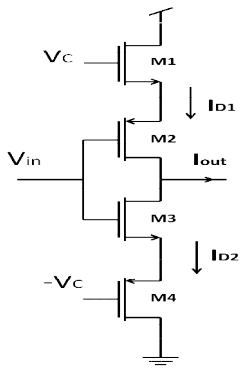


Fig. 2.2 Single Input-Single Output OTA [26]

The output current (I_{out}) of Single-Input Single-Output OTA is given as

$$I_{out} = I_{D1} - I_{D2} = 2K_{eq}(V_C - V_{Teq})V_{in} \quad (2.2)$$

where V_{in} is the input voltage, V_C is the control voltage, $K_{eq} = \sqrt{\frac{K_1 K_2}{K_1 + K_2}}$ and $V_{Teq} = V_{Tn} + |V_{Tp}|$ are the equivalent transconductance parameter and threshold voltage of composite transistors respectively, V_{Tn} and V_{Tp} are the threshold voltages of the NMOS and PMOS transistors respectively and K_1, K_2 are the transconductance parameter of M_1 and M_2 respectively.

Eq. (2.2) can be written as

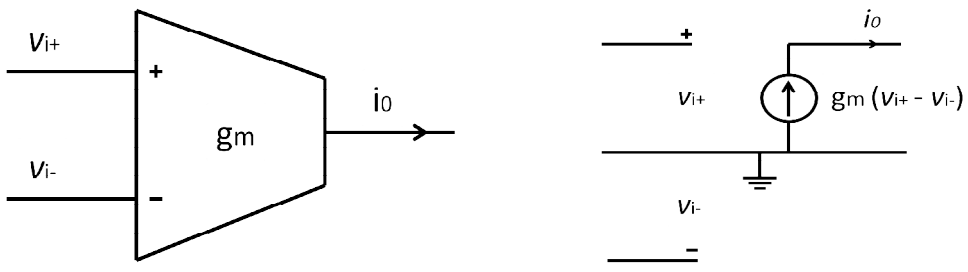
$$I_{out} = G_m V_{in} \quad (2.3)$$

where G_m $(= 2K_{eq}(V_C - V_{Teq})$ is the transconductance of Single-Input Single-Output OTA.

From Eqs. (2.2) and (2.3), it can be seen that the output current is linear function of the input voltage V_{in} and the equivalent transconductance is controlled by the control voltage.

2.2.2 DIFFERENTIAL INPUT-SINGLE OUTPUT

In Differential Input-Single Output OTA, the input voltage is given in differential form but the output is taken from only single node. The symbolic representation and the equivalent circuit diagram of this type of OTA are shown in Figs. 2.3 (a) and (b) respectively [19].



Figs. 2.3 Differential Input-Single Output OTA: (a) Symbol
(b) Equivalent circuit diagram [19]

The input-output relationship of Differential Input-Single Output OTA is given as

$$i_0 = g_m v_{in} \tag{2.4}$$

where g_m is the transconductance, $v_{in} = v_{i+} - v_{i-}$ is the input voltage and i_0 is the output current.

A Differential Input-Single Output OTA is shown in Fig. 2.4 [19]. In this circuit, a source-coupled differential-pair input stage is used, which can provide high input impedance, high gain, and high common-mode rejection.

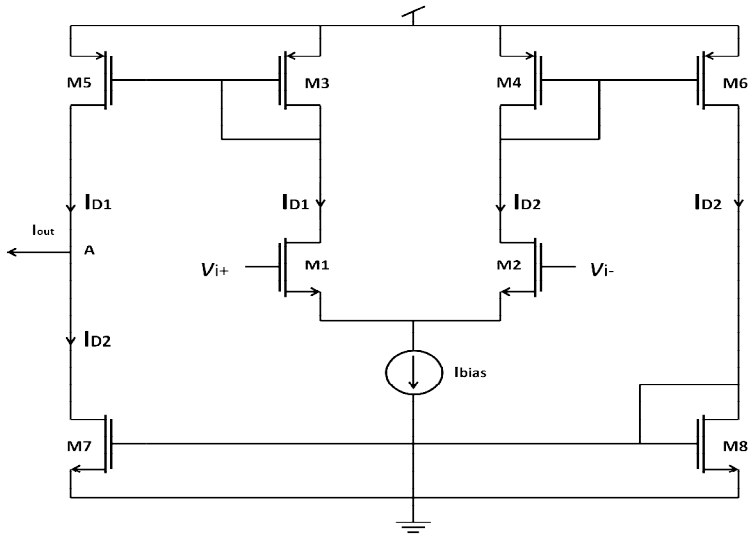


Fig. 2.4 Differential Input-Single Output OTA [25]

The input is given at the gate terminals of the input differential pair formed by the transistor M_1 and M_2. The output is the difference of the drain currents I_{D1} and I_{D2} of the input transistors M_1 and M_2 respectively. The two pairs of PMOS current mirrors formed by transistors M_3, M_5 and M_4, M_6 and one NMOS current mirror formed by transistors M_7, M_8 is used to transfer the drain currents I_{D1} and I_{D2} to the output node A. The output current (I_{out}) of the Differential Input-Single Output OTA is given as

$$I_{out} = I_{D1} - I_{D2} = \sqrt{I_{bias} K}\, V_{in} \sqrt{1 - \frac{V_{in}^2}{4I_{bias}/K}} \tag{2.5}$$

where $V_{in} = V_{i+} - V_{i-}$ is the differential input voltage, K is the transconductance parameter and I_{bias} is the bias current.

Eq. (2.5) can be written as

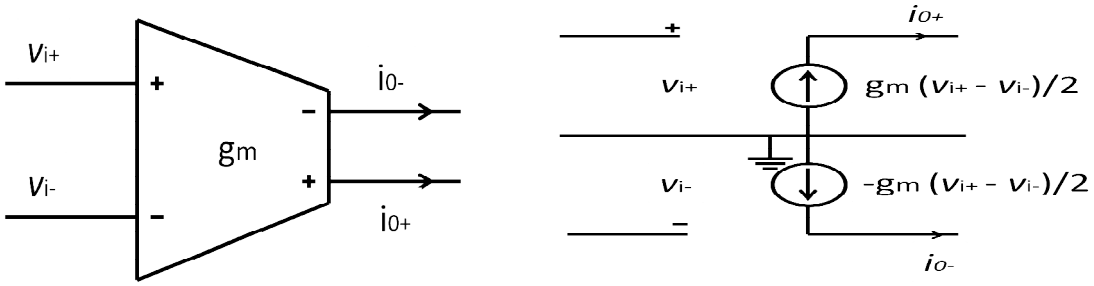
$$I_{out} = G_m V_{in} \tag{2.6}$$

where G_m ($=\sqrt{I_{bias}K}$) is the transconductance of Differential Input-Single Output OTA.

From Eqs. (2.5) and (2.6), it can be seen that the output current is linear function of the input voltage V_{in} and the equivalent transconductance is controlled by the bias current.

2.2.3 DIFFERENTIAL INPUT-DIFFERENTIAL OUTPUT

In Differential Input-Differential Output OTA, the input voltage is given differentially as in Differential Input-Single Output type of OTA but the output is taken in differential manner. The symbolic representation and equivalent circuit diagram of Differential Input-Differential Output OTA are shown in Figs. 2.5 (a) and (b) respectively [19].



(a) (b)

Figs. 2.5 Differential Input-Differential output OTA: (a) Symbol
(b) Equivalent circuit diagram [19]

The relationship between input and output of Differential Input-Differential Output OTA is given as

$$i_0 = i_{0+} - i_{0-} = g_m v_{in} \tag{2.7}$$

where g_m is the transconductance, $v_{in} = v_{i+} - v_{i-}$ is the input voltage and i_0 is the output current.

Fig. 2.6 shows a Differential Input-Differential Output OTA.

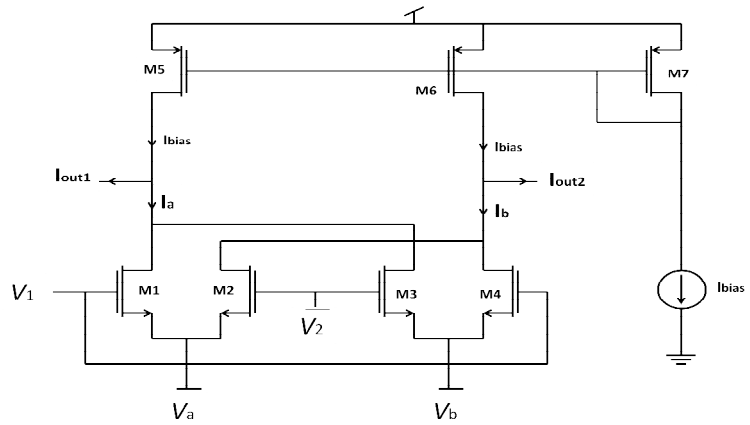


Fig. 2.6 Differential Input-Differential Output OTA [27]

The output current (I_{out}) of OTA is given as

$$I_{out} = K(V_b - V_a)V_{in} \tag{2.8}$$

where $V_{in} = V_1 - V_2$ is the differential input voltage, V_a and V_b are the voltages at the sources of M_1 and M_3 respectively and , K is the transconductance parameter.

Eq. (2.8) can be written as

$$I_{out} = G_m V_{in} \tag{2.9}$$

where G_m $(= K(V_b\text{-}V_a))$ is the transconductance of Differential Input-Differential Output OTA.

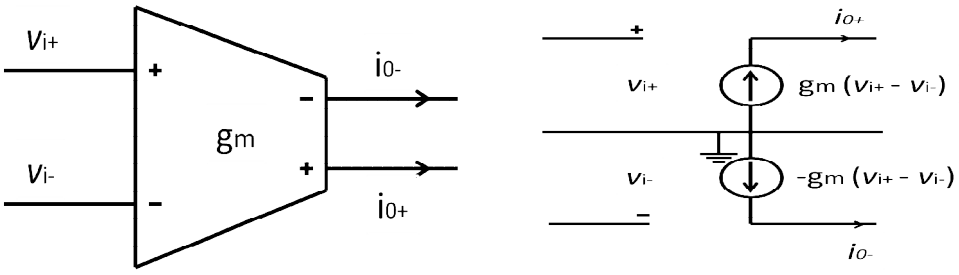
From Eqs. (2.8) and (2.9), it can be seen that the output current is linear function of the input voltage V_{in} and the equivalent transconductance is controlled by difference voltage (V_b-V_a).

2.2.4 DIFFERENTIAL INPUT-BALANCED OUTPUT

The Differential Input-Balanced Output OTA has two input voltages as in Differential-Input Single-Output type of OTA but it provides two balanced currents through the two output terminals i_{0+} and i_{0-} .The symbolic representation and equivalent circuit diagram of this type of OTA are shown in Figs. 2.7 (a) and (b) respectively [19]. The relationship between input and output of Differential Input-Balanced Output OTA is given as

$$i_{0+} = -i_{0-} = g_m v_{in} \tag{2.10}$$

where g_m is the transconductance, $v_{in} = v_{i+} - v_{i-}$ is the input voltage and i_{0+} and i_{0-} are the output currents.



(a) (b)

Figs. 2.7 Differential Input-Balanced Output OTA: (a) Symbol
(b) Equivalent circuit diagram [19]

Fig. 2.8 shows the circuit diagram of a Differential Input-Balanced Output OTA [19]. The structure of this OTA is same as that of Differential Input-Single Output OTA with the addition of two extra pair of PMOS current mirrors formed by transistors M_3, M_9 and M_4, M_{10} and one NMOS current mirror formed by transistors M_{11}, M_{12} to transfer the drain currents I_{D1} and I_{D2} to the second output node B. The polarity of the output currents I_{out1} and I_{out2} at the two output nodes are opposite to each other.

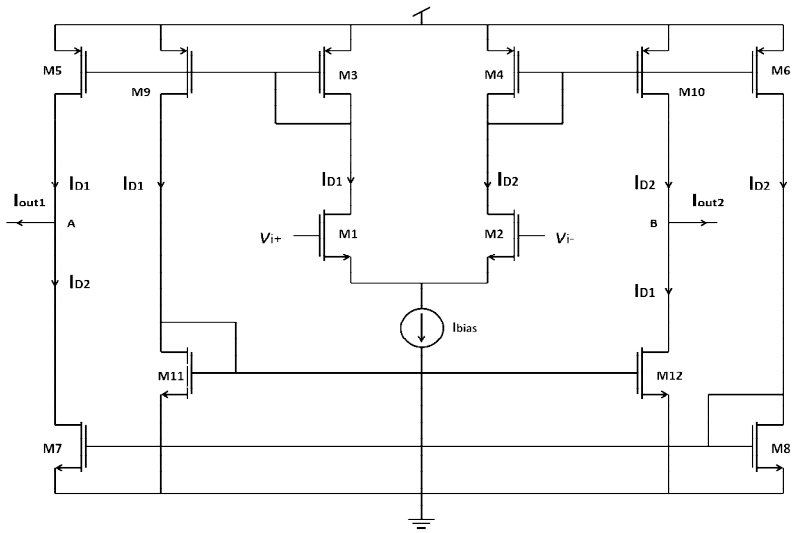


Fig. 2.8 Differential Input-Balanced Output OTA [19]

The output currents of the Differential Input-Balanced Output OTA is given as

$$I_{out1} = -I_{out2} = \sqrt{I_{bias}K}V_{in}\sqrt{1 - \frac{V_{in}^2}{4I_{bias}/K}} \tag{2.11}$$

where $V_{in} = V_{i+} - V_{i-}$ is the differential input voltage, K is the transconductance parameter and I_{bias} is the bias current.

Eq. (2.11) can be written as

$$I_{out} = G_m V_{in} \tag{2.12}$$

where G_m ($=\sqrt{I_{bias}K}$) is the transconductance of Differential Input-Balanced Output OTA.

From Eqs. (2.11) and (2.12), it can be seen that the output current is linear function of the input voltage V_{in} and the equivalent transconductance is controlled by the bias current.

All four configuration of OTA described above, the Single Input-Single Output OTA is the simplest to implement. The simplicity of this configuration makes it suitable for high frequency applications, while most preferred are the differential configurations shown in Fig. 2.3, Fig. 2.5 and Fig. 2.7 due to their ability to reject common-mode signal and flexibility to engage feedback configurations [28-30].

2.3 CONCLUSIONS

A brief overview of the operational transconductance amplifier is discussed in this chapter. The types of OTA such as Single Input-Single Output, Differential Input-Single Output, Differential Input- Differential Output and Differential Input- Balanced Output are also discussed, in which the Single Input-Single Output OTA is the simplest in structure and suitable for high frequency operations but OTAs with differential configuration are preferred due to their ability to reject common-mode signal and flexibility to engage feedback configurations.

CHAPTER 3

LITERATURE REVIEW

3.1 INTRODUCTION

In the last two decades, a large number of analog designers devoted themselves for the development of the Operational Transconductance Amplifier (OTA) because OTAs are one of the most important building blocks in analog signal processing applications. In this chapter various topologies to design OTAs suggested by researchers are discussed. The chapter is organized as follows. Section 3.2 discusses the various CMOS OTAs available in literature and OTAs based on floating gate MOSFET are discussed in section 3.3. The chapter is concluded in section 3.4.

3.2 OPERATIONAL TRANSCONDUCTANCE AMPLIFIER

In literature, different topologies have been presented by several authors to design OTAs [14, 17, 31-49]. Some of the authors have suggested topologies of OTA using CMOS whereas some of the authors have presented topologies of OTA using floating gate MOSFETs.

3.2.1 TUNABLE CMOS OTA

This section discusses different tunable CMOS OTAs available in literature. Tuning in OTA is achieved by either varying transconductance as function of control voltage or biasing current.

3.2.1.1 VOLTAGE-CONTROLLED CMOS OTA

Several researches have suggested voltage-controlled CMOS OTAs [17, 31-33]. The transconductance of an OTA can be changed by changing the control voltage. The main

advantage of voltage mode OTA circuits is that the operation of these circuits is quite simple.

A low-voltage pseudo differential continuous-time CMOS OTA for wideband applications is presented in [17]. In the circuit, input common-mode signal is cancelled by feed-forward cancellation technique and the input common mode voltage is kept constant. The transconductance of the circuit is controlled by a continuous bias voltage. Linearity is preserved during the tuning process for a moderate range of transconductance values but the input voltage swing of this OTA is restricted by the means of maintaining the transistors in saturation region.

A design of a linear OTA for low-voltage and low-power operation is presented in [31]. The realization of the OTA utilizes two techniques for low-voltage low-power operations. In the first technique, the floating voltage source is improved by employing low voltage cascode current mirror so that the accuracy of the current transfer factor becomes high in spite of small currents and low supply voltage. In the second technique, the tail current is controlled by an adaptive biasing so that the excess operating current is saved. The circuit operates in wide linear range by using small amount of reference current with low power consumption. The THD performance of the circuit gets deteriorated because of the use of adapting biasing.

J.M. Martinez-Heredia *et al.* [32] suggested a technique to improve the linearity and the output resistance of source-degenerated OTA using super transistors as voltage buffers. In this technique, voltage buffers developed by super transistors are used in order to take the advantage of the unity voltage gain, the very high output resistance of the drain node and the very low output resistance of the source node of super transistor. The weak inversion region is used to optimize the regulated cascode sources of the OTA, making them able to operate under low-voltage requirements while keeping a high value of output resistance.

A low voltage bulk-driven operational transconductance amplifier (OTA) is presented in [33]. The circuit uses a nonlinear terms cancelation technique employed by two paralleled differential topologies with opposite signs in the third-order harmonic distortion term of the differential output current to achieve the linearity of the OTA. In order to overcome some drawbacks of using bulk-driven structures, such as high noise, low bandwidth, and low DC gain, a transconductance enhancement technique using flipped voltage follower is applied to the circuit.

The voltage-controlled CMOS OTAs discussed above are compared in Table 3.1. From this table it can be seen that OTA in [17] has better transconductance gain as compared to others but it also required larger power supply. The power consumption and input voltage range of [31] is better but it has lower transconductance gain.

Table 3.1 Comparison of voltage-controlled CMOS OTAs

References	Year	CMOS Tech. (μm)	Power Supply (V)	G_m (μA/V)	Bandwidth (MHz)	Input Range (Vpp)	Power Consumption (mW)	THD (db) @freq (MHz) @i/p (Vpp)
[17]	2008	0.35	2	1400	600	-	1.2	-60@10@-
[31]	2009	0.18	1.8	22	-	1	0.057	-
[32]	2011	0.13	1.5	40	65	0.9	0.126	-110@0.001@0.35
[33]	2014	0.18	0.8	27	-	0.8	31.2	-40@1@0.8

3.2.1.2 CURRENT-CONTROLLED CMOS OTA

The main disadvantage of voltage-controlled OTAs is that they have limited controllable voltage range. For low voltage OTA applications, tuning is often achieved using bias current as it shows better linear range at low voltages. Several researches have suggested current-controlled OTAs [14, 34-44].

Ko-Chi Kuo [34] suggested a configuration for linear CMOS OTA, which uses two linearization methods namely source degeneration [35], and adaptive biasing [36]. The circuit has good tuning capability and it works for both fully-balanced and unbalanced input signals but for the unbalanced case the OTA provides slightly decreased performance.

A. Worapishet *et al.* [37] presented a highly linear current-feedback CMOS OTA with resistive source-degeneration. It consists of a cascade structure of a differential source follower with a classical source degenerated OTA. For nonlinearity cancellation, the drain current source degenerated is fed back to modulate the bias of the source follower, yielding an overall linear transfer function in the circuit. The circuit employs simple NMOS current mirrors to form the feedback path whose feedback gain is typically close to unity. To avoid well-substrate parasitic capacitances the bulk terminals of MOS

transistors are connected their corresponding supply rails which degrade the linearity of the OTA.

A Flipped Voltage Follower based compact low-voltage low-power differential linear OTA is presented in [38]. The circuit uses two identical Flipped Voltage Follower (FVF) buffers for the implementation of two low impedance floating voltage sources. The circuit takes advantage of class-AB behavior to achieve a high current efficiency and low power consumption.

Andreas Demosthenous *et al.* [39] suggested a Low-Voltage class AB MOS Linear OTA using flipped voltage follower. The circuit is based on square law behaviour of the MOS transistors operating in saturation region. This design uses cross-coupled matched MOSFET transistor pair and two identical dc floating-voltage sources. The authors have also used the same OTA to design an analog four-quadrant multiplier.

A circuit design technique for the synthesis of a linear electronically tunable CMOS OTA is presented in [40]. The technique is achieved by squaring the transconductance gain of the CMOS OTA. The transconductance gain of the circuit is directly controlled by the DC bias current. A balanced CMOS OTA or voltage-to-current transducer is employed as basic active circuit elements to realize the complete structure of the circuit.

Khanittha Kaewdang *et al.* [41] suggested the technique to realize a wide linearly and electronically tuned CMOS OTA. The design is the combination of a fully differential OTA and a variable current gain cell constructed using a current mode translinear circuit. The individual functions of the circuit are derived from the approximate square-law characteristic of MOS transistors operating in saturation region.

A linearly tunable OTA is presented by in [42]. The technique stabilizes the small-signal input transconductance by using a replica of the active differential pair in a negative feedback configuration. The replica circuitry tracks the bias conditions of the active differential pair monitoring any variation in the input transconductance. The small-signal input transconductance is linearly tuned over a wide range, using a DC tuning current offering the benefits of circuit simplicity and relative small dependency over process, supply voltage and temperature.

Sougata Kumar Kar *et al.* [43] proposed the design and analysis of a wide linear input range OTA that combines the techniques of signal attenuation and source degeneration in

order to reduce the odd order harmonic distortion significantly. In the linearization technique, a differential attenuator followed by a source-degenerated OTA is used. The differential output voltage from the attenuator serves as the differential input for a source degenerated OTA that is degenerated either by a resistor or MOS in linear region.

A linear local-feedback CMOS OTA for low frequency applications is suggested in [14]. The OTA is operating in sub-threshold region and has very low transconductance. The topology of the OTA is developed on the basis of the local-feedback OTA. To reduce the nonlinear effect of the transfer characteristic, the MOSFETs are operating in sub-threshold region. This OTA is optimally designed using maximally flat approximation method, Newton-Raphson method and Downhill simplex method.

A highly linear fully differential CMOS OTA architecture based on flipped voltage follower (FVF) is suggested in [44]. Mobility reduction compensation technique is used to increase the linearity of the differential CMOS OTA architecture. The input range and the stability of the OTA are improved by using level shifter and compensation capacitor respectively while the output impedance is improved because of the use of cascoded transistors.

The comparison between current-controlled OTAs discussed above is shown in Table 3.2.

Table 3.2 Comparison of current-controlled CMOS OTAs

References	Year	CMOS Tech. (μm)	Power Supply (V)	G_m (μA/V)	Bandwidth (MHz)	Input Range (Vpp)	Power Consumption (mW)	THD (db) @freq (MHz) @i/p (Vpp)
[34]	2001	0.35	3.3	40	5	2	1	-57@0.001@1.6
[37]	2003	0.35	2.5	500	-	-	3.4	-80@1@0.8
[38]	2004	0.8	1.5	155	40	0.6	0.042	-55@5@0.1
[39]	2005	0.8	2	266	175	0.6	0.160	-48@0.001@0.4
[40]	2007	-	10	539	120	3	-	-
[41]	2009	0.5	3	850	750	0.4	20	-
[42]	2010	0.18	1.8	1050	-	-	-	-
[43]	2012	0.18	1.8	90	-	1.2	0.45	-70@5@0.6
[44]	2012	0.13	1	88	-	0.4	0.345	-55@5@0.4

3.2.2 TUNABLE FLOATING GATE MOSFET BASED OTA

This section discusses different OTAs based on floating gate MOSFET available in literature [45-49]. The tunability of these OTAs can also be controlled either by control voltage or bias current.

3.2.2.1 VOLTAGE-CONTROLLED FLOATING GATE MOSFET BASED OTA

A technique is presented in [45] to design a programmable voltage-to-current (V-I) converters based on floating gate MOSFETs. In this technique, the V-I conversion is achieved by employing two passive resistors with one of their terminals tied to a very low impedance node. The programmable floating-gate MOSFET current mirrors that work in moderate inversion region are used to convey the resistor currents to the output.

J. M. A. Miguel *et al.* [46] suggested a class AB CMOS tunable OTA. The linearization of a MOS transistor operating in triode region, which performs voltage-to-current conversion, is achieved by Quasi-Floating-Gate (QFG) technique. The linearity is increased because of the negative local feedback. The negative local feedback is employed by the voltage followers, which translate the input voltage to the transistor operating in triode region.

Apirak Suadet *et al.* [47] presented a quasi floating gate (QFG) inverter-based class-AB linear transconductance for low voltage applications. The circuit uses positive feedback technique to enhance the input impedance, and feed-forward technique to suppress the common-mode gain. The frequency performance of the circuit degrades because of large standby currents and parasitic capacitance due to the large sized transistors which are required for high transconductance gain.

3.2.2.2 CURRENT-CONTROLLED FLOATING GATE MOSFET BASED OTA

V. Suresh Babu *et al.* [48] presented an operational transconductance amplifier realized using Floating Gate MOSFETs. In the circuit, differential pairs are used as input stage for Voltage-to-Current conversion. Floating gate MOSFET differential pair ensures low voltage operation and adaptability of the parameters. The same circuit is used to generate log sigmoid and tan sigmoid NAF functions, simultaneously. In the circuit the parameters of NAF functions can be changed by changing voltage applied at the control gate of floating gate MOSFET.

A low-voltage class-AB operational transconductance amplifier is suggested in [49]. In the design, a differential pair with constant sum of gate-to-source voltages is used to convert a voltage difference into a current difference. The differential pair is designed using p-type MOS transistor and a p-type floating gate MOSFET transistor and current source is used to implement constant sum of gate-to-source voltages.

The comparison between various specifications of floating gate MOSFET based OTAs discussed above are shown in Table 3.3. From this table it can be seen that the current-controlled OTAs based on floating gate MOSFET [48, 49] have better input voltage range and consume lesser amount of power.

Table 3.3 Comparison of floating gate MOSFET based OTAs

References	Year	CMOS Tech. (μm)	Power Supply (V)	G_m (μA/V)	Bandwidth (MHz)	Input Range (Vpp)	Power Consumption (mW)	THD (db) @freq (MHz) @i/p (Vpp)
[45]	2006	0.5	3	46	-	3	2.6	-60@0.1@3
[46]	2011	0.5	5	-	-	5	2.2	-52@1@2
[47]	2011	0.18	0.5	245	10	0.5	0.11	-45@5@0.4
[48]	2009	2	0.75	-	-	2	0.0003	-
[49]	2009	0.18	0.7	-	-	1.4	0.010	-35@5@0.4

3.3 CONCLUSIONS

In this chapter, different topologies suggested by various authors to design a tunable OTA based on either CMOS or floating gate MOSFET have been discussed. The tunability of these OTAs is controlled by either control voltage or bias current. But the current-controlled OTAs are preferred due to their high linear ranges and low voltage operations.

CHAPTER

4

HIGHLY LINEAR OTA USING SOURCE DEGENERATION TOPOLOGY

4.1 INTRODUCTION

The chapter proposes a highly linear floating gate MOSFET based source-degenerated OTA. The use of floating gate MOSFET reduces the power supply requirement of the circuit and source degeneration technique is used to increase the linearity of the proposed OTA. The chapter is organized as follows. Section 4.2 discusses the operation of the proposed floating gate MOSFET based source-degenerated OTA. In Section 4.3, the applications of proposed OTA such as active inductor, tunable resistors and filters are presented. The chapter is concluded in section 4.4.

4.2 FLOATING GATE MOSFET BASED SOURCE-DEGENERATED OTA

The proposed floating gate MOSFET based source-degenerated OTA is shown in Fig. 4.1. The proposed circuit is one of the examples of Differential Input-Balanced Output OTAs.

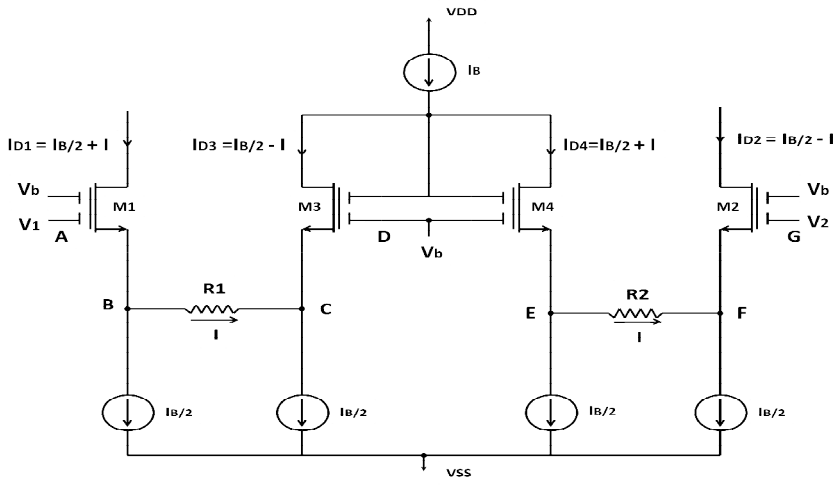


Fig. 4.1 Proposed floating gate MOSFET based source-degenerated OTA

In the proposed circuit, two differential pairs formed by floating gate MOSFETs M_1, M_3 and M_2, M_4 are connected in series to reduce the distortion [50]. All the transistors M_1-M_4 are biased in saturation region. The differential pairs are also source degenerated by resistors R_1 and R_2. Two input voltages V_1 and V_2 are applied at one of the gate terminals of transistors M_1 and M_2, respectively. The proposed circuit is properly biased with current sources of same values connected to the source terminals of transistors M_1, M_2, M_3 and M_4. Using Eq. (1.1), the drain currents I_{D1}, I_{D2}, I_{D3} and I_{D4} of transistors M_1, M_2, M_3 and M_4 respectively are given as

$$I_{D1} = K(V_{FGS1} - V_T)^2 \tag{4.1a}$$

$$I_{D2} = K(V_{FGS2} - V_T)^2 \tag{4.1b}$$

$$I_{D3} = K(V_{FGS3} - V_T)^2 \tag{4.1c}$$

$$I_{D4} = K(V_{FGS4} - V_T)^2 \tag{4.1d}$$

where $K = \frac{\mu_n C_{ox}}{2}\left(\frac{W}{L}\right)$ is the transconductance parameter, V_T is the threshold voltage and $V_{FGS}\left(= \frac{\sum_{i=1}^{N} C_i V_{iS}}{C_T} + \frac{C_{GD}}{C_T}V_{DS} + \frac{C_{GB}}{C_T}V_{BS}\right)$ is the voltage between floating-gate and source of the floating gate MOSFET.

Applying Kirchhoff's voltage law to the input loop A-G in Fig. 4.1, loop equation can be written as

$$V_1 - V_{FGS1} - IR_1 + V_{FGS3} - V_{FGS4} - IR_2 + V_{FGS2} - V_2 = 0 \tag{4.2}$$

where I is the current flowing through the resistor R_1 and R_2.

Substituting V_1-V_2 =V_{in} (differential input voltage) and R_1=R_2=R, Eq. (4.2) is modified as

$$V_{in} - 2IR = V_{FGS1} - V_{FGS3} + V_{FGS4} - V_{FGS2} \tag{4.3}$$

Substituting the values of V_{FGS1}, V_{FGS2}, V_{FGS3} and V_{FGS4} from Eq. (4.1) in Eq. (4.3), the Eq. (4.3) can be written as

$$V_{in} - 2IR = 2\sqrt{\frac{\frac{I_B}{2}+I}{K}} - 2\sqrt{\frac{\frac{I_B}{2}-I}{K}} \tag{4.4}$$

After simplification of Eq. (4.4), the current flowing through resisters R_1 and R_2 (I) is given as

$$I = \frac{K(V_{in}-2IR)}{2}\sqrt{\frac{I_B}{2k} - \frac{(V_{in}-2IR)^2}{16}} \tag{4.5}$$

From Fig. 4.1, the output current of OTA (I_{out}) is observe as

$$I_{out} = I_{out1} = -I_{out2} = I_{D1} - I_{D2} = 2I \tag{4.6}$$

Using Eqs. (4.5) and (4.6), the output current I_{out} can be written as

$$I_{out} = K(V_{in} - I_{out}R)\sqrt{\frac{I_B}{2k} - \frac{(V_{in}-I_{out}R)^2}{16}} \tag{4.7}$$

The Eq. (4.7) shows the relationship between output current I_{out} and input differential voltage V_{in} of proposed OTA. The transconductance of the proposed OTA can be calculated as

$$G_m = \frac{g_m}{1+g_mR} \tag{4.8}$$

where $g_m = \sqrt{KI_B/2}$ is the transconductance of the transistors M_1-M_4.

The nonlinear term in Eq. (4.7) depends on $V_{in} - I_{out}R$ rather than V_{in}. When $R>>1/g_m$, the nonlinear term becomes zero and thereby high linearity can be obtained.

The complete circuit of proposed OTA (Fig 4.1) is shown in Fig. 4.2, in which resistors R1 and R2 are replaced with the help of transistors M_{R1}-M_{R2} and M_{R3}-M_{R4}, respectively. These transistors (M_{R1}-M_{R4}) are operating in the ohmic region. A current source formed by PMOS transistor M_5 is used for biasing purpose. Three current mirrors are formed using NMOS transistors M_6–M_7, M_{17}–M_{18}, M_{19}–M_{20} and two current mirrors are formed using PMOS transistors M_{11} – M_{12}, M_{14} – M_{15}. These current mirrors are used to copy the currents at appropriate nodes of the circuit. The remaining transistors are used to transfer the currents at appropriate nodes.

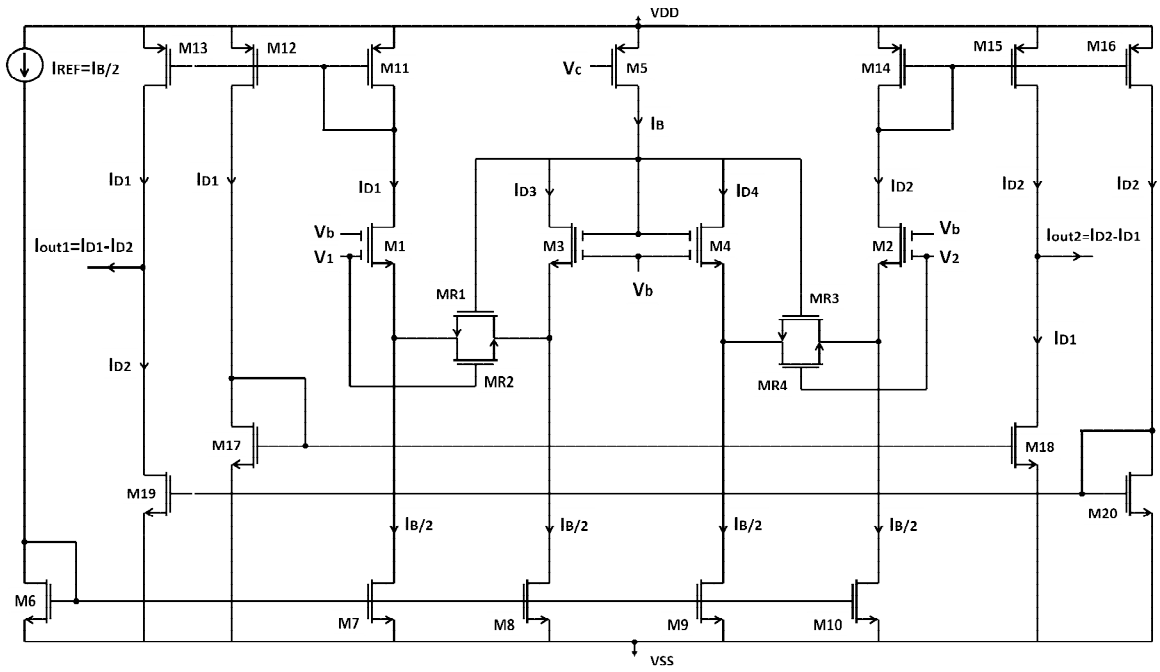


Fig. 4.2 Complete circuit of floating gate MOSFET based source-degenerated OTA

4.3 APPLICATIONS OF THE PROPOSED OTA

The proposed OTA is also used to develop some of the analog circuits such as active inductor, tunable resistors and filters.

4.3.1 ACTIVE INDUCTOR

An active inductor shown in Fig. 4.3 is designed using proposed OTA. The inductor is designed using a capacitor C and OTA.

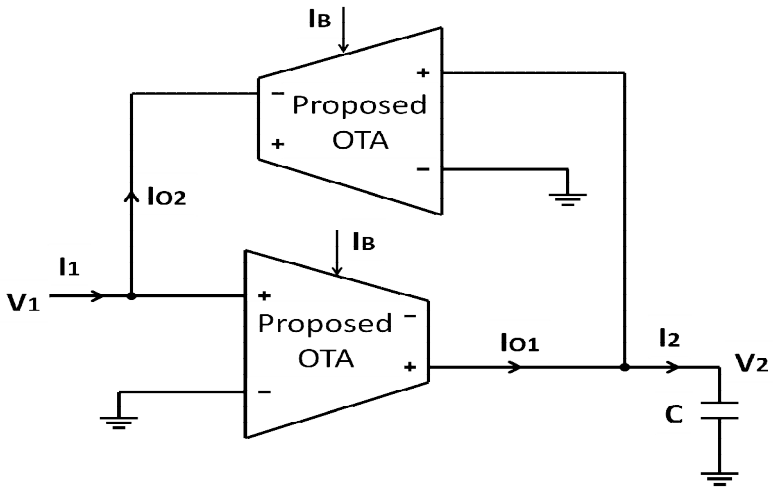


Fig. 4.3 Active inductor using proposed OTA

From Fig. 4.3, current flowing through capacitor C is given as

$$I_2 = I_{O1} = G_m V_1 \tag{4.9}$$

where G_m is the transconductance of the proposed OTA and V_1 is the input voltage.

Input current I_1 is given as

$$I_1 = I_{O2} = G_m V_2 \tag{4.10}$$

where V_2 is the voltage across capacitor C.

Substituting $V_2 = I_2/sC$, Eq. (4.10) is modified as

$$I_1 = \frac{G_m I_2}{sC} \tag{4.11}$$

Now, substituting the value of I_2 from Eq. (4.9), Eq. (4.11) is modified as

$$I_1 = \frac{G_m^2}{sC} V_1 \tag{4.12}$$

Comparing Eq. (4.12) with $I_1 = \frac{1}{sL_{eq}} V_1$, the equivalent inductance L_{eq} is given as

$$L_{eq} = \frac{C}{G_m^2} \tag{4.13}$$

From Eq. (4.13), it can be seen that the value of equivalent inductance depends on the transconductance G_m of the proposed OTA. Hence, the proposed circuit behaves like an active inductor.

4.3.2 TUNABLE RESISTORS

Tunable resistors have a significant role in the analog circuit design because they can be employed as tuning elements in various analog circuit applications. The proposed OTA is used to develop tunable grounded and floating resistors.

4.3.2.1 GROUNDED RESISTORS

A tunable grounded resistor shown in Fig. 4.4 is designed using proposed OTA. The negative output terminal of the proposed OTA is connected back to its positive input terminal.

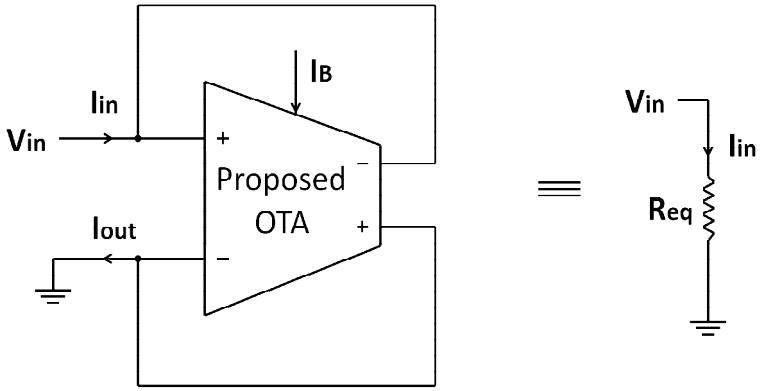


Fig. 4.4 Grounded resistor using proposed OTA

The input current I_{in} is equal to the output current I_{out} of the OTA which is equal to

$$I_{in} = G_m V_{in} \tag{4.14}$$

where V_{in} is the input voltage and G_m is the transconductance of proposed OTA.

From Eq. (4.14) the equivalent resistance R_{eq} is given as

$$R_{eq} = \frac{V_{in}}{I_{in}} = \frac{1}{G_m} \tag{4.15}$$

From Eq. (4.15), it can be seen that the equivalent resistance (R_{eq}) can be varied with the transconductance G_m. Hence, the proposed circuit behaves like a grounded resistor.

4.3.2.2 FLOATING RESISTOR

A tunable floating resistor shown in Fig. 4.5 is designed using proposed OTA. For designing of the floating resistor by OTA, a differential input is given to the OTA.

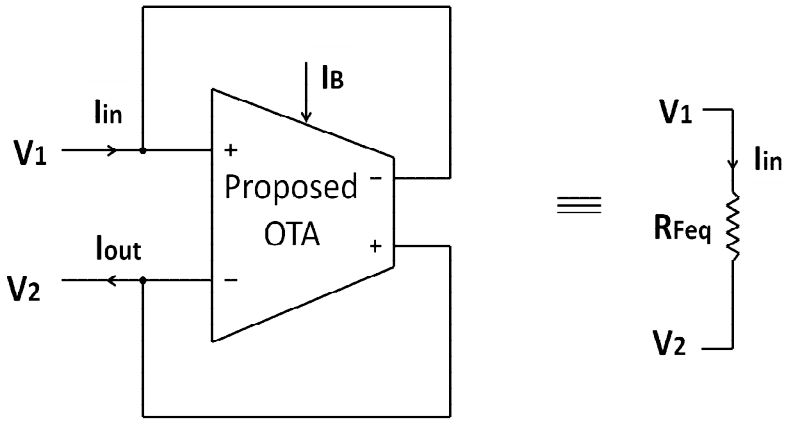


Fig. 4.5 Floating resistor using proposed OTA

The input current I_{in} is equal to the output current I_{out} of the OTA which is equal to

$$I_{in} = G_m(V_1 - V_2) \tag{4.16}$$

where V_1 and V_2 are the input voltages and G_m is the transconductance of proposed OTA.

From Eq. (4.16) the equivalent floating resistance R_{Feq} is given as

$$R_{Feq} = \frac{V_1 - V_2}{I_{in}} = \frac{1}{G_m} \tag{4.17}$$

From Eq. (4.17), it can be seen that the equivalent floating resistance (R_{Feq}) can be varied with the transconductance G_m. Hence, the proposed circuit behaves like a floating resistor.

4.3.3 FILTERS

The proposed OTA is used to design first and second order low pass, high pass and band pass tunable filters.

4.3.3.1 FIRST ORDER LOW PASS FILTER

A first order low pass filter shown in Fig. 4.6 is designed using proposed OTA.

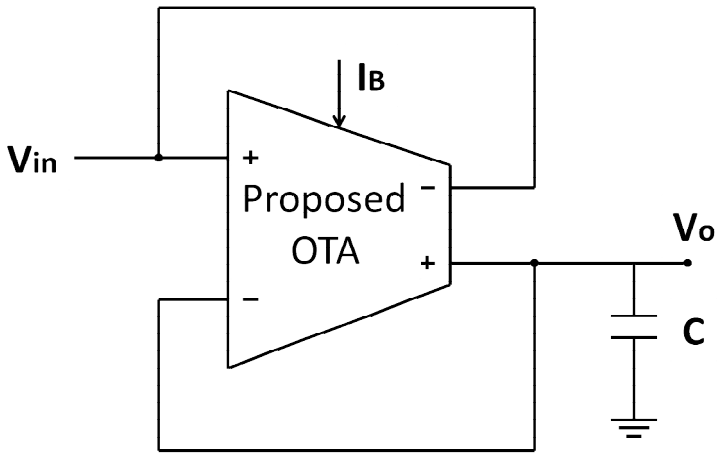


Fig. 4.6 First order low pass filter using proposed OTA

The transfer function of the first order low pass filter is expressed as

$$\frac{V_o}{V_{in}} = \frac{G_m}{G_m + sC} \tag{4.18}$$

where G_m is the transconductance of OTA and C is the capacitor.

4.3.3.2 SECOND ORDER LOW PASS FILTER

A second order low pass filter shown in Fig. 4.7 is designed using proposed OTA.

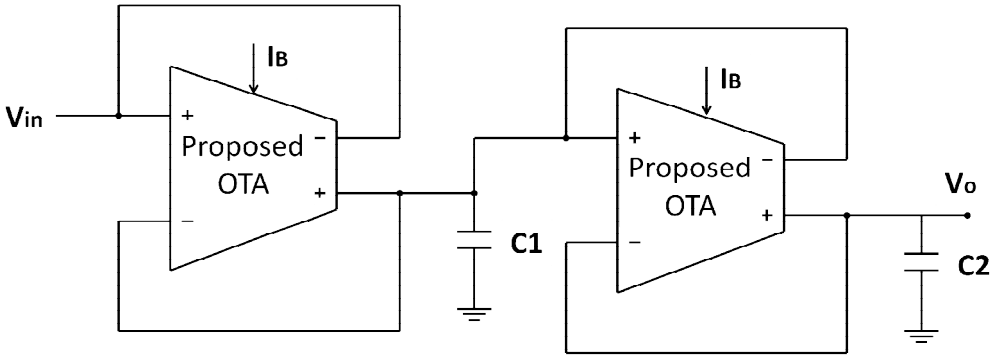


Fig. 4.7 Second order low pass filter using proposed OTA

This filter is designed by cascading two first order low pass filter. The transfer function of this second order low pass filter is expressed as

$$\frac{V_o}{V_{in}} = \frac{G_m^2}{s^2C_1C_2+sG_m(C_1+2C_2)+G_m^2} \tag{4.19}$$

where G_m is the transconductance of OTA and C_1, C_2 are the capacitors.

4.3.3.3 FIRST ORDER HIGH PASS FILTER

A first order high pass filter shown in Fig. 4.8 is designed using proposed OTA.

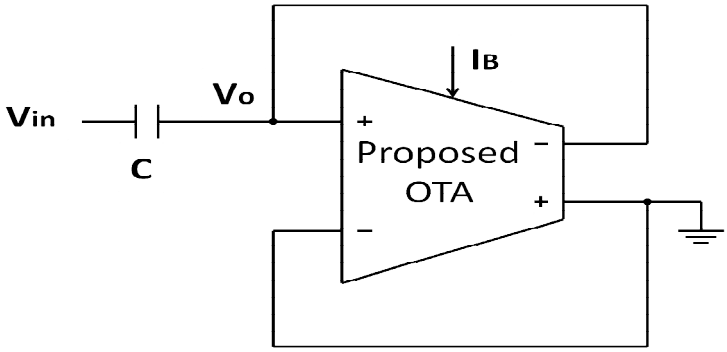


Fig. 4.8 First order high pass filter using proposed OTA

The transfer function of this first order high pass filter is expressed as

$$\frac{V_o}{V_{in}} = \frac{sC}{G_m+sC} \tag{4.20}$$

where G_m is the transconductance of OTA and C is the capacitor.

4.3.3.4 SECOND ORDER HIGH PASS FILTER

A second order high pass filter shown in Fig. 4.9 is designed using proposed OTA.

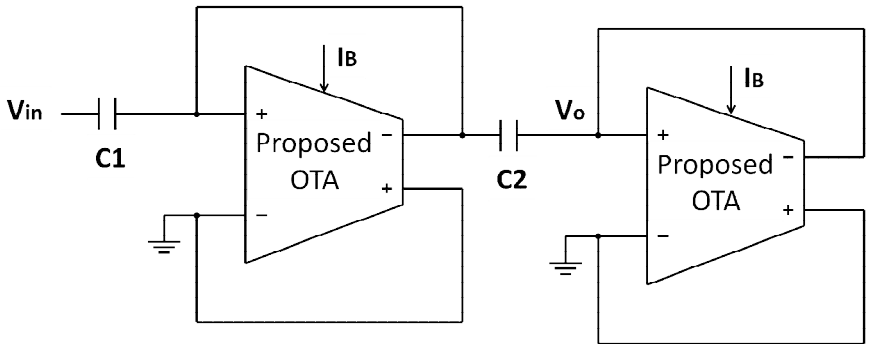


Fig. 4.9 Second order high pass filter using proposed OTA

This filter is designed by cascading two first order high pass filter. The transfer function of this second order high pass filter is expressed as

$$\frac{V_o}{V_{in}} = \frac{s^2 C_1 C_2}{s^2 C_1 C_2 + s G_m (C_1 + 2C_2) + G_m^2} \tag{4.21}$$

where G_m is the transconductance of OTA and C_1, C_2 are the capacitors.

4.3.3.5 FIRST ORDER BAND PASS FILTER

A first order band pass filter shown in Fig. 4.10 is designed using proposed OTA.

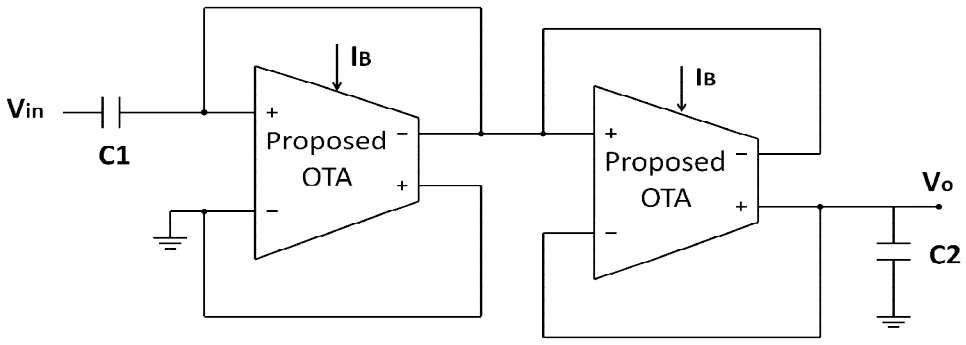


Fig. 4.10 First order band pass filter using proposed OTA

The filter is designed by cascading first order high pass filter with first order low pass filter. The transfer function of this first order band pass filter is expressed as

$$\frac{V_o}{V_{in}} = \frac{s C_1 G_m}{s^2 C_1 C_2 + s G_m (C_1 + 2C_2) + G_m^2} \tag{4.22}$$

where G_m is the transconductance of OTA and C_1, C_2 are the capacitors.

4.3.3.6 SECOND ORDER BAND PASS FILTER

A second order band pass filter shown in Fig. 4.11 is designed using proposed OTA.

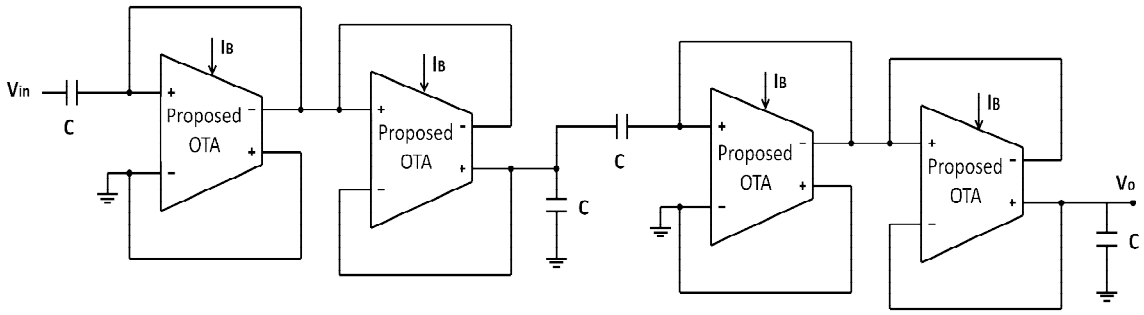


Fig. 4.11 Second order band pass filter using proposed OTA

This filter is designed by cascading two first order band pass filter. The transfer function of this second order band pass filter is expressed as

$$\frac{V_o}{V_{in}} = \frac{sCG_m^4}{s^4C^4+8s^3C^3G_m+21s^2C^2G_m^2+8sCG_m^3+G_m^4} \quad (4.23)$$

where G_m is the transconductance of OTA and C is the capacitor.

4.4 CONCLUSIONS

A highly linear floating gate MOSFET based source-degenerated OTA has been proposed in this chapter. The requirement of the power supply of the proposed circuit has been reduced because of the use of floating gate MOSFET and the use of source-degeneration topology enhances the linearity of the designed OTA. Some of the applications of the proposed OTA such as active inductor, tunable resistors and filters have also been presented.

CHAPTER

5

SIMULATION RESULTS AND LAYOUT

5.1 INTRODUCTION

This chapter presented the simulation results of proposed highly linear floating gate MOSFET based source-degenerated OTA using UMC 0.18µm CMOS process technology parameters. The chapter is organized as following. Section 5.2 presents the simulation results of the proposed OTA. The simulation results of the applications of the proposed OTA are presented in section 5.3. Section 5.4 addresses the layout of the proposed OTA using UMC 0.18µm CMOS process technology parameters. The chapter is concluded in section 5.5.

5.2 SIMULATION RESULTS OF THE PROPOSED FLOATING GATE MOSFET BASED SOURCE-DEGENERATED OTA

The proposed floating gate MOSFET based source-degenerated OTA shown in Fig. 4.2 has been simulated using UMC 0.18µm CMOS process technology parameters. The dimension of the transistors of proposed circuit is listed in Table 5.1.

Table 5.1 Transistor sizing in proposed circuit

MOSFETS	W (µm)	L (µm)
M_1-M_4	1	0.2
M_{R1}-M_{R4}	10	0.2
M_5	2.1	0.2
M_6-M_{10}	30	0.2
M_{11}-M_{14}	3.8	0.2
M_{15}-M_{20}	18	0.2

The DC transfer characteristic of the proposed OTA is shown in Fig. 5.1. From this characteristic it can be seen that the output currents of the OTA is linearly varied with respect to the input differential voltage V_{in}. The range of the input differential voltage for linear operation of the OTA is equal to the supply rail i.e. -0.6V to 0.6V.

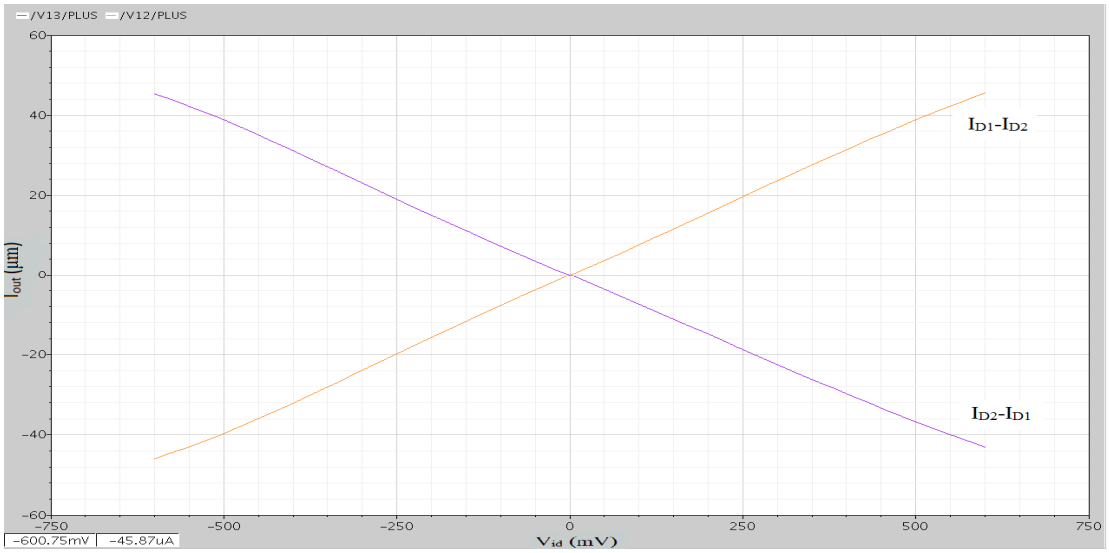


Fig. 5.1 DC transfer characteristic of proposed OTA

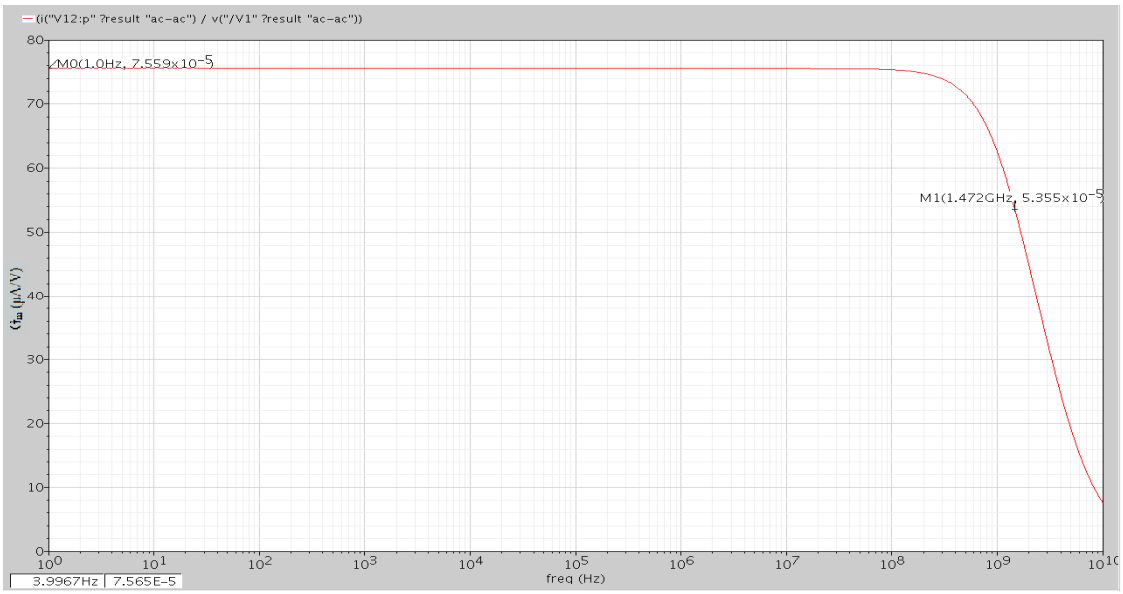


Fig. 5.2 Frequency response of proposed OTA

The frequency response of the designed OTA is shown in Fig. 5.2. From this response it can be seen that the transconductance of the proposed OTA is 75.5µA/V and the -3db bandwidth is equal to 1.47GHz.

The tunability of the OTA with respect to I_B is shown in Fig. 5.3. The value of I_B is varied from 120µA to 200µA with the increment of 20µA.

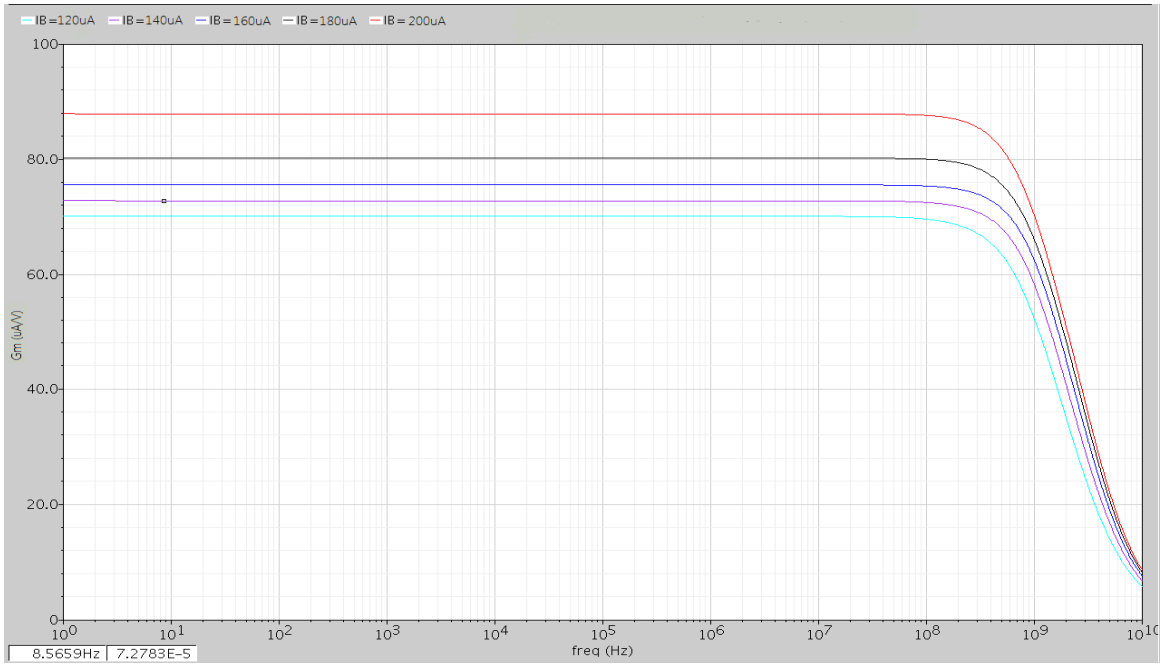


Fig. 5.3 Tuning of transconductance with respect to I_B

The corresponding values of transconductance of the OTA for different values of bias current are listed in Table 5.2.

Table 5.2 Transconductance (G_m) of the proposed OTA for different values of bias current (I_B)

I_B (µA)	G_m (µA/V)
120	70.08
140	72.78
160	75.54
180	80.18
200	87.85

From the Fig. 5.3 and Table 5.2 it is clear that the transconductance of the proposed OTA can be tuned by bias current.

The time domain output response of the proposed OTA corresponding to a sinusoidal input of amplitude $0.6V_{pp}$ at frequency 1MHz is shown in Fig. 5.4.

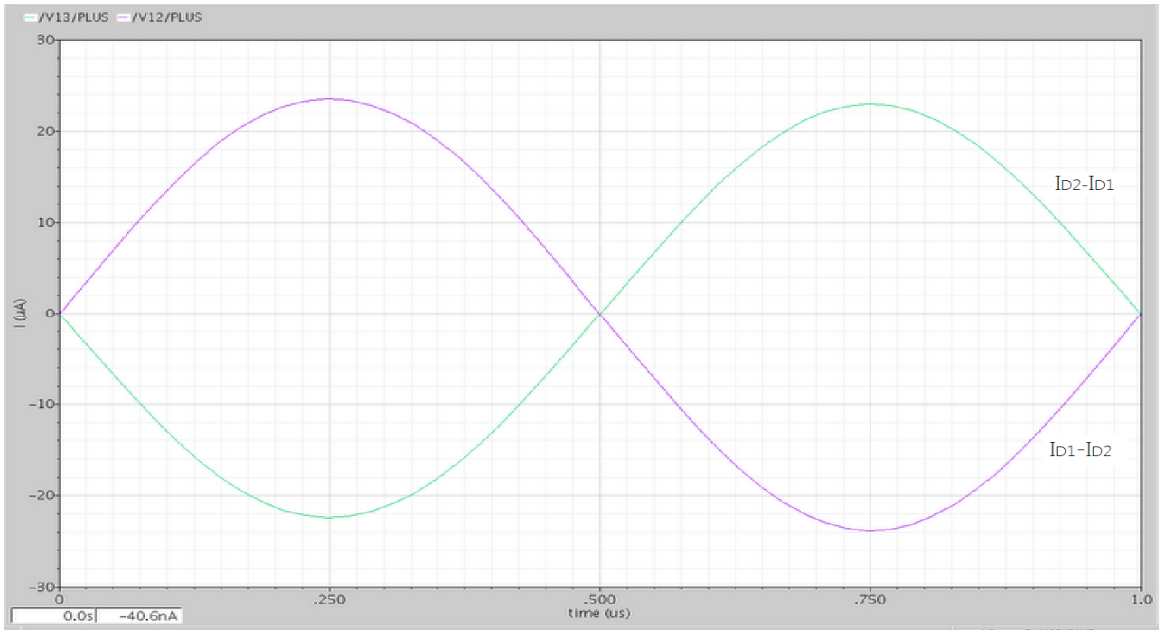


Fig. 5.4 Time domain response of proposed OTA

The THD performance of the proposed OTA is shown in Fig. 5.5. From this figure it can be seen that the proposed OTA has the THD of -42db for 1Vpp input differential voltage at 5MHz frequency.

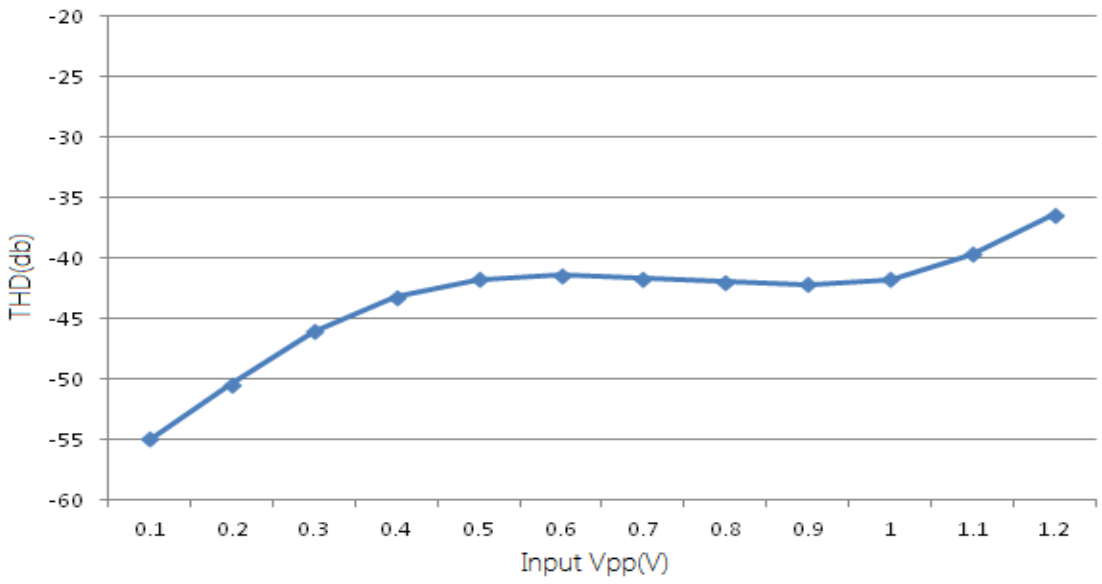


Fig. 5.5 THD performance of proposed OTA

5.3 APPLICATIONS OF THE PROPOSED OTA

The applications of the proposed OTA such as active inductor, tunable resistors and filters are developed and simulated using UMC 0.18µm CMOS process technology parameters. The simulation results of these applications are presented in this section.

5.3.1 SIMULATION RESULTS OF ACTIVE INDUCTOR

The active inductor using proposed OTA (Fig. 4.3) is simulated using UMC 0.18µm CMOS process technology parameters. Fig. 5.6 shows the inductance vs. frequency plot for G_m=75.5µA/V and C=1pF.

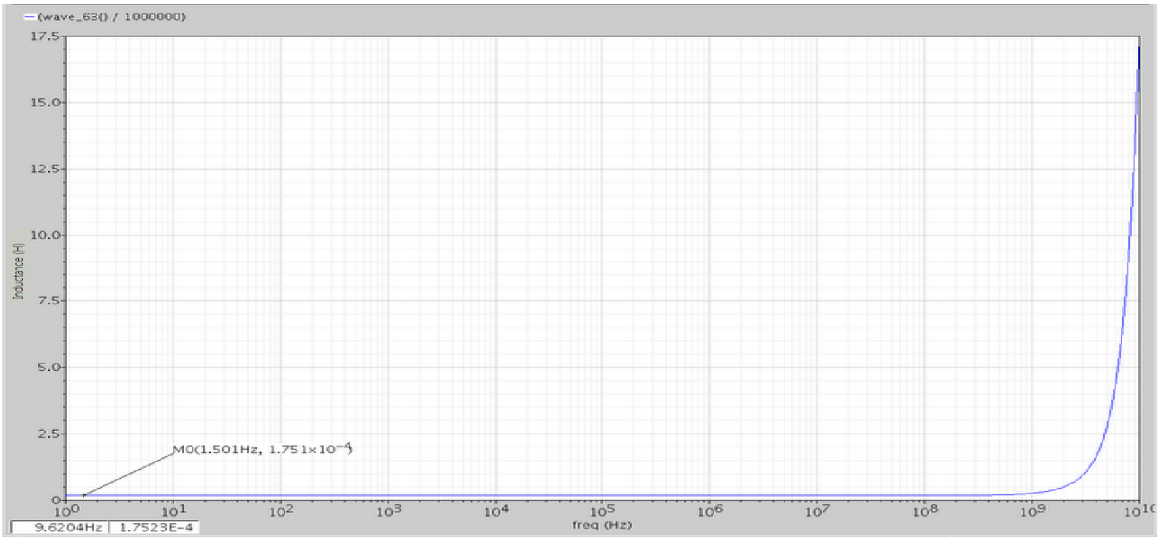


Fig. 5.6 The value of inductance vs. frequency

The values of the equivalent inductance (L_{eq}) for different values of transconductance (Gm) are listed in Table 5.3.

Table 5.3 Equivalent inductance (L_{eq}) for different values of G_m

G_m (µA/V)	Equivalent Inductance L_{eq} (mH)
70.08	0.203
72.78	0.188
75.54	0.175
80.18	0.155
87.85	0.129

5.3.2 SIMULATION RESULTS OF TUNABLE RESISTORS

The tunable grounded resistor and floating resistor shown in Fig. 4.4 and Fig. 4.5 respectively are developed by using proposed OTA and simulated using UMC 0.18µm CMOS process technology parameters. The DC characteristic of the grounded resistor for G_m=75.5µA/V is shown in Fig. 5.7.

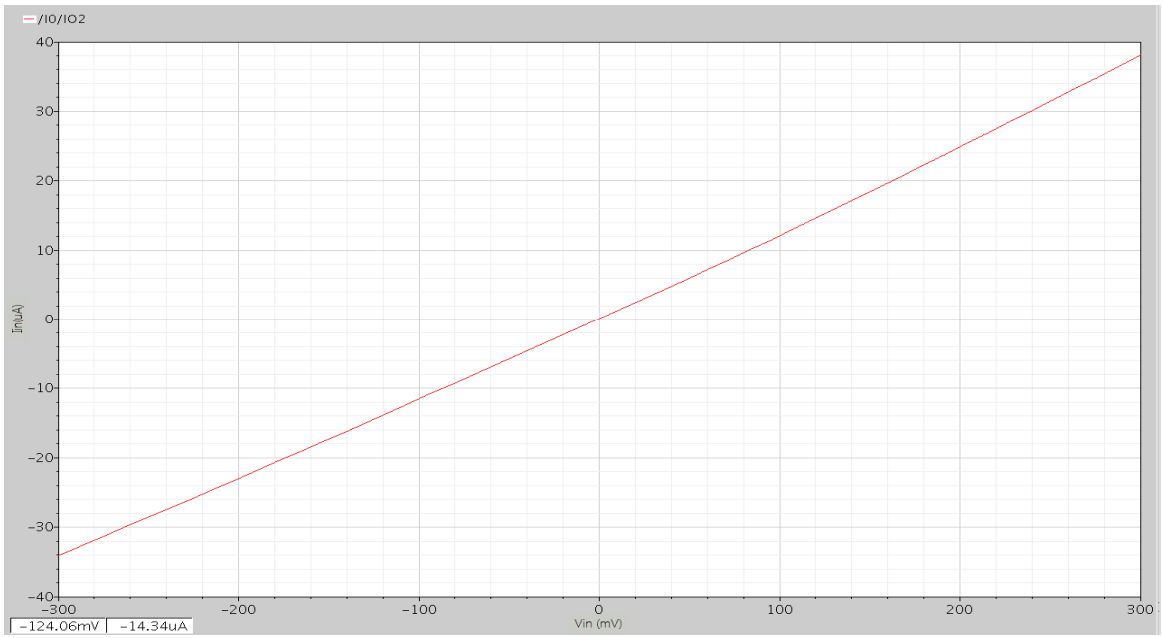


Fig. 5.7 DC characteristic of grounded resistor

The values of the equivalent grounded resistor (R_{eq}) for different values of bias current (I_B) are listed in Table 5.4.

Table 5.4 Equivalent grounded resistance (R_{eq}) for different values of I_B

I_B (µA)	Equivalent Resistance R_{eq} (KΩ)
120	10.82
140	9.5
160	8.69
180	7.75
200	7.19

Fig. 5.8 shows the DC characteristics of the floating resistor shown in Fig. 4.5. To obtain this plot input voltage V_1 is varied from -0.3V to 0.3V for various values of input voltage V_2 ranging from -0.3V to 0.3V with the increment of 0.15V.

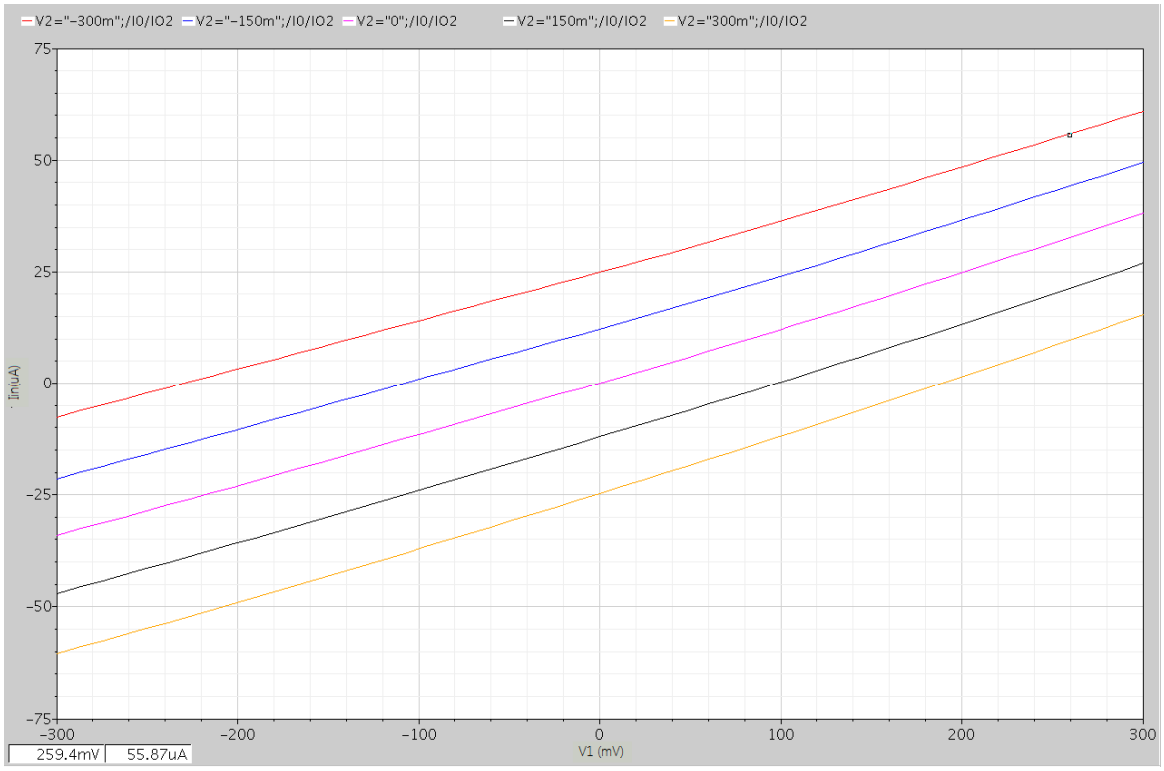


Fig. 5.8 DC characteristic of floating resistor

The values of the equivalent floating resistor (R_{Feq}) for different values of input voltage (V_2) are listed in Table 5.5.

Table 5.5 Equivalent floating resistance (R_{Feq}) for different values of V_2

V_2 (V)	R_{Feq} (KΩ)
-0.3	9.21
-0.15	8.84
0	8.69
0.15	8.43
0.3	8.21

5.3.3 SIMULATION RESULTS OF FILTERS

The proposed OTA is used to develop first and second order low pass, high pass and band pass filters. These filters are simulated using UMC 0.18µm CMOS process technology parameters. Fig. 5.9 shows the frequency response of the first order low pass filter using proposed OTA for various values of bias current ranging from 120µA to 200µA with the increment of 20µA.

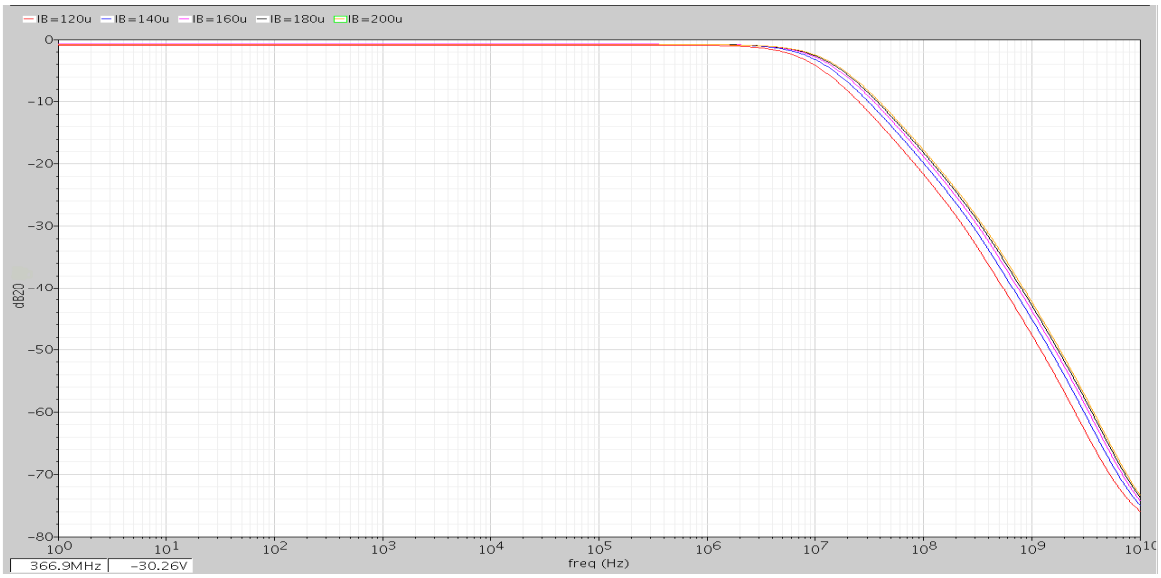


Fig. 5.9 Frequency response of first order low pass filter

The frequency response of second order low pass filter using proposed OTA is shown in Fig. 5.10. This plot also shows the comparison of first and second order low pass filter.

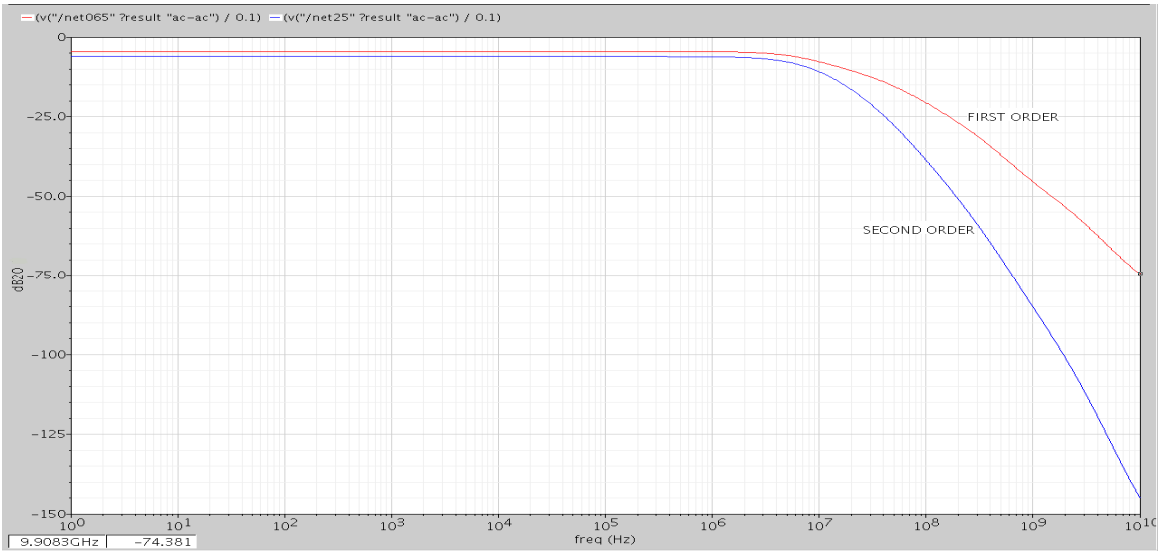


Fig. 5.10 Frequency response of second order low pass filter

The frequency response of the first order high pass filter using proposed OTA for various values of bias current ranging from 120µA to 200µA with the increment of 20µA is shown in Fig. 5.11.

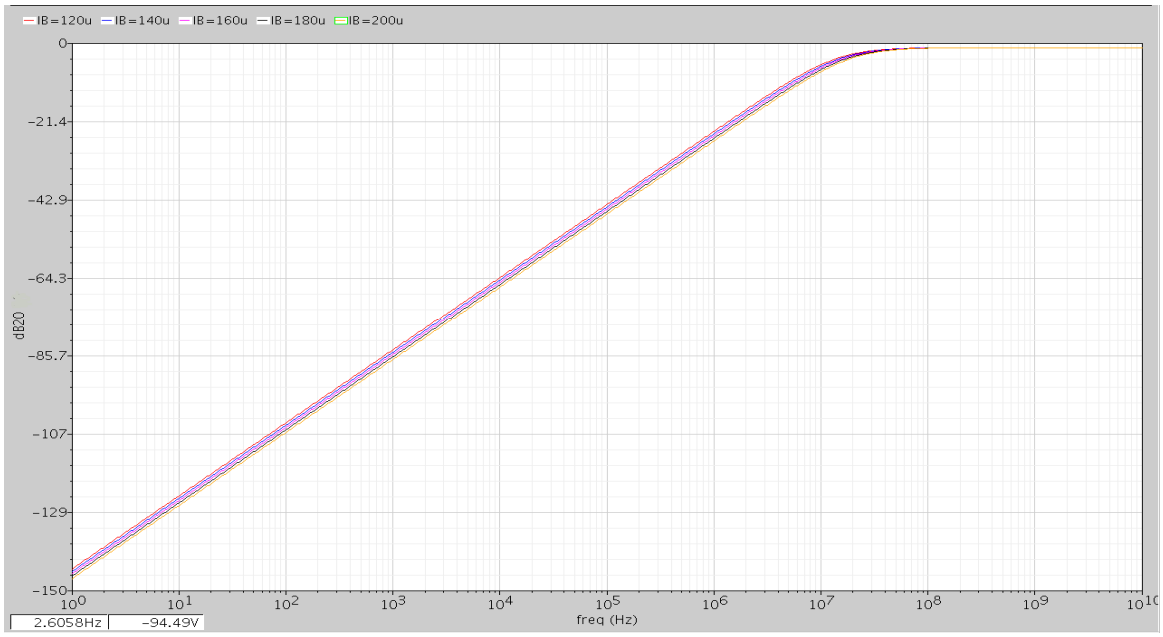


Fig. 5.11 Frequency response of first order high pass filter

The frequency response of second order high pass filter using proposed OTA is shown in Fig. 5.12. This plot also shows the comparison of first and second order high pass filter.

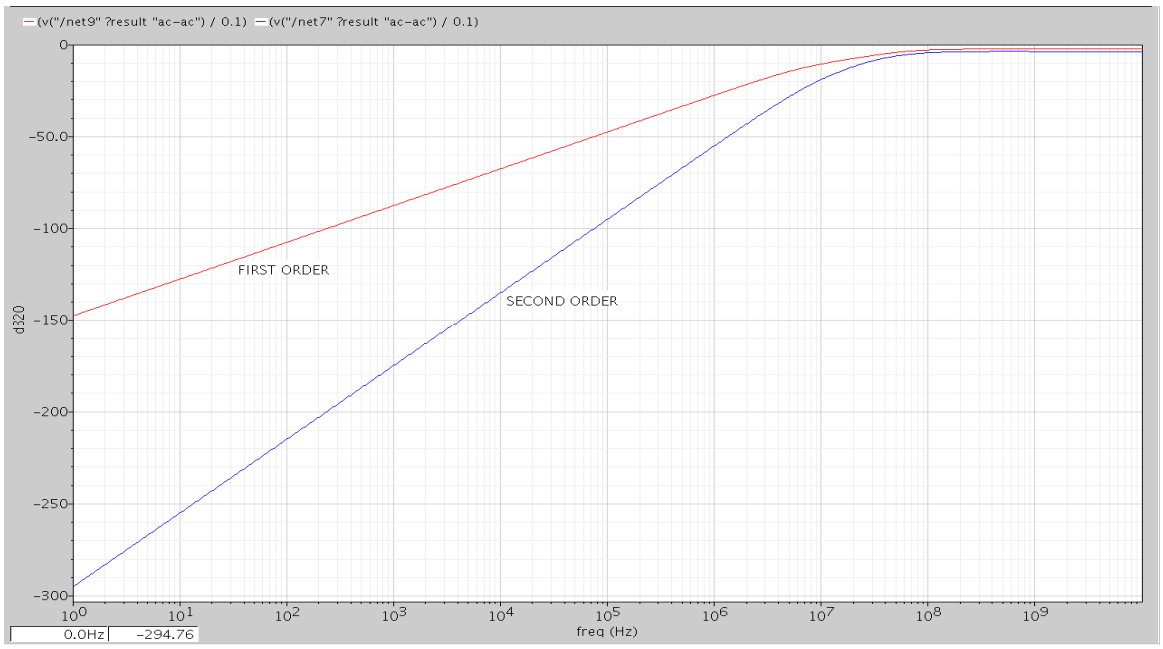


Fig. 5.12 Frequency response of second order high pass filter

The frequency response of the first order band pass filter using proposed OTA for various values of bias current ranging from 120µA to 200µA with the increment of 20µA is shown in Fig. 5.13.

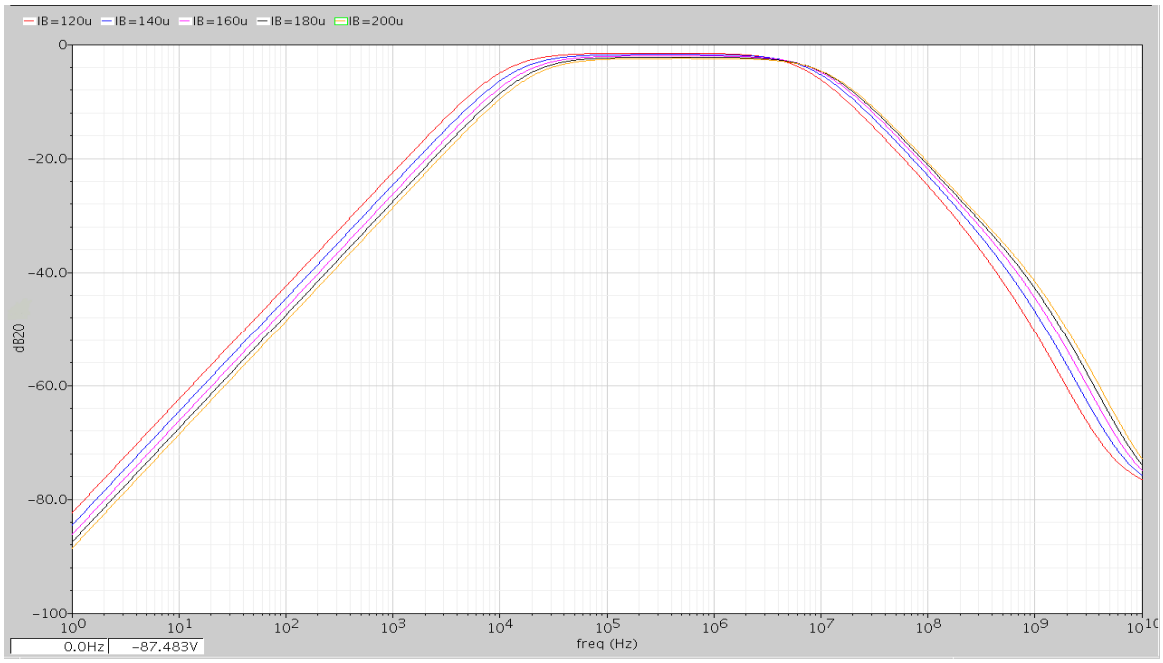


Fig. 5.13 Frequency response of first order band pass filter

The frequency response of second order band pass filter using proposed OTA is shown in Fig. 5.14. This plot also shows the comparison of first and second order band pass filter.

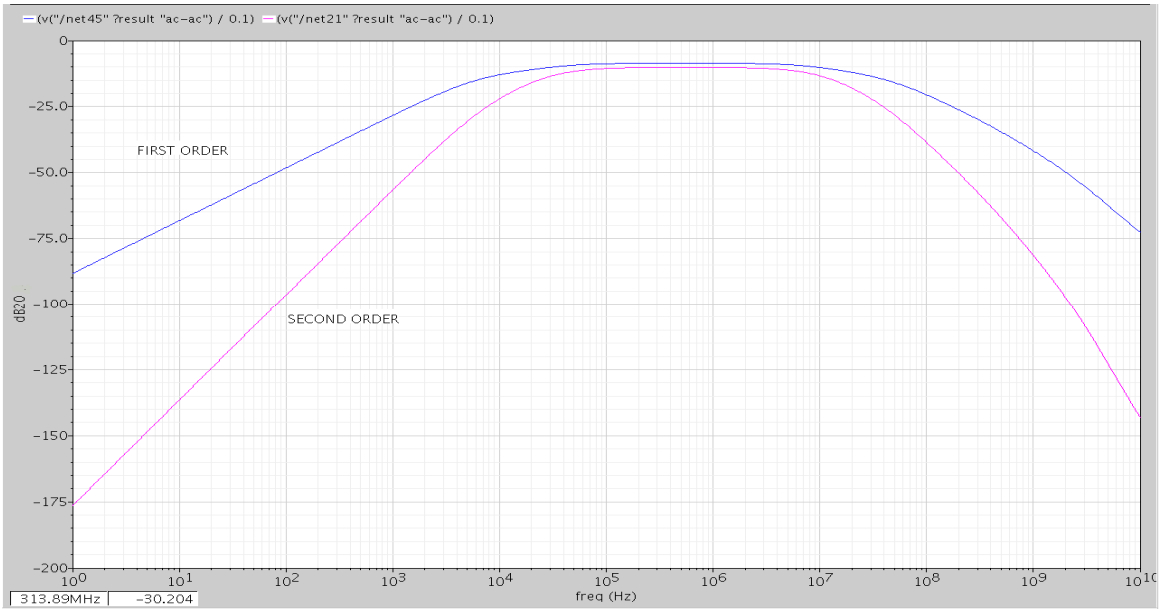


Fig. 5.14 Frequency response of second order band pass filter

5.4 LAYOUT OF PROPOSED HIGHLY LINEAR FLOATING GATE MOSFET BASED SOURCE-DEGENERATED OTA

The physical layout of proposed highly linear floating gate MOSFET based source-degenerated OTA has been designed using UMC 0.18µm CMOS process technology in Cadence Virtuoso XL layout editor. Design Rule Check (DRC) is performed in order to verify that layout fulfills all electrical and geometric rules provided by foundry. The basic design rules are:

Metal 1 to metal 1 spacing	0.24µm
Minimum contact size	0.24µm * 0.24µm
Poly to poly spacing	0.24µm
Poly to metal spacing	0.28µm
Contact overlap to p+ diffusion	0.1µm
Metal 1 width	0.24µm
Poly extension beyond active	0.22µm
Minimum contact spacing	0.26µm
N well overlap p+ diffusion	0.43µm
Diffusion contact to poly spacing	0.15µm
Minimum p+ implant overlap p+ diffusion	0.22µm
Poly width	0.18µm
Minimum poly extension on to field region	0.22µm
Poly contact to diffusion edge spacing	0.18µm
Minimum poly overlap contact	0.1µm
Minimum metal area	$0.1764\mu m^2$
Minimum metal2 width	0.28µm
Metal1 and metal2 overlap over via	0.08µm

The layout of proposed highly linear floating gate MOSFET based source-degenerated OTA is shown in Fig. 5.15.

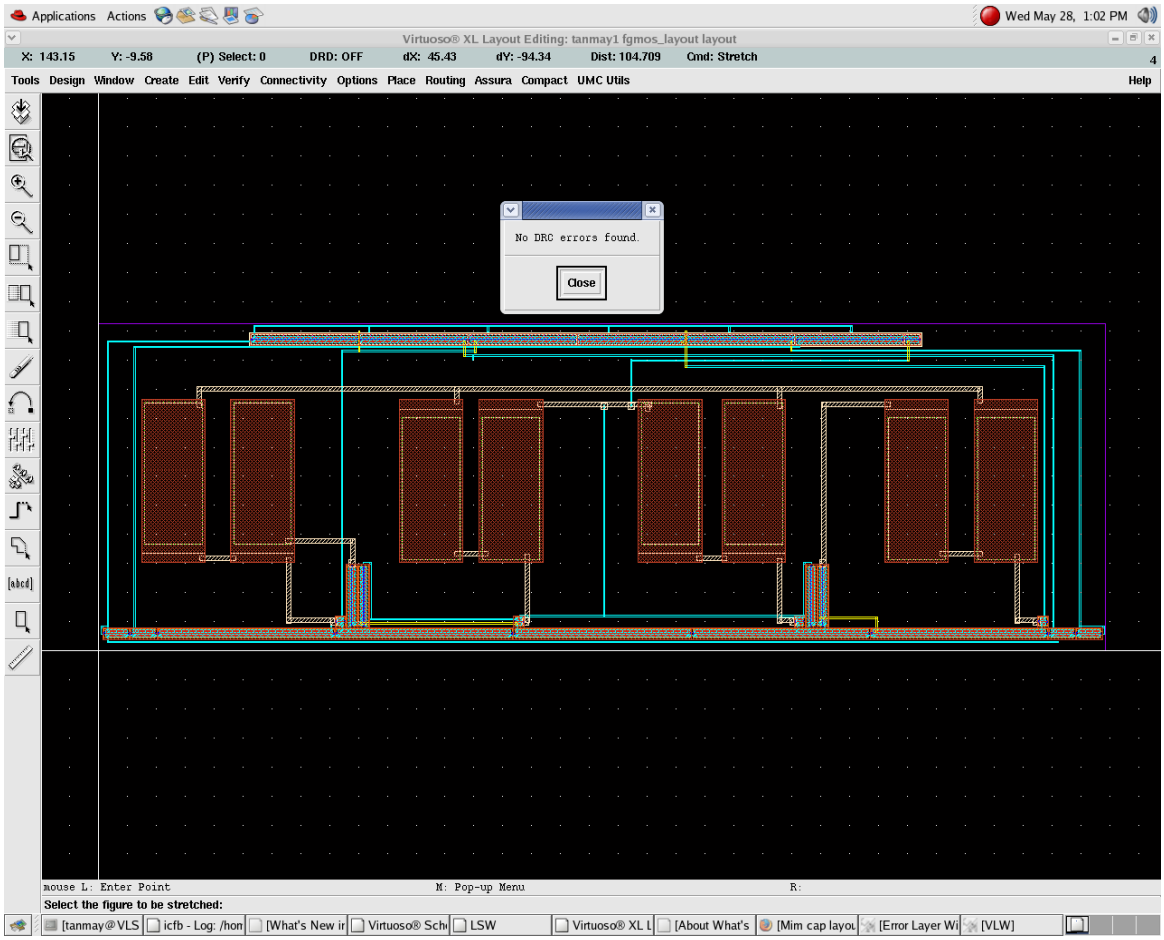


Fig. 5.15 Layout of the proposed OTA

The comparison between the performance parameters of proposed highly linear floating gate MOSFET based source-degenerated OTA with the existing OTAs available in literature is listed in Table 5.6. From the table it is observed that the proposed circuit has rail-to-rail input voltage range with low power supply and high bandwidth.

Table 5.6 Comparison of proposed OTA with other OTAs available in literature

Circuit Parameter	Year	CMOS Tech. (μm)	Power Supply (V)	G_m (μA/V)	Bandwidth (MHz)	Input Range (Vpp)	Power Consumption (mW)	THD (db) @freq (MHz) @i/p (Vpp)
[17]	2008	0.35	2	1400	600	-	1.2	-60@10@-
[31]	2009	0.18	±0.9	22	-	1	0.057	-
[32]	2011	0.13	1.5	40	65	0.9	0.126	-110@0.001@0.35
[33]	2014	0.18	0.8	27	-	0.8	31.2	-40@1@0.8
[34]	2001	0.35	3.3	40	5	2	1	-57@0.001@1.6
[38]	2004	0.8	1.5	155	40	0.6	0.042	-55@5@0.1
[39]	2005	0.8	2	266	175	0.6	0.160	-48@0.001@0.4
[41]	2009	0.5	±1.5	850	750	0.4	20	-
[45]	2006	0.5	±1.5	46	-	3	2.6	-60@0.1@3
[47]	2011	0.18	0.5	245	10	0.5	0.11	-45@5@0.4
[49]	2009	0.18	0.7	-	-	1.4	0.010	-35@5@0.4
Proposed Work	2014	0.18	±0.6	75.5	1472	1.2	0.56	-42@5@1

5.5 CONCLUSIONS

The simulation results of proposed highly linear floating gate MOSFET based source-degenerated OTA are presented. The designed OTA has also been compared with the existing OTAs available in literature and the proposed OTA has rail-to-rail input range with ±0.6V power supply and has transconductance gain of 75.5μA/V with 1.47GHz bandwidth. The layout of the proposed OTA has also been also presented.

CHAPTER

CONCLUSIONS AND FUTURE SCOPE

6.1 CONCLUSIONS

In this dissertation, a highly linear floating gate MOSFET based source-degenerated OTA is developed. The proposed OTA utilizes floating gate MOSFETs to reduce the power supply requirement of the circuit and source-degeneration technique is used to increase the linearity of the designed OTA. The proposed OTA operates at ±0.6V power supply. The circuit has rail-to-rail input voltage range with transconductance gain of 75.5μA/V. The 3db bandwidth of the designed OTA is 1.47GHz. The circuit has the THD of -42db at 1MHz for $0.6V_{pp}$ input differential voltage. The proposed OTA is used to develop some applications such as active inductor, tunable resistors and filters. The simulation results of these applications are also presented. The physical layout of the proposed OTA is designed in Cadence virtuoso layout editor using UMC 0.18μm CMOS process technology. The proposed circuit has been compared with the existing OTAs available in literature and it has been observed that the proposed OTA has wide input voltage differential range and low power supply requirement. The bandwidth of the designed OTA is better than the other OTAs available in literature.

6.2 FUTURE SCOPE

Some ideas and suggestions for the future work:

- The voltage gain of the proposed circuit can be increased by using different voltage gain enhancement techniques such as positive feedback with feed-forward, negative impedance compensation, self-cascoding, etc.
- Different techniques such as active-error feed-forward, mobility compensation, etc can be used to improve the THD of the circuit proposed in this dissertation.

- The bandwidth of the proposed OTA can be enhanced by using resistive compensation technique.

REFERENCES

[1] C. J. B. Fayomi, M. Sawan and G. W. Roberts, "Reliable Circuit Techniques for Low Voltage Analog Design in Deep Submicron Standard CMOS: A Tutorial," *Analog Integrated Circuits and Signal Processing*, vol.39, pp. 21-38, April 2004.

[2] P. R. Gray, P. J. Hurst, S. H. Lewis and R. G. Meyer, "Analysis and Design of Analog Integrated Circuits," *4th Edition, John Wiley and Sons, New York*, 2001.

[3] "The International Technology Roadmap for Semiconductors," ITRS, 2011, Tech. Rep. http://public.itrs.net.

[4] S. Chatterjee, K. P. Pun, N. Stanic, Y. Tsividis and P. Kinget, "Analog circuit Design Techniques at 0.5V", *Springer*, ISBN. 0387699538, 2007.

[5] E. Sanchez-Sinencio, and A.G. Andreou, "Low Voltage/Low Power Integrated Circuits and Systems: Low-Voltage Mixed-Signal Circuits," *IEEE Press, New York*, 1999.

[6] S. Yan, E. Sanchez-Sinencio, "Low Voltage Analog Circuit Design Techniques: A Tutorial," *IEICE Transactions on Fundamentals of Electronics, Communications and Computer Sciences*, pp. 179-196, 2000.

[7] S.S. Rajput, S.S. Jamuar, "Low Voltage Analog Circuit Design Techniques," *IEEE Circuits and Systems Magazine*, vol. 2, no. 1, pp. 24-42, 2002.

[8] Ramirez-Angulo, J., S. C. Choi, and G. Gonzalez-Altamiran, "Low Voltage Circuits Building Blocks Using Multiple Input Floating Gate Transistors," *IEEE Transactions on Circuits and Systems. 1, Fundamental Theory and Applications*, vol. 42, no. 11, pp. 971-974, 1995.

[9] S. Sharma, S.S. Rajput, L.K. Magotra, and S.S. Jamuar, "FGMOS Based Wide Range Low Voltage Current Mirror and Its Applications," *Asia-Pacific Conference on Circuits and Systems, APCCAS'02*, vol. 2, pp. 331-334. *IEEE*, 2002.

[10] R. Pandey and M. Gupta, "FGMOS Based Voltage-Controlled Grounded Resistor," *Radioengineering Journal*, vol.19, no.3, pp 455-459, 2010.

[11] H. Voorman and H. Veenstra, "Tunable High-Frequency Gm-C Filters," *IEEE Journal of Solid-State Circuits*, vol. 35, no. 8, pp. 1097–1108, August 2000.

[12] E. Sànchez-Sinencio, R.L. Gieger and H. Nevarez-Lozano, “Generation of Continuous-Time Two Integrator Loop OTA Filter Structures,” *IEEE Transaction on Circuits and Systems*, vol. 35, no. 8, pp. 936-946, August 1988.

[13] F. Rezaei and S.J. Azhari, “Ultra Low Voltage, High Performance Operational Transconductance Amplifier and Its Application in a Tunable Gm-C Filter,” *Microelectronics Journal*, vol. 42, Issue 6, pp. 827-836, June 2011.

[14] T. Ohbuchi and F. Matsumoto, “A New Design of a Linear Local Feedback MOS Transconductor for Low Frequency Applications,” *Analog Integrated Circuits and Signal Processing*, vol. 75, Issue 2, pp. 257-266, May 2013.

[15] T Kim and B Kim. "A L3-Db IIP3 Improved Low-Power CMOS RF Programmable Gain Amplifier Using Differential Circuit Transconductance Linearization for Various Terrestrial Mobile D-TV Applications," *IEEE Journal of Solid-State Circuits*, vol. 41, pp. 945-953, 2006.

[16] H.H. Nguyen, Q.H. Duong, H.B. Le, J.S. Lee and S.G. Lee, ”Low-Power 42 db-Linear Single Stage Digitally-Controlled Variable Gain Amplifier,” *Electronics Letters*, vol.44, no.13, pp. 780-782, 2008.

[17] B. Calvo, S. Celma, M.T. Sanz, J.P. Alegre and F. Aznar, “Low-Voltage Linearly Tunable CMOS Transconductor with Common-Mode Feed-forward,” *IEEE Transaction on Circuit and Systems-I*, vol. 55, no. 3, pp. 715 -721, 2008.

[18] S. Sengupta, “Adaptively Biased Linear Transconductor,” *IEEE Transaction on Circuits and Systems: 1 regular papers*, vol. 52, no. 11, pp. 2369–2375, November 2005.

[19] E. Sanchez-Sinencio, and J. Silva, “CMOS Transconductance Amplifiers, Architectures and Active Filters: A Tutorial,” *Proc. Proceedings of The IEE Circuits Devices and Systems*, vol.147, no. 1, pp. 3–12, 2000.

[20] V. Srinivasan, D. W. Graham and P. Hasler, "Floating-Gates Transistors for Precision Analog Circuit Design: An Overview," *48th Midwest Symposium on Circuits and Systems*, vol. 1, pp.71-74, 2005.

[21] F. Masuoka, R. Shirota, and K. Sakui, “Reviews and Prospects of Non-volatile Semiconductor Memories,” *IEICE Transaction.*, vol. E 74-C, no. 4, pp. 868-874, April 1991.

[22] S. Lai, “Flash Memories: Where we were and where we are going,” *IEDM Digest, San Francisco*, CA, 1998, pp. 971-974.

[23] E. O. R. Villegas, A. Rueda and A. Yufera, " Low Voltage Analog Filters using Floating gate MOSFETs" *IEEE Solid State Circuits Conference,* pp. 29-32, 2000.

[24] Esther Rordriguez-Villegas," Low Power and Low Voltage Circuit Design with the FGMOS Transistor*," The Institute of Engineering and Technology, London, United Kingdom*, 2006.

[25] R. Pandey and M. Gupta, "FGMOS Based Tunable Grounded Resistor," *Analog Integrated Circuits and Signal Processing*, vol.65, pp. 437-443, 2010.

[26] C.S. Park and R. Schaumann, "A High-Frequency CMOS Linear Transconductance Element," *IEEE Transaction on Circuits and Systems*, vol. 33, no.11, November 1986.

[27] S.A. Mahmoud and A.M. Soliman, "New CMOS fully differential difference transconductors and application to fully differential filters suitable for VLSI," *Microelectronics Journal,* vol. 30, no. 2, pp. 169-192, 1999.

[28] T. Deliyannis, Y. Sun and J. K. Fidler, "Continuous-Time Active Filter Design," *CRC Press,* 1998.

[29] G. Meyer-Brotz and A. Kley, "The Common-Mode Rejection of Transistor Differential Amplifiers," *IEEE Transaction Circuit Theory*, vol. 13, no. 2, pp. 171-175, June 1966.

[30] A. N. Mohieldin, E. Sanchez-Sinencio, and J. Silva-Martinez, "A Fully Balanced Pseudo-Differential OTA with Common-Mode Feed-forward and Inherent Common mode Feedback Detector," *IEEE Journal of Solid-State Circuits*, vol. 38, no. 4, pp. 663-668, April 2003.

[31] F. Matsumoto, T. Miyazawa, S. Nakamura, and Y. Noguchi, "Techniques for A Low-voltage Low-power Linear MOS Transconductor," *IEEE, International Symposium on Intelligent Signal Processing and Communication Systems,* pp. 1-4, 2009.

[32] J.M. Martinez-Heredia n and A. Torralba, "Enhanced Source-Degenerated CMOS Differential Transconductor," *Microelectronics Journal*, vol. 42, pp. 306-402, February 2011.

[33] S. Abbasalizadeh, S. Sheikhaei and B. Forouzandeh," A 0.8-V Supply Bulk-Driven Operational Transconductance Amplifier and Gm-C Filter in 0.18μm CMOS Process," *International Journal of Circuit Theory and Applications,* 2014.

[34] Ko-Chi Kuo, "A Linear MOS Transconductor Using Source Degeneration and Adaptive Biasing," *IEEE Transactions on Circuits And Systems—II: Analog and Digital Signal Processing*, vol. 48, no. 10, pp. 1293-1301, October 2001.

[35] F. Krummenacher and N. Joehl, "A 4-MHz CMOS Continuous-Time Filter with On-Chip Automatic Tuning," *IEEE Journal of Solid-State Circuits*, vol.23, pp. 750–758, June 1988.

[36] A. Nedungadi and T. R. Viswanathan, "Design of Linear CMOS Transconductance Elements," *IEEE Transaction on Circuits System*, vol. CAS-31, pp. 891–894, October. 1984.

[37] A.Worapishet and C. Naphaphan, "Current-Feedback Source-Degenerated CMOS Transconductor with Very High Linearity," *Electronics Letters*, vol. 39 no. 7, pp. 17-18, 9th January 2003.

[38] M. Laguna,C. De la Cruz-Blas, A. Torralba, R.G. Carvajal, A. Lopez-Martin and A.Carlosena, "A Novel Low-Voltage Low-Power Class-AB Linear Transconductor," *IEEE ISCAS 2004*, vol.1, pp. 725-8, 2004.

[39] Andreas Demosthenous, "Low-Voltage MOS Linear Transconductor/Squarer and Four-Quadrant Multiplier for Analog VLSI," *IEEE transactions on circuits and systems—I: regular papers*, vol. 52, no. 9, pp. 1721-1731, September 2005.

[40] K. Kaewdang and W. Surakampontorn, "On the Realization of Electronically Current-Tunable CMOS OTA," *International Journal of Electronics and Communications*, pp. 300-306, 2007.

[41] K. Kaewdang and W. Surakampontorn, "A Balanced Output CMOS OTA with Wide Linear Current Tunable Range," *International Journal of Electronics and Communications*, pp. 728-733, 2011.

[42] G. Raikos and S. Vlassis," A Versatile Technique for Linearly Tunable Transconductors," *17th IEEE International Conference on Electronics, Circuits, and Systems (ICECS)* 2010.

[43] S.K. Kar and S. Sen, "A Highly Linear CMOS Transconductance Amplifier in 180nm Process Technology," *IEEE Analog Integrated Circuits and Signal Processinlg*, vol. 72, pp. 163-171, July 2012.

[44] T. Farouk, A.N. Mohieldin and A.H. Khalil, "A Low-Voltage Low-Power CMOS Fully Differential Linear Transconductor with Mobility Reduction Compensation," *Microelectronics Journal*, vol. 63, pp. 69-76, Jan 2012.

[45] A.J. Lopez-Martin, A. Carlosena, J. Ramirez-Angulo and R. G. Carvajal, "Rail-to-Rail Tunable CMOS V-I Converter," ISCAS 2006.

[46] J. M. A. Miguel, A. J. Lopez-Martin, L. Acosta, J. Ramirez-Angulo, and R. G. Carvajal, "Using Floating Gate and Quasi-Floating Gate Techniques for Rail-To-Rail

Tunable CMOS Transconductor Design," *IEEE Transactions on Circuits and Systems I: Regular Papers,* vol. 58, no. 7, pp. 1604-1614, 2011.

[47] A. Suadet, T. Thongleam and V. Kasemsuwan, "Quasi-Floating-Gate (QFG) Inverter-Based Class-AB Linear Transconductor for Low Voltage Applications," *Proceedings of International Conference on Circuits, System and Simulation (ICCSS)* 2011.

[48] V. S. Babu, A. Sekhar, R.S. Devi, and M.R. Baiju," Floating Gate MOSFET Based Operational Transconductance Amplifier and Study of Mismatch," *4th IEEE Conference on Industrial Electronics and Applications, ICIEA* 2009.

[49] E. Farshidi, "A Low-Voltage Class-AB Linear Transconductance based on Floating-Gate MOS Technology," *IEEE Conference on Circuit Theory and Design,* pp. 437-440, 2009.

[50] R.R. Torrance, T.R. Viswanathan and J.V.Hanson, "CMOS Voltage to Current Transducers," *IEEE Transaction on Circuits and Systems,* vol. CAS-32, no. 11, November 1985.

APPENDIX A

EQUIVALENT MODEL OF FLOATING GATE MOSFET

The equivalent model of floating gate MOSFET is shown in Fig. A.1. This equivalent model is required to simulate the floating gate MOSFET by using ordinary simulator. In this model, to avoid the DC convergence problem resistors R_1, R_2,… R_N and R_{GD}, R_{GS} and R_{GB} are parallelly connected to the input capacitance C_1, C_2,…C_N, floating gate to drain parasitic capacitance C_{GD}, floating gate to source capacitance C_{GS} and floating gate to bulk capacitance C_{GB} respectively. The time constant of every branch should be same i.e.

$$R_1C_1 = R_2C_2 = \cdots = R_NC_N = R_{GD}C_{GD} = R_{GS}C_{GS} = R_{GB}C_{GB} \qquad (A.1)$$

and it is chosen in such a manner that it makes the introduced resistance as large as possible. This condition makes sure that the DC voltage at the floating gate is not affected by the introduction of resistors.

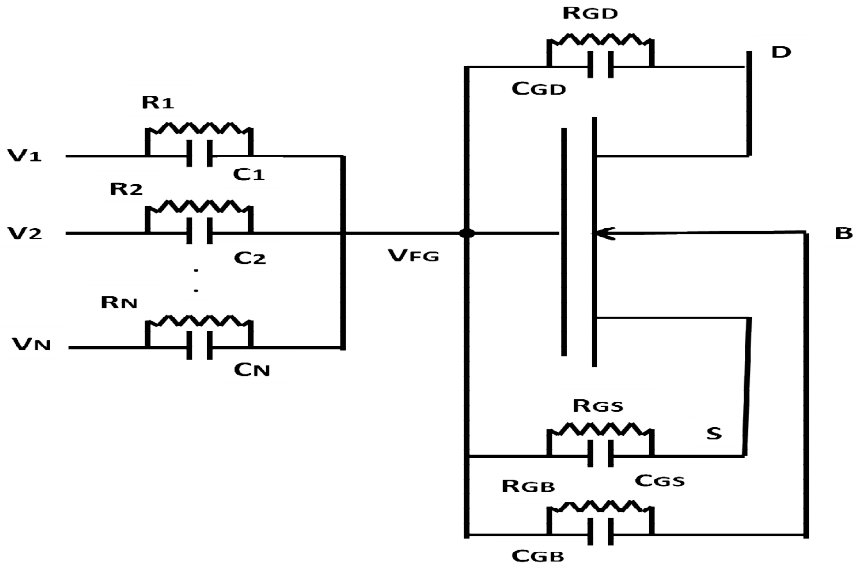


Fig. A.1 Equivalent model of floating gate MOSFET

APPENDIX B

MODELS PARAMETERS

The UMC 0.18μm CMOS technology model file is listed below:

```
model n_18_mm bsim3v3 type=n
+ version=3.2000e+00        binunit=1.0000e+00     mobmod=1.0000e+00
+ capmod=2.0000e+00         nqsmod=0.0000e+00
+ tox=4.2000e-09 + dtox_n_18_mm                      toxm=4.2000e-09
+ xj=1.6000e-07             nch=3.7446e+17           rsh=8.0000e+00
+ ngate=1.0000e+23          vth0=3.0750e-01 + dvth0_n_18_mm
+ k1=4.5780e-01             k2=-2.6380e-02           k3=-1.0880e+01
+ k3b=2.3790e-01            w0=-8.8130e-08           nlx=4.2790e-07
+ dvt0=4.0420e-01           dvt1=3.2370e-01         dvt2=-8.6020e-01
+ dvt0w=3.8300e-01          dvt1w=6.0000e+05       dvt2w=-2.5000e-02
+ lint=1.5870e-08           wint=1.0220e-08          dwg=-3.3960e-09
+ dwb=1.3460e-09            u0=3.1410e+02 + du0_n_18_mm
+ ua=-9.2010e-10            ub=1.9070e-18             uc=4.3550e-11
+ vsat=7.1580e+04           a0=1.9300e+00             ags=5.0720e-01
+ b0=1.4860e-06             b1=9.0640e-06            keta=1.7520e-02
+ a1=0.0000e+00             a2=1.0000e+00           voff=-1.0880e-01
+ nfactor=1.0380e+00        cit=-1.5110e-03          cdsc=2.1750e-03
+ cdscd=-5.0000e-04         cdscb=8.2410e-04         eta0=1.0040e-03
+ etab=-1.4590e-03          dsub=1.5920e-03          pclm=1.0910e+00
+ pdiblc1=3.0610e-03        pdiblc2=1.0000e-06    pdiblcb=0.0000e+00
+ drout=1.5920e-03          pscbe1=4.8660e+08      pscbe2=2.8000e-07
+ pvag=-2.9580e-01          rdsw=4.9050e+00          prwg=0.0000e+00
+ prwb=0.0000e+00           wr=1.0000e+00          alpha0=0.0000e+00
+ alpha1=0.0000e+00         beta0=3.0000e+01        xpart=1.0000e+00
+ cgso=2.3500e-10 + dcgso_n_18_mm
+ cgdo=2.3500e-10 + dcgdo_n_18_mm                     cgbo=0.0000e+00
+ cgsl=0.0000e+00           cgdl=0.0000e+00        ckappa=6.0000e-01
+ cf=1.5330e-10             clc=1.0000e-07           cle=6.0000e-01
+ dlc=2.9000e-08            dwc=0.0000e+00         vfbcv=-1.0000e+00
+ noff=1.0000e+00           voffcv=0.0000e+00        acde=1.0000e+00
+ moin=1.5000e+01           lmin=1.8000e-07          lmax=5.0000e-05
+ wmin=2.4000e-07           wmax=1.0000e-04
+ xl= - 1.0500e-08 + dxl_n_18_mm
+ xw=0.0000e-00 + dxw_n_18_mm                         js=1.0000e-06
+ jsw=7.0000e-11            cj=1.0300e-03 + dcj_n_18_mm
+ mj=4.4300e-01             pb=8.1300e-01
+ cjsw=1.3400e-10 + dcjsw_n_18_mm                     mjsw=3.3000e-01
+ tnom=2.5000e+01           ute=-1.2860e+00          kt1=-2.2550e-01
+ kt1l=-4.1750e-09          kt2=-2.5270e-02           ua1=2.1530e-09
+ ub1=-2.6730e-18           uc1=-3.8320e-11           at=1.4490e+04
+ prt=-1.0180e+01           xti=3.0000e+00            wl=0.0000e+00
+ wln=1.0000e+00            ww=7.2620e-16             wwn=1.0000e+00
+ wwl=0.0000e+00            ll=-1.0620e-15            lln=1.0000e+00
+ lw=2.9960e-15             lwn=1.0000e+00            lwl=0.0000e+00
+ llc=-2.1400e-15           lwc=0.0000e+00           lwlc=0.0000e+00
+ wlc=0.0000e+00            wwc=0.0000e+00           wwlc=0.0000e+00
+ lvth0= - 1.0000e-03 + dlvth0_n_18_mm
+ wvth0=6.027e-02 + dwvth0_n_18_mm          pvth0=0 + dpvth0_n_18_mm
+ lnlx=-2.8540e-08          wnlx=0.0000e+00          pnlx=0.0000e+00
+ wua=-1.8800e-11           wu0=5.4000e-01 + dwu0_n_18_mm
```

```
+ pub=3.8000e-20            pw0=1.3000e-09          wrdsw=0.0000e+00
+ weta0=0.0000e+00          wetab=0.0000e+00        leta0=1.5740e-03
+ letab=0.0000e+00          peta0=0.0000e+00        petab=0.0000e+00
+ wpclm=0.0000e+00          wvoff=-4.0780e-04      lvoff=-4.2080e-03
+ pvoff=-3.7880e-04         wa0=-4.7310e-02          la0=-4.6670e-01
+ pa0=-2.6490e-02           wags=4.2420e-03          lags=3.0280e-01
+ pags=0.0000e+00           wketa=0.0000e+00       lketa=-1.9420e-02
+ pketa=0.0000e+00          wute=6.3730e-02          lute=0.0000e+00
+ pute=0.0000e+00           wvsat=5.0660e+03        lvsat=0.0000e+00
+ pvsat=0.0000e+00 + dpvsat_n_18_mm             lpdiblc2=-4.7520e-03
+ wat=7.0670e+03            wprt=0.0000e+00          ldif=8.0000e-08
+ hdif=2.6000e-07           n=1.0000e+00            pbsw=8.8000e-01
+ cjswg=5.0000e-10 + dcjgate_n_18_mm                ctp=9.1400e-04
+ ptp=9.2400e-04            cta=9.1900e-04           pta=1.5800e-03
+ elm=5.0000e+00            tlevc=1.0000e+00
+ noimod=2                  noia=1.3182567385564E+19
noib=144543.977074592
+ noic=-1.24515794572817E-12                         ef=0.92
+ em=41000000
```

```
model p_18_mm bsim3v3 type=p
+ mobmod=3.0000e+00         version=3.2000e+00     capmod=2.0000e+00
+ binunit=1.0000e+00        nqsmod=0.0000e+00
+ tox=4.2000e-09 + dtox_p_18_mm                      toxm=4.2000e-09
+ xj=1.0000e-07             nch=6.1310e+17          ngate=1.0000e+23
+ vth0= - 4.5550e-01 + dvth0_p_18_mm                 k1=5.7040e-01
+ k2=6.9730e-03             k3=-2.8330e+00          k3b=1.3260e+00
+ w0=-1.9430e-07            nlx=2.5300e-07          dvt0=4.8850e-01
+ dvt1=7.5780e-02           dvt2=1.2870e-01        dvt0w=-1.2610e-01
+ dvt1w=2.4790e+04          dvt2w=6.9150e-01         lint=-1.0410e-08
+ wint=-1.5250e-07          dwg=-1.1510e-07          dwb=-1.0390e-07
+ u0=1.1450e+02 + du0_p_18_mm                         ua=1.5400e-09
+ ub=2.6460e-19             uc=-9.5870e-02          vsat=5.3400e+04
+ a0=1.3500e+00             ags=3.8180e-01           b0=-3.0880e-07
+ b1=0.0000e+00             keta=1.0440e-02          a1=0.0000e+00
+ a2=1.0000e+00             voff=-1.0730e-01      nfactor=1.5350e-00
+ cit=-1.0670e-03           cdsc=7.5780e-04         cdscd=-2.8830e-05
+ cdscb=1.0000e-04          eta0=1.0710e+00          etab=-9.2910e-01
+ dsub=1.9191e+00           pclm=2.6530e+00       pdiblc1=0.0000e+00
+ pdiblc2=5.0000e-06        pdiblcb=0.0000e+00      drout=1.4570e+00
+ pscbe1=4.8660e+08         pscbe2=2.8000e-07        pvag=1.1620e+00
+ rdsw=7.9210e+02           prwg=0.0000e+00          prwb=0.0000e+00
+ alpha0=0.0000e+00         alpha1=0.0000e+00       beta0=3.0000e+01
+ cgdo=2.0540e-10 + dcgdo_p_18_mm                     cgbo=0.0000e+00
+ cgso=2.0540e-10 + dcgso_p_18_mm                    xpart=1.0000e+00
+ cf=1.5330e-10             dlc=5.6000e-08           cgsl=0.0000e+00
+ cgdl=0.0000e+00           ckappa=6.0000e-01         clc=1.0000e-07
+ cle=6.0000e-01            dwc=0.0000e+00         vfbcv=-1.0000e+00
+ noff=1.0000e+00           voffcv=0.0000e+00        acde=1.0000e+00
+ moin=1.5000e+01           lmin=1.8000e-07          lmax=5.0000e-05
+ wmin=2.4000e-07           wmax=1.0000e-04
+ xl= - 2.0000e-09 + dxl_p_18_mm
+ xw=0.0000e+00 + dxw_p_18_mm                         js=3.0000e-06
+ jsw=4.1200e-11            cj=1.1400e-03 + dcj_p_18_mm
+ mj=3.9500e-01             pb=7.6200e-01
+ cjsw=1.7400e-10 + dcjsw_p_18_mm                     mjsw=3.2400e-01
+ tnom=2.5000e+01           ute=-4.4840e-01          kt1=-2.1940e-01
+ kt1l=-8.2040e-09          kt2=-9.4870e-03           ua1=4.5710e-09
+ ub1=-6.0260e-18           uc1=-9.8500e-02           at=1.2030e+04
+ prt=0.0000e+00            xti=3.0000e+00            ww=1.2360e-14
+ lw=-2.8730e-16            ll=6.6350e-15             wl=0.0000e+00
+ wln=1.0000e+00            wwn=1.0000e+00            wwl=0.0000e+00
+ lln=1.0000e+00            lwn=1.0000e+00            lwl=0.0000e+00
+ llc=-7.4500e-15           lwc=0.0000e+00           lwlc=0.0000e+00
+ wlc=0.0000e+00            wwc=0.0000e+00           wwlc=0.0000e+00
+ lvth0=4.4000e-03 + dlvth0_p_18_mm
+ wvth0= - 1.4800e-02 + dwvth0_p_18_mm
+ pvth0=3.2000e-03 + dpvth0_p_18_mm                  lnlx=-1.5840e-08
+ wrdsw=1.0070e+01          weta0=0.0000e+00        wetab=0.0000e+00
+ wpclm=0.0000e+00          wua=2.6300e-09           lua=-8.1530e-11
+ pua=5.8550e-11            wub=0.0000e+00           lub=0.0000e+00
+ pub=0.0000e+00            wuc=0.0000e+00           luc=0.0000e+00
+ puc=0.0000e+00            wvoff=-9.8160e-03      lvoff=-9.8710e-04
+ pvoff=-9.8330e-05         wa0=-4.8070e-02          la0=-2.8100e-01
+ pa0=8.6610e-02            wags=-4.1770e-02         lags=4.4540e-02
+ pags=-4.0760e-02          wketa=0.0000e+00       lketa=-1.2000e-02
+ pketa=0.0000e+00          wute=-2.6820e-01         lute=0.0000e+00
+ pute=0.0000e+00           wvsat=-1.4200e+04       lvsat=0.0000e+00
+ pvsat= - 4.3400e+02 + dpvsat_p_18_mm           lpdiblc2=3.0120e-03
+ cjswg=4.200e-10 + dcjgate_p_18_mm                   wat=-6.4050e+03
+ wprt=2.1660e+02           n=1.0000e+00             pbsw=6.6500e-01
+ cta=1.0000e-03            ctp=7.5300e-04           pta=1.5500e-03
```

```
+ ptp=1.2400e-03            ldif=8.0000e-08           rsh=8.0000e+00
+ rd=0.0000e+00             rsc=0.0000e+00            rdc=0.0000e+00
+ hdif=2.6000e-07           rs=0.0000e+00
+ noimod=2                  noia=3.57456993317604E+18 noib=2500
+ noic=2.61260020285845E-11 ef=1.1388
+ em=41000000
```