

DESIGN OF LOW-VOLTAGE CURRENT MIRRORS USING FLIPPED VOLTAGE FOLLOWER CELL

A Dissertation Submitted In Partial Fulfilment of the Required for the Degree of

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In
VLSI Design

Submitted By

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DECLARATION

I hereby declare that the work which is being presented in the dissertation titled "**DESIGN OF LOW-VOLTAGE CURRENT MIRRORS USING FLIPPED VOLTAGE FOLLOWER CELL**" in the partial fulfilment of the requirement for the award of degree of Master of Technology in VLSI Design submitted in Electronics and Communication Engineering Department of Thapar university, Patiala is an authentic record of my study carried out as under the guidance of **Dr. Rishikesh Pandey** (Assistant Professor, ECED) during 2013-2015.

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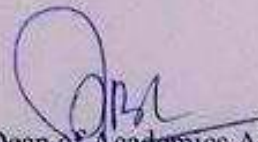

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ABSTRACT

The desire for portability of electronics equipment generated a need for low voltage/ low power system in battery products like hearing aids, implantable cardiac pacemakers, cell phones and hand held multimedia terminals.

The dissertation discusses the basic cell known as “Flipped voltage follower” for low voltage/low power operation and includes the benefits of flipped voltage follower over conventional voltage follower. In this work, a new low-voltage current mirror (LVCM) is proposed. The circuit has low power supply requirement of 1.2V, wide input current range of 0-100 μ A, low DC error of 5.7%, low DC power dissipation of 111.20 μ W and low input impedance of 14.1 K Ω . Flipped voltage follower based low-voltage current mirror I (FVFLVCM I) has also been proposed to reduce voltage supply requirement of the current mirror. The proposed FVFLVCM I has wide input current range of 0-50 μ A, low DC error of 2.26%, low DC power dissipation of 36.74 μ W, low input impedance of 1.84 K Ω and low voltage supply requirement of 1V. In addition, the flipped voltage follower based low-voltage current mirror II (FVFLVCM II) has been proposed in order to improve input current range, DC error and bandwidth. The FVFLVCM II has low power supply requirement of 1.2V, wide input current range of 0-150 μ A, low DC error of 3.7%, low DC power dissipation of 99.40 μ W, high bandwidth of 629MHz and low input impedance of 30.08 K Ω . The stability of the proposed circuits has been performed by time-domain approach and frequency domain approach using Routh-Hurwitz stability criteria and phase margin calculations, respectively. The bandwidth of all the proposed current mirrors has also been enhanced using resistive and active compensation techniques. The applications such as LDPC decoder, adder and subtractor are also designed. The results have been simulated using SPICE in the TSMC 0.18 μ m CMOS technology and are presented to validate the effectiveness of the proposed current mirrors.

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LIST OF SYMBOLS

g_m	Transconductance
K	Process Transconductance
W	Width
L	Length
I	Current
V	Voltage
V_T	Threshold Voltage
R	Resistance
C	Capacitance
$B.W$	Bandwidth
D_i	Timing Delay
V_{DD}	Supply Voltage

ABBREVIATIONS

MOS	Metal Oxide Semiconductor
CM	Current Mirror
CMOS	Complementary Metal Oxide Semiconductor
VLSI	Very Large Scale Integration
FVF	Flipped Voltage Follower
CVF	Conventional Voltage Follower
LDO	Low Drop Out
OTA	Operational Transconductance Amplifier
LDPC	Low Density Parity Check
LVCM	Low-Voltage Current Mirror
FVFLVCM	Flipped Voltage Follower based Low-Voltage Current Mirror
SPICE	Simulation Program with Integrated Circuit Emphasis
TSMC	Tiawan Semiconductor Manufacturing Company
LSFVF	Level Shifter using Flipped voltage follower
FFVF	Folded Flipped Voltage Follower
CFVF	Cascoded Flipped Voltage Follower
FVFCS	Flipped Voltage Follower Current Sensors
DFVF	Differential Structure based on Flipped Voltage Follower
CCII	Second Generation Current Conveyor
R H	Routh Hurwitz Stability Criteria

CHAPTER

1

INTRODUCTION

Due to downscaling of CMOS analog circuits are operating with continuously decreasing supply voltages. This process is done in order to reduce power consumption of the digital circuits in mixed-mode very large-scale integration (VLSI) systems and to prevent breakdown of oxide with decrease in gate-oxide thickness. Low supply voltages requirements and low power consumption are the main need of the portable electronic market. There are several techniques to reduce supply voltage requirements in analog and mixed-signals circuits, some of them are folding, current-mode processing and subthreshold operation of MOS transistors, floating-gate techniques, and triode-mode [1]–[5].

In this chapter, a voltage follower with low voltage supply requirement and high slew rate known as “Flipped voltage follower cell” is discussed along with basic low- voltage current mirror. The motivations of the dissertation are also presented, followed by key contribution which describes the main objective, achieved in the dissertation. Lastly, the chapter wise flow of the dissertation is discussed.

1.1 Flipped voltage follower

A basic cell for low-power and/or low voltage operation is discussed. It is shown how different topologies of flipped voltage follower (FVF) can be used for many applications. The basic topologies derived from the FVF are also discussed. A design showing the application of the FVF to build systems based on translinear loops is described which shows the

flexibility of this cell to design the high-performance low-power/low-voltage analog and mixed-signal circuits.

The common drain amplifier is shown in Figure 1.1, known as a voltage buffer. If body effect is ignored the circuit follows the input voltage with a dc level shift, i.e., $V_o = V_i + V_{SG}$ where V_{SG} is the source-to-gate voltage of transistor. Considering large-signal behaviour, this circuit can source a large current from the load, but its sinking capability is restricted by the biasing current source. Dependency of the circuit on the output current is considered as a drawback of this circuit; hence, for resistive loads and capacitive loads at high frequencies, the unity voltage gain can't be achieved. The circuit shown in Figure 1.2 also works as a source follower, having the current through transistor constant, independent on the output current. It could be explained as a voltage follower with shunt feedback. Ignoring the short-channel effect and body effect, voltage gain can be achieved unity. The circuit in Figure 2 (unlike the conventional voltage follower) is able to sink a large amount of current, but its source capability is limited by the biasing current source. The large sinking capability is because of the low output impedance.

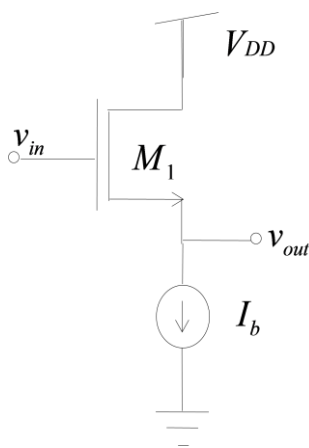


Figure 1.1 Conventional voltage follower [6]

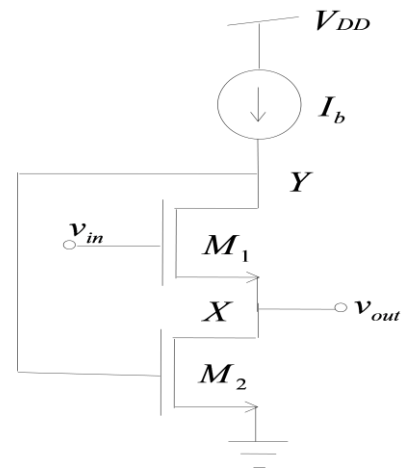


Figure 1.2 Flipped voltage follower [6]

1.1.1 Input voltage:

The FVF can be used with very low voltage supply requirement. The FVF can also be operated with a large supply voltage requirement, but biasing the transistor M1 in saturation can be difficult if the input voltage is taken to be low. If the circuit in Figure 1.2 is

considered, the relation can be obtained as: $V_{GSM2} = V_{DSM2} + V_{DSM1}$. Considering the transistor M1 is in saturation and ignoring second-order effects, the saturation condition for transistor M2 is given by [6]

$$V_{DSM2} = V_{DD} - \left(V_i + V_{mM1} + \sqrt{\frac{2I_o}{Kn(W/L)_{M1}}} \right) > \sqrt{\frac{2I_o}{Kn(W/L)_{M2}}} \quad (1)$$

where, I_o is the drain current (I_b in this case) and V_m is the transistor threshold voltage.

In the same way, assuming that transistor M2 is biased in saturation, the condition of saturation for transistor M1 is evaluated by as:

$$V_{GSM1} - V_{DSM1} = V_{DD} - \left(V_{mM2} + \sqrt{\frac{2I_o}{Kn(W/L)_{M2}}} \right) - V_i < V_{mM1} \quad (2)$$

The valid region of operation for the input signal is limited by:

$$V_{mM1} + \sqrt{\frac{2I_o}{Kn}} \left(\sqrt{\frac{1}{(W/L)_{M1}}} + \sqrt{\frac{1}{(W/L)_{M2}}} \right) < V_{DD} - V_i < V_{mM1} + V_{mM2} + \sqrt{\frac{2I_o}{Kn}} \sqrt{\frac{1}{(W/L)_{M2}}} \quad (3)$$

1.1.2 Output impedance:

It can be noted that M2 provides shunt feedback and that M1 and M2 form a two pole negative feedback loop. Figure 1.2 shows the same circuit with the feedback loop open at the gate of M2 and including a test voltage source V_T . This circuit has an open-loop gain $A_{ol} = -g_{m2}R_{OLY}$ (where the open-loop resistance at node is given by Y, $R_{OLY} \approx r_b \parallel g_{m1}r_{o1}r_{o2}$), a dominant pole at node Y, $R_{OLY} \omega_{pY} = 1/C_Y R_{OLY}$ and a high-frequency pole at node X, $\omega_{pX} = 1/C_X R_{OLX}$ (where the open-loop resistance at node X is given by $R_{OLX} \approx (1 + r_b / r_{o1}) / g_{m1} \parallel r_{o2}$ and C_X and C_Y are the parasitic capacitances at nodes X and Y respectively (C_X also includes the load capacitor, if any). The closed-loop resistance at node X is given by [6]:

$$R_{CLX} = \frac{R_{OLX}}{1 + |A_{OL}|} \sim \frac{\frac{1}{g_{m1}} \left(1 + \frac{r_b}{r_{o1}} \right) \parallel r_{o2}}{g_{m2} (r_b \parallel g_{m1} r_{o1} r_{o2})} \quad (4)$$

1.2 Low- voltage current mirror

A current mirror is a building block which is commonly used in analog and mixed mode VLSI circuits. A high input voltages are required by almost all high impedance CMs reported so far [7-8], which increase the capability of high output voltage signal swing. The performance of the current mirror can be determined by the accuracy and output impedance. A current mirror can be described as a current controlled current source which can be used to attenuate and amplify the reference current. The current mirrors source/sink must be designed to have infinite output impedance and capable to generate and draw a constant current over a wide range of voltages [9]. However, keeping value of output resistance finite and limiting output voltage in order to keep device in saturation will ultimately result in lowering of performance of the current mirrors. It is a two terminal device in which output current at any instant is known to be independent of voltage applied across its output terminals and depends on the input current/reference current [10]. It allows replication of the current, which has no sensitivity to variations in power supply and temperature [11].

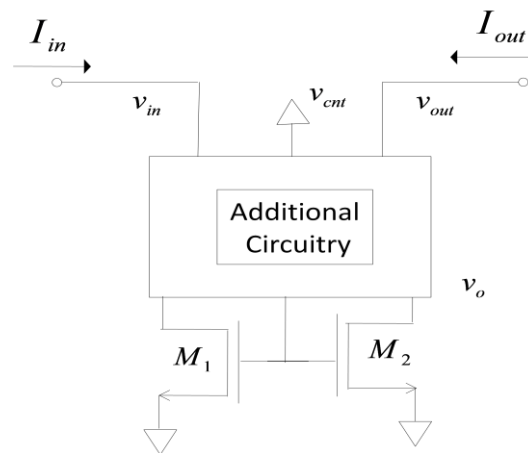


Figure 1.3 Basic block diagram of current mirror

1.3 Motivation

The low voltage circuits are commonly used in portable and mobile equipment. The applications of low voltage low power circuits in non-portable equipment are advancing because of reduction in the equipment weight and power consumption. The design of low voltage circuit structures is also carried out through current mirrors as basic element [12] and many low voltage current mirror structures have been developed [13-15]. Current mirrors are employed in many applications such as operational amplifiers, analog to digital (ADC) converters, digital to analog converters, multipliers, differential amplifiers [16], etc.

Voltage follower is one of the most widely used building blocks in analog and mixed-signal circuits [17]. As the modern deep submicron CMOS technologies have decreased, the requirement to design low power high speed MOS voltage buffers has increased rapidly. A voltage buffer having high slew-rate and low static power consumption is introduced known as flipped voltage follower (FVF) [6]. A FVF cell operates at low supply voltage requirement and has almost unity gain (the short-channel effects is ignored), which is performance wise found to be better than that of conventional voltage followers. The FVF cell has been used in current sensors [17], OTAs [18], instrumentation amplifiers [19], current mirrors [20, 21], arithmetic circuits [22] and many more low-voltage and/or low-power applications [17–22].

1.4 Key contribution

The work in this dissertation can be summarized as follows:

1. Design and simulate the proposed low-voltage current mirrors.
2. Design and simulate the low-voltage current mirrors using various compensations techniques in order to enhance the bandwidth.
3. Stability analysis and verification of proposed low-voltage current mirror.
4. Design and simulate the applications of proposed low-voltage current mirrors.

In this dissertation, low-voltage current mirrors namely low-voltage current mirror (LVCM), flipped voltage follower based low-voltage current mirror I (FVFLVCM I) and flipped voltage follower based low-voltage current mirror II (FVFLVCM II) are proposed. Various compensation techniques such as Resistive compensation and active compensation

techniques have been implemented in order to improve bandwidth of proposed circuits. Stability analysis is carried out by considering time domain and frequency domain approaches. The proposed circuits can be used in the various applications such as LDPC decoder, adder circuit, subtractor circuits etc. The results have been simulated using SPICE in the TSMC 0.18 μm CMOS technology and are presented to validate the effectiveness of the proposed current mirrors.

1.5 Organisation of the dissertation

The chapters in the dissertation are organised as follows:

Chapter 1 contains basic introduction of flipped voltage follower cell and low voltage current mirror. It also includes the key contribution, motivation and the organisation of the dissertation.

Chapter 2 contains the literature review, which includes all the study related to low voltage current mirror and all the applications of flipped voltage follower till date.

Chapter 3 proposes three current mirror namely LVCM, FVFLVCM I, FVFLVCM II. It performs the DC and the AC analysis of all the proposed circuits and discusses the location of dominant pole.

Chapter 4 discusses the stability analysis of all the three proposed current mirrors by time domain and frequency domain approaches.

Chapter 5 is basically for showing the applicability of all the proposed current mirrors. It includes three applications and the comparison of LDPC is discussed with conventional current mirror.

Chapter 6 shows the simulation results for all the proposed current mirrors. It categories into simulations for DC characteristics, AC characteristics, stability through phase margin, applications and at last the comparison is done with the current mirrors reported in literature till date.

Chapter 7 discusses the conclusion of the dissertation and also emphasizes on the future scope of the work done in dissertation.

CHAPTER

2

LITERATURE REVIEW

In literature, researchers have suggested several basic topologies and applications of flipped voltage follower (FVF). A succinct review based on the study of these papers is as follows:

2.1 Flipped voltage follower with level shifter (LSFVF):

LSFVF is a Level shifted version of the FVF [23]. LSFVF uses a voltage follower (common drain configuration) between feedback path of flipped voltage follower as a DC level shifter and increases the input/output swing, which is independent of power supply.

Advantages:

- LSFVF structure was introduced to increase the input/output swing of the FVF.
- LSFVF structure causes output impedance to get reduced as compared to conventional voltage follower.

2.2 Folded Flipped Voltage Follower (FFVF) :

The current sensing transistor is folded (from NMOS to PMOS) by introducing an additional biasing source [23]. Stability requires to limit Gain-Bandwidth to a value of at most one half of the effective high frequency pole of the negative feedback loop present in all FVF structures. For the FVF and the FFVF the effective high frequency pole is given by ratio of transconductance of transistor (input transistor) and load capacitance. In all FVF circuits

small compensation capacitors (C_c) can be used to limit the Gain-Bandwidth product to a value of less than one half of the effective high frequency pole of the FVF.

Advantages:

- The folded flipped voltage follower (FFVF) or “super source follower” is also an increased input/output swing modification of the FVF.
- The gain-bandwidth product is high and is given by ratio of transconductance of transistor (in a feedback loop) and coupling capacitance, much higher than suggested in LSFVF.
- FFVF structure causes output impedance to get reduced as compared to conventional voltage follower.

2.3 Cascoded Flipped Voltage Follower (CASFVF):

In CASFVF structure a PMOS cascoding transistor is introduced between the feedback path. The quiescent voltage at the output node is set close to V_{DD} by the cascoded voltage of current sensing transistor in FVF [23].

Advantages:

- CASFVF is designed to increase input/output swing of the FVF.
- Transistor in a loop provides additional gain to the negative feedback loop and leads to an extremely low output resistance (tenths of Ω).

2.4 FVF current sensors (FVFCS) :

The FVF cell can also be considered to as a current sensing cell known as FVF current sensors (FVFCS). FVFCS assumes that all transistors are properly biased to work in the saturation region [24]. Due to the shunt feedback provided by current sensing transistor, the impedance at output node is very low and the amount of current that flows through output node does not modify the value of its voltage.

Advantages:

- The FVFCS can be operated with very low voltage supply. The minimum supply voltage is the addition of absolute value of threshold voltage and twice of drain to source voltage in saturation and has very low output impedance.
- FVFCS is operated with low input voltage (order of drain to source voltage in saturation).
- The current can be easily removed from the output node by using current mirroring techniques, if it is needed for a specific application.

2.5 FVF differential structure (DFVF)

The differential structure based on the FVF cell is built by adding an extra transistor connected to output node [20,24]. As indicated in the FVFCS section, the impedance at output node is very low and its voltage remains approximately constant for large currents through additional transistor. Consider quiescent conditions when common mode is applied, and assuming the same transistor sizes, current through both differential pair transistor will be same. Differential voltage generates current variations in additional transistor that follow the MOS square law [25].

Advantages:

- The maximum output current can be much larger than the quiescent current I_b .
- The output is available as both, a current (the current through transistor replicated by means of a current mirror) and a voltage. This feature can be advantageously employed to simplify the circuit implementations reducing both noise and number of poles and zeroes.
- DFVF can also be operated with very low supply voltage.
- With a supply of V_{DDMIN} , there would be no room for variation of the differential input signals.

2.6 Low voltage high precision current mirror:

Current mirror was improved to allow very low input impedance and very high output impedance under low voltage operation [6,26]. The differential amplifier can be easily realized in a low-voltage environment, as its inputs are very close to ground potential. This topology combines a shunt input feedback, a regulated cascade output and a differential amplifier to achieve low input resistance, high accuracy and high output resistance.

Advantages:

- The input voltage required for such current mirror is in the (order of drain to source voltage in saturation), which can be as small as 0.1 V, which is much smaller than the drop required for the conventional low-voltage current mirror.
- Low voltage high precision current mirror allows very low input impedance and very high output impedance.
- The minimum voltage supply is given by the addition of absolute value of threshold voltage and twice of drain to source voltage in saturation.

2.7 Implementation of current conveyer generation II (CCII) using FVF:

Implementation of current conveyer generation II (CCII) includes simple dc level shifter formed by the diode-connected transistor biased by two identical current sources [27]. The circuit becomes very simple, having only two internal nodes (excluding biasing current mirrors).

Advantages:

- The input impedance of terminal is finite and output impedance is very low.
- The small-signal gain is nearly 1.
- Resistor R in the FVF cell has been introduced to improve the signal bandwidth.

2.8 Improved current conveyer generation II (CCII) [27]:

Advantages:

- The difference between input and output FVF dc levels is solved by driving the FVF with an amplifier.

- The diode-connected dc level shifter is avoided, leading to very high input impedance at the node.
- The amplifier feedback further reduces the output impedance and also makes the voltage gain come closer to the ideal (unity) value.
- Biasing of the cell also becomes simpler due to the avoidance of the dc level shifter.

2.9 Conventional Cascode Current Mirror:

The flipped voltage follower (FVF) cell has been employed for realizing low voltage current mirrors [12,24]. The minimum supply voltage requirement for the correct operation of the current mirror is equal to addition of threshold voltage and drain to source voltage on the edge of saturation. One of the most widely used current mirror topologies in low-voltage signal processing is the conventional cascode current mirror [28,29].

Advantages:

- The important factors that establish the capability of the current mirror to operate in a low voltage environment are the minimum input and output voltages.
- Conventional Cascade Current Mirror requires minimum supply voltage, low input resistance and high Output impedance.

2.10 Low-dropout regulator (LDO) using a flipped voltage follower:

Low-dropout regulator (LDO) topology intends to provide a detailed study on the stability of an LDO based on the FVF for different capacitors, equivalent series resistances (ESRs) and load conditions [30]. The regulators with a relatively big output capacitor, typically located off-chip as a discrete component and it helps to achieve the dominant pole at low frequencies, well separated from the remaining non-dominant poles, which guaranties stable operation [31].

The other solution of LDO regulators is based on very small on-chip capacitance connected to its output, mainly resulting from parasitic capacitance of an on-chip supply network. The small output capacitance makes the design of such on-chip regulators extremely difficult,

because in this case the dominant pole has to be realised inside a negative regulation loop. Several solutions were proposed to overcome the outlined difficulties. The single-transistor-control configuration using flipped voltage follower (FVF) is utilised to form a regulator able to operate stable with no output capacitance.

Advantages:

- FVF is used in LDO topology to reduce output impedance due to shunt feedback connection, which is the key for obtaining good regulation.
- Accuracy, power efficiency, response time, silicon area, and off-chip component free feature, all requirements are fulfilled.

2.11 Low-voltage, high-speed CMOS analog latched voltage comparator using the “flipped voltage follower” as input stage:

The voltage comparator is an important building block in ADC design. The performance and accuracy of an ADC are strongly determined by the comparator’s ability to resolve the smallest voltage difference at its inputs [32]. However, designing circuit for low-voltage operation can reduce its input dynamic range and the complementary differential techniques that are often used to enable rail-to-rail operation would increase power consumption.

In order to overcome limitations, a new approach to dynamic latch comparator design that replaces the input stage with a “flipped voltage follower” (FVF) cell was suggested. The circuit consists of a differential input stage with a common-mode signal detector, followed by a regenerative latch and a Set–Reset (S–R) latch.

Advantages:

- FVF cell offers the capacity for large voltage swing.
- FVF cell includes a voltage follower, its low output impedance allows it to source relatively large currents.
- The new input stage improves performance in terms of slew rate and resolution. The higher slew rate is achieved due to FVF’s dynamic bias current setting, and the higher resolution is attainable due to its larger voltage swing, resulting in a higher signal-over-noise ratio.

2.12 Internally compensated LDO regulator based on the cascoded FVF

A LDO is a linear voltage regulator that operates with a high efficiency with a small input–output voltage difference. An internal compensation of LDO is usually preferred, as it does not require external capacitors, reducing size and cost. The Flipped Voltage Follower, (FVF) was identified as the core cell for LDO design. The good performances of this cell as a current buffer and its low output impedance make it a highly efficient LDO regulator according to load regulation [33]. However, its response due to input voltage variations is limited by the biasing currents, which are responsible for the charge/discharge of the gate parasitic capacitance of the pass transistor. Thus, there is a trade-off between power consumption and transient response.

Further work on this structure has been done creating a path that couples the changes variations in the output voltage to the gate of the pass transistor. This can be implemented in a simple way by means of RC coupling.

Advantages:

- The regulator uses RC coupling to solve the transient problems of the circuits for input voltage variations without a significant increase in the quiescent power consumption.
- The regulator that uses RC coupling can be used to improve both, the line and load transient responses.

2.13 Current sensor for I_{DD} test :

Current sensor for I_{DD} test consists of a FVFCS plus a cascode output stage and a resistor that transforms a replica of the transient supply current into an observable voltage. The FVFCS is biased with the current source I_b which determines the effective bandwidth of the current sensor.

A high frequency buffer [34] is also included to drive the voltage signal across load resistance of chip and isolate it from the large output load capacitance.

Advantages:

- Current sensor has low supply voltage and low input voltage requirements, very low input impedance.

Current sensor has the capability to sink large currents with an approximately constant input voltage close to one of the supply rails.

2.14 Low voltage, low power, high performance current mirror for portable analog and mixed mode application [35,36]

A current mirror, which operates at low voltage supply requirement, is discussed. The mirror has high output and high input voltage swings. Adaptive current biasing is also introduced for reducing the effects of offset current. A compensation technique has been implemented to enhance the bandwidth. This makes the current mirror (CM) structure attractive for portable, high frequency applications.

2.15 A Comparative Study of the Performance of the Flipped Voltage Follower Based Low-Voltage Current Mirrors [37]

A comparative study of flipped voltage follower based current mirror topologies which are capable of operating with low-voltage supply requirement is performed. The comparison of FVF based cascade current mirror is done with conventional cascade current mirror is carried out and performance wise current mirror based on FVF cell is found better than conventional current mirror.

2.16 Very low input impedance low power current mirror [38]

A novel low input impedance current mirror/source is discussed. Simulation results in the paper show an input resistance for the proposed current mirror about 0.006Ω . This is 4×10^5 times lower than that of the simple one while both working with 1.5 V supply and 50 μA bias current. It consumes only 161 μW and exhibits an excellent current error value of Zero at 55 μA which remains below 0.6% up to 100 μA . Favorably its minimum output voltage is reduced to 0.2 V.

2.17 A New Low-Voltage Current Mirror Circuit with Enhanced Bandwidth [39]

In this paper, low-voltage current mirror circuit is presented. The proposed circuit is implemented by using four PMOS and five NMOS. The suggested circuit operates at the supply voltage of +1.3V. The bandwidth circuit has also been enhanced using resistive compensation technique.

2.18 High frequency flipped voltage follower with improved performance and its application [40]

A wideband flipped voltage follower (FVF) with low output impedance is discussed. Inductive-peaking-based bandwidth enhancement technique is implemented in the FVF cell. Wideband low-voltage current mirrors are also presented with high bandwidth.

CHAPTER

3

PROPOSED LOW-VOLTAGE CURRENT MIRRORS

This chapter contains three low-voltage current mirrors namely low-voltage current mirror (LVCM), flipped voltage follower based low-voltage current mirror I (FVFLVCM I) and flipped voltage follower based low-voltage current mirror II (FVFLVCM II) operating at +1.2V, +1.2V and +1.2V & +1V respectively. The AC equivalent models of these circuits have also been presented to estimate the bandwidth and to justify the stability criteria based on pole-zero concept.

3.1 Proposed Low-voltage Current Mirror

The proposed low-voltage current mirror (LVCM) is shown in Figure 3.1. The transistors M4 and M5 are used to generate the biasing current (I_b). At node 1, the two currents namely bias current (I_b) and input current (I_{in}) are injecting in and are entering into the transistor M0 with current I_b+I_{in} . The four pairs of transistors M0&M1, M2&M3, M4&M5 and M6&M7 are perfectly matched and are used to form current mirrors.

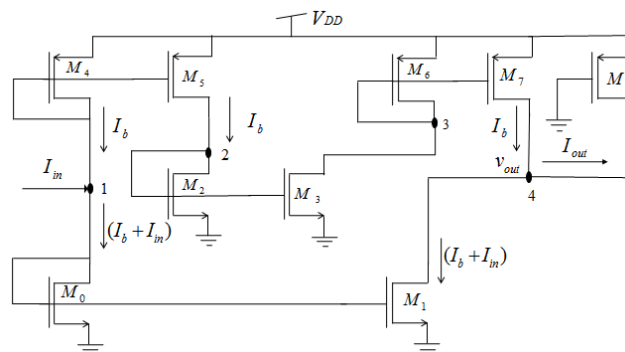


Figure 3.1 Proposed low-voltage current mirror

The AC equivalent model of the proposed LVCM is as shown in Figure 3.2. In this model, it is assumed that

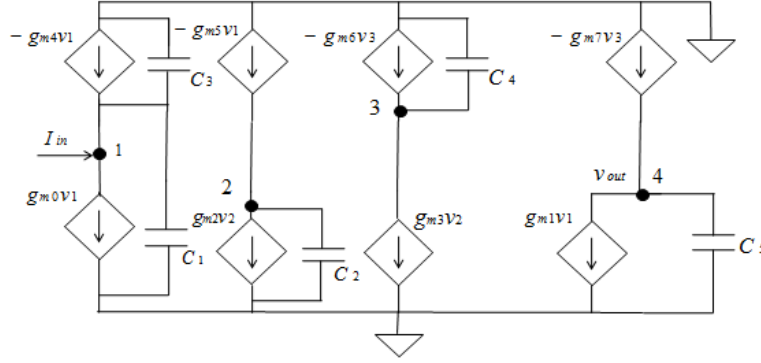


Figure 3.2 AC equivalent model of proposed LVCM

$$c_1 = C_{gs1} + C_{gs0}; c_2 = C_{gs2} + C_{gs3}; c_3 = C_{gs4} + C_{gs5}; c_4 = C_{gs6} + C_{gs7}; c_5 = C_{gs8}$$

(5)

where $C_{gsi(i=0 \text{ to } 10)}$ is the gate-to-source capacitance of the i^{th} transistor.

The equivalent capacitance (c) can be written as

$$c = c_1 + c_3$$

(6)

The output current can be written as

$$I_{out} = -sc_5 v_{out}$$

(7)

where v_{out} is the output voltage

On applying KCL at nodes 1, 2, 3 and 4 respectively, we get

$$I_{in} - g_{m4}v_1 - g_{m0}v_1 - scv_1 = 0$$

(8)

$$-g_{m5}v_1 - g_{m2}v_2 - sc_2v_2 = 0$$

(9)

$$-g_{m6}v_3 - g_{m3}v_2 - sc_4v_3 = 0$$

(10)

$$-g_{m7}v_3 - g_{m1}v_1 - sc_5v_{out} = 0$$

(11)

where g_{m_i} , ($i=0$ to 7) is the transconductance of the transistor M_i and v_1, v_2, v_3 and v_{out} are the voltages at the nodes 1, 2, 3 and 4 respectively.

Solving (6)(7)(8)(9)(10) and (11), the transfer function can be written as

$$\frac{I_{out}}{I_{in}} = \frac{g_{m8}}{c} \left[\frac{\left(\frac{g_{m7}g_{m5}g_{m3}}{c_4c_2} \right) + g_{m1} \left(s + \frac{g_{m2}}{c_2} \right) \left(s + \frac{g_{m6}}{c_4} \right)}{\left(s + \frac{g_{m2}}{c_2} \right) \left(s + \frac{g_{m6}}{c_4} \right) \left(s + \frac{g_{m0} + g_{m4}}{c} \right)} \right] \quad (12)$$

From (12), it is concluded that the transfer function exhibits a dominant pole (at $s = -\frac{g_{m2}}{c_2}$) which decides the bandwidth of the proposed LVCM circuit. By introducing the zero at frequency ($s = -\frac{g_{m2}}{c_2}$), dominant pole can be changed which finally results in enhancement of the bandwidth.

3.1.1 Proposed low-voltage current mirror with enhanced bandwidth

In this section, bandwidth of low-voltage current mirror (LVCM) has been improved using two types of compensations namely passive compensation and active compensation. The frequency analysis has also been performed to obtain the modified transfer function.

3.1.1.1 Bandwidth enhancement of proposed circuit by passive compensation

The proposed circuit improves the bandwidth of the LVCM by performing modification as shown in Figure 3.3.

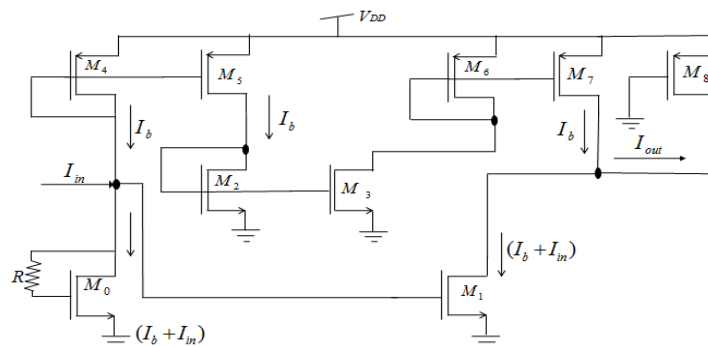


Figure 3.3 AC equivalent model of proposed LVCM

The AC equivalent model of the Figure 3.3 is as shown in Figure 3.4. In this model, it is assumed that

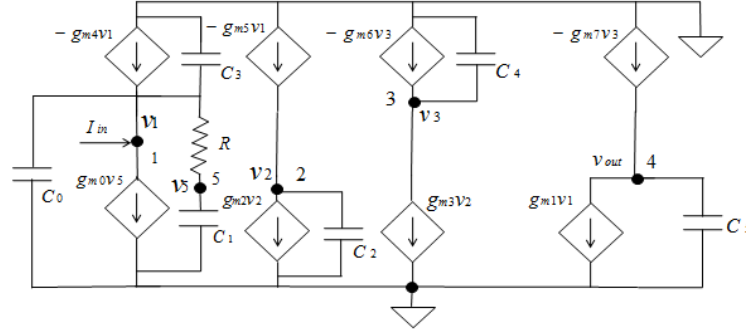


Figure 3.4 AC equivalent model of passively compensated LVCM

$$c_0 = C_{gs0}; c_1 = C_{gs1}; c_2 = C_{gs2} + C_{gs3}; c_3 = C_{gs4} + C_{gs5}; c_4 = C_{gs6} + C_{gs7}; c_5 = C_{gs8} \quad (13)$$

where $C_{gsi(i=0 \text{ to } 10)}$ is the gate-to-source capacitance of the i^{th} transistor.

The equivalent capacitance (c) can be written as

$$c = c_0 + c_3 \quad (14)$$

The output current can be written as

$$I_{out} = -sc_5 v_{out} \quad (15)$$

where v_{out} is the output voltage

On applying KCL at nodes 1, 2, 3, 4 and 5 respectively, we get

$$I_{in} - (g_{m4} + \frac{1}{R})v_1 - (g_{m0} - \frac{1}{R})v_5 - scv_1 = 0 \quad (16)$$

$$-g_{m5}v_1 - g_{m2}v_2 - sc_2v_2 = 0 \quad (17)$$

$$-g_{m6}v_3 - g_{m3}v_2 - sc_4v_3 = 0 \quad (18)$$

$$-g_{m7}v_3 - g_{m1}v_1 - sc_5v_{out} = 0 \quad (19)$$

$$sc_1v_5 - \frac{(v_1 - v_5)}{R} = 0 \quad (20)$$

where g_{m_i} , ($i=0$ to 7) is the transconductance of the transistor M_i and v_1, v_2, v_3, v_{out} and v_5 are the voltages at the nodes 1, 2, 3, 4 and 5 respectively.

Using (13)(14)(15)(16)(17)(18)(19) and (20), the transfer function can be obtained as

$$\frac{I_{out}}{I_{in}} = \frac{[g_{m3}g_{m5}g_{m7} + g_{m1}(g_{m3} + sc_4)(g_{m2} + sc_2)](Rsc_1 + 1)}{(g_{m3} + sc_4)(g_{m2} + sc_2)[(Rsc_1 + 1)(g_{m1} + s(c_0 + c_3) + \frac{1}{R}) + (g_{m0} - \frac{1}{R})]} \quad (21)$$

From (21), it can be observed that the insertion of R introduces a zero which cancels the dominate pole $\left(s = -\frac{g_{m2}}{c_2}\right)$ and enhances the bandwidth. The modified transfer function can

be written as

$$\frac{I_{out}}{I_{in}} = \frac{[g_{m3}g_{m5}g_{m7} + g_{m1}(g_{m3} + sc_4)(g_{m2} + sc_2)]}{(g_{m3} + sc_4)[(Rsc_1 + 1)(g_{m1} + s(c_0 + c_3) + \frac{1}{R}) + (g_{m0} - \frac{1}{R})]} \quad (22)$$

3.1.1.2 Bandwidth enhancement of proposed circuit by active compensation

The proposed circuit as shown in Figure 3.5, improves the bandwidth as well as the chip area by introducing a active device instead of passive device. The transistor M9 is inserted between transistors M0 & M1 and the gate terminal of M9 is connected to output node, which provides required bias voltage.

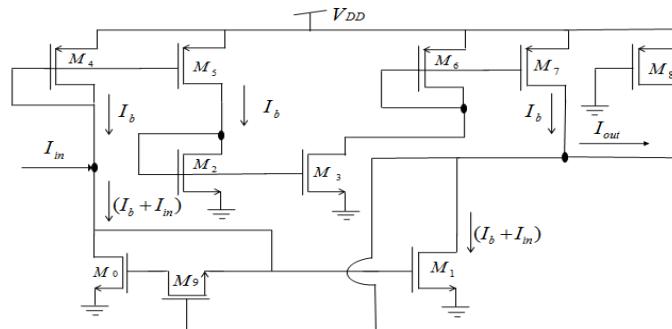


Figure 3.5 Actively compensated proposed LVCM

The AC equivalent model of the Figure 3.5 is as shown in Figure 3.6. In this model, it is assumed that

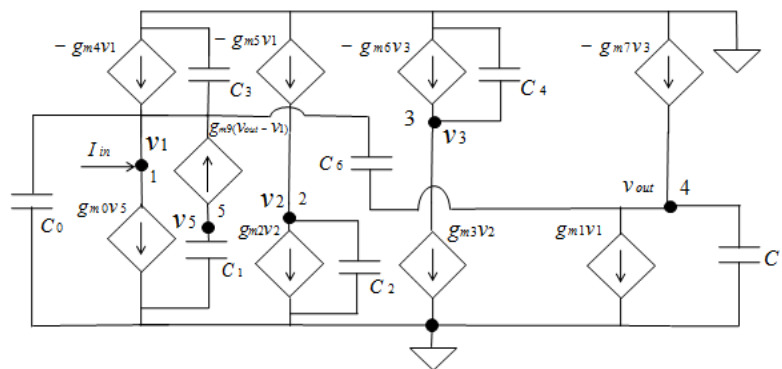


Figure 3.6 AC equivalent model of actively compensated LVCM

$$c_0 = C_{gs0}; c_1 = C_{gs1}; c_2 = C_{gs2} + C_{gs3}; c_3 = C_{gs4} + C_{gs5}; c_4 = C_{gs6} + C_{gs7}; c_5 = C_{gs8} \quad c_6 = C_{gs9} \quad (23)$$

where $C_{gs(i=0 \text{ to } 9)}$ is the gate-to-source capacitance of the i^{th} transistor.

The equivalent capacitance (c) can be written as

$$c = c_0 + c_3 \quad (24)$$

The output current can be written as

$$I_{out} = -sc_5 v_{out} \quad (25)$$

where v_{out} is the output voltage

On applying KCL at nodes 1, 2, 3, 4 and 5 respectively, we get

$$I_{in} - (g_{m4} + sc + g_{m9} + \frac{g_{m0}g_{m9}}{sc_1} + sc_6)v_1 - (g_{m9} + \frac{g_{m0}g_{m9}}{sc_1} + sc_6)v_{out} = 0 \quad (26)$$

$$-g_{m5}v_1 - g_{m2}v_2 - sc_2v_2 = 0 \quad (27)$$

$$-g_{m6}v_3 - g_{m3}v_2 - sc_4v_3 = 0 \quad (28)$$

$$-g_{m7}v_3 - g_{m1}v_1 - sc_5v_{out} + (v_1 - v_{out})sc_6 = 0 \quad (29)$$

$$sc_1v_5 + g_{m9}(v_{out} - v_1) = 0 \quad (30)$$

where g_{m_i} , ($i=1$ to 10) is the transconductance of the transistor M_i and v_1, v_2, v_3, v_{out} and v_5 are the voltages at the nodes 1, 2, 3, 4 and 5 respectively.

Solving (25)(26)(27)(28)(29) and (30), the transfer function can be evaluated as

$$\frac{I_{out}}{I_{in}} = \frac{s^2 c_1 c_5 [g_{m1}(g_{m6} + sc_4)(g_{m2} + sc_2) + g_{m3} g_{m5} g_{m7} - sc_6 (g_{m6} + sc_4)(g_{m2} + sc_2)]}{[g_{m1}(g_{m6} + sc_4)(g_{m2} + sc_2) + g_{m3} g_{m5} g_{m7} - sc_6 (g_{m6} + sc_4)(g_{m2} + sc_2)](s^2 c_6 c_1 + g_{m9} sc_1 + g_{m0} g_{m9}) + [g_{m4} sc_1 + g_{m9} sc_1 + g_{m0} g_{m9} + s^2 c_1 (c_0 + c_3 + c_6)](sc_5 + sc_6)}$$
(31)

From (31), it can be seen that insertion of the transistor M9 between transistors M0 and M1 modifies the characteristics equation due to which dominant poles get shifted (further away from origin), which enhances the bandwidth of the proposed LVCM.

3.2 Proposed Flipped Voltage Follower Based Low-Voltage Current Mirror I

The proposed flipped voltage follower based low-voltage current mirror I (FVFLVCM I) is shown in Figure 3.7. The transistors M7 and M8 are used to generate the biasing current (I_b). At node v_x , the two currents namely bias current (I_b) and input current (I_{in}) are injecting in and are entering into the transistor M5 with current $I_b + I_{in}$. The four pairs of transistors M2&M5, M3&M4, M7&M8, M9&M10 are perfectly matched and are used to form current mirrors. Therefore drain currents of transistor M3 and transistor M5 transfers to transistor M4, transistor M2 respectively. Also the drain current of transistor M9 is copied to transistor M10. In proposed circuit, the flipped voltage follower cell (FVF) is realised using two transistors M5 and M6 to reduce the power supply requirement of the circuit. The transistor M6 in FVF cell always remains in saturation in order to avoid quiescent point shifting and the transistor M5 bears all the changes in the drain current and remains in linear region.

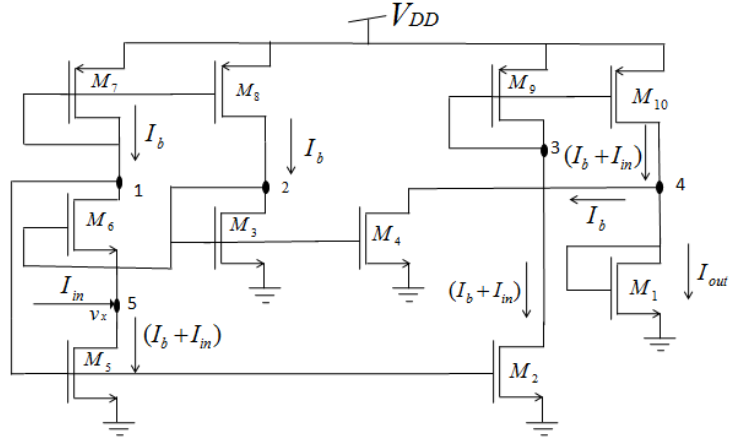


Figure 3.7 Proposed FVFLVCM I

The AC equivalent model of the proposed FVFLVCM I is as shown in Figure 3.8. In this model, it is assumed that

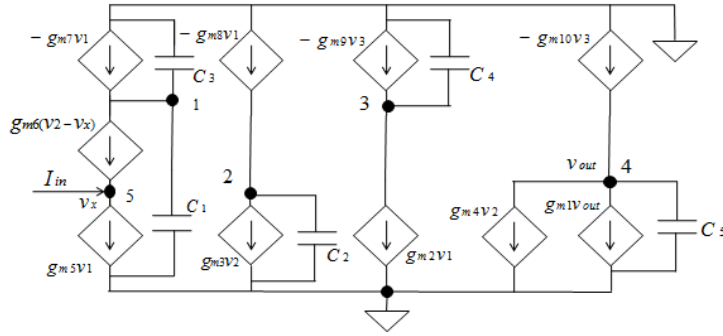


Figure 3.8 AC equivalent model of FVFLVCM I

$$c_1 = C_{gs2} + C_{gs5}; c_2 = C_{gs3} + C_{gs4} + C_{gs6}; c_3 = C_{gs7} + C_{gs8}; c_4 = C_{gs9} + C_{gs10}; c_5 = C_{gs1} \quad (32)$$

where $C_{gsi(i=1 \text{ to } 10)}$ is the gate-to-source capacitance of the i^{th} transistor.

The equivalent capacitance (c) is given as:

$$c = c_1 + c_3 \quad (33)$$

The output current (I_{out}) is given as

$$I_{out} = g_{m1}v_{out} \quad (34)$$

where g_{m1} is the transconductance of the transistor M_1 and v_{out} is the output voltage.

On applying KCL at nodes 1, 2, 3, 4 and 5 respectively, we get

$$-g_{m7}v_1 - scv_1 - g_{m6}(v_2 - v_x) = 0 \quad (35)$$

$$-g_{m8}v_1 - g_{m3}v_2 - sc_2v_2 = 0 \quad (36)$$

$$-g_{m9}v_3 - g_{m2}v_1 - sc_4v_3 = 0 \quad (37)$$

$$-g_{m10}v_3 - g_{m4}v_2 - g_{m1}v_{out} - sc_5v_{out} = 0 \quad (38)$$

$$I_{in} + g_{m6}(v_2 - v_x) - g_{m5}v_1 = 0 \quad (39)$$

where $g_{m_i(i=1 \text{ to } 10)}$ is the transconductance of the transistor M_i and v_1, v_2, v_3 and v_x are the voltages at the nodes 1, 2, 3 and 5 respectively.

Using (34)(35)(36)(37)(38) and(39), the transfer function is obtained as

$$\frac{I_{out}}{I_{in}} = \frac{g_{m1}[g_{m8}g_{m4}(g_{m9} + sc_4) + g_{m2}g_{m8}(g_{m3} + sc_2)]}{(g_{m5} + g_{m7} + sc)(g_{m9} + sc_4)(g_{m3} + sc_2)(g_{m1} + sc_5)} \quad (40)$$

From (40), it can be seen that the transfer function exhibits a dominant pole $\left(s = -\frac{g_{m3}}{c_2}\right)$

which decides the bandwidth of the proposed circuit. The dominant pole $\left(s = -\frac{g_{m3}}{c_2}\right)$ can be

cancelled out using pole zero cancellation method by introducing a zero which results in enhancement in the bandwidth of proposed circuit.

3.2.1 Proposed Flipped Voltage Follower Based Low-Voltage Current Mirror I With Enhanced Bandwidth

The proposed circuit in this section improves the bandwidth of the FVFLVCM I by performing modification as shown in Figure 3.9. In this circuit, a resistance R is connected between gate and drain terminals of the transistor M5 and M6 respectively which creates the voltage difference between two terminals.

$$-g_{m7}v_1 - sc v_1 - g_{m6}(v_2 - v_x) + g_{m5}v_y + \frac{v_1}{\left(R + \frac{1}{sc_1}\right)} = 0 \quad (44)$$

$$-g_{m8}v_1 - g_{m3}v_2 - sc_2v_2 = 0 \quad (45)$$

$$-g_{m9}v_3 - g_{m2}v_1 - sc_4v_3 = 0 \quad (46)$$

$$-g_{m10}v_3 - g_{m4}v_2 - g_{m1}v_{out} - sc_5v_{out} = 0 \quad (47)$$

$$g_{m6}(v_2 - v_x) = -I_{in} + g_{m5}v_1 \quad (48)$$

$$v_y = \frac{v_1}{1 + Rsc_1} \quad (49)$$

where $g_{m_i(i=1 \text{ to } 10)}$ is the transconductance of the transistor M_i and $v_1, v_2, v_3, v_{out}, v_x$ and v_y are the voltages at the nodes 1, 2, 3, 4, 5 and 6 respectively.

Using (43)(44)(45)(46)(47)(48) and (49), the transfer function is obtained as

$$\frac{I_{out}}{I_{in}} = \frac{g_{m1}[g_{m8}g_{m4}(g_{m9} + sc_4) + g_{m2}g_{m8}(g_{m3} + sc_2)](Rsc_1 + 1)}{(g_{m5} + g_{m7} + sc)(Rsc_1 + 1) + (sc_1 + g_{m5})(g_{m9} + sc_4)(g_{m3} + sc_2)(g_{m1} + sc_5)} \quad (50)$$

From (50), it is observed that the transfer function has five poles and two zeroes whereas in (40), there are four poles and one zero. The dominant pole $\left(s = -\frac{g_{m3}}{c_2}\right)$ in (46) can be cancelled by introducing

zero at $s = -\frac{1}{Rc_1}$ and then (50) is modified as

$$\frac{I_{out}}{I_{in}} = \frac{g_{m1}[g_{m8}g_{m4}(g_{m9} + sc_4) + g_{m2}g_{m8}(g_{m3} + sc_2)]}{(g_{m5} + g_{m7} + sc)(Rsc_1 + 1) + (sc_1 + g_{m5})(g_{m9} + sc_4)(g_{m1} + sc_5)} \quad (51)$$

From (51), it can be seen that the cancellation of pole $\left(s = -\frac{g_{m3}}{c_2}\right)$ shifts the dominant pole to

$s = -\frac{g_{m9}}{c_4}$ which lie further away from the origin and therefore enhances the bandwidth of the

proposed FVFLVCM I.

3.3 Proposed flipped voltage follower based low-voltage current mirror II

The proposed flipped voltage follower based low-voltage current mirror II (FVFLVCM II) is shown in Figure 3.11. The transistor pairs M2&M5, M3&M4, M7&M8, M9&M10 are perfectly matched and are used to form current mirrors. In proposed circuit, the flipped voltage follower cell (FVF) is realised using two transistors M5 and M6 in order to reduce the power supply requirement of the proposed circuit. The gate terminal of transistor M6 is connected to its drain terminal, as in FVF cell transistor M6 always remains in saturation in order to avoid quiescent point shifting. The transistor M5 bears all the changes in the drain current and remains in linear region.

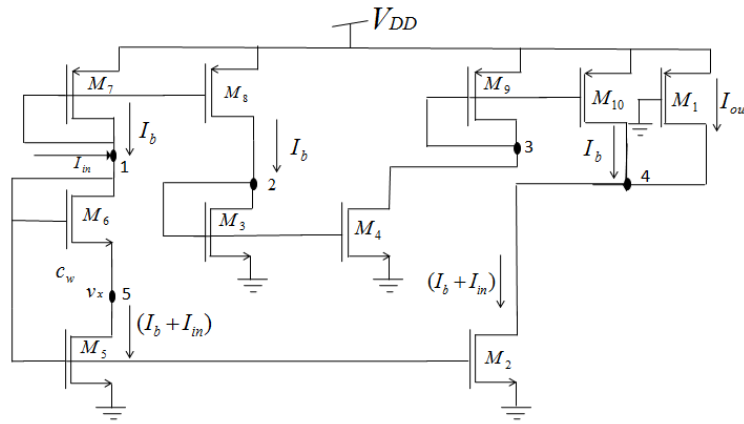


Figure 3.11 Proposed FVFLVCM II

The AC equivalent model of the proposed FVFLVCM II is as shown in Figure 3.12. In this model, it has been assumed that

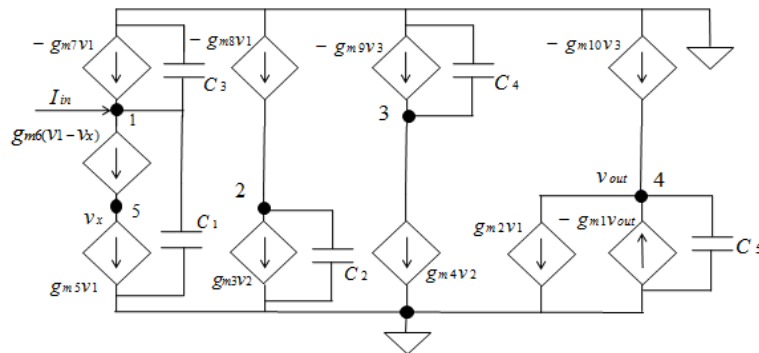


Figure 3.12 AC equivalent of FVFLVCM II

$$c_1 = C_{gs2} + C_{gs5} + C_{gs6}; c_2 = C_{gs3} + C_{gs4}; c_3 = C_{gs7} + C_{gs8}; c_4 = C_{gs9} + C_{gs10}; c_5 = C_{gs1} \quad (52)$$

where $C_{gs(i=1 \text{ to } 10)}$ is the gate-to-source capacitance of the i^{th} transistor.

The equivalent capacitance (c) is given as:

$$c = c_1 + c_3 \quad (53)$$

The output current (I_{out}) is given as

$$I_{out} = g_{m1} v_{out} \quad (54)$$

where g_{m1} is the transconductance of the transistor M_1 and v_{out} is the output voltage.

On applying KCL at nodes 1, 2, 3, 4 and 5 respectively, we get

$$I_{in} - g_{m7} v_1 - sC v_1 - g_{m6} (v_1 - v_x) = 0 \quad (55)$$

$$-g_{m8} v_1 - g_{m3} v_2 - sC_2 v_2 = 0 \quad (56)$$

$$-g_{m9} v_3 - g_4 v_2 - sC_4 v_3 = 0 \quad (57)$$

$$-g_{m10} v_3 - g_{m2} v_1 - g_{m1} v_{out} - sC_5 v_{out} = 0 \quad (58)$$

$$g_{m6} (v_1 - v_x) - g_{m5} v_1 = 0 \quad (59)$$

where $g_{m_i(i=1 \text{ to } 10)}$ is the transconductance of the transistor M_i and v_1, v_2, v_3 and v_x are the voltages at the nodes 1, 2, 3 and 5 respectively.

Using (54)(55)(56)(57)(58) and (59), the transfer function can be obtained as

$$\frac{I_{out}}{I_{in}} = \frac{g_{m1} [g_{m2} (g_{m3} + sC_2)(g_{m9} + sC_4) + g_{m10} g_{m8} g_{m4}]}{(g_{m5} + g_{m7} + sC)(g_{m9} + sC_4)(g_{m3} + sC_2)(g_{m1} + sC_5)} \quad (60)$$

From equation (60), it is observed that the transfer function exhibits a dominant pole

$\left(s = -\frac{g_{m9}}{c_4} \right)$ which decides the bandwidth of the proposed circuit. By introducing the zero at

frequency $\left(s = -\frac{g_{m9}}{c_4} \right)$ in order to perform pole-zero cancellation, dominant pole can be

changed which finally results in enhancement of the bandwidth.

3.3.1 Proposed flipped voltage follower based low-voltage current mirror with enhanced bandwidth

The proposed circuit shown in Figure 3.13 improves the bandwidth of the FVFLVCM II. In this circuit, a resistance R is connected between gate and drain terminals of the transistor M5 and M6 respectively which creates the potential difference between two terminals.

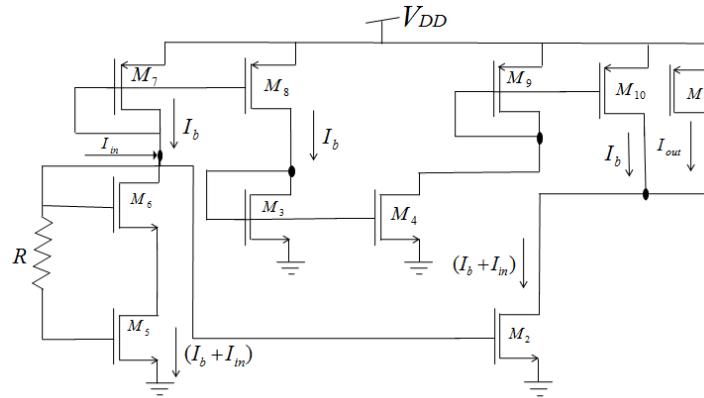


Figure 3.13 Passively compensated FVFLVCM II

The AC equivalent model of the proposed FVFLVCM II is as shown in Figure 3.14. In this model, it has been assumed that

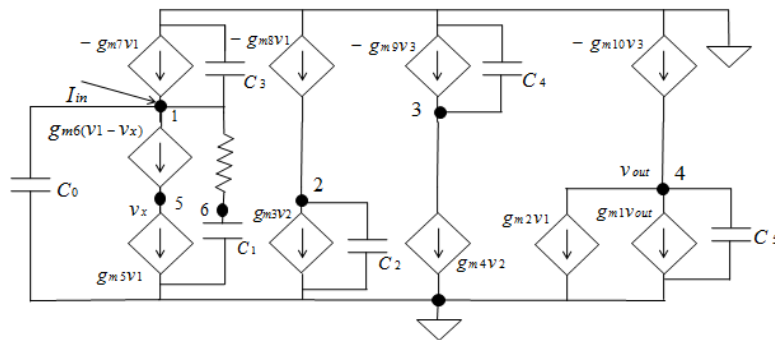


Figure 3.14 AC equivalent of Passively compensated FVFLVCM II

$$c_0 = C_{gs2}; c_1 = C_{gs5} + C_{gs6}; c_2 = C_{gs3} + C_{gs4}; c_3 = C_{gs7} + C_{gs8}; c_4 = C_{gs9} + C_{gs10}; c_5 = C_{gs1} \quad (61)$$

where $C_{gs(i=0 \text{ to } 10)}$ is the gate-to-source capacitance of the i^{th} transistor.

The equivalent capacitance (c) can be written as

$$c = c_0 + c_3 \quad (62)$$

The output current is given as

$$I_{out} = g_{m1}v_{out} \quad (63)$$

where g_{m1} , is the transconductance of the transistor M_1 and v_{out} is the output voltage

On applying KCL at nodes 1, 2, 3, 4, 5 and 6, we get

$$-g_{m7}v_1 - sc v_1 - g_{m6}(v_2 - v_x) + g_{m5}v_y + \frac{v_1}{\left(R + \frac{1}{sc_1}\right)} = 0 \quad (64)$$

$$-g_{m8}v_1 - g_{m3}v_2 - sc_2v_2 = 0 \quad (65)$$

$$-g_{m9}v_3 - g_{m2}v_1 - sc_4v_3 = 0 \quad (66)$$

$$-g_{m10}v_3 - g_{m4}v_2 - g_{m1}v_{out} - sc_5v_{out} = 0 \quad (67)$$

$$g_{m6}(v_2 - v_x) = -I_{in} + g_{m5}v_1 \quad (68)$$

$$v_y = \frac{v_1}{1 + Rsc_1} \quad (69)$$

where $g_{m_i(i=1 \text{ to } 10)}$ is the transconductance of the transistor M_i and $v_1, v_2, v_3, v_{out}, v_x$ and v_y are the voltages at the nodes 1, 2, 3, 4, 5 and 6 respectively.

Solving (63)(64)(65)(66)(67)(68) and (69), the transfer function can be written as

$$\frac{I_{out}}{I_{in}} = \frac{g_{m1}[g_{m10}g_{m8}g_{m4} + g_{m2}(g_{m9} + sc_4)(g_{m3} + sc_2)](Rsc_1 + 1)}{[(g_{m5} + g_{m7} + sc)(Rsc_1 + 1) + (sc_1 + g_{m5})](g_{m9} + sc_4)(g_{m3} + sc_2)(g_{m1} + sc_5)} \quad (70)$$

From (70), it is seen that the transfer function has five poles and two zeroes whereas in (60), there are 4 poles and two zeroes. The dominant pole (at $s = -\frac{g_{m9}}{c_4}$) in (60) can be cancelled by

introducing zero (at $s = -\frac{1}{Rc_1}$) and then (70) is modified as

$$\frac{I_{out}}{I_{in}} = \frac{g_{m1}[g_{m10}g_{m8}g_{m4} + g_{m2}(g_{m9} + sc_4)(g_{m3} + sc_2)]}{[(g_{m5} + g_{m7} + sc)(Rsc_1 + 1) + (sc_1 + g_{m5})](g_{m3} + sc_2)(g_{m1} + sc_5)} \quad (71)$$

From (71), it can be seen that the cancellation of pole (at $s = -\frac{g_{m9}}{c_4}$) shifts the dominant pole to $s = -\frac{g_{m3}}{c_2}$ which lie more away from the origin and therefore enhances the bandwidth of the proposed FVFLVCM II.

CHAPTER

4

STABILITY ANALYSIS OF PROPOSED CIRCUITS

Stability of the proposed current mirrors mainly depends upon the location of poles and zeroes. In this chapter the stability of proposed circuits is discussed by time domain and frequency domain approaches.

4.1 Routh Hurwitz stability criteria (Time Domain approach)

According to routh Hurwitz stability criteria [41] for a close loop system to be stable, it is necessary and sufficient that all the elements on the 1st column of routh's array must have same sign with no row results into all zeroes.

4.1.1 Routh Hurwitz stability criteria for low-voltage current mirror (LVCM)

From (12), the transfer function of the circuit can be written as

$$\frac{I_{out}}{I_{in}} = \frac{g_{m8}}{c} \left[\frac{\left(\frac{g_{m7} g_{m5} g_{m3}}{c_4 c_2} \right) + g_{m1} \left(s + \frac{g_{m2}}{c_2} \right) \left(s + \frac{g_{m6}}{c_4} \right)}{\left(s + \frac{g_{m2}}{c_2} \right) \left(s + \frac{g_{m6}}{c_4} \right) \left(s + \frac{g_{m0} + g_{m4}}{c} \right)} \right]$$

Table 4.1 Routh's array for LVCM

s^3	$c_4 c_2 c$	$\sum_{i=1}^3 c_4 g_{m6} (g_{m0} + g_{m4})$	0
s^2	$\sum_{i=1}^3 c_4 c g_{m2}$	$g_{m6} g_{m2} (g_{m4} + g_{m0})$	0
s^1	$\sum_{i=1}^8 c_4 c g_{m2} [c_4 g_{m6} (g_{m0} + g_{m4})]$	0	
s^0	$\sum_{i=1}^8 c_4 c g_{m2} [c_4 g_{m6} (g_{m0} + g_{m4})] g_{m6} g_{m2} (g_{m4} + g_{m0})$		

4.1.2 Routh Hurwitz stability criteria for flipped voltage follower based low-voltage current mirror I (FVFLVCM I)

The transfer function of the current mirror can be obtained from (40) as

$$\frac{I_{out}}{I_{in}} = \frac{g_{m1} [g_{m8} g_{m4} (g_{m9} + s c_4) + g_{m2} g_{m8} (g_{m3} + s c_2)]}{(g_{m5} + g_{m7} + s c) (g_{m9} + s c_4) (g_{m3} + s c_2) (g_{m1} + s c_5)}$$

Table 4.2 Routh's array for FVFLVCM I

s^4	$c_5 c_4 c_2 c$	$\sum_{i=1}^6 g_{m1} (g_{m5} + g_{m7}) c_4 c_2$	$(g_{m5} + g_{m7}) g_{m9} g_{m3} g_{m1}$
s^3	$\sum_{i=1}^{24} g_{m1} c_4 c_2 c$	$\sum_{i=1}^{24} g_{m9} g_{m3} g_{m1} c$	0
s^2	$\sum_{i=1}^{542} g_{m1} c_4 c_2 c [(g_{m5} + g_{m7}) g_{m2} c_4 c_2]$	$\sum_{i=1}^{24} g_{m2} c_4 c_2 c [(g_{m5} + g_{m7}) g_{m9} g_{m3} g_{m1}]$	0
s^1	$\sum_{i=1}^{518 \times 24} g_{m2} c_4 c_2 c [(g_{m5} + g_{m7}) g_{m2} c_4 c_2] [g_{m9} g_{m3} g_{m1} c]$	0	
s^0	$\sum_{i=1}^{518 \times 576} g_{m1} c_4^2 c_2^2 c^2 [(g_{m5} + g_{m7})^2 g_{m2} c_4 c_2] [g_{m9}^2 g_{m3}^2 g_{m1} c]$		

4.1.3 Routh Hurwitz stability criteria for flipped voltage follower based low-voltage current mirror II (FVFLVCM II)

The transfer function of the current mirror can be written from (60) as

$$\frac{I_{out}}{I_{in}} = \frac{g_{m1} [g_{m2} (g_{m3} + s c_2) (g_{m9} + s c_4) + g_{m10} g_{m8} g_{m4}]}{(g_{m5} + g_{m7} + s c) (g_{m9} + s c_4) (g_{m3} + s c_2) (g_{m1} + s c_5)}$$

Table 4.3 Routh's array for FVFLVCM II

s^4	$c_5 c_4 c_2 c$	$\sum_{i=1}^6 g_{m1} (g_{m5} + g_{m7}) c_4 c_2$	$(g_{m5} + g_{m7}) g_{m9} g_{m3} g_{m1}$
s^3	$\sum_{i=1}^{24} g_{m1} c_4 c_2 c$	$\sum_{i=1}^{24} g_{m9} g_{m3} g_{m1} c$	0
s^2	$\sum_{i=1}^{542} g_{m1} c_4 c_2 c [(g_{m5} + g_{m7}) g_{m2} c_4 c_2]$	$\sum_{i=1}^{24} g_{m2} c_4 c_2 c [(g_{m5} + g_{m7}) g_{m9} g_{m3} g_{m1}]$	0
s^1	$\sum_{i=1}^{518 \times 24} g_{m2} c_4 c_2 c [(g_{m5} + g_{m7}) g_{m2} c_4 c_2] [g_{m9} g_{m3} g_{m1} c]$	0	
s^0	$\sum_{i=1}^{518 \times 576} g_{m1} c_4^2 c_2^2 c^2 [(g_{m5} + g_{m7})^2 g_{m2} c_4 c_2] [g_{m9}^2 g_{m3}^2 g_{m1} c]$		

From Table 1, Table 2 and Table 3, it can be seen that all the element of 1st column of all three routh's arrays are of same sign (i.e positive), which means the proposed current mirrors forming close loop systems are stable and can be compensated to enhance the bandwidth.

4.2 Stability in terms of phase and gain margin (Frequency domain approach)

The stability of the close loop system through frequency domain approach can be estimated by obtaining positive values of gain (db) and phase margin. Though gain and phase margin can be used as measures of stability, phase margin stands as best measure of stability.

Table 4.4 Phase and Phase margin of proposed current mirrors

Current mirrors	Phase at gain cross over frequency (ϕ) (in degree)	Phase margin ($180 + \phi$) (in degree)
LVCM	180.43°	360.43°
Passively compensated LVCM	179.14°	359.14°
Actively compensated LVCM	179.57°	359.57°
FVFLVCM I	1.5°	181.5°
Passively compensated FVFLVCM I	1.4°	181.4°
FVFLVCM II	180.16°	360.16°
Passively compensated FVFLVCM II	180.13°	360.13°

From Table 4, it can be concluded that the proposed current mirrors have positive phase margins, the large value of phase margins indicate highly stable systems.

CHAPTER

5

APPLICATIONS OF PROPOSED CURRENT MIRRORS

This chapter presents current adder and subtractor circuits based on the proposed current mirrors. The proposed applications can be widely used in analog signal processing applications such as operational transconductance amplifiers (OTA), amplifiers, Gm-C filters, etc.

5.1 Application of proposed Current Mirrors to improve speed of analog LDPC decoder

The application of current mirror is widely found in the blocks of analog decoder circuit based on the sum product algorithm. The conventional current mirrors limit the speed, when analog decoder's inputs are loaded using long wires. When the inputs of the equality nodes are implemented using active current mirrors, their speed has found to be enhanced [41]. A (1024 x 512) H-Matrix of (6,3) low density parity check code is used to illustrate the applicability of proposed current mirrors. The code contains 512 equality nodes and 1024 check nodes having 3 and 6 edges connected to each node, respectively. A conventional current mirror is shown in Figure 5.1.

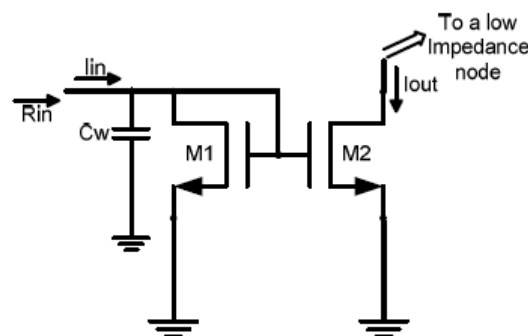


Figure 5.1 Conventional current mirror used at the inputs of an equality or check node with the modeled wiring capacitance of C_w [42]

The input resistance of circuit can be written in form of transconductance as

$$R_{in} = \frac{1}{g_m} \tag{68}$$

The -3db bandwidth of the circuit is given by

$$B.W(-3db) = \frac{g_m}{2\pi(c_{in} + c_w)} \tag{69}$$

where c_{in} is input capacitance and c_w is wiring capacitance (500fF)

From (69), the time delay of the analog decoder can be calculated as

$$\text{Timing Delay } (D_t) = \frac{1}{B.W(-3db)} \tag{70}$$

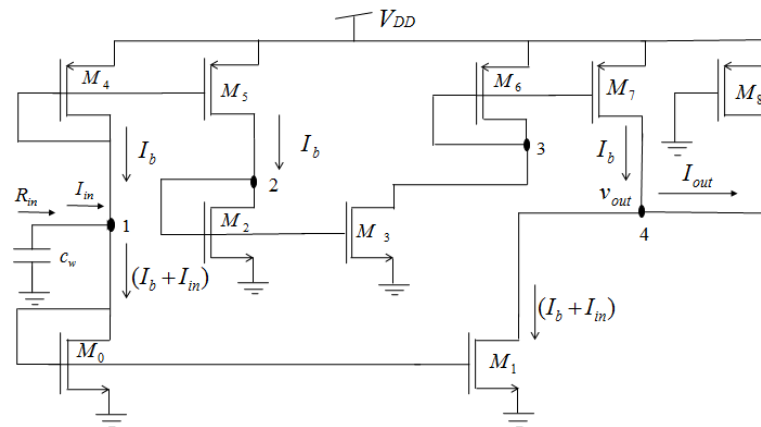


Figure 5.2 LVCM used at the inputs of an equality or check node with the modeled wiring capacitance of C_w

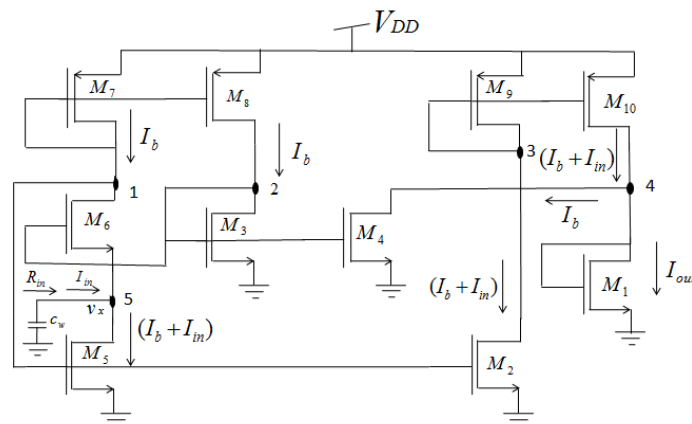


Figure 5.3 FVFLVCM I used at the inputs of an equality or check node with the modeled wiring capacitance of

C_w

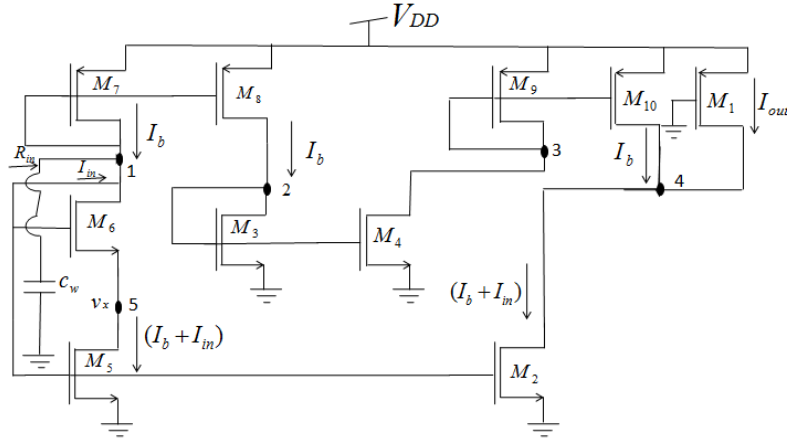


Figure 5.4 FVFLVCM II used at the inputs of an equality or check node with the modeled wiring capacitance of C_w

5.2 Current adder circuit based on proposed FVFLVCM I

The current adder using the proposed current mirror is shown in Figure 5.5. The adder circuit is designed using proposed current mirror namely FVFLVCM I, their functions are to precisely copy the input currents I_{in1} and I_{in2} at the drain terminal of M_1 .

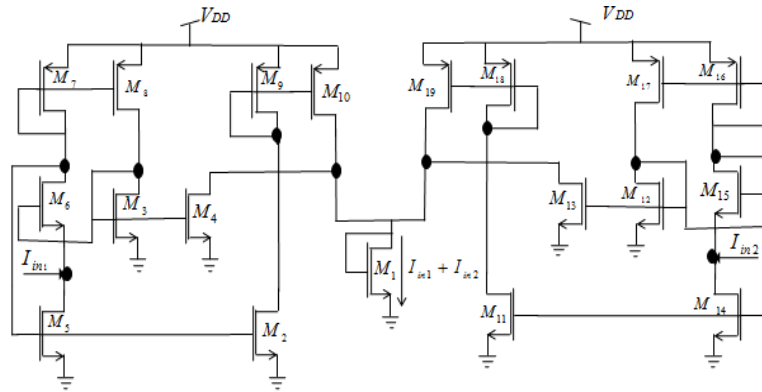


Figure 5.5 Proposed adder circuit using FVFLVCM

On applying KCL on drain terminal of M_1 ,

$$I_{M1} = I_{in1} + I_{in2} \quad (72)$$

From equation (72), it can be observed that the output current I_{M1} is the addition of two input currents I_{in1} and I_{in2} .

5.3 Current subtractor circuit based on proposed FVFLVCM I

The current subtractor is also designed using proposed FVFLVCM I, which is shown in Figure 5.6.

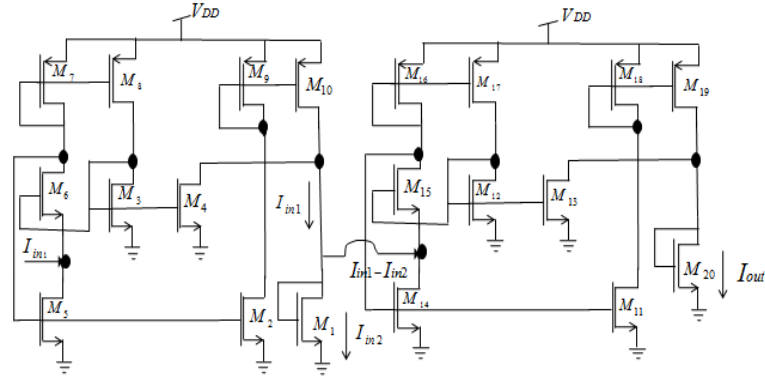


Figure 5.6 Proposed subtractor circuit using FVFLVCM

On applying KCL on drain terminal of M1,

$$I_{(\text{input to 2nd proposed FVFLVCM})} = I_{in1} - I_{in2} \quad (73)$$

From equation (73), it can be observed that the input current given to the 2nd FVFLVCM I is comes out to be $I_{in1} - I_{in2}$, which is replicated to M20 through FVFLVCM and output current is obtained as

$$I_{out} = I_{in1} - I_{in2} \quad (74)$$

CHAPTER

6

SIMULATION RESULTS

The proposed current mirrors and their applications are designed using SPICE in TSMC 0.18 μm CMOS technology. In this chapter, section 6.1 presents the DC characteristics of the proposed circuits and section 6.2 discusses the AC characteristics along with the comparison of proposed circuits with each other in tabular form. Phase and magnitude plot of the circuits to justify the stability are shown in section 6.3. In section 6.4, simulation results for applications of proposed circuits are presented. Lastly, the comparison of proposed current mirrors is presented in section 6.5 with the current mirrors available in literature.

6.1 DC characteristics

The DC responses of Figure 3.1, Figure 3.7 and Figure 3.10 are shown in Figure 6.1, Figure 6.2 and Figure 6.3, respectively. From the Figures, it is observed that there is no current flowing through the feedback path of the FVF cell at low frequency, so the DC characteristics remain unchanged on performing passive and active compensations.

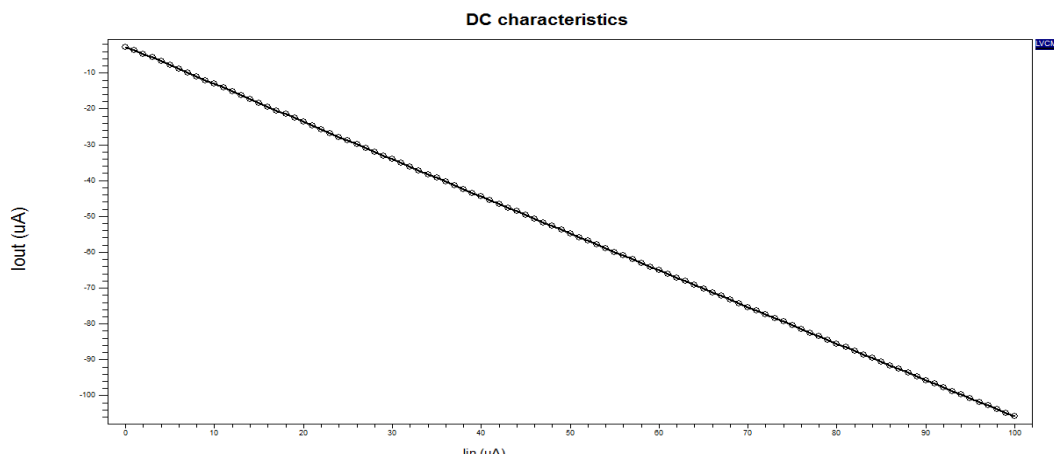


Figure 6.1 DC characteristics of proposed LVCM

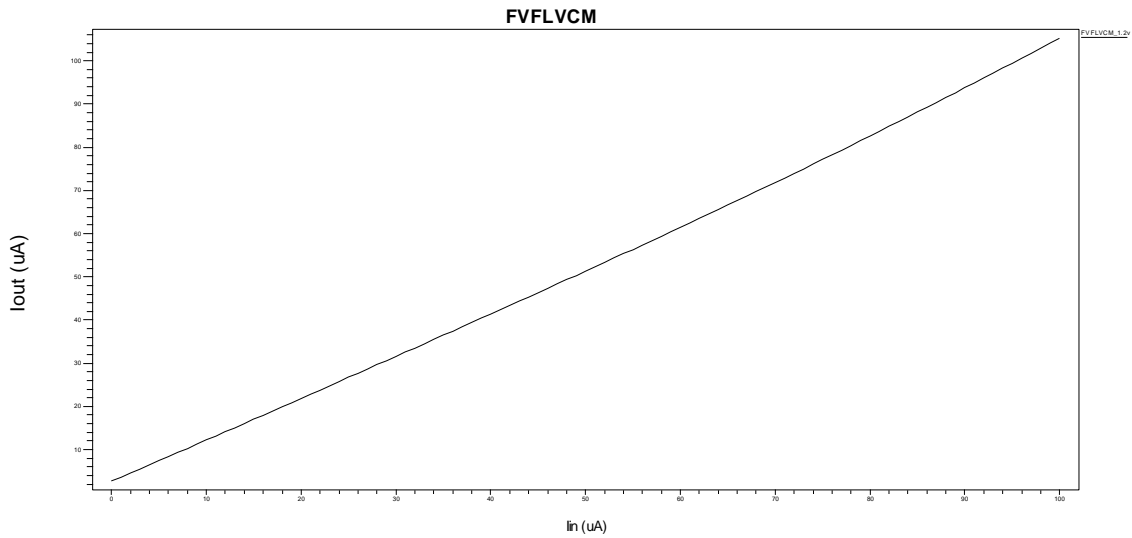


Figure 6.2 DC characteristics of proposed FVFLVCM I

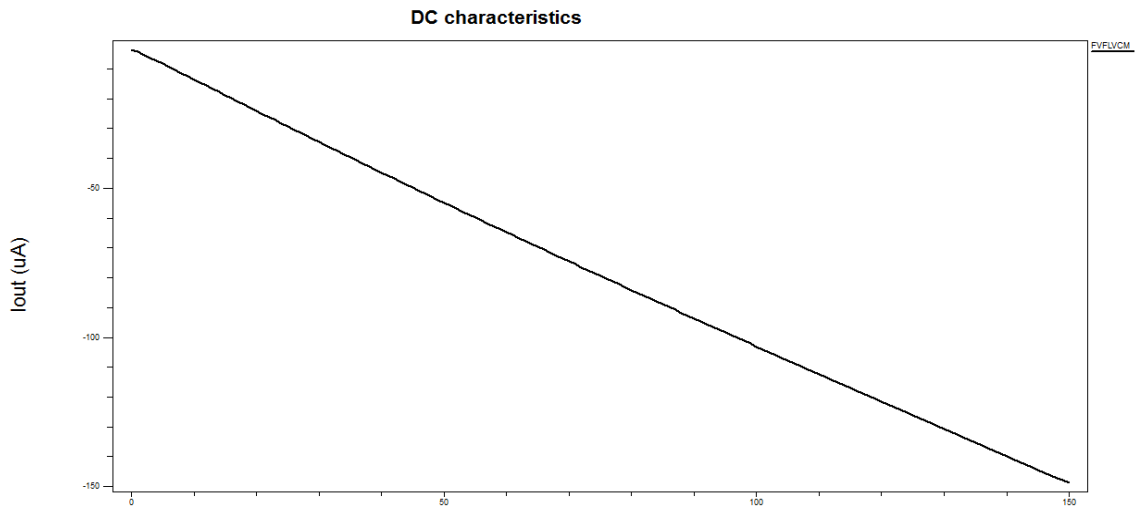


Figure 6.3 DC characteristics of proposed FVFLVCM II

From the Figures 6.1, 6.2 and 6.3, it is observed that output current is following the input current with the small dc errors ($I_{out} - I_{in}$) shown in Figure 6.4 and 6.5. Figure 6.4 and 6.5 Show DC errors of the proposed LVCM & FVFLVCM II and proposed FVFLVCM I at 1.2V & 1V, respectively. Figures 6.6 and 6.7 show the DC power dissipation at the output for the proposed current mirrors. Figures 6.8 and 6.9 show input voltage compliances and input DC resistance of the circuits respectively. The DC error and DC power dissipation of proposed LVCM and FVFLVCM II are obtained as 5.7% & 3.7% and 111.20 μ W & 99.40 μ W respectively. The DC error and the DC power dissipation for the proposed FVFLVCM I at 1.2V & 1V are calculated as 7.8% and 27.6 μ W & 2.26% and 36.74 μ W respectively.

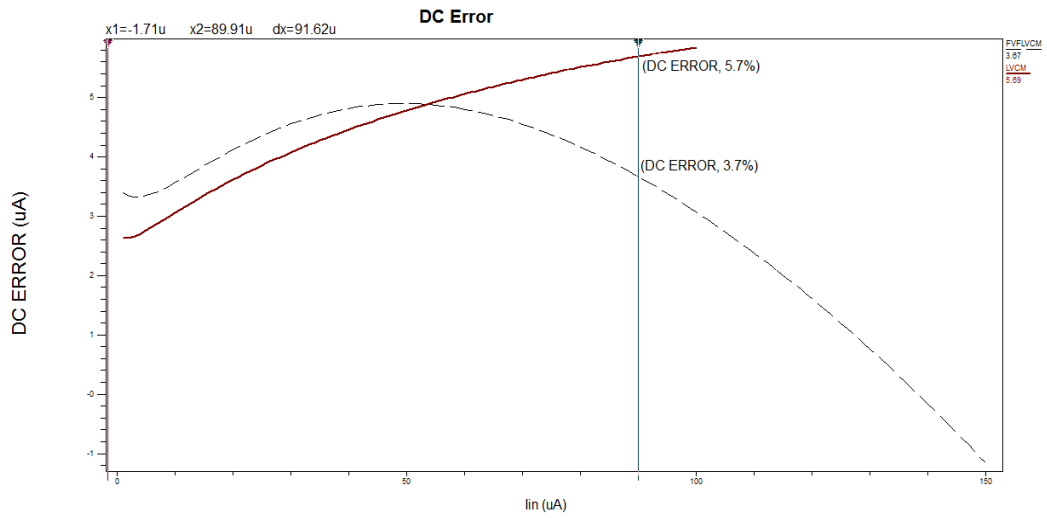


Figure 6.4 DC error of proposed LVCM & FVFLVCM II

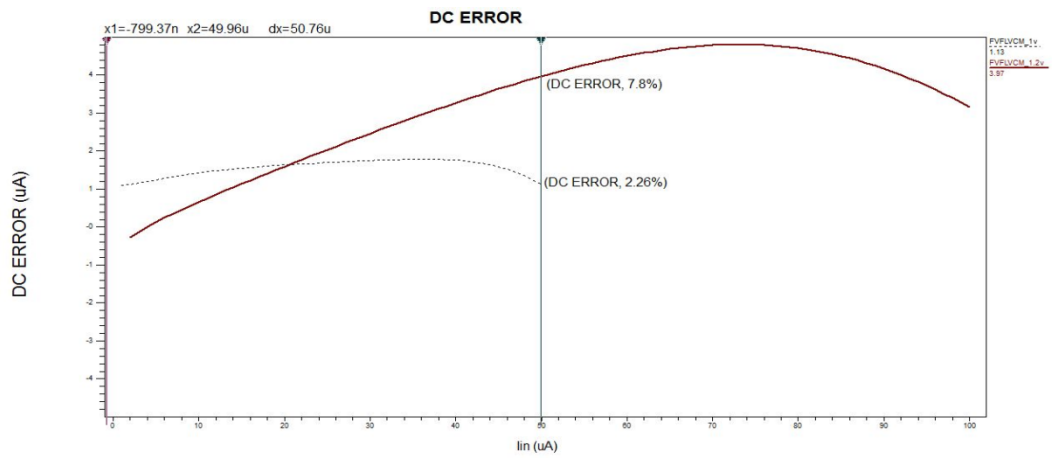


Figure 6.5 DC error of proposed FVFLVCM I at 1.2V & 1V

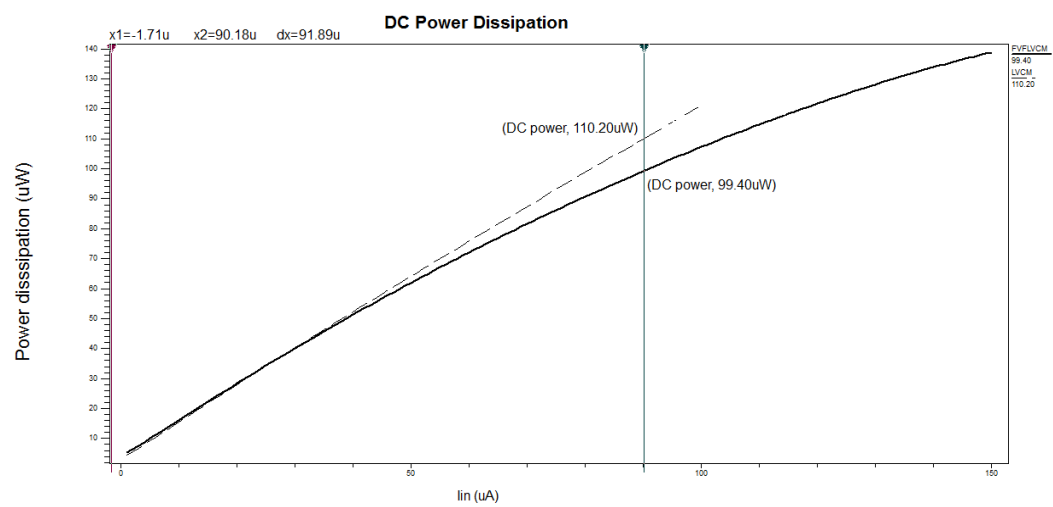


Figure 6.6 DC power dissipation of proposed LVCM & FVFLVCM II

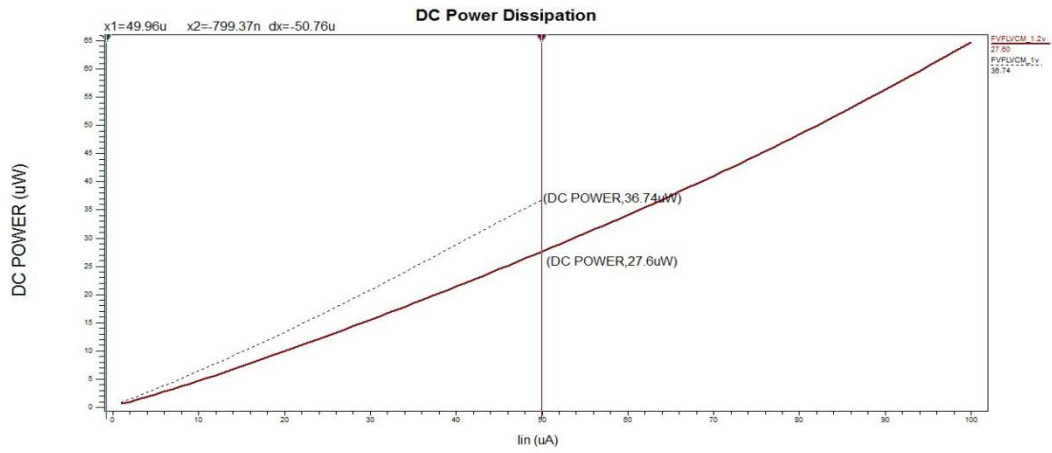


Figure 6.7 DC power dissipation of proposed FVFLVCM I at 1.2V & 1V

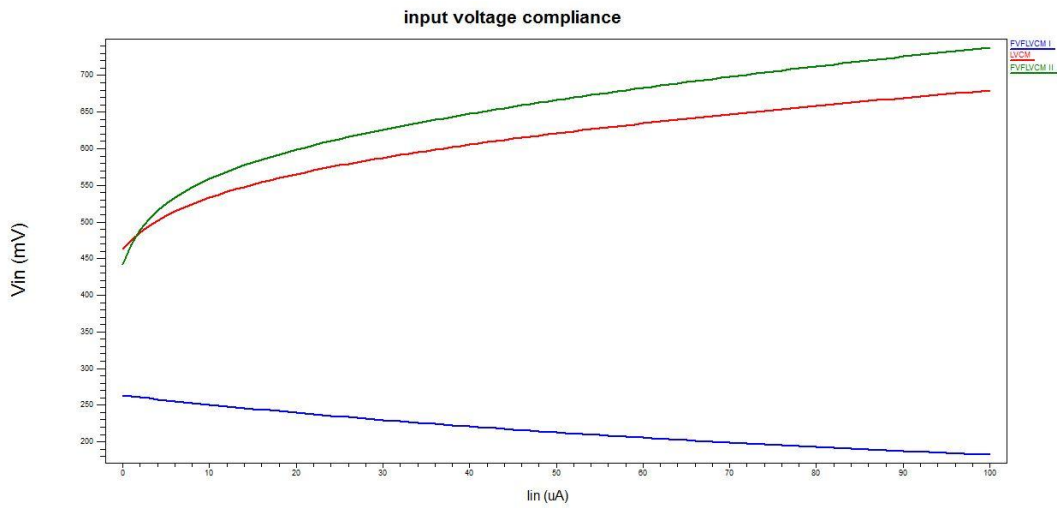


Figure 6.8 Input voltage compliances of proposed circuits

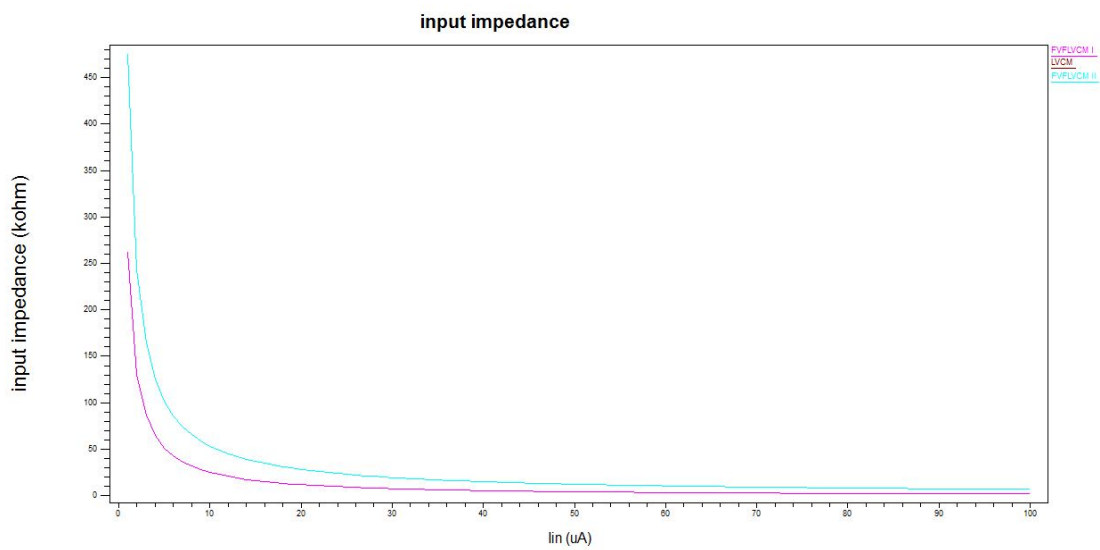


Figure 6.9 DC input resistance of proposed current mirrors

The DC error and DC power dissipation of the all the proposed current mirrors are listed in Table 6.1.

Table 6.1 DC error and DC power dissipation of proposed current mirrors

Current Mirrors	Supply Voltage	DC Error (%)	DC Power Dissipation (μW)
FVFLVCM I	1.2V	7.8%	27.6 μW
FVFLVCM I	1V	2.26%	36.74 μW
LVCM	1.2V	5.7%	111.2 μW
FVFLVCM II	1.2V	3.7%	99.4 μW

6.2 AC characteristics

The frequency responses of the proposed circuits are shown in Figures 6.10, 6.11, 6.12 and 6.13. The frequency responses of the circuits get affected by the value of the feedback element.

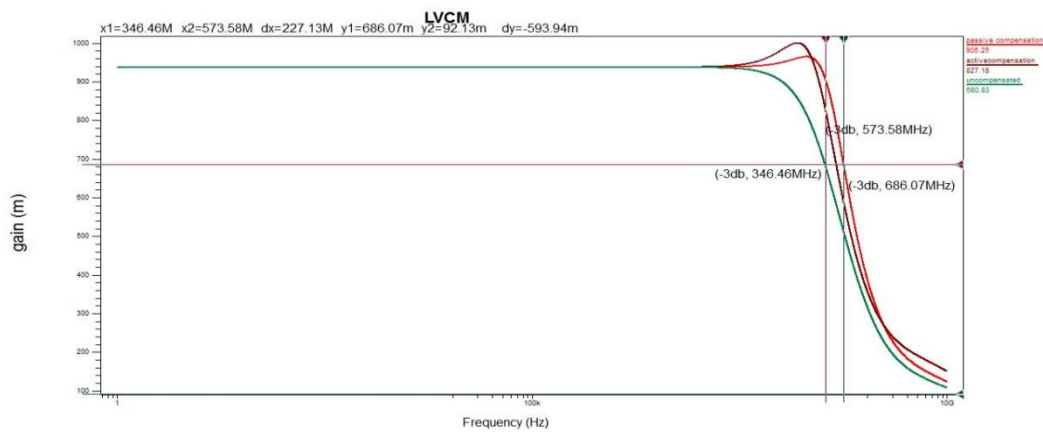


Figure 6.10 Frequency response of proposed LVCM with and without active & passive compensations

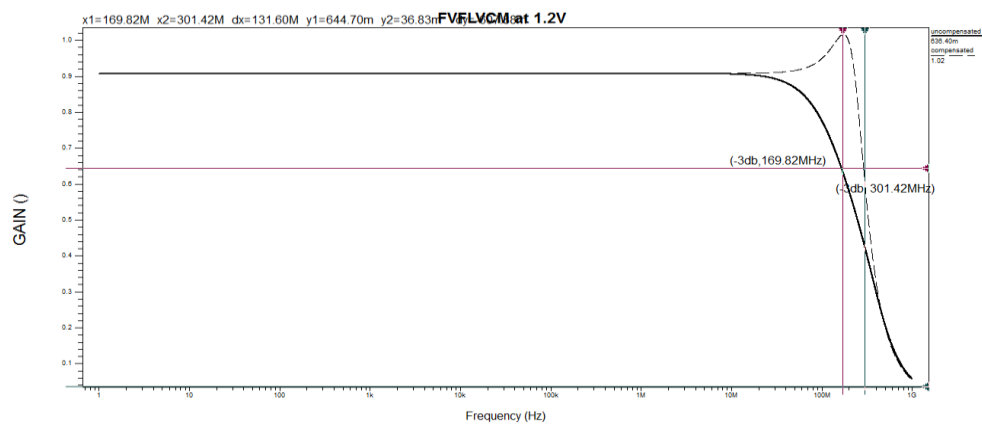


Figure 6.11 Frequency response of proposed FVFLVCM I at 1.2V

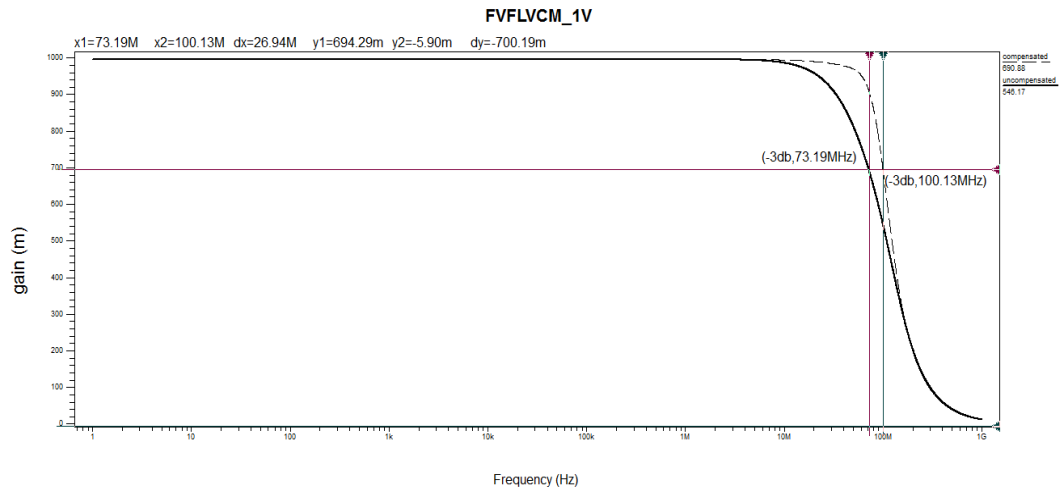


Figure 6.12 Frequency response of proposed FVFLVCM I at 1V

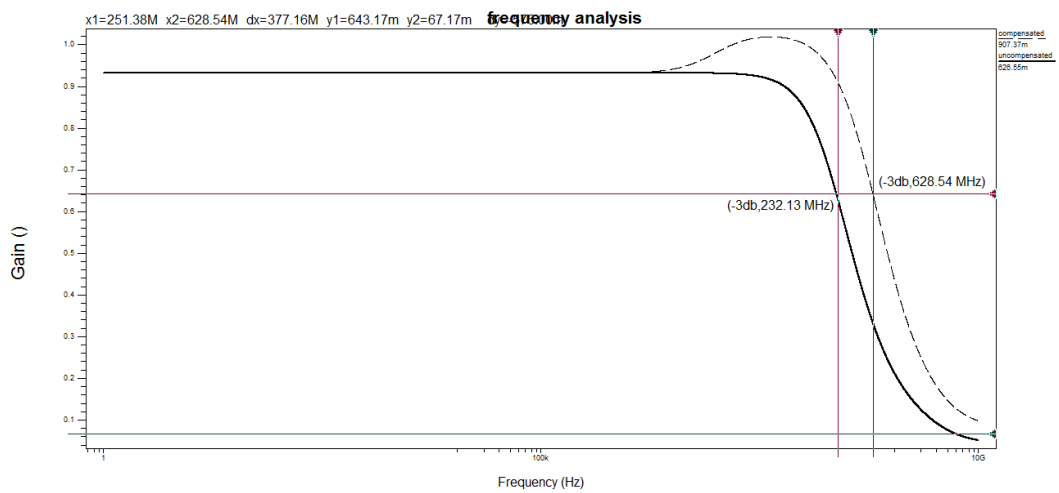


Figure 6.13 Frequency response of proposed FVFLVCM II with and without passive compensation

The -3dB frequency of the all the proposed current mirrors are listed in Table 6.2.

Table 6.2 -3db frequency of proposed current mirrors

Proposed Current Mirrors	Voltage supply	-3db frequency
LVCM	+1.2V	346.46MHz
Passively compensated LVCM	+1.2V	686.07 MHz
Actively compensated LVCM	+1.2V	573.58 MHz
FVFLVCM I	+1.2V	169.82 MHz
Passively compensated FVFLVCM I	+1.2V	301.42MHz
FVFLVCM I	+1V	73.19 MHz
Passively compensated FVFLVCM I	+1V	100.13 MHz
FVFLVCM II	+1.2V	232.13 MHz
Passively compensated FVFLVCM II	+1.2V	628.54 MHz

It is observed from frequency responses shown in Figures 6.10, 6.11, 6.12 and 6.13, the gain remains unchanged by using passive and active compensation techniques. From the table 6.2, it is observed that insertion of passive or active element in feedback path enhances the bandwidth of the LVCM from 79MHz to 122MHz , FVFLVCM I from 169MHz to 301MHz and FVFLVCM II from 232MHz to 629MHz. Figures 6.14 and 6.15 show input impedance variations with frequency of the signal applied to input terminal.

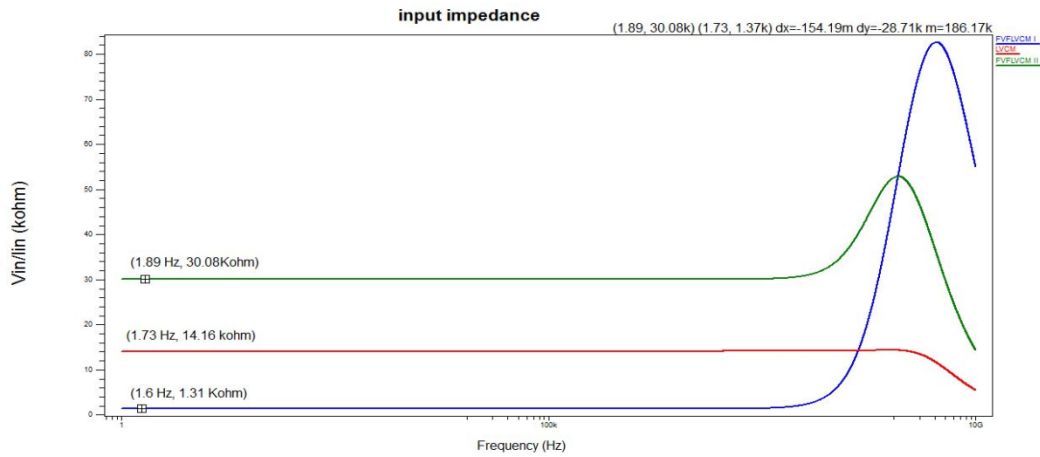


Figure 6.14 Input impedance variations with frequency of input signal

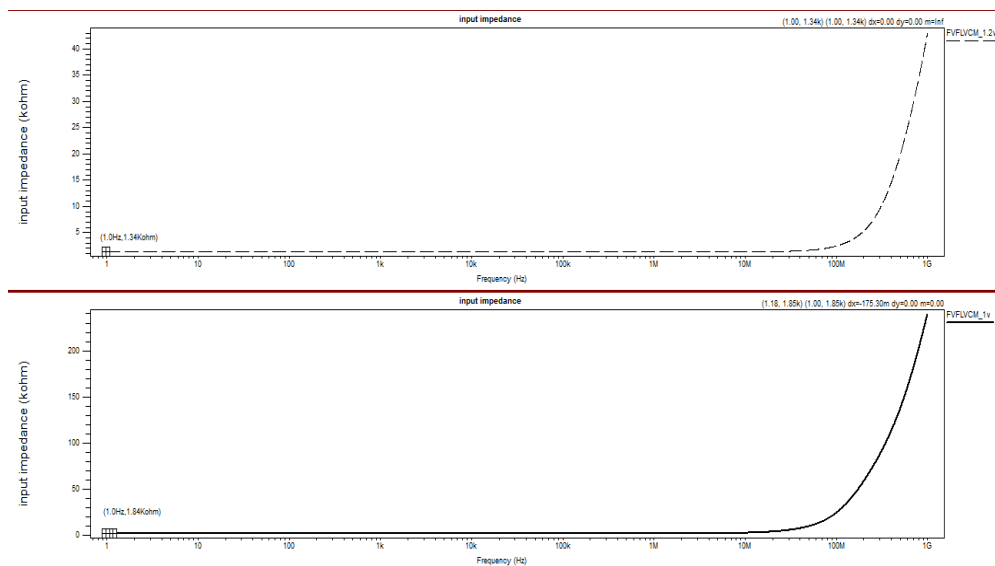


Figure 6.15 Input impedance variation with frequency of input signal at 1.2V and 1V

The Input impedance of the all the proposed current mirrors are listed in Table 6.3.

Table 6.3 Input impedance of proposed current mirrors

Current Mirrors	Voltage Supply	Input impedance
LVCM	+1.2V	14.16 K Ω
FVFLVCM I	+1.2V	1.31 K Ω
FVFLVCM I	+1V	1.84K Ω
FVFLVCM II	+1.2V	30.08 K Ω

From table, it is observed that the input impedance of LVCM, FVFLVCM I and FVFLVCM II are obtained as 14.16 K Ω , 1.31 K Ω at 1.2 V & 1.84K Ω at 1V and 30.08 K Ω respectively.

6.3 Phase and magnitude plots of proposed circuits

Figures 6.16, 6.17, 6.18, 6.19, 6.20, 6.21 and 6.22 show the magnitude and phase plot of the proposed current mirrors. In order to obtain phase margin of the current mirror, phase of the current mirror is noted at gain cross over frequency.

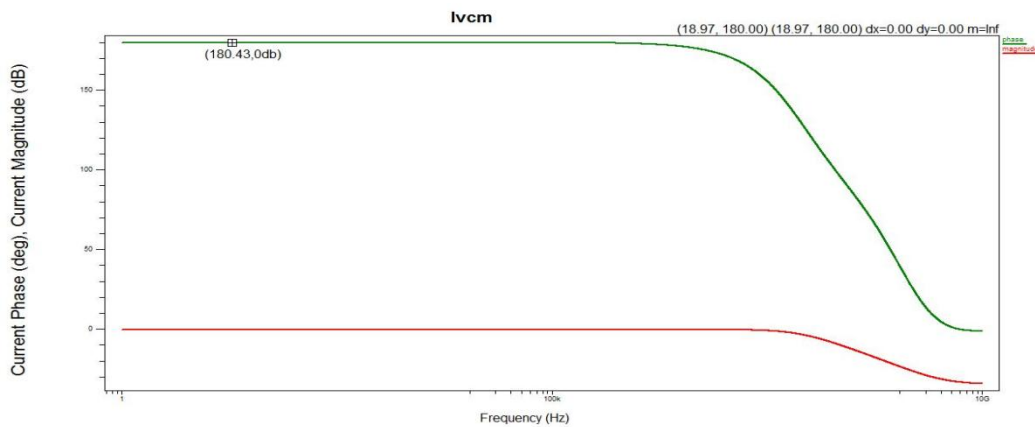


Figure 6.16 Magnitude and Phase plot of LVCM for phase margin calculation

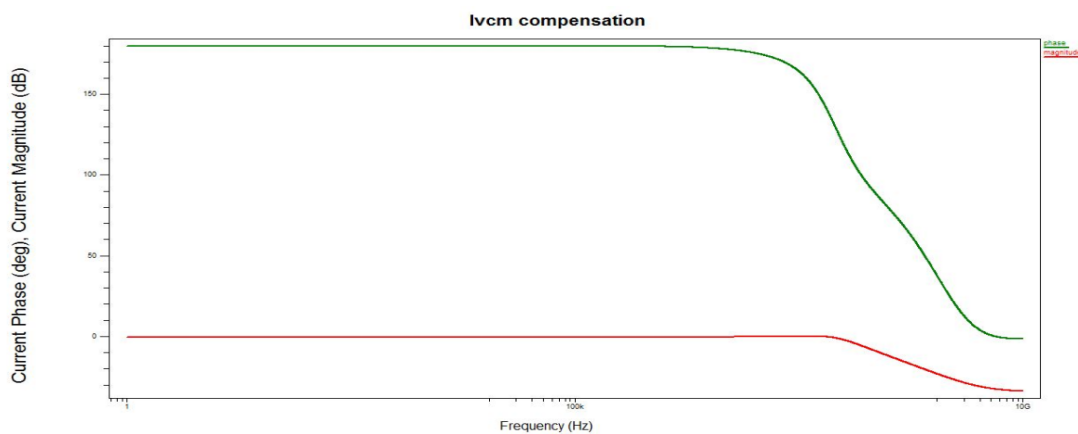


Figure 6.17 Magnitude and Phase plot of passively compensated LVCM for phase margin calculation

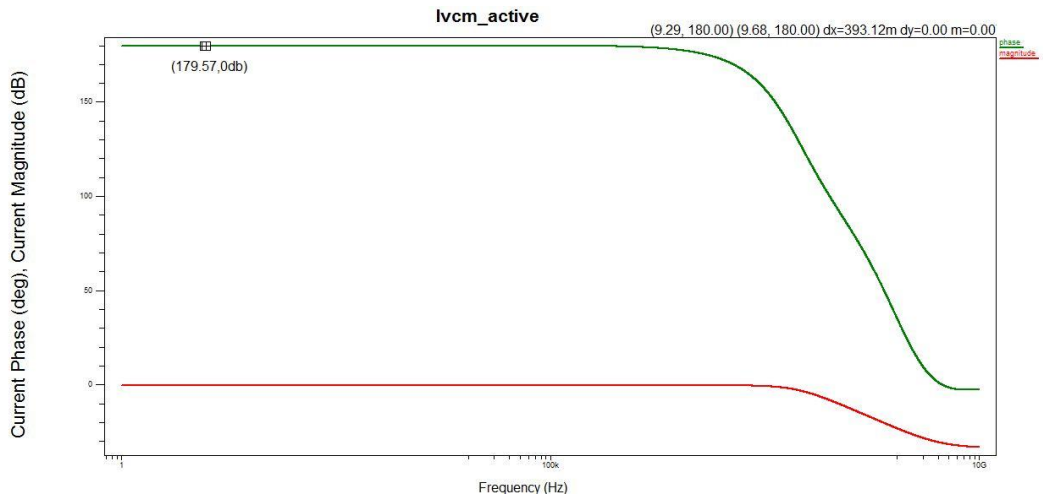


Figure 6.18 Magnitude and Phase plot of actively compensated LVCM for phase margin calculation

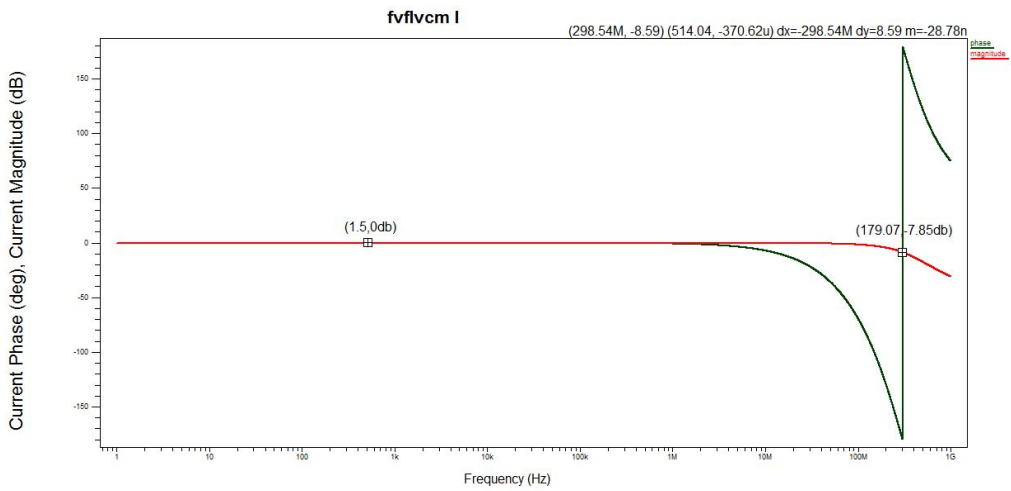


Figure 6.19 Magnitude and Phase plot of FVFLVCM I for phase margin calculation

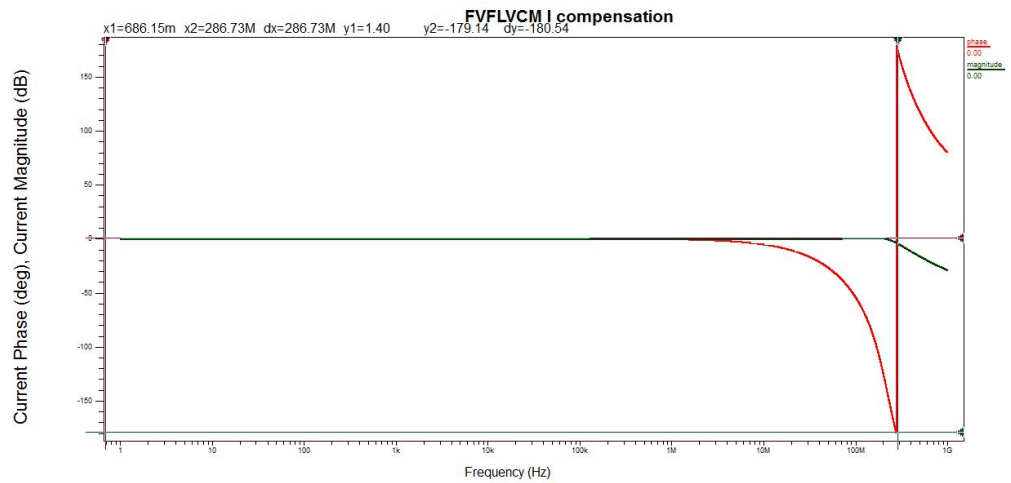


Figure 6.20 Magnitude and Phase plot of passively compensated FVFLVCM I for phase margin calculation

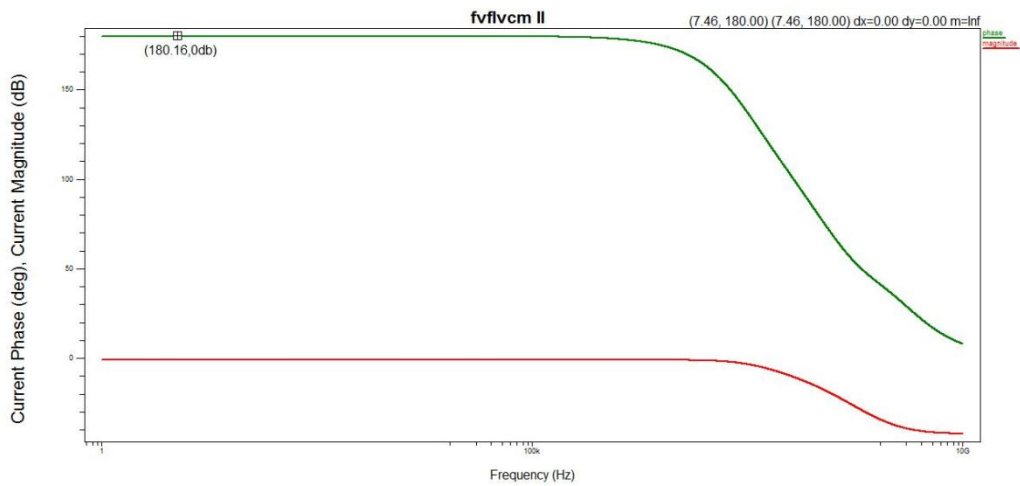


Figure 6.21 Magnitude and Phase plot of FVFLVCM II for phase margin calculation

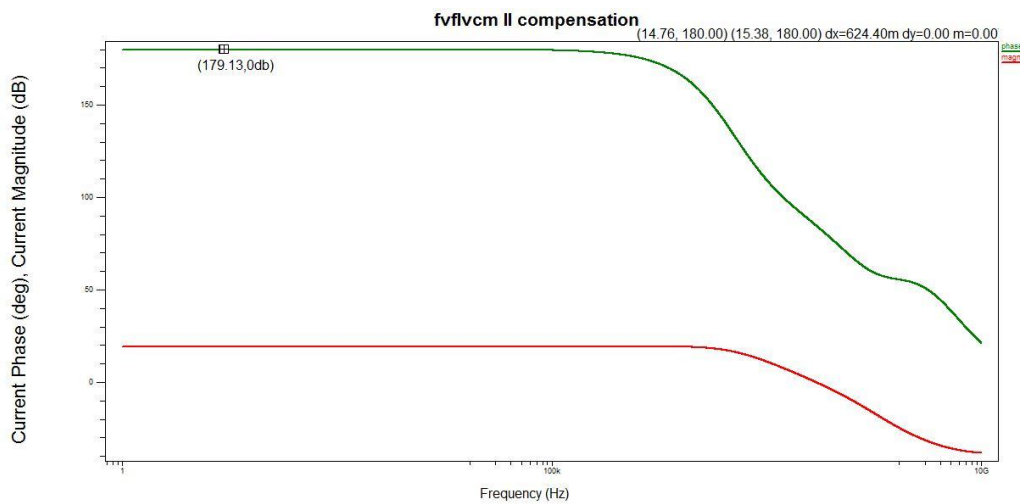


Figure 6.22 Magnitude and Phase plot of passively compensated FVFLVCM II for phase margin calculation

6.4 LDPC decoder

The worst case wiring capacitance of 500 fF is placed at input node of the conventional current mirror, the timing delay is found as $DI = 279$ ns which shows the extra delay due to wiring [42]. Similarly same wiring capacitance is placed at the input node of proposed current mirrors (Figure 5.2, Figure 5.3 and Figure 5.4) and results are obtained as shown in Figure 6.23.

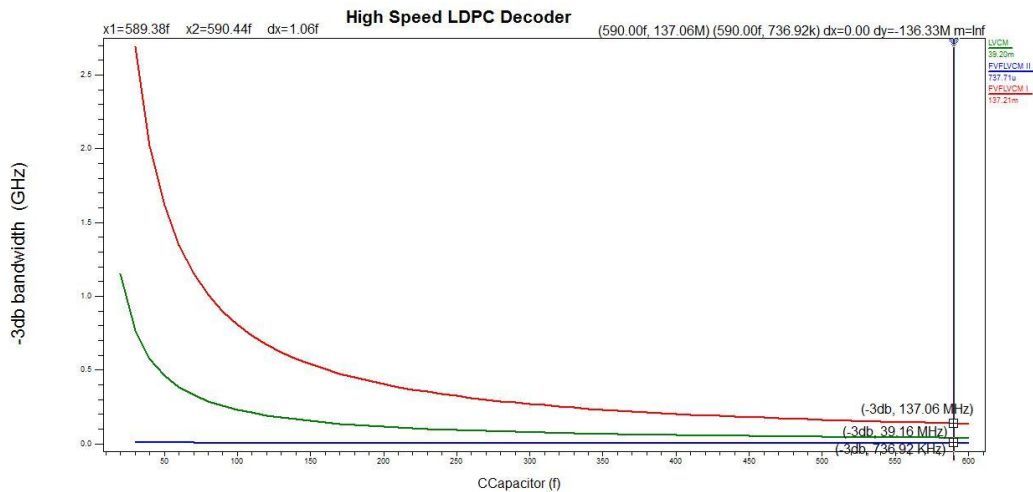


Figure 6.23 -3db bandwidth of proposed current mirrors for High speed LDPC decoder

Table 6.4, shows the Comparison of -3db bandwidth and timing delay for different proposed current mirrors with the conventional current mirror.

Table 6.4 Comparison of -3db bandwidth and timing delay for different proposed current mirrors with conventional current mirror ($c_{in}=90\text{fF}$)

Current Mirrors	-3db bandwidth	Timing Delay
Conventional Current Mirror [41]	483.4 KHz	279ns
FVFLVCM I	137.06 MHz	7.29ns
LVCm	39.16 MHz	25.53ns
FVFLVCM II	736.92 KHz	135.69ns

From Table 6.4, it is observed that the FVFLVCM II has maximum -3db bandwidth and minimum timing delay, therefore it can be preferred over all the proposed current mirrors as well as conventional current mirrors for analog LDPC decoder.

6.5 Adder circuit using FVFLVCM I

Figure 6.24, shows the output current of the adder circuit with respect to I_{in1} for $I_{in2}=10\ \mu\text{A}$. The DC error of 0.99% is calculated at $I_{in1}=100\ \mu\text{A}$ as shown in Table 6.5.

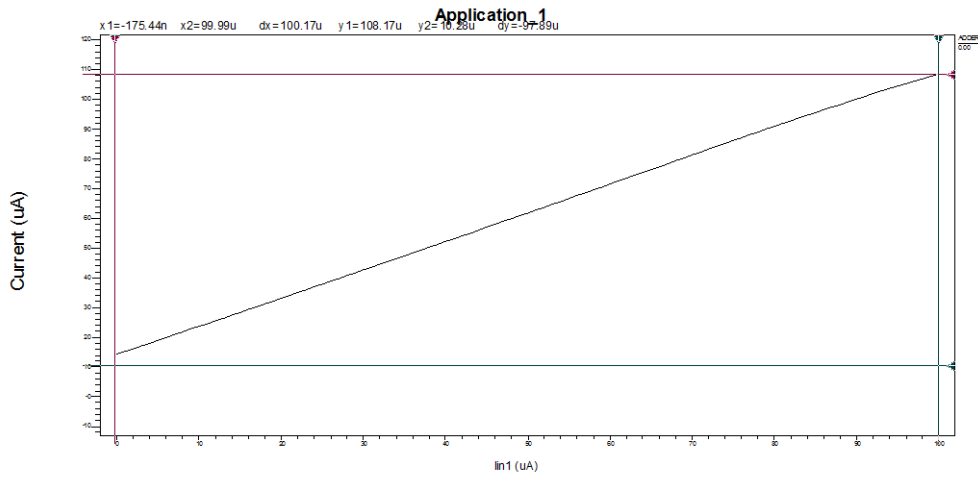


Figure 6.24 DC characteristics of proposed current adder circuit

6.6 Subtractor circuit using FVFLVCM I

Figure 6.25, shows the output current of the subtractor circuit with respect to I_{in1} for $I_{in2}=10 \mu\text{A}$. The DC error of 0.64% is obtained at $I_{in1}=50 \mu\text{A}$ shown in Table.

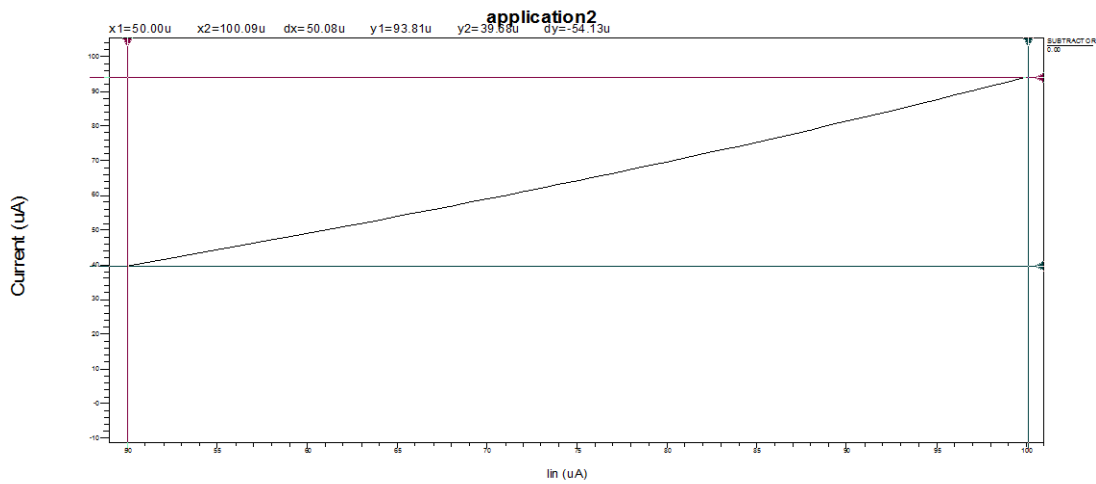


Figure 6.25 DC characteristics of proposed current subtractor circuit at $I_{in1}=50 \mu\text{A}$

Table 6.5, shows the DC error of the adder circuit and the subtractor circuit.

Table 6.5 DC Error of proposed applications

Application	I_{in1}	I_{in2}	I_{out}	DC Error(%)
Adder Circuit	100 μA	10 μA	109.01 μA	0.99%
Subtractor Circuit	50 μA	10 μA	39.68 μA	0.64%

6.7 Comparison of proposed Current mirrors

Table 6.6 compares different parameters of proposed current mirrors with the current mirrors available in literature [35-40].

Table 6.6 Comparison of proposed current mirrors with current mirrors available in literature

Circuit Parameters	[35,36]	[37]	[38]	[39]	[40]	Proposed LVCM	Proposed FVFLVCM I	Proposed FVFLVCM II	
Supply Voltage	1.5 V	1.5 V	1.5 V	1.3 V	1.5 V	1.2 V	1.2 V	1 V	1.2 V
CMOS technology	1.2 μm	0.18 μm	0.18 μm	0.18 μm	0.25 μm	0.18μm	0.18μm	0.18μm	0.18μm
Input current	1 -500 μA	---	0-100 μA	0-100 μA	0-50 μA	0-100 μA	0-100μA	0-50 μA	0-150 μA
-3db frequency	1.2 GHz	212MHz	577MHz	60MHz	403MHz	686 MHz	302MHz	101MHz	629MHz
Input impedance	---	3 K Ω	---	---	1.93 K Ω	17.1 KΩ	1.34KΩ	1.84 KΩ	30.08 KΩ
Output impedance	---	---	---	---	---	---	0.18MΩ	0.71MΩ	---
DC error	---	2.4 %	---	---	3.37 %	5.7 %	7.8 %	2.26%	3.7%
DC power dissipation	---	218 μW	---	---	324.3 μW	111.2μW	27.8 μW	36.74μW	99.4 μW

From the Table 6.6, it is observed that proposed FVFLVCM I has widest range of input current and very high bandwidth along with optimum DC error, supply voltage requirement, input impedance, dc error and dc power dissipation, though other proposed current mirrors also have improved parameters than the current mirrors available in literature, but it is found that FVFLVCM II is the best current mirror for the applicability purpose.

CHAPTER

7

CONCLUSION AND FUTURE SCOPE

The dissertation demonstrates low voltage current mirrors operating at +1V and +1.2V. The compensation techniques have been applied to enhance the bandwidth of the current mirrors. The stability analysis of all the proposed circuits have been performed using time domain and frequency domain approaches. The circuits have higher bandwidth, lower input impedance, lower supply voltage requirement, wider range for input current, lower power dissipation and lower DC error than the current mirrors reported in literature. The proposed current mirrors are also preferred over conventional current mirror for analog LDPC decoders as proposed current mirror are much faster than conventional current mirror. Adder and subtractor circuits with low DC error are also designed using one of the proposed current mirrors. The proposed design works well with low-power, low-voltage analog signal processing applications.

Future Scope

Some suggestions and ideas for future work:

- A high bandwidth low-voltage current mirror can be designed using wideband flipped voltage follower, which is designed by implementing inductive compensation technique.
- A current-mode technique can be applied to the proposed current mirrors of a block of equality nodes circuit by creating a negative feedback loop using an operational transconductance amplifier (OTA) in order to improve the timing delay.
- A gain boosting circuit block can be used in the proposed current mirrors in order to achieve the unity gain.

LIST OF PUBLICATIONS

- 1) Abhishek Shrivastava and Rishikesh Pandey, “A Novel Flipped Voltage Based Low-Voltage Current Mirror” Communicated for the possible publication in Radio Engineering.
- 2) Abhishek Shrivastava and Rishikesh Pandey, “Flipped voltage follower based low voltage current mirror with low input impedance and high output impedance” Communicated for the possible publication in Turkish Journal of Electrical Engineering and Computer Science.

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APPENDIX

➤ TSMC NMOS & PMOS model files 0.18 μ m CMOS technology

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+K3B  = 4.5116437  W0    = 1E-7      NLX  = 1.870758E-7
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+DVT0  = 1.3621338  DVT1  = 0.3845146  DVT2  = 0.0577255
+U0   = 259.5304169  UA   = -1.413292E-9  UB   = 2.229959E-18
+UC   = 4.525942E-11  VSAT = 9.411671E4   A0   = 1.7572867
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+KETA = -4.331915E-3  A1   = 0           A2   = 1
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+XL   = 0          XW    = -1E-8      DWG  = -1.365589E-8
+DWB  = 1.045599E-8  VOFF  = -0.0927546  NFACTOR = 2.4494296
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+CDSCB = 0         ETA0  = 3.175457E-3  ETAB  = 3.494694E-5
+DSUB = 0.0175288  PCLM  = 0.7273497  PDIBLC1 = 0.1886574
+PDIBLC2 = 2.617136E-3  PDIBLCB = -0.1      DROUT = 0.7779462
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+KT1L = 0          KT2   = 0.022     UA1   = 4.31E-9
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+LLN = 1 LW = 0 LWN = 1
+LWL = 0 CAPMOD = 2 XPART = 0.5
+CGDO = 8.53E-10 CGSO = 8.53E-10 CGBO = 1E-12
+CJ = 9.513993E-4 PB = 0.8 MJ = 0.3773625
+CJSW = 2.600853E-10 PBSW = 0.8157101 MJSW = 0.1004233
+CJSWG = 3.3E-10 PBSWG = 0.8157101 MJSWG = 0.1004233
+CF = 0 PVTH0 = -8.863347E-4 PRDSW = -3.6877287
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+PU0 = 16.6114107 PUA = 6.572846E-11 PUB = 0
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+K3B = 13.8420955 W0 = 1E-6 NLX = 1.337719E-7
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+DVT0 = 0.5281977 DVT1 = 0.2185978 DVT2 = 0.1
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+WR = 1 WINT = 0 LINT = 2.718137E-8
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+PDIBLC2 = 0.0402861  PDIBLCB = -1E-3      DROUT = 0
+PSCBE1 = 1.034924E10  PSCBE2 = 2.991339E-9  PVAG = 15
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+UB1 = -7.61E-18  UC1 = -5.6E-11   AT = 3.3E4
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+WWN = 1         WWL = 0         LL = 0
+LLN = 1         LW = 0         LWN = 1
+LWL = 0         CAPMOD = 2      XPART = 0.5
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+CJ = 1.160855E-3  PB = 0.8484374    MJ = 0.4079216
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