ANALYSIS AND DESIGN OF ROBUST POWER DOUBLE IMPLANTED MOSFET ON 6H SILICON CARBIDE WAFERS

A THESIS

SUBMITTED FOR THE AWARD OF THE DEGREE OF

DOCTOR OF PHILOSOPHY

BY

MUNISH VASHISHATH
(REGN.NO.-9021252)

DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING
THAPAR UNIVERSITY
PATIALA-147004, INDIA
NOVEMBER 2010

CERTIFICATE

Certified that the thesis entitled ***"Analysis and Design of Robust Power Double Implanted MOSFET on 6H Silicon Carbide Wafers"*** being submitted by **Mr. Munish Vashishath** to the **Department of Electronics and Communication Engineering, Thapar University, Patiala** in fulfillment of the requirements for the award of degree of "Doctor of Philosophy" is a record of bona fide research work carried out by him. He has worked under my guidance and supervision and fulfilled the requirements of submission of this thesis which has reached the requisite standard. The matter presented in this thesis does not incorporate any material previously published or written by any other person except where do references are made in the text.

The results contained in this thesis have not been submitted in part or full to any other institute or university for the award of degree or diploma.

(Dr.A.K.Chatterjee) 2.11.10
Professor and Head,
Department of Electronics and Communication Engineering,
Thapar University,
Patiala (Punjab)-147004
India

ACKNOWLEDGEMENT

Walking on the trail blazed by an exemplary phenomenon Baba Ji-the Supreme Commander of my life, I humbly and earnestly would like to thank one and all who acted as building material in the citadel of my success.

Although the Knowledge like electricity pervades everywhere yet the Teacher is the point where it shines as light. I am extremely lucky to have an opportunity to blossom under the supervision and guidance of Dr.A.K.Chatterjee, Professor and Head, Department of Electronics and Communication Engineering, Thapar University, Patiala who helped me to grow like Phoenix out of the ashes of my shortcomings and failures. His charismatic personality delves in the knowledge to bring zeal and enlightenments in the lives of not only his students but also humanity. To me, he is not a man but a current of love who treaded with me through thick and thin. Also Mrs. C.Chatterjee, wife of Dr.A.K.Chatterjee, has equally taken a lot of pains for me and deserves special thanks.

I am greatful to Dr.K.K.Raina, Deputy Director & Dean of Faculty Affairs, Thapar University, Patiala for valuable guidance and Dr. Ravinder Agarwal, Head, University Scientific Instrumentation Centre, Thapar University, Patiala for many helpful suggestions.

I express my profound sense of gratitude to Dr. P.K.Bansal, Principal, MIMIT, Malout and Dr. Ashok Kumar Arora, Director/Principal, YMCA Institute of Engineering, Faridabad for his invaluable guidance, support, valuable suggestions, sympathetic and encouraging attitude throughout this work. I am modestly bowing my head in feet of divine Lord to thank them all for their love, support and sacrifices.

I wish to express thanks to all persons who with their encouraging, caring words, constructive criticism and suggestions have contributed directly or indirectly in a significant way towards completion of this work. I gratefully acknowledge for the best wishes and prayers of my friends.

A boat held to its moorings will see the floods pass by; but detached of its moorings, may not survive the flood. The support of all the members of my family enthused me to work even while facing the blues. I take pride in being the son of ideal parents who sacrificed their little joys to bring me to the realization of my dreams and

their hopes. It is said that realization comes to those who are immersed in love. I owe a lot to my family members. It is my grandfather, Sh. Ram Ditta Mal, who being a teacher is responsible to provide me the encouragement for research work. It is my father, Sh. Joginder Lal Vashishath, who being a teacher is solely responsible for my falling in love with academics. Right from my childhood my mother, Smt. Nirmal Sharma inculcated in me the virtues of discipline and honesty. These traits of my character have played a vital role in the present endeavor. I am also thankful to my brothers Mr. Neeraj Vashishath and Mr. Rohit Vashishath who supported me from time to time during my research work. I am grateful to my wife, Mrs. Sharmila Sharma who encouraged me constantly in completing this work, to my daughter, Ritika and son, Rishi who remained deprived of my love and care during this period.

I am laying before you the result of numerous sleepless nights, strenuous hard work, determined and gritty solutions of the fights with my own self but everything is possible only with Almighty's grace:

"What you make me know,
That alone I know,
What you make me see,
That alone I see."

MVashishath 02-XI-2010
(Munish Vashishath)

ABSTRACT

Silicon Carbide is a wide energy gap semiconductor that possesses a combination of parameters that make it ideal for various applications in electronic industry. Its physical properties such as high electric field strength, high saturation drift velocity and high thermal conductivity has placed SiC at the center of renewed focus of semiconductor material and device research amongst other wide energy gap semiconductors. SiC has tremendous advantages because of rapidly maturing technology for making single crystal substrates. In addition, the ability to form a layer of thermal SiO_2 on SiC in a similar way to provide the fabrication of Silicon Carbide MOS-based electronic devices. Thus, given the superiority and success of MOS-based devices in applications like high power/temperature electronics and storage devices (nonvolatile memories), SiC is perceived to be the semiconductor of choice with potential to revolutionize the way the electronic systems are designed.

In view of current study of power switching devices, the large efforts are concentrated on unipolar devices. These include Field Effect Transistors (FETs) that exist in many types, JFET, MOSFET and MESFET. In low power electronic applications that require high switching speed, the Si MOSFETs have become the dominant technology for many reasons. The relatively low breakdown field in Si and the resistance of drift region that increases rapidly with increasing blocking voltage generally limit the use of Si MOSFETs to 500V and below. The advantages of SiC material properties, in particular breakdown field, makes SiC MOSFETs a very promising candidate for high power switching devices. The specific on-resistance of a SiC power device is expected to be 100-200 times lower than a rated silicon device. Its much lower thermal minority carrier

generation implies lower leakage currents and device operation at higher temperatures, arising from self heating due to power dissipation is more tolerable. Moreover, the thermal conductivity of SiC is three times higher than Si and even higher than copper at room temperature.

Due to excellent physical and electrical properties such as high breakdown electric field, wide bandgap, high thermal conductivity and high electron saturation velocity, silicon carbide offers great potential for development of high temperature, high power and high voltage devices. Significant progress in SiC power MOSFETs have been demonstrated with the fasbrication of UMOS,DIMOSFET, triple implanted vertical MOSFET and accumulation –mode MOSFET (ACCUFETs).

Power MOSFET requires excellent electrical characteristics. Due to these characteristics, it would be desirable to utilize power MOSFETs for high voltage/power electronic applications. However, the blocking capability of a MOSFET is based on the ratings of the reverse body of the diode of the drift region. The blocking voltage is determined in part by the distance from source to drain. High blocking capability implies high resistance because of geometry, so there is a trade off between low drift region resistance values and device voltage capability.

The research work carried out here on 6H-Silicon Carbide Double Implanted Power MOSFET has been an attempt to understand the performance of the device with respect to power dissipation and breakdown voltage for various types of doping profiles in the drift region of the device. The doping profiles used are primarily uniformly doped with field dependant and independent mobility, linearly graded, Gaussian and Complementary Error Function distribution. Although a lot of work has been has been

described in the literature over the last two decades, no specific work has been reported in which the graded profiles have been used in the drift region of 6H-SiC DIMOSFET for this type of analysis. The ultimate aim for making this study is to provide a graded profile in the drift region of the MOSFET with lower doping at the top of the device to a higher doping near the drain. This type of profile will help in increasing the breakdown voltage while at the same time will reduce the series parasitic resistance at the lower end of the device and thereby reduce the overall specific on-resistance. In this work, we have succeeded in establishing that the power dissipation is minimum in the linearly graded profile evaluated at a current density of 1000 A/cm^2, whereas breakdown voltage is maximum of 20kV in the Complementary Error Function profile.

TABLE OF CONTENTS

LIST OF TABLES

LIST OF FIGURES

CHAPTER 1

INTRODUCTION

1.1 PREAMBLE

Silicon carbide has been recently given the attention as a potential material for high power and high frequency device applications. Properties such as large breakdown electric field, large saturated electronic drift velocity, wide bandgap, small dielectric constant, reasonably high electron mobility and high thermal conductivity will make silicon carbide an attractive semiconductor for fabricating power devices with reduced power losses and die sizes. High thermal conductivity and breakdown electric field also suggest that integration of the devices made from SiC is possible with higher package densities. The high breakdown fields in Silicon Carbide allow for drift regions that are eight to ten times thinner than Silicon high voltage devices. This makes silicon carbide power devices viable even in kilovolt range and beyond. Hence, the improvement in the current handling capability of these devices can be achieved [1-5].

The SiC lattice consists of alternating planes of silicon and carbon atoms, and the stacking sequence of these planes defines different polytypes of the material identified by the repeat distance of the stacking sequence (e.g. 3C,4H & 6H). The lattice constant in the basal plane is virtually identical for all polytypes, but important electrical properties such as band gap energy, electron mobility and critical field differ significantly between the polytypes [6-7].

The high thermal and chemical stability of SiC makes certain types of fabrications difficult. Diffusion co-efficients for dopant atoms are extremely low at temperatures typically used for silicon device processing and for this reason selective doping of SiC are accomplished by ion implantation. Implant activation typically requires annealing at temperatures between 1000 and 1700°C. Chemical etching is impractical owing to the high chemical stability of SiC and selective etching is accomplished by reactive ion etching (RIE) using fluorinated gases [8-15].

SiC offers significant advantages for power electronics applications such as lamp ballasts, motor control, medical electronics, automotive electronics, high-density high-frequency power supplies and smart-power application-specific integrated circuits. Hence, Silicon Carbide based MOSFET can be used in high power applications [16-17].

1.2 SILICON CARBIDE POLYTYPES

Silicon is the material dominating the electronics industry today. Silicon Carbide (SiC), however, has superior properties for power devices as compared to Silicon. In recent years, activity in silicon carbide (SiC) device development has increased considerably due to the need for electronic devices capable of operation at high power levels and high temperature. The main strength of Silicon Carbide is that it can withstand high field strengths, it offers better heat-conducting capacity than copper at room temperature and it has a large energy band gap, which means that electrical components made from SiC continue functioning even when the mercury starts climbing. With very high thermal conductivity (~5.0 W/cm), high saturated electron drift velocity (~2.7 x 10^7

cm/s) and high breakdown electric field strength (~3 MV/cm), SiC is a material of choice for high temperature, high voltage, high frequency and high power applications. Table1 lists some electrical properties of the most common SiC polytypes in comparison to that of Si, GaAs and GaN [18-19].

The most important SiC property of all is the large bandgap, which is nearly three times larger than that of silicon. The large Si-C bonding energy makes SiC resistant to chemical attack and radiation. Silicon carbide belongs to a class of semiconductors commonly known as wide band gap semiconductors, where conventional semiconductors like Si and GaAs cannot adequately perform under extreme conditions. The wider band gap of SiC also enables one to design smaller, higher density devices that will withstand high voltages. Also, the thermal conductivity of SiC (4.9 W/m-K) is much larger than that of Si and GaAs and is a major advantage for SiC based devices. The high thermal conductivity of SiC decreases the need for special packaging and system cooling for successful device operation.

Silicon Carbide occurs in many different crystal structures (called polytypes, which is a condition known as polytypism) with each crystal structure having its own unique electrical and optical properties. The difference between the polytypes is the staking order between the double layers of carbon and silicon atoms. In Figure-1.1, the stacking sequence is shown for the three most common polytypes 3C, 4H and 6H-SiC. Cubic and hexagonal crystal structures of Silicon Carbide are shown in Figure-1.2. If we designate a Si-C atom pair in an A- plane in a close packed lattice as A, and in the B-plane as B, and in the C-plane as C, then we can generate a series of lattice unit cells by variation of SiC plane stacking sequence along the principal crystal axis as in Figure-1.1.

The ABCABC... stacking, will generate the 3C-SiC zinc-blende lattice, and ABAB... stacking, will generate the 2H-SiC wurtzite lattice. Other stacking sequences, such as ABACABAC.. will generate 4H-SiC; and ABCACB... will generate 6H-SiC. The number of atoms per unit cell varies from polytype to polytype, significantly affecting the number of electronic energy bands and vibrational branches possible for a given polytype. This diversity in electronic and vibrational band structures profoundly affect the physical properties of the different polytypes. Some of these differences are listed in Table-1.1.

Table-1.1 Comparison of electronic properties of SiC with Si, GaAs and GaN

	Si	**GaAs**	**GaN**	**6H-SiC**	**4H-SiC**	**3C-SiC**
Bandgap (eV)	1.1	1.142	3.39	3	3.26	2.2
Breakdown field @ $10^{17}cm^{-3}$(MV/cm)	0.6	0.6	3.3	3.2	3.0	1.5
Electron mobility @$10^{16}cm^{-3}$ (cm^2/V-s)	1100	6000	1000	370	800	750
Hole mobility @$10^{16}cm^{-3}$ (cm^2/V-s)	420	320	200	90	115	40
Saturated electron drift velocity (cm/s)	10^7	10^7	$2.5x10^7$	$2x10^7$	$2x10^7$	$2.x10^7$
Intrinsic concentration, n_i (cm^{-3})	$1.5x10^{10}$	$1.9x\ 10^{-10}$	$2.1x10^6$	$2.3x10^{-6}$	$8.2x10^{-9}$	$6.92x10^{-9}$
Thermal conductivity (W/cm-K)	1.5	0.55	1.3	4.9	4.9	5

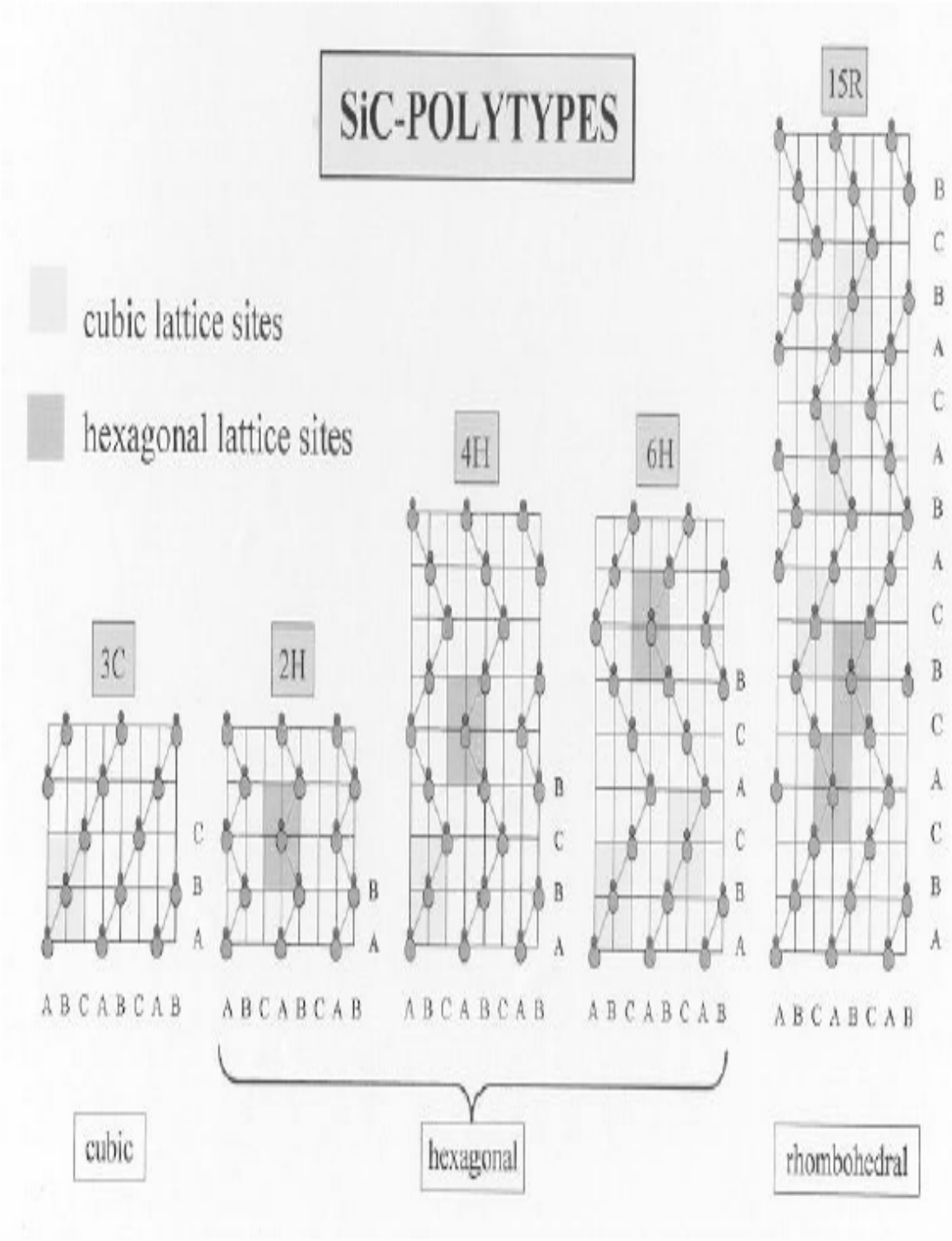

Figure-1.1: Stacking sequence of the most common polytypes of SiC

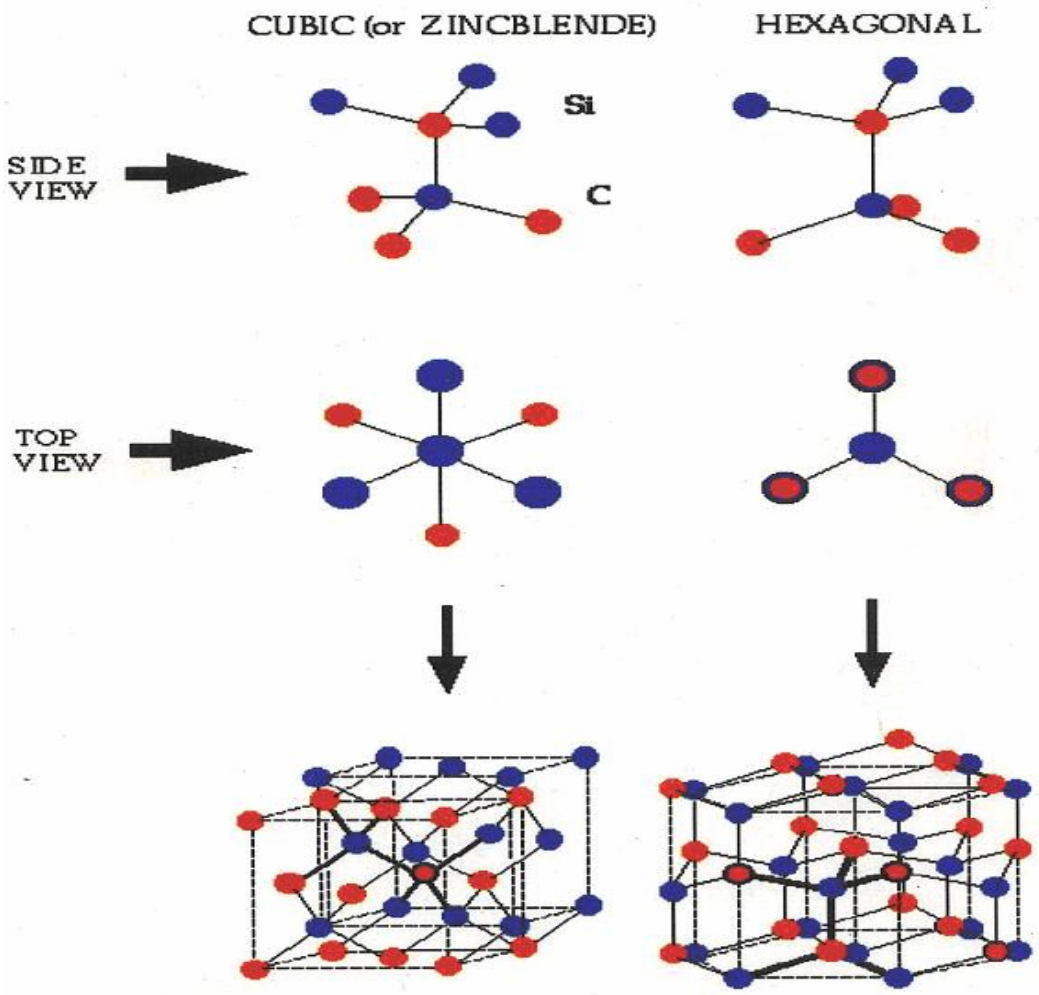

Figure-1.2: Crystal structure of Silicon Carbide

Considering the 6H-SiC polytype, the hexagonal site gives rise to the lowest donor level with an activation energy of approximately 85 meV (ΔEh =Ec-85 meV). The two cubic sites, k1 and k2, yield deeper donor levels with activation energies of 138 meV (ΔEk1 = Ec-138 meV) and 142 meV (ΔEk2 = Ec-142 meV), respectively. In the 4H-SiC polytype there are only two inequivalent sites, one hexagonal and one cubic. In 3C-SiC there is of course only one cubic site and in 2H there is only one hexagonal site. The 6H-SiC polytype can thus be characterized as having donors (or acceptors) which are 33%

hexagonal, whereas the 4H- and 2H-SiC polytypes are 50% and 100% hexagonal, respectively.

Of the numerous polytypic forms of Silicon Carbide, 4H- and 6H-SiC electronic devices presently are the most promising due to the availability and quality of reproducible single - crystal wafers of these polytypes. The availability of 6H-SiC and 4H-SiC polytypes in bulk wafer form as shown in Figure-1.1 has helped SiC to emerge as one of the relatively mature wide-band semiconductor technologies. SiC is a material with immense potential for use in heterostructure electronic devices, which take advantage of differing band gaps, carrier mobilities, etc. However, there are many crucial crystal growth and device fabrication issues that have to be addressed before SiC-based devices and circuits are ready for scale up and reliable incorporation into electronic systems. The most important issue is controlled and repeatable doping in SiC device structures [20].

1.3 POWER MOSFETs in SILICON CARBIDE

Power MOSFETs differ from bipolar transistors in operating principles, specifications and performance. In fact, the performance characteristics of MOSFETs are generally superior to those of bipolar transistors with significantly faster switching time, simpler driver circuitry, the absence of or reduction of the second breakdown failure mechanism, the ability to be paralleled and stable gain and response time over a wide temperature range [21-23].

A conventional n-p-n bipolar power transistor is a current driven device whose three terminals are connected to the silicon /silicon carbide by alloyed metal contacts. Bipolar transistors are described as minority carrier devices in which injected minority carriers recombine with majority carriers. A drawback of recombination is that it limits the operating speed of the device and because of its current driven base-emitter input, a bipolar transistor presents a low impedance load to its driving circuit. In most power circuits, this low-impedance input requires somewhat complex drive circuitry [24-25].

By the virtue of electrically-isolated gate, a MOSFET is described as a high-input impedance, voltage-controlled device, whereas a bipolar transistor is low-input impedance, current controlled device. As a majority carrier semiconductor, a MOSFET stores no charge and so can switch faster than a bipolar switch. Majority carrier semiconductors also tend to slow down as temperature increases. This effect, brought about by the carrier mobility (where mobility is a term that defines the average velocity of carrier in terms of the electrical field imposed on it) makes a MOSFET more resistive at elevated temperatures and much more immune to thermal-runaway problem as experienced by bipolar devices.

Power switches can be considered as the heart of all power electronic systems. The increased power capabilities, ease of control and reduced costs of power switches have made power electronic systems affordable in large number of applications. The first power switches were thyristors and bipolar transistors. Thyristors were used in higher power systems because their ratings were scaled at faster pace than bipolar transistors. Bipolar transistors were favored for low and medium power applications because of their faster switching capability. The rating of these devices grew steadily until the late 1970s,

the year in which the first power MOSFET was introduced. Since the introduction of the first power MOSFET, Si power MOSFET have been immensely improved and has become the dominant device technology since 1980s for many applications, the reasons being: (1) MOSFET has very high input impedance due to its MOS gate structure. Hence, it provides the simplest gate drive requirements. The creation of either inversion layers or accumulation layers under the MOS channel can be controlled using integrated circuits because small gate current is required to charge and discharge the high input gate capacitance. (2) The MOSFET is majority carrier device hence there is no minority charge storage involved in its operation. This results in faster switching operation. (3) Compared to bipolar transistors the MOSFET has superior ruggedness and forward biased safe operating area which allows the elimination of snubber circuits for protection of the switch during operation in typical hard-switching applications. (4) As the majority carriers in silicon exhibits increasing resistivity with temperature, the thermal runaway behaviour is avoided in MOSFETs. MOSFET devices are formed as parallel combinations of many thousands of individual MOSFET cells to take advantage of thermal behaviour. Any device carrying excess current will heat up and become more resistive, diverting current into parallel paths. Excessive loss still produces thermal failure in MOSFET, but there is no unstable runaway effect if the parasitic BJT does not act. Due to these excellent characteristics, it would be desirable to utilize power MOSFETs for high voltage/power electronic applications [26-27]. However, the blocking voltage capability of the MOSFET is based upon the ratings of the reverse body diode of the drift region. This blocking voltage is determined in part by the distance from source

to drain. High blocking voltage capability implies high resistance because of geometry, so there is a trade off between low drift region resistance and diode voltage capability.

Power MOSFET can be classified as: (i) Double Implanted or DIMOSFET (ii) UMOSFET and (iii) Lateral or LDMOSFET.

DMOS transistors are common in silicon power device technology where the p-base or body and n+ source regions are formed by diffusion of impurities through a common mask opening [28]. However, impurity diffusion is impractical in SiC because of the very low diffusion coefficients at any temperature. The Purdue group fabricated the first DMOS transistors in SiC using ion implantation to introduce dopants for the p-base and the n+ source [29-32]. The implanted DMOSFET requires that separate masks be used to define p-base and the n+ source. The construction is a vertical structure with a drift layer built on a highly conductive n+ layer. The n-drift region is designed to give the forward blocking capabilities. The forward blocking capability is achieved by the p-n junction between p-base region and n-drift region. During the device operation, a fixed potential to the p-base region is established by connecting it to the source metal by a break in the n+- source region.Upon short-circuiting the gate to the source and applying a positive bias to the drain, the p-base/n-drift region junction becomes reverse-biased and this junction supports the drain voltage by the extension of depletion layer on both sides. However due to the higher doping level of the p-base layer, the depletion layer extends into the n-drift region. By applying the positive bias to the gate electrode, the conductive path between n+-source region and the n-drift region is formed. Due to application of positive drain voltage a current flow takes place between drain and source through the n-drift region and conductive channel. The conductivity of the channel is modulated by the

gate bias voltage and the current flow is determined by the resistance of various resistive components. The total specific on-resistance or the resistance area product [33] is determined as:

$$R_{on\text{-}sp} = R_{n+} + R_C + R_A + R_J + R_D + R_S \; ; \qquad (1)$$

where $R_{on\text{-}sp}$ is the specific on resistance, R_{n+} is the contribution from the n+ -source, R_C is the channel resistance, R_A is the accumulation layer resistance, R_J is the resistance from the drift region between the p-base regions by virtue of the JFET pinchoff action, R_D is the drift region resistance and R_S is the substrate resistance. In a power MOSFET, blocking voltage appears across the drift layer and so the drift-region resistance is considered to be the minimum possible theoretical value for the on-resistance of a MOSFET. For an ideal DIMOSFET, the resistances associated with the n+-source, the n-channel, the accumulation region and the n+-substrate are usually neglected and the specific on-resistance of the power MOSFET is determined by the drift region alone. This assumption is not accurate at lower breakdown voltages where the drift region resistance R_D is comparable to the other resistive components and these resistances should be included in calculating $R_{on\text{-}sp}$. However at higher break down voltages, R_D is significantly higher than other resistances and $R_{on\text{-}sp}$ could be approximated by R_D. The drift region analysis for an ideal DIMOSFET structure can be performed by taking the depletion layer in the drift region as an abrupt one-dimensional junction fabricated in a uniformly doped semiconductor [34-36].

1.4 LITERATURE SURVEY

Silicon carbide based MOSFET can be used in high power applications and hence it requires a high breakdown voltage. The one-step field plate termination can enhance

the breakdown voltage to 910 V, embedded mesa termination can increase it to 1350 V, and the embedded mesa with step field plating can give a breakdown voltage of 1100 V [37]. However, 6H-SiC DIMOSFETs in practice have attained a maximum blocking voltage of 760 V [38]. The specific on-resistance of the drift region of the MOSFET can be significantly reduced by enhancing the inversion channel mobility using pyrogenic re-oxidation annealing [39], thereby reducing the power dissipation.

In late 1980s, it was observed that power silicon devices were approaching their theoretical limits and that these limits could be significantly extended by fabricating power devices in the materials with higher breakdown electric fields, such as silicon carbide [40]. For vertically oriented majority carrier devices, the theoretical minimum value of the resistance-area product under punch through condition is:

$$R_{on-sp} = \left(\frac{3}{2}\right)^3 \frac{V_B^2}{\mu_n \varepsilon_S E_C^3} = \frac{3.375 V_B^3}{\mu_n \varepsilon_s E_C^3} \qquad (2)$$

where Ron-sp is the specific on-resistance in Ω-cm^2, μ_n is the electron mobility perpendicular to the surface, ϵ_s is the permittivity of the semiconductor, E_c is the critical field for avalanche breakdown perpendicular to the surface and V_B is the designed blocking voltage of the drift region. Although it varies with doping, the critical field E_c in SiC is almost an order of magnitude higher than in silicon. Even allowing for the lower electron mobility, the specific resistance in SiC at a given blocking voltage is about 400 times higher than the silicon.

In 1994, silicon carbide MOS characteristics were explained in a paper by Brown et al [41]. This paper produced data which characterized the SiC/SiO_2 interface and explains one of the previously unexplained abnormalities observed in the characteristics

of SiC MOSFETs. The outstanding distinction between the MOS characteristics on p and n type SiC wafers obviously indicates that the difference is probably caused by the fact that the p type wafers are Al doped and the n type wafers are N doped. The redistribution of impurities that occurs during the thermal oxidation of SiC and Si behaves in a similar fashion. N type dopants are rejected by the oxide during growth whereas p type dopants are incorporated into the oxide**.** Hence, the Al dopant in the oxide is likely to be the causes of the p type SiO_2/SiC interface characteristics.

The first MOSFETs in SiC were reported in the late 1980s and the first power MOSFETs in 1994 [42]. The power devices were the vertical-trench MOSFETs or UMOSFETs. UMOSFETs are attractive because the base and source regions are formed epitaxially without the need for ion implantation and associated high temperature annealing. In UMOSFETs, the MOS channel is formed on the sidewalls of trenches created by RIE. However, SiC UMOSFETs were reported to have two serious problems: (i) A high electric field occurs in the gate oxide caused by higher electric fields in the SiC drift region. This problem occurs at the trench corners leading to catastrophic failure of the gate oxide at higher drain voltages, thus restricting the maximum operating voltage to less than 40% of ideal breakdown voltage, and (ii) The low inversion layer mobility along the trench sidewalls results in high specific on-resistance, which nullifies the advantage of lightly doped drift region in SiC [43-46]. By 1995, UMOSFETs fabricated on the carbon face of SiC had achieved the breakdown voltage of about 260V.

In 1995, the first reported noise characterization of 6H-SiC MOSFETs are demonstrated [47]. The noise spectra for n-channel, depletion-mode MOSFETs fabricated in 6H-SiC material were measured from 1-10^5 Hz at room temperature.

Devices were biased in the linear regime, where the noise spectra was found to be dependant upon the drain to source bias current density. At a drain to source current of 50μA for MOSFETs with a W/L of 400μm/4μm, the measured drain to source noise power spectral density was found to be A/f^{λ}, with A being $2.6x10^{-12}$ V^2, and λ being between 0.73 and 0.85, indicating a nonuniform spatial trap density skewed towards the oxide-semiconductor interface. The measured Hooge parameter (α_H) was $2x10^{-5}$.

In 1995, surface channel n-MOSFET devices in 6H-SiC are fabricated with n^+ polysilicon gates on 80 nm thick gate oxide using a self aligned process. The mobility and subthreshold slope, 40 cm^2/Vs and 500 mV/decade, are comparable to MOSFETs fabricated with a non selfaligned process. These MOSFETs exhibit a saturation drain current of $18mA/mm^2$ at 340˚C when the gate is 9V above threshold. This current density is approximately three times higher than the best self aligned 6H silicon carbide MOSFETs reported to date and approximately five times higher if scaled to the same oxide thickness [48-51].

In 1996, the presence of aluminum in thermally grown oxides on 6H-silicon carbide has been demonstrated; n-type and p-type 6H-silicon carbide wafers, along with p-type sifvflicon control wafers were oxidized in dry oxygen at 1275˚C for 45 minutes. Capacitance-voltage measurements on the SiO_2 films formed on the n-type 6H-SiC and the silicon control wafers yielded near ideal characteristics while the SiO_2 films on p-type 6H-SiC revealed high effective charge and interface state densities. Secondary ion mass spectroscopy performed on the oxides showed significant levels of aluminium and sodium in SiO_2 on both n-type and p-type 6H-SiC but not on the silicon control wafers indicating that neither element was introduced during processing. The presence of

aluminum in oxides on both types suggest that it is not solely responsible for the increased effective oxide charge and interface state densities commonly observed in oxides formed on p-type 6H-SiC [52-55].

In 1996, the advantages and limitations of 4H-SiC power UMOSFET structure were demonstrated by US Air Force (WPAFB, Dayton Ohio) and Office of Naval Research, Arlington, Virginia. According to this report, the use of p+ polysilicon gate leads to a higher breakdown voltage as the Fowler Nordheim injection from the gate electrode is reduced. It was also concluded that the insulator reliability is the limiting factor and therefore the high temperature operation of these devices may not be practical [56-58].

In 1997, Denso Corporation Japan introduced UMOSFET. This UMOSFET produced a blocking voltage of 450V [59], a specific on-resistance of 10.9 $m\Omega cm^2$, and $V_B^2/R_{on\text{-}sp}$ of 18.6 MW per cm^2. In the same year, Northrop Grumman Science and Technology Centre introduced and fabricated the 4H-SiC UMOSFETs at the blocking voltages of 1.1kV and 1.4 kV [60], as well as the 4H-SiC DIMOSFETs at a blocking voltage of 900V [61].

In 1998, Purdue University reported a SiC accumulation-channel UMOSFET with new structural features that shield the trench oxide from high electric fields in the blocking state [62-63]. The new features consisted of p-type region formed in the trench bottom by self-aligned ion implantation and a thin n-type epilayer incorporated between the n-drift region and the p-type base.

A way to avoid the problem with oxide breakdown at the trench corners is to eliminate the trenches. This was accomplished in 1996 with the introduction of planar

implanted DMOSFETs [62-63,30]. Since impurity diffusion is impractical in SiC, the base and source regions are formed by selective ion implantation using aluminum or boron for the p-type base and nitrogen for the n^+-source. Because p-type implants are conducted at temperatures between 1600 and 1700 ˚C, the self-aligned implant process using polysilicon gates is not practical in SiC. Hence, the realignment tolerances must be allowed between two sources and gate. This should also alter the alignment of the underlying base material. Due to these disadvantages, the elimination of the trench corners resulted in a threefold improvement in the device blocking voltage to 760V. This blocking voltage is achieved using 6H-SiC.

In 1998, the 4H-SiC UMOSFET was fabricated with a breakdown voltage of 1.4 kV and a specific on-resistance of 311 $m\Omega cm^2$ by the CREE Research Inc [63]. The fabricated device required the impurity concentration of the drift region of $1x10^{15}/cm^3$ and required n^- epitaxial layer thickness of 15μm. For the prototype module, three kinds of 2.0 kV UMOSFETs with different chip areas (0.7x0.7, 1.5x1.5, and 3.0x3.0 mm^2) were designed. All were fabricated in CREE Research Inc by using 4H-SiC wafers. In this report the relationship between the breakdown voltage and the specific on-resistance was presented by various groups which were involved in the fabrication of Silicon Carbide based power devices.

In 1998, the characteristics of ACCUFETs fabricated from 6H-SiC and 4H-SiC polytypes were compared. At room temperature a specific on resistance of $18m\Omega cm^2$ was measured on the best 6H-SiC device which is designed for the breakdown voltage of 1500V at a logic level gate drive voltage of only 5V which was in excellent agreement with 15 $m\Omega cm^2$ obtained in simulations. The $R_{on\text{-}sp}$ exhibited the positive temperature

coefficients. In contrast, the room temperature $R_{on\text{-}sp}$ for the best 4H-SiC reduced rapidly with increase in temperature to 128 $m\Omega cm^2$ and 450K. At room temperature, the unterminated 6H-SiC and 4H-SiC devices had a breakdown voltage of 350V and 450V, respectively, with a leakage current of <100μA. However, a breakdown voltage of 1240 V is obtainable from the epitaxial material on using an Ar implant edge termination [64].

In 1999, the usefulness of silicon carbide for the device application was explained [65]. In the same year, the theoretical and numerical analysis of SiC JFET and MOSFET at 6.5 kV was presented. According to this report, to improve the on-state/breakdown performance of the JFET, buried layers in conjunction with a highly doped buffer layer had been used. Trench technology was employed for the MOSFET. The devices were simulated and optimised using MEDICI simulator. In order to obtain a 6.5 kV breakdown voltage, the n-drift region length was 60μm long with a doping concentration of $2x10^{15}cm^{-3}$. The distance between the gate and the source diffusions was 0.6 μm. For a trench MOSFET, the p-well doping is $5x10^{17}$ cm^{-3} and its length is equal to 3.8 μm. The doping concentration of the n-drift region has to be decreased to $1.7x10^{15}$ cm^{-3}. In order to obtain the proposed breakdown voltage, the n-drift layer length was kept 60μm long. The gate oxide thickness for the simulated structure was 0.2μm [66-67].

In 1999, the viability of fabricating high voltage i.e.400V planar SiC DIMOS devices with reduced temperature (T_{max}=1400˚C) processing to minimize step bunching by using aluminum as the p-well dopant was demonstrated. At room temperature inversion layer electron mobility of 30 cm^2/Vs was obtained on aluminium implanted p-type regions. The p-well spacing was scaled to 5 μm without increasing $R_{on\text{-}sp}$ through the use of unique JFET spacer implants, in order to promote higher packing densities for

silicon carbide power devices. An R_{on-sp} of 42 mΩcm^2 has been observed on the 2 μm spacer implanted devices, which can be further reduced (35%) by decreasing the source window length in the process design [68].

In 1999, MOSFET parameters like inversion layer mobility, threshold voltage, intrinsic mobility reduction factor and interface state density extracted from the sub threshold slope were examined in detail for 6H-SiC enhancement mode n-channel MOSFETs. The inversion layer mobilities and the threshold voltage were determined as a function of substrate doping concentration as well as device temperature. The interface state density was studied for different substrate doping concentrations. The inversion layer mobility was found to decrease strongly with increasing substrate doping. Hence, fundamental dependencies of inversion layer and threshold voltage on substrate doping concentration and temperature are analogous to silicon devices. However, the experimental data verify that these dependencies are modified by an extremely high density of interface states near the conduction band edge [69].

In 2000, the characterization of SiC epitaxial channel MOSFETs was demonstrated. Silicon Carbide epitaxial channel MOSFETs were fabricated on 6H SiC substrates with n^+-epitaxial source and drain electrodes. The electrical characteristics were modelled in the sub-pinch off depletion and accumulation modes of operation. A buried channel mobility of 230 cm^2 per V-sec and an accumulation-mode surface mobility of 45 cm^2 per V-sec were extracted at room temperature under a 50% activation of channel donor impurities [70]. In 2000 again, the fast recovery of the 6H-SiC MOSFET reverse diode (Q_{rr}=30nC, t_{rr}=20ns) and fast switching as well as short circuit capability(1ms) of vertical JFETs have been demonstrated in this paper. The paper also

discussed the future of SiC switching power devices [71]. In the same year, N_2O grown oxide on both n- and p-type 6H-SiC wafers was successfully fabricated and demonstrated for the first time. Improved SiC/SiO_2 interface and oxide qualities were demonstrated in N_2O grown MOS devices, especially for p-type devices. Moreover, considerably enhanced device reliability under high field stress was observed with much smaller flat band voltage shift than N_2O nitrided and thermal oxide devices. All these gains are attributed to significant nitrogen incorporation near the SiC/SiO_2 interface duringN_2O oxidation. Hence, N_2O oxidation technique could have great potential in making high quality and high reliability SiC MOSFET's, especially n-channel ones [72].

In 2001, a 4H-SiC RF power MOSFET was fabricated and characterised for the first time [73]. The improved performance of this device was facilitated by a two-metal-layer process which optimises the conflicting requirements of the acceptable inversion-layer mobility and the low contact resistance. The cut-off frequency of the device with 1μm gate length was in excess of 7 GHz. The breakdown voltage of the newly fabricated MOSFET was found to scale with the drift length. A breakdown voltage of 950 V was achieved in MOSFETs with specific on-resistance of 24 Ωmm^2. The parasitic resistances were reasonably small due to dopant activation and post metallisation anneals. The sheet resistances of the n^+- source/drain and n-drift regions were measured to be 300 Ω per sq and 3400 Ω per sq respectively. The resistivity of the ohmic contact was $1.5x10^{-5}$ Ωcm^2. Models for the electron mobility in the three most important silicon carbide polytypes, namely, 4H, 6H, and 3C SiC were developed. A large number of experimental mobility data and Monte Carlo results reported in the literature have been evaluated and serve as the basis for the model development. The proposed models describe the dependence of

electron mobility on doping concentration, temperature and electric field. They consist of one analytical equation for each polytype and can be easily incorporated in a numerical device simulator. Hence, the presented mobility models can be used in device simulation to design and optimize RF power transistor structures and to compare the suitability of the three SiC polytypes for different RF power transistors [74].The results presented in this paper demonstrates that the effective channel mobility of lateral, inversion mode 4H-SiC MOSFETs is increased significantly after passivation of SiC/SiO_2 interface. States near the conduction band is by high temperature anneals in nitric oxide. Hi-lo capacitance-voltage (C-V) and ac conductance measurement indicate that, at 0.1 eV below the conduction band, the interface trap density decreases from approximately $2x10^{13}$ to $2x10^{12}$ eV^{-1} cm^{-2} following anneals in nitric oxide at 1175˚C for 2h. The effective channel mobility for MOSFETs fabricated with either wet or dry oxides increases by an order of magnitude to approximately 30-35 cm^2/V-sec following the passivation anneals [75]. A 2D, drift-diffusion based simulator specifically for SiC MOSFETs was developed and demonstrated in this paper. The use of new simulator was intended to extract internal details of the physical operation of SiC MOSFETs. By coordinating simulator development with experiment, a detailed SiC MOSFET mobility model, an interface state model, and an incomplete ionization model that yields agreement with experimental I-V curves were obtained. Included in this results was the extraction of an inversion layer saturation velocity that was approximately 20 times less than that of the bulk [76].

In 2002, a novel analytical model of a SiC MOSFET was presented [77]. In this paper, by using known experimental results, a semi-empirical relation for carrier mobility

(μ) dependence on electric field intensity, dopant concentration and temperature was formulated. Based on this relation, appropriate analytical mathematical-physical model for simulation of current-voltage characteristics, transconductance and conductance of MOSFET were developed. All models were formulated taking into account, among other effects, the dependence of threshold voltage on temperature and impurity concentration in the channel, as well as the effect of the channel narrowing. Using the proposed model a simulation algorithm was designed and a simulation of the MOSFET performance was performed. In 2002 again, a 10 A, 2.4 kV power DIMOSFET in 4H-SiC was reported and the characteristics of large area (3.3x3.3 mm^2), high-voltage 4H-SiC DIMOSFETs were demonstrated [78]. The MOSFETs showed a peak MOS channel mobility of 22 cm^2/V-sec and a threshold voltage of 8.5 V at room temperature. The DIMOSFETs exhibited an on-resistance of 42 $m\Omega cm^2$ at room temperature and 85 $m\Omega cm^2$ at 200 ºC. Stable avalanche characteristics at approximately 2.4 kV were observed. An on-current of 10 A was measured on a 0.103cm^2 device. High switching speed was also demonstrated. In this paper, the MOS channel length defined by the p-well and n-implants was 1.5μm. Electrons flowed laterally from the n source through a MOS channel on the implanted p-well, then flowed vertically through the JFET region formed by two adjacent p-well regions and then through the lightly doped n drift region into the drain. The cell pitch was 16 μm and the packing density of the gate periphery was 1250 cm/cm^2. A 20-μm thick drift layer with a doping concentration of 2.5x10^{15} cm^{-3} was chosen for a 2000 V blocking voltage design. This paper also suggested that the devices were capable of high-voltage, high-frequency and low-loss switching applications.

In 2003, the first observation of total dose effects of gamma-ray irradiation on enhancement mode 6H-SiC p-channel MOSFETs was presented and demonstrated. The electrical characterization of these transistors was performed before and after irradiation up to a total dose of 10^8 rad(SiO_2) by measuring the drain-source current as a function of gate voltage and drain-source voltage. These transistors were compared to 6H-SiC n-channel MOSFETs. The p-channel devices remained fully functional up to 10^6 rad (SiO_2), while the n-channel devices were fully functional through 10^8 rad(SiO_2). In this paper, it was observed that the generation of radiation-induced interface states in the n-channel transistors was substantially lower than that of the p-channel devices [79].

In 2003 and 2004, numerical device simulations on a 4H –SiC vertical MOSFET were presented [80-81]. The simulations mainly focused on reverse blocking voltage, threshold voltage and on-state resistance. The simulated gate MOSFET had a gate oxide thickness of 50nm, a source depth of 0.2 micron and a p-well depth of 1 micron. The channel length was 1micron.

In 2004, a comparison of modern SiC power devices was demonstrated. In this paper an analysis of the static and dynamic behaviour of a 2 kV SiC MOSFET and IGBT was presented. By comparing the circuit performances it was observed that IGBT is two times faster than MOSFET [82]. The reliability of SiO_2 in a SiC MOS based device is determined by tunneling current. If an intrinsic Fowler-Nordheim regime of tunneling is assumed, tunneling current is exponentially dependent on the electric field in the dielectric and barrier height to carriers. This barrier height is primarily determined by band offsets between metal/SiC and the dielectric. Since band offsets for SiC to most dielectrics are smaller than those with respect to Si, a lower reliability is expected for

SiC-dielectric based devices as compared to MOS devices for the same oxide electric field. SiC-dielectric interface states affect channel mobilities and may determine the barrier height for Fowler-Nordheim tunneling. There exists a trade-off between on-state resistance and SiC-dielectric reliability, which is influenced by the dielectric thickness in a forward biased SiC-dielectric structure. The uses of alternative dielectrics to improve trade off was suggested in this paper [83].

In 2004, compact silicon carbide power semiconductor device models for circuit simulation was developed for power Schottky, merged-PiN-Schottky, PiN diodes and MOSFETs. Different structural properties, such as a thinner and more highly doped base region, or material properties, such as carrier mobility and bandgap, result in different compact model expressions as compared to silicon technology [84].The various field plate termination techniques were investigated and compared for 4H-SiC power devices. It was demonstrated that all existing field plate terminations suffer from severe crowding problems in the oxide. When oxide breakdown and reliability concerns were taken into account, existing filed plate termination techniques yield device breakdown voltages that were generally unsatisfactory. A new termination technique utilizing dielectric mesa was proposed for SiC power devices to address the existing termination challenges associated with oxide breakdown. Dielectric reliability concerns were alleviated and a relatively high percentage of ideal breakdown voltage was achieved with the proposed termination techniques. The proposed termination techniques were relatively simple to fabricate and promised to be attractive for junction termination of SiC power devices [85]. In 2004 again, collaborative efforts for combining TCAD numerical simulation and VQM modeling provided a useful path for modeling MOS devices in the deep sub-0.1 micron

mesoscale regime. In this paper, modeling of the capacitance voltage characteristics of deep sub-0.1 micron mesoscale MOS devices was demonstrated [86].

In 2005, a design and fabrication of a 1600V 4H-SiC UMOSFET with a dual buffer layer structure was demonstrated [87]. The fabricated device exhibited 50mΩcm^2 of specific on-resistance with ~1μm of the channel length that could be further reduced to <1μm. In this paper, the n-type drift layer was ~25μm thick with 3-5x10^{15} cm^{-3} of doping concentration. Two n-type buffer layers were grown on top of the drift layer. The first buffer layer was ~3μm thick and 1-2x10^{16} cm^{-3} doped with nitrogen. The second layer was ~0.5μm thick, 0.5-1x10^{17} cm^{-3} doped with nitrogen followed by the final p-type, ~2μm thick base layer with 0.8-1x10^{17} cm^{-3} doped with aluminum. The n$^+$- layer was formed by high energy up to 700 KeV nitrogen implantations to obtain ~1μm channel length. UMOSFET trench gates were perpendicular to the primary flat of the SiC wafers to achieve high inversion channel mobility [87]. An on-state performance of trench oxide-protected SiC UMOSFETs on 115μm-thick n-type 4H-SiC epilayers designed for blocking voltages up to 14 kV was demonstrated [88]. In this paper, a current density of 137A/cm^2 and a specific on-resistance of 228 mΩcm^2 were achieved at a gate bias of 40 V. The effect of current spreading on the specific on-resistance for finite-dimension devices was investigated. A 115μm-thick, 7.5x10^{14} cm^{-3} n$^+$-type epilayer was first grown on n$^+$ -4H-SiC substrate, cut 8^o off axis and followed by a 0.4 μm, 2x10^{17} cm^{-3} n-type current spreading epilayer and a 1.5 μm, 2x10^{17} cm^{-3} p-type epilayer to form the base region of the UMOSFET. Source contacts were formed by implanting 4x10^{15} cm^{-2} nitrogen at 650 ^{o}C using a Ti-Au mask. Gate trenches approximately 2 μm deep were formed by reactive ion etching using a Ni mask. Sacrificial oxidations were performed to

smooth the trench sidewalls. The active area of the device was .018cm^2 and required a current of 2.5 A. The device required a current density of 137A per cm^2. The blocking layers of doping and the thickness used here were theoretically capable of blocking 14 kV and had actually been demonstrated to block 10 kV. However, problems with the edge terminations in the devices limited the blocking voltage to just over 5 kV [88].

In 2006, 4H-SiC DIMOSFETs with breakdown voltages of 1.2 kV and 1.8 kV were fabricated [89]. For 1.2 kV, an epilayer with a doping concentration of $6x10^{15}$ cm^{-3} and a thickness of 12 μm could be used. For 1.8 kV 4H SiC DMOSFET the device had a gate oxide of 500Å. The gate oxide electric field was limited to approximately 3 MV per cm. The active area of this device was 0.0936 cm^2. An on-resistance of 85 mΩ (R_{on-sp} = 8 mΩcm^2) and a drain current of 50 A (534 A/cm^2) at a forward drop of 5.7 V were measured at room temperature. In 2006 again, Silicon Carbide as an energy efficient wide band gap semiconductor for power devices was discussed. For RF applications, GaN HEMTs allowed the use of highly efficient Class E circuit topologies demonstrating a high power of 63 W at 2 GHz with 75% power added efficiency. SiC Schottky diodes were allowing up to a 25% reduction in losses in power supplies for computers and servers when used in the power factor correction circuit. Even higher efficiencies could be obtained when the SiC Schottkys were combined with a SiC MOSFET as the switch, resulting in yet another 22% reduction in losses. For motor control, SiC Schottky allowed a >35% reduction in losses as demonstrated for a 3 HP motor drive [90].

In 2007, a compact circuit simulator model was developed and used to describe the performance of a 2kV 4H-SiC power DIMOSFET. This model also made a comparison with the widely used 400V, 5A Si power MOSFET. The model's channel

current expressions were unique in that they include the channel regions at the corners of square and hexagonal cells that turn on at lower gate voltages and the enhanced linear region transconductance. This model also actively described the static and dynamic performance of both the Si and SiC devices. In this paper, the detailed device comparisons showed that both the on-state performance and switching performance at 25 °C were similar between the 400V Si and 2kV SiC MOSFETs with a difference that the SiC device required twice the gate drive voltage. The main difference between the devices was that SiC has a five times higher voltage rating without an increase in the specific on-resistance [91].

1.5 NEED FOR SUITABLE STRUCTURE IN SILICON CARBIDE:

Despite the superiority of SiC, device fabrication of SiC MOS devices presents unique problems many of which are not yet totally resolved. When the background of thesis was first undertaken, the issues related to the fabrication of SiC MOS-based devices could be summarized as follows:

- The dependency in quality of oxide grown on the crystal orientation of SiC epilayers.
- The resultant surface roughness in the trench surface due to the RIE technique used in the formation of the SiC Trench Structure.
- Unique problems in the activation of p-type implants and its effect on SiC n-MOSFET interface properties.
- The inversion layer mobilities obtained in 6H SiC MOSFETS were about 10-50 cm^2 per V-sec, even lower in the case of 4H-SiC MOSFETs.

In spite of these problems, the performance advantages of SiC devices have motivated a number of groups to begin development in parallel with the more fundamental work on materials and processing issues. The following points summarize the state of the art of SiC MOSFETs at the start of research:

- The UMOS structure was identified by other groups as the power MOSFET structure of choice for SiC. However, due to process-related issues pointed out above and severe enhancement in high-field stressing in the gate oxides at the bottom of the etched trench, poor inversion channel mobility and low blocking voltage capability in SiC UMOS-based devices was revealed.
- The utilization of power accumulation-mode MOSFET (ACCUFET) on SiC showed an encouraging way to overcome the problems associated with the poor inversion layer mobilities
- The DIMOS (Double Implanted Metal Oxide Semiconductor) type structures showed the promising results in terms of their blocking voltages as well as optimum values of power dissipation. However, DIMOS-based devices exhibited not only poor inversion channel mobility but also uncontrollable threshold voltages, due to unique problems in the activation of p-type implants that are part of their gate structure and its effect on interface properties.

1.6 OBJECTIVES OF RESEARCH

The main objectives of this work were as follows:

1. Study and Analysis of Double Implanted MOSFET on 6H-SiC wafer.
2. Analysis and Design of Double Implanted MOSFET with optimum power dissipation for large breakdown voltages.
3. Analysis and Design of 6H-DIMOSFET using uniform doping profile.
4. Analysis and Design of 6H-DIMOSFET with Linearly Graded Profile.
5. Analysis and Design of 6H- DIMOSFET with Gaussian Profile.
6. Analysis and Design of 6H- DIMOSFET with Complementary Error function Profile.
7. Comparison of the results of these profiles for minimum power dissipation and maximum breakdown voltage.

Mathematical calculations and graphical plots for this work was carried out using MAT LAB7.0 and MATHEMATICA 4.0.

1.7 ORGANIZATION OF RESEARCH

Chapter 1 focuses on literature survey of SiC power semiconductor devices and on material advantages of silicon carbide as a high power device along with the objectives of the thesis. This chapter also describes the various crystal structures of silicon carbide and its usefulness in making a MOSFET structure using silicon carbide.

Chapter 2 analyses the device structure of a 6H-SiC vertical double-implanted MOSFET (DIMOSFET) in order to provide a high breakdown voltage of about 10 kV and low power dissipation for a rise in device temperature of 600 ˚C. Analysis of 800 W power dissipation for stable device operation corresponding to this temperature rise shows optimum doping levels of the drift region lying between $5*10^{13}$ cm^{-3} and $5*10^{15}$ cm^{-3} for a breakdown voltage of 10 kV. In this chapter the analysis is based upon field independent mobility.

In Chapter 3, we analyzed the device structure of 6H-SiC vertical DIMOSFET. The device dimensions were decided using the sequence of plots of related device parameters ranging from the drift region doping level, the device blocking voltage, depletion region width, the specific on-resistance and the power dissipation. The basis for device design rests primarily on the device height at the breakdown voltage that extends into the drift region and has been used to estimate the thickness of the drift region. The device current has been modified to include field dependent mobility and these effects have been used to evaluate the power dissipation at various current densities. Finally, the results have been discussed by considering the variations of current density vs. forward voltage, drain current vs. forward voltage, drain current vs. drain to source voltage, drain

current vs. channel voltage, specific on-resistance vs. power dissipation at different doping levels. The estimated breakdown voltage was found to about 5kV.

Chapter 4 describes the device structure of vertical DIMOSFET with linearly graded profile in the drift region with a low doping of 10^{14} per cc near the source to higher values near the drain. The mathematical calculations of depletion region width as well effective doping concentration was done separately. The drift region defines the blocking voltage capabilities. After the calculations of depletion width and effective doping concentration, the drain voltages as well as channel voltages, specific on-resistance, breakdown voltages and power dissipations have been evaluated. The results have been analyzed by considering the variations of current density vs. forward voltage, drain current vs. forward voltage, drain current vs. drain to source voltage, drain current vs. channel voltage, specific on resistance vs. power dissipation at different concentration gradients. Finally, the current density vs. power dissipation for different profiles of uniform doping levels and linearly graded profiles and percentage reduction in power dissipation at current density of 1000 A/cm^2 have been calculated. The results of linearly graded profile have been compared with 6H-SiC DIMOSFET's having uniformly doped drift region given in Chapter 3. It was found that power dissipation in linearly graded profiles varies from a maximum of 61.4% to a minimum of 20% compared to uniformly doped drift region devices with a breakdown voltage of about 10kV.

Chapter 5 analyses the device structure of vertical DIMOSFET with Gaussian Profile. Doping profile used in semiconductor industry usually has non-linearly graded profile inside semiconductor layers. These profiles are usually a Gaussian or a Complementary Error Function distribution. The effective doping level of the former has

been evaluated with the Gaussian peak being displaced towards the drain end of the device. The overall doping level called the effective doping level (N_{eff}) has been obtained by integrating the Gaussian profile within specified ranges of the depth into the semiconductor from source to drain of the MOSFET. Theoretical formulations of depletion region width and effective doping concentration have been formulated and drain voltages as well as channel voltages, specific on-resistance, breakdown voltages and power dissipations are evaluated. The results have been analysed from the plots of power dissipation vs. current density and specific on-resistance versus drain to source voltage with different Gaussian profiles generated by the varying peak concentration. The estimated maximum breakdown voltage was found to be about 16kV.

Chapter 6 analyses the device structure of vertical DIMOSFET with Complementary Error Function profile. After the calculations of depletion width and effective doping concentration, the drain voltages, breakdown voltages and power dissipations are evaluated at different values of current density. The results have been analysed from the nature of variation of these parameters for various values of current density. The current density vs. power dissipation for different Gaussian profiles and Complementary Error Function profiles as well as percentage reduction power dissipation vs different doping concentrations at various current densities have been plotted. The results of Gaussian profile have been compared with Complementary Error Function profiles. After comparing the profiles, it has been observed that power dissipation in Gaussian Profile is less by 20 to 66% than that obtained in the Complementary Error Function profile at a current density of 1000A/cm^2 which has been taken as a standard value for this analysis with a maximum estimated breakdown voltage of 20 kV.

Chapter 7 summarizes the results of the analysis of this work and points to the fact that linearly graded drift region devices have least power dissipation. Maximum power dissipation has been observed with devices having Gaussian profiles followed by Complementary Error Function profiles and then uniformly doped drift region. In case of breakdown voltages, the Gaussian and Complementary Error Function profiles are better than uniformly doped and linearly graded profiles for 6H-SiC DIMOSFET.

CHAPTER 2

ANALYSIS AND DESIGN OF DIMOSFET WITH OPTIMUM POWER DISSIPATION

2.1 INTRODUCTION

This chapter analyses the device structure of a 6H-SiC vertical double-implanted MOSFET (DIMOSFET) in order to provide a high breakdown voltage of about 10 kV and low power dissipation for a rise in device temperature of 600 ^{o}C. Analysis of 800 W power dissipation for stable device operation corresponding to this temperature rise shows optimum doping levels of the drift region lying between $5*10^{13}$ cm^{-3} and $5*10^{15}$ cm^{-3} for a breakdown voltage of 10 kV. In this chapter the analysis is based upon field independent mobility.

2.2 STRUCTURE OF 6H-SiC DIMOSFET

DMOS transistors are common in silicon power device technology where the p-base and n+ source regions are formed by diffusion of impurities through a common mask opening. However, impurity diffusion is impractical in SiC because of the very low diffusion coefficients at any temperature. The Purdue group fabricated the first DMOS transistors in SiC using ion implantation to introduce dopants for the p-base and the n^{+} -source. The implanted DIMOSFET requires that separate masks be used to define p-base and the n^{+}-source as shown in Figure-2.1 (a) and Figure-2.1(b). The construction is a vertical structure with a drift layer built on a highly conductive n^{+}-layer [30].

A power MOSFET is a voltage driven device whose gate terminal is electrically isolated from its Silicon Carbide body by a thin layer of silicon dioxide (SiO_2). As a majority carrier semiconductor, the MOSFET operates at much higher speed than its bipolar counterpart because there is no charge-storage mechanism. A positive voltage applied to the gate of an n-type MOSFET creates an electric field in the channel region beneath the gate i.e. the electric charge on the gate causes the p-region beneath the gate to convert to an n-type region. This conversion, called the surface-inversion phenomenon, allows current to flow between the drain and source through an n-type material. The region between the source and drain can be represented as a resistor, although it does not behave linearly, as a conventional resistor would. Because of this surface inversion phenomenon, the operation of a MOSFET is entirely different from that of bipolar transistor which always retains its n-p-n characteristics.

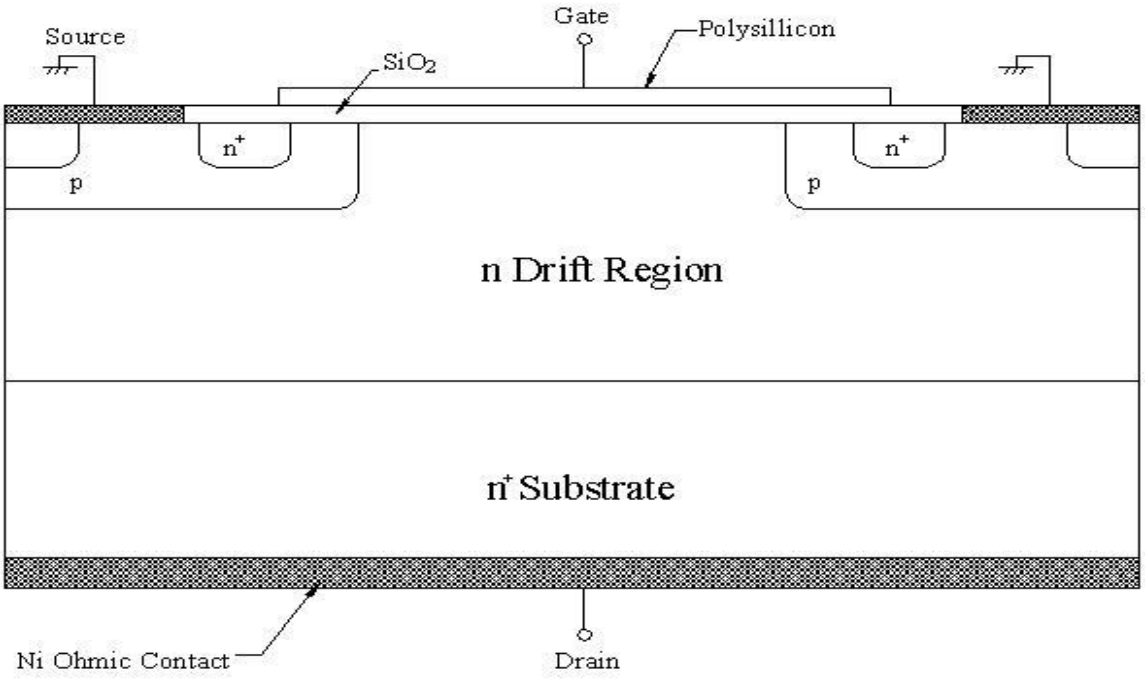

Figure- 2.1 (a)

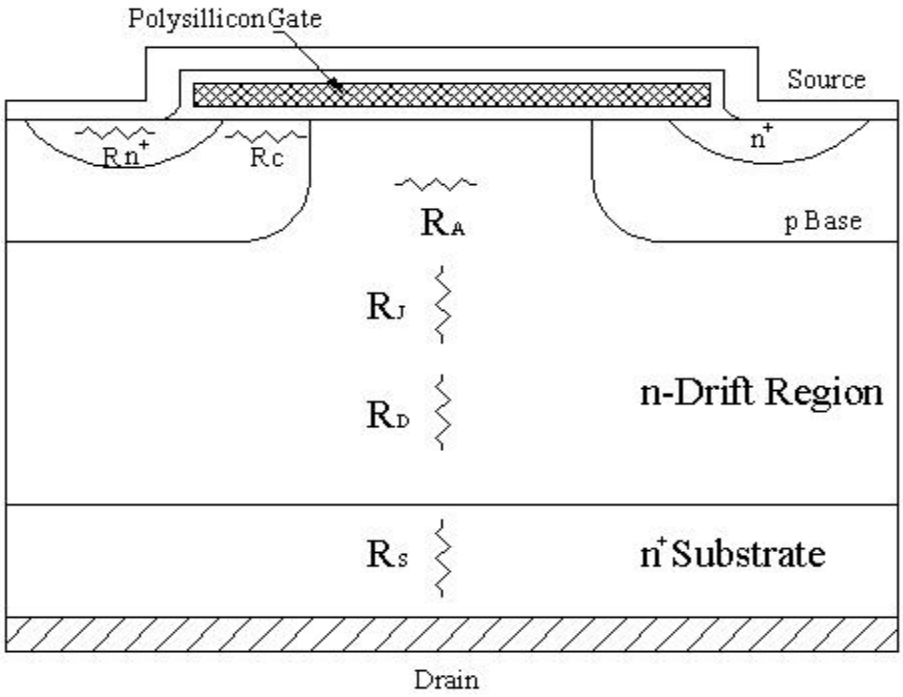

Figure-2.1 (b)

2.3 DEVICE THEORY & ANALYSIS

In order to understand the flow of current in the power DIMOSFET, it is essential to analyse the physics of the MOS device structure. It controls the characteristics of the channel region which is responsible for output characteristics of the device.

2.3.1 Forward Conduction Characteristics

The current flow in the power DIMOSFET during forward conduction is achieved by applying a positive gate bias voltage for an n-channel device to create conductive path. This flow is limited by the total resistance between the source and drain. This consists of several components as shown in Figure-2.1(b). Here, R_n+ is the contribution from n^+-sources diffusion region, R_C is the channel resistance, R_A is the accumulation

layer resistance, R_D is the drift region resistance, R_S is the substrate resistance and the portion of the drift region that comes to the upper surface between cells that contribute R_J that is enhanced at a higher drain voltage due to pinch-off action of depletion layer extending from the p-base regions due JFET action.

2.3.2 MOS Physics

When a p-type semiconductor region is assumed, then the analysis of current transport in the n-channel power MOS will be applicable. In this analysis, the oxide layer is assumed to be a perfect insulator that does not allow any charge carrier between gate and semiconductor. The energy band diagram of an ideal p-type semiconductor MOS at V=0 is shown in Figure-2.2 (a). The work function is the energy difference between the Fermi level and the vacuum level (i.e. $q\phi_m$ for the metal and $q\phi_s$ for the semiconductor) and electron affinity $q\chi$, which is the energy difference between the conduction band edge E_c and vacuum level. An ideal MOS is defined as follows [92]:

(i) At zero applied bias, the energy difference between the metal work function $q\phi_m$ and the semiconductor work function $q\phi_s$ is zero.

$$q\phi_{ms}=(q\phi_m- q\phi_s)=0 \quad (2.1)$$

(ii) The only charges that exist in the diode under any bias conditions are those in the semiconductor and those with equal and opposite sign on the metal surface adjacent to the oxide.

(iii) The resistivity of the oxide is infinite.

When an ideal MOS diode is biased with positive or negative voltages, three cases

may exist at the semiconductor surface. For the case of p-type semiconductor, when a negative voltage (V<0) is applied to the metal plate, excess positive carriers (holes) will be induced at SiO_2-Si interface. In this case, the bands near the semiconductor surface are bent upward as shown in Figure-2.2(b). The upward bending of the energy band at the semiconductor surface causes an increase in the energy E_i-E_F there, which in turn gives rise to an enhanced concentration, an accumulation of holes near the oxide-semiconductor interface. This is called accumulation case.

When a small voltage (V>0) is applied to ideal MOS diode, the energy bands bend near the semiconductor surface are bent downward and the majority carriers are depleted. This is called the depletion case as shown in Figure-2.2(c).

When a larger positive voltage is applied, the energy bands bend downward even more so that the intrinsic level E_i at the surface crosses over the Fermi level E_F. That means, the positive gate voltage starts to induce excess negative carriers at the SiO_2-SiC interface. Hence, the concentration of electrons at the interface is more than intrinsic concentration and the hole concentration as shown in Figure-2.2(d). Initially, the surface is in a weak inversion condition since the electron concentration is small. As the bands are bent further, the conduction band edge comes close to the Fermi level. The onset of the strong inversion occurs when the electron concentration near the SiO_2-SiC interface is equal to the substrate doping level.

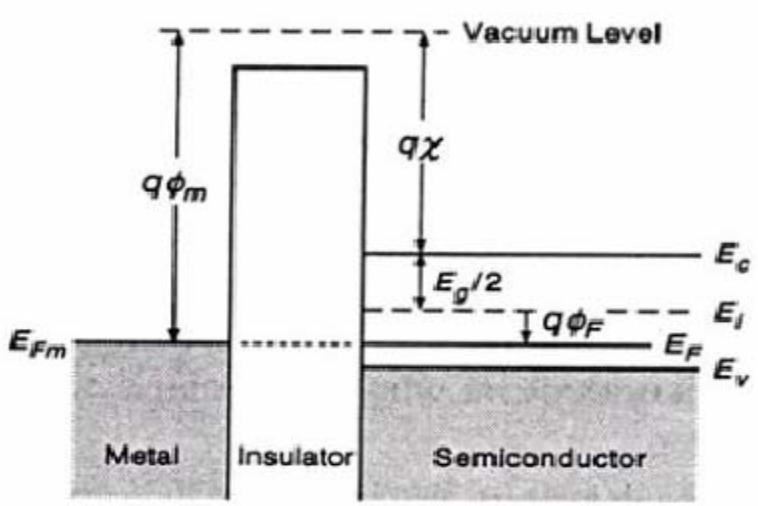

Figure-2.2 (a)

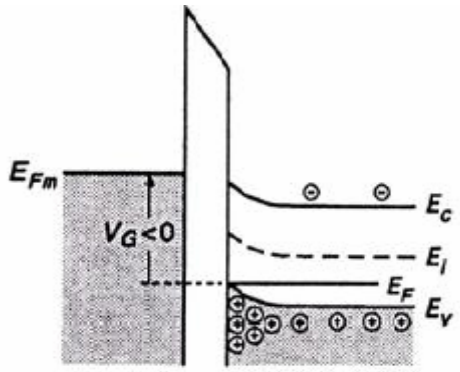

Figure-2.2 (b)

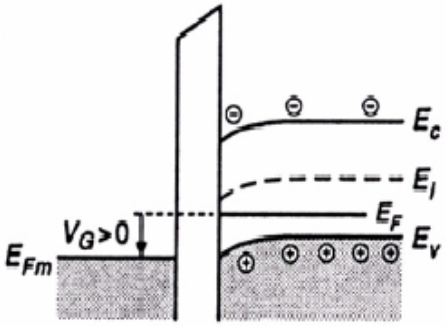

Figure-2.2(c)

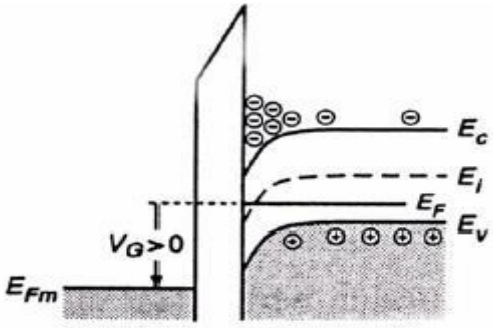

Figure-2.2(d)

Figure-2.2: Energy Band Diagrams of an Ideal MOS Diode: (a) at V=0, (b) in an accumulation mode (c) in depletion mode (d)in inversion mode

2.3.3 On-Resistance

The on-resistance of a power MOSFET is the total resistance between the source and drain terminals in the on-state [92-93] and is the important device parameter because it determines the maximum current rating. The cell structure with each component of the specific on-resistance ($R_{on\text{-}sp}$) is as shown in Figure-2.3. The application of positive gate bias results in a current flow between drain and source through the n-drift region and conductive channel. The conductivity of the channel is modulated by the gate bias voltage and the current flow is determined by the resistance of various resistive components as shown in Figure-2.3. The total specific on-resistance (Ron-sp) is determined as:

$$R_{on\text{-}sp} = R_{n+} + R_C + R_A + R_J + R_D + R_S \,, \qquad (2.2)$$

where $R_{on\text{-}sp}$ is the specific on resistance, R_{n+} is the contribution from the n^+-source, R_C is the channel resistance, R_A is the accumulation layer resistance, R_J is the resistance from the drift region between the p-base regions by virtue of the JFET pinchoff action, R_D is the drift region resistance and R_S is the substrate resistance. Additional resistances can arise from poor contact between the source-drain metal and the n^+ semiconductor regions as well as from the leads used to connect the device to the package.

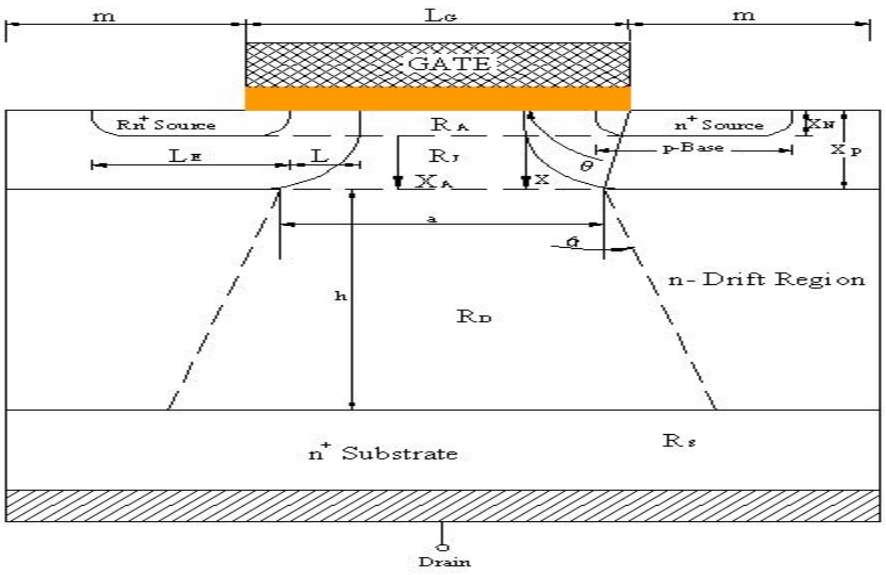

Figure-2.3: DMOSFET cell structure with each component of the on-resistance indicated

In a power DIMOS, blocking voltage is supported across the drift layer and thus, the drift region resistance is considered to be the minimum possible theoretical limit for the on-resistance of a DIMOS. For, an ideal DIMOS, the resistances associated with the n^+-source, the n-channel, the JFET, the accumulation region and the n^+-substrate are assumed to be negligible and the specific on-resistance of the power DIMOS is determined by the drift region only. This assumption is accurate at higher breakdown voltages, since R_D is significantly higher than other resistances and $R_{on\text{-}sp}$ could be approximated by R_D. However, at lower breakdown voltages where the drift region resistance R_D is comparable to the other resistive components and these resistances should also be included in calculating $R_{on\text{-}sp}$.

To analyze the contribution of n^+-source resistance, the DIMOS cell structure is as shown in Figure-2.3. In this cell, 2m is the cell diffusion window and L_G is the length of gate electrode between the adjacent cells. The cell diffusion window 2m is determined by the photolithographic design tolerances used for device fabrication. These tolerances

also determine the n^+-emitter length L_E. If the linear cell is considered with 1-cm extension perpendicular to the cross section as shown in Figure-2.3, the resistance per square centimeter due to the n^+ region is given by:

$$R_{n^+} = \frac{1}{2}\rho_{on^+} L_E (L_G + 2m) \tag{2.3}$$

where ρ_{on^+} is the sheet resistance of n^+ diffusion. In a typical device, ρ_{on^+} =10Ω.cm, L_E=10μm, and the cell repeat spacing (L_G+2m) =40μm. Hence, the resulting specific resistance of the n^+ emitter region is $2x10^{-5}\Omega\ cm^2$ which is negligible as compared to other resistances.

The channel resistance can be derived as a function of gate and drain voltages under the following assumptions:

(i) The gate structure is an ideal MOS structure

(ii) The free carrier mobility is a constant, independent of electric field strength.

(iii) The base region is uniformly doped

(iv) Current transport occurs exclusively by drift

(v) The leakage current is negligible

(vi) The longitudinal electric field along the surface is small compared with the transverse electric field resulting from gate bias.

The contribution from the channel depends on the ratio (L/Z), the gate oxide thickness and the gate drive voltage V_G. The contribution from the channel can be minimized by making the channel length L small and keeping its width Z large. The channel resistance per square centimeter for the linear cell is given by [92]:

$$R_{ch} = \frac{1}{2}\frac{L(L_G + 2m)}{\mu_n C_{ox}(V_G - V_T)} \tag{2.4}$$

where μ_n is the carrier mobility. For a typical device with channel length L of 2 μm, a gate oxide thickness of 1000A^o and a gate drive voltage of 10 V, the channel resistance per square centimeter is found to be $2.5x10^{-3}\Omega.cm^2$. Note that the channel resistance decreases when the cell repeat spacing is reduced. The channel resistance can also be reduced by decreasing the gate oxide thickness while maintaining the gate drive voltage.

The resistance of the accumulation layer R_A determines the current spreading from the channel into drift region. The accumulation layer resistance is dependant on the charge in the accumulation layer and the mobility for free carriers at the accumulated surface. For the linear cell geometry, the accumulation layer resistance per square centimeter is [92]:

$$R_A = \frac{K(L_G - 2x_p)(L_G + 2m)}{\mu_n C_{ox}(V_G - V_T)} \tag{2.5}$$

where K is a factor introduced to account for the two dimensional nature of the current flow from the accumulation layer into the bulk. For K=3, L_G=20μm and x_p=3μm, the accumulation layer resistance can be reduced by decreasing the length L_G of the gate electrode between the cells.

The resistance of drift region between the p-base diffusions can be calculated if the voltage drop along the vertical direction is neglected. Under the assumption that the depletion layer width of the p-base-n-drift layer junction is negligibly small and the current is flowing uniformly down from the accumulation layer into the JFET region. The resistance of the JFET region can be analyzed as a resistance with increasing cross section when proceeding downward from the surface. The cross section of the JFET region is given by [92]:

$$R_J = 2\rho_D(L_G + 2m)\left[\frac{1}{\sqrt{1-(2x_p/L_G)^2}}\tan^{-1}(0.414)\sqrt{\frac{L_G+2x_p}{L_G-2x_p}-\frac{\Pi}{8}}\right] \quad (2.6)$$

where ρ_D is the resistivity of the drift region.

The current spreading into the drift region is shown by the dashed lines as shown in Figure-2.3.The cross section of the drift region increases when proceeding down from the JFET region. For the current spreading at an angle α as shown in Figure-2.3, the drift region resistance per square centimeter is given by [92]:

$$R_D = \rho_D \frac{(L_G + 2m)}{\tan\alpha}\ln\left[1 + 2\frac{h}{a}\tan\alpha_1\right] \quad (2.7)$$

where the dimensions h and a are indicated in Figure-2.3. It has been found that a good approximation for α_1 is provided by:

$$\alpha_1 = 28^\circ - \left(\frac{h}{a}\right) \qquad \text{if } h \geq a \quad (2.8)$$

and

$$\alpha_1 = 28^\circ - \left(\frac{a}{h}\right) \qquad \text{if } h < a \quad (2.9)$$

2.4 CALCULATIONS OF POWER DISSIPATION

Consider the depletion region between the p-base region and the n-drift region as a one-dimensional abrupt p-n junction. It can be shown that the doping level N_B (per cm^3) that can support a given breakdown voltage V_B (V) and the depletion width W (cm) at breakdown can be given as [33]:

$$N_B = \frac{\varepsilon E_c^2}{2eV_B} \quad (2.10)$$

and $$W = \frac{2V_B}{E_C} \tag{2.11}$$

where e is the electron charge.

The specific on-resistance, $R_{on\text{-}sp}$ (Ω-cm^2) of the drift layer to support V_B is

$$R_{on-sp} = \frac{W}{eN_B\mu_n^2} \tag{2.12}$$

Substituting the values of eqs.(2.10) and (2.11) in eq.(2.12),

$$R_{on-sp} = \frac{4V_B^2}{\varepsilon E_C^3 \mu_n} \tag{2.13}$$

where ε is the permittivity (F per cm), E_C is the critical field for breakdown (V per cm) and μ_n is the electron mobility in cm^2 per V-sec.

The equation connecting the breakdown electric field strength E_C on the doping level N_B for a pn diode of 6H-SiC has been derived. Based on these results the relationship between E_C and N_B was obtained [33]:

$$E_C = 1.95x10^4 \, xN_B^{0.131} \text{ V per cm} \tag{2.14}$$

Eliminating E_C between eqs.(2.14) and (2.10),

$$N_B = \left(\frac{1.02x10^{15}}{V_B} \right)^{1.35} \tag{2.15}$$

This gives for $R_{on\text{-}sp}$ from eq. (2.12),

$$R_{on-sp} = (5.93x10^{-9})V_B^{2.5} \tag{2.16}$$

Finally the power dissipation P_D (W) for the device for a 50% duty cycle can be evaluated using the equation,

$$P_D = \frac{1}{2}(J_{on}^2 AR_{on-sp} + J_L AV_B) \tag{2.17}$$

where J_{on} is the on-state current density in the linear region of (I_{DS}-V_{DS}) characteristics of the device in A/cm^2, A is the device cross-sectional area in cm^2 and J_L is the reverse leakage current.

R_{on-sp} can be determined from the slope of I_{DS}-V_{DS} curve in the linear region. In our calculations, J_{on} is evaluated by using $J_{on}=\frac{I_{DS}}{A}$ to calculate the maximum power dissipation for a MOSFET, which is the maximum value corresponding to J_{on} for a given gate bias which is V_G =40V>> V_T. Again J_L<<J_{on} and the second term in eq.(2.15) can be neglected. Hence eq.(2.17) can be written as:

$$P_D=\frac{1}{2}(J_{on}^2 A R_{on-sp}) \tag{2.18}$$

The exact equations for I_{DS} [93] (current between drain and source), ρ_D (resistivity in drift region) and R_{on-sp} (specific on-resistance) can be given by [92]:

$$I_{DS}=\frac{Z\mu_n C_{ox}[2(V_G-V_T)-V_D^2]}{2L} \text{ and} \tag{2.19}$$

$$\rho_D=\frac{1}{\mu_n e N_B} \tag{2.20}$$

$$R_{on-sp}=\frac{\rho_D(L_G+2m)\ln(1+4\tan 26^0)10^{-4}}{\tan 26^0} \tag{2.21}$$

with

$$J_{on}=\frac{I_D}{A} \text{ A/cm}^2 \tag{2.22}$$

where A=12000x10^{-8}cm^{-2} is the cross-sectional area for half of the device of Figure-2.3 obtained by bisecting it into two parts by a vertical line.

$$V_f = R_{on-sp} \text{ x } J_{on} \tag{2.23}$$

where I_{DS} has been evaluated for V_{GS}= 40 volts, the threshold voltage V_T having been set equal to 1V as is usually the case. Z and L are the device dimensions shown in Figure 2, C_{OX} is the oxide capacitance; J_f and V_f are the forward current density and forward drop respectively. The rise in temperature of the device ΔT °K is proportional to P_D, the power dissipated:

$$\Delta T = \theta_{th} P_D \tag{2.24}$$

where θ_{th} is the thermal resistance associated with the device in ˚K per W, its value depending on the state of the art device packaging technology. With today's technology θ_{th} is about 1˚K/W [33]

$$\Delta T = P_D \tag{2.25}$$

For all calculations we have used an average value of μ_n of 530 cm^2/ V sec has been used.

2.5 CALCULATIONS AND RELATED GRAPHS

In calculating the current I_{DS} and power dissipation P_D, the following parameters with the value quoted against each one of them has been used: L_G=20μm, m=10 μm, Z= 10μm, L=3 μm, A=12000x$10^{-8}$$cm^2$, C_{ox}= ε_s/0.1, V_G=40V, V_D=2V, V_T=1V, μ_n=530 cm^2 per V-sec, h=30 μm, and a=15 μm. The set of the calculations were made on the basis of eqs. (2.10) to (2.25). By using these equations the following results have been obtained and are quoted in Tables 2.1-2.5. The related graphs are plotted in Figure-2.4-2.7.

Table 2.1: Values of drift region doping levels (N_B) for different values of the breakdown voltage (V_B)

Breakdown voltage V_B(kV)	Doping Level N_B/cc
1	$1.87*10^{16}$
2	$7.30*10^{15}$
3	$4.22*10^{15}$
4	$2.86*10^{15}$
5	$2.11*10^{15}$
6	$1.65*10^{15}$
7	$1.34*10^{15}$
8	$1.12*10^{15}$
9	$9.52*10^{14}$
10	$8.25*10^{14}$
11	$7.25*10^{14}$
12	$6.45*10^{14}$
13	$5.78*10^{14}$
14	$5.23*10^{14}$
15	$4.76*10^{14}$
16	$4.36*10^{14}$
17	$4.02*10^{14}$
18	$3.72*10^{14}$
19	$3.46*10^{14}$
20	$3.23*10^{14}$

Table 2.2: **Values of critical electric field (E_c) at different drift region doping levels (N_B) for different values of breakdown voltages (V_B).**

Breakdown voltage(kV)	**$N_B=10^{13}$/cc**	**$N_B=10^{14}$/cc**	**$N_B=5*10^{14}$/cc**	**$N_B=10^{15}$/cc**	**$N_B=5*10^{15}$/cc**
	E_C(V/cm)	**E_C(V/cm)**	**E_C(V/cm)**	**E_C(V/cm)**	**E_C(V/cm)**
1	$6.1*10^4$	$19.3*10^4$	$43.2*10^4$	$61.1*10^4$	$136.6*10^4$
2	$8.6*10^4$	$27.3*10^4$	$61.1*10^4$	$86.4*10^4$	$193.1*10^4$
3	$10.6*10^4$	$33.4*10^4$	$74.8*10^4$	$105.8*10^4$	$236.5*10^4$
4	$12.2*10^4$	$38.6*10^4$	$86.4*10^4$	$102.1*10^4$	$273.1*10^4$
5	$13.7*10^4$	$23.2*10^4$	$96.6*10^4$	$136.6*10^4$	$305.4*10^4$
6	$15.0*10^4$	$27.3*10^4$	$195.8*10^4$	$149.6*10^4$	$334.5*10^4$
7	$16.2*10^4$	$51.1*10^4$	$114.3*10^4$	$161.6*10^4$	$361.2*10^4$
8	$17.3*10^4$	$54.6*10^4$	$122.1*10^4$	$172.7*10^4$	$386.3*10^4$
9	$18.3*10^4$	$57.9*10^4$	$129.6*10^4$	$183.2*10^4$	$409.7*10^4$
10	$19.3*10^4$	$61.1*10^4$	$136.6*10^4$	$193.1*10^4$	$431.9*10^4$
11	$20.3*10^4$	$64.0*10^4$	$143.2*10^4$	$202.6*10^4$	$452.9*10^4$
12	$21.2*10^4$	$66.9*10^4$	$149.6*10^4$	$211.6*10^4$	$473.1*10^4$
13	$22.0*10^4$	$69.6*10^4$	$155.7*10^4$	$220.2*10^4$	$492.4*10^4$
14	$22.8*10^4$	$72.2*10^4$	$161.6*10^4$	$228.5*10^4$	$511.0*10^4$
15	$23.6*10^4$	$74.8*10^4$	$167.3*10^4$	$236.5*10^4$	$528.9*10^4$
16	$24.4*10^4$	$75.2*10^4$	$172.7*10^4$	$244.3*10^4$	$546.3*10^4$
17	$25.2*10^4$	$71.6*10^4$	$178.1*10^4$	$251.8*10^4$	$563.1*10^4$
18	$25.9*10^4$	$81.9*10^4$	$183.2*10^4$	$259.9*10^4$	$579.4*10^4$
19	$26.6*10^4$	$84.2*10^4$	$188.2*10^4$	$266.2*10^4$	$595.3*10^4$
20	$27.3*10^4$	$86.3*10^4$	$193.1*10^4$	$273.1*10^4$	$610.9*10^4$

Table-2.3: Values of the specific on-resistance (R_{on-sp}) at different values of the break down voltages (V_B) for the different vales of drift region doping levels (N_B).

Doping N_B/cc	V_B =1kV	V_B =5kV	V_B =10kV	V_B =15kV	V_B =20kV
	R_{on-sp} (Ωcm^2)	R_{on-sp} (Ωcm^2)	R_{on-sp} (Ωcm^2)	R_{on-sp} (Ωcm^2)	R_{on-sp} (Ωcm^2)
$1*10^{13}$	74.35	158.65	221.55	269.85	310.65
$5*10^{13}$	7.33	14.85	20.51	24.82	28.47
$1*10^{14}$	2.77	5.44	7.44	8.97	10.26
$5*10^{14}$	0.315	0.555	0.745	0.0875	0.985
$1*10^{15}$	0.1325	0.2225	0.2725	0.3225	0.3725
$5*10^{15}$	0.0185	0.0262	0.0315	0.0365	0.0395
$1*10^{16}$	0.00835	0.01105	0.01305	0.01455	0.01585

Table-2.4: Values of the specific on-resistance (R_{on-sp}) at different drift region doping levels (N_B) for different values of breakdown voltages (V_B).

Break down voltage V_B (kV)	N_B $=10^{13}$/cc	N_B $=5*10^{13}$/cc	N_B $=10^{14}$/cc	N_B $=5*10^{14}$/cc	N_B $=10^{15}$/cc	N_B $=5*10^{15}$/cc	N_B $=10^{16}$/cc
	R_{on-sp} (Ωcm^2)	R_{on-sp} (Ωcm^2)	R_{on-sp} (Ωcm^2)	R_{on-sp} (Ωcm^2)	R_{on-sp} (Ωcm^2)	R_{on-sp} (Ωcm^2)	R_{on-sp} (Ωcm^2)
1	74.35	7.33	2.775	0.315	0.1325	0.0185	0.00835
2	102.55	9.85	3.675	0.395	0.1625	0.0215	0.00925
3	124.15	11.75	4.355	0.455	0.1825	0.0235	0.00995
4	152.38	13.45	4.935	0.505	0.2025	0.0247	0.01055
5	158.65	14.85	5.445	0.555	0.2225	0.0262	0.01105
6	172.95	16.16	5.905	0.595	0.2325	0.0275	0.01155
7	186.35	17.35	6.325	0.645	0.2425	0.0285	0.01195
8	198.85	18.46	6.715	0.675	0.2525	0.0295	0.01235
9	210.45	19.50	7.085	0.705	0.2625	0.0305	0.01265
10	221.55	20.51	7.435	0.745	0.2725	0.0315	0.01305
11	232.11	21.43	7.765	0.765	0.2825	0.0325	0.01335
12	242.15	22.33	8.085	0.795	0.2925	0.0335	0.01365
13	252.55	23.19	8.395	0.815	0.3125	0.0345	0.01405
14	260.85	24.03	8.685	0.835	0.3125	0.0355	0.01425
15	269.85	24.82	8.965	0.875	0.3225	0.0365	0.01455
16	278.35	25.59	9.235	0.895	0.3325	0.0365	0.01485
17	286.85	26.34	9.505	0.915	0.3425	0.0375	0.01515
18	294.95	27.07	9.765	0.945	0.3525	0.0385	0.01535
19	302.85	27.78	10.005	0.965	0.3625	0.0395	0.01565
20	310.65	28.47	10.255	0.985	0.3725	0.0395	0.01585

TABLE 2.5: Values power dissipation (P_D) for different drift region doping levels (N_B) for different values of breakdown voltages (V_B)

Break down voltage V_B (kV)	N_B =10^{13}/cc	N_B =5*10^{13}/cc	N_B =10^{14}/cc	N_B =5*10^{14}/cc	N_B =10^{15}/cc	N_B =5*10^{15}/cc	N_B =10^{16}/cc
	P_D(Watts)	P_D(Watts)	P_D(Watts)	P_D(Watts)	P_D(Watts)	P_D(Watts)	P_D(Watts)
1	834.39	82.26	31.13	3.535	1.49	0.21	0.09
2	1150.85	110.54	41.24	4.433	1.82	0.24	0.10
3	1393.27	131.86	48.87	5.106	2.05	0.26	0.11
4	1597.86	150.72	55.38	5.667	2.27	0.28	0.12
5	1780.45	166.65	61.11	6.228	2.50	0.29	0.12
6	1940.93	181.36	66.27	6.677	2.61	0.31	0.13
7	2091.31	194.71	70.98	7.239	2.72	0.32	0.13
8	2231.59	207.17	75.36	7.575	2.83	0.33	0.14
9	2361.78	218.84	79.51	7.912	2.95	0.34	0.14
10	2486.34	230.17	83.44	8.361	3.06	0.35	0.15
11	2604.85	240.50	87.14	8.585	3.17	0.36	0.15
12	2717.53	250.60	90.73	8.922	3.28	0.38	0.15
13	2823.02	260.25	94.21	9.146	3.51	0.39	0.16
14	2927.39	269.61	97.47	9.371	3.51	0.40	0.16
15	3028.39	278.54	100.61	9.820	3.62	0.41	0.16
16	3123.78	287.18	103.64	10.044	3.73	0.41	0.17
17	3219.17	295.60	106.67	10.269	3.84	0.42	0.17
18	3310.08	303.79	109.59	10.605	3.96	0.43	0.17
19	3398.73	311.76	112.28	10.830	4.07	0.44	0.18
20	3486.27	319.50	115.09	11.054	4.18	0.44	0.18

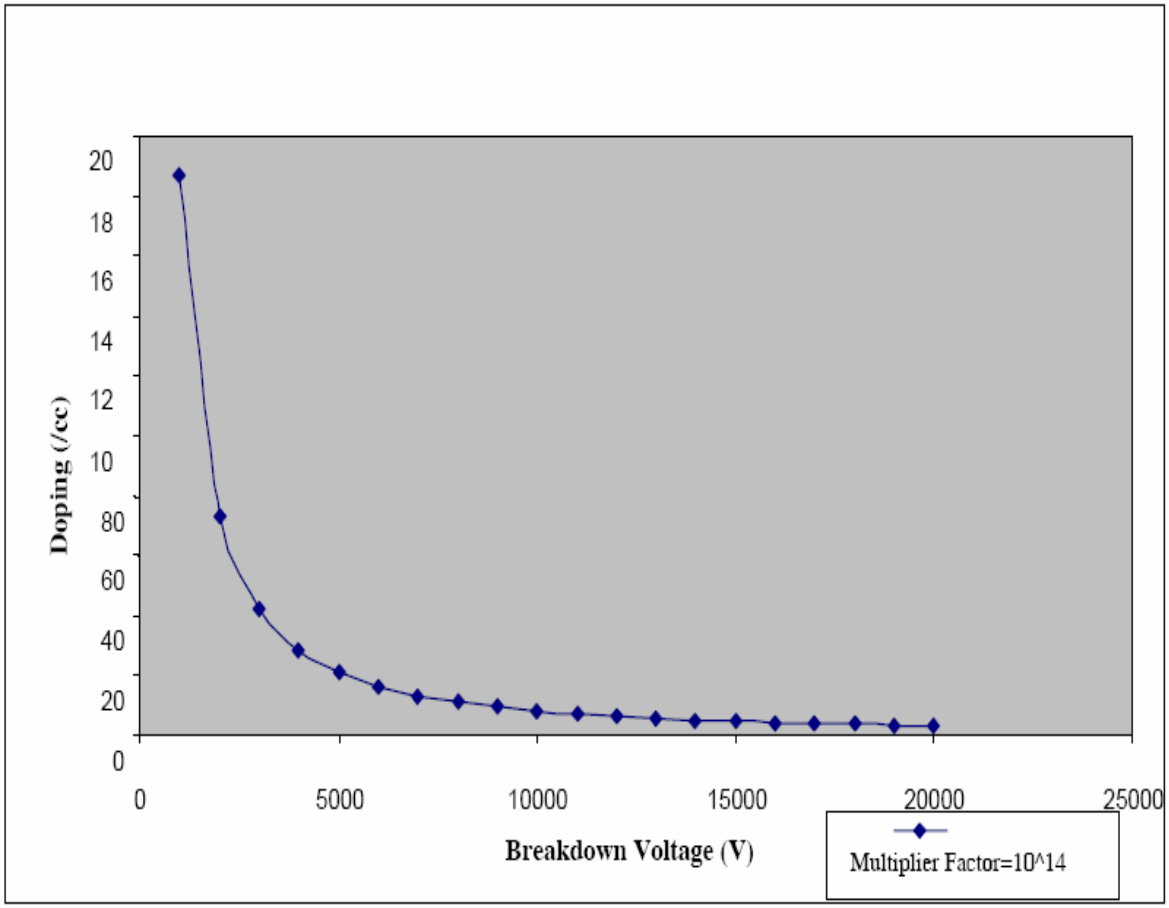

Figure 2.4: Plot of Drift region doping level (N_B) vs. Breakdown Voltage (V_B) for a 6H-SiC DIMOSFET

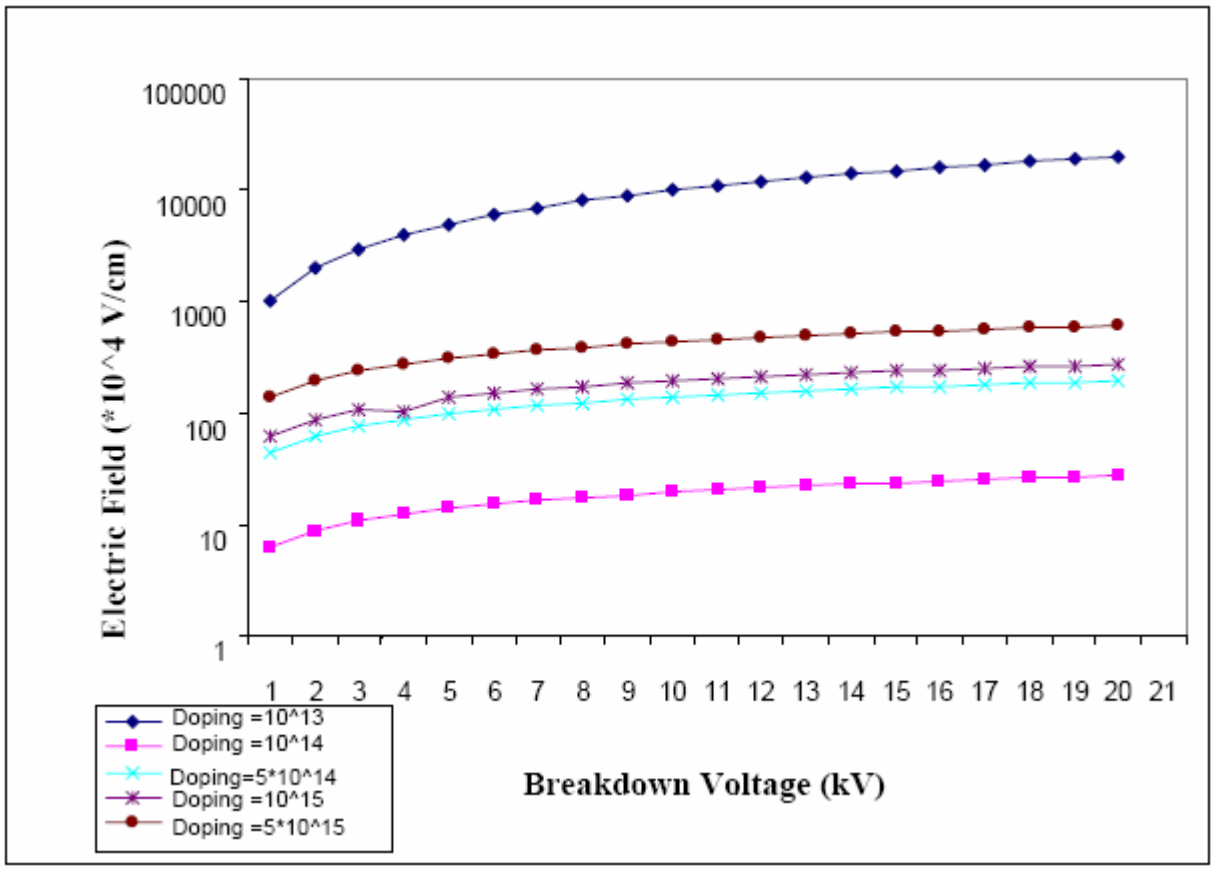

Figure 2.5: Plot of Electric Field (E_c) vs. Breakdown Voltage (V_B) for a 6H-SiC DIMOSFET for various values of drift region doping levels (N_B)

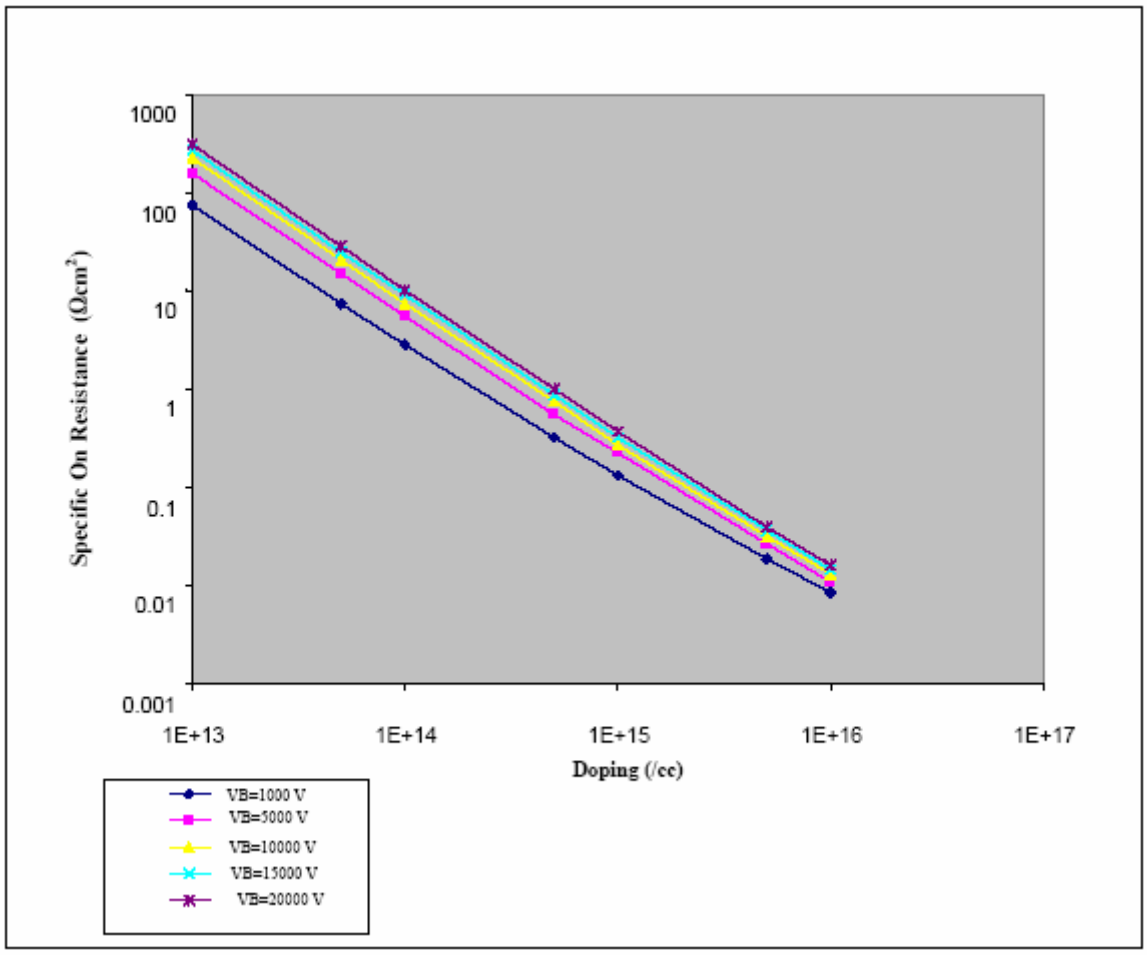

Figure 2.6: Plot of specific on-resistance (R_{on-sp}) vs. Drift region doping level (N_B) for a 6H-SiC DIMOSFET at different values of breakdown voltages (V_B)

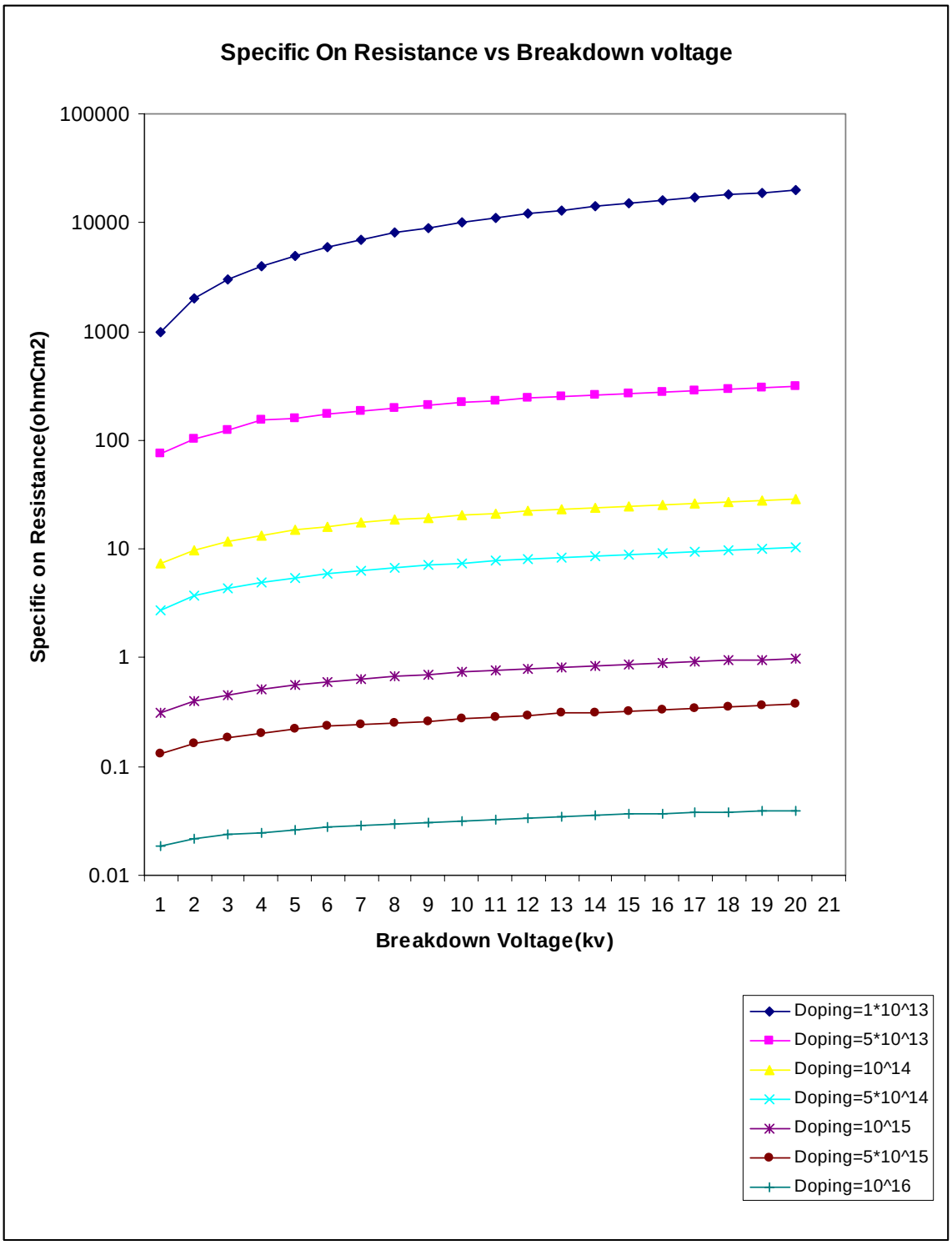

Figure 2.7: Plot of specific on-resistance (R_{on-sp}) vs. breakdown voltage (V_B) for a 6H-SiC DIMOSFET at different drift region doping level (N_B)

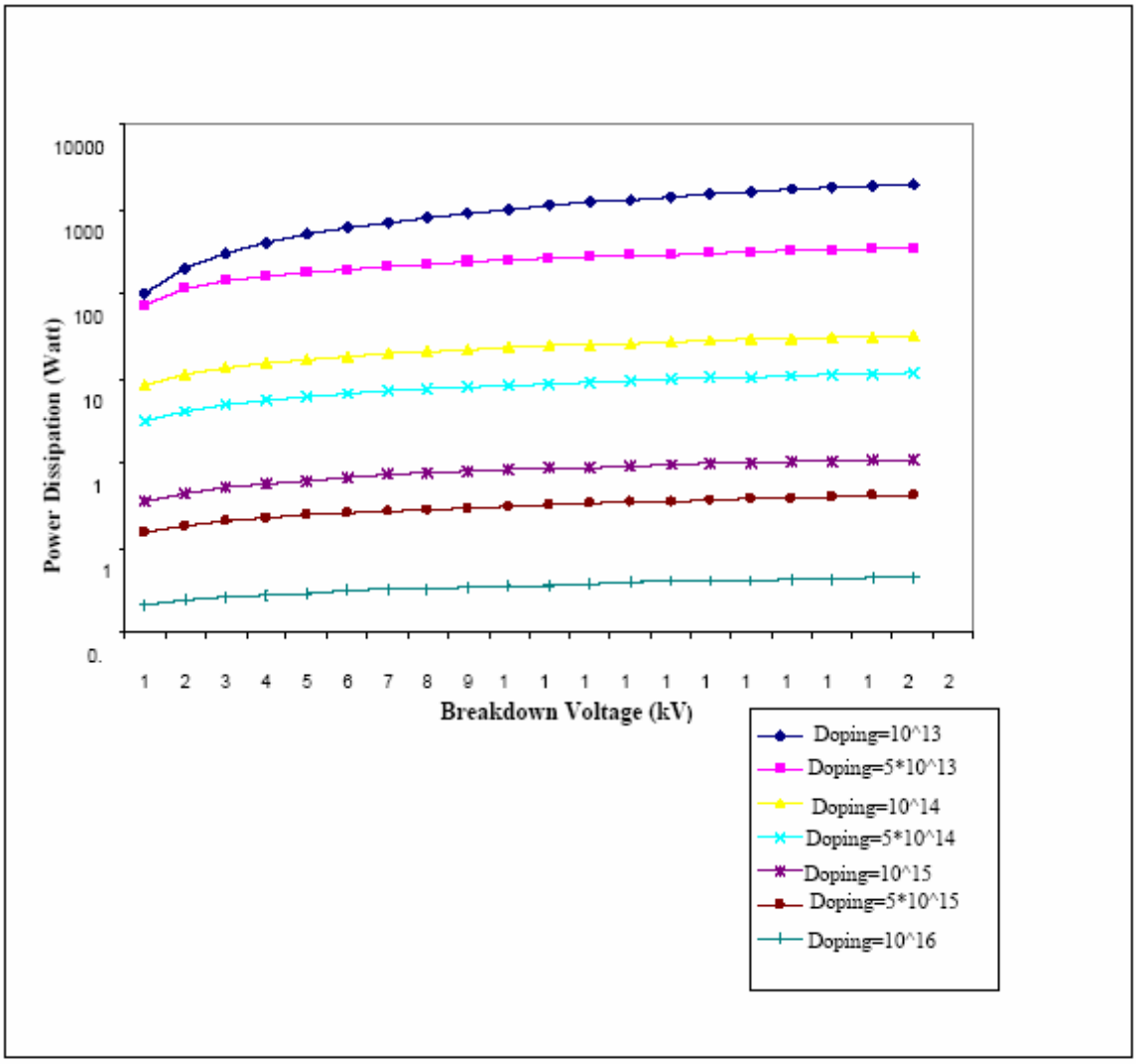

Figure 2.8: Plot of specific on-resistance (R_{on-sp}) vs. Breakdown Voltage for a 6H-SiC DIMOSFET at different drift region doping level (N_B)

2.6 RESULTS AND DISCUSSION

Having set the device dimension given above, it can be seen from Figure-2.4 which shows that high breakdown voltage ≅ 10 kV can be attained by using the low doping level of the order of 10^{15} per cm^3 or less. However very low doping levels can

give rise to a large parasitic drop across the drift region. Hence there is need to reduce this parasitic loss. We begin with the design rule that a maximum value of the temperature rise ΔTmax of 600°C≅800 K for power dissipation is permissible with the latest packaging technology. This gives ΔTmax = P_{Dmax}=800 W from eq.(2.25). From Figure-2.8, it is seen that at $V_B \geq 10$ kV, P_{Dmax} of 400 W can be attained with a doping level of $5*10^{13}cm^{-3}$. Making allowance for an increase in the R_{on-sp} to twice its room temperature [33] value over this range of the temperature rise for SiC power MOSFET, the safe margin would be to set $N_B = 5*10^{13}/cm^3$. At V_B = 10 kV and $N_B = 5*10^{13}/cm^3$, the R_{on-sp} = 205 Ω-cm^2 (see Figure2.7). Hence doubling of R_{on-sp} at $N_B = 5*10^{13}/cm^3$ with rise in temperature could lead to doubling the level of permissible power dissipation to 800 W. This value of R_{on-sp} can be checked from Figure 5, which gives a plot of R_{on-sp} vs. N_B for different values of V_B. Finally for V_B = 10 kV, $N_B = 5*10^{13}/ cm^3$, the critical field for breakdown, i.e. E_c can be obtained from Figure 2.5 giving $E_c \cong 4.3*10^5$V/cm. Thus, apart from the device dimensions quoted above, it is recommended that a doping level of $5*10^{13}/ cm^3$ for an n-drift layer of 30μm thickness can be used for the safe operation of a 6H-SiC power MOSFET with a breakdown voltage of 10 kV and a maximum rise in the device temperature of 600°C. However, in order to reduce parasitic loading effect of R_{on-sp} of the drift region, it is recommended that values of N_B should be 10^{15} per cm^3. Hence, the limit of N_B for a safe operation of 6H-SiC power MOSFET for 800W power dissipation shown in Figure 2.7 can be obtained by setting any value of N_B between $5*10^{13}/cm^3$ and $10^{15}/cm^3$ for V_B =10 kV with E_c lying between $4.3*10^5$ V/cm and $4.3*10^6$ V/cm respectively.

2.7 SUMMARY

The results of this chapter are based primarily on the variation of specific on-resistance with temperature and its effect on the power dissipation using the concept of field independent mobility which helps to estimate the optimum doping levels of the drift region. The 6H-SiC power DIMOSFET designed in the chapter has a low specific on-resistance, a high breakdown voltage of 10 kV, not-too-high electric field of Ec $\cong 10^6$V/cm, and a low power dissipation much less than a maximum limit of 800W. In this analysis, an average value of carrier mobility of 530 cm^2 per V-sec has been used. However, for still more accurate work it is advisable to use the field dependent mobility given by the equation: $\mu=\mu_0/ [1+ (\mu_0 E/ v_{sat})^{\beta}]^{1/\beta}$ where μ_0 = low field doping dependant mobility of 530 cm^2 per V-sec at $N_B = 10^{14}/cm^3$ with an electric field of about 1000 V/cm and β is a constant, its value lying between1 and 2. However, experimental verification of such a device designed along the lines given in the paper remains to be done.

CHAPTER 3

ANALYSIS AND DESIGN OF 6H-DIMOSFET USING UNIFORM DOPING PROFILE

3.1 INTRODUCTION

This chapter analyzes the device structure of 6H-SiC vertical DIMOSFET using uniformly doped profiles. The device dimensions were decided using the sequence of plots of related device parameters ranging from the drift region doping level, the device blocking voltage, depletion region width, the specific on-resistance and the power dissipation. The basis for device design rests primarily on the device width at the breakdown voltage that extends into the drift region and has been used to estimate the thickness of the drift region. The device current has been modified to include field dependent mobility and these effects have been used to evaluate the power dissipation at various current densities. Finally, the results have been discussed by considering the variations of current density vs forward voltage, drain current vs forward voltage, drain current vs drain to source voltage, drain current vs channel voltage, specific on resistance vs power dissipation at different doping levels. The estimated breakdown voltage was found to about 5kV.

3.2 VERTICAL DIMOSFET USING UNIFORM DOPING PROFILE

There are large numbers of material and electronic properties which make SiC a promising material for high power devices, such as wide bandgap (~ 3eV), high breakdown field of 3MV/cm and good thermal conductivity (3W per cm K). Some of the

prominent devices are the inversion and accumulation mode DIMOSFET's [94-95] and accumulation mode UMOS [96-97] have already being successfully developed and tested. For vertically oriented majority carrier devices, the specific- on-resistance, $R_{on\text{-}sp}$ has been shown to have a theoretical minimum value, under punch through conditions, given by [35]:

$$R_{on-sp} = \left(\frac{3}{2}\right)^3 \frac{V_B^2}{\mu_n \varepsilon_S E_C^3} = \frac{3.375 V_B^3}{\mu_n \varepsilon_s E_C^3} \tag{3.1}$$

where $R_{on\text{-}sp}$ is the resistance-area product expressed in $\Omega\text{-cm}^2$, μ_n is the electron mobility perpendicular to the surface, ε_s is the permittivity of the semiconductor, E_c is the critical field for avalanche breakdown normal to the surface and V_B is the breakdown or blocking voltage of the drift region. The critical field E_c in SiC is almost an order of magnitude higher than in Silicon. Hence, even if the electron mobility in SiC is lower than in silicon, the high value of E_c gives a substantially a lower value of specific on resistance, typically 400 times less. These parameters and their variations have been extensively analyzed by Cooper et al [38].

The most notable among the DIMOSFET's are those that have been made on 6H-SiC wafer and are the accumulation channel DIMOSFET developed at the University of North Carolina in 1997[98]. This increased the effective channel mobility and reduced the magnitude of $R_{on\text{-}sp}$ to 18 $m\Omega\text{-cm}^2$. The other parameters that affect the inversion channel mobility is the density of interface states (D_{it}) on p-type SiC since all n-channel devices are made on top of it. It was found that the density of interface states rises exponentially towards the conduction band edge in upper half of the band gap reaching levels of 10^{13} $eV^{-1}cm^{-2}$. However, post oxidation annealing in nitric oxide (NO) can significantly reduce (D_{it}) yielding higher inversion layer mobilities [99-102]. Further

reduction in R_{on-sp} has been made with the development of ACCUFET which has drastically increased the channel mobility from very low values [103] to 120 cm^2 per volt-sec [64]. This brought down the value of R_{on-sp} to 18mΩ-cm^2. Further improvements in channel mobility in 6H-SiC MOSFETs has also been made using a buried channel with mobilities going upto 180 cm^2 per volt-sec [104].

The ultimate aim in reducing the magnitude of R_{on-sp} of vertical DIMOSFET is to reduce its power dissipation, P_D or its power loss which is given by $P_D \sim J_{on}^2 R_{on-sp} A$, where J_{on} is the on-state current density and A is the device cross sectional area. The reduction of power dissipation suggested in this chapter has been made on the basis of using a uniform doping profile in the epitaxial layer of the DIMOSFET.

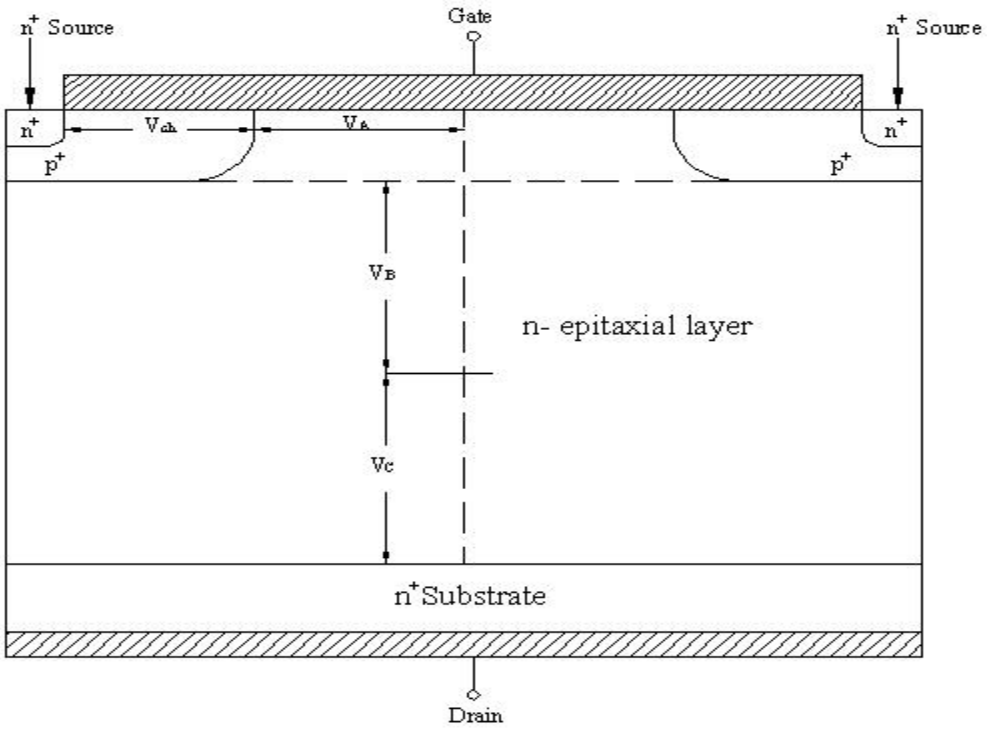

Figure-3.1

3.3 THEORETICAL ANALYSIS

The basic structure of the DIMOSFET as shown in Figure-3.1 is redrawn labeled with the device dimensions using suitable symbols and is shown in Figure-3.2.

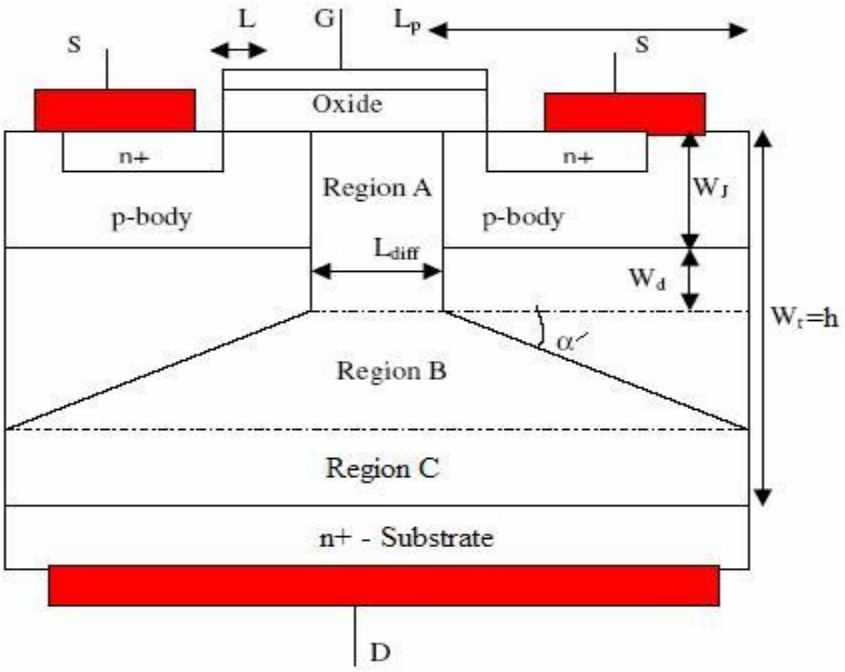

Figure-3.2

The power dissipation, P_D for a 50% duty cycle of these two devices for various current levels can then be calculated using the basic equations:

$$P_D = \frac{1}{2}\left(J_{on}^2 AR_{on-sp} + J_L V_B A\right) \tag{3.2}$$

where, J_{on} is the on state current density, J_L is the reverse leakage current density of the p-body/n-drift region junction located in region B(Figure-3.1), V_B is the breakdown voltage of the DIMOSFET and A is the device area. Since J_L is negligible in SiC diode [33], eq(3.2) can be simplified:

$$P_D = \frac{1}{2}\left(J_{on}^2 AR_{on-sp}\right) \tag{3.3}$$

Writing J_f as the forward current density considered to be same as J_{on}, eq(3.3) gives,

$$P_D = \frac{1}{2}\left(J_f^2 AR_{on-sp}\right) \tag{3.3}$$

The channel current I_{ch} which equals the drain current I_{DS} in on-state can be expressed by [80]

$$I_{DS} = I_{ch} = \frac{W\mu_n}{2L[1+(\mu_n / 2v_{sat}L)V_{ch}]} V_{ch}[2C_{ox}(V_{GS} - V_T) - (C_{ox} + C_{do})V_{ch}], \tag{3.4}$$

where W is the device width, L is the channel length, μ_n is the effective zero field doping dependent carrier mobility corresponding to doping level N_B of the drift region obtained from[33], V_{ch} is the voltage across the channel region, v_{sat} is the saturated drift velocity of the carrier taken to be $2x10^7$ cm per sec, C_{ox} is the oxide capacitance per unit area, V_{GS} is the gate source voltage, C_{do} is the body depletion capacitance considered to be much less than C_{ox} and can be neglected.

The voltage drops across regions A, B and C have been derived [80] and found to be of the form:

$$V_A = \frac{I_{DS}(W_j + W_d)}{W(L_{diff} eN_B)\mu_n - I_{DS}/E_c} \tag{3.5}$$

$$V_B = \frac{I_{DS}}{WeN_B\mu_n \cot\alpha} \log\left[\frac{WeN_B\mu_n(L_{diff} + L_p) - I_{DS}/E_c}{WeN_B\mu_n L_{diff} - I_{DS}/E_c}\right] \tag{3.6}$$

$$V_C = \frac{I_{DS}\left(W_t - W_j - W_d - L_p \tan\alpha\right)}{WeN_B\mu_n(L_s + 2L_p) - I_{DS}/E_c} \tag{3.7}$$

Where the symbols are the same as those shown in Figure-3.2 and L_{diff} is the separation of p-bodies. Here W_t=h, the device height which has been set by using the maximum depletion region width i.e. the punch through width for a given breakdown voltage, W_j is the p-body thickness and W_d is the depletion region width under on-state condition, the

drain to source voltage V_{DS} obtained by adding V_{ch}, V_A, V_B and V_C. The drift region voltage drop $V_{drift}=V_A+V_B+V_C$ and $V_{DS}=V_{drift}+V_{ch}$. The device height, h has been set by setting the depletion region width at punch through breakdown voltage equal to that at the avalanche breakdown voltage. The quantity 'E_c' in equations (3.5) to (3.7) is the critical field for avalanche breakdown.

For uniformly doped drift region, the critical field is given by [33]

$E_c=1.95x10^4xN_B^{0.131}$ volts per cm (3.8)

where N_B is the drift region doping level.

The values of V_{ch} can be evaluated by using equation (3.4). For this equation, the value of C_{do} is much less than C_{ox} and can be neglected. The value of V_{GS}=40V and V_T=1V, the equation (3.4) now becomes

$$I_{ch}=\frac{W\mu_n C_{ox} V_{ch}[78-V_{ch}]}{2L[1+(\mu_n/2v_{sat}L)V_{ch}]} \tag{3.9}$$

After solving eq. (3.9), we get

$$I_{ch}=\frac{W\mu_n C_{ox} V_{ch}[78-V_{ch}]}{2v_{sat}L+\mu_n V_{ch}} \tag{3.10}$$

Eq.(3.10) can be written as

$$W\mu_n v_{sat} C_{ox} V_{ch}^2+(\mu_n I_{ch}-78W\mu_n v_{sat} C_{ox})V_{ch}+2v_{sat}LI_{ch}=0 \tag{3.11}$$

Eq.(3.11) is quadratic, the value of V_{ch} can be evaluated to give :

$$V_{ch}=\frac{-(\mu_n I_{ch}-78W\mu_n v_{sat} C_{ox})\pm\sqrt{(\mu_n I_{ch}-78W\mu_n v_{sat} C_{ox})^2-8LWI_{ch}\mu_n v_{sat}^2 C_{ox}}}{2W\mu_n v_{sat} C_{ox}} \tag{3.12}$$

Lastly, the specific on-resistance of the DIMOSFET can be expressed using Figure-3.2as [80]:

$$R_{on-sp} = RA = \rho l = \frac{\left(W_t - W_j - W_d - L_p \tan\alpha'\right)}{\mu_n e N_B} \tag{3.13}$$

where α' is the angle of the slope of the drift region narrowing and μ_n has been obtained from [33] corresponding to the effective concentration of N_{eff} of the uniformly doped drift region. Thus N_B and μ_{neff} give the overall average value of doping level and carrier mobility in the drift region respectively. A fixed value of device current $I_{DS}=I_{ch}$ is used and W_d is obtained by iteration from eq. (3.5). Finally R_{on-sp} can be calculated. The magnitude of power dissipation P_D can be calculated by knowing R_{on-sp}, J_{on} and the device cross sectional area A for different doping levels. The value of V_B and V_C are then calculated using eqs.(3.6) and (3.7). The magnitude of V_{ch} is obtained knowing a preset value of $I_{DS,}$ the value V_{DS} is obtained form: $V_{DS} = V_{drift}+V_{ch}= V_{ch} + (V_A+V_B+V_C)$, where V_{drift} is the voltage drop across the drift region. Finally, the forward voltage drop can be calculated using the equation $V_f=J_{on}\cdot R_{on-sp}$.

3.3.1 The Critical Field, E_c and the Breakdown Voltage Calculations

The critical field E_c for avalanche breakdown for uniformly doped drift region can be calculated using eq(3.8). The depletion region width at breakdown can be estimated by first estimating the depletion region width for punch through breakdown voltage, V_{BPT} and is obtained using the equation

$$W = \sqrt{\frac{2\varepsilon_s (V_{BPT} + V_{bi})}{eN_B}} \approx W = \sqrt{\frac{2\varepsilon_s V_{BPT}}{eN_B}} \tag{3.14}$$

where V_{bi} is the built in potential for uniformly doped case as $V_{bi} \ll V_{BPT}$. For the case of a uniformly doped drift region, the breakdown voltage for avalanche breakdown V_{BAV} is obtained by knowing the depletion width W from eq. (3.14) and using the equation

$$V_{BAV} = \frac{1}{2} E_C W \qquad (3.15)$$

3.3.2 Calculations & Related Graphs

The device dimensions of 6H-DIMOSFET have been set so that the height $h \approx W_t$ equals the depletion region width, W_d under a reverse bias of 5kV applied on the p-body/n-epitaxial layer junction. In other words the DIMOSFET was designed for a maximum blocking voltage of 5kV. The dimensions of other variables as shown in Figure-3.2 have been taken to be: W_j=1μm, L_p=25μm, $\alpha^{/}=64^0$,

where $\alpha^{/}$ is the angle of slope of drift region narrowing and a smaller value of $\alpha^{/}$ corresponds to be wider spread of the current from the accumulation region A has been used here. The quantity W_j has been taken to be 1μm as implant depth in 6H-SiC is of this order [105].

The device cross-sectional area was taken with width x length as $300x80\mu m^2$ $=24000x10^{-8}$ cm^2. The device has been split into two by a vertical line bisecting the device of Figure-3.1, giving a single unit of calculations with a cross sectional area $A=12000x10^{-8}$ cm^2.

The calculations for the case of uniform doping of drift region involved the drift region doping level of $N=10^{15}$, μ_n=530 cm^2 per volt sec obtained from [33] and $h=W_t$=.0073 cm for a punch-through breakdown voltage of 5kV. The magnitude of the forward current density in the on-state, J_F which is also represented by J_{on}, the on-state current density had been set at 1, 10, 100 and 1000 amps per cm^2. The corresponding values of the device current was obtained by knowing the values of V_{ch}, for a given channel current $I_{ch}=I_{DS}$, the drain to source current was obtained by solving eq.(3.4). The magnitude of W_d, the depletion width was obtained by iteration from eq.(3.5) for V_A. The

voltage V_B was calculated knowing I_{ch} and V_C was calculated knowing W_d obtained from eq.(3.5). The sum total of all these voltages gave V_{DS}, the drain to source voltage.

The specific on-resistance of the device $R_{on\text{-}sp}$ was calculated using all the parameters in eq.(3.13), which were now known. The forward drop over DIMOSFET, V_f was then calculated using the equation, $V_f=J_F.R_{on\text{-}sp}$.

The power dissipation, P_D of the device was calculated from a knowledge of $R_{on\text{-}sp}$ and the current density, J_F. This was repeated for all values of J_F from 1 to 1000 amps per cm^2. Same set of calculations had been performed for uniformly doped drift region with doping levels of 10^{16}, 10^{17} and 10^{18} per cc. The results are shown in Table 3.1 to 3.4. A plot of power dissipation versus current density is shown in Figure-3.3 for the various doping levels of drift region. The variation of the specific on resistance of the device for the various values of V_{DS} is shown in Figure-3.4.The variations of current density vs forward voltage, drain current vs forward voltage, drain current vs drain to source voltage, drain current vs channel voltage, specific on resistance vs power dissipation at different doping levels are shown in Figs. 3.5-3.9.

Table-3.1: Results of currents, voltages, $R_{on\text{-}sp}$ and power dissipation for $N_B = 10^{15}$ per cc, μ_n=530cm^2/V-sec, A=12000x10^{-8} cm^2, h=.0073 cm

J_F (A/cm^2)	I (A)	V_{ch} (V)	V_A (V)	V_B (V)	V_C (V)	$V_{DS}=V_A+V_B+V_C+V_{ch}$ (V)	W_d (cm)	$R_{on\text{-}sp}$ (Ω-cm^2)	V_f (V)	P_D (W)
1	12e-5	.0028	.0020	.041	.018	.064	2.61e-5	.0359	.0359	2.16e-6
10	12e-4	.028	.029	.41	.176	.643	8.3e-5	.0331	.331	2.11e-4
100	12e-3	.283	.571	4.10	1.659	6.616	2.67e-4	.0292	2.92	.0199
1000	12e-2	3.16	14.85	41.24	13.25	72.49	8.82e-4	.024	24.20	1.552

Table-3.2: Results of currents, voltages, R_{on-sp} and power dissipation for $N_B = 10^{16}$ per cc, $\mu_n = 500 cm^2/V\text{-}sec$, $A = 12000 \times 10^{-8} cm^2$, h=.0073 cm

J_F (A/cm^2)	I (A)	V_{ch} (V)	V_A (V)	V_B (V)	V_C (V)	$V_{DS}=V_A+V_B+V_C+V_{ch}$ (V)	W_d (cm)	R_{on-sp} (Ω-cm^2)	V_f (V)	P_D (W)
1	12e-5	.003	1.72e-4	.0044	.0019	.0094	3.18e-6	.0039	.0039	2.3e-7
10	12e-4	.029	.0018	.0435	.0192	.094	1e-5	.0037	.037	2.3e-5
100	12e-3	.3	.0220	.435	.190	.947	3.19e-5	.0034	.3424	.0023
1000	12e-2	3.37	.339	4.35	1.86	9.92	1.03e-4	.0031	3.116	.2229

Table-3.3: Results of currents, voltages, R_{on-sp} and power dissipation for $N_B = 10^{17}$ per cc, $\mu_n = 300 cm^2/V\text{-}sec$, $A = 12000 \times 10^{-8} cm^2$, h=.0073 cm

J_F (A/cm^2)	I (A)	V_{ch} (V)	V_A (V)	V_B (V)	V_C (V)	$V_{DS}=V_A+V_B+V_C+V_{ch}$ (V)	W_d (cm)	R_{on-sp} (Ω-cm^2)	V_f (V)	P_D (W)
1	12e-5	.0050	2.8e-5	.00072	.00032	.0061	8.07e-7	.0008	.0008	3.84e-8
10	12e-4	.050	2.85e-4	.0072	.0032	.061	2.55e-6	.0006	.0063	3.84e-6
100	12e-3	.50	.0030	.072	.032	.607	8.08e-6	.0003	.0343	3.83e-4
1000	12e-2	5.82	.0353	.725	.318	6.897	2.72e-5	.0002	.2158	.0381

Table-3.4: Results of currents, voltages, R_{on-sp} and power dissipation for $N_B = 10^{18}$ per cc, $\mu_n = 140 cm^2/V\text{-}sec$, $A = 12000 \times 10^{-8} cm^2$, h=.0073 cm

J_F (A/cm^2)	I (A)	V_{ch} (V)	V_A (V)	V_B (V)	V_C (V)	$V_{DS}=V_A+V_B+V_C+V_{ch}$ (V)	W_d (cm)	R_{on-sp} (Ω-cm^2)	V_f (V)	P_D (W)
1	12e-5	.011	5.97e-6	1.55e-4	6.86e-5	.0112	3.47e-7	1.12e-4	1.12e-4	8.23e-9
10	12e-4	.11	6.02e-5	.0016	6.86e-4	.1123	1.1e-6	9.43e-5	9.43e-4	8.23e-7
100	12e-3	1.08	6.15e-4	.0155	6.85e-3	1.103	3.44e-6	8.14e-5	8.14e-3	8.23e-5
1000	12e-2	14.28	.0067	.1552	.0684	14.51	1.24e-5	6.86e-5	6.85e-2	.0088

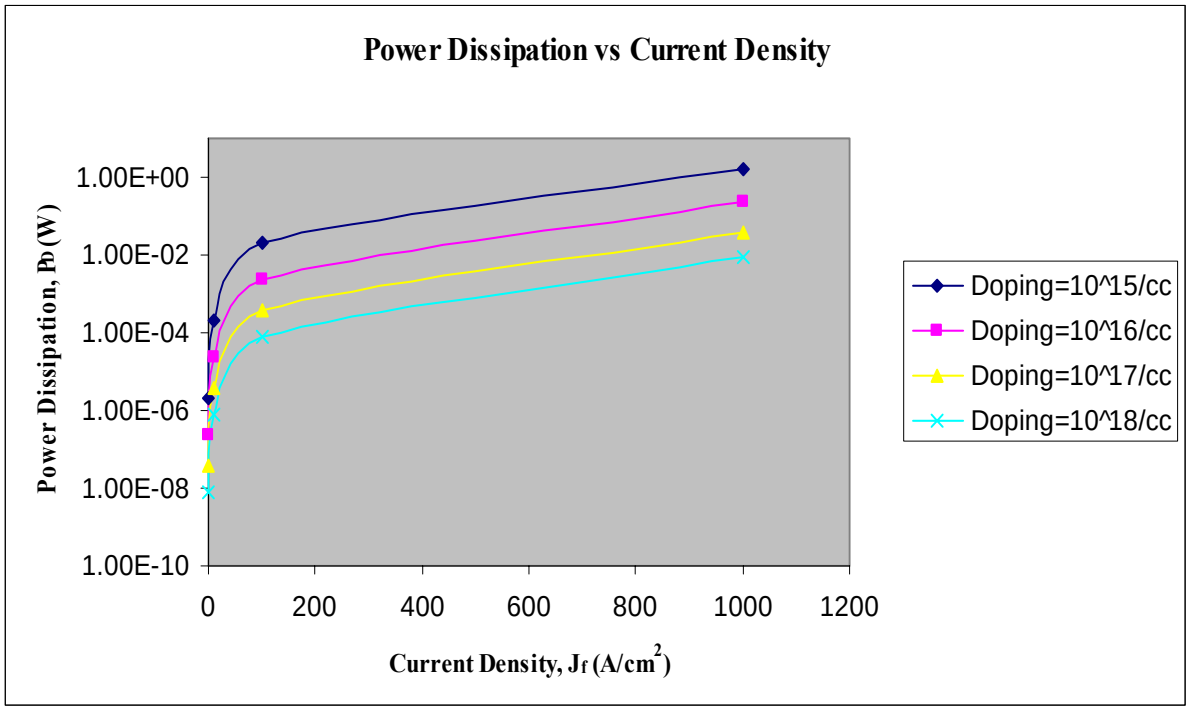

Figure-3.3: Plot of Power Dissipation vs Current Density for a 6H-SiC DIMOSFET for various values of drift region doping levels (N_B) for uniform profile

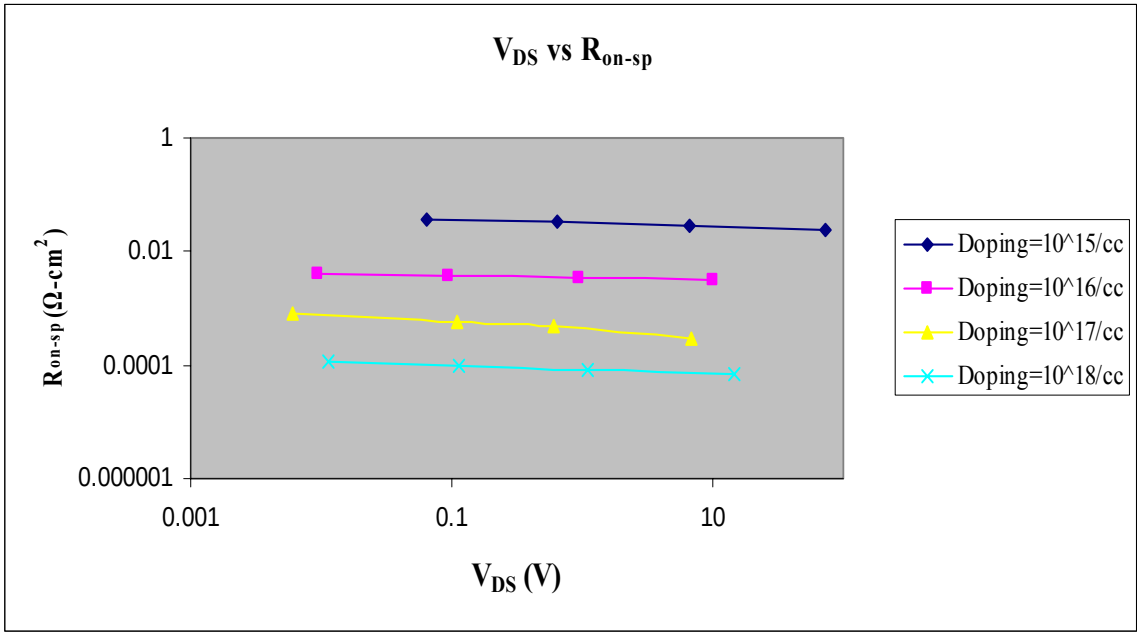

Figure-3.4: Plot of V_{DS} vs. R_{on-sp} for a 6H-SiC DIMOSFET for various values of drift region doping levels (N_B) for uniform profile

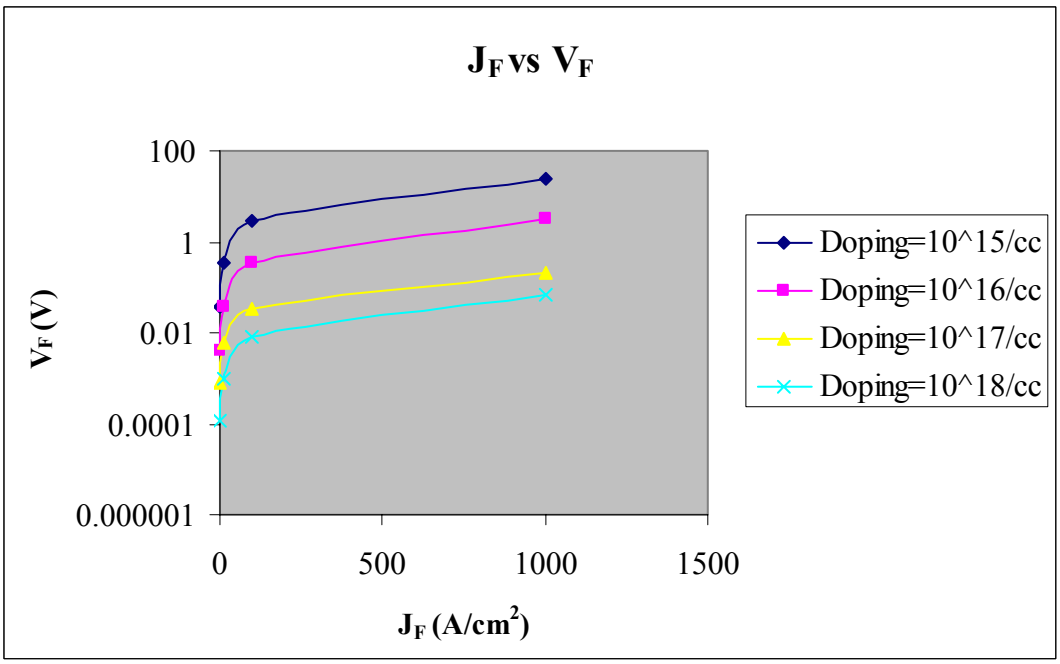

Figure-3.5: Plot of Forward Current Density vs. Forward Voltage Drop for a 6H-SiC DIMOSFET for various values of drift region doping levels (N_B) for uniform profile

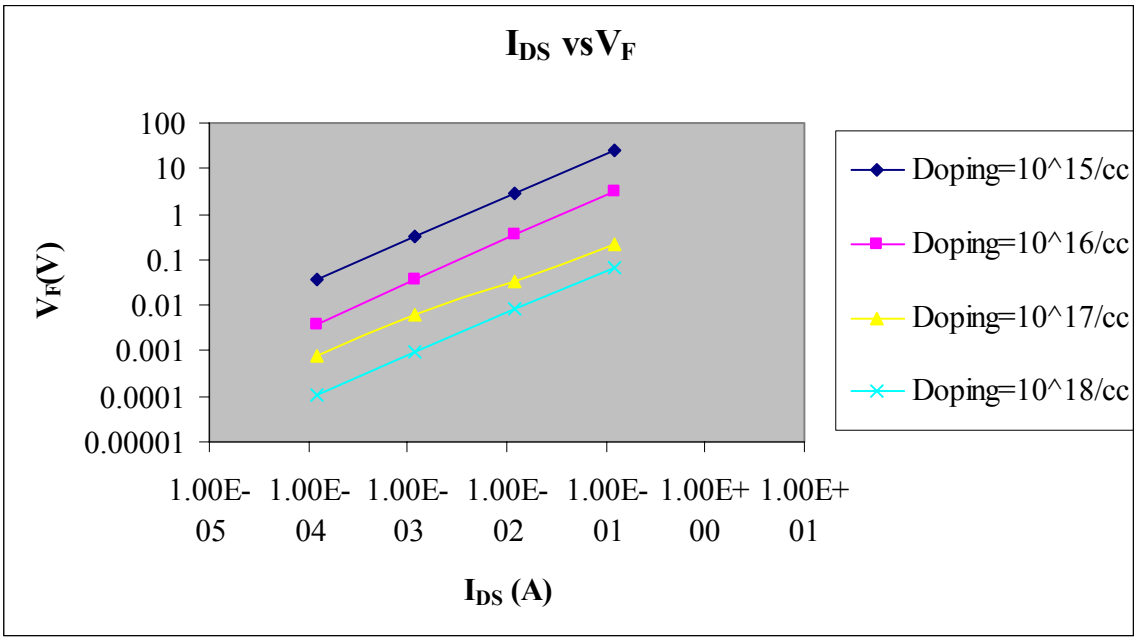

Figure-3.6: Plot of Drain Current vs. Forward Voltage Drop for a 6H-SiC DIMOSFET for various values of drift region doping levels (N_B) for uniform profile

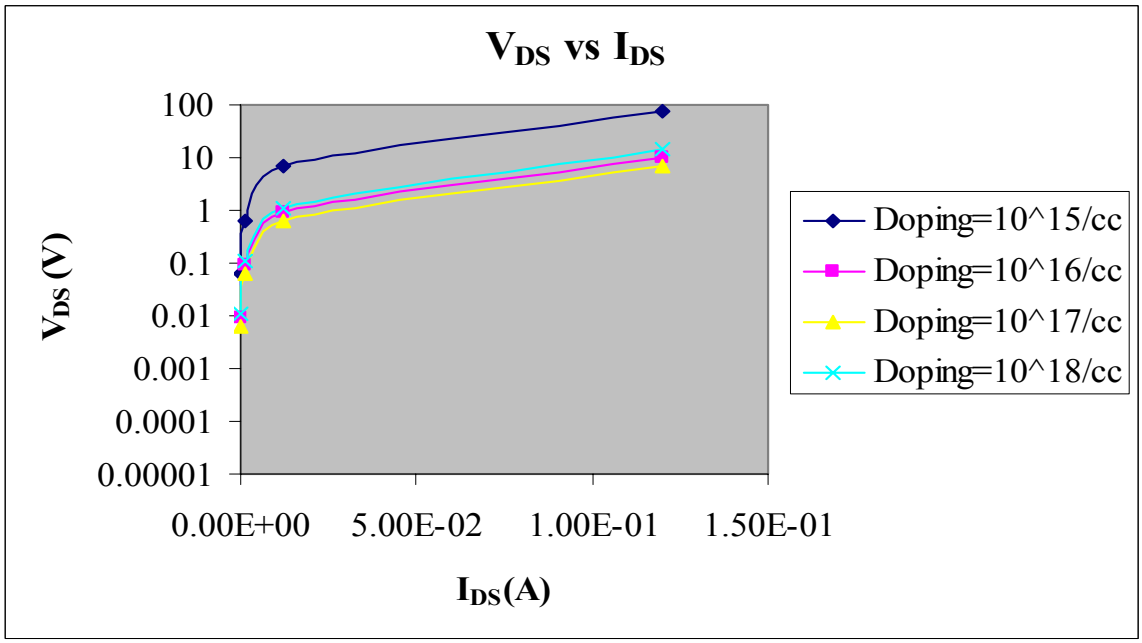

Figure-3.7: Plot of Drain Current vs. Drain to Source Voltage for a 6H-SiC DIMOSFET for various values of drift region doping levels (N_B) for uniform profile

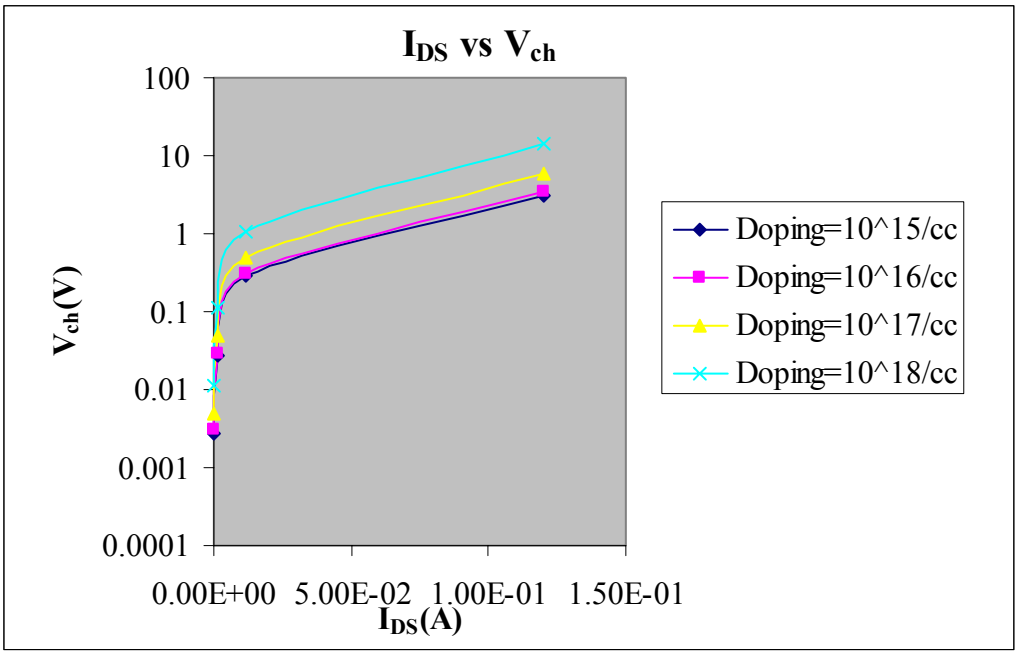

Figure-3.8: Plot of Drain Current vs. Channel Voltage for a 6H-SiC DIMOSFET for various values of drift region doping levels (N_B) for uniform profile

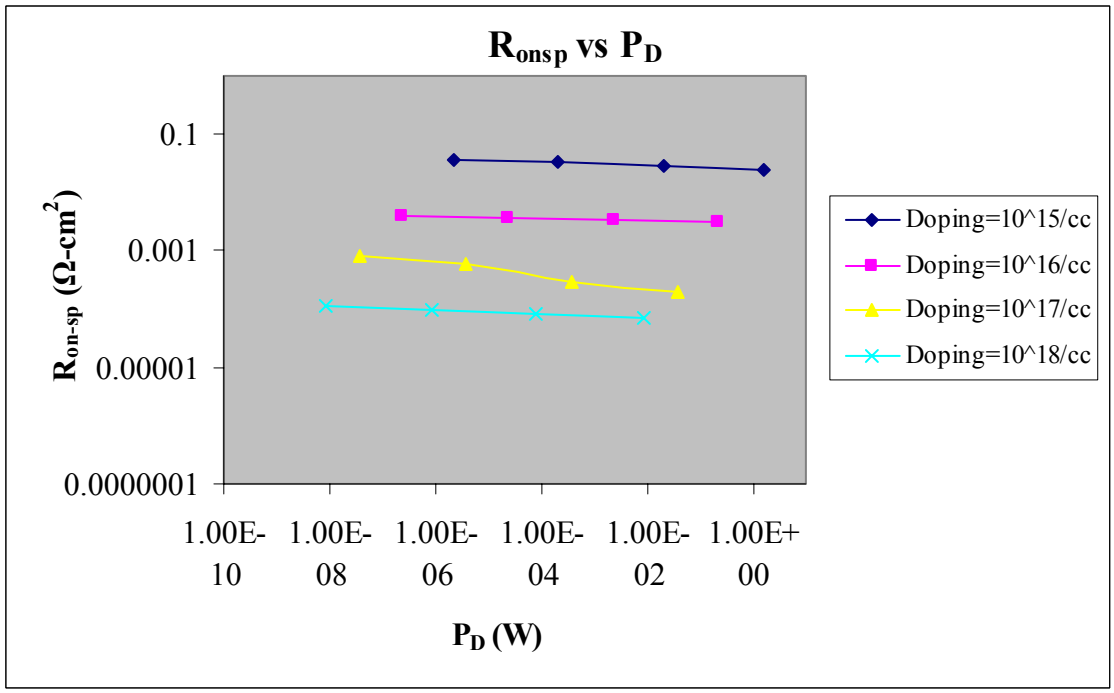

Figure-3.9: Plot of Power Dissipation vs. Specific-on-resistance for a 6H-SiC DIMOSFET for various of values of drift region doping levels (N_B) for uniform profile

3.4 CALCULATION OF BREAKDOWN VOLTAGES (V_{BPT} & V_{BAV})

The breakdown voltage considered here are the punch-through breakdown voltage, V_{BPT} and the avalanche breakdown voltage, V_{BAV}. For a given voltage, device design requires that the two voltages be made equal to each other. In this work, the lower breakdown voltage has been considered for use as the device breakdown voltage.

For the uniformly doped region of the DIMOSFET, the punch through breakdown voltage V_{BPT} has been set at 5kV for a doping level of 10^{15} per cc, giving the depletion region width of 73μm where use has been made of equation (3.14). For given value of doping, the critical field was calculated from eq. (3.8) and the avalanche breakdown voltage, V_{BAV} had been obtained using eq. (3.15). This was repeated from other values of doping level. The results are shown in Table 3.5.

Table-3.5: Results of calculation of breakdown voltages, V_{BAV} and V_{BPT} for different values of doping level (N_B) for 6H DIMOSFET with uniformly doped drift region

N_B /cc	W(μm)	E_c(V/cm)	$V_{BAV}=(.5)(E_cW)$	V_{BPT}
10^{15}	73	$1.78x10^6$	6.4kV	5kV
10^{16}	10	$2.43x10^6$	1.21kV	1kV
10^{17}	1.8	$3.29x10^6$	296V	300V
10^{18}	.243	$4.44x10^6$	55V	54.3V

3.5 SUMMARY

An analysis of calculated data of uniformly doped drift regions of the 6H-DIMOSFET presented in Tables 3.1 to3.4 showed that increasing current levels for a given drift region doping level caused an increase in the magnitudes of V_{ch}, V_A, V_B, V_C

and consequently V_{DS}. An increase in V_{DS} caused an increase in magnitude of the depletion region width, W_d, the forward drop, V_f and the power dissipation, P_D. However, the magnitude of R_{on-sp} decreased with an increase in the value of W_d and could be verified from eq.(3.13). This is shown in Figure-3.3 which shows the non-linear increase in power dissipation, P_D with forward current density, J_f. The variation of R_{on-sp} with V_{DS} is shown in Figure-3.4. As the doping level of the drift region was increased, the drop over the channel, V_{ch} increased but all other values including V_{DS}, V_f, W_d, R_{on-sp} and P_D are found to decrease. The decrease in power dissipation, P_D at higher doping levels of the drift region was primarily due to a decrease in the magnitude of R_{on-sp}. At a current density, J_f of 1000 A/cm^2, the power dissipation, P_D was estimated to fall by about 1.552 to .0088 W as the drift region doping levels changes from 10^{15} per cc to 10^{18} per cc. However, high doping levels limited the value of breakdown voltage, V_B and so an optimum value of drift region doping level would have to be selected which could give a low value of P_D and a high value of V_B.

Estimation of breakdown voltages, i.e. punch through (V_{BPT}) and avalanche (V_{BAV}) breakdown voltage could be made on the basis of the calculated data presented in Table 5.4 for uniformly doped drift region devices. The results in Table 5.5 are for a given drift region doping level N_B, the punch through depletion width W, the critical field E_C and the avalanche breakdown voltage (V_{BAV}) and also V_{BPT}. From a tally of breakdown voltages shown in Table 5.5, it was found that a uniformly doped drift region device at a doping level of 10^{15} per cc with a device height of 73μm gave a V_{BAV} of 6.4kV and V_{BPT} of 5kV. Hence, uniformly doped drift region devices could be designed for the breakdown voltages of 5kV as $V_{BPT} < V_{BAV}$.

CHAPTER 4

ANALYSIS AND DESIGN OF 6H-DIMOSFET USING LINEARLY GRADED DRIFT REGION PROFILE

4.1 INTRODUCTION

This chapter describes the device structure of vertical DIMOSFET with linearly graded profile in the drift region with a low doping of 10^{14} per cc near the source to higher values near the drain. The effect of a linearly graded drift region in a 6H-SiC vertical DIMOSFET on the power dissipation of the device has been discussed. The profile used has a low peak doing level at the top near the source and increases linearly towards the drain. The mathematical calculations of depletion region width as well effective doping concentration was done separately. The drift region defines the blocking voltage capabilities. After the calculations of depletion width and effective doping concentration, the drain voltages as well as channel voltages, specific on-resistance, breakdown voltages and power dissipations have been evaluated. The results have been analyzed by considering the variations of current density vs forward voltage, drain current vs forward voltage, drain current vs drain to source voltage, drain current vs channel voltage, specific on resistance vs power dissipation at different concentration gradients. Finally, the current density vs power dissipation at different profiles of uniform doping levels and linearly graded profiles and percentage reduction in power dissipation at a current density of 1000 A/cm^2 have been calculated. The results have been compared

with those of a device with uniformly doped drift region with a doping level almost equal to the effective doping level of the graded profiles given in Chapter 3.The power dissipation has been shown to decrease significantly by a maximum of about 61% for linearly graded profiles compared to those with uniformly doped drift regions. Breakdown voltages are about 5kV for uniformly doped devices compared to 10 kV for linearly graded ones, with the later being thinner devices [107-115].

4.2 VERTICAL DIMOSFET WITH INEARLY GRADED PROFILE

The ultimate aim in reducing the magnitude of $R_{on\text{-}sp}$ of vertical DIMOSFET is to reduce its power dissipation, P_D or its power loss which is given by $P_D \sim J_{on}^2 R_{on\text{-}sp} A$, where J_{on} is the on state current density and A is the device cross sectional area. The reduction of power dissipation suggested in this chapter has been made on the basis of using a linearly graded doping profile in the epitaxial layer of the DIMOSFET with a lightly doped region at the top to a linearly increasing doping level near the drain and at the bottom of the device. Such a profile has a linearly graded profile in the accumulation region (A), JFET region (B) and drift region (C) of the vertical DIMOSFET shown in Figure-4.1. The device should give a wide depletion region owing to low doping level in region B and a low parasitic series resistance in region C because of a higher doing level. This structure should significantly reduce the magnitude of $R_{on\text{-}sp}$ because of an increase in magnitude of the effective doping level and a corresponding decrease in the depletion region width at given value of V_{DS}. Such devices are likely to have lower power dissipation, smaller device thickness and a lower blocking voltage than devices with uniformly doped epitaxial layers.

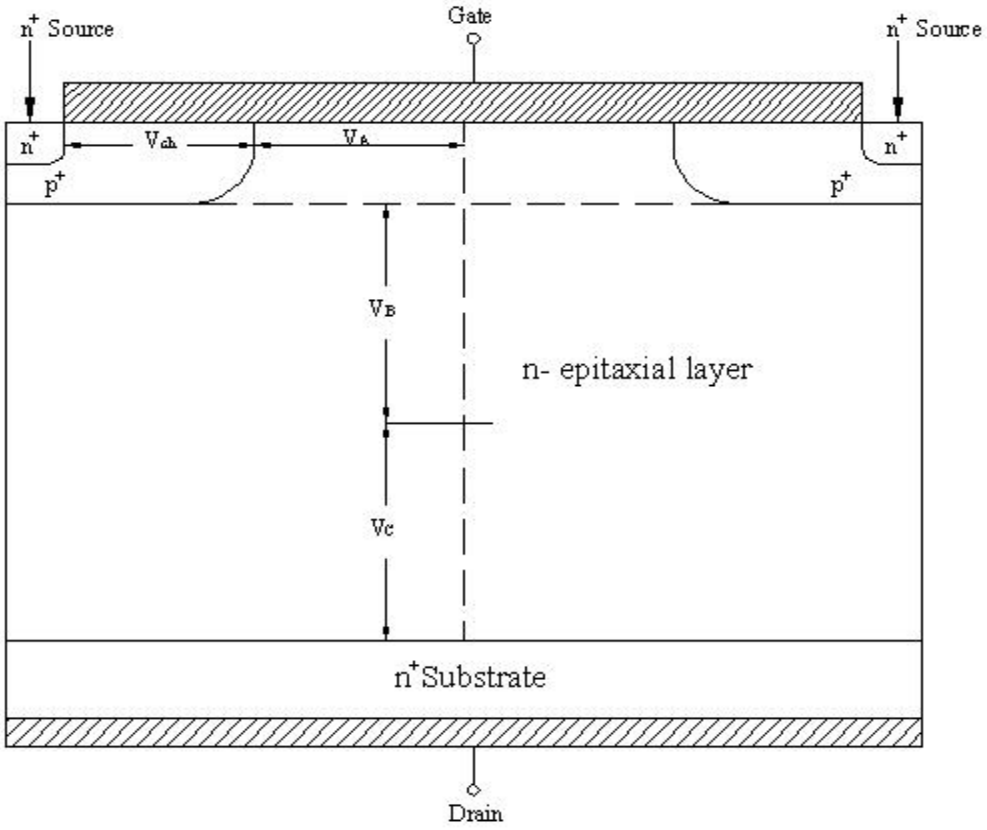

Figure-4.1

4.3 THEORETICAL ANALYSIS

The basic structure of the DIMOSFET as shown in Figure-4.1 is redrawn labeled with the device dimensions using suitable symbols and is shown in Figure-4.2. In this section DIMOSFET with linearly graded drift regions have been discussed.

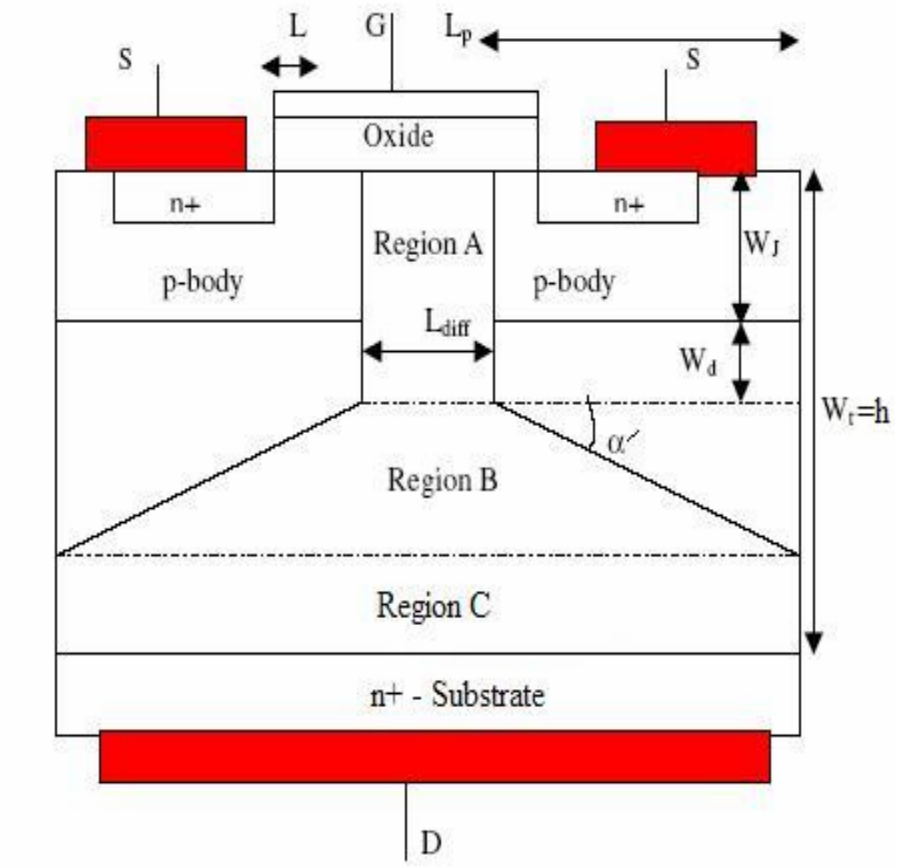

Figure-4.2

The power dissipation, P_D for a 50% duty cycle of these two devices for various current levels can then be calculated using the basic equations:

$$P_D = \frac{1}{2}\left(J_{on}^2 AR_{on-sp} + J_L V_B A\right) \tag{4.2}$$

Where, J_{on} is the on state current density, J_L is the reverse leakage current density of the p-body/n-drift region junction located in region B(Figure-4.1), V_B is the breakdown voltage of the DIMOSFET and A is the device area. Since J_L is negligible in SiC diode [33], eq(4.2) can be simplified

$$P_D = \frac{1}{2}\left(J_{on}^2 AR_{on-sp}\right) \tag{4.3}$$

Writing J_f as the forward current density considered to be same as J_{on}, eq(4.3) gives,

$$P_D = \frac{1}{2}\left(J_f^2 AR_{on-sp}\right) \tag{4.3}$$

The channel current I_{ch} which equals the drain current I_{DS} in on-state can be expressed by [80]

$$I_{DS} = \frac{W\mu_n}{2L[1+(\mu_n / 2v_{sat}L)V_{ch}]} V_{ch}[2C_{ox}(V_{GS}-V_T)-(C_{ox}+C_{do})V_{ch}] \tag{4.4}$$

where W is the device width, L is the channel length, μ_n is the effective zero field doping dependent carrier mobility corresponding to doping level N_B of the drift region obtained from[33], V_{ch} is the voltage across the channel region, v_{sat} is the saturated drift velocity of the carrier taken to be $2x10^7$ cm per sec, C_{ox} is the oxide capacitance per unit area, V_{GS} is the gate source voltage, C_{do} is the body depletion capacitance considered to be much less than C_{ox} and can be neglected.

The voltage drops across regions A, B and C have derived [80] and found to be of the form:

$$V_A = \frac{I_{DS}(W_j + W_d)}{W(L_{diff} eN_{eff})\mu_n - I_{DS}/E_c} \tag{4.5}$$

$$V_B = \frac{I_{DS}}{WeN_{eff}\mu_n \cot\alpha} \log\left[\frac{WeN_{eff}\mu_n(L_{diff}+L_p)-I_{DS}/E_c}{WeN_{eff}\mu_n L_{diff}-I_{DS}/E_c}\right] \tag{4.6}$$

$$V_C = \frac{I_{DS}\left(W_t - W_j - W_d - L_p \tan\alpha\right)}{WeN_{eff}\mu_n(L_s+2L_p)-I_{DS}/E_c} \tag{4.7}$$

where the symbols are the same as those shown in Figure-4.2 and L_{diff} is the separation of p-bodies. Here W_t=h, the device height which has been set by using the maximum depletion region width i.e. the punch through width for a given breakdown voltage, W_j is the p-body thickness and W_d is the depletion region width under on-state condition, the drain to source voltage V_{DS} obtained by adding V_{ch}, V_A, V_B and V_C. The drift region

voltage drop $V_{drift}=V_A+V_B+V_C$ and $V_{DS}=V_{drift}+V_{ch}$. The device height, 'h' has been set by setting the depletion region width at the punch through breakdown voltage equal to that at the avalanche breakdown voltage.

For the case of DIMOSFET with a linearly graded drift region with a gradient α, the p-body/n-epitaxial layer junction, depletion region width had been evaluated using the equation of a one-sided linearly graded junction as the depletion region could be regarded as negligible. The effective concentration, N_{eff} of a linearly graded drift region has been obtained by integrating over the device height,h [106]

$$N_{eff} = \frac{h\alpha}{\ln\left(1+\frac{\alpha h}{N_0}\right)} \tag{4.8}$$

where N_0 is the value of the n-drift region doping level at the p-base /n-drift region junction assumed to be 10^{14} or 10^{15} per cc in this chapter.

The values of V_{ch} can be evaluated by using equation (4.4). For this equation, the value of C_{do} is much less than C_{ox} and can be neglected and the value of V_{GS}=40V and V_T=1V, the equation (4.4) now becomes

$$I_{ch} = \frac{W\mu_n C_{ox} V_{ch}[78 - V_{ch}]}{2L[1+(\mu_n / 2v_{sat}L)V_{ch}]} \tag{4.9}$$

where μ_n is the mobility at the effective doping level, N_{eff}.

After solving eq. (4.9), we get

$$I_{ch} = \frac{W\mu_n C_{ox} V_{ch}[78 - V_{ch}]}{2v_{sat}L + \mu_n V_{ch}} \tag{4.10}$$

Eq.(4.10) can be written as

$$W\mu_n v_{sat} C_{ox} V_{ch}^2 + (\mu_n I_{ch} - 78W\mu_n v_{sat} C_{ox})V_{ch} + 2v_{sat} L I_{ch} = 0 \tag{4.11}$$

Eq.(4.11) is again a quadratic equation, the value of V_{ch} could be evaluated as:

$$V_{ch} = \frac{-(\mu_n I_{ch} - 78W\mu_n v_{sat} C_{ox}) \pm \sqrt{(\mu_n I_{ch} - 78W\mu_n v_{sat} C_{ox})^2 - 8LWI_{ch}\mu_n v_{sat}^2 C_{ox}}}{2W\mu_n v_{sat} C_{ox}} \quad (4.12)$$

Lastly, the specific on-resistance of the DIMOSFET could be expressed using Figure-4.2 as [80]:

$$R_{on-sp} = RA = \rho l = \frac{(W_t - W_j - W_d - L_p \tan\alpha')}{\mu_{neff} e N_{eff}} \quad (4.13)$$

Where α' is the angler of the slope of the drift region narrowing and μ_{neff} has been obtained from [33] corresponding to the effective concentration of N_{eff} of the linearly graded drift region. Thus N_{eff} and μ_{neff} give the overall average value of doping level and carrier mobility in the drift region respectively. A fixed value of device current $I_{DS}=I_{ch}$ is used and W_d is obtained by iteration from eq. (4.5). Finally Ron-sp could be calculated using eq. (4.13).

The magnitude of power dissipation P_D can be calculated by knowing R_{on-sp}, J_{on} and the device cross sectional area A. Values of P_D for different doping levels, concentration gradients for different current levels. The value of V_B and V_C are then calculated using eqs. (4.6) and (4.7). The magnitude of V_{ch} is obtained knowing a preset value of I_{DS}. The $V_{DS}= V_{drift}+V_{ch}= V_{ch} + (V_A+V_B+V_C)$, where V_{drift} is the voltage drop across the drift region. Finally, the forward voltage drop can be calculated using the equation $V_f = J_{on} \cdot R_{on-sp}$.

4.3.1 The Critical Field, E_c and the Breakdown Voltage Calculations

The depletion region width at breakdown can be estimated by first estimating the depletion region width for punch through breakdown voltage, V_{BPT} and was obtained by using the equation

$$W = \left[\frac{12\varepsilon_s (V_{BPT} + V_g)}{eN_{eff}}\right]^{\frac{1}{3}} \approx \left[\frac{12\varepsilon_s V_{BPT}}{eN_{eff}}\right]^{\frac{1}{3}} \tag{4.14}$$

as Vg « V_{BPT}, where V_g is the gradient voltage for the linearly graded drift region.

The depletion region width W for a linearly graded drift region corresponding to punch through breakdown voltage, V_{BPT} could be obtained from eq.(4.14). The corresponding critical field E_c for avalanche breakdown could be obtained using the equation [28]:

$$E_c = \left(\frac{e\alpha W^2}{8\varepsilon_s}\right) \tag{4.15}$$

where $W^{/}$ represents the depletion region width at breakdown.

The avalanche breakdown voltage V_{BAV} was then calculated using the equation

$$V_{BAV} = \frac{2}{3} E_C W \tag{4.16}$$

where the depletion width at the two breakdown voltages had again been set equal to each other.

4.3.2 Calculations & Related Graphs

The device dimensions of 6H DIMOSFET had been set so that the height $h \approx W_t$ equals the depletion region width, W_d under a reverse bias of 5kV applied on the p-body/n-epitaxial layer junction. In other words the DIMOSFET was designed for a maximum blocking voltage of 5kV. The dimensions of other variables as shown in Figure-4.2 have been taken to be:

W_j=1μm, L_p=25μm, $\alpha^{/}=64^0$, where $\alpha^{/}$ is the angle of slope of drift region narrowing. The quantity W_j had been taken to be 1μm as before an implant depth in 6H-SiC is of this order [105]. The device cross-sectional area A for a single unit was taken to be 12000 $x10^{-8}$ cm^2.

Calculations of the 6H-SiC DIMOSFET with a linearly graded drift region had been made by using a doping profile with a doping level of 10^{14} per cc near the source to 10^{16}, 10^{17} and 10^{18} per cc near the drain and other with a 10^{15} to 10^{19} per cc gradient of the device height W_t=h. The device height 'h' had been set at 65μm instead of 73 μm for the uniformly doped profiles as graded profiles yield smaller depletion region width at a given voltage than do uniformly doped profiles. The corresponding reverse voltage which was the punch through voltage, V_{BPT} obtained from eq.(4.16) is 6.75kV. The gradient α was obtained by taking the difference in carrier concentration from source to drain and dividing it by W_t=h=65μm.

The specific $R_{on\text{-}sp}$ is obtained by calculating N_{eff} from eq. (4.8), finding the effective value of mobility, μ_{neff} from the μ versus field plot [33] and using eq.(4.13) with $\alpha^{/}=64^0$.

The values of power dissipation, P_D were then calculated using current densities, J_F ranging in magnitude from 1 to 1000 amperes per cm^2. This was repeated for other values of concentration gradient 'α'. The results are shown in Tables 4.1 to 4.4. The plot of power dissipation vs. J_F, the forward current density is shown in Figure-4.3. The variation of the specific on resistance of the device for the various values of V_{DS} is shown in Figure-4.4. The variations of current density vs forward voltage, drain current vs forward voltage, drain current vs drain to source voltage, drain current vs channel

voltage, specific on resistance vs power dissipation at different concentration gradients are shown in Figure- 4.5-4.9. A comparison of plots of power dissipation of 6H-SiC DIMOSFET for devices having uniformly doped and linearly graded drift regions for different doping levels (N_B) obtained in Chapter3 and gradient values (α) respectively is shown in Figure-4.10.

Table-4.1: Results of currents, voltages, R_{on-sp} and power dissipation for doping of 10^{16}-10^{14} per cc, h=.0065 cm, $N_{eff}=2.15x10^{15}$/cc, $\mu_n=530cm^2$/V-sec,$\alpha=1.58x10^{18}$ cm^{-4}, $A=12000x10^{-8}cm^2$

J_F (A/cm^2)	I (A)	V_{ch} (V)	V_A (V)	V_B (V)	V_C (V)	$V_{DS}=V_A+V_B+V_C+V_{ch}$ (V)	W_d (cm)	R_{on-sp} (Ω-cm^2)	V_f (V)	P_D (W)
1	12e-5	.0028	.0015	.0191	.0059	.0293	1.07e-4	.0119	.0119	7.13e-7
10	12e-4	.028	.024	.191	.0561	.299	2.33e-4	.0099	.099	6.72e-5
100	12e-3	.283	.4383	1.91	.487	3.116	5.1e-4	.00883	.883	.0058
1000	12e-2	3.16	8.80	19.20	3.23	34.32	.0011	.00847	8.46	.3761

Table-4.2: Results of currents, voltages, R_{on-sp} and power dissipation for doping of 10^{17}-10^{14} per cc, h=.0065 cm, N_{eff}=1.45x10^{16}/cc, μ_n=500cm^2/V-sec,α=1.54x10^{19} cm^{-4}, A=12000x$10^{-8}$$cm^2$

J_F (A/cm^2)	I (A)	V_{ch} (V)	V_A (V)	V_B (V)	V_C (V)	$V_{DS}=V_A+V_B+V_C+V_{ch}$ (V)	W_d (cm)	R_{on-sp} (Ω-cm^2)	V_f (V)	P_D (W)
1	12e-5	.003	1.52e-4	.0030	9.6e-4	.0071	3.1e-5	.0019	.0019	1.16e-7
10	12e-4	.029	.0019	.030	.0095	.071	6.66e-5	.0016	.0163	1.15e-5
100	12e-3	.3	.0281	.301	.0921	.721	1.4e-4	.0014	.1428	.0011
1000	12e-2	3.37	.480	3.01	.847	7.70	3.18e-4	.0011	1.1429	.1015

Table-4.3: Results of currents, voltages, R_{on-sp} and power dissipation for doping of 10^{18} -10^{14} per cc, h=.0065 cm, N_{eff}==1.09x10^{17}/cc,μ=300cm^2/V-sec,α=1.54x10^{20} cm^{-4}, A=12000x10^{-8} cm^2

J_F (A/cm^2)	I (A)	V_{ch} (V)	V_A (V)	V_B (V)	V_C (V)	$V_{DS}=V_A+V_B+V_C+V_{ch}$ (V)	W_d (cm)	R_{on-sp} (Ω-cm^2)	V_f (V)	P_D (W)
1	12e-5	.0050	2.91e-5	6.67e-4	.00022	.0059	1.35e-5	.00042	.00042	2.61e-8
10	12e-4	.050	3.31e-4	6.67e-3	.0022	.059	2.92e-5	.00040	.0040	2.59e-6
100	12e-3	.50	.0042	.0667	.021	.592	6.28e-5	.00037	.03658	2.55e-4
1000	12e-2	5.82	.0617	.667	.205	6.754	1.41e-4	.00034	.3387	.025

Table-4.4: Results of currents, voltage, R_{on-sp} and power dissipation for 10^{19}-10^{15} per cc, h=.0065 cm, $N_{eff}=1.09x10^{18}$/cc,$\mu=140cm^2$/V-sec,$\alpha=1.54x10^{21}$ cm^{-4},$A=12000x10^{-8}cm^2$

J_F (A/cm^2)	I (A)	V_{ch} (V)	V_A (V)	V_B (V)	V_C (V)	$V_{DS}=V_A+V_B+V_C+V_{ch}$ (V)	W_d (cm)	R_{on-sp} (Ω-cm^2)	V_f (V)	P_D (W)
1	12e-5	.011	5.91e-6	1.42e-3	4.66e-5	.0112	7.77e-6	9.32e-5	9.32e-5	5.59e-9
10	12e-4	.11	6.51e-5	1.43e-3	4.64e-4	.112	1.67e-5	8.68e-5	8.68e-4	5.57e-7
100	12e-3	1.08	7.45e-4	1.429e-2	4.61e-3	1.103	3.58e-5	7.65e-5	7.65e-3	5.53e-5
1000	12e-2	14.28	.0101	.143	.0453	14.48	8.46e-5	6.79e-5	6.79e-2	.0054

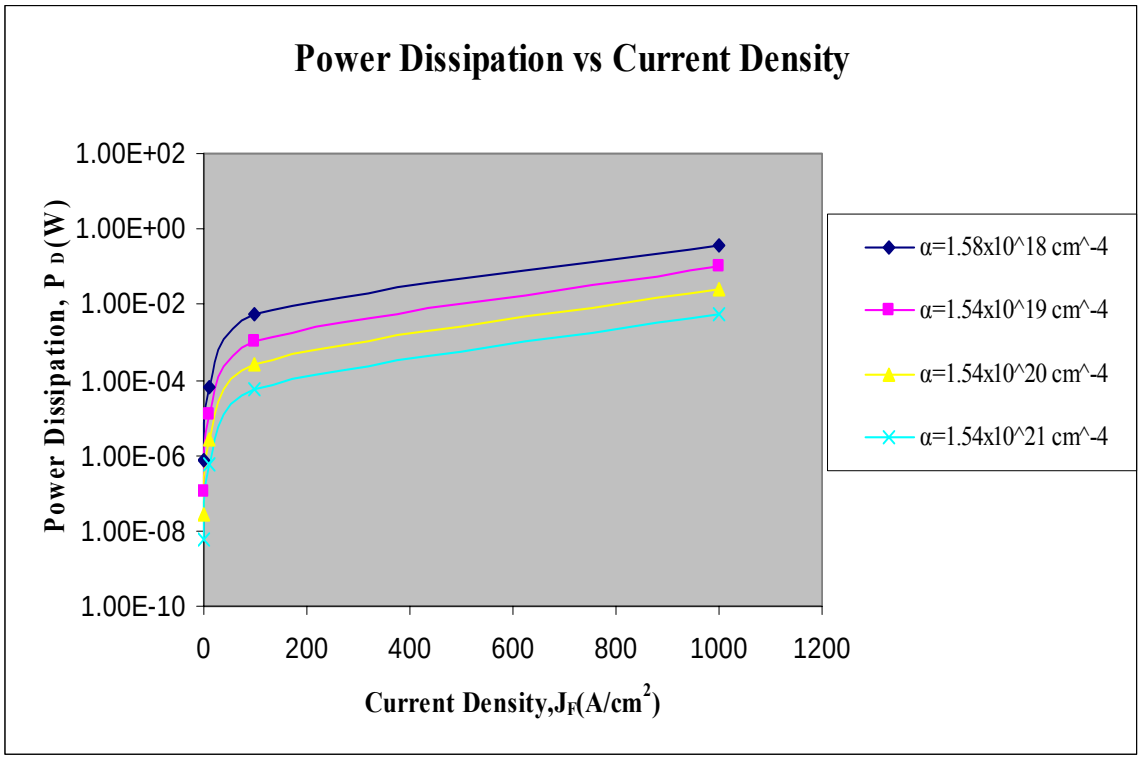

Figure-4.3: Plot of Power Dissipation vs. Current Density for a 6H-SiC DIMOSFET for various values of drift region gradient α for Linearly Graded Profile

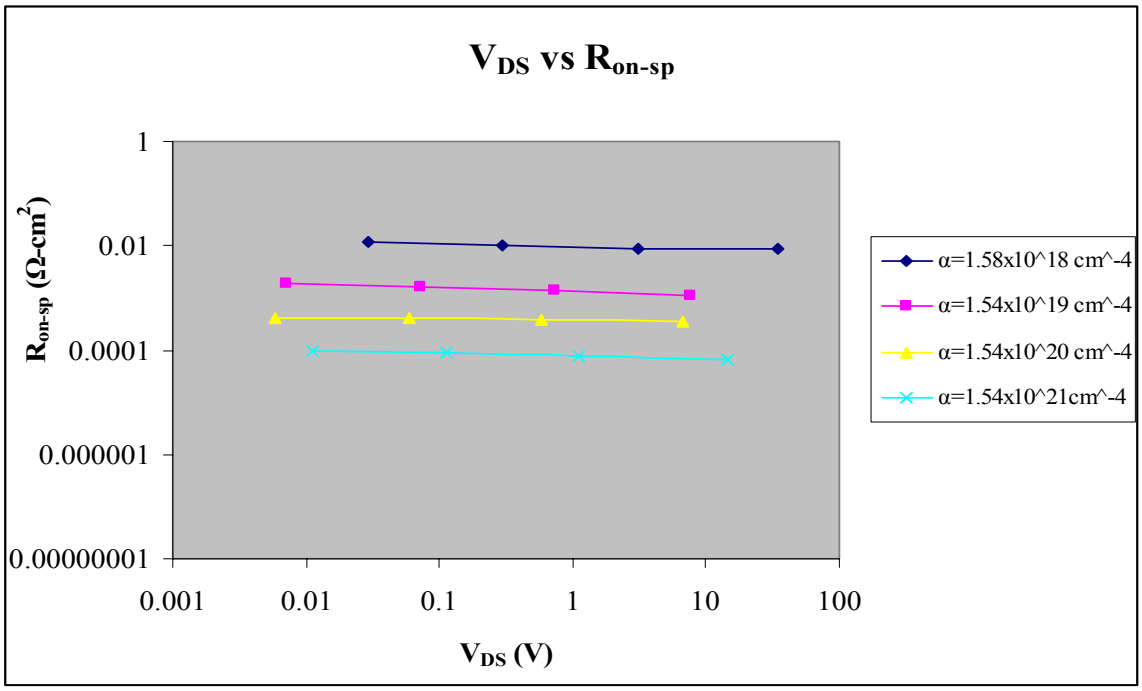

Figure-4.4: Plot of Drain Voltage vs. Specific on Resistance for a 6H-SiC DIMOSFET for various values of drift region gradient α for Linearly Graded Profile.

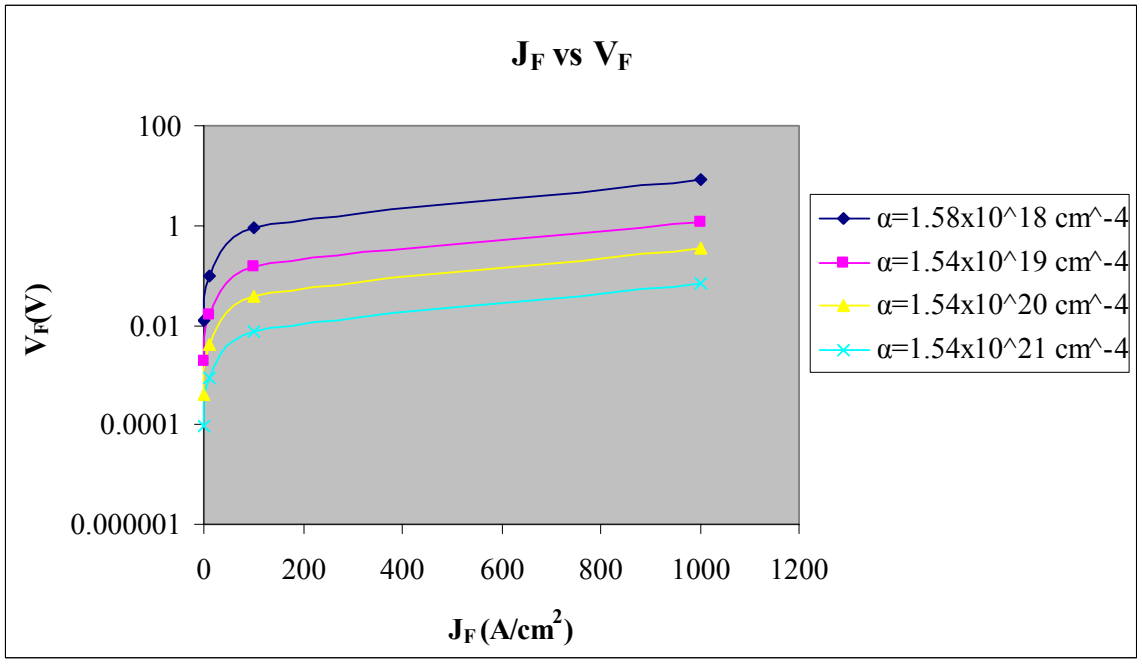

Figure-4.5: Plot of Forward Current Density vs. Forward Voltage Drop for a 6H-SiC DIMOSFET for various values of drift region gradient α for Linearly Graded Profile

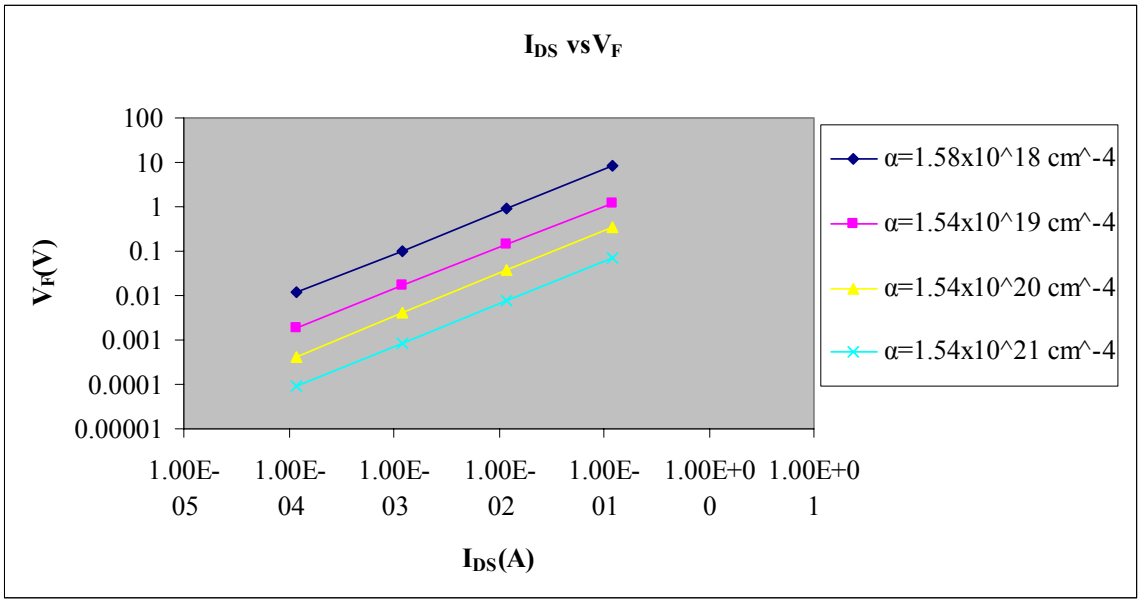

Figure-4.6: Plot of Drain Current vs. Forward Voltage Drop for a 6H-SiC DIMOSFET for various values of drift region gradient α for Linearly Graded Profile

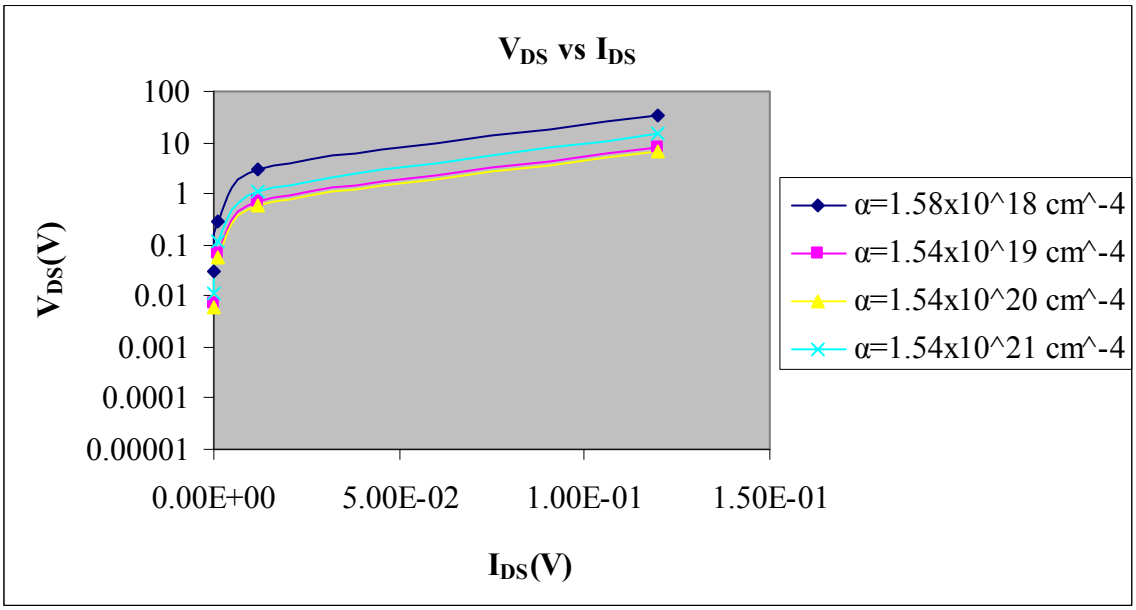

Figure-4.7: Plot of Drain Current vs. Drain to Source Voltage for a 6H-SiC DIMOSFET for a 6H-SiC DIMOSFET for various values of drift region gradient α for Linearly Graded Profile

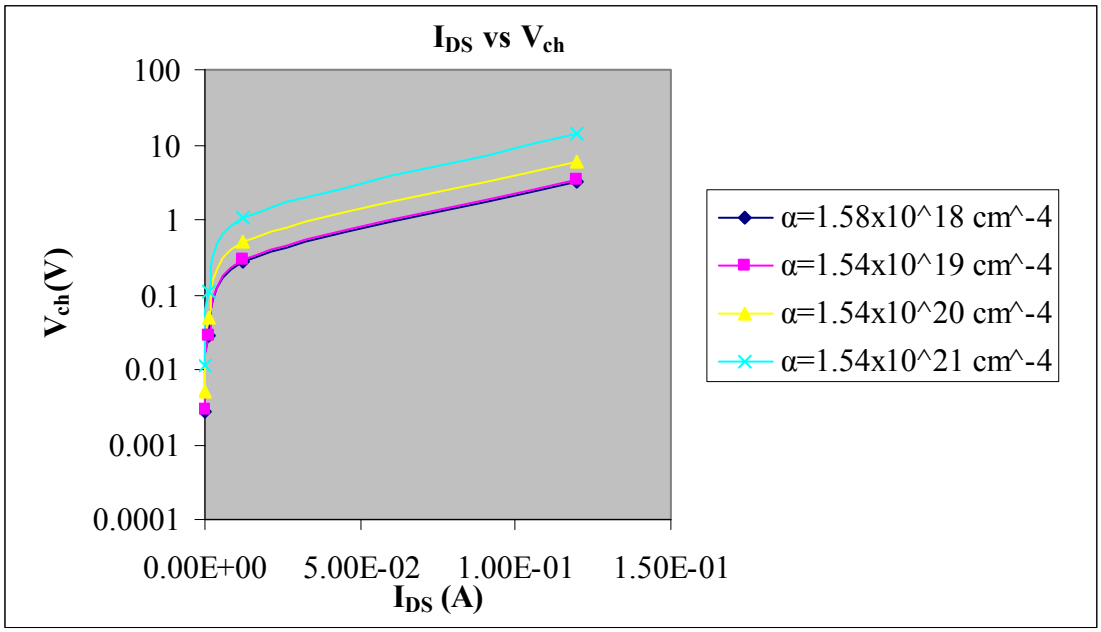

Figure-4.8: Plot of Drain Current vs. Channel Voltage for a 6H-SiC DIMOSFET for various values of drift region gradient α for Linearly Graded Profile

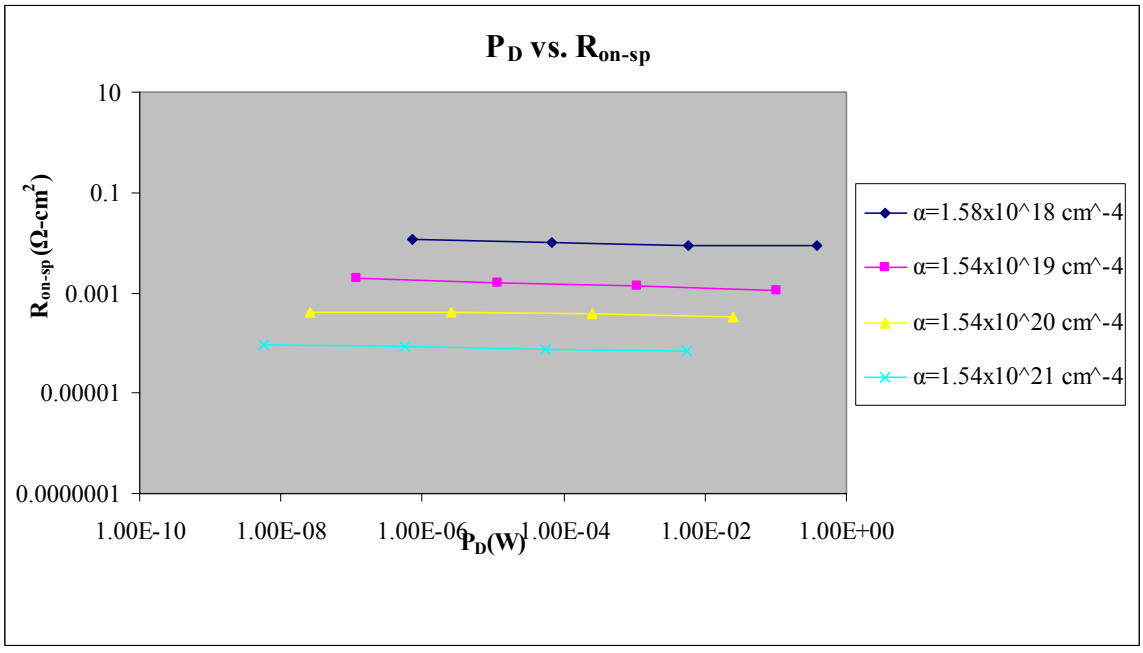

Figure-4.9: Plot of Power Dissipation vs. Specific-on-resistance for a 6H-SiC DIMOSFET for various values of drift region gradient α for Linearly Graded Profile

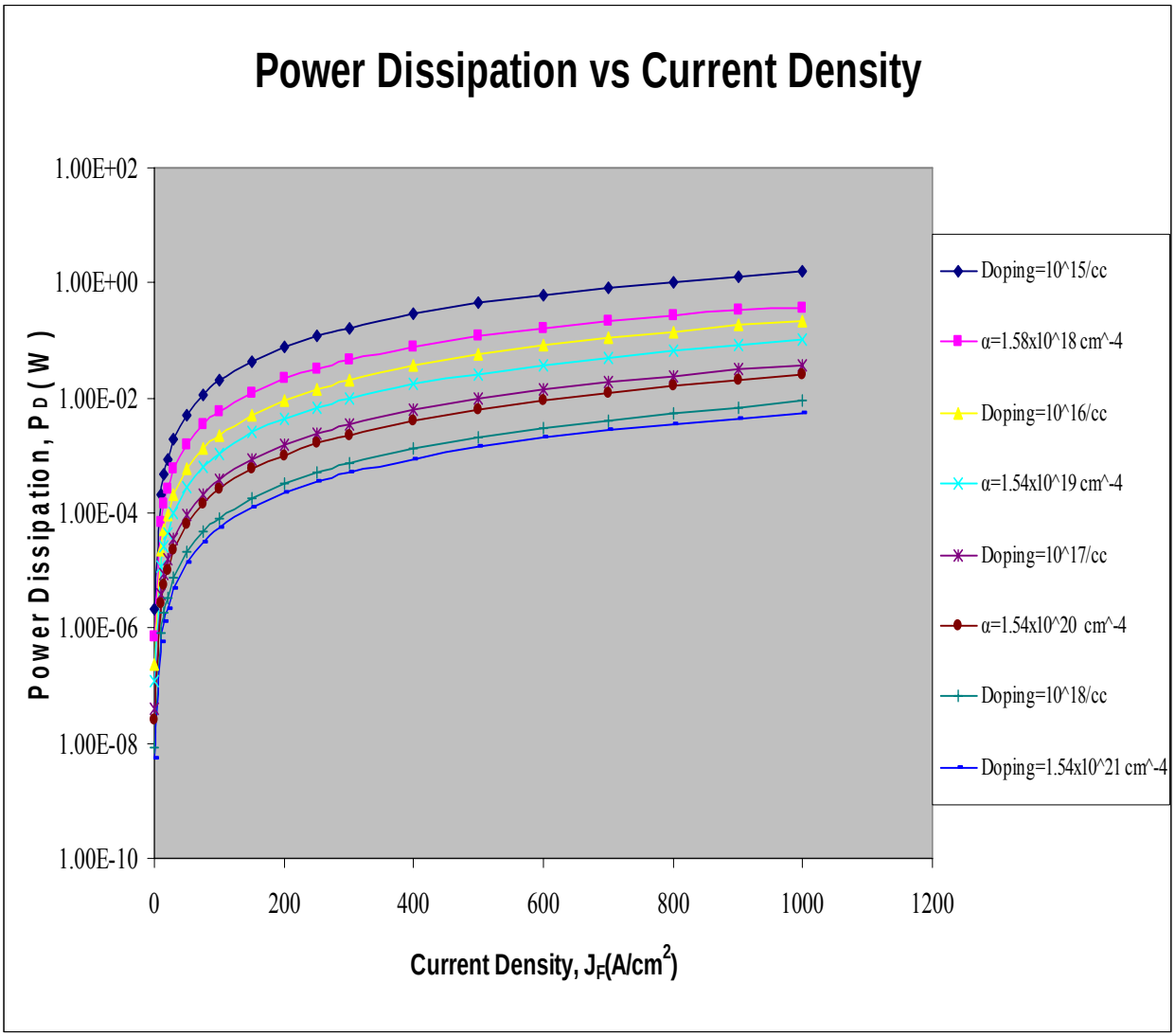

Figure-4.10: Comparison of power dissipation values of 6H-SiC DIMOSFET for different doping levels (N_B) of uniformly doped drift region and gradient values (α) of linearly graded drift region.

4.4 CALCULATION OF BREAKDOWN VOLTAGES (V_{BPT} and V_{BAV})

The breakdown voltage considered here are the punch-through breakdown voltage, V_{BPT} and the avalanche breakdown voltage, V_{BAV}. For a given voltage, device design requires that the two voltages be made equal to each other. In this work, the lower breakdown voltage has been considered for use as the device breakdown voltage.

In case of linearly graded profile, the punch through breakdown voltage V_{BPT} was set at 6.75kV for a depletion region width W of 65 μm considered equal to device height W_t=h with a gradient of $1.58x10^{18}$ cm^{-4}. The value of critical field, E_c was calculated using equation (14) and avalanche breakdown voltage V_{BAV} from equation (15). The depletion region width W for the values of α was calculated by using equation (12). The results are shown in Table 4.5.

Table-4.5: Results of calculation of breakdown voltages, V_{BAV} and V_{BPT} for linearly graded drift region devices

Grad 'α' cm^{-4}	W'(μm)	$E_c = \left(\frac{e\alpha W'^2}{8\varepsilon_s}\right)$ (V/cm)	$V_{BAV}=(2/3)(E_cW')$ (volts)	V_{BPT} (volts)
$1.32x10^{18}$	75	$1.73x10^6$	8.75 kV	10 kV
$1.58x10^{18}$	65	$1.55x10^6$	6.74 kV	6.75kV
$1.54x10^{19}$	26	$2.42x10^6$	4.20 kV	4kV
$1.54x10^{20}$	8.56	$2.63x10^6$	1.49 kV	1.5kV
$1.54x10^{21}$	3.42	$4.20x10^6$	956.37V	1kV

4.5 SUMMARY

The analysis of power dissipation values, P_D with linearly graded drift regions showed a similar variation in the magnitudes of V_{ch}, V_A, V_B and V_C with J_f as in the case of uniformly doped drift region of 6H-SiC DIMOSFET's over the range of concentration gradients, α from $1.58x10^{18}$ to $1.54x10^{21}$ cm^{-4}. However, the channel voltage V_{ch} corresponding to effective concentrations at a given current level was found to be almost the same as in the case of uniformly doped devices with equivalent carrier concentrations. The magnitudes of V_A, V_B, and V_C as also V_{DS} showed a decrease with increasing value of α. This was also found to be true for R_{on-sp}, V_f and P_D as shown in Figs.4.3-4.5. The power dissipation P_D at 1000 A/cm^2 dropped from .3761 to .0054W. Hence, the maximum amount of reduction in power dissipation that could be achieved over the range of values of power dissipation considered here was found to be 60% compared to uniformly doped drift region devices.

Estimation of breakdown voltages, i.e. punch through (V_{BPT}) and avalanche (V_{BAV}) breakdown voltage was made on the basis of the calculated data presented in Table 3.5 for uniformly doped drift region devices in Chapter 3 and Table 4.5 for linearly graded drift region devices in Chapter 4. The results in Table 3.5 of Chapter 3 were for a given drift region doping level N_B, the punch through depletion width W, the critical field E_C and the avalanche breakdown voltage (V_{BAV}) and also V_{BPT}. Table 4.5 of Chapter 4 gives the calculated values of V_{BAV} and V_{BPT} for various values of α, the concentration gradients of the drift region of the 6H-SiC DIMOSFET. From a tally of breakdown voltages shown in Table 3.5 of Chapter 3 and 4.5 of Chapter 4, it was found that a uniformly doped drift region devices with a drift region doping level of 10^{15} per cc with a

device height of 73μm gives a V_{BAV} of 6.4kV and V_{BPT} of 5kV but with a linearly graded drift region with the value of α of $1.58x10^{18}$ cm^{-4} with a device height of 65 μm would give the V_{BAV} of 6.74kV and V_{BPT} of 6.75kV. Considering the higher value of breakdown voltage as the breakdown voltage of the device, the former with uniformly doped profile should have a breakdown voltage equal to V_{BPT}=5kV and the latter with V_{BAV}=6.74kV. The device height in linearly graded drift region devices was 8μm less than those used in uniformly doped drift region devices. This could be achieved by increasing the breakdown voltage of (6.74-5) kV=1.74kV. The corresponding decline in power dissipation, P_D was about 61.41% at J_f=100A/cm^2.

In conclusion, it may be stated that 6H-SiC DIMOSFET's having linearly graded drift regions have significantly low values of power dissipation, P_D at any current level than uniformly doped drift region devices. This is shown in Figure-4.10. The former have slightly higher breakdown voltage than latter but are about 10 to11% thinner than them. Thus, it was useful to obtain 6H-SiC DIMOSFET's with linearly graded drift regions as these devices could be fabricated with lesser device height and give a low power dissipation but a slightly more breakdown voltage than uniformly doped drift region devices. At W_t=h=75μm, the linearly graded profile could provide the maximum breakdown voltage of 10kV.

CHAPTER 5

ANALYSIS AND DESIGN OF 6H-DIMOSFET USING DRIFT REGION GAUSSIAN PROFILE

This chapter analyses the device structure of vertical DIMOSFET with Gaussian Profile in the drift region. Doping profile used in semiconductor industry usually has non-linearly graded profile inside semiconductor layers. These profiles are usually a Gaussian or a Complementary Error Function distribution. The effective doping level of the former has been evaluated with the Gaussian peak being displaced towards the drain end of the device. The overall doping level called the effective doping level (N_{eff}) has been obtained by integrating the Gaussian profile within specified ranges of the depth into the semiconductor from source to drain of the MOSFET. Theoretical formulations of depletion region width and effective doping concentration have been formulated and drain voltages as well as channel voltages, specific on-resistance, breakdown voltages and power dissipations are evaluated. The results have been analysed from the plots of power dissipation vs current density and specific on-resistance versus drain to source voltage with different Gaussian profiles generated by the varying peak concentration. The estimated maximum breakdown voltage was found to be about 16kV.

5.1 INTRODUCTION

The analysis of power dissipation (P_D) and breakdown voltages (V_{BPT} and V_{BAV}) had been made in the last chapter with a linearly graded drift region of 6H-SiC

DIMOSFET. However, a similar type of variation in P_D and the breakdown voltages could be observed with a Gaussian profile in the drift region of the device. The device may be considered with its drift region doping profile to be a Gaussian function with its peak located near the drain end of the device and the impurity concentration may be expected to fall to very small values near the n-drift region and p-body junction. This would also give a low parasitic series resistance near the drain and a large depletion region in the drift region near the junction. The theoretical analysis first determines the effective concentration (N_{eff}) in the drift region considered over the device height 'h' which was fixed by using a predetermined punch through voltage of 16kV to evaluate the depletion region width at punch through. The Poisson's equation for the junction has been solved for the voltage V(x) across the junction using the Gaussian profile as the carrier concentration model and obtaining the solution to the depletion region width at predetermined voltages. The calculation of voltages V_{ch}, $V_{A,}$ V_B, and V_C had also been done and power dissipation (P_D) at the same current levels as those in Chapter 4 had been obtained.

Since the punch through depletion region width 'W' at a blocking voltage of 16kV is large and so is the device height 'h'. Hence for large value of 'h', the Gaussian function may be considered to yield very low impurity concentration near the n-drift region and p-body junction. The carrier concentration near this junction can to a first approximation may be regarded as uniform and avalanche breakdown voltages may be calculated by considering the equation for V_{BAV} for uniformly doped junctions. The breakdown voltages V_{BPT} and V_{BAV} are thus obtained and the lower of the two for a given Gaussian profile had been selected as the actual breakdown voltage of the device.

5.2 THEORETICAL ANALYSIS

Since silicon carbide has very low value of diffusion coefficient 'D' for impurities, a Gaussian profile carrier concentration in thin drift region needs to be grown by some special technique other than ion-implantation, as the device height 'h' considered here is quite large.

5.2.1 Effective Concentration (N_{eff}):

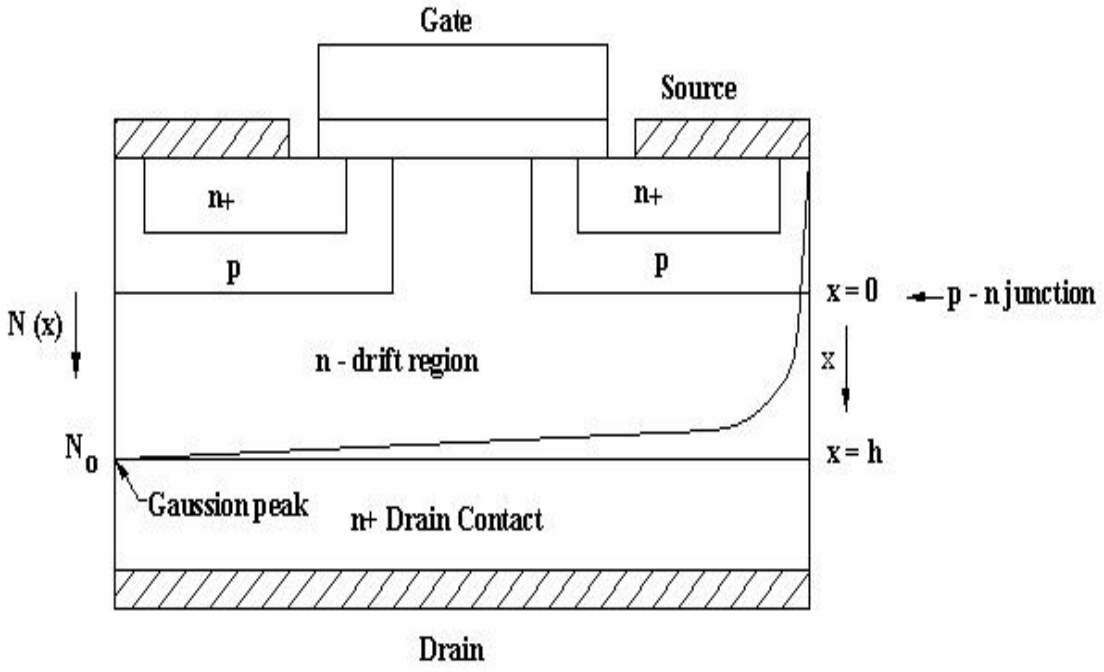

Figure-5.1: Cross-sectional structure of DIMOSFET showing Gaussian profile in the drift region

The equation for the effective concentration, N_{eff} in the Gaussian profile can be derived with reference to Figure-5.1. The drift region here has a non uniform doping level, i.e. a Gaussian function with a peak values of N_0 near the drain decreasing upwards to very low values near the n-drift region and p-body junction. The equation to this profile may be written as,

$$G(x) = N_0 e^{-\left(\frac{h-x}{m}\right)^2} \quad , \tag{5.1}$$

where m is constant, h is the device height and x is the distance from the junction as shown in Figure- 5.1.

The total carrier concentration N_{Total} in the device can be written down as:

$$N_{Total} = \int_0^h G(x)Adx = \int_0^x N_0 e^{-\left(\frac{h-x}{m}\right)^2} Adx \, , \tag{5.2}$$

where A is the cross-sectional area of the device.

Since the integral of a Gaussian function is an error function given by:

$$erf(x) = \frac{2}{\sqrt{\pi}} \int_0^h G(x)dx \tag{5.3}$$

Eq.(5.2) can be written as,

$$N_{Total} = \frac{N_0 mA\sqrt{\pi}}{2} erf\left(\frac{h}{m}\right) \tag{5.4}$$

Hence, effective carrier concentration (N_{eff}) of the drift region per cc can be expressed as:

$$N_{eff} = \frac{N_{Total}}{Ah} = \frac{N_0 m\sqrt{\pi}}{2h} erf\left(\frac{h}{m}\right) \tag{5.5}$$

5.2.2 Equation for Obtaining the Depletion Region Width 'W'

The depletion region width at any given reverse voltage, V_R can be obtained by solving the Poisson's equation for the system. Hence, for the Gaussian function G(x) , the Poisson's equation becomes

$$-\frac{\partial^2 V}{\partial x^2} = \frac{e}{\varepsilon_s} G(x) = \frac{eN_0 e^{-\left(\frac{h-x}{m}\right)^2}}{\varepsilon_s} \tag{5.6}$$

Integrating eq.(5.6) once from 0 to x gives the electric field E:

$$E = -\frac{dV}{dx} = -\frac{\sqrt{\pi}eN_0 m}{2\varepsilon_s}\,\mathrm{erf}\left(\frac{h-x}{m}\right) + C \ , \tag{5.7}$$

where C is a constant of integration

Since, at x=h, E=0, hence C=0. Eq.(5.7) then becomes,

$$E = -\frac{\sqrt{\pi}eN_0 m}{2\varepsilon_s}\,\mathrm{erf}\left(\frac{h-x}{m}\right) \tag{5.8}$$

The maximum field E_m occurs at x=0, giving

$$E_m = -\frac{\sqrt{\pi}eN_0 m}{2\varepsilon_s}\,\mathrm{erf}\left(\frac{h}{m}\right) \tag{5.9}$$

Finally integrating eq.(5.8) again from 0 to x gives the potential V(x)

$$-V(x) = -\int_0^x \frac{\sqrt{\pi}eN_0 m}{2\varepsilon_s}\,\mathrm{erf}\left(\frac{h-x}{m}\right)dx \tag{5.10}$$

For $x \to h, \frac{(h-x)}{m} < 1$, the error function can be expressed as:

$$\mathrm{erf}\left(\frac{h-x}{m}\right) = \frac{2}{\sqrt{\pi}}\left[\left(\frac{h-x}{m}\right) - \frac{1}{3}\left(\frac{h-x}{m}\right)^3 + ----\right] \tag{5.11}$$

Substituting eq.(5.11) in eq.(5.10) retaining the first two terms and integrating gives

$$-V(x) = \frac{eN_0}{\varepsilon_s}\left[\frac{x^4}{12m^2} - \frac{hx^3}{3m^2} - \frac{x^2}{2}\left(1 - \frac{h^2}{m^2}\right)\right] \tag{5.12}$$

At x=W, the depletion region width under a reverse bias V_R, then

$$V(W) = V_{bi} + V_R \tag{5.13}$$

where V_{bi} is the built in potential.

Substituting x=W and $V(W) \approx V_R$, because $V_R \gg V_{bi}$ in eq. (4.12) and simplifying gives:

$$\frac{W^4}{12m^2}-\frac{hW^3}{3m^2}-\frac{W^2}{2}\left(1-\frac{h^2}{m^2}\right)-\frac{\varepsilon_s V_R}{eN_0}=0 \qquad (5.14)$$

Eq.(5.14) can be used to calculate the depletion region width W at a given reverse bias V_R between the p-body and n-drift region of DIMOSFET.

5.2.3 Equation for Breakdown Voltages, V_{BAV} and V_{BPT}

The maximum attainable depletion region width at highest value of voltage V_R in eq.(5.14) for a given value of m gives the punch through voltage V_{BPT}. Since the Gaussian profile generated by ion-implantation falls off sharply from its peak value as one moves towards the source, the doping profile in the drift region may be considered to be almost uniform equal to N_{eff} (see eq.5.5) over the entire device height W_t=h as shown in Figure-5.1. Hence the magnitude of critical field 'E_C' can be calculated using eq. (3.8) in Chapter 3 with N_B replaced by N_{eff}. Finally, the avalanche breakdown voltage, V_{BAV} can be calculated using the equation for uniformly doped profiles i.e. $V_{BAV}=\frac{1}{2}E_C W$, where W is the maximum depletion region width at breakdown.

5.3 RESULTS AND CALCULATIONS

5.3.1 The Device Height 'h'

This has been set at h=350μm as eq. (4.14) gives real value of 'W' for all values of reverse voltages and has a maximum value of W=153μm at 16kV. Further increase in reverse bias does not alter the value of W. Hence, 16kV has been considered equal to the punch through breakdown voltage. For the values of h less than 350μm, eq. (5.14) does

not give any real value of W at any voltage. Hence, the device height has been set at h=350 μm.

5.3.2 Power Dissipation

Calculations of the values of voltages V_A, V_B, VC, V_{DS} and power dissipation, P_D have been made using equations (3.2)-(3.7) in chapter 3 for current densities of 1,10,100 and 1000 amperes per cm^2 for the values of peak concentration N_0 of 10^{18} and 10^{19} per cc with m=1x10^{-4}cm and N_B being replaced by N_{eff}. The maximum attainable depletion region width 'W' obtained from eq. (5.14) at a voltage of 16kV is 153.1μm for the device height, h of 350 μm. For higher voltages the magnitude of W does not change appreciably or that the depletion region width becomes constant which may be due to non linear nature of the Gaussian profile increasing towards the drain. The other values of N_0 used were 10^{19} and 4x10^{18} per cc with m=10x10^{-4}cm. The values of N_{eff} was calculated using eq. (5.5) and had been used for carrier concentration for calculating V_A, V_B and V_C. The mobility μ_{eff} corresponding to N_{eff} had been estimated from [33]. The critical field E_C had been calculated using eq.(3.8) in Chapter 3 using N_{eff} as the value of N_B. The results are shown in Tables 5.1-5.4 and Figures-5.2-5.8.

The maximum values of power dissipation, P_D ranges from 6.683W at a current density of 1000 Amps per cm^2as shown in Table 5.1 for N_0=10^{18} per cc and m=1x10^{-4} cm. The quantity 'm' can be determined in terms of the Gaussian profile generated by ion-implantation in terms of longitudinal straggle σ given by modified version of eq.(5.1) as:

$$G(x) = N_0 e^{-\left(\frac{h-x}{m}\right)^2} \qquad (5.15)$$

The minimum value of P_D with $N_0=4x10^{18}$ per cc and $m=10x10^{-4}$ cm was found to be 0.058W at a current density of 1000A/cm^2. The drop due to parasitic series resistance determined by V_C is maximum of 57.25V with the profile with $N_0 =10^{18}$ per cc with $m=1x10^{-4}$ cm and decreases to a minimum of 0.484V for $N_0=4x10^{18}$ per cc and $m=10x10^{-4}$ cm. The corresponding decrease in R_{on-sp} is 0.0685 cm^2 to 0.00026 Ω-cm^2 respectively. The values of V_{DS} varied from 76.66V with $N_0=10^{18}$ and $m=1x10^{-4}$ to 7.29V with $N_0=10^{19}$ and $m=10x10^{-4}$ cm. The depletion region width W had a maximum vale of 5.14μm for $N_0=10^{18}$ per cc, $m=1x10^{-4}$ cm to a minimum of 0.106μm for $N_0=4x10^{18}$ per cc to $m=10x10^{-4}$ cm. Thus, increase in the values of m results in a decrease in power dissipation P_D. This can be seen from Tables 5.2 & 5.3.

5.3.3 Breakdown Voltages, V_{BAV} and V_{BPT}

Results for the values of the punch through breakdown voltage V_{BPT} and V_{BAV} are shown in Table 5.5 with h=350μm. These results of Table 5.6 show that the breakdown voltages V_{BPT} and V_{BAV} are approximately the same for all sets of values of N_0 and m. However, an increase in the value of m at a fixed value of N_0 results in a decrease in breakdown voltages as seen in the case of $N_0=10^{19}$ per cc and m=1 & $10x10^{-4}$ cm changing V_B from 10 to 7 kV respectively. However, a decrease in the value of N_0 at fixed values of m decreases the breakdown voltage. This can be seen in the case of $N_0=10^{19}$ to $4x10^{18}$ per cc for $m=10x10^{-4}$ cm reduces the breakdown voltage from 7kV to 3kV. However, the opposite is true for low values of $m=1x10^{-4}$ cm. As N_0 decreases from 10^{19} per cc to 10^{18} per cc for $m=1x10^{-4}$ cm, the breakdown voltage increases from 10kV to 16 kV.

Table-5.1: Results of currents, voltages, R_{on-sp} and power dissipation for $m=1x10^{-4}$, $h=350x10^{-4}cm$, $Neff=3.12x10^{15}/cc$, $\mu=530cm^2/V\text{-}sec$

J_F (A/cm^2)	I (A)	V_{ch} (V)	V_A (V)	V_B (V)	V_C (V)	$V_{DS}=V_A+V_B+V_C+V_{ch}$ (V)	W_d (cm)	R_{on-sp} (Ω-cm^2)	V_f (V)	P_D (W)
1	12e-5	.0028	5.85e-4	.013	.058	.0747	1.6e-5	.1163	.1163	6.98e-6
10	12e-4	.028	.0076	.131	.581	.747	5.07e-5	.08972	.8972	6.97e-4
100	12e-3	.749	.132	1.32	5.79	7.52	1.61e-4	.07976	7.9763	.0694
1000	12e-2	21.03	3.077	13.16	57.25	76.66	5.14e-4	.0685	68.486	6.863

Table-5.2: Results of currents, voltages, R_{on-sp} and power dissipation for $m=1x10^{-4}$, $h=350x10^{-4}cm$, $Neff=2.69x10^{16}/cc$, $\mu=500cm^2/V\text{-}sec$

J_F (A/cm^2)	I (A)	V_{ch} (V)	V_A (V)	V_B (V)	V_C (V)	$V_{DS}=V_A+V_B+V_C+V_{ch}$ (V)	W_d (cm)	R_{on-sp} (Ω-cm^2)	V_f (V)	P_D (W)
1	12e-5	.003	6.33e-5	.0016	.0072	.0118	2.17e-6	.0143	.0143	8.58e-7
10	12e-4	.029	6.22e-4	.0162	.072	.1173	6.84e-6	.0088	.0876	8.58e-5
100	12e-3	.3	.0075	.162	.715	1.184	2.15e-5	.0068	.6759	.0086
1000	12e-2	3.37	.1053	1.623	7.146	12.23	6.99e-5	.0059	5.8658	.856

Table-5.3: Results of currents, voltages, R_{on-sp} and power dissipation for $m=10x10^{-4}$, $h=350x10^{-4}$cm, $Neff=2.69x10^{17}$/cc, $\mu=300cm^2$/V-sec

J_F (A/cm^2)	I (A)	V_{ch} (V)	V_A (V)	V_B (V)	V_C (V)	$V_{DS}=V_A+V_B+V_C+V_{ch}$ (V)	W_d (cm)	R_{on-sp} (Ω-cm^2)	V_f (V)	P_D (W)
1	12e-5	.0050	1.04e-5	2.69e-4	1.19e-3	.0065	5.08e-7	.0024	.0024	1.43e-7
10	12e-4	.050	1.04e-4	.0027	.012	.065	1.61e-6	.0019	.0186	1.43e-5
100	12e-3	.5	.0011	.027	.119	.647	5.08e-6	.0016	.1567	.0014
1000	12e-2	5.82	.0121	.269	1.191	7.29	1.71e-5	.0014	1.3872	.1429

Table-5.4: Results of currents, voltages, R_{on-sp} and power dissipation for $m=10x10^{-4}$, $h=350x10^{-4}$cm, $Neff=1.42x10^{18}$/cc, $\mu=140cm^2$/V-sec

J_F (A/cm^2)	I (A)	V_{ch} (V)	V_A (V)	V_B (V)	V_C (V)	$V_{DS}=V_A+V_B+V_C+V_{ch}$ (V)	W_d (cm)	R_{on-sp} (Ω-cm^2)	V_f (V)	P_D (W)
1	12e-5	.011	4.204e-6	1.09e-4	4.83e-4	.0116	2.96e-7	.0009	.0009	5.81e-8
10	12e-4	.106	4.23e-5	.0011	.0048	.112	9.2e-7	.00065	.0065	5.81e-6
100	12e-3	1.08	4.32e-4	.011	.0483	1.086	2.94e-6	.00048	.048	5.81e-4
1000	12e-2	14.28	.0046	.109	.484	14.88	1.06e-5	.00026	.3245	.05837

Table-5.5: Results for estimated values of breakdown voltages, V_{BPT} and V_{BAV} for different values of N_0 and m

N_0 (per cc)	N_{eff} (per cc)	$mx10^{-4}$ (cm)	V_{BPT} (V)	E_C (V)	V_{BAV} (V)
10^{18}	$3.12x10^{15}$	1	16kV	$2.09x10^{6}$	16.31kV
10^{19}	$2.69x10^{16}$	1	10kV	$2.77x10^{6}$	9.927kV
10^{19}	$2.69x10^{17}$	10	7kV	$3.74x10^{6}$	6.96kV
$4x10^{18}$	$1.42x10^{18}$	10	3kV	$4.66x10^{6}$	3.21kV

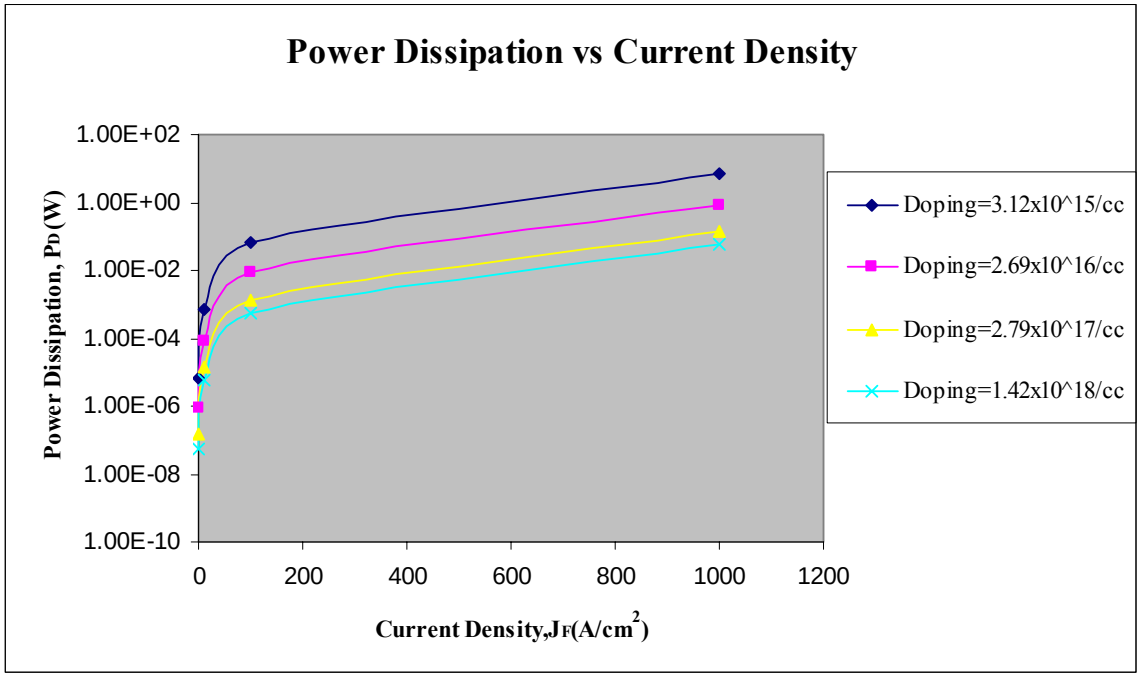

Figure-5.2: Plot of Forward Current Density vs. Forward Voltage Drop for a 6H-SiC DIMOSFET for different values of effective drift region doping levels (N_{eff}) for Gaussian Profile

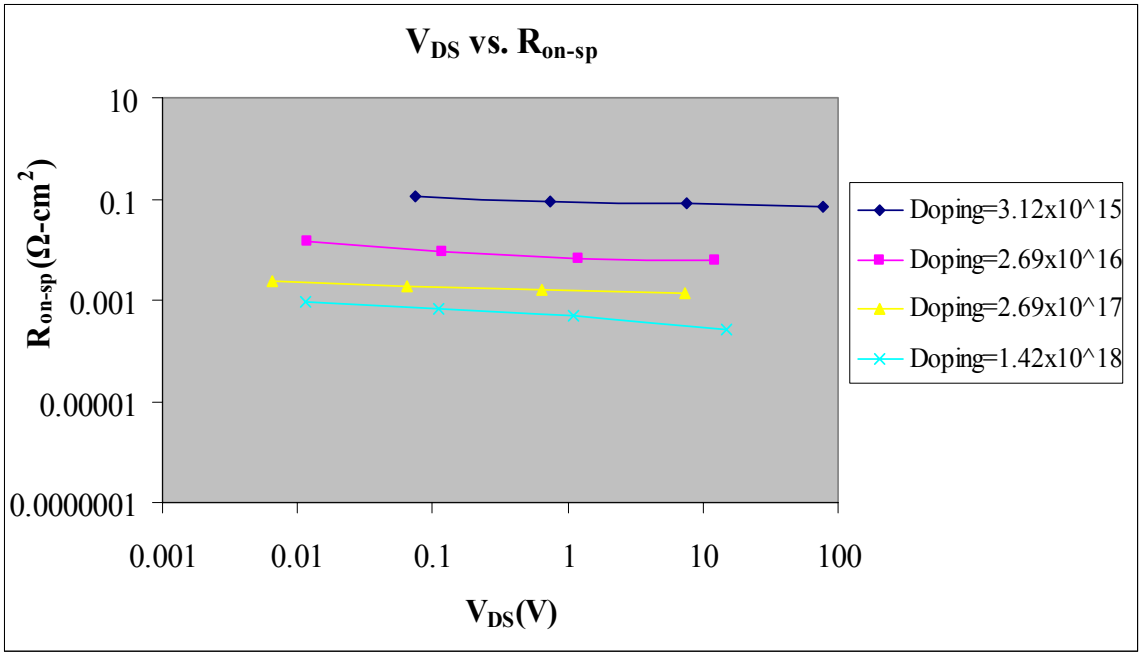

Figure-5.3: Plot of Drain Voltage vs. Specific on Resistance for a 6H-SiC DIMOSFET for different values of effective drift region doping levels (N_{eff}) for Gaussian Profile

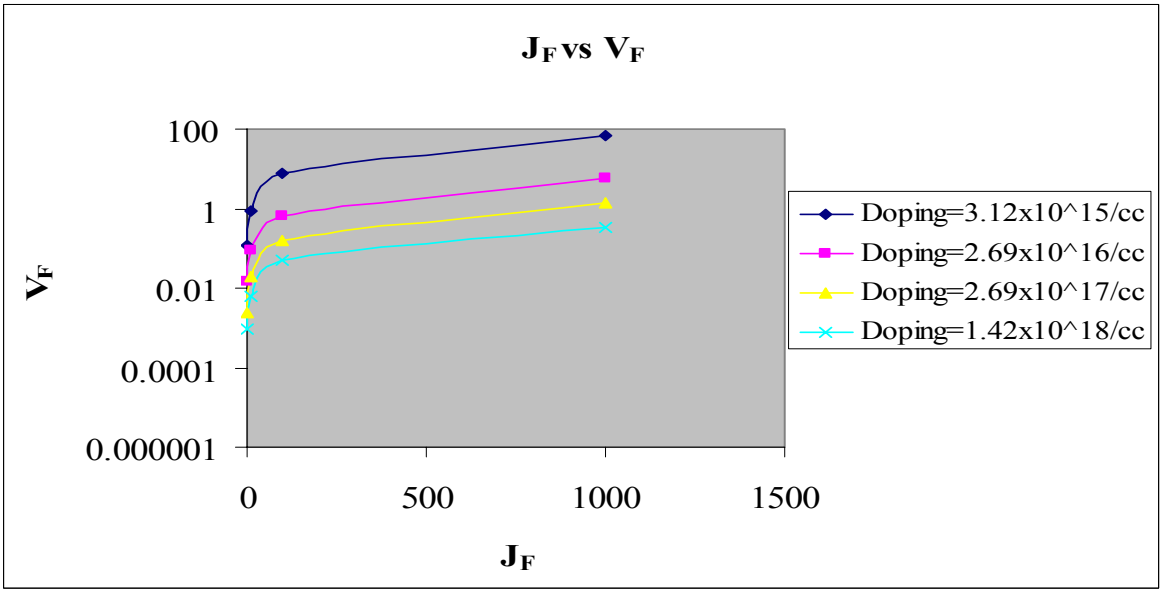

Figure-5.4: Plot of Forward Current Density vs. Forward Voltage Drop for a 6H-SiC DIMOSFET for different values of effective drift region doping levels (N_{eff}) for Gaussian Profile

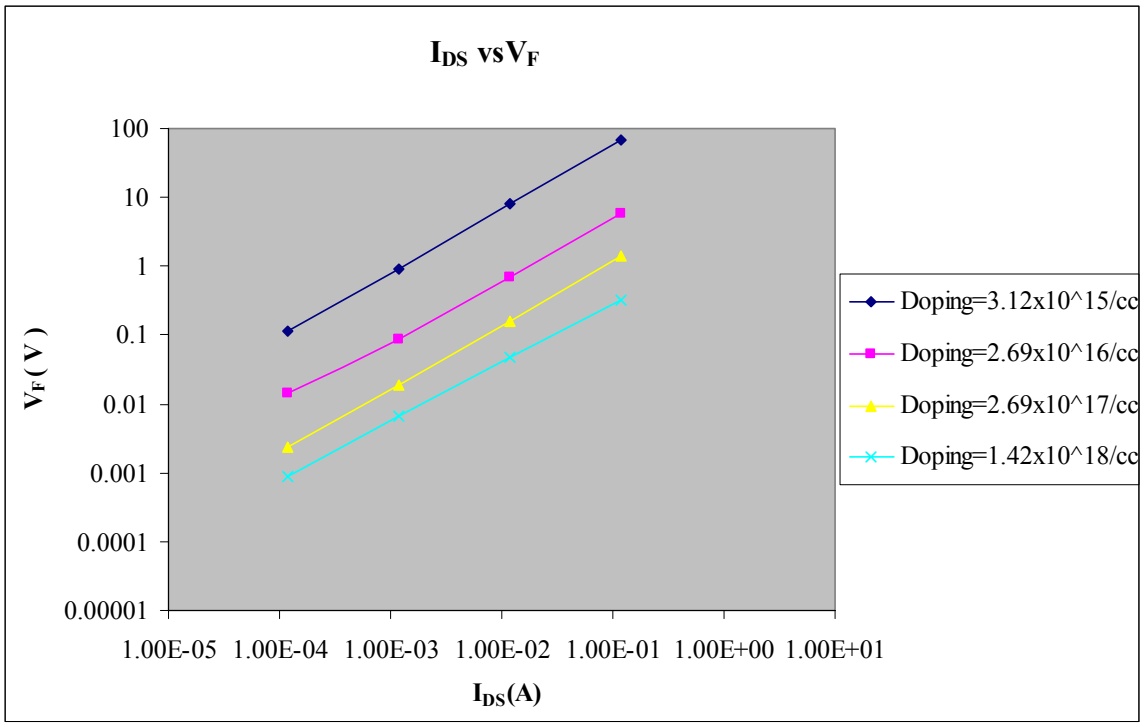

Figure-5.5: Plot of Drain Current vs. Forward Voltage Drop for a 6H-SiC DIMOSFET for different values of effective drift region doping levels (N_{eff}) for Gaussian Profile

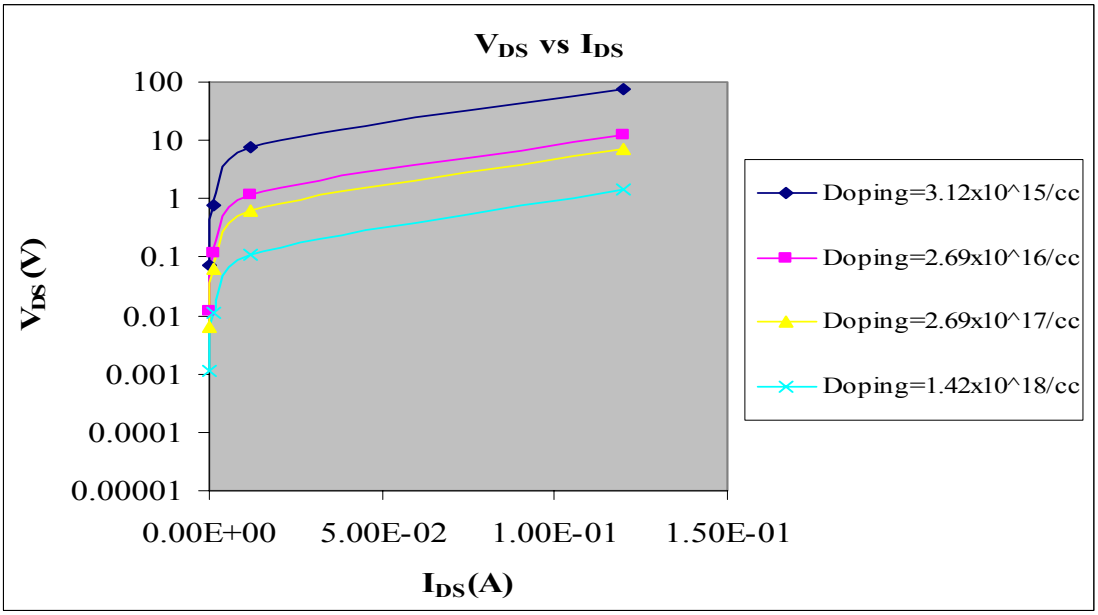

Figure-5.6: Plot of Drain Current vs. Drain to source Voltage for a 6H-SiC DIMOSFET for different values of effective drift region doping levels (N_{eff}) for Gaussian Profile

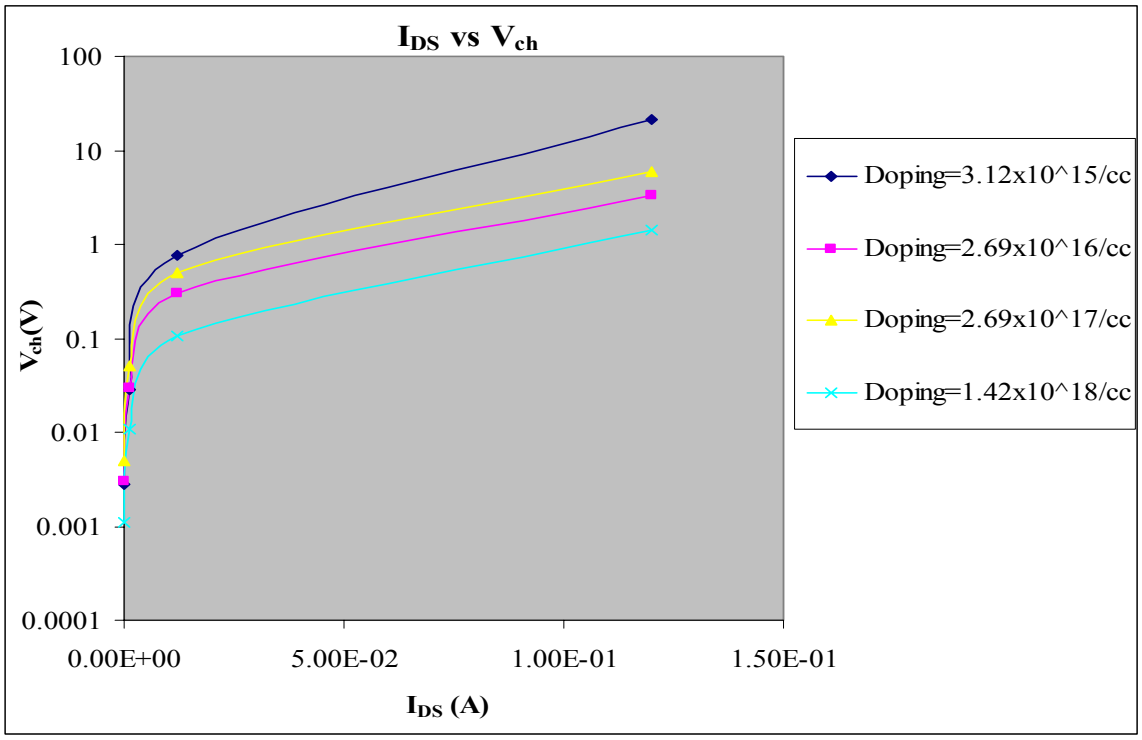

Figure-5.7: Plot of Drain Current vs. Channel Voltage for a 6H-SiC DIMOSFET for different values of effective drift region doping levels (N_{eff}) for Gaussian Profile

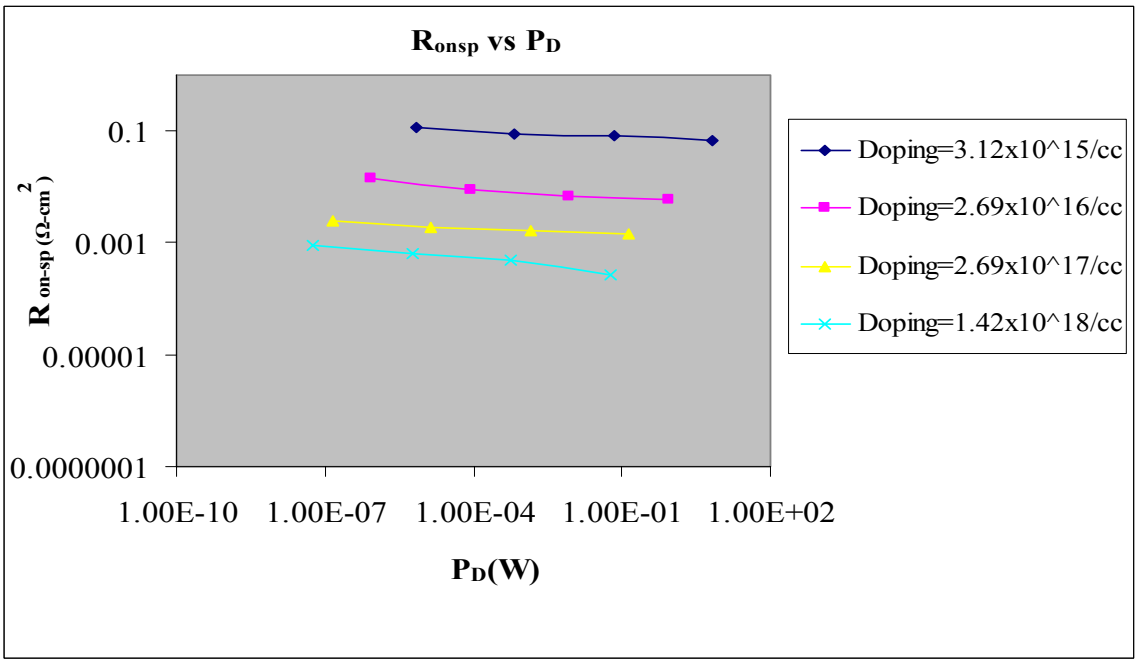

Figure-5.8: Plot of Power Dissipation vs. Specific-on-resistance for a 6H-SiC DIMOSFET for different values of effective drift region doping levels (N_{eff}) for Gaussian Profile

In conclusion it can be said that an increase in the value of m at a fixed value of N_0 decreases the breakdown voltage. At low values of m, a decrease in N_0 results in an increase in breakdown voltage, whereas opposite will hold for high values of m.

CHAPTER 6

ANALYSIS AND DESIGN OF 6H-DIMOSFET USING COMPLEMENTARY ERROR FUNCTION DRIFT REGION PROFILE

This chapter analyses the device structure of the vertical 6H-SiC DIMOSFET with Complementary Error Function doping profile in the drift region. After the calculations of depletion width and effective doping concentration, the drain voltages, breakdown voltages and power dissipations were evaluated at different values of current density. The results had been analysed from the nature of variation of these parameters for various values of current density. The current density vs. power dissipation for different Gaussian profiles and Complementary Error Function profiles as well as percentage reduction in power dissipation vs. different doping concentrations at various current densities were plotted. The results of Gaussian profile were compared with those of Complementary Error Function profiles. After comparing the results, it was found that power dissipation in Gaussian Profile is less 20 to 66% less than that obtained in the complementary error function profile at a current density of 1000A/cm^2 which was taken as a standard value for this analysis with an estimated breakdown voltage of 20 kV.

6.1 INTRODUCTION

The analysis of the 6H-SiC DIMOSFET with a complementary error function impurity doping profile in the drift region needs to be considered in order to study the salient features of this profile and its effect on two main quantities, namely the power

dissipation (P_D) and the breakdown voltages i.e. V_{BAV} and V_{BPT} as analysed in the case of linearly graded impurity profile and the Gaussian profile in the drift region given in chapters 4 and 5 respectively. The complementary error function profile, may in certain cases considered here, be considered as a nearly linear graded profile. However, a somewhat non-linear approach has been analysed for deriving the expression for the depletion region width W, similar to what was done in the case of Gaussian distribution analysed in chapter 5.

The calculation of power dissipation (P_D) was done by using the equation for the effective carrier concentration derived in the theory to calculate N_{eff} and values of voltages V_{ch}, V_A,V_B, and V_C, R_{on-sp} for various levels of current density were calculated.

The maximum reverse voltage required to obtain a predetermined depletion region width which had been set equal to 350μm as has been considered in Chapter 5 was used to obtain the punch through breakdown voltage, V_{BPT} where as the avalanche breakdown voltage, V_{BAV} was estimated using the equation for critical field E_C used for linearly graded profile (because of its similarity with complementary error function profile) in Chapter 4 and the equation $V_{BAV}=(2/3)\ E_C W^{/}$, the magnitude of $W^{/}$ being dependant on the peak impurity concentration, N_0 near the drain and applied reverse bias, V_R.

6.2 THEORETICAL ANALYSIS:

6.2.1 The Device Height 'h'

This was kept at 350μm in order to compare power dissipation values at different current levels with those obtained for Gaussian distribution.

6.2.2 The Depletion Region Width (W)

The device structure of the 6H-SiC DIMOSFET with its complementary error function (erfc) doping profile with a device height "h" is shown in Figure-6.1.

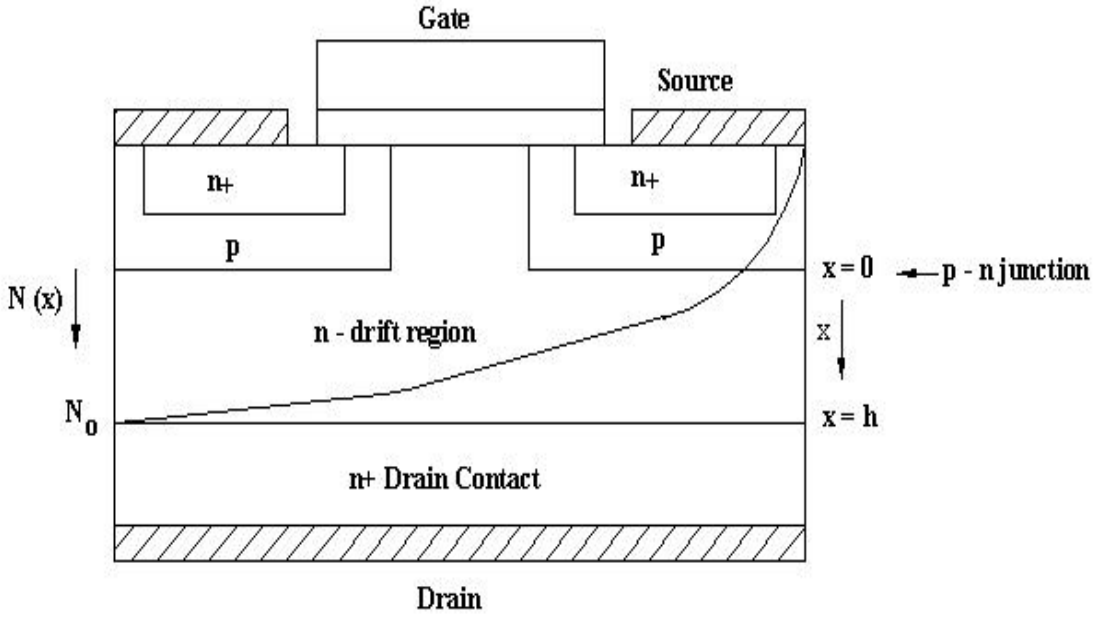

Figure-6.1:Cross-sectional structure of DIMOSFET showing Complementary Error Function profile in the drift region

The peak carrier concentration N_0 is located near the drain and decreases upwards as on moves towards the source. The equation to the erfc doping profile can be written as

$$N(x)=N_0\text{erfc}(h-x)=N_0[1-\text{erf}(h-x)] \quad (6.1)$$

where erf(h-x) is the error function and can be expressed as:

$$\text{erf}(h-x)=\frac{2}{\sqrt{\pi}}\left[(h-x)-\frac{1}{3}(h-x)^3+\frac{1}{2!}\frac{1}{5}(h-x)^5-.....\right] \quad (6.2)$$

Since (h-x)<1 and retaining first two terms of eq.(6.2) gives

$$\text{erf}(h-x)=\frac{2}{\sqrt{\pi}}\left[(h-x)-\frac{1}{3}(h-x)^3\right] \quad (6.3)$$

Hence, the equation for the erfc doping profile given in eq. (6.1) becomes:

$$N(x) = N_0\left[1 - \frac{2}{\sqrt{\pi}}\left\{(h-x) - \frac{1}{3}(h-x)^3\right\}\right] \tag{6.4}$$

The Poisson's equation for the system then becomes

$$-\frac{\partial^2 V}{\partial x^2} = \frac{eN_0}{\varepsilon_s}\left[1 - \frac{2}{\sqrt{\pi}}\left\{(h-x) - \frac{(h-x)^3}{3}\right\}\right] \tag{6.5}$$

Integrating eqn.(6.5) w.r.t x once gives,

$$E = -\frac{\partial V}{\partial x} = \frac{eN_0}{\varepsilon_s}\left[x - \frac{2}{3\sqrt{\pi}}\left\{3hx - \frac{3}{2}x^2 - h^3x + \frac{x^4}{4} - x^3h + \frac{3}{2}h^2x^2\right\}\right] + C \tag{6.6}$$

At x=0, E=-E_m , so C=-E_m

$$E = -\frac{\partial V}{\partial x} = \frac{eN_0}{\varepsilon_s}\left[x - \frac{2}{3\sqrt{\pi}}\left\{3hx - \frac{3}{2}x^2 - h^3x + \frac{x^4}{4} - x^3h + \frac{3}{2}h^2x^2\right\}\right] - E_m \tag{6.7}$$

Again at x=h, E=0 gives

$$E_m = \frac{eN_0}{\varepsilon_s}\left[h - \frac{2}{3\sqrt{\pi}}\left\{\frac{3}{2}h^2 - \frac{h^4}{4}\right\}\right] \tag{6.8}$$

Combining eqn.(6.7) and (6.8) gives

$$\begin{aligned} E = -\frac{\partial V}{\partial x} &= \frac{eN_0}{\varepsilon_s}\left[x - \frac{2}{3\sqrt{\pi}}\left\{3hx - \frac{3}{2}x^2 - h^3x + \frac{x^4}{4} - x^3h + \frac{3}{2}h^2x^2\right\}\right] \\ &- \frac{eN_0}{\varepsilon_s}\left[h - \frac{2}{3\sqrt{\pi}}\left\{\frac{3}{2}h^2 - \frac{h^4}{4}\right\}\right] \end{aligned} \tag{6.9}$$

or

$$E = \frac{eN_0}{\varepsilon_s}\left[(x-h) - \frac{2}{3\sqrt{\pi}}\left\{3hx - \frac{3}{2}x^2 - h^3x + \frac{x^4}{4} - x^3h + \frac{3}{2}h^2x^2 - \frac{3}{2}h^2 - \frac{h^4}{4}\right\}\right] \tag{6.9}$$

Integrating once again gives the potential V(x) as:

$$-V(x)=\frac{eN_0}{\varepsilon_s}\left[\left(\frac{x^2}{2}-hx\right)-\frac{2}{3\sqrt{\pi}}\left\{\begin{array}{l}\frac{3hx^2}{2}-\frac{1}{2}x^3-\frac{1}{2}h^3x^2+\frac{x^5}{20}-\frac{1}{4}x^4h\\+\frac{1}{2}h^2x^3-\frac{3}{2}h^2x-\frac{h^4x}{4}\end{array}\right\}\right]+C' \qquad (6.10)$$

where $C^{/}$ is a constant of integration.

At x=0, V=0 and $C^{/}$=0.

Hence,

$$-V(x)=\frac{eN_0}{\varepsilon_s}\left[\left(\frac{x^2}{2}-hx\right)-\frac{2}{3\sqrt{\pi}}\left\{\begin{array}{l}\frac{3hx^2}{2}-\frac{1}{2}x^3-\frac{1}{2}h^3x^2+\frac{x^5}{20}-\frac{1}{4}x^4h\\+\frac{1}{2}h^2x^3-\frac{3}{2}h^2x-\frac{h^4x}{4}\end{array}\right\}\right] \qquad (6.11)$$

At x=W, V=-(V_R+V_{bi}), where V_R is the applied reverse bias and V_{bi} is the built-in potential. Since V_{bi}<< V_R, V=-(V_R), eq.(6.11) then becomes

$$-V_R=\frac{eN_0}{\varepsilon_s}\left[\left(\frac{W^2}{2}-hW\right)-\frac{2}{3\sqrt{\pi}}\left\{\begin{array}{l}\frac{3hW^2}{2}-\frac{1}{2}W^3-\frac{1}{2}h^3W^2+\frac{W^5}{20}-\frac{1}{4}W^4h\\+\frac{1}{2}h^2W^3-\frac{3}{2}h^2W-\frac{h^4W}{4}\end{array}\right\}\right] \qquad (6.12)$$

$$\begin{aligned}-\frac{\varepsilon_s V_R}{eN_0}&=-\frac{W^5}{30\sqrt{\pi}}+\frac{1}{6\sqrt{\pi}}W^4h+\left[\frac{1}{3\sqrt{\pi}}-\frac{1}{3\sqrt{\pi}}h^2\right]W^3\\&+\left[\frac{1}{2}-\frac{1}{\sqrt{\pi}}h+\frac{1}{3\sqrt{\pi}}h^3\right]W^2+\left[-h+\frac{1}{\sqrt{\pi}}h^2-\frac{h^4}{6\sqrt{\pi}}\right]W\end{aligned} \qquad (6.13)$$

which finally gives

$$\begin{aligned}&\frac{W^5}{30\sqrt{\pi}}-\frac{1}{6\sqrt{\pi}}W^4h-\left[\frac{1}{3\sqrt{\pi}}-\frac{1}{3\sqrt{\pi}}h^2\right]W^3\\&-\left[\frac{1}{2}-\frac{1}{\sqrt{\pi}}h+\frac{1}{3\sqrt{\pi}}h^3\right]W^2-\left[-h+\frac{1}{\sqrt{\pi}}h^2-\frac{h^4}{6\sqrt{\pi}}\right]W-\frac{\varepsilon_s V_R}{eN_0}=0\end{aligned} \qquad (6.14)$$

eq. (6.14) was used to evaluate the magnitude of depletion region width, W for different values of applied reverse voltages, V_R.

6.2.3 The Effective Concentration (N_{eff}) of the Drift Region:

The effective concentration of the drift region was evaluated using the erfc impurity concentration profile given in eq.(6.4). Considering a volume element of thickness dx as in the case of linearly graded profile and integrating from x=0 to h, gives the total impurity concentration.

$$N_T = \int_0^h AN(x)dx = \int_0^h A.N_0\left[1 - \frac{2}{\sqrt{\pi}}\left\{(h-x) - \frac{1}{3}(h-x)^3\right\}\right]dx, \qquad (6.15)$$

where A is the device cross-sectional area.

Eq.(6.15) gives upon integration:

$$N_T = A.N_0.\frac{2}{\sqrt{\pi}}\left[\frac{\sqrt{\pi}}{2}h - \frac{h^2}{2} + \frac{h^4}{12}\right] \qquad (6.16)$$

Hence, the effective carrier concentration of the drift region can be obtained by dividing eq.(6.16) by the total volume i.e. Ah:

$$N_{eff} = \frac{N_T}{Ah} = \frac{2N_0}{\sqrt{\pi}}\left(\frac{\sqrt{\pi}}{2} - \frac{h}{2}\right) \qquad (6.17)$$

where the terms in h^3 has been neglected as h<1. Eq.(6.17) was used to calculate the effective carrier concentration, N_{eff} of the drift region knowing the value of N_0.

6.2.4 BREAKDOWN VOLTAGES (V_{BPT} and V_{BAV})

Since the complementary error function profile is to a first approximation a linearly graded profile [see eq.(6.4)], the equation for calculating avalanche breakdown voltage (V_{BAV}) which was used for linearly graded junctions in Chapter 4 were used here as well. The values of concentration gradients (α) for various erfc profiles used were evaluated alongwith the depletion region width ($W^{/}$) and V_{BAV} were calculated using the equation:

$$V_{BAV} = \frac{2}{3} E_C W', \tag{6.18}$$

where the critical field E_c is given by:

$$E_c = \left(\frac{e\alpha W'^2}{8\varepsilon_s} \right) \tag{6.19}$$

has been used

The magnitude of E_c may also be evaluated by the following equation

$$E_c = 1.95x10^4 \, x N_{eff}^{.131} \tag{6.20}$$

where N_{eff} is the effective concentration of the drift region given the eq.(6.17). The equation for concentration gradient α was obtained by differentiating eq. (6.4) with respect to x and neglecting terms in $(h-x)^3$ and higher gives

$$\alpha = \frac{2N_0}{\sqrt{\pi}}. \tag{6.21}$$

The punch through breakdown voltage, V_{BPT} was evaluated by using the maximum value of W obtained from eq. (6.14).

6.2.5 THE POWER DISSIPATION (P_D)

The value of power dissipation P_D for 50% duty cycle was calculated using the same equation was used in previous chapters for R_{on-sp} at a current density of J_{on} and a given depletion region width, W_d.

$$P_D=(1/2)(J_{on}^2.R_{on-sp}.A) \tag{6.22}$$

The magnitude of voltages $V_{ch,}$ $V_{A,}V_B$, V_C, V_F and V_{DS} at different current levels were calculated using eqns. in the previous chapters for various erfc profiles.

6.3 CALCULATION AND RELATED GRAPHS

The device dimensions used are the same as those in chapter 4 except that the device height h had been set at 350 μm for comparison of results with those obtained for Gaussian distribution. The magnitude of N_{eff} have been evaluated for various peak concentrations, N_0 using eq. (6.17). Current density values of J_{on} equal to J_F at levels of 1, 10,100 and 1000 amperes per cm^2 were used for calculating values of voltages Vch, V_A, V_B and V_C. The voltage V_{DS} which is the sum total of these voltages was then estimated. The value of R_{on-sp} and power dissipation P_D for various values of current density J_F were then calculated. The results are shown in Tables 6.1 to 6.4. The variation of power dissipation (P_D) with current density for different values of N_{eff} is shown in Figure-6.2. The variation of R_{on-sp} with V_{DS} is shown in Figure-6.3 for different values of $N_{eff.}$ A comparative graphical plot for Gaussian and Complementary Error Function profiles for variation of power dissipation with current density is shown in Figure- 6.9.

6.3.1 The Breakdown Voltages (V_{BPT} and V_{BAV})

The values of V_{BPT} was estimated by increasing the magnitude of V in eq.(6.14) and finding out the maximum value of N_{eff} for a given value of N_0 and α. The corresponding avalanche breakdown voltages, V_{BAV} was calculated using equation (6.18) and (6.19). The results are shown in Table 6.5.

6.4 RESULTS AND DISCUSSION

Power Dissipation: An analysis of results shown in Tables 6.1 to 6.4 showed that the effective or overall concentration of the medium, i.e. N_{eff} was almost equal to the peak concentration N_0 of the error function profile. This can be verified from Table 6.1 in

which an N_0 of 10^{15} per cc gives an N_{eff} of $9.8x10^{14}$ per cc of doping level in the drift region. In other words, the concentration gradient α in the profiles used here is quite small over the device height h of 350μm.

The channel voltage, V_{ch} increases with increase in current density, J_f from 1 to 1000 amperes per cm^2 by a factor of 1000 as do all other voltages V_A, V_B, V_C and V_{DS}. All these voltages were again found to decrease with increase in the magnitude of all erfc profiles ranging from $N_0=10^{15}$ per cc to $N_0=10^{18}$ per cc. Correspondingly specific on resistance R_{on-sp} decreased and so did the forward drop, V_f. The power dissipation, P_D was found to decrease for erfc profile with $N_0=10^{15}$ per cc from 18.37 W at a current density of 1000 amperes per cm^2 to 0.073W for the profile with $N_0=10^{18}$ per cc. Hence, increasing the magnitude of N_0 results in decreasing the value of P_D as the effective carrier concentration, N_{eff} increases with increasing N_0, thereby decreasing the specific on resistance R_{on-sp} of the drift region. The corresponding values of depletion region width W_d as shown in tables 6.1 to 6.4 show a decline in magnitude with increasing values of J_f and V_{DS}. The variation of power dissipation P_D with current density for different values of N_{eff}, both for the Gaussian profile obtained in Chapter 5 and the erfc distribution is shown in Figure- 6.9. It was seen that all Gaussian profiles exhibited a lower level of power dissipation at all current levels as compared to similar erfc profile.

6.4.1 The Breakdown Voltages (V_{BPT} and V_{BAV})

The calculated values of punch through breakdown voltage, V_{BPT} and V_{BAV} are shown in Table 6.5. It was found that with decrease in magnitude of concentration gradient α, the depletion width increases and so does the breakdown voltage. The critical field E_c, however decreases from$4.52x10^6$ V/cm to $1.81x10^6$ V/cm over the range of values of α

considered here. The magnitude of V_{BAV} and V_{BPT} are found to be approximately equal for all values of α. The highest attainable value of breakdown voltage is 20 kV for $\alpha=1.13x10^{15}$ cm^{-4}. The depletion region width W reaches a maximum of 168μm at a breakdown voltage of 20kV. The magnitude of W declines gradually to 167 μm for voltages exceeding 20 kV meaning that breakdown voltages higher than 20kV for $\alpha=1.13x10^{15}$ cm^{-4} are not possible and carrier injection may have started from the drain end into the drift region. This is shown in Table 6.6.

Table-6.1: Results of currents, voltages, R_{on-sp} and power dissipation for $N_0=10^{15}$ per cc, $h=350x10^{-4}$cm, $N_{eff}=9.8x10^{14}$/cc, $\mu=530cm^2$/V-sec

J_F (A/cm^2)	I (A)	V_{ch} (V)	V_A (V)	V_B (V)	V_C (V)	$V_{DS}=V_A+V_B+V_C+V_{ch}$ (V)	W_d (cm)	R_{on-sp} (Ω-cm^2)	V_f (V)	P_D (W)
1	12e-5	.0028	.0020	.0363	.160	.2014	4.38e-5	.3207	.3207	1.92e-5
10	12e-4	.028	.0333	.363	1.60	2.02	1.39e-4	.2961	2.9614	.0019
100	12e-3	.283	.332	3.63	15.83	20.49	4.41e-4	.2707	27.0685	.1899
1000	12e-2	3.16	3.103	36.47	153.71	214.37	.0014	.2518	251.0759	18.3711

Table-6.2: Results of currents, voltages, R_{on-sp} and power dissipation for $N_0=10^{16}$ per cc, $h=350x10^{-4}$cm, $N_{eff}=9.8x10^{15}$/cc, $\mu=500cm^2$/V-sec

J_F (A/cm^2)	I (A)	V_{ch} (V)	V_A (V)	V_B (V)	V_C (V)	$V_{DS}=V_A+V_B+V_C+V_{ch}$ (V)	W_d (cm)	R_{on-sp} (Ω-cm^2)	V_f (V)	P_D (W)
1	12e-5	.003	1.55e-4	.0039	.017	.024	4.78e-6	.0340	.0340	2.04e-6
10	12e-4	.029	.0017	.0385	.170	.239	1.51e-5	.03079	.340	2.04e-4
100	12e-3	.3	.0218	.385	1.70	2.41	4.78e-5	.02795	3.399	.0204
1000	12e-2	3.37	.2134	3.85	16.94	24.53	1.53e-4	.02486	23.854	2.03

Table-6.3: Results of currents, voltages, R_{on-sp} and power dissipation for $N_0=10^{17}$per cc, $h=350x10^{-4}$cm, $N_{eff}=9.8\ x10^{16}$/cc, $\mu=300cm^2$/V-sec

J_F (A/cm^2)	I (A)	V_{ch} (V)	V_A (V)	V_B (V)	V_C (V)	$V_{DS}=V_A+V_B+V_C+V_{ch}$ (V)	W_d (cm)	R_{on-sp} (Ω-cm^2)	V_f (V)	P_D (W)
1	12e-5	.0050	2.48e-5	6.41e-4	.0028	.0085	8.99e-7	.0057	.0057	3.47e-7
10	12e-4	.050	2.52e-4	.0064	.0284	.085	2.84e-6	.0051	.00508	3.4e-5
100	12e-3	.5	.0027	.064	.284	.85	8.99e-6	.0048	.00479	.0034
1000	12e-2	5.82	.025	.641	2.859	9.32	2.98e-5	.0045	.00448	.3401

Table-6.4: Results of currents, voltages, R_{on-sp} and power dissipation for $N_0=10^{18}$ per cc, $h=350x10^{-4}$cm, $N_{eff}=9.8x10^{17}$/cc, $\mu=140cm^2$/V-sec

J_F (A/cm^2)	I (A)	V_{ch} (V)	V_A (V)	V_B (V)	V_C (V)	$V_{DS}=V_A+V_B+V_C+V_{ch}$ (V)	W_d (cm)	R_{on-sp} (Ω-cm^2)	V_f (V)	P_D (W)
1	12e-5	.0011	5.29e-6	1.37e-4	6.08e-4	.0118	3.34e-7	.0012	.0012	7.3e-8
10	12e-4	.011	5.32e-5	.0014	.0061	.118	1.06e-6	.0004	.00421	7.3e-6
100	12e-3	.108	5.44e-4	.014	.061	1.16	3.31e-6	.0003	.0334	7.3e-4
1000	12e-2	1.428	.0059	.137	.608	15.31	1.2e-5	.00049	.4876	.073

Table-6.5: Values for Breakdown Voltages (V_{BPT} and V_{BAV}) for the various values of concentration gradients α for the profiles in the drift region of 6H-SiC DIMOSFET

Grad 'α' cm^{-4}	W (μm)	E_C (V/cm)	$V_{BAV}=(2/3)(E_cW)$ (V)	V_{BPT} (V)
$1.13x10^{15}$	168	$1.81x10^6$	20.274kV	20 kV
$1.13x10^{16}$	98	$2.47x10^6$	16.14 kV	16.00kV
$1.13x10^{17}$	50	$3.34x10^6$	11.08 kV	11kV
$1.13x10^{18}$	20.41	$4.52 x10^6$	6.15kV	6.00kV

Table-6.6: Depletion Width calculations for Complementary Error Function Profile in the drift region of 6H-SiC DIMOSFET for the voltages greater than 20kV

Sr.No.	Voltage (V)	Depletion Region Width (µm)
1.	20k	168.21
2.	21k	167.93
3.	24k	167.72
4.	25k	167.61
5.	26k	167.53
6.	28k	167.49
7.	30k	167.48

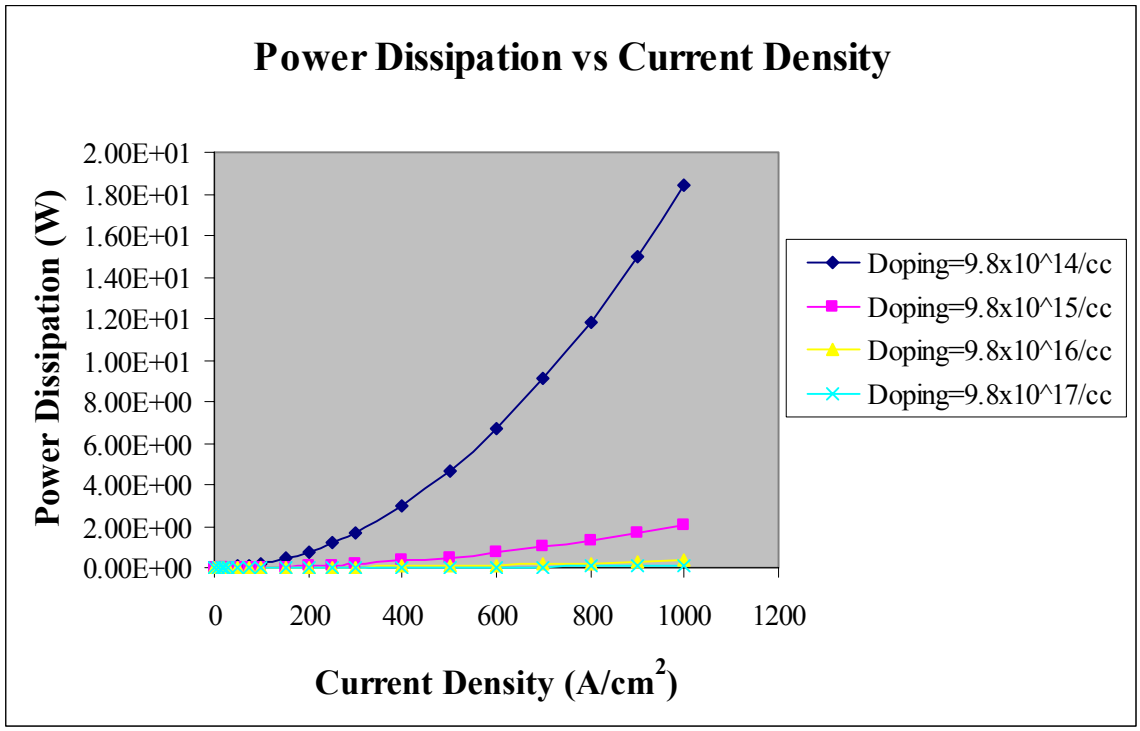

Figure-6.2: Plot of Power Dissipation vs. Current Density for a 6H-SiC DIMOSFET For different values of effective drift region doping levels (Neff) for Complementary Error Function profile

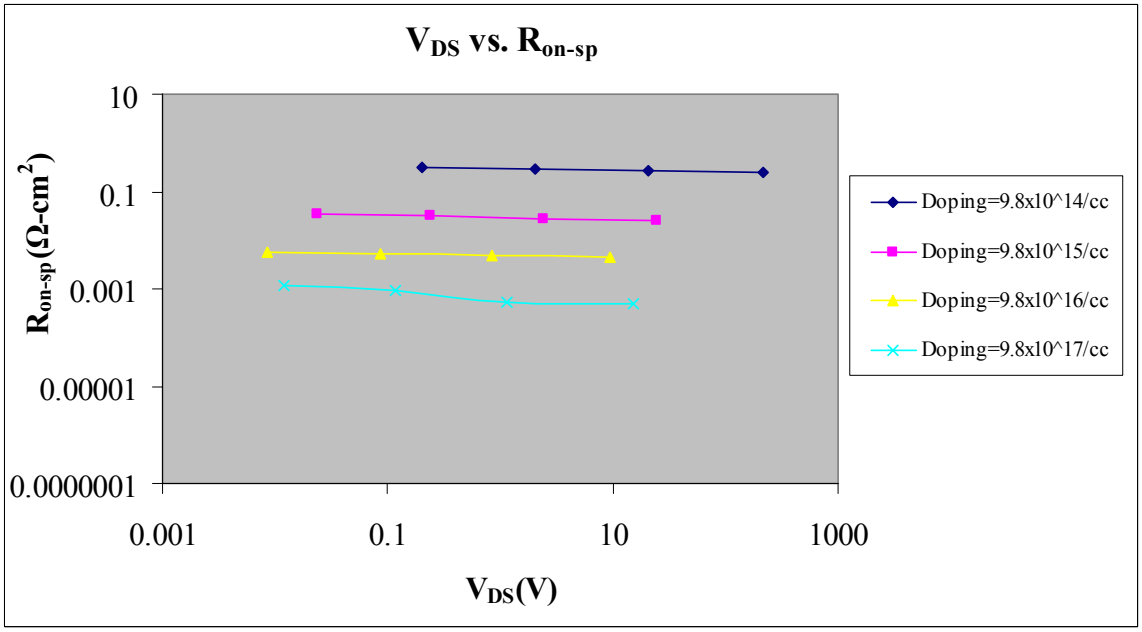

Figure-6.3: Plot of Drain Voltage vs. Specific on Resistance for a 6H-SiC DIMOSFET for different values of effective drift region doping levels (N_{eff}) for Complementary Error Function profile

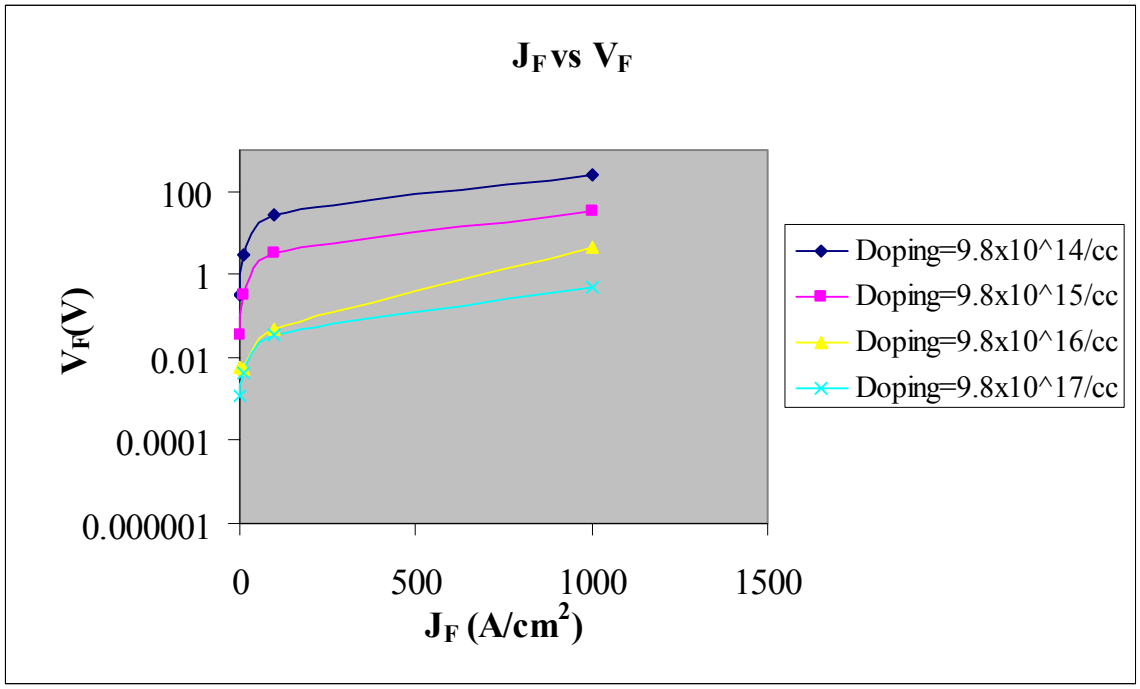

Figure-6.4: Plot of Forward Current Density vs. Forward Voltage Drop for a 6H-SiC DIMOSFET for different values of effective drift region doping levels (N_{eff}) for Complementary Error Function profile

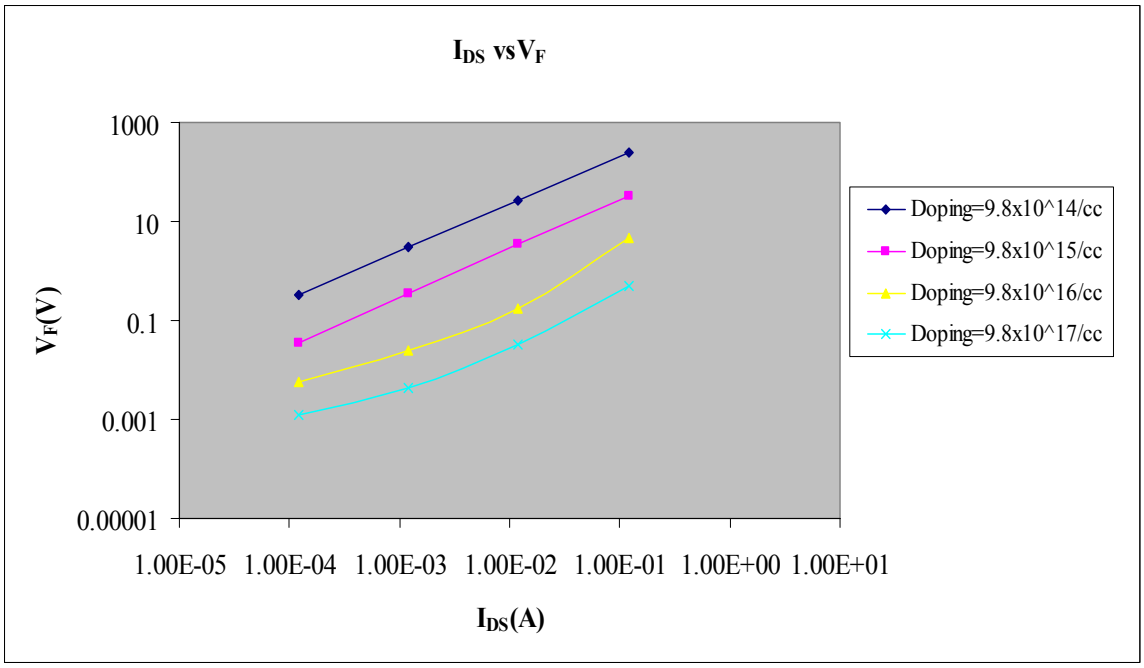

Figure-6.5: Plot of Drain Current vs. Forward Voltage Drop for a 6H-SiC DIMOSFET for different values of effective drift region doping levels (N_{eff}) for Complementary Error Function profile

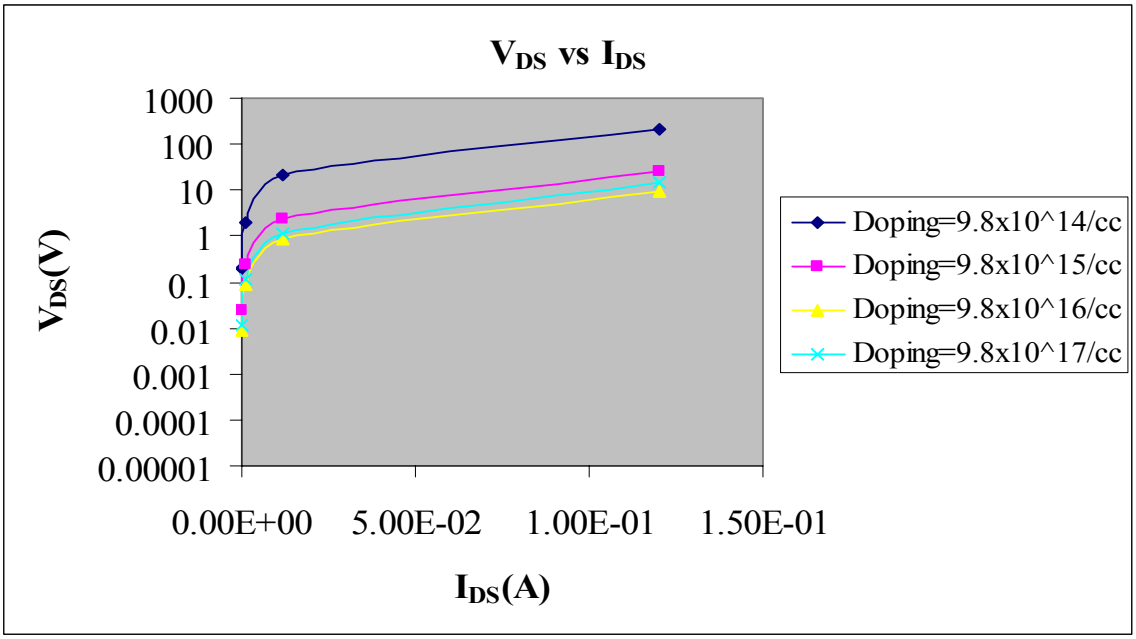

Figure-6.6: Plot of Drain Current vs. Drain to source Voltage for a 6H-SiC DIMOSFET for different values of effective drift region doping levels (N_{eff}) for Complementary Error Function profile

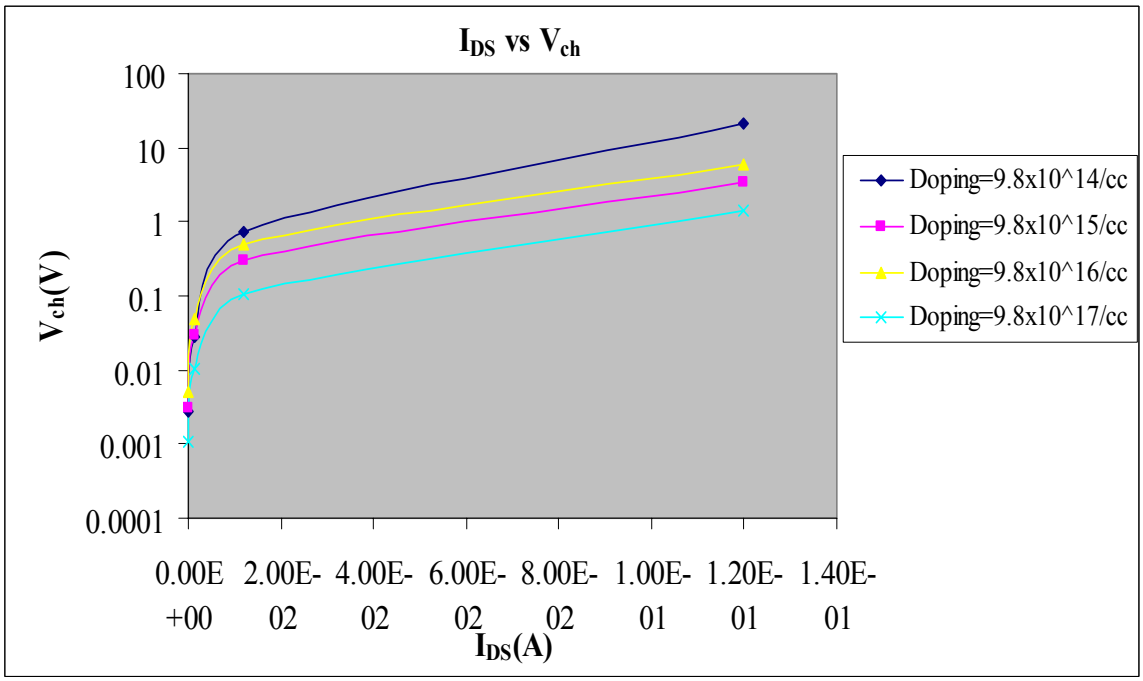

Figure-6.7: Plot of Drain Current vs. Channel Voltage for a 6H-SiC DIMOSFET for various values of drift region doping levels (N_B) for Complementary Error Function Profile

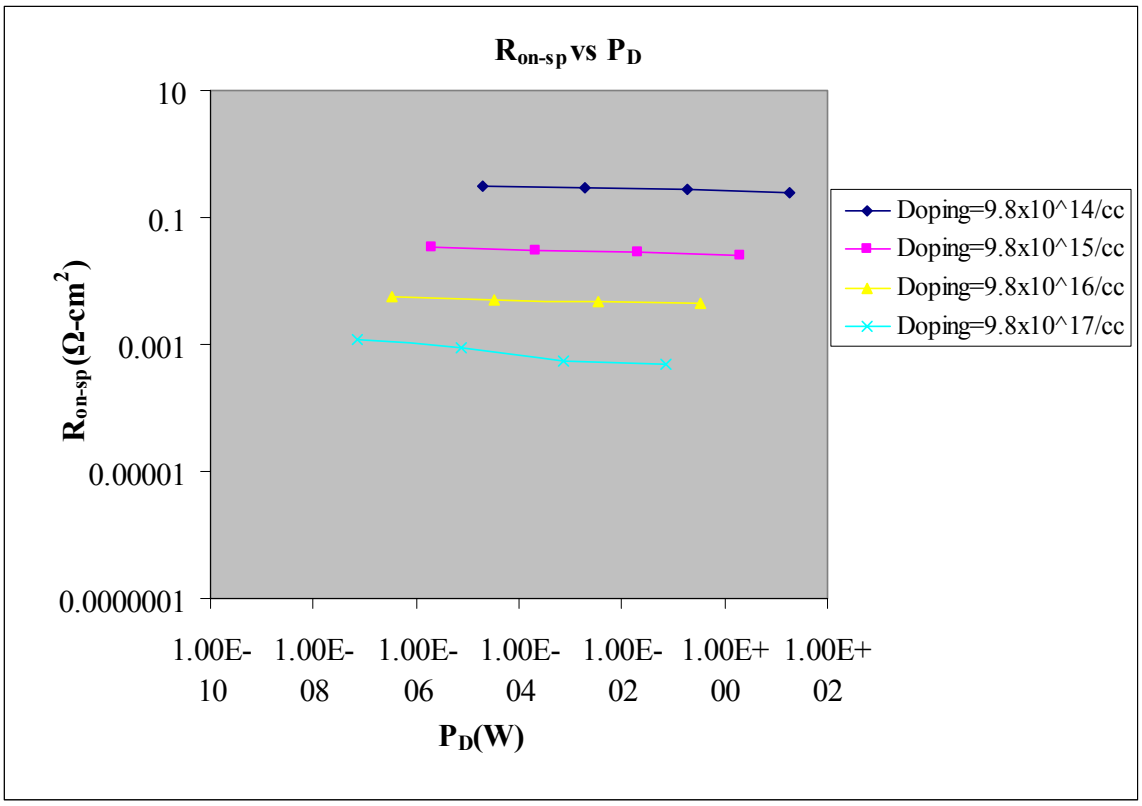

Figure-6.8: Plot of Power Dissipation vs. Specific-on-resistance for a 6H-SiC DIMOSFET for various valuesdrift region doping levels (N_B) for Complementary Error Function Profile

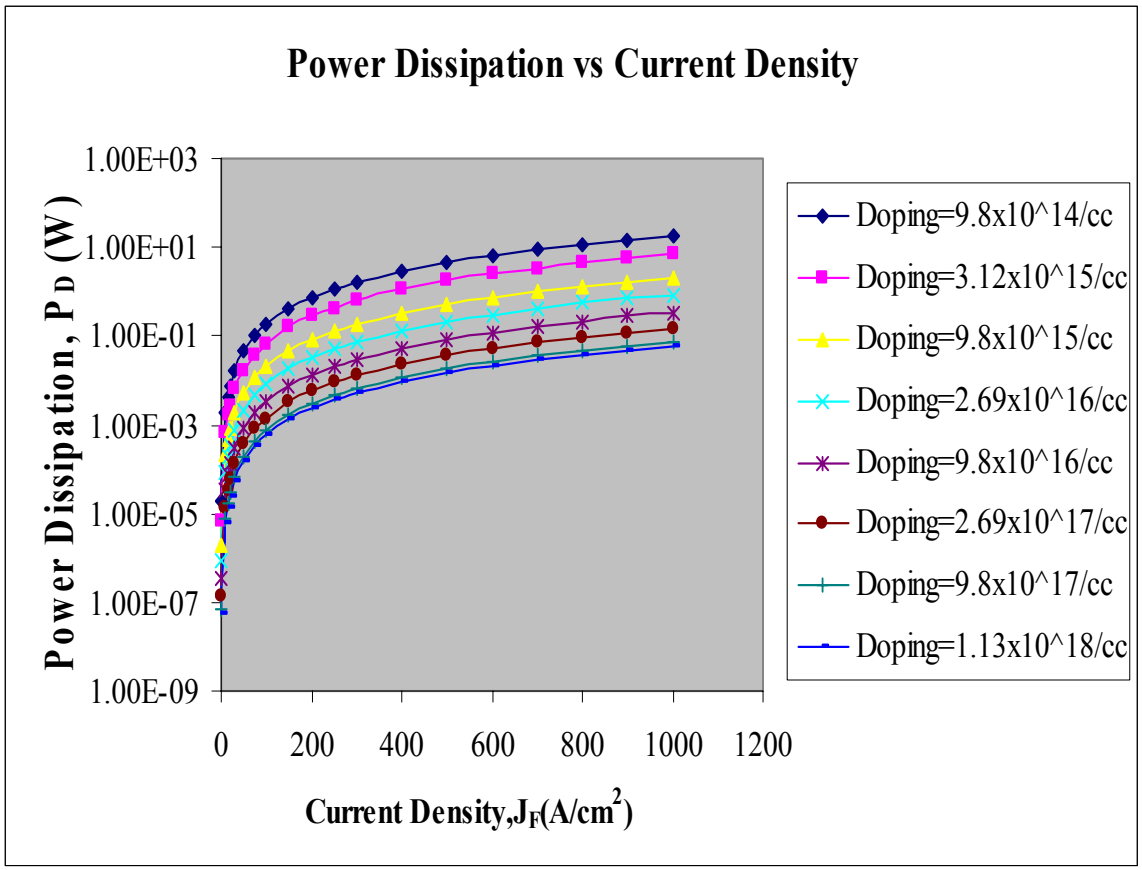

Figure-6.9: Plot of Power Dissipation vs. Current Density for a 6H-SiC DIMOSFET for different values of drift region doping levels (N_{eff}) for Gaussian and Complementary Error Function Profile

CHAPTER 7

CONCLUSIONS AND SCOPE OF FUTURE WORK

Substantial amount of work on 6H-SiC DIMOSFET's has already been done by a large number of researchers over the last two decades. The present work has presented certain details which can help to reduce the power dissipation and increase the breakdown voltages of these devices.

The results quoted in chapter 2 are merely an analytical finding based on existing theoretical device equations and lead one to obtain the optimum doping level of the drift region lying between $5x10^{13}$ per cc to $5x10^{15}$ per cc with breakdown voltage going upto about 10kV. This analysis also ensures a lower power dissipation going upto 800W for a rise in temperature of 600˚C and can ensure stable device operation. However, a detailed analysis of the device based on variation of V_{ch}, $V_{A,}$ V_B, $V_{C,}$ and V_{DS} with increase in doping level shows that the magnitude of V_{ch} increases whereas all other voltages including the forward drop, V_f and the power dissipation, P_D are found to decrease. The magnitude of P_D is found to decrease significantly from 1.552 to 0.0088 W at a current density of 1000 amperes per cm^2 as the drift region doping level changes from 10^{15} per cc to 10^{18} per cc. However, increasing doping level decreases the breakdown voltage and hence a trade off between the two needs to be established for good device design. For uniformly doped drift region devices with a device height of 73μm and a drift region doping level of 10^{15} per cc , the punch through breakdown voltages of 5kV should be used as avalanche breakdown voltages are somewhat higher i.e. 6.4kV.

The devices with a linearly graded doping profile in the drift region showed a nature of variation of V_{ch}, $V_{A,}$ $V_{B,}$ V_C with J_f which is similar to those obtained with uniformly doped drift region devices over concentration gradient α of magnitude ranging from $1.58x10^{18}$ to $1.54x10^{21}$ cm^{-4}. The magnitudes of the device voltages and also V_{DS} are found to decrease with increase in the value of α. The power dissipation, P_D is significantly low corresponding to those obtained with uniformly doped profiles, being as low as 0.3761 to 0.0054 W at a value of J_f of 1000ampers per cm^2. Comparison of plots of power dissipation with current density shown in Figure- 4.5 showed that for all uniformly doped drift region devices have corresponding linearly graded profile which can generate lower values of power dissipation. The other great advantage of linearly graded drift region devices is that they exhibit higher breakdown voltages, i.e. 6.75kV with a concentration gradient of $1.58x10^{18}$ per cm^{-4} for a device height of 65μm as against uniformly doped devices with a doping level of 10^{15} per cc can yield a breakdown voltage of 5kV with a device height of 73 μm. Hence, linearly graded drift region devices are thinner and yield higher breakdown voltages.

The devices with Gaussian profile in the drift region yield equations for depletion region width which give that solutions for a device height of 350 μm or higher which is considerably large for peak concentrations of N_0 ranging from 10^{18} to 10^{19} per cc with constant $m=1x10^{-4}$ cm. The corresponding power dissipation with $N_0=10^{18}$ per cc is 6.683W at current density of 1000 amperes per cm^2. However, a minimum values of P_D of 0.058W with the same value of N_0 results when m is increased to $10x10^{-4}$ cm.

The depletion region width, W shows a value of 153.1 μm at a reverse voltage of 16kV and tends to saturate at a slightly lower value of 152 μm for voltages exceeding

16kV. It is possible that carrier injection from the heavily doped drift regions near the drain into the drift region begins and causes breakdown which may be called the punch through breakdown characterized by V_{BPT}. The results obtained in Chaper5 showed that the two breakdown voltages, V_{BPT} and V_{BAV} are found to be approximately the same for all sets of values of N_0 and m going upto a maximum of 16kV at N_0 of 10^{18} per cc and m=1x10^{-4} cm. It has also been found that an increase in the value of m at a fixed value of N_0 leads to a decrease in the value of breakdown voltage and vice versa.

The Complementary Error Function (erfc) profile in the drift region of 6H-SiC MOSFET gives a decrease in the magnitude of the power dissipation P_D of 18.37W with peak concentration $N_0=10^{15}$ per cc at a current density of 1000 amperes per cm^2 to 0.073 W for the profile with $N_0=10^{18}$ per cc at the same device height of 350 μm that was used for analyzing the Gaussian profile in chapter5. The variation in power dissipation for various profiles, i.e. Gaussian and erfc, showed that for the same device height, the Gaussian profile exhibited a lower value of P_D at all current levels. Such variation can be seen from graphs shown in Figure-6.3, which shows that for all erfc profiles at a given current density has similar Gaussian profiles which have correspondingly lower power dissipation.

The nature of variation of depletion region width,W for complementary error function profiles with reverse bias, showed a similar type of variation as the Gaussian profile. The depletion region width saturates at 168 μm at 20kV and remains at a slightly lower value of 167 μm at higher voltages. A punch through breakdown voltage of 20kV using erfc profile can thus be obtained for $\alpha=1.13x10^{15}$ cm^{-4}, where α is the concentration gradient of the erfc profile which in the limit was approximated to a linearly graded

profile. The magnitude of the two breakdown voltages, V_{BPT} and V_{BAV} were found to be approximately the same for a given value of α. This was similar to the nature of the two breakdown voltages in a Gaussian profile.

In conclusion, it may be mentioned that linearly graded profiles in the drift region yield least value of power dissipation with smallest device or wafer thickness. The highest power dissipation was estimated in devices with Complementary Error Function profiles followed by Gaussian profiles and then the uniformly doped profile. On the other hand for thicker devices highest breakdown voltage could be obtained using the complementary error function profile followed by the Gaussian profile. However, for thinner devices the linearly graded profile should be preferred for obtaining breakdown voltages exceeding 5kV over uniformly doped drift region DIMOSFETs.

The experimental verification of these results would require fabricating 6H-SiC wafers with thickness of the order of 350 μm and generating a Gaussian and a Complementary Error Function profile in them using ion-implantation and other techniques. Device fabrication and study of power dissipation and breakdown voltages can then be undertaken to obtain the experimental results and tallied with those presented in this work.

REFERENCES

[1] M. Ostling and N. Lundberg, **"**Low Ohmic Cobalt Silicide contacts to p-type 6H-SiC", IEEE Device Research Conf., Santa Barbara, CA, USA, p 157, June, 1996.

[2] T. Ouisse, N. Becourt, F. Templier, J. Vuiolld, S. Cristoloveanu, T. Billon, and F. Mondon, "Noise in 6H-SiC ion implanted *p–n* diodes", 5th Int. Conf. on Silicon Carbide and Related Materials, Conf. Ser. No. 137, pp.683-686, September, 1995.

[3] R. F. Davis, G. Kelner, M. Shur, J. W. Palmour, and J. A. Edmond, "Thin film deposition and microelectronic and optoelectronic device fabrication and characterization in mono crystalline alpha and beta silicon carbide, *Proceedings* of IEEE, vol. 79, p. 677, 1991.

[4] H. Morkoc, S. Strite, G. B. Gao, M. E. Lin, B. Sverdlov, and M. Burns, "Large-bandgap SiC, III-V notride, and II-VI ZbSe-based semiconductor device technologies", *J. Appl. Phys.,* vol, 76, p. 1363, 1994.

[5] H. M. Hobgood, D. L. Barrett, J. P. McHugh, R. C. Clarke, S. Sriram, A. A. Burk, J. Greggi, C. D. Brandt, R. H. Hopkins, and W. J. Choyke, "Large diameter 6H-SiC for microwave device applications", *J. Crystal Growth*, vol. 137, p. 181, 1994.

[6] G. A. Lomakina, "Electrical properties of various polytypes of silicon carbide", in *Silicon Carbide-1973*, R. C. Marshall, J. W. Faust, Jr., and C. E. Ryan, Eds. Columbia, SC: University of South Carolina Press, p. 520, 1973.

[7] W. J. Schaffer, G. H. Negley, K. G. Irvine, and J. W. Palmour, "Conductivity anisotrophy in epitaxial 6H and 4H SiC", *Mat. Res. Soc. Symp. Proc.*, vol. 339, Diamond, SiC, and Nitride Wide-Bandgap Semiconductors, C. H. Carter, Jr., G. Gildenblatt, and S. Nakamura, Eds. Pittsburgh, PA : Materials Research Society, p. 595, 1994.

[8] S. Sridevan, P. K. Mclarty, and B. J. Baliga, "On the presence of aluminum in thermally grown oxides on 6H-silicon carbide [power MOSFETs]", *IEEE Electron Device Lett.*, *17*, 136-138, 1996.

[9] J. A. Cooper Jr., "Recent advances in silicon carbide MOS technology", 6th Int. Conf. on Silicon Carbide and Related Materials, Kyoto, Japan, September **1995**, pp.186-188.

[10] P. G. Neudeck, D. J. Larkin, J. W. Starr, J. A. Powell, C. S. Salupo, and L. G. Matus, "Electrical properties of epitaxial 3C- and 6H-SiC p-n junction diodes produced side-by-side on 6H-SiC wafers", *IEEE Trans. Elect. Dev*., vol. 41, p. 826, 1994.

[11] P. G. Neudeck, D. J. Larkin, J. E. Starr, J. A. Powell, C. S. Salupo, and L. G. Matus, "Greatly improved 3C-SiC p-n junction didoes grown by chemical vapor deposition", *IEEE Elect. Dev. Lett.*, vol 14, p. 136, 1993.

[12] K. Christian and R. Helbig, "Anisotropic oxidation of 6H-SiC", *J. Appl. Phys*., vol. 69, p.3276, 1996.

[13] K. Ueno and Y. Seki, "Orientation dependence of thermal oxidation rates in 6H-SiC", in *Proc. Intl. Conf. on Silicon Carbide and Rel. Mat.*, Institute of Phys. Conf. Series no. 142, p. 629, 1996.

[14] T. Kimoto, A Itoh, H. Matsunami, T. Nakata, and M. Watanabe, "Aluminum and boron ion-implantations into 6H-SiC epilayers", J. Elect. Mat., vol 25, p. 879, 1996.

[15] P. Godignon, X. Jorda, M. Vellvehi, S. Berberich, J. Montserrat, and L. Ottaviani, "Effect of boron implantation on 6H-SiC N-MONSFET interface properties", Mat. Sci. Forum. Vols. 338-342, p. 1303, 2000.

[16] http:// www.ecn.purdue.edu/WBG/Data_Bank.

[17] T. Tachibana, H. S. Kong, Y. C. Wang, and R. F. Davis, "Hall measurements as a function of temperature on monocrystalline SiC thin films", *J. Appl. Phys*., vol. 67, p. 6375, 1990.

[18] S. Nishino, H. Suhara, H. Ono, and H. Matsunami, "Epitaxial growth and electric characteristics of cubic SiC on silicon", J. Appl. Phys., vol. 61, p. 4889, 1981.

[19] J. W. Palmour, Cree Research, private communication, 1996.

[20] http.//www.ierc.nasa.gov/WWW/SiC/redhot.html.

[21] ST Microelectronics, Data Sheet for power MOSFET component series : STP5NC70Z-STP5NC70ZP-STP5NC70Z-1, 2000.

[22] R. R. Tummala, E. J. Rymaszewski, Microelectronics Packaging Handbook, New York: Van Nostrand Reinhold, 1989.

[23] G. Ghibaudo, "New method for the extraction of MOSFET parameters," *Elect. Lett.,* vol. 24, p. 543, 1988.

[24] I. K. Budihardjo, P. O. Lauritzen, and H. A. Mantooth, "Performance requirements for power MOSFET models," *IEEE Trans.* Power Elect., vol. 12, p. 36, 1997.

[25] M. Brown, Practical Switching Power Supply Design, San Diego: Academic Press, Inc., 1990.

[26] S. C. Sun and J. D. Plumner, "Modeling of the on-resistance of LDMOS, VDMOS, and VMOS power transistors," *IEEE Trans. Elect. Dev*., vol. ED-27, pp. 356-357, 1980.

[27] V. A. K. Temple and P. V. Gray, "Theoretical comparison of DMOS and VMOS structures for voltage and on-resistance," in *IEDM Tech. Dig*., p. 88, 1979.

[28] S.M.Sze, "Physics of Semiconductor Devices," 2nd Edn., John Wily & Sons, New York, 1985.

[29] Jayarama.N.Shenoy, James.A. Cooper and Michael.R.Melloch, "High-voltage double-implanted MOS power transistors in 6H-SiC," IEEE Device Research conference, Santa Barbara, CA, June, 1996.

[30] Jayarama.N.Shenoy, James.A.Cooper and Michael.R.Melloch, "High-Voltage Double-Implanted Power MOSFET's in 6H-SiC," IEEE Trans. Electron Device Lett., March, 1997, vol. 18, pp.93-95.

[31] Praveen M. Shenoy and B.Jayant Baliga, "The planar 6H-SiC ACCFET: A new high-voltage power MOSFET structure," IEEE Trans. Electron Device Letters, December, 1997, vol. 18, pp. 589-591.

[32] M.Ruff, H. Mitlehner, and R.Helbig, "SiC devices: Physics and numerical simulation", IEEE Trans .on Electron Device, June, 1994, vol. 41, pp. 1040-1054.

[33] M. Bhatnagar and B. J. Baliga, "Comparison of 6H-SiC, 3C-SiC, and Si for power devices", IEEE Trans. Elect. Dev., vol. ED-40, p. 645, 1993.

[34] K.Shenai, R.S.Scott and B.J.Baliga, "Optimum semiconductors for high power electronics," IEEE Trans. on Electron Devices, September, 1989, 36(9), pp1811-1823.

[35] B.J.Baliga, "Trends in power semiconductor devices," IEEE Trans. on Electron Devices, October, 1996, 43(10), pp. 1717-1731.

[36] R. B. Hillborn and H. Kang, "Charge carrier concentration and mobility in n-type 6H polytypes of SiC", University of South Carolina Press, 1973.

[37] Shuntao Hu and Kuang Shan, "A new edge termination technique for SiC power devices", Solid State Electronics, June 2004, vol. 48, pp.122-123.

[38] James.A.Cooper, Michael.R.Melloch, Ranbir Singh, Anant Aggarwal and John.W.Palmour,"Status and prospect for SiC MOSFET", IEEE Trans. Electron Devices, April 2002, vol. 49, no. 4, pp. 658-664.

[39] R. Kosugi, S. Suzuki, M. Okamoto, S. Harada, J. Senzaki and K. Fukuda, "Strong dependence of the inversion channel mobility of 4H and 6H SiC (0001) MOSFETs on the water content in pyrogenic re-oxidation annealing, IEEE Electron Device Lett., 2002, vol.23, pp. 136-138.

[40] B.J.Baliga, "Power semiconductor device figure of merit for high-frequency applications", IEEE Electron Device Lett., October 1989, vol.10, pp 455-457.

[41] Dale M. Brown, Mario Ghezzo, James Kretchmer, Evan Downey, Joseph Pimbley, and John Palmour, "SiC MOS interface characteristics", IEEE Trans. Electron Devices, April 1994,vol.41, no.4, pp. 618-620.

[42] J. W. Palmour, J. A. Edmond, H. S. Kong, and C. H. Carter, Jr., "Vertical power devices in silicon carbide," In Proc. Silicon Carbide and Related Materials, 1994, p. 499.

[43] N. S. Rebello, F. S. Shoucair, and J. W. Palmour, 'High-temperature electrical characteristics of 6H silicon carbide MOSFETs (25-500 ^{0}C)", in *Trans. 2nd int. High Temp. Elect. Conf.,* D. B. Kind and F. V. Thome, Eds., (Phillips Laboratory Sandia National Laboratories, Wright Laboratory, 1994), p. IV-27, 1994.

[44] W. J. Schaffer, G. H. Negley, K. G. Irvine, and J. W. Palmour, "Conductivity anisotropy in epitaxial 6H and 4H SiC", in *Mat. Res. Soc. Symp. Proc.*, vols. 339, p. 595, 1994.

[45] S. Takagi, A. Toriumi, M. lwase, and H. Tango, “On the universality of inversion-layer mobility in Si MOSFETs–Part I: Effect of substrate impurity concentration”, *IEEE Trans. Elect. Dev.*, vol. 41, p. 2357, 1994.

[46] J. W. Palmour, J. A. Edmonds, H. S. Kong and C. H. Carter, “Silicon carbide power devices,” Inst. of Phys. Conf. Series, no. 137: Ch. 7, p. 499, 1994.

[47] J. B. Casady, W. Dillard, R. W. Johnson, A. K. Agarwal, R. R. Siergiej, and W. E.. Wagner, "Low Frequency Noise in 6H-SiC MOSFETs," IEEE Electron Device Letters, vol.16, no.6, pp.274-276, 1995.

[48] J.N. Pan, J.A. Cooper, Jr., and M.R. Melloch, “Self-aligned 6H-SiC MOSFETs with improved current drive”, IEEE Electronics Letters, vol.31, no.14, pp. 1200-1201, 1995.

[49] R. P. Joshi, “Monte Carlo calculations of the temperature- and field-dependent electron transport parameters for 4H-SiC”, *J. Appl. Phys*., vol. 78, p. 5518, 1995.

[50] B. J. Baliga, “Critical nature of oxide/interface quality for SiC power devices”, *Microelect. Eng*., vol. 28, p. 177, 1995.

[51] R. Siergiej, A. Agarwal, W. Wagner, M. White, C. Brandt, M. Driver, and R. Hopkins, “Novel SiC device technology featuring enhancement and depletion mode transistors,” in Digest 53rd Annual Device Res. Conf., p. 98, 1995.

[52] S. Sridevan, P.K. McLarty, and B.J. Baliga, “On the Presence of Aluminum in Thermally Grown Oxides on 6H-Silicon Carbide,” IEEE Electron Device Letters, vol.17, no.3, pp.136-138, 1996.

[53] J. N. Shenoy, M. K. Das, J. A. Cooper, Jr., M. R. Melloch and J. W. Palmour, “Effect of substrate orientation and crystal anisotropy on thermally oxidized SiO_2/SiC interface,” *J. Appl. Phys.*, vol. 79, p. 3042, 1996.

[54] S. Nakashima and H. Harima, “Characterization of structural and electrical properties in SiC by Raman spectroscopy”, in *Inst. Phys. Conf. Series*, p. 269, 1996.

[55] T. Kimoto, A. Itoh, H. Matsunami, T. Nakata, and M. Watanabe, “Aluminum and boron ion-implantations into 6H-SiC epilayers”, *J. Elect. Mater*., vol. 25, p. 879, 1996.

[56] C.Zetterling, and M. Ostiling, 'A novel UMOS capacitor test structure for SiC devices," *Solid-State Elect*., vol. 39, p. 1396, 1996.

[57] K. Christiansen and R. Helbig, "Anisotropic oxidation of 6H-SiC," J. Appl. Phys. vol. 79, p. 3276, 1996.

[58] A. K. Agarwal, R. R. Siergiej, S. Seshadri, M. H. White, P. G. McMullin, A. A. Burk, L. B.Rowland, C.D. Brandt and R. H. Hopkins, A critical look at the performance advantages and limitations of 4H-SiC power UMOSFET Structures, 8th Int. Symposium on Power Semiconductor Devices and ICs, Maui, HI, USA, pp. 119-122, May 1996.

[59] A.K.Agarwal, J.B.Cascady, L.B.Rowland, W.F.Valek, M.H.White and C,D.Brandt, " 1.1KV 4H- SiC Power UMOSFET's," IEEE Trans. Electron Device Letters, December, 1997, vol. 18, pp. 586-588.

[60] Yoshitaka Sugawara and Katsunori Asano, "1.4 kV 4H-SiC UMOSFET with low specific on resistance," Int. Symposium on Power Semiconductor Devices & ICs, 1998, Kyoto, Japan, pp.119-122.

[61] J.B.Casdy, A.K.Agarwal, L.B.Rowland, W.F.Valek and C.D.Brandt, "900V DMOS and 1100 V UMOS 4H-SiC power FET's," IEEE Dev. Res. Conf., Fort Collins, USA, June 1997, pp 32-33.

[62] J.B.Casady, A.K.Agarwal, L.B.Rowland, S.Seshadri, P.A.Sanger and C.D.Brandt, "Silicon carbide MOSFET technology", IEEE Trans. Electron Devices, 1998, pp.359-362.

[63] Yoshitaka Sugawara and Katsunori Asan, "1.4kV 4H-SiC UMOSFET with low specific on- resistance", 10th Int. Symposium on Power Semiconductor Devices and ICs, Kyoto, Japan, June, 1998, pp.119-122.

[64] Ravi K**.** Chilukuri, Praveen M. Shenoy, and B**.** Jayant Baliga, Comparison of 6H-SiC and 4H-SiC high voltage planar ACCUFETs", "Proceedings of International Symposium on Power Semiconductor Devices & ICs, Kyto, pp.115-118, 1998.

[65] C Mark Johnson, Nick G Wright, Sylvie Ortolland, Dominique Morrison, Kazuhiro Adachi and Anthony O'Neill, "Silicon carbide power devices: hopeful or hopeless?", IEE Colloquium on recent advances in power devices, 1999, London, UK, pp. 10/1 - 10/5.

[66] A. Mihaila, F. Udrea, R. Azar, J. Liang, G. Amaratungal, A. Rusu and G. Brezeanu , " Theoretical and numerical investigation of SiC JFET and MOSFET at 6.5kV", Semiconductor Conference 1999, Sinaia, Romania, October, 1999, pp.191-194.

[67] C. H. Carter Jr. et al, "Progress in SiC: From material growth to commercial device development", *Mat. Sci. Eng.,* vols. B61-62, p. 1, 1999.

[68] Vathulya V.R, Shang, H, White, M.H, "A novel 6H-SiC power DMOSFET with implanted p-well spacer", IEEE Electron Device Letters, vol.26, no.7, pp.354-356, 1999.

[69] Reinhold Schörner, Peter Friedrichs and Dethard Peters, " Detailed Investigation of N-channel enhancement 6H-SiC MOSFET's", IEEE Transactions on Electron Devices, vol. 46, no.3, 1999.

[70] William E. Wagner, III and Marvin H. White, "Characterization of silicon carbide epitaxial channel MOSFETs", IEEE Trans. on Electron Devices, November,2000, vol. 47, pp.2214-2220.

[71] Peter Friedrichs, Heinz Mitlehner, Karl Otto Dohnke, Dethard Peters, Reinhold Schorner, Ulrich Weinert, Eric Baudelot and Dietrich Stephani, "SiC power devices with low on-resistance for fast switching applications, The 12th International Symposium on Power Semiconductor Devices and ICs, France, pp.213-216, 2000.

[72] J. P. Xu**,** P. T. Lai**,** C. L. Chan**,** B**.** Li, and Y. C. Cheng, Improved Performance and Reliability of N_2O-Grown Oxynitride on 6H-SiC, IEEE Electron Device Letters, vol.21, no.6, pp. 298-300, 2000.

[73] D. Alok, E. Arnold, R. Egloff, J. Barone, J. Murphy, R. Conrad, and J. Burke, "4H-SiC RF power MOSFETs", IEEE Electron Device Lett., December, 2001,vol. 22, pp. 577-578.

[74] Matthias Roschke and Frank Schwierz, "Electron mobility models for 4H, 6H, and 3C SiC", IEEE Transactions on Electron Devices, vol.48, no. 7, pp.1442-1447, 2001.

[75] G.Y.Chung, C.C.Tin, J.R. Williams, K. McDonald, R.K. Chanana, R.A.Weller, S.T. Pantelides, L.C.Feldman, O.W. Holland, M.K. Das, J.W. Palmour,

"Improved Inversion Channel Mobility for 4H-SiC MOSFETs following High Temperature Anneals in Nitric Oxide", IEEE Electron Device Letters, vol.22, no.4, pp.176-178, 2001.

[76] Stephen K.Powell, Neil Goldsman, C.J.Scozzie, Aivars Lelis and James M. McGarrity, "Self-consistent surface mobility and interface charge modeling inconjunction with experiment of 6H-SiC MOSFETs", International Semiconductor Device Research Symposium, pp.572-572, 2001.

[77] Ramovi, M. Jevti, J. Hadzi-Vukovi and D. Randjelov, "A novel analytical model of a SiC MOSFET", 23rd international conference on microelectronics (MIEL 2002), vol. 2, NIS, Yugoslavia, May,2002, pp. 447-450.

[78] Sei-Hyung Ryu , Anant Agarwal, James Richmond, John Palmour, Nelson Saks, and John Williams, "10 A, 2.4 kV Power DIMOSFETs in 4H-SiC", IEEE Electron Device Lett., June, 2002, vol. 23, pp. 321-323.

[79] Kin Kiong Lee, Takeshi Ohshima and Hisayoshi Itoh, "Performance of Gamma Irradiated P-Channel 6H-SiC MOSFETs: High Total Dose", IEEE Transactions on Nuclear Science, vol.50, no.1, 194-200, 2003.

[80] Md. Hasanuzzaman, Syed.K. Islam and Leon. M. Tolbert, "Model Simulation & Verification of Vertical Double Implanted (DIMOSFET) Transistor in 6H-SIC", International Journal of Modeling and Simulation, June, 2003, vol.4, pp. 1-4.

[81] Manoara Avram, Gheorghe Brezeanu and Daniel Puiu Poenar, "The comparison of modern SiC power devices", IEEE Int. Conference on Industrial Technology, Hammamet, Tunisia, December, 2004, vol.1, pp.504-509.

[82] L.Chen, O.J.Guy, M.R.Jennings, S.P.Wilks and P.A.Mawby, "Simulation study of 1.2kV 4H-SiC DIMOSFET structures", 7th Int. Conference on solid-state and integrated circuits technology, Beijing, China, October, 2004, vol.3, pp. 2341-2344.

[83] Ranbir Singh and Allen R.Hefner, "Reliability of MOS Devices", Solid State Electronics, vol.48, pp.1717-1720, 2004.

[84] Ty Mc Nutt, Allen Hefner, Alan Mantooth, David Bearing and Ranbir Singh, "Compact model for Silicon Carbide Devices", Solid State Electronics, vol.48, pp.1757-1762, 2004.

[85] Shuntao Hu and Kuang Sheng, "New Edge termination technique for SiC power devices", Solid State Electronics, vol.48, pp.1861-1866, 2004.

[86] Norman G.Gunter, Iliya I.Pesic, Ayhan A.Mutlu and Mahmud Rahman, "Modeling C-V characteristics of deep sub - 0.1 micron mesoscale MOS devices", Solid State Electronics, vol.48, pp.1883-1890, 2004.

[87] Q. Zhang, M. Gomez, C. Bui and E. Hanna, "1600V 4H-SiC UMOSFETs with dual buffer layers", 17th Int. Symposium on Power Semiconductor Devices & IC's at Santa Barbara, CA, May, 2005, pp.211-214

[88] Y. Sui, T. Tsuji, and J. A. Cooper, Jr., "On-state characteristics of SiC power UMOSFETs on 115 μm drift layers", IEEE Electron Device Letters, April, 2005, vol. 26, pp. 255-257.

[89] Anant Agarwal, Mrinal Das, Brett Hull, Sumi Krishnaswami, John Palmour, James Richmond, Sei Hyung Ryu and Jon Zhang, "Progress in silicon carbide power devices", 64th Device Research Conference, Pennsylvania , June, 2006, pp. 155-158.

[90] John W. Palmour, "Energy efficient wide bandgap devices", Compound Semiconductor Integrated Circuit Symposium 2006, November, 2006, pp.4-7.

[91] Ty.R. McNutt, Allen R. Hefner, H. Alan Mantooth, David Berning, and Sei Hyung Ryu, "Silicon carbide power MOSFET model and parameter extraction sequence", IEEE Trans. on Power Electronics, March, 2007, vol. 22, pp. 353-362.

[92] S.M.Sze, Semiconductor Devices-Physics and Technology, IInd Edition, John Wiley & Sons, INC, New York,2002.

[92] B. J. Baliga, *Power Semiconductor Devices*, Boston: PWS Publishing, 1995.

[93] B. J. Baliga, "Prospects for SiC power devices," in *Int. Conf. on Silicon Carbide and Rel. Mat.* Abstr. MoA-I-1, p. 3, 1995.

[94] J.A.Cooper, S.H.Ryu, M.Matin, J.Spitz, D.T.Morisette, H.M.Meglothlin, M.K.Das, M.R.Melloch, M.A.Capano and J.M. Woodall, " SiC power electronic devices, MOSFETs and Rectifiers," Int. Mat. Res. Soc. Symp. Proc., vol. 572, 1999, pp. 3-12.

[95] H. Morkoe, S. Strite, G.B.Gao, M.E.Lin, B.Sverdlov, and M.Burns, " Large bandgap SiC, III-V nitride and II-VI ZnSe-based semiconductor device technologies," J.Appl.Phys., vol.76, pp.1363-1398, Aug.1994.

[96] D. M. Brown, E.Downey, M. Ghezzo, J. Kretchmer, V.Krishnamurthy, W.Hennessy and G.Michon, " Silicon carbide MOSFET Technology", Solid-State Electron, vol.39, pp.1531-1542, 1996.

[97] R.Schorner, P.Friedrichs, D.Peters and D.Stephani, "Significantly improved performance of MOSFETs on silicon Carbide using the 15R-SiC polytype," IEEE Electron Device Lett., vol.20, pp.241-244, July 1999.

[98] P. M. Shenoy and B. J. Baliga, "High voltage planar 6H-SiC ACCUFET," in silicon carbide, III-Nitrides and Related Materials, Zurich, Switzerland: Trans Tech, 1998, p.993.

[99] C.Y.Chung, C.C.Tin, J.R.Williams, K.McDonald, M.Di Ventra, S.T.Pantelides, L.C.Feldman and R.A.Weller, "Effect of nitric oxide annealing on the interface trap densities near the band edges in the 4H polytype of silicon carbide," Appl. Phys. Lett., vol.76, p.1713, 2000.

[100] C.Y.Chung, C.C.Tin, T.Issacs-Smith, J.R.Williams, K.McDonald, M.Di Ventra, S.T.Pantelides, L.C.Feldman, R.A.Weller and O.W.Holland, "Nitrogen passivation of interface states near the conduction band in silicon carbide," Mat. Res. Soc. Symp., Boston, MA, Nov. 27-Dec.1, 2000.

[101] M.K.Das, L.A.Lipkin, J.W.Palmour, G.Y.Chung, J.R.Williams, K.McDonald and L.C.Feldman, "High mobility 4H-SiC inversion mode MOSFETs using thermally grown, NO annealed SiO_2," IEEE Trans. Device Research Conf., Denver, CO, June 19-21,2000.

[102] M.G.Spencer, J.W.Palmour, and C.H.Carter, "Substrate and Epitaxial Issues for SiC Power Devices," IEEE Trans. Electron Devices, vol.49, Apr.2002.

[103] P. M. Shenoy and B. J. Baliga, "The Planar 6H-SiC ACCUFET: A new high-voltage power MOSFET structure," *IEEE Elect. Dev. Lett.*, vol. 18, p. 589, 1997.

[104] Scott T.Sheppard, Michael R.Melloch and James A.Cooper, "Characteristics of inversion channel and buried channel MOS Devices in 6H-SiC," IEEE Trans. Electron Devices, vol.41, pp. 1257-1264, July,1994.

[105] Vikram R. Vathulya, Huiling Shang and Marvin H. White, "A novel 6H-SiC power DMOSFET with implanted p-well spacer, IEEE Trans. Electron Device Letters, vol. 20, pp. 354-356, July, 1999.

[106] Rajneesh Talwar and A.K.Chatterjee, unpublished work, 2009.

[107] Y. Wang, C. Weitzel and M. Bhatnagar, "Design issues of SiC accumulation channel power MOSFET", *Mat. Sci. Forum, vols.* 338-342, p. 1287. 2000.

[108] S. M. Sze and G. Gibbons, "Avalanche breakdown voltages of abrupt and linearly graded p-n junctions in Ge, Si, GaAs, and GaP", *Appl. Phys. Lett.*, vol. 8, p. 111, 1966.

[109] J. W. Palmour and L. A. Lipkin, Cree, Inc. "High temperature power devices in silicon carbide." In *Trans. 2nd Intl. High Temp. Elect. Conf.,* Charlotte, June 5-10, p. XI-3, 1994.

[110] V.V.Afanasev, M.Bassler, G.G.Pensl and M.Scultz, "Intrinsic SiC/SiO_2 interface states," Phys. Stat. Sol., vol. 162, p.321, 1997.

[111] D. Foty, MOSFET Modeling with SPICE Principles and Practice, New Jersey: Prentice- Hall, 1997.

[112] G. Ghibaudo, "New method for the extraction of MOSFET parameters,"*Elect. Lett.*, vol. 24, p. 543, 1988.

[113] J. Wang, and B. W. Williams, "Evaluation of high-voltage 4H-SiC switching devices," IEEE Trans. Elect. Dev., vol. 46, p. 589, 1999.

[114] S. Onda, R. Kumar, and K. Hara, "SiC integrated MOSFETs," Phys. Stat. Sol. (a), vol. 162, p. 369, 1997.

[115] T. P. Chow, "SiC and GaN high-voltage power switching devices", *Mat. Sci. Forum,* vols. 338-342, p- 1155, 1999.

[116] K. Hara, "Vital issues for SiC power devices", Mat. Sci. Forum, vols, 264-268, p. 901, 1998.

LIST OF RESEARCH PAPERS PUBLISHED AND PRESENTED

[P.1] Theoretical Analysis And Design Of Double Implanted MOSFET On 6H Silicon Carbide Wafer For Low Power Dissipation And Large Breakdown Voltage", *Maejo International Journal of Science & Technology, vol.2*, no.2, pp. 308-319, 2008.

[P.2] "Recent Trends In Silicon Carbide Device Research", *Maejo International Journal of Science & Technology,* vol.2, no.3, pp. 444-470, 2008.

[P.3] "Recent Advances in Silicon Carbide Device Based Power MOSFETs", *Journal of Electrical Engineering*, vol.9, no.1, pp.21-32, 2009.

[P.4] "Estimation of Power Dissipation of 6H DIMOSFET with a Linearly Graded Drift region", submitted to *Elsevier Microelectronic Journal*.

[P.5] "Analysis of Breakdown Voltage and Power Dissipation of 6H DIMOSFET with Gaussian Profile in Drift Region" submitted to *Elsevier Microelectronic Journal*.

[P.6] "Analysis of Breakdown Voltage and Power Dissipation of 6H DIMOSFET with Complementary Error Function Profile in Drift Region" submitted to *Elsevier Solid State Electronics Journal*.

[P.7] "Performance of Silicon Carbide wafers for Semiconductor Power Devices", *National conference of Materials and Related Technologies*, TIET-Patiala, September19-20, 2003.

[P.8] "Optimum Doping Level of Drift Region of 10 KV 6H- SiC Power DIMOSFET For the Power Dissipation", *International Conference on Resource Utilization and Intelligent Systems (INCRUIS- 2006)*, Kongu Engineering College- Erode, Tamil Nadu, January 4-5, 2006.

[P.9] "Mathematical Analysis and Design of Power DIMOSFET on 6H-SiC Wafer", *National Conference on "Innovations 2005*", BBSBEC-Fathehgarh Sahib from Nov.25-26, 2005.

[P.10] "Field Dependent Mobility Analysis of High Voltage SiC DIMOSFET using Graded Doping in the Drift Region", *Second National Conference on Electronic Circuits & Communication Systems (ECCS-2006)*, TIET, Patiala on 09-10 February 2006.

[P.11] "Field Independent Mobility Analysis of High Voltage SiC DIMOSFET using Graded Doping in the Drift Region", *National Conference On Circuits , Computer & Communication Systems (NCCCB-2006)*, Engineering College-Kota on 09-10 March, 2006

[P.12] "Analysis & Design Of 6H-SiC Double Implanted MOSFET and Optimize Doping Level In Drift Region & Power Dissipation", *IEEE International Conference on Computer & Communication Engineering* , Islamic University, Kuala Lumpur, Malaysia, on 9-11May 2006 .

[P.13] "Estimation of Effective Doping level of a semiconductor having a Gaussian Profile", *National Conference on "Communications 2006*", CIET-Banur on 27-28 July 2006.

[P.14] "Design of a DIMOSFET on 6H SiC Wafer using Field Dependent Mobility", *National Conference on "Communications 2006*", CIET-Banur on 27-28, July 2006.

[P.15] "Design of Double Implanted Power MOSFET for Large Breakdown Voltage on 6H SiC Wafer", *National conference on "DTVC-2007*", NIT-Hamirpur on 14-15 May 2007.

[P.16] "Performance analysis of 6H-SiC DIMOSFET using Gaussian Doping Profile", *National Conference on CCWN -2008*, P.D.M.C, Bahdurgarh.