DESIGN OF LOW POWER
AND HIGH SPEED SENSE AMPLIFIER

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Submitted by

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CERTIFICATE

I hereby declare that the work which is being presented in the thesis entitled "**DESIGN OF LOW POWER AND HIGH SPEED SENSE AMPLIFIER"** in the partial fulfilment of the requirements for the award of degree of **Master of Technology in VLSI Design & CAD at Thapar University, Patiala** is an authentic record of my own work carried under the supervision of **Mr. Arun K. Chatterjee**, Assistant Professor, Department of Electronics & Communication Engineering and refers other researcher's work which are duly listed in the reference section.

The matter embodied in this thesis has not been submitted for the award of any other degree of the Thapar University or any other university.

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Himanshu

Technology is just a tool. In terms of getting the kids working together and motivating them, the most important thing is teacher.

Bill gates

Never cut a tree down in the wintertime. Never make a negative decision in the low time. Never make your most important decisions when you are in your worst moods. Wait. Be patient. The storm will pass. The spring will come.

Robert H. Schuller

ABSTRACT

The sense amplifier plays an important role to reduce the overall delay and power dissipation of the memory. This thesis work explores the design and analysis of voltage mode sense amplifier and current mode sense amplifier using Mentor Graphics (V2006.4_4.1) at 180nm process technology.

The voltage mode sense amplifier circuit has been designed and simulation has been done on Mentor Graphic. A delay of 9.5ns and power dissipation of 243µW was found.

Next, the current mode sense amplifier has been designed. From the simulation results it is found that the net delay of sense amplifier is 8.2ns and power dissipation is 0.21µW. This shows a significant improvement in delay and power dissipation in comparison of the voltage mode sense amplifier.

The current mode sense amplifier is further designed using a low power and high speed circuit design technique which reduces the power dissipation to 0.073µW.

Finally, the layout for voltage mode sense amplifier and current mode sense amplifier have been drawn and layout versus schematic simulation results has been compared.

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LIST OF SYMBOLS

V_{DD} Supply Voltage

I_{stat} Static current

P_{stat} Static power

f Frequency

C_{in} Input Capacitance

W Width of MOSFET

L Length of MOSFET

V_{th} Threshold voltage

V_{ref} Reference voltage

NOMENCLATURE

SRAM	Static random access memory
CMRR	Common mode rejection ratio
PSRR	Power supply rejection ratio
MTCMOS	Multi threshold CMOS
VTCMOS	Variable threshold CMOS
DTCMOS	Dynamic threshold CMOS
SOI	Silicon on insulator
WL	Word line
BL	Bit line

CHAPTER 1 INTRODUCTION

Moore's law was the breakthrough and evolution in the semiconductor industry. Moore's law gave the idea to integrate large memory blocks with logic circuits on a single chip but the on-chip memory limits the speed and performance of the overall system. The limiting factor is the increasing bit line capacitance, which results in increased time to develop bit line differential voltage and increase in the delay. For fast and power efficient memory design, both time and signal swing on the bit lines needs to be minimized.

1.1 MOTIVATION

From the past few decades, the growth of the electronics industry is very fast and also the use of integrated circuits in computing, telecommunications and consumer electronics. In the 1958 there was only a single transistor on the chip called single transistor era and at present day ULSI (Ultra Large Scale Integration) systems with more than 50 million transistors in a single chip [1].

Power consumption awareness began worldwide around 1990-1992. Before that, only functional markets required low power integrated circuits. Power dissipation was not the main issue' just proper output and the circuit operation were the main preference [3]. The low power intend in circuit design is used because of:-

1. If the system dissipates high power, then extra design is required for the cooling system, thus the system will become very bulky and will not be portable.
2. Due to the extra cooling system the cost of the system will increase.
3. Due to the sky-scraping power dissipation the performance and reliability of the system decreases.

4. Memory is the main and important field of design. Today the size of the memory is decreasing and the storing capacity is increasing. As the storing capability is increasing, the time response for the data writing and reading from the memory should be very fast. For this purpose different types of sense amplifiers are used.

1.2 NECESSITY OF SENSE AMPLIFIER

In the memory, it is common to reduce the voltage swing on the bit lines to a value significantly below the supply voltage. This reduces both the propagation delay and the power consumption. Noise and other disturbances may be occurred in the memory array, for this sufficient noise margin is obtained even for these small signal swings. During the interfacing of the memory to the external field, the amplification of the internal swing is required. This is achieved by the *sense amplifiers*. Design of a high performance and efficient sense amplifier is very important for design SRAMS but with increasing parameter variations, the developing of a reliable and fast sense amplifier is a big problem in itself.

Sense amplifiers play a major role in the functionality, performance and reliability of memory circuit. Reduction in delay and power is acquired by using sense amplifier in memory circuits.

1.3 THESIS ORGANISATION

The primary goal of this thesis is to make obvious a low power and high speed circuit, used in the memory design for sensing the data rapidly. This thesis is organized as follows:

Chapter 2 explains the 6T SRAM and its read and write operation with size constraints of the memory cell. This chapter also introduces the sense amplifier, need of sense amplifier in the memory design. Finally, this chapter describes the different types of sense amplifiers.

Chapter 3 briefly introduces the different sources of power dissipation that occur in CMOS digital circuits and also the different techniques of reducing power dissipation in CMOS digital circuits.

Chapter 4 tells about the tool and technology used for the design and simulation of the 6T SRAM with precharge circuit has been done. Finally, this chapter explains the voltage and current mode sense amplifiers with their layout and simulation results.

Chapter 5 describes the conclusion of the work done and tells about the future scopes of the work.

CHAPTER

MEMORY DESIGN AND SENSE AMPLIFIER

Modern digital systems require the capability of storing large amount of data information with high speed. Memories circuits or systems store digital information in large extent. Memory circuits are of different types like SRAM, DRAM, ROM, EPROM, EEPROM, Flash and FRAM, each form has a different cell design, the basic structure and organisation. The total market share for semiconductor memories is expected to be over $45 billion in 2003, which is twice as large as it was in 1998 and will further increase [1]. Reliability and power dissipation are large concern of the semiconductor memory designer.

The propagation delay and the power consumption of the memory cell can be reduced by lowering the voltage swing on the bit lines. By reducing the voltage on the bit lines there will be a very small difference between bit and bit bar and it will be very difficult to differentiate logic ‘0’ and logic ‘1’ on the bit lines. This problem is eliminated and better results are achieved by the Sense Amplifier. The sense amplifier is mainly used in the digital memory circuit design, where it can detect even the small change in the current and voltage of the circuit. This chapter focus on the 6T SRAM and different types of sense amplifiers.

2.1 THE MEMORY CORE

The most compelling issue in design large memories is to keep the sizes of the cell as small as possible, this should be done so that other important design qualities such as speed and reliability do not highly affected. There are different type of memories like *read only, volatile, non-volatile,* and *read-write* memories. Here only SRAM is discussed.

2.2 STATIC RANDOM ACCESS MEMORY (SRAM)

RAM is a volatile memory. The data stored in this memory is lost when the power supply is switch off. It retains its memory patterns for as long as power is being supplied. Basically, RAM can be classified into two categories:-

1. Static RAM (SRAM)
2. Dynamic RAM (DRAM)

SRAM utilizes a flip flop mechanism. SRAM is a type of semiconductor memory. It does not need to be refreshed but it is volatile memory.

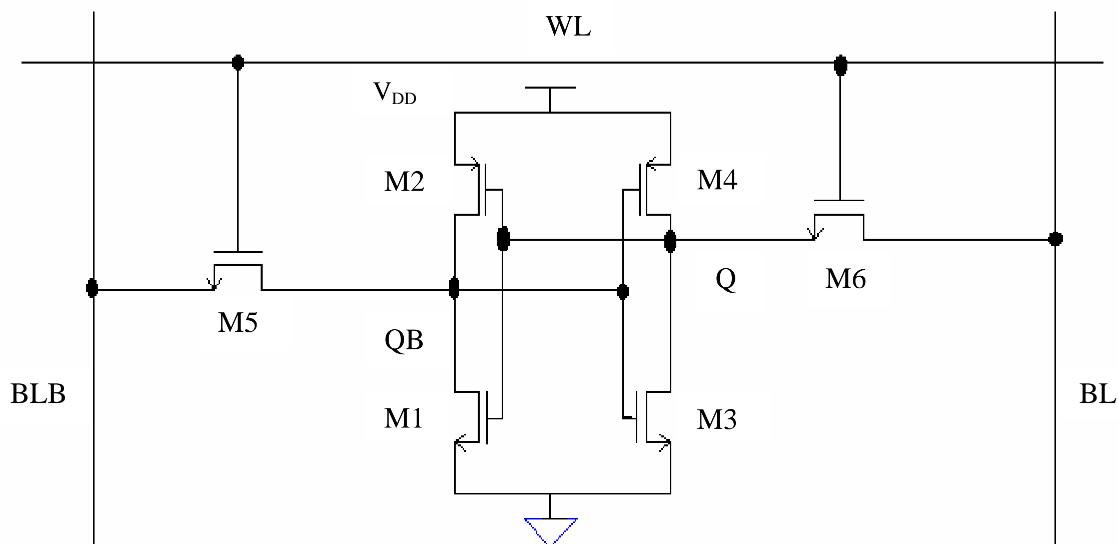


Figure 2.1 Six-transistor CMOS SRAM cell.

The SRAM cell should be sized as small as possible to achieve high memory densities. A 6T SRAM is shown in Figure 2.1. It is made of 6 transistors so it is called 6T SRAM. In this 6T SRAM two inverters (M1, M2 and M3, M4) are cross coupled. Each bit of data is stored on these four transistors in an SRAM cell. This storage cell has two stable states which are us ‘0’ and ‘1’. Two additional *access* transistors M5 and M6 are used to control the access to a storage cell during read and write operations and these are connected to the *bit lines* and *word line*. For the accurate operation the size of the transistors are designed properly.

2.2.1 CMOS SRAM READ OPERATION

Assume that a '1' is stored at Q, so the '0' will be at Q bar. Both the bit lines are precharged to V_{dd}. Read cycle will not be start until the word line is low. As the word line will be high both the access transistors M5 and M6 will turned on and the read cycle initiate.

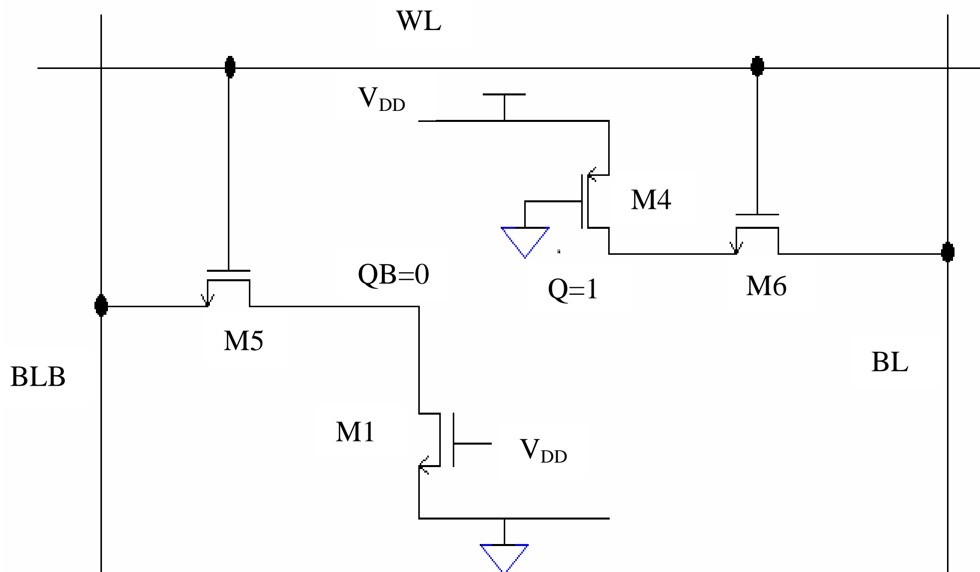


Figure 2.2 Simplified circuit of CMOS SRAM cell read operation [2].

During a correct read operation, the values stored in Q and Q bar are transferred to the bit lines by leaving *BL* at its precharge value and by discharging *BL bar* through M1-M5. A careful sizing of transistors is necessary for reading the data from memory. A simplified circuit of read operation is shown in Figure 2.2.

As the '1' is stored at Q, due to which the transistor M1 will be turned on and the transistor M3 WILL turned off as the '0' is stored at Q bar. Transistor M5 is already on due to high word line, a direct path will be forms between BL bar and ground as both the transistors M1 and M5 are on. Now the BL bar will be discharge through transistors M1 and M5.

SIZE CONSTRAINTS

During the read operation transistor M1 is on due to the value '1' stored at Q. Word line is already high so both the transistors M5 and M6 are on. Transistors M2 and M3 are in the off mode due to the value stored at Q and Q bar. The sizes of the transistors M1 and M5 are of the type that a high value voltage cannot be generate at Q bar, if this happens due to the high voltage at Q bar transistor M3 will become on and a direct path is occurred between $V_{dd}$and ground. So the size of the transistor M1 must be greater than transistor M5 so that it discharge the node Q bar. Transistor M4 is on as the '0' is stored at Q bar. The value stored at Q should be nearby '1' so that the transistor M1 can remain on.

2.2.2 CMOS SRAM WRITE OPERATION

The simplified model of CMOS SRAM cell during write operation is shown in Figure 2.3. For the proper SRAM write operation, assume that a '1' is stored in the cell Q, then the value stored at Q bar will be '0'.due to the values stored at Q and Q bar, transistors M2 and M3 will turned off.

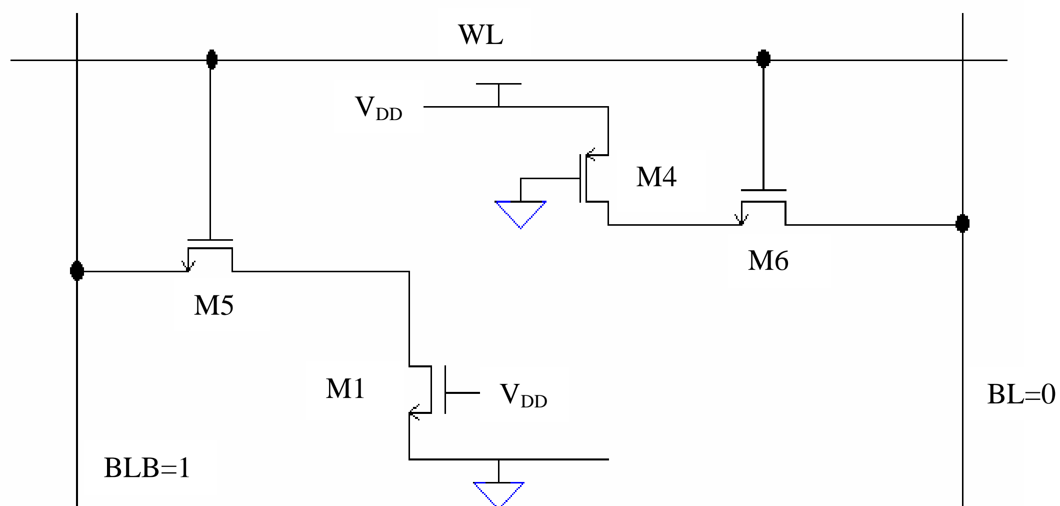


Figure 2.3 Simplified model of CMOS SRAM cell write operation [2].

As the word line becomes high the write cycle will starts. For the write cycle value '0' is to be stored at Q, for this bit line BL is kept at '0'. As the write cycle will start, a path will be formed between supply voltage and BL and BL start charging. By keeping the proper sizes of

the transistors, the transistor M6 will discharge the node Q very fast as compare to the charging of the node by transistor M4. Due to the fast discharging of the Q a value ‘0’ will be set at this node.

SIZE CONSTRAINTS

During the write operation transistor M6 is on as the word line is high, and the value stored at the Q is ‘1’. This node is discharging through transistor M6, as well as transistor M4 is on and charging the node Q. The sizes of the transistors M4 and M6 are of such type that the value stored at Q will be ‘0’ after write operation. As the transistor M4 is charging node Q, the size of the transistor M6 must be greater than transistor M4 so that it can discharge the node Q rapidly than the charging.

According to the sizes M1>M5>M2

According to the resistance M1<M5<M2

2.3 SENSE AMPLIFIER

When reading a memory cell, bit lines are initially precharged. In the memory operation, one of the bit lines goes down and one remain charged. The pulling down of the bit line is very slow because the discharging through MOS is low and the capacitance of the bit line is very high. So, delay will increases in reading the data of the memory. Sense amplifiers are used to detect small variation on bit lines and produce full swing.

A sense amplifier used in the memory architecture is shown in Figure 2.4. In this, a square memory is designed, for selecting the proper row for reading or writing the data a row decoder is used. Column decoder is used to select a proper memory cell. Sense amplifier is connected with the memory cell so that it can detect and amplify the signal. A proper sense amplifier is used in design the memory.

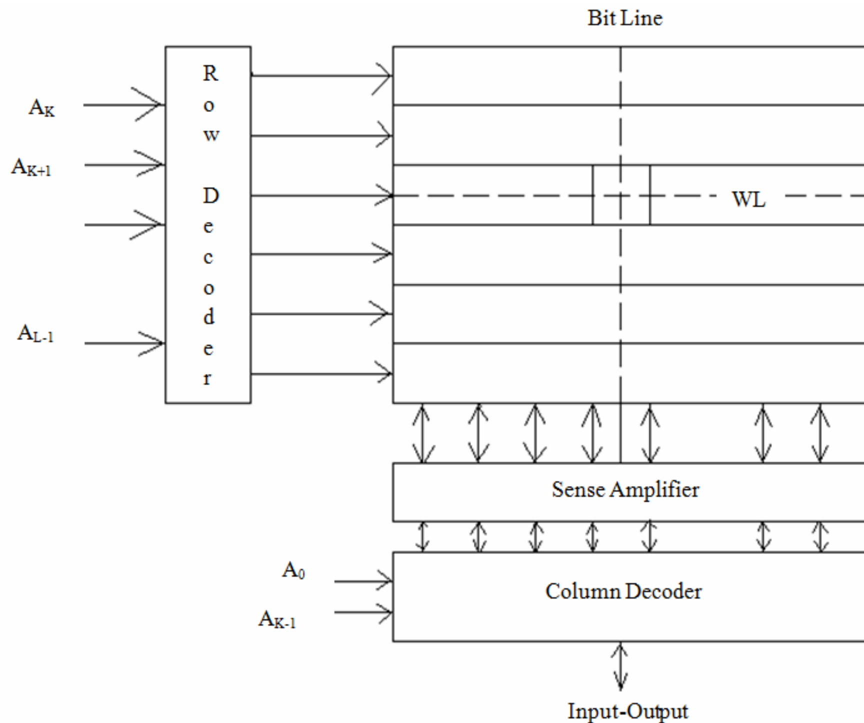


Figure 2.4 Sense amplifier in memory architecture.

2.4 FUNCTIONS OF SENSE AMPLIFIER [2]

1. Amplification: In certain memory structure, amplification is required for proper functionality since the typical circuit swing is limited. In other memories, it allows resolving data with small bit line swings, enabling reduced power dissipation and delay.
2. Delay reduction: The amplifier detects and amplifies small transition on the bit line to large signal output swings, due to which a small swing input is used and the delay will reduce.
3. Power reduction: Reducing the signal swing on bit lines can eliminate a substantial part of power dissipation related to charging and discharging the bit lines.

2.5 SENSING APPROACH

Figure 2.5 shows a fully differential two stage sensing approach along with the SRAM bit differential amplifier. A read cycle proceeds as follows:

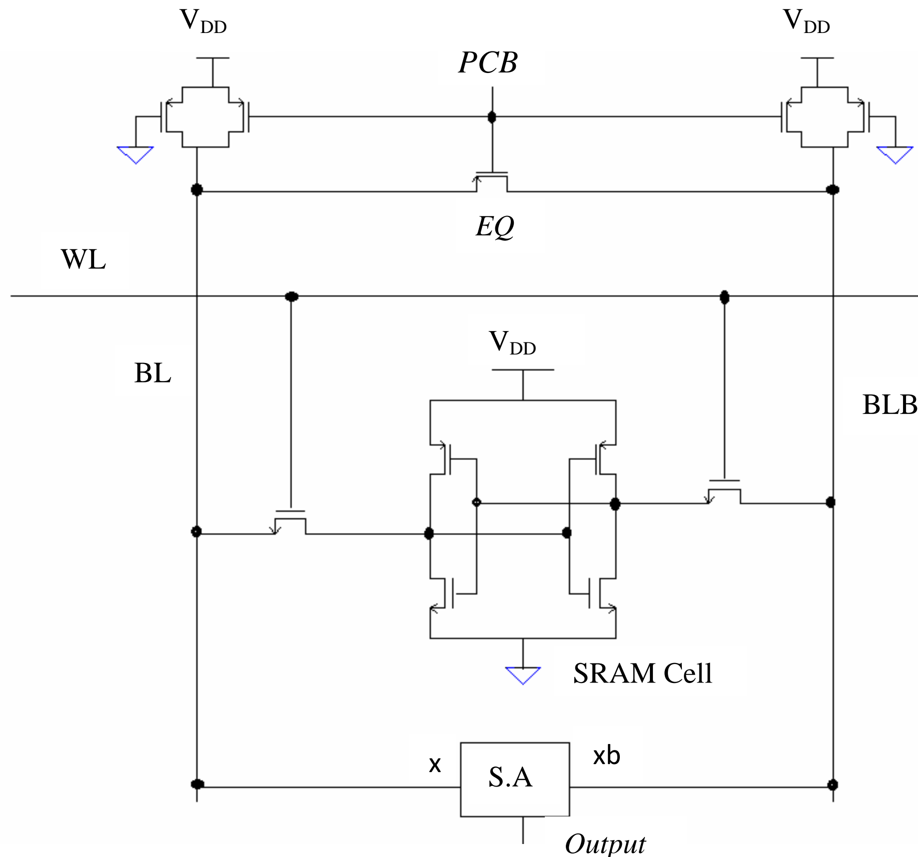


Figure 2.5 SRAM sensing scheme.

1. Bit lines are connected to V_{DD} through the PMOS transistors. In the first step, the bit lines are pre-charged to V_{DD}. By pulling *PCB* low PMOS transistors will turned on and the bit lines are precharged to V_{DD}. At the same time *EQ* transistor will turned on and it equalizes the voltage on both the bit lines.
2. The read operation is started by disabling the pre-charge and equalization devices and enabling the word line. One of the bit lines is pulled down by the combination of the transistors and one remain at V_{DD}. A difference in voltage will set up on the bit lines but the bit lines swing is limited.
3. Bit lines are connected to the sense amplifier. Sense amplifier will take the bit lines swing as the input and it will amplify the signal and produce the proper rail to rail swing output.

2.6 CLASSIFICATION OF SENSE AMPLIFIER

Sense amplifier is the main circuit used in the memory design. There are mainly two types of sense amplifiers and they can be categorized into:-

1. Voltage mode sense amplifier
2. Current mode sense amplifier

Voltage mode sense amplifier detects the voltage difference between the bit lines to determine whether a “1” or a “0” is stored in the memory cell. It amplifies the voltage signal and transfers it on the output circuits, where Current mode sense amplifier detects the current difference between the bit lines.

2.6.1 VOLTAGE MODE SENSE AMPLIFIER

Sense amplifier which detects the voltage difference on the bit lines is called voltage mode sense amplifier. There are some voltage mode sense amplifiers like single ended sense amplifiers, differential amplifiers and current mirror sense amplifiers. Different types of sense amplifier are used in different types of memory cells according to the proper design and efficient performance. According to the characteristics of the amplifiers, they are used in the design.

2.6.1.1 SINGLE ENDED SENSING

Memory cells used in ROMs, E(E)PROMs and DRAMs are inherently single ended . Single ended amplification is required for these types of memory cells. An interesting variant, called the charge redistribution amplifier Figure 2.6, is often used in small memory structure. The basic idea is to exploit the imbalance between a large capacitance C_{large} and a much smaller capacitance C_{small}.

The two capacitors are isolated by the pass transistor M1. The initial voltages on nodes L and S (V_{L0} , V_{S0}) are pre-charged to V_{ref}-V_{tn} and V_{DD} by connecting node S to the supply voltage. Because of the voltage drop over M1, V_L only precharges to V_{ref}-V_{tn}. When one of the pull

down devices (M2) turns on, node L with its large capacitances slowly discharges. As long as V_{ref}-V_{tn} ≤ V_L transistor M1 is off, and V_S remains constant.

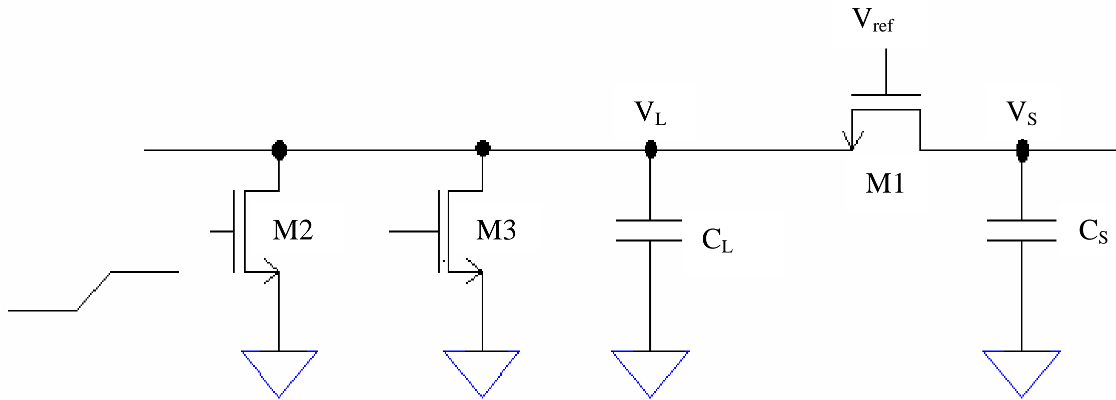


Figure 2.6 Charge-redistribution amplifier [2].

Once V1drops below the trigger voltage (V_{ref}-V_{tn}), M1 turns on, a charge redistribution is initiated, and nodes L and S equalize. This can happen very fast due to the small capacitance on the latter node. A small voltage variation on node L translates into a large voltage drop on node S. The circuit thus acts as an amplifier. The resulting signal can be fed into an inverter with a switching threshold larger than V_{ref}-V_{tn} to produce a rail-to-rail swing.

2.6.1.2 SINGLE TO DIFFERENTIAL CONVERSION

Single ended sense amplifiers do not have the proper characteristics that they can be used in the memory design. These amplifiers cannot be used in the Larger memories (>1MBit). Even a small noise signal can affect the functioning of the single ended sense amplifiers. A noise signal produced at the node L or S may turn on the transistor M1 and affect the circuit operation. So the single ended sense amplifiers are converted into the differential sense amplifiers [2].

The basic concept behind the single-to differential conversion is shown in the Figure 2.7. A differential sense amplifier is connected to a single-ended bit line on one side and a reference voltage, positioned the ‘0’ and ‘1’ levels, at the other end. Depending upon the value of the BL, the amplifier toggles in one or the other direction. It is not an easy task to create a good

reference source because the voltage level varies. Both the inputs of the differential sense amplifier should be complementary to each other.

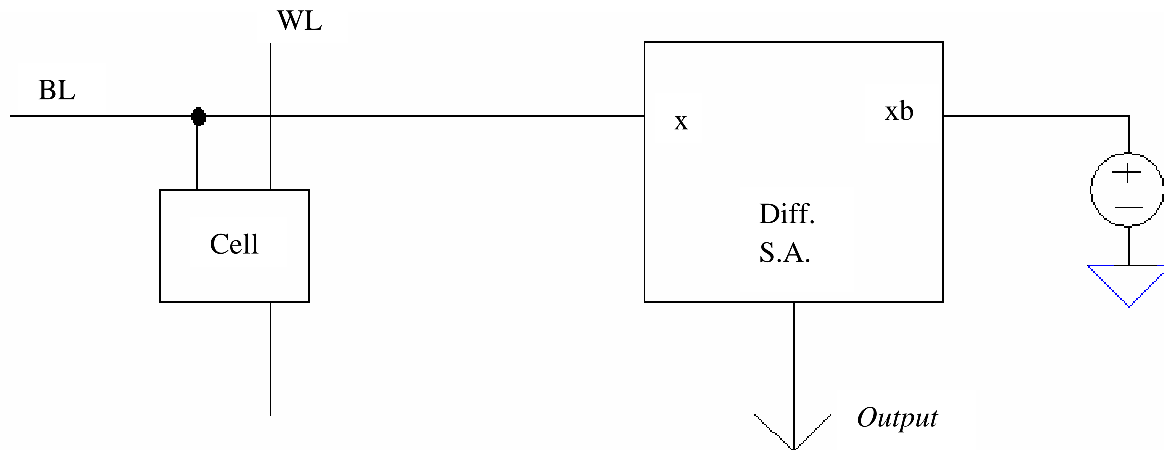


Figure 2.7 Single-to-differential conversion circuit [2].

If a high voltage is present at BL then source voltage should be zero and vice versa. The reference source is designed in such a way that it must be opposite to the BL.

2.6.1.3 DIFFERENTIAL VOLTAGE SENSE AMPLIFIER

A differential amplifier takes small-signal differential inputs (the bit line voltages), and amplifies them to a large signal single-ended output. It is generally known that a differential approach has the advantages over its single-ended counterpart –one of the most important being the common-mode rejection. That is, such an amplifier rejects noise that is equally injected to both inputs. This is especially attractive in memories where the exact values of bit line signal either '1' or '0' is not exactly known and might vary over quite a large range. The impact of those noise signals can be substantial, especially when we realize that the amplitude of the signal to be sensed is generally small. The effectiveness of a differential amplifier is characterized by its ability to reject the common noise and amplify the correct difference between the signals. The signals common to both inputs are suppressed at the output of the amplifier by a ratio called the common mode rejection ratio (CMRR). Similarly, spikes on the power supply are suppressed by a ratio called the power-supply rejection ratio (PSRR). Differential sensing is therefore considered the technique of the choice.

Unfortunately, the differential approach is only directly applicable to SRAMs memories, since these are only the memory cell that offer an accurate differential output. Figure 2.8 shows the most basic differential sense amplifier. Amplification is accomplished with a single stage, based on the current mirroring concept. The input signals (bit and bit bar) are heavily loaded and driven by the SRAM memory cell .The swing on those lines is small as the small memory cell drives a large capacitive load. The inputs are fed to the differential input devices (M1 and M2), and transistor M3 and M4 act as an active current mirror load.

The amplifier is conditioned by the sense amplifier enable signal, SE. Initially, the inputs are precharged and equalized to a common value, while SE is low disabling the sense circuit. Once the read operation is initiated, one of the bit lines drops. SE is enabled when a sufficient differential signal has been established, and the amplifier evaluates. The gain of such the differential-to-single ended amplifier is given by

$$A_{SENSE} = -g_m \; (r_{02} \, r_{04})$$

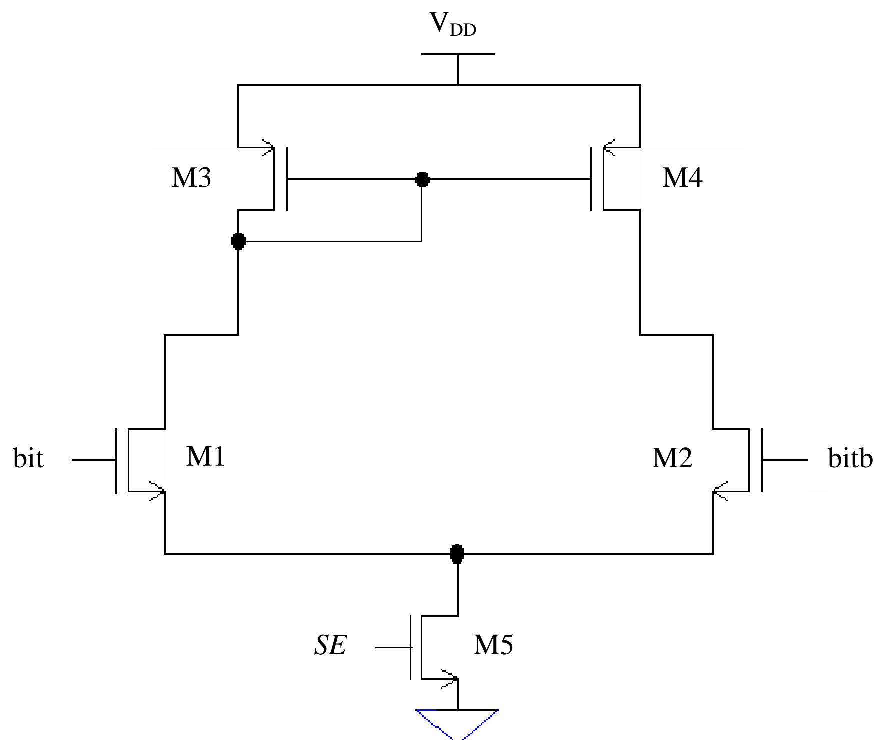


Figure 2.8 Basic differential sense amplifier [2].

Where g_m is the transconductance of the input transistors, and r_{04} the small signal device resistance of the transistor. The r_{04} of the MOS transistor is very high in the saturation region of the MOSFET .The transconductance of the input devices can be increased by either widening the devices, or by increasing the bias current . The latter also reduces the output resistance of M2, which limits the usefulness of this approach. A gain of around 100 can be achieved. However, the gain of sense amplifiers is typically set to around 10. The main goal of the sense amplifier is the rapid production of an output signal. Gain is hence secondary to response time. Multiple stages are required to achieve the desired full swing signal.

2.6.2 CURRENT MODE SENSE AMPLIFIER

Current mode sense amplifier is used to detect the current difference between the bit lines to determine whether a ‘1’ or ‘0’ is stored in the memory cell. It directly measures the cell read current and transfers it to the output circuits. This approach can overcome the restriction of gain reduction brought on by voltage mode sense amplifier at low power supply voltage. The simplest structure of the current mode sense amplifier is described in the following. The conventional current sense amplifier basically consists of four equal sized PMOS transistors as shown in Figure 2.9. It features a current sensing character since it represents a virtual short circuit to the bit lines, which transfer the cell current directly to the output circuits [4].

Figure 2.9 Conventional current mode sense amplifier [4].

Suppose the cell is accessed and, storing a logic “0” in the cell, it draws a current I. The gate source voltage of MP1 will equal that of MP3 since their currents are equal, their sizes are equal, and both transistors are in saturation. This voltage is represented by V1. The same applies to MP2 and MP4. Their gate voltages are represented by V2. It follows that Y_{sel} is grounded, the left bit line will have voltage V1+V2, and the right bit line will also have voltage V1+V2. Therefore the potentials of the two bit lines will be equal and independent of current distribution. This means that there exists a virtual short circuit across the bit lines. Since the bit line voltages are equal, the bit line load currents will also be equal. As the cell draws current I, the right hand leg of the sense amplifier must pass more current then the left leg. The drain currents of MP3 and MP4 are passed through the current conveyor is therefore equal to the cell current. But if a logic ‘1’ is stored in the cell, a current would then flow out of the cell and cause the left hand leg to pass more current than the right hand leg. This difference in current implies a logic ‘1’ is being stored in the cell.

Owing to an intrinsic precharge property, current consumption for the current sense amplifier decreases, yet sensing speed improves. The virtual short circuit character ensures equal bit line voltages, thus eliminating the need for bit line equalization during a read access. The sensing delay is insensitive to bit line capacitances since no capacitor discharging is required to sense the cell data. Therefore, current sense amplifier has better performance than voltage sense amplifier in terms of smaller delay and less current consumption [4].

CHAPTER 3 POWER DISSIPTTION AND ITS REDUCTION IN CMOS CIRCUIT

Power consumption is one of the basic parameters of any kind of integrated circuit (IC). Power and performance are always traded off to meet the system requirements. Power has a direct impact on the system cost. If an IC is consuming more power, then a better cooling mechanism would be required to keep the circuit in normal conditions. Otherwise, its performance is degraded and on continuous use it may be permanently damaged.

3.1 POWER AND ENERGY DEFINATION

It is important at this point, to distinguish between energy and power. The power consumed by a device is, by definition, the energy consumed per unit time. In other words, the energy (*E*) required for a given operation is the integral of the power (*P*) consumed over the operation time (T_{OP}), hence,

$$E = \int_0^{Top} P(t)dt \quad (3.1)$$

Here, the power of digital CMOS circuit is given by

$$P = C\, V_{DD} \quad V_S\, f \quad (3.2)$$

Where, *C* is the capacitance being recharged during a transition. V_{DD} is the supply voltage, V_S is the voltage swing of the signal, and *f* is the clock frequency. If it is assumed that an

operation requires *n* clock cycles, T_{OP} can be expressed as n / f. Hence, Equation (3.2) can be rewritten as

$$E = V_S \quad n \quad CV_{DD}$$

(3.3)

It is important to note that the energy per operation is independent of the clock frequency. Reducing the frequency will lower the power consumption but will not change the energy required to perform a given operation [1]. Since the energy consumption is what determines the battery life, it is imperative to reduce the energy rather than just the power. It is, however important to note that the power is critical for heat dissipation considerations.

The power consumed when the CMOS circuit is in use can be decomposed into two basic classes: static and dynamic.

3.2 STATIC POWER DISSIPATION

The static or steady state power dissipation of a circuit is expressed by the following relation [1]

$$P_{stat} = I_{stat} V_{DD}$$

(3.4)

Where, I_{stat} is the current that flows through the circuit when there is no switching activity. Ideally, CMOS circuits dissipate no static (DC) power since in the steady state there is no direct path from V_{DD} to ground as PMOS and NMOS transistors are never on simultaneously. Of course, this scenario can never be realized in practice since in reality the MOS transistor is not a perfect switch. Thus, there will always be leakage currents and substrate injection currents, which will give to a static component of CMOS power dissipation. For a sub-micron NMOS device $W/L = 10/0.5$, the substrate injection current is of the order of 1- 100 μA for a V_{DD} of 5 V [8].

Another form of static power dissipation occurs for the so-called Ratioed logic. Pseudo-NMOS is an example of a Ratioed CMOS logic family. In this, the PMOS pull-up is always on and acts as a load device for the NMOS pull-down network. Therefore, when the gate

output is in low-state, there is a direct path from V_{DD} to ground and the static currents flow. In this state, the exact value of the output voltage depends on the ratio of the strength of PMOS and NMOS networks – hence the name. The static power consumed by these logic families can be considerable. For this reason, logic families such as this, which experience static power consumption, should be avoided for low-power design. With that in mind, the static component of power consumption in low-power CMOS circuits should be negligible and the focus shifts primarily to dynamic power consumption.

3.3 DYNAMIC POWER DISSIPATION

The dynamic component of power dissipation arises from the transient switching behaviour of the CMOS device. At some point during the switching transient, both the NMOS and PMOS devices will be turned on. This occurs for gate voltages between V_{tn} and V_{DD} - V_{tp}. During this time, a short circuit exists between V_{DD} and ground and the currents are allowed to flow. A detailed analysis of this phenomenon by Veendrick reveals that with careful design of the transition edges, this component can be kept below 10-15% of the total power, this can be achieved by keeping the rise and fall times of all the signals throughout the design within a fixed range (preferably equal). Thus, although short circuit dissipation cannot always be completely ignored, it is certainly not the dominant component of power dissipation in well-designed CMOS circuits. Instead, dynamic dissipation due to capacitance charging consumes most of the power. This component of dynamic power dissipation is the result of charging and discharging of the parasitic capacitances in the circuit.

The situation is modelled in Figure 3.1, where the parasitic capacitances are lumped at the output in the capacitor *C*. Consider the behaviour of the circuit over one full cycle of operation with the input voltage going from V_{DD} to ground and back to V_{DD} again. As the input switches from high to low, the NMOS pull-down network is cut-off and PMOS pull-up network is activated charging load capacitance *C* up to V_{DD}. This charging process draws energy equal to CV_{DD}^2 from the power supply. Half of this is dissipated immediately in the PMOS transistors, while the other half is stored on the load capacitance. Then, when the input returns to V_{DD}, the process is reversed and the capacitance is discharged, its energy being in the NMOS network. In summary, every time a capacitive node switches from ground to V_{DD} (and back to ground), energy of V_{DD}^2 is consumed.

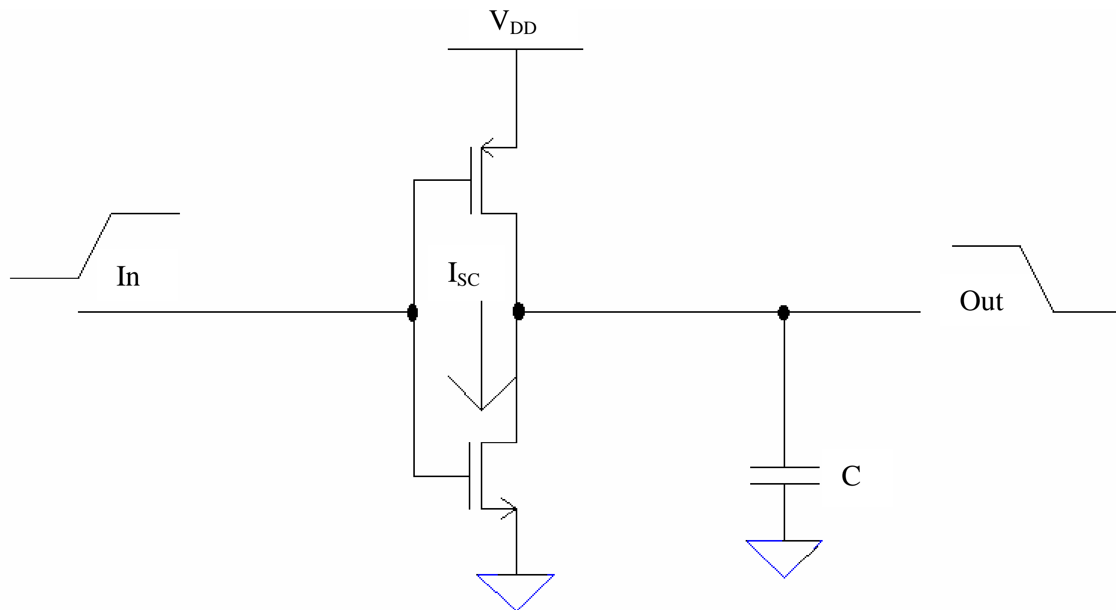


Figure 3.1 CMOS Inverter for Power Analysis.

This leads to the conclusion that CMOS power consumption depends on the *switching activity* of the signals involved. We can define *activity*, *α* as the expected number of zero to one transition per data cycle. If this is coupled with the average data rate, *f*, which may be the clock frequency in a synchronous system, then the effective frequency of nodal charging is given the product of the activity and the data rate: *αf*. This leads to the following formulation for the average CMOS power consumption:-

$$P_{dyn} = \alpha C V_{DD}^2 f \tag{3.5}$$

This classical result illustrates that the dynamic power is proportional to the switching activity, capacitive loading and the square of the supply voltage. In CMOS circuits, this component of power dissipation is by far the most important accounting for at least 90% of the total power dissipation.

So, to reduce the power dissipation, the circuit designer can minimize the switching event, decrease the node capacitance, reduce the voltage swing or apply a combination of these methods. Yet, in all these cases, the energy drawn from the power supply is used only once before being dissipated. To increase the energy efficiency of the logic circuits, other measures can be introduced for recycling the energy drawn from the power supply.

3.4 POWER REDUCTION

For a CMOS circuit, the total power mode, the power dissipation is due to the standby leakage current. For dynamic power dissipation, there are two components. One comes from the switching power due to charging and discharging of load capacitance. The other is short circuit power due to the nonzero rise and fall time of input waveforms. The static power of a CMOS circuit is determined by the by the leakage current through each transistor. The dynamic power (P_D) and leakage power (P_{LEAK}) are expressed as

$$P_D = \alpha \, C V_{DD}^2 f \tag{3.6}$$

$$P_{LEAK} = I_{LEAK} \cdot V_{DD} \tag{3.7}$$

Where α is the switching activity, f is the operational frequency, C is the load capacitance, V_{DD} is the supply voltage, and I_{LEAK} is the cumulative leakage current due to all components of the leakage current.

The dynamic power dissipation of the circuit can be overcome by reducing load capacitance and power supply V_{DD}. If the supply is reduced the delay of the circuit will increase and circuit will effected badly. If the threshold voltage V_{th} is reduced then the leakage current of the circuit will increase and hence the static power.

3.5 POWER REDUCTION TECHNIQUES

Any circuit used in the designing is preferred on the basis of its characteristics, so the circuit should have high speed, gain, less delay, and less power dissipation. There are different techniques which are used for the low power dissipation.

3.5.1 MULTITHRESHOLD-VOLTAGE CMOS (MTCMOS)

The multithreshold-voltage CMOS (MTCMOS) circuit was proposed by inserting high threshold devices in series into low V_{th} circuitry. Figure 3.2 shows the schematic of an MTCMOS circuit. A sleep control scheme is introduced for efficient power management.

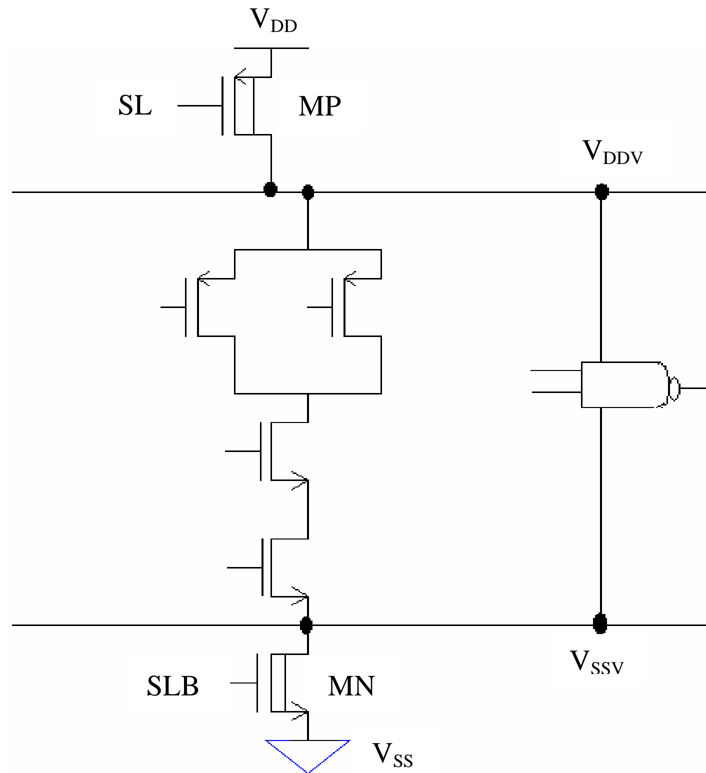


Figure 3.2 Multi-threshold CMOS (MTCMOS) [8].

Two high V_T transistors are used, high V_T PMOS is connected to the power supply, where NMOS is connected to the ground. Due to these transistors a virtual power supply and ground are appeared respectively on the drain terminal nodes of the both transistors. In the active mode, SL is set low and sleep control high-V_{th} (MP and MN) are turned on. Since their on-resistance are small, the virtual supply voltage (V_{DDV} and V_{SSV}) almost function as real power lines. In the standby mode, SL is set high, MN and MP are turned off and the leakage current is very low. In this only one type of high V_{th} transistor is enough for leakage control [5].

3.5.2 VARIABLE THRESHOLD CMOS (VTCMOS)

Variable threshold CMOS (VTCMOS) is a body biasing design technique. Figure 3.3 shows the VTMOS scheme. In order to achieve different threshold voltages, a self substrate bias circuit is used to control the body bias. In the active mode, a nearly zero body bias is applied.

While in standby mode, a deeper reverse body bias is applied to increase threshold voltage and to cut off leakage current. Furthermore, in active mode, a slightly forward substrate bias can be used to increase the circuit speed while reducing short channel effect.

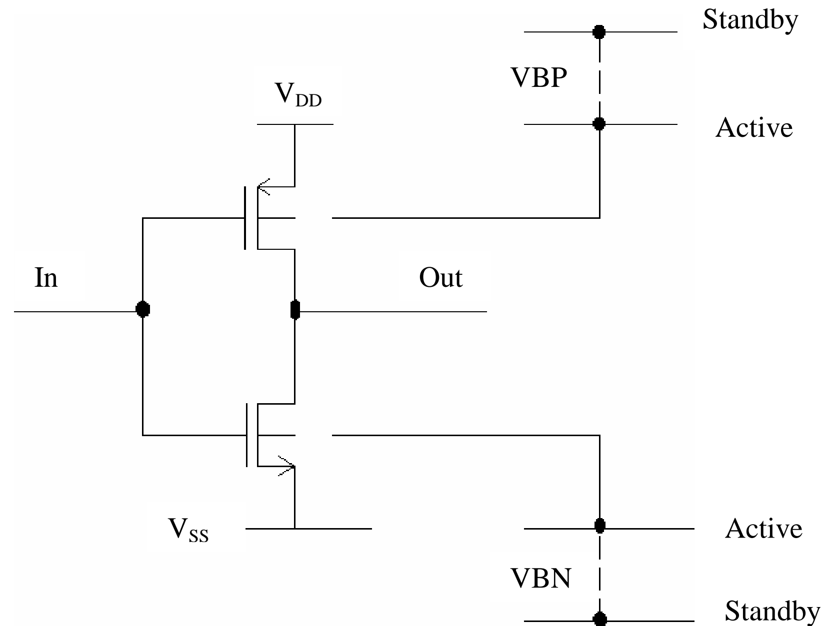


Figure 3.3 Variable threshold CMOS (VTCMOS) [5].

3.5.3 DYNAMIC THRESHOLD CMOS (DTCMOS)

For dynamic threshold CMOS, the threshold voltage is altered dynamically to suit the operating state of the circuit. A high threshold voltage in the standby mode gives low leakage current, while a low threshold voltage allows for higher current drives in the active mode of operation.

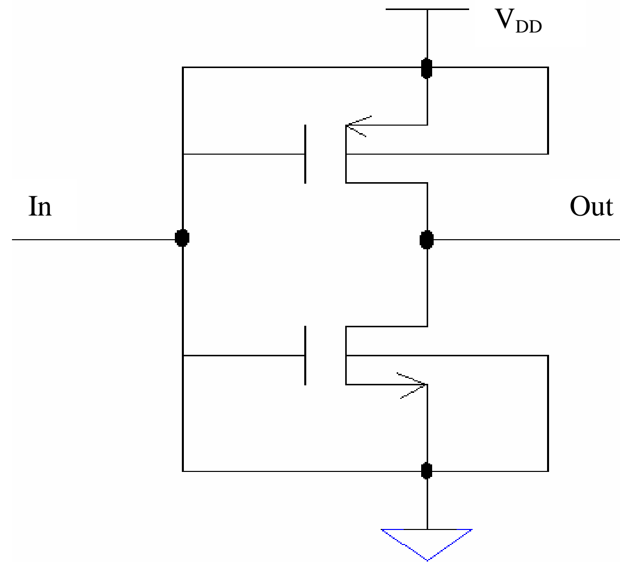
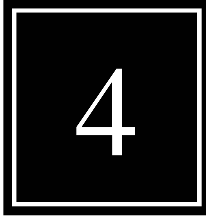


Figure 3.4 Dynamic threshold CMOS (DTCMOS) [5].

Dynamic threshold CMOS can be achieved by tying the gate and body together DTMOS. Figure 3.4 shows the schematic of a DTMOS inverter. DTMOS can be developed in bulk technologies by using triple wells. Stronger advantage of DTMOS can be seen in partially depleted Silicon-on-Insulator (SOI) devices.

The supply voltage of DTMOS is limited by the diode built-in-potential. The *pn* diode between source and body should be reverse biased. Basically, this technique is only suitable for ultra-low voltage (0.6 and below) circuits [5].

CHAPTER



DESIGN OF SENSE AMPLIFIER AND SIMULATION

In the design of the memory cell, for obtaining the better results like less power dissipation minimum delay sense amplifiers are used. Different types of sense amplifiers are used in memory design according to their performance. The delay of the sense amplifier should be very small so that it can detect even the small change on the bit lines as the read and write operation get starts. Sense amplifier reduces the power dissipation of the whole circuit. While design the sense amplifier, it is kept in mind that the delay and power dissipation remain minimum. This chapter describes the design of voltage and current mode sense amplifiers and compare their simulation results.

4.1 TOOL AND TECHNOLOGY USED

As the number of components on a single chip and technology both are increasing and keep on increasing. It is very important for a designer that on which technology and on which tool he designed the circuit. As the design technology increases, the delay time decrease but the leakage current of the circuit increases. As the feature size of technology decreases the threshold voltage of the MOS decreases, due to the decreases of the threshold voltage MOS turned on at the lower voltage so the delay of the circuit decreases and also the power dissipation as the supply voltage decreases. For the design of voltage and current mode sense amplifiers in this chapter, the 0.18 technology is used.

Tool used in the design of the circuit plays a very important role. The design of the circuit also depends on the tool used in designing that what is the response time for simulating the

schematic, it is easy to handle or working with it. Parameters and the characteristics of the circuit are depends on the tool. Mentor graphics is used for the design of the different types of sense amplifiers in this chapter.

4.2 6T SRAM DESIGN WITH PRECHARGE CIRCUIT

Preacharge circuit is used in the memory design for pull up or charging of the bit lines. The 6T SRAM cell with the precharge circuit is shown in the Figure 4.1. Transistors M7 and M9 are used for the charging of the bit lines up to the V_{DD}. Bit lines are connected to the supply voltage through the PMOS. When the clock given to the transistors M7 and M9 is low, then both the transistors are turned on and charging of the bit lines takes place.

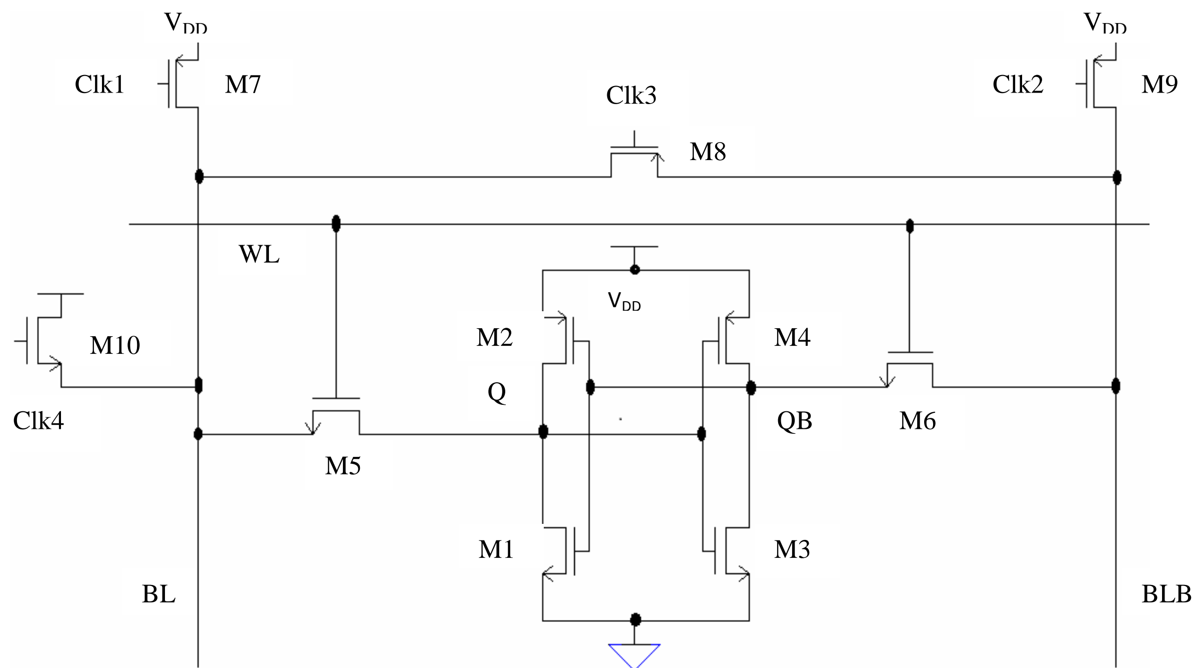


Figure 4.1 6T SRAM with the precharge circuit.

Transistor M8 is used in the circuit for the equalization of the voltage present at the bit lines. This transistor remains on only during the read operation, during the write operation it remains off. Transistor M10 is used for providing the low level of voltage at one of the bit line. This transistor remains on during the write operation, during the read operation it remains off. Transistors M5 and M6 are the access transistors which are connected to the

word and bit lines. Transistors M1, M2 and M3, M4 are connected to form cross coupled inverters.

4.2.1 SIMULATION RESULTS OF SRAM MEMORY

The 6T SRAM is shown in the above Figure. Different clocks are applied on the inputs of the precharge circuit transistors. The clock given to the WL is shown in Figure 4.2. The voltage level of the word line remains low during the 0 to 20ns. During this time period transistors M7 and M9 are turned on as the clock at their input is low. The clock given to the inputs of these transistors are shown in Figures 4.3 and 4.4 respectively. During this time period, a value '0' is stored at QB and a value '1' is stored at Q. During this time period 0 to 20ns transistor M10 is in off state and transistor M8 is in on state for the voltage equalization on the bit lines. The clock given to the transistors M8 and M10 are shown in Figures 4.5 and 4.6 respectively.

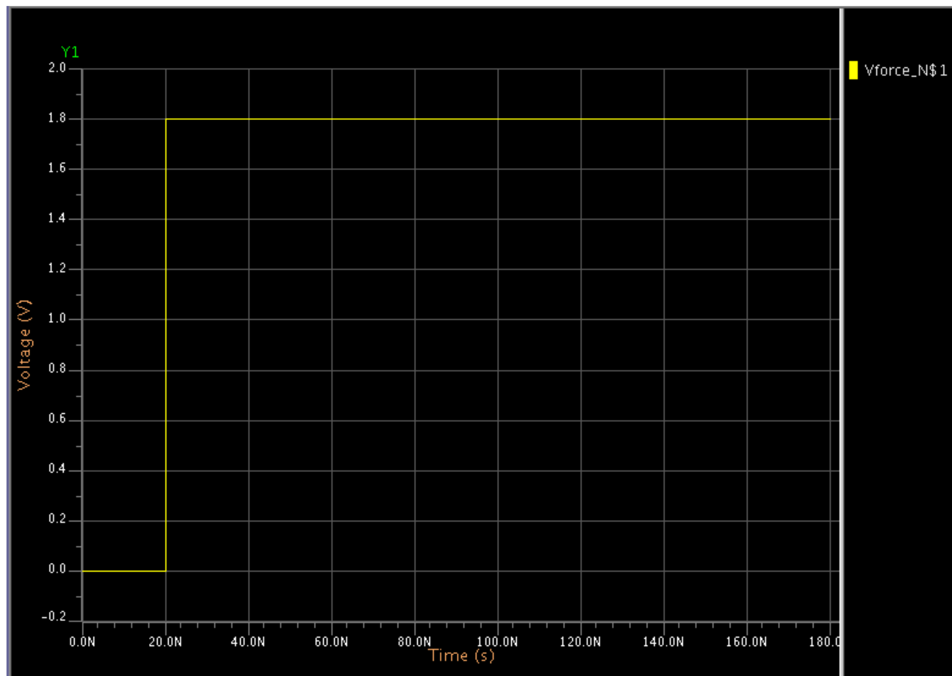


Figure 4.2 Clock given to the word line.

For the write operation, one of the bit lines should be at low voltage level. As the voltage of the word line becomes high, write operation starts. The write operation is performed during the time period 20 to 90ns. During this time period, transistor M10 become on and a low

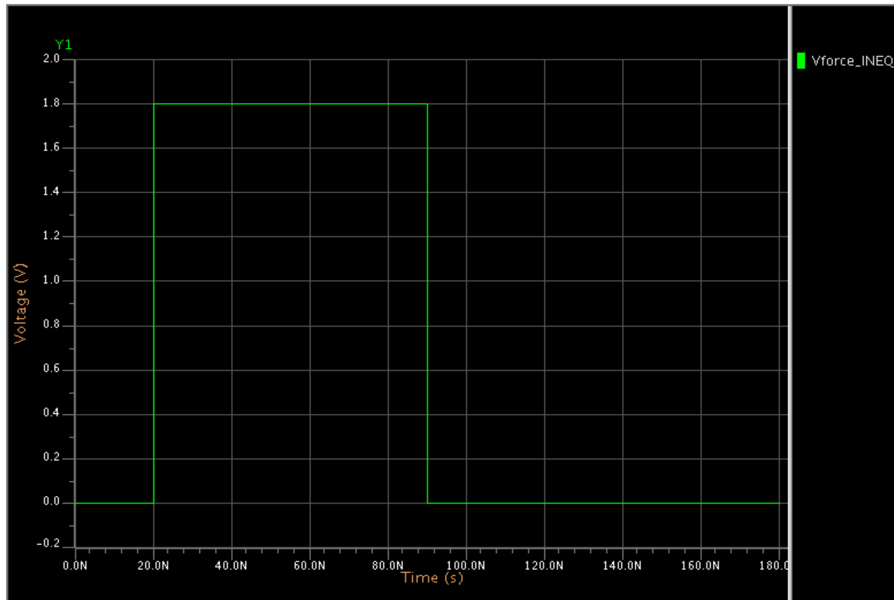


Figure 4.3 Clock given to the transistor M7.

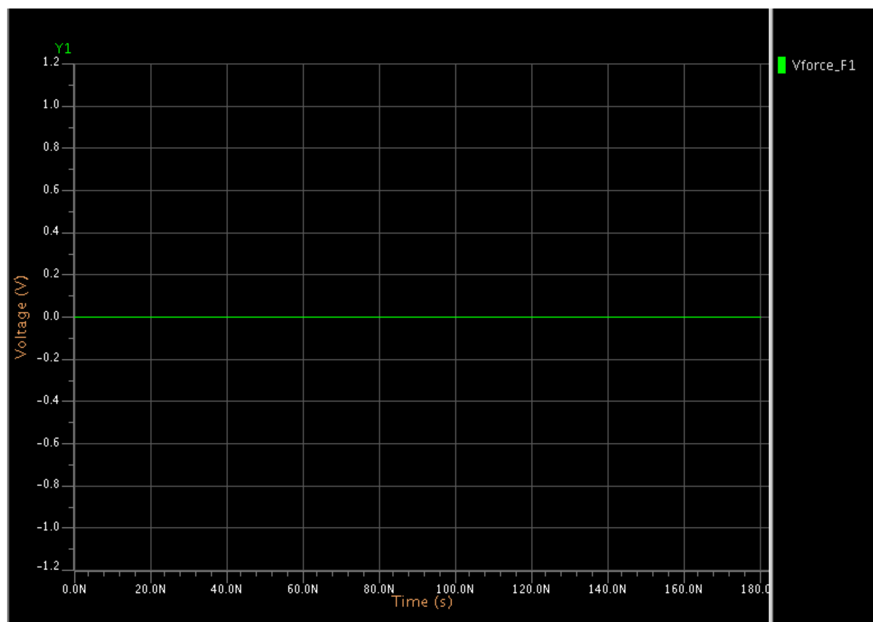


Figure 4.4 Clock given to the transistor M9.

Voltage level is set on the BL as the transistor M7 is off during this time period. The voltage at the BL is very low and transistor M5 is on, so the node Q discharges through transistor M5and BL start charging. In this way a value '0' is stored at node Q. The simulation result of the write cycle is shown in Figure 4.7. A value '1' is stored at time 20ns and as the write cycle starts '0' is stored in the memory cell.

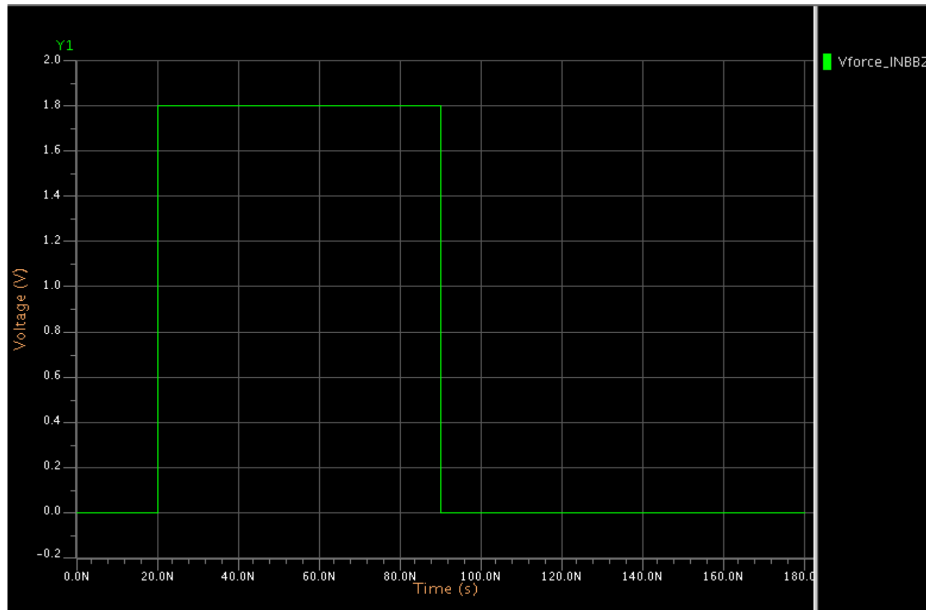


Figure 4.5 Clock given to the transistor M8.

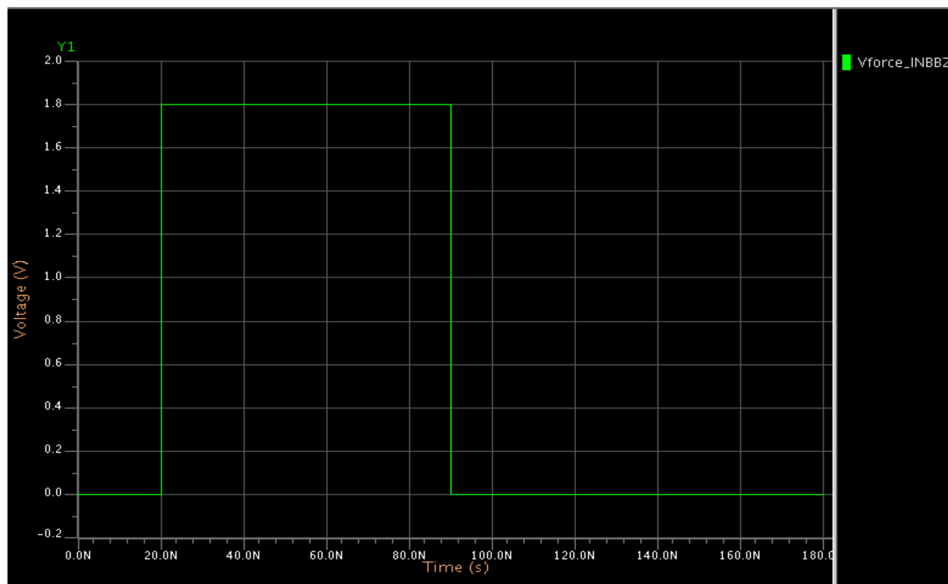


Figure 4.6 Clock given to the transistor M10.

For the read operation, both the bit lines should be high. Read operation is performed during the time period 90 to 180ns. During this time period transistor M8 turn on, transistor M7 is in on state and transistor M10 remains in off state. At this time, both the bit lines are precharged up to the power supply and both the access transistors are on. The value stored at the node QB is ‘1’, due to which transistor M1is turned on and the BL is discharges through the transistors M1 and M5. The simulation results are shown in Figure 4.7.

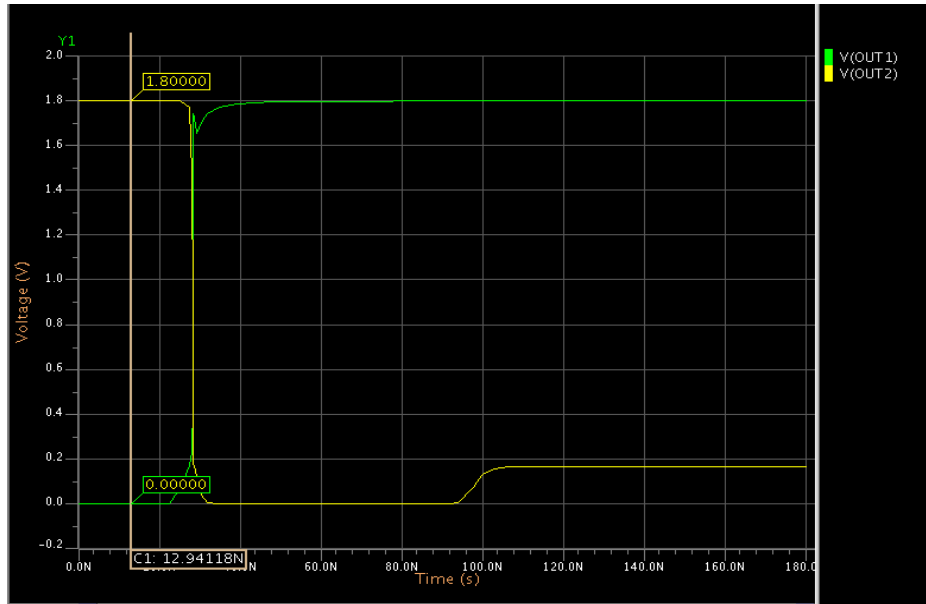


Figure 4.7 Simulated results of read and write cycles.

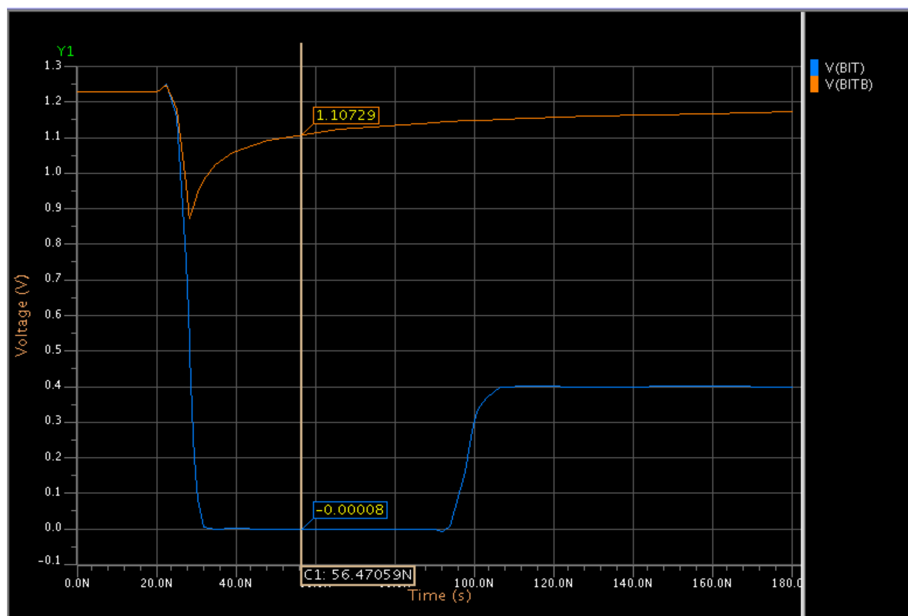


Figure 4.8 Simulated results of the voltage at the bit lines.

During the read and write cycle, the voltages at the bit lines are shown in Figure 4.8. It is very clear from the waveforms that there is only a small voltage difference between the bit lines. This is very difficult for a circuit to recognise these bit line voltages as ‘0’ and ‘1’. None of the bit line is either low or high. To overcome this problem sense amplifiers are used.

4.3 DESIGN OF VOLTAGE MODE SENSE AMPLIFIER

Sense amplifier is the main part of the memory design. Voltage mode sense amplifiers detect the low voltage level signal from the bit lines and produce a high swing signal as an output. A design circuit of voltage mode sense amplifier is shown in Figure 4.9. In this, transistors M5 and M6 are the input transistors. These transistors are connected to the bit lines. Output is taken through the cross coupled inverter via S0 and SON. Two extra transistors are connected in parallel to the PMOS transistors. The circuit is connected to the ground through transistor M9. The gate of this transistor is connected with the transistors M7 and M8. A clock is applied on the input of these transistors.

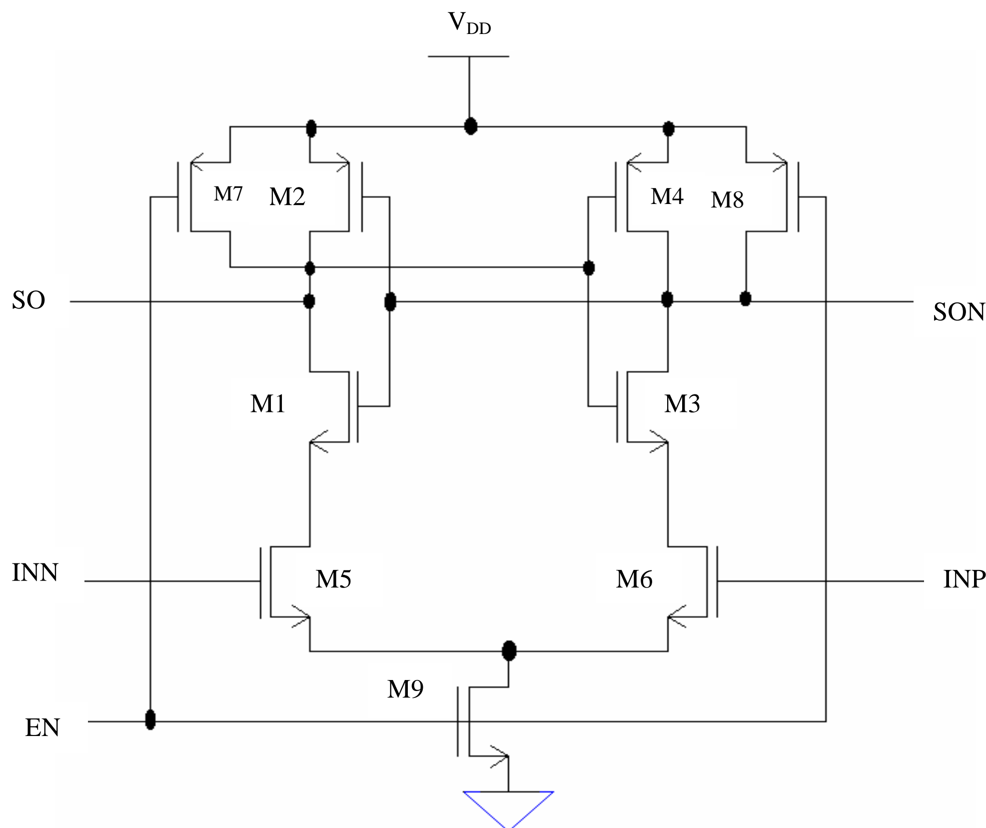


Figure 4.9 Voltage mode sense amplifier.

4.3.1 SIMULATION RESULTS

Bit lines are connected to the input of the sense amplifier. A clock is given at the signal EN. When the signal is low, transistors M7 and M8 will turned on and the transistor M9 will remain in off state. Due to these transistors M1 and M3 will turned on. If the input INN is

low, transistor M5 will be off and if the EN signal is high then there will be no path to ground and a high voltage will be obtained as an output at SO node and a low output at SON node. This is shown in Figure 4.10.

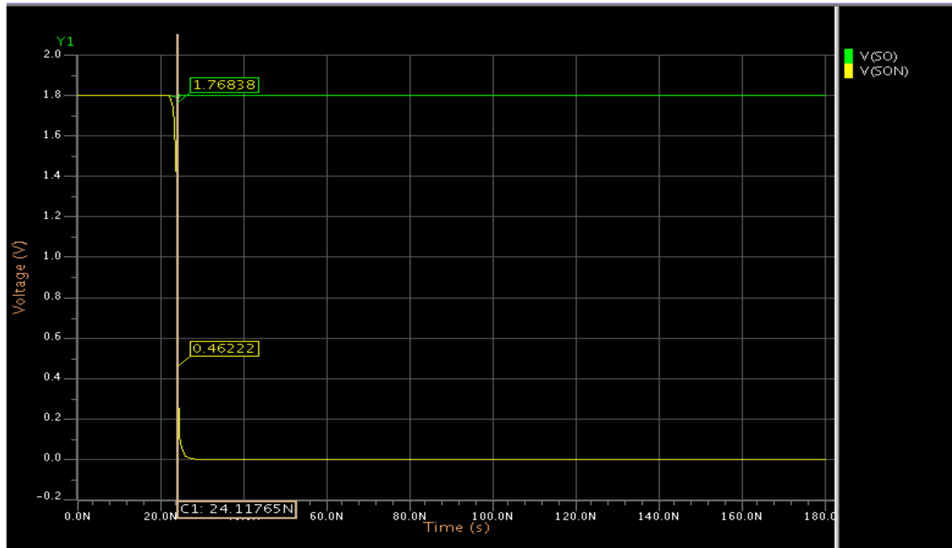


Figure 4.10 Output of the voltage mode sense amplifier without bit line capacitances.

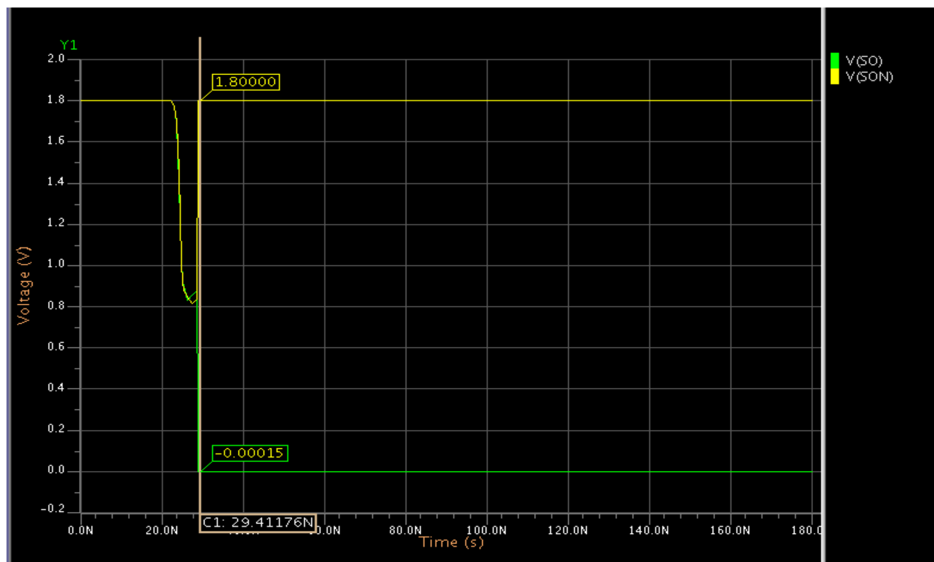


Figure 4.11 Output of voltage mode sense amplifier with 0.2 *pf* bit line capacitances.

The voltage sense amplifier depends on the bit line capacitances. As the bit line capacitances of the memory cell increases the delay also increases. This is shown in Figures 4.11. This is shown in this Figures that as the capacitance increases delay also increases. The waveform

obtained in Figure 4.10 is without any capacitances. The delay obtained is 4.1ns. If the capacitance is 0.2 *pf* then the delay is more than 9ns. This circuit dissipates 243.8µW power. Layout of voltage mode sense amplifier is shown in Figure 4.12.

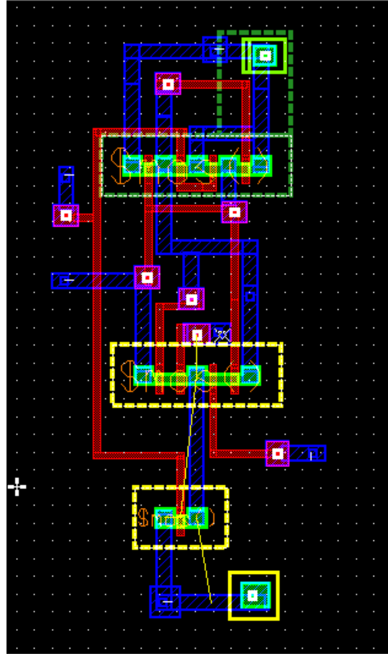


Figure 4.12 Layout of voltage mode sense amplifier.

4.4 DESIGN OF CURRENT MODE SENSE AMPLIFIER

The delay of the voltage mode sense amplifier increases as increases of the capacitances. So, voltage mode sense amplifier is not the perfect choice where the time is primary concern. This designed sense amplifier is based on the current mode approach. The sensing speed is independent of the bit line and data line capacitances and a separated positive feedback technique is employed to give the circuit high speed, low power operation. As the density of memory devices increases, certainly the associated parasitic capacitances also increase. Large capacitive loads cause a major sensing delay in memory devices, so high speed sense amplification of small memory cell signals is the key to achieving a fast access time in SRAM. Conventional sense amplifiers are based on voltage sensing techniques, which are sensitive to parasitic capacitance. Recent approaches to designing sense amplifiers employs current sensing techniques the advantages in term of speed are obvious and very attractive,

especially if the supply voltage is low and the memories are large. A current-mode sense amplifier using MTCMOS technology, which gives fast access time and low power consumption, is presented. In addition, it is insensitive to both bit-line and data-line capacitances.

The circuit is shown in Figure 4.13. This design is based on the multi threshold voltage CMOS technique. A high V_T PMOS transistor P2 is connected to the power supply which generates a voltage near to supply voltage at the node T. The current conveyor (P3-P6) used in the conventional current sense amplifier is adopted for column sensing. The pre-charge equalizing device is omitted because the current conveyor intrinsically keeps the bit-line at equal potentials once CL is initiated. The N5-N6 and P7-P8 are formed in ways similar to positive feedback latches. N1 and N2 connect the input nodes and pull down the data-lines close to the ground level. The transistors N7 and N8 are the separating transistors and the transistors N3 and N4 are the equalization transistors. The data-line capacitance are represented by CDL, CL is the column-line selector signals.

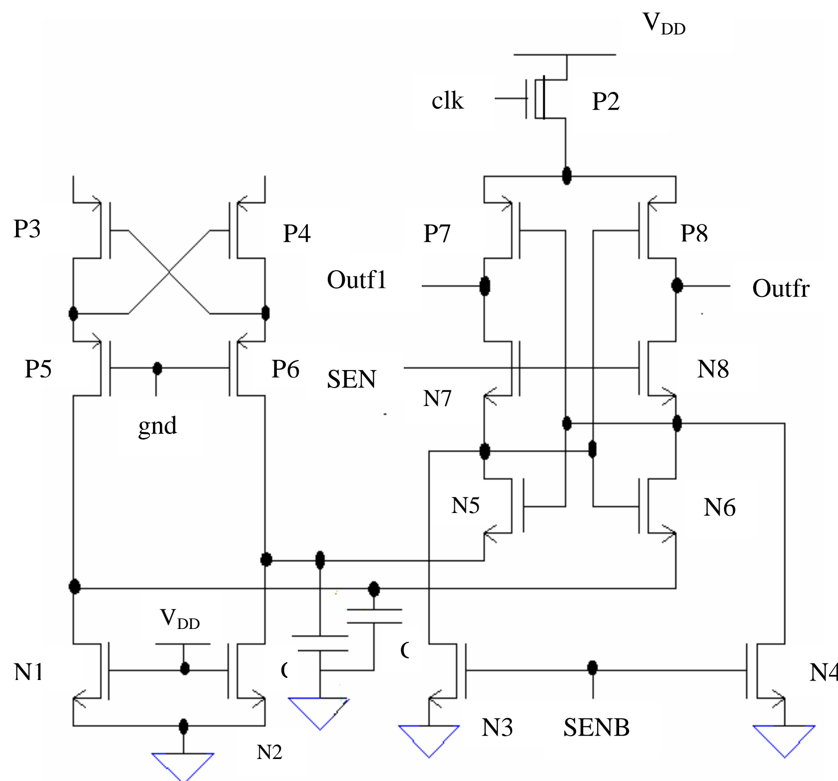


Figure 4.13 Current mode sense amplifier with MTCMOS technique.

The inputs to the current- mode cross-coupled latch are at the sources of the N5 and N6. Due to the low impedance at the input nodes, the current signals at the data-lines are injected to

the cross-coupled latch without charging or discharging of the data-line capacitances. Therefore the sensing speed is insensitive to both bit line and data-line capacitances.

4.4.1 SIMULATION RESULTS

The design is based on the MTCMOS technique. In this technique, a high V_T PMOS is connected to the power supply. A clock signal is applied at the input of this transistor. This clock is shown in Figure 4.14. This PMOS will be turned on only when the circuit required the power supply otherwise it will be off. Power supply is not connected to the circuit when PMOS is off, in this way power dissipation is reduced. It provides a virtual voltage at node T.

During the time period 0 to 20ns the circuit is in standby mode. When the sense amplifier is in the standby state, the signal “SENB” is at high-level and the signal “SEN” is at low-level. In this condition, the N3 and N4 are turned on, so the nodes A and B are pulled down to low-level. Hence, the N5 and N6 are at the cut-off state, and the P7 and P8 are operated in the linear region due to their gate voltages being at low level. Since the “SEN” is at low-level, the N7 and N8 are at the cut-off state, which separates the cross coupled latch, therefore, there is no DC current flow in the sense amplifier.

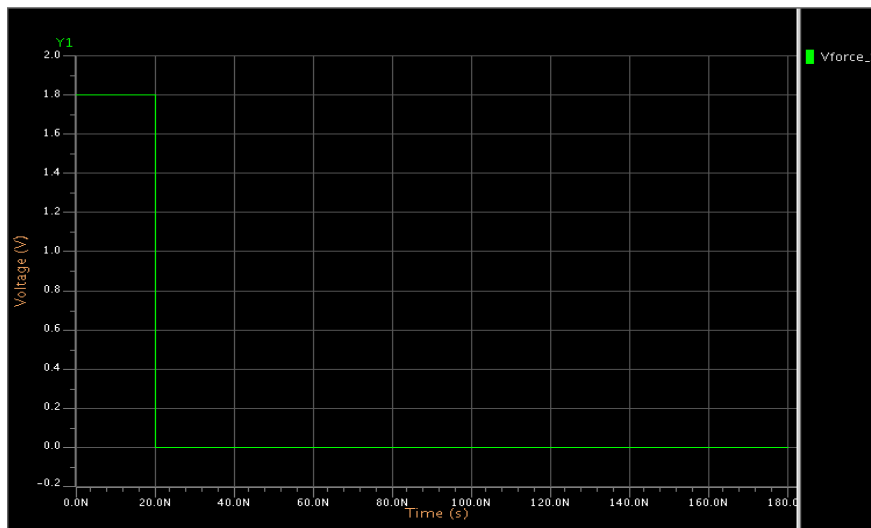


Figure 4.14 Clock given to the high V_T PMOS.

During the time period 20 to 180ns the circuit is in active mode. During the read operation, both WL and CL lines are activated. The “SENB” is at low-level, which turns off N3 and N4,

and the "SEN" is at high-level to turn on the cross-coupled latch. When a particular memory cell is accessed, a differential current signal appears at the common bit-lines BL and BLB. The current conveyor (P3-P6) transports the differential currents to the data-line. Because the output nodes of the cross-coupled latch are at high-level, at the standby state, there is a large current driven by P7 and P8 and a particular result is obtained at the output. The simulation results are shown in Figure 4.15.

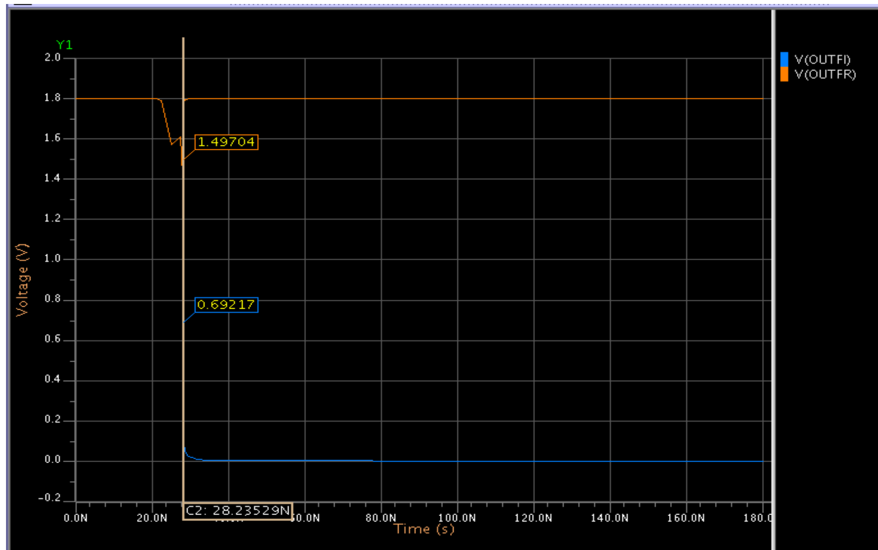


Figure 4.15 Output of the current mode sense amplifier.

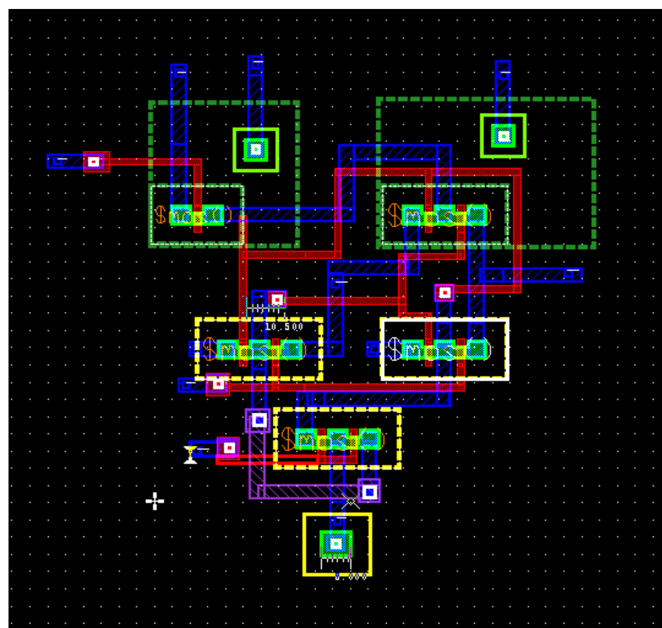


Figure 4.16 Layout of the current mode sense amplifier.

It is observed from the Figure 4.15 that a delay of only 8.2ns is obtained using current mode sense amplifier as it is independent of the capacitances. The sense amplifier differentiates the both voltages after a delay of 8.2ns as the WL is activate at 20ns and sense amplifier amplify and detect the signals at 28.2ns. This current mode sense amplifier using MTCMOS technique dissipates only 73.37µW power. Layout of the current mode sense amplifier is shown in Figure 4.16.

4.5 RESULT SUMMARY

It is proved that the delay in current mode sense amplifier is very less as compare to the voltage mode sense amplifier. Current sensing is independent of the bit line and word lines capacitances where voltage mode sense amplifier depends on the capacitances. The delay in the voltage mode sense amplifier increases as increases in the capacitances. Comparison of delay and power dissipation of current mode and voltage mode sense amplifier is shown in Table 4.1.

Table 4.1 Comparison of current mode sense amplifier and voltage mode sense amplifier

CAPACITANCE (pF)	VOLTAGE MODE SENSE AMPLIFIER		CURRENT MODE SENSE AMPLIFIER		CURRENT MODE SENSE AMPLIFIER USING MTCMOS	
	DELAY (ns)	POWER DISSIPATION (μW)	DELAY(ns)	POWER DISSIPATION (μW)	DELAY(ns)	POWER DISSIPATION (μW)
0.0	4.1	243	8.2	0.23	8.2	0.073
0.1	6.5	243	8.2	0.23	8.2	0.073
0.2	9.5	243	8.2	0.23	8.2	0.073

As shown in the table that the power dissipation of the current mode sense amplifier is much lower than the voltage mode sense amplifier. It is also observed that voltage mode sense amplifier has less delay where the bit line capacitances is very small and the current mode sense amplifier is independent of the capacitances.

CHAPTER

CONCLUSION AND FUTURE SCOPE

CONCLUSION

- The simulation results show that the delay of the voltage mode sense amplifier is 9.5ns whereas the delay of current mode sense amplifier is 8.2ns. So the delay of the sense amplifier using current mode can be reduced by 86%.
- The power dissipation of the voltage mode sense amplifier is 243µW and the power dissipation of the current mode sense amplifier is 0.21µW. Hence, the power dissipation of sense amplifier can be reduced 1000 times using current mode operation.
- The power dissipation of the circuit can be further reduced using MTCMOS technique in current mode sense amplifier. The power dissipation using this technique is 0.73µW. Therefore, the power is reduced by 33% as compare to simple current mode sense amplifier.
- Also for smaller memories voltage mode sense amplifier shows about 50% better performance than current mode sense amplifier.

FURURE SCOPE

The power dissipation and delay of the sense amplifier circuit can be further reduced by using several low power and high speed techniques like VTCMOS, DTCMOS and Adaptive CMOS. As we go for the higher technology the leakage power dissipation becomes a severe problem. By using these techniques this problem can be solved significantly. Also different

sense amplifier circuits using low power and high speed design techniques can be employed for reducing the power dissipation and delay of the memory.

REFERENCES

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APPENDIX A

LVS FOR VOLTAGE MODES SENSE AMPLIFIER

```
##################################################
##                    ##
##    C A L I B R E   S Y S T E M    ##
##                    ##
##      L V S   R E P O R T      ##
##                    ##
##################################################
```

REPORT FILE NAME: himvoltagesram_1_anand.lvs.report
LAYOUT NAME: himvoltagesram_1_anand.calibre.gds
SOURCE NAME:
/home/student/himvoltagesram_1_anand/himvoltagesram_1_anand.src.net
('himvoltagesram_1_anand')
RULE FILE: /home/student/_tsmc018.rules_
LVS MODE: Mask
RULE FILE NAME: /home/student/_tsmc018.rules_
CREATION TIME: Mon Jun 28 15:20:32 2010
CURRENT DIRECTORY: /home/student
USER NAME: student
CALIBRE VERSION: v2006.2_30.26 Fri Jul 7 22:37:10

```
*************************************************************************************************************
OVERALL COMPARISON RESULTS
*************************************************************************************************************

     #     ###################    _   _
    #      #                #     *   *
 #  #      #    CORRECT     #       |
  ##       #                #     \___/
   #       ###################
```

--

INITIAL NUMBERS OF OBJECTS

	Layout	Source	Component Type
Ports:	7	7	
Nets:	10	10	
Instances:	5	5	MN (4 pins)
	4	4	MP (4 pins)
Total Inst:	9	9	

NUMBERS OF OBJECTS AFTER TRANSFORMATION

	Layout	Source	Component Type
Ports:	7	7	
Nets:	8	8	
Instances:	1	1	MN (4 pins)
	4	4	MP (4 pins)
	2	2	SMN2 (4 pins)
Total Inst:	7	7	

****
****

LVS PARAMETERS

****
****

o LVS Setup:

// LVS COMPONENT TYPE PROPERTY
// LVS COMPONENT SUBTYPE PROPERTY

```
// LVS PIN NAME PROPERTY
// LVS POWER NAME
// LVS GROUND NAME
LVS CELL SUPPLY                                 NO
LVS RECOGNIZE GATES                             ALL
LVS IGNORE PORTS                                NO
LVS CHECK PORT NAMES                            NO
LVS IGNORE TRIVIAL NAMED PORTS                  NO
LVS BUILTIN DEVICE PIN SWAP                     YES
LVS ALL CAPACITOR PINS SWAPPABLE                NO
LVS DISCARD PINS BY DEVICE                      NO
LVS SOFT SUBSTRATE PINS                         NO
LVS INJECT LOGIC                                NO
LVS EXPAND UNBALANCED CELLS                     YES
LVS EXPAND SEED PROMOTIONS                      NO
LVS PRESERVE PARAMETERIZED CELLS                NO
LVS GLOBALS ARE PORTS                           YES
LVS REVERSE WL                                  NO
LVS SPICE PREFER PINS                           NO
LVS SPICE SLASH IS SPACE                        YES
LVS SPICE ALLOW FLOATING PINS                   YES
LVS SPICE ALLOW UNQUOTED STRINGS                NO
LVS SPICE CONDITIONAL LDD                       NO
LVS SPICE CULL PRIMITIVE SUBCIRCUITS            NO
LVS SPICE IMPLIED MOS AREA                      NO
// LVS SPICE MULTIPLIER NAME
LVS SPICE OVERRIDE GLOBALS                      NO
LVS SPICE REDEFINE PARAM                        NO
LVS SPICE REPLICATE DEVICES                     NO
LVS SPICE STRICT WL                             NO
// LVS SPICE OPTION
LVS STRICT SUBTYPES                             NO
LAYOUT CASE                                     NO
SOURCE CASE                                     NO
LVS COMPARE CASE                                NO
LVS DOWNCASE DEVICE                             NO
LVS REPORT MAXIMUM                              50
LVS PROPERTY RESOLUTION MAXIMUM                 32
// LVS SIGNATURE MAXIMUM
// LVS FILTER UNUSED OPTION
// LVS REPORT OPTION
LVS REPORT UNITS                                YES
// LVS NON USER NAME PORT
// LVS NON USER NAME NET
// LVS NON USER NAME INSTANCE

// Reduction
```

```
LVS REDUCE SERIES MOS                          NO
LVS REDUCE PARALLEL MOS                        YES
LVS REDUCE SEMI SERIES MOS                     NO
LVS REDUCE SPLIT GATES                         YES
LVS REDUCE PARALLEL BIPOLAR                    YES
LVS REDUCE SERIES CAPACITORS                   YES
LVS REDUCE PARALLEL CAPACITORS                 YES
LVS REDUCE SERIES RESISTORS                    YES
LVS REDUCE PARALLEL RESISTORS                  YES
LVS REDUCE PARALLEL DIODES                     YES
LVS REDUCTION PRIORITY                         PARALLEL

// Filter

LVS FILTER  sch_filter_direct_open  OPEN SOURCE DIRECT
LVS FILTER  sch_filter_direct_short  SHORT SOURCE DIRECT
LVS FILTER  sch_filter_mask_open  OPEN SOURCE MASK
LVS FILTER  sch_filter_mask_short  SHORT SOURCE MASK
LVS FILTER  lay_filter_direct_open  OPEN LAYOUT DIRECT
LVS FILTER  lay_filter_direct_short  SHORT LAYOUT DIRECT
LVS FILTER  v OPEN
LVS FILTER  i  OPEN
LVS FILTER  e  OPEN
LVS FILTER  f  OPEN
LVS FILTER  g  OPEN
```

****

INFORMATION AND WARNINGS

****

	Matched Layout	Matched Source	Unmatched Layout	Unmatched Source	Component Type
	-------	-------	---------	---------	---------
Ports:	7	7	0	0	
Nets:	8	8	0	0	
Instances:	1	1	0	0	MN(N)
	4	4	0	0	MP(P)
	2	2	0	0	SMN2
	-------	-------	---------	---------	
Total Inst:	7	7	0	0	

o Initial Correspondence Points:

Ports: gnd vdd inp so son ena inn

****

SUMMARY

****

Total CPU Time: 0 sec
Total Elapsed Time: 0 sec

APPENDIX B

LVS REPORT FOR CURRENT MODE SENSE AMPLIFIER

```
##################################################
##                        ##
##    C A L I B R E   S Y S T E M      ##
##                        ##
##      L V S   R E P O R T        ##
##                        ##
##################################################
```

REPORT FILE NAME: himanshusensemem_1_anand.lvs.report
LAYOUT NAME: himanshusensemem_1_anand.calibre.gds
SOURCE NAME:
/home/student/himanshusensemem_1_anand/himanshusensemem_1_anand.src.net
('himanshusensemem_1_anand')
RULE FILE: /home/student/_tsmc018.rules_
LVS MODE: Mask
RULE FILE NAME: /home/student/_tsmc018.rules_
CREATION TIME: Wed Jun 23 17:07:23 2010
CURRENT DIRECTORY: /home/student
USER NAME: student
CALIBRE VERSION: v2006.2_30.26   Fri Jul 7 22:37:10 06

```
**************************************************************************
**************************************
                OVERALL COMPARISON RESULTS
**************************************************************************
**************************************


     #     ###################     _  _
    #      #              #      *   *
 #  #      #   CORRECT    #        |
  # #      #              #      \___/
   #       ###################
```

```
--------------------------------------------------------------------------------------------------------
--

NUMBERS OF OBJECTS
------------------

                   Layout   Source        Component Type
                   ------   ------        --------------
Ports:               11       11

Nets:                14       14

Instances:            6        6          MN (4 pins)
                      3        3          MP (4 pins)
                   ------   ------
Total Inst:           9        9


**********************************************************************************************************
                    LVS PARAMETERS
**********************************************************************************************************


o LVS Setup:

   // LVS COMPONENT TYPE PROPERTY
   // LVS COMPONENT SUBTYPE PROPERTY
   // LVS PIN NAME PROPERTY
   // LVS POWER NAME
   // LVS GROUND NAME
   LVS CELL SUPPLY                                     NO
   LVS RECOGNIZE GATES                                 ALL
   LVS IGNORE PORTS                                    NO
   LVS CHECK PORT NAMES                                NO
   LVS IGNORE TRIVIAL NAMED PORTS                      NO
   LVS BUILTIN DEVICE PIN SWAP                         YES
   LVS ALL CAPACITOR PINS SWAPPABLE                    NO
   LVS DISCARD PINS BY DEVICE                          NO
   LVS SOFT SUBSTRATE PINS                             NO
   LVS INJECT LOGIC                                    NO
   LVS EXPAND UNBALANCED CELLS                         YES
   LVS EXPAND SEED PROMOTIONS                          NO
   LVS PRESERVE PARAMETERIZED CELLS                    NO
```

```
LVS GLOBALS ARE PORTS                          YES
LVS REVERSE WL                                 NO
LVS SPICE PREFER PINS                          NO
LVS SPICE SLASH IS SPACE                       YES
LVS SPICE ALLOW FLOATING PINS                  YES
LVS SPICE ALLOW UNQUOTED STRINGS               NO
LVS SPICE CONDITIONAL LDD                      NO
LVS SPICE CULL PRIMITIVE SUBCIRCUITS           NO
LVS SPICE IMPLIED MOS AREA                     NO
// LVS SPICE MULTIPLIER NAME
LVS SPICE OVERRIDE GLOBALS                     NO
LVS SPICE REDEFINE PARAM                       NO
LVS SPICE REPLICATE DEVICES                    NO
LVS SPICE STRICT WL                            NO
// LVS SPICE OPTION
LVS STRICT SUBTYPES                            NO
LAYOUT CASE                                    NO
SOURCE CASE                                    NO
LVS COMPARE CASE                               NO
LVS DOWNCASE DEVICE                            NO
LVS REPORT MAXIMUM                             50
LVS PROPERTY RESOLUTION MAXIMUM                32
// LVS SIGNATURE MAXIMUM
// LVS FILTER UNUSED OPTION
// LVS REPORT OPTION
LVS REPORT UNITS                               YES
// LVS NON USER NAME PORT
// LVS NON USER NAME NET
// LVS NON USER NAME INSTANCE

// Reduction

LVS REDUCE SERIES MOS                          NO
LVS REDUCE PARALLEL MOS                        YES
LVS REDUCE SEMI SERIES MOS                     NO
LVS REDUCE SPLIT GATES                         YES
LVS REDUCE PARALLEL BIPOLAR                    YES
LVS REDUCE SERIES CAPACITORS                   YES
LVS REDUCE PARALLEL CAPACITORS                 YES
LVS REDUCE SERIES RESISTORS                    YES
LVS REDUCE PARALLEL RESISTORS                  YES
LVS REDUCE PARALLEL DIODES                     YES
LVS REDUCTION PRIORITY                         PARALLEL

// Filter

LVS FILTER sch_filter_direct_open  OPEN SOURCE DIRECT
LVS FILTER sch_filter_direct_short  SHORT SOURCE DIRECT
```

```
LVS FILTER  sch_filter_mask_open  OPEN SOURCE MASK
LVS FILTER  sch_filter_mask_short  SHORT SOURCE MASK
LVS FILTER  lay_filter_direct_open  OPEN LAYOUT DIRECT
LVS FILTER  lay_filter_direct_short  SHORT LAYOUT DIRECT
LVS FILTER  v  OPEN
LVS FILTER  i  OPEN
LVS FILTER  e  OPEN
LVS FILTER  f  OPEN
LVS FILTER  g  OPEN
```

****

INFORMATION AND WARNINGS

****

	Matched Layout	Matched Source	Unmatched Layout	Unmatched Source	Component Type
Ports:	11	11	0	0	
Nets:	14	14	0	0	
Instances:	6	6	0	0	MN(N)
	3	3	0	0	MP(P)
Total Inst:	9	9	0	0	

o Initial Correspondence Points:

Ports: vdb vdd vcb in7 out1 gnd senb va vb sen out2

****

SUMMARY

****

Total CPU Time: 0 sec
Total Elapsed Time: 0 sec