" Low Voltage Power Dissipation Analysis of 6H-SiC DIMOSFET with Gaussian Profile in the Drift Region "

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CERTIFICATE

This is to certify that the thesis entitled **" Low Voltage Power Dissipation Analysis of 6H-SiC DIMOSFET with Gaussian Profile in the Drift Region "** which is being submitted by **Ms. Shweta Rani (Regn.No. 8044125)** in partial fulfillment for the award of the degree of **Master of Engineering in Electronics & Communication Engineering of Thapar Institute of Engineering & Technology (Deemed University), Patiala** is an authentic record of the student's own work carried out under my supervision and guidance. The matter presented in the thesis has not been submitted elsewhere in part or full to any other University or Institute for the award of any other degree.

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ABSTRACT

It is increasingly recognized that semiconductor based electronics that can function at ambient temperatures higher than 150^{o}C without external cooling could greatly benefit a variety of important applications, especially in the automotive, aerospace, and energy production industries. The fact that wide bandgap semiconductors are capable of electronic functionality at much higher temperatures than silicon has partially fueled their development, particularly in the case of SiC.with a wider band gap of 6H-SiC of 3.0 electron volt a saturated drift velocity of 2x10 ^{7}cm/sec,a higher critical field for breakdown of 4x10^{6}V/cm with a dielectric constant of 9.7,and thermal conductivity of 4.9 W/cm°K it has almost all the qualities for becoming a better candidate than silicon or even 3C-SiC as a basic material. *However, practical operation of silicon power devices at ambient temperature above 200^{o}C appears problematic, as self-heating at higher power levels results in high internal junction temperatures and leakages. Thus, most electronic subsystems that simultaneously require high-temperature and high-power operation will necessarily be realized using wide bandgap devices, once the technology for realizing these devices become sufficiently developed that they become widely available.*

The present work aims at analyzing power dissipation levels of the 6H-SiC DIMOSFET in the low voltage or linear region the drain characterstics.results of power dissipation using Gaussian profile with effective doping levels of 9.2x10^{16} or higher in the drift region show lower power dissipation levels than those obtained using uniformly doped drift regions with identical doping levels.it is seen that the Gaussian profiles yield lower power dissipation and somewhat higherbreakdown voltages than uniformly doped drift regions

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CHAPTER – I
INTRODUCTION

Silicon carbide (SiC) is currently under intensive investigation as an enabling material for a variety of new semiconductor devices in areas where silicon devices cannot effectively compete. These include high-power high-voltage switching applications, high temperature electronics, and high power microwave applications in the 1 - 10 GHz regime. SiC is attractive for these applications because of its extreme thermal stability, wide bandgap energy, and high breakdown field. The thermal stability promises long term reliable operation at high temperatures, but it also presents problems in certain fabrication steps, e.g. selective doping, where impurities must be introduced by ion implantation due to the exceedingly low diffusion coefficients of common dopant impurities at reasonable processing temperatures. Because of the wide bandgap energy (3.0 eV and 3.25 eV for the 6H and 4H polytypes respectively), leakage currents in SiC are many orders of magnitude lower than in silicon, and the intrinsic temperature is well over 800°C. These electronic properties make SiC attractive for high temperature electronics applications. In addition, the breakdown field in SiC is around 8x higher than in silicon. This is critical for power switching devices, since the specific on-resistance scales inversely as the cube of the breakdown field. Thus, SiC power devices are expected to have specific on-resistances 100 - 200x lower than comparable silicon devices [1]. Finally, SiC is the only compound semiconductor which can be thermally oxidized to form a high quality native oxide (SiO_2). This makes it possible to fabricate MOSFETs, insulated gate bipolar transistors (IGBTs), and MOS-controlled thyristors (MCTs) in SiC.

Although it offers substantial advantages over silicon, SiC is still immature as a semiconductor material. Single crystal wafers of SiC have only been commercially available since around 1990 [5], and a number of critical material and processing issues are still under active investigation.The main limitations of the technology are in the area of crystal growth, and will be addressed in more detail below. In addition, certain critical fabrication processes are still under development. The most important of these fabrication

issues are (i) activation of ion implanted impurities, (ii) formation of thermally stable low resistance ohmic contacts, and (iii) thermal oxidation (or deposition) of high quality dielectric films suitable for MOS devices. In the following sections we shall review the current status of the technology in these four critical areas: crystal growth, selective doping, ohmic contact formation, and thermal oxidation.

1.1 Crystal Growth

Before the mid-1950's, SiC was available only through the industrial Acheson process for making abrasive materials [6]. In 1955, a laboratory sublimation process for growing a-SiC crystals was developed by J. A. Lely at Philips Research Labs in Einhoven [7]. In the Lely process, the nucleation of individual crystals is uncontrolled and the resulting crystals are randomly-sized hexagonal-shaped a-SiC platelets [8]. In 1978, Tairov and Tsvetkov pioneered the growth of SiC single crystals by the physical vapor transport process. In 1983, Ziegler et al. [96] introduced a modified sublimation process for growing SiC single crystals, and in 1987, a research group under R. F. Davis at North Carolina State University (NCSU) announced the successful implementation of a seeded-growth sublimation process [10], a modification to the original Lely sublimation process. In the modified sublimation process, only one large crystal is grown, and this crystal consists of a single polytype. In this process, which is the basis of current commercial growth systems, a charge of polycrystalline SiC is heated in a graphite crucible containing argon at 200 Pa. A temperature gradient is established, with the polycrystalline SiC at about 2400 C and a seed crystal at about 2200 C. At these temperatures, SiC sublimes from the polycrystalline source and condenses on the cooler seed crystal.

In 1987, students from the NCSU group founded a small company, Cree Research, to produce SiC wafers commercially. The introduction of 25 mm single crystal wafers of 6H-SiC by Cree in 1990 catalyzed the current resurgence in SiC research and

initiated an unprecedented level of device development in this material. At present, 35 mm diameter wafers of both 4H and 6H SiC are commercially available from Cree

Research (Durham, NC, USA) and from Advanced Technology Materials, Inc. (Danbury, CT, USA). 50 mm diameter wafers are used in the production of blue LEDs at Cree, and 75 mm diameter wafers have been prototyped by both Cree and Westinghouse (now Northrup Grumman).

Current research in crystal growth centers around increasing the growth rate, increasing the wafer diameter, and reducing material defects. Current SiC wafers have etch pit densities of the order of 10^4 cm^{-2}. These defects fall into three types, which have been classified as EP-1, EP-2, and EP-3 by Nakata, et al. [11]. The EP-1 defects are known as "micropipes", and are the open cores of giant screw dislocations with large Burgers vectors. Micropipes are holes, 0.5 - 10 microns in diameter, which run completely through the wafer and subsequently grown epilayers and are fatal to most kinds of devices. Micropipe densities have been steadily declining in recent years. Current Cree production wafers have micropipe densities in the 50-100 cm^{-2} range, and wafers with as few as 3.5 micropipes cm^{-2} have been reported [12].

Epitaxial layer growth is by chemical vapor deposition (CVD) on slightly off-axis substrates (3.5 degrees for 6H and 8 degrees for 4H). The use of off-axis substrates enables step-controlled epitaxy [13 in which steps on the growth surface expose several alternating silicon and carbon planes, thereby transferring stacking information which preserves the polytype in the epitaxially grown film. Typical growth rates are 1 - 5 microns/hour at a temperature of 1200 - 1500 C in SiH_4, C_3H_8, and H_2 [14].In-situ doping is accomplished by the introduction of nitrogen (for n-type) and trimethylaluminum or triethylaluminum (for p-type). Recently, the development of site-competition epitaxy has extended the doping range achievable by CVD, with dopings as low as $1x10^{14}$ cm^{-3} and

as high as >1x10^{19} cm^{-3} having been reported [15]. Very recently, E. Janzen, et al. [16] of Linkoping University reported a modified CVD technique capable of growing films up to 100 microns thick with a background doping level of 1x10^{14} cm^{-3}. Carrier lifetimes in these lightly doped layers are on the order of 1 microsecond. These results are very exciting because they would theoretically enable the fabrication of power devices having blocking voltages in excess of 10 kV.

1.2 Selective Doping

Selective doping of SiC is accomplished by ion implantation, since the diffusion coefficients of aluminum and nitrogen are so low that thermal diffusion is impractical. The implantation and activation of nitrogen to produce n-type regions is well understood, and activated concentrations above 1x10^{19} cm^{-3} can be obtained routinely. P-type selective doping, however, is an area of current research. The two common p-type dopants, aluminum and boron, produce relatively deep acceptor levels (211 meV and 300 meV respectively), but aluminum is generally used because of its smaller ionization energy. To minimize amorphization during implantation, it is common to implant at elevated temperatures, typically around 650 C for nitrogen and up to 1100 C for aluminum. Boron can be successfully implanted at room temperature. Kimoto, et al. [17, 18] report amorphization thresholds of 4x10^{15} cm^{-2} for nitrogen, 1x10^{15} cm^{-3} for aluminum, and 5x10^{15} cm^{-3} for boron.

Implant activation is accomplished by a high temperature anneal in argon. Ghezzo, et al. [19] report a series of isochronal (30 min.) anneals of nitrogen in 6H-SiC for various implant temperatures. They obtain a sheet resistance of 906 Ohms/square with a 1300 C anneal following implantation at 600 - 700 C. Pan, et al. [20] investigated the effect of anneal time on nitrogen implants in 6H-SiC at three temperatures: 1200, 1050, and 900 C. They found an optimum anneal time at each temperature, with the optimum times being < 5 min., 40 min., and 40 hr. at 1200, 1050, and 900 C, respectively.

Minimum sheet resistances obtained at the three temperatures were 700, 810, and 1005 Ohms/square, respectively.

Kimoto, et al. [18] report sheet resistivities as low as 22 kOhms/square for aluminum implanted into 6H-SiC at room temperature. They investigated implant doses ranging from $1x10^{14}$ to $1x10^{16}$ and anneal temperatures from 1200 - 1500 C, with all anneals conducted for 30 min. in argon. The minimum sheet resistivity occurred at a dose of $2x10^{15}$ cm^{-3} and an anneal temperature of 1500 C. Redistribution of aluminum is negligible at 1500 C. In the anneal, they utilized an RF induction heated furnace, which

allows very fast heating (40 C/sec) and may help to minimize defect formation during annealing. Rao, et al. [21] investigated the implantation of aluminum, along with the co-implantation of Al/C and Al/Si, into 6H-SiC at an in-situ temperature of 850 C. The implants were annealed at temperatures of 1500, 1600, and 1650 C for 45 min. in a ceramic furnace with a heating rate of 10 C/min. and a cooling rate of 3 C/min. The minimum sheet resistivities were 4.6 and 1.5 kOhms/square for aluminum implanted at a dose of $2.66x10^{15}$ cm^{-2} and annealed at 1500 and 1600 C, respectively. The co-implantations did not result in improvement in aluminum activation. In order to preserve surface morphology at these anneal temperatures, the samples were encapsulated in a SiC crucible during annealing. Even with this encapsulation, surface morphology deteriorated at 1650 C.

1.3 Ohmic Contact Formation

Ohmic contacts are of great importance to power devices, since the high current densities give rise to intolerable voltage drops across even small resistances. Ohmic contacts to n-type material are typically formed by annealed nickel. The contacts are annealed at high temperatures, typically between 850 - 1050 C, in argon or vacuum.

Specific contact resistivities < $5x10^{-6}$ Ohm-cm^2 can be obtained to heavily doped n-type layers [22]. Contacts to p-type material have been more difficult. The p-type contacts are typically formed by annealed aluminum, or by a bilayer of aluminum covered with titanium. Anneal temperatures are similar to those used for nickel contacts, but the contact resistivities are in the 10^{-3} to 10^{-5} Ohm-cm^2 range, depending on doping density [23]. Very recently, Ostling and Lundberg [24] reported contact resistivities to p-type 6H-SiC in the mid-10^{-6} Ohm-cm^2 range using sequential electron beam evaporation of cobalt and silicon, followed by a two step vacuum annealing process at 500 C and 900C.

The thermal integrity of the metallization system is of importance for high temperature applications. Nickel ohmic contacts used for n-type material have been shown to be stable to very high temperatures (negligible change in resistance after 329 hours at 650 C or after short thermal cycles to 1300 C) [23], but aluminum p-type contacts will not be capable of high temperature operation. The use of metal silicides, as recently reported for p-type ohmic contacts [24], will enable operation to much higher temperatures.

1.4 Thermal Oxidation and MOS Properties

SiC is the only compound semiconductor which can be thermally oxidized to form a device-quality native oxide, SiO_2. This capability removes one of the basic limitations of all other compound semiconductors and places SiC in a unique position to compete with silicon. To take full advantage of this unprecedented opportunity, every effort must be made to advance thermal oxidation technology so that SiC MOS interfaces have electrical characteristics comparable to those obtained on silicon.

SiC is oxidized using the same equipment and techniques used for silicon, but the oxidation rates are slower. In the oxidation process, the oxidizing species diffuses through the growing film and reacts with SiC at the oxide/semiconductor interface. The reaction products are SiO_2 and CO, with the CO molecules diffusing out through the growing oxide. The reaction kinetics are similar to silicon, with the early portion of the oxidation process being reaction rate limited and the later stages diffusion limited. However, oxidation rates depend strongly on the crystalline surface being oxidized, with the (0001-) carbon face oxidizing 5-10x faster than the (0001) silicon face. The oxidation rate of (11- 00) and (112- 0) "a-axis" surfaces is intermediate between that on the silicon and carbon faces. Oxidation rate is also a weak function of substrate doping density, increasing for more heavily doped material.

Early papers on the electrical properties of the MOS interface on SiC reported nearly ideal interfaces, comparable to those obtained on silicon. These early reports proved inaccurate, however, because the authors failed to take into account the effect of the wide bandgap on conventional MOS analysis techniques. At room temperature, interface states more than about 0.5 eV away from the band edges cannot respond fast enough to follow changes in DC bias during capacitance-voltage (CV) sweeps [25]. As a result, these deep states do not change their charge state, and exert no influence on the CV characteristic, thereby going undetected. Careful measurements conducted at elevated

temperatures (250 - 350 C) revealed interface state densities in the low 10^{11} eV^{-1} cm^{-2} range on n-type SiC [26, 27] and in the mid-to-upper 10^{11} eV^{-1} cm^{-2} range on p-type SiC [25, 26]. MOS capacitors formed on n-type material exhibit a flat band voltage near zero, while similar capacitors on p-type material have large negative flat band voltages (typically -7 to -15 V, depending upon oxide thickness). These observations lead many investigators to conclude that the MOS interface on p-type SiC is inferior to that on n-type SiC. Speculation centered on the role of the aluminum dopant in p-type material,

since SIMS studies indicated that aluminum is incorporated in the growing SiO_2 film at about half the concentration present in the semiconductor.

In the last few years, however, the picture has improved considerably. Work at our laboratory and other locations, including Laboratoire de Physique des Composants a Semiconducteurs (LPCS) and Cree Research, has lead to a reduction in interface state density on p-type SiC to the low 10^{11} eV^{-1} cm^{-2} range [25], comparable to that obtained on n-type SiC. Several studies [25, 28, 29] have shown that the aluminum dopant is not responsible for either interface states or fixed charges on p-type material. The flat band voltage of p-type SiC MOS capacitors remains negative, while on n-type SiC it is near zero. However, much of this difference in flat band voltage is due to the difference in position of the Fermi energy on n-type and p-type MOS capacitors (near the conduction band on n-type and near the valence band on p-type), and does not necessarily indicate a larger fixed oxide charge on p-type SiC [30].

Most of the MOS studies to date have been confined to the (0001) silicon face of 6H-SiC. Recently, it has been shown that MOS interfaces on 4H SiC have interface state and fixed oxide charge densities comparable to those on 6H [31]. However, MOS interfaces formed on the (11- 00) and (112- 0) "a-axis" surfaces of 6H-SiC are definitely inferior to those on the silicon face [27], with interface state densities approximately 6 - 10x higher. The "a-axis" surfaces lie perpendicular to the basal plane of the hexagonal lattice, and therefore contain an equal number of silicon and carbon atoms per unit area. Evidence is mounting that the presence of carbon on the plane being oxidized leads to serious degradation in the resulting interface quality, but a clear picture of the

microscopic details has yet to emerge. This is a critical issue, because these surfaces are important for several types of power switching devices, including trench MOSFETs, trench IGBTs, and trench MCTs.

One final area which is attracting attention is that of deposited insulators. One reason is the desire for an insulator having a dielectric constant comparable to or higher than that of the substrate. This is important for power devices because the electric field in SiO_2 is approximately 2.5x higher than the peak field in SiC, due to the dielectric constant ratio. Thus, in many cases the maximum blocking voltage of SiC power devices is limited by the SiO_2 and not by the semiconductor. An insulator having a higher dielectric constant would have a correspondingly lower electric field at a given operating voltage. AlN and TiO_2 are among the insulators under investigation, but this work is still at a very preliminary stage.

1.5 present work

It is well known that electric field plays a significant role in altering the mobility of carriers in a Semiconductor. It was therefore felt that there is a mud for analysis of the operation of SiC DIMOSFET in the voltage regime i.e. for $V_{DS}<V_{DSsat}$ wherin mobility variation is affected by the longitudinal voltage in the channel region i.e. Vch,which is only about 15% of the magnitude of V_{DS}, the drain to source voltage. The present work aims analyzing the variation in the drain current (I_{DS}) with V_{DS} under field dependent mobility variations and the associated power dissipation (P_D) moreover, a mathematical model has also been presented to evaluate the effective doping level(N_{eff}) for the drift region doped with impurities having a Gaussian profile .The magnitude of N_{eff} has also been void to evaluate the drain current (I_{DS}) and power dissipation(P_D). The magnitude of P_D obtained using Gaussian profile has been shown to be less than those obtained by uniformly doped drift region for similar doping levels,the results are given in chapter iv.

CHAPTER-II
SILICON CARBIDE POLYTYPES

2.1 Introduction

Silicon is the material dominating the electronics industry today. Silicon Carbide (SiC), however, has superior properties for power devices as compared to silicon. In recent years, activity in silicon carbide (SiC) device development has increased considerably due to the need for electronic devices capable of operation at high power levels and high temperature. The main strength of silicon carbide is that it can resist high field strengths, it offers better heat-conducting capacity than copper at room temperature and it has a large energy band gap, which means that electrical components continue functioning even when the mercury starts climbing. With very high thermal conductivity (~5.0 W/cm), high saturated electron drift velocity (~2.7 x 10^7 Cm/s) and high breakdown electric field strength (~3 MV / Cm), SiC is a material of choice for high temperature, high voltage, high frequency and high power applications[1]. Table 2.1 lists some electrical properties of the most common SiC polytypes in comparison to that of Si and GaAs [2].

The most important SiC property of all is the large bandgap, which is nearly three times larger than that of silicon. The large Si-C bonding energy makes SiC resistant to chemical attack and radiation. Silicon carbide belongs to a class of semiconductors commonly known as wide band gap semiconductors, where conventional semiconductors like Si and GaAs cannot adequately perform under extreme conditions. The wider band gap of SiC also enables one to design smaller, higher density devices that will withstand high voltages. Also, the thermal conductivity of SiC (4.9 W/Cm-K) is much larger than that of Si and GaAs and is a major advantage for SiC – based devices.The high thermal conductivity of SiC decreases the need for special packaging and system cooling for successful device operation[2].

Table 2.1. Comparison of properties of SiC with Si and GaAs at room temperature [2]

Property	Units	Silicon	GaAs	6H-SiC	4H-SiC
Bandgap	eV	1.11	1.43	2.9	3.2
Dielectric const	Er	11.8	12.8	9.7	9.7
Breakdown Field ($Nd=1x10^{17}cm^{-3}$)	V/cm	$6x10^5$	$6.5X10^5$	$35X10^5$	35X105
Saturated Velocity	cm/sec	$1x10^7$	$1x10^7$	$2x10^7$	2x107
Electron Mobility	cm^2/V-sec	1350	6000	380 $\perp$ to c-axis 380	800 $\perp$ to c axis
Hole Mobility	cm^2/V-sec	450	330	95	120
Thermal Conductivity	W/cm-º k	1.5	0.46	4.9	4.9

Silicon Carbide occurs in many different crystal structures (called polytypes, which is a condition known as polytypism) with each crystal structure having its own unique electrical and optical properties. The difference between the polytypes is the staking order between the double layers of carbon and silicon atoms. In fig 2.1, the stacking sequence is shown for the three most common polytypes 3C, 4H and 6H-SiC. Cubic and hexagonal Crystal Structures of Silicon Carbide are shown in In figure 2.2. If we designate a Si-C atom pair in an A- plane in a close packed lattice as A, and in the B-plane as B, and in the C-plane as C, then we can generate a series of lattice unit

cells by variation of SiC plane stacking sequence along the principal crystal axis (Fig 2.1).

The ABCABC... stacking, will generate the 3C-SiC zinc-blende lattice, and ABAB... stacking, will generate the 2H-SiC wurtzite lattice. Other stacking sequences, such as ABACABAC.. will generate 4H-SiC; and ABCACB... will generate 6H-SiC. The number of atoms per unit cell varies from polytype to polytype, significantly affecting the number of electronic energy bands and vibrational branches possible for a given polytype. This diversity in electronic and vibrational band structures profoundly affect the physical properties of the different polytypes. Some of these differences are listed in Table 2.1.

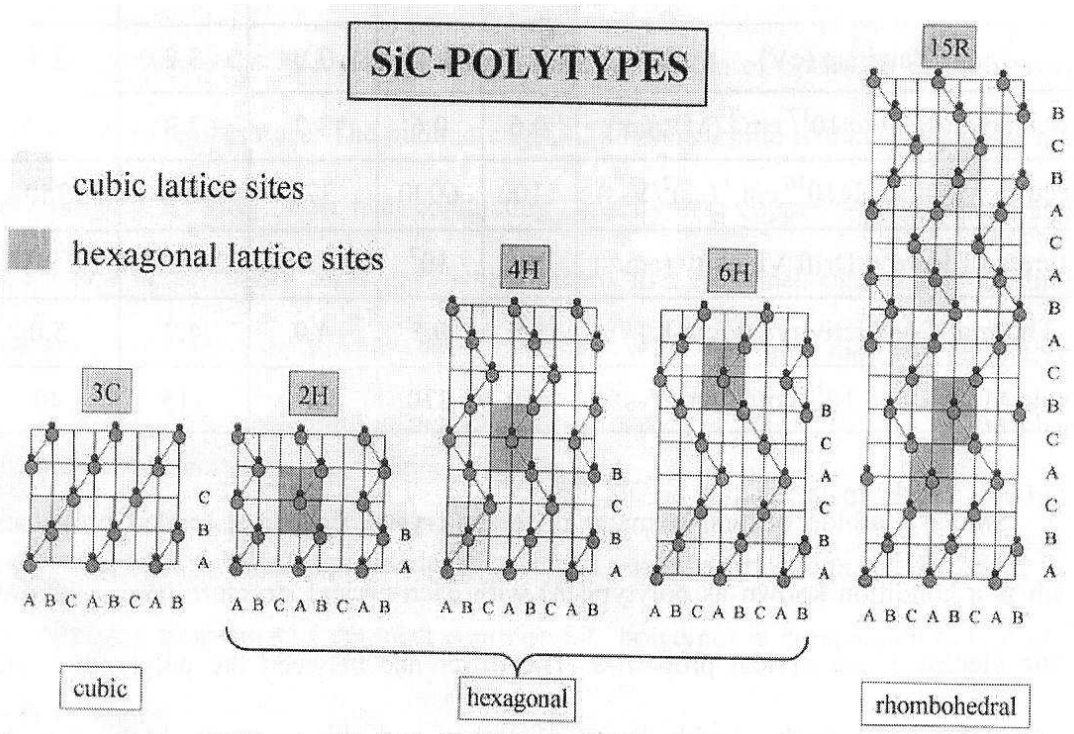

Fig 2.1 Stacking sequence of the most common polytypes of SiC [2]

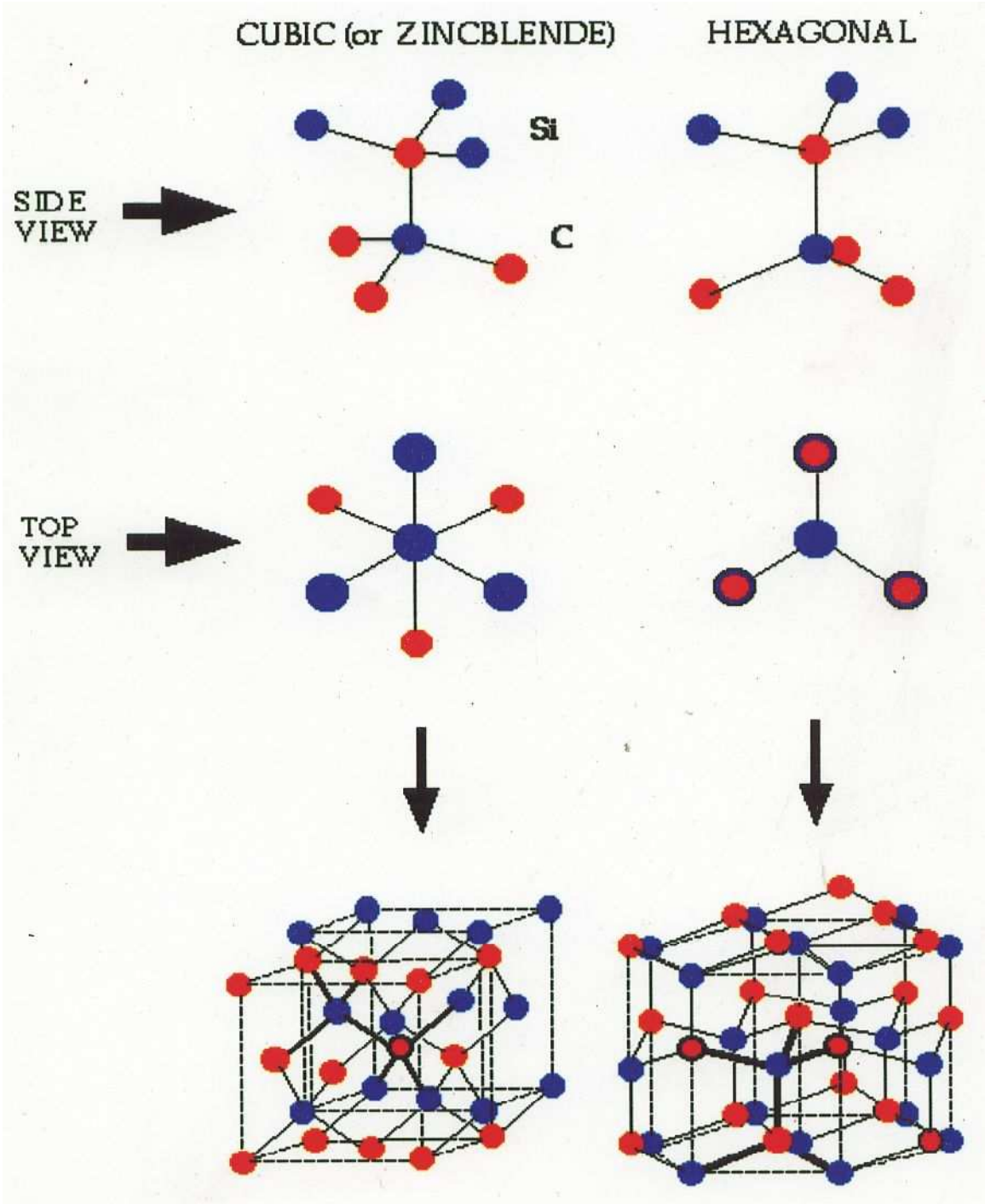

FIGURE: 2.2 Crystal Structures of Silicon Carbide

Considering the 6H-SiC polytype, the hexagonal site gives rise to the lowest donor level with an activation energy of approximately 85 meV ($\Delta E_h = E_c$-85 meV). The two cubic sites, k_1 and k_2, yield deeper donor levels with activation energies of 138 meV ($\Delta E_{k1} = E_c$-138 meV) and 142 meV ($\Delta E_{k2} = E_c$-142 meV), respectively. In the 4H-SiC polytype there are only two inequivalent sites, one hexagonal and one cubic [1]. In 3C-SiC there is of course only one cubic site and in 2H there is only one hexagonal site. The 6H-SiC polytype can thus be characterized as having donors (or acceptors) which are 33% hexagonal, whereas the 4H- and 2H-SiC polytypes are 50% and 100% hexagonal, respectively [1].

> Of the numerous polytypic forms of silicon carbide, 4H- and 6H-SiC electronic devices presently exhibit the most promise due to the availability and quality of reproducible single - crystal wafers of these polytypes. The availability of 6H-SiC and 4H-SiC polytypes [see Fig 2.1] in bulk wafer form has helped SiC to emerge as one of the relatively mature wide-band semiconductor technologies. SiC is a material with immense potential for use in heterostructure electronic devices, which take advantage of differing band gaps, carrier mobilities, etc. However, there are many crucial crystal growth and device fabrication issues that have to be addressed before SiC-based devices and circuits are ready for scale up and reliable incorporation into electronic systems. The most important issue is controlled and repeatable doping in SiC device structures.

2.2 Doping in Silicon carbide

The material advantages of silicon carbide are being exploited in the development of high power and high temperature semiconductor devices. However, in order to achieve the theoretically calculated advantages, advancements are needed in the growth techniques and dopant incorporation [3]. For a pure semiconductor the concentration of free holes and electrons is a function of thermal energy which determines the percentage of broken covalent bonds in the material. For an intrinsic semiconductor, the free electron concentration (n) and the free hole concentration (p) are equal (i.e., $np = n^2$ where n is the intrinsic carrier concentration). The electron and

hole concentration may be manipulated by adding a certain amount of impurity atoms to the semiconductor crystal in a process called doping. By introducing impurities with a different number of valence electrons, the number of available charge carriers in the semiconductor can be varied. An important consequence of doping is the creation of intermediate energy levels in the forbidden region because of the impurity atoms present in the host lattice.

Doping control is the most important technology for any semiconductor system. Epitaxy growers can control carrier densities in semiconductors by substituting foreign atoms (i.e., dopants) for host (i.e., lattice) atoms during growth. The difference in valencies between the dopant and host atoms provides excess mobile carriers. If an impurity atom has an extra valence electron than the host atom, it is called donor doped or an n-type semiconductor because of the excess free electrons. If the impurity atom contains less valence electrons than the host lattice, an electron vacancy or hole is created in the crystal lattice and is called acceptor doped or a p-type semiconductor.

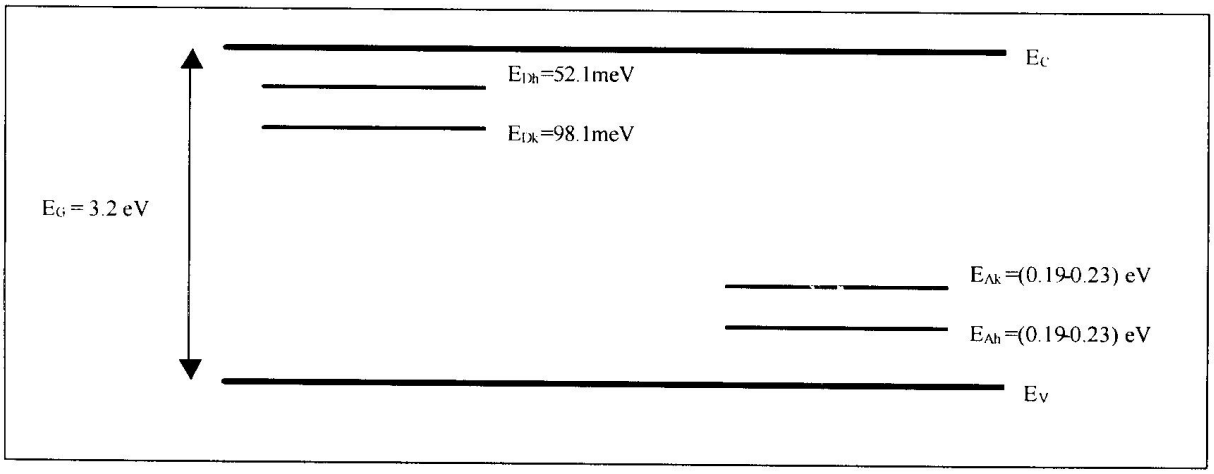

Fig 2.3 Band structure of n-type (left) and p-type (right) 4H-SiC showing the split energy levels due to the varying crystal symmetry[3].

In the band structure picture (see Fig 2.3), impurity states are created much closer to the conduction band in the case of n-type (donor) doping and much closer to

the valence band in the case of p-type (acceptor) doping. Donors donate electrons to the conduction band whereas acceptors accept electrons from the valence band, thus creating holes in the valence band. In either case, it is easy to liberate electrons (or holes) for conduction at low thermal energy, provided the activation energy of the dopant levels is on the order of 3 kT [37]. The holes are positively charged with charge +q since a hole is really the absence of an electron of the charge -q. Holes can move through the crystal, since a nearby electron can jump into a hole, filling it up, but leaving a hole nearby. Such materials are called p-type semiconductors, because it is 'he positive charge (hole) that can be viewed as a quasi - particle which can move freely in the material.

Doping in Silicon Carbide may be performed during epitaxial layer growth or after crystal growth by ion implantation. Ion implantation is more selective in nature but of lower quality than doped epilayers due to crystal damage created during ion bombardment. Typically, the first step in making silicon carbide semiconductor devices is to grow epitaxial layers using a process called chemical vapor deposition (CVD), which allows single - crystal layers (called epitaxial layers or "epilayers") of varying electrical conductivity to be grown. The silicon carbide epilayers are produced in the CVD process by thermally decomposing silicon and carbon source gases (called precursors) onto boule - derived SiC substrates. The electrical character is changed by adding dopants, impurity elements that affect the epilayer electrical properties as just described, during the CVD SiC epilayer growth by flowing either nitrogen (for n-type) or trimethylaluminum and/or boron (for p-type) material.

Control over dopant incorporation in CVD SiC epilayers has been very limited [3]. Dopant incorporation during the growth of SiC epilayers must be understood and reliably controlled. Site competition epitaxy is a recent development for the control over dopant incorporation for both aluminum and boron (both p-type) and nitrogen (n-type) doped epilayers [32]. It has greatly helped in increasing the doping range and

doping reproducibility of CVD SiC epilayers. This has also led to improved device performance, which includes high voltage diodes and high temperature JFETS [3].

Site competition epitaxy has been successfully used for the control of B, Al and N doping, partly because A1 substitutes for Si - sites and N substitutes for C - sites in the SiC lattice. In contrast, boron has been reported to substitute for both the carbon and silicon sites of the SiC lattice [32]. As previously mentioned, site - competition epitaxy is a dopant control technique based on appropriately adjusting the ratio of Si to C within the growth reactor to effectively control the amount of dopants incorporated substitutionally into the SiC crystal lattice. Nitrogen donor atoms are believed to occupy only the C - sites for densities below $I0^{20}$ cm^{-3} whereas aluminum acceptor atoms occupy only Si - sites in the SiC lattice [32]. In order to utilize the site - competition dopant control technique, it must first be determined whether a specific dopant occupies either the C - site or the Si - site. As stated earlier, boron has been reported to occupy both the C and Si sites [32] but experiments by Yankin et al indicate that boron preferentially occupies the Si - site of the SiC lattice. In summary, the nitrogen donor concentration in the grown epilayer is proportional to the Si/C ratio during epilayer growth, whereas the aluminum and boron acceptor concentration is inversely proportional to the Si/C ratio [3].

Although site competition epitaxy is an effective means of dopant control, it involves changing precursor gas flow conditions during epi growth to vary the dopant levels. This can lead to difficulties over control of unintentional impurities, making it difficult to control and achieve a desired epilayer thickness. The other method of doping Silicon Carbide is selective doping after epitaxial layer formation. Selective doping of SiC is accomplished by ion implantation, since diffusion coefficients of aluminum and nitrogen are so low that thermal diffusion in SiC is impractical [33].

Diffusion in SiC at such high temperatures (>1800^{0}C) produce significant surface damage and no dielectric masking layer is available. Therefore, ion implantation is the only selective area doping technique available for the fabrication of planar SiC integrated circuits [34].

Successful fabrication of implanted layers in SiC depends on the proper choice of post – implant anneal conditions. Implant activation can be accomplished by a high

temperature anneal. The anneal temperatures typically range from 1200°C - 1800°C. If the anneal temperature is too low, the implanted ions are only partially activated, and the crystalline defects created by the implant damages are not completely removed [35]. On the other hand, if the temperature is too high, the SiC surface restructures and becomes much rougher (called "step bunching"), which makes the wafer useless for device fabrication [35]. The available process window depends on a wide variety of factors, including SiC polytype, implant species, implant and anneal temperatures, and capping material or gas ambient used during the anneal process [35].

To preserve the surface morphology at these anneal temperatures, the samples may be encapsulated in a silicon carbide crucible during annealing [35]. Electrical activation of nitrogen implants of greater than 50%, has been achieved for doping concentrations up to around 10^{18} cm^3 [34]. For higher implanted dopant concentrations, the electrical activation decreases significantly. Activation of p-type dopants is reported to be even lower [34]. The high dose nitrogen implant that is typical for source and drain contacts results in amorphization of the SiC surface, yet requires anneal temperatures in excess of 1500° C. Such high temperature anneals preclude fabrication of structures such as polysilicon - gate self - aligned MOSFET's because the polysilicon - gate and the oxide cannot withstand such high temperature [34]. To minimize

amorphization during implantation, the implantation process is usually carried out at elevated temperatures (650° C for nitrogen and up to 1100° C for aluminum [33]).

Ion Engineering Research Institute Corporation in Japan has tried simultaneous short - wavelength pulsed laser annealing during ion implantation (SLII) as an alternative technique for hot implantation. They reported that implantation - induced damage in SiC can be reduced by short wavelength pulsed laser annealing. The short wavelength pulsed laser annealing process is a non - thermal equilibrium process and can be carried out at RT or lower temperatures.

Researchers at the Emerging Materials Research Laboratory, Mississippi State University, have developed and reported a successful process of using silicon

overpressure, provided by silane in a CVD reactor during the implant anneal, to prevent destruction of the silicon carbide surface [36].

Ion Implantation generates crystallographic defects (vacancies, interstitials, etc.) which can serve to form complexes with donors and acceptors in the lattice.

2.3: Hydrogen Passivation of Silicon Carbide

The specific physical and electronic properties of silicon carbide make it one of the promising semiconductors for use in electronic devices, especially those applications where operation at high power, extreme temperature, or high radiation levels is needed. Many of these applications require the growth of thick, high quality epitaxial layers with controlled doping concentrations and carrier lifetimes. This has led to significant progress in the technologies for both bulk and epitaxial growth in the past few years. During processes such as chemical vapor deposition (CVD), hydrogen in known to be trapped at defects or impurities and to alter the electrical properties [53]. This effect is known as "hydrogen passivation".

In addition to the observed hydrogen passivation of shallow impurities in SiC crystals, it is important to know whether, and how, hydrogen present in the epi-reactor can passivate doping impurities during the growth of the material [54]. One problem is that hydrogen passivation makes it difficult to know the true free carrier concentration in

the material. Also, variations in hydrogen incorporation affect the net doping density and make process control difficult.

The intrinsic material advantages of silicon carbide are currently being exploited in the development of high power and high frequency semiconductor devices for service in high temperature, corrosive and high radiation environment[32]. However, in order to obtain the theoretically calculated advantages of using SiC, advancements are needed both in the field of bulk growth and epilayer growth of SiC [32]. For example, improvements in the bulk growth of SiC are needed for the elimination of device limiting defects such as micropipes and closed-core screw

dislocations [32]. Other advancements are also needed in the growth process of epitaxial layers in silicon carbide. In particular, dopant incorporation both during the growth of SiC epilayers or by ion implantation must be understood and reliably controlled which will help to achieve desired device results [32]. In Silicon Carbide, hydrogen incorporation is known to occur during epitaxial growth by chemical vapor deposition since CVD growth uses C_3+SiH_4 and hydrogen as a typical carrier gas. It has also been observed that hydrogen incorporation occurs during plasma treatment, ion implantation, or treatment in hydrogen gas [54]. In most reports, hydrogen trapping at defects plays a significant role. The process temperatures necessary to induce detectable mobility of hydrogen is SiC crystals are in excess of 900 K [54]. Hydrogen forms complexes with known dopants in Sic (both donors and acceptors) and has been observed to make them electrically inactive [55]. The presence of hydrogen therefore reduces the effective carrier density within the material and masks the true dopant level. This process is usually referred to as "hydrogen passivation of silicon carbide".

Hydrogen passivation has been observed in both p-type and n-type SiC with the observation of the latter being less observable. But before presenting the model, one has to take into account various factors such as the atomic number of the dopant species, its activation energy in the SiC lattice, number of valence electrons, etc. All of these values have been tabulated in Table 2.2

Table 2.2: Atomic Number and Activation Energies of the most common dopants in SiC[3]

	N donor	Al acceptor	B acceptor
Atomic Number	7	13	5
Activation	$E_{Dh}=E_C - 52.1meV$	$E_A=E_V+(0.19\text{-}0.23)$ eV	$E_A=E_V+(0.285\text{-}0.39)$ eV

Energy in 4H-SiC	$E_{Dk}=E_C-91.8meV$		
Activation Energy in 6H – SiC	$E_{Dh}=E_C-81meV$ $E_{Dk1}=E_C-137.6meV$ $E_{Dk2}=E_C-142.4meV$	$E_A=E_V+(0.20\text{-}0.25)$ eV	$E_A=E_V+(0.27\text{-}0.40)$ eV

The most common acceptor impurities (A1 or B) can be introduced during growth or afterwards by ion implantation. A substitutional atom with a group – III valency normally acts as an acceptor in SiC since there is a deficit of one valence electron to complete the tetrahedral bonding. At sufficiently high temperatures, it ionizes and give rise to p-type conduction. On the other hand, an atom with a group – V valency normally acts as a donor in SiC since there is an excess of one valence electron. Since SiC is a compound semiconductor, an additional variable is which lattice site (Si or C) the dopant occupies. Boron and Aluminum are known to substitute for the silicon site in the structure and nitrogen is known to replace carbon.

The free carrier concentration has been observed to decrease after hydrogenation due to hydrogen – dopant complex formation. The free concentration has been observed to increase after de – hydrogenation (annealing the sample at high temperatures to break the bonding existing between complexes).

2.4 : Introduction to Ion Implantation

Impurity Doping is the controlled amounts of impurity dopants into semiconductors.the practical use of impurity doping has been mainly to change the electrical properties of the semiconductors.Diffusion and ion implantation are the two key mehods of impurity doping.

Until the early1970s,impurity doping was done mainly by diffusion at elevated temperatures.In this method the dopant atoma are placed on or near the surface of the waferby deposition from the gas phase of the dopant or by using doped-oxide sources.the doping concentration decreases monotonically from the surface,and the profile of the dopant distribution is determined by the temperaure and diffusion time.

Many Doping operations have been performed by ion implantation ,in this process the dopant ions are implanted into the semiconductor by means of an ion beam. The Doping concentration has a peak distribution inside the semiconductor and the profile

of the Dopant distribution is determined mainly by the ion mass and the implanted –ion energy.ion implantation is used for fabricating discrete devices and integrated circuits ,these processes complement each other,for example,diffusion is used to form a deep junction(e.g.,a twin well in CMOS) whereas ion implantation is used to form a shallow junction (e.g., a sorce/drain junction of a MOSFET).

Ion implantation has been established as the main method for selective doping of SiC. With ion implantation the electrical or chemical properties of the target can be modified. Typical ion doses vary from 10^{11} to 10^{16} ions/cm^2.

The depth profile of implanted ions can roughly be described by a Gaussian distribution with a maximum at R_p and a width ΔR_p . The projected range R_p increases approximately linearly with the energy. The straggle ΔR_p also increases with increasing energy. The implantation at elevated temperatures is known to be effective to reduce implantation induced damage and to improve the electrical activation of implanted ions.

Ion implantation in covalent semiconductors is accompanied by the formation of intrinsic point defects due to elastic collision processes between the ion and lattice atoms.

For high ion energies the energy loss is almost entirely to target electrons, whereas in the low-energy regime atomic collisions with vacancy cascade formation prevail. The density of point-defect formation in the region near the end of the ion range is thus much higher than in the rest of the ion track, which we refer to as the trace region

Recently, there has been an interest in the fabrication of microelectronic circuits that can operate as high-power/highspeed devices in both elevated-temperature and high radiation environments where Si integrated circuits (ICs) would fail. The wide band-gap semiconductor, SiC (*Eg* = 3.0 eV for the 6H polytype and 3.25 eV for 4H), is the leading contender for such applications.[66] Its high breakdown electric field (~8 times that of Si) and high thermal conductivity (~ 3.3 times higher than Si) are attractive for the fabrication of high-power circuits. Additional benefits of SiC are high electron saturation drift velocity (two times higher than Si) as well as the ability to create semi-insulating

layers by group V doping,[67] traits that are useful for making microwave frequency range devices. Monolithic *n*-type metal–oxide semiconductor (NMOS) digital ICs,[68] MOS analog ICs[69[complementary metal–oxide-semiconductor (CMOS) ICs[70] high performance microwave devices[71] insulated-gate bipolar transistors[72] and CCD image sensors[73] have all been made using SiC.

For making planar ICs, selective area doping is required. Thermal diffusion is precluded for this purpose in SiC due to the small diffusivity of impurities at temperatures (1800°C), where the surface integrity of the material can be maintained. As a result, ion implantation is the only possible selective area doping technique available for SiC. The group V and group III elements constitute the commonly used donor and acceptor dopants, respectively, in SiC. Nitrogen implantation yields *n*-type layers with good donor activation in SiC.[74–77] Nitrogen implanted *n*-type layers with room-temperature carrier concentrations as high as 10^{19} cm-3 have been achieved.[74-77] This behavior is due to the fact that N is a relatively shallow donor (E_D = 80 meV for 6H–SiC) [78] in SiC. Aluminum implantation, on the other hand, will produce *p*-type layers in SiC.[77,79,80] Due to the high acceptor binding energy (E_A=240 meV for 6H–SiC) [81] of Al, at room temperature it is not possible to obtain the same level of hole concentration as the electron concentration that was achieved for N-implanted material.

Since the ionization energy of P, in 6H–SiC, is comparable to that of N,[78] P implantation in SiC has the potential of producing *n*-type layers with high carrier concentrations even at room temperature. In addition, since it's atomic mass is not high enough to cause excessive lattice damage during implantation, phosphorus has become the most popular donor impurity in Si processing. The P atoms are believed to reside predominantly on Si lattice sites,[82] whereas N locates predominantly on C sites.[83] Hence, if it is possible to activate P implants satisfactorily, then the co implantation of P and N may be useful in obtaining high carrier concentrations by populating both Si and C sites with P and N, respectively. This is important since high carrier concentrations are needed to obtain low contact resistance and low neutral region resistance in SiC devices, an attribute especially critical for attaining optimum performance in high power and

microwave devices. Though B is a deep acceptor impurity with E_A=350 meV,[84] its low mass, and its availability in gaseous source form (BF3) make B implantation an attractive choice for obtaining deep *p*-type regions of low carrier concentration in SiC. The p – n junctions made by the B implantation exhibited lower leakage currents than those formed by the Al implantation.[85]. However, Al is preferred over B because it's acceptor level is shallower and, therefore,can yield higher hole concentrations, which is important for making low-resistance Ohmic contacts. Deep B implantation at the junction and an overlapping shallow Al implant at the surface looks attractive for obtaining planar p – n junctions in n-type SiC.

The range statistics [the two moments of the implant depth distribution, namely, projected range (Rp), range straggle (ΔRp) of the implanted ions were established at various energies by analyzing the secondary ion mass spectrometry (SIMS) atom concentration depth profiles of implants using mathematical formulas given below .

After implantation, the SIMS measurements were conducted on the as-implanted samples to obtain the implant depth profiles. These profiles were then analyzed, using formulas[86] given below to establish the experimental range statistics of the implanted ions at various energies.

Rp(average range) = $\int x\, f(x)dx$,

Rp (range straggle) = $\{ \int \{x-Rp\}^2 f(x)dx \}^{-1/2}$

Table –2.3: Energy /Dose Values When Phosphorous ion implant is used [87].

Ion Energy E	**Dose(cm^{-2}) S**
50 Kev	$3.4x10^{14}$
100Kev	$6.0x10^{14}$
100Kev	$6.0x10^{13}$
100Kev	$6.0x10^{12}$
250Kev	$1.2x10^{15}$
500Kev	$1.8x10^{15}$
750Kev	$2.2x10^{15}$
1.0Mev	$2.4x10^{15}$
2Mev	$2.8x10^{15}$
3Mev	$3.0x10^{15}$
4Mev	$3.2x10^{15}$

Implant depth profiles

These SIMS profiles were analyzed, using Eqs. (1)–(2) to determine the first two moments of the distribution for various ion energies. The first (*Rp*) and second (ΔRp) moments refer to the location of the peak of the distribution and the spread of the distribution around the peak, respectively.Phosphorous ion range statistics in 6H-SiC.

Table –2.4: Values of Projected Range and Longitudnal Straggle at various Ion Energy levels[88].

Ion Energy	Projected Range(µm) R_P	Logitudnal Straggle(µm) $б_P$
50 Kev	0.059	0.027
100Kev	0.097	0.039
250Kev	0.249	0.073
500Kev	0.47	0.109
750Kev	0.616	0.119
1.0Mev	0.764	0.131
2Mev	1.28	0.157
3Mev	1.67	0.163
4Mev	2	0.168

CHAPTER – III
SILICON CARBIDE DEVICES

Silicon carbide has several unique properties that can lead to enhanced performance in devices, as discussed below. These properties include higher breakdown field, wider band gap, lower thermal generation rate, and lower intrinsic carrier concentration.

1. Power MOSFETs

The breakdown electric field of SiC is approximately 8x higher than silicon. This makes it possible to design power switching devices having correspondingly higher blocking voltages than their silicon counterparts. More importantly, the specific on-resistance (i.e. resistance-area product) of a power device scales inversely as the *cube* of the breakdown field, so the on-resistance of SiC power MOSFETs are 100-200x lower than comparable devices in silicon.

2. Lateral Power MOSFETs

The maximum blocking voltage of vertical power devices in SiC is presently limited by the thickness of commercially available epilayers. The first *lateral* power MOSFETs developed in SiC devices exhibit blocking voltages of 2.6 kV, a new record.

3. Schottky Barrier Diodes

Schottky barrier diodes (SBD's) are attractive as power rectifiers because they do not store minority carriers in the on-state, and therefore can be switched off quickly with negligible reverse current. It is widely felt that SBD's will be the first SiC power devices to go into commercial production. SBD's are fabricated on 4H-SiC that exhibit blocking voltages of 1720 V, equal to the current world record.

4. IMPATT Diode Microwave Oscillators

IMPATT diodes are two-terminal semiconductor devices that generate RF power by introducing a 180° phase shift between current and voltage waveforms at microwave frequencies. The first IMPATT diodes are fabricated in 4H-SiC. These devices exhibit microwave oscillations at around 8 GHz when operated in an X-band waveguide cavity under pulsed bias.

5. CMOS Integrated Circuits

The first 6H-SiC CMOS digital integrated circuits are completed in September 1996. A second generation was completed in March 1997. These are the first SiC CMOS circuits fabricated with an implanted P-well process, and the first to operate on a single 5 V power supply.

6. Nonvolatile Memories

The thermal generation rate in semiconductors is proportional to the intrinsic carrier concentration n_i, and n_i decreases *exponentially* with band gap energy. Wide band gap semiconductors have dramatically lower thermal generation, with the thermal generation rate of 6H-SiC being about 16 order-of-magnitude lower than silicon. This makes it

possible to construct on-transistor memory cells in SiC which retain information for many years without power.

7. **Charge Coupled Devices**

CCDs are unique MOS devices in which charge packets are shifted laterally along the semiconductor surface by appropriate clocking applied to surface electrodes. CCDs are widely used as imagers in video cameras and digital still cameras. The first CCDs developed in SiC, where the wider bandgap makes it possible to image scenery in the UV portion of the spectrum without being overwhelmed by visible light.

8. **NMOS Integrated Circuits**

The low thermal generation rate in SiC makes it possible to operate integrated circuits at much higher temperatures than silicon. The first digital integrated circuits in SiC were developed in late 1993. These early circuits were implemented in enhancement mode NMOS.

Now the first four relevant devices are discussed in detail.

3.1 Silicon Carbide Power MOSFETs :

Power switching devices are reaching fundamental limits imposed by the low breakdown field of silicon, and substantial improvements can only be achieved by using a semiconductor with a higher breakdown field. Power switching devices in silicon carbide (SiC), a compound semiconductor with a breakdown field about 10x higher than silicon are developed.

SiC is unique among compound semiconductors in that its native oxide is SiO_2, the same oxide as silicon. This means that the workhorse power devices used in silicon, i.e. the power MOSFET, insulated gate bipolar transistor (IGBT), and various types of MOS-controlled thyristors (MCTs) can all be fabricated in SiC. Because of the higher breakdown field, SiC power devices can have specific on-resistances up to 400x lower than similar devices in silicon.

MOSFET work is centered on two types of devices: DMOS and UMOS. The DMOS, or "Double-implanted MOS", power transistor is shown in Fig. 3.1. This device is analogous to the silicon "DMOS", or "double-Diffused MOS", power transistor except that the P base and N+ source regions are produced by ion implantation instead of thermal diffusion (diffusion is not practical in SiC because of the very low diffusion coefficients in the material). In this device, a positive bias on the polysilicon gate creates a surface inversion layer at the interface between the SiO_2 and the P-type SiC. Electrons flow from the N+ source along the inversion layer to the N- drift region. Upon reaching the drift region, electrons flow vertically to the N+ drain at the bottom. The thick, lightly

doped N- drift region is needed to withstand a large drain voltage when the device is in the off state (gate at ground).

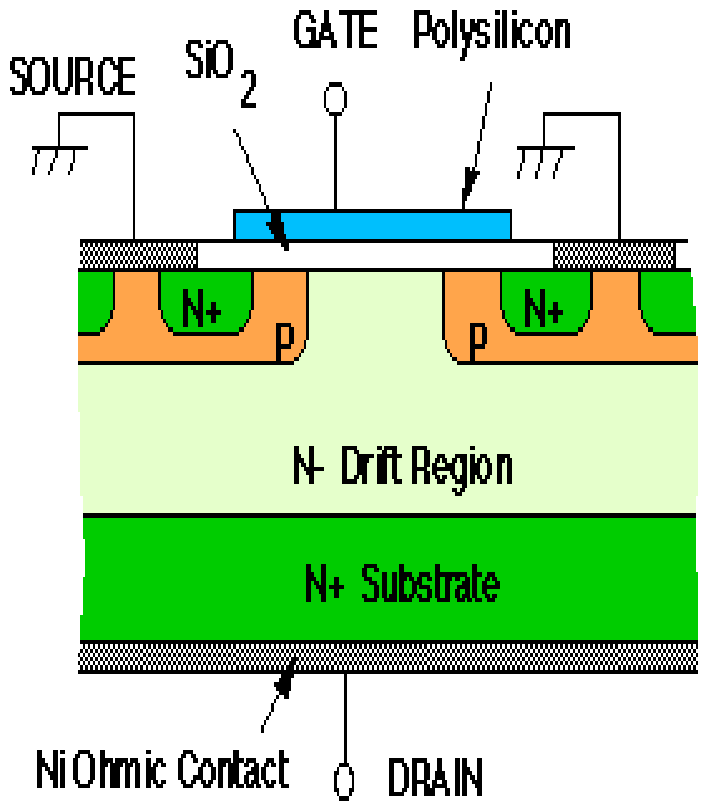

Figure 3.1. Cross section of a SiC ion-implanted "DMOS" power transistor [38,39].

The first SiC DMOS power transistors were developed in June 1996 [38,39]. These devices exhibited blocking voltages in excess of 760 V, approximately 3x higher than the best SiC MOSFETs up to that time. Specific on-resistance was 125 mOhm-cm^2 for the 760 V devices and 66 mOhm-cm^2 for 2 µm channel length devices on the 500 V wafer [40,41]. These devices exhibited a blocking voltage of 2.6 kV, which is still the highest blocking voltage for any SiC power switching device.

Most of the previous work in SiC power transistors has been devoted to the trench-gate or "UMOS" power transistor, shown schematically in Fig. 3.2. The electric fields in the blocking state (transistor OFF) are shown at the right. Looking at the blue (right-hand) plot, note that the electric field in the oxide at the bottom of the trench is 2.5x higher than the peak field in the semiconductor. Such a high electric field will lead to catastrophic breakdown of the oxide. The field at the corner of the trench is even higher due to two-dimensional effects. This oxide breakdown problem represents a major limitation to the UMOSFET structure in SiC.

Fig. 3.3 shows a novel UMOS structure with Integral Oxide Protection (IOP) that limits the electric field in the trench oxide while simultaneously reducing on-resistance. Fig.3.3, along with the electric fields in the blocking state. The new P-type region in the bottom of the trench reduces the electric field at the oxide/semiconductor interface to zero, thereby protecting the oxide from high electric fields in the blocking state. The new N-type epilayer beneath the P-base prevents pinch-off of the conducting channel in the on-state and facilitates lateral current spreading into the drift region. The device in Fig. 3.3 also includes a lightly-doped N-type epilayer grown on the sidewalls of the trench. This layer converts the device into an *accumulation-layer* MOSFET, or "ACCUFET", increasing the MOSFET mobility and further reducing on-resistance.

Figure 3.4 shows the static I-V characteristics of an IOP-UMOS ACCUFET in 4H-SiC. The blocking voltage is 1400 V, which is 87% of the theoretical value for the 10 μm drift region in our device. Breakdown is non-destructive, indicating that oxide failure does not occur. In fact, numerical simulations show that the peak electric field in the oxide is only 3 MV/cm at the blocking voltage of 1400 V. The specific on-resistance is 15.7 mOhm-cm^2, and the figure-of-merit V_B^2/R_{on} is 125 MW/cm^2, the highest value ever reported for a power MOSFET in any material system and 25x higher than the theoretical limit for silicon power MOSFETs.

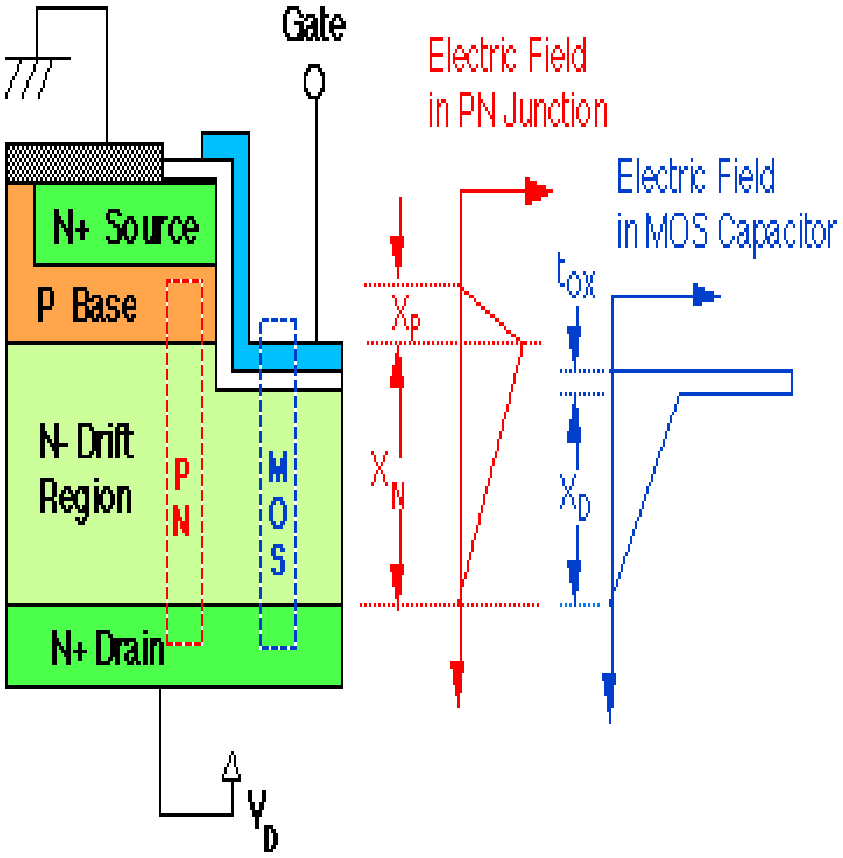

Figure 3.2. Cross section of a UMOS power transistor in silicon carbide. The electric field is illustrated on the right side for two regions within the device, the pn junction region and the MOS capacitor region. The field in the oxide at the base of the trench is 2.5x higher than the peak field in the semiconductor because of the discontinuity in dielectric constants at the interface [38,39].

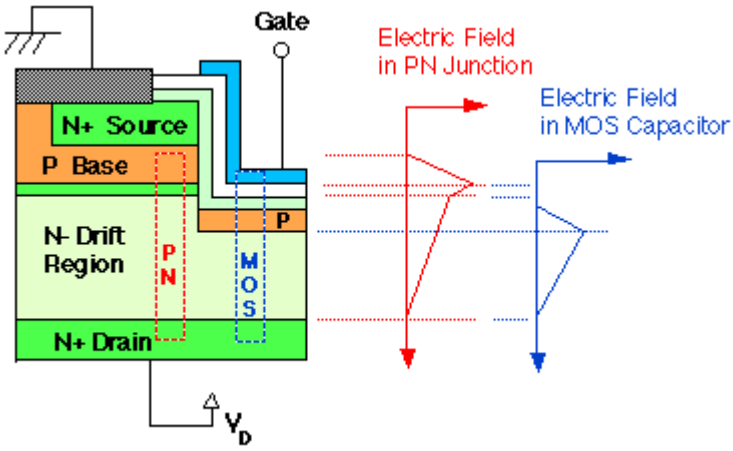

Figure 3.3. Cross section of the recently-introduced IOP-UMOS power transistor. The electric field is illustrated on the right side for two regions within the device. The P-type region under the trench reduces the field in the oxide at the base of the trench to zero [38,39].

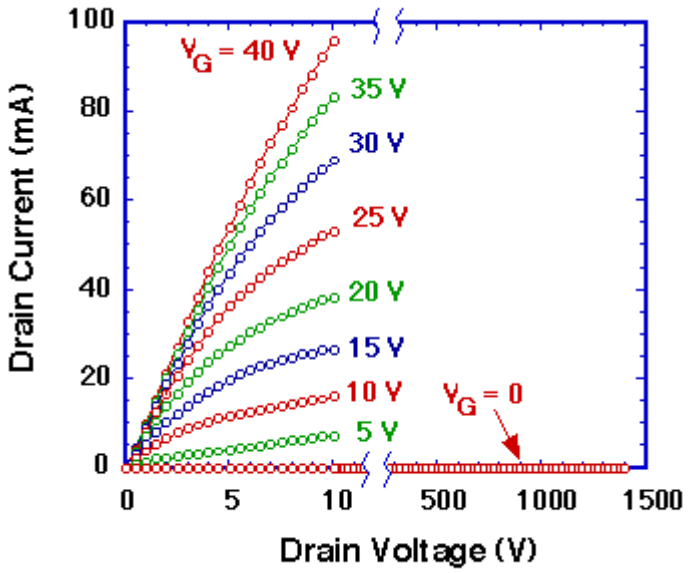

Figure 3.4. I-V characteristics of the IOP-UMOS ACCUFET in 4H-SiC at room temperature. The gate width is 3.168 mm, gate length is 1.2 μm, oxide thickness is 130 nm, and the active area is 1.728x10-4 cm2 [38,39].

3.2 Silicon Carbide Lateral Power MOSFETs

Power switching devices in SiC, both MOSFETs and thyristors, were fabricated as vertical structures, with the substrate serving as the anode terminal. In the off state, voltage is blocked by a reverse-biased pn junction. To achieve high blocking voltage, one side of this junction, the "drift region", is thick (typically around 10 microns) and lightly doped (5 - 10^{15} cm^{-3}). Figure 3.5 below shows how the blocking voltage depends on the doping and thickness of the drift region. Note that for a given thickness, there is a maximum possible blocking voltage, regardless of doping. Up until very recently, commercially available SiC epilayers were limited to about 10 microns in thickness, and the maximum possible blocking voltage for this thickness is about 1600 V.

One way to avoid this limitation is to *turn the device on it's side,* i.e. build a *lateral* device. The basic structure of our lateral DMOSFET [40,41] is shown in Fig. 3.6. In the blocking state, the depletion layer spreads mainly into the lightly doped drift region. Once the depletion region reaches the insulating substrate, it continues spreading toward the drain, which is now located on the top surface. In this device, the maximum blocking voltage is not limited by the thickness of the epilayer.

Figure 3.7 shows the room temperature current-voltage characteristics of a lateral DMOSFET having a 10 micron gate length and a 35 micron gate-to-drain spacing [40,41]. As seen, the blocking voltage of this device is about 2.6 kV. This voltage is not

limited by electrical breakdown in the device, but rather by arcing in the Flourinert solution in which the device is immersed during testing.

It is important to realize that by implementing the device laterally rather than vertically, do not necessarily increase the surface area required for the device. If the device design incorporates the REduced-SURface-Field (RESURF) concept [43,44], the specific on-resistance (resistance-area product) can actually be *lower* than that of a comparable vertical device. The present device does not incorporate RESURF features.

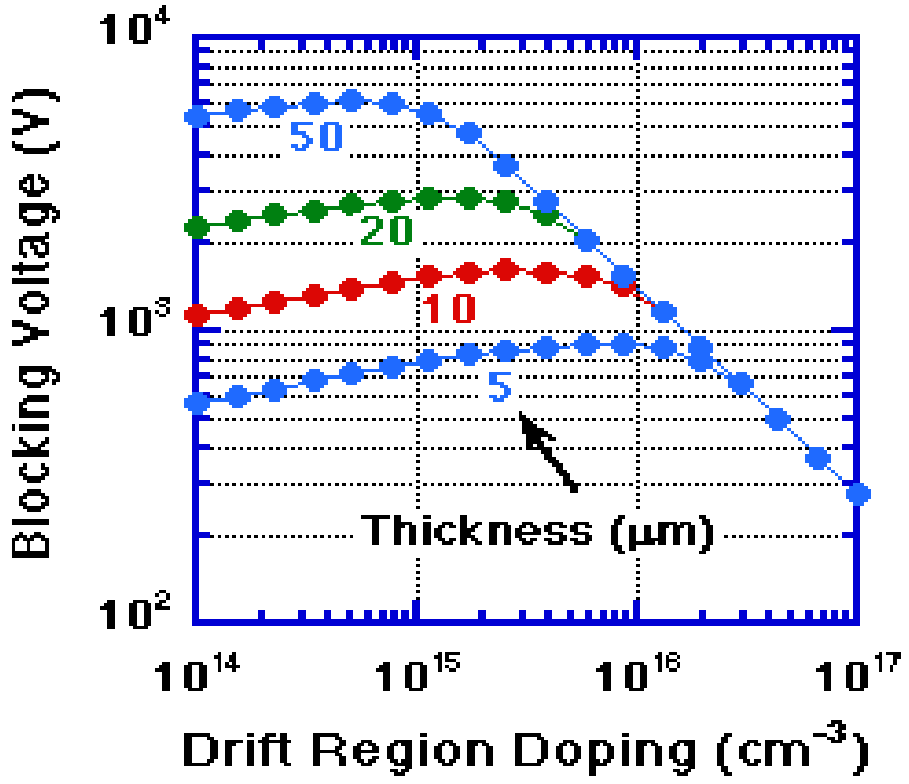

Figure 3.5. Blocking voltage as a function of drift region doping, with drift region thickness as a parameter. For a 10 micron drift region, the maximum possible blocking voltage is about 1600 V [41].

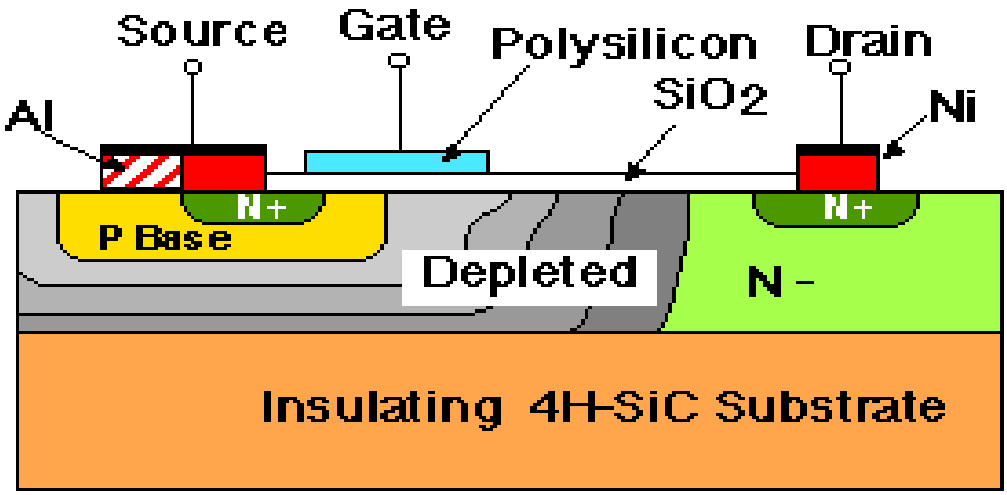

Figure 3.6. Cross section of lateral DMOSFET in the blocking state. The depletion region extends from the p-base toward the drain, and the blocking voltage is not limited by epilayer thickness [40,41].

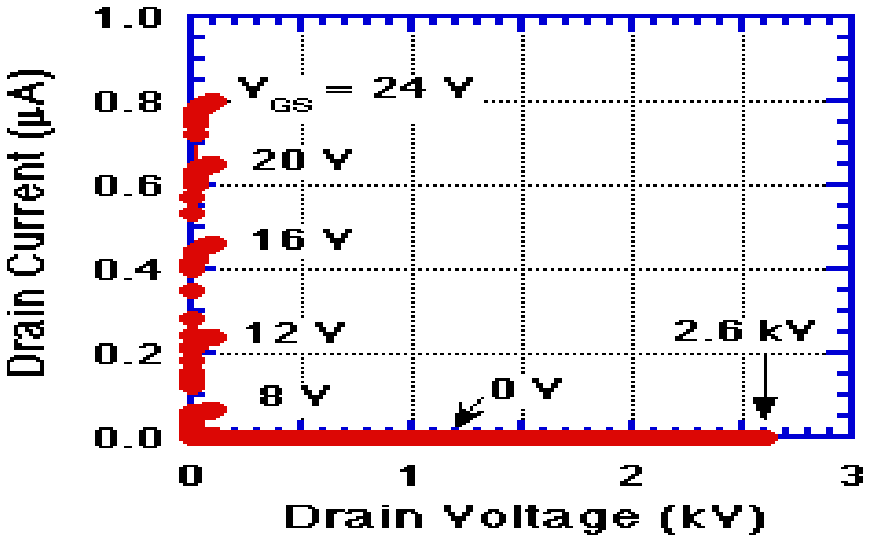

Figure 3.7. Current-voltage characteristics at room temperature. This device withstands a maximum drain voltage of 2.6 kV in the blocking state. I-V curves are not measured in the "middle" of the plot because of the high power dissipation in this region [40,41].

3.3 Silicon Carbide Schottky Barrier Diodes

Schottky barrier diodes (SBD's) are used as high-voltage rectifiers in many power switching applications. Whenever current is switched to an inductive load such as an electric motor, high-voltage transients are induced on the lines. To suppress these transients, diodes are placed across each switching transistor to clamp the voltage excursions. PN junction diodes could be used for this application, but they store minority carriers when forward biased, and extraction of these carriers allows a large transient reverse current during switching. Schottky barrier diodes are rectifying metal-semiconductor junctions, and their forward current consists of majority carriers injected

from the semiconductor into the metal. Consequently, SBD's do not store minority carriers when forward biased, and the reverse current transient is negligible. This means the SBD can be turned off faster than a PN diode, and dissipates negligible power during switching.

SiC Schottky barrier diodes are especially attractive because the breakdown field of SiC is about 8x higher than in silicon. In addition, because of the wide bandgap, SiC SBD's should be capable of much higher temperature operation than silicon devices. SBD's on 4H-SiC using both Ni and Ti as Schottky metals were fabricated [45]. Special edge termination is required to minimize field crowding at the edge of the metal contact. Boron atoms at 30 keV with a dose of $1x10^{15}$ cm^{-2} are implanted [46]. The sample is then annealed at 1050 C for 90 min. to remove the implant damage without activating the boron atoms. This results in a resistive layer at the surface that spreads the field lines without causing a significant increase in junction leakage. The cross section of the experimental device is shown in Fig. 3.8.

Forward and reverse I-V characteristics for the Ti and Ni SBD's are shown in Fig. 3.9. The barrier heights for Ti and Ni on 4H-SiC at room temperature are 0.8 and 1.3 V, respectively. The lower barrier height Ti gives lower forward voltage drop but higher reverse leakage current as compared to the Ni barrier. The reverse blocking voltages are 1480 and 1720 V, respectively. The blocking voltage of the Ni SBD is the highest yet reported for any SBD on SiC.

Ni Schottky diodes recently fabricated on a 50 μm epilayer of 4H-SiC [47]. These diodes exhibited blocking voltages as high as 4.9 kV, the highest yet reported for a SiC Schottky diode. Figure 3.10 shows forward and reverse current-voltage characteristics of a 425 μm diameter diode at room temperature

SiC Schottky diodes for in-circuit testing are also fabricated on large-area. These diodes were packaged at Cree Research and shipped to Harris Semiconductor, Mountaintop, PA, where they replaced silicon PiN diodes in an IGBT-driven inductive

switching circuit. Tests by Harris indicated that the switching energy of the IGBT circuit is reduced by a factor of four compared to the case with silicon PiN diodes [48].

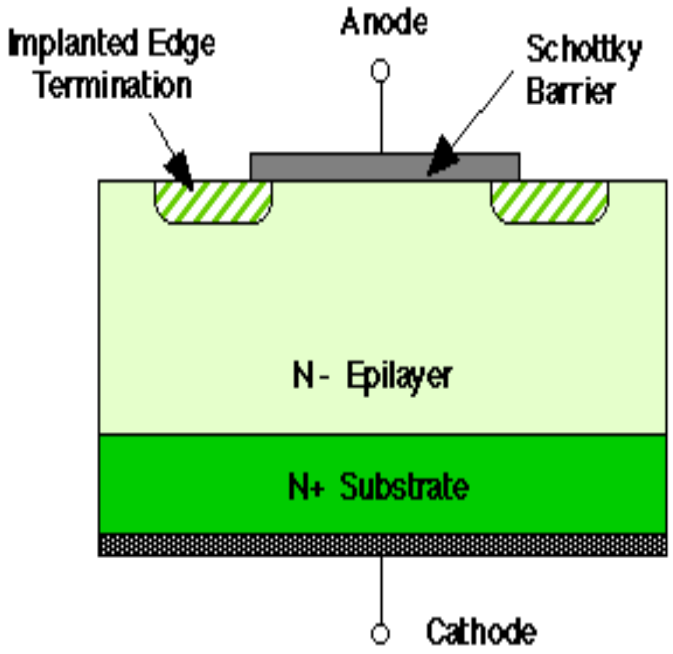

Figure 3.8. Cross section of an implant-edge-terminated Schottky barrier diode in SiC [45,46].

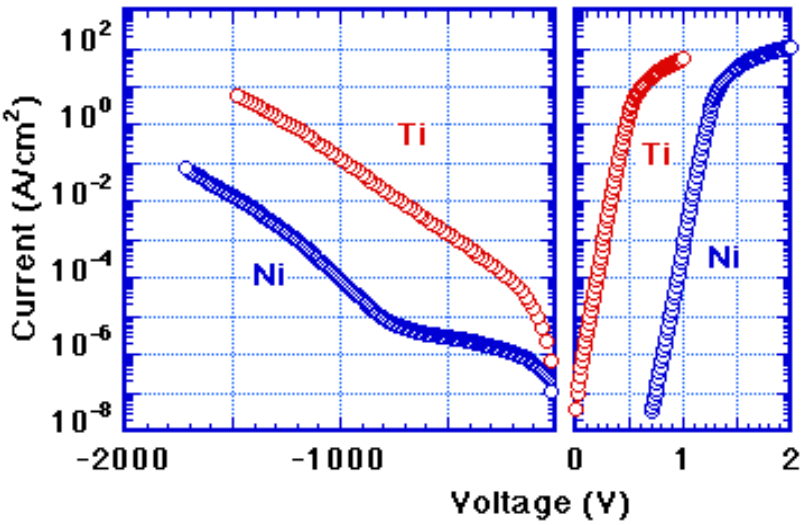

Figure 3.9. Forward and reverse current-voltage characteristics for Ti and Ni Schottky barrier diodes on 4H-SiC at room temperature [45,46].

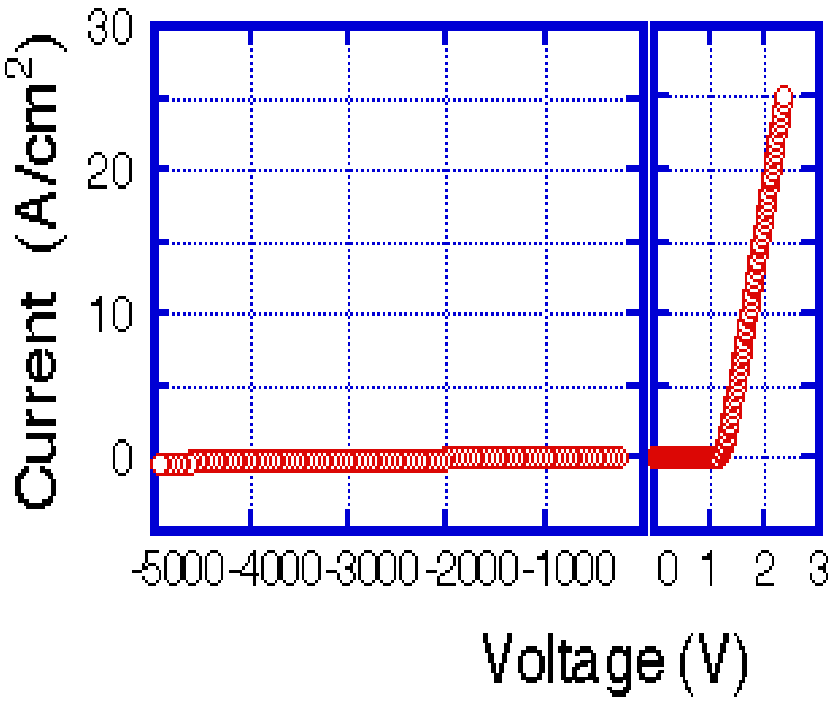

Figure 3.10 Forward and reverse current-voltage characteristics of a 425 μm diameter Ni Schottky barrier diode on a 50 μm 4H-SiC epilayer at room temperature. Blocking voltage is 4.9 kV and specific on-resistance is 43 mOhm-cm^2 [45,46].

3.4 Silicon Carbide IMPATT Diode Microwave Oscillatorss

Because of its high breakdown field, silicon carbide is an ideal semiconductor for the fabrication of high-power microwave devices. One device, in particular, that benefits from the high breakdown field of SiC is the IMPact ionization Avalanche Transit-Time (IMPATT) diode oscillator. IMPATT diodes deliver the highest RF power of any semiconductor microwave oscillator, and are used to produce carrier signals for microwave transmission systems, particularly airborne and ground-based radar.

Depending upon the design, IMPATT diodes can operate from a few GHz to a few hundred GHz.

The power-frequency product ($p f^2$) of an IMPATT diode scales as the square of the critical field for avalanche breakdown times the electron saturation drift velocity. In SiC, the critical field is about 10x higher than in silicon or GaAs, and the saturation drift velocity is about 2x higher. Thus, the power-frequency product (in the electronic limit) is theoretically expected to be about 400x higher for SiC IMPATT diodes than for diodes in silicon or GaAs.

A typical cross section of a Read-type (Hi-Lo) IMPATT diode is shown in Fig. 3.11. The diode is operated in reverse bias near breakdown, and both the N and N-

regions are completely depleted. The internal electric field is shown at the bottom of the figure. Because of the difference in doping between the "drift region" and "avalanche region", the electric field is highly peaked in the avalanche region and nearly flat in the drift region. In operation, avalanche breakdown occurs at the point of highest electric field, and this generates a large number of hole-electron pairs by impact ionization. The holes are swept into the cathode, but the electrons travel across the drift region toward the anode. As they drift, they induce image charges on the anode, giving rise to a displacement current in the external circuit that is 180° out of phase with the nearly sinusoidal voltage waveform. Figure 3.12 shows the buildup of microwave oscillations in the diode current and voltage when the diode is embedded in a resonant cavity and biased at breakdown. Figure 3.13 shows a close-up of the current and voltage waveforms after oscillations have stabilized. It is clear from Fig. 3.13 that the current is 180° out of phase with the voltage. This represents a NEGATIVE AC RESISTANCE, and corresponds to the net generation of microwave power by the diode.

Experimental IMPATT diodes have been fabricated in 4H-SiC with drift regions designed for X-band (10 GHz) and Ka-band (35 GHz) operation [50]. The breakdown characteristic is stable and non-destructive, provided the current is properly limited by the external circuit.

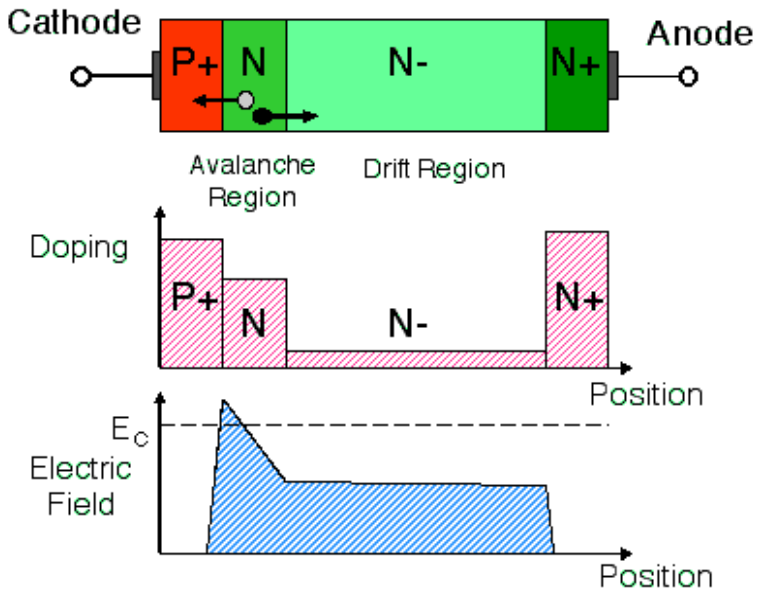

Figure 3.11. Cross section of a SiC IMPATT diode. Hole-electron pairs are created at the point of highest electric field (the "Avalanche Region"). Holes are swept into the cathode, but electrons drift toward the anode, inducing a displacement current in the external circuit as they drift [49].

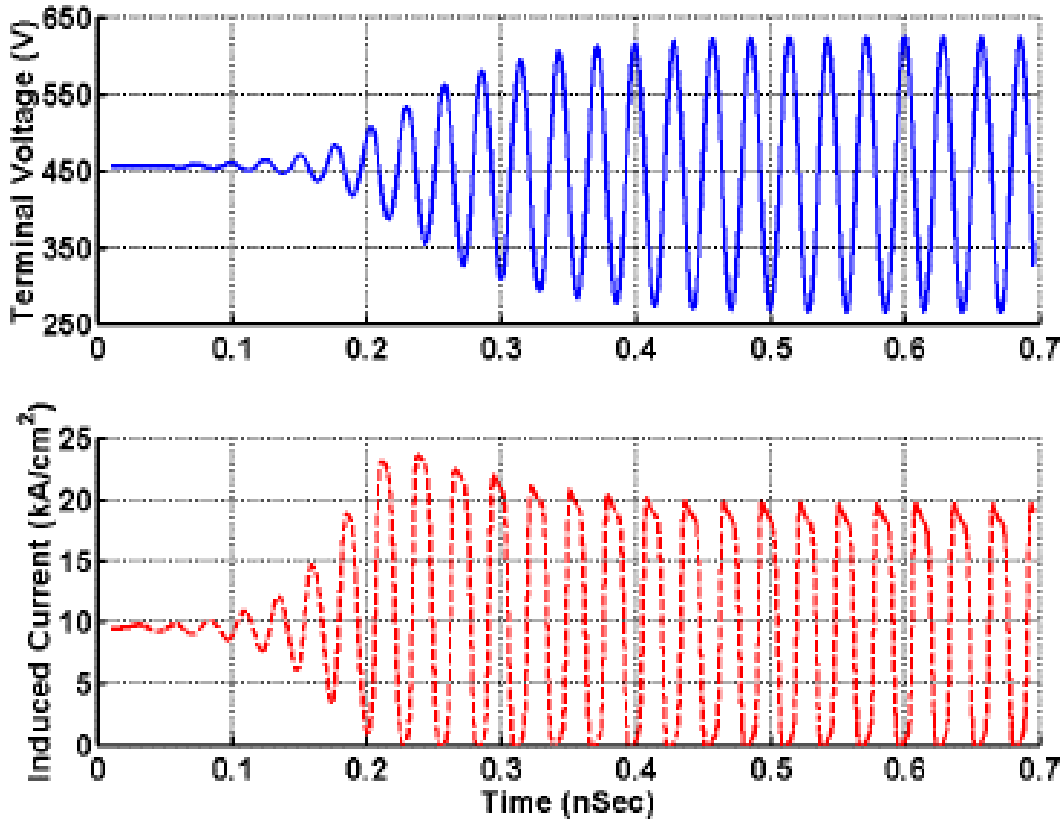

Figure 3.12. Buildup and stabilization of microwave oscillations, as predicted by a two-dimensional transient device simulator [49].

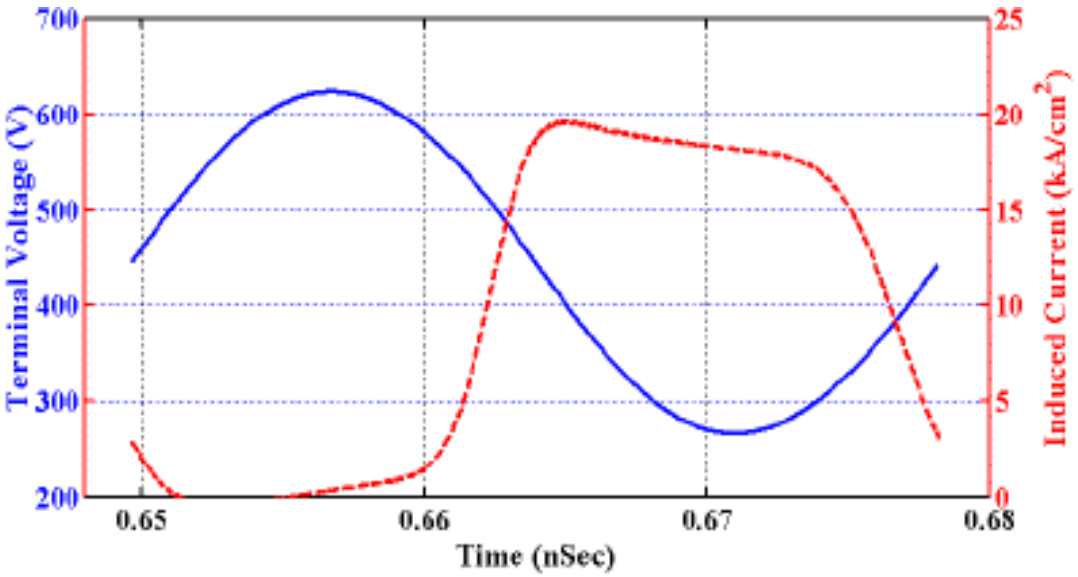

Figure 3.13. Close-up of a single cycle of Figure 3.12 after oscillations have stabilized. Note that the current and voltage are 180° out of phase, implying a negative ac resistance and the net generation of microwave power[49].

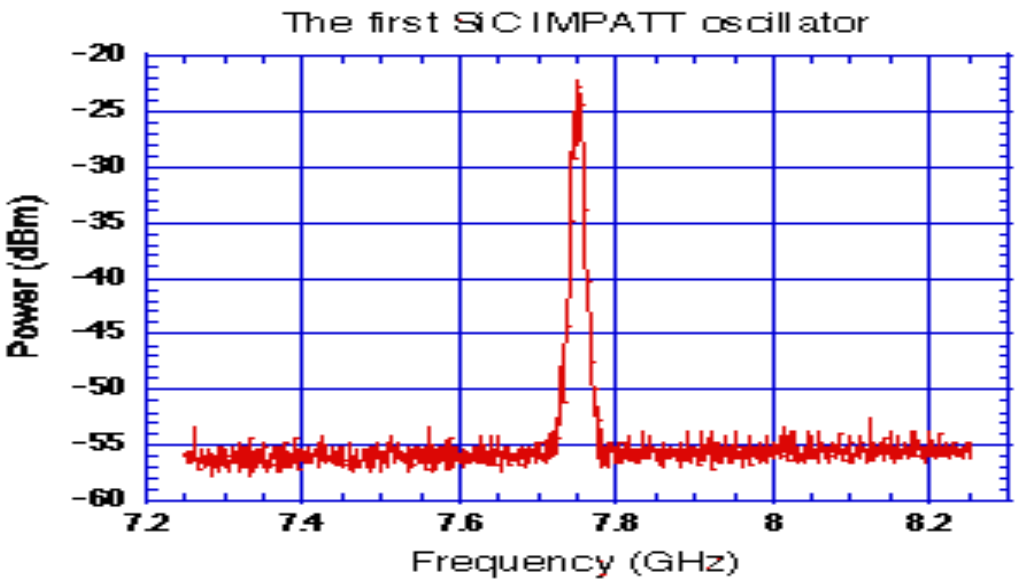

Figure 3.14. Spectrum of a SiC IMPATT diode operating in a waveguide cavity at X-band. The diode is pulsed at a low duty cycle to avoid excessive heating [49].

Figure 3.14 shows the spectrum of oscillation of an X-band diode in a microwave resonant cavity, as measured by a Tektronix 2755 spectrum analyzer [50]. The diode is pulsed to minimize internal heating, and the RF signal is heavily attenuated to protect the spectrum analyzer. This spectrum, first observed in the laboratory on May 16, 2000, is believed to be the first observation of IMPATT diode operation in SiC. Work is currently underway to optimize the microwave cavity design and bias circuit to achieve optimum microwave performance of the diode.

CHAPTER IV

Low Voltage Power Dissipation Analysis of 6H-SiC DIMOSFET with Gaussian Profile in the Drift Region

It has been pointed out earlier that Silicon Carbide is a potential candidate for high power devices. These include large breakdown voltages, large value of saturated drift velocity, low dielectric constant, high on state current density and lower specific on resistance dissipation. This would entail an additional advantage of a lower power dissipation and hence a reduction in the die-size which would eventually offset the cost of production of SiC devices.With a wider band gap of 6H-SiC of 3.0 electron volt a saturated drift velocity of $2x10^7$cm/sec, a higher critical field for breakdown of $4x10^6$V/Cm with a dielectric constant of 9.7[50,59], it has almost all the qualities for becoming a better candidate than silicon or even 3C-SiC as a basic material.

The 6H-SiC DIMOSFET need for low voltage analysis has a Gaussian profile as its impurity content in the drift region. The profile can be generated by ion-implantation from the drain end of the device, so that the projected R_P is close to the drain end of the device.The impurity concentration decays upwards from R_P as we approach the source. The mathematical analysis for evaluation the effective impurity concentration (N_{eff}) has been evaluated by integrating the Gaussian profile over the length of the drift region . the saturated value of V_{DS} has been set approximately equal to V_{GS}. The gate to source voltage .the maximum value of V_{GS} is evaluated using an oxide thickness of .1μm with an oxide breakdown field of 4MV per Cm. This gives a maximum value of V_{GS} of 40 V . Hence ,drain current and power dissipation analysis has been made for various values of V_{DS} <40V and V_{GS}<40V.

4.1 Basic Structure of the 6H-SiC Power MOSFET

Fig. 4.1 shows a cross section of a power MOSFET that has been fabricated using the process of diffusion using Silicon as substrate. The planar diffusion technology uses a infractory gate such as polysilicon. The P-base and N^+- source region are diffused through a common window that is determined by the edge of the

polysilicon gate. The difference in the lateral diffusion of these two regions determines the surface channel region. The p-base and N-drift region gives the forward blocking capability. The N-drift region is normally grown epitaxially on an N^+ substrate of 6H-SiC crystal, where the P-base and N^+ source regions are formed by ion-implantation.

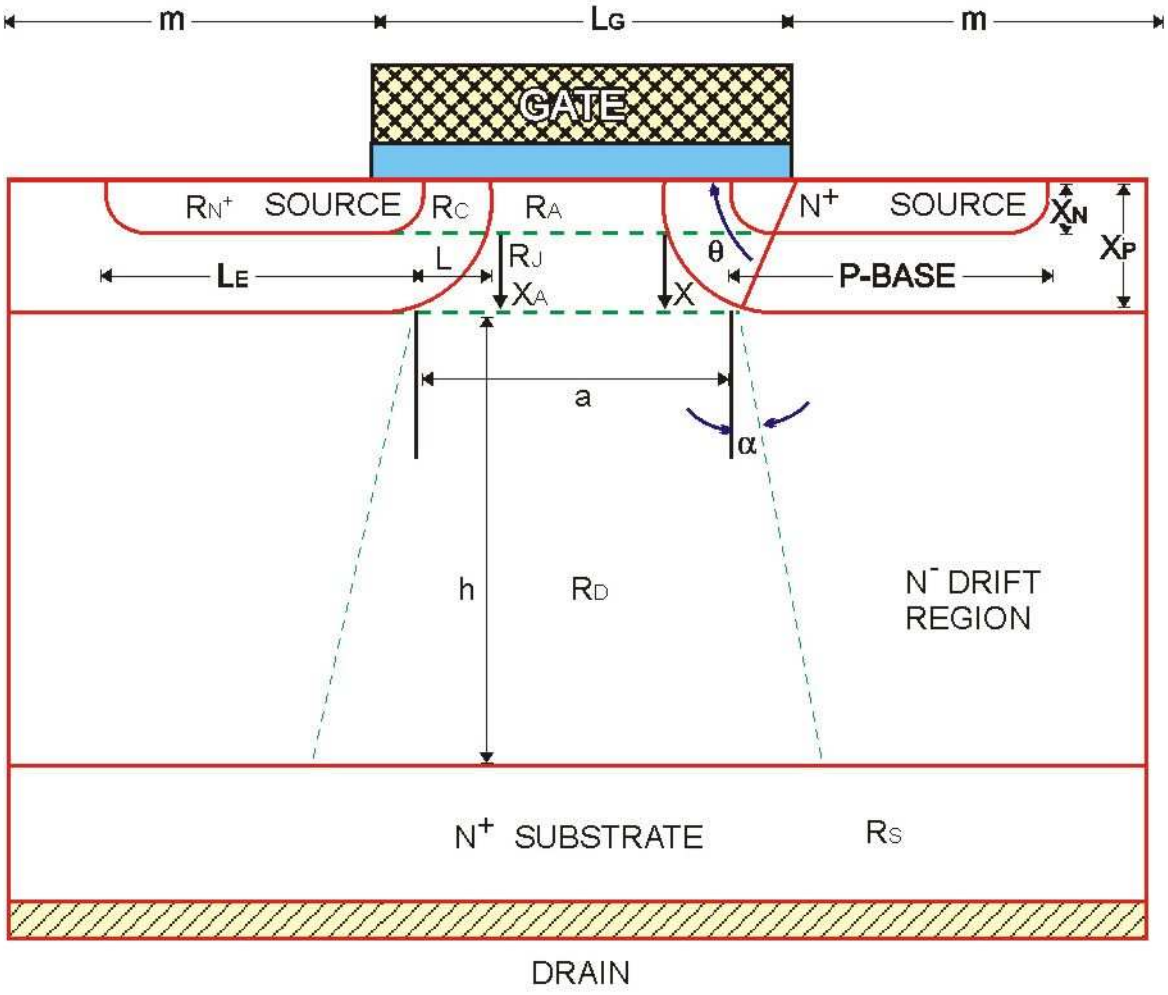

FIGURE 4.1: Cross Section of Power MOSFET

When operating the device, the p-base region is connected to the source metal by a break in the N^+ source region and a fixed potential is given to the p-base region. The gate and source are short circuited and a positive bias is applied to the drain. The p-base and N-drift region form a reverse biased p-n junction and this junction supports the drain voltage across the junction depletion region. Since the p-region is more heavily doped than the N-drift region, the depletion region is wider in the drift region than the p-base region. Then for a positive bias applied to the gate, an inversion channel is generated on top of p-region which allows an electron current to flow from N^+ source. At the edge of the p-base region and N-drift region near the surface and beneath the gate an accumulation layer is forward. This provides a second conducting path for the electron current which then enters the N-drift region and eventually flows to the drain. Between the accumulation and drift regions there exists an in-built n-channel JFET which has its own channel resistance. If we write down the total resistance or basically the specific on resistance of the device (or resistance area product) R_{onsp}, we may put it as:

$$R_{onsp} = R_{n+} + R_c + R_A + R_J + R_D + R_S \qquad (4.1)$$

Where,

R_{n+} is the contribution from the N^+ source region,

R_c is the channel resistance,

R_A is the accumulation layer resistance,

R_J is the resistance of the JFET pinchoff region,

R_D is the drift region resistance and,

R_S is the substrate resistance

These components are shown in Fig 4.1 and the unit of R_{onsp} is Ω-Cm^2. The blocking voltage is supported across the drift layer and serves as the minimum possible theoretical limit for the on resistance of a power MOSFET. Also at high applied voltages, resistance of the device is approximately equal to R_D as all other terms on the RHS of eq. (4.1) are negligible as compared to R_D and so, $R_{onsp} \cong R_D$. At lower values of V_B or smaller drain bias, eq. (4.1) will have to be evaluated as considering all

components on the RHS of that equation. This is because all of them are comparable to each other at these values of drain voltages, i.e. $V_{DS} << V_B$ [52]

In order to evaluate the device power dissipation Fig 4.1 has been modified[88] and appears as Fig 4.2.

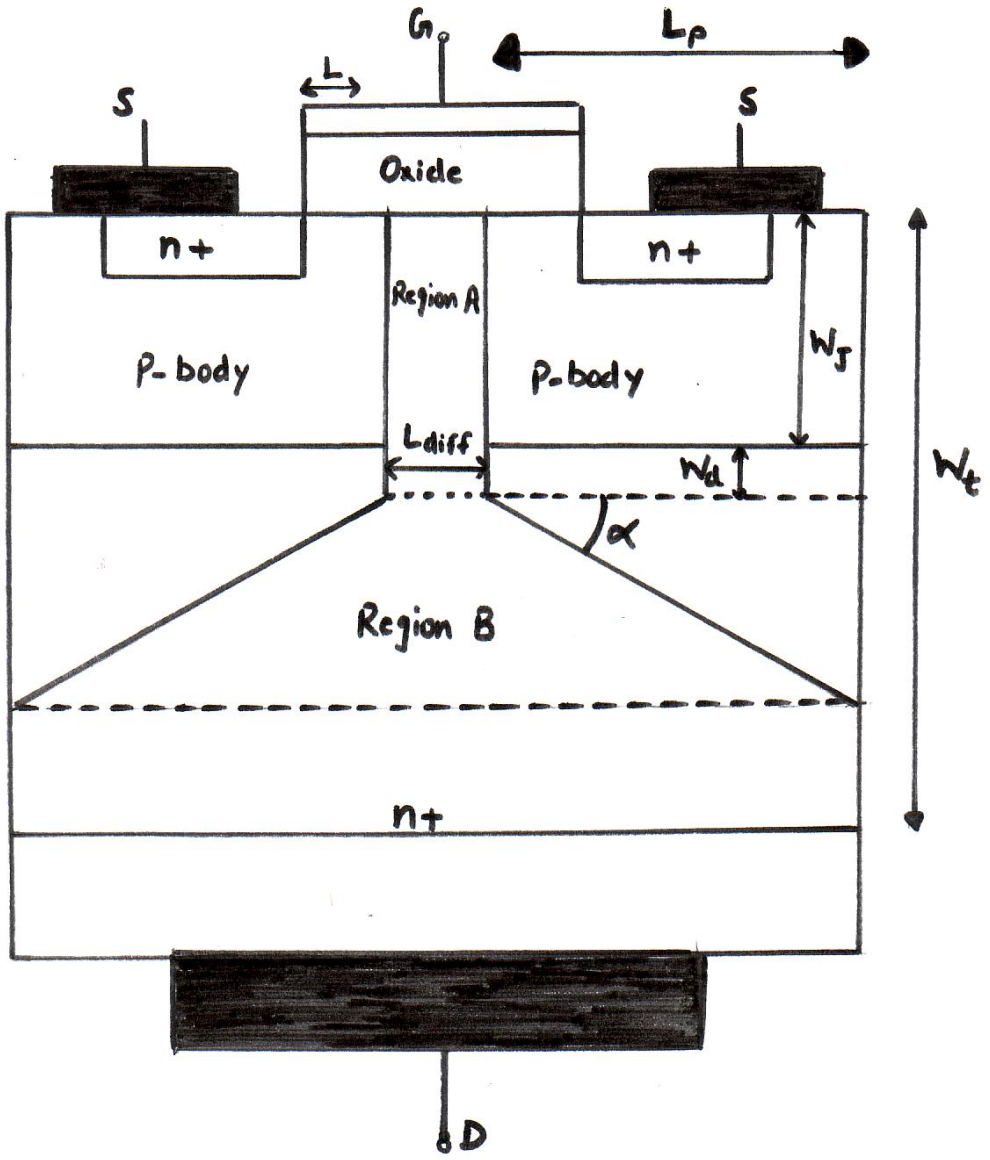

Fig 4.2

This includes the region namely an accumulation region A, a drift region B with a varying cross –sectional area and a drift region C with constant cross-sectin . Hence Wt

is the total vertical height ,Wj is the thickness of p-body ,Wd is the width of the depletion region ,L is the channel length formed below the gate and on the p-body ,L sep is the separation between p-bodies,Lp is the length of the p-body ,α is the slope of the drift region and W is the channel width.

4.2 <u>Mathematical Analysis</u> : in this section the basic device equations and a derivation to evaluate effective carrier concentration of a Gaussian profile

Consider the depletion region between the p-base and n-drift region as a one dimensional abrupt p-n junction .The width of the depletion region Wd is given by:

$$W_d = \{2\varepsilon s V_{DS}\}^{1/2} / \{qN_B\}^{1/2} \quad (4.2)$$

Where q is the electronic charge,N_B is the drift region doping level assumed uniform and the built –in potential V_{bi} has been neglected in comparison to V_{DS}.

The Specific on resistance ,R_{on-sp} of the drift layer can be given by using Fig 4.2 as:

$$R_{on-sp} = 1/ \mu_{eff} qN_B (W_t - W_j - W_d - L_p \tan\alpha) \quad (4.3)$$

the power dissipation $P_D(W)$ for the device for a 50% duty cycle is given by [89]:

$$P_D = 1/2(jon^2 R_{on-sp} + J_L V_B) \quad (4.4)$$

Where Jon is the on state current density in the linear region of (IDS-VDS) characterstics of the device in A/cm2, A is the device cross-sectional area , JL is the reverse saturation current and VB is the breakdown voltage since JL<<Jon,eq(4.4) may be simplified to give,

$$P_D = 1/2 (Jon^2 \, A \, R_{onsp}) \quad (4.5)$$

The magnitude of Jon can be calculated using the equation,

$$J_{on} = I_{DS}/A = I_{ch}/A \quad (4.6)$$

Where Ich is the channel current which flows from the n-Source over the p-body surface beneath the gate and is equal to the source to drain current IDS.

The voltagedrop across the channel region is Vch.

Calculations of the drop across the channel regions A,B,C gives the total voltage VDS from source to drain IDS=Ich, that Vch is about 15% of VDS. The magnitude of Ich is given by[88]

$$I_{DS}=I_{ch}= W\mu_{eff}V_{ch}[2C_{ox}(V_{GS}-V_T)-(C_{ox}+C_{do})V_{ch}] / 2L[1+(\mu_{eff}/2v_{sat}L)] \quad (4.7)$$

C_{ox} is the oxide capacitance ,C_{do} is the body capacitance and where μ_{eff} is the field dependent mobility and is given by[89]:

$$\mu_{eff} = \mu_o /1 +\{\mu_oE/v_{sat}) \quad (4.8)$$

Here μo is the doping dependent zero field mobility and its value is obtained from the 6H-SiC plot[59] since $C_{do}<<C_{ox}$ and $V_{GS}>>V_T$ eq.(4.7) simplifies to

$$I_{CH} = W\mu_{eff}V_{ch}[C_{OX}(2V_{GS}-V_{CH})] /2L[1+(\mu_{eff}/2v_{sat}L)] \quad (4.9)$$

The electric field E in eq.(4.8) is typically the longitudinal field in the channel and is given by,

$$E= Vch/L \quad (4.10)$$

Where Lis the channel length,the breakdown voltage VB can be calculated from the equation,

$$V_B =E_CW_d /2 \quad (4.11)$$

where Ec is the critical field given by,

$$Ec=1.95x10^4xN_B.^{131} \quad (4.12)$$

Hence for any given doping level N_B, it is easy to calculate $R_{o\ nsp}$ and V_B for any given value of V_{DS}.

4.2.2 The Effective Carrier Concentration (N_{eff}) of a Gaussian profile in the drift region.

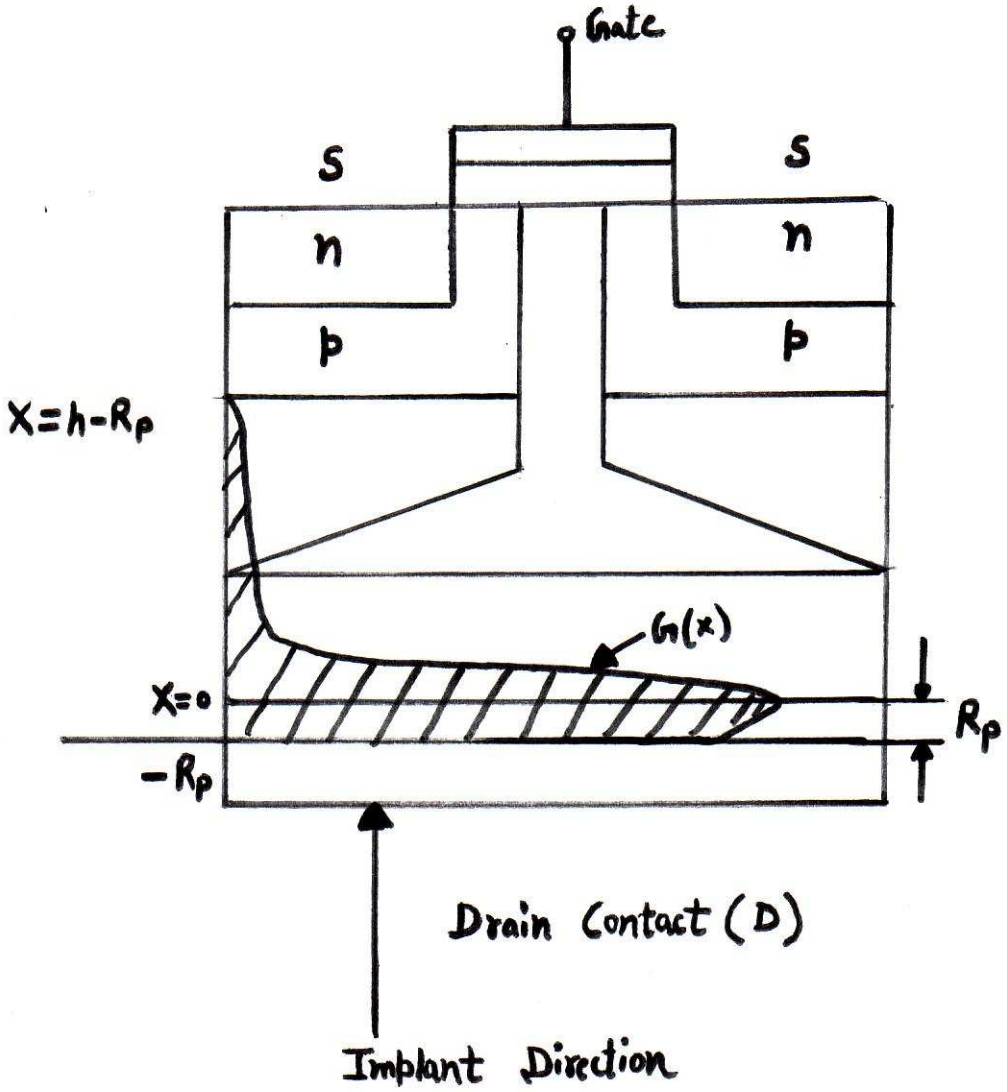

Fig 4.3

The doping profile considered here is generated in the drift region by carrying out ion – implantation from the drain end into the drift region.The projected range Rp and the

Gaussian profile that is generated is shown as the function G(x) in the drift region and is expressed as:

$$G(x) =(S/ (2\Pi)^{1/2}\sigma_p)\exp[-(x-Rp)^2/2\sigma p^2] \quad (4.13)$$

where S is the ion dose per unit area and σ_p is the longitudinal or projected straggle. Consider an element dx at a distance x from the origin with cross-sectional area $A_o$equal to the area of the drift region.This gives the total impurity content in the element dx as $A_oG(x)dx$ from –Rp to h-Rp

$$N_d=\int_{-Rp}^{h-Rp} A_OG(x)dx =\int_{-Rp}^{h-Rp}A_O (S/(2\Pi)^{1/2}\sigma_p)\exp[-(x-Rp)^2/2\sigma p^2] \, dx \quad (4.14)$$

Eq.(4.14) upon integration yields,

$$N_d=A_OS[\text{erf}(y)]_{Y1}^{y2}$$

$$Y_1= - (2R_p) / (\sigma_p)$$

$$\text{and } y_2 = h-2R_p / \sigma_p \quad (4.15)$$

where erf is the error function the limits of Y being
thus effective impurity concentration in the drift region is given by,

$$N_{eff}= N_d/ A_oh = S/h [\text{erf}(y)]_{Y1}^{y2} \quad (4.16)$$

Calculations for evaluation of channel current ,I_{ch} and power dissipation ,P_D can be carried out using the same set of equations given in sec.4.2.1 above, the only change being that N_B will have to be replaced by N_{eff} given by eq.(4.16). The magnitude of N_{eff} will of course depend upon the ion doze and ion energy and will be effected in the magnitude of R_p and σ_p.

4.3 Calculations and Related Graphs.

In calculating the current I_{DS} and power dissipation P_D. We have used the following parameters with the value quoted against each of them:

Channel length L =5μm

h =65μm

a =15μm

w =300μm =300x10^{-4}cm

A =wxlength=(300x15) μm^2=4500x$10^{-8}$$cm^2$

Cox=8.59x10-8 F/cm^2

V_G =40V

V_D=(5 to 40) V

V_{ch}=15% of V_{DS}

V_T =1V

W_t=40x10-^{4}cm

W_j=10x10-^{4}cm

L_p=25x10-^{4}cm

α =25°

For $N_B=10^{15}$, μ_o =530 cm^2/V.sec

For $N_B=10^{16}$,μ_o =500 cm^2/V.sec

For $N_B=10^{17}$,μ_o =280 cm^2/V.sec

The set of equations were then made on the basis of eqs.(4.2) to (4.15). The results are quoted in tables (4.1 to 4.15). The plots are given in Figs 4.2 to 4.15 respectively.

4.4 Device Discussions

The drift region of the 6H-SiC DIMOSFET using a Gaussian profile shows that with increase in energy and dose of implanted Phosphorous ions results in an increase in the projected range,longitudnal straggle and the effective doping(N_{eff}). This is shown in Table 4.1.it is also seen that the effective doping level of the drift region using a Gaussian

profile can be easily raised to 10^{16} atoms/cc or above.the effective mobility(μ_{eff}) of carriers in the channel region is field dependent and depends both on the doping level of the p-body taken to be equal to N_{eff} or N_B of the drift region. The results are shown in table 4.2 & 4.3 and are reproduced in Figs . 4.4 and 4.5. An analysis of this data shows that there are very little variations in μeff in case of both Gaussian and Uniform doping for the same doping level and drain –to-source voltage,V_{DS}.

The breakdown voltage V_B for different values of V_{DS} but same doping level shows that V_B remains almost the same .this can be verified for the data for N_{eff}=9.2x1016/cc and $N_B=10^{17}$/cc.from tables 4.4 and 4.5 respectively.the related graphs appear in Fig.4.6 and 4.7 respectively.The values of critical field for breakdown,E_C also follows the same pattern as V_B when its variations with doping level and V_{DS} is analysed.these are shown in table 4.6 & 4.7 and also in Figs. 4.8 and 4.9 respectively. The nature of variations of Ron-sp with N_B and V_B as also N_{eff} and V_B has been obtained from equations (4.11) & (4.12) and follows the normal pattern of inverse proportionality of V_B and $R_{on\text{-}sp}$ with doping level.Figs 4.10 and 4.11 shows these results.

The channel current densities J_{ch} treated equal to the drain current for different values of N_{eff} and N_B have been obtained using equation (4.9) for various values of V_{DS}. The results show Jch increase with increase in V_{DS} but a decrease in Jch can be seen at a single value of V_{DS} for incresing N_B. The latter effect is due to a decrease in μ_{eff} with increase in V_{DS} or channel voltage V_{ch} treated to 15% of V_{DS}.

The power Dissipation (P_D) of the DIMOSFET for different values of V_{DS} and N_B or N_{eff} is shown in Table 4.12 and 4.13 .It is seen an increase in P_D results for a decrease in N_B and an increase in V_{DS}. However,Gaussian profiles show a decline in P_D at the same

value of N_{eff} compared to N_B for uniform doping at the same V_{DS}. This can be verified from Tables 4.12 and 4.13 as also graphs shown in Figs 4.12 & 4.13

Lastly P_D obtained for different V_B show an increase in P_D with decrease in doping level and increase in V_B. The results are shown in Table 4.14 and 4.15 for uniform doping and Gaussian profiles.The results also graphically shown in Figs 4.14 & 4.15

4.3 Tables and their related Graphs :

Table 4.1: Effective Doping N(eff) for Phosphorous in Gaussian Distribution:

Energy	Dose	Projected Range	Logitudnal Straggle	Integral	N(eff) /CC
Kev	(cm-2)	$R_p(\mu m)$	$\sigma_p(\mu m)$	I	
50	$3.4x10^{14}$	0.059	0.027	$8.54x10^{14}$	$5.2x10^{16}$
100	$6.0x10^{14}$	0.097	0.039	$1.50x10^{15}$	$9.3x10^{16}$
250	$1.2x10^{15}$	0.249	0.073	$3.01x10^{15}$	$1.9x10^{17}$
500	$1.8x10^{15}$	0.47	0.109	$6.28x10^{15}$	$3.9x10^{17}$
750	$2.2x10^{15}$	0.616	0.119	$5.53x10^{15}$	$3.4x10^{17}$
1.0 **Mev**	$2.4x10^{15}$	0.764	0.131	$6.03x10^{15}$	$3.7x10^{17}$
2.0 **Mev**	$2.8x10^{15}$	1.28	0.157	$7.03x10^{15}$	$4.3x10^{17}$
3.0 **Mev**	$3.0x10^{15}$	1.67	0.163	$7.54x10^{15}$	$4.6x10^{17}$
4.0 **Mev**	$3.2x10^{15}$	2	0.168	$8.04x10^{15}$	$4.9x10^{17}$

Table 4.2 : Values of Mobility(μ cm^2/vsec) at different values of Uniform Doping(N_B/CC) equal to p-body doping for different values of V_{DS} levels of Uniform Distribution.

V_{DS}	$N_{B=10^{15}}$/cc μ_o=530cm^2/v.sec	$N_{B=10^{16}}$/cc μ_o=500cm^2/v.sec	$N_{B=10^{17}}$/cc μ_o=280cm^2/v.sec
V_{DS}(Volts)	μ(cm^2/vsec)	μ(cm^2/vsec)	μ(cm^2/vsec)
5	382.67	366.63	232.62
15	245.74	239.09	173.79
25	181.02	177.38	138.72
35	143.28	140.99	115.42

Table 4.3: Values of Effective Mobility(μcm^2/vsec) at different values of N_{eff} equal to p body doping for different V_{DS} levels of Gaussian Distribution.

V_{DS}	$N_{eff=5.2x10^{16}}$ /cc μ_o=500cm^2/v.sec	$N_{eff=9.2x10^{16}}$ / cc μ_o=280cm^2/v.sec	$N_{eff=18.5x10^{17}}$/cc μ_o=280cm^2/v.sec	$N_{eff=38.5x10^{17}}$/cc μ_o=280cm^2/v.sec	$N_{eff=33.9x10^{17}}$/ cc μ_o=280cm^2/v.sec
V_{DS}(Volts)	μ_{eff}(cm^2/vsec)	μ_{eff}(cm^2/vsec)	μ_{eff}(cm^2/vsec)	μ_{eff}(cm^2/vsec)	μ_{eff}(cm^2/vsec)
5	366.63	232.62	232.62	232.62	232.62
15	239.09	173.79	173.79	173.79	173.79
25	177.38	138.72	138.72	138.72	138.72
35	140.99	115.42	115.42	115.42	115.42

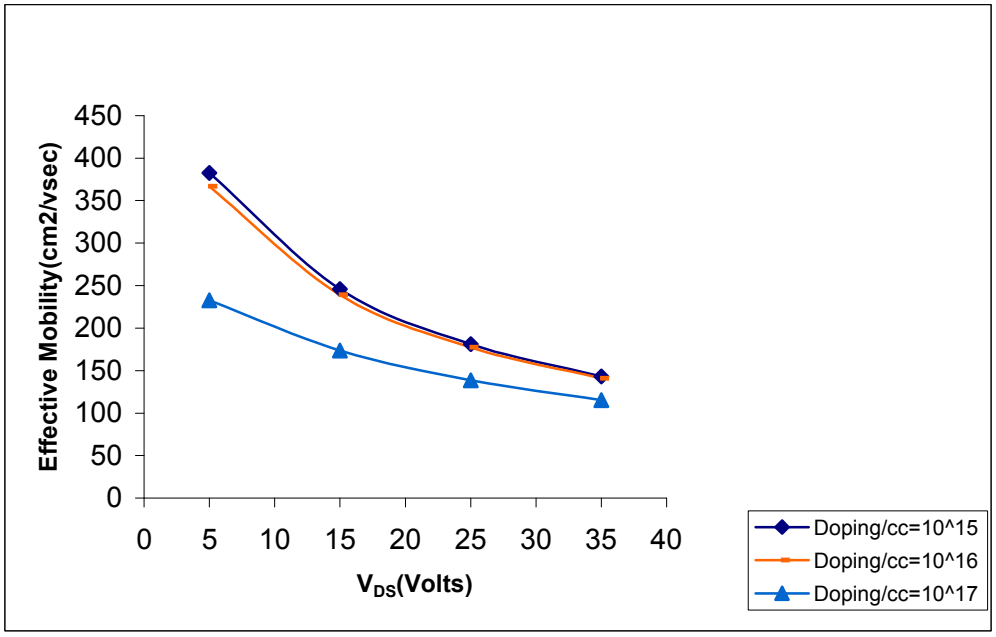

Fig 4.4 : Plot of Mobility at different values of Doping for different V_{DS} levels of Uniform Doping.

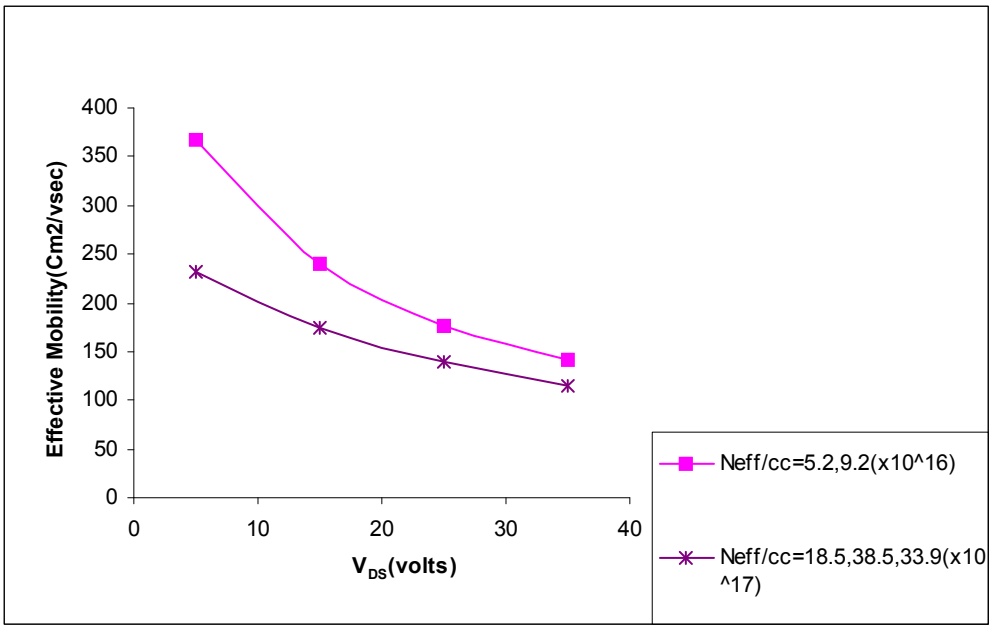

Fig 4.5: Plot of Effective Mobility at different values of N_{eff} for different V_{DS} levels of Gaussian Distribution

Table 4.4 : Values of Breakdown voltage at different values of V_{DS} for different values of Doping(N_B/CC) of Uniform Distribution.

Doping ($N_{B/CC}$)	**V_{DS}=5V**	**V_{DS}=15V**	**V_{DS}=25V**	**V_{DS}=35V**
N_B/ccx10^{15}	**$V_{B(Volts)}$**	**$V_{B(Volts)}$**	**$V_{B(Volts)}$**	**$V_{B(Volts)}$**
1	208.5	361.2	466.3	551.7
10	89.09	154.29	199.21	235.71
100	38.11	66.01	85.23	100.84

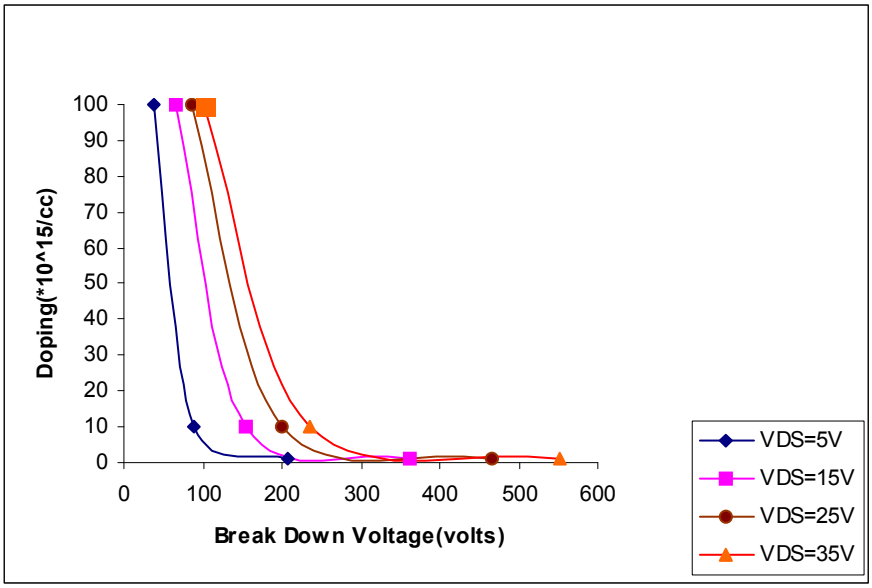

Fig 4.6: Plot of Breakdown voltage at different levels of V_{DS} for different values of Doping of Uniform Distribution.

Table 4.5 : Values of Breakdown voltage at different values of V_{DS} for different values of N_{eff} of Gaussian Distribution:

Neffective (N_{eff}/cc)	**V_{DS}=5V**	**V_{DS}=15V**	**V_{DS}=25V**	**V_{DS}=35V**
Neffective (x 10^{16} /cc)	**$V_{B(Volts)}$**	**$V_{B(Volts)}$**	**$V_{B(Volts)}$**	**$V_{B(Volts)}$**
5.2	48.48	83.98	108.42	128.28
9.2	39.63	68.64	88.62	104.85
18.5	30.32	52.52	67.8	80.22
38.5	23.04	39.89	51.51	60.95
33.9	24.31	42.09	54.36	64.33

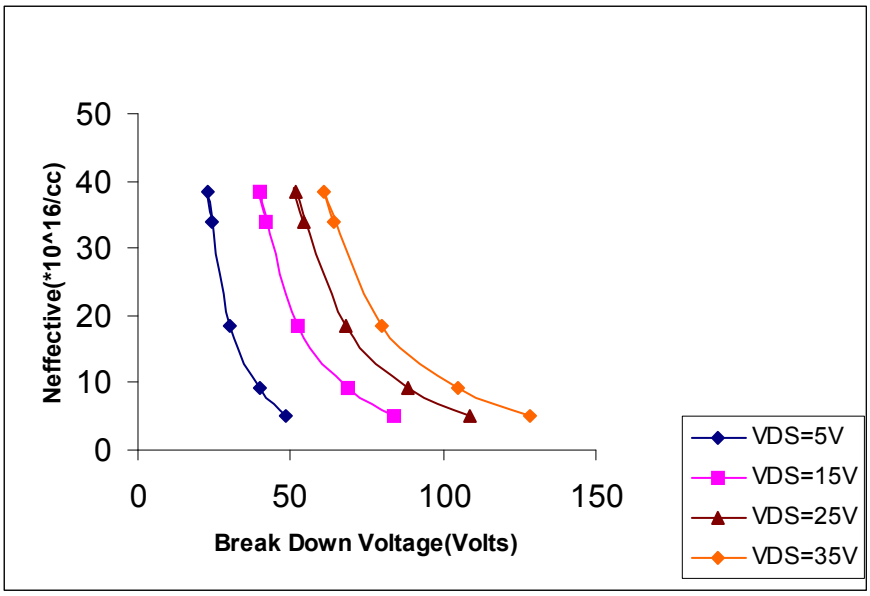

Fig 4.7 : Plot of Breakdown voltage at different levels of V_{DS} for different values of N_{eff} of Gaussian Distribution.

Table 4.6 : Values of Breakdown Voltages at different values of V_{DS} for different Electric Field(E_C) levels of Uniform Distribution.

E_C(V/cm)	V_{DS}=5 v	V_{DS}=15 v	V_{DS}=25 v	V_{DS}=35 v
Electric Field(x10^6)	$V_{B(Volts)}$	$V_{B(Volts)}$	$V_{B(Volts)}$	$V_{B(Volts)}$
(N_B=10^{15}) E_C=1.8	208.5	361.2	466.3	551.7
(N_B=10^{16}) E_C =2.4	89.09	154.29	199.21	235.71
(N_B=10^{17}) E_C =3.3	38.11	66.01	85.23	100.84

Table 4.7 : Values of Breakdownvoltage(V_B) at different values of V_{DS} for different Electric Field(E_C) levels for Gaussian Distribution.

Electric Field (V/cm)	V_{DS}=5V	V_{DS}=15V	V_{DS}=25V	V_{DS}=35V
E_C(x10^6 V/cm)	$V_{B(Volts)}$	$V_{B(Volts)}$	$V_{B(Volts)}$	$V_{B(Volts)}$
(N_{eff}=5.2x10^{16}) E_C=3	48.48	83.98	108.42	128.28
(N_{eff}=9.2x10^{16}) E_C=3.3	39.63	68.64	88.62	104.85
(N_{eff}=1.85.2x10^{16}) E_C=3.6	30.32	52.52	67.8	80.22
(N_{eff}=3.85.2x10^{16}) E_C= 3.9	23.04	39.89	51.51	60.95
(N_{eff}=3.39x10^{16}) E_C=3.8	24.31	42.09	54.36	64.33

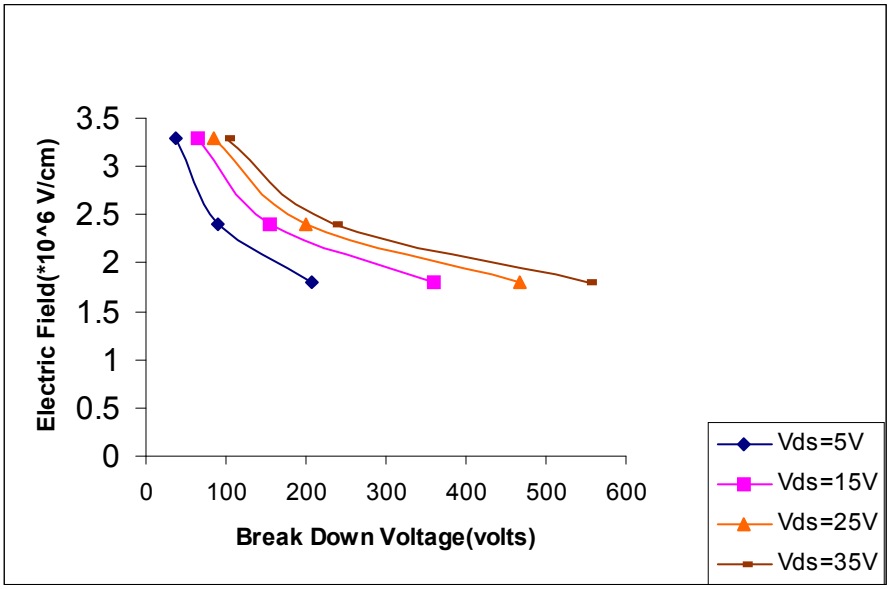

Fig 4.8 : Plot of Breakdown Voltages at different values of V_{DS} for different Electric Field levels of Uniform Distribution.

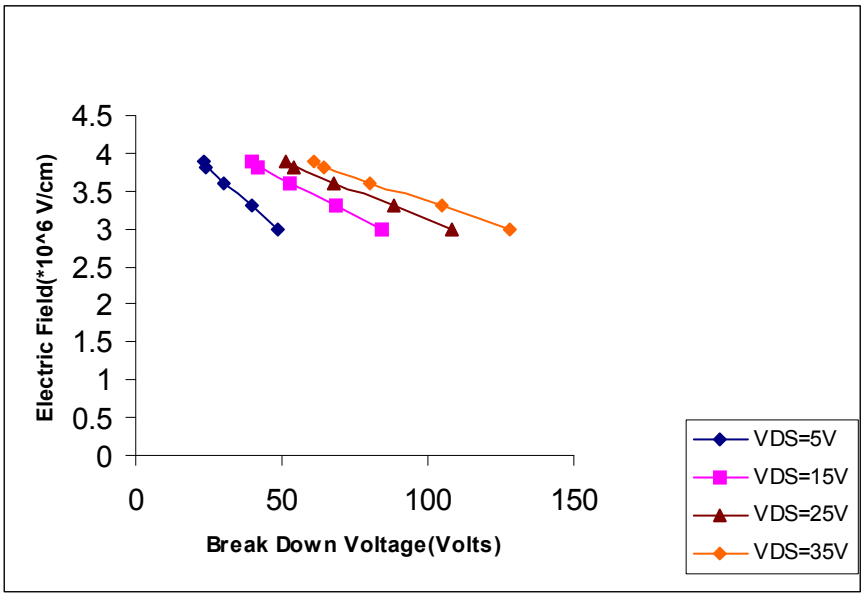

Fig 4.9: Plot of Breakdown voltage at different values of V_{DS} for different Electric Field levels for Gaussian Distribution.

Table 4.8 : Values of Specific On-Resistance at different values of Breakdown Voltages(volts) for different Doping levels(N_B) of Uniform Distribution.

$N_{B=1015/cc}$	$N_{B=10}^{15}$/cc	$N_{B=10}^{16}$/cc	$N_{B=10}^{16}$/cc	$N_{B=10}^{17}$/cc	$N_{B=10}^{17}$/cc
$V_{B(Volts)}$	$R_{ON-SPX10}^{-1}$ (ΩCm2)	$V_{B(Volts)}$	$R_{ON-SPX10}^{-1}$ (ΩCm2)	$V_{B(Volts)}$	$R_{ON-SPX10}^{-1}$ (ΩCm2)
208.5	0.26	89.09	0.03	38.11	0.0048
294.92	0.31	125.99	0.037	53.9	0.0056
361.21	0.36	154.29	0.044	66.01	0.0064
417.09	0.41	178.17	0.052	76.23	0.0072

466.32	0.45	199.21	0.059	85.23	0.008
510.82	0.49	218.22	0.066	93.36	0.0088
551.76	0.53	235.71	0.073	100.84	0.0096
589.86	0.57	251.97	0.079	107.8	0.0103

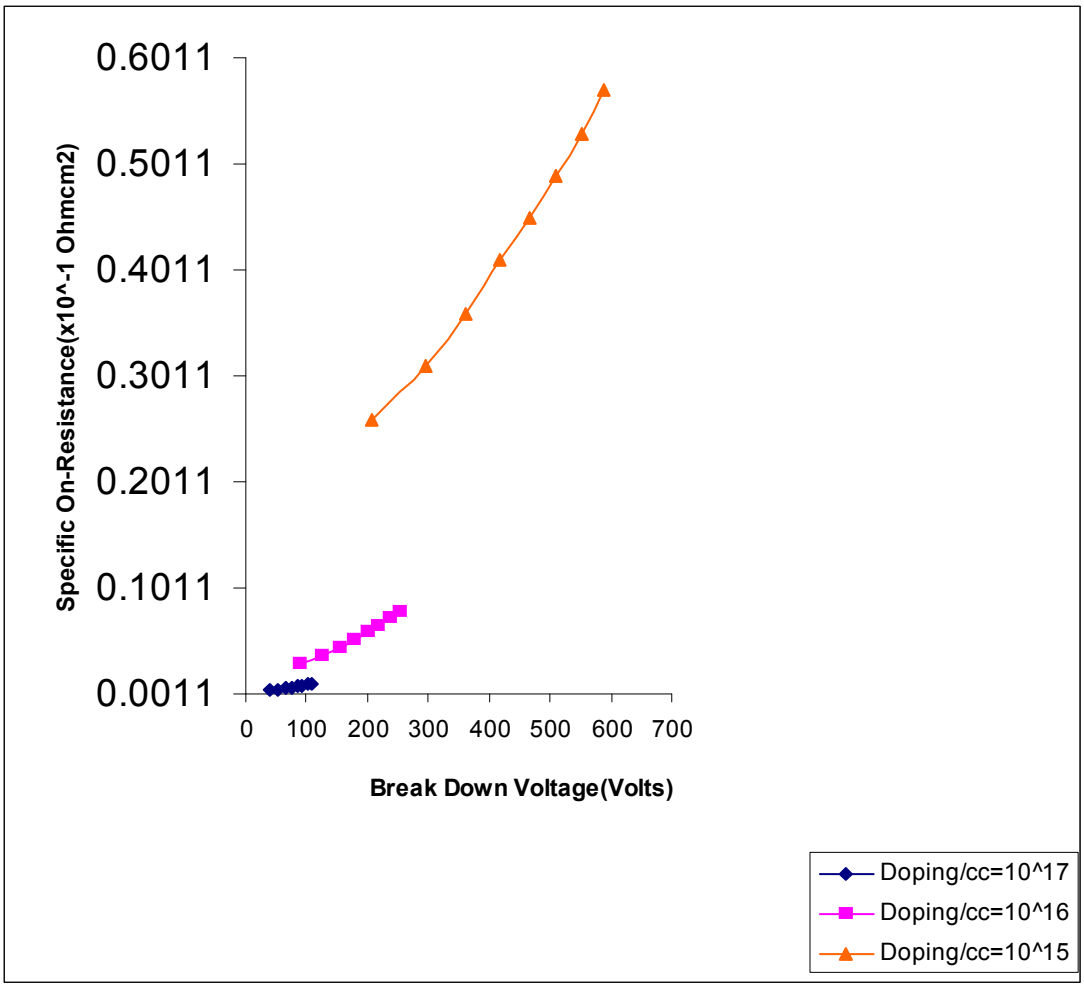

Fig 4.10 : Plot of Specific On-Resistance at different values of Breakdown Voltages(volts) for different Doping levels(N_B) of Uniform Distribution.

Table 4.9 : Values of Specific On Resistance at different values of Breakdown Voltages for different Neffective levels of Gaussian Distribution.

$N_{eff=5.2x10^{16}/cc}$	$N_{eff=5.2x10^{16}/cc}$	$N_{eff=9.2x10^{16}/cc}$	$N_{eff=9.2x10^{16}/cc}$	$N_{eff=18.5x10^{17}/cc}$	$N_{eff=18.5x10^{17}/cc}$	$N_{eff=38.5x10^{17}/cc}$	$N_{eff=38.5x10^{17}/cc}$	$N_{eff=33.9x10^{17}/cc}$	$N_{eff=33.9x10^{17}/cc}$
$V_{B(Volts)}$	$R_{ON-SPX10^{-4}}$ (ΩCm2	$V_{B(Volts)}$	$R_{ON-SPX10^{-4}}$ (ΩCm2)	$V_{B(Volts)}$	$R_{ON-SPX10^{-4}}$ (ΩCm2	$V_{B(Volts)}$	$R_{ON-SPX10^{-4}}$ (ΩCm2)	$V_{B(Volts)}$	$R_{ON-SPX10^{-4}}$ (ΩCm2)
48.48	5.91	39.63	3.33	30.32	2.64	23.04	1.27	24.31	1.44
68.57	7.43	56.05	4.21	42.88	3.07	32.58	1.48	34.38	1.68
83.98	9.01	68.64	5.08	52.52	3.51	39.89	1.69	42.09	1.92
96.97	10.48	79.26	5.95	60.64	3.94	46.07	1.9	48.62	2.16
108.42	11.95	88.62	6.78	67.8	4.37	51.51	2.11	54.36	2.4
118.77	13.43	97.06	7.64	74.27	4.81	56.43	2.32	59.55	2.64
128.28	14.91	104.85	8.49	80.22	5.23	60.95	2.54	64.33	2.87
137.14	16.41	112.1	9.34	85.77	5.66	65.17	2.75	68.76	3.11

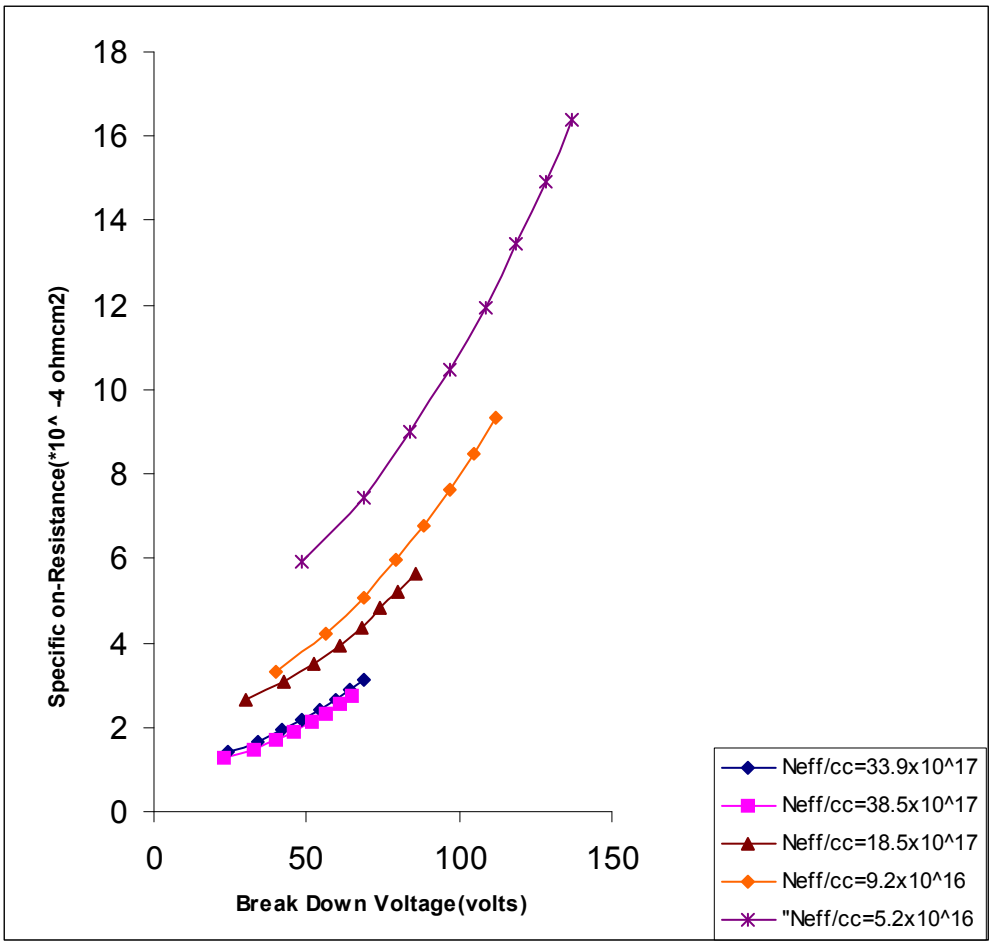

Fig 4.11 : Plot of Specific On Resistance at different values of Breakdown Voltages for different Neffective levels of Gaussian Distribution.

Table 4.10: Values of Channel Current and Channel Current density at various values of V_{CH} and V_{DS} for different Doping levels(N_B) of Uniform Distribution.

V_{DS}	V_{CH}	$N_B=10^{15}$	$N_B=10^{15}$	$N_B=10^{16}$	$N_B=10^{16}$	$N_B=10^{17}$	$N_B=10^{17}$
(Volts)	(Volts)	I_{CH} (A)	$J_{CH}x10^3$ (A/cm2)	I_{CH}(A)	$J_{CH}x10^3$ (A/cm2)	I_{CH}(A)	$J_{CH}x10^3$ (A/cm2)
5	0.75	0.056	1.252	0.053	1.199	0.034	0.765
10	1.5	0.086	1.924	0.083	1.862	0.057	1.288
15	2.25	0.105	2.334	0.102	2.272	0.074	1.663
20	3	0.117	2.606	0.114	2.546	0.087	1.942
25	3.75	0.125	2.793	0.123	2.737	0.097	2.155
30	4.5	0.131	2.926	0.129	2.874	0.104	2.32
35	5.25	0.136	3.022	0.133	2.973	0.11	2.45
40	6	0.139	3.093	0.137	3.046	0.114	2.552

Table 4.11: Values of Channel current and channel current density at various values of V_{CH} and V_{DS} for different Doping levels(N_B) of Gaussian Distribution.

V_{DS}	V_{CH}	$N_{eff}=5.2x10^{16}$	$N_{eff}=5.2x10^{16}$	$N_{eff}=1.85x10^{17},9.2x10^{16}$	$N_{eff}=1.85x10^{17},9.2x10^{16}$
(Volts)	(Volts)	I_{CH}(A)	$J_{CH}x10^3$ (A/cm2)	I_{CH}(A)	$J_{CH}x10^3$ (A/cm2)
5	0.75	0.053	1.199	0.034	0.765
10	1.5	0.083	1.862	0.057	1.288
15	2.25	0.102	2.272	0.074	1.663
20	3	0.114	2.546	0.087	1.942
25	3.75	0.123	2.737	0.097	2.155
30	4.5	0.129	2.874	0.104	2.32
35	5.25	0.133	2.973	0.11	2.45
40	6	0.137	3.046	0.114	2.552

Table 4.12 :Values of Power Dissipation(w) at different values of Doping for different V_{DS}(volts) levels of Uniform Distribution.

V_{DS}	$N_{B=10^{15}/CC}$	$N_{B=10^{16}/CC}$	$N_{B=10^{17}/CC}$
V_{DS}(Volts)	P_D(w)	P_D(w)	P_D(w)
5	0.92	0.097	0.0064
15	4.4	0.51	0.040
25	7.9	0.9	0.083
35	10.9	1.45	0.12

Table 4.13 : Values of Power Dissipation(mw) at different values of Neffective levels(N_{eff}/cc) for different V_{DS}(Volts) levels of Gaussian Distribution.

V_{DS}	$N_{eff=5.2x\ 10^{16}/cc}$	$N_{eff=9.2x\ 10^{16}/cc}$	$N_{eff=18.5x\ 10^{17}/cc}$	$N_{eff=38.5x\ 10^{17}/cc}$	$N_{eff=33.9x\ 10^{17}/cc}$
V_{DS}Volts)	P_D (mw)	P_D (mw)	P_D (mw)	P_D (mw)	P_D (mw)
5	19.13	3.19	3.48	1.67	1.9
15	104.81	20.16	21.85	10.55	11.98
25	201.44	42.42	45.75	22.06	25.11
35	296.66	65.87	70.76	34.3	38.87

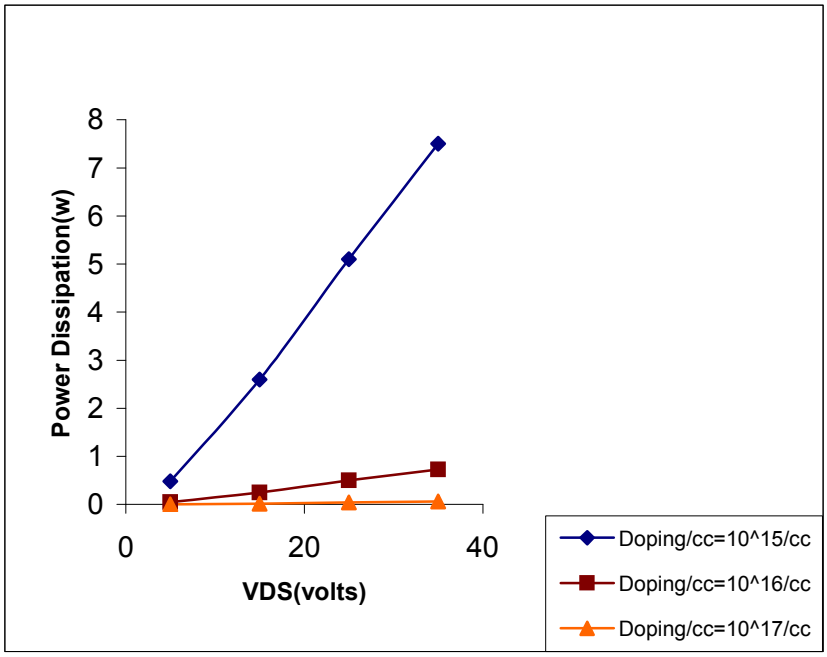

Fig 4.12 :Plot of Power Dissipation(w) at different values of Doping for different V_{DS}(volts) levels of Uniform Distribution.

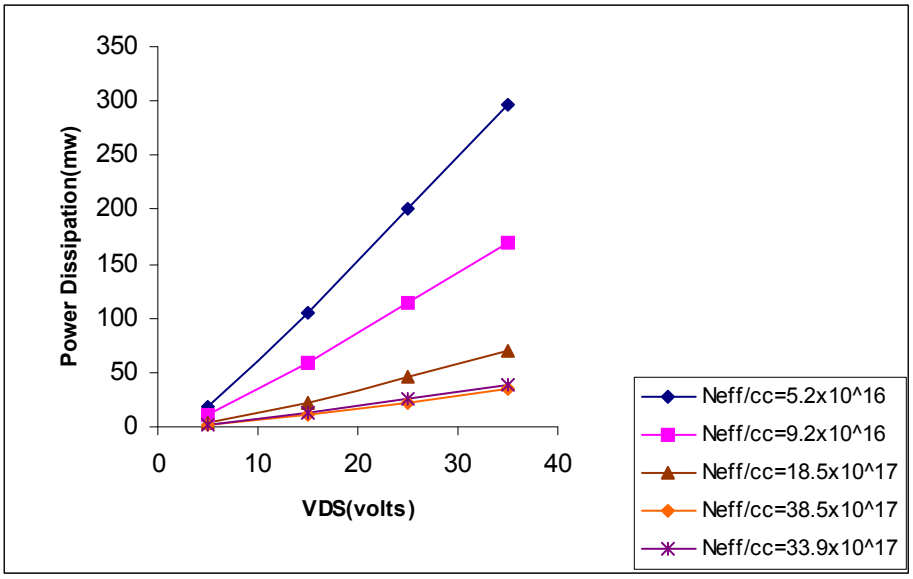

Fig 4.13 :Plot of Power Dissipation(w) at different values of Doping for different V_{DS}(volts) levels of Gaussian Distribution.

Table 4.14 : Values of Power Dissipation(mw) at different values of Breakdown voltages(volts) for different Doping levels(N_B) of UniformDistribution.

$N_{B=10^{15}/cc}$	$N_{B=10^{15}/cc}$	$N_{B=10^{16}/cc}$	$N_{B=10^{16}/cc}$	$N_{B=10^{17}/cc}$	$N_{B=10^{17}/cc}$
$V_{B(Volts)}$	P_D(w)	$V_{B(Volts)}$	P_D(w)	$V_{B(Volts))}$	P_D(w)
208.5	0.92	89.09	0.097	38.11	0.0064
294.92	2.62	125.99	0.29	53.9	0.021
361.21	4.45	154.29	0.51	66.01	0.04

417.09	6.29	178.17	0.76	76.23	0.061
466.32	7.98	199.21	0.99	85.23	0.083
510.82	9.57	218.22	1.22	93.36	0.1
551.76	10.95	235.71	1.45	100.84	0.12
589.86	12.27	251.97	1.66	107.8	0.15

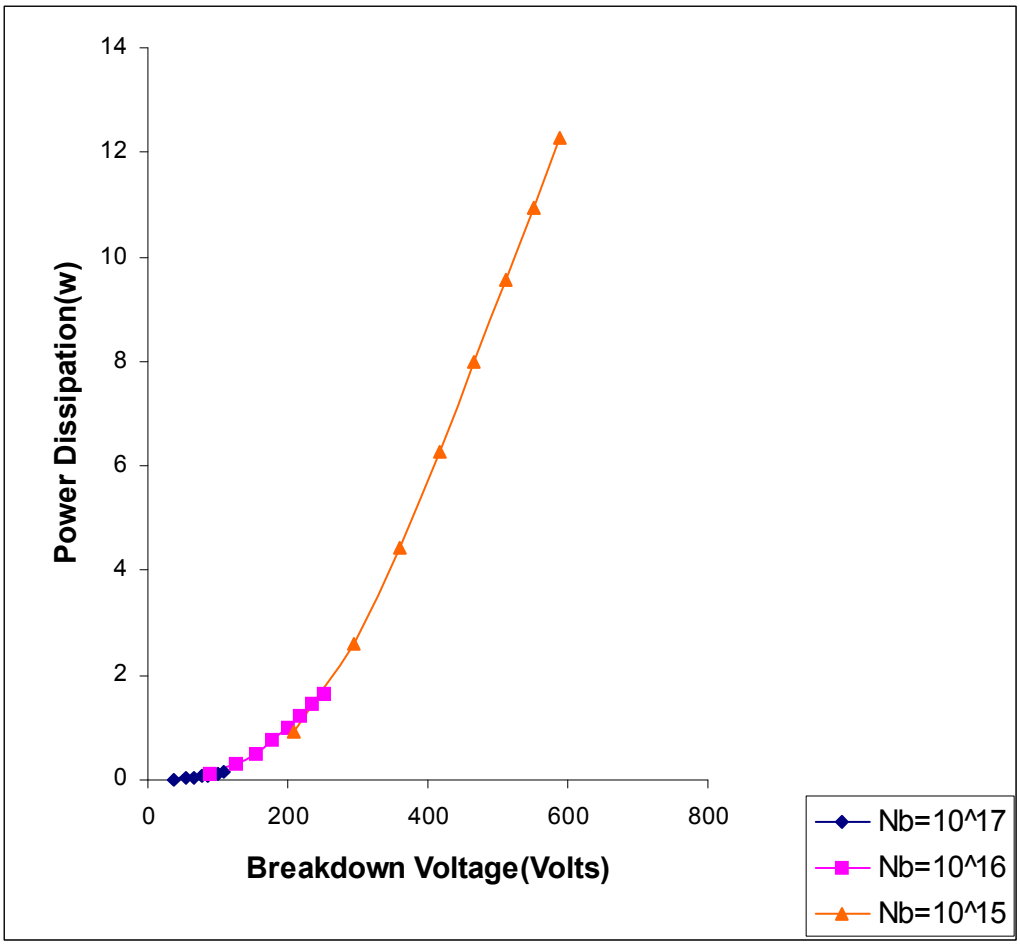

Fig 4.14 : Plot of Power Dissipation(w) at different values of Breakdown voltages(volts) for different Doping levels(N_B) of Uniform Distribution.

Table 4.15 : Values of Power Dissipation at different values of Breakdown Voltages for different N_{eff} Doping levels of Gaussian Distribution.

$N_{B=5.2x10^{16}/CC}$		$N_{B=9.2x10^{16}/CC}$		$N_{B=18.5x10^{17}/CC}$		$N_{B=38.5x10^{17}/CC}$		$N_{B=33.9x10^{17}/CC}$	
V_B (Volts)	P_D (mw)	V_B (Volts)	P_D (mw)	V_B (Volts)	P_D (mw)	V_B (Volts)	P_D (mw)	V_B (Volts)	P_D (mw)
48.48	19.13	39.63	3.19	30.32	3.48	23.04	1.67	24.31	1.9
68.57	57.99	56.05	10.55	42.88	11.47	32.58	5.53	34.38	6.28
83.98	104.81	68.64	20.16	52.52	21.85	39.89	10.55	42.09	11.98
96.97	152.89	79.26	30.98	60.64	33.48	46.07	16.15	48.62	18.21
108.42	201.44	88.62	42.42	67.8	45.75	51.51	22.06	54.36	25.11
118.77	249.56	97.06	54.13	74.27	58.27	56.43	28.2	59.55	32.01
128.28	296.66	104.85	65.87	80.22	70.76	60.95	34.3	64.33	38.87
137.14	342.71	112.1	77.51	85.77	83.11	65.17	40.31	68.76	45.72

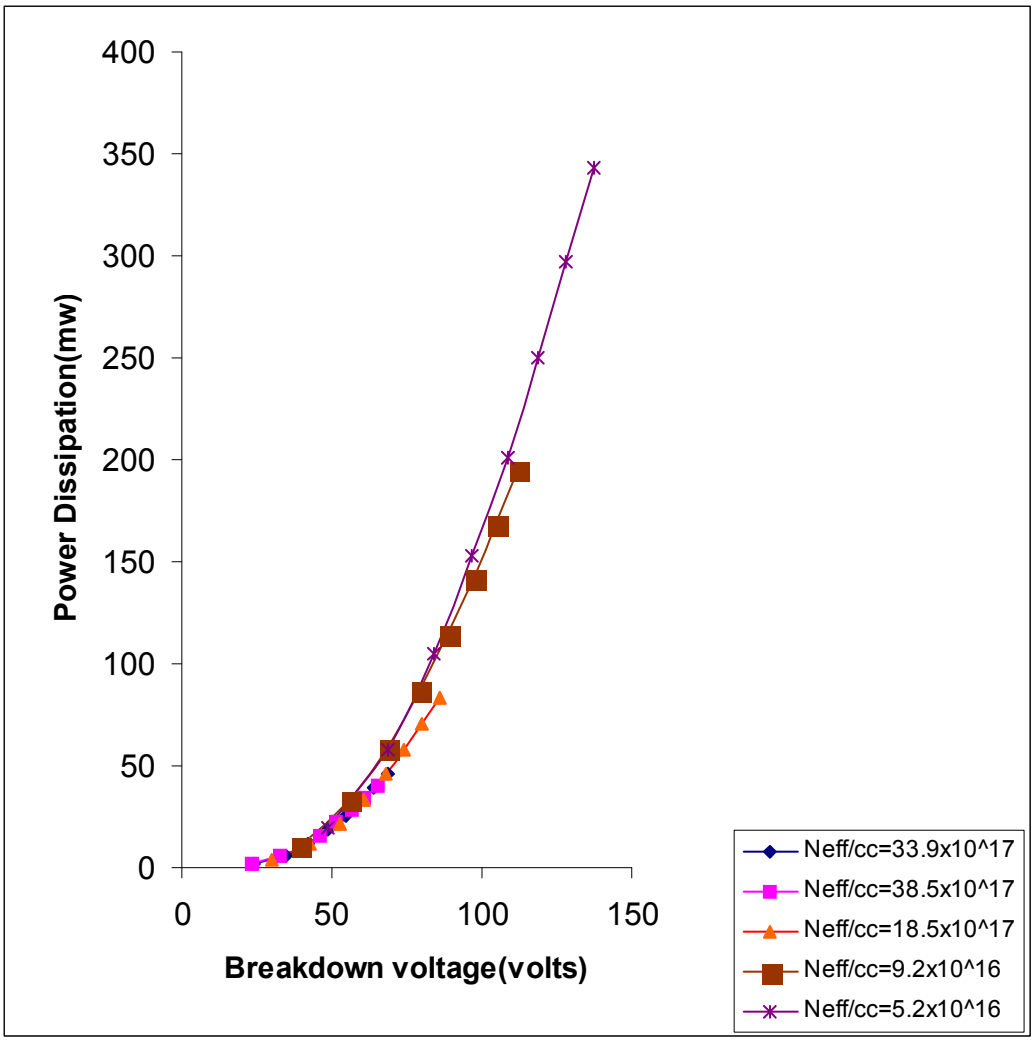

Fig 4.15 : Plot of Power Dissipation at different values of Breakdown Voltages for different N_{eff} levels (N_{eff}) of Gaussian Distribution

CHAPTER V

Conclusion and Future Work

The present analysis of the 6H-SiC DIMOSFET in the linear region shows that the Gaussian profile in the drift region obtained from experimental values is easier to generate with a relatively high peak doping levels and moderortely high effective doping concentrations. The Gaussian profiles gives for given value of N_{eff}, a somewhat higher breakdown voltage but a much less power dissipation than those for Uniform doping. This can be verified from Tables 4.14 and 4.15 for a doping level of 10^{17}/cc and $9.2x10^{16} \approx 10^{17}$./cc for uniform doping and Gaussian profile. The former gives a V_B of 107.8 as against 112.1 V for the Gaussian whereas correspondind P_D is 150 mw for the Uniform doping as against 77.51mw for the Gaussian profile. Hence 6H-SiC DIMOSFET having a Gaussian profile in the drift region yield better devices with lower power dissipation and higher voltages.

The other profiles that may be considered could be an exponential or an error function profile for doping the drift region and an analysis for the power dissipation of the device can be made. The results could then be compared with those obtained in this work for uniform ang Gaussian doping profiles. It is possible that one of these two ,i.e. exponential or error function profiles may yield better values for the device breakdown voltage and power dissipation. This work could also be extended to cover the saturation region of the DIMOSFET.

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