High Frequency Low Voltage CMOS Current Feedback Operational Amplifier based Analog Building Blocks

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in

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DECLARATION

I hereby declare that the work which is presented in the dissertation entitled, **"High Frequency Low Voltage CMOS Current Feedback Operational Amplifier based Analog Building Blocks"** in partial fulfilment of the requirement for the award of degree of Master of Technology in VLSI Design submitted in Electronics and Communication Engineering Department of Thapar University, Patiala, is an authentic record of my own work carried out under the supervision of Dr. Rishikesh Pandey, Assistant Professor, ECED and refers other researcher's work which are duly listed in the reference section.

The matter presented in this dissertation has not been submitted in any other University/Institute for the award of degree.

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ABSTRACT

Analog integrated circuit design has reached to an advanced stage of circuit pattern by mixing of analog and digital functions on single chip. Merging both the functions on the same chip has led to the higher component densities along with the need of smaller device geometries, which in turn require low-voltage and low power operation of the devices. Traditionally analog circuits dominated by the voltage-mode circuits get severely affected by the reduction in power supply voltages. In current mode circuits, the signals are represented by flowing of the currents in branches so the performance of the current-mode circuits are less affected when power supply is reduced as compared to their counterparts. An important building block of current-mode circuit is current feedback operational amplifier.

In this dissertation, high frequency low voltage CMOS current feedback operational amplifier (HFLVCFOA) and positive second generation current conveyor (CCII+) circuits are proposed. The CFOA is developed by cascading of the proposed CCII+ and a voltage buffer circuit. Analog building blocks like notch filter, frequency dependent negative resistor (FDNR) and inductor circuits are developed as the applications of the proposed CFOA. The proposed circuits are simulated in UMC 0.18µm CMOS process technology parameters. The layout of the proposed CFOA is designed using Cadence Virtuoso XL layout editor. The performance parameters of proposed CFOA and CCII has also been compared with the existing circuits available in the literature and the comparison shows that proposed CFOA has high gain bandwidth product and proposed CCII has wide input current linearity.

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LIST OF SYMBOLS

g_m	Transconductance
I	Current
V	Voltage
R	Resistance
C	Capacitor
W	Channel Width
L	Channel Length
μ	Mobility of Carriers
C_{OX}	Oxide Capacitance
β	Transconductance Parameter.
V_{th}	Threshold Voltage
r_o	Output Resistance of MOSFET

ABBRIVEATIONS

MOSFET	Metal Oxide Semiconductor Field Effect Transistor
CMOS	Complementary Metal Oxide Semiconductor
CFOA	Current Feedback Operational Amplifier
VFOA	Voltage Feedback Operational Amplifier
CCII+	Positive Second Generation Current Conveyor
FDNR	Frequency Dependent Negative Resistor
UMC	United Microelectronics Corporation
OTA	Operational Transconductance Amplifier
VCVS	Voltage Controlled Voltage Source
THD	Total Harmonic Distortion
dB	Decibel
GBW	Gain Bandwidth
PM	Phase Margin
DRC	Design Rule Check
LVS	Layout vs Schematic

CHAPTER

1

INTRODUCTION

1.1 Introduction

With growing opportunities, analog integrated circuit design is becoming more and more significant. Interfacing of the digital circuits with the real world applications like analog signal processing, biomedical measurements, industrial process is invariably handled out by the analog systems. Mixing of analog and digital functions on a single chip has led to an advanced stage of integrated circuit pattern. Incorporating both the functions on the same chip along with the demand for the smaller device geometry has led to higher component densities. Decreasing the size of transistors in integrated circuit technology and increase in the portable devices has led to the rise in the demand for low-power and low-voltage circuits and systems. But, by reducing the supply voltages and decreasing the transistor size enforce serious issues with the designing of analog devices [1].

Traditionally, analog systems are dominated by the voltage-mode approaches, in which all the current signals are also transferred into voltage domain. The performance of voltage-mode circuits gets severely affected by the reduction in power supply voltages and threshold voltages [1].

Voltage-mode operational amplifier suffers from the limited bandwidth at high closed loop gain because of its constant gain-bandwidth product. Complexity in the design of the voltage-mode operational amplifier increases and the required performance characteristics are also not obtained, when low power consumption, low supply voltage and high bandwidth are required simultaneously. So, analog techniques to overcome the shortcomings of the voltage-mode operational amplifier design are needed [2].

Since, in current-mode circuits, main attention is on the branch currents rather than the voltages at specific nodes, so the performance of the current-mode circuits are less affected when power supply is reduced as compared to their counterparts. CMOS current-mode circuits are receiving attention from the industry because of its high operational speed and capability of overcoming the shortcomings due to the supply voltages reduction [3]. An important current mode circuit is the current feedback operational amplifier (CFOA) which has inherent advantage over the traditional voltage operational amplifier of having constant bandwidth with respect to closed loop gain. Current conveyor (CC), the input stage of the

CFOA is an important building block of current-mode circuits as it has unity gain, high linearity and better frequency performance. CC is a three terminal device, when connected with the other circuits externally can perform many analog signal processing purposes. Current conveyor is characterized by one voltage buffer block and one current buffer block. The conveyor is described by a transcendent frequency response for the voltage transfer function between the two terminals Y and X when dealing with the voltage follower. Conveyor also shows higher current transfer function between the two current terminals X and Z as the current buffer [4].

1.2 Motivation

Ideal voltage-mode circuits are characterized by infinite input impedance, zero output impedance and constant voltage gain. Ideal operational amplifier is considered as the appropriate example of the ideal voltage-mode circuits. Cascading of voltage-mode operational amplifiers can be achieved very easily without the loading effect due to its infinite input impedance and zero output impedance. Gain of the voltage-mode circuit falls at high frequencies. Unlike their counterparts, current-mode circuits are characterized by zero input impedance and infinite output impedance and constant current gain. Current gain is set to unity in ideal current-mode circuits so that the static power consumption does not increase by the current amplification. Due to constant current gain up to high frequencies, current-mode circuits are used in variety of high frequency applications [3].

For high performance analog circuit design, along with the simpler circuit realization, it is preferable to process the signals in the current domain rather than in voltage domain. For processing of signals to take place in current form, MOS transistors are preferred because for common-source and common-gate configuration the output is in the form of current. Bipolar current mirror are prone to the process variation and inaccuracy when compared with MOS current mirrors. Therefore, current-mode integrated circuit design is easier to realize using MOS transistors than the conventional voltage-mode integrated circuit design [5].

Limitations of voltage-mode circuits of constant gain-bandwidth product and tradeoff between speed and bandwidth is surmounted with the help of current-mode circuits.

In voltage-mode, the parasitic capacitances are charged and discharged, due to which speed of the operation is decreased and power consumption is increased. But, in current-mode circuits, charging and discharging of the local nodes cannot be avoided due to which their parasitic capacitances are less and therefore it is possible to achieve higher speed of operation and lower dynamic power consumption [5].

1.3 Key Contributions

The work in this dissertation can be summarized as follows:

1. Design and simulate two positive second generation current conveyors (CCII+).
2. Design and simulate differentiator, integrator and transconductance amplifier as applications of the proposed CCII+.
3. Design and simulate two current feedback operational amplifiers (CFOA) using the proposed CCII+ as the input stage.

4. Design and simulate notch filter, ideal inductor and frequency dependent negative resistor (FDNR) as applications of the proposed CFOA.

In the dissertation, two CMOS second generation positive current conveyor circuits are proposed namely MOSFET-resistor voltage divider biased CCII+ (MRCCII+) and MOSFET-only voltage divider biased CCII+ (MOCCII+). These proposed CCII+ circuits are used as the input stage to develop current feedback operational amplifier circuits namely high frequency low voltage current feedback operational amplifier based on MRCCII+ (HFLVCFOA-MR) and high frequency low voltage current feedback operational amplifier based on MOCCII+ (HFLVCFOA-MO). The applications of proposed MOCCII+ such as integrator, differentiator and transconductance amplifiers and the applications of proposed HFLVCFOA-MO such as notch filter, ideal inductor and frequency dependent negative resistor (FDNR) are also proposed. All the proposed circuits have been simulated using UMC 0.18μm CMOS process technology parameters and their simulation results are presented. The performance parameters of proposed MOCCII+ and HFLVCFOA-MO are also compared with the existing current conveyor circuits and current feedback operational amplifier circuits, respectively available in literature.

1.4 Organization of dissertation:

The summary of each chapter is discussed in this section. A brief overview of the current feedback operational amplifier circuits and current conveyor circuits along with their applications is given in second chapter. Different topologies suggested by various authors to design current conveyors and current feedback operational amplifiers have been discussed and compared in the third chapter. In the fourth chapter, two CMOS second generation positive current conveyor circuits namely MOSFET-resistor voltage divider biased CCII+ (MRCCII+) and MOSFET-only voltage divider biased CCII+ (MOCCII+) and two current feedback operational amplifies namely high frequency low voltage current feedback operational amplifier based on MRCCII+ (HFLVCFOA-MR) and high frequency low voltage current feedback operational amplifier based on MOCCII+ (HFLVCFOA-MO) are proposed. The applications of proposed MOCCII+ such as differentiator, integrator, and transconductace amplifier and the applications of proposed HFLVCFOA-MO such as notch filter, inductor and frequency dependent negative resistor (FDNR) are also proposed in this chapter. The simulation results of the proposed CCII+ and CFOA circuits and their applications are presented in the fifth chapter. Layout design of the proposed CFOA is also presented in fifth chapter. Summary of the dissertation and future scope for the work is suggested in the sixth chapter.

CHAPTER

2

CURRENT FEEDBACK OPERATIONAL AMPLIFIER

2.1 Introduction

Current feedback operational amplifier (CFOA) is a versatile building block for analog signal processing applications having high slew rate and gain independent bandwidth. Various topologies for developing CFOA include cascading of a positive second generation current conveyor and a voltage buffer stage [6], cascading two blocks of current conveyors [7] and current feedback amplifier (CFB) operational transconductance amplifier (OTA) stage followed by a cross coupled buffer stage [8]. The chapter is organized as follows. In Section 2.2, the theory of Adjoint networks is addressed. Section 2.3 gives the overview of the current feedback operational amplifier. Applications of current feedback operational amplifier are listed in section 2.4. The conclusions are drawn in section 2.5.

2.2 Theory of Adjoint Networks

A circuit containing voltage amplifiers and passive components is converted into circuits which contains current amplifiers and passive components. Like, an ideal voltage-mode circuit has infinite resistance and zero output resistance, whereas an ideal current- mode circuit has zero input impedance and infinite output impedance, so by substituting the voltage amplifiers by current amplifier will result into a different behavior. In order to design current-mode circuits it is beneficial to use the Theory of Adjoint Network [9]. The network N and N_a with the same transfer functions are shown in Figure 2.1(a) and 2.1(b) respectively.

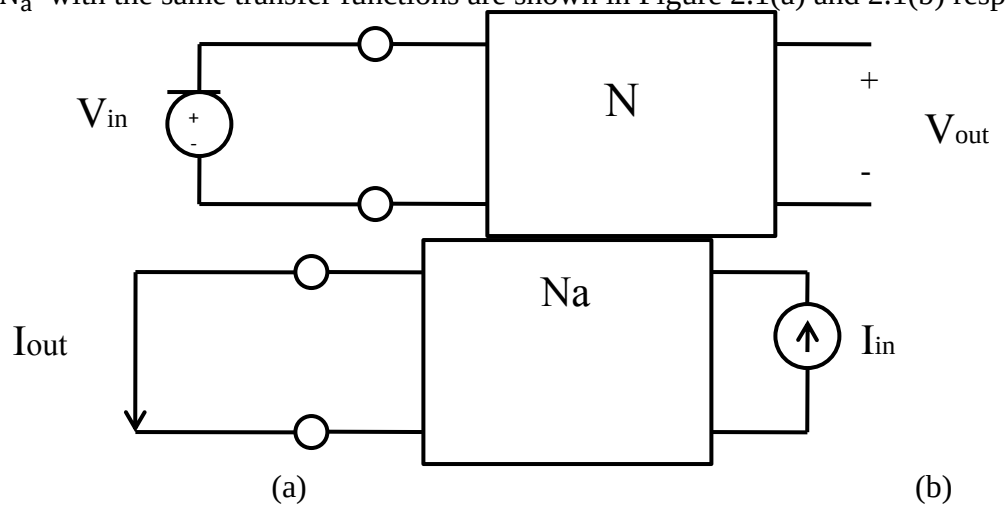

Figure 2.1(a): Network N. (b) Network N_a [9].

The adjoint network of N is considered as N_a and it can be obtained by interchanging the excitation and response of network N and thereby network N is replaced by network N_a. So, the same transfer function is obtained where N and N_a are said to be the inter-reciprocal of each other (A network is known as reciprocal if same transfer function is obtained by interchanging the excitation and response). The input voltage source of network N is short circuited and current passing through it becomes the output response of Network N_a. Similarly, the output voltage in the network N is replaced by a current excitation in Network N_a, which gives the same transfer function as

$$\frac{V_{out}}{V_{in}} = \frac{I_{out}}{I_{in}} \tag{2.1}$$

where,

V_{in} = Input voltage for network N,

V_{out}= Output voltage for network N,

I_{out} = Current response for network N_a,

I_{in} = Current excitation for network N_a.

From equation 2.1, it can be seen that transfer functions are same.

2.3 Current Feedback Operational Amplifier

The current feedback operational amplifier (CFOA) is a basic building block which can perform functions of both current-mode and voltage-mode circuits. Unlike, conventional voltage feedback operational amplifier (VFOA), CFOA is an amplifier whose inverting input is sensitive to currents rather than the voltage.

Current feedback operational amplifier is implemented by cascading second generation current conveyor (CCII+) and a voltage buffer at the output terminal of the current conveyor as shown in Figure 2.2 [6].

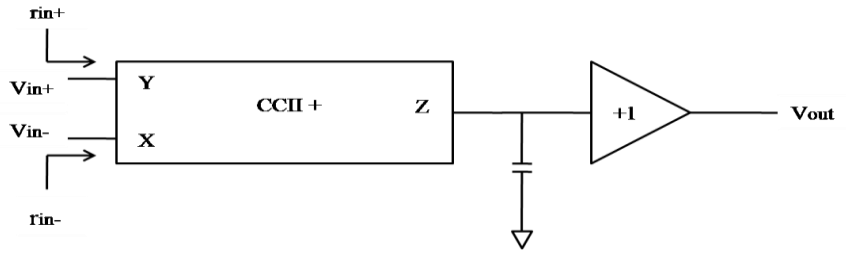

Figure 2.2: CFOA implemented using second generation current conveyor and voltage buffer [6]

Another topology for developing current feedback operational amplifier includes cascading of two blocks of current conveyor [7] as shown in Figure 2.3.

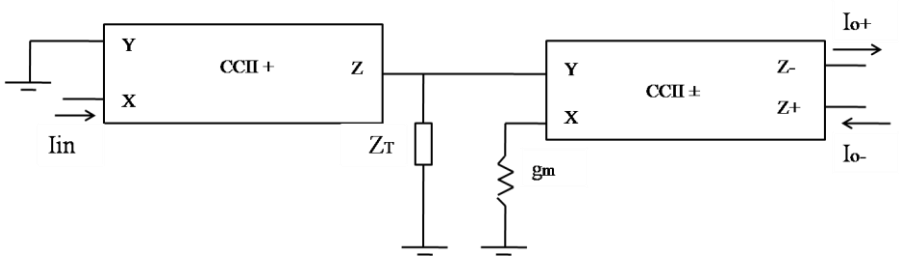

Figure 2.3 CFOA implemented using two current conveyors [7]

Current feedback operational amplifier is also developed using current feedback amplifier (CFB) operational transconductance amplifier (OTA) stage followed by a cross coupled buffer stage [8] as shown if Figure 2.4.

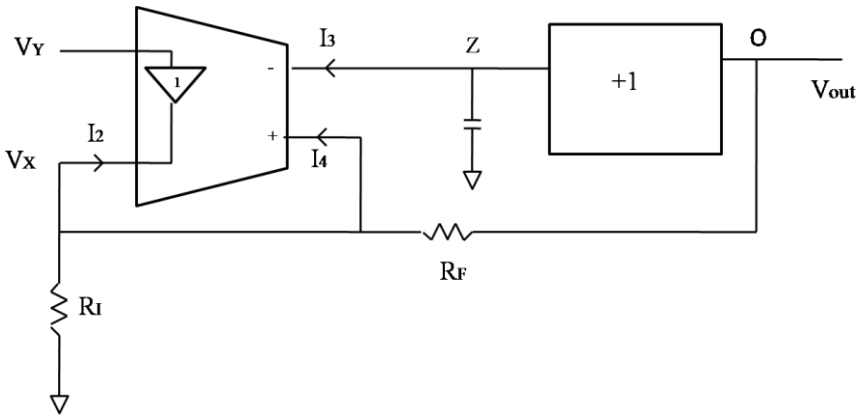

Figure 2.4 CFOA implemented using OTA and cross coupled buffer [8]

CFOA doesn't have the proper matched parameters because of the absence of traditional differential amplifier input structure and thus precision equivalent to VFOA is not obtained. Factors due to which precision is decreased results in higher bandwidth and increased slew rate. Higher bandwidth in CFOA is independent of closed loop gain, which is not the case in VFOA. High slew rate is possible in CFOA because their structure enables the output stage to supply slewing current until the output reaches its final value. Therefore VFA are used in high precision applications whereas, CFA's are used for high frequency applications [10].

The CFOA is a four terminal device as shown in Figure 2.5. The input and output terminals are represented by X, Y and O, Z, respectively.

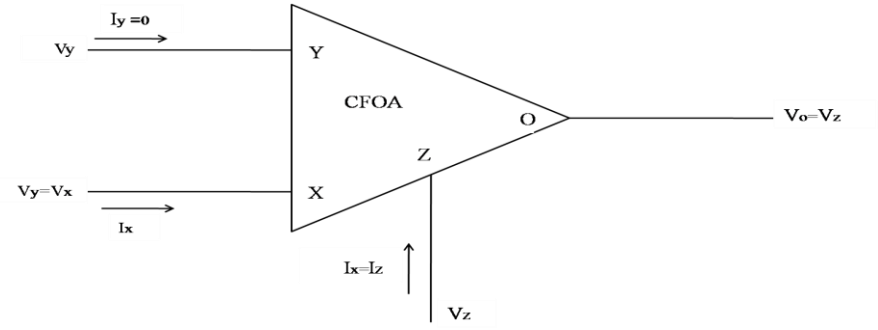

Figure 2.5: Current Feedback Operational Amplifier (CFOA) [11]

The behavior of CFOA is described by the following matrix [12]:

$$\begin{bmatrix} I_Y \\ V_X \\ I_Z \\ V_O \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 & 0 \\ 1 & 0 & 0 & 0 \\ 0 & 1 & 0 & 0 \\ 0 & 0 & 1 & 0 \end{bmatrix} \begin{bmatrix} V_Y \\ I_X \\ V_Z \\ I_O \end{bmatrix} \quad (2.2)$$

According to the Figure 2.5 and matrix, the potential V_Y applied at the terminal Y is transferred to the terminal X, which is denoted by V_X. Also, same current I_Z is obtained at compensating terminal Z when a current source I_X is applied at the terminal X. The output voltage V_O obtained at terminal O is equivalent to the potential V_Z applied at compensating terminal Z. In order to achieve ideal characteristics, the impedance level at terminal Y should be infinite as it is the input terminal for the voltage buffer. Impedance level at terminal X should be zero ideally, as it is the output terminal for the voltage buffer and input terminal for the current buffer. Similarly, the impedance level of compensating terminal Z should be infinite as it is the input excitation for the second voltage buffer present between terminals Z and O and output terminal for the current buffer present between terminals X and Z. In a CFOA, both voltage buffering action and current mirroring action is performed. Terminal Y is considered as non-inverting terminal and terminal X is considered as inverting terminal for the amplifier.

The internal model of current feedback operational amplifier [10] is shown in Figure 2.6. Non-inverting terminal of the CFOA acts as an input terminal for the input buffer therefore the terminal is having a very high impedance. Inverting terminal of CFOA is connected to the output of the input buffer, so its input impedance is equal to the buffer output impedance and is having low value of impedance.

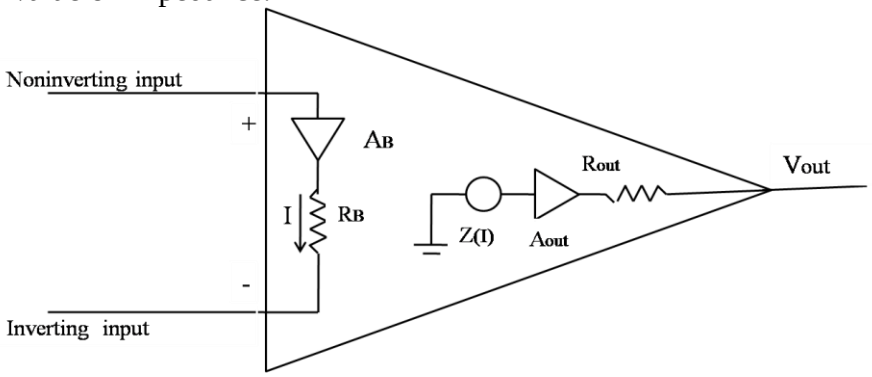

Figure 2.6: Current Feedback Operational Amplifier (CFOA) model [10]

R_B is modeled as the output impedance of the input buffer. A_B is modeled as the input buffer gain, which is close to unity. R_{out} is the output buffer for the amplifier and A_{out} is the output buffer gain, which is also close to unity. At higher frequencies, stability of the amplifier is affected by the output impedance of the input buffer. The value of the trans-impedance is normally very high so that the CFOA can achieve more accuracy with the help of closed feedback loop [10].

2.3.1 Second Generation CMOS Current Conveyors

Current conveyors have been considered as very useful building blocks in the design of analog circuits since, its introduction by Smith and Sedra in 1968 [13]. They have high bandwidth, simpler structure and they can be operated at lower supply voltages. The block

diagram of current conveyor [14] shown in Figure 2.7, in which the potential V_y applied at the terminal Y, is transferred to the terminal X. The potential at terminal X is denoted by V_x. Also, when a current I_X is applied at the terminal X, the obtained current I_z at terminal Z is same as I_X.

Current Conveyor is a three terminal device having terminals named as Y, X and Z.

- X is used as the input terminal for the current conveying operation and the output terminal for voltage transferring operation.
- Y is used as input terminal in case of voltage transferring operation and is connected to ground while the current conveying operation is performed between the terminals X and Z.
- Z is the output terminal for the current conveying operation. The direction of the current at this terminal defines the operation of the current conveyor as positive or negative.

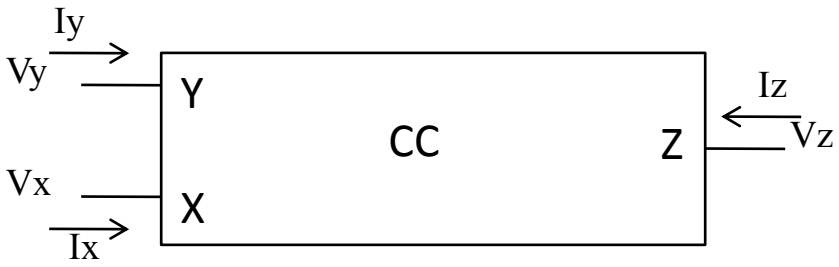

Figure 2.7 Block Diagram of Current Conveyor [14]

The Current conveyors are categorized into three generations namely First generation current conveyor (CCI), second generation current conveyor (CCII) and third generation current conveyor (CCIII). These three generations of current conveyors can be explained with the help of matrix [15]:

$$\begin{bmatrix} V_X \\ I_Y \\ I_Z \end{bmatrix} = \begin{bmatrix} 0 & 1 & 0 \\ m & 0 & 0 \\ K & 0 & 0 \end{bmatrix} \begin{bmatrix} I_X \\ V_Y \\ V_Z \end{bmatrix} \quad (2.3)$$

where, m = 1 for 1st generation of current conveyors, m = 0 for 2nd generation of current conveyors, and m = -1 for 3rd generation of current conveyors, K = 1 for positive current conveyors (CC+) and K= -1 for negative current conveyors (CC-) [15].

First generation current conveyor (CCI±) was introduced by Smith and Sedra [13] in 1968 as the first basic current mode block shown in Figure 2.8 (a). The current and the voltage at terminals X and Y, becomes equal, so for accurate current and voltage conveying the impedance level at terminal Y should be low, ideally zero [13].

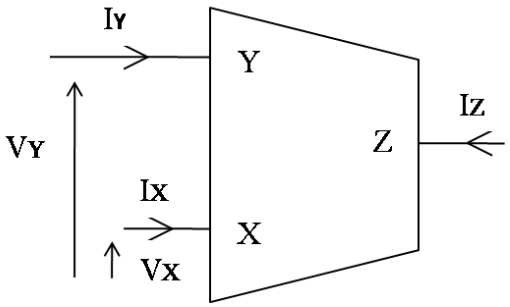

Figure 2.8(a) First Generation Current Conveyor [4]

Sedra and Smith developed another current mode block shown in Figure 2.8 (b) in 1970 known as second generation current conveyors (CCII±) [16]. Ideally in CCII±, no current flows through the Y terminal. Therefore, the impedance level at the Y terminal is infinite.

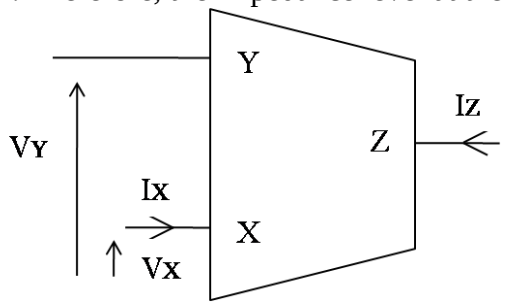

Figure 2.8(b) Second Generation Current Conveyor [4]

A. Fabre introduced third generation current conveyor (CCIII±) [17] shown in Figure 2.8 (c) in 1995. In CCIII the current in terminal X and Y are equal and flow in the opposite directions, that is $I_Y = - I_X$.

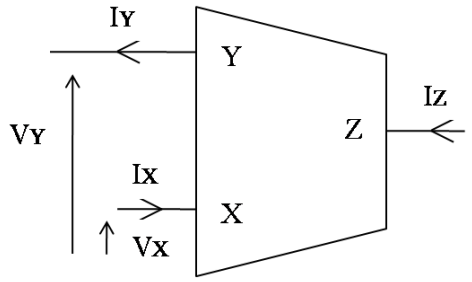

Figure 2.8(c) Third Generation Current Conveyor [4]

Generally, voltage buffers are characterized by high impedance level at the input for accurate voltage transferring and since, the input stage of CFOA is a voltage buffer they are developed using only second generation of current conveyors as their input stage.

2.3.2 Voltage Buffer

Prime function of a voltage buffer is to transfer voltage from a high-impedance source to a low-impedance load without attenuation or distortion of the signal. In an ideal voltage buffer the input impedance is infinite and output impedance is zero. Voltage buffers are developed using high-gain operational amplifier in negative feedback as shown in Figure 2.9[18].

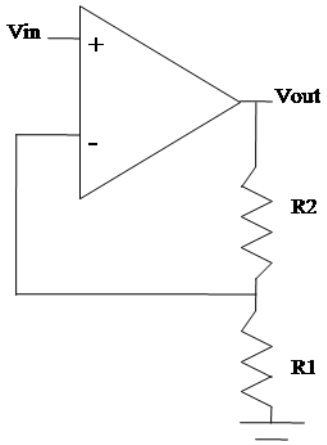

Figure 2.9 Op-amp buffer configuration [18]

Voltage buffer is the output stage of the current feedback operation amplifier and it transfers the voltage from the high input impedance terminal to the low input impedance terminal. To achieve high input impedance, voltage buffers are developed generally using differential amplifier, common drain configuration and flipped voltage follower [19].

2.4 Applications of Current Feedback Operational Amplifier

CFOAs are used as essential building blocks due to the presence of compensating terminal (Z) to develop various analog signal processing applications such as voltage controlled voltage sources (VCVS), grounded inductors, frequency dependent negative resistors, filters, oscillators, triangular-square wave generators, multipliers, etc [20-26].

2.5 Conclusions

In this chapter, the brief idea of the current feedback operational amplifiers (CFOA) has been discussed. The overview of current conveyors and the second generation current conveyor due to its high input impedance is used as basic building block of CFOA is addressed. Another building block of CFOA as voltage buffers is also discussed.

CHAPTER

3

LITERATURE REVIEW

3.1 Introduction

Current conveyors and current feedback operational amplifiers are considered as the basic building blocks for analog signal processing applications. The circuit parameters like input impedance, voltage and current bandwidths, power consumption, total harmonic distortion etc. are used to demonstrate the effectiveness of these circuits. The chapter is organized as follows. Section 3.2 discusses the various topologies of current conveyors available in the literature. The different topologies used to develop current feedback operational amplifier suggested by researchers are discussed in section 3.3. The chapter is concluded in section 3.4.

3.2 Current conveyors

Several authors have suggested different topologies to develop current conveyors [27-36]. H.O. Elwan *et al.* [27] proposed low voltage low power CMOS current conveyors. The

circuits use two differential pairs as their input stage to provide rail to rail swing capability. The first proposed current conveyor operates in class-A mode, which draws large standby currents and dissipates large power. To reduce the power dissipation and standby currents, second current conveyor was proposed which operates in class-AB mode. The limitations are overcome by class-AB mode current conveyor at the expense of dual power supply in comparison with the single power supply used by class-A mode current conveyor. CMOS realization of the negative second generation current conveyor (CCII-) has been suggested in [28]. The input stage of circuit is formed using simple differential transistors whereas output stage is formed by floating current source. The suggested circuit provides very low input impedance level along with wide dynamic voltage range. The circuit has low current tracking error ability. B. Calvo *et al.* [29] suggested a high speed high precision CMOS current conveyor. The circuit is based on high performance voltage follower topology consisting of cascaded complementary source followers and complementary level shifters. The circuit has low input impedance, high precision in voltage and current transference. The circuit operates at low supply voltage but it imposes several limitations on the voltage output range. The voltage-to-current convertor and current feedback operational amplifier using the same circuit of current conveyor have also been suggested. A wide band low power CMOS current conveyor has been proposed in [30]. The voltage follower section is developed by cascading of two flipped voltage followers, which removes the large offset voltages. Current following stage is developed using push-pull and levels shifting transistors. The current conveyor has low input impedance, precise voltage tracking ability and precise current tracking ability. W. S. Hassanein *et al.* [31] suggested a current conveyor based on long tail pair transistors. The circuit has low input impedance and high accuracy in voltage tracking with the help of adaptive voltage offset cancellation methodology. In order to achieve high gain, the bandwidth of the circuit is reduced. S. B. Salem *et al.* [32] suggested a high performance CMOS CCII configuration based on improved trans-linear circuit. Heuristic algorithm was used to find the optimum sizing of the transistors. The current conveying path in the circuit is separated from the signal conveying path by making a different path for the current transfers because of that the input impedance is decreased. Applications like current controlled oscillator, high frequency tunable band pass filter were developed using suggested CCII. H. Barthélemy *et al.* [33] proposed CMOS inverters based positive type second generation current conveyor. CMOS inverters used to develop current conveyor operates in transconductance mode when a common mode voltage is connected at the output. At this common mode voltage, the inverter is simulated as a transconductor between the input voltage and the output current. The circuit operates at low supply voltage and exhibits large voltage and current swings. A wideband self-biased CMOS CCII has been suggested in [34]. CCII based on long tail n-type and p-type differential pair achieves rail to rail voltage swing. The circuit does not use any additional biasing of voltage or current sources except the power supply. As an application of the suggested current conveyor, a wide band high output impedance current mode band-pass filter is developed. F. Kacar *et al.* [35] proposed a CMOS dual-X second generation current conveyor (DXCCII) and a frequency dependent negative resistor (FDNR) as its application. The DXCCII is implemented by standard CCII and the inverting current conveyor. Output impedance of the circuit is increased by using as improved active-feedback cascade current mirror. The DXCCII provides good linearity, high output impedance and excellent input-output current gain accuracy. The current mode fifth-order elliptic filter and a tunable frequency dependent negative resistance (FDNR) circuit based on

DXCCII are also suggested. Low-voltage low-power multifunction current controlled conveyor (MFCCCII) has been suggested in [36]. Differential pairs are used to design the MFCCCII. The circuit operates as CCCII± with both positive and negative intrinsic resistance. A grounded inductance and current mode band pass filter are developed as the applications of the circuit. The current conveyors developed using different topologies discussed above are compared and listed in Table 3.1.

Table 3.1 Parameters comparison of various current conveyors

Parameters	[28]	[30]	[33]	[35]	[36]
Supply Voltage (V)	±3.3	±1.5	2.5	±1.5	±0.5
Technology (µm)	1.2	0.5	0.35	0.35	0.18
Bias Current (µA)	100	100	40	N.A	N.A
Power Consumption (mW)	N.A	1.5	N.A	N.A	0.0048
Input voltage range (V)	-3 to 2	-0.63 to 0.25	0.8 to1.6	-0.5 to 0.6	±0.150
Voltage offset variation (V)	0.09 to 0.27	−0. 0058 to 0.00254	N.A	N.A	N.A
3-dB B/W (MHz) (V_X/V_Y)	222	1150	103	1050	70
Voltage Gain	1	0.99385	0.972	0.95	0.989
Input Current range (µA)	±100	±100	0 to 200	-100 to 125	±40
Current Offset variation (µA)	-0.3 to 0.2	−1.04 to −0.023	N.A	N.A	N.A
3-dB B/W (MHz) (I_Z/I_X)	110	76	200	10350	130
Current Gain	1.0015	1.0037	0.986	0.98	0.985
Rx(Ω)	0.003	5.9	4500	N.A	3.8K Ω to 1.4MΩ
Voltage THD (%) @V@ MHz	N.A	0.0919@ 0.5 Vp-p@ 100Khz	0.091% @ 100mV p-p	N.A	0.94% @ 0.2V
Current THD (%) @I@ MHz	N.A	N.A	0.066% @100µA p-p	N.A	N.A

From the Table, the voltage transfer bandwidth of current conveyor suggested in [30] is higher than that of other conveyors suggested in [28, 33, 35, 36]. The current conveyor suggested in [28] has low input impedance as compared to other current conveyors suggested in [30, 33, 35, 36].

3.3 Current Feedback Operational Amplifiers

A.M. Ismail *et al*. [37] proposed CMOS current feedback operational amplifier for high frequency applications. The input voltage buffer of the circuit uses two long tail structures. The circuit does not use PMOS current mirrors since the PMOS current mirrors gate and drain capacitances usually have a major role in bandwidth degradation. The circuit has low input impedance, wide bandwidth and accurate voltage following action. Also second order notch filter is developed using the suggested CFOA. The major disadvantage of this topology is that it requires several precise current sources. B. Maundy *et al*. [38] suggested a current feedback

operational amplifier. The gain of the circuit is adjusted over positive and negative values by changing the value of grounded resistor. The input current limitations and buffer input resistance affects the overall performance of the circuit. An offset-compensated wide-bandwidth CMOS current feedback operational amplifier has been proposed in [39]. The compensation technique consists of voltage averaging circuits, two voltage substractors and a pseudo negative input. The circuit reduces the input offset voltage arising due to the mismatching between transistors threshold voltages. Circuit is characterized by high bandwidth and low power dissipation, but all these improved parameters are obtained on the expense of reduced gain and increased total harmonic distortion (THD). R. Mita *et al.* [40] suggested a low-voltage high drive CMOS current feedback operational amplifier. The circuit is developed by cascading of two current conveyors (CCII). The input voltage follower stage of CCII is developed using transconductance amplifier which is developed using two complementary differential amplifiers and an inverting transconductance class AB output stage. The circuit operates at low supply voltages and provides a wide input and output swing in addition to high current drive capability. The main drawback of the circuit is poor slew rate. This is because of class-A operation of the input differential stage which charges or discharges the compensation capacitor with constant current. S. Pennisi [41] proposed a high performance CMOS current feedback operational amplifier. The circuit is developed using two voltage buffers. These buffers are realized by class-AB differential stage. The circuit exhibits high slew rate and low input impedance. Low voltage CMOS current feedback operational amplifier and its application have been proposed in [42]. The circuit is realized by cascading the voltage buffer at the output of the CCII. The input voltage buffer stage of CCII is developed using two matched parallel connected differential pairs, two matched biasing current source transistors, a cascoded current mirror and two pairs of matched source follower transistors. The circuit has rail-to-rail input/output operations along with high driving current capability. A second order all-pass filter is implemented using the suggested CFOA. A drawback of the proposed topology is that it does not provide a constant transconductance over the variation of the input voltage. A current feedback operational amplifier (CFOA) has been suggested in [43], which is based on composite current conveyor. The applications of the circuit such as grounded and floating inductors, grounded capacitance multipliers and frequency dependent negative resistors (FDNR) are also suggested. H. Jassim [8] proposed a CMOS current feedback operational amplifier (CFOA) in which a current feedback (CFB) operational transconductance amplifier (OTA) is used as the input stage and it is cascaded with the class AB cross coupled buffer stage. The circuit has high gain bandwidth product (GBW), low input offset voltage and low total harmonic distortion (THD).

Table 3.2 lists and compares different topologies used to develop current feedback operational amplifier as discussed above

Table 3.2 Parameters comparison of current feedback operational amplifier

Parameters	[41]	[42]	[8]
Supply Voltage (V)	±3.3	±0.75	±2.5
Technology(µm)	0.35	0.25	0.35
Power Consumption(mW)	5.3	0.456	5.5
Input voltage range(V)	N.A	±0.65	±1
Input offset Voltage(mV)	1.3	<20	0.2

GBW(MHz)	58	120	104
Phase Margin(Degree)	57.5	68	N.A
DC gain(dB)	74	N.A	67
Input Current range(μA)	N.A	±1000	N.A
THD @V@ MHz (dB)	-52 @ 0.2V p-p @ 5Mhz	N.A	-67

From the Table, the power consumption of current feedback operational amplifier suggested in [42] is less than that of other current feedback operational amplifier suggested in [41, 8]. The current feedback operational amplifier suggested in [8] has low input offset voltage as compared to other current feedback operational amplifier suggested in [41, 42].

3.4 Conclusions

Different topologies suggested by various authors to design current conveyors and current feedback operational amplifiers have been discussed in this chapter. The circuit parameters of CCII and CFOA are also presented.

CHAPTER 4

PROPOSED HIGH FREQUENCY LOW VOLTAGE CMOS CURRENT FEEDBACK OPERATIONAL AMPLIFIER

4.1 Introduction

In this chapter, high frequency low voltage CMOS current feedback operational amplifier (HFLVCFOA) circuits developed using biased positive second generation current conveyor circuits (CCII+) and voltage buffer have been proposed. Voltage divider circuits bias the current mirrors to copy the appropriate currents between the transistors of the current mirror. The chapter is organized as follows. Section 4.2 discusses the proposed positive second generation current conveyor circuits namely MOSFET-resistor voltage divider biased CCII+ (MRCCII+) and MOSFET-only voltage divider biased CCII+ (MOCCII+). The applications of proposed MOCCII+ are also discussed in the section. The high frequency low voltage current feedback operational amplifier based on MRCCII+ (HFLVCFOA-MR) and high frequency low voltage current feedback operational amplifier based on MOCCII+ (HFLVCFOA-MO) developed using the proposed MRCCII+ and MOCCII+, respectively are discussed in section 4.3. The applications of proposed HFLVCFOA-MO are also discussed in the section. The chapter is concluded in section 4.4.

4.2 Proposed Positive Second Generation Current Conveyors (CCII+)

Two positive second generation current conveyor (CCII+) circuits based on the mixed trans-linear loop [44] namely MOSFET-resistor voltage divider biased CCII+ (MRCCII+) and MOSFET-only voltage divider biased CCII+ (MOCCII+) have been proposed. In current mirrors, due to the short channel effects, accurate mirroring of the currents is not possible. In the proposed circuits reference voltages derived from power supply with the help of voltage divider circuits are used to bias the gates of the current mirror transistors to reduce the current difference. MOSFET-resistor voltage divider and MOSFET-only voltage divider circuits are used for generating the reference voltages [45]. The applications of the proposed MOCCII+ such as current integrator, current differentiator and transconductance amplifier are also proposed.

4.2.1 Proposed MOSFET-Resistor Voltage Divider Biased Positive Second Generation Current Conveyor (MRCCII+)

The proposed MOSFET–resistor voltage divider biased positive second generation current conveyor (MRCCII+) is shown in Figure 4.1. Three current mirrors are formed using PMOS transistors M_1-M_2, M_4-M_5, M_{10}-M_{11} and three current mirrors are formed using NMOS transistors M_8-M_9, M_{13}-M_{14} and M_{15}-M_{16}. The input stage of current conveyor is developed

using mixed trans-linear loop and it comprises of transistors M_8-M_{11}. MOSFET-resistor voltage divider formed by transistor M_6 and resistor R_2 bias the PMOS current mirror. NMOS current mirror is biased by the MOSFET-resistor voltage divider circuit comprising of transistor M_{18} and resistor R_4.

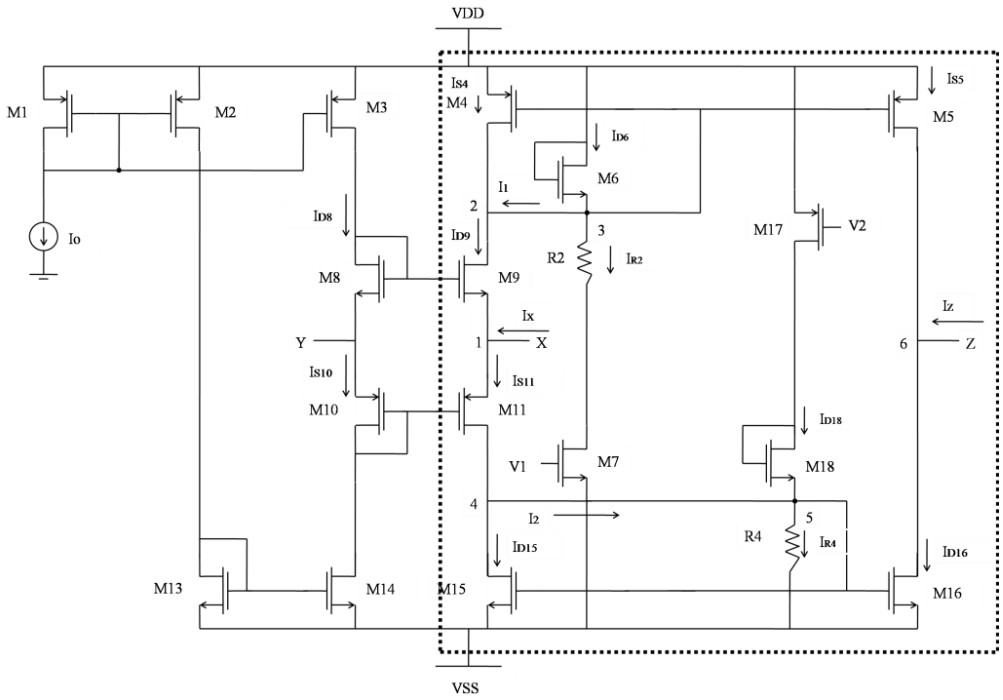

Figure 4.1 Proposed MRCCII+

Mixed trans-linear loop

The transistors M_8-M_{11} represents the mixed trans-linear loop as shown in Figure 4.1, which conveys the voltage V_Y applied at terminal Y to terminal X. Voltage at this terminal is represented by V_X. Transistors M_1, M_2, M_3, M_{13} and M_{14} are used to provide the DC reference current I_o to the mixed trans-linear loop.

From Figure 4.1 the gate-to-source voltages V_{GS8} and V_{GS9} of transistors M_8 and M_9 are given as

$$V_{GS8} = V_{G8} - V_Y \tag{4.1}$$

$$V_{GS9} = V_{G9} - V_X \tag{4.2}$$

where V_Y and V_X represents the voltage at terminal Y and X respectively

The transistors M_8 and M_9 are operating in the saturation region, so

$$V_{GS8} = V_{GS9} \tag{4.3}$$

Using equations (4.1), (4.2) and (4.3), we get

$$V_Y = V_X \tag{4.4}$$

If a varying voltage is applied to the terminal Y, current flows through the transistors M_8 and M_{10} corresponding to the varying voltage. If the transistor pairs are of the same size then same drain current will flow in transistors M_8-M_9 and M_{10}-M_{11}, provided the transistors are in saturation region. The relationship between drain currents I_{D_9}, $I_{D_{11}}$, I_{D_8}, $I_{D_{10}}$ of the transistors M_9, M_{11}, M_8 and M_{10}, respectively is given as [46]

$$\sqrt{\frac{I_{D_9}}{\beta_n}} + \sqrt{\frac{I_{D_{11}}}{\beta_p}} = \sqrt{\frac{I_{D_8}}{\beta_n}} + \sqrt{\frac{I_{D_{10}}}{\beta_p}} \tag{4.5}$$

where β_n and β_p are the transconductance parameter of NMOS and PMOS transistors

The relationship between voltage V_Y and V_X can be written as [44]

$$V_Y = V_X + \frac{I_X}{\sqrt{2I_o C_{OX}}\left(\sqrt{\mu_p \left(\frac{W}{L}\right)_p} + \sqrt{\mu_n \left(\frac{W}{L}\right)_n}\right)} \tag{4.6}$$

and the input resistance at terminal X (Z_x) can be written as

$$Z_X = \frac{1}{\sqrt{2I_o C_{OX}}\left(\sqrt{\mu_p \left(\frac{W}{L}\right)_p} + \sqrt{\mu_n \left(\frac{W}{L}\right)_n}\right)} \tag{4.7}$$

From equation (4.7) it is observed that Z_X depends on DC reference current I_O. Therefore, the value of the reference current should be chosen properly to obtain low value of input impedance at terminal X.

The relationship between the input current I_X and output current I_Z is derived with the help of Figure 4.1. Applying KCL at node 3, the current I_1 is given as

$$I_1 = I_{D6} - I_{R2} \tag{4.8}$$

where I_{D6} and I_{R2} are the currents of the transistor M_6 and resistor R_2 respectively.

Applying KCL at node 2, the current I_{D9} is given as

$$I_{D9} = I_{S4} + I_1 \tag{4.9}$$

where I_{D9} and I_{S4} are the drain and source currents of the transistors M_9 and M_4 respectively.

Applying KCL at node 1, the current I_{S11} is given as

$$I_{S11} = I_{D9} + I_X \tag{4.10}$$

where I_{S11} and I_{D9} are the currents of the transistors M_{11} and M_9 respectively, I_X is the applied input current.

Applying KCL at node 5, the current I_2 can be written as

$$I_2 = I_{R4} - I_{D18} \tag{4.11}$$

where I_{D18} and I_{R4} are the currents of the transistor M_{18} and resistor R_4 respectively.

Applying KCL at node 4, the current I_{D15} is given as

$$I_{D15} = I_{S11} - I_2 \quad (4.12)$$

where I_{D15} and I_{S11} are the drain and source currents of the transistors M_{15} and M_{11}. respectively.

Using equations (4.8) to (4.12), the current I_{D15} can be written as

$$I_{D15} = I_{S4} + I_{D6} - I_{R2} + I_X - I_{R4} + I_{D18} \quad (4.13)$$

Because of the current mirroring action equal currents flow in transistor pairs M_4-M_5 and M_{15}-M_{16}

$$I_{D16} = I_{D15} \quad (4.14)$$

where I_{D16} and I_{D15} are the currents of the transistors M_{16} and M_{15} respectively.

$$\text{and } I_{S4} = I_{S5} \quad (4.15)$$

where I_{S4} and I_{S5} are the currents of the transistors M_4 and M_5 respectively

Applying KCL at node 6, the current I_{D16} is written as

$$I_{D16} = I_{S5} + I_Z \quad (4.16)$$

where I_{D16} and I_{S5} are the currents of the transistors M_{16} and M_5 respectively and I_Z is the current at node 6

Substituting the expression of I_{D16} from equation (4.16) in equation (4.13), we get

$$I_{S4} + I_{D6} - I_{R2} + I_X - I_{R4} + I_{D18} = I_{S5} + I_Z \quad (4.17)$$

By keeping appropriate width and resistance value of the transistor M_6 and resistor R_4 respectively, the current equation can be written as

$$I_{D6} = I_{R4} \quad (4.18)$$

By keeping appropriate widths of transistors M_7, M_{17} and M_{18} and applying appropriate biasing voltages V_1 and V_2 the relation between currents through resistor R_2 and transistor M_{18} is expressed as

$$I_{R2} = I_{D18} \quad (4.19)$$

From equations (4.15) to (4.19), it can be concluded as

$$I_X = I_Z \quad (4.20)$$

Small Signal Analysis

To calculate, impedance level at terminal Y we apply a test signal v_t as shown in Figure 4.2.

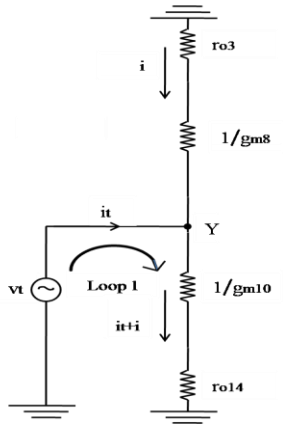

Figure 4.2 Impedance at terminal Y

The current i is given as

$$i = \frac{-v_t}{r_{o3} + \frac{1}{g_{m8}}} \tag{4.21}$$

where r_{o3} is the output resistance of transistor M_3, g_{m8} is the transconductance of transistor M_8 and v_t is the test signal applied.

By applying KVL in loop 1, we get

$$v_t = (i + i_t)\left(\frac{1}{g_{m10}} + r_{o14}\right) \tag{4.22}$$

where, i_t is test current from the source v_t, g_{m10} is the transconductance of transistor M_{10} and r_{o14} is the output resistance of transistor M_{14}

Substituting the value of i from equation (4.21) in equation (4.22) the impedance at terminal Y is given as

$$\frac{v_t}{i_t} = Z_Y = \frac{\left(r_{o3} + \frac{1}{g_{m8}}\right)\left(r_{o14} + \frac{1}{g_{m10}}\right)}{r_{o3} + \frac{1}{g_{m8}} + r_{o14} + \frac{1}{g_{m10}}} \tag{4.23}$$

where r_{o3} and r_{o14} are the output resistance of transistors M_3 and M_{14} respectively, g_{m8} and g_{m10} are the transconductance of transistors M_8 and M_{10} respectively.

The small signal model for calculating the voltage gain between the terminals Y and X is shown in Figure 4.3.

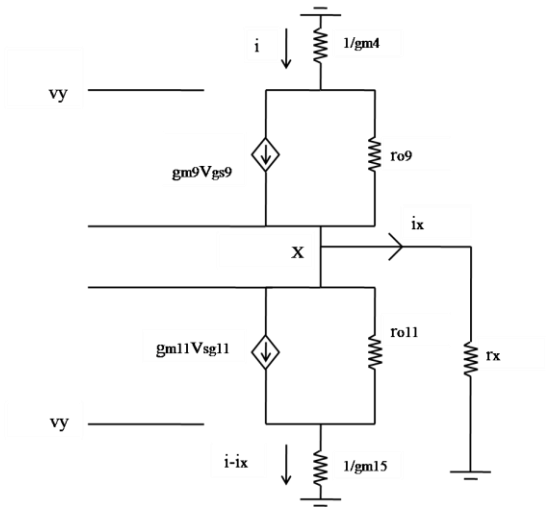

Figure 4.3 Small signal model for voltage gain

The current i is given as

$$i = g_{m9}v_{gs9} + \frac{v_9}{r_{o9}} \tag{4.24}$$

where, g_{m9} and r_{o9} are the transconductance and output resistance of transistor M_9 respectively ,v_9 is the potential drop across resistor r_{o9} and v_{gs9} is the gate-to-source voltage of transistor M_9.

Applying KCL at node X, we get

$$i - i_x = g_{m11}v_{sg11} + \frac{v_{11}}{r_{o11}} \tag{4.25}$$

where, g_{m11} and r_{o11} are the transconductance and output resistance of transistor M_{11} respectively , v_{11} is the potential drop across resistor r_{o11}, v_{sg11} is the source-to-gate voltage of transistor M_{11} and i_x is the current through load resistance r_x.

Voltage v_x across resistor r_x is given as

$$v_x = r_x i_x = v_{11} + \frac{1}{g_{m15}}(i - i_x) \tag{4.26}$$

The source-to-gate voltage of transistor M_{11} is given as

$$v_{sg11} = v_x - v_y \tag{4.27}$$

The gate-to-source voltage of transistor M_9 is given as

$$v_{gs9} = v_y - v_x \tag{4.28}$$

Using equations (4.24) to (4.28), the voltage gain of the current conveyor is obtained as

$$\frac{v_X}{v_Y} = \frac{g_{m9} + g_{m11}}{g_{m9} + g_{m11} + \frac{1}{r_{o9}} + \frac{1}{r_{o11}} + \frac{1}{r_X}} \tag{4.29}$$

where, r_{o9} and g_{m9} are the output resistance and transconductance of transistor M_9, r_{o11} and g_{m11} are the output resistance and transconductance of transistor M_{11} and r_x is the load resistance at terminal X.

From equation 4.29, it is evident that to maximize the voltage gain, the transconductance of the transistors M_9 and M_{11} should be kept high.

For calculating the input impedance at terminal X (Z_X), we apply a voltage source v_X at terminal X as shown in Figure 4.4.

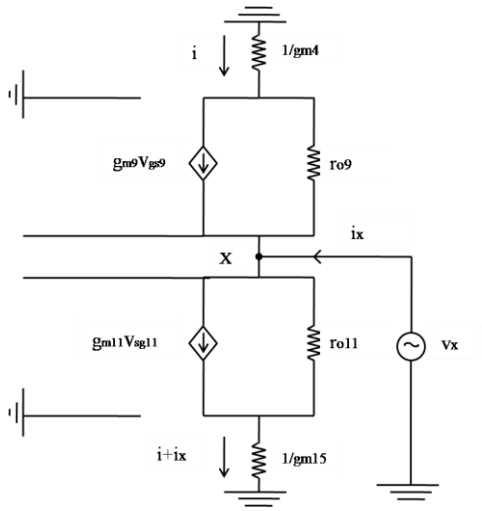

Figure 4.4 Input impedance at terminal X

The current i is given as

$$i = g_{m9}v_{gs9} + \frac{v_9}{r_{o9}} \tag{4.30}$$

where, g_{m9} and r_{o9} are the transconductance and output resistance of transistor M_9 respectively ,v_9 is the potential drop across resistor r_{o9} and v_{gs9} is the gate-to-source voltage of transistor M_9.

The voltage v_9 across resistor r_9 is given as

$$v_9 = - v_x - \frac{i}{g_{m4}} \tag{4.31}$$

where g_{m4} is the transconductance of transistor M_4 , v_x is the applied voltage source at node X.

Substituting the value of v_9 from equation (4.31) in equation (4.30), the current i is given as

$$i = g_{m9}v_{gs9} - \frac{v_x}{r_{o9}} - \frac{i}{g_{m4}r_{o9}} \tag{4.32}$$

where, g_{m9} and r_{o9} are the transconductance and output resistance of transistor M_9 respectively ,v_x is the applied voltage source and v_{gs9} is the gate-to-source voltage of transistor M_9.

Applying KCL at node X, we get

$$i + i_x = g_{m11}v_{sg11} + \frac{v_{11}}{r_{o11}} \quad (4.33)$$

where g_{m11} and r_{o11} are the transconductance and output resistance of transistor M_{11} respectively, v_{11} is the potential drop across r_{o11}, i_x is the input current at node X .

The gate-source voltage of transistor M_9 is written as

$$v_{gs9} = -v_x \quad (4.34)$$

The source-gate voltage of transistor M_{11} is given as

$$v_{sg11} = v_x \quad (4.35)$$

The voltage v_{11} across resistor r_{11} is given as

$$v_{11} = v_x - \frac{(i + i_x)}{g_{m15}} \quad (4.36)$$

Using equations (4.30) to (4.36), input impedance at terminal X is given as

$$\frac{v_x}{i_x} = Z_x = \frac{1}{g_{m9} + \frac{1}{r_{o9}} + g_{m11} + \frac{1}{r_{o11}}} \quad (4.37)$$

where g_{m11} and r_{o11} are the transconductance and output resistance of transistor M_{11} respectively and $g_{m9}$and r_{o9} are the transconductance and output resistance of transistor M_9 respectively

The small signal current gain expression of the proposed block can be derived with help of Figure 4.5 and considering $g_m r_o >> 1$ where g_m and r_o are the transconductance and output resistance of the transistor respectively.

The current i is given as

$$i = g_{m4}v_{sg4} - \frac{v_{g4}}{R_5} \quad (4.38)$$

where v_{g4} is the gate voltage of transistor M_4 and equivalent resistance $R_5 = r_{04} \| \frac{1}{g_{m6}} \| (R_2 + r_{07})$, in which r_{04} and r_{07} are the output resistance of transistors M_4 and M_7, g_{m6} is the transconductance of transistor M_6.

Applying KCL at node 1, we get

$$g_{m4}v_{sg4} - \frac{v_{g4}}{R_5} = g_{m9}v_{gs9} + \frac{v_{g4} - v_x}{r_{o9}} \quad (4.39)$$

where v_{g4} is the gate voltage of transistor M_4, v_{sg4} is the source-to-gate voltage of transistor M_4, v_{gs9} is the gate-to-source voltage of transistor M_9 and v_x is the voltage at terminal X.

Applying KCL at node X, we get

$$i + i_x = g_{m11}v_{sg11} + \frac{v_x - v_{g15}}{r_{o11}} \quad (4.40)$$

where v_{g15} is the gate voltage of transistor M_{15} , v_x is the voltage at node X, g_{m11} and r_{o11} are the transconductance and output resistor of transistor M_{11} respectively, v_{11} is the potential drop across r_{o11}.

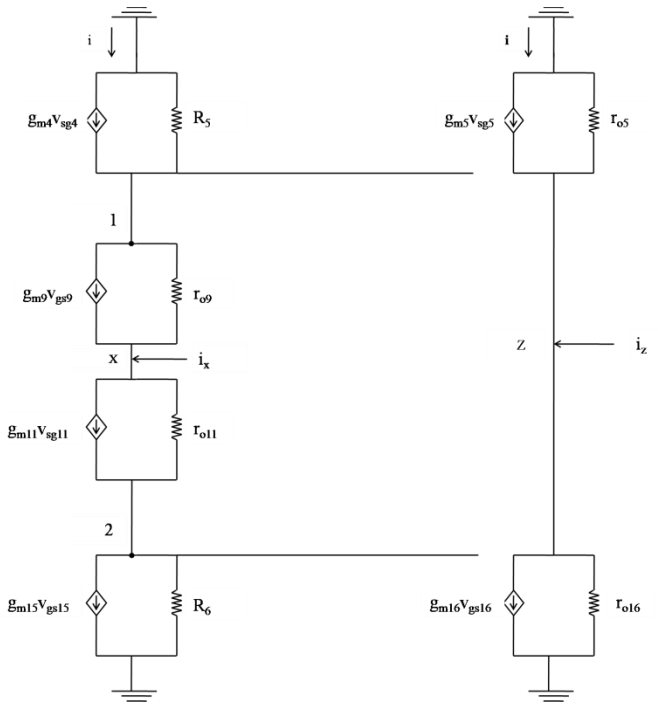

Figure 4.5 small signal model for current gain

Applying KCL at node 2, we get

$$g_{m11}v_{sg11} + \frac{v_x - v_{g15}}{r_{o11}} = \frac{v_{g15}}{R_6} + g_{m15}v_{g15} \tag{4.41}$$

where v_x is the voltage at node X, equivalent resistance $R_6 = r_{015} \| R_4 \| (\frac{1}{g_{m18}} + r_{017})$, in which r_{015} and r_{017} are the output resistor of transistors M_{15} and M_{17}, g_{m18} is the transconductance of transistor M_{18}.

The current i can also be written as

$$i = g_{m5}v_{sg5} - \frac{v_z}{r_{o5}} \tag{4.42}$$

where v_z is potential drop across resistor r_{o5} , g_{m5} and v_{sg5} are the transconductance and source-to-gate voltage of transistor M_5.

Applying KCL at node Z, we get

$$i + i_z = g_{m16}v_{gs16} + \frac{v_z}{r_{o16}} \tag{4.43}$$

where g_{m16}, v_{gs16} and r_{o16} are the transconductance, gate-to-source voltage and output resistance of transistor M_{16}.

Using equations (4.38) to (4.43) and considering $v_{g4} = v_{g5}$, expression of current gain can be written as

$$\frac{i_z}{i_x} = \frac{g_{m9}\, g_{m15} g_{m5} + g_{m11} g_{m4} g_{m16}}{g_{m4} g_{m15}\, (g_{m9} + g_{m11})} \tag{4.44}$$

From equation (4.44), it can be concluded that if $g_{m4}= g_{m5}$ and $g_{m16}= g_{m15}$, then the current transfer ratio is equal to unity.

The output stage of proposed MRCCII+ is shown by dotted lines in Figure 4.1. The class –AB current output stage is developed using PMOS current mirror transistor pair M_4-M_5 along with the NMOS current mirror transistor pair M_{15}-M_{16}. Due to short channel effects drain current in both the branches of current mirror are not equal. So, to copy the appropriate currents a reference voltage is applied at the gates of current mirror transistor pairs. The reference voltage derived by the MOSFET-resistor voltage divider is equal to the potential drop across the resistor R as shown in Figure 4.6.

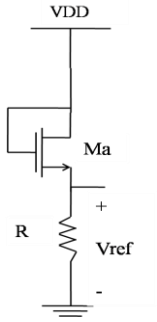

Figure 4.6 MOSFET-resistor voltage divider [39]

Transistor M_a is operating in saturation region, the current through Transistor M_a is given as as

$$\frac{\beta_a (V_{DD}- V_{ref}-V_{th})^2}{2} = \frac{V_{ref}}{R} \tag{4.45}$$

where, V_{ref} is the reference voltage across resistor R, V_{th} is the threshold voltage of transistor M_a and $\beta_a$is the transconductance parameter of transistor M_a.

The sensitivity ($S_{V_{DD}}^{V_{ref}}$) of the reference voltage to V_{DD} [39] when V_{DD}>>V_{ref} is given as

$$S_{V_{DD}}^{V_{ref}} = \frac{1}{V_{th}\sqrt{\frac{2R\beta_a}{V_{DD}}+2}} \tag{4.46}$$

The voltage divider formed using MOSFET-resistor has the advantage of less sensitivity towards power supply variation as shown by equation (4.46). The main problem with this circuit is that to reduce the power dissipation, the value of the resistance must be very large [39]. So to reduce the power consumption a MOSFET-only voltage divider biased positive second generation current conveyor (MOCCII+) is proposed.

4.2.2 Proposed MOSFET-Only Voltage Divider Biased Positive Second Generation Current Conveyor (MOCCII+)

The proposed MOSFET–only voltage divider biased positive second generation current conveyor (MOCCII+) is shown in Figure 4.7. Three current mirrors are formed using PMOS transistors M_1-M_2, M_4-M_5, M_{10}-M_{11} and three current mirrors are formed using NMOS transistors M_8-M_9, M_{13}-M_{14} and M_{15}-M_{16}. The input stage of current conveyor is developed using mixed trans-linear loop and it comprises of transistors M_8-M_{11}. MOSFET-only voltage divider circuit formed by transistors M_6 and M_7 bias the PMOS current mirror. NMOS

current mirror is biased by the MOSFET-only voltage divider circuit comprising of transistor M_{18} and M_{19}.

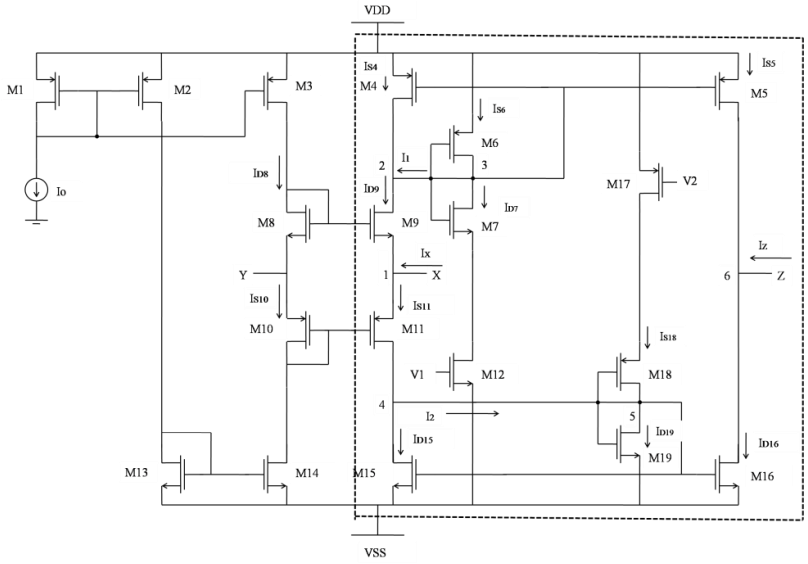

Figure 4.7 Proposed MOCCII+

Mixed trans-linear loop

The input stage of current conveyor which is represented by a mixed trans-linear loop as shown in Figure 4.7 comprises of transistors M_8-M_{11}. The role of the mixed trans-linear loop is to convey the voltage V_Y applied at terminal Y to terminal X. Voltage at this terminal is represented by V_X. Biasing current is transferred to the mixed trans-linear loop with the help of transistors M_1, M_2, M_3, M_{13} and M_{14}.

The relationship between voltage V_Y and V_X can be written as [44]

$$V_Y = V_X + \frac{I_X}{\sqrt{2I_o C_{OX}}\left(\sqrt{\mu_p \left(\frac{W}{L}\right)_p} + \sqrt{\mu_n \left(\frac{W}{L}\right)_n}\right)} \tag{4.47}$$

and the input resistance at terminal X (Z_X) can be written as

$$Z_X = \frac{1}{\sqrt{2I_o C_{OX}}\left(\sqrt{\mu_p \left(\frac{W}{L}\right)_p} + \sqrt{\mu_n \left(\frac{W}{L}\right)_n}\right)} \tag{4.48}$$

From equation (4.48) it is observed that Z_X depends on DC reference current I_O. Therefore, the value of the reference current should be chosen properly to obtain low value of input impedance at terminal X.

The relationship between the input current I_X and output current I_Z is derived with the help of Figure 4.7. Applying KCL at node 3, the current I_1 is given as

$$I_1 = I_{S6} - I_{D7} \tag{4.49}$$

where I_{S6} and I_{D7} are the currents of the transistor M_6 and M_7 respectively

Applying KCL at node 2, the current I_{D9} is given as

$$I_{D9} = I_{S4} + I_1 \tag{4.50}$$

where I_{D9} and I_{S4} are the drain and source currents of the transistors M_9 and M_4 respectively.

Applying KCL at node 1, the current I_{S11} is given as

$$I_{S11} = I_{D9} + I_X \quad (4.51)$$

where I_{S11} and I_{D9} are the currents of the transistors M_{11} and M_9 respectively, I_X is the applied input current.

Applying KCL at node 5, the current I_2 can be written as

$$I_2 = I_{D19} - I_{S18} \quad (4.52)$$

where I_{S18} and I_{D19} are the currents of the transistors M_{18} and M_{19} respectively

Applying KCL at node 4, the current I_{D15} is given as

$$I_{D15} = I_{S11} - I_2 \quad (4.53)$$

where I_{D15} and I_{S11} are the drain and source currents of the transistors M_{15} and M_{11} respectively.

Using (4.49) to (4.53), the current I_{D15} can be written as

$$I_{D15} = I_{S4} + I_{S6} - I_{D7} + I_X - I_{D19} + I_{S18} \quad (4.54)$$

Because of the current mirroring action equal currents flow in transistor pairs M_4-M_5 and M_{15}-M_{16}

$$I_{D16} = I_{D15} \quad (4.55)$$

where I_{D16} and I_{D15} are the currents of the transistors M_{16} and M_{15} respectively

and $I_{S4} = I_{S5}$ (4.56)

where I_{S4} and I_{S5} are the currents of the transistors M_4 and M_5 respectively

Applying KCL at node 6, the current I_{D16} is given as

$$I_{D16} = I_{S5} + I_Z \quad (4.57)$$

where I_{D16} and I_{S5} are the currents of the transistors M_{16} and M_5 respectively, I_Z is the current at node 6

Substituting the expression of I_{D16} from equation (4.57) in equation (4.54), we get

$$I_{S5} + I_Z = I_{S4} + I_{S6} - I_{D7} + I_X - I_{D19} + I_{S18} \quad (4.58)$$

By keeping appropriate width of the transistors M_6 and M_{19} respectively, the current equation can be written as

$$I_{S6} = I_{D19} \quad (4.59)$$

By keeping appropriate widths of transistors M_{12}, M_{17},M_{18} and M_7 the relation between currents through transistors M_{18} and M_7 is expressed as

$$I_{D7} = I_{S18} \quad (4.60)$$

From equations (4.55) to (4.60), it can be concluded as

$$I_X = I_Z \quad (4.61)$$

The output stage of MOCCII+ is shown by dotted line in Figure 4.7.

In order to copy appropriate current, the gates of both transistors pairs M_4-M_5 and M_{15}-M_{16} are biased as shown in Figure 4.7 by the reference voltages. A reference voltage equal to the voltage at the gate of the MOSFETS with respect to the ground is generated by the MOSFET-only voltage divider [39] as shown in Figure 4.8

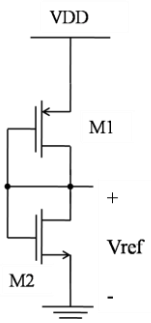

Figure 4.8 MOSFET-only voltage divider [39]

Equal current flows through the transistors M_1 and M_2, therefore the current equation can be written as

$$\frac{\beta_1 (V_{DD}-V_{ref}-V_{thp})^2}{2} = \frac{\beta_2 (V_{ref}-V_{thn})^2}{2} \tag{4.62}$$

where V_{ref} is the reference voltage across the transistor M_2 . V_{thn} and V_{thp} are the threshold voltages of M_2 and M_1 transistors respectively. β_1 and β_2 are the transconductance parameter of M_1 and M_2 transistors respectively.

Rearranging equation (4.62), the value of reference voltage is given as

$$V_{ref} = \frac{V_{DD}-V_{thp}+\sqrt{\frac{\beta_2}{\beta_1}}V_{thn}}{1+\sqrt{\frac{\beta_2}{\beta_1}}} \tag{4.63}$$

The sensitivity of V_{ref} with respect to V_{DD} ($S_{V_{DD}}^{V_{ref}}$) is given as in [39]

$$S_{V_{DD}}^{V_{ref}} = \frac{V_{DD}}{V_{DD}-V_{thp}+\sqrt{\frac{\beta_2}{\beta_1}}\,V_{thn}} \tag{4.64}$$

From equation (4.64), it can be seen that the reference voltage is highly sensitive to the variation in power supply as compared to MOSFET-resistor voltage divider. The main advantage of MOSFET-only voltage divider circuit is that the circuit has less power dissipation as compared to MOSFET-resistor voltage divider circuit.

Small Signal Analysis

The impedance at terminal Y is given by the equation (4.23) as

$$\frac{v_t}{i_t} = Z_Y = \frac{\left(r_{o3}+\frac{1}{g_{m8}}\right)\left(r_{o14}+\frac{1}{g_{m10}}\right)}{\left(r_{o3}+\frac{1}{g_{m8}}+r_{o14}+\frac{1}{g_{m10}}\right)} \tag{4.65}$$

where, r_{o3} and r_{o14} are the output resistance of transistors M_3 and M_{14}, g_{m10} and g_{m8} are the transconductance of transistors M_{10} and M_8 .

Using equation (4.29) the voltage gain of the current conveyor is written as

$$\frac{v_X}{v_Y} = \frac{(g_{m9} + g_{m11})}{g_{m9} + g_{m11} + \frac{1}{r_{o9}} + \frac{1}{r_{o11}} + \frac{1}{r_X}} \quad (4.66)$$

where, r_{o9} and g_{m9} are the output resistance and transconductance of transistor M_9, r_{o11} and g_{m11} are the output resistance and transconductance of transistor M_{11} and r_x is the load resistance at terminal X.

The small signal current gain expression is written using the equation (4.44) as

$$\frac{i_z}{i_x} = \frac{g_{m9}\, g_{m15} g_{m5} + g_{m11} g_{m4} g_{m16}}{g_{m4} g_{m15} (g_{m9} + g_{m11})} \quad (4.67)$$

Since the proposed MOCCII+ is implemented using MOSFETS only therefore large resistors are avoided hence power dissipation and layout area is reduced.

4.2.3 Applications of The Proposed MOCCII+

The proposed MOSFET-only voltage divider biased positive second generation current conveyor (MOCCII+) is used to develop some of the important analog signal processing building blocks like current integrator, current differentiator and transconductance amplifier as its applications.

4.2.3.1 Proposed Current Integrator using MOCCII+

A current integrator is shown in Figure 4.9. The circuit has been developed using proposed MOCCII+.

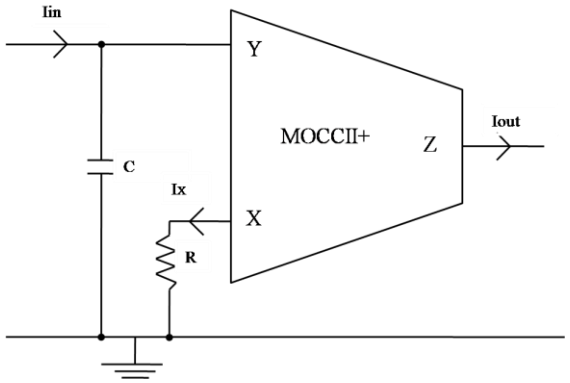

Figure 4.9 Proposed current integrator using MOCCII+

The output current of proposed integrator is

$$I_{out} = I_Z \quad (4.68)$$

From equation (4.61)

$$I_Z = I_X \quad (4.69)$$

$$I_{out} = \frac{V_X}{R} = \frac{V_Y}{R} \quad (4.70)$$

where V_X and V_Y are voltage at terminals X and Y and R is the load resistance at terminal X

$$V_Y = \frac{I_{in}}{sC} \quad (4.71)$$

where I_{in} is the current applied at terminal Y.

Using equations (4.70) and (4.71), the output current is modified as

$$I_{out} = \frac{I_{in}}{sCR} \quad (4.72)$$

From equation (4.72), it can be seen that the proposed circuit behaves like a current integrator.

4.2.3.2 Proposed Current Differentiator using MOCCII+

As an application of the proposed MOCCII+ a CCII based current differentiator is developed as shown in Figure 4.10

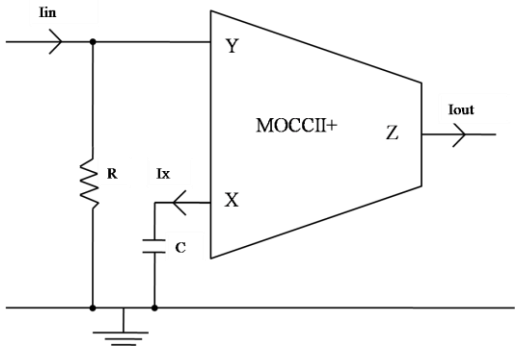

Figure 4.10 Proposed current differentiator using MOCCII+

The output current of proposed differentiator is

$$I_{out} = I_Z \quad (4.73)$$

From equation (4.61) the current I_Z is given as

$$I_Z = I_X \quad (4.74)$$

where I_X is the current passing through capacitor C

From equations (4.74) and (4.73)

$$I_{out} = \frac{V_X}{\frac{1}{sC}} = sCV_X \quad (4.75)$$

Since $V_X = V_Y$, so equation (4.75) can be written as

$$I_{out} = sCV_Y \quad (4.76)$$

The voltage at terminal Y (V_Y) is

$$V_Y = RI_{in} \quad (4.77)$$

where I_{in} is the current applied at terminal Y

From equations (4.76) and (4.77), the currentI_{out} is given as

$$I_{out} = sCRI_{in} \quad (4.78)$$

From equation (4.78), it can be seen that the proposed circuit behaves like a current differentiator.

4.2.3.3 Proposed MOCCII+ Based Transconductance Amplifier

A MOCCII+ based transconductance amplifier is developed as application of the proposed MOCCII+ is shown in Figure 4.11

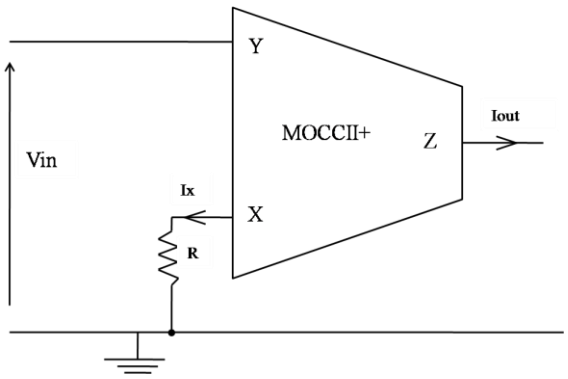

Figure 4.11 MOCCII+ based transconductance amplifier

The output current of transconductance amplifier is

$$I_{out} = I_Z \tag{4.79}$$

The input voltage applied at terminal Y is given as

$$V_{in} = V_Y \tag{4.80}$$

Since $V_Y = V_X = I_X R$ (4.81)

where I_X is the current across resistor R, the input voltage V_{in} is given as

$$V_{in} = I_X R \tag{4.82}$$

From equation (4.61), the current I_X is given as

$$I_X = I_Z \tag{4.83}$$

Using equations (4.81), (4.82) and (4.83), input voltage V_{in} is given as

$$V_{in} = I_z R \tag{4.84}$$

From equations (4.83) and (4.84), transconductance expression can be written as

$$\frac{I_{out}}{V_{in}} = \frac{1}{R} \tag{4.85}$$

From equation (4.85), it can be seen that the proposed circuit behaves like a transconductance amplifier.

4.3 Proposed High Frequency Low Voltage CMOS Current Feedback Operational Amplifiers (HFLVCFOA)

In this section, two current feedback operational amplifiers namely high frequency low voltage current feedback operational amplifier based on MRCCII+ (discussed in section 4.2.1) and high frequency low voltage current feedback operational amplifier based on MOCCII+ (discussed in section 4.2.2) are proposed.

4.3.1 Proposed High Frequency Low Voltage Current Feedback Operational Amplifier Based on MRCCII+ (HFLVCFOA-MR)

The proposed high frequency low voltage current feedback operational amplifier based on MRCCII+ (HFLVCFOA-MR) is shown in Figure 4.12. The circuit is developed by cascading a voltage buffer stage at the output of the proposed MRCCII+. The voltage buffer stage is based on mixed trans-linear loop.

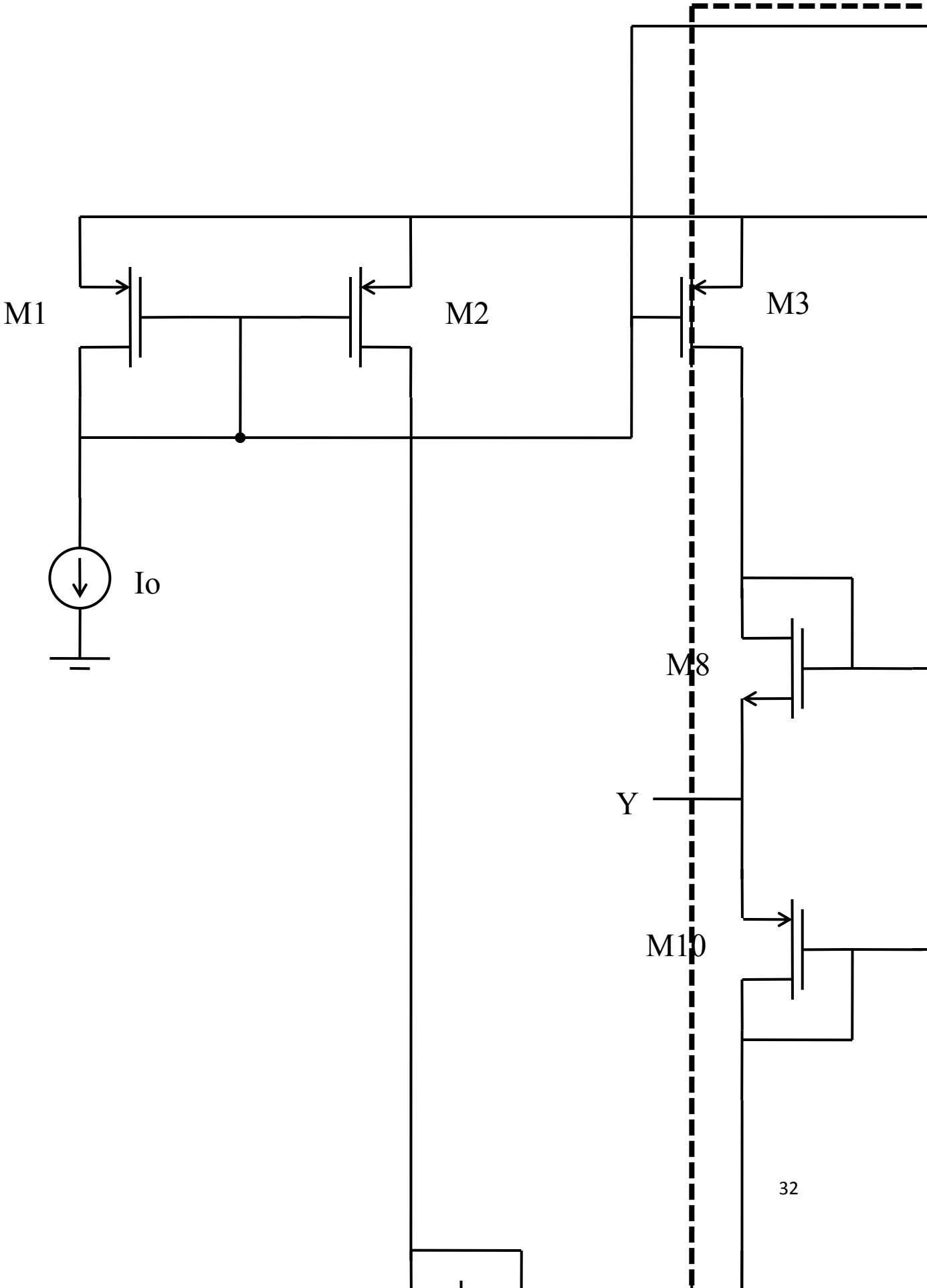
M1
M2
M3
Io
M8
Y
M10

Figure 4.12 Proposed HFLVCFOA-MR based on MRCCII+

The NMOS current mirror transistors M_{20}-M_{21} and PMOS current mirror transistors M_{22}-M_{23} forms the mixed trans-linear loop which acts as voltage buffer between the terminals Z and O. DC reference current I_O is provided to the mixed trans-linear loop with the help of transistors M_{19} and M_{24}. A varying voltage at terminal Z is conveyed to the terminal O till the current mirror transistor pairs M_{20}-M_{21} and M_{22}-M_{23} remains in saturation.

Using equation (4.23) the input impedance level at the terminal Z is given by the equation

$$Z_Z = \frac{\left(r_{o19} + \frac{1}{g_{m20}}\right)\left(r_{o24} + \frac{1}{g_{m22}}\right)}{\left(r_{o19} + \frac{1}{g_{m20}} + r_{o24} + \frac{1}{g_{m22}}\right)} \tag{4.86}$$

where r_{o19} . and r_{o24} are the output resistance of transistors M_{19} and M_{24}, g_{m20} and g_{m22} are the transconductance of transistors M_{20} and M_{22} respectively

Using equation (4.29) small signal voltage gain between the terminals Z and O is expressed by the equation

$$\frac{v_o}{v_z} = \frac{g_{m21} + g_{m23}}{g_{m21} + g_{m23} + \frac{1}{r_{o21}} + \frac{1}{r_{o23}} + \frac{1}{r_o}} \tag{4.87}$$

where r_{o21} and g_{m21} are the output resistance and transconductance of transistor M_{21} respectively and r_{o23} and g_{m23} are the output resistance and transconductance of transistor M_{23} respectively, $r_o$is the load resistance at terminal O.

From equation (4.87), it is apparent that in order to maximize the voltage gain, the transconductance of the transistors M_{21} and M_{23}should be kept high. The transconductance of transistor can only be increased by increasing the width of the transistors for a fixed value of I_o and length of the transistors. So in order to increase the voltage gain, the width of the transistors forming mixed linear loop should be kept large.

4.3.2 Proposed High Frequency Low Voltage Current Feedback Operational Amplifier Based on MOCCII+ (HFLVCFOA-MO)

The proposed high frequency low voltage current feedback operational amplifier based on proposed MOCCII+ (HFLVCFOA-MO) as shown in Figure 4.13 is developed by cascading the proposed MOCCII+ and a voltage buffer stage.

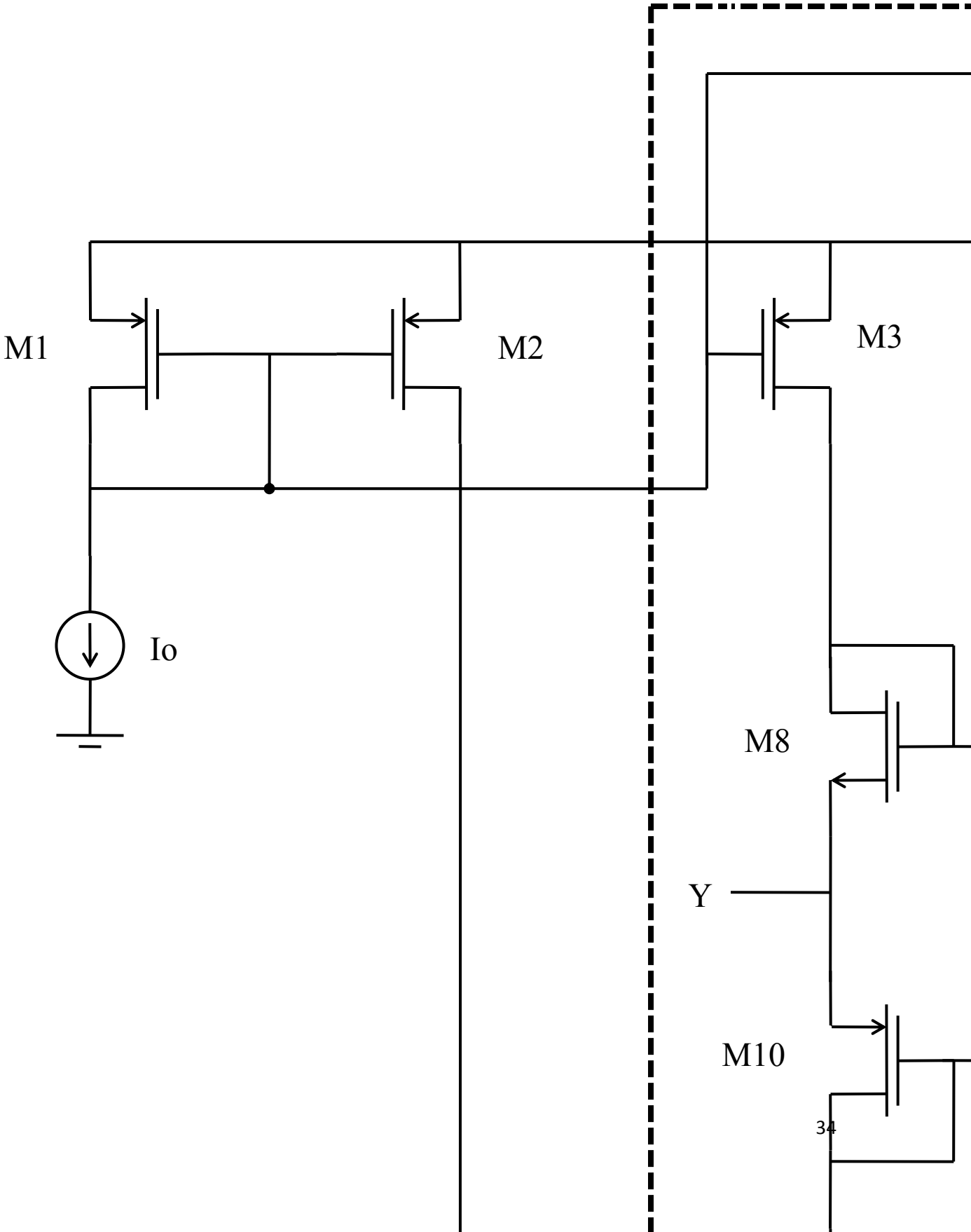
M1
M2
M3
Io
M8
Y
M10

Figure 4.13 Proposed HFLVCFOA-MO based on MOCCII+

Voltage buffer developed by mixed trans-linear loop which conveys the voltage at terminal Z to terminal O and comprises of PMOS current mirror transistors M_{21}-M_{22} and NMOS current mirror transistors M_{23}-$M_{24.}$ Transistors M_{20} and M_{25} provides the DC bias current to the mixed trans-linear loop.

Using equation (4.65) the input impedance level at the terminal Z is given as

$$Z_Z = \frac{\left(r_{o20} + \frac{1}{g_{m21}}\right)\left(r_{o25} + \frac{1}{g_{m23}}\right)}{\left(r_{o20} + \frac{1}{g_{m21}} + r_{o25} + \frac{1}{g_{m23}}\right)} \tag{4.88}$$

where r_{o20} and r_{o25} are the output resistance of transistors M_{20} and M_{25}, g_{m21} and g_{m23} are the transconductance of transistors M_{21} and M_{23} respectively.

Using equation (4.66) small signal voltage gain between the terminals Z and O is given as

$$\frac{v_o}{v_z} = \frac{g_{m22} + g_{m24}}{g_{m22} + g_{m24} + \frac{1}{r_{o22}} + \frac{1}{r_{o24}} + \frac{1}{r_o}} \tag{4.89}$$

where r_{o22} and g_{m22} are the output resistance and transconductance of transistor M_{22} respectively and r_{o24} and g_{m24} are the output resistance and transconductance of transistor M_{24} respectively, $r_o$is the load resistance at terminal O.

From equation 4.89, it is apparent that in order to maximize the voltage gain, the transconductance of the transistors M_{22} and M_{24}should be kept high. For increasing the transconductance width of the transistors should be increased for a fixed value of I_o and length of the transistors. So in order to increase the voltage gain, the width of the transistors forming mixed linear loop should be kept large.

The advantage of the proposed HFLVCFOA-MO is that the circuit has high gain bandwidth product.

4.3.3 Applications of Proposed HFLVCFOA-MO

The applications of the proposed high frequency low voltage current feedback operational amplifier based on MOCCII+ (HFLVCFOA-MO) as notch filter, inductor and frequency dependent negative resistor (FDNR) are also developed.

4.3.3.1 Proposed HFLVCFOA-MO Based Notch Filter

An application of the proposed HFLVCFOA-MO in the positive feedback topology is the notch filter using VCVS of gain K<1 as shown in Figure 4.14.

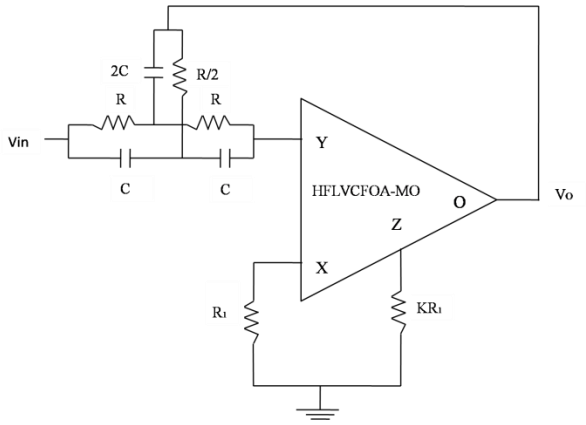

Figure 4.14 Proposed HFLVCFOA-MO based notch filter

The transfer function of the non-inverting notch filter is given as [23]

$$T(s) = \frac{1+K\,s^2C^2R^2}{s^2C^2R^2 + 4(1-K)sRC+1} \tag{4.90}$$

From equation (4.90), it can be seen that the proposed circuit behaves like a notch filter.

4.3.3.2 Proposed HFLVCFOA-MO Based Inductor

Inductor [23] based on the proposed HFLVCFOA-MO is shown in Figure 4.15.

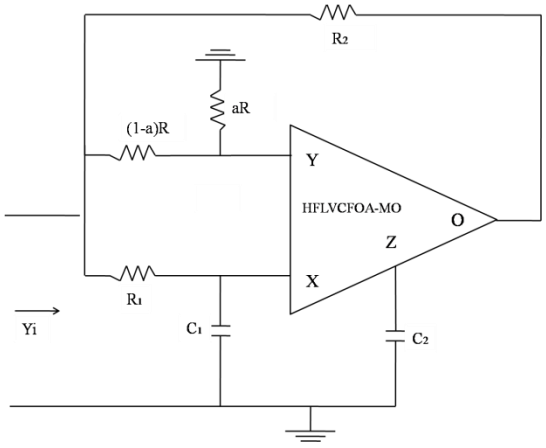

Figure 4.15 Proposed HFLVCFOA-MO based inductor

The input admittance is given as

$$Y_i = \frac{1-a}{sC_2R_1R_2} + \frac{1}{R} + \frac{1-a}{R_1} + \frac{1}{R_2} - \frac{a\,C_1}{C_2R_2} \tag{4.91}$$

The condition to realize an inductor is given as

$$\frac{a\,C_1}{C_2} = 1 + \frac{R_1}{R} + \frac{R_2(1-a)}{R_1} \tag{4.92}$$

By assuming appropriate values of capacitors and resistors and fulfilling the condition given in equation (4.92) an inductor circuit is realized.

4.3.3.3 Proposed HFLVCFOA-MO Based Frequency Dependent Negative Resistor (FDNR)

Frequency dependent negative resistor (FDNR) [23] as shown in Figure 4.16 is developed as an application of the proposed HFLVCFOA-MO.

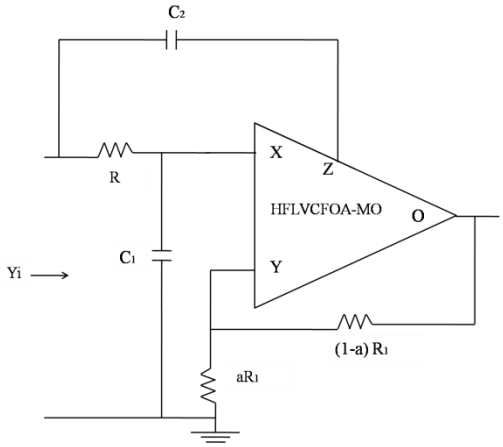

Figure 4.16 HFLVCFOA-MO based FDNR

FDNR shown in Figure 4.16 employs two capacitors. The circuit realizes the FDNR of magnitude $2C_2^2$R.

4.4 Conclusions

In the chapter, current feedback operational amplifier circuits have been developed using the proposed MRCCII+ and proposed MOCCII+. The applications based on the proposed MOCCII+ such as transonductance amplifier; current differentiator and current integrator are also developed. Notch filter, inductor and FDNR are also developed as applications of proposed HFLVCFOA-MO.

CHAPTER 5

SIMULATION RESULTS & LAYOUT

5.1 Introduction

All the proposed circuits such as MOSFET-resistor voltage divider biased positive second generation current conveyor (MRCCII+), MOSFET-only voltage divider biased positive second generation current conveyor (MOCCII+), MOCCII+ based current integrator, MOCCII+ based current differentiator, MOCCII+ based transcondutance amplifier, high frequency low voltage CMOS current feedback operational amplifier based on MRCCII+ (HFLVCFOA-MR) and high frequency low voltage CMOS current feedback operational amplifier based on MOCCII+ (HFLVCFOA-MO), HFLVCFOA-MO based Notch filter, HFLVCFOA-MO based inductor and HFLVCFOA-MO based frequency dependent negative resistor have been simulated using UMC 0.18µm CMOS process technology parameters. The circuits operate at power supply of ±0.9V and the reference DC current source I_o is 50µA. The organization of the chapter is as follows. Section 5.2 presents the simulation results of the proposed MOSFET-resistor voltage divider biased CCII+ (MRCCII+) and MOSFET-only voltage divider biased CCII+ (MOCCII+) along with the applications developed using the proposed MOCCCII+. The simulation results of the proposed high frequency low voltage current feedback operational amplifier developed using proposed MRCCII+ and MOCCII+ are discussed in section 5.3 and the results of the applications developed using proposed HFLVCFOA-MO are also presented. The layout design of the proposed HFLVCFOA-MO, designed in Cadence Virtuoso XL layout editor using UMC 0.18µm CMOS process technology is addressed in Section 5.4.The chapter is concluded in section 5.5.

5.2 Simulation Results of The Proposed Positive Second Generation Current Conveyors

In this section, simulation results of the proposed MRCCII+ and MOCCII+ are presented. Simulation results of MOCCII+ based current integrator, current differentiator and transconductance amplifier developed as the applications of proposed MOCCII+ are also discussed.

5.2.1 Simulation Results of The Proposed MOSFET-Resistor Voltage Divider Biased Positive Second Generation Current Conveyor (MRCCII+)

The proposed MRCCII+ has been simulated using UMC 0.18 µm CMOS process technology parameters. The transistors dimension of the proposed MRCCII+ are listed in Table 5.1.

Table 5.1 Transistor dimensions of MRCCII+

MOSFETS	W(µm)/L(µm)
M_1-M_2	1.2/0.22
M_3	1.34/0.22
M_4-M_5	92/0.22
M_6	0.3/0.22
M_7	1.5/0.22
M_8-M_9	30/0.22
M_{10}-M_{11}	100/0.22
M_{13}-M_{14}	1/0.22
M_{15}-M_{16}	60/0.22
M_{17}	8.8/0.22
M_{18}	2.6/0.22
R_2	0.5K
R_4	13K

DC voltage characteristic at terminal X of proposed MRCCII+ is shown in Figure 5.1. The voltage V_X is plotted for input voltage V_Y , which is varied from -0.5V to 0.5V along the X-axis. The voltage V_X varies linearly with the input voltage for a range of ± 0.3V. The variation of input offset voltage in linear range is 0.021 to 0.027 V.

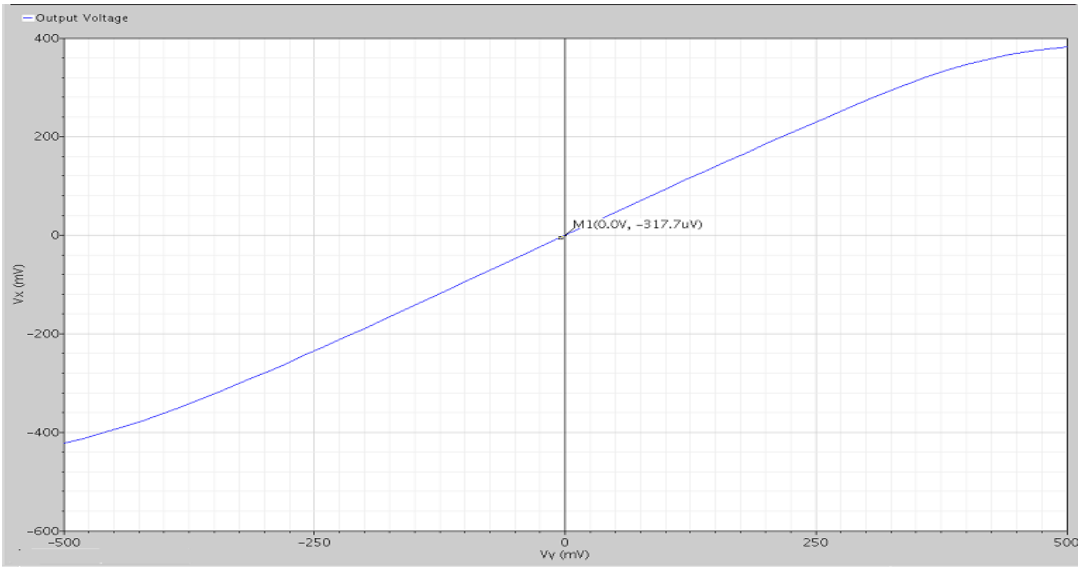

Figure 5.1 DC voltage characteristic of proposed MRCCII+

The frequency response of voltage transfer gain of proposed MRCCII+ is shown in Figure 5.2. The plot shows that the voltage transfer gain of proposed MRCCII+ remains constant till 1.16GHz.

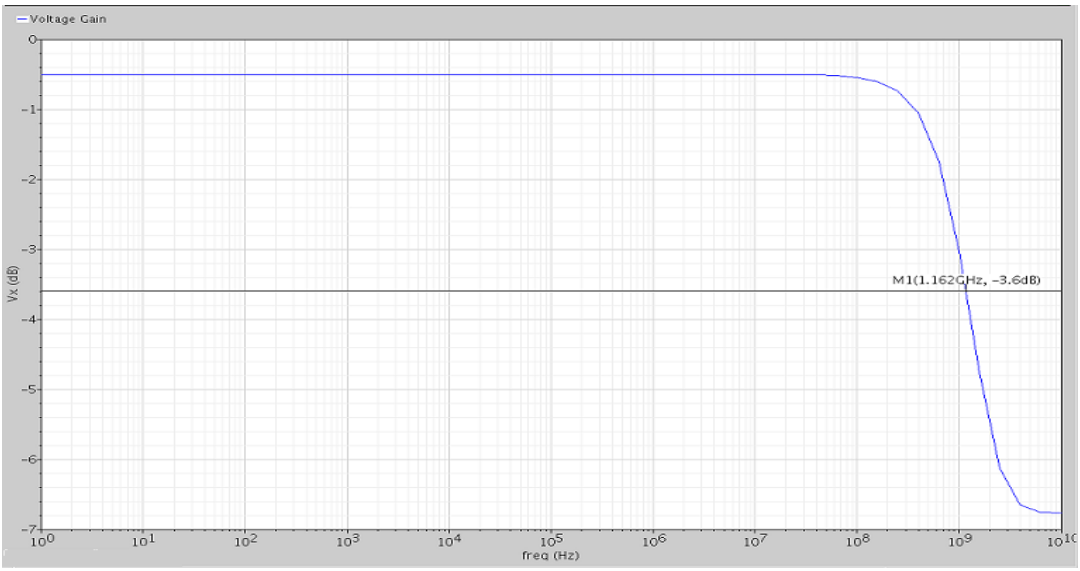

Figure 5.2 Frequency response of voltage transfer gain of proposed MRCCII+

The DC current characteristic at terminal Z for the proposed MRCCII+ is shown in Figure 5.3. The current at terminal Z (I_Z) is plotted for input current at terminal X (I_X) which is varied from -130µA to 130µA along the X-axis. The current I_Z varies linearly with the input current I_X for the entire range. The input current offset variation in the linear range is 0.9 µA to 2 µA.

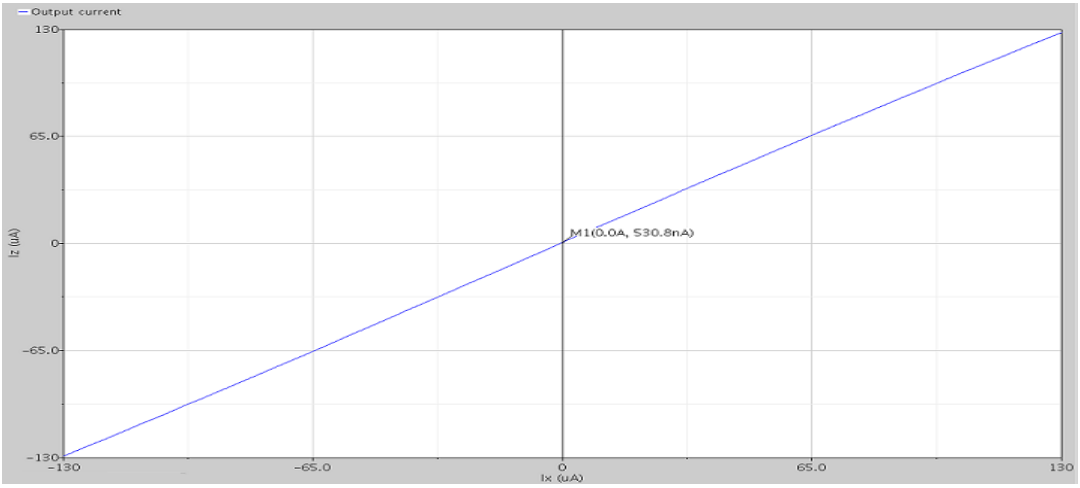

Figure 5.3 DC current characteristic of proposed MRCCII+

The frequency response of current transfer gain of proposed MRCCII+ is shown in Figure 5.4. The plot shows that the current transfer gain of proposed MRCCII+ remains constant till 419 MHz.

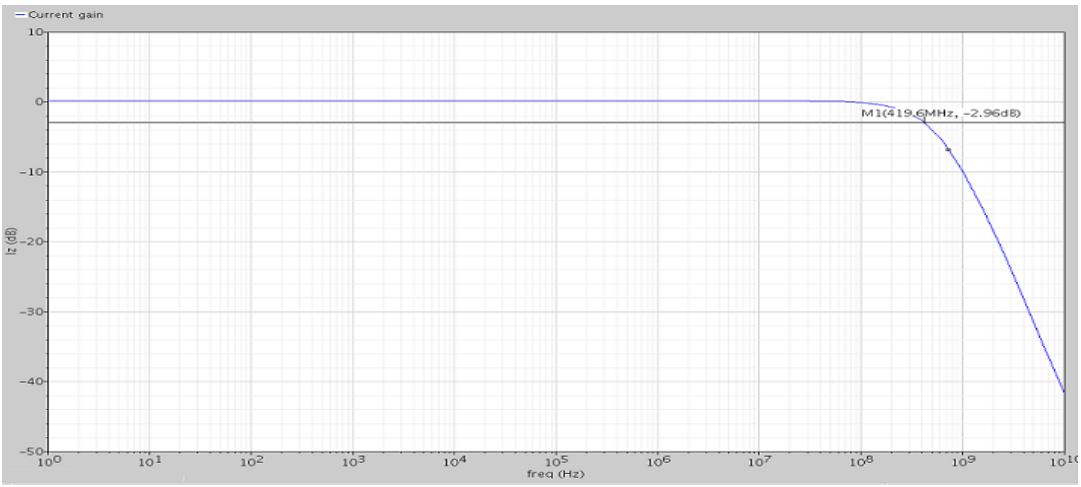

Figure 5.4 Frequency response of the current transfer gain of proposed MRCCII+

The variation of input resistance Z_X at terminal X as a function of DC reference current I_O of proposed MRCCII+ is shown in Figure 5.5.The DC reference current I_O is varied from 0µA to 100µA along the X-axis. From the plot it can be observed that at I_O= 50µA, the value of input resistance is 562Ω.

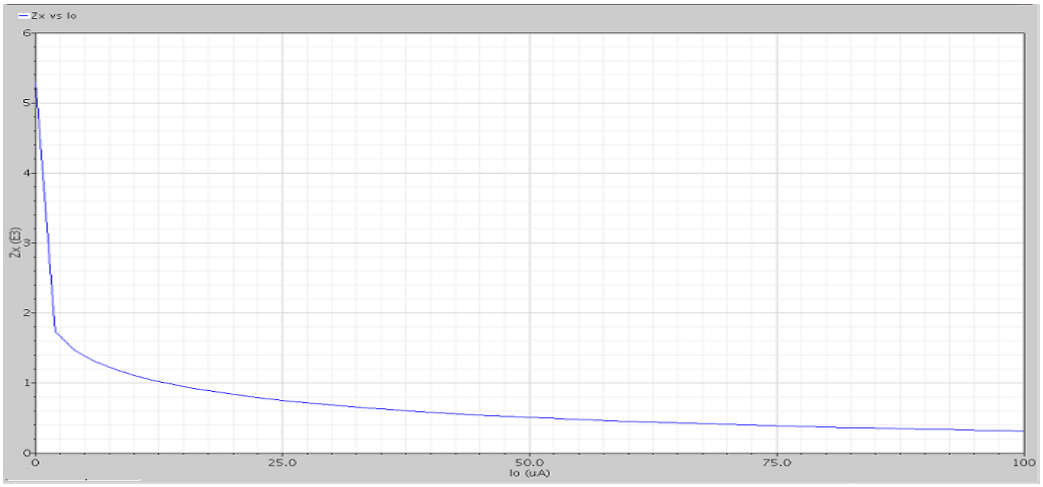

Figure 5.5 Variation of Z_X as a function of DC reference current I_O of proposed MRCCII+

Table 5.2 compares the proposed MRCCII+ with the existing current conveyors available in the literature.

Table 5.2 Comparison of proposed MRCCII+ circuit with CCII available in literature [28, 30, 33, 35, 36]

Parameters	[28]	[30]	[33]	[35]	[36]	Proposed MRCCII+
Supply Voltage (V)	±3.3	±1.5	2.5	±1.5	±0.5	±0.9
Technology (µm)	1.2	0.5	0.35	0.35	0.18	0.18
Bias Current (µA)	100	100	40	N.A	N.A	50
Power Consumption (mW)	N.A	1.5	N.A	N.A	0.0048	0.722
Input voltage range (V)	-3 to 2	-0.63 to 0.25	0.8 to1.6	-0.5 to 0.6	±0.150	±0.3
Voltage offset variation (V)	0.09 to 0.27	−0. 0058 to 0.00254	N.A	N.A	N.A	0.021 to 0.027

3-dB B/W (MHz) (V_X/V_Y)	222	1150	103	1050	70	1167
Voltage Gain	1	0.99385	0.972	0.95	0.989	0.943
Input Current range (µA)	±100	±100	0 to 200	-100 to 125	±40	±130
Current Offset variation (µA)	-0.3 to 0.2	−1.04 to −0.023	N.A	N.A	N.A	0.9 to 2
3-dB B/W (MHz) (I_Z/I_X)	110	76	200	10350	130	419
Current Gain	1.0015	1.0037	0.986	0.98	0.985	1.01
Rx(Ω)	0.003	5.9	4500	N.A	3.8K to 1.4M	562
Voltage THD (%) @Vpp@ MHz	N.A	0.0919 % @ 0.5 @0.1	0.091 % @ 0.1@ N.A	N.A	0.94 %@0.2@-	0.256 % @ 0.1 @0.1
Current THD (%) @I(µA)@ MHz	N.A	N.A	0.066% @100@ N.A	N.A	N.A	0.321 % @ 50@ 0.1

From the table it can be concluded that the proposed MRCCII+ circuit has the highest voltage transfer bandwidth, wide input current linear range and highest current gain among the current conveyors suggested in [28, 30, 33, 35, 36].

5.2.2 Simulation Results of The Proposed MOSFET-Only Voltage Divider Biased Positive Second Generation Current Conveyor (MOCCII+)

The proposed MOCCII+ has been simulated using UMC 0.18 µm CMOS process technology parameters. The transistors dimension of the proposed MOCCII+ are listed in Table 5.3.

Table 5.3 Transistor Dimensions of MOCCII+

MOSFETS	W(µm)/L(µm)
M_1-M_2	1.2/0.22
M_3	1.34/0.22
M_4-M_5	50/0.22
M_6	3/0.22
M_7	0.8/0.22
M_8-M_9	30/0.22
M_{10}-M_{11}	100/0.22
M_{12}	1/0.22
M_{13}-M_{14}	1/0.22
M_{15}-M_{16}	46/0.22
M_{17}	2/0.22
M_{18}	0.8/0.22
M_{19}	4/0.22

DC voltage characteristic at terminal X of proposed MOCCII+ is shown in Figure 5.6. The voltage V_X is plotted for input voltage V_Y , which is varied from -0.5V to 0.5V along the X-axis. The voltage V_X varies linearly with the input voltage for a range of ± 0.3V. The variation of input offset voltage in linear range is 0.019 to 0.023 V.

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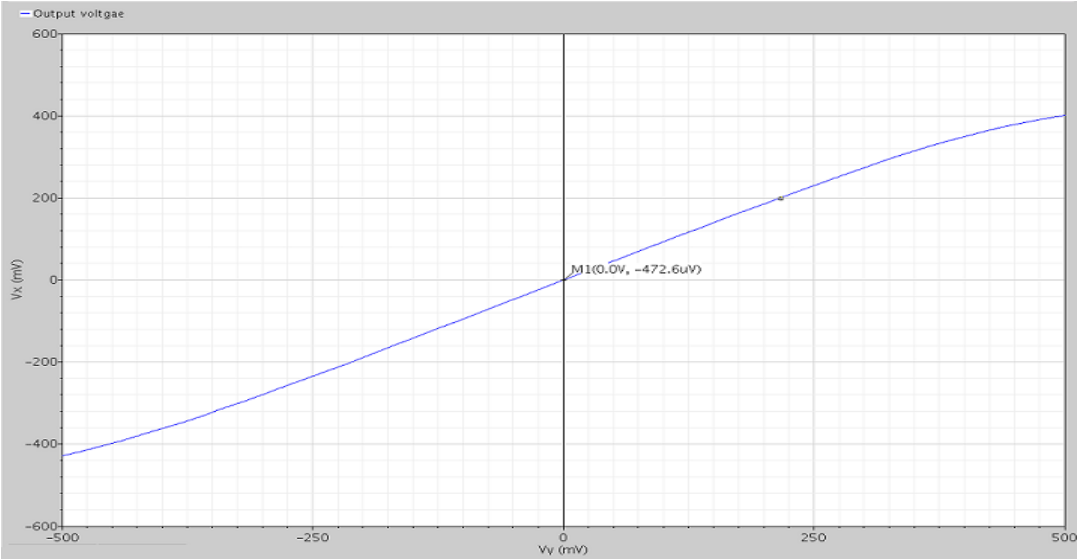

Figure 5.6 DC voltage characteristic of proposed MOCCII+

The frequency response of proposed MOCCII+ is shown in Figure 5.7. The plot shows that the voltage transfer gain of proposed MOCCII+ remains constant till 1.192GHz.

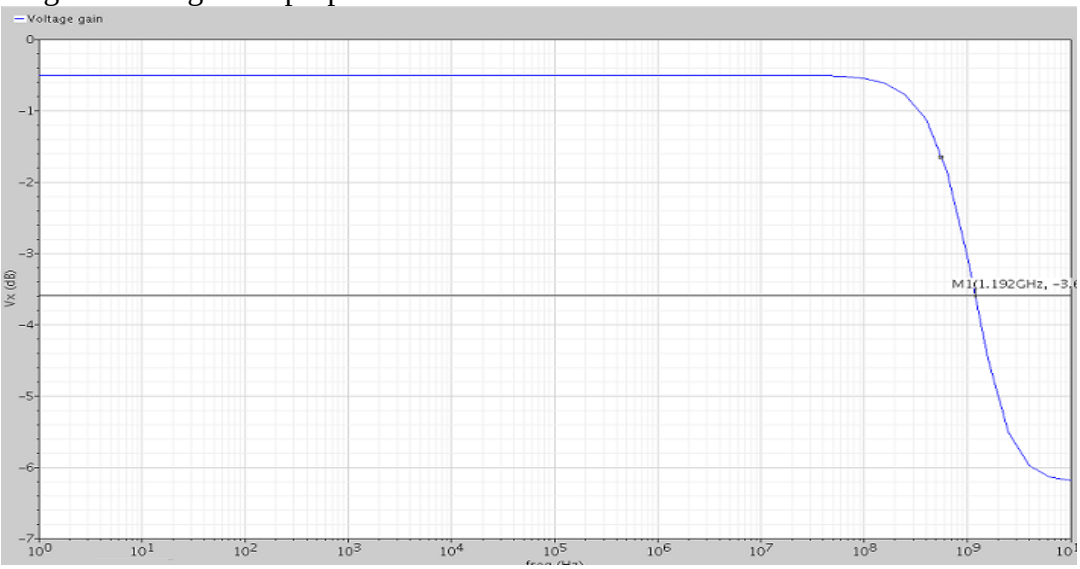

Figure 5.7 Frequency response of voltage transfer gain of proposed MOCCII+

The DC current characteristic at terminal Z for the proposed MOCCII+ is shown in Figure 5.8. The current at terminal Z (I_Z) is plotted for input current at terminal X (I_X) which is varied from -150µA to 150µA along the X-axis. The current I_Z varies linearly with the input current I_X for the entire range. The input current offset variation in the linear range is 0.8µA to -0.1 µA.

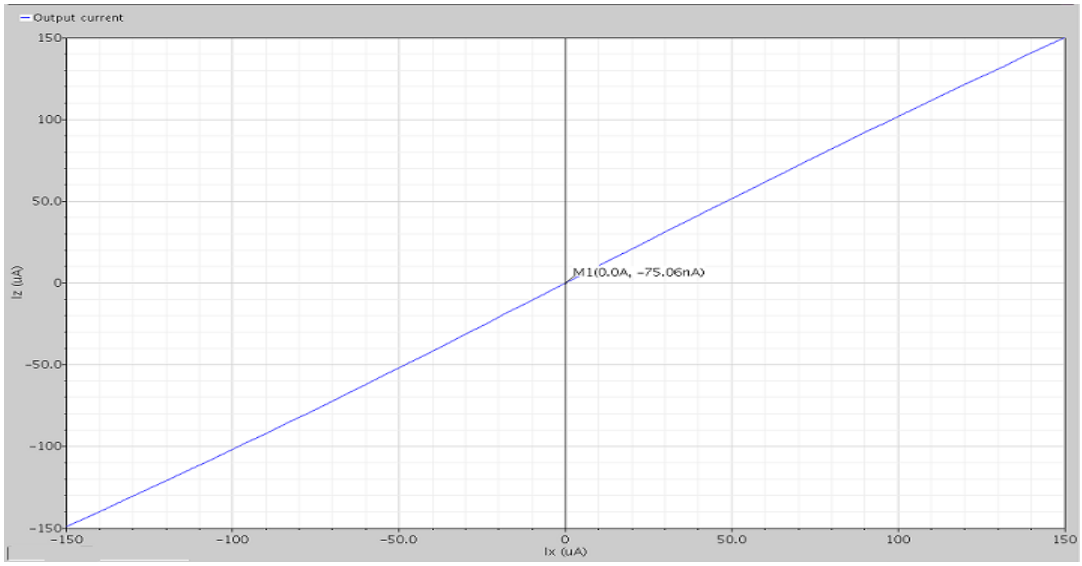

Figure 5.8 DC current characteristic of proposed MOCCII+.

The frequency response of current transfer gain of proposed MOCCII+ is shown in Figure 5.9. The plot shows that the current transfer gain of proposed MOCCII+ remains constant till 480 MHz.

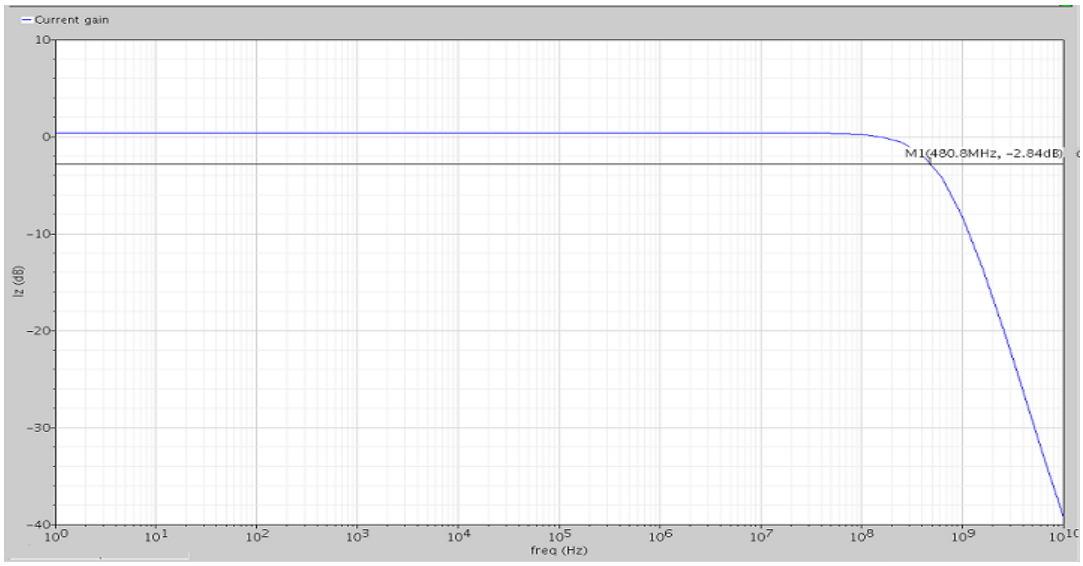

Figure 5.9 Frequency response of current transfer gain of proposed MOCCII+

The variation of input resistance Z_X at terminal X as a function of DC reference current I_O of proposed MOCCII+ is shown in Figure 5.10.The DC reference current I_O is varied from 0µA to 100µA along the X-axis. From the plot it can be observed that at I_O= 50µA, the value of input resistance is 566Ω.

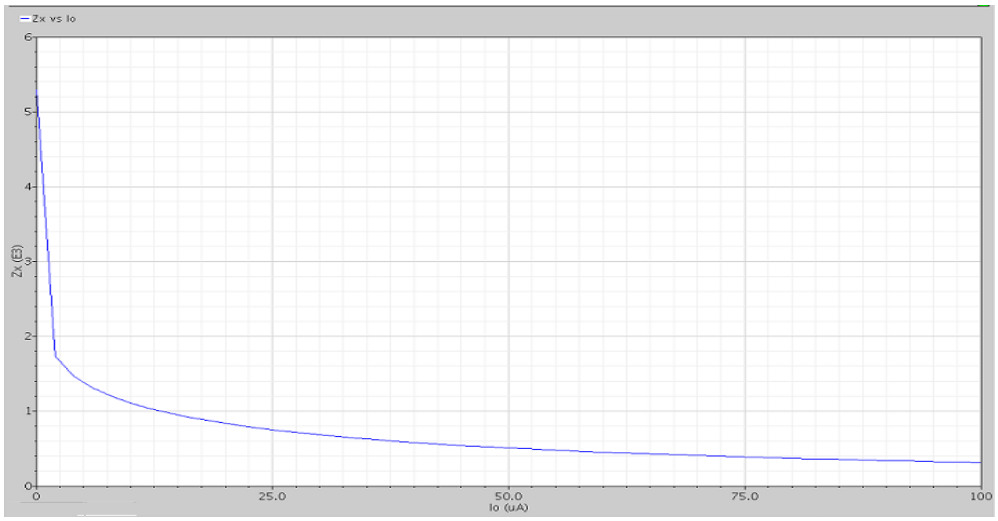

Figure 5.10 Variation of Z_X as function of DC reference current I_O of proposed MOCCII+

Comparison between the proposed MOCCII+ and MRCCII+ with the existing current conveyors available in the literature is presented in table 5.4.

Table 5.4 Comparison of proposed MOCCII+ and the CCII+ available in literature [28, 30, 33, 35, 36]

Parameters	[28]	[30]	[33]	[35]	[36]	Proposed MRCCII+	Proposed MOCCII+
Supply Voltage (V)	±3.3	±1.5	2.5	±1.5	±0.5	±0.9	±0.9
Technology (µm)	1.2	0.5	0.35	0.35	0.18	0.18	0.18
Bias Current (µA)	100	100	40	N.A	N.A	50	50
Power Consumption (mW)	N.A	1.5	N.A	N.A	0.0048	0.722	0.463
Input voltage range (V)	-3 to 2	-0.63 to 0.25	0.8 to1.6	-0.5 to 0.6	±0.150	±0.3	±0.3
Voltage offset variation (V)	0.09 to 0.27	−0. 0058 to 0.00254	N.A	N.A	N.A	0.021 to 0.027	0.019 to 0.023
3-dB B/W (MHz) (V_X/V_Y)	222	1150	103	1050	70	1167	1194
Voltage Gain	1	0.99385	0.972	0.95	0.989	0.943	0.943
Input Current range (µA)	±100	±100	0 to 200	-100 to 125	±40	±130	±150
Current Offset variation (µA)	-0.3 to 0.2	−1.04 to 0.023	N.A	N.A	N.A	0.9 to 2	0.8 to - 0.1
3-dB B/W (MHz) (I_Z/I_X)	110	76	200	10350	130	419	480
Current Gain	1.0015	1.0037	0.986	0.98	0.985	1.01	1.04
Rx(Ω)	0.003	5.9	4500	N.A	3.8K Ω to 1.4MΩ	562	566
Voltage THD (%) @Vpp(V)@ MHz	N.A	0.0919@ 0.5 @ 0.1	0.091@0.1 @ N.A	N.A	0.94 @ 0.2	0.256 % @ 0.1 @0.1	0.259 % @ 0.1 @ 0.1
Current THD (%) @I@ MHz	N.A	N.A	0.066% @100µA	N.A	N.A	0.321 % @ 50@ 0.1	0.160% @ 50 µA @0.1

From the table 5.4 it can be shown that the proposed MOCCII+ have highest voltage transfer bandwidth, wide input current linearity and highest current gain as compared to the other

conveyors suggested in the literature [28, 30, 33, 35, 36] and to the proposed MRCCII+. The proposed MOCCII+ dissipates less power as compared to the proposed MRCCII+.

5.2.3 Simulation Results of The Applications of Proposed MOCCII+

The simulation results of the applications such as current integrator, current differentiator and transconductance amplifier developed using the proposed MOCCII+ simulated using UMC 0.18 µm CMOS process technology parameters are presented.

5.2.3.1 Simulation Result of The Proposed Current Integrator Using MOCCII+

The output response of the current integrator developed as an application for the proposed MOCCII+ for values of C= 100pF and R= 3K is shown in Figure 5.11 when a input pulse of 100µA amplitude is applied. The triangular output response has amplitude of 100µA.

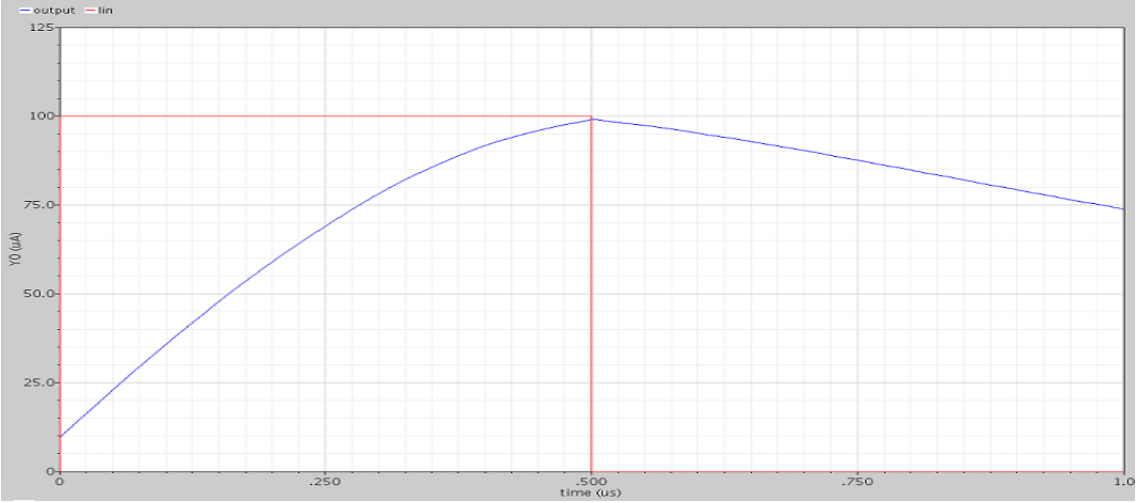

Figure 5.11 Proposed current integrator using MOCCII+ response

5.2.3.2 Simulation Result of The Proposed Current Differentiator Using MOCCII+

Simulation result of the current differentiator developed using proposed MOCCII+ is shown in Figure 5.12 for the values of R= 2.5KΩ and C=1pF when pulse excitation of amplitude ±100µA is applied. The impulse response of the excitation is having amplitude of ±100µA.

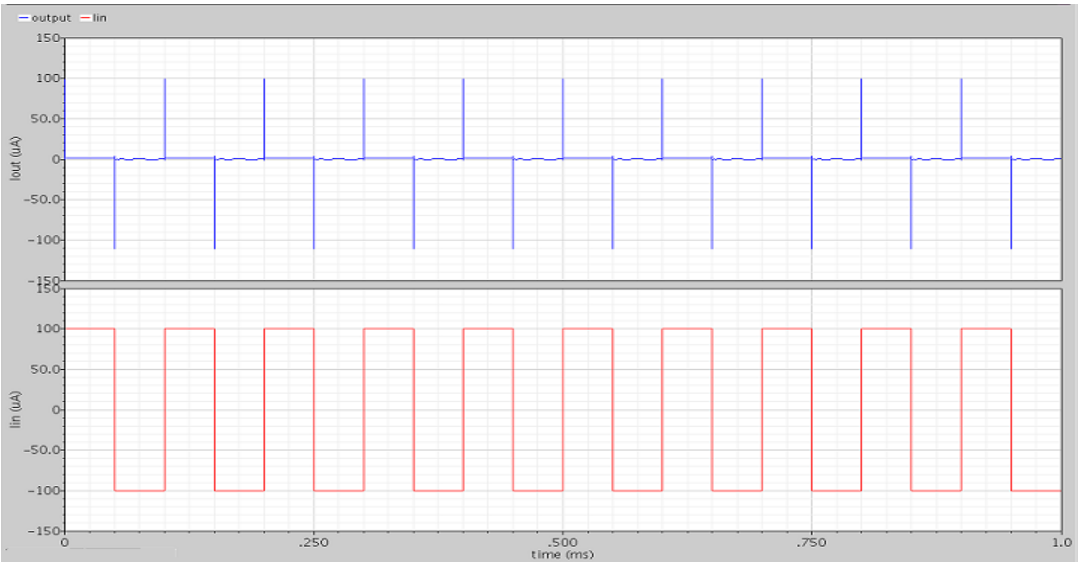

Figure 5.12 Proposed current differentiator using MOCCII+ response

5.2.3.3 Simulation Result of The Proposed Transcondutance Amplifier Using MOCCII+.

Simulation result of transconductance amplifier developed using proposed MOCCII+. Figure 5.13 shows the DC characteristic of the transconductance amplifier. The input voltage is varied from -0.5V to 0.5V along the X-axis. The output current at terminal Z varies linearly with the input voltage for a range of ± 0.250V.

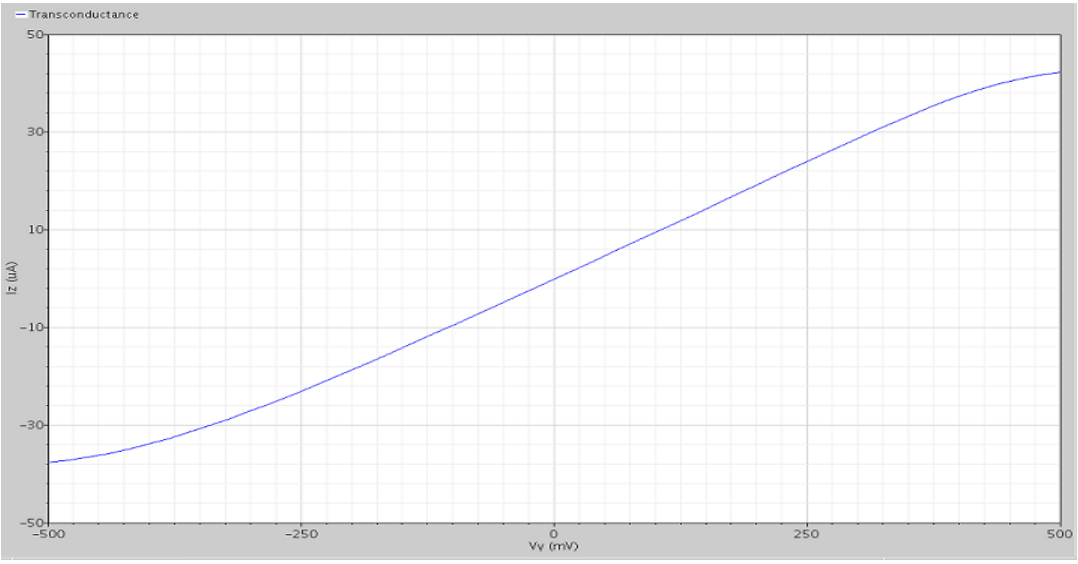

Figure5.13 Proposed transconductance amplifier using MOCCII+ response

5.3 Simulation Results of The Proposed High Frequency Low Voltage Current Feedback Operational Amplifier (HFLVCFOA)

Simulation results of the proposed high frequency low voltage current feedback operational amplifier (HFLVCFOA) circuits developed using proposed MRCCII+ and MOCCII+ circuits are presented. Simulation results of notch filter, frequency dependent negative resister (FDNR) and inductor developed as applications of the proposed HFLVCFOA-MO circuit are

also discussed.

5.3.1 Simulation Results of The Proposed High Frequency Low Voltage Current Feedback Operational Amplifier Based on Proposed MRCCII+ (HFLVCFOA-MR.)

The proposed HFLVCFOA-MR developed using proposed MRCCII+ has been simulated using UMC 0.18 µm CMOS process technology parameters. Table 5.5 lists the transistors dimension of the proposed HFLVCFOA-MR.

Table 5.5 Transistor dimensions of HFLVCFOA-MR.

MOSFETS	W(µm)/L(µm)
M_1-M_2	1.2/0.22
M_3	1.34/0.22
M_4-M_5	92/0.22
M_6	2/0.22
M_7	1.58/0.22
M_8-M_9	30/0.22
M_{10}-M_{11}	100/0.22
M_{13}-M_{14}	1/0.22
M_{15}-M_{16}	60/0.22
M_{17}	7.9/0.22
M_{18}	4.5/0.22
R_2	0.5K
R_4	13K
M_{19}	10/0.22
M_{20}-M_{21}	30/0.22
M_{22}-M_{23}	50/0.22
M_{24}	11/0.22

The DC current characteristic at terminal Z for the proposed HFLVCFOA-MR is shown in Figure 5.14. The current at terminal Z (I_Z) is plotted for input current at terminal X (I_X) which is varied from -130µA to 130µA along the X-axis. The current I_Z varies linearly with the input current I_X for the entire range.

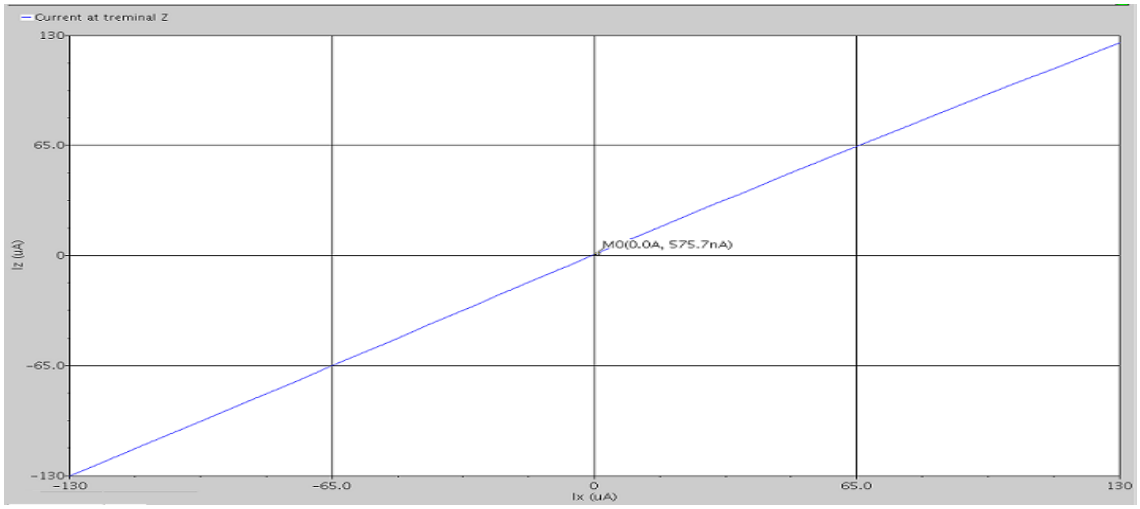

Figure 5.14 DC current characteristic of proposed HFLVCFOA-MR

Figure 5.15 shows the effect on the closed loop voltage gain when value of resistor R_1 is varied.

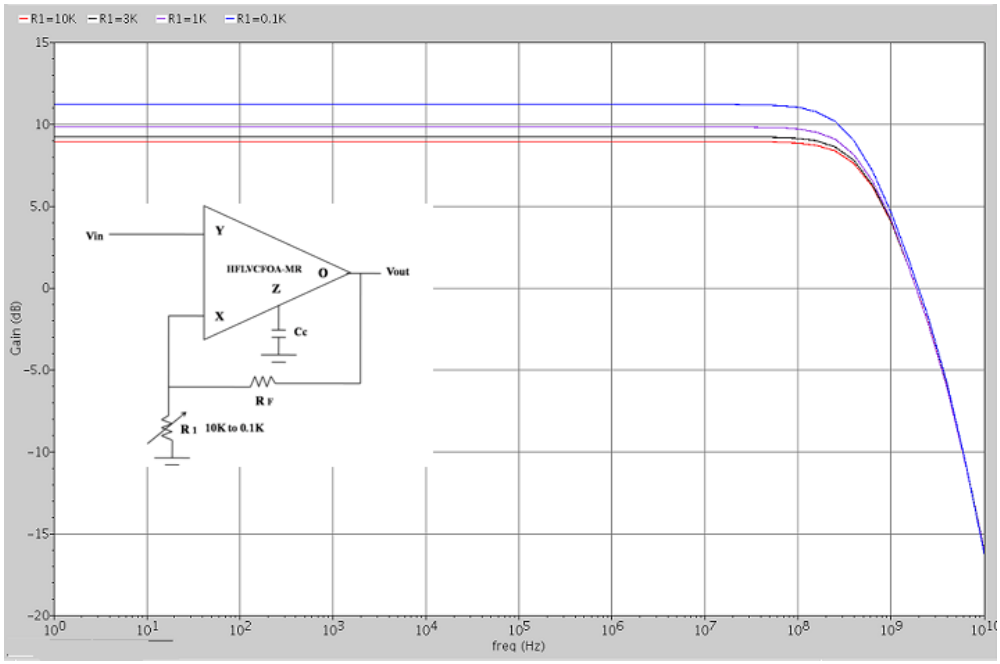

Figure 5.15 Closed loop frequency response for different values of R_1

Table 5.6 shows the effect on the performance parameters like closed loop voltage gain (Av), gain bandwidth product (GBW), phase margin (PM) and total harmonic distortion (THD) when the value of the resistor R_1 is varied and value of C_c = 0.5pF and R_F = 10KΩ.

Table 5.6 Performance parameters of proposed HFLVCFOA-MR with variation in feedback resistor

Feedback Resistor R_1 (KΩ)	A_V (dB)	GBW(GHz)	PM(Deg)	THD(dB)
10	8.93	1.9	110.5	-52.21
3	9.246	1.85	110.2	-51.37
1	9.83	1.82	109.45	-50.04

0.1	11.21	1.79	105.65	-45.99

From the plots shown in Figure 5.15 for different values of resistor R_1 and table 5.6, it is observed that as the closed loop voltage gain increases, the gain bandwidth (GBW) product remains nearly constant.

Table 5.7 compares the performance parameters of the proposed CFOA with the other CFOA available in literature.

Table 5.7 Comparison of proposed HFLVCFOA-MR with the existing CFOA available in literature.

Parameters	[41]	[42]	[8]	Proposed HFLVCFOA-MR
Supply Voltage (V)	±3.3	±0.75	±2.5	±0.9
Technology(µm)	0.35	0.25	0.35	0.18µm
Power Consumption(mW)	5.3	0.456	5.5	2.05
Input voltage range(V)	N.A	±0.65	±1	±0.3V
Input offset Voltage(mV)	1.3	<20	0.2	-0.288
GBW(MHz)	58	120	104	1900
Phase Margin(Degree)	57.5	68	NA	110.5
DC gain(dB)	74	NA	67	11.33
Input Current range(µA)	NA	±1000	NA	±130
THD @V@ MHz (dB)	-52 @ 0.2V p-p @ 5Mhz	NA	-67	-52.21

From Table 5.7 it is observed that, the proposed HFLVCFOA-MR has high gain bandwidth product and phase margin than the existing CFOAs available in the literature [41, 42, 8]. The proposed HFLVCFOA-MR also has less power consumption than some of the existing CFOAs available in the literature [41, 8].

5.3.2 Simulation Results of The Proposed High Frequency Low Voltage Current Feedback Operational Amplifier Based on Proposed MOCCII+ (HFLVCFOA-MO)

The proposed HFLVCFOA-MO developed using proposed MOCCII+ has been simulated using UMC 0.18 µm CMOS process technology parameters. Table 5.8 lists the transistors dimension of the proposed CFOA.

Table 5.8 Transistor dimension HFLVCFOA-MO

MOSFETS	W(µm)/L(µm)
M_1-M_2	1.2/0.22
M_3	1.34/0.22
M_4-M_5	50/0.22
M_6	3/0.22

M_7	0.8/0.22
M_8-M_9	30/0.22
M_{10}-M_{11}	100/0.22
M_{12}	1/0.22
M_{13}-M_{14}	1/0.22
M_{15}-M_{16}	46/0.22
M_{17}	1.3/0.22
M_{18}	0.8/0.22
M_{19}	4/0.22
M_{20}	11/0.22
M_{21}-M_{22}	45/0.22
M_{23}-M_{24}	100/0.22
M_{25}	10/0.22

The DC current characteristic at terminal Z for the proposed HFLVCFOA-MO is shown in Figure 5.16. The current at terminal Z (I_Z) is plotted for input current at terminal X (I_X) which is varied from -150µA to 150µA along the X-axis. The current I_Z varies linearly with the input current I_X for the entire range.

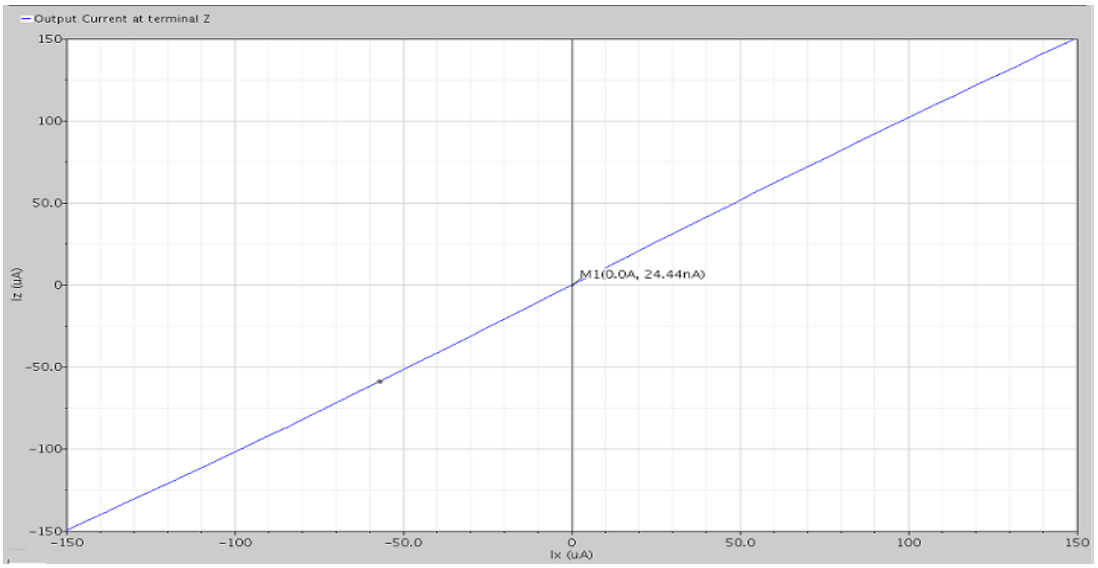

Figure 5.16 DC current characteristic of proposed HFLVCFOA-MO.

Figure 5.17 shows the effect on the closed loop voltage gain when value of resistor R_1 is varied.

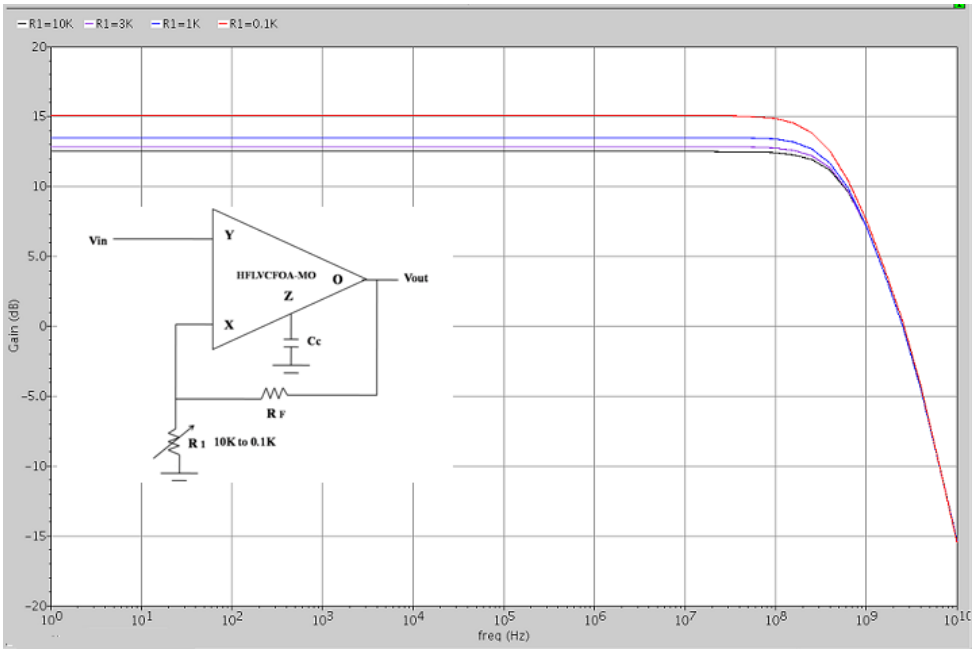

Figure 5.17 Closed loop frequency response for different values of R_1

Table 5.9 shows the effect on the performance parameters like closed loop voltage gain (Av), gain bandwidth product (GBW), phase margin (PM) and total harmonic distortion (THD) when the feedback resistor R_1 is varied and C_c = 0.5pF and R_F = 10KΩ.

Table 5.9 Performance parameters of proposed HFLVCFOA-MO with variation in feedback resistor

Feedback Resistor R_1 (KΩ)	A_V (dB)	GBW(GHz)	PM(Deg)	THD(dB)
10	12.51	2.72	94.5	-59.25
3	12.86	2.66	94	-59.09
1	13.53	2.61	93.29	-56.47
0.1	15.09	2.56	90.57	-49.84

From the plots shown in Figure 5.17 for different values of resistor R_1 and table 5.9, it is observed that as the closed loop voltage gain increases, the gain bandwidth product remains nearly constant.

Table 5.10 compares the performance parameters of the proposed HFLVCFOA-MO with proposed HFLVCFOA-MR and other CFOAs available in literature.

Table 5.10 Comparison of proposed HFLVCFOA-MO with the existing CFOA available in literature.

Parameters	[41]	[42]	[8]	Proposed HFLVCFOA-MR	Proposed HFLVCFOA-MO
Supply Voltage (V)	±3.3	±0.75	±2.5	±0.9	±0.9
Technology(µm)	0.35	0.25	0.35	0.18	0.18
Power Consumption(mW)	5.3	0.456	5.5	2.05	1.947
Input voltage range(V)	NA	±0.65	±1	±0.3	±0.3
Input offset Voltage(mV)	1.3	<20	0.2	-0.288	-0.426

GBW(MHz)	58	120	104	1900	2720
Phase Margin(Degree)	57.5	68	NA	110.5	94.51
DC gain(dB)	74	NA	67	11.33	15.56
Input Current range(µA)	NA	±1000	NA	±130	±150
THD @V@ MHz (dB)	-52 @ 0.2V p-p @ 5Mhz	NA	-67	-52.21	-59.25

From Table 5.10 it is observed that, the proposed HFLVCFOA-MO has the highest gain bandwidth product than the existing CFOAs available in the literature [41, 42, 8] and the proposed HFLVCFOA-MR. The proposed HFLVCFOA-MO also has less power consumption than some of the existing CFOAs available in the literature [41, 8] and proposed HFLVCFOA-MR.

5.3.3 Simulation Results of The Applications Based on Proposed HFLVCFOA-MO

The simulation results of the applications such as notch filter, frequency dependent negative resistor (FDNR) and inductor circuits developed using the proposed HFLVCFOA-MO simulated using UMC 0.18 µm CMOS process technology parameters are presented.

5.3.3.1 Proposed HFLVCFOA-MO Based Notch Filter

The frequency response of notch filter developed using proposed HFLVCFOA-MO is shown in Figure 5.18 for the values of R= 1KΩ, C= 300fF, R_1= 600Ω and k=0.9. The simulated frequency is f_0 = 250 MHz.

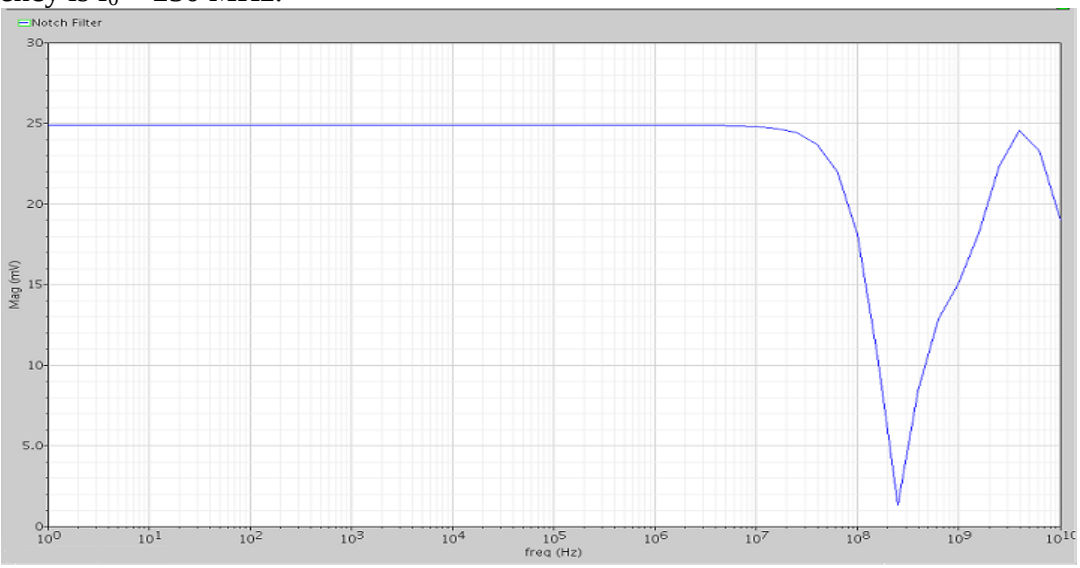

Figure 5.18 Frequency response of proposed HFLVCFOA-MO based notch filter

5.3.3.2 Proposed HFLVCFOA-MO Based Inductor

The simulation result of the inductor developed using the proposed HFLVCFOA-MO is shown in Figure 5.19 for the values of a=0.5, $R_1 = R_2 = R/2$, R=6KΩ, C_1 = 100nF and C_2 = 30nF. The plot in Figure 5.19 the shows the linear variation of the impedance of inductor with the frequency.

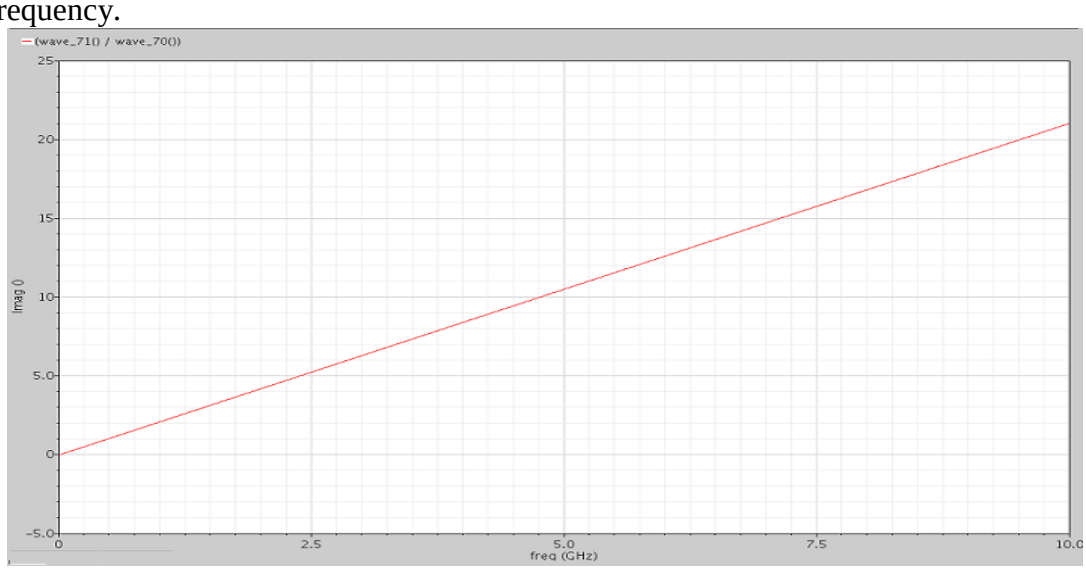

Figure 5.19 Frequency response of proposed HFLVCFOA-MO based inductor

5.3.3.3 Proposed HFLVCFOA-MO Based Frequency Dependent Negative Resistor (FDNR)

The simulation results of the frequency dependent negative resistor (FDNR) developed using the proposed HFLVCFOA-MO are shown in Figure 5.20 for the values of R=15KΩ, C1=5fF, C2= 2fF, R1= 20Ω and a = 0.5.

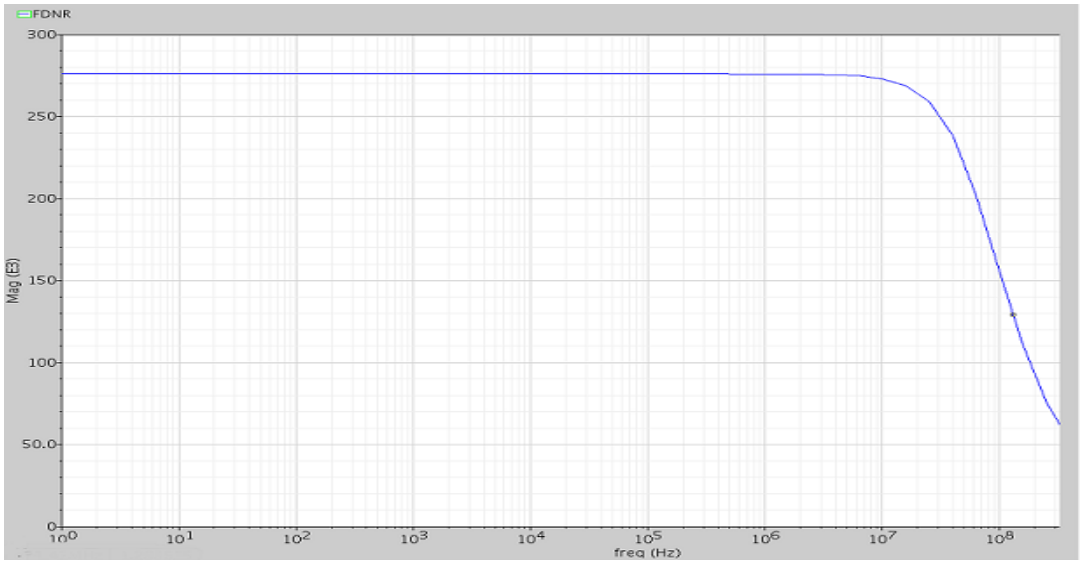

Figure 5.20 Frequency response of proposed HFLVCFOA-MO based FDNR

5.4 Layout of The Proposed High Frequency Low Voltage Current Feedback Operational Amplifier Developed Using Proposed MOCCII+ (HFLVCFOA-MO)

The physical layout of proposed HFLVCFOA-MO has been designed using UMC 0.18µm CMOS process technology in Cadence Virtuoso XL layout editor. Design Rule Check (DRC) is performed in order to verify that layout fulfills all electrical and geometric rules provided by foundry. The basic design rules are:

Metal 1 to metal 1 spacing	0.24µm
Minimum contact size	0.24µm * 0.24µm
Poly to poly spacing	0.24µm
Poly to metal spacing	0.28µm
Contact overlap to p+ diffusion	0.1µm
Metal 1 width	0.24µm
Poly extension beyond active	0.22µm
Minimum contact spacing	0.26µm
N well overlap p+ diffusion	0.43µm
Diffusion contact to poly spacing	0.15µm
Minimum p+ implant overlap p+ diffusion	0.22µm
Poly width	0.18µm
Minimum poly extension on to field region	0.22µm
Poly contact to diffusion edge spacing	0.18µm
Minimum poly overlap contact	0.1µm
Minimum metal area	$0.1764\mu m^2$
Minimum metal2 width	0.28µm
Metal1 and metal2 overlap over via	0.08µm

The layout of proposed HFLVCFOA-MO is shown in Figure 5.21.

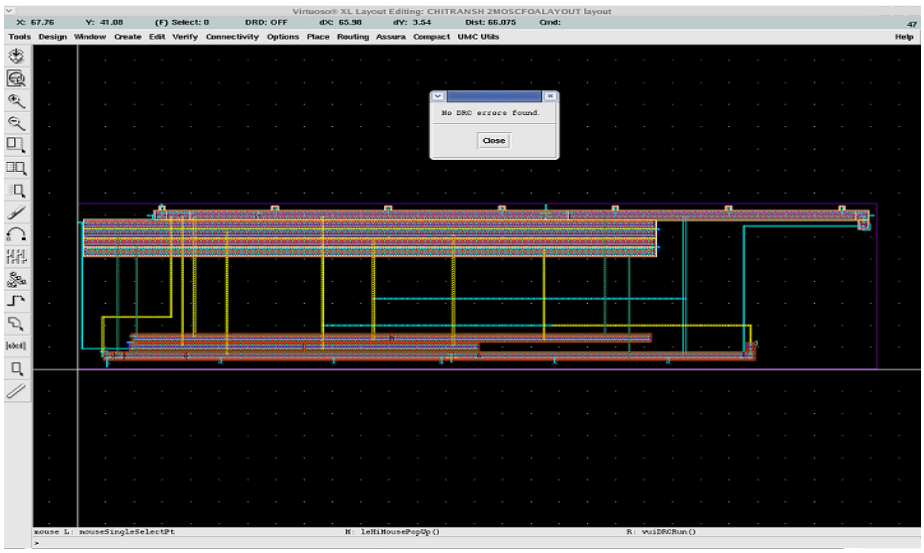

Figure 5.21 Layout of the proposed HFLVCFOA-MO

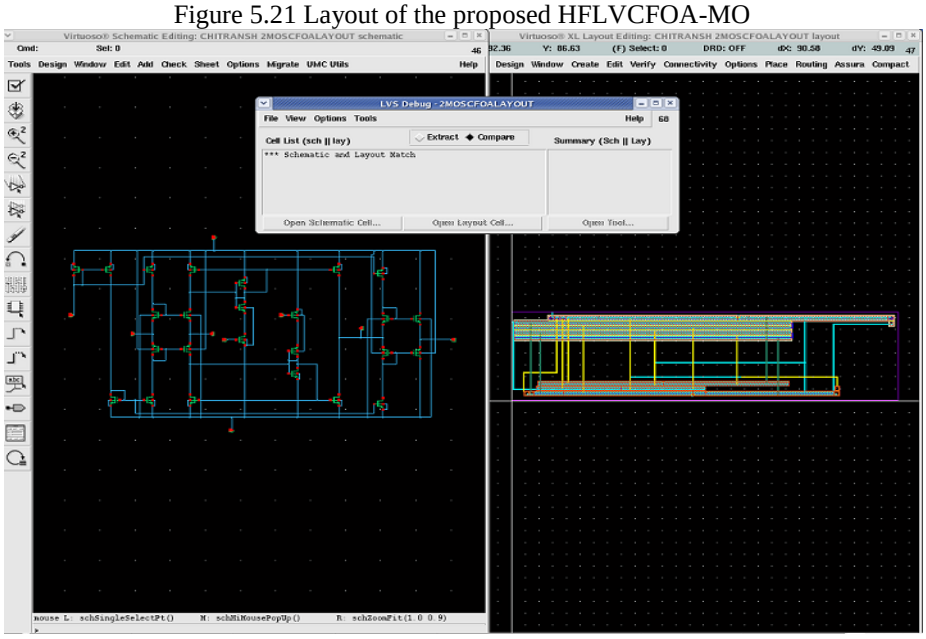

Figure 5.22 Layout vs Schematic of proposed HFLVCFOA-MO

The Layout vs. Schematic (LVS) analysis of proposed HFLVCFOA-MO has also performed in order to match the layout with the schematic and is shown in Figure 5.22. The LVS report is shown in Appendix B.

5.5 Conclusions

The proposed voltage divider biased current conveyor circuits and high frequency low voltage CMOS current feedback operational amplifier along with their applications have been simulated using the UMC 0.18µm CMOS process technology parameters and the simulation results are presented. The proposed HFLVCFOA-MO has the high gain bandwidth product

among the various CFOAs available in literature. The layout of the proposed CFOA is also presented.

CHAPTER

6

CONCLUSIONS AND FUTURE SCOPE

6.1 Conclusions

The current-mode circuits offer some advantages over voltage-mode circuits like high speed, low power consumption, simple schematics. An important current-mode block is current feedback operational amplifier (CFOA) which removes the limitation of voltage feedback operational amplifiers (VFOA) of having constant gain-bandwidth product. CFOAs are developed from a versatile current-mode block called as current conveyor (CC) as it has unity gain, high linearity and better frequency performance.

In this dissertation, high frequency low voltage CMOS current feedback operational amplifiers (HFLVCFOA) are developed using the proposed positive second generation current conveyors (CCII+). Positive second generation current conveyor circuits were developed with the help of MOSFET-resistor voltage divider and MOSFET-only voltage divider circuits. The proposed circuits have been simulated using the UMC 0.18µm CMOS process technology parameters. The CFOA circuits have been developed by cascading the proposed CCII+ and a voltage buffer stage. The voltage buffer stage is based on mixed trans-linear loop circuit. The proposed HFLVCFOA-MO circuit have been compared with the existing circuits available in the literature and it has been observed that the circuits has high gain bandwidth product (GBW) of 2.72 GHz and phase margin (PM) of 94.5^0. Analog building blocks such as notch filter, frequency dependent negative resistor and inductor circuits are also developed as applications of the proposed HFLVCFOA-MO and simulated. The physical layout of the proposed HFLVCFOA-MO is designed in Cadence Virtuoso XL layout editor using UMC 0.18µm CMOS process technology. Design Rule Check (DRC) and Layout vs. Schematic (LVS) analysis are performed.

6.2 Future scope

Some ideas and suggestions for the future work.

- The current transfer bandwidth of the current feedback operational amplifier can be increased by using bandwidth extension techniques like resistor peaking.
- The input impedance (Z_X) of the current conveyor can be decreased by using push-pull output stage.

REFERENCES

[1] C. Toumazou, F. J. Lidgey and D. G. Haigh, "Analogue IC Design: The Current-mode Approach," *Peter Peregrinus Ltd*, 1990.

[2] K. Koli and K. Haloen, "CMOS current amplifiers speed versus linearity," *London Kluwer Academic Publishers*, 2003.

[3] F. Yuan, "CMOS current-mode circuits for data communications," *Springer*, 2007.

[4] G.Ferri and N.C. Guerrini, "Low-Voltage Low-Power CMOS Current Conveyors," *Kluwer Academic Publishers*, 2003.

[5] S.I. Long and J.Q. Zhang, "Low power GaAs current-mode 1.2 Gb/s interchip interconnections," *IEEE Journal Solid-State Circuits,* vol. 32, pp.890-897, June 1997.

[6] A.H. Madian, S.A. Mahmoud and A.M. Soliman, "New 1.5-V CMOS Current Feedback Operational Amplifier," *IEEE 13th International Conference on Electronics, Circuits and Systems,* pp.600-603, 2006.

[7] T. Kaulberg, "A CMOS current-mode operational amplifier," *IEEE journal of Solid-State Circuits*, vol. 28, no. 7, July 1993.

[8] H. Jassim, "A New Design Technique of CMOS Current Feed Back Operational Amplifier (CFOA)," *Circuits and Systems*, vol. 4, no. 1, pp. 11-15, 2013.

[9] G.W. Roberts and A.S. Sedra, "All current-mode frequency selective circuits," Electronic Letters, vol. 25, no. 12, pp. 759-761, June 1989.

[10] R. Mancini, " Op-Amp for everyone," *Texas Instruments*, September 2001.

[11] S.A. Mahmoud, H.O. Elwan and A.M. Soliman, "Low voltage rail to rail CMOS current feedback operational amplifier and its applications for analog VLSI," *Analog Integrated Circuits and Signal Processing*, vol.25, no.1, pp.47-57, 2000.

[12] A.H. Madian, S.A. Mahmoud and A.M. Soliman, "Configurable analog block based on CFOA and its application," *WSEAS Transactions on Electronics*, vol. 5, no. 6,pp. 220-225, 2008.

[13] K.C. Smith and A.S. Sedra, "The current conveyor—A new circuit building block," *IEEE proceedings*, vol. 56, no. 8, pp. 1368-1369, August 1968.

[14] A.S. Sedra, G.W. Roberts and F. Gohh, "The current conveyor: history, progress and new results," *IEE Proceedings of Cirucits, Device and Systems*, vol. 137, no. 2, April 1990.

[15] A.M. Ismail and A.M. Soliman, "Novel CMOS current conveyor realizations suitable for high-frequency applications," Microelectronics journal, vol. 30, no. 12, pp. 1231–1239, December 1999.

[16] A.S. Sedra and K.C. Smith, "A second-generation current conveyor and its applications." *IEEE Transactions on Circuit Theory*, vol. 17, no. 1, pp. 132-134, 1970.

[17] A. Fabre, "Third-generation current conveyor: a new helpful active element," Electronics Letters, vol. 31, pp. 338-339, March 1995.

[18] S.Wolfer, D.T. Comer and D.J. Comer, "A high speed, precision voltage buffer in a submicron CMOS process," *International journal of electronics*, vol. 87, no. 1, pp. 1443-1452, 2000.

[19] R.G. Carvajal, J. Ramírez-Angulo, A.J. López-Martín, A. Torralba, J.A.G. Galán, A. Carlosena and F. M. Chavero, "The flipped voltage follower: A useful cell for low-voltage low-power circuit design," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 52, no. 7, pp. 1276-1291, July 2005.

[20] M. T. Abuelma'atti, "New grounded immittance function simulators using single current feedback operational amplifier," *Analog Integrated Circuits and Signal Processing*, vol. 71, no. 1, pp. 95-100, April 2012.

[21] S. Kilinc and U. Cam, "Current-mode oscillator configuration using single current operational amplifier," *3rd International Conference on Electrical and Electronics Engineering*, pp.107-111, December 2003.

[22] M.T.A.A.S. M. Al-shahrani, "Novel CFOA-based sinusoidal oscillators," *International journal of electronics,* vol. 85, no.4, pp. 437-441, 1998.

[23] A.M. Soliman, "Applications of the current feedback operational amplifiers," *Analog Integrated Circuits and Signal Processing,* vol. 11, no. 3, pp. 265-302, 1996.

[24] A.K.M.S. Haque, M.M. Hossain, W.A. Davis and H.T. Russell, "Design of sinusoidal, triangular, and square wave generator using current feedback operational amplifier (CFOA)," IEEE in region 5 Conference, pp. 1-5, 2008.

[25] M.T.A.A.S.M. Al-shahrani, "New CFOA-based triangular/square wave generator," *International journal of electronics,* vol. 84, no. 6, pp. 583-588, 1998.

[26] A.M. Soliman, "Current feedback operational amplifier based oscillators," *Analog Integrated Circuits and Signal Processing,* vol. 23, no. 1, pp. 45-55, 2000.

[27] H.O. Elwan and A.M. Soliman, "Low-voltage low-power CMOS current conveyors," *IEEE transaction on Circuits and Systems I: Fundamental Theory and Applications,* vol. 44, no. 9, September 1997.

[28] I.A. Awad and A.M. Soliman, "New CMOS realization of the CCII," *IEEE Transactions on Circuits and Systems II: Analog and Digital Signal Processing*, vol. 46, no. 4, April 1999.

[29] B. Calvo, S. Celma, P.A. Martinez and M.T. Sanz, "High speed high precision CMOS current conveyor," *Analog Integrated Circuits and Signal Processing,* vol.34, no. 3, pp.265-269, March 2003.

[30] W.S. Hassanein, I.A. Awad and A.M. Soliman, "New wide band low power CMOS current conveyors," *Analog Integrated Circuits and Signal Processing,* vol. 40, no. 1, pp. 91-97, July 2004.

[31] W.S. Hassanein, I.A. Awad and A.M. Soliman, "New high accuracy CMOS current conveyors," *AEU-International Journal of Electronics and Communications,* vol. 59. no. 7, pp.384-391, November 2005.

[32] S.B. Salem, M. Fakhfakh, D.S. Masmoudi, M. Loulou, P.Loumeau and N. Masmoudi, "A high performances CMOS CCII and high frequency applications," *Analog Integrated Circuits and Signal Processing,* vol. 49, no. 1, pp. 71-78, 2006.

[33] H. Barthélemy, M. Fillaud, S. Bourdel and J.Gaubert, "CMOS inverters based positive type second generation current conveyor," *Analog Integrated Circuits and Signal Processing,* vol. 50, no. 2, pp. 141-146, 2007.

[34] E. Arslan, A. Morgul, "Wideband self-biased CMOS CCII," *IEEE Research in Microelectronics and Electronics, Ph.D, pp. 217-220, 2008.*

[35] F. Kacar, B. Metin and H. Kuntman, "A new CMOS dual-X second generation current

conveyor (DXCCII) with an FDNR circuit application," *AEU-International Journal of Electronics and Communications, vol. 64, no. 8, pp. 774-778, August 2010.*

[36] H.Ercan, S.A. Tekin and M.Alçı, "Low-voltage low-power multifunction current-controlled conveyor." *International Journal of Electronics,* pp. 1-18, 2014.

[37] A.M Ismail and A.M. Soliman, "Novel CMOS current feedback op-amp realization suitable for high frequency applications," *IEEE Transactions on Circuits and Systems I: Fundamental Theory and Applications,* vol. 47, no. 6, pp. 918-921, 2000.

[38] B. Maundy, P.B. Aronhime and S. Gift, "A new configuration for current feedback operational amplifiers," *IEEE 45th Midwest Symposium on Circuits and Systems*, vol. 1, pp. 547-550, 2002.

[39] M. Djebbi, A. Assi and M. Sawan, "An offset-compensated wide-bandwidth CMOS current-feedback operational amplifier," *IEEE Canadian Conference on Electrical and Computer Engineering*, vol. 1, pp. 73-76, 2003.

[40] R. Mita, G. Palumbo and S. Pennisi, "Low-voltage high-drive CMOS current feedback op-amp," *IEEE Transactions on Circuits and Systems Part 2: Express Briefs*, vol. 52, no.6, pp. 317-321, 2005.

[41] S. Pennisi, "High-performance CMOS current feedback operational amplifier," *IEEE International Symposium on Circuits and Systems*, pp. 1573-1576, 2005.

[42] S.A. Mahmoud, A.H. Madian, and A.M. Soliman, "Low-voltage CMOS current feedback operational amplifier and its application," *ETRI journal*, vol. 29, no. 2, pp. 212-218, 2007.

[43] E. Yuce and S. Minaei, "A modified CFOA and its applications to simulated inductors, capacitance multipliers, and analog filters," *IEEE Transactions on Circuits and Systems I: Regular Papers,* vol. 55, no. 1, pp. 266-275, 2008.

[44] N. Hassen, T. Ettaghzouti and K. Besbes, "High performance second generation controlled current conveyor CCCII and high frequency applications," *World Academy of Science, Engineering and Technology,* vol. 60, pp. 1361-1370, 2011.

[45] R.J. Baker, H.W. Li and D.E. Boyce, "CMOS circuit design, layout and simulation," *New York, IEEE press*, 1998.

[46] S.B. Salem, A. Fakhfakh, M. Loulou, P. Loumeau and N. Masmoudi, "A 2.5 V 0.35 μm CMOS current conveyor and high frequency high-Q band-pass filter," *IEEE proceedings 16th International Conference on Microelectronics*, pp. 328-333, 2004.

APPENDIX A

MODEL PARAMETERS

The UMC 0.18μm CMOS technology model file is listed below:

```
model n_18_mm bsim3v3 type=n
+ version=3.2000e+00        binunit=1.0000e+00     mobmod=1.0000e+00
+ capmod=2.0000e+00         nqsmod=0.0000e+00
+ tox=4.2000e-09 + dtox_n_18_mm                      toxm=4.2000e-09
+ xj=1.6000e-07             nch=3.7446e+17           rsh=8.0000e+00
+ ngate=1.0000e+23          vth0=3.0750e-01 + dvth0_n_18_mm
+ k1=4.5780e-01             k2=-2.6380e-02           k3=-1.0880e+01
+ k3b=2.3790e-01            w0=-8.8130e-08           nlx=4.2790e-07
+ dvt0=4.0420e-01           dvt1=3.2370e-01         dvt2=-8.6020e-01
+ dvt0w=3.8300e-01          dvt1w=6.0000e+05       dvt2w=-2.5000e-02
+ lint=1.5870e-08           wint=1.0220e-08          dwg=-3.3960e-09
+ dwb=1.3460e-09            u0=3.1410e+02 + du0_n_18_mm
+ ua=-9.2010e-10            ub=1.9070e-18             uc=4.3550e-11
+ vsat=7.1580e+04           a0=1.9300e+00             ags=5.0720e-01
+ b0=1.4860e-06             b1=9.0640e-06            keta=1.7520e-02
+ a1=0.0000e+00             a2=1.0000e+00           voff=-1.0880e-01
+ nfactor=1.0380e+00        cit=-1.5110e-03          cdsc=2.1750e-03
+ cdscd=-5.0000e-04         cdscb=8.2410e-04         eta0=1.0040e-03
+ etab=-1.4590e-03          dsub=1.5920e-03          pclm=1.0910e+00
+ pdiblc1=3.0610e-03        pdiblc2=1.0000e-06    pdiblcb=0.0000e+00
+ drout=1.5920e-03          pscbe1=4.8660e+08      pscbe2=2.8000e-07
+ pvag=-2.9580e-01          rdsw=4.9050e+00          prwg=0.0000e+00
+ prwb=0.0000e+00           wr=1.0000e+00          alpha0=0.0000e+00
+ alpha1=0.0000e+00         beta0=3.0000e+01        xpart=1.0000e+00
+ cgso=2.3500e-10 + dcgso_n_18_mm
+ cgdo=2.3500e-10 + dcgdo_n_18_mm                     cgbo=0.0000e+00
+ cgsl=0.0000e+00           cgdl=0.0000e+00        ckappa=6.0000e-01
+ cf=1.5330e-10             clc=1.0000e-07           cle=6.0000e-01
+ dlc=2.9000e-08            dwc=0.0000e+00         vfbcv=-1.0000e+00
+ noff=1.0000e+00           voffcv=0.0000e+00        acde=1.0000e+00
+ moin=1.5000e+01           lmin=1.8000e-07          lmax=5.0000e-05
+ wmin=2.4000e-07           wmax=1.0000e-04
+ xl= - 1.0500e-08 + dxl_n_18_mm
+ xw=0.0000e-00 + dxw_n_18_mm                         js=1.0000e-06
+ jsw=7.0000e-11            cj=1.0300e-03 + dcj_n_18_mm
+ mj=4.4300e-01             pb=8.1300e-01
+ cjsw=1.3400e-10 + dcjsw_n_18_mm                    mjsw=3.3000e-01
+ tnom=2.5000e+01           ute=-1.2860e+00          kt1=-2.2550e-01
+ kt11=-4.1750e-09          kt2=-2.5270e-02           ua1=2.1530e-09
+ ub1=-2.6730e-18           uc1=-3.8320e-11           at=1.4490e+04
```

```
+ prt=-1.0180e+01           xti=3.0000e+00            wl=0.0000e+00
+ wln=1.0000e+00            ww=7.2620e-16             wwn=1.0000e+00
+ wwl=0.0000e+00            ll=-1.0620e-15            lln=1.0000e+00
+ lw=2.9960e-15             lwn=1.0000e+00            lwl=0.0000e+00
+ llc=-2.1400e-15           lwc=0.0000e+00           lwlc=0.0000e+00
+ wlc=0.0000e+00            wwc=0.0000e+00           wwlc=0.0000e+00
+ lvth0= - 1.0000e-03 + dlvth0_n_18_mm
+ wvth0=6.027e-02 + dwvth0_n_18_mm          pvth0=0 + dpvth0_n_18_mm
+ lnlx=-2.8540e-08           wnlx=0.0000e+00           pnlx=0.0000e+00
+ wua=-1.8800e-11            wu0=5.4000e-01 + dwu0_n_18_mm
+ pub=3.8000e-20             pw0=1.3000e-09          wrdsw=0.0000e+00
+ weta0=0.0000e+00           wetab=0.0000e+00         leta0=1.5740e-03
+ letab=0.0000e+00           peta0=0.0000e+00         petab=0.0000e+00
+ wpclm=0.0000e+00           wvoff=-4.0780e-04       lvoff=-4.2080e-03
+ pvoff=-3.7880e-04          wa0=-4.7310e-02           la0=-4.6670e-01
+ pa0=-2.6490e-02            wags=4.2420e-03           lags=3.0280e-01
+ pags=0.0000e+00            wketa=0.0000e+00        lketa=-1.9420e-02
+ pketa=0.0000e+00           wute=6.3730e-02           lute=0.0000e+00
+ pute=0.0000e+00            wvsat=5.0660e+03         lvsat=0.0000e+00
+ pvsat=0.0000e+00 + dpvsat_n_18_mm             lpdiblc2=-4.7520e-03
+ wat=7.0670e+03             wprt=0.0000e+00           ldif=8.0000e-08
+ hdif=2.6000e-07            n=1.0000e+00              pbsw=8.8000e-01
+ cjswg=5.0000e-10 + dcjgate_n_18_mm                   ctp=9.1400e-04
+ ptp=9.2400e-04             cta=9.1900e-04            pta=1.5800e-03
+ elm=5.0000e+00             tlevc=1.0000e+00
+ noimod=2                   noia=1.3182567385564E+19
noib=144543.977074592
+ noic=-1.24515794572817E-12                           ef=0.92
+ em=41000000



model p_18_mm bsim3v3 type=p
+ mobmod=3.0000e+00         version=3.2000e+00     capmod=2.0000e+00
+ binunit=1.0000e+00        nqsmod=0.0000e+00
+ tox=4.2000e-09 + dtox_p_18_mm                        toxm=4.2000e-09
+ xj=1.0000e-07             nch=6.1310e+17           ngate=1.0000e+23
+ vth0= - 4.5550e-01 + dvth0_p_18_mm                    k1=5.7040e-01
+ k2=6.9730e-03             k3=-2.8330e+00            k3b=1.3260e+00
+ w0=-1.9430e-07            nlx=2.5300e-07           dvt0=4.8850e-01
+ dvt1=7.5780e-02           dvt2=1.2870e-01        dvt0w=-1.2610e-01
+ dvt1w=2.4790e+04          dvt2w=6.9150e-01         lint=-1.0410e-08
+ wint=-1.5250e-07          dwg=-1.1510e-07           dwb=-1.0390e-07
+ u0=1.1450e+02 + du0_p_18_mm                          ua=1.5400e-09
+ ub=2.6460e-19             uc=-9.5870e-02           vsat=5.3400e+04
+ a0=1.3500e+00             ags=3.8180e-01            b0=-3.0880e-07
+ b1=0.0000e+00             keta=1.0440e-02           a1=0.0000e+00
+ a2=1.0000e+00             voff=-1.0730e-01      nfactor=1.5350e-00
+ cit=-1.0670e-03           cdsc=7.5780e-04         cdscd=-2.8830e-05
+ cdscb=1.0000e-04          eta0=1.0710e+00          etab=-9.2910e-01
+ dsub=1.9191e+00           pclm=2.6530e+00        pdiblc1=0.0000e+00
+ pdiblc2=5.0000e-06        pdiblcb=0.0000e+00       drout=1.4570e+00
+ pscbe1=4.8660e+08         pscbe2=2.8000e-07         pvag=1.1620e+00
+ rdsw=7.9210e+02           prwg=0.0000e+00           prwb=0.0000e+00
```

```
+ alpha0=0.0000e+00          alpha1=0.0000e+00        beta0=3.0000e+01
+ cgdo=2.0540e-10 + dcgdo_p_18_mm                      cgbo=0.0000e+00
+ cgso=2.0540e-10 + dcgso_p_18_mm                     xpart=1.0000e+00
+ cf=1.5330e-10              dlc=5.6000e-08            cgsl=0.0000e+00
+ cgdl=0.0000e+00            ckappa=6.0000e-01          clc=1.0000e-07
+ cle=6.0000e-01             dwc=0.0000e+00          vfbcv=-1.0000e+00
+ noff=1.0000e+00            voffcv=0.0000e+00         acde=1.0000e+00
+ moin=1.5000e+01            lmin=1.8000e-07           lmax=5.0000e-05
+ wmin=2.4000e-07            wmax=1.0000e-04
+ xl= - 2.0000e-09 + dxl_p_18_mm
+ xw=0.0000e+00 + dxw_p_18_mm                           js=3.0000e-06
+ jsw=4.1200e-11             cj=1.1400e-03 + dcj_p_18_mm
+ mj=3.9500e-01              pb=7.6200e-01
+ cjsw=1.7400e-10 + dcjsw_p_18_mm                      mjsw=3.2400e-01
+ tnom=2.5000e+01            ute=-4.4840e-01           kt1=-2.1940e-01
+ kt1l=-8.2040e-09           kt2=-9.4870e-03            ua1=4.5710e-09
+ ub1=-6.0260e-18            uc1=-9.8500e-02            at=1.2030e+04
+ prt=0.0000e+00             xti=3.0000e+00             ww=1.2360e-14
+ lw=-2.8730e-16             ll=6.6350e-15              wl=0.0000e+00
+ wln=1.0000e+00             wwn=1.0000e+00             wwl=0.0000e+00
+ lln=1.0000e+00             lwn=1.0000e+00             lwl=0.0000e+00
+ llc=-7.4500e-15            lwc=0.0000e+00            lwlc=0.0000e+00
+ wlc=0.0000e+00             wwc=0.0000e+00            wwlc=0.0000e+00
+ lvth0=4.4000e-03 + dlvth0_p_18_mm
+ wvth0= - 1.4800e-02 + dwvth0_p_18_mm
+ pvth0=3.2000e-03 + dpvth0_p_18_mm                    lnlx=-1.5840e-08
+ wrdsw=1.0070e+01           weta0=0.0000e+00         wetab=0.0000e+00
+ wpclm=0.0000e+00           wua=2.6300e-09            lua=-8.1530e-11
+ pua=5.8550e-11             wub=0.0000e+00            lub=0.0000e+00
+ pub=0.0000e+00             wuc=0.0000e+00            luc=0.0000e+00
+ puc=0.0000e+00             wvoff=-9.8160e-03       lvoff=-9.8710e-04
+ pvoff=-9.8330e-05          wa0=-4.8070e-02           la0=-2.8100e-01
+ pa0=8.6610e-02             wags=-4.1770e-02          lags=4.4540e-02
+ pags=-4.0760e-02           wketa=0.0000e+00        lketa=-1.2000e-02
+ pketa=0.0000e+00           wute=-2.6820e-01          lute=0.0000e+00
+ pute=0.0000e+00            wvsat=-1.4200e+04        lvsat=0.0000e+00
+ pvsat= - 4.3400e+02 + dpvsat_p_18_mm            lpdiblc2=3.0120e-03
+ cjswg=4.200e-10 + dcjgate_p_18_mm                    wat=-6.4050e+03
+ wprt=2.1660e+02            n=1.0000e+00              pbsw=6.6500e-01
+ cta=1.0000e-03             ctp=7.5300e-04             pta=1.5500e-03
+ ptp=1.2400e-03             ldif=8.0000e-08            rsh=8.0000e+00
+ rd=0.0000e+00              rsc=0.0000e+00             rdc=0.0000e+00
+ hdif=2.6000e-07            rs=0.0000e+00
+ noimod=2                   noia=3.57456993317604E+18 noib=2500
+ noic=2.61260020285845E-11 ef=1.1388
+ em=41000000
```

APPENDIX B

LAYOUT VS SCHEMATIC (LVS) REPORT

The LVS report of layout of the proposed high frequency low voltage CMOS current feedback operational amplifier based on MOCCII+ (HFLVCFOA-MO) is shown in Figure B.1.

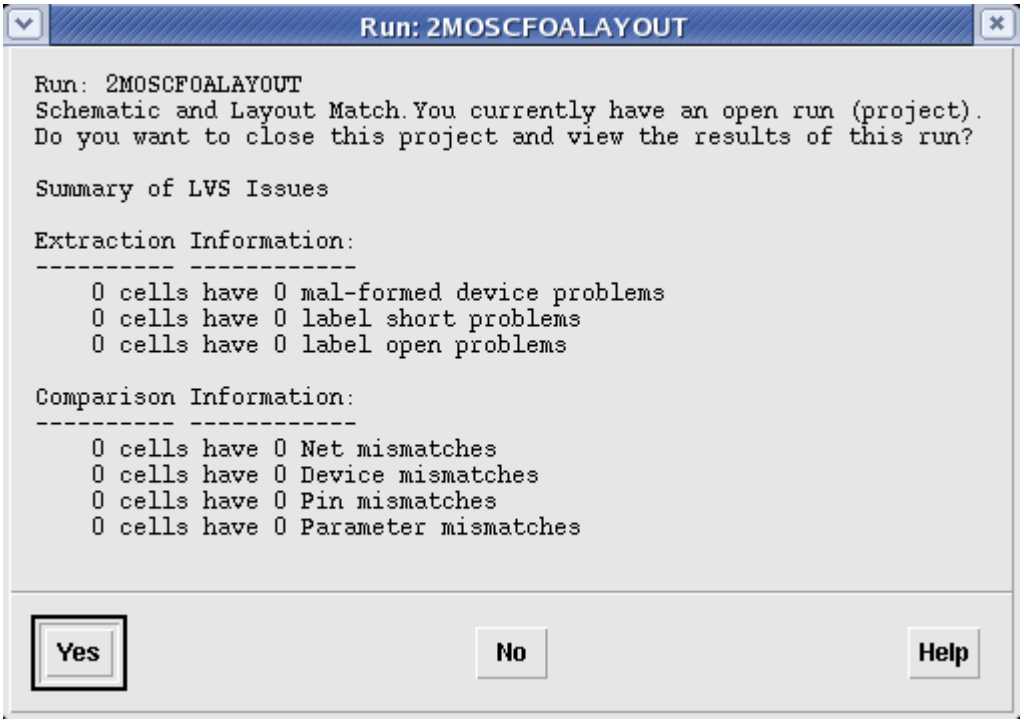

Figure B.1 LVS report