CMOS LOW NOISE RF AMPLIFIER DESIGN AND PARAMETER ESTIMATION USING ANN

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CERTIFICATE

This is to certify that the work which is being presented in this thesis entitled "**CMOS LOW NOISE RF AMPLIFIER DESIGN AND PARAMETER ESTIMATION USING ANN**" is a bonafide record of my own work carried under the supervision and guidance of Dr. Ravi Kumar, Assistant professor, Department of Electronics and Communication, Thapar University, Patiala submitted to Head of Department (Electronics and Communication), Thapar University in partial fulfillment for the award of the Degree of Master of Technology in VLSI Design & CAD and that the thesis has not previously formed the basis for the award of any other degree, Diploma, Associateship, Fellowship or other title.

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It is certified that the above statement is correct to the best of my knowledge and belief.

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ABSTRACT

In recent years, down-scaling in CMOS advanced technologies has provided high performance in digital circuits and reduced costs thereby meeting to a large extent the increasing demand of wireless communication products. With this technology advancement, the unity-current gain frequency of CMOS technology is now over several tens of GHz making the realization of system-on-chip solution possible which in turn, further reduces the cost. The demand of highly integrated CMOS RF building blocks with low noise has served as a motivation for present research initiative. Therefore, it becomes necessary to explore the area of low noise and power CMOS RFIC design for applications in a LOW NOISE AMPLIFIER. A low-noise amplifier (LNA) is an electronic device used to amplify possibly very weak signals (for example, captured by an antenna). It is usually located very close to the detection device to reduce losses in the feedline. It is necessary for an LNA to boost the desired signal power while adding as little noise and distortion as possible, so that the retrieval of this signal is possible in the later stages in the system. A good LNA has a low noise figure (NF), a large enough gain and should have large enough intermodulation and compression point. LNA is designed using the Cadence Spectre_RF tool on UMC 0.18μm technology to validate their performance. The various topologies of LNA are designed and simulated in this thesis report. The various topologies like single-ended LNA, differential LNA and CRLNA are compared in terms of their performance parameters. This thesis also reports a novel endeavour in the form of an Artificial Neural Network (ANN) model which estimates different amplifier parameters based upon the obtained simulation results, thereby, providing an alternative to the popular simulation tools which are based on complex analytical and mathematical models.

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List of Abbreviations

CMOS: Complementary metal oxide semiconductor

RFIC: Radio Frequency integrated circuit

LNA: Low Noise Amplifier

NF: Noise Figure

CRLNA: Current Reuse Low Noise Amplifier

ANN: Artificial Neural Network

CRT: Current - Reuse Technique

PCSNIM: Power constraint simultaneous noise and input matching

FCPCSNIM: Folded Cascade Power constraint simultaneous noise and input matching

GPC: Power Gain Circle

GAC: Available Gain Circle

SP: S-Parameters

PSS: Periodic Steady State Analysis

VSWR: Voltage standing wave ratio

FOM: Figure of merit

BP: Back Propagation

HC: Hard computing

SC: Soft computing

SNR: Signal-to-Noise Ratio

BW: Bandwidth

List of Symbols

V_{out}: Output voltage

V_{in}: Input voltage

Γ_s: Source impedance

Γ_L: Load impedance

F: Noise Factor

T_N: Noise Temperature

T_{ref}: Reference temperature

IP3: Third-order intercept

P_{1dB}: 1-dB compression point

K: Stability factor

Δf: Bandwidth

f_0: Centre frequency

G_m: Transconductance

P_D: Power dissipation

C: Correlation coefficient

v_{sat}: saturation velocity

Q: Quality factor

L: Channel Length

g_{d0}: Drain to source conductance at zero V_{DS}

ϒ: Drain noise coefficient

δ: Gate noise coefficient

K_f : Stern stability factor

w_T: Cut-off frequency

w_0: Central frequency

C_{gs}: Gate-source capacitance

ε: Dielectric constant

W: Width of MOSFET

I_D: Drain current

L: inductance

R: Resistance

C: Capacitance

r_n: Total input referred noise

φ: Activation function

η: Learning-rate parameter

CHAPTER 1

INTRODUCTION AND LITERATURE REVIEW

The first chapter is an introduction to low noise amplifiers (LNAs), and their applications in wireless communication. The present chapter introduces popular topologies of LNA, and design challenges associated with them. A thorough literature review has been undertaken to formulate the current research problem based upon which specific aspects of this thesis have been enlisted.

1.1 Overview of Low noise amplifier (LNA)

The growth of wireless services and other telecom applications has pushed the semiconductor industry towards complete system-on-chip solutions. Wireless systems comprise of a front-end and a back-end section. The front-end section processes analog signals in the high radio frequency (RF) range while the back-end section processes analog and digital signals in the baseband low frequency range. Radio frequency (RF) refers to the frequency range in the electromagnetic spectrum that is used for radio communications. It lies typically from 100 KHz to 100 GHz. However in general, frequencies below 1 GHz are considered baseband frequencies while those greater are described as RF.

RF circuits must process analog signals with a wide dynamic range at high frequencies. It is interesting to note that the signals must be treated as analog even if the modulation is digital or the amplitude carries no information. The trade-offs involved in the design of such circuits can be summarized in the “RF design hexagon” shown in Figure 1.1, where almost any two

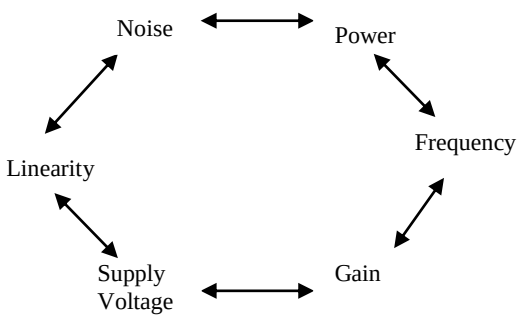


Figure 1.1: RF design hexagon.

of six parameters trade with each other to some extent. The radio frequency signal received at the antenna is weak. Therefore, an amplifier with a high gain and good noise performance is needed to amplify this signal before it can be fed to other parts of the receiver. Such an amplifier is referred to as a Low Noise Amplifier and forms an essential component of any RF integrated circuit receiver. The total noise performance of the receiver depends on the Gain and Noise Figure of the LNA, as can be seen from the Friss equation which is reproduced here for convenience.

$$F_{cascade} = F_{stage\,1} + \frac{(F_{stage\,2}-1)}{Gain_{stage\,1}} + \frac{(F_{stage\,3}-1)}{Gain_{stage\,1} \times Gain_{stage\,2}} + \cdots \quad (1.1)$$

$$NF = 10log_{10}(F) \quad (1.2)$$

In the above equations, Gain stands for the power gain of the particular block and stage1, stage2, stage3 are the cascade blocks of the receiver from the antenna to the demodulator. Since the LNA forms the first major stage of the receiver therefore, as evident from equation (1.1), its gain and noise performance contributes significantly towards the total noise performance of the receiver. The general topology of the LNA can be broken down into the three stages: Input Matching Network, the Amplifier and the Output Matching Network. The performance of these blocks is characterised by the S-parameters S_{11}, S_{12}, S_{21} and S_{22}. A brief introduction of S parameters is given in Chapter 2. LNA is used in various applications like ISM Radios, Cellular/PCS Handsets, GPS Receivers, Cordless Phones, Wireless LANs, Wireless Data, satellite communications etc. During reception of radio signal sent by satellite in a communication system, in the receiver section, second element after antenna is LNA. It is required because the signal typically travels through a very large distance and carries important information. While travelling through a medium it suffers due to various types of noise resulting in a very small signal to noise ratio. Due to this, direct reception of signal is not possible. Hence LNA is used to boost up the signal of desire energy from the weak information signal of required frequency.

1.2 Popular LNA Topologies

Low noise amplifier is the first stage in the receiver design. Since, the operating frequency of LNA is in RF frequency band, the circuit should be as simple as possible, especially for the RF path. Otherwise, the circuit noise becomes too high. Moreover, if the circuit is too complicated, the parasitic effects may distort the amplified signal. Hence, there are several fundamental low noise amplifier topologies for single ended narrow band low power low voltage design, such as resistive termination common source, common gate, shunt series

feedback common source, inductive degeneration common source, cascode inductor source degeneration, which are shown in Figure 1.2.

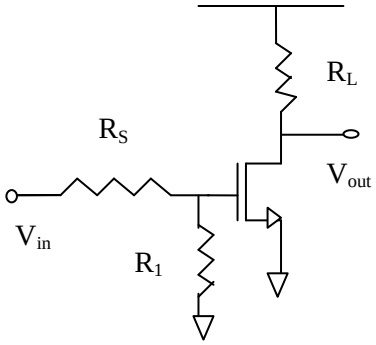


Figure 1.2(a): Resistive termination common source

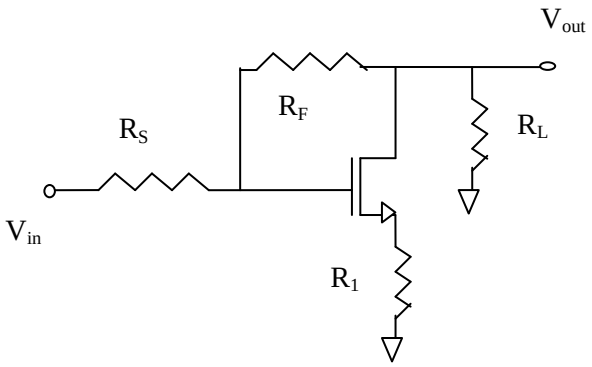


Figure 1.2(b): Shunt series feedback common source

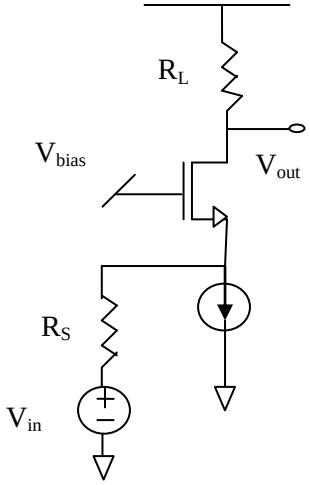


Figure 1.2(c): Common gate

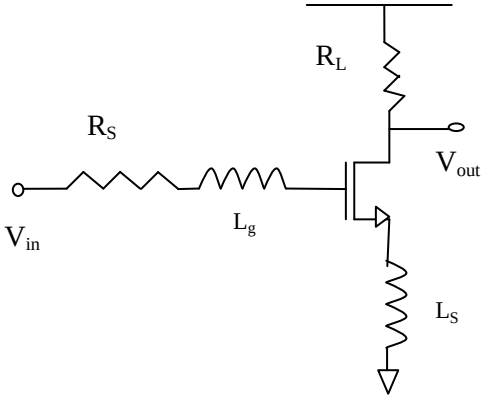


Figure 1.2(d): Inductive degeneration common source

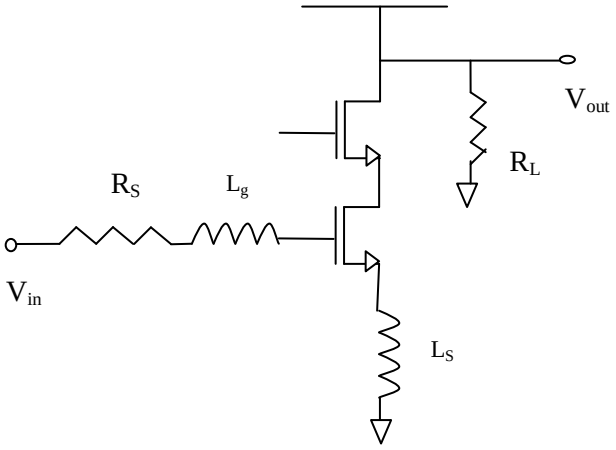


Figure 1.2(e): Cascode inductor source degeneration

Figure 1.2: Different LNA topologies

Out of the several topologies for narrow band single ended LNA design, an appropriate topology should be selected for low power and low voltage optimized LNA design. For common gate topology, the gain is less than 10.0 dB with very low power consumption. For shunt series feedback common source topology, it is difficult to trade off among gain, small noise figure and better input/output matching with very low power consumption. Resistor termination common source topology adds noise to the LNA because of the resistor thermal noise. Inductive degeneration common source topology satisfies the specification in very low power consumption, but the isolation is not good enough compared to the cascade inductor source degeneration topology, which can get the similar low noise amplifier performance with very low power consumption. Above all, the cascode inductor source degeneration topology provides higher gain with a low noise figure. The advantages and disadvantages of different kinds of LNA topologies are shown in Table 1.1.

Type	**Advantages**	**Disadvantages**
Resistive termination common source	Broad band amplifier	Adding the noise from the resistor
Common gate	The input impendence is equal to $1/g_m$. It is practical to get 50 Ω.	The impedance varies with the bias current.
Shunt series feedback common source	Broad band amplifier	Adding the noise from resistor
Inductive degeneration common source	The source and gate inductors make the input impendence 50 Ω. Not adding noise from the input.	The inductor is off chip at low frequency and low isolation.
Cascode inductor source degeneration	Isolation of input and output is good, higher gain, lower noise figure.	The inductor is off chip at low frequency.

Table 1.1: Advantages and disadvantages of LNA topologies

1.3 Literature Review

Several topologies of the low noise amplifier are proposed in the literature. Shaeffer and Lee [1] have proposed a CMOS low noise amplifier (LNA) which operates at 1.5V and 1.5 GHz frequency. Noise figure optimization techniques are also presented in this paper, with the detail discussion of the effects of induced gate noise in MOS devices. Goo et al. [2] presented a integrated low noise amplifier in which optimal noise performance is obtained by adjusting the source degeneration inductance. The effect of device geometry on NF is also presented in this paper. Chang et al. [3] have presented a fully integrated 5GHz low voltage and low

power LNA using current reuse forward bias technology through 0.18µm technology. Molavi and Hashemi [4] have proposed a wideband CMOS LNA which is an extension of the narrowband power constrained simultaneous noise input matching LNA design technique. Qi and Jie [5] present a 1.5V, 0.18µm CMOS low noise amplifiers with differential topology thereby highlighting the benefits of this topology are also discussed in this paper. Muhamad and Nardin [6] presented the design for low noise amplifier at 0.18µm technology using power constrained noise optimization method. Wang et al. [7] present a low noise and high gain differential LNA for the frequency range of 3.3GHz - 3.8GHz. In this work reduced noise figure and enhanced gain has been obtained using the differential and cascade circuit with active balun. Fan et al. [8] have reported methods of noise reduction and linearity improvement of differential LNA. In this paper an inductor is connected at the gate of cascode transistor to reduce the noise. Azevedo et al. [9] have made use of active balun integrated circuit with low noise amplifier (LNA). The concept of single-ended to differential signal transformation is also discussed in this paper. Andreani and Sjoland [10] present a technique for substantially reducing the noise of CMOS low noise amplifier implemented in the inductive source degeneration topology by taking into account the effect of gate induced current noise on the noise performance. Thus the efficacy of inductive source degeneration technique has been established beyond doubt. Radic et al. [11] present a current-reuse technique of low noise amplifier operating at frequency 2.4 GHz. In this work the cumulative effects of source, output and degeneration inductances on NF and gain has been rigorously dealt with. Thus, this work identifies the most influential LNA parameters on which gain and NF depend, taking into account the LNA design requirements for higher figures of merit. Nor et al. [12] present the various topologies like current - reuse technique (CRT), (PCSNIM) power constraint simultaneous noise and input matching and folded cascade (FC) PCSNIM of low noise amplifiers. Yousef et al. [13] proposed the design of a 2-16GHz ultra wide band low noise amplifier using current-reuse topology. Xuan et al. Li [14] have proposed a 2.5 GHz differential CMOS LNA using 0.18µm CMOS process. In this two inputs and two outputs architecture are designed.

1.4 Design Challenges

In the communication system, Low noise amplifier is the second element after antenna. LNA is used to boost up the signal of desire energy from the weak information signal of required energy with noise suppression. So, noise figure (NF) is the key issue of concern in this design. The receiver is the most power hungry block and the power consumption should be as

low as possible. So, noise figure and power consumption are no less important issues than gain.

With the small power consumption, the LNA should amplify the weak receiving signal to the level suitable for processing and provide gain to overcome the noise of subsequent stages while adding small amount of noise as possible. Matching of each block of the receiver is also an important issue in order to provide maximum power transfer at a particular frequency the matching is required. Furthermore, input and output matching to the source and load can maximize the gain. Input and output impedance matching is characterized by the input and output return loss. Since, it can affect the performance of the device. The gain should be large enough and the same time noise should be as less as possible. However, the gain of LNA should not be too high otherwise in the following stages, mixer is saturated. The LNA should present specific impedance at the input, e.g. 50 Ω to interface with the filter or antenna. Finding the delicate balance in all issues or parameters becomes the challenge more often than simply maximizing a single key parameter. The most recognizable trade-off is between LNA gain and noise figure (NF). Linearity is also an important design issue. Third order intercept point, IP3 has emerged as an important parameter in LNA design. The easiest way to improve the IP3 performance for a given frequency is to increase the current density or current drawn of LNA. If current drawn is of less important to us than IP3 performance, then keeping the power consumption to preoptimized permissible limits, we can improve IP3 performance by allowing slightly higher current drawn. Input and output return losses, S11 and S22, are also available for trading off to achieve improved gain and NF performance. Typically, the input and output matches are designed to afford good gain and NF performance. It is a balance of performance parameters. Emitter degeneration presents an entire range of opportunities for trading off performance parameters. Added emitter degeneration can also bring the match required for good return losses closer to the match for better NF.

Adding emitter feedback, however, trades off gain with IP3 and P1dB performance. Emitter degeneration also trades off linearity and stability, especially at higher frequencies. At the lower frequencies of the cellular bands, stability improves with emitter degeneration, while at frequencies greater than around 5 GHz, stability decreases as degeneration increases. So the tradeoff between linearity and stability must be examined across a full range of frequencies.

Small changes in inductance added to the emitter of a LNA can have large impacts on gain, NF and stability. As inductance increases, stability increases at the expense of gain. NF can also improve. However, continued increases in inductance can soon lead to degraded gain

and NF. In the LNA transistor, device size can be increased to improve linearity at the expense of current draw. Increasing current density in the LNA device can improve gain and NF, but again it is at the expense of current draw.

1.5 Specific aspects of this thesis

In this thesis design of a Low noise amplifier (LNA) with different topologies has been accomplished. Apart from considering obvious design goals of high gain and low noise figure, amplifier parameters for various topologies have been compared. This thesis also reports a novel endeavour in the form of an Artificial Neural Network (ANN) model which estimates different amplifier parameters based upon the obtained simulation results, thereby, providing an alternative to the popular simulation tools which are based on complex analytical and mathematical models. Before describing the organization of this thesis, it is necessary to enlist some of the salient and novel features.

- Detailed theoretical analysis and power constrained optimization of LNA
- Performance Comparison of three different LNA topologies.
- LNA performance analysis w.r.t the changing device geometry.
- ANN modelling for parameter estimation based on the obtained simulated values which has the potential to serve as an easier way for the future workers to optimize different LNA parameters w.r.t. the others without resorting to standard simulation (which though more accurate, are mostly lengthy, time consuming and require high expertise and dexterity in handling the tool).

This thesis is organized as into the following five chapters:

Chapter 2 describes the target specifications and noise optimization methods of low noise amplifier. The selection of various models of components used in the design of LNA, design steps involved and the analysis required are also presented in this chapter.

In Chapter 3 the design of various topologies of LNA (single-ended LNA, differential LNA, CRLNA) are presented. The simulated results and waveforms of resulted parameters are also presented.

Chapter 4 describes the comparison of the topologies of LNA in terms of simulated results. All the topologies are compared in terms of gain, noise figure and linearity.

In Chapter 5 ANN modeling for amplifier parameter estimation based on the obtained simulated values are presented. The ANN modelling provides an easier way for the future workers to optimize different LNA parameters w.r.t. the others without resorting to standard simulation.

Finally the thesis is concluded and scope for further development is discussed in the sixth chapter.

CHAPTER 2

DESIGN STEPS AND FUNDAMENTAL ANALYSIS

This chapter specifies the parameters, target specifications for different topologies of low noise amplifiers (LNAs). Noise optimization techniques, design steps and analysis required for LNA is also discussed in this chapter.

2.1 Target Specifications

For the designing of a low noise amplifier (LNA) it seems appropriate to establish what the target specifications are. This is done in terms of a number of various parameters.

2.1.1 S-Parameters

To represent a two-port network at microwave frequencies, scattering parameters (S-parameters) can be used. S-parameters themselves (S_{11}, S_{12}, S_{21}, S_{22}) represent reflection and transmission coefficients of the two-port under certain "matched" conditions. S_{11} is the reflection coefficient and S_{21} is the transmission coefficient at port 1 when port 2 is terminated in a load whose impedance is equal to that of the transmission line characteristic impedance. Likewise S_{22} is the reflection coefficient and S_{12} is the transmission coefficient at port 2 when port 1 is terminated in a matched load.

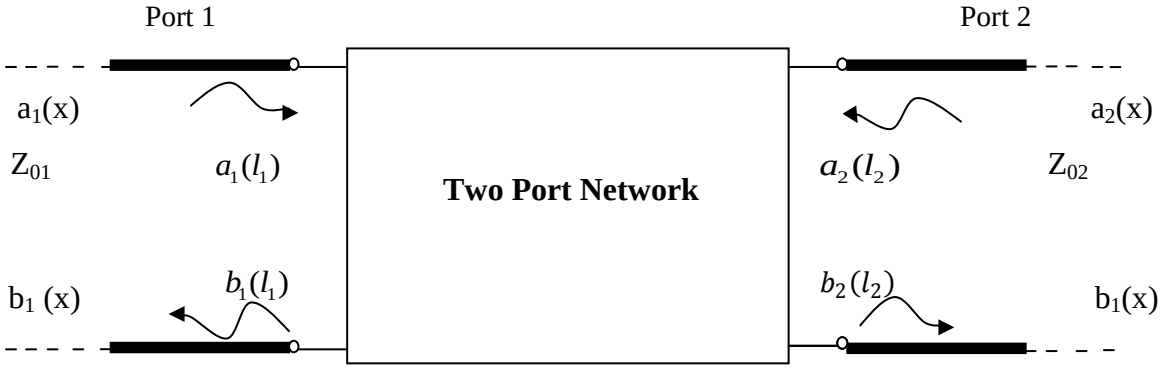


Figure 2.1: Incident and reflected waves in a two-port network.

In matrix form,

$$\begin{bmatrix} b_1(l_1) \\ b_2(l_2) \end{bmatrix} = \begin{bmatrix} S_{11} & S_{12} \\ S_{21} & S_{22} \end{bmatrix} \begin{bmatrix} a_1(l_1) \\ a_2(l_2) \end{bmatrix} \quad (2.1)$$

Where $a_1(l_1)$ and $a_2(l_2)$ represent incident waves and $b_1(l_1)$ and $b_2(l_2)$ represent reflected waves. Note that when the output port is terminated with $Z_L = Z_{02}$, $a_2(l_2) = 0$ (no reflection occurs at Z_L). Therefore S_{11} and S_{21} can be defined as the following:

$S_{11} = b_1(l_1) / a_1(l_1)$ and $a_2(l_2) = 0$ (input reflection coefficient; output port matched) (2.2)

$S_{21} = b_2(l_2) / a_1(l_1)$ and $a_2(l_2) = 0$ (forward transmission coefficient; output port matched) (2.3)

Similarly, when the input is terminated with $Z_S = Z_{01}$, $a_1(l_1) = 0$ (no reflection occurs at Z_S) then S_{22} and S_{12} are defined as follows:

$S_{22} = b_2(l_2) / a_2(l_2)$ and $a_1(l_1) = 0$ (input reflection coefficient; input port matched) (2.4)

$S_{12} = b_1(l_1) / a_2(l_2)$ and $a_1(l_1) = 0$ (reverse transmission coefficient; input port matched) (2.5)

2.1.2 Gain

The gain of the device is its ability to amplify the amplitude or the power of the input signal. It is defined as the ratio of the output to the input signal and is often referred to in terms of decibels.

$$Voltage\ gain = 20\ log\left(\frac{V_{out}}{V_{in}}\right) \quad (2.6)$$

Power gain is generally defined as the ratio of the power actually delivered to the load to the power actually delivered by the source. Three power gains are commonly used in LNA design.

(1) G_T, transducer power gain

(2) G_P, operating power gain

(3) G_A, available power gain

Besides these three gain definitions, there are three additional gain definitions we can use to evaluate the LNA design.

- G_{umx}, maximum unilateral transducer power gain
- G_{max}, maximum transducer power gain
- G_{msg}, maximum stability gain

Besides these six gain definitions, there are two gain circles that are helpful to the design of input and output matching networks.

- GPC, power gain circle
- GAC, available gain circle

2.1.2.1 Transducer Power Gain

Transducer power gain, G_T is defined as the ratio between the power delivered to the load and the power available from the source.

$$G_T = \frac{1-|\Gamma_S|^2}{|1-S_{11}\Gamma_S|^2}|S_{21}|^2 \frac{1-|\Gamma_L|^2}{|1-\Gamma_{out}\Gamma_L|^2} \quad (2.7)$$

The transducer gain expressions are too complex for manual design. To effect an approximate gain solution, let us ignore the feedback, that is assume that $S_{12} = 0$. If an amplifier has no feedback, signals pass one way through it. Accordingly this is called unilateral gain. If $S_{12} = 0$, then $\Gamma_{IN} = S_{11}$ and $\Gamma_{OUT} = S_{22}$ and transducer gain becomes the unilateral gain.

2.1.2.2 Operating Power Gain

Operating power gain, G_P is defined as the ratio between the power delivered to the load and the power input to the network.

$$G_P = \frac{1}{1-|\Gamma_{in}|^2}|S_{21}|^2 \frac{1-|\Gamma_L|^2}{|1-S_{22}\Gamma_L|^2} \quad (2.8)$$

The LNA scattering matrix is normalized in terms of the source and load resistance in Equation 2.9.

$$\Gamma_S = \Gamma_L = 0 \quad (2.9)$$

Thus, the input and output reflection coefficients are simply expressed in terms of Equations 2.10 and 2.11.

$$\Gamma_{in} = S_{11} \quad (2.10)$$

$$\Gamma_{out} = S_{22} \quad (2.11)$$

From these Equations,

$$G_P = \frac{1}{1-|S_{11}|^2}|S_{21}|^2 \quad (2.12)$$

2.1.2.3 Available Power Gain

Available power gain, G_A is defined as the ratio between the power available from the network and the power available from the source.

$$G_A = \frac{1-|\Gamma_S|^2}{|1-S_{11}\Gamma_S|^2}|S_{21}|^2 \frac{1}{1-|\Gamma_{out}|^2} \quad (2.13)$$

From Equations 2.9 and 2.11,

$$G_A = |S_{21}|^2 \frac{1}{1-|S_{22}|^2} \quad (2.14)$$

Because the power available from the source is greater than the power input to the LNA network, $G_P > G_T$. The closer the two gains are, the better the input matching is. Similarly,

because the power available from the LNA network is greater than the power delivered to the load, $G_A > G_T$. The closer the two gains are, the better the output matching is.

2.1.2.4 Maximum Unilateral Transducer Power Gain

Maximum unilateral transducer power gain, G_{umx} is the transducer power gain when we assume that the reverse coupling of the LNA, S_{12} is zero, and the source and load impedances are conjugately matched to the LNA. That is $\Gamma_S = S_{11}$ and $\Gamma_L = S_{22}$. If S_{12} = 0 and the input and output reflection coefficients are $\Gamma_{in} = S_{11}$, $\Gamma_{out} = S_{22}$.Thus from Equation 2.8 we get Equation 2.15.

$$G_{umx} = \frac{1}{\left|1-|S_{11}|^2\right|}|S_{21}|^2\frac{1}{\left|1-|S_{22}|^2\right|} \tag{2.15}$$

2.1.2.5 Maximum Transducer Power Gain

Maximum transducer power gain, G_{max} is the simultaneous conjugate matching power gain when both the input and output are conjugately matched. That is $\Gamma_S = S_{in}$ and $\Gamma_L = S_{out}$.When the reverse coupling, S_{12} is small, G_{umx} is close to $G_{max.}$

$$G_{max} = \frac{|S_{21}|}{|S_{12}|}(K - \sqrt{K^2 - 1}) \tag{2.16}$$

Where, K is stability factor.

2.1.2.6 Maximum Stability Gain

Maximum stability gain, G_{msg} is the maximum of G_{max} when the stability condition K > *1* is still satisfied.

$$G_{msg} = \frac{|S_{21}|}{|S_{12}|} \tag{2.17}$$

2.1.2.7 Power Gain Circle

Power gain circle in short form is *GPC*. From Equation 2.8, G_P is solely a function of the load reflection Γ_L. Thus we can draw power gain contours on the Smith chart of Γ_L.The location for the peak of the contour corresponds to Γ_L producing the maximum G_P. We can move the peak location by changing the design of the output matching network. The best location for the contour peak is at the center of the Smith chart, that is where $\Gamma_L = 0$.

2.1.2.8 Available Gain Circle

Available gain circle in short form is *GAC*. From Equation 2.13, we can see that G_A is solely a function of the source reflection Γ_S. Thus we can draw available gain contours on the Smith

chart of Γ_S. The location for the peak of the contour corresponds to Γ_S producing the maximum G_A. We can move the peak location by changing the design of the input matching network. The best location for the contour peak is at the center of Smith chart that is where $\Gamma_S = 0$.

2.1.3 Noise Performance

The fundamental noise performance parameter is the Noise Factor (F), which is defined as the ratio of the total output noise power to the output noise due to input source. If the Noise Factor is expressed in decibels it is called the Noise Figure (NF) (Equation 2.18). Another related and often talked about parameter in RF applications is the Signal-to-Noise Ratio (SNR), which is the ratio of the signal power and the noise power (Equation 2.19). The Noise Factor is equivalent to the ratio of the SNR at the input and that at the output of the LNA (Equation 2.20). Hence, the Noise Factor is a measure of to what extent the LNA degrades the SNR. An alternative way to express just that is the Noise Temperature (T_N), which is particularly useful with cascaded amplifier systems or in applications where the Noise Figure is extremely low, as it allows greater resolution. The Noise Temperature is calculated with a reference temperature (T_{ref}) that is normally 290 K. By definition T_N is the temperature increase that is required in the source resistance, so that it alone produces the noise that corresponds to the output noise at T_{ref}. Consequently, if there is no additional noise at the output of the amplifier, then T_N is 0 K.

$$NF = 10 \log F \tag{2.18}$$

$$SNR = \frac{P_{signal}}{P_{noise}} \tag{2.19}$$

$$F = (P_{Si} / P_{Ni}) / (P_{So} / P_{No}) = 1 + T_e / T_s \tag{2.20}$$

2.1.4 Linearity

The linearity of the LNA is another concern that must be taken into account. Linear operation is crucial, particularly when the input signal is weak with a strong interfering signal in close proximity. This is because in such a scenario there is a possibility for undesired intermodulation distortion such as blocking and cross modulation.

Third-order intercept (IP3) and 1-dB compression point (P_{1dB}) are two measures of linearity. IP3 shows at what power level the third-order intermodulation product is equal to the power of the first-order output. IIP3 and OIP3 are the input power and output power respectively, that corresponds to IP3. P_{1dB} shows at what power level the output power drops 1 dB, as a consequence of non-linearities, relative the theoretical linear power gain, Figure 2.2.

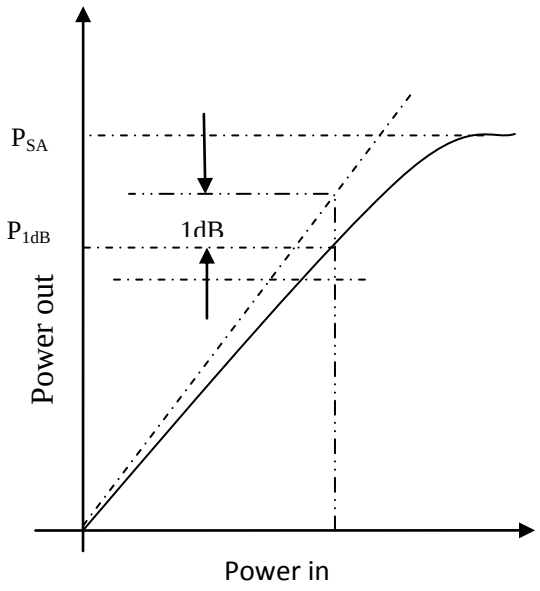


Figure 2.2: 1 dB compression point.

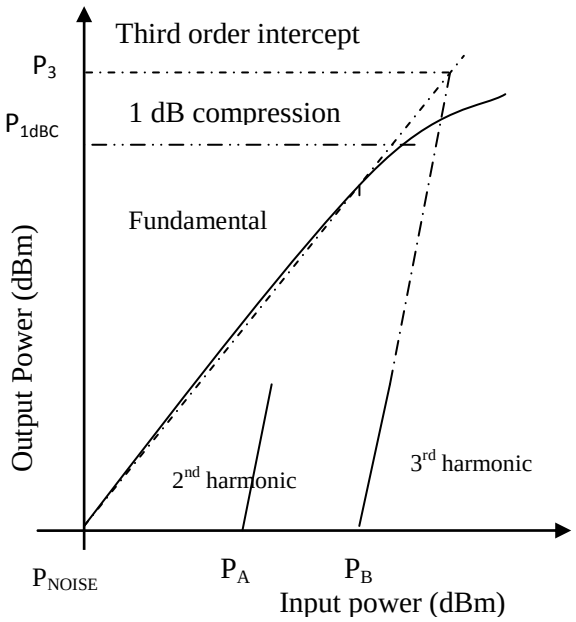


Figure 2.3: Third order intersect point

By knowing either IP3 or P_{1dB} the other can be estimated with the following rule-of-thumb formula:

$$IP3 = P_{1dB} + 10dB \tag{2.21}$$

Third-order intercept point is shown in Figure 2.3. Both measurements indicate an upper distortion limit for the tolerable input power, whereas the noise figure sets a lower limit. The ratio of the two determines the dynamic range of the amplifier.

2.1.5 Stability

In the presence of feedback paths from the output to the input, the circuit might become unstable for certain combinations of source and load impedances. An LNA design that is normally stable might oscillate at the extremes of the manufacturing or voltage variations, and perhaps at unexpectedly high or low frequencies. The stability factor is given as in Equation 2.22.

$$K = \frac{1+\left|\Delta\right|^2-\left|S_{11}\right|^2-\left|S_{22}\right|^2}{2\left|S_{21}\right|\left|S_{12}\right|} \tag{2.22}$$

Where,

$\Delta = S_{11}S_{22} - S_{12}S_{21}$

When $K > 1$ and $\Delta < 1$, the circuit is unconditionally stable. That is, the circle does not oscillate with any combination of source and load impedances. We should perform the

stability evaluation for the S parameters over a wide frequency range to ensure that *K* remains greater than one at all frequencies. As the coupling (S_{12}) decreases, that is as reverse isolation increases, stability improves. Techniques such as resistive loading and neutralization are used to improve stability for an LNA. Equation 2.22 is valid for small-signal stability. If the circuit is un-conditionally stable under small-signal conditions, the circuit is less likely to be unstable when the input signal is large. Aside from the two metrics *K* and Δ, the source and load stability circles can be used to check LNA stability.

2.1.6 Centre Frequency and Bandwidth

As the LNA will operate with input signals of a particular frequency band, it is desired to design it with a centre frequency and bandwidth accordingly. Looking at the transfer function of the LNA, the differential of the two points around the centre frequency f_0, where the power gain is halved, is the bandwidth, denoted Δf in Figure 2.4. Although the target bandwidth should be specified numerically, by naming convention there are two options: narrowband and wideband.

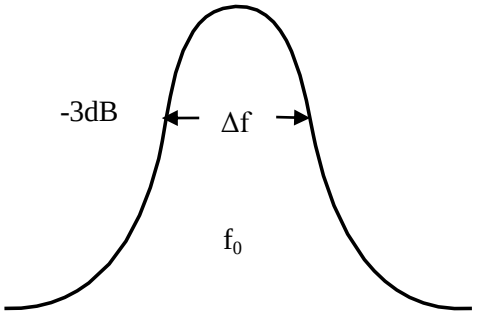


Figure 2.4: Illustration of centre frequency and bandwidth.

2.1.7 Return Loss

The Return Loss is a measure of how well the input impedance is matched to the reference impedance or how well the output impedance is matched to the load impedance in a power transfer perspective. Strictly speaking it signifies how much power is reflected due to impedance mismatch relative the transmitted power. Return loss is typically specified as IRL, which corresponds to the return loss at the input port. The input return loss value can be expressed in terms of the measured S parameter S_{11}:

$$\text{Input Return Loss} = -S_{11}\,(\text{dB}) = -20 \log |S_{11}| \tag{2.23}$$

Similarly, output return loss is represented by S-parameter S_{22}:

$$\text{Output Return Loss} = -S_{22}\,(\text{dB}) = -20 \log |S_{22}| \tag{2.24}$$

Input return loss is of more concern than output return loss, however because too big a mismatch at the input of the LNA can lead to degradation in noise performance.

2.1.8 Input and Output Impedance Matching

The input and output are each connected to the LNA with filters whose performance relies heavily on the terminal impedance. Furthermore, input and output matching to the source and load can maximize the gain. Input and output impedance matching is characterized by the input and output return loss.

$$20\log|\Gamma_{in}| = 20\log|S_{11}| \tag{2.25}$$

$$20\log|\Gamma_{out}| = 20\log|S_{22}| \tag{2.26}$$

We can also characterize the LNA's input and output impedance matching by the voltage standing wave ratio (VSWR):

$$VSWR_{in} = \frac{1+|\Gamma_{in}|}{1-|\Gamma_{in}|} = \frac{1+|S_{11}|}{1-|S_{11}|} \tag{2.27}$$

$$VSWR_{out} = \frac{1+|\Gamma_{out}|}{1-|\Gamma_{out}|} = \frac{1+|S_{22}|}{1-|S_{22}|} \tag{2.28}$$

Our primary design goals are to minimize the return loss and make the VSWR close to 1.

2.1.9 Design Target

Based on the preliminary studies of LNA, the design target for low noise amplifier is specified in the Table 2.1.

Parameter	Specification			Units
	Single-ended LNA	Differential LNA	CR-LNA	
Frequency	2	2	2	GHz
Noise Figure	< 3	< 3	< 3	dB
Voltage Gain	>12	>15	>20	dB
Power Gain(S_{21})	>10	>15	>20	dB
S_{22}	<-10	<-10	<-10	dB
S_{11}	<-10	<-10	<-10	dB
S_{12}	<-10	<-10	<-10	dB
K_f	>1	>1	>1	
Power consumption	5-8	10-16	2-5	mW
Source/load impedance	50	50	50	ohm
1-dB Point	>-15	>-12	>-25	dBm
IP3 Point	>-5	>-2	>-15	dBm
Power supply	1.8	1.8	1.8	V
Current	<5	<10	<3	mA
Technology	CMOS 0.18 μm	CMOS 0.18 μm	CMOS 0.18 μm	μm

Table 2.1 LNA specifications design target.

2.2 Noise Optimization Methods

In low noise amplifier design, determination of the minimum noise figure is a common and well-understood procedure. Typically, a small-signal model of the amplifier is assumed, an expression for F is formed and differentiation leads to the unique conditions for optimized noise performance [1]. In the noise optimization techniques we seek the conditions that guarantee optimized noise performance for a specified fixed design parameter, such as gain or power consumption, under the condition of perfect input matching. Now, we fix the necessary design criteria and determine the appropriate small-signal model through the optimization procedure. Because the architecture permits selection of Q_L and L_S independently, so we can optimize the noise performance that coincides with the input match. There are two approaches for the optimization of noise figure. The first assumes a fixed transconductance, G_m, for the amplifier. The second assumes fixed power consumption. We know the equation of noise figure is [2]:

$$F = 1 + \frac{R_l}{R_s} + \frac{R_g}{R_s} + \gamma\chi g_{d0} R_s \left(\frac{\omega_0}{\omega_T}\right)^2 \tag{2.29}$$

To illustrate these approaches, the expression for F in Equation (2.29) can be recast to make its dependence on power dissipation (P_D). From eq. (2.30) it is clear that condition for constant G_m is equivalent to the condition of constant ω_T.

$$G_m = g_{m1} Q_{in} = \frac{g_{m1}}{\omega_0 C_{gs}(R_s + \omega_T L_S)} = \frac{\omega_T}{\omega_0 R_s (1 + \frac{\omega_T L_S}{R_s})} = \frac{\omega_T}{2\omega_0 R_s} \tag{2.30}$$

To maintain a fixed ω_T, we need only fix the value of ρ. Hence, we will reformulate F in terms of P_D and ρ to facilitate both optimizations. The equation of F in terms of P_D and ρ is given below [2].

$$F = 1 + \frac{\gamma\omega_0 L}{3v_{sat}} P(\rho, P_D) \tag{2.31}$$

In this equation we have neglected the contributions of the gate resistance and inductor losses to the noise factor. In this equation (2.31) P (ρ, P_D), is a ratio of two sixth-order polynomials of ρ given by

$$P(\rho, P_D) = \frac{\frac{P_D}{P_0} P_1(\rho) + P_2(\rho) + \frac{P_0}{P_D} P_3(\rho)}{\rho^3 \left(1 + \frac{\rho}{2}\right)^2 (1 + \rho)} \tag{2.32}$$

With,

$$P_1(\rho) = (1+\rho)^6 + \frac{\delta}{5\gamma}(1+\rho)^2 \left(1 + \frac{\rho}{2}\right)^2$$

$$P_2(\rho) = 2|c|\sqrt{\frac{\delta}{5\gamma}}(1+\rho)^3 \left(1 + \frac{\rho}{2}\right)\rho^2$$

$$P_3(\rho) = \frac{\delta}{5\gamma}\left(1+\frac{\rho}{2}\right)^2 \rho^4$$

Because F is a function of two variables, one can define contours of constant noise figure in ρ and P_D. Equation (2.31) suggests that optimization of proceeds by minimizing with respect to one of its arguments, keeping the other one fixed.

2.2.1 Fixed G_m optimization

To fix the value of the transconductance, G_m , we need only assign a constant value to ρ. We know,

$$\omega_T \approx \frac{g_m}{C_{gs}} = \frac{g_m}{\frac{2}{3}WLC_{ox}} = \frac{3}{2}\frac{\alpha\mu_{eff}V_{od}}{L^2} = \frac{3\alpha\rho\, v_{sat}}{L} \tag{2.33}$$

The appropriate value for G_m is easily determined by substituting (2.33) into the expression for as found in (2.30). The value of G_m which relates to ρ, is

$$G_m = \frac{3v_{sat}}{2\omega_0 R_s L}\frac{\rho\left(1+\frac{\rho}{2}\right)}{(1+\rho)^2} \tag{2.34}$$

Once ρ is determined, we can minimize the noise factor by taking:

$$\frac{\partial P(\rho,P_D)}{\partial P_D} = 0 \tag{2.35}$$

Which, after some algebraic manipulations results in

$$P_{D,opt,G_m} = P_0\sqrt{\frac{P_3(\rho)}{P_1(\rho)}} = P_0\frac{\rho^2}{1+\rho}\left[1+\frac{5\gamma}{\delta\alpha^2}\right]^{-1/\,2} \tag{2.36}$$

This expression gives the power dissipation which yields the best noise performance for a given G_m under the assumption of matched input impedance. We know Q_L is:

$$Q_L = \frac{P_0}{P_D}\frac{\rho^2}{1+\rho} \tag{2.37}$$

By comparing (2.36) to (2.37), we see immediately that this optimum occurs when

$$Q_L = Q_{L,opt,G_m} = \sqrt{1+\frac{5\gamma}{\delta\alpha^2}} \geq 1.87 \tag{2.38}$$

Hence, the best noise performance for a given transconductance is achieved at some specific input. Note that the value 1.87 is valid only for long-channel devices. For short-channel lengths, where $\alpha < 1$, we can expect the optimum Q_L to be somewhat larger. By substituting (2.38) into (2.29), we determine that the minimum noise factor (neglecting inductor and gate losses) is

$$F_{min,G_m} = 1+\sqrt{\frac{4}{5}\delta\gamma}\left(\frac{\omega_0}{\omega_T}\right)\left\{|C|+\sqrt{1+\frac{5\gamma}{\delta\alpha^2}}\right\} \geq 1+1.33\left(\frac{\omega_0}{\omega_T}\right) \tag{2.39}$$

The value 1.33 is only valid for long-channel devices; it may be three to four times larger in the presence of high electric fields.

2.2.2 Fixed P_D Optimization

An alternate method of optimization fixes the power dissipation and adjusts ρ to find the minimum noise factor. If we assume that α < < 1, then P (ρ, P_D) can be simplified to:

$$P(\rho, P_D) \approx \frac{\frac{P_D}{P_0}\left(1+\frac{\delta}{5\gamma}\right)+2|C|\sqrt{\frac{\delta}{5\gamma}}\rho^2+\frac{P_0}{P_D}\frac{\delta}{5\gamma}\rho^4}{\rho^3} \quad (2.40)$$

This expression is minimized for a fixed P_D when $\frac{\partial P(\rho,P_D)}{\partial \rho} = 0$ (2.41)

The solution of this equation, under the assumption that α < < 1 is:

$$\rho^2{}_{opt,P_D} = \frac{P_D}{P_0}|C|\sqrt{\frac{5\gamma}{\delta}}\left[1+\sqrt{1+\frac{3}{|C|^2}\left(1+\frac{\delta}{5\gamma}\right)}\right] \quad (2.42)$$

By comparing (2.42) to (2.37), it is clear that this value for ρ is equivalent to an optimum Q_L of

$$Q_{L,opt,P_D} = |C|\sqrt{\frac{5\gamma}{\delta}}\left[1+\sqrt{1+\frac{3}{|C|^2}\left(1+\frac{\delta}{5\gamma}\right)}\right] \approx 3.9 \quad (2.43)$$

So, it is clear that the optimum Q_L for fixed power dissipation is *larger* than the optimum Q_L for a fixed G_m. From these equations

$$F_{min,P_D} \approx 1 + 2.4\frac{\gamma}{\alpha}\left(\frac{\omega_0}{\omega_T}\right) \geq 1 + 1.62\left(\frac{\omega_0}{\omega_T}\right) \quad (2.44)$$

Where the value of 1.62 is valid only in the long-channel limit; the value will be somewhat larger for short-channel devices in velocity saturation.

2.3 Selection of appropriate circuit components

Because MOSFETs, spiral inductors and capacitors are often used in LNA circuit, the accurate RF models are very important to predict the silicon performance of gigahertz circuits. The characteristic of transistor in low frequency is different from the one in high frequency. The parasitic effects of transistor should be considered in circuit design, which are not included in the low frequency circuit design. So the transistor model for low frequency design is quite different with the model for high frequency design. Moreover in high frequency, the inductance and Q value varies with the operating frequency and capacitor also has parasitic effects. Spectre RF simulator or Affirma RF simulator of Cadence is used for the design of various topologies of LNA. So transistor, inductor and capacitor models should also be chosen carefully for correct design from the design library of Spectre RF simulator. The analogLib library in Cadence Affirma is used for selecting other active and passive components.

2.3.1 MOSFET RF Models

MOSFET models, especially the RF MOSFET models are required to predict the silicon performance accurately, such as sub-circuit short channel MOSFET models for RFIC designs. In the sub-circuit models, MOSFET is divided into two parts, an intrinsic part and an extrinsic part. The intrinsic part represents the main active part of the device, which can be any compact model, such as Berkeley Short-Channel IGFET Model (BSIM). However, the extrinsic part consists of most of the parasitic elements, including all the terminal access series resistance, gate resistance, overlap and junction capacitance, and substrate network. The UMC_18_CMOS library in SpectreRF contains various MOSFET models given in the appendix A

From these MOSFETs, N_L18W500_18_RF device is used for the designing of LNAs. The length of this transistor is constant 180.0nm and finger number is variable. The range of finger number is 5-21. The maximum allowable width of N_L18W500_18_RF in SpectreRF is 105µm (21×5). Two or more transistors are used in parallel for the bigger transistors. For the PMOSFET, P_L18W500_18_RF device is used for designing of LNAs.

2.3.2 Inductors RF Models

Spiral inductors with reasonable Q and self-resonant frequency are widely used in the RFIC designs, such as fully integrated LNA, oscillator and impedance matching network. They are proved to be most difficult passive components to be implemented on chip. Circular square spiral inductor is defined by side length, wire width, wire space and number of turns. The UMC_18_CMOS library in SpectreRF contains the inductor model given in the appendix A.

L_SLCR20K_RF inductor model is used for the designing of LNAs. It is a three terminal inductor. Model range of turn numbers is 1.5-5.5 and the model range of width is 6 µm-20 µm. The model range of diameter is 126.0 µm-238.9 µm. As the turn number decreases the inductance also decreases. The maximum value of inductance is 14.054 nH and if I want more than 14.054 nH then two inductors in series are used.

2.3.3 Capacitors RF Models

Capacitors are another important passive components widely used in RF circuit design, such as impedance matching and DC block. The usage of a capacitor is primarily dependent upon the characteristics of its dielectric. The dielectric's characteristics also determine the voltage levels and the temperature extremes at which the device may be used. The UMC_18_CMOS library in SpectreRF contains various capacitors models given in the appendix B.

From these capacitors, MIMCAPM_RF device is used for the designing of LNAs. It is a three terminal capacitor. The model range of width and length is 10-70 µm and range of ratio is =<6 and >=1. The maximum value of this capacitor is 5.047 pF and minimum value is 103.00f.

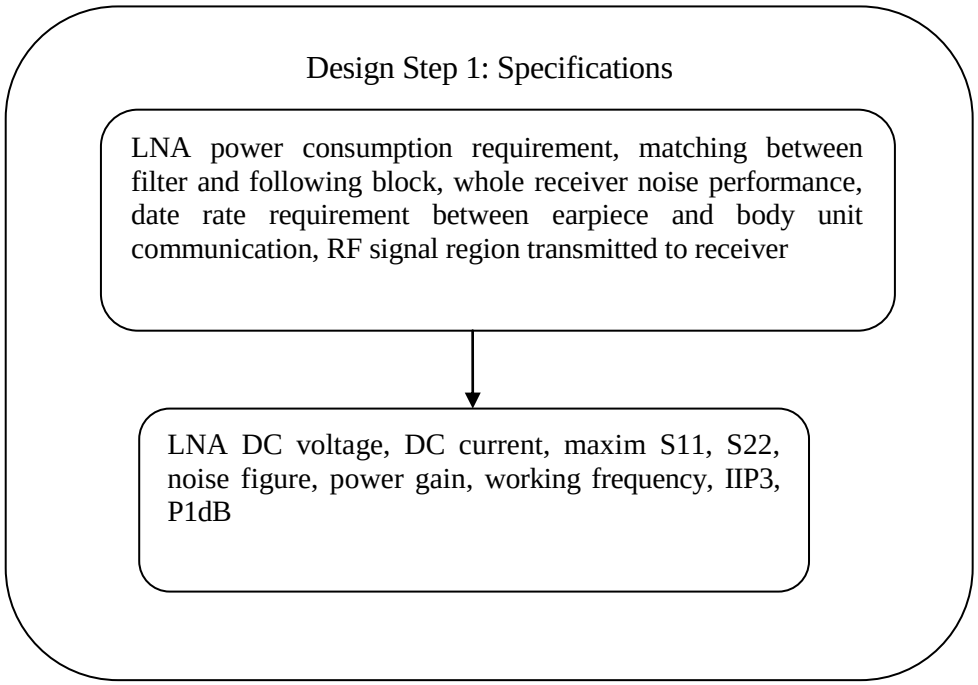
2.3.4 Resistors RF Models

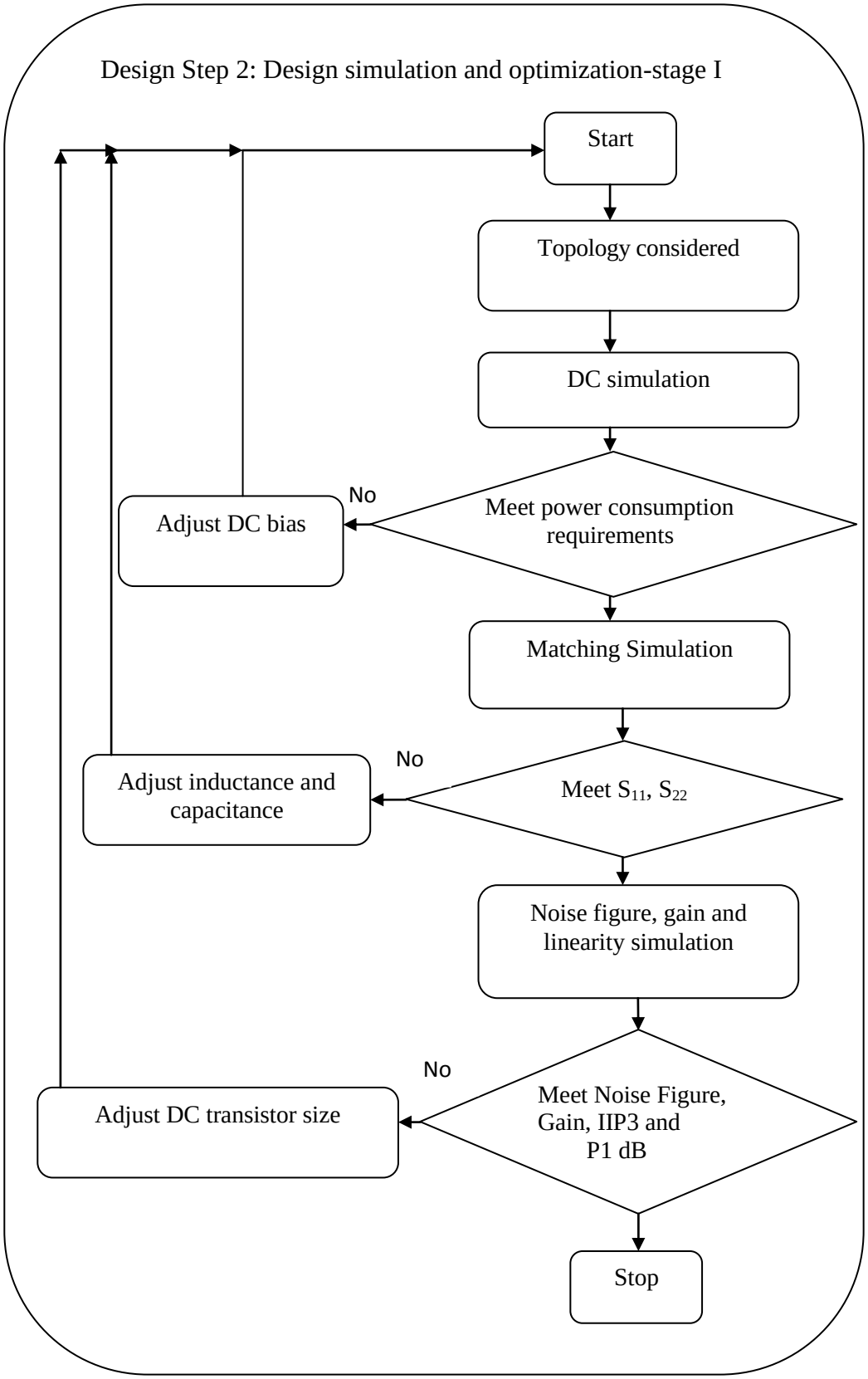
Resistance is the property of a material that determines the rate at which electrical energy is converted into heat energy for a given electric current. At very high frequencies and with low-value resistors (under 50 ohms), lead inductance and skin effect may become noticeable. The UMC_18_CMOS library in SpectreRF contains various resistors models given in the appendix B.

From these capacitors, RNNPO_RF device is used for the designing of LNAs. It is a three terminal resistor. The model range of width is 2-10 µm. The model range of length is 2-100 µm and range of ratio is <=10 and >=1. The maximum value of resistance is 1.205465KΩ and minimum value is 136.6264 Ω.

2.4 LNA Design and Optimization Steps

The design and optimization steps followed in the design of presented LNAs are mentioned below. For each step, the design flow is shown in Fig. 2.5.




Design Step 2: Design simulation and optimization-stage I
Start
Topology considered
DC simulation
Meet power consumption requirements
No
Adjust DC bias
Matching Simulation
Meet S_{11}, S_{22}
No
Adjust inductance and capacitance
Noise figure, gain and linearity simulation
Meet Noise Figure, Gain, IIP3 and P1 dB
No
Adjust DC transistor size
Stop

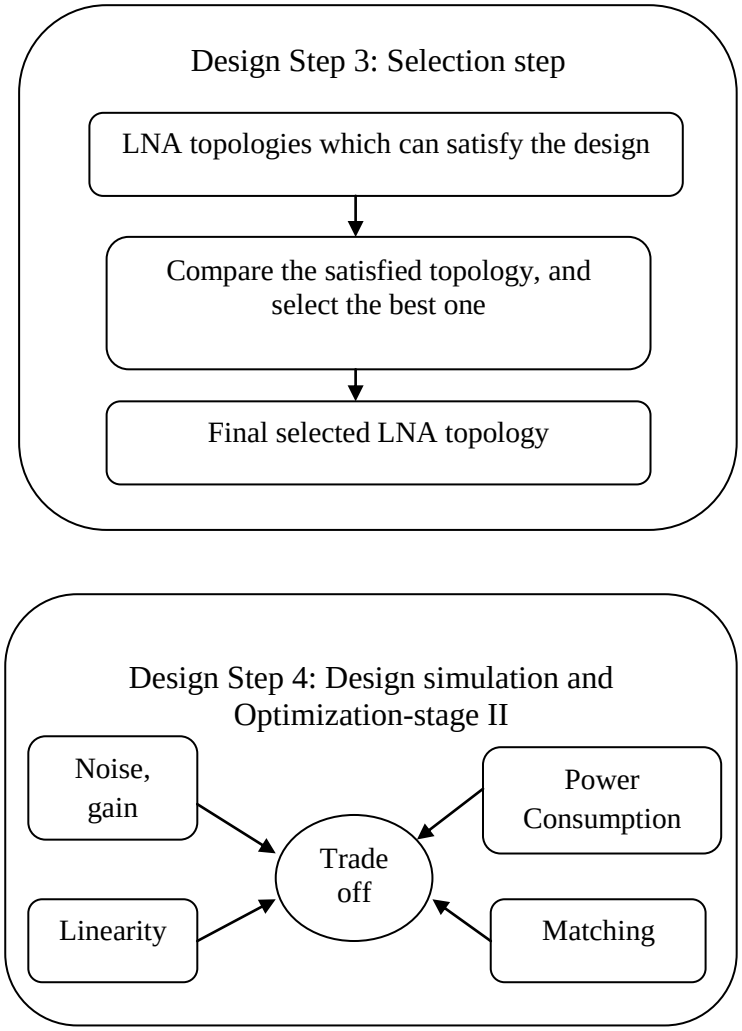


Figure 2.5: Design steps of LNA

2.5 Analysis required

S-Parameters (SP), Periodic Steady State Analysis (PSS) and P_{noise} analysis available in SpectreRF is used by me to simulate the parameters of LNA. Usually there is more than one method available to simulate the desired parameter. The procedure that takes less simulation time is used by me. The various analyses required are given below:

1. S-Parameter Analysis

- Small Signal Gain (S_{21}, G_A, G_T, G_P)
- Small Signal Stability (K_f and Δ or B_{if})
- Small Signal Noise (SP and P_{noise})
- Input and Output Matching (S_{11}, S_{22}, S_{12})

2. Large Signal Noise and voltage gain Simulation (PSS and P_{noise})

3. 1dB Compression Point and IP3 Simulation (Swept PSS)

2.5.1 S-Parameter Analysis

The S-Parameter analysis is used to compute scattering and noise parameters for n-port circuits that exhibit frequency translation. S-Parameter analysis is used for small-signal and linear noise analyses, where the circuits are linearized around the DC operating point. Such circuits include LNAs, mixers, samplers and other similar circuits. SP analysis also calculates noise parameters in frequency-converting circuits. SP computes noise figure, input referred noise, equivalent noise parameters, and noise correlation matrices. For the SP analysis, I required to specifying the input and output ports and the range of sweep frequencies. After setting SP analysis for the LNA, I can extract and plot the following gain and matching parameters measurements.

- S_{11}, input reflection coefficient
- S_{21}, forward gain
- $S_{12,}$ reverse gain
- S_{22}, output reflection coefficient
- G_T, transducer power gain
- G_P, operating power gain
- G_A, available power gain
- G_{umg}, maximum unilateral power gain
- G_{max}, maximum power gain
- G_{msg}, maximum stability gain

In these plots G_{umx} is very close to G_{max} which means the reverse coupling, S_{12}, is small and G_{msg} is the largest among the above gains. SpectreRF also offers two gain circles.

- GPC draws the G_P contour on the Smith chart of Γ_L
- GAC draws the G_A contour on the Smith chart of Γ_S.

By setting the input and output noise port, I can plot NF and NF_{min} with respect to frequency. The Stern stability factor K_f and Δ can be plotted with respect to frequency. By this analysis, I can plot input and output voltage standing wave ratios (VSWRs) with respect to the frequency sweep.

2.5.2 PSS and P_{noise} Analysis

Use the PSS and P_{noise} analyses for large-signal and nonlinear noise analyses, where the circuits are linearized around the periodic steady-state operating point. As the input power level increases, the circuit becomes nonlinear, the harmonics are generated and the noise

spectrum is folded. Therefore, PSS and P_{noise} analyses are used by me. When the input power level remains low, the NF calculated from the P_{noise}, Noise, and SP analyses should all match. SpectreRF simulation uses a technique called the shooting method to implement PSS analysis. This method is an iterative, time-domain method that finds an initial condition that directly results in a steady-state. It starts with a guess of the initial condition. By the PSS analysis, I can determine the voltage gain of the low noise amplifier. The P_{noise} analysis summary shows you the contributions of different noise sources in the total noise. This is very powerful feature to focus the effort to improve the noise performance of the device which contributes the maximum noise. First PSS analysis is required for the P_{noise} analysis. After the P_{noise} analysis, I can plot the noise figure with respect to frequency.

2.5.3 Swept PSS

After the PSS analysis with swept input power level, plot the output power against the input power level. This plot shows the 1 dB compression point. A two-tone test is used to measure an IP3 curve where the two input tones are ω_1 and ω_2. Since the first-order components grow linearly and third-order components grow cubically, they eventually intercept as the input power level increases. The IP3 is defined as the cross point of the power for the 1st order tones, ω_1 and ω_2, and the power for the 3rd order tones, $2\omega_1 - \omega_2$ and $2\omega_2 - \omega_1$, on the load side. There are three ways to Simulate IIP3, Using Swept PSS, PSS and PAC and QPSS. I used Swept PSS Analysis. Two input frequencies are chosen for the swept PSS. The IPN curves option is selected from the Affirma window. Then IP3 and P1 dB point can be plotted.

CHAPTER 3

DESIGN OF LNA WITH DIFFERENT TOPOLOGIES

In this chapter, the various topologies of LOW NOISE AMPLIFIERS (LNA), single stage LNA, differential LNA and current reuse LNA are introduced. The design equations, schematic and simulated results are also introduced.

3.1 Single-Ended LNA Design

The first topology chosen is a single-ended LNA. The circuit diagram is shown in Figure 3.1. It employs inductive source degeneration (inductor L_S connected to the source of transistor M_1). This method has the advantage that one has a greater control over the value of the real part of the input impedance through the choice of inductance. Cascoding transistor M_2 is used to reduce the interaction of the tuned output with the tuned input. The RF input is coupled to the gate of the amplifier by the coupling capacitance C_0. Transistor M_3 is the biasing transistor and forms a current mirror with transistor M_1. The width of M_3 is kept a small

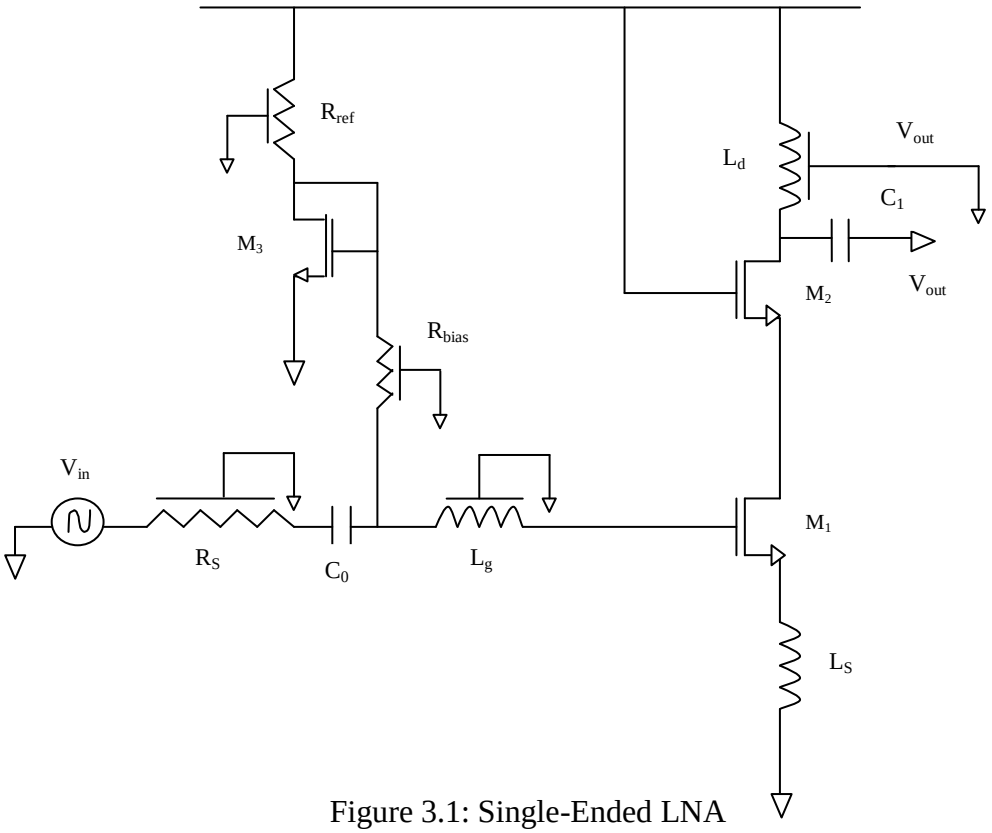


Figure 3.1: Single-Ended LNA

fraction of the width of M_1 to minimize the power overhead of the bias circuit. Output Inductor, L_d resonates with output load to maximize output power transfer and gain at resonance frequency. The width of the cascoded transistor must be sized to trade-off common source gain reduction and increase of parasitic source capacitance of M_2 (both are consequence of a wider M_2). Cascode transistor helps to reduce S_{21} and reduce C_{gd1} Miller effect. R_{bias} is large enough so that its equivalent current noise is small enough to be ignored. L_g is used to set the resonant frequency. The test bench for the simulation of single ended LNA is shown in Figure 3.2.

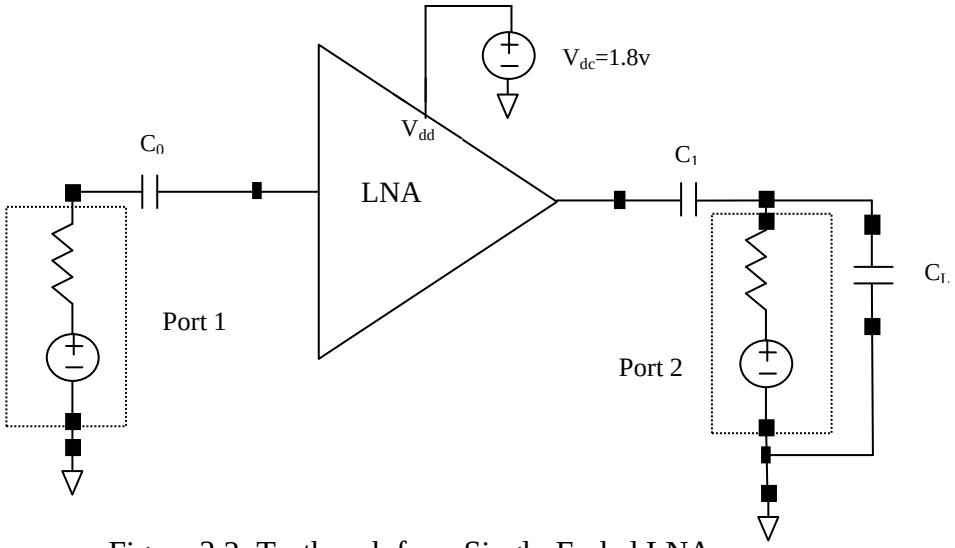


Figure 3.2: Testbench for a Single-Ended LNA

The capacitors are DC decoupling capacitors that eliminate the effect of the port resistor on the LNA's DC bias. They are added when necessary. Below table shows the port parameters which are required to set for the simulation of LNA. For swept PSS analysis two frequencies

Parameter	Port 1	Port 2
Cell name	psin	psin
Frequency Name	frf1	
Resistance	50Ω	50Ω
Port number	1	2
DC voltage	0.7V	
Source type	sine	
Amplitude (dBm)	prf	
Frequency	frf	
AC magnitude	1 V	

Table 3.1: Port parameters of Single-ended LNA

(frf 1, frf 2) are selected in port 1. After the setting of the port parameters, the variables (frf, prf) in the Affirma design variable window is required to assign values. The frequency (frf) is set to 2GHz and prf = -20 dBm.

3.1.1 Basic steps and calculation

The design procedure followed by me for the design of single-ended LNA is Power optimization based. The input impedance for the single stage LNA design is:

$$R_{in} = R_g + \frac{L_S.g_m}{C_{gs}} + j(wL_S - \frac{1}{wC_{gs}}) \quad (3.1)$$

It can be written as,

$$R_{in} = R_g + R_a + j(X_{LS}-X_{CGS}) \quad (3.2)$$

Where,

$$R_a = \frac{L_s.g_m}{C_{gs}}$$

Therefore, the impedance of the MOSFET without feedback is:

$$R_{in} = R_g - jX_{CGS} \rightarrow R_{in} = -jX_{CGS} \quad (3.3)$$

Adding series feedback adds the $R_a + jX_{LS}$ term to the original input impedance. Additionally, another inductor is added in series with the gate L_g that is selected to resonate with the C_{gs} Capacitor. The Input resistance (R_{in}) achieved is: $R_{in} = L_s.g_m / C_{gs}$. Where R_{in} may be say 50 ohms. L_g is designed so that at the resonant frequency it cancels out C_{gs} i.e. $j(wL_S - 1/wC_{gs}) = 0$. In most LNA designs the value of L_s is picked and the values of g_m and C_{gs} are calculated to give the required R_{in}. The design steps followed by me for the design of single-ended low noise amplifier are given below:

1. **Find the optimum device width**: The optimal value of Q in case of power optimization technique is:

$$Q_{L,opt,P_D} = |C|\sqrt{\frac{5\gamma}{\delta}}\left[1 + \sqrt{1 + \frac{3}{|C|^2}\left(1 + \frac{\delta}{5\gamma}\right)}\right] \approx 3.9 \quad (3.4)$$

Where, γ = 2, δ = 4, α =.85. The equation for the device (M_1) width is

$$W_{M1,opt,P_D} = \frac{3}{2C_{ox}LQ_{L,opt,P_D}R_S\omega_0} \quad (3.5)$$

The operating frequency (f_0) is 2.4GHz and ω_0=2×3.14×2.4G=15Grps. The value of R_S is 50Ω.

For 0.18 µm technology,

μ_n =332.1 c.m^2/v/s, C_{ox}=8.221×10^{-15}F/ µm^2, $\mu_n C_{ox}$=273.03µ, L=.18 µm,

So, W_{M1,opt,P_D}=346.55 µm.

2. **Find C_{GS}(Gate-Source capacitance): W**e know,

$$C_{gs1} = \frac{2}{3} C_{ox} \times \mathrm{W_{M1}} \times \mathrm{L_{min}} \tag{3.6}$$

So, $C_{gs1} = \frac{2}{3} \times 8.221 \times 10^{-3} \times 346.55 \times .18 \times 10^{-12} = 0.33\text{PF}$

3. **Find the device transconductance (g_{M1})**

$$g_{M1} = \sqrt{2\mu_n C_{ox} \left(\frac{W}{L}\right)_{M1} I_{DM1}} \tag{3.7}$$

I take I_{DM1}= 5 mA. So, g_{M1}=72.49 mA/V.

4. **Find the transistor unity gain frequency (ω_T)**

$$\omega_T = \frac{g_{M1}}{C_{gs1}} = 219.66\ Grps \tag{3.8}$$

5. **Expected noise figure F_{min,P_D}:**The expected noise figure can be computed by below formula:

$$F_{min\,,P_D} \approx 1 + 2.4\frac{\gamma}{\alpha}\left(\frac{\omega_0}{\omega_T}\right) \geq 1 + 1.62\left(\frac{\omega_0}{\omega_T}\right) \tag{3.9}$$

Where, γ =2 and α=1 So, $F_{min\,,P_D} \approx$ 1.32 dB.

When I_D increase then ω_T increase and NF decreases at the expense of more power.

6. **Starting value of Degeneration Inductor L_S:** The value of this inductor is fairly arbitrary but is ultimately limited on the maximum size of inductance allowed by the technology, which is typically about 10nH.

$$R_s = \frac{g_m L_S}{C_{gs}} = \omega_T L_S \tag{3.10}$$

So, $L_S = \frac{R_S}{w_T}$ =0.227 nH.

7. **Evaluation of L_g:** We know,

$$L_g = \frac{1}{w_o{}^2 C_{gs}} - L_S \tag{3.11}$$

So, L_g =13.4 nH.

8. **Evaluation of L_d:** Here the value of C_L=1 pF

$$L_d = \frac{1}{\omega_0{}^2 C_L} \tag{3.12}$$

So, L_d= 4.44 nH.

9. **Width of transistors:** Size of M_3 is chosen to minimize power consumption. So W_{M3} = 60 µm. size of M_1 = M_2, So that they can have shared drain area. It can reduce the

impedance looking into gate and drain of M_1 degrading the input match and noise performance, so both transistors sizes are to made equal. Transistor M_2 is used to reduce the miller effect.

10. **Value of bias resistor:** R_{bias} must be large enough so that it's equivalent current noise can be neglected. So, R_{bias}=2KΩ.
11. **Calculation of power dissipation (P_d) :**We know,

$$P_d = V_{dd} I_D \quad (3.13)$$

So, $P_d = 1.8 \times 5 \times 10^{-3} = 9$ mW.

From the analysis and iterative simulations of single-ended LNA, the components values of LNA are optimized and summarized in Table 3.2.

Component	Theoretically calculated value	Experimentally optimized valued	Functionality
M_1, M_2	346.55 µm	300.00 µm	Amplify the RF signal
M_3	60 µm	60 µm	DC bias current mirror
L_g	13.4 nH	11.25 nH	Input matching
L_s	0.227 nH	0.283 nH	Input matching
L_d	4.44 nH	3.69 nH	Output matching
C_0	2pF	2.49pF	Input matching
C_1	2pF	1.612pF	Output matching
R_{bias}	2KΩ	2.008KΩ	Reduce the input noise from DC bias circuit
R_{ref}	2KΩ	2.008KΩ	DC bias

Table 3.2: Component values of single-ended LNA

3.1.2 Schematic and simulation results

Using the library UMC_18_CMOS for 0.18µm technology in cadence, the schematic of single ended LNA on Virtuoso schematic editor tool was created as shown in Figure 3.3. The RF transistor models, inductor models, capacitor models and resistor models are provided by library UMC_18_CMOS in 0.18 µm technology, which are mentioned in the above section. The simulation includes DC simulation, S-parameter simulation, P_{noise}, PSS and swept PSS simulation as described above in chapter 2. From DC simulation the power consumption is got. The transistors operation points are optimized from DC simulation. It is important to give the larger gain for LNA design with the optimum operation point.

Schematic of single ended LNA: Figure 3.3 shows the schematic of single-ended LNA on Cadence-Virtuoso tool. The widths of the transistors are increased by arranging the various transistors in parallel.

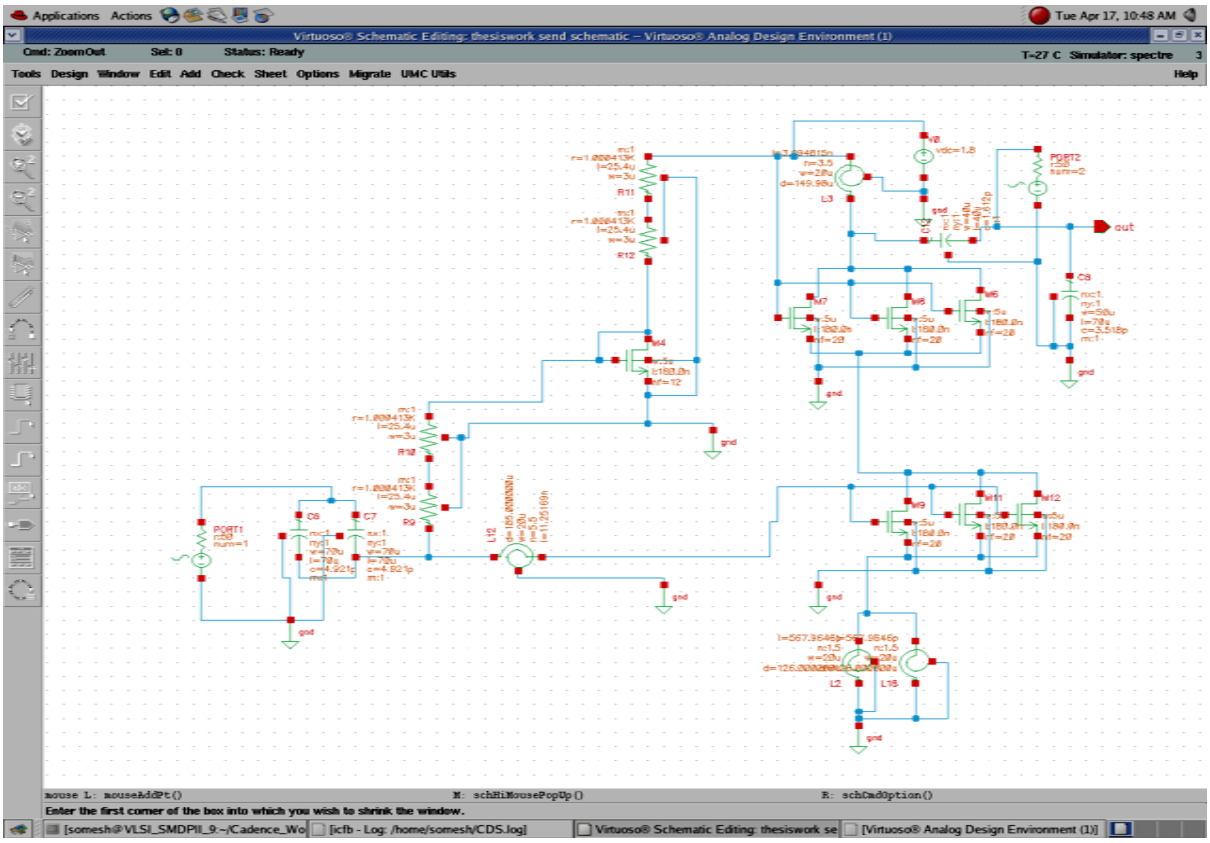


Figure 3.3: Schematic of Single-Ended LNA.

The various simulation iterations are performed on the proposed LNA circuit to meet design

Performance Parameter	Value	Unit
Noise Figure (NF_{min})	2.49	dB
Noise Figure (NF)	2.965	dB
Voltage Gain	16.7	dB
Power Gain (S_{21})	18.22	dB
S_{22}	-12.21	dB
S_{11}	-8.032	dB
S_{12}	-40.86	dB
I_D	4.5	mA
Power consumption	8.1	mW
K_f	5.391	
B_{if}	1.055	
r_n	0.6461	Ω
1-dB Point	-19.3297	dBm
IP3 Point	-10.3012	dBm
Total input referred noise	3.971×10^{-19}	V^2/Hz

Table 3.3: Performance parameters of the Single Ended LNA (RF frequency 2GHz)

requirements. The simulation results of single-ended LNA achieved at the typical process are summarized in the Table 3.3.

Waveforms of single-ended LNA: The simulated curves of noise figure, input/output matching, and gain for S-parameters are shown in Figure 3.4.

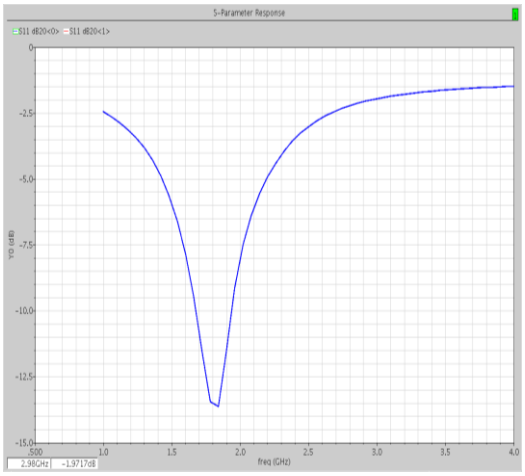


Figure 3.4(a): S11 plot for Single Ended LNA.

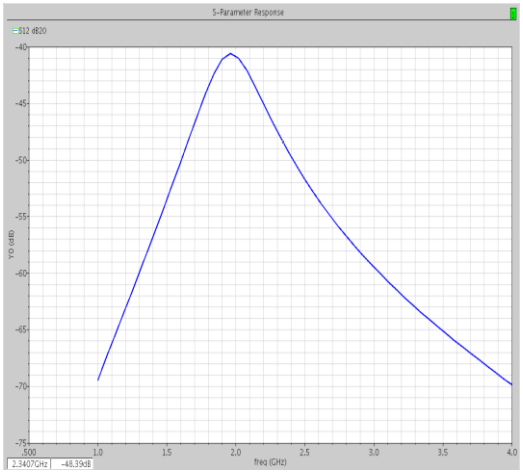


Figure 3.4(b): S12 plot for Single Ended LNA.

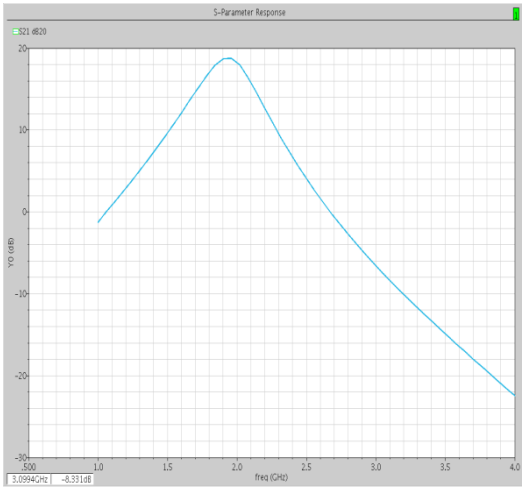


Figure 3.4(c): S21 plot for Single Ended LNA.

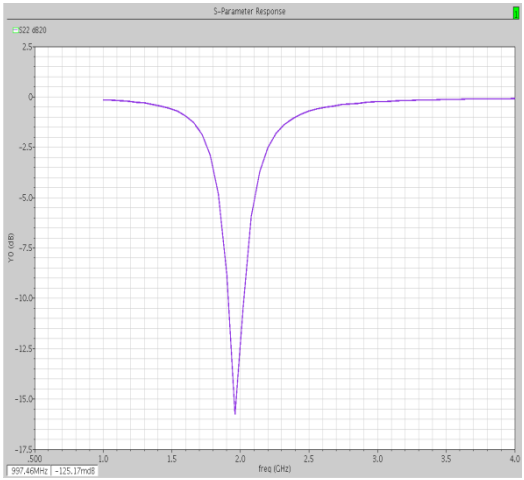


Figure 3.4(d): S22 plot for Single Ended LNA.

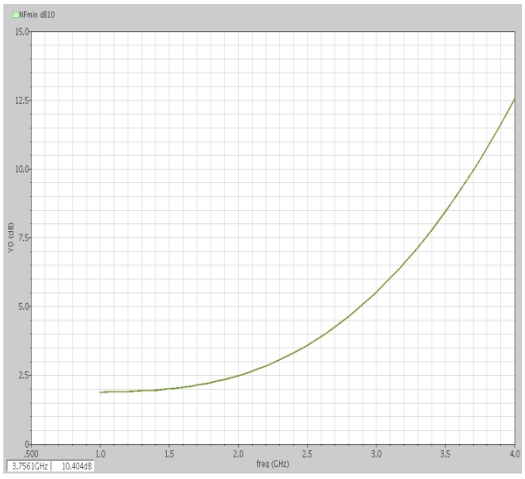


Figure 3.4(e): NF_{min} plot for Single Ended LNA.

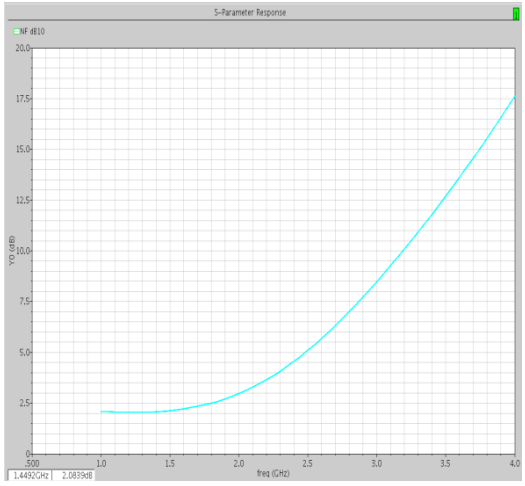


Figure 3.4(f): NF plot for Single Ended LNA

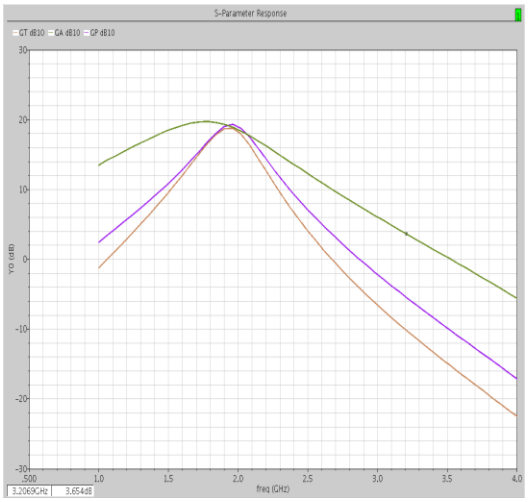


Figure 3.4(g): G_T, G_A, G_P plot for Single Ended LNA.

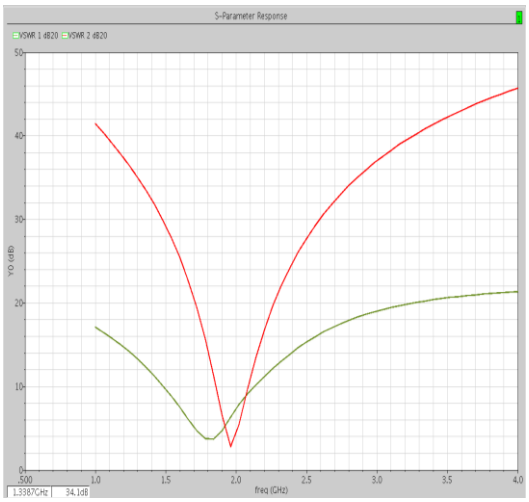


Figure 3.4(h): VSWR plot for Single Ended LNA.

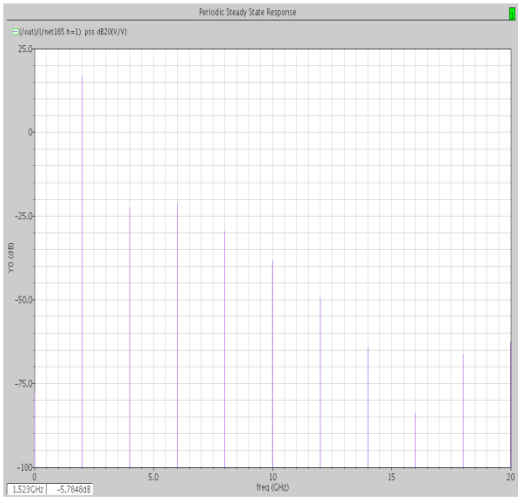


Figure 3.4(i): Voltage gain plot for Single Ended LNA.

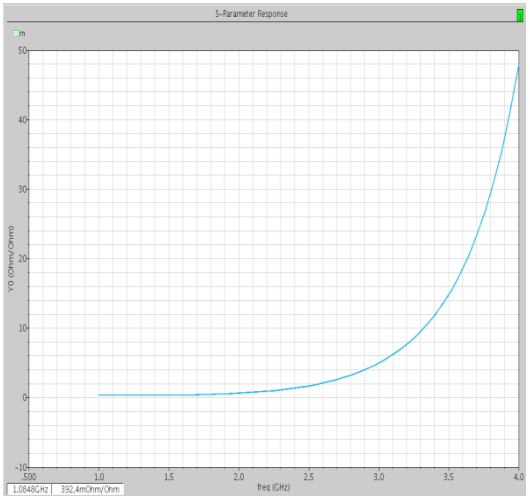


Figure 3.4(j): r_n plot for Single Ended LNA.

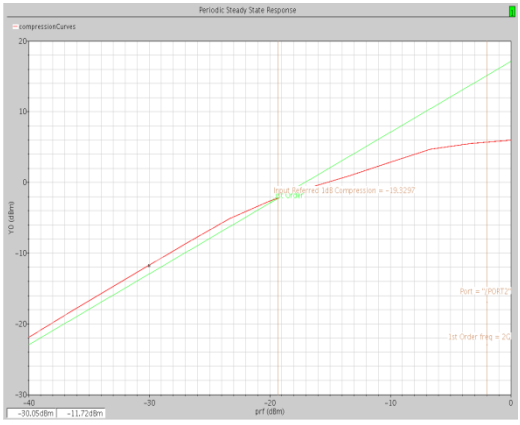


Figure 3.4(k): 1-dB plot for Single Ended LNA.

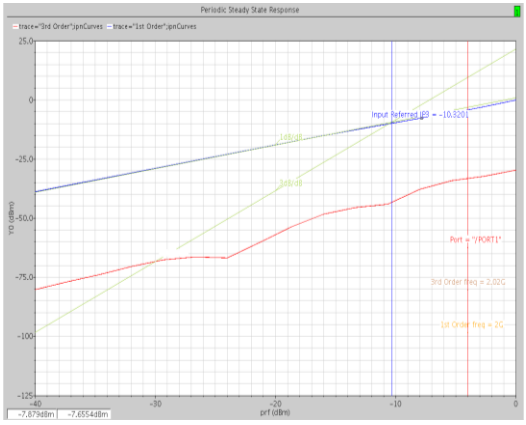


Figure 3.4(l): IP_3 plot for Single Ended LNA.

Figure 3.4: Simulated curves of Single Ended LNA.

3.2 Differential LNA Design

Differential circuits are an important part of integrated circuit design because they offer several important advantages over single-ended circuits. The first important advantage is the differential LNA offers a stable reference point. With any type of circuit, the measured values are always taken with respect to a reference. In the differential LNA the measured results of one-half circuit are always taken with respect to other half circuit. Another significant and relevant benefit of using a differential circuit is noise reduction. Differential LNA can restrain common mode interference, so the noise of source voltage and underlay voltage can also be restrained.

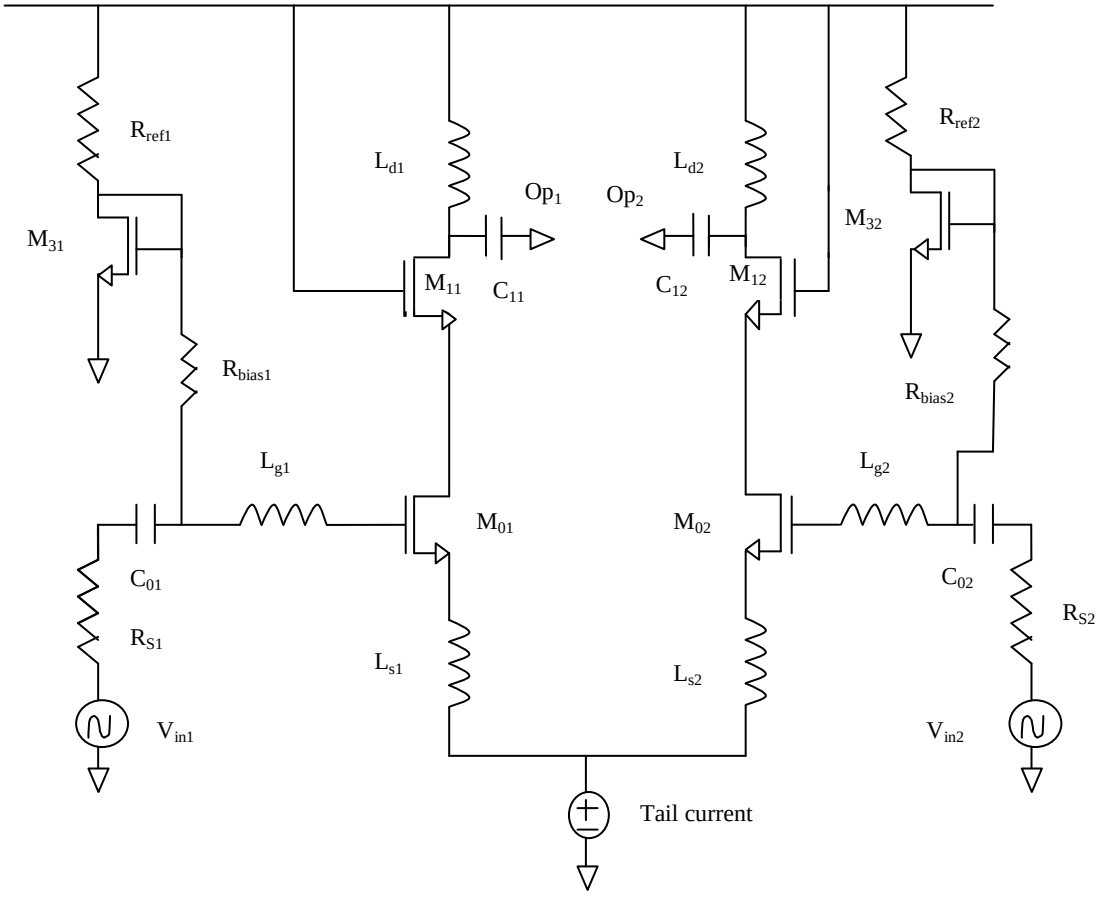


Figure 3.5: Differential LNA

The virtual ground formed at the tail removes the sensitivity to parasitic ground inductances which makes the real part of the input impedance purely controlled by source degeneration inductance (L_s). Provided the noise source at the input of the amplifier is distributed equally between the incoming signal lines such that they see the same input noise, the noise will not be amplified by the same gain factor as the input signals. In order to make the differential LNA circuit, two single-ended circuits built, where each transistor and circuit component has

a complimentary transistor or component. The positive input voltage is measured at the gate of one of the half-circuit CS amplifiers, while the negative input voltage is measured at the gate of the other half-circuit. The overall output of the LNA is measured between the sources of each half-circuit. In this case, it is now the difference between the two input signals that is being amplified. In the differential LNA the power consumed is twice of the single ended LNA because the current flow is twice of the single-ended LNA. The complete differential LNA is shown in Figure 3.5. The test bench for the simulation of single ended LNA is shown below in Figure 3.6.

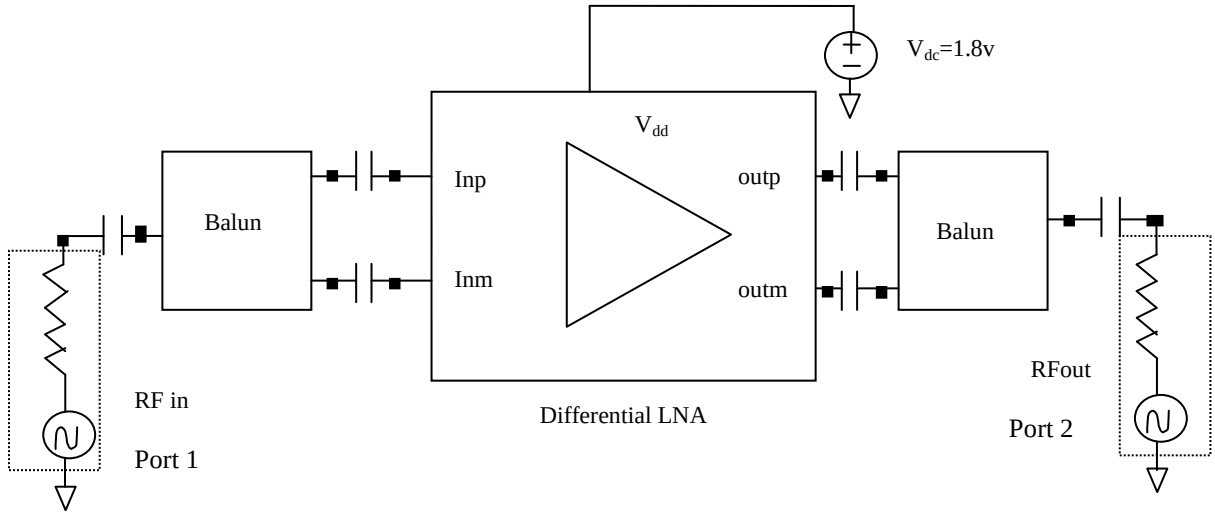


Figure 3.6: Testbench for a Differential LNA

To supply a differential signal to each LNA input, an 'ideal' balun (balanced to unbalanced) transformer has been used (The two AC sources each set to some voltage and opposite polarity can be used). In addition another balun is used on the amplifier output to re-combine the signal to allow the voltage gain to be simulated. When balun is not used at the output then two ports are required at the output. The parameters selected for three ports differential LNA is given below in table 3.4.

Parameter	Port 1	Port 2	Port 3
Cell name	psin	psin	psin
Frequency Name	frf1		
Resistance	50Ω	50Ω	50Ω
Port number	1	2	3
DC voltage	0.7V		
Source type	sine		
Amplitude (dBm)	prf		
Frequency	frf		
AC magnitude	1V		

Table 3.4: Port parameters of Differential LNA

After the setting of the port parameters, the variables (frf, prf) in the Affirma design variable window is required to assign values. The frequency (frf) is set to 2GHz and prf = -20 dBm. For swept PSS analysis two frequencies (frf 1, frf 2) are selected in port 1.

3.2.1 Basic steps and calculation

The steps followed for the design of the differential LNA is same as single ended LNA. It comprises of two single-ended configurations connected back to back. It contains a tail current source which contains the twice of the current of single ended LNA. So, the power consumption of the differential LNA is twice of the single ended LNA. From the analysis and iterative simulations of differential LNA with balun, the components values of LNA are optimized and summarized in Table 3.5.

Component	Theoretically calculated value	Experimentally optimized valued	Functionality
$M_{01}= M_{02}$, $M_{11}= M_{12}$	346.55 µm	300.00 µm	Amplify the RF signal
$M_{31}= M_{32}$	60 µm	60 µm	DC bias current mirror
$L_{g1}= L_{g2}$	13.4 nH	11.25 nH	Input matching
$L_{s1}= L_{s2}$	0.227 nH	0.282 nH	Input matching
$L_{d1}= L_{d2}$	4.44 nH	3.14 nH	Output matching
$C_{01}= C_{02}$	2pF	1.841pF	Input matching
$C_{11}= C_{12}$	2pF	1.512 pF	Output matching
$R_{bias1}= R_{bias2}$	2KΩ	2.008KΩ	Reduce the input noise from DC bias circuit
$R_{ref1}= R_{ref2}$	2KΩ	2.008KΩ	DC bias

Table 3.5: Component values of differential LNA

3.2.2 Schematic and simulation results

Using the library UMC_18_CMOS for 0.18µm technology in cadence, the schematic of differential LNA on Virtuoso schematic editor tool is created as shown in Figure 3.7. The RF transistor models, inductor models, capacitor models and resistor models are provided by library UMC_18_CMOS in 0.18 µm technology, which are mentioned in the above section. The simulation includes DC simulation, S-parameter simulation, P_{noise} , PSS and swept PSS simulation as described above in chapter 2. From DC simulation the power consumption is calculated. The transistors operation points are optimized from DC simulation. It is important to give the larger gain for LNA design with the optimum operation point.

Schematic of Differential LNA: Below two Figures shows the schematic of Differential LNA on Cadence-Virtuoso tool. First Figure 3.7 shows the schematic of LNA without balun transformer and second Figure 3.8 shows the schematic of differential LNA with balun transformer. The widths of the transistors are increased by arranging the various transistors in parallel. The simulation results of differential LNA achieved are summarized in the Table 3.6

Performance Parameter	Value	Unit
Noise Figure (NF_{min})	2.67	dB
Noise Figure (NF)	3.775	dB
Voltage Gain	18.67	dB
Power Gain (S_{21})	15.87	dB
S_{22}	-14.15	dB
S_{11}	-9.842	dB
S_{12}	-42.86	dB
I_D	9	mA
Power consumption	16.2	mW
K_f	3.221	
B_{if}	0.255	
r_n	1.101	Ω
1-dB Point	-12.5176	dBm
IP3 Point	-2.86127	dBm
Total input referred noise	5.05394×10^{-19}	V^2/Hz

Table 3.6: Performance parameters of the differential LNA (RF frequency 2GHz).

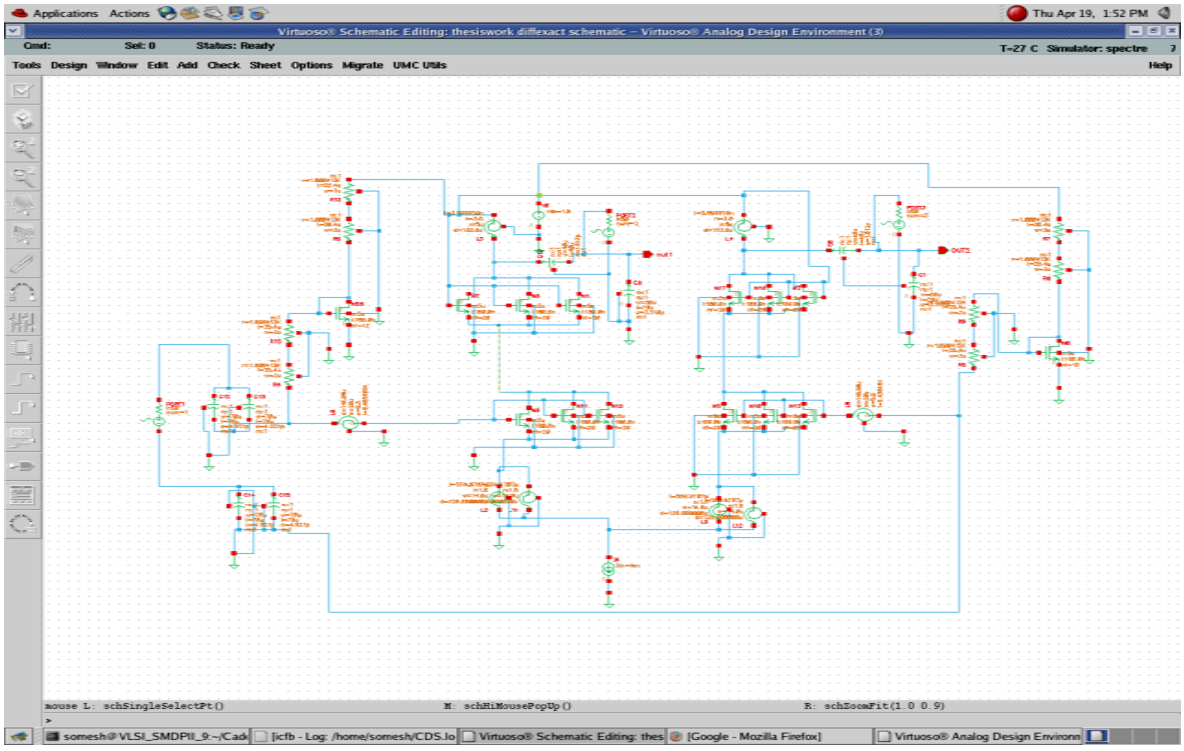


Figure 3.7: Schematic of differential LNA without Balun circuit.

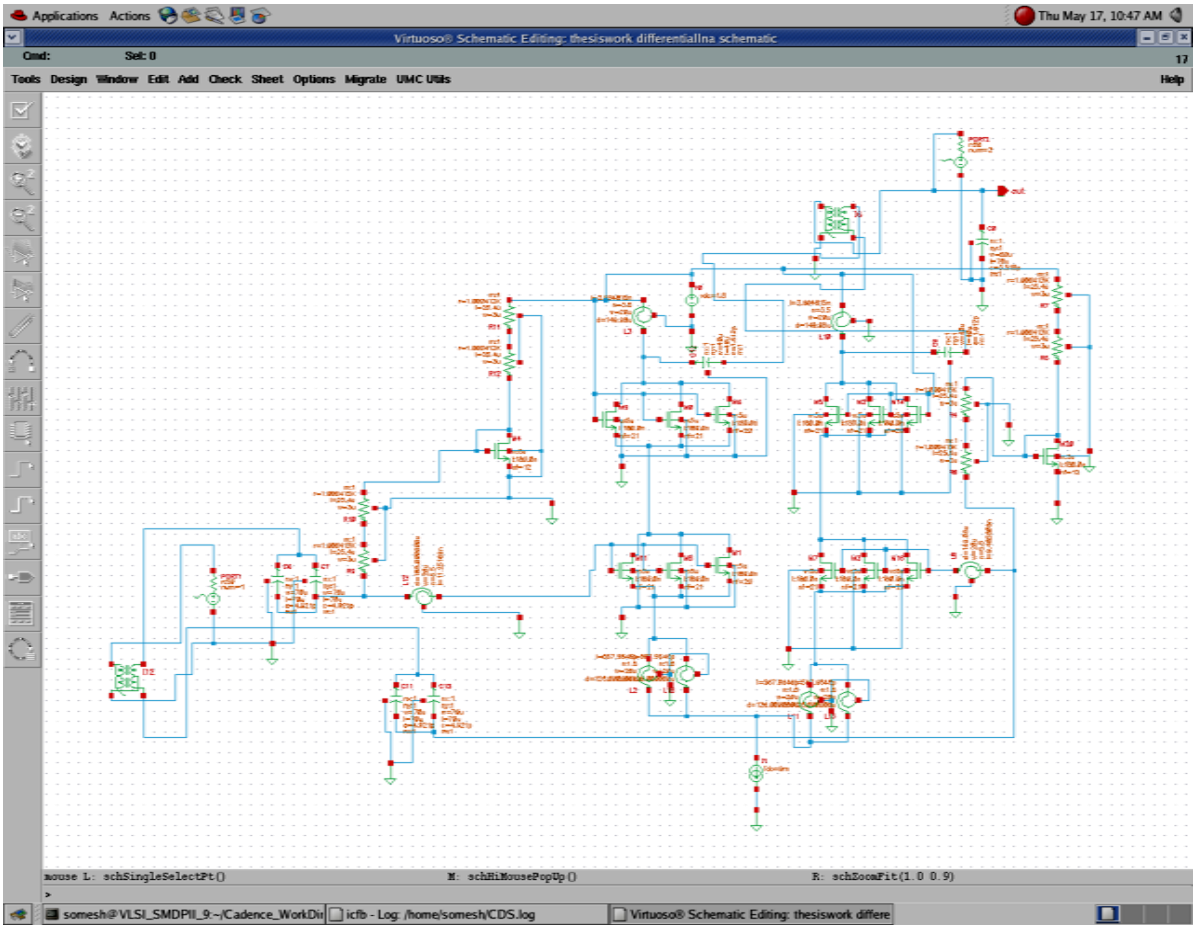


Figure 3.8: Schematic of differential LNA with Balun circuit.

The various simulation iterations are performed on the proposed LNA circuit to meet design requirements.

Waveforms of Differential LNA: The simulated curves of noise figure, input/output matching, and gain for S-parameters are shown in Figure 3.9.

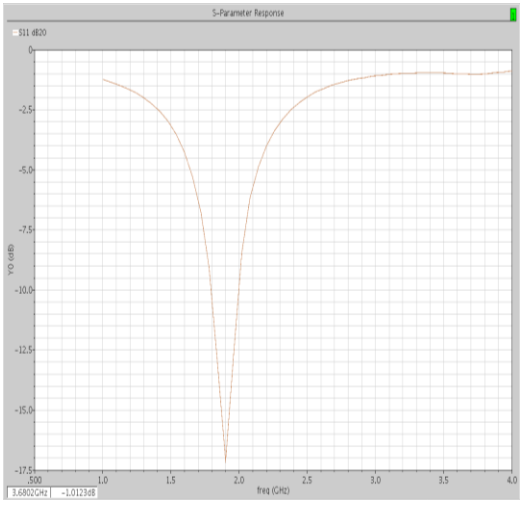


Figure 3.9(a): S11 plot for Differential LNA

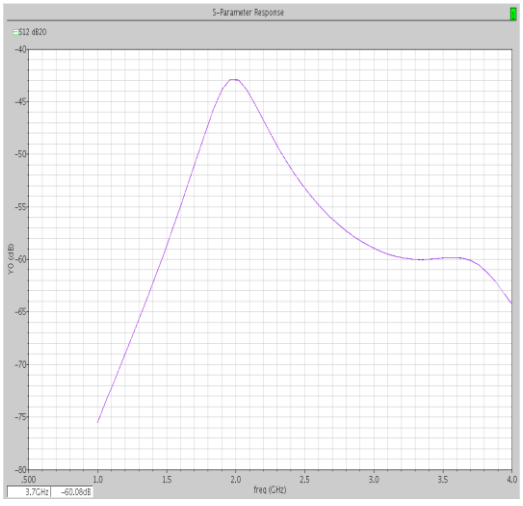


Figure 3.9(b): S12 plot for Differential LNA

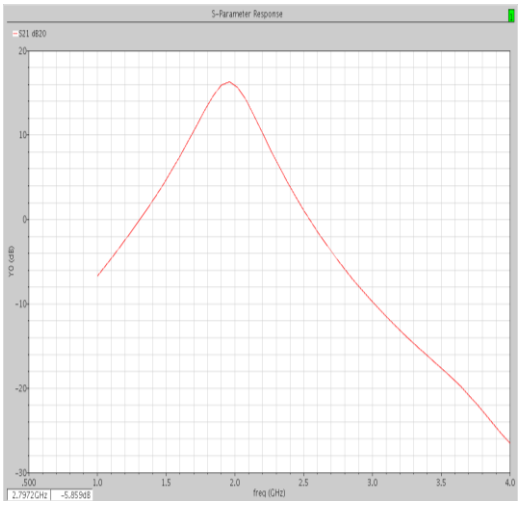


Figure 3.9(c): S21 plot for Differential LNA

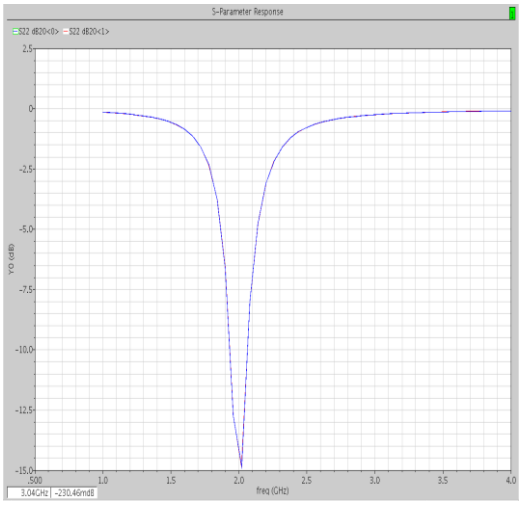


Figure 3.9(d): S22 plot for Differential LNA

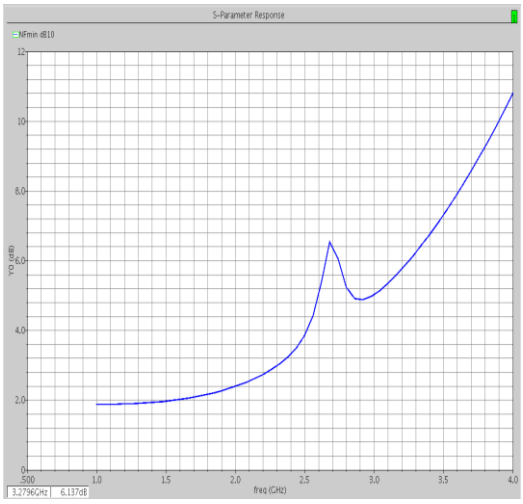


Figure 3.9(e): NF_{min} plot for Differential LNA

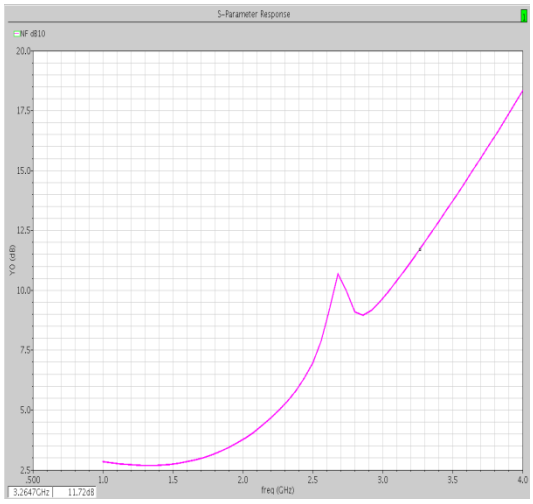


Figure 3.9(f): NF plot for Differential LNA

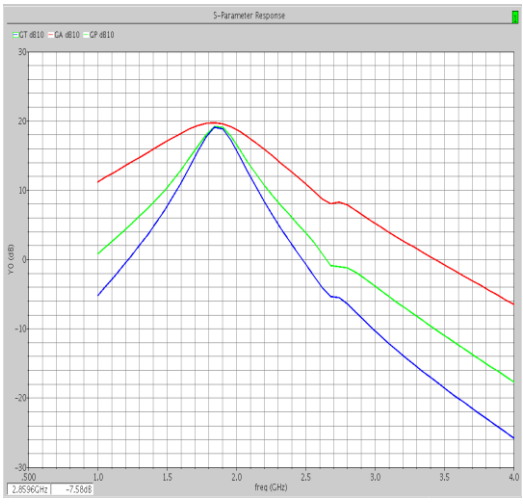


Figure 3.9(g): G_T, G_A, G_P plot for Differential LNA.

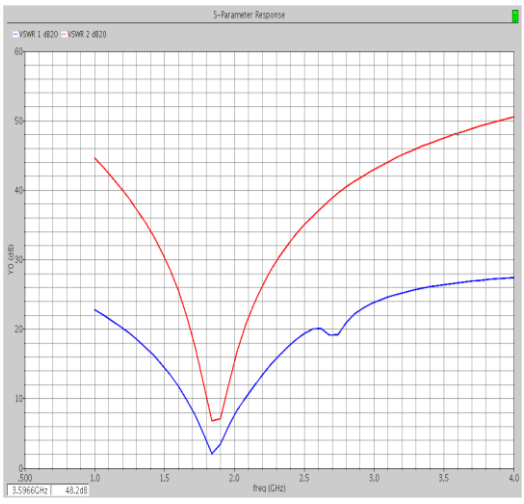


Figure 3.9(h): VSWR plot for Differential LNA

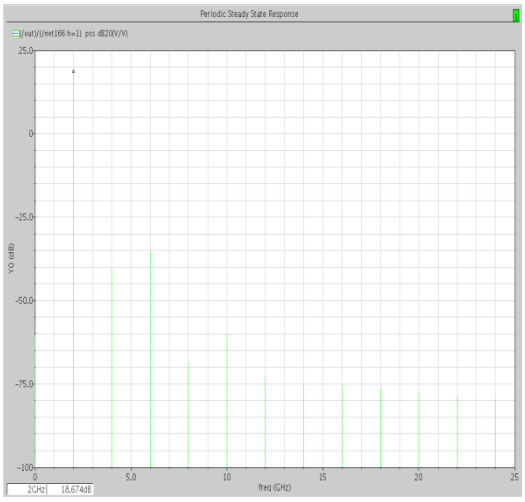


Figure 3.9(i): Voltage gain plot for Differential LNA.

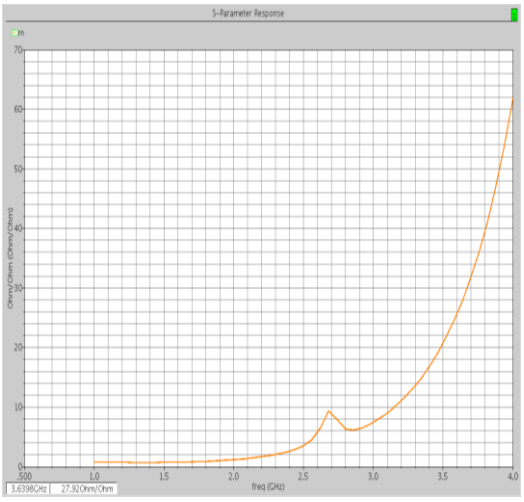


Figure 3.9(j): r_n plot for Differential LNA

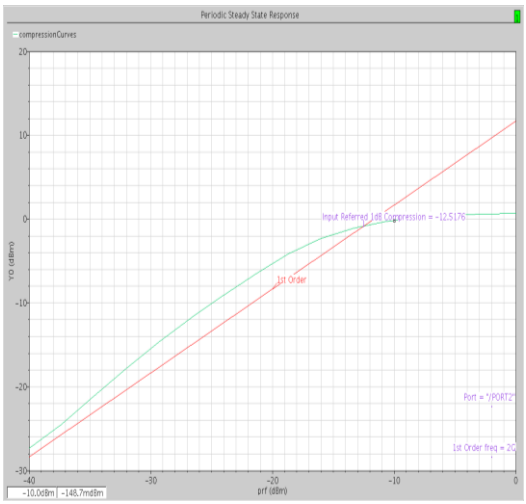


Figure 3.9(k): 1-dB plot for Differential LNA.

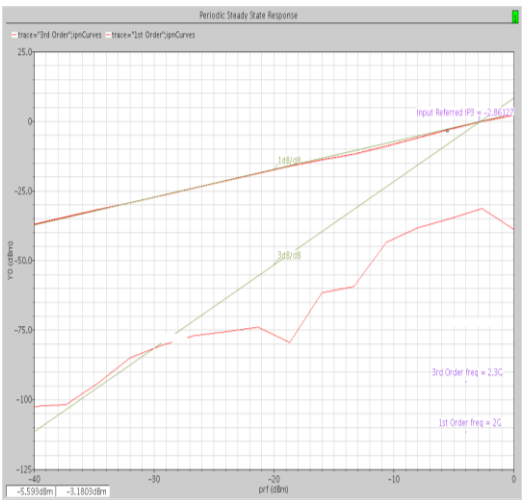


Figure 3.9(l): IP_3 plot for Differential LNA

Figure 3.9: Simulated curves of Differential LNA

3.3 Current Reuse LNA (CRLNA) Design

CRLNA is mainly used for low power. The current reuse means to recycle the bias current so that it can be used by more than one stage. The basic issue with using a CMOS transistor for the LNA is its inherently low transconductance and hence low gain. However if the current reuse technique is employed, transconductance could be increased as much as two fold. The key point is that given the same bias current the effective transconductance is $g_{M1}+ g_{M2}$, while it is simply g_{M1} in single ended topology.

A major drawback of this design is its high input and output impedance, thus requiring external matching networks. This prevents the use this LNA in fully integrated applications. Due to high gain property, the strong miller effect reduces the reverse isolation of LNA. In the actual design, two identical stages are cascaded to improve the reverse isolation. Below

Figure 3.10 shows the basic circuit of the current reuse LNA. When the amplifier is designed with optimized parameter, a broadband input matching network is required to generate good return loss performance across the entire bandwidth without adding noise. Using the current reuse technology, one amplifying stage is placed on the top of the other. Apropos, the cascode configuration is used for LNA. With this approach, higher gain has been obtained without both, usage of the cascade configuration and increase in consumption as two amplifier stages have the same bias current ($P_D = V_{dd} I_D$). Since it is required for the LNA to have high gain and good circuit stability, cascode amplifier (M_1 and M_2 transistors) is the main contributor to the overall LNA gain. Besides high gain, the cascade amplifier provides high output impedance and good input to output isolation. As drain AC load of transistor M_1 in the cascode amplifier is approximately $1/g_{m2}$ (input impedance of transistor M_2, common gate CG amplifier), drain M_1 represents low impedance point. As transistor M_1 gate to drain gain is small, effect of Miller gate-drain overlap capacitance can be neglected. Additional amplifying stage (transistor M_3) has common source topology in case capacitor C_i , i =1,2 is large. Resistor R_S represents source output impedance (the most usual value is 50 Ω). For providing a good input matching the inductive source degeneration with inductor L_S is used. Additional degree of freedom, while setting resonant frequency ω_0, is introduced with inductor L_g . Bias circuit consists of transistor M_4 and resistor R_{ref}. The resistor R_{bias} is chosen large enough to represent high impedance to the carrier that prevents AC signal flow to the bias circuit, giving at the same time small contribution to the overall circuit noise. Voltage V_{bias} is transistor M_2 bias voltage. Large capacitor C_1 enables coupling of two amplifier stages by transmitting signal from M_2 transistor drain to M_3 transistor gate. Moreover, capacitor C_2 should have the highest possible value to provide the ideal AC ground for the second amplifier stage. Inductors L_1, L_2 and L_{out} represent loads of first and second amplifier stage. Capacitors C_g and C_b are input and output blocking capacitors.

From the LNA topology it can be seen that the total node capacitance at the drain of M_3 is parallel of capacitance C_d and transformed capacitance C_b. This equivalent capacitance forms parallel resonant circuit with inductance L_{out} both to provide highly desirable band-pass filtering of output signal and increase gain at the center frequency. The test bench for the simulation of CRLNA is shown the Figure 3.11. The capacitors are DC decoupling capacitors that eliminate the effect of the port resistor on the LNA's DC bias. They are added when necessary. Below table shows the port parameters which are required to set for the simulation of LNA. For swept PSS analysis two frequencies (frf1, frf2) are selected in port 1.

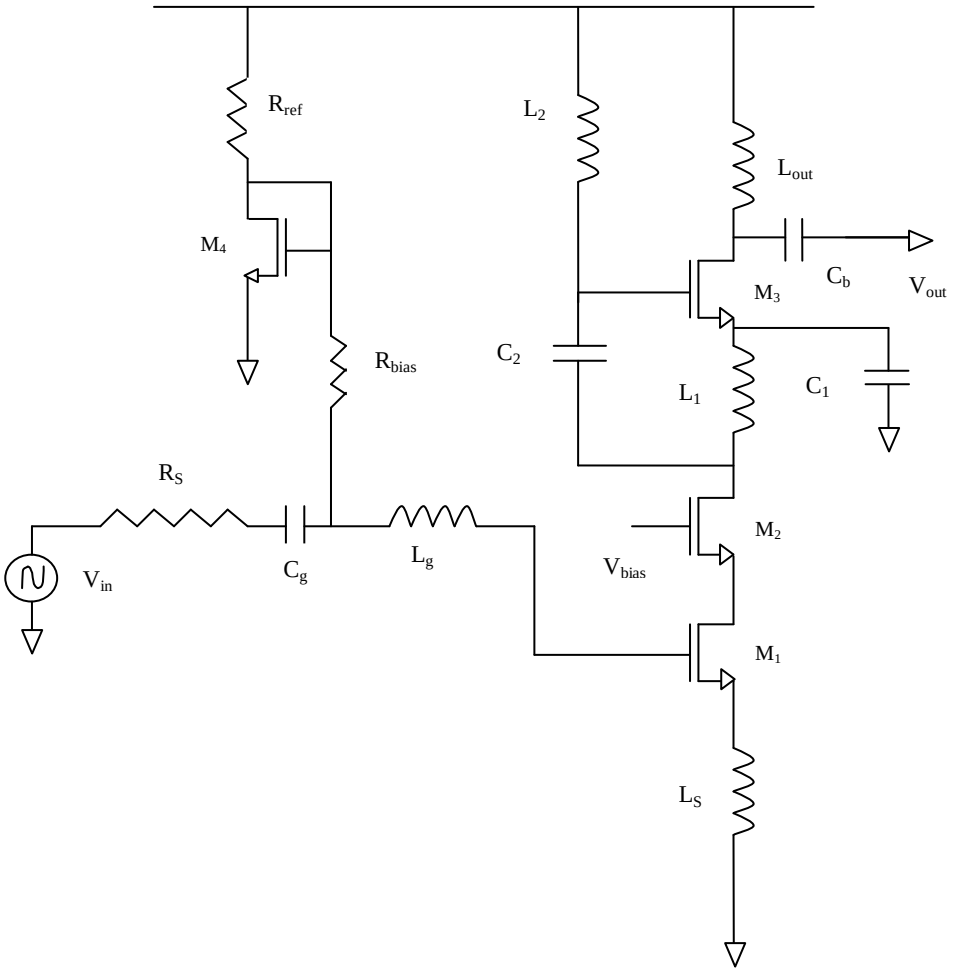


Figure 3.10: Current reuse LNA (CRLNA)

After the setting of the port parameters, the variables (frf, prf) in the Affirma design variable window is required to assign values. The frequency (frf) is set to 2GHz and prf = -20 dBm.

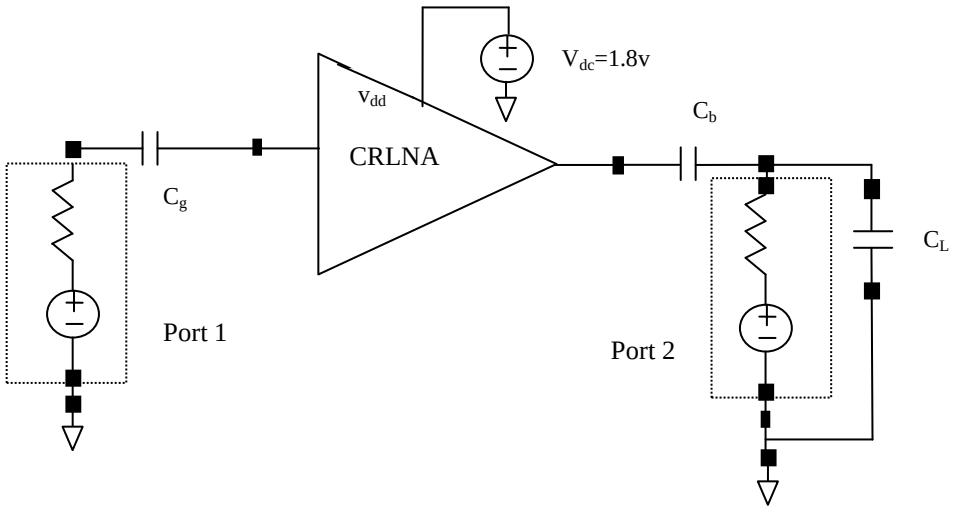


Figure 3.11: Testbench of Current reuse LNA (CRLNA).

Parameter	Port 1	Port 2
Cell name	psin	psin
Frequency Name	frf1	
Resistance	50Ω	50Ω
Port number	1	2
DC voltage	0.7V	
Source type	sine	
Amplitude (dBm)	prf	
Frequency	frf	
AC magnitude	1 V	

Table 3.7: Port parameters of CRLNA

3.3.1 Basic steps and calculation

The steps followed for the CRLNA is same as single ended LNA. It comprises of an extra transistor M_2 with biasing V_{bias}. For the high gain the biasing voltage of M_2 should be as large as possible. Large capacitor C_1 is added that enables coupling of two amplifier stages by transmitting signal from M_2 transistor drain to M_3 transistor gate. From the analysis and iterative simulations of differential LNA, the components values of LNA are optimized and summarized in Table 3.8.

Component	Theoretically calculated value	Experimentally optimized valued	Functionality
M_1, M_3	346.55 µm	300 µm	Amplify the RF signal
M_2	300 µm	300 µm	Amplify the RF signal
M_4	60 µm	60 µm	DC bias current mirror
L_g	13.4 nH	15.9851 nH	Input matching
L_s	0.227 nH	0.283 nH	Input matching
L_2	10 nH	4.0725 nH	Increase gain
L_1	10 nH	14.5 nH	Increase the gain
L_{out}	5 nH	3.376 nH	Output matching
C_g	2pF	2.5 pF	Input matching
C_b	2pF	2.010pF	Output matching
C_2	5pF	3.518pF	provide the ideal AC ground
R_{bias}	2KΩ	2.008KΩ	Reduce the input noise from DC bias circuit
R_{ref}	2KΩ	2.008KΩ	DC bias

Table 3.8: Component values of CRLNA.

3.3.2 Schematic and simulation results

Using the library UMC_18_CMOS for 0.18μm technology in cadence, the schematic of CRLNA on Virtuoso schematic editor tool is created as shown in Figure 3.12. The RF transistor models, inductor models, capacitor models and resistor models are provided by library UMC_18_CMOS in 0.18 μm technology, which are mentioned in the above section. The simulation includes DC simulation, S-parameter simulation, P_{noise} and PSS simulation as described above in chapter 2. From DC simulation the power consumption is calculated. The transistors operation points are optimized from DC simulation. It is important to give the larger gain for LNA design with the optimum operation point. The current flow through the circuit of current reuse low noise amplifier is 3.312mA and the supply voltage is 1.8V. So the power consumption of the current reuse low noise amplifier is 5.958mW. The bandwidth of the current reuse low noise amplifier measured from the sp analysis is 1.051×10^{9}. By the P_{noise} analysis the noise contribution by the each component of current reuse low noise amplifier can be printed. From the noise summary the maximum noise is contributed by the inductors and input port.

Schematic of CRLNA: Figure 3.12 shows the schematic of current-reuse LNA on Cadence-Virtuoso tool. The widths of the transistors are increased by arranging the various transistors in parallel. The biasing voltage applied to transistor M_2 for minimum power consumption is 1.4V. The simulation results of current-reuse LNA achieved are summarized in the Table 3.9.

Performance Parameter	Value	Unit
Noise Figure (NF_{min})	2.663	dB
Noise Figure (NF)	3.034	dB
Voltage Gain	19.96	dB
Power Gain (S_{21})	23.41	dB
S_{22}	-12.01	dB
S_{11}	-12.49	dB
S_{12}	-72.86	dB
I_D	3.312	mA
Power consumption	5.958	mW
K_f	116.9	
B_{if}	0.9711	
r_n	0.6214	Ω
1-dB Point	-25.9921	dBm
IP3 Point	-16.4029	dBm
Total input referred noise	7.818×10^{-18}	V^2/Hz

Table 3.9: Performance parameters of the current-reuse LNA (RF frequency 2GHz)

The gain (S_{21}) obtained from the simulation of current reuse low noise amplifier is above 20 dB. The power consumption is also less than single-ended LNA and differential low noise amplifier. The various simulation iterations are performed on the proposed LNA circuit to meet design requirements.

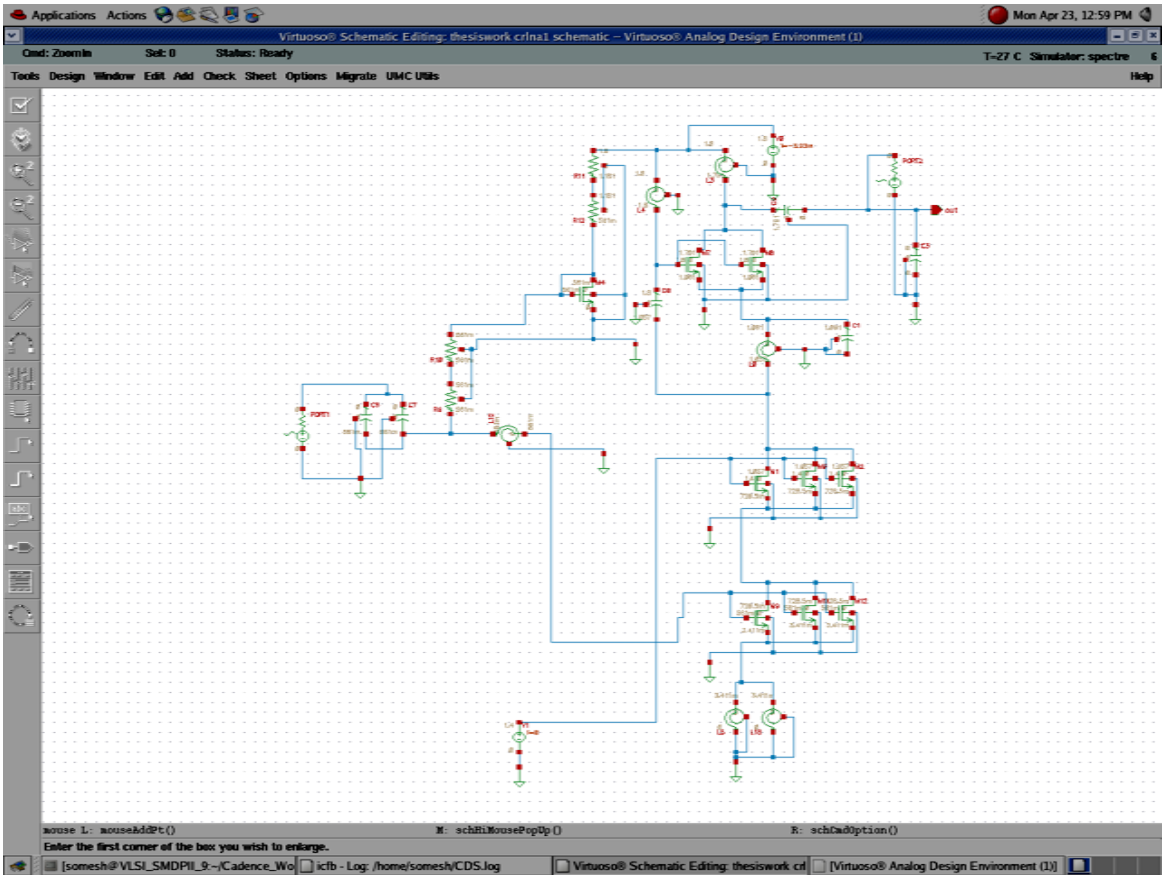


Figure 3.12: Schematic of current-reuse LNA.

Waveforms of CRLNA: The simulated curves of noise figure, input/output matching, and gain for S-parameters are shown in Figure 3.13.

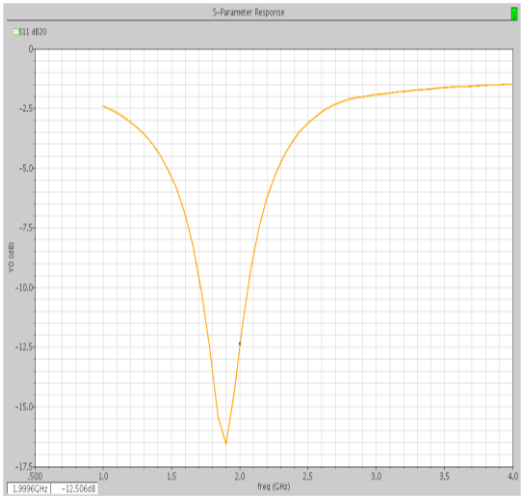


Figure 3.13(a): S11 plot for current-reuse LNA

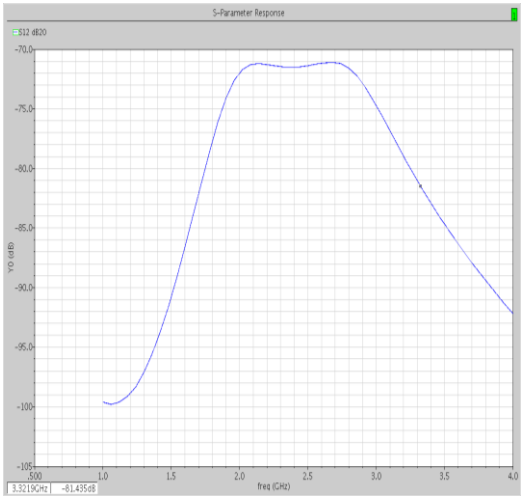


Figure 3.13(b): S12 plot for current-reuse LNA

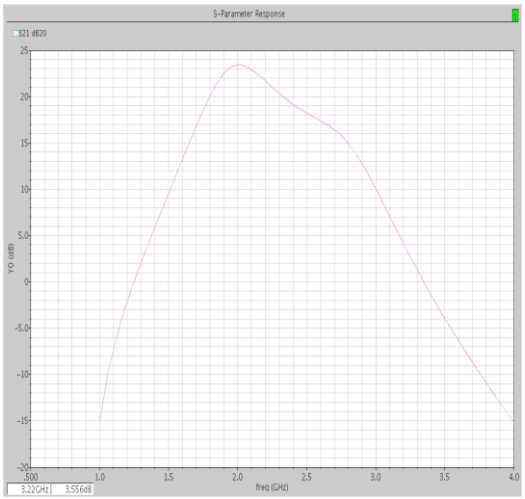


Figure 3.13(c): S21 plot for current-reuse LNA

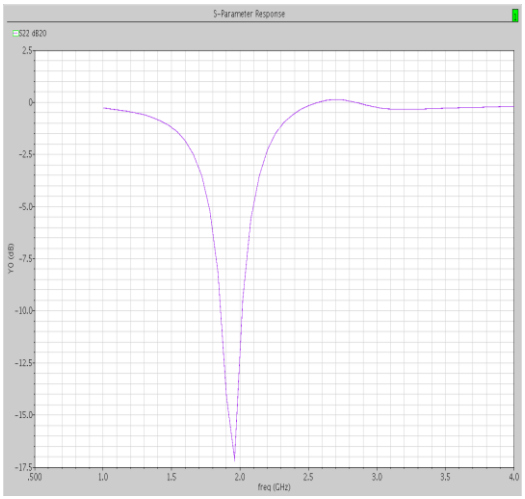


Figure 3.13(d): S22 plot for current-reuse LNA

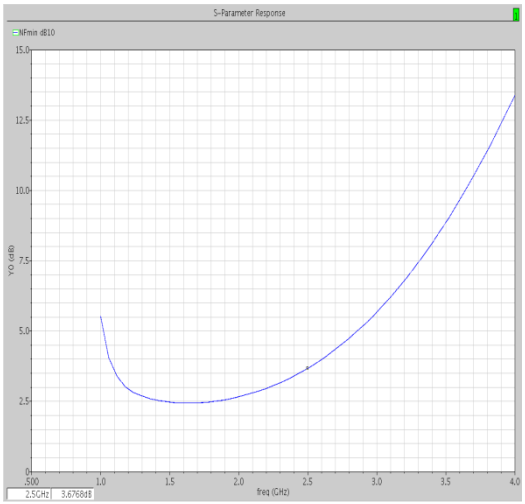


Figure 3.13(e): NF_{min} plot for current-reuse LNA

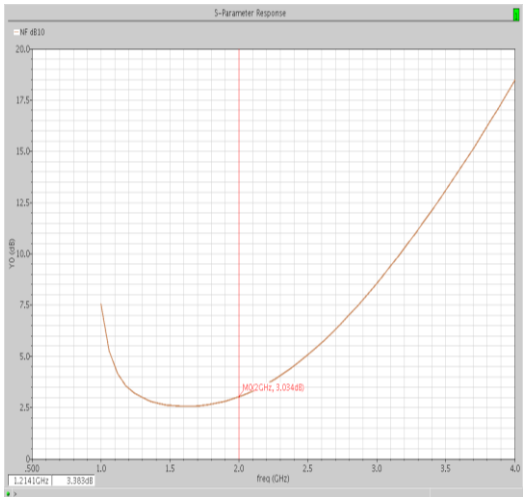


Figure 3.13(f): NF plot for current-reuse LNA

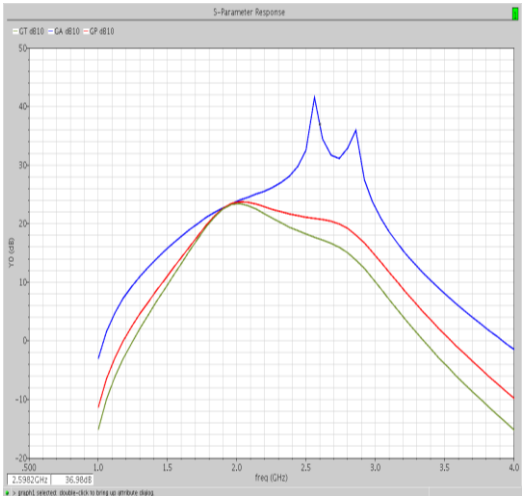


Figure 3.13(g): G_T, G_A, G_P plot for current-reuse LNA.

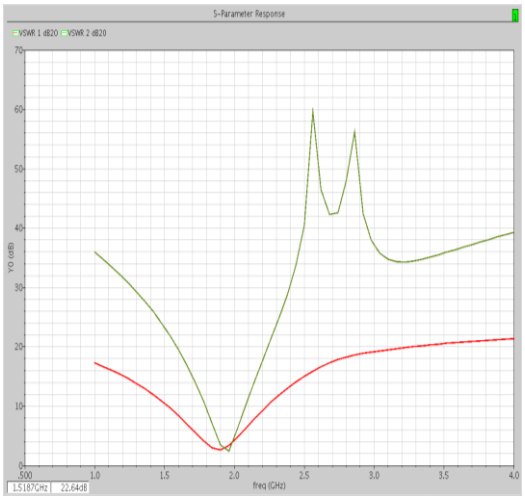


Figure 3.13(h): VSWR plot for current-reuse LNA

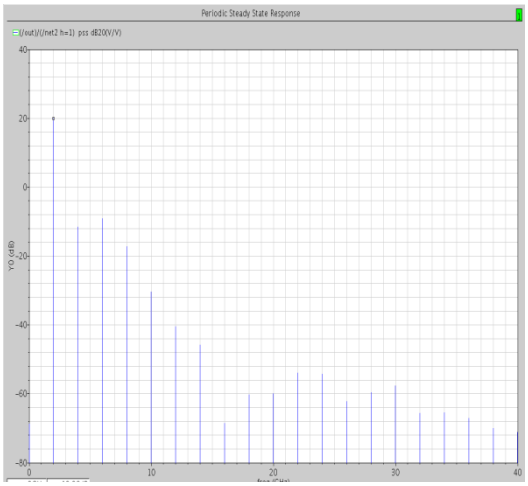


Figure 3.13(i): Voltage gain plot for current-reuse LNA.

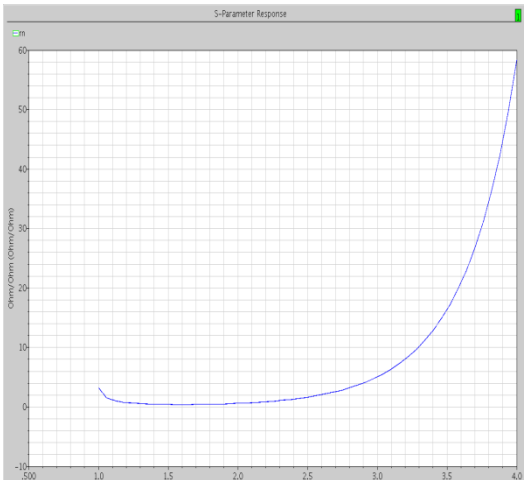


Figure 3.13(j): r_n plot for current-reuse LNA

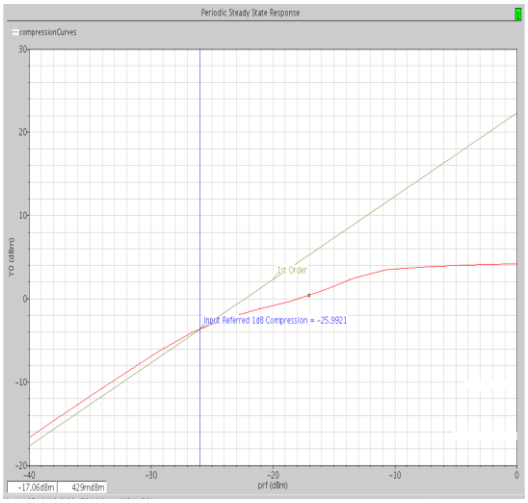


Figure 3.13(k): 1-dB plot for current-reuse LNA.

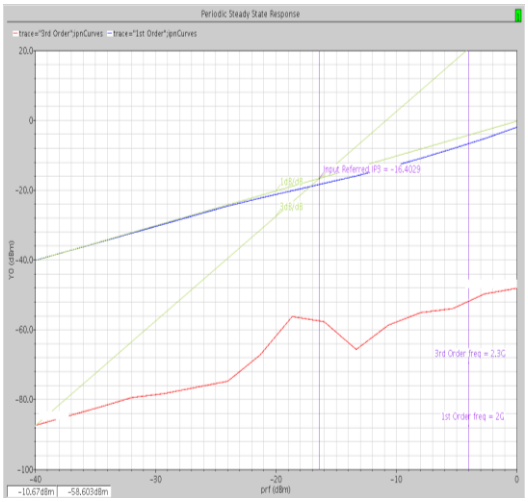


Figure 3.13(l): IP_3 plot for current-reuse LNA

Figure 3.13: Simulated curves of current-reuse LNA

CHAPTER 4

SIMULATION BASED COMPARISION OF DESIGNED LNAs

In this chapter the performance parameters like gain, noise figure, compression point, stability factor and figure of merit (FOM) of various LNA topologies are compared with the help of MATLAB tool.

4.1 Gain comparison

An LNA needs to provide enough gain to amplify received weak signal to overcome the noise of the subsequent stages. At the same time, circuit power consumption (P_D) has to be minimized, without adding too much noise and distortion. To achieve these goals three LNA topologies, single ended, differential and current reuse, are designed at 0.18μm CMOS technology at 2GHz frequency. From the simulation of all three topologies the various performance parameters are estimated. Moreover, to obtain good input matching $S_{11} < -10$dB and high voltage gain (S_{21}) the low inductor L_s value is needed. The power gain (S_{21}) and voltage gain obtained after the simulation of the single-ended, differential LNA and current reuse LNA topology are given in table 4.1.The current reuse topology shows lowest power dissipation equal to 5.958mW at V_{dd} = 1.8V. For the single-ended LNA topology power consumption is 8.1mW at the same voltage supply. This result is in conformity with common belief that current reuse technique has low power consumption than single-ended and differential LNA. Power dissipation in current reuse LNA can be further reduced with R_{ref} increase or W4 increase. To obtain optimum values for P_D, S_{11} and S_{21} the iterative simulation are performed for all three topologies. Input matching could be achieved with C_{gs} (W1) increase which resulted in higher power dissipation and better S_{21}. In the differential LNA the minimum value of S_{22} could not be set to 2GHz due to higher power consumption and trade-off between S_{22} and S_{21}. Figure 4.1 shows the variations of gain w.r.t frequency for all three topologies. The variation of gain (S_{21}) with the device geometry is shown in Figure 4.2 for all three topologies. From the graph we conclude that the gain of CRLNA is better than single-ended and differential low noise amplifier. From the simulation results we

conclude that as frequency increases the gain decreases. After a saturation value of device width the gain in all three topologies decreases with width increases.

Parameters	Single-ended LNA	Differential LNA	Current-reuse LNA	Units
Power gain(S_{21})	18.22	15.87	23.41	dB
Voltage gain	16.7	18.67	19.96	dB
Power consumption(P_D)	8.1	16.2	5.958	mW

Table 4.1: Gain and power consumption of various topologies

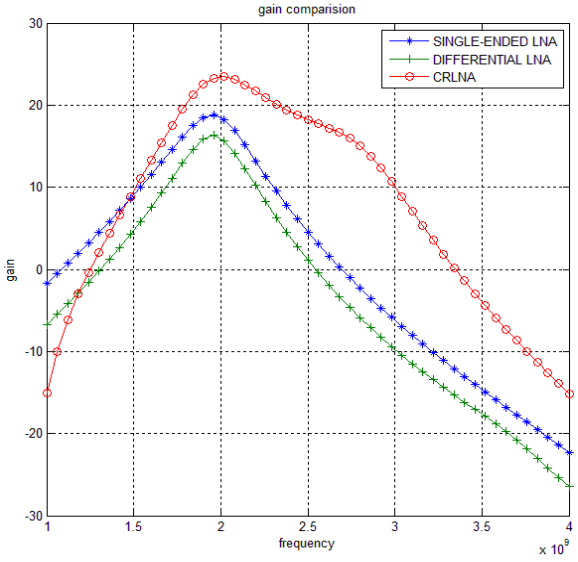


Figure 4.1: Comparison of gain of various LNA topologies w.r.t frequency

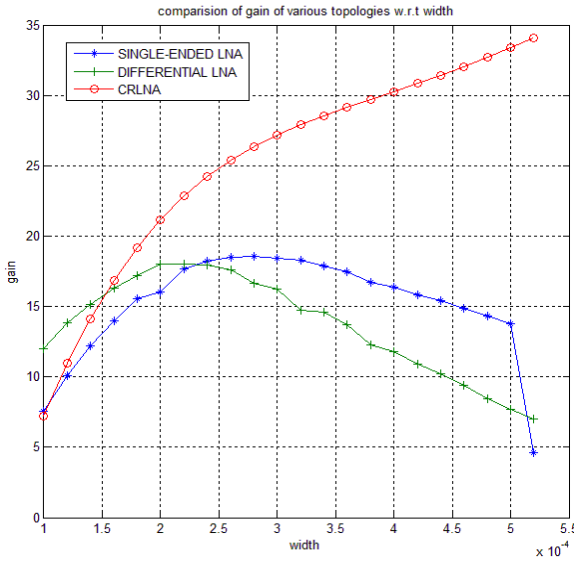


Figure 4.2: Dependence of gain of various LNA topologies on width of transistors

4.2 Noise figure (NF) comparison

Since an LNA is the first part of the receiver, its noise performance has a significant impact on the noise of the whole receiver. Hence, a stringent requirement of 0-5 dB has been placed on the Noise Figure. The other requirement of an LNA is to provide significant gain, as this will further reduce the noise contribution of the following stages to the total Noise Figure of the receiver. The single-ended LNA topology and differential LNA has managed to achieve lower power dissipation with increase in R_{ref}. As a result, NF is increased due to increase in R_{ref}. NF of LNA is also affected by L_g inductor at the input and the value of Q selected for the design of LNA. We know that resonant frequency ω_0 at the input can be dominantly adjusted

with L_g and C_{gs}. The change of L_g inductor also affects the noise figure. The simulation results shown in Table 4.2 shows that the differential LNA has minimum noise figure than

Parameters	Single-ended LNA	Differential LNA	Current-reuse LNA	Units
NF(noise figure)	2.965	3.774	3.034	dB
NF_{min}	2.49	2.67	2.663	dB
r_n(total input referred noise)	3.971×10^{-19}	5.05394×10^{-19}	7.818×10^{-18}	V^2/Hz

Table 4.2: Noise figure and total input refereed noise of various topologies.

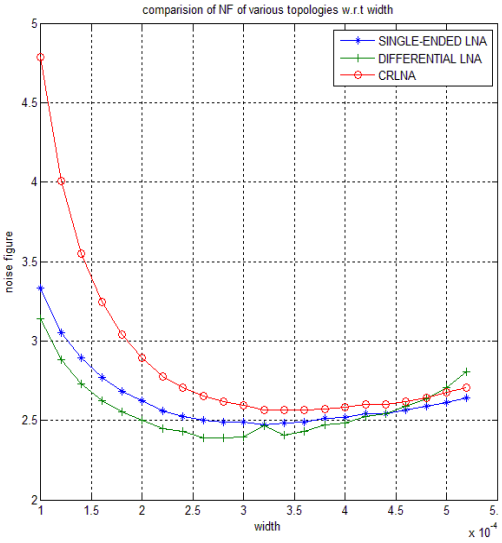


Figure 4.3: Dependence of NF_{min} of various LNA topologies on width of transistors.

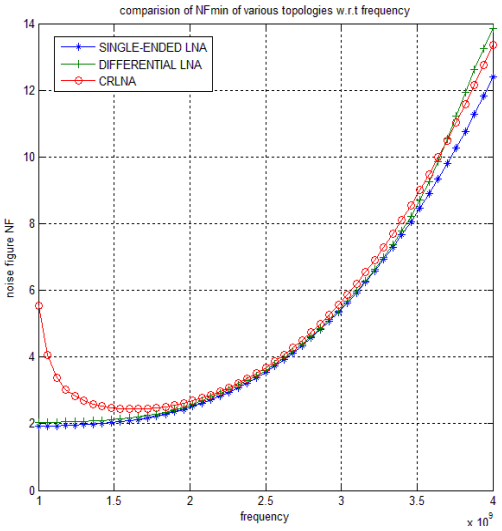


Figure 4.4: Comparison of NF_{min} of various LNA topologies w.r.t frequency

single-ended and current reuse LNA while overall noise figure is minimum in the single-ended topology. The total input referred noise (r_n) is minimum for the single-ended LNA. In Figure 4.4 the noise figure is around 2.5 dB for all three topologies at 2 GHz frequency. The noise figure is high in low frequency and high frequency. In low frequency, the flick noise dominates the noise performance, which characteristic is proportional to 1/f. However in high frequency, with the distortion of the circuit gain, the noise performance degrades. As the width of the transistors increases the NF_{min} decreases till 400µm and after this there are slightly increases in the noise figure of all three topologies. The noise figure of CRLNA is higher than both the single-ended and differential LNA. The value of r_n increases as the frequency of operation increases.

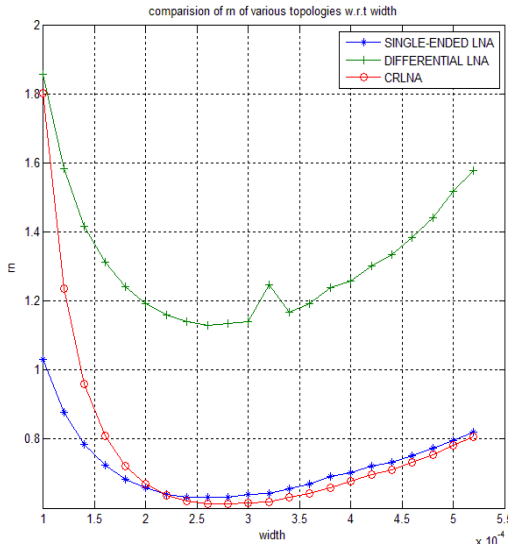


Figure 4.5: Dependence of r_n of various LNA topologies on width of transistors.

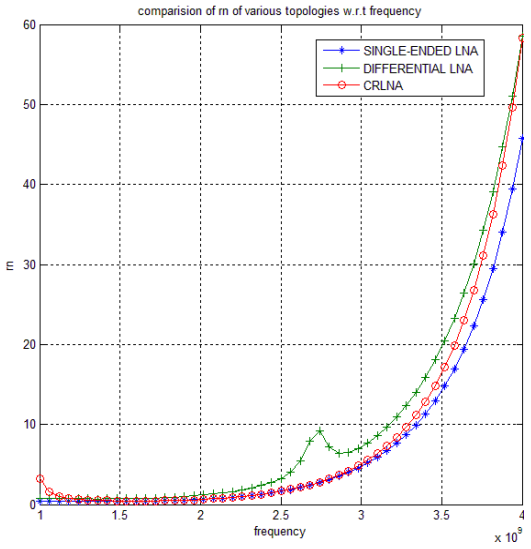


Figure 4.6: Comparison of r_n of various LNA topologies w.r.t frequency.

4.3 Linearity and Stability comparison

IP3 point is a measure of linearity of the LNA. The IP3 point allows us to operate the LNA at significant power levels without worrying about non-linear effects. 1-dB point is another measure of the linearity of the LNA and hence should be as high as possible. Based on the input signal power we have selected our 1-dB requirements to be greater than -15 dB for single-ended topology. Stability parameters simulations were performed from 1GHz to 4GHz. For whole simulated range single-ended LNA and differential LNA topologies satisfy unconditional stability requirements, where Rollet stability factor K_f >1 and alternate stability factor B_{1f} > 0. At 2GHz for current reuse topology K_f = 116.9 and B_{1f}=0.978 while for the single-ended topology K_f =5.391 and B_{1f} =1.055. So, CRLNA is more stable than the differential and single-ended LNA. Figure 4.7 and 4.8 shows the stability factor (K_f , B_{1f}) comparison of various LNA topologies.

Parameters	Single-ended LNA	Differential LNA	Current-reuse LNA	Units
P1dB	-19.3297	-12.5176	-25.9921	dBm
IIP3	-10.3012	-2.86127	-16.4029	dBm
K_f	5.391	3.221	116.9	
B_{1f}	1.055	0.255	0.9711	

Table 4.3: P1dB, IIP3, K_f and B_{1f} of various LNA topologies.

A higher third-order intercept point (IIP3) for the LNA may be obtained by increasing the degeneration resistor, R_s. However, it is important not to increase R_s too much since, despite an improvement in the linearity of the LNA, it will also have an adverse effect on both the gain and noise of the circuit. To avoid the effects on gain and noise and to increase an IIP3,

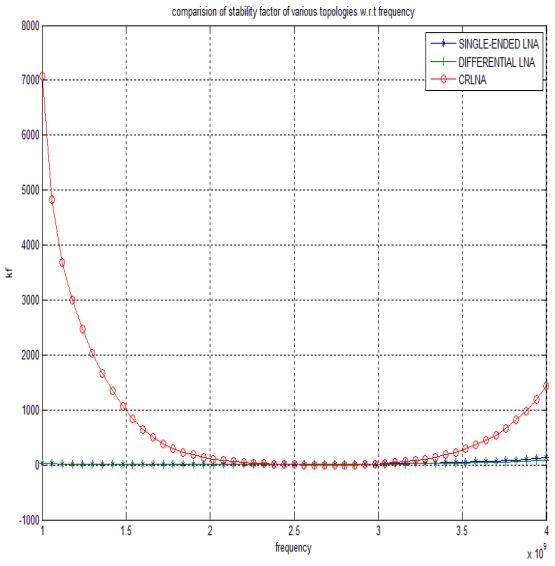


Figure 4.7: Comparison of K_f of various LNA topologies w.r.t frequency.

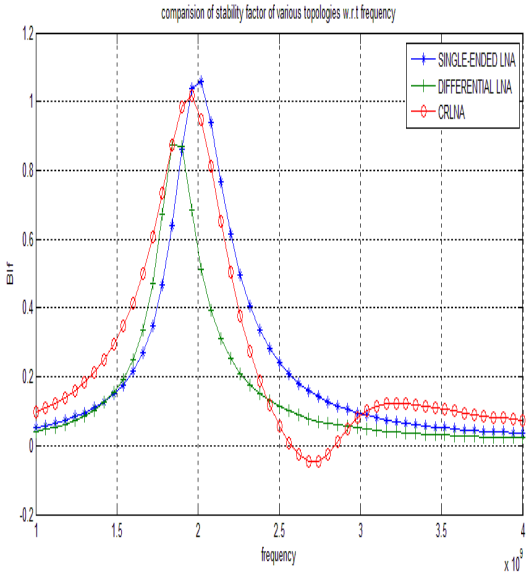


Figure 4.8: Comparison of B_{1f} of various LNA topologies w.r.t frequency.

the total current consumed by the LNA may be increased. This can be accomplished by increasing the size of the driver transistors.

4.4 Figure of merit (FOM) comparison

To evaluate the overall performance of an LNA, figure of merit (FOM) is adopted. Figure of merit includes power gain, noise figure, power dissipation and the operation frequency. Each performance factor of FOM is analytically expressed in device parameters. Although there are many performance factors in LNAs, we concentrate on three important characteristics such as power gain, noise figure and power dissipation. These are included in figure of merit equation which is defined as below.

$$FOM = \frac{S_{21} \times BW}{NF \times P_{dc}} \qquad (4.1)$$

Where S_{21} is signal power gain, NF is noise figure, P_{dc} is power dissipation, and BW is the bandwidth of low noise amplifier. The overall performance of an LNA is evaluated by using Equation (4.1). Now, we calculate the FOM for all the three topologies of low noise amplifiers at 2GHz frequency.

The figure of merit for the single ended LNA is:

$$FOM1 = \frac{18.22 \times 1.0245}{2.49 \times 8.1} = 0.925\ GHz/mW \quad (4.2)$$

Where, S_{21}=18.22 dB, NF=2.49dB, BW=1.0245GHz and P_{dc}=8.1 mW at 2 GHz frequency.

The figure of merit for the differential LNA is:

$$FOM2 = \frac{15.87 \times 1.0658}{2.4 \times 16.2} = 0.435 GHz/mW \quad (4.3)$$

Where, S_{21}=15.87 dB, NF=2.4dB, BW=1.0658GHz and P_{dc}=16.2 mW at 2 GHz frequency.

The figure of merit for the CRLNA is:

$$FOM3 = \frac{23.41 \times 1.051}{2.663 \times 5.958} = 1.5507 GHz/mW \quad (4.4)$$

Where, S_{21}=23.41 dB, NF=2.663dB, BW=1.051GHz and P_{dc}=5.958 mW at 2 GHz frequency.

Table 4.4 shows the figure of merit of various topologies of LNA obtained after the simulation.

Parameters	Single-ended LNA	Differential LNA	Current-reuse LNA	Units
FOM	0.925	0.435	1.5507	GHz/mW

Table 4.4: Figure of merit (FOM) of various LNA topologies

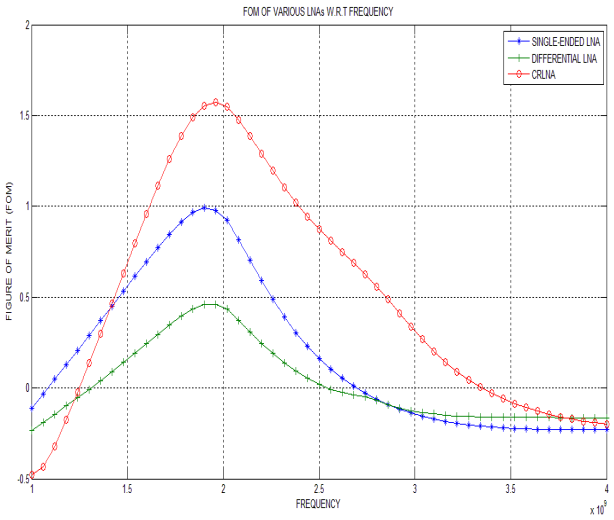


Figure 4.9: Comparison of FOM of various LNA topologies w.r.t frequency.

To maximize figure of merit, each factor is expressed analytically in device parameters. The higher the gain is and the lower the NF is the better is the LNA. The bandwidth (BW) of the amplifier was set by the range of frequencies that the multi-band receiver front-end has to support. One LNA circuit may have a larger BW, while another may have a larger gain, making comparison between different LNAs difficult. To enable such a comparison,

designers typically map the multitude of circuit specifications into a single scalar figure of merit. Clearly the best circuit will have the highest FOM. Figure 4.9 shows the comparison of FOM of various LNA topologies with the frequency range of 1GHz to 4GHz at constant bandwidth and power dissipation. These plots are obtained with the help of MATLAB. From the Figure 4.9 it is clear that the current-reuse LNA has best figure of merit (FOM). Therefore it can be concluded that CRLNA gives the best performance among all LNA topologies discussed above. The next chapter deals with the issue of LNA parameter estimation using artificial neural networks.

CHAPTER 5

ANN MODELING FOR-AMPLIFIER PARAMETER ESTIMATION

In this chapter the ANN modeling for amplifier parameter estimation based on the obtained simulated values are presented. The ANN modelling provides an easier way for the future workers to optimize different LNA parameters w.r.t. the others without resorting to standard simulation.

5.1 Need of ANN modeling

As evident from the discussions in the precious two chapters there is need of a simple and accurate device modeling technique in problems related to amplifier design. Moreover the intricacies involved in accentuating each and every device parameter for various permutations of trade off are highly complex. All popular simulation platforms (e.g. Cadence Spectre_RF in this work) make use of electromagnetic field solvers which form a part of EDA tools. These electromagnetic solvers typically rely on the solution of a large number of integral equations which, in turn require substantial memory and specialized resources. Comparative analysis being the common way for rigorous assessment of the various designs, the above mentioned requirement of specialized resources becomes all the more important. Thus a need has been felt that a modeling technique be put in place which is more general in nature, consumes lesser number of resources and has the capability to approximate all the design parameters when require to do so.

Artificial neural networks (ANN) are such a modeling technique which has capability to learn data, to approximate any unseen data and to model non linear parameter. Above over the last twenty years ANN has extensively been applied in many areas including signal processing applications, remote sensing [15]. In the previous decade ANN has been applied in microwave design [16], microwave impedance matching [16] and antenna design [17]. Based upon these reported developments an effort has been made in this work to estimate different LNA parameters from the obtained simulation data. The emphasis in this part has been to construct and train such an ANN which is capable of estimating unseen mappings of different

LNA parameters. The present work makes use of one of the most popular ANN architecture i.e. Multilayer Perceptron trained with Back Propagation (BP) algorithm. A brief introduction of ANN in general and BP algorithm in particular is presented in the subsequent sub section.

5.2 Brief introduction of ANN

Around three decades ago, we had a limited computational capability at our disposal. That was the time when computers had just begun to show their promise in real-world applications. To solve a problem at hand we needed a precise mathematical and analytical model of it. Real-world problems more often than not are defined only by a set of observational data. It is hard to devise a model for each and every data set. However, with the increase in the capacity of computers it gradually became possible to have a connectionist approach to computing where, it is assumed that any input-output mapping can be modelled as an interconnection of several computing units and thus was the emergence of artificial neural networks in applied sciences. However, the concept was already there in mathematics. In line with these developments there emerged the concepts of fuzzy logic and evolutionary computing. All three put together are now termed collectively as soft computing as something fundamentally different from traditional hard computing. **Hard computing (HC)** requires a precisely stated analytical model and often a lot of computation time. **Soft computing (SC)** differs from hard computing in that, unlike hard computing, it is tolerant of imprecision, uncertainty, partial truth, and approximation. In effect, the role model for soft computing is the human mind. Following points make it clear how soft computing is different from the hard one.

- HC is based on binary logic, crisp systems, numerical analysis and crisp software but SC is based on fuzzy logic, neural nets and probabilistic reasoning.
- HC requires programs to be written, while SC can evolve its own programs.
- HC uses two-valued logic, while SC can use multivalued or fuzzy logic.
- HC is deterministic, contrary to this SC incorporates stochasticity.
- HC requires exact input data, SC can deal with ambiguous and noisy data.
- HC is strictly sequential, SC allows parallel computations.
- HC produces precise answers, SC can yield approximate answers.

Recently, there is increased interest of scientists to integrate different soft computing techniques together for solving real world problems. Kumar et. al. has attempted simultaneous identification and quantification of odours using a combination of fuzzy logic and ANN[18]. However, ANN still is the most dominant of all soft computational techniques.

5.2.1 Inspiration from Neurobiology

Biological Neural Network

A biological neuron receives inputs from other sources, combines them in some way, performs a generally nonlinear operation on the result, and then output the final result. Output can be excited or not excited, subject to attenuation in the synapses, which are junction parts of the neuron. Incoming signals from other neurons determine if the neuron shall excite ("fire").

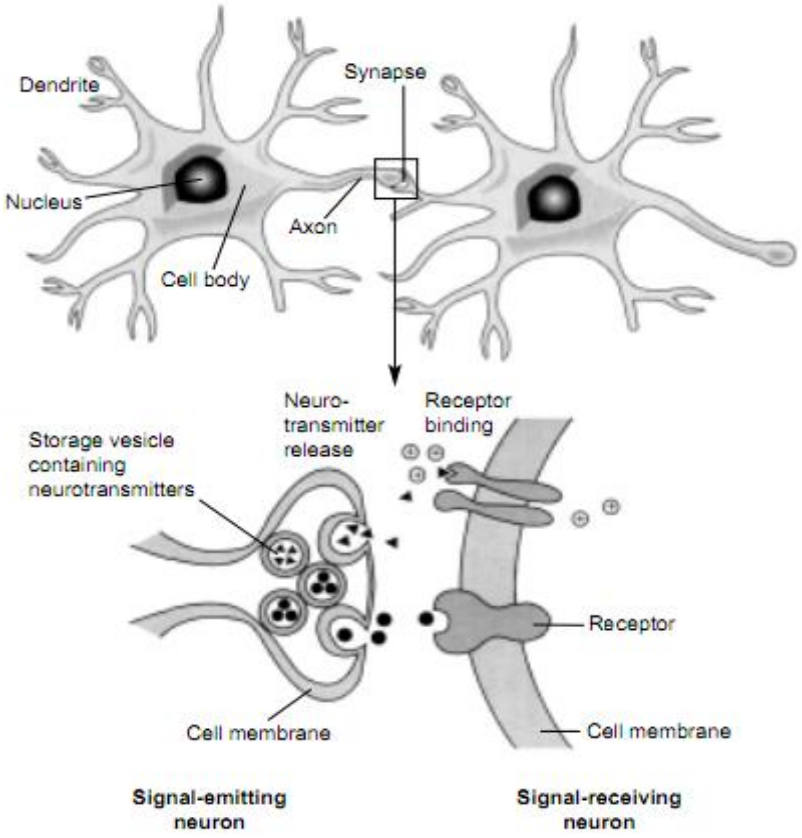


Figure 5.1: Neuron structure and Synapse[20].

Neuron: many-inputs / one-output unit

Inputs: Dendrites

Processing: Soma

Outputs: Axons

Synapse: Electrochemical contact between Neurons

The facts about Biological Neural Networks which motivated humans to implement architecture similar to them

- The number of neurons in the human brain: 10^{11}
- The average number of connections of each neuron: 10^4
- Highly parallel computation

Synapse: In the nervous system, a synapse is a structure that permits a neuron to pass an electrical or chemical signal to another cell (neural or otherwise). The word "synapse" comes from "synaptein", which Sir Charles Scott Sherrington and colleagues coined from the Greek "syn-" ("together") and "haptein" ("to clasp").

Hebb's Rule: The synapse resistance to the incoming signal can be changed during a "learning" process, following quoted by **Donald Olding Hebb** in his book "The Organization Behavior" [1949], later known as Hebb's Rule.

Let us assume that the persistence or repetition of a reverberatory activity (or "trace") tends to induce lasting cellular changes that add to its stability. When an axon of cell A is near enough to excite cell B and repeatedly or persistently takes part in firing it, some growth process or metabolic change takes place in one or both cells such that A's efficiency, as one of the cells firing B, is increased.

5.2.2 Mathematical Model

The block diagram of Fig. 5.2 shows the mathematical model of a neuron, which forms the basis for designing ANNs. Here we identify three basic elements of the neuronal model.

1. A set of Synapses or connecting Links, each of which is characterized by a Weight or Strength of its own. Specifically, a signal x_i at the input of synapse I connected to neuron k is multiplied by the synaptic weight w_{ki}.
2. An Adder for summing the input signals, weighted by the respective synapses of the neuron.
3. An Activation Function for limiting the amplitude of the output of a neuron. The activation function is also referred to as a Squashing Function in that it squashes (limits) the permissible amplitude range of the output signal to some finite value.

The neuronal model of Fig. 5.2 also includes an externally applied bias denoted by B_k. The bias B_k has the effect of increasing or lowering the net input of the activation function, depending on whether it is positive or negative, respectively.

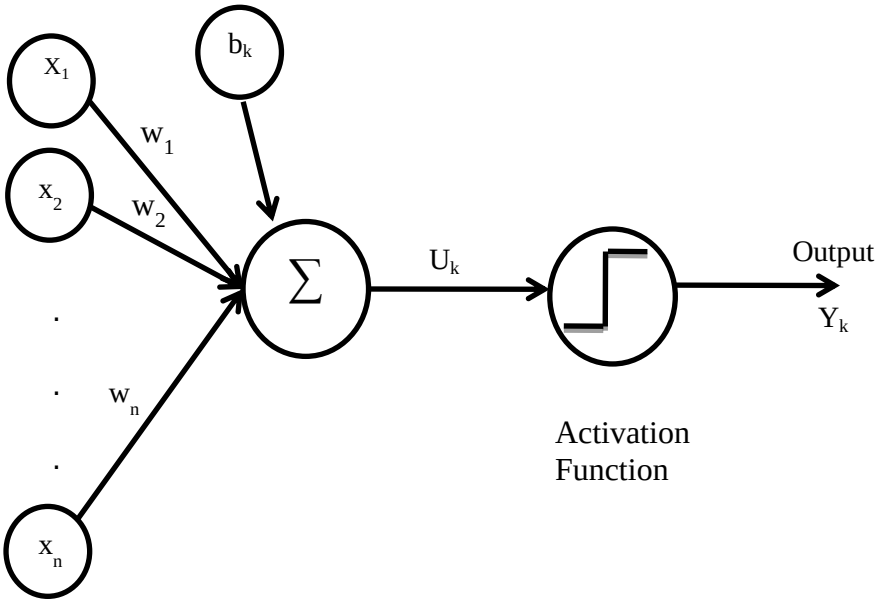


Figure 5.2: Mathematical Model of Neuron

In mathematical terms, we may describe a neuron k by writing the following pair of equations:

$$u_k = \sum_{i=1}^{n} w_{ki} * x_i + b_k \tag{5.1}$$

And

$$y_k = \varphi(u_k) \tag{5.2}$$

Where X_i are the input signals; W_{ki} are the synaptic weights of neuron k; B_k is the bias; U_k is the adder output, $\varphi(.)$ is the activation function; and Y_k is the output of the neuron. The use of bias b_k has the effect of applying an affine transformation to the output U_k of the linear combiner in the model of Figure 5.2.

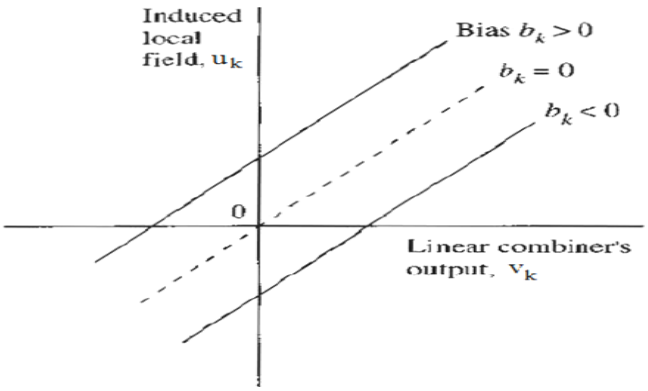


Figure 5.3: Affine transformation produced by the presence of a bias[20].

5.2.2.1 Types of Activation Function

The activation function, denoted by $\varphi(v)$, defines the output of a neuron in terms of the induced local field v. Here we identify three basic types of activation functions:

(a) Threshold Function: For this type of activation function, described in Figure 5.4(a), we have:

$$\varphi(v) = \begin{cases} 1 \text{ if } v \geq 0 \\ 0 \text{ if } v \leq 0 \end{cases} \tag{5.3}$$

Such a neuron is referred to in the literature as the McCulloch-Pitts model, in recognition of the pioneering work done by McCulloch and Pitts (1943). In this model, the output of a neuron takes on the value of 1 if the induced local field of that neuron is non-negative and 0 otherwise. This statement describes the all-or-none property of the McCulloch-Pitts model.

(b) Piecewise-Linear Function: For the piecewise-linear function described in Figure 5.4(b)we have

$$\varphi(v) = \begin{cases} 1, & v \geq +\frac{1}{2} \\ v, & -\frac{1}{2} > v > +\frac{1}{2} \\ 0, & v \leq -\frac{1}{2} \end{cases} \tag{5.4}$$

Where the amplification factor inside the linear region of operation is assumed to be unity. This form of an activation function may be viewed as an approximation to a non-linear amplifier. The piecewise-linear function reduces to a threshold function if the amplification factor of the linear region is made infinitely large.

(c) Sigmoid Function: The sigmoid function, whose graph is s-shaped, is by far the most common form of activation function used in the construction of ANNs. It is defined as a strictly increasing function that exhibits a graceful balance between linear and nonlinear behaviour. An example of the sigmoid function is the logistic function, defined by

$$\varphi(v) = \frac{1}{1+e^{(-av)}} \tag{5.5}$$

Where a is the slope parameter of the sigmoid function. By varying the parameter a, we obtain sigmoid functions of different slopes, as illustrated in Figure 5.4(c). In fact, the slope at the origin equals a/4. In the limit, as the slope parameter approaches infinity, the sigmoid function becomes simply a threshold function. Whereas a threshold function assumes the value of 0 or 1, a sigmoid function assumes a continuous range of values from 0 to l.

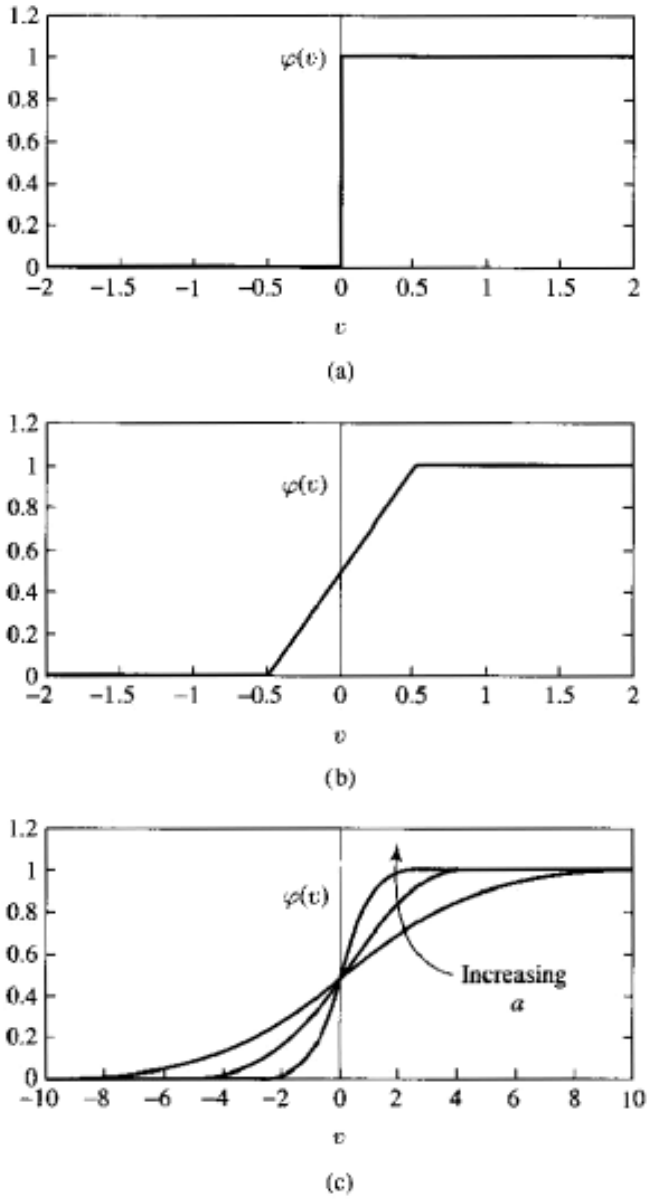


Figure 5.4: Types of activation functions (a) Threshold function (b) Piecewise-linear function (c) Sigmoid function for varying slope parameter *a* [20].

The activation functions defined in above range from 0 to +l. It is sometimes desirable to have the activation function range from -1 to +1, in which case the activation function assumes an anti-symmetric form with respect to the origin; that is, the activation function is an odd function of the induced local field. Specifically, the threshold function of is now defined as:

$$\varphi(v) = \begin{cases} -1 & if\ v > 0 \\ 0 & if\ v = 0 \\ 1 & if\ v < 0 \end{cases} \tag{5.6}$$

which is commonly referred to as the signum function. For the corresponding form of a sigmoid function we may use the hyperbolic tangent function, defined by

$$\varphi(v) = \tanh(v) \tag{5.7}$$

To describe this algorithm consider Figure 5.5, which depicts neuron j being fed by a set of function signal produced by a layer of neurons to its left. The induced local field $y_j(n)$ produced at the input of the activation function associated with neuron j is therefore

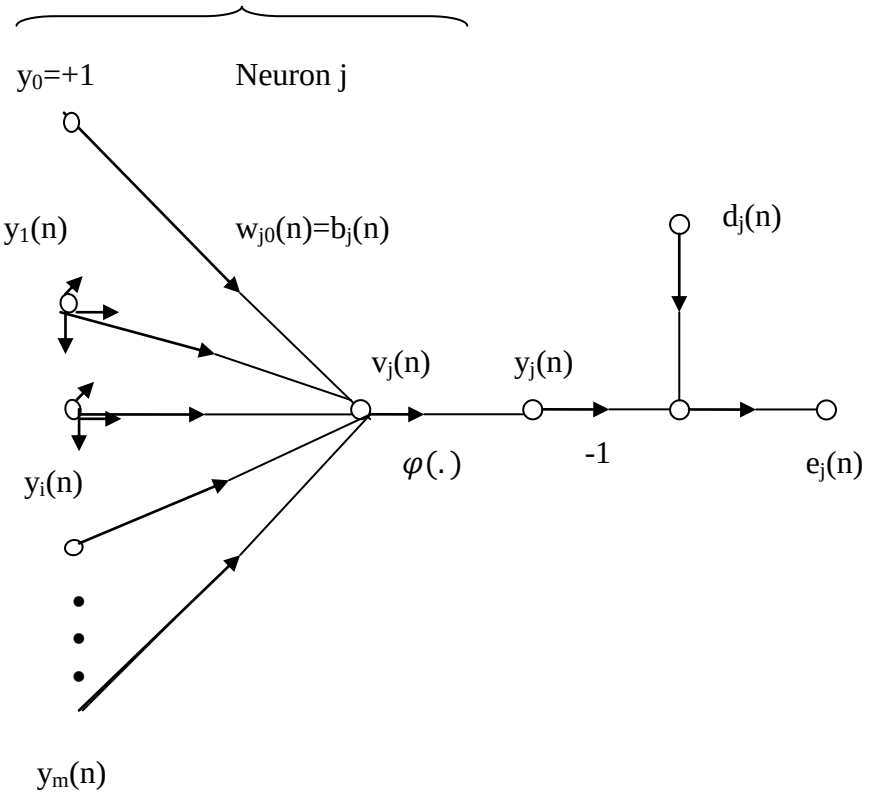


Figure 5.5: Signal-flow graph highlighting the details of output neuron j.

$$v_j(n) = \sum_{i=0}^{m} w_{ji}(n) y_i(n) \tag{5.8}$$

Where m is the total number of inputs (excluding the bias) applied to neuron j. The synaptic weight w_{j0} equals to the bias b_j applied to neuron j. Hence, the function signal $y_i(n)$ appearing at the output j at iteration n is

$$y_i(n) = \varphi_j(v_j(n)) \tag{5.9}$$

According the chain rule of the calculus, we may express:

$$\frac{\partial \xi(n)}{\partial w_{ji}(n)} = \frac{\partial \xi(n)}{\partial e_j(n)} \frac{\partial e_j(n)}{\partial y_j(n)} \frac{\partial y_j(n)}{\partial v_j(n)} \frac{\partial v_j(n)}{\partial w_{ji}(n)} \tag{5.10}$$

The partial derivative $\frac{\partial \xi(n)}{\partial w_{ji}(n)}$ represents a sensitivity factor, determining the direction of search in weight apace for the synaptic weight w_{ji}. We know

$$\frac{\partial \xi(n)}{\partial e_j(n)} = e_j(n) \text{ and } \frac{\partial e_j(n)}{\partial y_j(n)} = -1 \tag{5.11}$$

Now, differentiating Equation (5.11) with respect to e_j (n), we get

$$\frac{\partial y_i(n)}{\partial v_j(n)} = \varphi'_j(v_j(n)) \tag{5.12}$$

Where the use of prime signifies differentiation with respect to the argument. Finally, differentiating Equation (5.8) with respect to w_{ji}(n) yields

$$\frac{\partial v_j(n)}{\partial w_{ji}(n)} = y_i(n) \tag{5.13}$$

The use of Equation 5.11, 5.12, 5.13 in Equation 5.10 yields

$$\frac{\partial \xi(n)}{\partial w_{ji}(n)} = -e_j(n)\varphi'_j\left(v_j(n)\right) y_i(n) \tag{5.14}$$

The correction $\Delta w_{ji}(n)$ applied to $w_{ji}(n)$ is defined by the delta rule, or

$$\Delta w_{ji}(n) = -\eta \frac{\partial \xi(n)}{\partial w_{ji}(n)} \tag{5.15}$$

Where η is the learning-rate parameter of the back-propagation algorithm. The use of minus sign in this Equation accounts for gradient descent in weight space. Accordingly, the use of Equation 5.14 in Equation 5.15 yields

$$\Delta w_{ji}(n) = \eta \delta_j(n) y_i(n) \tag{5.16}$$

Where the local gradient $\delta_j(n)$ is defined by

$$\delta_j(n) = \frac{\partial \xi(n)}{\partial v_j(n)} = \frac{\partial \xi(n)}{\partial e_j(n)} \frac{\partial e_j(n)}{\partial y_j(n)} \frac{\partial y_j(n)}{\partial v_j(n)} = e_j(n)\varphi'_j\left(v_j(n)\right) \quad (5.17)$$

The local gradient points to required changes in synaptic weights. According to Equation m, the local gradient $\delta_j(n)$ for output neuron j is equal to the product of the corresponding error signal $e_j(n)$ for the neuron and the derivative $\varphi'_j\left(v_j(n)\right)$ of the associated activation function.

5.3 ANN models of simulated topologies

All the simulated topologies were modeled using backpropogation algorithm trained ANN for parameter estimation and prediction. BP algorithm was used as it is the most popular and offers many advantages in the form of low computational complexity, a reasonable convergence time and a simple architecture. In this work ANN models of three different topologies were constructed for the estimation of gain and noise figure for a given combination of operating frequency, width and r_n. The optimum architecture for ANN models of different topologies were optimized experimentally. In all the cases single hidden layer architecture was chosen for simulation. The number of neurons in the hidden layer was varied experimentally and the simulation results were compared with the desired output which was stored in the form of test target vectors. Seventy percent of the data were labeled as training data while the rest 30% were designated as test vectors. For a given combination of learning rate **η** and momentum constant α, the ANN was trained for a fixed 10,000 epochs with an error goal of 0.005. The architecture converging to desired error goal was then fed with the test data to judge its generalization performance. To minimize the possibility of overfitting an *m*-fold cross validation scheme with m=6 was used. The data to be used as test vector were picked from the whole data set six times in six different ways in a random manner. The next subsection describes the optimized ANN architectures and their performance with respect to estimation of simulated LNA parameters[19].

5.3.1 Single-Ended LNA

The parameters obtained after the simulation of the single-ended LNA is discussed in the chapter 3. With the help of ANN modeling the approximate data is obtained for the Single-Ended LNA which is shown in Fig. 5.6. There is a little difference between the desired values and the obtained values of gain and noise figure. The variation between the desired and obtained values after ANN modeling of Single-Ended LNA is more when gain and noise figure is varied with respect to frequency than width.

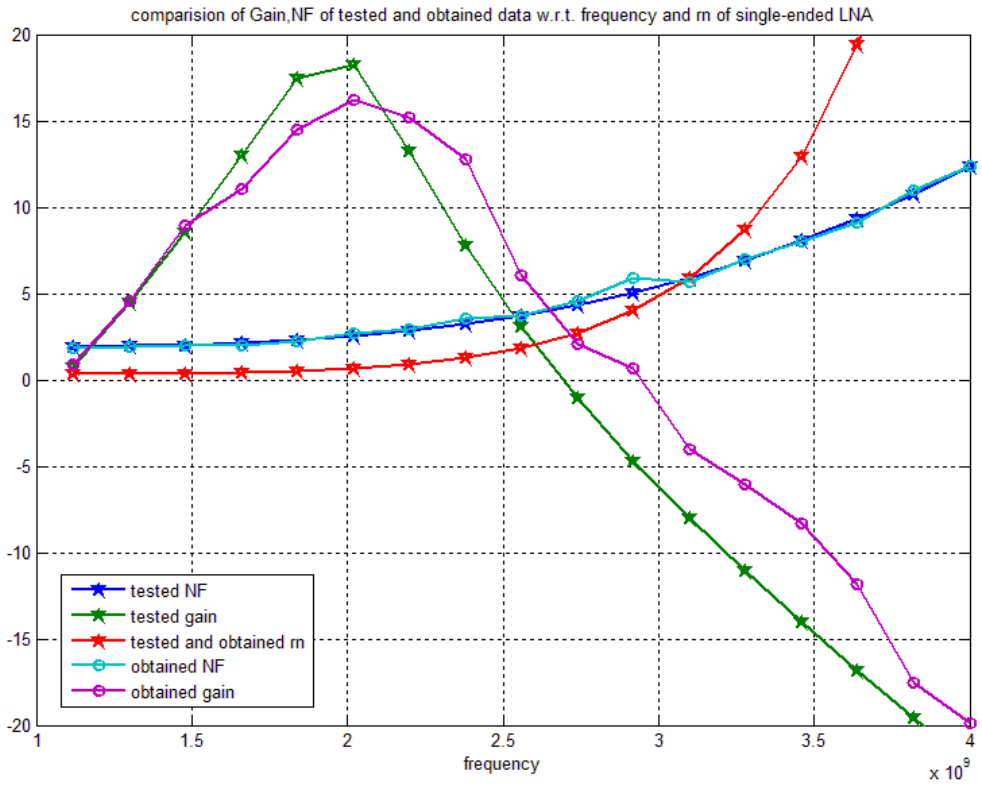


Figure 5.6: Comparison of desired and obtained values of gain and noise figure of single-ended LNA w.r.t. frequency.

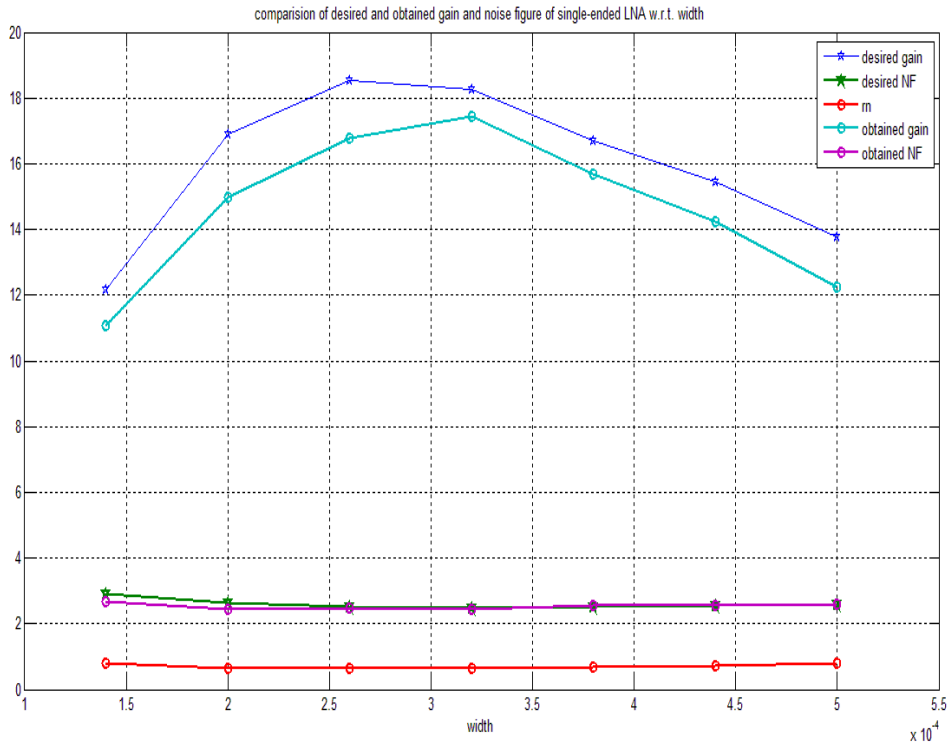


Figure 5.7: Comparison of desired and obtained values of gain and noise figure of single-ended LNA w.r.t. width.

5.3.2 Differential LNA

The back propagation algorithm is used for the prediction of the desired values of gain and noise figure. The comparison of the desired and obtained values of the gain and noise figure is shown in the Fig. 5.8 and 5.9.

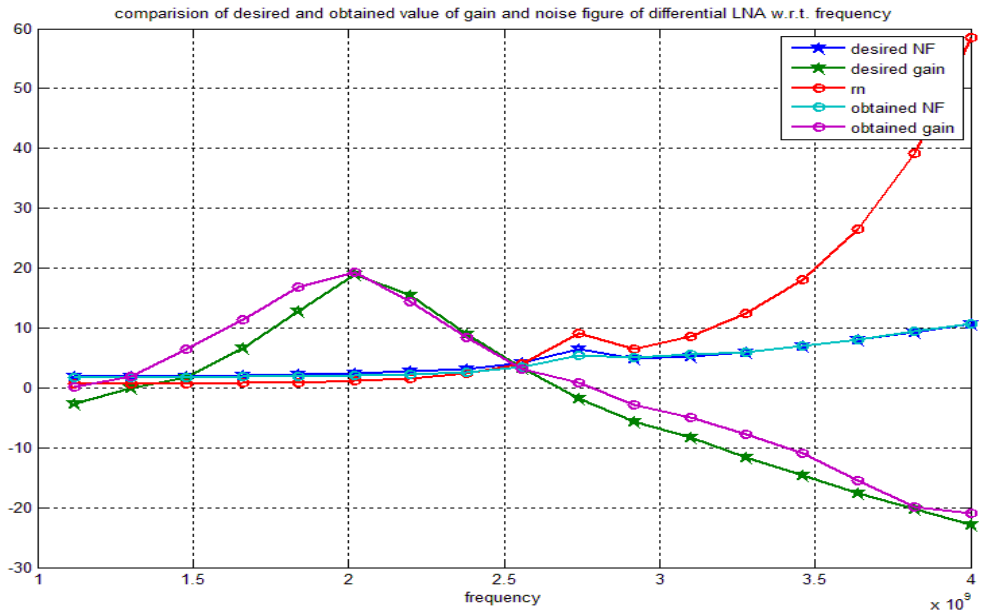


Figure 5.8: Comparison of desired and obtained values of gain and noise figure of Differential LNA w.r.t. frequency.

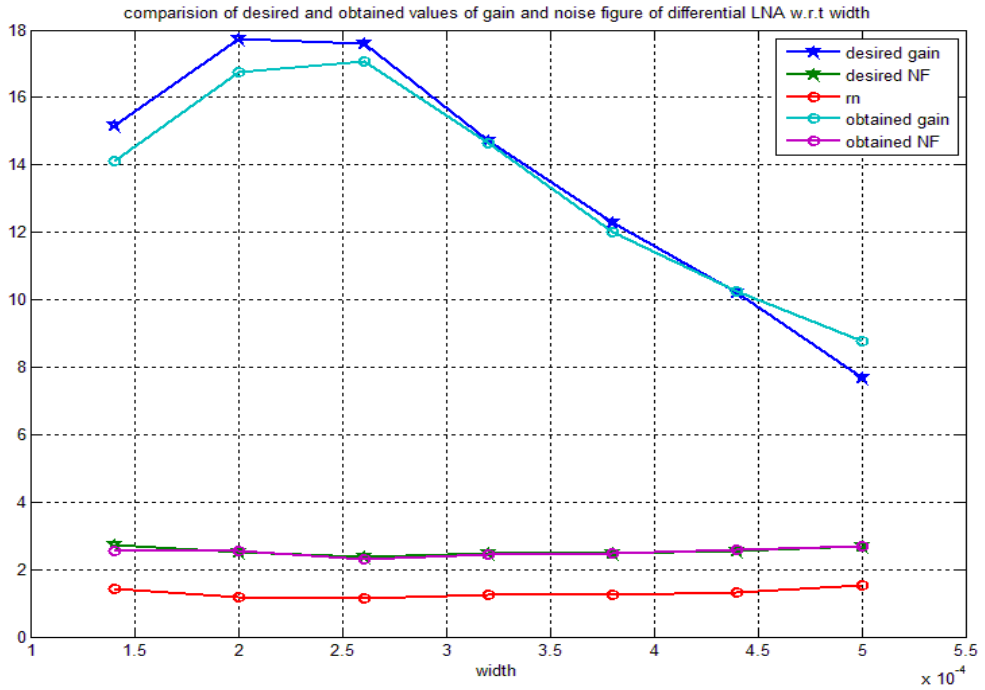


Figure 5.9: Comparison of desired and obtained values of gain and noise figure of Differential LNA w.r.t. width.

In the Fig. 5.8 the obtained values of noise figure exactly follows the desired value of the noise figure of differential LNA with the variation of frequency. But there is little difference in the desired and obtained values of gain.

5.3.3 Current-reuse LNA

From the simulation results of the various topologies as discussed above, we conclude the CRLNA is the best low noise amplifier among all. The parameters of the CRLNA are also approximated with the ANN algorithm. The results obtained after the ANN modeling of the CRLNA is shown in the Fig. 5.10 and 5.11.

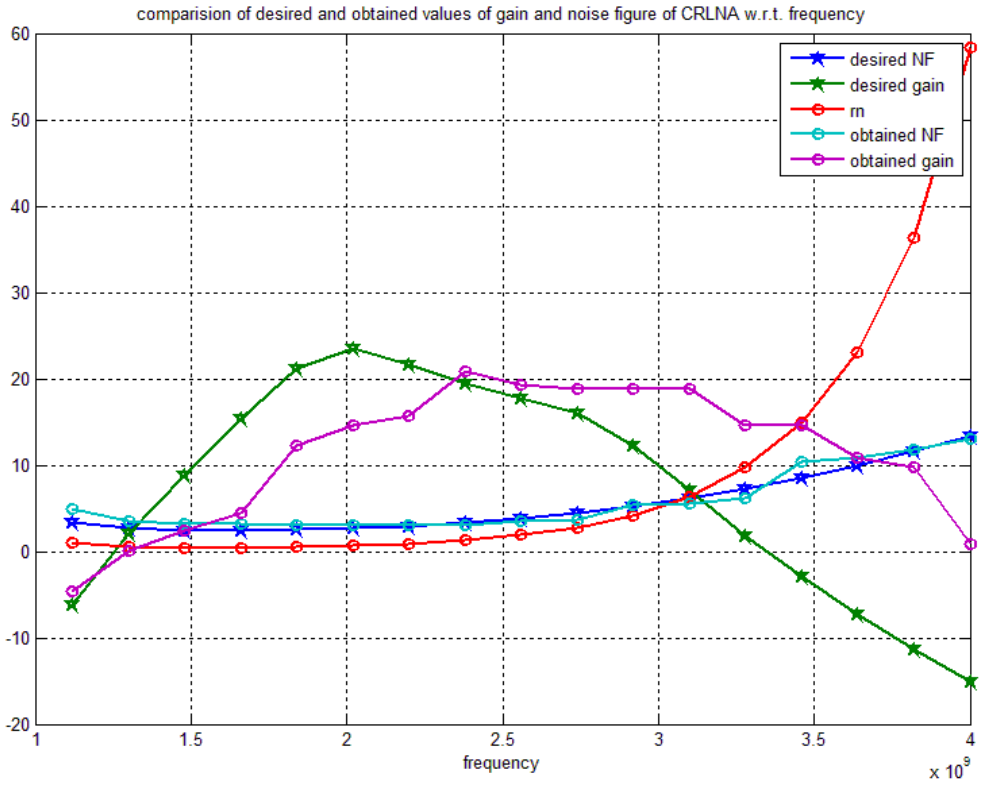


Figure 5.10: Comparison of desired and obtained values of gain and noise figure of CRLNA w.r.t. frequency.

There is a close proximity in the obtained and desired values of the noise figure of the current reuse LNA. Fig. 5.10 shows the variation of the desired and obtained values of the noise figure and gain of the CRLNA varied with respect to frequency and Fig. 5.11 shows the variation of these parameters with respect to width. From the convergence performance of all optimized ANN models of topologies of LNAs, we conclude that the best optimization is achieved in the case of current reuse low noise amplifier. The obtained NF exactly follows the desired noise figure but there is high difference in the obtained and desired values of gain.

There is very less mismatching in the desired and obtained values of gain in differential LNA which is better than the single-ended LNA and the CRLNA.

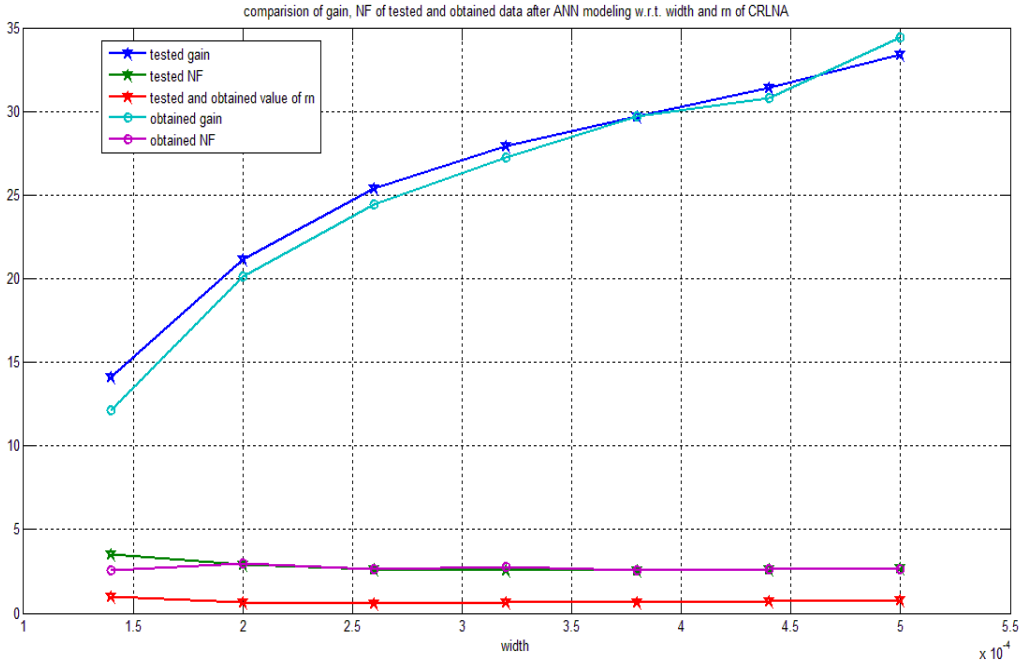


Figure 5.11: Comparison of desired and obtained values of gain and noise figure of CRLNA w.r.t. width.

CHAPTER 6 CONCLUSION AND FUTURE WORK

6.1 Conclusion

This thesis is an effort towards rigorous comparative analysis with an aim to design a low noise RF amplifier with a high figure of merit. The target specifications at the start of the design having 2GHz operating frequency, gain of more than 15dB and maximum noise figure 3dB. The corresponding values obtained by simulating three different topologies have been reported in the previous chapters and it was found that the design using all the three topologies approximated the target specifications reasonably well. As expected from the analytical results the current-reuse topology of Low noise amplifier design as resulted in an overall low noise figure, highest gain obtained and thus the best figure of merit possible. All the design topologies are simulated using Cadence Spectre_RF and UMC 180nm CMOS technology. In addition to the design ANN models for the simulated topologies were constructed for effective parameter estimation and prediction in resource constrained conditions. It has been observed that the ANN models approximated the simulated results flawlessly in almost all the conditions barring a few exceptions. The ANN modeling is expected to reduce the dependency of the designer on the electromagnetic solver based popular RF simulation tool, thus providing a viable alternative.

6.2 Future Work

The present design task undertaken during this work can be extended to incorporate the modeling and measurement based errors that creep into the RF IC design. Other parameters related to LNA performance can be incorporated into a more complex ANN model, so that the dependency on electromagnetic solver based simulation tools can be minimized. Naturally, this work can be extended to design a fully integrated RF front end.

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APPENDIX A

(A) Spectre_RF MOSFET models

- N_18_MM – 1.8 volt NMOS transistor
- P_18_MM – 1.8 volt PMOS transistor
- N_33_MM – 3.3 volt NMOS transistor
- P_33_MM – 3.3 volt PMOS transistor
- N_LV_18_MM – 1.8 volt low v_t NMOS transistor
- P_LV_18_MM – 1.8 volt low v_t PMOS transistor
- N_LV_33_MM – 3.3 volt low v_t NMOS transistor
- P_LV_33_MM – 3.3 volt low v_t PMOS transistor
- N_ZERO_18_MM – 1.8 volt zero v_t NMOS transistor
- N_ZERO_33_MM – 3.3 volt zero v_t NMOS transistor
- N_BPW_18_MM – 1.8 volt triple-well NMOS transistor
- N_BPW_33_MM – 3.3 volt triple-well NMOS transistor
- N_L18W500_18_RF – 1.8 volt variable finger RF NMOS transistor
- N_L34W500_33_RF – 3.3 volt variable finger RF NMOS transistor
- N_PO7W500_18_RF – 1.8 volt variable length RF NMOS transistor
- N_PO7W500_33_RF – 3.3 volt variable length RF NMOS transistor
- P_L18W500_18_RF – 1.8 volt variable finger RF PMOS transistor
- P_L34W500_33_RF– 3.3 volt variable finger RF PMOS transistor
- P_PO7W500_18_RF– 1.8 volt variable length RF PMOS transistor
- P_PO7W500_33_RF – 3.3 volt variable length RF PMOS transistor

(B) Inductors RF models

- L_SLCR20K_RF– Circular spiral RF inductor

APPENDIX B

(A) Capacitors RF models

- MIMCAPS_MM – Single-squared mixed-mode metal-to-metal capacitor
- NCAP_MM - NMOS transistor configured as a capacitor
- PCAP_MM - PMOS transistor configured as a capacitor
- MIMCAPM_RF – RF Metal Capacitor

(B) Resistors RF models

- RSPD_MM – P+ diffused resistor w/salicide
- RSND_MM – N+ diffused resistor w/ salicide
- RNPPO_MM – P+ poly resistor w/o salicide
- RNNPO_MM – N+ poly resistor w/o salicide
- RSNWELL_MM – N-Well resistor
- RNHR1000_MM – High Resistive poly resistor
- RNND_MM – N+ diffused resistor w/o salicide
- RNPD_MM – P+ diffused resistor w/o salicide
- RM1_MM – Metal resistor
- RM1_MM – Metal 2 resistor
- RM3_MM – Metal 3 resistor
- RM4_MM – Metal 4 resistor
- RM5_MM – Metal 5 resistor
- RM6_MM – Metal 6 resistor
- RNHR_RF - RF High resistive poly resistor
- RNNPO_RF - RF N+ poly resistor w/o salicide
- RNPPO_RF - RF P+ poly resistor w/o salicide