

# **Analysis of Power Dissipation and Breakdown Voltages of 200 $\mu$ m, 3C-SiC Schottky Barrier Diodes**

*Thesis submitted towards the partial fulfillment of the requirements for the  
award of the degree of*

**Master of Technology**

**In**

**(VLSI Design & CAD)**

Submitted by

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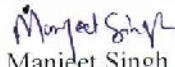
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## CERTIFICATE

I hereby certify this work, which is being presented in the thesis work, entitled "Analysis of Power Dissipation and Breakdown Voltages of 200 $\mu$ m, 3C-SiC Schottky Barrier Diodes" in partial fulfillment of the requirement for the award of degree of "master of technology" in VLSI Design & CAD at Electronics and Communication engineering department of Thapar university, Patiala, is an authentic record of my own work carried out under the guidance of Dr. A.K. Chatterjee.

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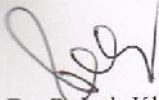
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# ABSTRACT

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Silicon carbide is a wide band gap semiconductor material for high temperature, high power and high-frequency device applications. The fact that wide band gap semiconductors are capable of electronic functionality at much higher temperatures than silicon. Because of its wide band gap, the leakage current of SiC is many orders of magnitude lower than that of silicon.

There are number of possible crystal structure. These are 2H, 3C, 4H and 6H; but the most important are 3C, 4H and 6H. These structures differ by band gap energy, carrier mobility and breakdown field. Silicon Carbide is the only chemical compound of carbon and silicon. It was originally produced by a high temperature electro-chemical reaction of sand and carbon. Schottky barrier diodes (SBDs) have many benefits compared to other rectifying devices, such as fast switching speeds and relatively easy fabrication.

The present work aims at the design of high breakdown voltage and lower power dissipation 3C-SiC schottky barrier diode and study the effect of Power Dissipation, critical electric field, breakdown voltage on Specific on Resistance for Uniformly doping profile and linearly graded profile. At the different value of current density  $J_{on}$ . After that the drift region depletion width is calculated at different doping levels. By using linearly graded profile, it is possible to design thinner devices with higher breakdown voltages and low Power dissipation.

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## LIST OF SYMBOLS:

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A	Area of the diode
$A^*$	Richardson constant ( $\text{cm}^{-2}\text{K}^{-2}$ )
$E_v$	Valence band energy level (eV)
$E_C$	Energy level of the conduction band (eV)
$E_F$	Fermi level Energy (eV)
$E_{F,M}$	Fermi level of the metal (eV)
$E_G$	Band gap energy (eV)
$E_i$	Intrinsic energy level (eV)
$E_{\text{vacuum}}$	Energy of the free electron (eV)
$I_0$	Saturation current (A)
$I_F$	Forward current (A)
$J_{\text{on}}$	Current density ( $\text{A}\cdot\text{cm}^{-2}$ )
k	Boltzmann constant (J/K)
$K_S$	Dielectric constant
$\alpha$	Gradient
$N_A$	Acceptor doping concentration ( $\text{holes}/\text{cm}^3$ )
$N_D$	Donor doping concentration ( $\text{electrons}/\text{cm}^3$ )
q	Electron charge (Coulombs)
$R_{\text{on}}$	On resistance ( $\Omega\cdot\text{cm}^2$ )
$R_S$	Sheet resistance ( $\Omega$ )
T	Temperature in Kelvin (K)
$V_a$	Applied bias voltage (V)
$V_{\text{bi}}$	Built- in potential (eV)
W	Width of the depletion region (cm)
$\epsilon_0$	Permittivity of the material (F/m)
$\chi$	Electron affinity (eV)
$\Phi_B$	Schottky Barrier Height (eV)
$\Phi_m$	Metal work function (eV)
$\Phi_s$	Semiconductor work function (eV)
$\alpha'$	angle of slope of the drift region narrowing (Degree)

## ABBREVIATIONS

---

H	Hexagonal
C	Cubic
Si	Silicon
R	Rhombohedral
SiC	Silicon Carbide
DIMOSFET	Double implanted metal oxide field effect transistor
IGBT	Insulated-gate bipolar transistors
GaAs	Gallium arsenide
IMPATT	Impact ionization Avalanche Transit-Time
SBD	Schottky barrier diodes
CCDs	Charge coupled devices

In today's technology everyone is interested in high power and high temperature devices. The development and improvement of hybrid vehicles, electric vehicles and fuel cell hybrid vehicles is a major effort by the automotive industries to meet the challenge for reduction in fuel consumption and emission of greenhouse gases. Key performances for the next generation are high breakdown voltage, low on-resistance, high current operation and high temperature operation up to 300°C [1]. Presently, almost all the power electronics converter systems use silicon- (Si) based power semiconductor switches. The performance of these switches is approaching the theoretical limits of the Si material. Another material, silicon carbide (SiC), with superior properties compared to Si, is a good candidate to be used in the next generation of power devices, especially for high voltage or high temperature applications. The compared and contrasted Si-based and SiC-based power electronic devices and have described the relative merits of using wide band gap semiconductors like silicon carbide for high voltage applications[2]

Schottky diodes are discrete devices with special functions in high power electronics and other integrated circuitry; they are basic building blocks for many transistors such as IGBTs, MOSFETs etc. Due to their high frequency behavior, Schottky barrier diodes (as opposed to pn-junction diodes) are being extensively used in different applications such as high frequency switches, gas sensors, mixers, microwave circuits and UV detectors.

### **1.1. General introduction**

The increasing dependence of modern society on electrical appliances for comfort, transportation, and healthcare has motivated great advances in power generation, power distribution and power management technologies. These advancements owe their allegiance to enhancements in the performance of power devices that regulate the flow of electricity.

After the displacement of vacuum tubes by solid state devices in the 1950s, the industry relied upon silicon bipolar devices, such as bipolar power transistors and thyristors. Although the ratings of these devices grew rapidly to serve an ever broader system need, their fundamental limitations in terms of the cumbersome control and protection circuitry led to bulky and costly solutions. The advent of MOS technology for digital electronics enabled the creation of a new class of devices in the 1970s for power switching applications as well. These silicon power MOSFETs have found extensive use in high frequency applications with relatively low operating voltages (under 100 volts). The merger of MOS and bipolar physics enabled creation of yet another class of devices in the 1980s. The most successful innovation in this class of devices has been the Insulated Gate Bipolar transistor (IGBT). The high power density, simple interface, and ruggedness of the IGBT have made it the technology of choice for all medium and high power applications with perhaps the exception of high voltage DC transmission systems. Power devices are required for systems that operate over a broad spectrum of power levels and frequencies. In , Figure 1.1

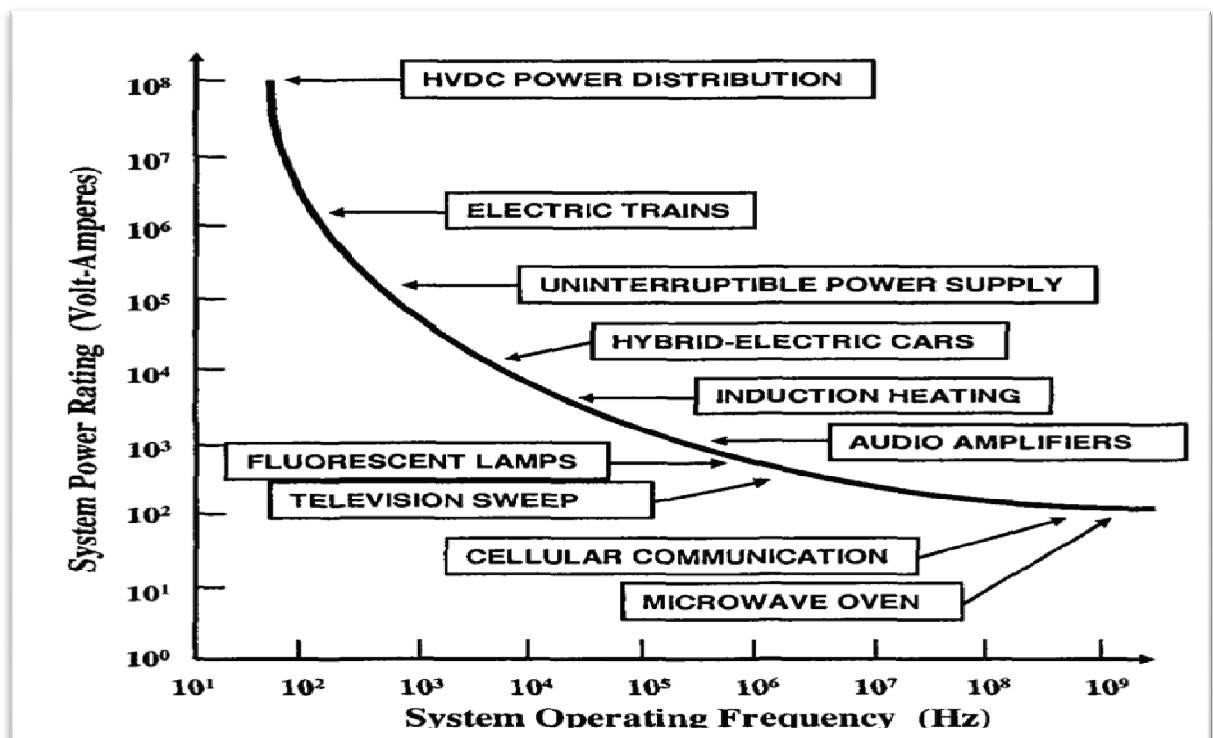


Figure 1.1 Applications for Power Devices.[1]

The applications for power devices are shown as a function of operating frequency. High power systems, such as HVDC power distribution and locomotive drives, requiring the control of megawatts of power operate at relatively low frequencies. As the operating frequency increases, the power ratings decrease for the devices with typical microwave devices handling about 100 watts. All of these applications are served by silicon devices. Thyristors are favored for the low frequency, high power applications, IGBTs for the medium frequency and power applications, and power [1]

## 1.2. Brief History of SiC

Silicon carbide (SiC) has a long and famous history. The first observation of SiC or at least of a Si-C bond containing compound goes back to Jons Jakob Berzelius, Professor in chemistry at the Karolinska Institute in Stockholm.<sup>1</sup> In 1823, Berzelius burnt an unknown compound and observed an equal number of silicon (Si) and carbon (C) atoms. Nowadays, SiC has developed into one of the leading contenders among the wide band gap semiconductors. [3] This leading role is due to the fact that

- (a) Large SiC substrates are commercially available (3 inch in diameter),
- (b) SiC can homo epitaxial be grown avoiding lattice mismatch,
- (c) n- and p-type conductivity can be achieved either by doping during crystal growth or afterwards by ion implantation and
- (d) Oxide films can thermally be grown on both the Si- and C-face.

Its formation was confirmed by Eugene and Alfred Cowes in 1885. It does not occur naturally on earth, although it occurs in meteorites. In 1955, Lely introduced a new method of growing this material in the laboratory, and the current method used is a modification of this, now referred to as the modified Lely technique. This breakthrough led to the formation in 1987, of Cree, Inc, the first commercial supplier of SiC. SiC is part of a family of materials which exhibit a one-dimensional polymorphism called polytypism. The difference among the polytypes is in the arrangement of layers of Si and C. In Sic, Si and C are bonded tetrahedrally, shown in figure 1.2

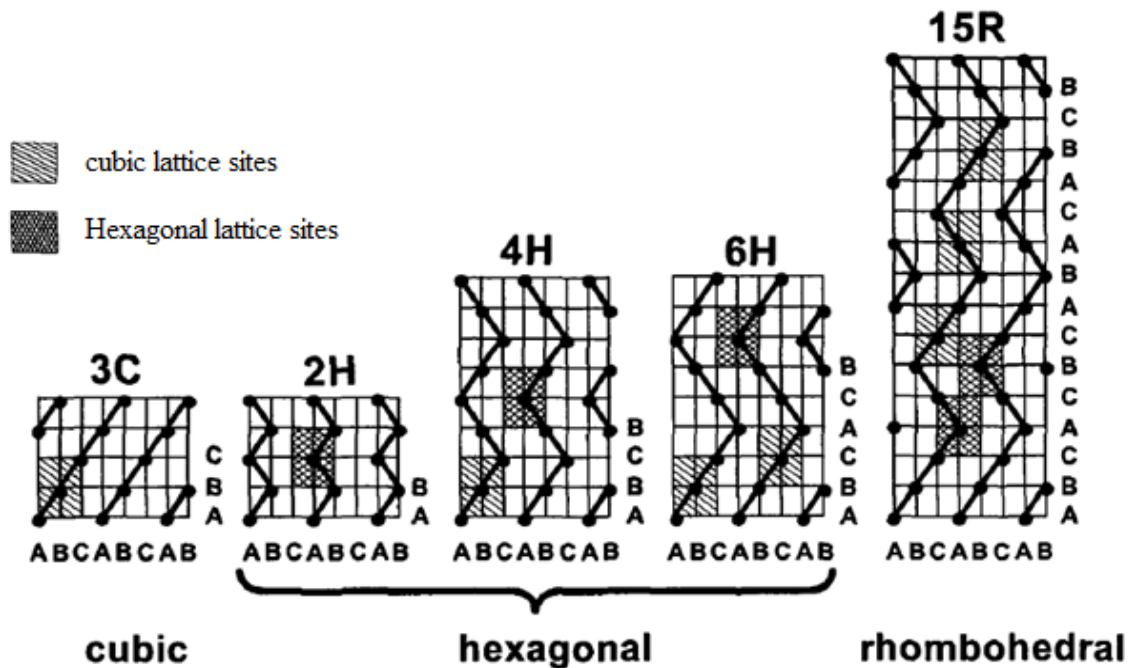


Figure1.2: SiC poly-types [1]

Over 200 polytypes of SiC are known to exist. Some of the common polytypes includes 3C, 2H, 4H, 6H, 8H, 9R, 10H, 14H, 15R, 19R, 20H, 21H, and 24R. With the exception of 2H and 3C, all of the polytypes form one-dimensional super lattice structures. [3]

**In this thesis work, we will calculate the Power Dissipation for Uniformly doped profile and Linearly graded profile at different value of current density  $J_{on}$ . We will also calculate the punch through voltage  $V_{PBV}$ .**

### 1.3. Outline of the thesis

**Chapter-1** Introduces the reader to the world of silicon, gives the limitations imposed by silicon across a wide spectrum of applications and further suggests the new material, Silicon Carbide.

**Chapter-2** Starts with the physical and electrical properties of SiC, The chapter also surveys the SiC material growth, SiC technology, its polytypes (3C, 4H, 6H etc), properties and its applications.

**Chapter-3** In this chapter starts with the Schottky barrier diode, working of Schottky barrier diode and its limitation.

**Chapter-4** The formulation for uniformly doping profile for 3C-SiC Schottky barrier diode , calculation of  $R_{on-sp}$ , power dissipation, critical electric field and for the avalanche breakdown voltage.

**Chapter-5** Presents the formulation & calculations for linearly graded profile for Power dissipation, for the depletion region width and doping concentration  $N_{eff}$  It then presents the stability in the avalanche breakdown voltage nearly closed to the punch through voltage.

**Chapter-6** Includes conclusion and further improvement which is possible.

## Silicon Carbide Materials- Properties and Silicon Carbide Devices

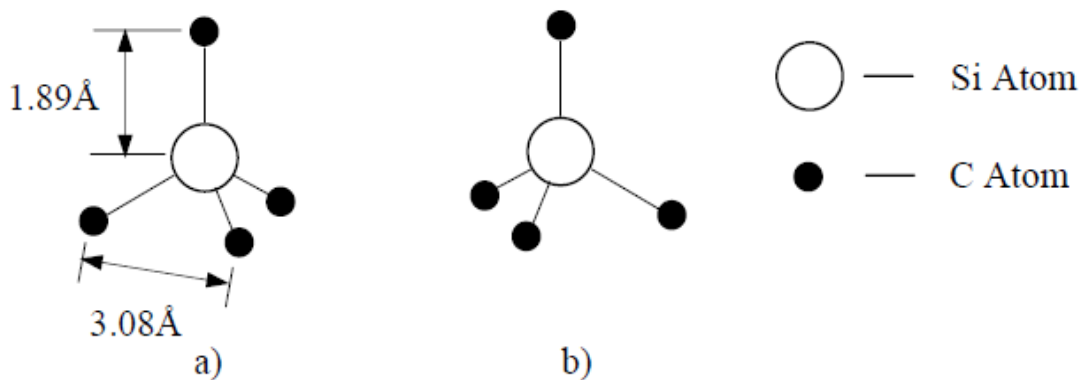
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Silicon Carbide (SiC) is a wide band gap semiconductor with specific electrical properties such as a high breakdown electric field, a high thermal conductivity and a high inertness. Recently, new breakthroughs in the fields of material growth and of technological processes have been proposed [1], which will boost the development of SiC microelectronic devices and its industrial production. Concretely, production of high quality material on large area wafers is now possible, allowing the fabrication of reliable high temperature, high frequency or high current power electronic devices, improving the already optimized Silicon based structures. SiC devices possess a very wide range of industrial applications, such as spacecraft, aircraft, automobile, communication or energy distribution, among others. Therefore, SiC devices are expected to play a fundamental role, in normal life and in the cutting edge investigations, for high current/voltage management or harsh environments in the 21century. An additional advantage of SiC is that among compound semiconductors, only These insulating layers are of paramount importance in nearly all the SiC applications described below. The breakdown field in SiC is about 8 times higher than in silicon. SiC can be thermally oxidized to grow insulating, high quality SiO<sub>2</sub> layers.

This is important for high-voltage power switching transistors. For example, a device of given size in SiC will have a blocking voltage 8 times higher than the same device in silicon. More importantly, the on-resistance of the SiC device will be about 100 times lower than the silicon device [2].

**2.1. Fundamental SiC Material Properties:** SiC offers significant advantages for power electronics applications such as lamp ballasts, motor controls, medical electronics, automotive electronics, high-density high-frequency power supplies and smart-power application-specific integrated circuits. Quality native oxide for use as an insulator in

electronic devices. Silicon carbide can resist high field strengths and offers better heat conducting capacity than copper at room temperature. Due to high thermal conductivity and high breakdown electric field strength, SiC can be used at high temperature, high voltage, high frequency and high power applications. This chapter briefly surveys the SiC semiconductor electronics technology. In particular, the differences between SiC electronics technology and well-known silicon VLSI technology are highlighted. Projected performance benefits of SiC electronics are highlighted for several large-scale applications. Key crystal growth and device-fabrication issues that presently limit the performance and capability of high temperature and/or high power SiC electronics are identified [5]. The arrangement of Si and C atoms in SiC can be described as a covalently bonded tetrahedral, as shown in Figure 2.1(a).



**Figure 2.1:** Basic tetrahedral unit in SiC consisting of a tetrahedron of four C atoms with one Si atom in the middle: a) Basic tetrahedron with bond lengths. b) Basic tetrahedron rotated 180° around the stacking direction [6].

The approximate bond length between the Si-Si or C-C atoms is 3.08 Å, while the approximate bond length between the Si-C atoms is 1.89 Å [6]. The SiC crystals are formed by the tetrahedrons joined to each other at the corners. In order to maintain the tetrahedral geometry of the lattice, each successive bilayer can be placed in one of only three positions with respect to the underlying plane. The probability of occurrence of different polytypes depends on temperature. Among the many polytypes, 3C-SiC and 6H-SiC have a higher

probability of occurrence. Generally 3C-SiC is stable in the low-temperature region below 1800<sup>0</sup>C, and 6H-SiC is stable in the higher temperature region above 1800<sup>0</sup>C. Although 4H SiC also sometimes occurs in the high temperature region, the probability is very lower compared to 6H-SiC. [7]

Each polytype has unique electrical and physical properties. Silicon carbide has been regarded as a wide band gap semiconductor material for visible light- emitting devices, since electro luminescence was observed for the first time in 1907, and a light emitting diode was fabricated for the first time in 1923 [7]. However, the stable characteristics of SiC have caused difficulty in producing high quality layers and large single crystal growth, and thus the development of semiconductor technology in SiC has been delayed. However a wide range of devices have already been demonstrated, including: Bipolar Junction Transistor (BJT), Insulated Gate Bipolar Transistor (IGFET), MESFET, JFET, p-n Junction and Schottky diodes. Silicon carbide is a new material, and the processes involved are different to those of silicon, and some of the process steps are still in their infancy. SiC is a very hard material and almost inert, which makes SiC processing problematical. Implantation of dopants is difficult to perform, especially p-type, and the etch rate is slow. Schottky and Ohmic contacts are now fairly well developed processes in SiC. SiC epitaxial layer growth is also well established, and bulk wafers with an epitaxial layer structure are supplied from wafer manufacturers. Hence, the etching of structures in epitaxial layers is the most common method for the manufacture of SiC devices. SiC has SiO<sub>2</sub> as its naturally occurring oxide, although the quality of the oxide layer reported is not as good as for silicon, suffering from both low surface mobility and low breakdown strength. This is large drawback for MOSFET devices which would be very promising for high temperature electronic devices. However, much research is focused on this particular area and the quality is constantly increasing.[8]

Rhenium is the only known metal that is thermodynamically stable in contact with SiC, i.e., Re has a tie-line to SiC in a ternary Si-C-Re phase diagram. The stability of Re thin films on 3C-SiC up to 1100 C was experimentally confirmed in a study. This stability makes Re an interesting candidate for a stable Schottky contact in high-temperature applications. However, chemical stability is too crude a guide to ensure the stability of the electrical characteristics of the contact. The present study aims at evaluating the thermal stability of the Schottky barrier height of sputter-deposited Re contacts to n-type 6H-SiC. [32]

### **2.1.1 Transport Properties:**

A large part of this work has been devoted to discovering reliable transport parameters for different SiC polytypes, mainly 4H-SiC. For reliable and efficient device performance, analysis of transport parameters is required. Published measurements are the main source of information used in the tuning process of the transport models. The immature nature of silicon carbide, and lack of measurements for many transport properties, implies that the available set of transport parameters is incomplete.

#### **2.1.1.1 Mobility**

The mobility defines that how easily the electrons and holes can be moved in an electric field. Due to random scattering within the crystal, the velocity does not increase with constant acceleration as in a vacuum. The electron velocity rather quickly reaches an equilibrium mean-velocity proportional to the mobility and the electric field. The mobility in SiC is somewhat lower than for silicon and much lower than in high mobility materials, such as GaAs. The low mobility in SiC devices is compensated by operation at larger electric fields taking advantage of the higher carrier velocity. To some extent the mobility can be described using the same models as those used for silicon. The parameters for the mobility models are collected from measurements for a temperature dependent mobility model [15].

#### **2.1.1.2 Saturation Velocity**

At high electric fields the velocity ceases to be proportional to the electric field, due to increased scattering. The velocity saturates at  $v_{sat}$ , which for SiC is approximately twice the value for silicon. A high saturation velocity allows faster devices with shorter switching times.

#### **2.1.1.3 Band Gap**

The band gap is a forbidden zone in the energy spectra for a crystal. Without a band-gap the crystal is a metal, and with a large band-gap the crystal is an insulator. A semiconductor has a band-gap up to a few eV. For some traditional semiconductors the band gaps are: 1.1eV for Si, 0.7eV for Ge, and 1.4eV for GaAs. Many of the favorable transport parameters in SiC are related to the large band-gap, which is of the order of 3eV. For such a

large band gap the intrinsic carrier concentration is negligible at temperatures up to 600°C. The intrinsic carrier concentration is responsible for the thermal noise, and also partly responsible for the leakage current, which are both very small in large band-gap materials. The minimum energy required to create an electron-hole pair is equal to the band-gap that in SiC falls within the 3eV range corresponding to a photon with wavelength close to 400 nm. SiC devices are thus also insensitive to the main part of the visible spectrum, making SiC suitable as a detector material for UV radiation with minimal noise from the visible background [10].

### **2.1.2. Critical Electric Field**

For high electric fields the carrier energy is increasing and as the energy exceeds the band-gap, the probability of an impact ionization event increases. In an impact-ionization event the carrier knocks out one electron from the valence-band, creating an electron-hole pair (EHP). As the energy must be conserved, the energy for the incident carrier is reduced by the band gap energy plus the initial energy for the created electron and hole.

The critical electric field is related to the impact ionization rate, which increases as the carrier energy exceeds the band-gap. Due to the large band- gap the critical electric field is thus about 10 times higher in SiC than for small band-gap materials, such as Si and GaAs. With high Ecrit devices can be much smaller for the same voltage, alternatively operate at much higher voltages.

### **2.1.3. Thermal Conductivity**

The thermal conductivity for SiC is close to copper. Thermal conductivity is a quality that is very important in power semiconductor devices in order to transport the heat in the device. For high power devices the thermal effects constitute one of the main limiting factor of the performance. One of SiC's competitors is gallium nitride (GaN), which is a material with similar properties to those of SiC but which are less mature. One drawback of gallium nitride is the even lower thermal conductivity than silicon (1.3 W/cmK). However, gallium nitride is often grown on SiC substrates, with its better thermal conductivity. Nevertheless, the GaN-SiC interface has lower thermal conductivity than GaN itself which leads to a degradation of the performance.

#### **2.1.4. Surface Mobility**

The surface mobility describes the transport in the inversion layer of a MOSFET device and is critical for device performance. Pioneering experiments have given very poor values for the surface mobility in SiC devices in the range of  $10 \text{ cm}^2/\text{Vs}$  [10]. The low mobility is related to the high defect density in the oxide-semiconductor interface and doubts about SiC MOSFETs as commercial devices have been expressed in many quarters. The mobility is presently reaching values above  $150 \text{ cm}^2/\text{Vs}$  and commercial MOSFETs are expected to appear in the market shortly.[15]

#### **2.1.5. Impact Ionization**

For high-power devices the impact ionization process is very important for accurate predictions of the high power performance. Many of the pioneering measurements reported a positive temperature coefficient of the impact ionization coefficient. As the impact ionization heats the lattice, such behavior would further increase the impact ionization. This would be a very serious problem, causing local hot spots, unstable operation and thermal runaway, destroying the device. In later measurements the impact ionization coefficient shows a negative temperature dependency and thus the positive sign presented previously was mainly contributed to by the presence of deep levels in the samples used.

The SiC lattice consists of alternating planes of silicon and carbon atoms, and the stacking sequence of these planes defines different polytypes of the material identified by the repeating distance of the stacking sequence (e.g. 3C, 4H & 6H). Silicon carbide occurs in many different crystal structures, called polytypes. Despite the fact that all SiC polytypes chemically consist of 50% carbon atoms covalently bonded with 50% silicon atoms, each SiC polytype has its own distinct set of electrical semiconductor properties. While there are over 100 known polytypes of SiC, only a few are commonly grown in are producible forms

### **2.2 SiC Semiconductor Electrical Properties**

Some of the more important semiconductor electrical properties of the 3C, 4H, and 6H silicon carbide polytypes are given in table.2.1 [10]. Even within a given poly-type, some important electrical properties are non-isotropic, in that they are a strong functions of crystallographic direction of current flow and applied electric field. Do pants in SiC can

incorporate into energetically in equivalent quasi-hexagonal (h) C-sites or Si-sites, or quasicubic (k) C-sites or Si-sites. While all dopant ionization energies associated with various do pant incorporation sites should normally be considered for almost accuracy.

**Table 2.1:** Table 2.1 Comparison of electronic properties of SiC with Si, GaAs and GaN [10]

	Si	GaAs	GaN	6H-SiC	4H-SiC	3C-SiC
Band gap (eV)	1.1	1.142	3.39	3	3.26	2.2
Breakdown field @ $10^{17} \text{ cm}^{-3}$ (MV/cm)	0.6	0.6	3.3	3.3	3.0	1.5
Electron mobility@ $10^{16} \text{ cm}^{-3}$ ( $\text{cm}^2/\text{V-s}$ )	1100	6000	1000	370	800	750
Hole mobility @ $10^{16} \text{ cm}^{-3}$ ( $\text{cm}^2/\text{V-s}$ )	420	320	200	90	115	40
Saturated electron drift velocity (cm/s)	$10^7$	$10^7$	$2.5 \times 10^7$	$2 \times 10^7$	$2 \times 10^7$	$2 \times 10^7$
Intrinsic concentration, $n_i(\text{cm}^{-3})$	$1.5 \times 10^{10}$	$1.79 \times 10^6$	$2.1 \times 10^6$	$2.3 \times 10^{-6}$	$8.2 \times 10^{-9}$	6.9
Thermal conductivity	1.5	0.55	1.3	4.9	4.9	5

Silicon is the semiconductor employed in most commercial solid-state electronics; it is the yardstick by which other semiconductor materials must be evaluated against. To varying degrees the major SiC poly-types exhibit advantages and disadvantages in basic material properties compared to silicon. The most beneficial inherent material superiorities of SiC over silicon are its exceptionally high breakdown electric field, wide band gap energy, high thermal conductivity and high carrier saturation velocity.

## 2.3 SiC important poly-types and definition

Silicon carbide exists in hundreds of different polytypes, the most common being 3C-SiC, 4H-SiC and 6H-SiC. Furthermore, islands of 15R-SiC can be found on 4H-SiC and 6H SiC wafers and small crystals of 2H-SiC have been grown. The digit in the name is the number of double layers (one Si and one C layer) in the primitive lattice cell; the character gives the type of crystal symmetry. H stands for hexagonal, C for cubic and R for rhombohedral. A schematic view of some of the different SiC polytypes is presented in Fig.2.2. In the hexagonal structure a clear distinction exists between the different directions in the lattice. The direction parallel to the central axis in the hexagonal structure is called the crystal axis, or c-axis. In commercially available wafers the c-axis is normally oriented perpendicular to the surface, usually being a few degrees off axis. SiC is the only known stable binary compound of Silicon (Si) and Carbon (C). It contains an equal number of Silicon and Carbon atoms. The basic structural unit of SiC is a covalently bonded (88% covalent and 12% ionic) tetrahedron between Si and C atoms. Each Si atom is covalently bonded with four C atoms in a tetrahedral structure and similarly, each C atom is bonded to four Si atoms. The approximate bond length between the Si-Si or C-C atoms is 3.08Å, while the approximate bond length between the Si-C atoms is 1.89Å [1]. The SiC crystals are formed by the tetrahedrons joined to each other at the corners.

The transport parameters for the most common SiC polytypes, together with some other semiconductors, are presented in Table 2.1[10].

### 2.3.1 6H-SiC

6H-SiC has a large anisotropy due to the long repetition length in the crystallographic lattice. The mobility in the direction perpendicular to the c- axis (commonly parallel to the surface) is four times greater than in the c- axis direction. Compared with Si the mobility in 6H-SiC is about 25% in the direction perpendicular to the c-axis, and 7% in the direction parallel to it. The saturation velocity for 6H-SiC is  $2 \times 10^7$  cm/s in the direction perpendicular to the c-axis, but only  $0.6 \times 10^7$  cm/s in the direction parallel to it.

### 2.3.2 4H- SiC

The low-field mobility for 4H-SiC is about half that of silicon with a small anisotropy (20% higher in the direction parallel to the c-axis). The anisotropy in 4H-SiC depends on the electric field, and at high electric fields the saturation velocity is 20% lower in the c-axis direction. 4H-SiC and 6H-SiC are the most mature polytypes and they are the ones which have been characterized most thoroughly. The transport properties are better for 4H-SiC and, at present, this polytype forms the basis for most of the commercial products [5].

### 2.3.3. 3C-SiC

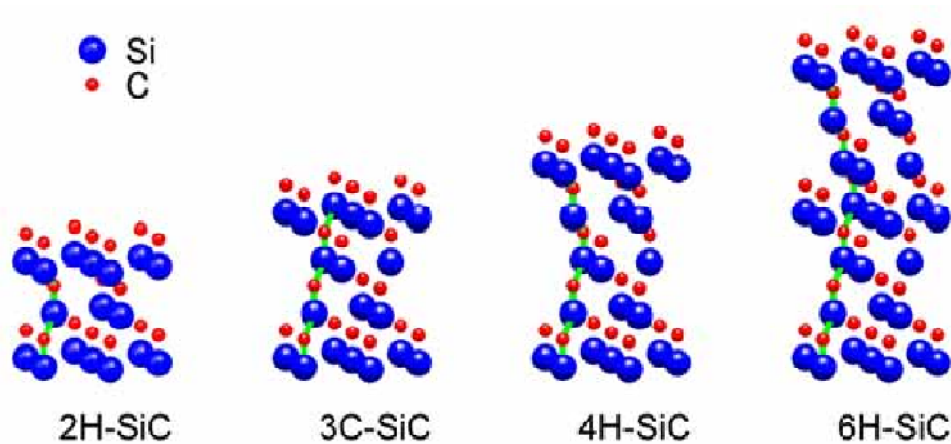
3C-SiC has an advantage as it is able to be grown on silicon substrates, however at the moment with reduced quality. It allows the possibility of integration of 3C-SiC devices with silicon technology on the same chip in future. Another advantage is that 3C-SiC does not suffer from stacking faults growth, as these tend to grow towards 3C-SiC. 3CSiC has larger electron mobility than for 4H-SiC but has reduced hole mobility. The main disadvantages when compared to other polytypes are the lower band-gap and breakdown field and the advantage of replacing existing silicon devices is strongly reduced [1].

### 2.3.4 15R-SiC

15R-SiC is very complex, namely 15 atomic layers ordered in a rhombohedral structure. A few years ago, much attention was focused on 15R-SiC, owing to improved experimental MOSFET performance when compared to the other polytypes [8]. These devices have been manufactured on 4H-SiC or 6H-SiC, where pieces of 15R-SiC were found. Mono-crystalline 15R- SiC wafers are however not a reality in the near future.

### 2.3.5. 2H-SiC

2H-SiC is not a commercially available substrate, but small mono-crystalline pieces have been grown. The performance perpendicular to the c-axis direction is similar to 4H-SiC, but the mobility is better in the parallel to the c axis direction (similar to silicon) [8]



**Figure.2.2.** Schematic Structure for some Different SiC Poly-types [8]

## 2.4 Silicon carbide devices

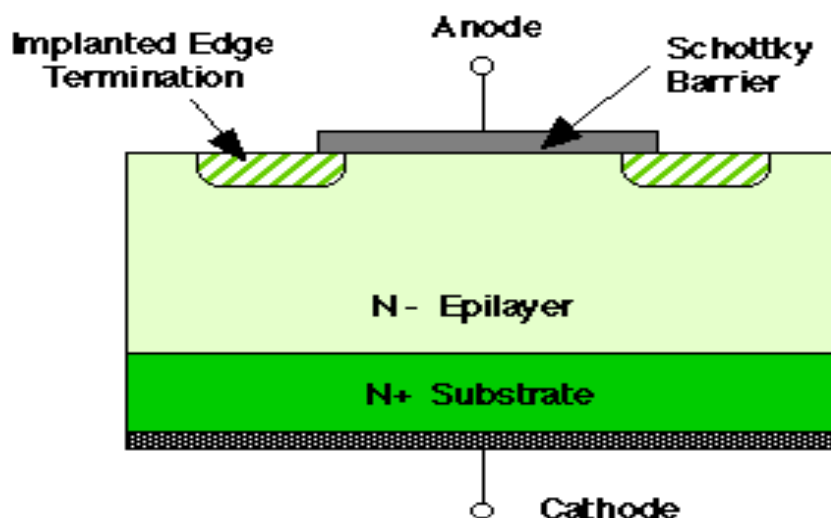
Most of silicon carbide's superior intrinsic electrical properties have been known for decades. At the genesis of the semiconductor electronics era, SiC was considered an early transistor material candidate along with germanium and silicon. However, reproducible wafers of reasonable consistency, size, quality, and availability are a prerequisite for commercial mass-production of semiconductor electronics. Many semiconductor materials can be melted and reproducibly recrystallized into large single-crystals with the aid of a seed crystal, such as in the Czochralski method employed in the manufacture of almost all silicon wafers, enabling reasonably large wafers to be mass-produced [9]. SiC sublimes instead of melting at reasonably attainable pressures, therefore SiC cannot be grown by conventional melt-growth techniques. This prevented the realization of SiC crystals suitable for mass production until the late 1980's. Prior to 1980, experimental SiC electronic devices were confined to small (typically  $\sim 1 \text{ cm}^2$ ); irregularly shaped SiC crystal platelets grown as a by-product of the Acheson process for manufacturing industrial abrasives (e.g., sandpaper) or by the Lely process [12]. In the Lely process, SiC sublimed from polycrystalline SiC powder at temperatures near  $2500^\circ\text{C}$  are randomly condensed on the walls of a cavity forming small-hexagonally shaped platelets. While these small, non-reproducible crystals permitted some basic SiC electronics research, they were clearly not suitable for semiconductor mass production. As such, silicon became the dominant semiconductor fuelling the solid-state technology revolution, while interest in SiC-based microelectronics was limited.

### Different Silicon Carbide Devices:

Silicon carbide has several unique properties that can lead to enhanced performance in device. These properties include higher breakdown field, wider band gap, lower thermal generation rate, and lower intrinsic carrier concentration.[12] the fabrication and characterization of silicon carbide (SiC) Schottky-barrier mixer diodes of 25- and 50- m diameter on a conducting 4H-SiC wafer. The single-balanced mixer circuits with a diode in each arm (two diodes total) were tested at 200 MHz (VHF) and 1.5 GHz [global positioning system (GPS)][33].

#### 2.4.1 Schottky Barrier Diode

Schottky barrier diodes offer unique advantages over conventional p-n rectifiers in terms of lower resistance, faster response, and negligible transient reverse current during switching. In addition, the reverse saturation current of Schottky diodes [10] is larger than that of p-n junction diodes. Therefore, a Schottky diode requires less forward bias voltage to achieve a given current than does a p-n junction diode. Schottky diodes based on silicon carbide (SiC) are of special importance owing to their capability of handling high voltages and high temperatures.

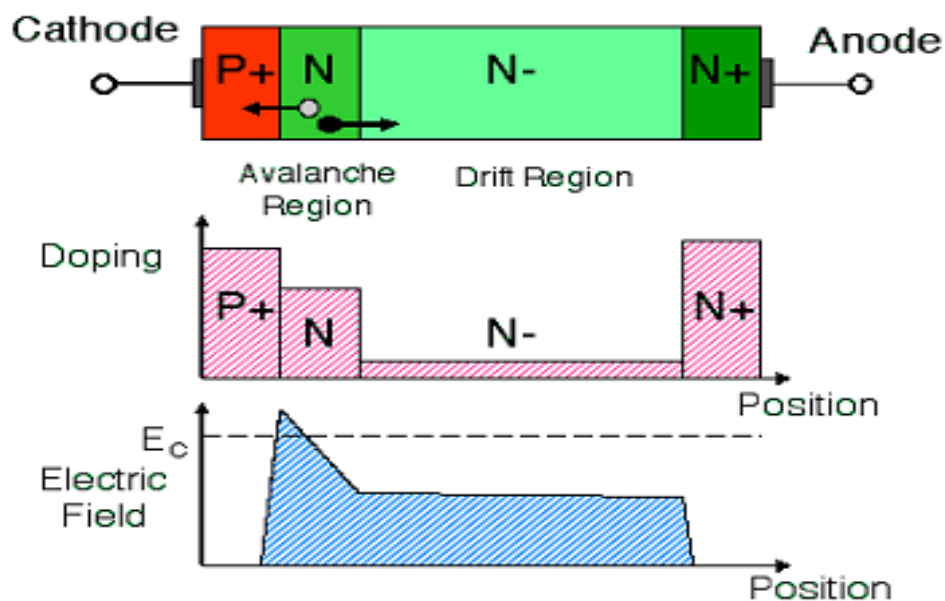


**Figure2.3:** Cross section of an implant-edge-terminated Schottky barrier diode in SiC [10]

SiC possesses exceptional chemical and physical properties such as high thermal conductivity, a wide band gap, high breakdown field, high saturation velocity, and chemical stability. Therefore, metal-SiC Schottky contacts are suitable electrical devices for harsh environments such as high voltage rectifiers, UV radiation detectors, signal mixers, and high temperature gas sensor. cross section of SBD shown in figure 2.3

#### 2.4.2 Silicon Carbide IMPATT Diode:

Silicon carbide is an ideal semiconductor for the fabrication of high-power microwave devices due to its high breakdown field. One device, in particular, that benefit from the high breakdown field of SiC is the IMPact ionization Avalanche Transit-Time (IMPATT) diode oscillator. [16]



**Figure: 2.4** Cross section of a SiC IMPATT diode [16]

IMPATT diodes deliver the highest RF power of any semiconductor microwave oscillator, and are used to produce carrier signals for microwave transmission systems, particularly airborne and ground-based radar. Depending upon the design, IMPATT diodes can operate from few GHz to few hundred GHz. The power-frequency product ( $p f_2$ ) of an IMPATT

diode scales as the square of the critical field for avalanche breakdown times the electron saturation drift velocity. Hole-electron pairs are created at the point of highest electric field (the "Avalanche Region"). Holes are swept into the cathode, but electrons drift toward the anode, inducing a displacement current in the external circuit as they drift. Figure 2.4 shows the buildup of microwave oscillations in the diode current and voltage when the diode is embedded in a resonant cavity and biased at breakdown.

### 2.4.3 Charge Coupled Devices

Charge coupled devices (CCDs) are linear shift registers formed by a series of closely spaced MOS plates on the surface of a semiconductor. Application of bias voltages to the MOS plates results in the creation of localized potential wells in the semiconductor under each plate. Charge packets can be confined in the potential wells and shifted along the surface under the influence of appropriate clocking waveforms applied to the gates. Silicon CCDs are widely used as image sensors, particularly in digital still cameras and hand-held video cameras. SiC is of interest as a specialized image sensor because its wide band gap makes it transparent to visible light, resulting in an ultraviolet (UV) sensor which is virtually blind to solar radiation. Such a sensor has applications in aerospace research, UV astronomy and in military systems. In this structure, the source and drain junctions and the buried n-type channel are formed by nitrogen ion implantation and the implants are activated by high temperature annealing. The gate oxide is thermally grown using the optimized conditions identified in MOS investigations. Then deposit a layer of polysilicon for the first-level gates and dope the poly with phosphorus. The polysilicon is patterned by reactive ion etching and oxidized to form a passivation layer. A second layer of polysilicon is then deposited and doped to form the second-level gates.[16]

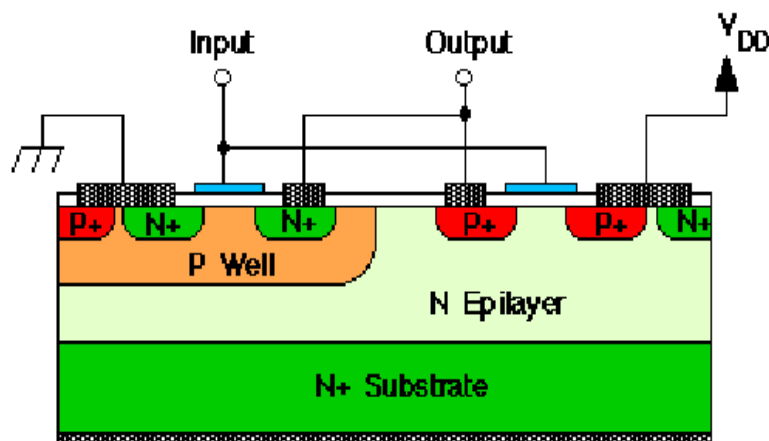
### 2.4.4 Silicon Carbide Non-volatile Memory Devices

4H silicon carbide is a single-crystal semi conducting material with a band gap of 3.26 eV. This wide band gap results in an extremely low value for the intrinsic carrier concentration in room temperature, about 16 orders of magnitude lower than silicon. Since thermal generation scales directly with the intrinsic carrier concentration, leakage currents in SiC are negligible [17]

### 2.4.5 Digital CMOS Integrated Circuits in SiC

CMOS technology is attractive for digital logic because it offers low power consumption, full rail-to-rail output swing, and greater noise margins than NMOS circuits. CMOS also provides active current sources for linear applications. Development of CMOS technology in SiC is expected to provide low power, high temperature circuits as well as reliable control circuitry for smart power integrated circuits. Process utilized an implanted n-well and deposited oxides, but due to other processing problems the PMOSFETs exhibited a very high threshold voltage. Implanted p-well and thermally grown oxide is used to fabricate this device. The fabrication sequence is as follows:[18]

1. P-wells are formed on n-type epilayers doped at  $8 \times 10^{15} \text{cm}^{-3}$  by boron implantation. Al and N are then implanted through polysilicon masks to form P+ and N+ source/drain regions, respectively.



**Figure: 2.5** Cross section of a CMOS inverter in the implanted p-well process [18].

2. NMOSFETs are formed on p-wells while the PMOSFETs are formed on n-type epilayers. Implants are annealed at  $160^{\circ}\text{C}$  for 40 minutes in argon, followed by an  $115^{\circ}\text{C}$ , 2 hour wet oxidation to form a 40 nm gate oxide layer.
3. Poly silicon is then deposited and patterned to form the gates. Al-Ni is used for p type ohmic contacts and Ni for n-type contacts. A silicon oxynitride layer is deposited as an inter-metallic dielectric.
4. Vi as are opened and interconnect metal is deposited and patterned.

#### 2.4.6 3C-SiC Power MOSFETs

The breakdown electric field of SiC is approximately 8 times higher than silicon. This makes it possible to design power switching devices having correspondingly higher blocking voltages than their silicon counter parts. More importantly, the specific on resistance (i.e. resistance-area product) of a power device scales inversely as the cube of the breakdown field, so the on resistance of SiC power MOSFETs are 100-200 times lower than comparable devices in silicon.[19]

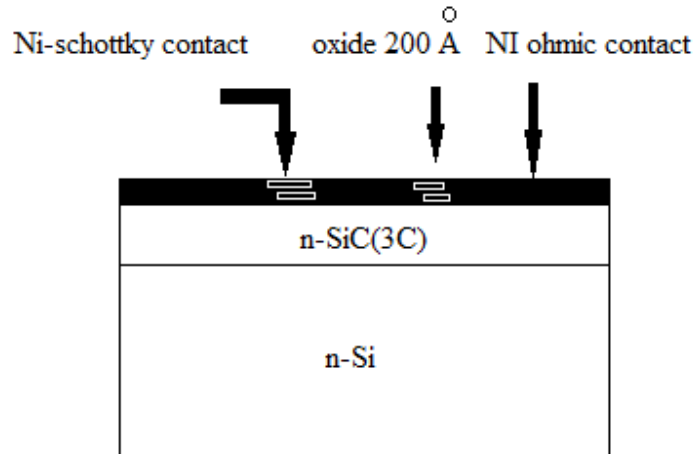
**Introduction**

Because SiC has excellent properties such as a wide band gap, a high critical electric field, a high thermal conductivity and a high electron saturation velocity, silicon carbide (SiC) is one of the most prominent candidates for the next generation semiconductor devices. Implantation, oxidation, self aligned silicides formation, etc., have been applied to SiC, and a variety of high-power and high-frequency SiC devices (Schottky diodes, MESFETs, VJFETs, SITs, etc.) have been demonstrated in the last years. The best expression of the potentialities of the material remains strictly related to the improvement of some technological concerns.[11]

**3C-SiC Schottky barrier diode**

SiC has many desirable characteristics for high power, high temperature, high frequency semiconductor devices: wide band gap, high thermal conductivity, high electron saturated velocity. In the area of power semiconductors, Si devices can usually provide either high speed (Schottky barrier diodes) or high breakdown (p-i-n diodes), but not both. In principle, SiC can provide both of these characteristics. Indeed, very high breakdown voltage has been achieved with 6H-SiC p-n junction diodes ( $V_b=1000V$ ) and with 3C-SiC p-n junction diodes ( $V_w=200V$ ) grown on 6H-SiC substrates. 6H SiC Schottky diodes have been reported to provide 400V breakdown and a switching speed superior to Si p- i- n diodes. However, all of these structures use 6H-SiC substrates which, while being a tremendous technical advance, [19] have a small diameter are quite expensive and are available in only limited quantities. A cross-section of the 3C-SiC/Si Schottky diode is shown schematically in

Fig.3.1. The SiC film (-2000Å) is grown by propane carbonization of n-Si substrates at 1300°C for 90 sec. To provide isolation between the

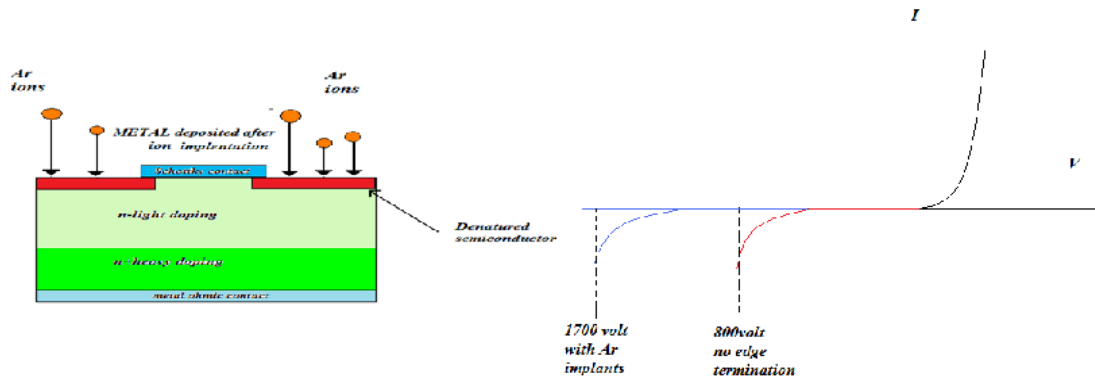


**Figure: 3.1** Schematic of Al-Ni 3C-SiC/Si Schottky diode on 5-7  $\Omega$ -cm n-Si substrates.[20]

Schottky and ohmic metal-SiC contacts, SiC oxidation is performed next in steam at 1050°C for 20 minutes producing ~200Å of SiO<sub>2</sub>. A photolithographic process then defines the ohmic contact region followed by Ni= deposition by magnetron sputtering. The thickness of the Ni film is 4000 Å. After a lift-off process, high temperature (900°C) rapid thermal annealing is carried-out for 3-5 min in a N<sub>2</sub> ambient. The Ni Schottky contact region is fabricated last, with the same process as the ohmic contact except for the omission of the high temperature annealing step.[21]

Metal-semiconductor contacts fall into two basic categories, the ohmic and the rectifying (or Schottky) contacts. An ohmic contact has a linear and symmetric current-voltage characteristic for positive and negative applied voltages and a negligible resistance compared with that of the bulk of the device. Conversely, a rectifying Schottky contact is characterized by the current flow for only one voltage sign. In order to introduce the important physical parameters which affect the contact performance, the classical description of the Schottky barrier formation is briefly reported. Silicon Carbide was one of the earliest semiconductor materials discovered. However, due to the difficulties of growing good quality crystals, the progress of SiC devices has lagged behind those of its counterpart materials. In recent years, SiC devices development have enjoyed remarkable progress and demonstrated significant

advantages over Si devices in the area of high power electronics due to its superior physical and electrical properties. With a significantly wider band gap (2.3eV for 3C-SiC, 2.9eV for 6H-SiC and 3.2eV for 4H-SiC) than silicon, the critical field of SiC is approximately eight to ten times higher than that of the latter. As a result,



**Figure: 3.2:** cross-section of SBD and V-I characteristic [22]

SiC high voltage devices can be realized on much thinner drift layers with higher doping, leading to orders-of-magnitude lower device on-state resistance. Silicon Carbide (SiC) Schottky Barrier Diode (SBD) was the first SiC power device demonstrated. It was studied as early as 1974 Throughout the years, as single crystalline SiC material became commercially available and its quality improved steadily, substantial amount of work and study has been done on SiC SBDs as well as Merged P-i-N Schottky diodes (MPS) and Junction Barrier Schottky (JBS) diodes. Schottky contacts on 3C, 6H and 4H SiC with a large variety of metals were made and their performance studied. Device designs on SBD, MPS and JBS diodes were also extensively investigated. Impressive progresses and developments have been made. Recently, SiC SBDs with breakdown voltage higher than 10 KV has been reported. SiC MPS diodes capable of 4.3kV were also reported.[24]

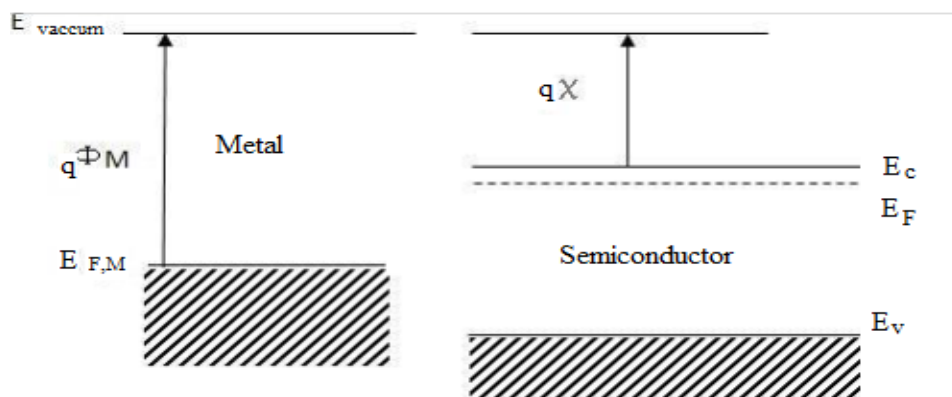
### 3.2 Operation

Forward current in a Schottky diode is due to majority carrier injection from the semiconductor to the metal. Reverse current is also due to majority carriers that overcome the Schottky barrier and this is very dependent on temperature. The Schottky has fast switching

action, and switching speed is controlled by thermalization of hot injected doping carriers of semiconductors across the junction. The switching speed of a Schottky diode will occur in few picoseconds. The semiconductor material used in the research was 3C-SiC with n-type doping. The Schottky diode has two different metal contacts on a semiconductor, a Schottky (rectifying) contact and an ohmic contact. Metal to semiconductor contacts are important since they are present in every semiconductor device [25]. A metal to semiconductor contact can behave as a Schottky barrier or as an ohmic contact depending upon the characteristics of the interface. A metal can be characterized by a work function ( $\Phi_m$ ), the minimum energy required to move an electron from the metal to the vacuum level. The barrier between the metal and semiconductor can be identified on an energy band diagram. In an energy band diagram, metal and semiconductor are aligned using the same vacuum level as shown in Figure 3.3 and Figure 3.4. When the metal and semiconductor are brought together there will be a barrier established between the metal and semiconductor interface. This barrier height  $\Phi_B$  is the energy required to free up an electron from metal ( $\Phi_m$ ) minus the energy required to remove the electron from n-type semiconductor material (called electron affinity,  $\chi$ ) which is given by 3.2[23].

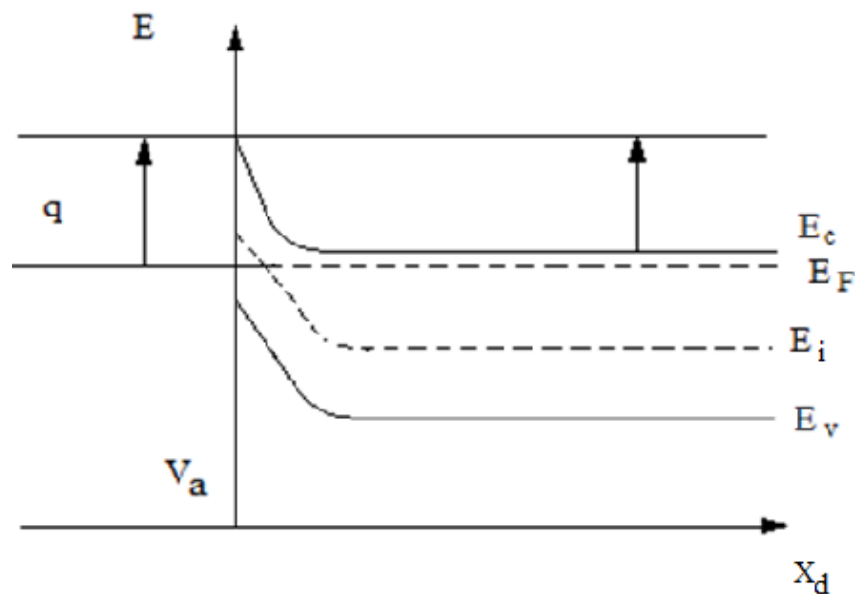
$$\Phi_B = \Phi_m - \chi \quad (3.1)$$

Barrier height is measured in the eV and the electron affinity for 4H-SiC is 4.17 eV.



**Figure. 3.3.** Energy band gap of M-S before contact[24]

Whenever metal and semiconductor align together, only a small number of electrons have the energy to get over the barrier and cross to the metal. When a bias voltage is applied to the junction, it can have two effects: it can make the barrier appear lower from the semiconductor side, or it can make it appear higher. The bias does not change the barrier from the metal side. When the barrier is large, the electrons need more energy to cross the barrier and the contact has rectifying behavior also called Schottky contact. When the barrier is small, electrons can move freely from the semiconductor to the metal and the contact is called ohmic contact. The ohmic behavior is indicated by a linear current-voltage characteristic. [24]



**Figure3.4** Energy band gap of M-S after contact and before thermal equilibrium [24]

Experimental barrier height often differs from the calculated barrier height due to the chemical reactions between the metal and the semiconductor. The cleaning procedure used and the ideal metal-semiconductor theory assumes both the materials are pure, and that there is no interaction between the two materials and no unwanted interfacial layer [24].

Electrons in the n-type semiconductor can lower energy by traversing the junction. As electrons leave the semiconductor, a positive charge stays behind due to the ionized donor atoms. Electrons flow into the metal until equilibrium is reached between the diffusion of

electrons from the semiconductor into the metal and the drift of electrons caused by the field created by ionized impurity atoms. This equilibrium is called thermal equilibrium and it is characterized by a constant Fermi level throughout the structure as shown in Figure 3.4. Under thermal equilibrium with no external voltage applied, there is a region in the semiconductor close to the junction which is depleted of mobile carriers; this is called depletion region [22]. The built-in potential, the applied voltage, and the doping concentration play a large role in the width of the depletion region. When a forward-bias voltage  $V_a$  is applied to the Schottky barrier, the contact potential will be reduced by  $qV_a$ . As a result, electrons in the semiconductor conduction band diffuse across the depletion region to the metal. This gives rise to a forward current. Conversely, a reverse bias increases the barrier and the electron flow from semiconductor to metal is negligible.

### 3.3 Current-Voltage (I-V) characterization

Current flows in a Schottky barrier diode because charge transfers from the semiconductor to the metal or vice versa. The four basic mechanisms by which carrier transportation can occur are:

- 1) Thermionic emission over the energy barrier
- 2) Tunneling through the barrier
- 3) Carrier recombination or generation in the depletion region
- 4) Carrier recombination in the natural region of the semiconductor

Thermionic emission is the dominant mechanism in Schottky barrier junctions. The thermionic emission is derived from the assumption that the barrier height ( $\phi_B$ ) is much larger than  $kT$ . Thermal equilibrium established at the junction determines emission and the existence of a net current flow. At the junction, there are two currents, one flow from the metal to the semiconductor and the other flows from the semiconductor to the metal. The current flow depends on the barrier height. In thermionic emission theory, the effect of drift and diffusion in the depletion region is assumed to be negligible [24, 29]. Therefore, the standard thermionic emission relation for electron transport from the metal to the semiconductor with low doping concentration is given by. (3.2)

$$I_F = I_0 \left[ \frac{q(V_a - IR_S)}{nKT} \right] \left( 1 - \exp \left\{ \frac{-q(V_a - IR_S)}{KT} \right\} \right) \quad (3.2)$$

$I_0$  is the reverse saturation current which is dependent on the barrier  $\phi_B$  for electron injection from the metal into the semiconductor and is given by

$$I_0 = AA^* T^2 \exp\left(\frac{-q\phi_B}{KT}\right) \quad (3.3)$$

where  $I_F$  is the forward current,  $A$  = area of the Schottky contact,  $\phi_B$  = Zero bias Schottky barrier height,  $A^*$  = Richardson constant,  $R_S$  = series resistance,  $K$  = Boltzmann constant and  $n$  = ideality factor. The barrier is unaffected by the applied bias voltage. Under negligible series resistance and high bias ( $3kT/q \ll V_a \ll IR_S$ ), the forward current simplifies to 3.4

$$I_F = I_0 \exp\left(\frac{qV_a}{nKT}\right) \quad (3.4)$$

From the forward bias current equation Schottky diodes behave as rectifiers with easy current flow in the forward direction and little current in the reverse direction. Figure 3.4 shows the energy band diagram of the metal semiconductor junction under forward and reverse biased conditions.

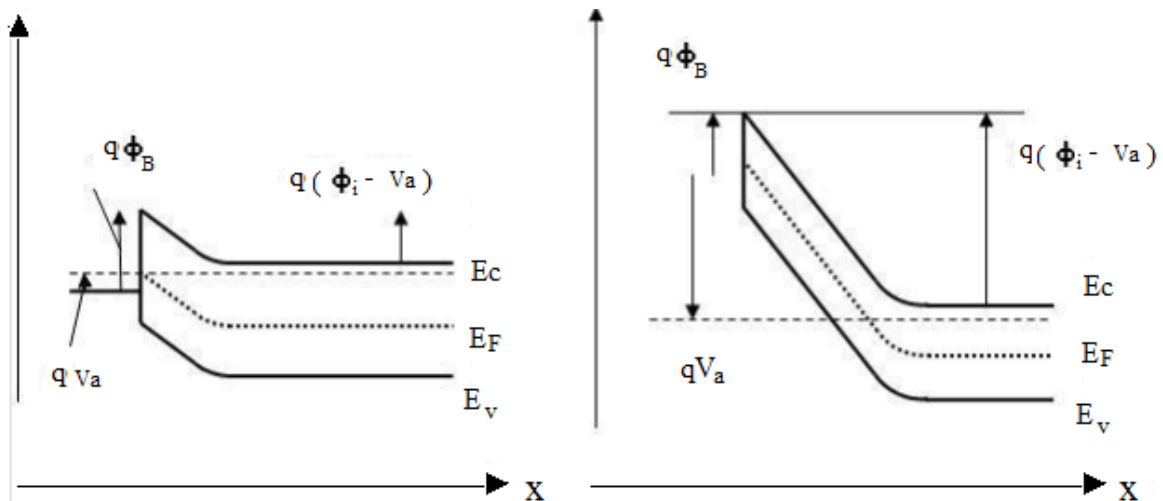


Figure 3.5 Energy band diagram of (a) forward biased (b) reverse biased M-S junction[24]

The depletion width is also dependent on the high doping density. High doping concentration makes a thin depletion width and promotes more tunneling. The depletion width is given by (3.4)

$$W = \sqrt{\frac{2\epsilon(V_{bi}-V_a)}{N_D}} \quad (3.5)$$

Where

$W$	=	Width of the depletion region
$V_{bi}$	=	Built-in potential.
$V_a$	=	Applied voltage.
$N_D$	=	Doping concentration.
$\epsilon$	=	permittivity

Taking natural logs of both sides of (3.5) gives

$$\ln(I_F) = \ln(I_0) + \frac{q}{nKT} V_a \quad (3.6)$$

From (3.3)

$$\ln(I_0) = \ln(AA^*T^2) - \frac{q}{KT} \phi_B \quad (3.7)$$

From the (3.3), the plot of  $\ln(I_F)$  versus the applied voltage  $V_a$  gives a straight line whose slope is  $q/nkT$  and intercept is  $\ln(I_0)$ . From this current-voltage (I-V) characterization, the ideality factor ( $n$ ) can be determined from the slope and the barrier height ( $\phi_B$ ) can be determined from the intercept and by using (3.6)

### 3.4 The On-Resistance ( $R_{on}$ )

The specific on-resistance ( $R_{on}$ ) of the diode is an important parameter for high efficiency power devices. In this study, on-resistance was obtained by first determining the series resistance  $R_s$  of the diode for the non-linear region of the  $\ln(I_F)$  versus  $V_a$  plot. For  $V \gg 3kT/q$ , (3.2) simplifies to

$$I = AA^*T^2 \exp\left(\frac{-q\phi_B}{KT}\right) \exp\left[\frac{q(V-IR_S)}{nKT}\right] \quad (3.8)$$

where now  $I_F$  is represented by  $I$  and  $V_a$  is represented by  $V$ . (3.8) can be rearranged to give

$$I = \frac{1}{R_S} \left[ \frac{dV}{d[\ln(I)]} \right] - \left( \frac{KT}{q} \right) \left( \frac{n}{R_S} \right) \quad (3.9)$$

By plotting current ( $I$ ) against  $dV/d[\ln(I)]$ , the series resistance is obtained from the reciprocal of the slope of the linear section of the graph or from the intercept. The on resistance ( $R_{on}$ ) is determined by multiplying series resistance with the area of the diode.[28]

### 3.5 Capacitance in a Schottky Barrier Diode

A useful technique for determining not only barrier height, but also the average ionized doping concentration profile is measuring the capacitance,  $C$ , of a deeply depleted Schottky barrier diode. To perform the measurement, a small a.c. signal is superimposed on top of a d.c. bias. The a.c. signal provides a measurable charge fluctuation at the edge of the depletion region.[29] The d.c. bias is used to sweep the SBD further and further into reverse bias. This increasing depletion width reduces capacitance as given by

$$C = \frac{K_S \epsilon_0 A}{W} \quad (3.10)$$

where  $C$  is the measured capacitance and  $A$  is the area of the contact. Knowing the width of the depletion region as a function of applied bias from (3.7), a doping profile can be extracted from this measurement.

### 3.6 Breakdown Voltage in a Schottky Barrier Diode

An important characteristic of power devices is the blocking voltage that the device can handle before “breaking down”. The breakdown of a device is characterized by the impact ionization of carriers within the depletion region. Applying larger reverse biases leads to an increase in the peak electric field inside the device as established. As the electric field grows, the acceleration of the carriers being swept through the depletion region is increased. The acceleration will increase to the point where the carrier has enough energy to ionize an atom

in the semiconductor lattice, in other words, create an electron-hole pair. This is known as impact ionization. Impact ionization can begin to occur unbounded if the electron-hole pair that is originally created through impact ionization gains enough energy to impact ionize another lattice site, and the newly created electron-hole pair causes impact ionization at another site, and so on.

As newly created electron-hole pairs create their own new electron-hole pairs, an avalanche of electron-hole pair creation begins. This exponentially increasing avalanching causes the current to quickly tend towards negative infinity. As such, this snowball effect of electron hole pair creation is aptly named avalanche breakdown. This occurs at the breakdown voltage,  $V_{bd}$ , which can be found as

$$V_{bd} = \frac{K_S \epsilon_0 E_{cr}^2}{2qN_D} \quad (3.11)$$

Where  $E_{cr}$  is the critical electric field and  $N_D$  is the doping of the substrate or epi-layer, provided the epilayer is not punched-through. This is the simplest definition of breakdown. For a more rigorous derivation, the reader is referred to [25]

### 3.7 Schottky Diode Performances

Schottky diodes are of interest for high-power devices because they are majority carrier devices and consequently have very fast switching times and no reverse recovery current. Here, some important properties of Schottky barrier diodes for power rectifiers will be described.[28]

#### 3.7.1 Specific on-Resistance

The specific on-resistance should be as low as possible for high power device operation..The specific on-resistance is given by

$$R_{on-sp} = \frac{W}{q\mu_n N_D} = \frac{4V_B^2}{e\mu_n E_c^3} \quad (3.12)$$

$$= \left( \frac{W}{q\mu_n N_D} \right)_{Epi-layer} + \left( \frac{W}{q\mu_n N_D} \right)_{substrate} \quad (3.13)$$

Where  $W$  is the thickness of epilayer and substrate,  $V_B$  is the breakdown voltage,  $q$  charge of Electron,  $n \mu$  is electron mobility,  $N_D$  is doping,  $E_C$  is critical electric field.

### 3.7.2 Forward Voltage Drop

Forward voltage drop is given by the equation

$$V_F = \frac{nKT}{q} \ln \left( \frac{J_F}{A^* T^2} \right) + \eta \phi_B + R_{on-sp} J_F \quad (3.14)$$

Where  $h$  is the ideality factor,  $k$  is the Boltzman's constant,  $J_F$  is the forward current density  $\phi_B$  is barrier height,  $R_{on-sp}$  is specific on resistance and  $A^*$  is the Richardson's constant. The forward voltage drop ( $V_F$ ) is a function of the temperature, Schottky barrier height, and specific on resistance.[31]

### 3.7.3 Breakdown Voltage and Reverse Leakage Current

The breakdown is given by

$$V_B = \frac{\epsilon_s E_C^2}{2qN_D} \quad (3.15)$$

The breakdown voltage depends on the critical field, epilayer doping and thickness, and edge termination. For a given epilayer thickness, a decrease in epilayer doping does not necessarily increase the breakdown voltage since the decrease in doping may correspondingly decrease the critical field. The reverse leakage current is given by the equation

$$J_L = A^* T^2 \exp \left( \frac{-q\phi_B}{KT} \right) \quad (3.16)$$

The reverse leakage current is affected by Schottky barrier height, temperature, and image force barrier height lowering. The leakage current density of the Schottky rectifier increases rapidly with the temperature. Using (3.15) a plot of the leakage current of a Schottky rectifier as a function of the temperature and Schottky barrier height is shown in figure (3.4).the leakage current density of the Schottky rectifier increases rapidly with the temperature.



4

## Calculations for Uniformly Doped Drift Region Profile

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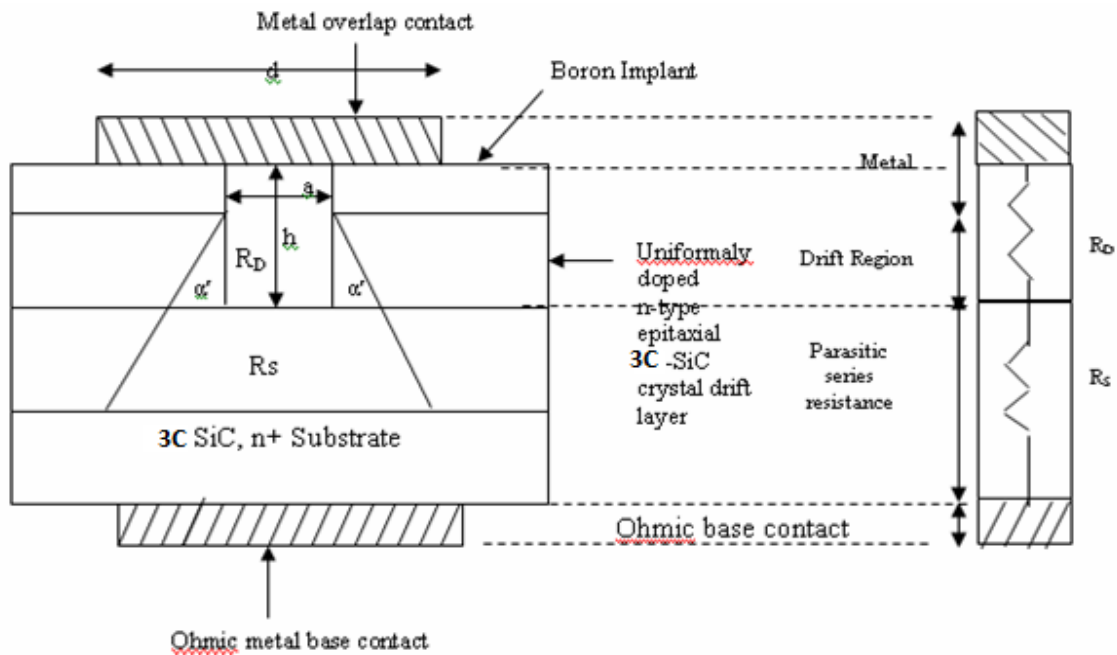
### Introduction

Compared to silicon, silicon carbide (SiC) has certain physical properties that put it on a higher platform for use in solid-state power devices. A low intrinsic carrier concentration of the order of  $10^{-7}$  per cc, a 10x higher breakdown electrical field, typically about 3 MV/cm, and a 3-fold higher thermal conductivity coupled with a large saturated drift velocity of  $2 \cdot 10^7$  cm/s are some of the salient features of SiC. These devices are extremely attractive in applications requiring blocking voltages ranging from 300 V to 3 kV. High-voltage SiC devices are thinner and can be heavily doped if needed.[30] At equivalent breakdown voltages, they offer specific on-resistance ( $R_{on-sp}$ ) which may be up to two orders of magnitude lower compared to silicon devices. The forward voltage drop of SiC devices is well below 2.5 V for a 600V Schottky barrier diode (SBD) even at a current density of 4000 A/cm<sup>2</sup> and  $R_{on-sp}$  of these devices, due to the thinner drift region, is 200 times less than that of the silicon counterparts .

### 4.1 Uniformly doped profile:

The common device structure of a 3C-SiC SBD is shown in figure 4.1 and it's equivalent circuit is also drawn in figure 4.2. The SBD shown in figure 4.1 consists of a block of n-type 3C-SiC crystal with a given height 'h'. The metal contact at the top has a cross-sectional area 'A' and there is a base contact which may be formed using a metal or an alloy. Boron implant is made for edge termination on either side of the Schottky contact. An overlap exists between the top metallic contact of width 'd' and the contact length 'a'. The current flow from the top contact is considered trapezoidal in shape spreading through the drift region by an angle ' $\alpha$ ' with the vertical at the corner edge of the boron implant beneath the contact. A standard value of ' $\alpha$ ' =  $26^\circ$  is taken for this model, which allows a small

spread of current from the top contact to uniformly flow into the n+-substrate below. The equivalent circuit shown in Figure 4.2 of the SBD has  $R_{on-sp}$  which is the sum of the series  $R_{on-sp}$  of the drift region ( $R_D$ ) and the parasitic series resistance ( $R_s$ ) with uniform current flow. Beneath this region is the n+-type heavily doped substrate region whose resistance may be considered to be zero.



**Figure 4.1:** The structure and region of a SBD [30]      **Figure 4.2:** Equivalent circuit of SBD

#### 4.2 Device equations:

The equation to evaluated  $R_{on-sp}$  of the device can be given by[26]

$$R_{on-sp} = \rho_D \frac{d}{\tan \alpha'} \ln \left[ 1 + \frac{2h}{a} \tan \alpha' \right] \quad 4.1$$

$$R_{on-sp} = \rho_D \frac{a}{\tan \alpha'} \ln \left[ 1 + \frac{2h}{a} \tan \alpha' \right] \quad 4.2$$

Where

$d=a$  for minimum overlap of contact metal considered and

$h$  = Device height ( $\mu\text{m}$ ),

$\alpha'$  = Angle of slope of the drift region narrowing (Degree)

Where

$$\rho_D = \frac{1}{\mu_N e N_D} \quad 4.3$$

$N_D$  is the donor density in the epitaxial layer.(/cc)

$\mu_N$  is the electron mobility (cm<sup>2</sup>/v.sec)

### Depletion region width:

The depletion width is calculated using the formula

$$W = \sqrt{\frac{2\epsilon_s(V_{bi}+V_R)}{eN_D}} = \sqrt{\frac{2\epsilon_s V_R}{eN_D}} \quad 4.4$$

Where

$V_{bi}$  is the built in potential and  $V_{bi} \ll V_R$ , the applied reverse voltage which is equal to the avalanche breakdown voltage,  $\epsilon_s$  denotes the permittivity of 3C-SiC.

### Critical electrical field:

The equation connecting the breakdown field strength  $E_c$  on the doping level  $N_D$  for a p<sup>+</sup>-n diode of 3C-SiC has been given. Based on these result the relationship between  $E_c$  and  $N_B$  was obtained [15]

$$E_c^{3C-SiC} = 1.95 \times 10^4 N_B^{0.131} \text{ (V/cm)} \quad [15] \quad 4.5$$

### The power dissipation:

The equation for power dissipation  $P_D$  for a 50% duty cycle can be written as[30]

$$P_D = \frac{1}{2} (J_{on}^2 A R_{on-sp} + J_l A V_B) \text{ (watts)} \quad 4.6$$

Where

$J_{on}$  = On-state current density (amps/cm<sup>2</sup>),

$A$  = Device cross-sectional area for current flow (cm<sup>2</sup>),

$V_B$  = reverse blocking voltage

$J_l$  =leakage current density, the magnitude of  $J_l$  in SiC devices is too small compared to that in silicon devices and hence the second term in equation can be neglected giving:

$$P_D = \frac{1}{2} (J_{on}^2 A R_{on-sp}) \text{ (watts)} \quad 4.7$$

### Breakdown voltage

The punch-through breakdown voltage ( $V_{PBV}$ ) is determined at a high reverse bias voltage ( $V_R$ ) for a uniformly doped semiconductor of 3C-SiC SBD and the depletion region width ( $W$ ) at this voltage is set equal to the device height ( $h$ ).

$$V_{AVBV} = \frac{1}{2} E_c W \text{ (V)} \quad 4.8$$

### Calculations:

The Punch through breakdown voltage  $V_{PBV}$  corresponding to the device height 'h' is set for 5 KV, whose depletion width is calculating using 4.4. Hence the device height 'h' is set equal to the maximum depletion region width 'W' corresponding to a breakdown voltage of 5 KV for the uniformly doped epitaxial layer with the lowest doping level of  $10^{15}$  per cc using equation 4.4. This gives a value of  $73.24\mu\text{m}$  for the device height 'h' taking  $\epsilon_s = 9.7$  for 4H-SiC. The doping-dependent mobility value is obtained from Roschke and Schwierz. The magnitude of  $R_{on-sp}$  is calculated using equation 4.2 with angle  $\alpha' = 26^\circ$  and Schottky contact of length 'a' equal to  $100\mu\text{m}$ . The contact width is equal to  $100\mu\text{m}$ . The device cross-sectional area 'A' is then  $10^{-4}\text{cm}^2$ . Specific values of the on-state current density ( $J_{on}$ ) ranging from 100 to 1000 amps/ $\text{cm}^2$  are used and the corresponding values of power dissipation ( $P_D$ ) are calculated using equation 4.7. This is repeated for doping levels of  $10^{16}$ ,  $10^{17}$  and  $10^{18}$  per cc. The results are shown in Table 4.1

Where

Permittivity of semiconductor in free space  $\epsilon_0 = 8.85 \times 10^{-14} \text{ F/cm}$

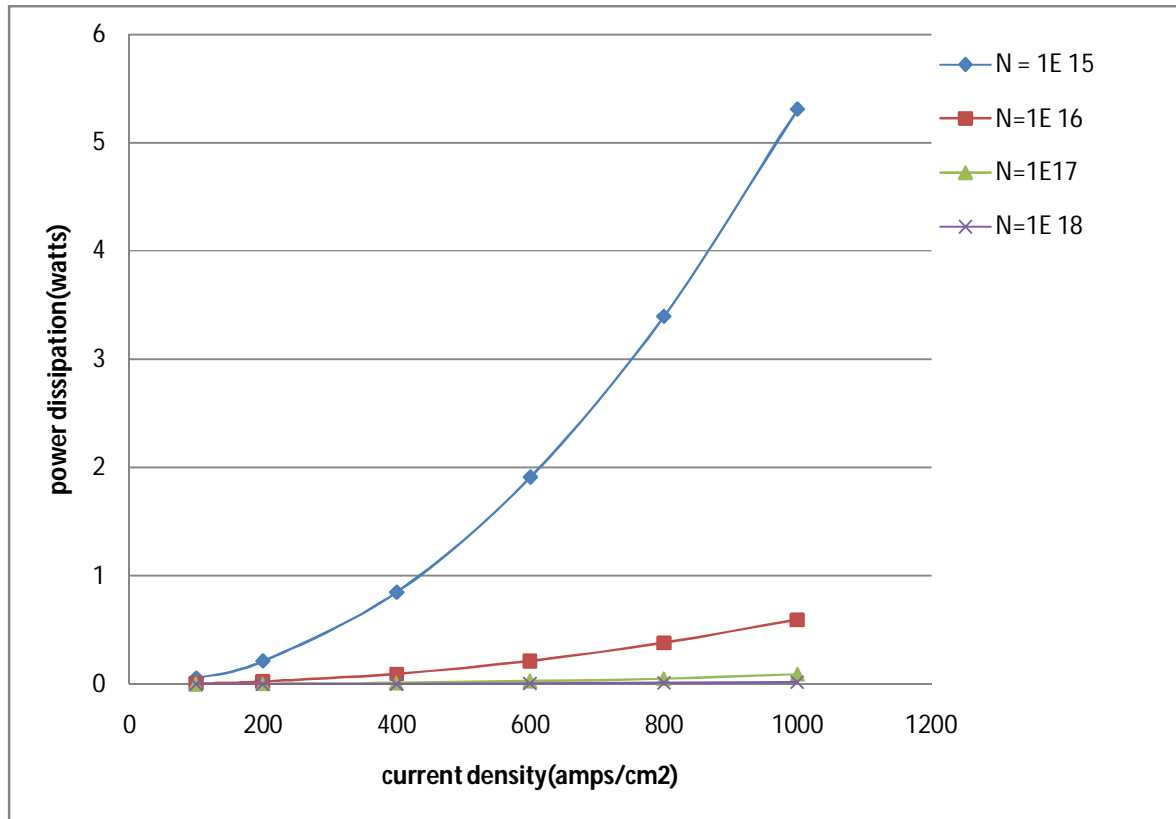
Doping concentration  $N_D = 10^{15}/\text{cm}^3$

Permittivity of SiC semiconductor  $\epsilon_s = 9.7 \epsilon_0$

Electron charge  $e = 1.6 \times 10^{-19} \text{ coulomb}$

**Table 4.1:** Calculation for Power Dissipation of 3C-SiC SBD with Uniformly Doped Profile

Current density (amps /cm <sup>2</sup> )	$N_d=1\times 10^{15}$ (atoms/cc)	$N_d=1\times 10^{16}$ (atoms/cc)	$N_d=1\times 10^{17}$ (atoms/cc)	$N_d=1\times 10^{18}$ (atoms/cc)
	$\mu_n=650\text{ cm}^2/\text{Vs}$ [15]	$\mu_n=580\text{ cm}^2/\text{Vs}$	$\mu_n=368\text{ cm}^2/\text{Vs}$	$\mu_n=192\text{ cm}^2/\text{Vs}$
	$R_{\text{on-sp}}=106.20\times 10^{-3}\ \Omega\text{-cm}^2$	$R_{\text{on-sp}}=11.5\times 10^{-3}\ \Omega\text{-cm}^2$	$R_{\text{on-sp}}=1.80\times 10^{-3}\ \Omega\text{-cm}^2$	$R_{\text{on-sp}}=0.353\times 10^{-3}\ \Omega\text{-cm}^2$
	$P_D(\times 10^{-3})$ watts	$P_D(\times 10^{-3})$ watts	$P_D(\times 10^{-3})$ watts	$P_D(\times 10^{-3})$ watts
100	53.10	5.95	0.78	0.176
200	212.42	23.86	3.13	0.706
400	249.64	95.22	12.54	2.824
600	1911.6	214.20	28.22	6.35
800	3348.4	380.50	50.17	11.29
1000	5310	595.12	90.40	17.65



**Figure: 4.3** Plot between power dissipation and current density

### Calculation for breakdown voltage

The punch through break down voltage  $V_{PBV}$  was set for a break down voltage 5KV for a 3C-SiC SBD with a uniformly doped drift region having a doping level of  $10^{15}$  per cc. The corresponding device height was equal to the depletion width  $W$  at this voltage the value was founded  $73.24 \mu\text{m}$ . the Avalanche break down voltage is calculated for the doping level of  $10^{15}$ ,  $10^{16}$ ,  $10^{17}$ ,  $10^{18}$  per cc. The avalanche breakdown voltage is obtained using the condition  $\alpha_p W = 1$ , to give the magnitude of  $\alpha_p$ .The critical field ( $E_c$ ) corresponding to this value of  $\alpha_p$  is obtained from [30].Calculation shows in table 4.1.

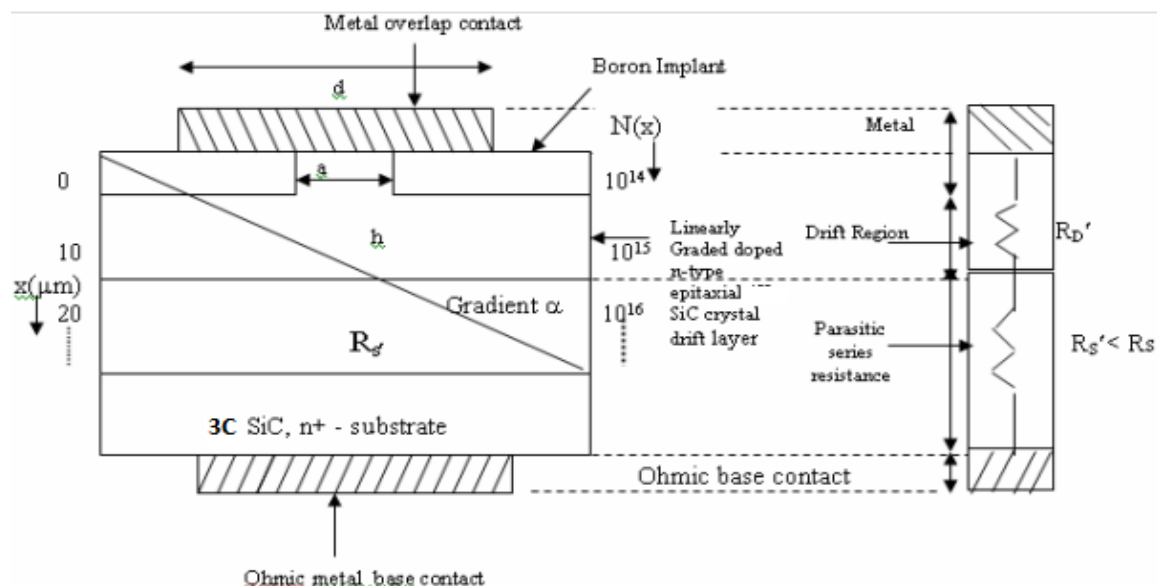
**Table 4.2:** Calculation for  $V_{AVBV}$  &  $V_{PBV}$  for uniformly doped profile  
(Device height = 73.24 $\mu$ m)

S. NO.	Doping level $N_d$ (/cc)	W( $\mu$ m)	$\alpha_p$	$E_c$ (V/cm) $\times 10^6$	$V_{AVBV}$ (KV)	$V_{PBV}$ (KV)
1.	$10^{15}$	73.24	136.53	1.799	6.58	5
2.	$10^{16}$	23.16	431.77	2.432	2.81	5
3.	$10^{17}$	7.32	1366.12	3.288	1.20	5
4.	$10^{18}$	2.31	4329	4.442	0.512	5

## Calculation for 3C-SiC SBD using Linearly Graded Drift Region

In this chapter an analysis of power dissipation, depletion region width and breakdown voltages of 3C-SiC SBD using linearly graded doped profile. In the model proposed here for the 3C-SiC SBD, the epitaxial layer is not uniformly doped but is linearly graded with a gradient  $\alpha$ . Near the contact, the device has the lowest doping level ( $N_0$ ), which increases with the gradient to any desired doping level ( $N$ ) at the substrate. This is shown in Figure 5.1. The equivalent circuit of the device is similar to Figure 5.2, with  $R_D$  replaced by  $R_D'$  and the new  $R_s$  ( $< R_s$ ) being used.  $R_s$  has a lower value than  $R_s$  as the doping level is nearer to the substrate than the contact at the top of the device.

### 5.1: linearly graded profile



**Figure:5.1** The 3C-SiC SBD with linearly graded drift region profile with gradient  $\alpha$  [26]

**Figure:5.2** The equivalent circuit of the SBD

The doping level  $N_D$  of the epitaxial layer has to be replaced by the effective doping level  $N_{eff}$  of the linearly graded drift layer.[30]

## 5.2 Device equation for linearly graded profile:

Gradient of the profile is given by the formula [30]

$$\alpha = \frac{N(x)-N(0)}{h} \quad (\text{cm}^{-4}) \quad 5.1$$

Where

$\alpha$  = gradient of profile

$N(x)$  = Desired doping density

$N(0)$  = Lower doping density, used as reference doping level for calculating the gradient at different desired doping density.

$h$  = Device height

## The equation for $R'_{on-sp}$ :

The specific on resistance of the device is given by

$$R_{on-sp} = \rho_D' \frac{a}{\tan\alpha'} \ln \left[ 1 + \frac{2h}{a} \tan\alpha' \right] \quad 5.2$$

Where

$a$  for minimum overlap of contact metal considered and

$h$  = Device height ( $\mu\text{m}$ ),

$\alpha'$  = Angle of slope of the drift region narrowing (Degree)

Where

$$\rho_D' = \frac{1}{\mu_N e N_{eff}} \quad 5.3$$

$\mu_N$  = electron mobility ( $\text{cm}^2/\text{v}\cdot\text{sec}$ )

$N_{eff}$  = Effective doping concentration (/cc)

**Depletion region width:** for linearly graded drift region of SBD,

$$W' = \sqrt[3]{\frac{12\varepsilon_s(V_g+V_R)}{e\alpha}} = \sqrt[3]{\frac{12\varepsilon_s(V_R)}{e\alpha}} \quad (\mu\text{m}) \quad 5.4$$

Where

$V_g$  is the gradient voltage and  $V_g \ll V_R$ , the applied reverse voltage which is equal to the avalanche breakdown voltage. In the two equations,

Where  $\varepsilon_s$  = Permittivity of 3C-SiC  
 $e$  = electron charge ( $1.6 \times 10^{-19}$  coulombs)  
 $V_g$  = Gradient voltage (V)  
 $N_{\text{eff}}$  = Effective doping concentration (/cc)

**Effective doping concentration:** given by [30]

$$N_{\text{eff}} = \frac{\alpha h}{\ln\left(1 + \frac{\alpha h}{N_0}\right)} \quad (/cc) \quad 5.5$$

Where

$\alpha$  = gradient of profile  
 $h$  = device height ( $\mu\text{m}$ )

**Power dissipation:**

the equation for power dissipation in linearly graded profile is given as[30]

$$P_D = \frac{1}{2} \left( J_{\text{on}}^2 A R'_{\text{on-sp}} \right) \quad (\text{watts}) \quad 5.6$$

Where

$J_{\text{on}}$  = on state current density  
 $A$  = device cross section area ( $\text{cm}^2$ )  
 $R_{\text{on-sp}}$  = specific on resistance of the device

**Critical electric field:** the critical electrical field given by

$$E_c' = \frac{e\alpha(W')^2}{8\epsilon_s} \text{ (V/cm)} \quad 5.7$$

Where

e = electron charge

W' = depletion region width for linearly graded profile ( $\mu\text{m}$ )

**The Avalanche Breakdown voltage:**

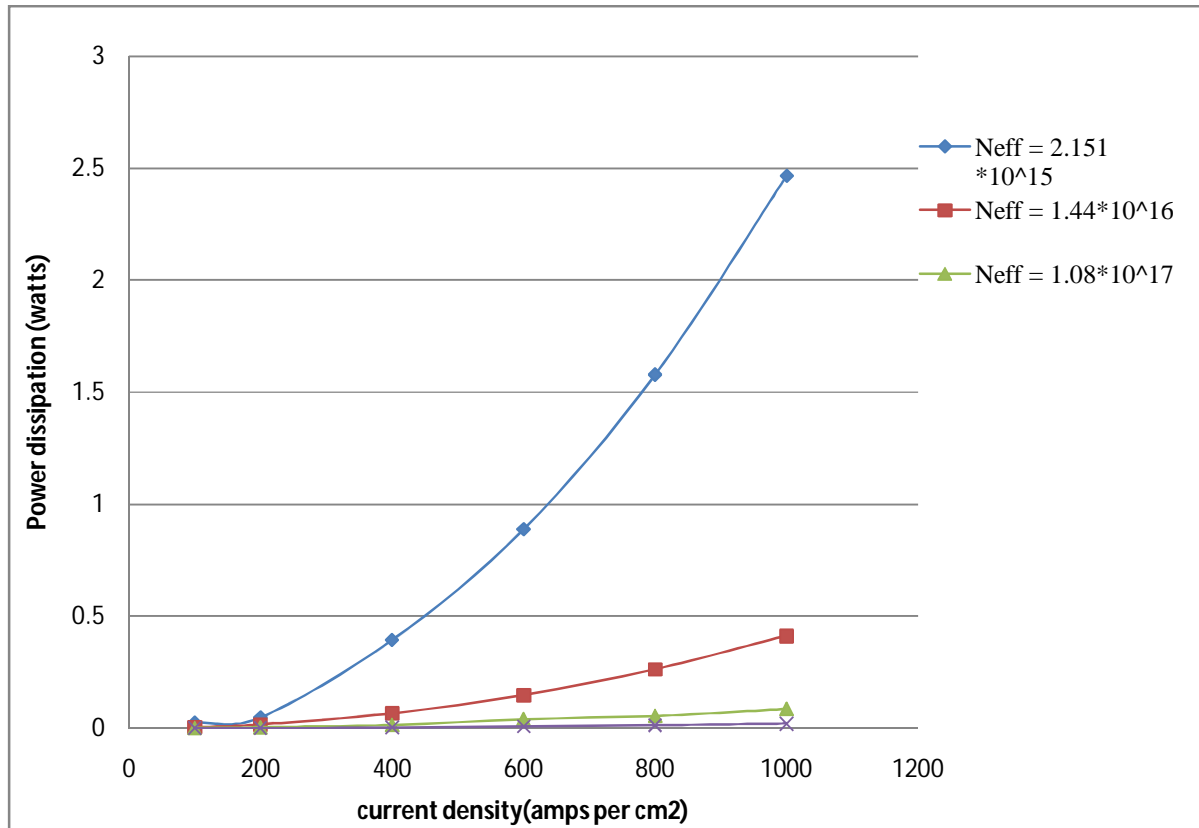
for linearly graded profile the avalanche break down voltage is give by

$$V_{AVBV} = \frac{2}{3} E_c W' \quad 5.8$$

**Calculations for power dissipation:** calculate the value of power dissipation using the set of equation of 5.1 - 5.6 for linearly graded profile and also find the value of the avalanche break down voltage and set the value of punch through voltage at 5KV. The value of power dissipation corresponding the value of current density  $J_{on}$  100 to 1000 amps/cm<sup>2</sup>. Shown in the table 5.1.

**Table 5.1:** Calculation for Power Dissipation

Current density  $J_{on}$ (amps /cm <sup>2</sup> )	Neff = $2.151 \times 10^{15}$ atoms/cc	Neff = $1.447 \times 10^{16}$ atoms/cc	Neff = $1.085 \times 10^{17}$ atoms/cc	Neff = $0.868 \times 10^{18}$ atoms/cc
	$\mu'_n = 650$ cm <sup>2</sup> per Vs	$\mu'_n = 580$ cm <sup>2</sup> per Vs	$\mu'_n = 368$ cm <sup>2</sup> per Vs	$\mu'_n = 192$ cm <sup>2</sup> per Vs
	$R'_{on-sp} = 49.39 \times 10^{-3}$ $\Omega$ -cm <sup>2</sup>	$R'_{on-sp} = 8.22 \times 10^{-3}$ $\Omega$ -cm <sup>2</sup>	$R'_{on-sp} = 1.72 \times 10^{-3}$ $\Omega$ -cm <sup>2</sup>	$R'_{on-s} = 0.408 \times 10^{-3}$ $\Omega$ -cm <sup>2</sup>
	$P_D$ (watts) $\times 10^{-2}$	$P_D$ (watts) $\times 10^{-2}$	$P_D$ (watts) $\times 10^{-2}$	$P_D$ (watts) $\times 10^{-2}$
100	2.469	0.41	0.086	0.020
200	9.576	1.64	0.344	0.081
400	39.50	6.57	1.376	0.326
600	88.88	14.79	3.096	0.734
800	158.01	26.30	5.504	1.305
1000	246.90	41.10	8.600	2.040

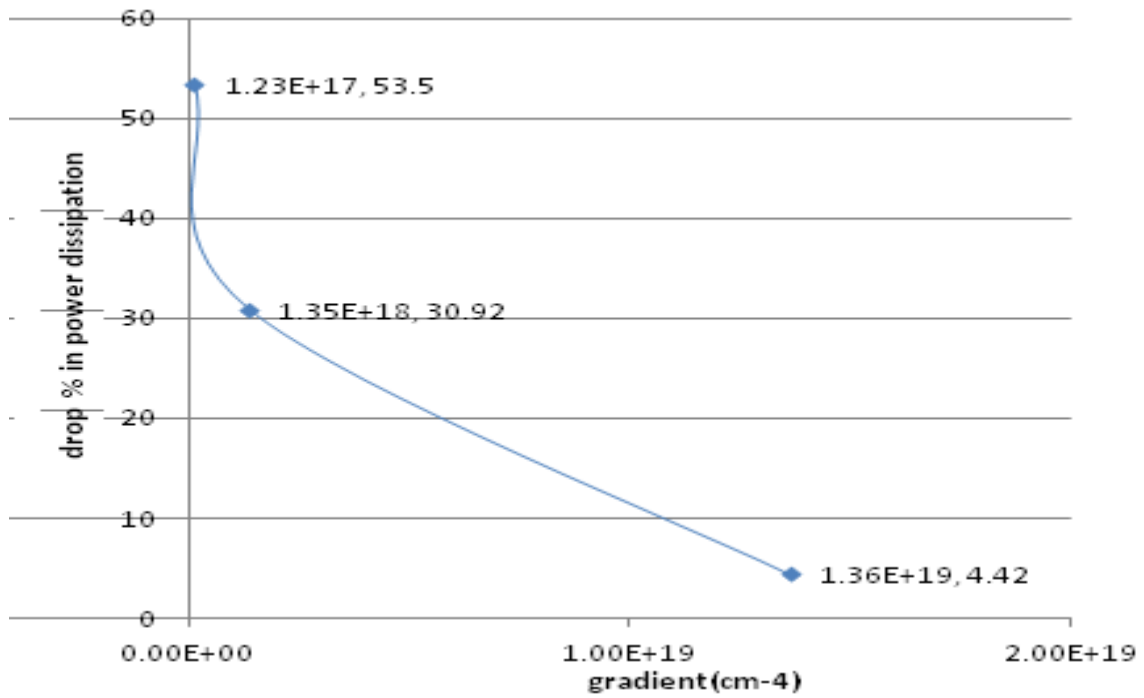


**Figure 5.3:** Plot between Current Density and Power dissipation

**Table 5.2:** Breakdown voltages  $V_{AVBV}$  &  $V_{PBV}$  of 3C-SiC SBD for linearly graded doped epitaxial layer:

(Device height  $h= 72.68\mu\text{m}$ )

S.No.	$\alpha$ (cm <sup>-4</sup> )	W' ( $\mu\text{m}$ )	Ec (V/cm)	$V_{AVBV}$ (KV)	$V_{PBV}$ (KV)
1.	$8.42 \times 10^{17}$	72.68	$1.03 \times 10^6$	4.95	5
2.	$13.54 \times 10^{17}$	62.01	$1.21 \times 10^6$	5.02	5
3.	$13.69 \times 10^{18}$	28.63	$2.60 \times 10^6$	4.99	5
4.	$13.65 \times 10^{19}$	13.31	$5.63 \times 10^6$	4.94	5
5.	$13.65 \times 10^{20}$	6.17	$1.21 \times 10^7$	4.97	5



**Figure 5.2** Plot between power dissipation drop (%) and gradient (cm<sup>-4</sup>)

In this graph, it shows that the percentage drop in power dissipation is found to increase with a decrease in gradient from 53.5% at a gradient  $1.23 \times 10^{17} \text{ cm}^{-4}$  to 4.42% at  $1.36 \times 10^{19} \text{ cm}^{-4}$ .

The calculations for power dissipation for 3C-SiC SBD with uniformly doped profile in the drift region with doping ranging from  $10^{15}$  per cc. to  $10^{18}$  per cc. have been made on the basis of variation and mobility of carriers. The effective values of  $\mu_n$  ranging from 650  $\text{cm}^2/\text{V-s}$  to 192  $\text{cm}^2/\text{V-s}$  obtained from published data [15] have been used. The estimated  $R_{on-sp}$  ranges from  $106.20 \times 10^{-3} \Omega\text{-cm}^2$  to  $0.353 \times 10^{-3} \Omega\text{-cm}^2$ . The range of on state current density for calculation of power dissipation has been considered for  $J_{on} = 100 \text{ amps/cm}^2$  to  $1000 \text{ amps/cm}^2$ . It is seen that the value of power dissipation increases significantly with increase in each order of 10 of doping level of the drift region. Thus for  $J_{on}$  of  $100 \text{ amps/cm}^2$  the value of power dissipation is 53.10mW at  $N_D = 10^{15}/\text{cc.}$ , which falls to 0.176mW at a value of  $N_D$  of  $10^{18}/\text{cc.}$  The same nature of variation can be observed at  $J_{on}$  of  $1000 \text{ amps/cm}^2$ , whereas change in power dissipation ranges from 5310mW to only 17.65mW. These variations of power dissipation with current density  $J_{on}$  are non linear in nature as shown in Figure 5.3. Power dissipation using linearly graded drift region for effective doping level which is close to those used in uniformly doped profile shows significantly high drop in power dissipation shown in Table 5.1. Thus the power dissipation at  $J_{on}$  of  $100 \text{ amps/cm}^2$  at an effective doping level of  $2.151 \times 10^{15} / \text{cc.}$  is only 24mW as against 53mW in the uniformly doped case. The power dissipation at  $10^{18}/\text{cc}$  at the same current density in the uniformly doped drift region device is 0.176mW which increases slightly to 0.20mW at almost the same level of doping of  $0.868 \times 10^{18}/\text{cc.}$  This nature of variation of reduction in power dissipation can also be seen at a current density of  $1000 \text{ amps/cm}^2$ . On the basis of the analysis of power dissipation of 3C-SiC SBDs with uniformly doped and linearly graded drift region. It can be inferred from Table 4.1 and 5.1 that linearly graded profile

devices can yield lower power dissipation, when the atomic doping level in the drift region ranges from  $10^{15}$  to  $10^{18}$ .atom/cc. in the linearly graded devices.

The plot of drop in power dissipation as percentage (%) versus concentration gradient of the drift region has been shown in Figure 5.2. It is seemed that decreasing the gradient value yields higher drop in power dissipation ranging from 4.42% at a gradient of  $1.36 \times 10^{19}$   $\text{cm}^{-4}$ , to 53.5% at a gradient of  $1.23 \times 10^{17}$   $\text{cm}^{-4}$ .

The calculation of Breakdown Voltages which includes the Avalanche Breakdown ( $V_{AVBV}$ ) and Punch-through Breakdown voltage ( $V_{PBV}$ ) for uniformly doped drift region devices have been shown in Table 4.2 and those for linearly graded drift region devices have been shown in Table 5.2. This is seen for all doping levels used in uniformly drift region device. There is hardly any tally between the two breakdown voltages. The closest equality between  $V_{AVBV}$  and  $V_{PBV}$  of 6.58 KV to 5 KV respectively can be seen at a doping level of  $10^{15}/\text{cc}$ . For higher doping level there is significant deviation of  $V_{AVBV}$  from the design  $V_{PBV}$  of 5KV. So reliable device design is difficult to achieve.

On the other hand linearly graded profile using concentration gradient  $\alpha = 8.42 \times 10^{17}$   $\text{cm}^{-4}$  to  $13.15 \times 10^{20}$   $\text{cm}^{-4}$  gives almost the same value of the two break down voltages of 5KV. Hence the linearly graded drift region device is the better option to the design. It should be noted that the device height used is 73.24 $\mu\text{m}$ .

7

## Conclusions and Future work

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The present analysis has been used to design 3C-SiC SBDs using linearly graded drift region devices, which analytically appears to be a better option for device design rather than common uniformly doped drift region devices. With recent development in crystal growth of 3C-SiC crystal by “HOYA” corporation Japan, where the crystal thickness is as large as 200 $\mu$ m has been made; hence wide depletion region width can be used, which can be used for application of higher voltage levels and subsequently fabrication of 3C-SiC SBDs with much higher breakdown voltages can be made. It would still be advisable to carry out future work on the level of Power Dissipation with such thicker devices using the uniformly doped and linearly graded drift region devices will have to be under taken and the result experimentally verified.

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