HIGH SPEED PCB DESIGNING FOR EMC IN BIOMEDICAL SYSTEMS

Thesis

Submitted for the award of

Doctor of Philosophy

by

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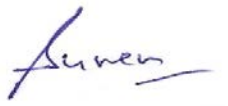
CERTIFICATE

I hereby certify that the work which is being presented in the thesis entitled "**High Speed PCB Designing for EMC in Biomedical Systems**" for the award of degree of **Doctor of Philosophy** in Electrical and Instrumentation Engineering Department, Thapar University, Patiala, is an authentic record of my own work carried out under the supervision and guidance of Dr. Ravinder Agarwal, Professor, EIED, Thapar University, Patiala and Dr. V.R. Singh, Director, School of ECE, Delhi NCR.

The results presented in this thesis have not been submitted in part or in full to any other University or Institute for the award of any degree or diploma.



Surender Singh

This is to certify that the above statement made by the candidate is correct and true to the best of our knowledge and the contents of the thesis has reached the requisite standards.

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To my dearly beloved daughter Ritika, my son, Lakshya, and my parents

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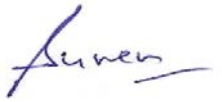
Although, I have tried to express my gratitude to every person who contributed in this work directly or indirectly, there may still be someone hiding behind the veils of my forgetful part of memory. Last but not the least, I would like to thank my parents, my wife, Kusum, my son, Lakshya, and my daughter, Ritika, for their humorous ways of motivating and supporting me through this entire process.

Above all, I owe it all to Almighty God for granting me the wisdom, health and strength to undertake this research task and enabling me to its completion.



(Surender Singh)

Abstract

High speed data (Gbps) demand for next generation high performance computing devices makes electromagnetic compatibility (EMC) and signal integrity (SI) crucial for modern medical product design. EMC and SI technologies on the printed circuit board (PCB) are the bottlenecks to achieve such high data rate.

EMC and signal integrity are major challenges in PCB, which might itself inject switching noises, thereby decreasing the EMC performance of electronic equipment, especially sensitive equipment requiring high precision, such as medical instruments.

In this research, we focus on four major problems in PCB, i.e. fiber weave effect, split plane effect, SSN and finally EMC problem. Four solutions are proposed for reducing these effects on PCB level and adversity effect to increase the EMC performance of the system.

The first solution for reducing the phase difference between the differential pair is explored, studied, and simulated on IBIS-AMI models and a solution is proposed. Fiberglass and epoxy-based dielectric substrates are ubiquitous in manufactured printed circuit boards. Their construction usually involves various woven fiberglass fabrics saturated with epoxy resin. These two materials have different electrical properties; hence, as the data rate increases and structure feature-size decreases, the fiber weaves in the substrates can have profound impacts on the effective dielectric constants of printed circuit boards, which can cause unforeseen degradations in signal integrity. This work proposes a systematic way of modeling the fiber weave effect on high-speed interconnects over low-cost substrates, and also presents a statistical analysis of the impact of the fiber weave effect on intra-pair skew of differential microstrip lines.

The second solution is proposed to overcome the split plane crossing problem for high speed interconnects. It is a geometry based method which is very effective during slot crossing. When a high frequency signal crosses the split plane gap, the return current path inductance is increased during the crossing of the plane. The inherent inductance leads to two EMC problems, creation of a radiating dipole and increased magnetic coupling. An efficient radiating dipole is created by high frequency current passing through the inductance, developing a voltage that appears across the two parts of the plane, each of which has a high capacitance. The third proposed method is directly related to the EMC parameter of the system which is very effective during the noise condition, i.e. plane coupling is used to dramatically improve the EMC parameter of the system. The last method is proposed to reduce SSN effect on the system without adding any extra cost to the product. In this work, power supply distribution network noise caused by simultaneous switching noise at printed circuit board level is controlled effectively by the use of integrated capacitors between the power planes at data speed 2.133Gbps.

In the present research work, a test board was designed for improving EMC performance of the medical system by using the proposed method. Simulation results were compared with the real measurement results of the test board, which is the right approach to correlate the results. These methodologies could be treated as handy references and general guidelines applicable to different PCB designs and could result in significant improvements of overall signal integrity performance and EMC in high speed medical system links.

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ACRONYMS

BER	Bit Error Rate
DA	Dielectric Absorption
DK	Dielectric Constant
DDR3	Double Data Rate 3
EMC	Electromagnetic compatibility
EMI	Electromagnetic Interference
EM	Electromagnetic
ESD	Electrostatic Discharge
EOS	Electric over Stress
HDMI	High-Definition Multimedia Interface
PCB	Printed Circuit Board
PDN	Power Distribution Network
PI	Power Integrity
SSN	Simultaneously switching Noise
SI	Signal Integrity
RFI	Radio Frequency Interference

CHAPTER 1

BACKGROUND DETAILS AND A SURVEY ON RELATED WORK

1.0 Introduction

Electromagnetic Compatibility **(**EMC) and Signal Integrity (SI) are important for medical devices because of the highest accuracy and quality required to meet the criticality and sensitivity of these devices [1]. The eventuality of reduced accuracy and quality may be fatal or the cause of injury at the minimum. Many hospitals are lack of awareness regarding the problem of electromagnetic compatibility of medical instruments [2]. A lot of studies are nowadays focusing on the use of several communication devices in medical environments, due to the crucial importance of the most suitable working required to hospital sophisticated electronic equipment [3]. The wide spread of wireless technology is causing concerns about EMI in the hospital environment, even if such topic remains controversial [4].

Medical devices are not only used within the premises of a medical setup, but used outside as implantable devices and medical equipment installed at residences; for example, pressure or ECG Holter, peritoneal dialysis equipment, and son. Therefore, these devices are open to the effect of a plethora of modern electronic and electrical equipment, which are ubiquitous in this modern age and each of which can be a potential electromagnetic interference (EMI) source [5]; including other medical devices that are either designed to emit electromagnetic waves or become sources because of the inherent electronic circuitry [6].

As with all electronic devices, the Printed Circuit Board (PCB) is the core of medical instruments. Power and signal integrity, which are major challenges in PCB, hat must be attended to while designing biomedical systems. PCBs can be used in essentially types of devices including lab diagnostics, drug delivery systems, imaging equipment, wireless controllers, medical implants, etc. Multi-layer PCB is very commonly used in medical electronic device. Plenty of signal integrity issues are faced with the PCB level if high speed signals travelling on the PCB [7]. In general, SI problems arise because of electromagnetic (EM) problems, such as reflection, crosstalk, and ground bounce. Therefore, understanding of the physical behavior of SI problems from EM perspective provides insight into the problem; for

example, transmission line theory is one of the most useful concepts in SI analysis. Digital instruments are often more sensitive to radio frequency interference (RFI) because they incorporate low power integrated electronic circuitry that can be much more sensitive to electromagnetic fields than electrical and electromechanical instrument [8-10]. In brief, EMC/SI in medical devices is a result of the following special characteristics of medical devices:

- Failure of medical devices can be fatal or lead to injury at the minimum.
- Some medical devices emit electromagnetic energy by design for therapy purposes such as an electrosurgical unit and radiation unit, ultra-sound.
- Some medical devices are designed to detect very small physiological signals, such as patient monitors or EEG recorders.
- Implantable medical devices and devices installed at residences are open to interference by EMI by various regularly used electronic devices.

1.2 Electromagnetic Compatibility (EMC)

Electromagnetic compatibility (EMC) is the concept of enabling different electronics devices to operate without mutual interference, that is, Electromagnetic Interference (EMI), when they are operated in close proximity to each other [11]. All electronics circuits have the possibility of picking up unwanted radiations or electrical interference, which can compromise the operation of one or other of the circuits [12]. In the early days of electronics, comparatively few items of electronics equipment were in use. However today the number of electronics items in everyday has vastly risen. Some of these transmit signals, while many others are sensitive receivers and still others may utilize digital electronics systems that could be falsely triggered by transient signals. These any many more examples make EMC a crucial element of any electronics design.

PCB design techniques for EMC compliance help to minimize the emission or reception of unwanted RF energy generated by components and circuits, thus achieving acceptable levels of EMC for electrical equipment [13]. There are two main elements of EMC:

1. Emissions: Propagation of electromagnetic interference (EMI) from noncompliant devices and, in particular, radiated and conducted electromagnetic interference.
2. Susceptibility or immunity: The detrimental effects on susceptible devices (victims) in forms that include EMI, electrostatic discharge (ESD), and electrical overstress (EOS).

EMC is grouped into two categories: Internal and External.

1. Internal: Signal degradation along a transmission path, including parasitic coupling between circuits in addition to field coupling between internal subassemblies, such as a power supply to a disk drive constitutes the internal category. These problems are specifically signal losses and reflections along the path, along with crosstalk between adjacent signal traces.
2. External Category: External problems are, emissions derived primarily from harmonics of clocks or other periodic signals and remedies to address the periodic signal to as small an area as possible, blocking parasitic coupling paths to the outside world.

To improve EMC for high-speed PCB design it is necessary for designers to analyze the power and signal integrity issues at the initial design level before the prototype board is fabricated. The integrity of an electrical signal can be measured in terms of parameters like voltage-level overshoot, undershoot, rise time, settling time, delay time, peak time, steady state response, frequency domain response, and current level in the signal. Signal Integrity concerns must be identified to effectively fix the design issues which can be controlled at the board design stage itself.

1.3 EMC Standards

The introduction of new technologies has resulted in interference problems in every day environments, such as mobile equipment onboard planes or in hospitals. Many examples and literature can cited to substantiate this statement. The Federal Aviation Association (FAA) reported many interferences on-board planes, and a pilot complained about the increasing number of interferences on-board automated planes [14]. The Food and Drug Administration (FDA)) reported 90 incidents due to EMI, with 3 people killed. One of these happened due to a malfunctioning defibrillator due to communication antennas on top an ambulance with a plastic roof [15-16]. Many interference reports have been made and there is widespread acceptance that interference is a fact of life.

With the growing awareness and need to maintain high standards of electromagnetic compatibility, many standards have been introduced to help manufacturers maintain full electromagnetic compatibility of their products.

Many organizations are looking at the issues of interference affecting day to day activities.…

- Government

  (FDA / CDRH, FCC)

- Standards Organizations

  (IEEE, ANSI, AAMI, ISO, IEC, etc.)
- Industry Groups

  (AHA, AMA, JCAHO, etc.)

International Electro technical Commission (IEC) 61000-4-3 [17] describes an EMI evaluation method for electrical devices, including medical devices, exposed to a far-field radiated Radio Frequency (RF) electromagnetic field. However, mobile phones can come into direct contact with medical devices [18-20]. In other words, electric circuits of medical devices and mobile phone antennas might have direct interaction in a near electromagnetic field region.

The electromagnetic fields radiated by the electrical devices have to be managed, and the electromagnetic interference and compatibility and the human hazard investigated. CISPR (International Special Committee on Radio Interference) SC-B WG1 has researched on the guidelines and the measurement methods for the RF interference with ISM devices, and IEC TC 62 has managed the international guidelines for the medical devices.

1.1 Electromagnetic Interference (EMI) in PCB

Electromagnetic interference (EMI) refers to undesired and unintentional electromagnetic influence on any electrical or electronic system manifesting as causative entities for a number of signal impairments and system malfunctions or degradations observed. It stems from an electromagnetic (EM) source and poses in the vicinity (of any system/ device) an EM force field (that causes the observed disruption of operation in such EMI-prone electronic device/systems). Mitigating such EMI influences with appropriate preventive strategies and designs (so as to minimize the ill-effects posed on electronic systems) defines the art of rendering EMI-prone systems being electromagnetic compatible. That is, electromagnetic compatibility (EMC) is the resulting ability of the devices/systems to operate in EMI ambient with lessened undesired impairments/degradation in performance (achieved via EMI mitigation efforts). For example, design for EMC is required for better SI. So, EMC implies a compliance- specific term dictated by specifications on a device/equipment such as medical instrumentation imposed by the Government, standard Organization, and Industry Groups.

It is almost impossible to adequately filter signal and power lines given to the current limit, making leakage current limit an important EMI-related concern while designing medical devices.

Another area of concern is emissions from equipment, which may be propagated as radiation or conduction or a combination of the two [21-22]. A PCB trace of just an inch can radiate in digital circuits operating in GHz frequencies with rise times in the order of fifty picoseconds. Radiating traces create voltage, timing, and interference problems on the line as well as across the entire board and even across adjacent boards. The problem is even more critical with mixed-signal circuits [23].

External influences, such as radio frequency interference, initially affects I/O lines through propagated fields that couple with the lines, eventually the effects are transferred to the inside of the unit and, ultimately affects to case shielding. High-speed transmission lines and sensitive adjacent traces, particularly those terminated with edge-triggered components, are the principal recipients of these effects.

1.3 Contributions and Dissertation Outline

Scope of Study:

The main focus of this thesis is to propose novel methods in identifying SI problems at PCB level of the equipment, such as medical instrumentation and to indicate design techniques to improve the EMC of such systems. This study explores the SI/EMI problems occurring due to poorly designed printed circuit board with passive and active components such as integrated circuits (I.C.s), surface mounted components, and power supply. The main aim of the study is to propose a structural approach to improve EMC in a high-speed PCB in biomedical systems.

Objectives:

1. Design high speed PCB techniques for improving EMC in biomedical systems.
    - Objectively, the research proposes a design to achieve “significant improvements” on the overall SI across high-speed transmissions at PCB level of electronics units used in medical equipment.
2. Investigate EMI effect on PCB designing by using signal integrity analysis to achieve EMC.
    - The study is conceived to investigate possible EMI effect at PCB level so that improvements on SI can be attempted to realize the mandated EMC requirements in critical medical instrumentation.

3. Validate the simulation result for high speed PCB techniques using simulation software.
    - The tasks performed thereof, are pertinent to simulations studies using, Mentor and Sigrity 3DFEM simulation tools that validate the suggested SI improvements at board level in supporting high speed signal transmission.

Motivation:

Electromagnetic Compatibility **(**EMC) and Signal Integrity (SI) are important for medical devices because of the highest accuracy and quality required to meet the criticality and sensitivity of these devices. The eventuality of reduced accuracy and quality may be fatal or the cause of injury at the minimum. In addition, design constraints, notably leakage current limitations, make the EMC design of medical electronic devices more difficult than their nonmedical counterparts. With many devices, particularly small ones, the design approach is straightforward, using basic EMC design practices including shielding and filtering. But with more complex equipment, it may not be possible to protect the entire system, for one reason or another.

My endeavor is to contribute towards the precision and effectiveness of medical equipment; thereby, enabling better diagnosis leading to optimized service to all patients in general.

Methodology:

In the present research work, test boards of 4, 6, and 8 layers were designed using Allegro tools for improving EMC performance of the medical system by using high speed PCB techniques. FR4 dielectric material is used in layer stackup in all the three boards to achieve the worst case scenario. FR4 material is used in 80-90 % of PCBs. But FR4 is a high-loss material if signal frequency is in the GHz range. Other dielectric materials available in the market are costly increasing the overall cost of the product. Dielectric material is mentioned in chapter-2 in more details.

Two simulation tools, Hyper Lynx and Sigrity 3DFEM, are used to validate the results of the test boards. The simulation accuracy of these tools is very high and are used by a majority in the industry to validate their designs. Sigrity 3DFEM tool is the fastest simulation tool; the other simulation tools usually take more than 5 days to complete a single simulation running in a high-end server with 150GB or more RAM. If any failure occurs during simulation, it adds to the wait time to run the simulation. But Sigrity 3DFEM completes single simulation in 1 or 2 days.

Finally, measurement and simulation results were compared, one set of results came from simulation tools and the other came from real measurement results on PCB. Simulation results were compared with the real measurement results of the test board, being the correct approach to correlate the results. Real measurement on PCB was done by using conventional instrument like digital CRO and spectrum analyzer.

Research Outcome:

These outcomes could be treated as handy references and general guidelines applicable to different PCB designs and could result in significant improvements of overall signal integrity performance in high-speed medical systems.

The following are the outcome from this research work.

- Design and implementation of a cost-effective impedance control method validated by the simulation results- to achieve SI in biomedical systems, specifically in PCB supporting high-speed signal transmission critically required in certain medical products.
- Reducing cost-effective, the EMI- specific noise and improve the EMC performance of medical instruments.
- Minimizing the so-called simultaneous switching noise (SSN) (typically arising from a class of EMI-specific crosstalk from adjacent driving circuits) in PCBs having high speed interfaces.
- Minimizing the so-called fiber weave effect in the PCBs supporting high-speed transport of signals, so as to significantly improve the differential pair skew.

1. The following is a brief account of the rest of the contents of this thesis. Chapter 2, includes design techniques for signal integrity, the transmission-line concept and; methods for power aware signal integrity analysis and techniques for frequency domain analysis for interconnects. This chapter also addresses alternative methods and optimal designs on several components and structures for PCB electrical interconnects, including modeling of multi-layer stackup techniques.
2. Fiber weave effect is becoming more of an issue as bit rates continue to soar upwards to 5GB/s and beyond. In Chapter 3, a method is proposed to minimize the fiber weave effect.

3. In Chapter 4, the impedance control method is proposed for minimizing the slot plane effect when high frequency signals cross the slot gaps. It is a geometry based method to understand the physical degradations in the PCB.
4. Chapter 5 elaborates how better EMC is achieved by using plane layers as an inbuilt capacitor in a multilayer PCB of medical devices.
5. In Chapter 6, the effect of simultaneous switching noise coupling with traces and vias is investigated and a solution is proposed for a high-speed PCB in medical systems. It explains how a test board is built and analyzed and how the measurements are compared with simulation results.
6. The dissertation is concluded in Chapter 7

CHAPTER 2

PCB Related EMI Issues and EMC Designs: A Review

2.0 Introduction

Printed circuit boards (PCBs) are a method of assembling modern electronic circuits. The design of the printed circuit board can be as important as the circuit design to the overall performance of the final system. High speed signals connect by using metallic structure on the PCB which is known as a transmission line. These interconnect carry high speed data as well as low speed data. In medical systems, high speed interfaces are used for transferring the data from one device to another device. PCB effects that are harmful to precision circuit performance include leakage resistances, IR voltage drops in trace foils, vias, and ground planes, the influence of stray capacitance, and dielectric absorption (DA) [24].

A transmission line is a two-port network connecting a generator circuit at the sending end to a load at the receiving end as shown in figure 2.1.

Figure 2.1: Transmission line on PCB.

Electrical signals are transmitted through metal conductors called transmission lines. Transmission lines are connections capable of carrying the signal from transmitter to receiver at high speed.

Transmission lines are connections capable of carrying the signal from transmitter to receiver at high speed. Digital signals on PCB transmit at high speeds.

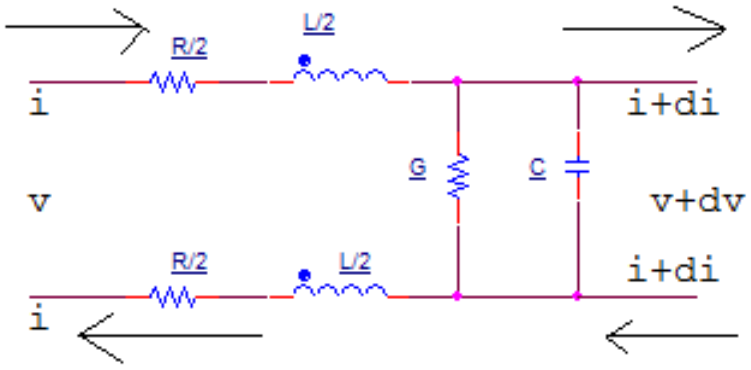


Figure 2.2: Equivalent circuit of transmission line (R, L, G, and C per unit length) draw in orcad.

The relationship between voltage and current on the line may be determined by writing Kirchhoff's voltage law (KVL) [25] around the outer loop in figure 2.2, and by writing Kirchhoff's current law (KCL) at the right-hand node.

Assuming,

R: series resistance per unit length, for both conductors, in Ω/m

L: series inductance per unit length, for both conductors, in H/m

G: shunt conductance per unit length, in S/m

C: shunt capacitance per unit length, in F/m

Apply KVL,

$$-v + \frac{Rdz}{2} i + \frac{Ldz}{2} \frac{\partial i}{\partial t} + v + dv + \frac{Rdz}{2} i + \frac{Ldz}{2} \frac{\partial i}{\partial t} = 0 \quad (2.1)$$

The change in voltage per unit length,

$$\frac{\partial v}{\partial z} = -Ri - L \frac{\partial i}{\partial t} \quad (2.2)$$

In phasor form of equation 2.2

$$\frac{\partial \tilde{V}}{\partial z} = -(R + j\omega L)\tilde{I} \quad (2.3)$$

Apply KCL at the right-hand node of figure 2.2,

$$-i + i + di + Gdz(v + dv) + Cdz\frac{\partial(v + dv)}{\partial t} = 0$$

$$\frac{\partial i}{\partial z} = -Gv - C\frac{\partial v}{\partial t} \quad (2.4)$$

In phasor form of equation 2.4

$$\frac{\widetilde{\partial I}}{\partial z} = -(G + j\omega C)\tilde{V} \quad (2.5)$$

The partial derivative of the voltage phasor equations 2.3 & 2.5 and combine these,

$$\frac{\partial^2 \tilde{V}}{\partial z^2} = (R + j\omega L)(G + j\omega C)\tilde{V} = \gamma^2 \tilde{V} \quad (2.6)$$

where, $\gamma = \sqrt{(R + j\omega L)(G + j\omega C)} = \alpha + j\beta$ and γ, α, and β are the propagation, attenuation, and phase constants, respectively.

The characteristic impedance of transmission line is,

$$Z_0 = \sqrt{\frac{(R+j\omega L)}{(G+j\omega C)}} \quad (2.7)$$

And in traveling wave solutions:

$$V(z) = V^+(z) + V^-(z) = {V_0}^+ e^{-\gamma z} + {V_0}^- e^{+\gamma z} \quad (2.8)$$

$$I(z) = I^+(z) + I^-(z) = {I_0}^+ e^{-\gamma z} + {I_0}^- e^{+\gamma z} \quad (2.9)$$

2.1 Lossy Behavior of the Transmission Line

At higher operating frequencies there is some resistive loss in the conductor itself and this loss is frequency dependent. The main component of a lossy line can be defined using the series resistance of the trace and dielectric loss of the prepreg. A transmission line with characteristic impedance Z_0 is terminated with a load impedance Z_L.

$$V(z) = V^+(z) + V^-(z) = {V_0}^+ e^{-j\beta z} + {V_0}^- e^{+j\beta z} \quad (2.10)$$

$$I(z) = I^+(z) + I^-(z) = {I_0}^+ e^{-j\beta z} + {I_0}^- e^{+j\beta z} = \frac{1}{Z_0}({V_0}^+ e^{-j\beta z} + {V_0}^- e^{+j\beta z}) \quad (2.11)$$

where, $$Z_0 = \frac{{V_0}^+}{{I_0}^+} = -\frac{{V_0}^-}{{I_0}^-} \quad (2.12)$$

2.1.1 Impedance Matching with Device Impedance

One of the important parameters of the transmission line is the characteristic impedance (Z_0). In order to maximize the signal transfer we have to design transmission lines whose characteristic impedance is matched with an impedance of the transmitter and receiver. If the lines are mismatched with the terminal impedance then the signal gets reflected. Multiple reflections can occur within the system, thus reducing the performance of the system. At high data rates this has detrimental effects on signals and causes effects such as like overshoot, undershoot, ringing and stair step waveform, all of which produce error in the signaling. Line impedance is determined by width and thickness of the conductor, height of the PCB core on either side of the trace, configuration of the lines and dielectric constant of the core.

2.2 Types of Transmission Lines

2.2.1 Microstrip Transmission Line

Microstrip lines are routed on top and bottom layer of the PCB where one side is a ground plane, and the other side is air as a dielectric medium. Microstrip lines are also used in high-speed digital PCB designs, where signals need to be routed from one part of the assembly to another with minimal distortion, and avoiding high crosstalk and radiation.

A cross-sectional view of a two-layer PCB illustrates this microstrip geometry as shown in figure 2.3 and figure 2.4 shows the 3D view of the partially session of microstip line routed on top layer.

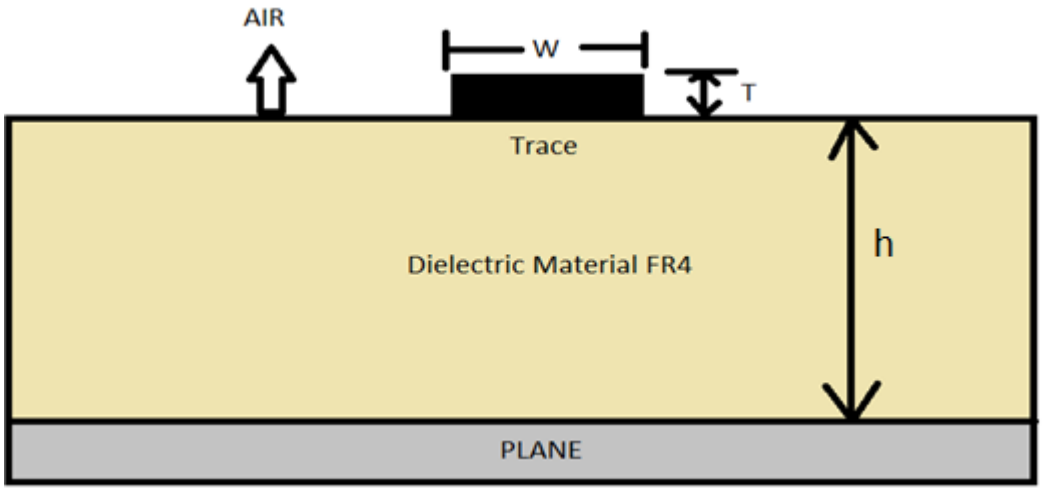


Figure: 2.3: A cross-sectional view of microstrip geometry.

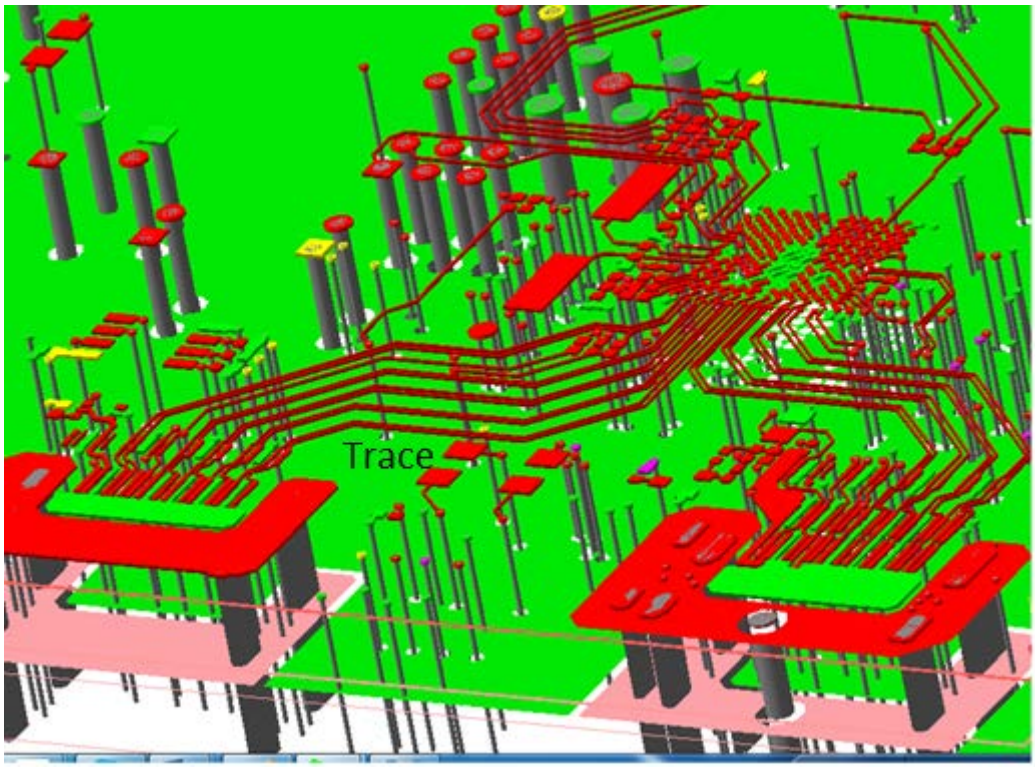


Figure: 2.4: 3D view of microstrip geometry for HDMI interface board using Allegro Tool.

The characteristic impedance of the transmission line is inversely proportional to the capacitance per unit length between the conductors. As per IPC, the most popular approximation of the microstrip equation for characteristic impedance and propagation delay are;

$$Z_0 = \frac{87}{\sqrt{\varepsilon_r + 1.41}} \ln \frac{5.98h}{0.8w + r} \qquad (2.13)$$

where, h in (mil) is dielectric thickness below the signal trace to the plane, w is line width in (mil), r is metal thickness in (mil), and ε_r is dielectric constant.

The propagation delay of the microstrip line can also be calculated, as per below equation. This is the one-way transit time for a microstrip signal trace.

$$T_P = 85\sqrt{0.475\ \varepsilon_r + 0.67} \qquad (2.14)$$

2.2.2 Stripline Transmission Line

A stripline circuit uses a flat strip of metal which is sandwiched between two parallel ground planes. The insulating material of the substrate forms a dielectric as shown in figure 2.5. The width of the strip, the thickness of the substrate and the relative permittivity of the substrate determine the characteristic impedance of the strip which is a transmission line.

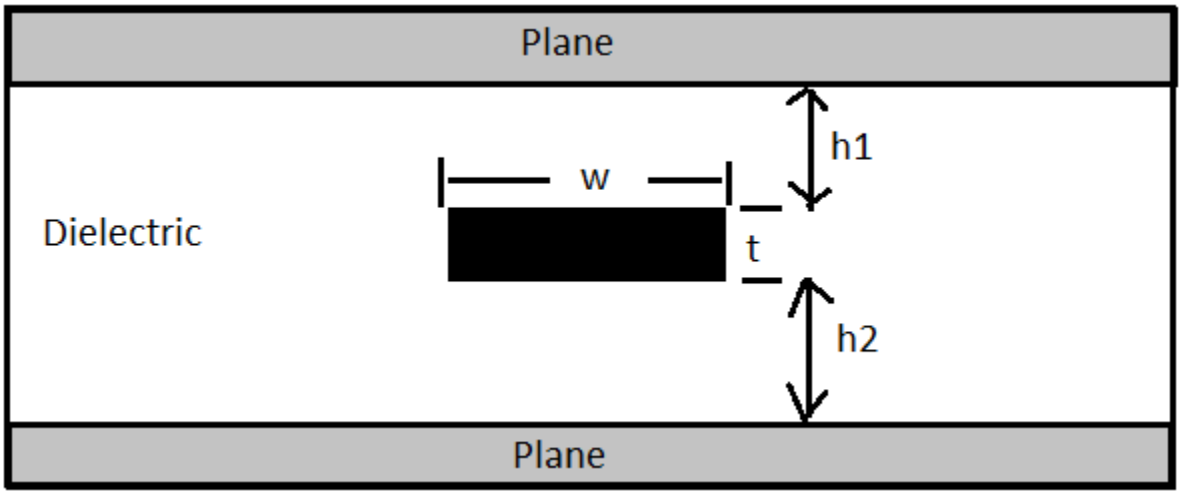


Figure 2.5: The cross-sectional view of stripline.

As shown in figure2.5, the characteristic impedance of this arrangement is dependent upon geometry and ε_r of the PCB dielectric. An expression for Z_0 of the stripline transmission line is:

$$Z_0 = \frac{60}{\sqrt{\varepsilon_r}} \ln \frac{1.9(h1+h2)}{0.8w+t} \qquad (2.15)$$

The propagation delay of the symmetric stripline is,

$$T_P = 85\sqrt{\varepsilon_r} \qquad (2.16)$$

2.2.3 Single Ended and Differential Transmission Lines

2.2.4 Single Ended Transmission Lines

Single-ended transmission line is probably the most common way to connect devices. In this device driver and receiver are connected by a single conductor as shown in figure 2.6. For single-ended transmission lines, a reference plane (ground planes) provides the current return paths.

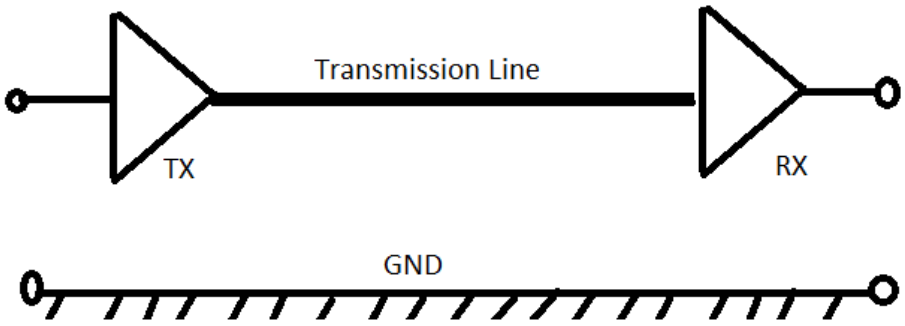


Figure 2.6: Single ended transmission line.

The signal and return lines differ in geometry the cross-section of the signal conductor is different from that of the return ground plane conductor. The characteristic impedance of the single-ended transmission line is determined by width and thickness of the conductor, height of the dielectric and dielectric constant of the system. The number of conductors used in a complex design will be less when compared to a system that uses differential pairs, however the receiver receives noise signal with respect to ground planes.

2.2.5 Differential Transmission Lines

Differential transmission lines are driven as a pair with one line transmitting the signal waveform of the opposite polarity (180^{o}) to another as shown in figure 2.7.

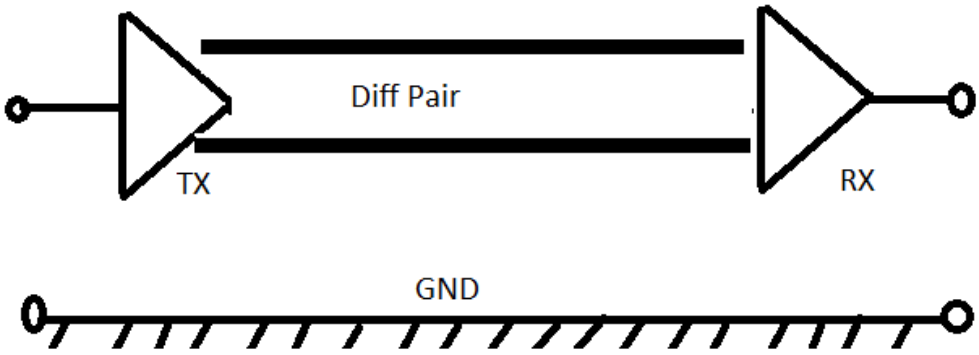


Figure 2.7: Differential transmission lines.

The characteristic impedance of the differential pair is determined by width, thickness and spacing of the conductor, height of the dielectric medium and dielectric constant of the medium. The number of conductors more when compared with single ended, but common mode noise,

generated in the two lines will tend to cancel out and EMI lower in the differential lines therefore problems with noise reduced [26].

2.2.6 Advantages of Differential over Single Ended Transmission Lines

Differential lines reduce electronic crosstalk and electromagnetic interference. Owing to the ability of noise rejection, signal swing can less in differential signaling when compared to single ended, which can result in lower power systems at higher data rates.

2.3 Layer Stack up

Layer stackup play a very important role to design a multilayer impedance control board for any system. On medical application board both analog and digital circuit exist on the board. The analog circuit is more sensitive to noise compared to digital circuit. In layer stackup each layer conductor layer is separated by a dielectric material as shown in figure 2.8.

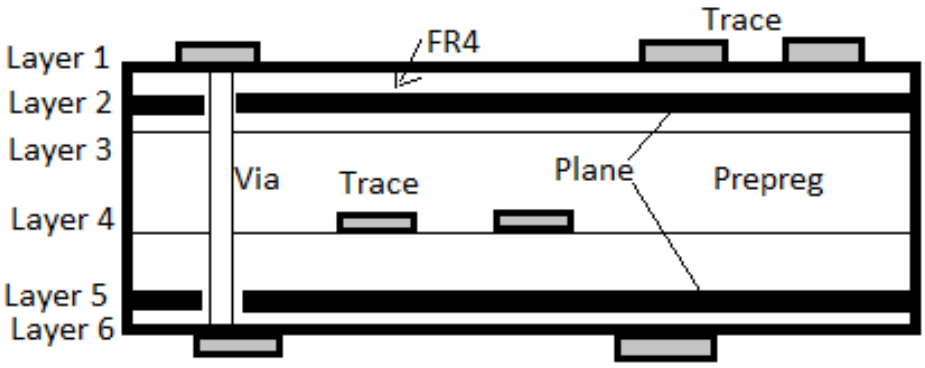


Figure 2.8: Multilayer board layer stackup.

1. Copper foil is a thin sheet of copper that bonds to the prepreg layer. Traces are formed by etching the copper foil. The usual thickness of copper layer is 16.25µm, 32.5µm and 65µm, depending on the impedance, current carrying capacity and thermal effect of the trace. The trace width is a design parameter, depending on the required impedance of the trace.

2. Core: The core material is a rigid sheet usually made of cured fiberglass resin material that provides isolation between layers. Most commonly used core material is Fr4 epoxy glass. The dielectric strength, coefficient of thermal expansion and the cost of the core play an important role in selecting the core of PCB design.

3. Prepreg: The prepreg is made of a material similar to core material but is uncured. It behaves as an adhesive to bond the copper layers. When heated and pressed, the prepreg will cure holding the copper layers firmly, hence it is used to stick the core layers together.
4. Via: - is a hole in the PCB which is for connecting different layers of PCB and is metal coated from inside.

2.4 Resistive and Dielectric Losses

Loss refers to the phenomenon in which PCB-trace resistance and the heating of dielectric materials cause signals to reduce the amplitude and suffer shape distortion, particularly at higher frequencies. Accurately analyzing loss is complex because lossy effects are frequency dependent and digital signals contain a wide range of frequencies.

2.4.1 Dielectric Loss

One of the techniques to control the signal integrity problem on the PCB by using low dielectric loss materials. The main effects contributing to transmission line loss are skin effect and dielectric loss. Generally PCBs are made of FR4 or a similar dielectric that is a combination of a glass and resin structure. Since these structures are not perfect insulators, it results in some amount of attenuation and dispersion of the signal known as dielectric loss.
This imperfection of the dielectric material is measured by its loss tangent. The amount of loss from the dielectric is proportional to the frequency of the signal on the PCB. FR4 is the most commonly used material in PCB design; it has a relatively high loss tangent as compared to other available materials as shown in table 2.1. The higher the signal frequency, greater the loss. These losses combine to change the shape of a signal launched at a driver IC as it travels down a trace. Higher-frequency components of a signal are attenuated as compare to frequency components which tend a signal’s shape and drop its amplitude. Shape changes also result from the fact that different frequencies propagate at different speeds. Dielectric loss grows roughly linearly with frequency effect grows only as the square root of frequency.

Table 2.1: Parameters of various dielectric materials [27]: A comparison

Material	Dielectric Constant	Tangent Loss	Cost
FR4	4.0-4.5	0.02	⇩
GETEK	3.6	0.013	
BT	4.1	0.013	
POLYMIDE	4.3	0.014	
NELCON	3.3	0.003	
ROGER	3.5	0.0018	

Dielectric materials, such as RogersRF35 and Nelcon offer much lower loss tangents, but they are more expensive than FR4. Dielectric loss arises from the fact that although the dielectric between the conductor of a transmission line and its reference ground behaves like a perfect insulator at DC. It absorbs some amount of energy at higher frequencies. This can be modelled as a distributed, frequency dependent conductance between the conductor and ground. Dielectric loss generally depends only on dielectric material properties and not on geometry. Linear scaling of the cross-section of a transmission line structure will keep the characteristic impedance constant but will also keep the conductance associated with dielectric loss constant.

As shown in figure 2.9 a 50 ohm buried microstrip line which is simulated in Hyper lynx tool and figure 2.10 shows the simulated result of dielectric loss due to FR402.

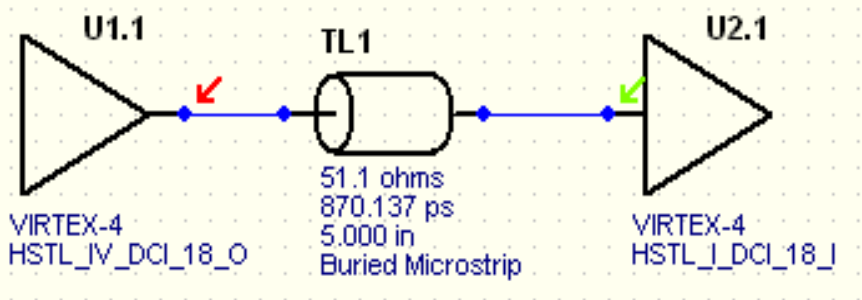


Figure 2.9: 50 ohm buried micro strip line model.

Case: 1 FR402

Trace length - *L* = 5 inches (0.17 m)

Conductor thickness -*T* = 1.5 mils

Width - *W* = 5 mils

Dielectric Height - *h1* = 0.04 mils

Dielectric Height - *h2* = 4.40 mils

Dielectric constant - *Er* = 4.3

Loss tangent - *Lt* = 0.02

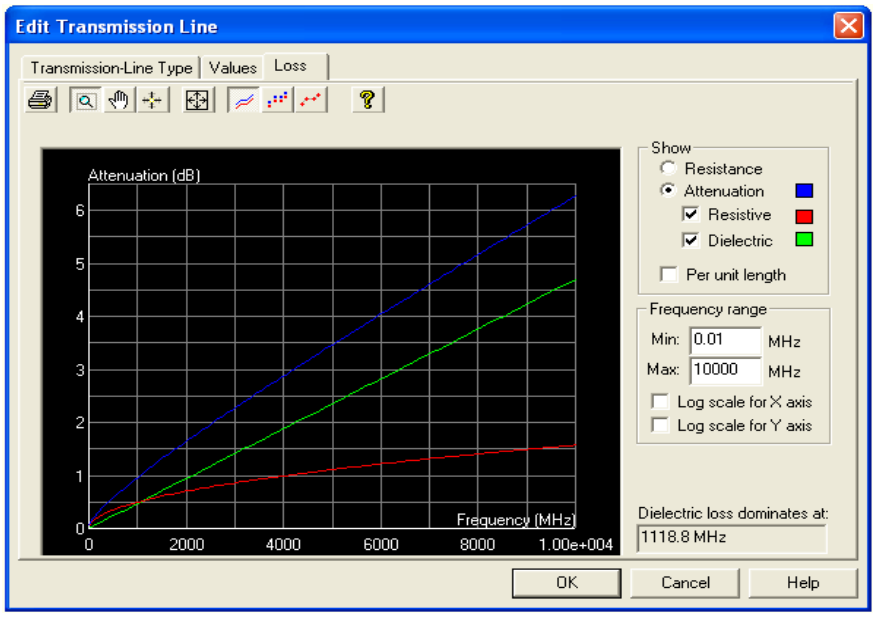


Figure 2.10: Dielectric loss at 3GHz for FR4 ~1.5dB.

Case: 2 RogerRF35

Trace length - *L* = 5 inches (0.17m)

Conductor thickness -*T* = 1.5 mils

Width - *W* = 5 mils

Dielectric Height - *h1* = 0.04 mils

Dielectric Height - *h2* = 4.40 mils

Dielectric constant - *Er* = 3.5

Loss tangent - *Lt* = 0.0018

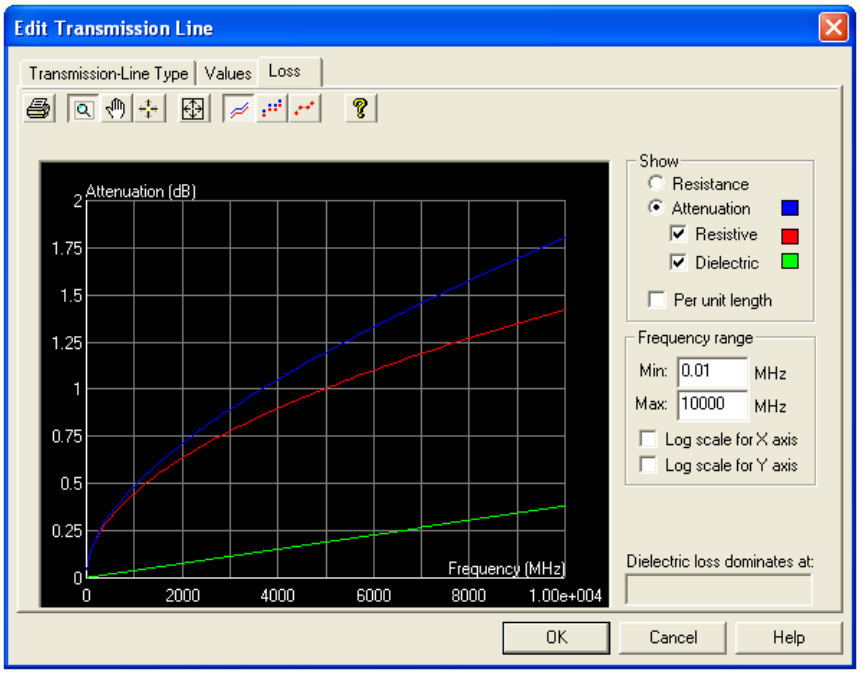


Figure 2.11: Dielectric loss at 3 GHz for RogerFR ~.13dB.

In figure 2.11 the simulated result of the dielectric loss in Roger Fr material is significantly improved compared to Fr403 material. The Roger material is very costly which increased the overall cost of the product. The hybrid layer stackup is the solution to maintain the cost of the product and take the benefit of the low dielectric loss Roger material.

2.4.2 Resistive Loss

At frequency up to megahertz, the dc current utilizes the whole cross section of a conductor. Skin effect results from the fact that current is not evenly distributed across a conductor at higher frequencies. The higher the frequency of the signal more current flow on the surface and not in the center of a conductor. Effectively with increasing frequency this reduces the usable area of the conductor and increases its resistance.

Reduce skin effect by using wider traces on the PCB. Widening traces increases the effective cross sectional area of the conductor and as a result reduce the resistive loss. If the trace width is increased to overcome resistive loss, but all other parameters have stayed the same, it results in a reduction in the transmission line impedance. This happened because of the increase in capacitance in the transmission line. From the lossy transmission line equations 2.11, shows that increased the capacitance would reduce effective impedance of a transmission line.

$$Z_0 = \sqrt{\frac{(R+j\omega L)}{(G+j\omega C)}} \qquad (2.17)$$

Case:1-A

Width - W = 5 mils

Trace length - L = 8 inches (0.2032m)

Trace impedance = 49.9 ohms

Conductor thickness -T = 1.5 mils

Dielectric Height - $h1$ = 0.04 mils

Dielectric Height - $h2$ = 4.20 mils

Dielectric constant - Er = 4.3

Loss tangent - Lt = 0.02

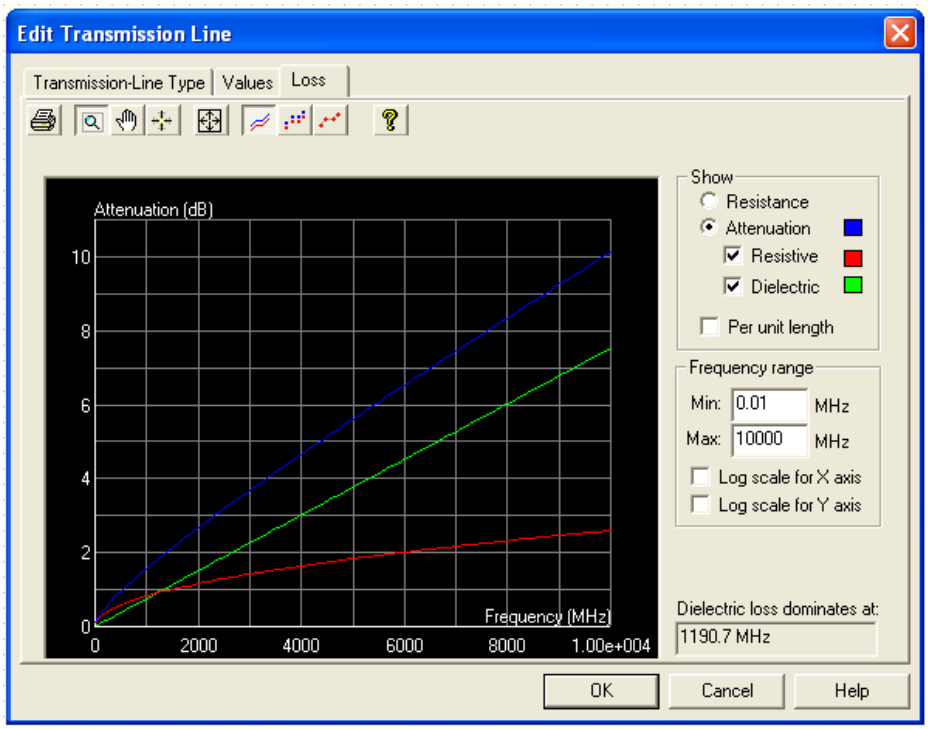


Figure 2.12: Shows Dielectric loss at 4 GHz is 1.8dB.

Case: 1-B

Width - *W* = 15 mils

Trace length - *L* = 8 inches (0.2032m)

Trace impedance = 50.3 ohms

Conductor thickness -*T* = 1.5 mils

Dielectric Height - *h1* = 0.04 mils

Dielectric Height - *h2* = 9 mils

Dielectric constant - *Er* = 4.3

Loss tangent - *Lt* = 0.02

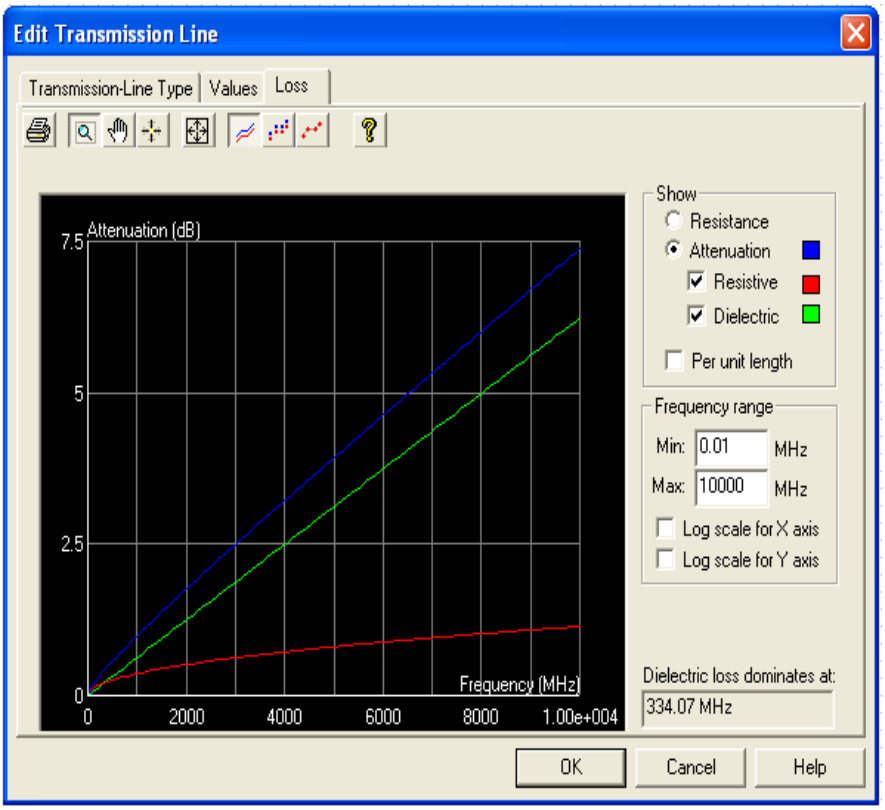


Figure 2.13: Shows Dielectric loss at 4 GHz is 1.2dB.

In figure 2.12 and figure 2.13 shown the simulation result of resistive loss when different trace width is used. The resistive loss in wider trace width is less compare to thin trace on the PCB. If the dielectric and resistive losses in the transmission line are constant, its means every frequency

must be attenuated for the same amount. The amplitude of the signal might be reduced as the rise time of the signal would be exactly the same for incoming and outgoing signals.
The skin depth is analytically analysis by using equation 2.6.

$$\delta = \sqrt{\frac{1}{\pi\mu\sigma f}} \qquad (2.18)$$

where, conductor's σ (in S/m), conductivity and the frequency 'f' (in Hz) of the signal

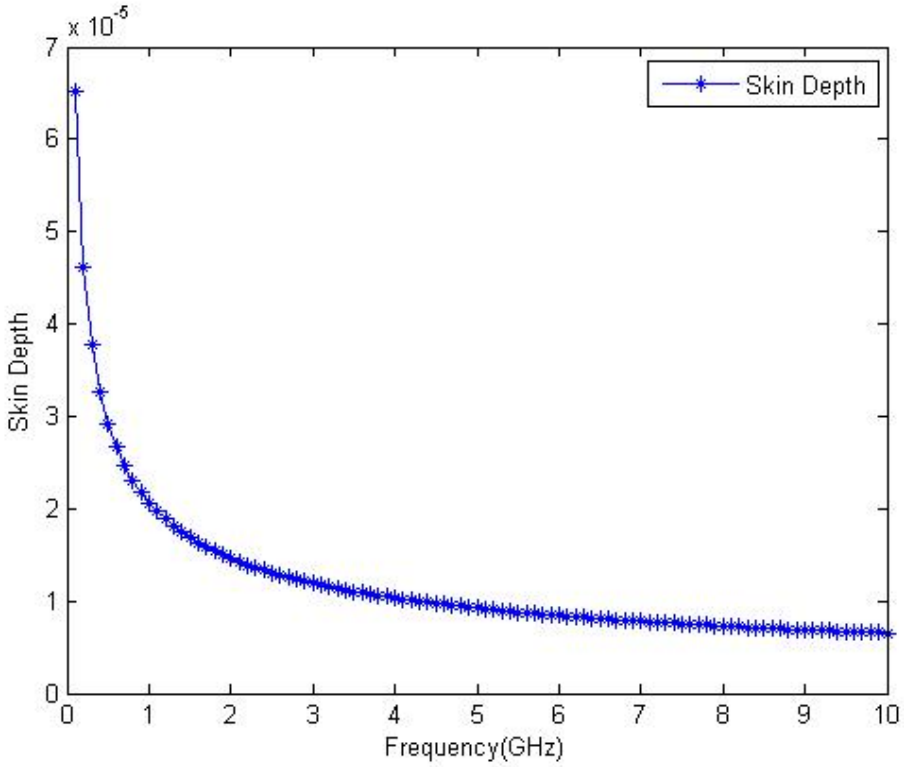


Figure 2.14: Skin depth on microstrip line.

The skin effect also causes frequency dependence of the strip line inductance; inductance of the trace is higher at low frequencies and falls noticeably at the transition frequency where skin depth becomes comparable with conductor dimensions as shown in figure 2.14. With the increase of operating frequency, although the flux density between the microstrip trace and reference conductor remains constant, the magnetic flux of the microstrip trace keeps reducing, hence the inductance at higher frequency becomes low. These effects produce altogether different copper characteristic impedance than originally designed for.

2.5 Signal Integrity

Signal integrity (SI) issues in medical environments are gaining a lot of importance. Most of the Signal Integrity (SI) problems are EM problems in nature, such as reflection, crosstalk and ground bounce [28]. The medical instruments like CT scan and others diagnostic instrument requirement is of very high signal accuracy. Instrument accuracy may lead to misinterpretation of diseases. SI in medical environments arises due to the special characteristic of medical devices. Failure of medical devices may lead to injury. One of the technique to control the signal integrity problem on the PCB by using low dielectric loss materials. The main effects contributing to transmission line loss are skin effect and dielectric loss. Newer ICs, today have edge rates in the sub-nanosecond range; the fastest of which are multi-gigabit transceivers that have edge rates of less than 50ps. As driver ICs switch faster and faster, more and more boards suffer from signal degradations like overshoot and undershoot, ringing, crosstalk, and excessive settling delays [29]. When these degradations become serious enough, the logic on a board may begin to fail. With such fast edge rates, it is important to tightly control trace impedance to meet signal integrity requirements and have consistent reference planes to meet our electromagnetic compatibility requirements [30-31].

Signal Integrity is a measure of the signal quality at the receiver. The amplitude of the wave shape at the receiver pin is same as at the driver pin. In reality, there is always some distortion of signals on a PCB [32]. A signal waveform distortion, severe enough to cause a timing violation is considered a signal integrity violation. Ring back, overshoot, undershoot and non-monotonic edges are some of the metrics used to measure signal quality in digital PCB design. The two primary factors that affect signal integrity of high speed signals on a PCB are impedance discontinuities and losses (resistive and dielectric). Different signaling technologies require different trace impedances. Generally recommended traces impedances for high speed signals are 50 or 60 ohms for single ended tracks and 70 or 100 ohms for differential tracks. The impedance of a trace on a PCB is controlled by the trace width and dielectric thickness. To attain the desired trace impedances on the PCB, need to determine the required trace and stack up parameters.

2.5.1 Causes of Degradation in Signal Integrity on PCB

2.5.2 Impedance mismatched and Reflections: Impedance mismatches produce several detrimental effects in digital circuits.

- Digital signals are reflected between the input on the receiving device and the output on the transmitting device. The reflected signals are bounced back and forward between the two ends of the line until eventually they are absorbed by resistive losses.
- The reflected signals introduce ringing on the signal being sent across the trace. Ringing impacts the voltage level and timing of the signal and can severely corrupt the trace.
- A mismatched signal path can cause the signal to be radiated into the environment.

2.5.3 Split Planes

When a signal crosses the split plane, the energy on the return path is disrupted at split location, generating scattered waves in all directions and, particularly, back to the source. Figure 2.15 shows the current flow when a signal trace is routed over a ground plane slot. The return current is forced around the slot, thus creating a large loop area.

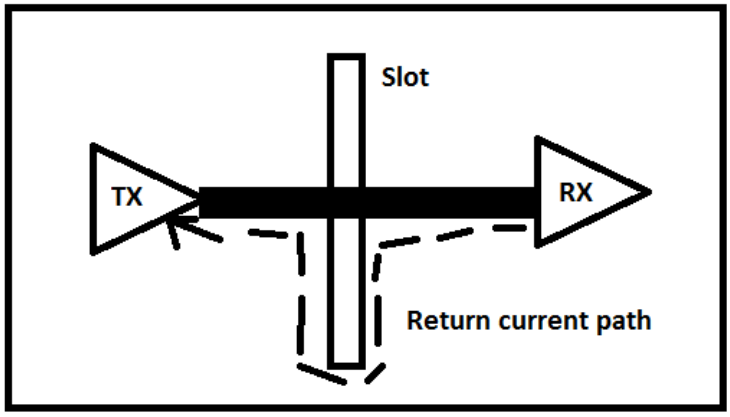


Figure 2.15: Split plane effect.

The loops act as antennas. Generally, a greater loop area increases the chances of the loop radiating and conducting. The high-speed signals over slots of nearby reference planes can cause undesirable effects such as impedance discontinuities, EMI noise, or crosstalk [33].

2.5.4 Crosstalk

Crosstalk is the coupling of energy from one line to another via Mutual capacitance (electric field) and Mutual inductance (magnetic field).In digital designs inductive crosstalk usually dominates capacitive crosstalk as shown in figure 2.16 [34] . Inductive coupling results from return currents which generate magnetic fields in other traces leading to crosstalk.

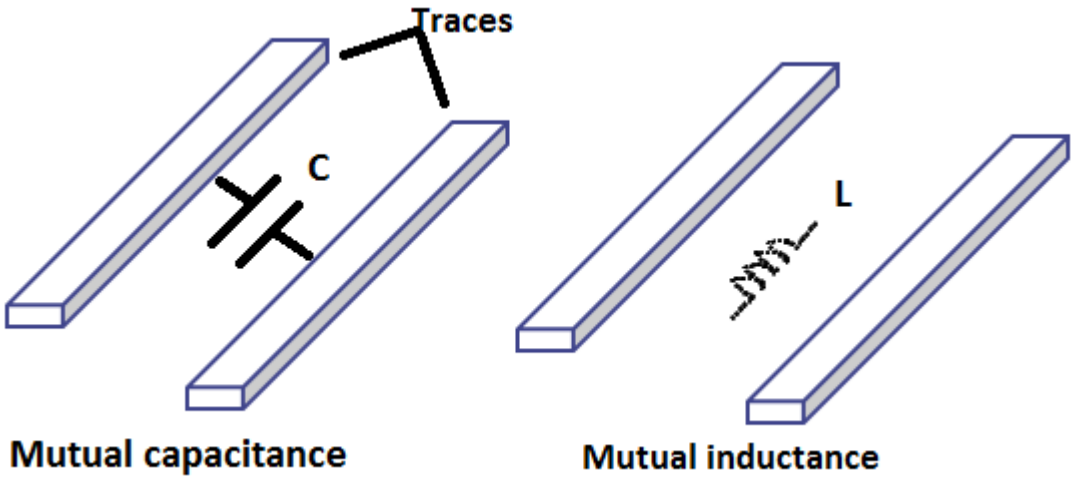


Figure 2.16: Crosstalk via mutual capacitance and mutual inductance.

The circuit element that represents this transfer of energy are the following familiar equations 2.18 & 2.19:

$$V_{Lm} = L_m \frac{dI}{dt} \qquad (2.19)$$

$$I_{Cm} = C_m \frac{dV}{dt} \qquad (2.20)$$

The mutual inductance (L_m) induces current (I_{Cm})on the victim line opposite of the driving current and the mutual capacitance (C_m) pass current through the mutual capacitance that flows in both directions on the victim line. Crosstalk on the PCB can be minimized by using effective layer stackup [35].

2.5.5 Electromagnetic Interference (EMI)

EMI is the disruption of operation of an electronic device when it is in the vicinity of an electromagnetic field (EM) in the radio frequency (RF) spectrum that is caused by another electronic device. Radiation of energy from one electronic device to another capable of disrupting the proper functioning of the latter is Electromagnetic Interference. EMI can arise from many sources, being either man made or natural. It can also have a variety of characteristics dependent upon its source and the nature of the mechanism giving rise to the interference. EMI is an unwanted signal at the signal receiver, and in general methods are sought to reduce the level of the interference.

EMI can also lead to serious consequences, such as, malfunctioning of medical equipment while monitoring condition of patients [36].

There are three essential elements of an EMI:

1. EMI sources: Any device or apparatus that transmits, distributes, processes, or otherwise utilizes any form of electrical energy can be a source of EMI.

2. EMI receptors: The receptor refers to the generic class of devices, equipment and/ or system that, when exposed to EMI, either malfunction or degrade performance. These EMI receptors may be natural or man-made.

3. Coupling paths: There are four type of coupling paths may exist between an emitter and a receptor:

a. Common Impedance Coupling
b. Capacitive Coupling
c. Inductive Coupling
d. Radiation Coupling

2.5.6 Simultaneous Switching Noise (SSN)

Switch power supply noise: Due to parasitic of the power/ground delivery system during drivers' switching output (SSO). SSN occurs at both the chip level and the board level. At the chip level, the power supply is not perfect. Any sudden demand for current must be supplied by the board-level power though the inductive chip package and lead frame [37]. On the board level, sudden current demands must be supplied through inductive connectors. The coupled SSN decreases noise and timing margins of digital and analog circuits, resulting in reduction of achievable jitter performance, bit error ratio (BER), and system reliability.

2.5.7 Electromagnetic Compatibility (EMC)

Electromagnetic Compatibility (EMC) essentially ensures proper working of an electrical system when it is placed in an electromagnetic environment shared by other electrical systems. This means that conducted or radiated emissions from an electrical system are kept within specified limits so that they may not degrade the performance of any other electrical system placed in the same environment [38].

There are three elements in the EMC model to analyze and understand an EMC problem:

• A **Noise source,** a source that generates an electromagnetic perturbation**,**

• A **victim,** an electronic device that receives a perturbation which causes dysfunctionalities,

• A **coupling path**, a medium that transmits energy from the noise source to the victim.

2.6 Target Impedance of Power Distribution Network (PDN)

Digital components are broadband circuits whose switching circuits typically have energy concentrated in multiple discrete frequencies, which tend to be harmonics of the various clock frequencies that are employed. On the other hand, the transient behavior of the system depends on a large number of variables, including some high level considerations such as the program being executed.

The PDN has a capacitive behavior at low frequencies and shows inductive behavior as we move towards the higher frequency range. However, this inductive trend is punctuated with a number of discrete resonances and anti-resonances. As far as a driver on-chip is concerned, the PDN must appear to be an ideal AC ground between its power and ground terminals. Therefore, the inductance of the PDN must be reduced to enable easy flow of charge to the required active circuits to mitigate the noise. The target impedance of the PDN is decided based on the core voltage (*Vdd*) and average current (*Id*) drawn by the processor as mention in equation 2.20 [39]. In practice, the maximum allowed ripple is assumed be 5% of the power supply voltage (*Vdd*).

$$Z_{tar} = \frac{Vdd\ X\ 5\ \%}{Id\ X\ 50\ \%} \qquad (2.21)$$

The current term in the denominator is 1/2 the switching current in a clock cycle, which is assumed to be the current in each clock edge. Decreasing supply voltages coupled with increasing power requirements tends to place stringent requirements on the target impedance of the digital part.

2.7 S Parameters

S-parameters or scattering parameters describe the electrical behavior of electrical networks when undergoing various steady state changes by electrical signals. Many electrical properties of components like resistance, inductance, and capacitance can be captured using S-parameters such as gain, return loss, insertion loss, and voltage standing wave ratio and reflection coefficient. S-parameters are generally expressed as complex numbers either in rectangular form

or polar form. An electrical network may have N number of ports. Ports are the points where the signal enters or exits the system.

Advantage of S parameter

- Analysis of all the inputs and outputs at the same time is not possible.
- S parameters are to study relative effect of one port on others.
- It is to understand the effect input of a one port on the output of another port.
- By creating an S parameter matrix (Scattering matrix), it becomes easy to solve multiport networks.
- Conversion is easy to other parameters.

2.7.1 2-Port Network

With $V1+$ as input, $V1-$ as reflected wave reaching input port, $V2+$ as the reflected wave from the load and $V2-$ as the wave reflected from source as shown in figure 2.17.

Figure 2.17: 2 port network of transmission line.

$$V_1^- = S_{11}V_1^+ + S_{12}V_2^+ \qquad (2.22)$$

$$V_2^- = S_{21}V_1^+ + S_{22}V_2^+ \qquad (2.23)$$

- Note that (V_2^+) can be easily made 0, using characteristics imp as load, so that there is no reflection at load.

- It can be seen that if the reflected wave form load (V_2^+) becomes 0, S_{11} can be easily calculated as (V_1^- / V_1^+).
- Note that S_{11} is also known as reflection coefficient from source Gamma *S* and return loss from input.
- When (V_2^+) is 0, S_{21} can be calculated as (V_2^- / V_1^+).
- Note that S_{21} is also known as forward transfer gain or insertion loss of transmitted wave V_1^+.
- Similarly, S_{21} and S_{22} are called reverse transfer loss and reverse return loss respectively.
- To calculate the loss in dB just take 20 Log at the base 10 of the transfer parameters.
- In the case of *N* ports, to calculate Sij just terminate the ports with their respective characteristic impedance (mostly same).
- Note that Z_0 is not the same as input impedance Z_{in}, which is $Z_0 (V_1^+ + V_1^-) / (V_1^+ - V_1)$.
- Z_{in} can also be written as $Z_0 (S_{11} + 1) / (1 - S_{11})$.

2.7.2 Insertion Loss and Return Loss

Insertion loss

Insertion loss is the extra loss produced by the network present between the ports and is expressed in decibels. Insertion loss (*IL*) is a measurement of forward transmission coefficient.

$$IL = -20 * \log (S_{21}) \text{ dB} \qquad (2.24)$$

For maximum signal transfer forward transmission coefficient should be high and insertion loss should be close to 0 dB

Return loss

If the system impedance does not match with terminal impedance then the signal gets reflected at the input terminal and output terminal. Return loss (*RL*) is expressed in terms of decibels and is a measure of input port reflection coefficient.

$$RL = -20 * \log (S_{11}) \text{ dB (15)} \qquad (2.25)$$

For maximum transfer of signal reflections at the input port should be low and return loss should be below -10 dB.

2.8 Summary

Signal integrity is among the most important issues for high-speed digital design. This chapter has presented the fundamentals of signal integrity for digital hardware, including:

• Physical isolation of sensitive components from noisy components;

• Impedance control, reflections and terminations on signal traces;

• The use of solid planes for power and ground;

• Routing of signals to avoid right angle corners and stub traces;

• Routing of differential pairs to achieve length matching;

• Crosstalk in high-speed designs; and

• Power supply de-coupling.

CHAPTER 3

EFFECT OF FIBER IN THE PCB ON ROUTED HIGH SPEED SIGNALS: 3DFEM EVALUATION

3.0 Introduction

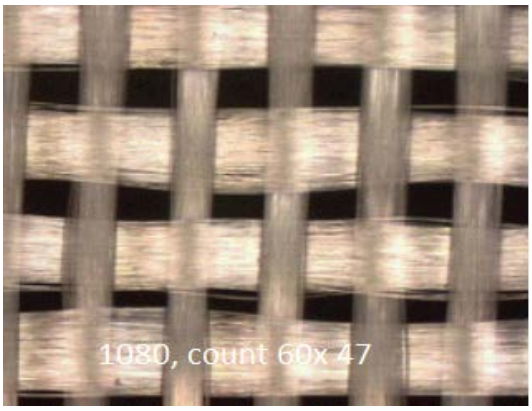
Differential pairs have high tolerance to noise leading to a widespread use in bus and interconnect designs of modern high-speed medical systems. If the two conductors in a differential pair are not perfectly balanced, there will be a difference in the phase velocities of the signals in each conductor resulting in intra-pair skew and modal conversion at the receiver. Laminate materials often adversely affect the differential pair conductor balance, playing a major role in PCB performance. Laminates are constructed by reinforcing a material such as woven glass, ceramic or glass microfibers on a resin system [40]. A laminate is referred to in terms of the reinforcing material used. The ratio of the resin to the reinforcing material affects the dielectric properties of a laminate.

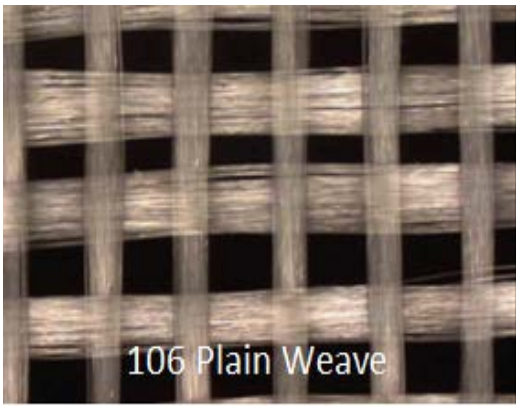
PCB substrates or laminates, which are manufactured by impregnating and strengthening a woven fiber glass fabric with an epoxy resin, are not homogeneous materials but are inhomogeneous and anisotropic in nature [41]. Depending on the position, there are local variations of their dielectric characteristics. Typically, the effective permittivity of the glass bundles is ~ 5.0, while that for resin is ~ 3.3. As bit rates are climbing, often going up to 5 GB/s or even beyond, the fiber weave effect is becoming a major challenge in PCBs. The difference in the properties of the glass bundles and resin creates a non-homogenous medium for the signals in the fiberglass weave pattern, causing the signals to propagate at different speeds within differential pair traces. The difference in speed leads to timing skew and mode conversion at the receiver, resulting in reduced bit-error-rate (BER) performance and increased EMI radiation [42]. The relative dielectric constant (Dk) surrounding a trace, ultimately determines the propagation delay of signals in the trace. This research work deals with the issue and presents a novel approach to practically establish worst case min/max values for dielectric constant and use these values to model the fiber weave effect using Sigrity 3DFEM modeling software. In context

of the extensive use of HDMI interface in modern medical systems, a HDMI base board case study is used to practically demonstrate the model and to explore the design space.

3.1 Fiber Weave Material Background

Most PCB substrates are made of woven fiberglass fabrics saturated in epoxy resin to enhance mechanical and fire-resistant properties and to be cost-effective; however, rendering the substrates electrically inhomogeneous. Homogenized dielectric constants are effective for modeling transmission lines on these substrates operating in single-ended configuration, using typical microstrip and stripline models [43]. A microscopic top view of different type of weave patterns is shown in figure 3.1 which are very commonly used in PCB fabrication. As the figure 3.1 picture shows, the fiber glass (1080) bundles (warp and fill) leave gaps which are filled with resin as part of the lamination process to bind and strengthen the fiberglass fabrics. The different electrical characteristics of the resin and the glass bundles lead to the fiber weave effects. The 106 weave pattern has yarn count of 56 x 56 threads/inch and yarn pitch of 17.9 x 17.9 mils, which yield roughly 0.2 mm fiber bundle width and 0.2 mm bundle distance. The weave effect, because of uncertainty of the pattern around differential pairs, can lead to data transmission failures because of the unpredictability of the intra-pair skew at high data rates where links are sensitive to skews.





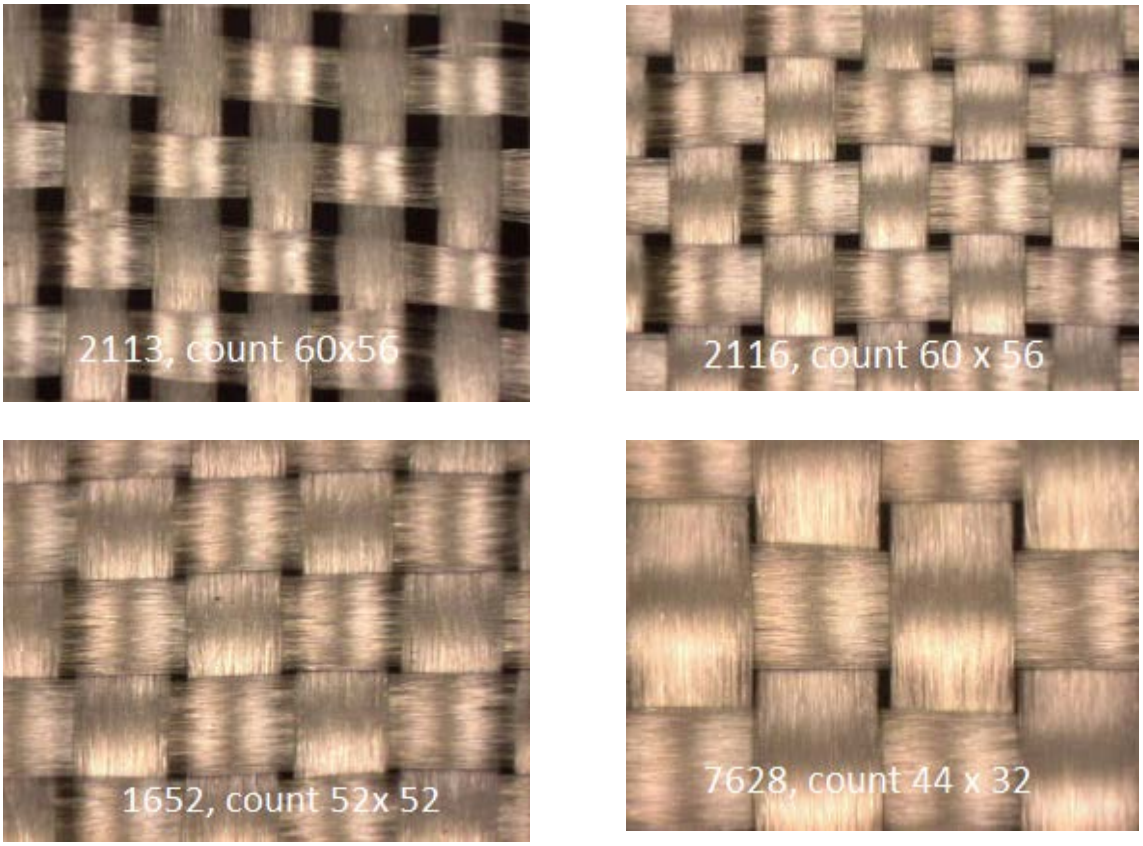


Figure 3.1: Picture of different type of fiberglass fabrics which are very commonly used in PCB fabrication.

A higher resin content means a lower Dk, a material's relative permittivity (e_r) also known as dielectric constant (Dk). Therefore, to determine the maximum delta Dk variation to model the fiber weave effect, we can consider the loose weave of 106 with one of the high resin content and the tight weave of 7628 with one of the lowest. The glass and epoxy have relative permittivity's of ~ 5 and ~ 3.5, respectively, presenting a non-homogeneous medium for signal propagation. The PCB manufacturers control the resin-to fiberglass ratio to adjust the desired "bulk" permittivity. Traces running parallel to the board edge are especially susceptible to this non-homogeneity [44].

Higher the Dk, slower the signal propagates along the transmission line. By knowing the Dk, propagation delay can be determined using equation 3.1. Since the fiberglass yarn has a higher Dk than resin, maximum intra-pair timing skew will occur for the section shown in figure 3.2.

$$t_{pd} = \frac{\sqrt{\varepsilon r}}{c} \qquad (3.1)$$

where t_{pd} is propagation delay (in seconds/inch), e_r is relative permittivity and c is speed of light (2.998 x 10^8 m/s) and speed of signal is 1.18 x10^{10} in/s. Modern serial link interfaces use differential signaling on a pair of transmission lines of equal length for interconnect between two points [45]. Any timing skew between the positive (D+) and negative (D-) data will convert some of the differential signal into a common signal component. Ultimately, this results in eye closure at the receiver.

3.2 Modeling Fiber Weave Effects

PCB is used in practical applications of high speed communication channel in bio-medical application, such as HDMI interface, to investigate fiber weave effect. The construction corresponds to an offset stripline as shown in figure 3.2.

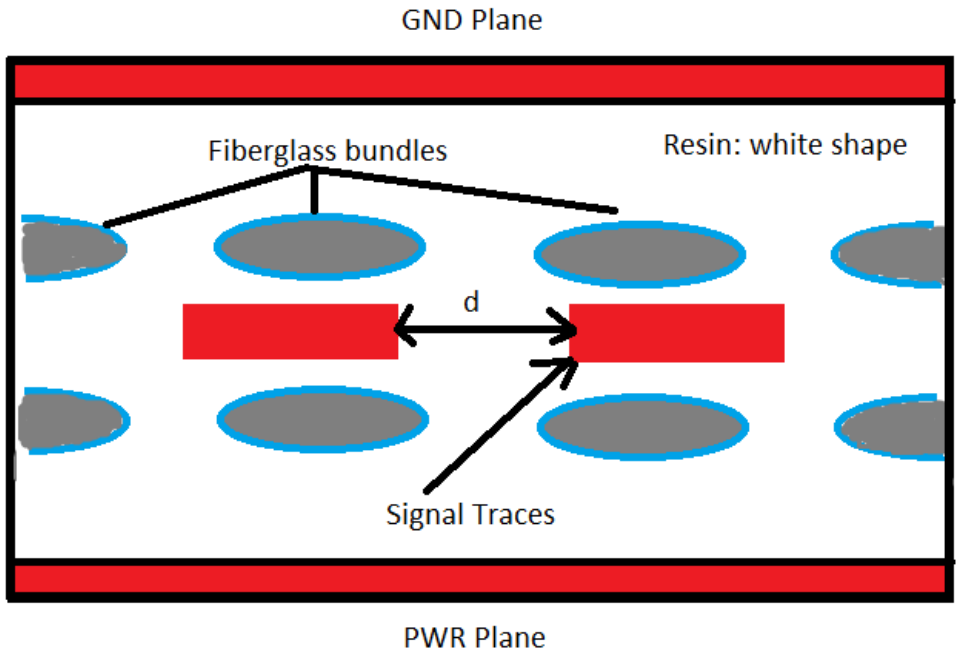


Figure 3.2: Modeling of off-set stripline.

In this model, it is assumed that the fiber weave effect is dominant between the high speed traces and the closest reference plane. As a corollary, the fiber weave effects originating from the laminates underneath the traces are neglected [46]. There are several reasons which justify these assumptions. First, significant fiber weave effects can be expected in the upper side of signal

traces because due to the close proximity to the upper return plane, the electric and magnetic fields will be stronger on the upper side of the signal traces, leading to a strong interaction between the fields and fiberglass. Secondly, the upper section of the PCB is typically composed of a single layer of laminate, thereby enhancing fiber weave effects. On the other hand, the lower side of the traces exhibits a homogenous behavior because it is typically comprised of more than one layer of laminate, making it unlikely that the fiberglass bundles from the different laminates will be aligned. Thus, the lower side can be treated as a homogeneous material characterized by "bulk" electrical properties in the model under consideration.

An increase in data rates can cause an increase in deterministic jitter at low as well as tens of Gbps. First, any asymmetry (imbalance) in differential traces because of the fiber resin dielectric inhomogeneity in differential interconnect cross-section can cause either skew in un-coupled pairs or differential to common mode transformation in coupled pairs leading can to additional losses and change in differential impedance, and an increase of deterministic jitter even at lower Gbps data rates [32]. On the other hand an increase in deterministic jitter of tens of Gbps for typical PCB materials can be caused by the fiber-resin dielectric inhomogeneity along the interconnect causing additional signal degradation due to variations in propagation constant and characteristic impedance along the line [47]. This is also related to the resonant type increase in insertion and reflection losses. 3D electromagnetic analysis by using a detailed description of weave geometry and resin filling can accurately and effectively model the fiber-weave effect.

3.3 Models for Non-Uniform Dielectric along Transmission Lines

Glass weave induced skew arises when signals in the two lines that make up a differential pair travel at different speeds due to local variations in the dielectric constant. The dielectric constant variation is due to the higher dielectric constant of the glass weave, compared to the resin and its bunching into fiber bundles. This is illustrated in the figure 3.3.

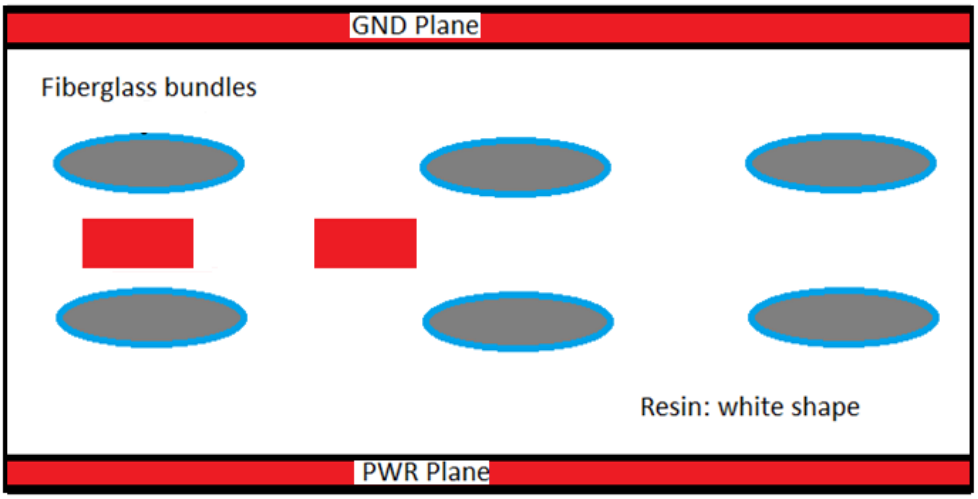


Figure 3.3: Models for non-uniform dielectric along traces transmission lines.

Although, models for transmission lines are usually constructed with either 2D or 3D field solvers, transmission lines with inhomogeneous dielectric may require analysis with a full-wave 3D solver to account for the high-frequency dispersion. Accuracy of solver results depends upon the availability of parameters of dielectric models. Availability of accurate parameters of material models is the most important element for 3DFEM solver engine. Manufacturers of dielectric laminates usually provide dielectric parameters at 1-3 frequency points in the best cases. Those frequency points may be acceptable to define the wideband Debye model [48]. Wideband Debye (Djordjevic-Sarkar) and multi-pole Debye models are examples of causal dispersive dielectric models suitable for accurate analysis of PCB interconnects.

Lichten-Ecker-Rother upper boundary model (layered dielectric):

$$\varepsilon_{eff,\,max} = \varepsilon_2 . f . \varphi + (1 - \varphi . f) . \varepsilon_1 \qquad (3.2)$$

and lower boundary model (comb-like dielectric):

$$\varepsilon_{eff,\,min} = \frac{\varepsilon 1 . \varepsilon 2}{\emptyset . f . \varepsilon 1 + (1 - \emptyset . f) . \varepsilon 2} \qquad (3.3)$$

where ϕ is the Imbalance Factor. Assuming dielectric 2 is glass with higher DK and lower LT and dielectric 1 is resin with lower DK and higher LT and both simulated with causal models

$\phi = 1$, corresponds to the original "homogenized" model

$\phi > 1$, increases the dielectric constant and automatically decreases the loss tangent

$\phi < 1$, decreases the dielectric constant and automatically increases the loss tangent.

At the lower GHz frequency range, the composite mixture can be simply homogenized and an effective broadband dielectric multi-pole or wideband Debye (Djordjevic-Sarkar) model [48] can be identified and used for the analysis of signal propagation. Cadence Sigrity 3DFEM full solver is used to develop models for non-uniform dielectric along transmission lines of traces.
Further, the investigation of fiber weave effect on high speed HDMI interface is analyzed by using a board made with FR408HR.

3.4 Investigation of Fiber Weave Effects on HDMI Channels

An increase in the date rate of a HDMI interface leads to a reduction in the timing margin of the interface. The timing margin reduction requires very tight time skew control such as time skew between positive and negative channel in a differential pair. In HDMI timing topologies, data rate is above 5 Gbps. For this timing topology, intra-pair skews are important factors that impact timing performance. Additional time skew impacted by fiber weave effect can be a potential performance risk. Furthermore, intra-pair time skew is an important design parameter to control the jitter of the eye diagram.

Figure 3.4 (a)-(b), shows the HDMI board layout snapshot. Four differential pairs are used to transmit high speed signals and another four pairs are used for receiver. In both the groups, high speed data is floating above 5 Gbps. At this high data rate, the fiber weave effect could affect the skew of the differential pairs.

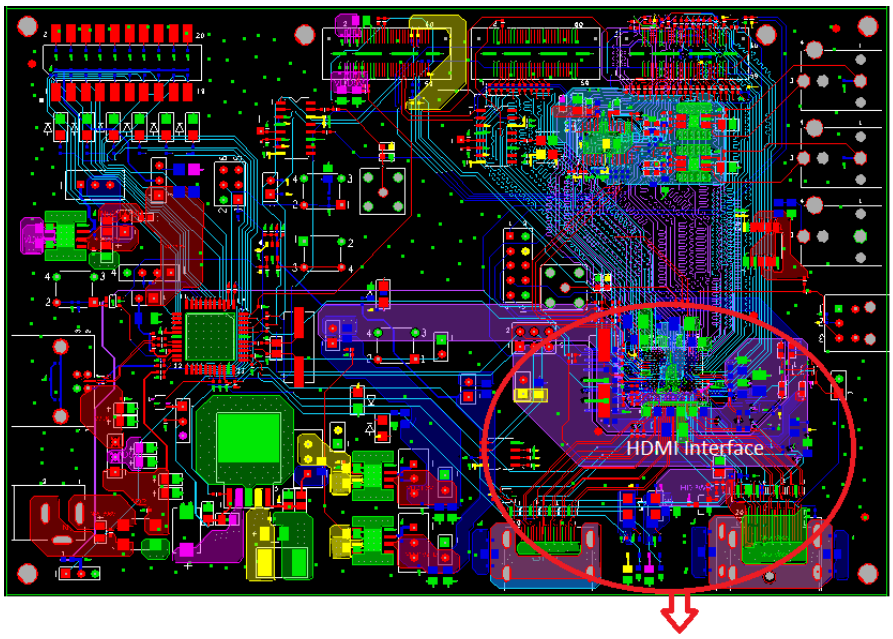


Figure 3.4(a): HDMI board layout

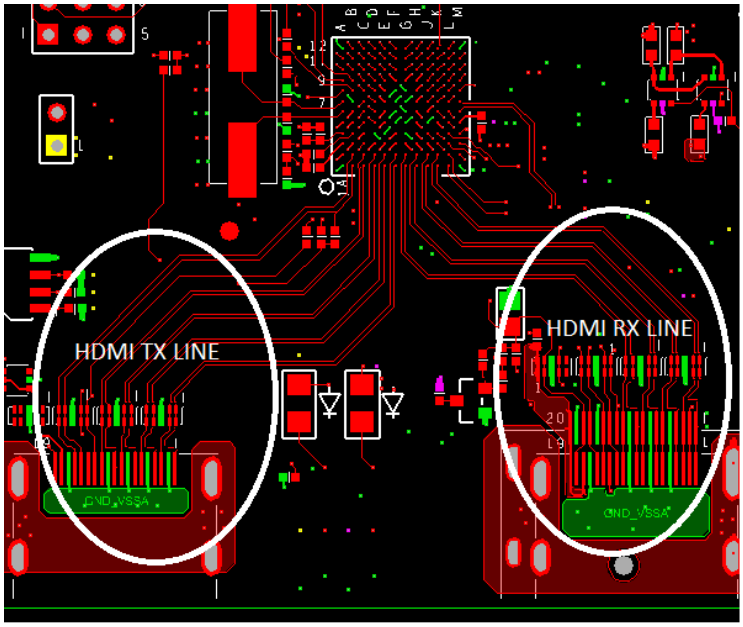


Figure 3.4(b): HDMI board layout: four lines for TX and another four for RX

In order to analyze this effect, a 3D FEM full wave simulation model has been carefully defined to make the traces unbalanced as in a practical PCB design. Figure 3.5 shows a cross-sectional profile of transmission lines with and without fiber weave effect. The differential pairs trace width is 4 mils and separation is 8 mils for all differential pairs used in the test layout.

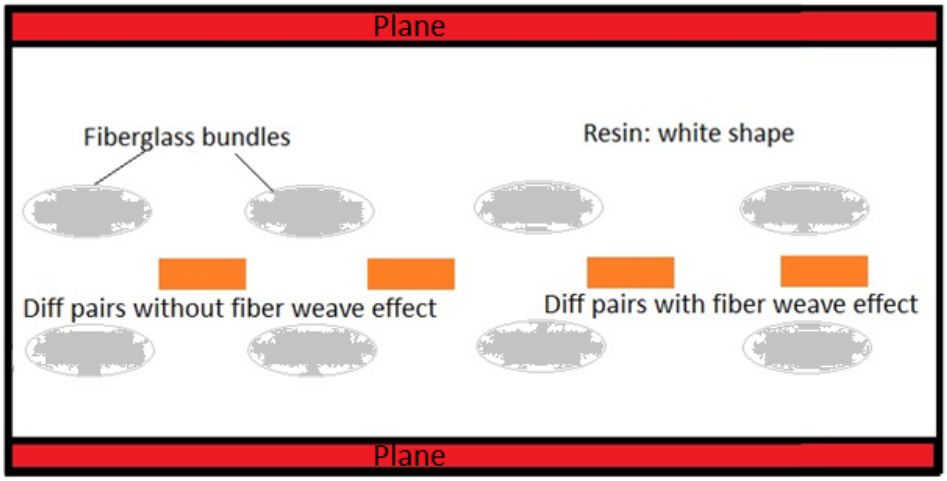


Figure 3.5. Cross-sectional profile of HDMI transmission line model with/without FWE.

For testing purpose, start this process by selecting an asymmetric differential stripline for glass type 2116, as shown in figure 3.5. In differential pair without fiber weave effect, both traces are placed with a specific width and spacing to have the same Dk value. This means that the inter-pair skew in differential pair is less effected. At high data rates, the difference in propagation velocities leads to skew between the two traces, which can amount to a substantial fraction of the transmission unit interval, resulting in an increased common mode voltage and a correspondingly degraded differential signal.

$$V = \frac{C}{\sqrt{\varepsilon r}}$$

$$\text{Propagation delay } (t_d) = \frac{1}{v}$$

$$= \frac{\sqrt{\varepsilon r}}{c}$$

$$\varepsilon r = (t_{pd} \times C)^2 \qquad (3.4)$$

Velocity of stripline is 85 ps/inch approx., putt this value in equation 3.4.

$$\varepsilon r = (t_{pd} \times \frac{1}{85})^2 \qquad (3.5)$$

By using the worst case skew by placing the traces with specific width and spacing to have the largest difference in Dk values, where one trace is positioned in the region containing the most

glass by volume and the other trace positioned in the region with the most resin [49-50]. The skew is varied as a function of trace position by maintaining the same differential impedance. To accomplish this, one trace is centered in the maximum resin region while the location of the other trace is shifted. It should be noted that by the differential impedance is kept at a constant value (100 ohms) and the edge coupling between the traces is increased.

Figure 3.6: 3D transmission line model in Sigrity 3DFEM tool.

With the 3D transmission line model, the intra-pair time skew have been analyzed using the transient simulation engine in Sigrity 3DFEM as shown in figure 3.6. In this transient simulation, a step pulse is simulated with differential termination to observe the time skews with respect to transmission line length.

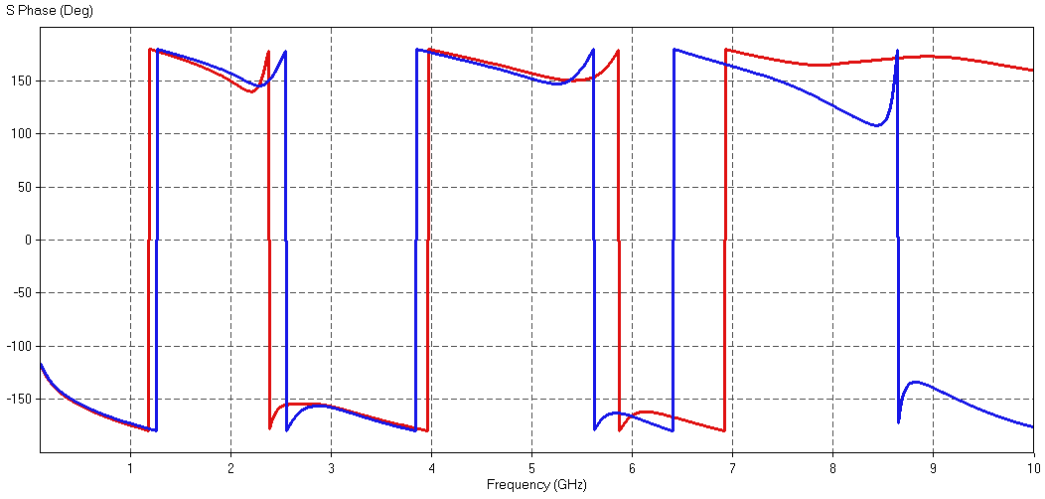


Figure 3.7: Simulated phase corresponding to each of the traces on asymmetric structure.

Here, figure 3.7 shows the simulated phase corresponding to each of the traces when both traces run on asymmetric structure. There is an obvious phase difference between the traces owing to the fiber weave effect. First of all, the red line corresponds to the trace running primarily over the glass bundle. The fiber glass bundle has a higher permittivity than resin; therefore, the phase changes more rapidly per unit length of the trace [51]. The red trace runs primarily over the resin, so phase is changed slowly. Because the resin has a lower permittivity than the glass fibers, the phase changes more slowly per unit length of the trace.

In the second case, figure 3.9 shows the simulated phase corresponding to each of the traces on the 3D model of figure 3.8 when both traces run on symmetric structure.

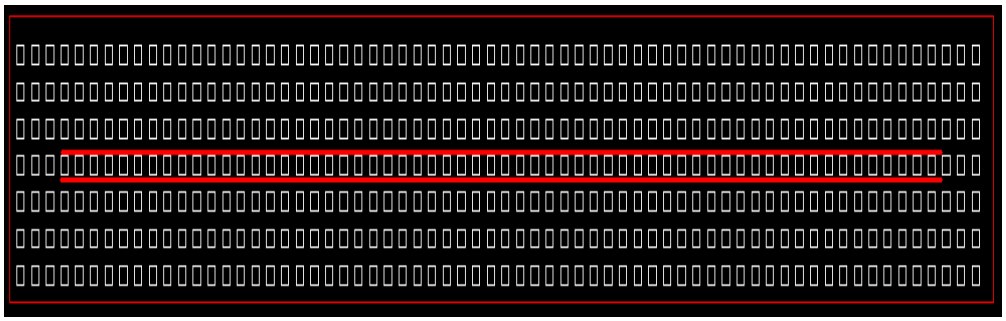


Figure 3.8: The simulated phase corresponding to each of the traces on symmetric structure.

Figure 3.9 shows that there is a lesser phase difference between the traces owing to the fiber weave effects. Both the lines correspond to the trace running primarily over the resin bundle, so the phase changes more slowly per unit length of the trace.

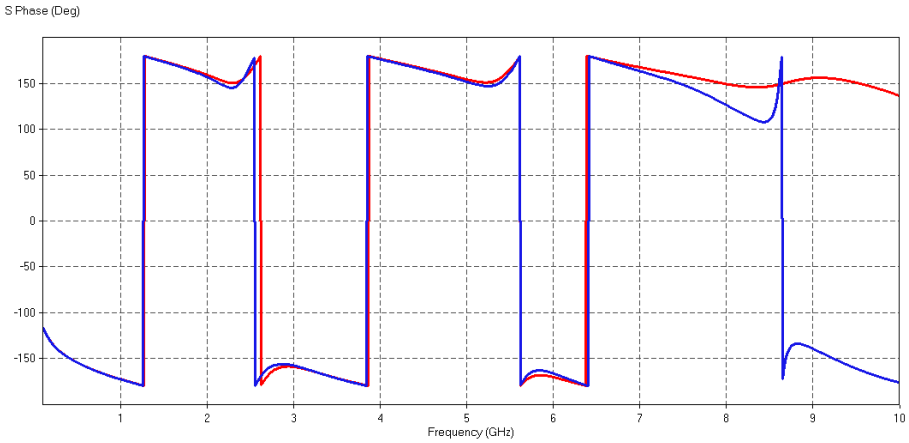


Figure 3.9: The simulated phase corresponding to each of the traces on symmetric structure.

3.5 Solution to Reduce Fiber Weaves Effect

A solution to mitigate the effects of fiber weaves is proposed. Route the transmission lines on the PCB by using different routing angle 0^0 to 20^0 to average out the effects of anisotropicity of fiber disposition. Four cases, $0^{0,}$ $10^{0,}$ 15^0 and 20^0 angle of routed signals on PCB are investigated. S-parameters are extracted for each angle of rotation and inserted into the board model in test bench setup; the channel performance is checked using Sigrity tool as shown in figure 3.10. AMI model is assigned to TX and Rx and the eye parameters and BER curve are measured.

Simulation setup:

TX = 4 differential pairs to transmit high speed data

RX = 4 differential pairs for receiver

AMI model is assigned at TX and RX.

S- Parameter is extracted from the board and assigned to the board block of the test bench as shown in figure 3.10.

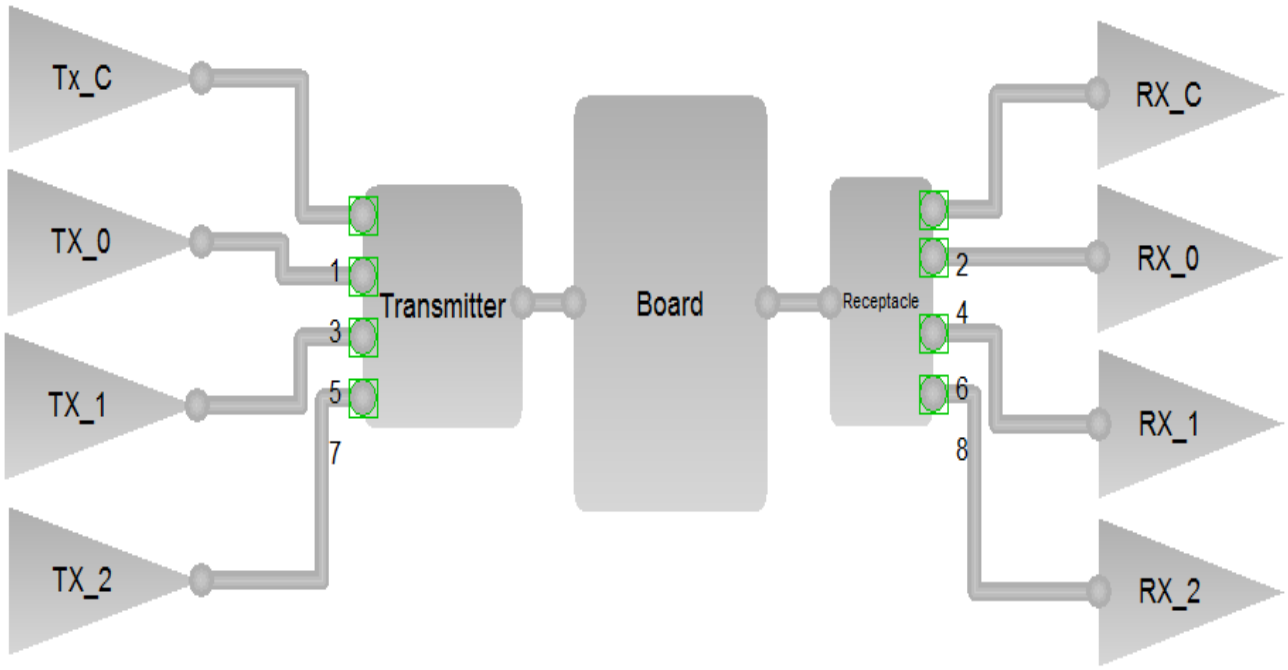


Figure 3.10: Test bench setup for HDMI channel simulation.

3.5.1 Case1: 0º Rotation

TX and RX lines mounted on the printed circuit board is 0º as shown in figure 3.11. Glass weave induces a skew if location variation in the dielectric constant makes signals in the two lines of a differential pair travel at different speeds. The glass weave with a high dielectric constant bunched into fiber bundles causes a variation in the dielectric constant.

Figure 3.11: TX lines routed with 0 degree rotation on the PCB.

3.5.2 Simulation Result for 0º Rotation

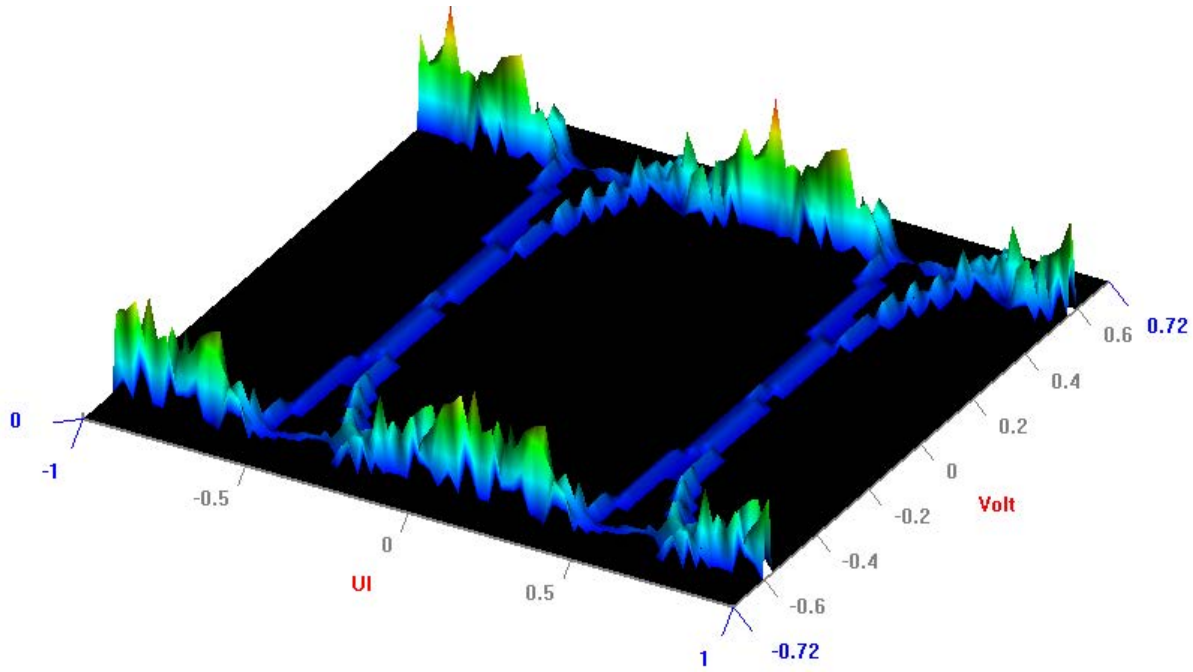


Figure 3.12(a): Eye diagram, when 0º rotation routing on the board.

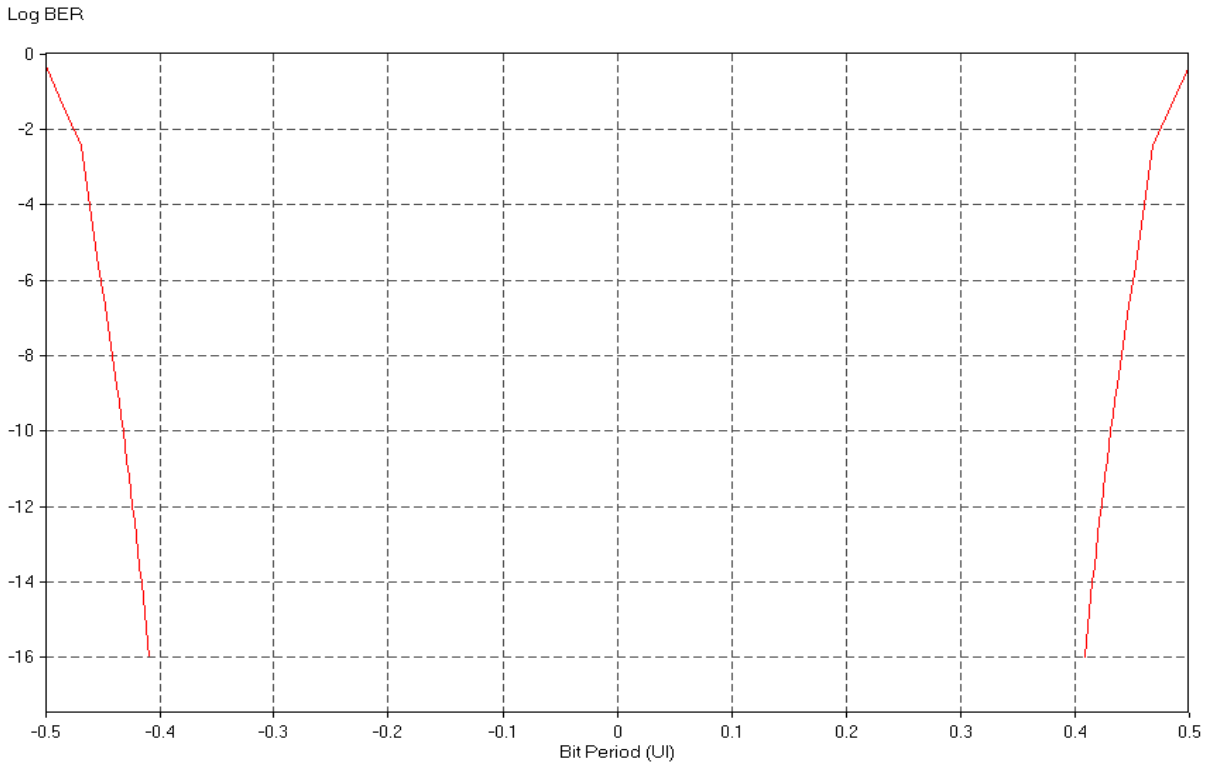


Figure 3.12(b): BER plot, when 0^{o} rotation routing on the board.

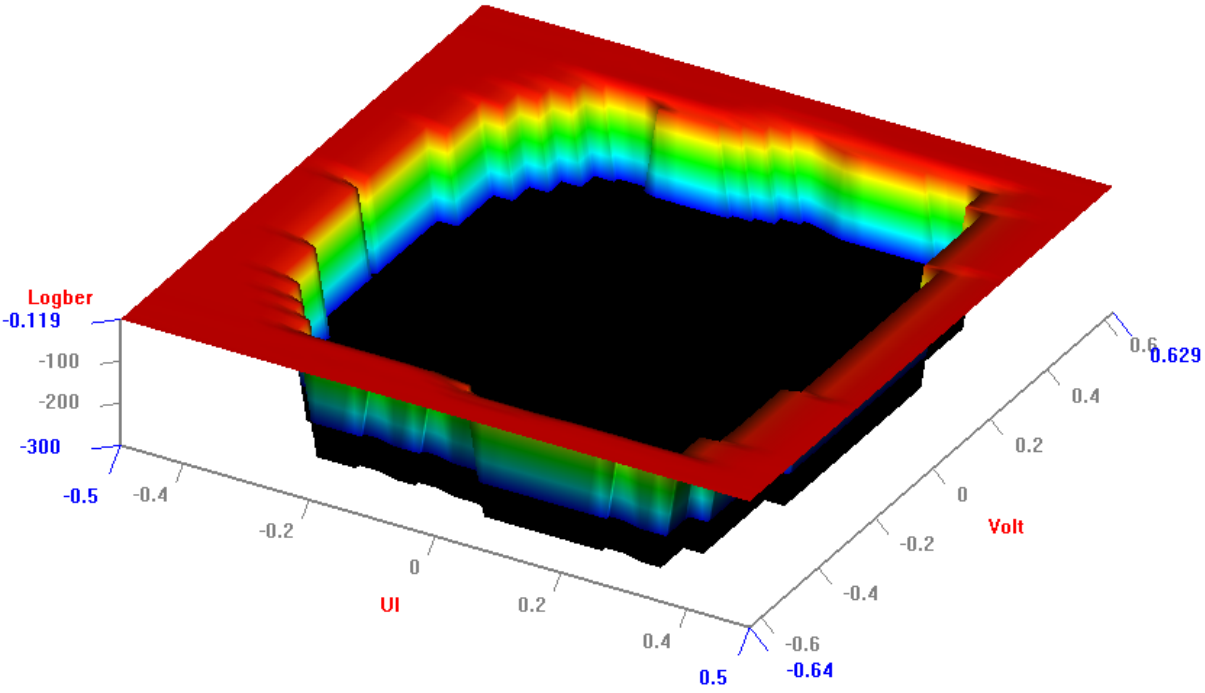


Figure 3.12(c): Batch tub curve plot, when 0^{o} rotation routing on the board.

Table 3.1 shows the simulation results for 0^o rotation

Trace Length	2.5 inch
No of Bits	100439
No. of Eye Bits	100626
Inter pair skew	11.3
Eye height	973mV
Eye norm Jitter	0.47

Figure 3.12 shows the three results, (a) eye diagram, (b) BER plot and (c) bathtub curve. Table 3.1 shows that eye height is decreased and jitter increased. In table 3.1 shows the simulated measured values from simulated curves.

3.5.3 Case2: 10^o Rotation

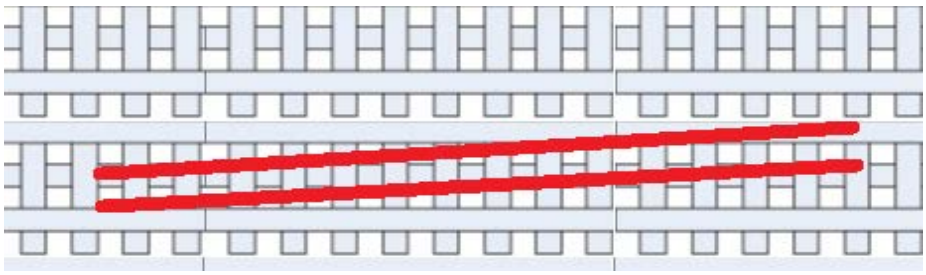


Figure 3.13: TX lines routed with 10^o rotation on the PCB.

3.5.4 Simulation Results for 10º Rotation

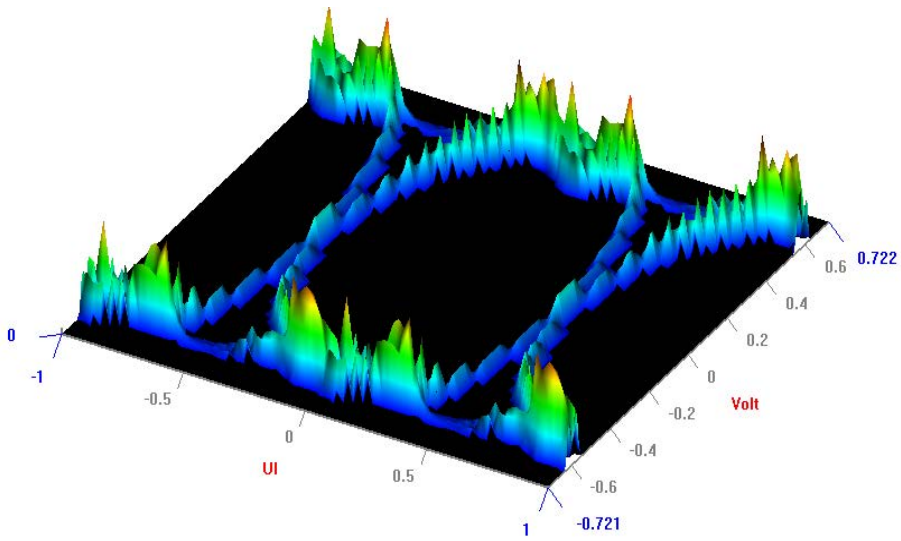


Figure 3.13(a): Eye diagram, when 10º rotation routing on the board.

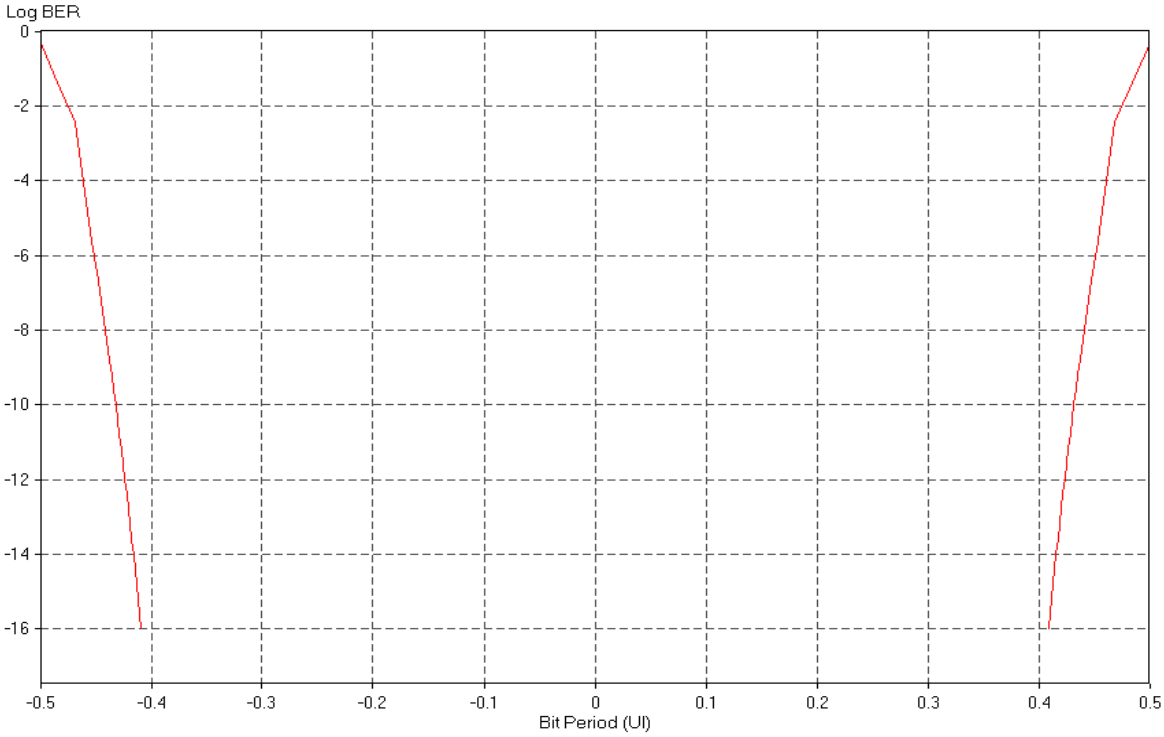


Figure 3.13(b): BER plot, when 10º rotation routing on the board.

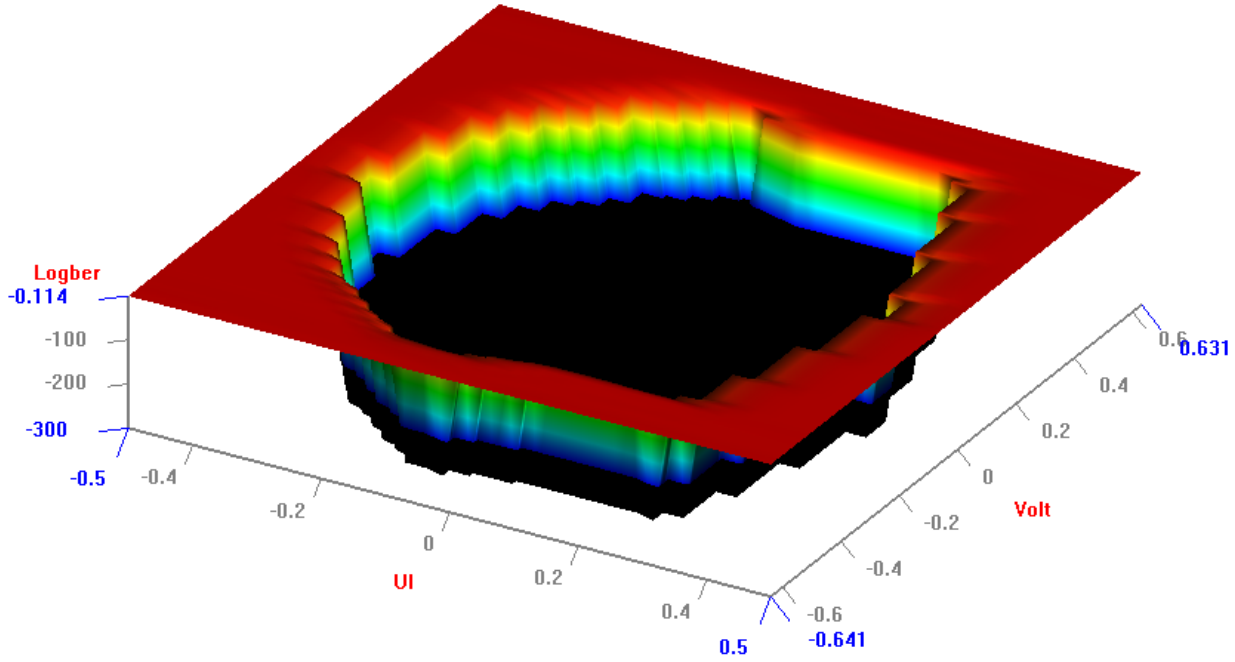


Figure 3.13(c): Batch tub curve plot, when 10^{o} rotation routing on the board.

Table 3.2 shows the simulation results for 10^{o} rotation

Trace Length	2.5 inch
No of Bits	100439
No. of Eye Bits	100626
Intra pair skew	2.8
Eye height	1137mV
Eye norm Jitter	0.38

3.5.5 Case 3: 15^{o} Rotation

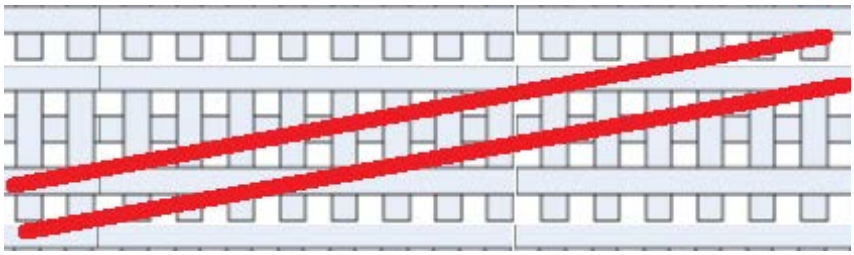


Figure 3.14, TX lines routed with 15^{o} rotation on the PCB.

3.5.6 Simulation Result for 15º Rotation

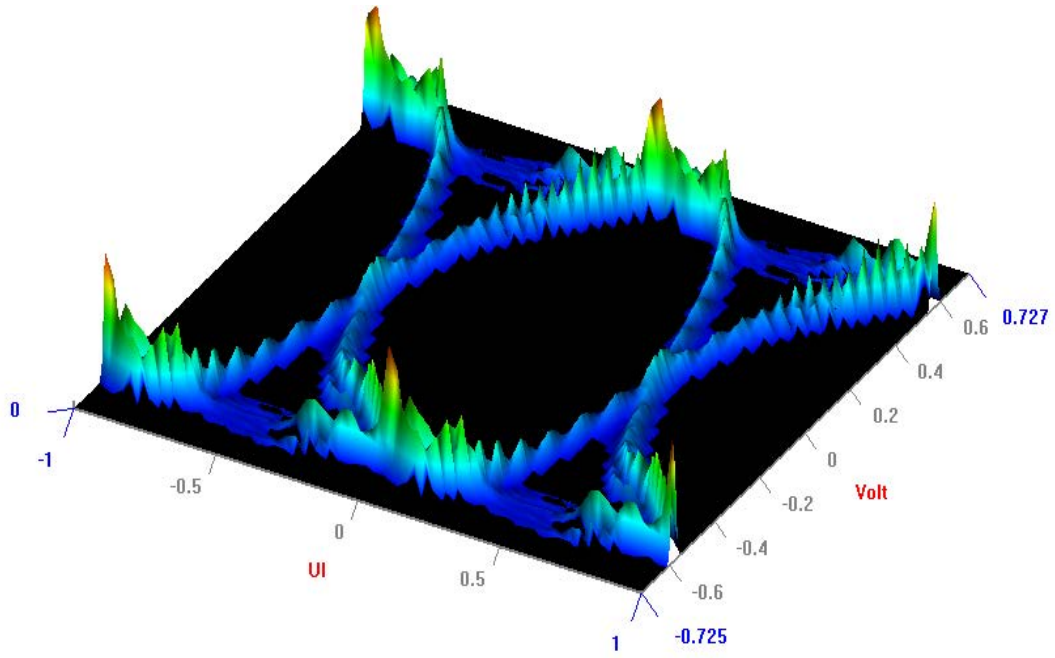


Figure 3.15(a): Eye diagram, when 15º rotation routing on the board.

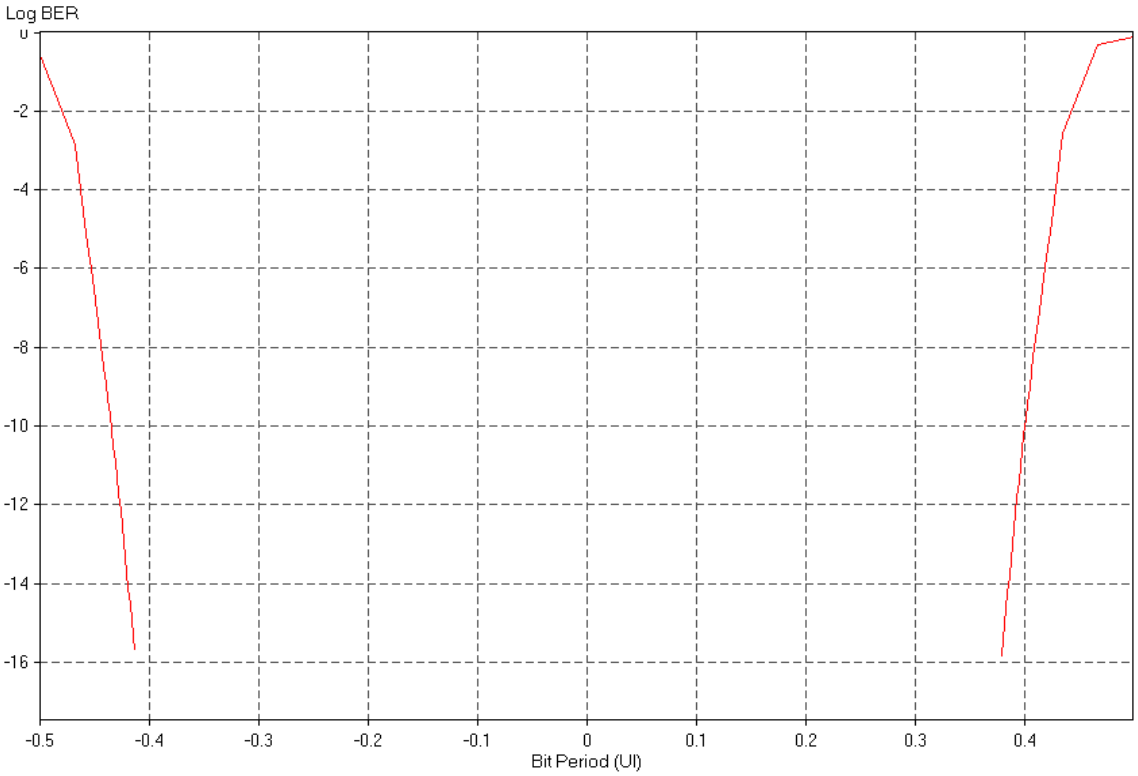


Figure 3.15(b): BER plot, when 15º rotation routing on the board.

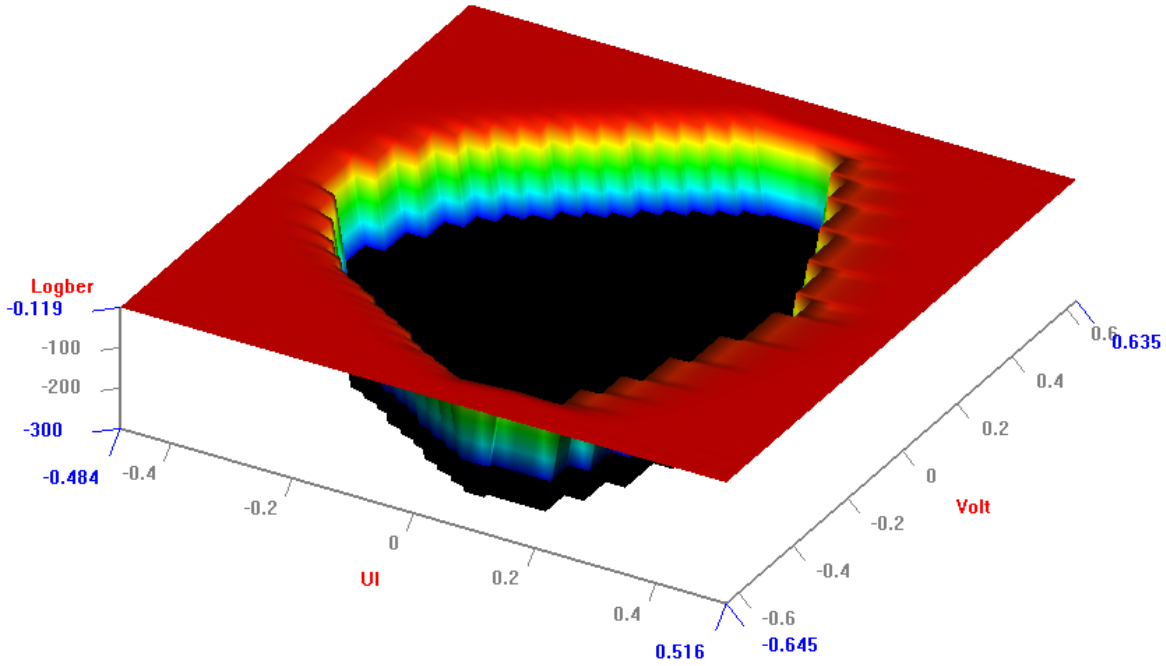


Figure 3.15(c): Batch tub curve plot, when 15^{o} rotation routing on the board

Table 3.3 shows the simulation results for 15^{o} rotation

Trace Length	2.5 inch
No of Bits	100439
No. of Eye Bits	100626
Intra pair skew	6.195
Eye height	1113mV
Eye norm Jitter	0.27

3.5.7 Case4: 20^{o} Rotation

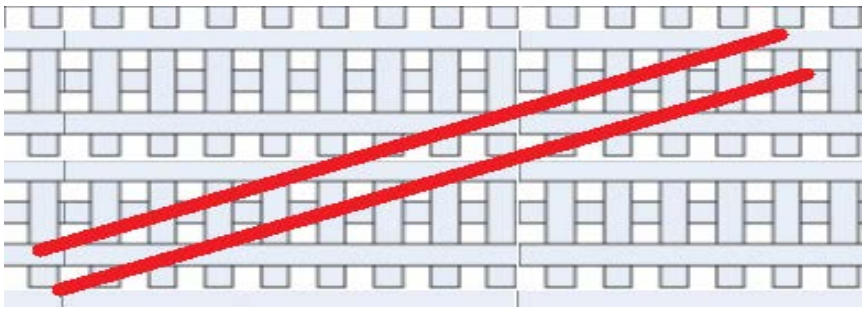


Figure 3.16: TX lines routed with 20^{0} rotation on the PCB.

3.5.8 Simulation Result for 20º Rotation

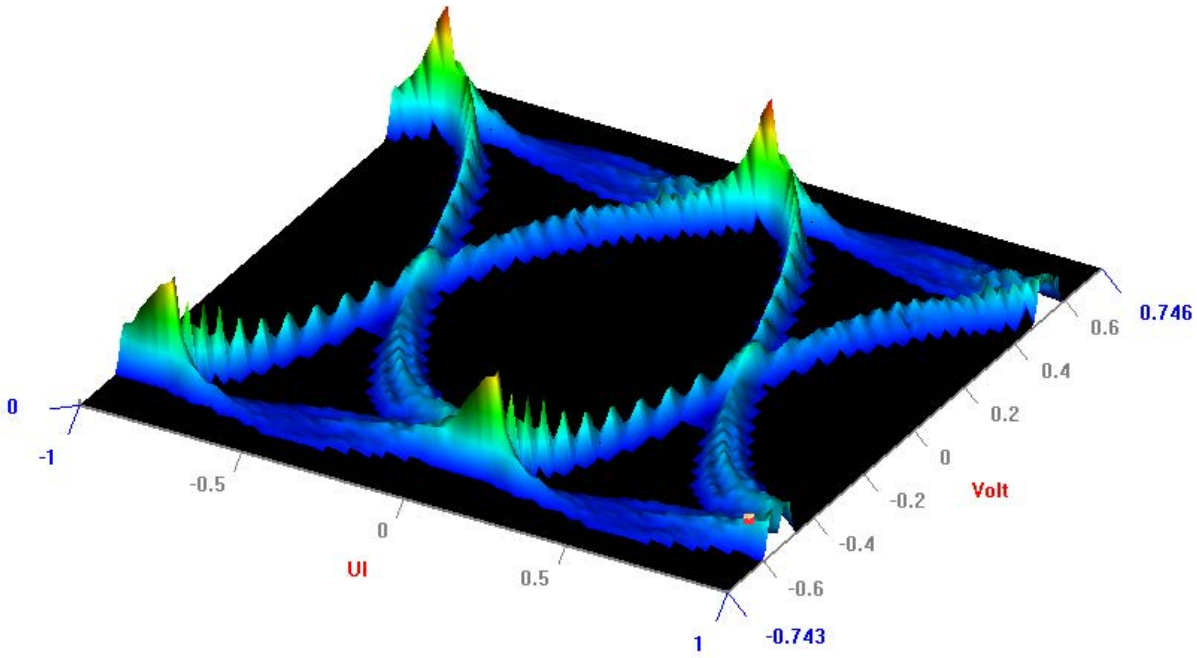


Figure 3.17(a): Eye diagram, when 20º rotation routing on the board.

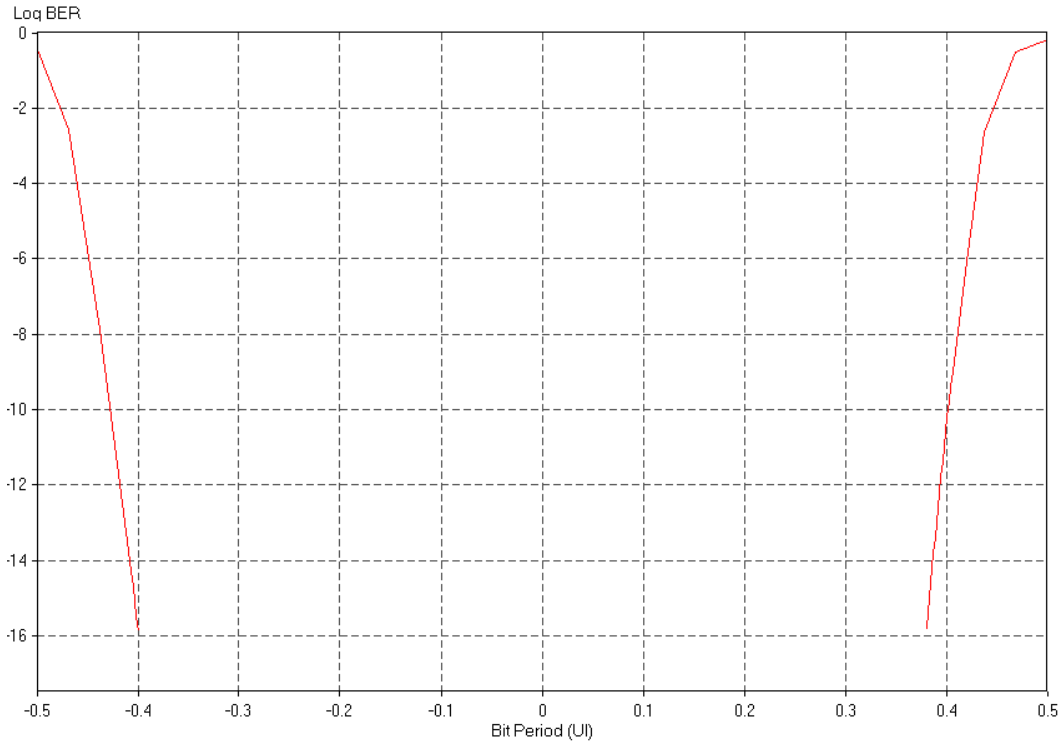


Figure 3.17(b): BER plot, when 20º rotation routing on the board.

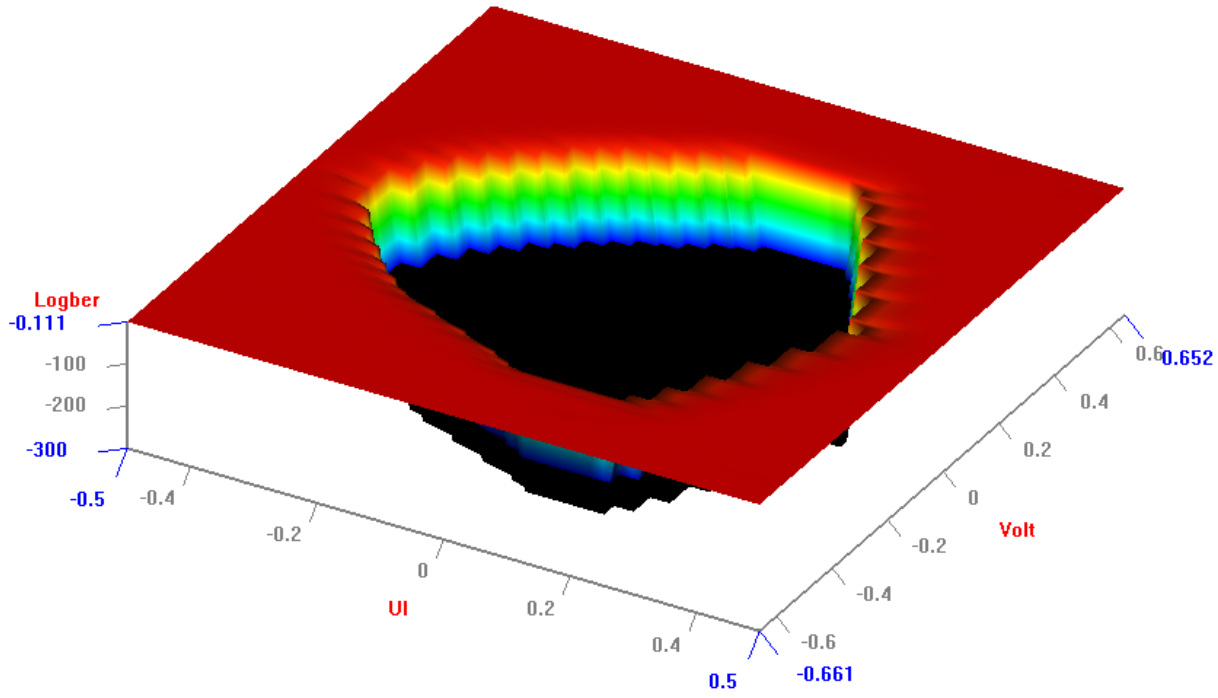


Figure 3.17(c): Batch tub curve plot, when 20^{o} rotation routing on the board.

Table 3.4 shows the simulation results for 20^{o} rotation

Trace Length	2.5 inch
No of Bits	100439
No. of Eye Bits	100626
Intra pair skew	7.2
Eye height	1156mV
Eye norm Jitter	0.17

Tables 3.1, 3.2, 3.3 and 3.4 shows the intra-pair time skew due to fiber weave effect and also shows the eye height and eye jitter. Table 3.5 shows the intra-pair time skew with respect to change in the rotation angle due to fiber weave effect and table 3.6 shows the BER measurement parameters for all four cases. The intra-pairs skew is lowest when rotation angle is 10^{o}, as shown in table 3.5. Intra-pair timing skew in a differential path causes an increase in the differential

insertion loss profile due to timing induced resonances. Increasing the fiber weave effect length, results in a proportional increase in timing skew leading to a decrease in the resonant frequency by the same proportion.

Table 3.5: Shows the intra-pair time skew with respect to change in the rotation angle

Routing Angle	**Skew**
0	11.3
10	2.8
15	6.195
20	7.2

Table 3.6: Bathtub curve (BER) measurement comparison table

	Eye Width(UI)				Eye Height(mV)			
LBER	10^0	15^0	20^0	0^0	10^0	15^0	20^0	0^0
-16	0.81	0.79	0.80	0.78	1025	1024	1008	855
-15	0.82	0.79	0.81	0.78	1030	1027	1014	859
-14	0.83	0.8	0.81	0.79	1036	1031	1020	863
-13	0.83	0.81	0.79	0.8	1043	1034	1026	867
-12	0.84	0.81	0.82	0.81	1049	1038	1032	872
-11	0.85	0.82	0.82	0.82	1056	1042	1039	877
-10	0.86	0.83	0.83	0.82	1064	1046	1046	882
-9	0.87	0.84	0.85	0.83	1071	1050	1053	887
-8	0.88	0.85	0.84	0.84	1079	1055	1061	892
-7	0.89	0.86	0.85	0.85	1088	1059	1068	898
-6	0.9	0.87	0.86	0.86	1093	1064	1074	904
-5	0.91	0.88	0.86	0.88	1099	1069	1080	909
-4	0.92	0.89	0.88	0.89	1104	1074	1085	923
-3	0.93	0.9	0.9	0.89	1109	1097	1092	945

Eye width and height is improved when rotation angle is 10^{o}, as shown in table 3.6.

Another solution to mitigate the effects of anisotropic is the use of tight/spread weaves. Traditional fabrics (106, 1080) are loosely woven fabrics with resin filling the gaps. This affects the signal propagation. In case of tight/spread weaves (7628), fibers are closely spaced leaving small pores filled with resin, this has a minor affect on signal propagation.

3.6 Summary

Results demonstrate the fiber weave effect introduces unwanted intra-pair skew on differential signaling, which, if not resolved can lead to failure of high-speed designs. It is, therefore, essential to identify and characterize skew to ensure a robust design for improving the timing margin between differential pairs of high-speed signals. The characterization must include analysis of skew data in manufactured products.

Several low-loss laminates, characterized above 10GHz, makes it possible to extend the copper-based interconnect to above Gbps backplane links. The result of this work, as demonstrated by Table 3.6, is a systematic and practical methodology to analyze and minimize fiber-weave effect for above 5 Gbps interconnects at 10^{0} rotation.

The fiber weave effect must be comprehended and properly accounted for in future high speed bus designs by using routing angle 10^{0} of traces on PCB (only for high speed signals). Table 3.5 shows when the fiber weave effect requires special accommodations to alleviate its effects and when it can be ignored.

CHAPTER 4

IMPEDANCE CONTROL METHOD TO MINIMISE THE SPLIT PLANE EFFECT

4.0 Introduction

Signal integrity is important in all applications requiring precision and quality, including in medical environments that use sensitive medical devices. Medical devices are affected by electromagnetic interference (EMI) factors, such as electrostatic discharge and power line disturbances, emanating from various sources, like electronic devices within and, even, outside premises. In addition, the use of high frequency signals in the medical devices themselves leads to signal integrity problems at the PCB level of these devices. A digital system can be examined at three levels of abstraction, namely, logic, circuit theory and electromagnetic (EM) fields; the logic level being the highest level where SI problems can be easily identified. Most of the SI problems, such as reflection, crosstalk and ground bounce, are EM problems.

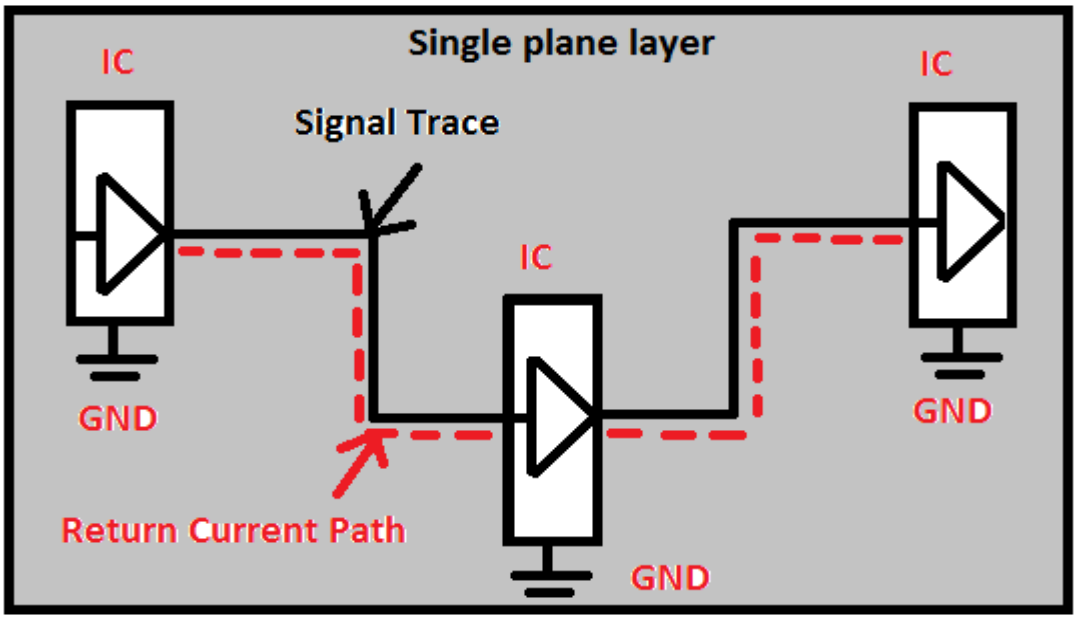


Figure 4.1: Currents on the PCB follow the path of least inductance.

The currents on the PCB follow the path of least inductance when high-speed signals flow in the trace as shown in figure 4.1. The only way for that to happen is if the return current travels directly under the signal trace on its way back to the source, as long as no discontinuities exist in the return plane.

In high-speed design PCBs, ground and power noises need to be isolated and different parts of the circuits in a layer requires a different supply voltage level; DC power supply voltages may be at different voltage levels of PCB because different values of voltages are required on the PCB due to semiconductor devices working on different voltages. To ensure noise isolation and to provide different supply voltages, the PCB needs to be partitioned. However, this leads to serious and high multitude of problems in the domain of signal integrity. The partitioning breaks the current return path of the signal current through either power plane or ground plane, causing significant undesirable radiation effects due to reflection or crosstalk. The reflection of signals causes delay, skew and jitter problems.

When a high frequency signal crosses the split plane gap, the return current path inductance is increased during the crossing of the plane [52]. The inherent inductance leads to two EMC problems, creation of a radiating dipole and increased magnetic coupling [53]. An efficient radiating dipole is created by high frequency current passing through the inductance and, thereby, developing a voltage that appears across the two parts of the plane, each of which has a high capacitance. The radiating dipole is then enhanced if cables are attached to the board. In the other case, the inductance represents the increased magnetic coupling through the enclosed loop area. Although, it can be concluded that split planes should be avoided or high frequency currents should be prevented from flowing between the two separated segments to remove the additional inductance, power and ground gap is mandatory in many cases in practical layouts [54]. For instance, for systems implemented on PCBs with only one metal layer for power distribution but requiring multiple power supplies, it becomes imperative to cut the ground or power planes into several sections to distribute multiple level voltages with low inductance.

Figure 4.2 shows the signal integrity and timing parameter of a device is changed by the return path discontinuities on high speed bus. This is brought by the impedance discontinuities because of local return inductance and capacitive changes as also undesirable side effects on the PCB due to radiation effect, reflection of signal, or crosstalk, all produced by return path discontinuities.

To add to this, impedance alteration in the power distribution network (PDN) caused by return path discontinuities also impact power integrity (PI).

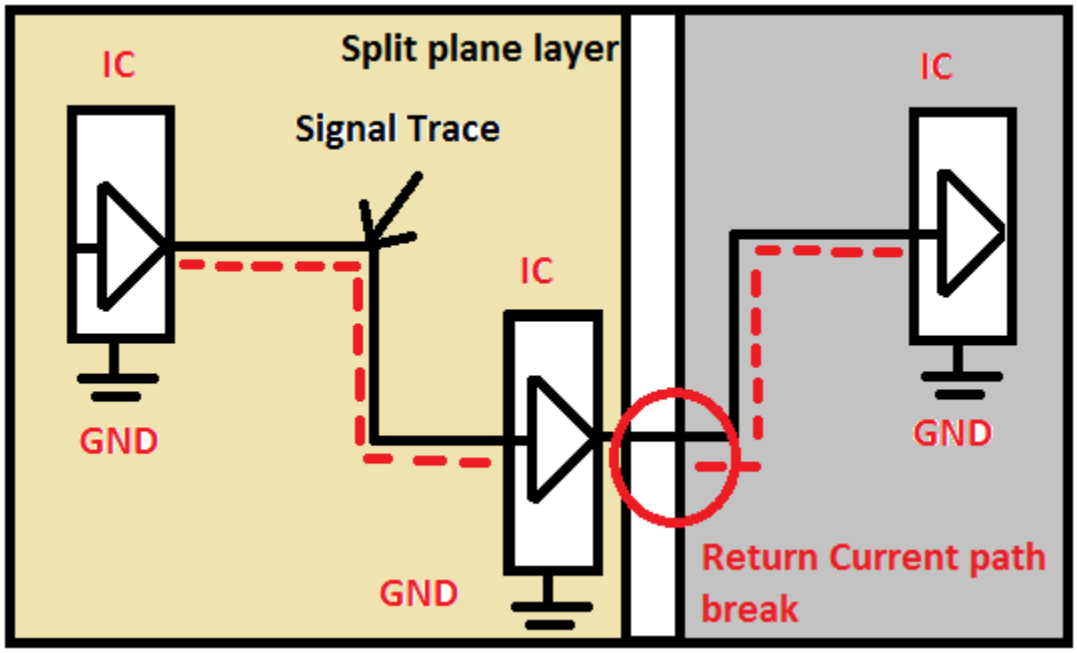


Figure 4.2: Return path discontinuities when high speed bus crossing the split slot.

As a solution to solution to minimize the slot plane effect of high frequency signals crossing slot gaps, this chapter proposes an impedance control method. It is a geometry based method to understand the physical degradations in the PCB in a holistic manner, integrating both power integrity (PI) and signal integrity (SI) analyses, to arrive at closer to reality and practical results. Historically, SI analysis studied signal behavior while traversing PCB traces, connectors, passive components and on assuming near perfect power supply; whereas PI analysis studied a design's power delivery networks to evaluate power plane impedance, decoupling capacitance, and so on without properly factoring the impact of the switching signals. The two are inextricably linked and should be simulated simultaneously to avoid over-optimistic results. In this chapter, power aware signal integrity is analyzed for high speed links in a medical system.

In this chapter, the following two different configurations are investigated:

1) High speed signals crossing the slot gap on PWR/GND planes.

3) High speed signals crossing the slot gap on PWR/GND planes with capacitor near the slot gap crossing.

The chapter starts by briefly describing the test vehicle, which is used as reference for the simulations/measurements, and by presenting a validation of one of the considered modules. This is followed by a discussion of the impact of the return path discontinuity (RPD) on SI and mode conversion, augmented by a section that quantifies the incidence of the same RPDs on PI both in time and frequency domains.

4.2 Return Current Path Discontinuity

Different devices on a PCB with different supply voltages makes it necessary for PCBs have several power domains, because on the other hand, numerous high speed serial channels and splits in the power planes of modern PCB boards disrupt the propagation of signals or cause EMI problems. Instead of the least resistance path, high-speed return current path follows the path of least inductance, which lies directly under a signal conductor minimizing the total loop area between the outgoing and returning current paths [55]. When a signal crosses the split plane, the energy on the return path is disrupted at split location, generating scattered waves in all directions and, particularly, back to the source.

Figure 4.3 shows speed signals crossing split power planes generated by splitting a plane into two islands, one used for 1.2 V and another for 3.3 V, isolated from each other by a small gap. The split plane gap is crossed by tracks at different locations. In addition to capacitance, the impedance of the track, which depends upon the height of the track from the nearest plane and changes in frequency, also varies while crossing the split plane gap.

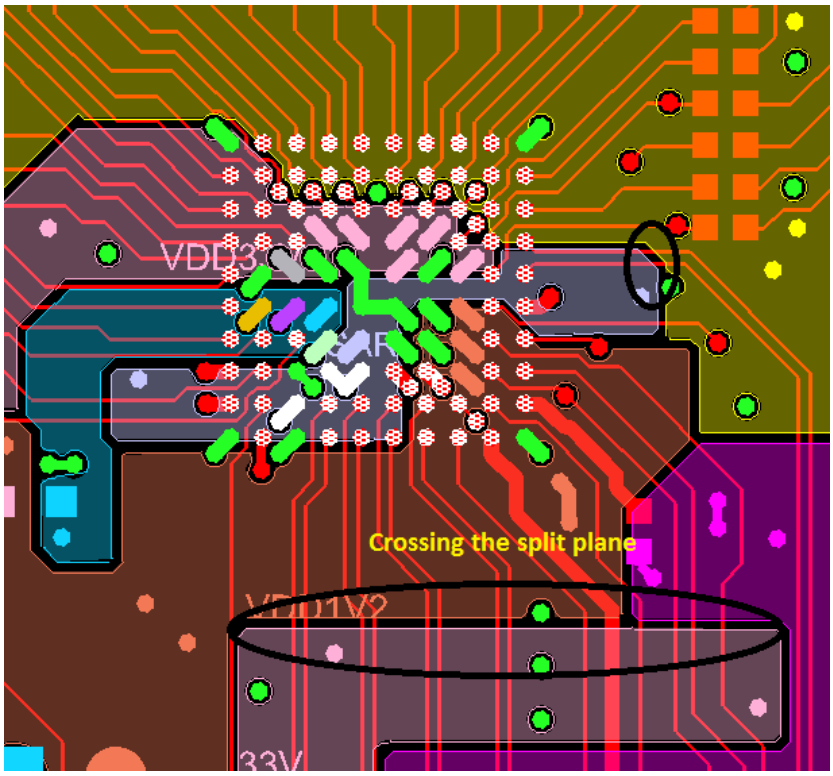


Figure 4.3: High speed interface crossing the multiple split power planes.

4.3 Impact of Signal: Crossing a Split Reference Plane

In figure 4.4 a power plane divided into three isolated split planes i.e. 2.5V, 1.2 V and 3.3 V. High frequency signals crossing over split gaps result in a change in the track impedance due to absence of solid copper in the gap area. The impedance of the traces increases as frequency increases due to an increase in the height with respect to the nearest reference plane. Routing high-speed signals over slots of nearby reference planes can cause undesirable effects such as impedance discontinuities, EMI noise, or crosstalk [56].

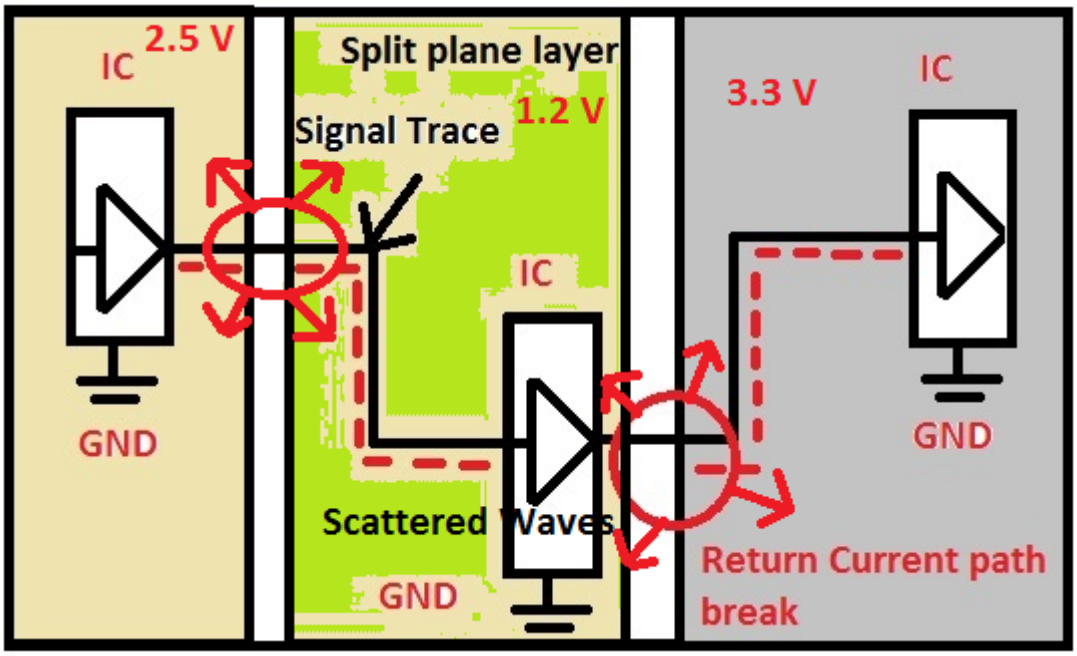


Figure 4.4: High frequency signals crossing the multiple split planes.

Figure 4.5 illustrates the electric field building up in a transmission line as the signal propagates down the line. The speed of the signal in the transmission line depends on how fast electric and magnetic fields change [57]. A sudden voltage change creates a sudden electric and magnetic-field change. This sudden change of field propagates through the dielectric material surrounding the transmission line at the speed of changing electric and magnetic field.

$$V_0 = \frac{1}{\sqrt{\varepsilon_0 \varepsilon_r \mu_0 \mu_r}} \qquad (4.1)$$

where ε_0 is the permittivity of free space (8.89 x 10^{-12} F/m), ε_r is the relative dielectric constant of the material, μ_0 is the permeability of free space (4π x 10^{-7} H/m) and μ_r is the relative permeability of the material. Virtually for all interconnect materials; the magnetic permeability of the dielectrics, μ_r, is 1. The speed of the signals in the strip line depends upon the dielectric constant of the dielectric material. Generally, Fr4 material is used in PCB fabrication.

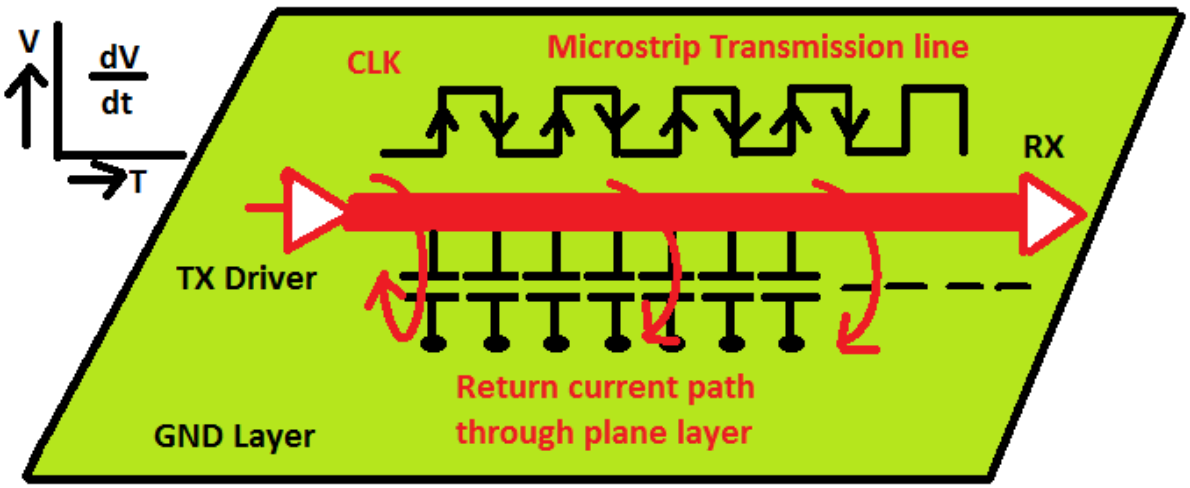


Figure 4.5: Signal current return path through distributed capacitance of transmission line.

When the signal propagates into a transmission line, capacitor comes into the picture (Figure 4.5). As the voltage across the capacitance changes, current flows through the capacitor into the nearest plane, whereas when the signal voltage is constant, there is no current flow through the capacitor. When the signal propagates through the transmission line, the voltage across the signal and return path conductor ramps up. During transition time at signal edge, voltage changes and current flows through the initial capacitor. When current flows in the signal path, the capacitor is charged and the same amount of current flows out of the return path. While the signal propagates down the transmission line, the return current flows through the capacitance to the return-path conductor and loops back to the source. The instantaneous impedance (Z_o) of the transmission line is the ratio of the signal voltage (V) to the signal current (I).

$$Z_0 = \frac{V}{I} \qquad (4.2)$$

Low transmission lines operate in the low loss region. The characteristic impedance of the low loss line is

$$Z_0 = \sqrt{\frac{L}{C}} \qquad (4.3)$$

where L is the inductance and C is the capacitance.

Delay per inches is

$$T_P = \sqrt{LC}. \tag{4.4}$$

where T_P is the propagation delay. From the Eq. (3) and (4)

$$L = Z_0 T_P \tag{4.5}$$

$$C = \frac{T_P}{Z_0} \tag{4.6}$$

The characteristic impedance of the transmission line is inversely proportional to the capacitance per unit length between the conductors. As per IPC, the most popular approximation of the microstrip equation for characteristic impedance and propagation delay are;

$$Z_0 = \frac{87}{\sqrt{\varepsilon_r + 1.41}} ln \frac{5.98h}{0.8w + r} \tag{4.7}$$

where, (h) is dielectric thickness below the signal trace to the plane, (w) is line width, (r) is metal thickness, and ε_r, is dielectric constant.

$$T_P = 85\sqrt{0.475\varepsilon_r + 0.67} \tag{4.8}$$

Equation (4.6) and (4.8) gives the capacitance per unit length, Put $T_P = CZ_0$

$$CZ_0 = 85\sqrt{0.475\varepsilon_r + 0.67}$$

$$C = \frac{85\sqrt{0.475\varepsilon_r + 0.67}\sqrt{\varepsilon_r + 1.41}}{87 \ln\frac{5.98h}{0.8w + r}} \tag{4.9}$$

$$C_0 = \frac{3.6}{\ln\frac{5.98h}{0.8w + r}} \tag{4.10}$$

From Equation (4.9) and (4.10), ε_r =1 the characteristics impedance per unit length is

$$Z_0 = \frac{90.95}{C_0} \tag{4.11}$$

Equation 4.11 shows that the characteristics impedance is inversely proportional to the capacitance of the track. Both, capacitance and characteristic impedance of the track depend on the height (h) between the reference plane and track [58]. In split plane, the height (h) increases with respect to the nearest reference plane. The capacitance is also dependent on the track width and track thickness during the crossing of the split plane gap. Generally, a layout engineer ignores these parameters during split plane crossing.

Characteristic impedance and capacitance of signal track are affected during crossing through the split plane. Figure 4.6 & 4.7 shows the Matlab simulation results for characteristic impedance and capacitance of signal track with respect to height (h). The signal crossing the split plane causes a change in impedance and decrease in the capacitance, during crossing. Figure 4.6 shows the capacitance value of the track with respect to height (h) having a track width (w) 8 mil, metal thickness (r) 1.14 mils when the signal crosses the split gap. The capacitance decreases when the height of the nearest plane layer increases. When impedance control method is used, height and thickness remains constant during crossing. Thus, the capacitance is increased. The inverse effect is seen when track capacitance increases and characteristic impedance of the track is decreased. SI problem in biomedical equipment is more when high frequency signals cross the slot gaps. The track capacitance is decreased due to change of the reference plane and an increase in the impedance of the track. There is reflection due to the mismatch of impedance of transmission lines. This reflection is the combination of adding and subtracting of travelling and reflected wave from each other, which causes the original signal to be distorted [59]. These reflections cause the receiver device to falsely interpret the logic levels. When the track width is increased during slot crossing, the capacitance of track (equation 4.10) is decreased and impedance of the transmission line during slot crossing is matched with that of the transmission line. The reflection effect of signal is minimized and SI is improved.

Figure 4.7 shows the impedance of the crossing track with respect to height; an increase in height leads to an increase in the characteristic impedance of the track. As the amount of signals reflected back depends on the magnitude of the change in the impedance, changing the track width from 8 mils to 18 mils during split plane crossing leads to a decrease in the impedance.

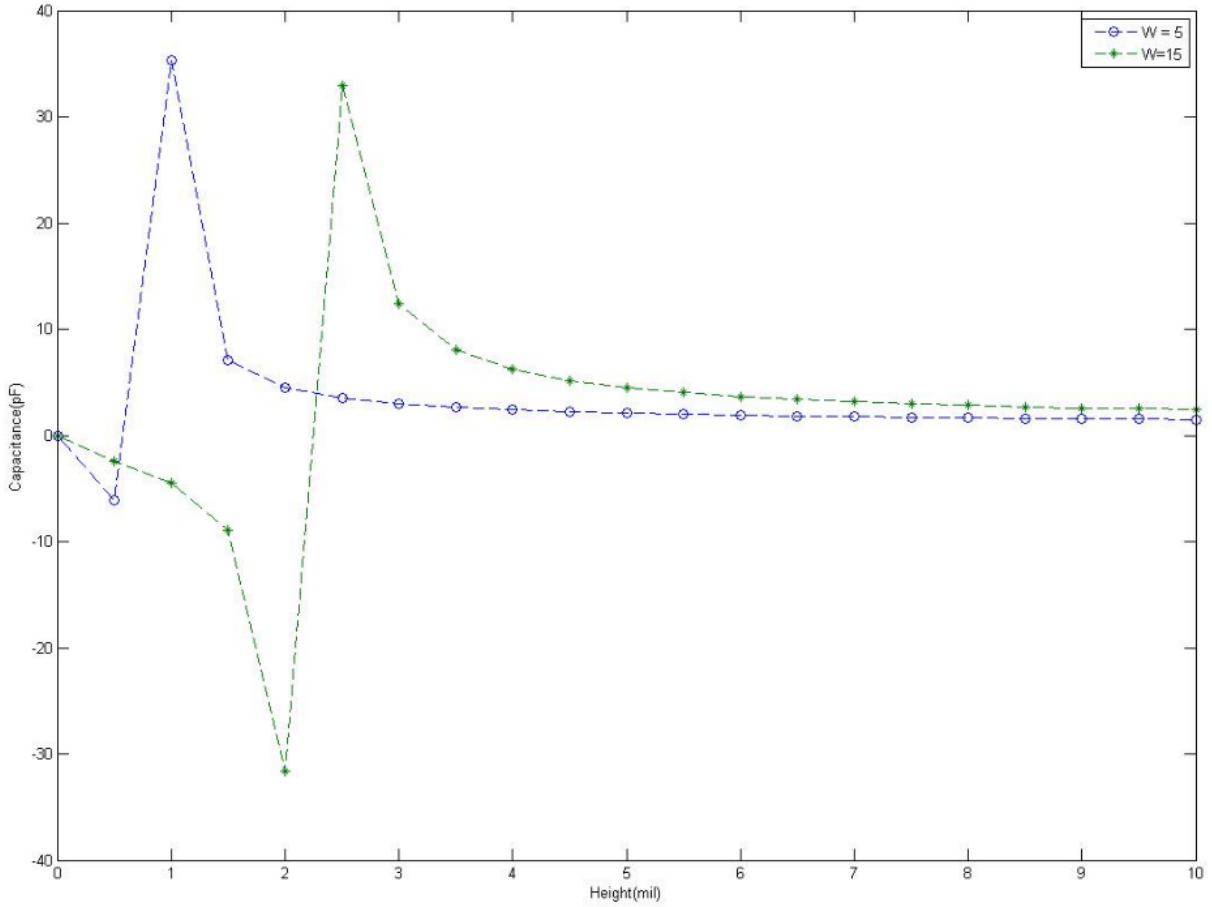


Figure 4.6: MatLab simulation result for track capacitance with respect to height during split plane crossing.

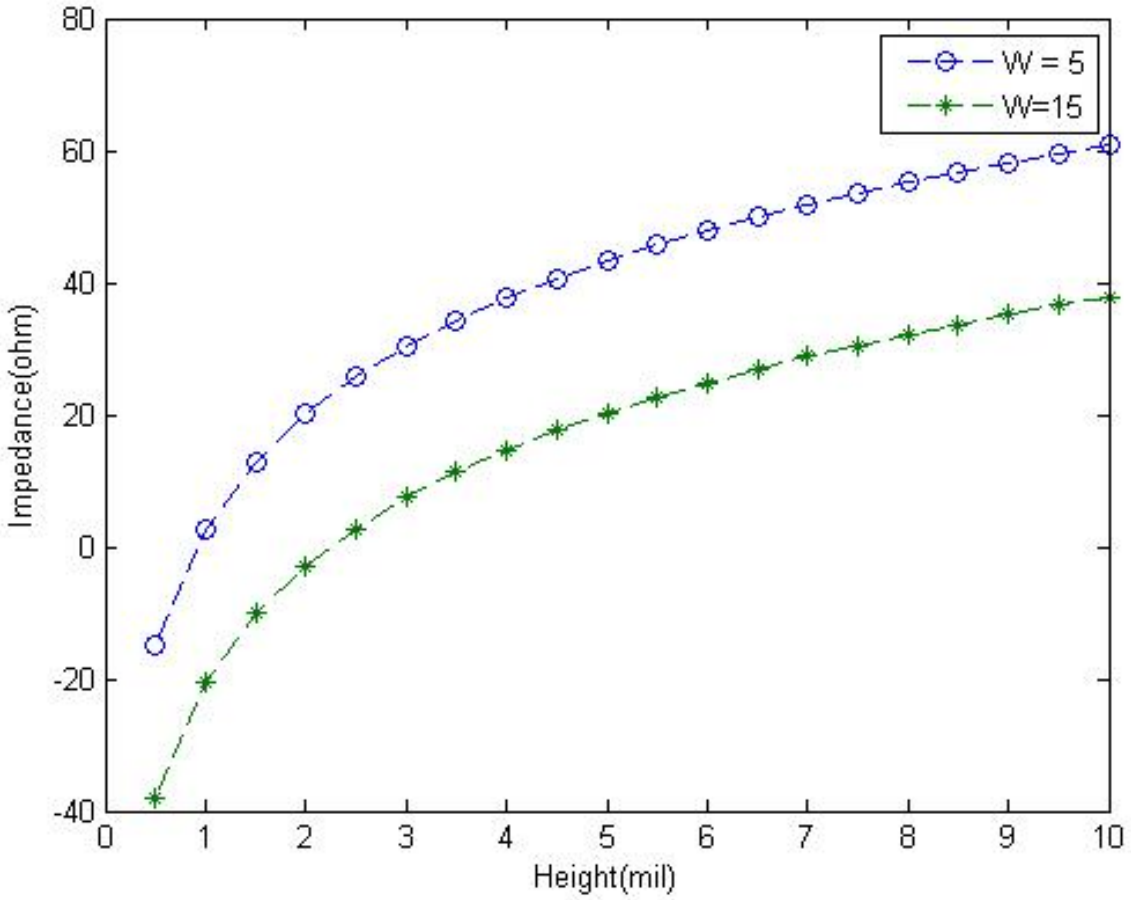


Figure 4.7: MatLab simulation result for track impedance with respect to height during split plane crossing.

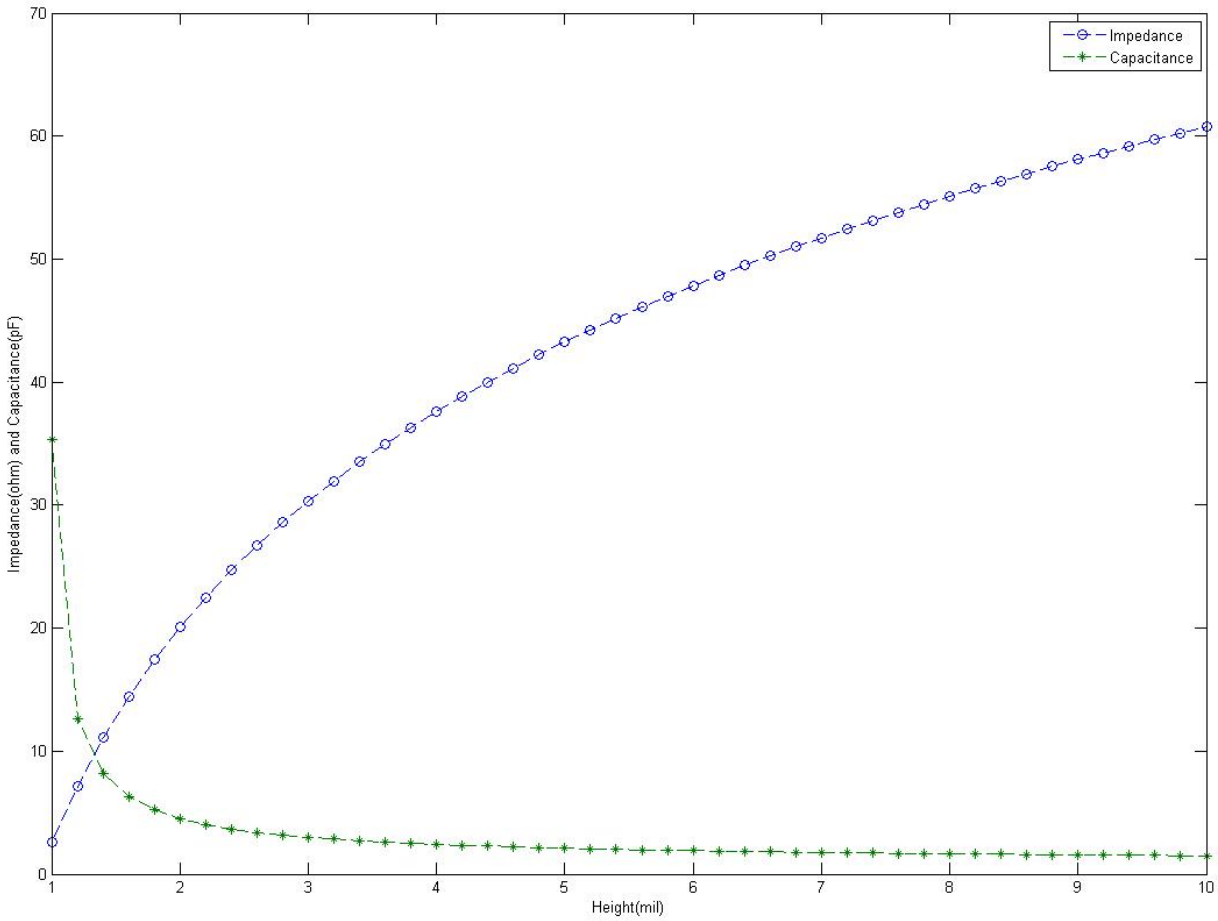
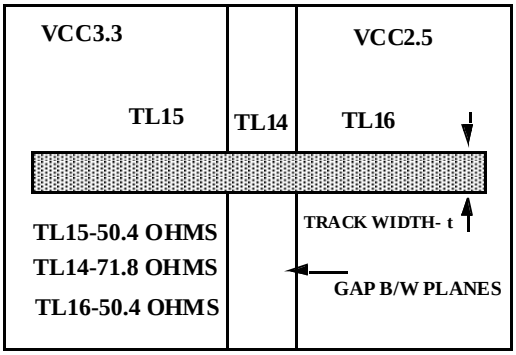


Figure 4.8: MatLab simulation result for track impedance and capacitance with respect to height during split plane crossing.

Figure 4.8 shows the impedance and capacitance of the crossing track with respect to height. When capacitance decreases, the characteristic impedance of track increases. The characteristic impedance of signal track is inversely proportional to the capacitance. In an un-balanced transmission line, the impedance is increased due to increase in the height with respect to the nearest reference plane. The characteristic impedance of the track can be controlled by increasing the track width during slot crossing. It results in a decrease in the track impedance and is matched with the rest of the transmission line. When high-speed current travels along the PCB track, an equal and opposite return current flows in the reference plane [60-61].

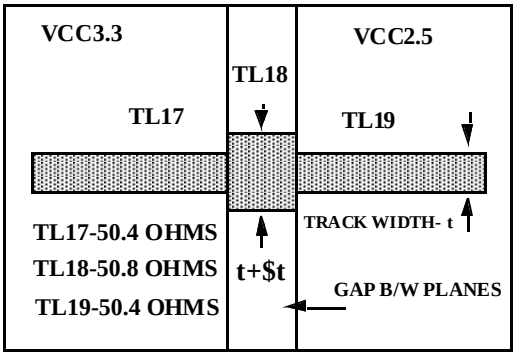
4.4 Proposed Impedance Control Methodology

An impedance control method is proposed to control the track impedance during crossing through the split gaps. Figure 4.9(a) shows the un-balanced transmission lines during the crossing of the slot gap and figure 4.9(b) shows the balanced transmission line by using the impedance control method. In figure 4, power plane layer is split into two planes, i.e., VCC3.3 and VCC2.5, which are isolated from each other by 50 mils gap.



Un-balanced transmission line , due to split plane

(a)



Balanced transmission line , track width is increased during crossing the gap

(b)

Figure 4.9(a): Un-Balanced (b) balanced transmission line during crossing through the split gap.

When the high frequency signal crosses the split gap, characteristic impedance changes. All high speed signals are controlled by impedance value. Generally, 50 Ω control impedance

transmission lines are used in the PCB applications. Here, 50 Ω control transmission lines are divided into three segments: TL15 having 50.4 Ω, TL14 with 71.8 Ω and TL16 with 50.4 Ω. The TL15, and TL16 transmission lines are crossing above a solid reference plane and the TL14 line is crossing over the second nearest reference plane instead of the first reference plane. TL14 transmission line track impedance is increased from 50.4 Ω to 71.8 Ω due to crossing of split gap, which indicates the moving of conductors further apart from the first plane. Thus, there is a decrease in capacitance and an increase in the characteristic impedance. During impedance discontinuities between TL15, and TL14 lines, some part of the signal is reflected back in the opposite direction and some of it continues to have different amplitude.

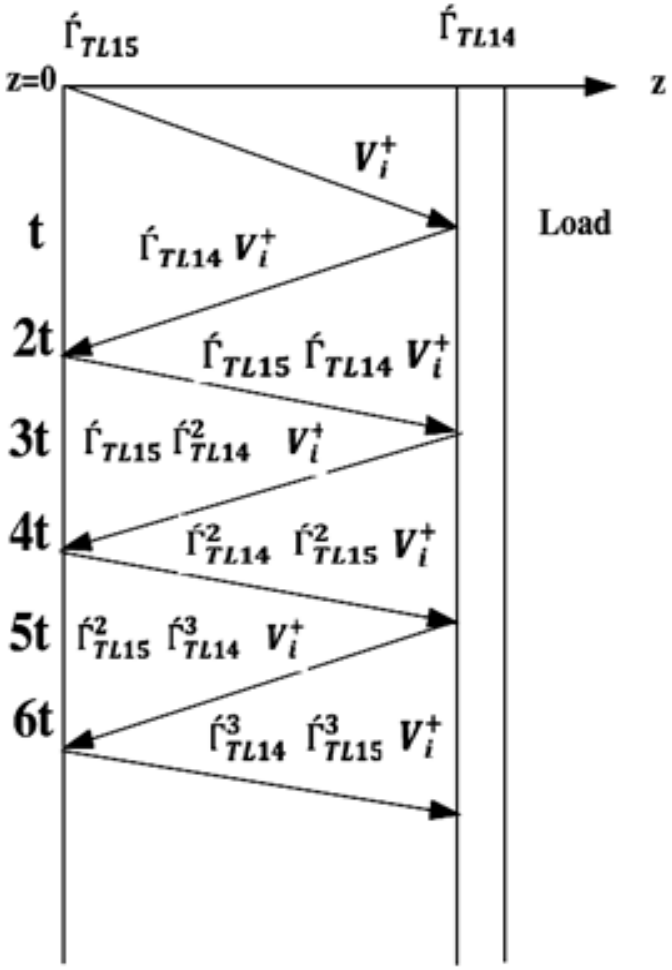


Figure 4.10: Bounce diagram for unbalanced transmission lines.

The bounce diagram is very helpful in the analysis of the reflection of signal of transmission line due to variations in the impedance. The bounce diagram shows [figure 4.10] the distance along the horizontal axis and time along the vertical axis. The lines in the diagonal form in the diagram represent the trailing edges of the signal. The sloping lines indicate signal traveling in the +z and –z directions. V_i^+represents the input voltage, and $\acute{\Gamma}_{TL14}$, $\acute{\Gamma}_{TL15}$are thereflection coefficientat the particular discontinuity. The reflection is due to impedance variation in the transmission line. The voltage amplitudes are calculated by multiplying the incident voltage by the reflection coefficient at TL14; transmission line side is the sum of all voltage intersecting in a vertical line.

$$V(Z_0, \infty) = V_i^+ + \acute{\Gamma}_{TL15}\acute{\Gamma}_{TL14}V_i^+ + \acute{\Gamma}_{TL15}\acute{\Gamma}_{TL15}\acute{\Gamma}_{TL14}\acute{\Gamma}_{TL14}V_i^+ + \ldots\ldots\ldots\ldots$$

$$V(Z_0, \infty) = V_i^+ \left(1 + \acute{\Gamma}_{TL14}\acute{\Gamma}_{TL15} + \acute{\Gamma}_{TL14}^2\acute{\Gamma}_{TL15}^2 + \ldots\ldots\ldots\right) \quad (4.12)$$

The voltage amplitude of transmission line on TL15 transmission line side is the sum of all voltages intersecting in vertical line.

$$V(Z_0, \infty) = V_i^+\acute{\Gamma}_{TL14} + \acute{\Gamma}_{TL15}\acute{\Gamma}_{TL14}^2V_i^+ + \acute{\Gamma}_{TL15}^2\acute{\Gamma}_{TL14}^3V_i^+ + \acute{\Gamma}_{TL15}^3\acute{\Gamma}_{TL14}^4V_i^+ + \ldots\ldots$$

$$V(Z_0, \infty) = V_i^+\acute{\Gamma}_{TL14}\left(1 + \acute{\Gamma}_{TL14}\acute{\Gamma}_{TL15} + \acute{\Gamma}_{TL14}^2\acute{\Gamma}_{TL15}^2 + \acute{\Gamma}_{TL14}^3\acute{\Gamma}_{TL15}^3\ldots\ldots\ldots\right) \quad (4.13)$$

Adding the infinite number of bounces, from equation (12) and (13)

$$V(Z_0, \infty) = V_i^+\left(1 + \acute{\Gamma}_{TL14}\acute{\Gamma}_{TL15} + \acute{\Gamma}_{TL14}^2\acute{\Gamma}_{TL15}^2 + ..\right) + V_i^+\acute{\Gamma}_{TL14}\left(1 + \acute{\Gamma}_{TL14}\acute{\Gamma}_{TL15} + \acute{\Gamma}_{TL14}^2\acute{\Gamma}_{TL15}^2 + \acute{\Gamma}_{TL14}^3\acute{\Gamma}_{TL15}^3\ldots\ldots\ldots\right) \quad (4.14)$$

By applying the geometric series on equation 14, $\sum_{k=0}^{\infty} Z^k = \frac{1}{1-Z}$, z<1

$$V(Z_0, \infty) = \frac{V_i^+}{1-\acute{\Gamma}_{TL14}\acute{\Gamma}_{TL15}} + \frac{V_i^+\acute{\Gamma}_{TL14}}{1-\acute{\Gamma}_{TL14}\acute{\Gamma}_{TL15}}$$

$$V(Z_0, \infty) = \frac{1+\acute{\Gamma}_{TL14}}{1-\acute{\Gamma}_{TL14}\acute{\Gamma}_{TL15}}V_i^+ \quad (4.15)$$

Equation (4.15) shows that the voltage variation is the combination of adding and subtracting of travelling and reflected wave due to impedance mismatch in the transmission line.

When track width is increased during slot crossing, the impedance of the TL14 line decreases due to increase in the capacitance of track.

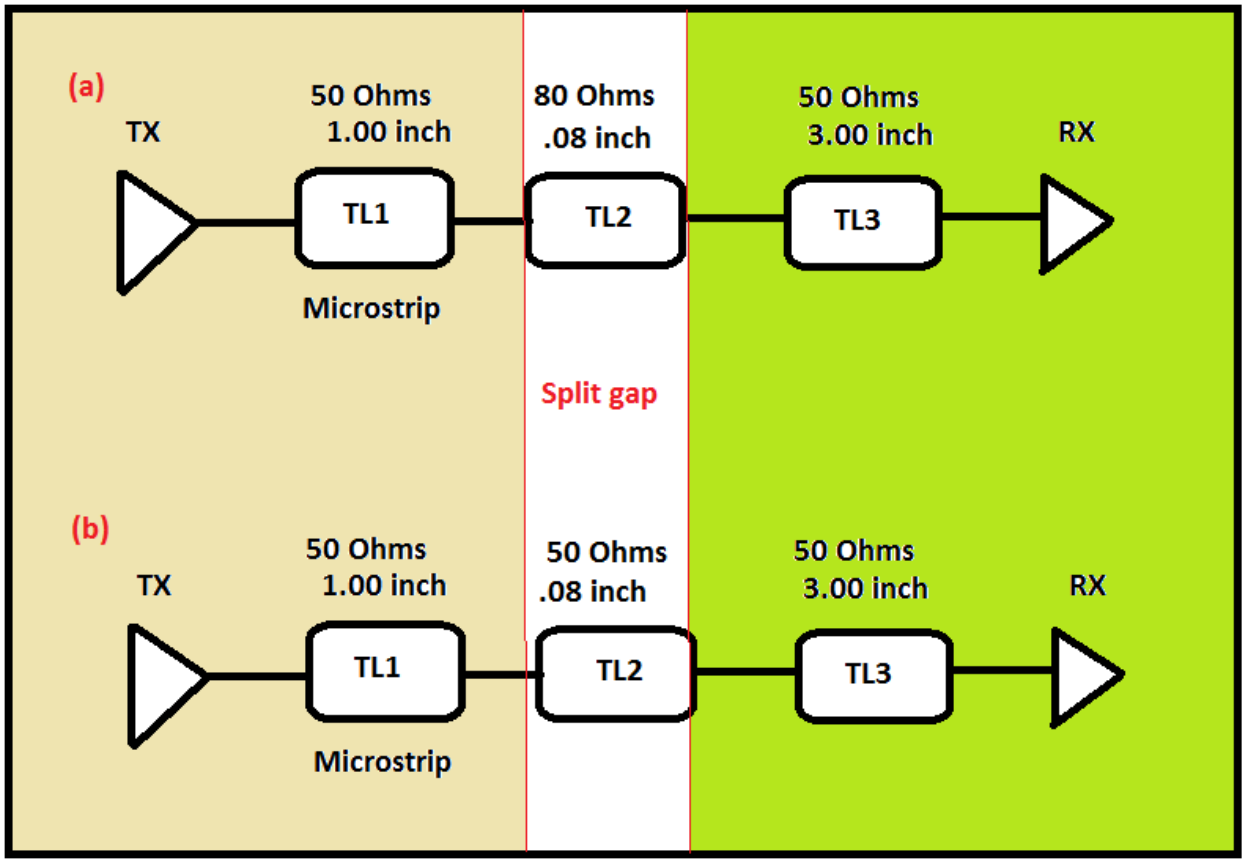
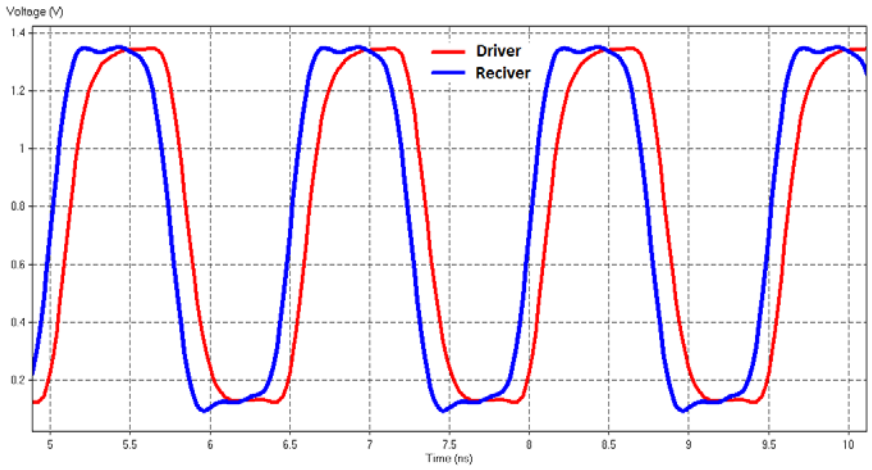


Figure 4.11(a): Un-balanced transmission line (b) Balanced transmission line

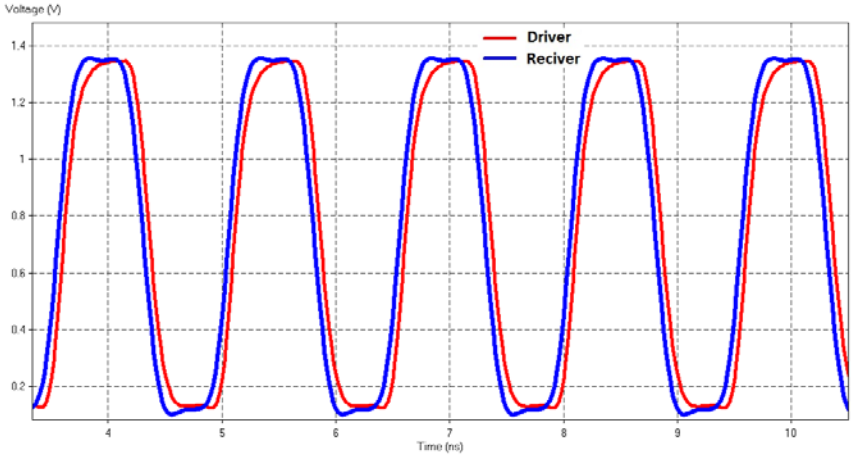
Figure 4.11(a) shows the un-balanced transmission line, when high speed track crossing the split plane gap. There are three transmission lines represented by TL1, TL2, and TL3. TX is the source driver and RX is the receiver driver. TL2 transmission line represents the high frequency signal that crosses the split plane gap. Virtex-4 IBS model is assigned to the input and output pins of the device. Figure 4.11(b) shows the balanced transmission line in a schematic editor. TL2 transmission line is balanced by increasing the track width during the crossing of the split gap. Capacitance is increased if thicker track crosses the split plane gap. In the present investigation, Virtex-4 IBS model has been used during simulation.

SI issues in biomedical equipment are very important when dealing with electronic designs with fast rising edges. With an increase in speed and reduced board size, the traditional design

methods are becoming inadequate. Figure 4.12(a) and 4.12(b) show the simulation results of the un-balanced and balanced transmission lines, shown in figure 4.11; the driver is shown in red and load in blue in figures 4.11(a) and 4.12(b).



(a)



(b)

Figure 4.12(a): Simulation results in HyperLynx software for un-balanced and 4.12(b) balanced transmission lines.

When the signal passes the gap, the track width remains the same but the plane height with respect to signal changes. The impedance of unbalanced transmission line increases from 50 Ω to 80 Ω. In the simulation result shown in figure 4.12(a), the wave shape degrades at the receiver

end because some signal is reflected back to the source. The wave shape degradation is with significant improvement on the received output signal shown in figure 4.12(b).

4.5 Impedance Control Method with Stitching Capacitor during Crossing the Slot Gap

The proposed solution for signal integrity degradations due to high-speed signals jumping cross a reference plane slot gap is to use a capacitor that bridges the slot, so that the signal's return current can mostly follow alongside the source current. In this section, a stitching capacitor is used to help guide the return current directly alongside the source current. Figure 4.13 highlights this kind of a situation.

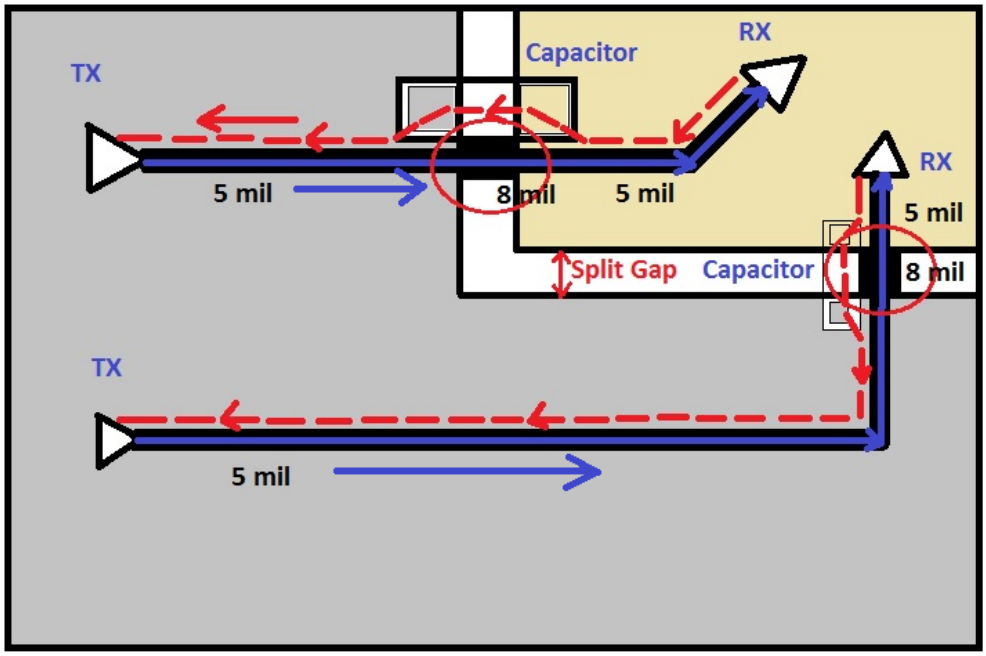


Figure 4.13: Two capacitors used to help guide the return currents alongside the source currents.

From figure 4.13, a 2.5 V power plane is AC coupled to a 1.8 V power plane through the use of two capacitors. By doing so, the return currents mostly propagate alongside their source currents. This tends to minimize the loop areas associated with those parts of the signal paths that cross the gap between the two power planes [45]. The slot gap between two planes islands is 80 mils. The track width of signal is increased during crossing the gap, so impedance of the trace remains unchanged. A 402 capacitor is used for guiding the return currents back to their sources. The placement of the capacitors across the cutout then adds a return path for the currents. Therefore,

the return current traverses these separate paths back to its source. The net effect of the reference plane cutout is to induce an inductive discontinuity along the propagation path [46].

4.6 Return Loss

Figure 4.14(a) shows the return loss when signal is crossing the split plane. The return loss is 14dB at 2 GHz. Return loss is increased when signal frequency is increased. The energy is spilt while crossing the slot gap and more signal is reflected back to the source. When using impedance control method along with capacitor during split plane crossing, the return loss is 19dB. It means return loss is improved by 5dB using the proposed method. It's a very significant value for any high speed medical system.

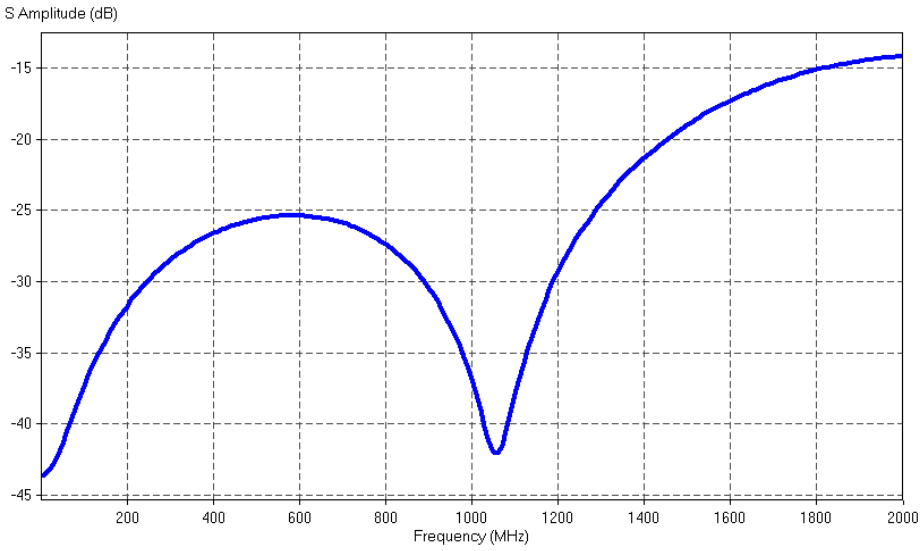


Figure 14.4(a) Return loss when signal crossing the split plane.

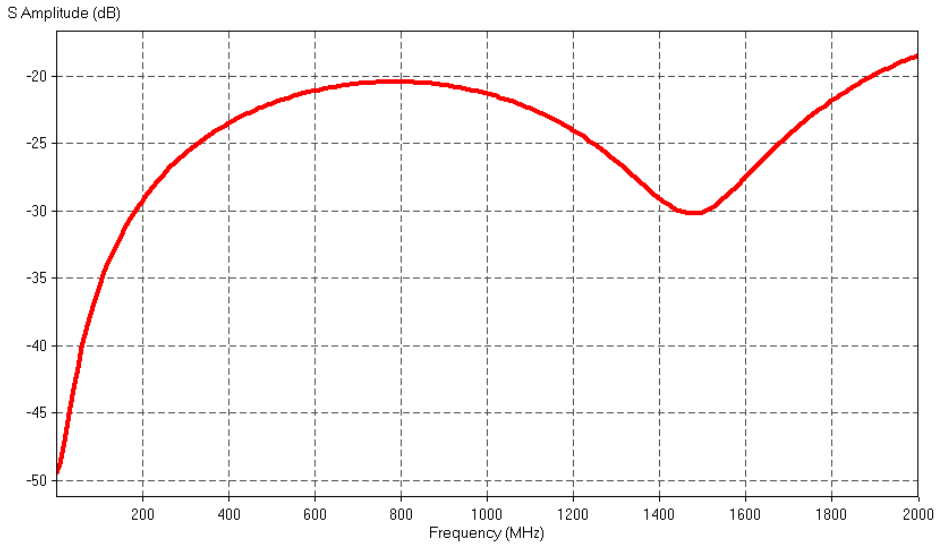


Figure 14.4(b) Return loss when signal crossing the split plane with proposed method.

4.7 Insertion Loss

Figure 14.5(a) shows the insertion loss, when signal crossing the split plane. The insertion loss is around 0.75dB at 2GHz. In figure 14.5(b), the insertion loss is 0.55dB at 2GHz, when impedance control method and stitching capacitor is used during split plane crossing. Insertion loss is improved by 0.2dB in the proposed method.

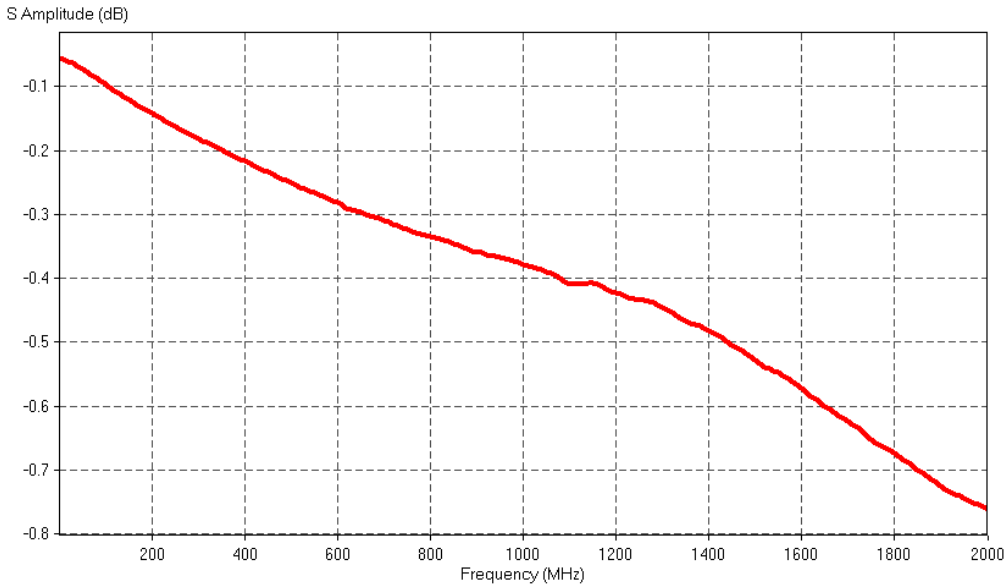


Figure14.5 (a) Insertion loss when signal crossing the split plane.

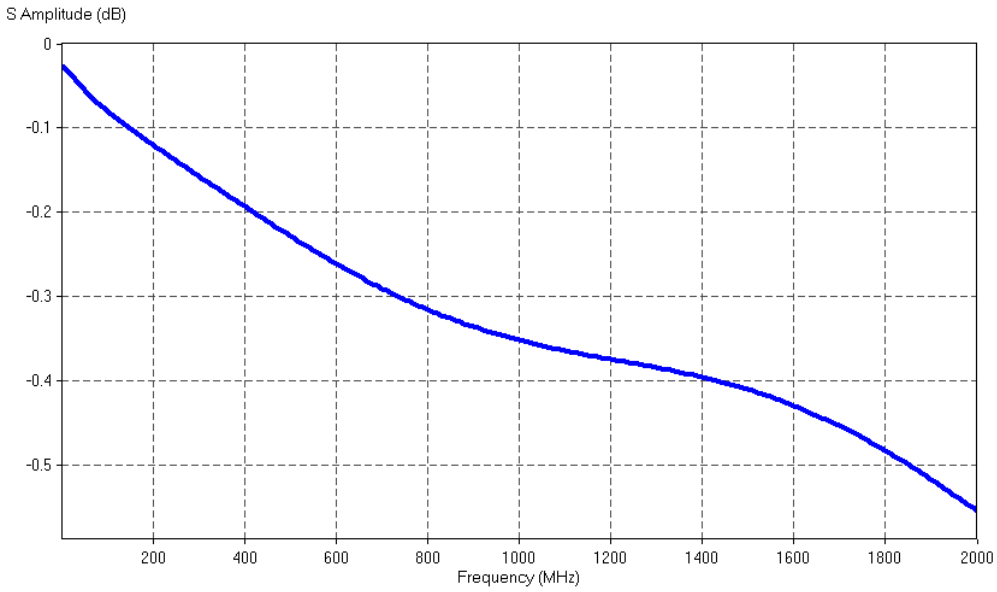
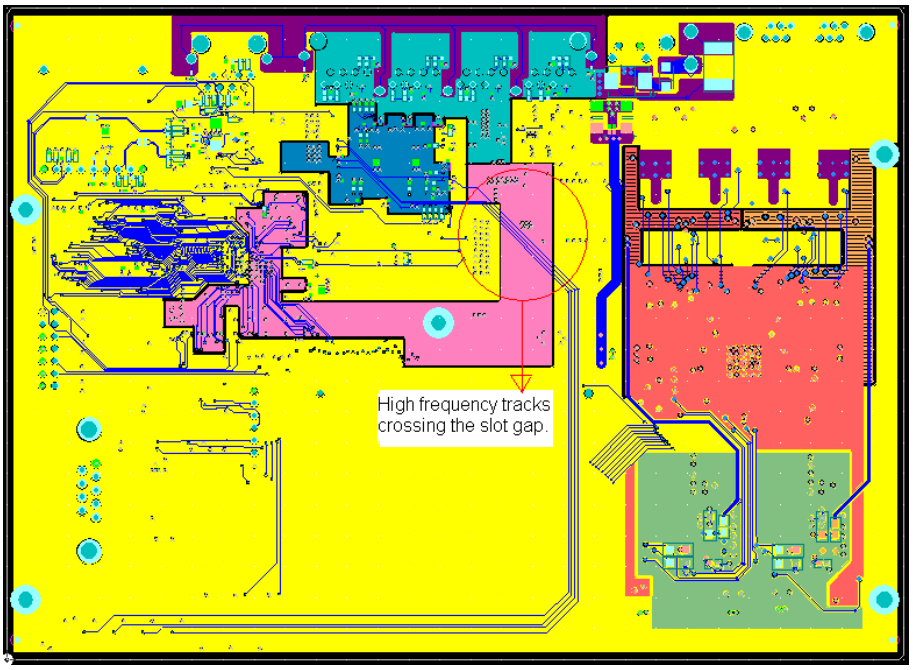


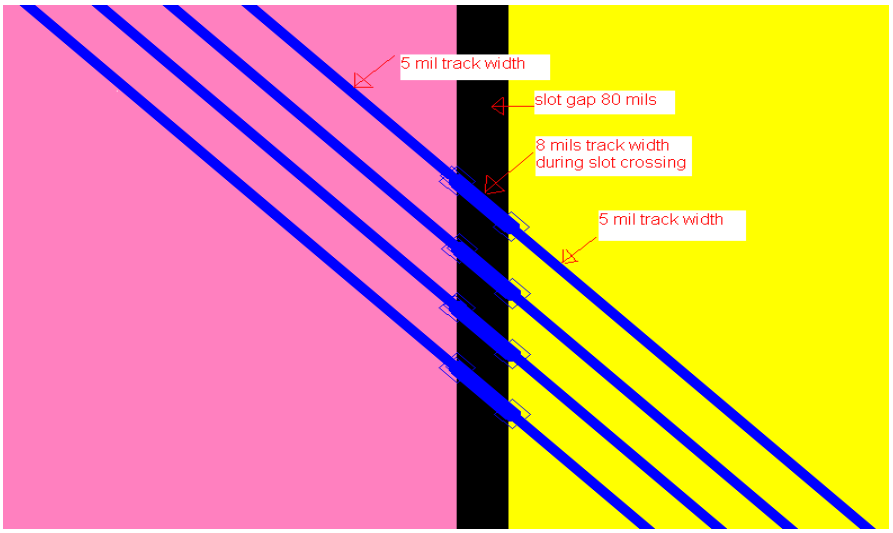
Figure 14.5(b) Insertion loss when signal crossing the split plane with proposed method.

4.8 Test Vehicle and Correlation with Hardware Results

A 4-layer PCB is used as the test vehicle to study the impact of split plane on return path discontinuity on SI, as shown in figure 4.16(a) and (b).The PCB layout of the board is used for fabrication of PCB with dimension of is 6 x 4 inch, the trace width is 5 mils, and slot gap size is 80 mils. The blue tracks are routed in bottom side as in figure 4.16(a).The third layer in the layout is a power layer which splits into many small islands. Each island is separated from each other by 80 mils gap. Many tracks are routed in the bottom side crossing the split gap. These tracks are 50 Ω control impedance tracks. The impedance of track is increased during slot crossing due to the change of reference plane. When track width is increased from 5 mils to 8 mils during slot crossing, as shown in figure 4.16(b), the impedance of track is decreased, which matches with the line.



(a)

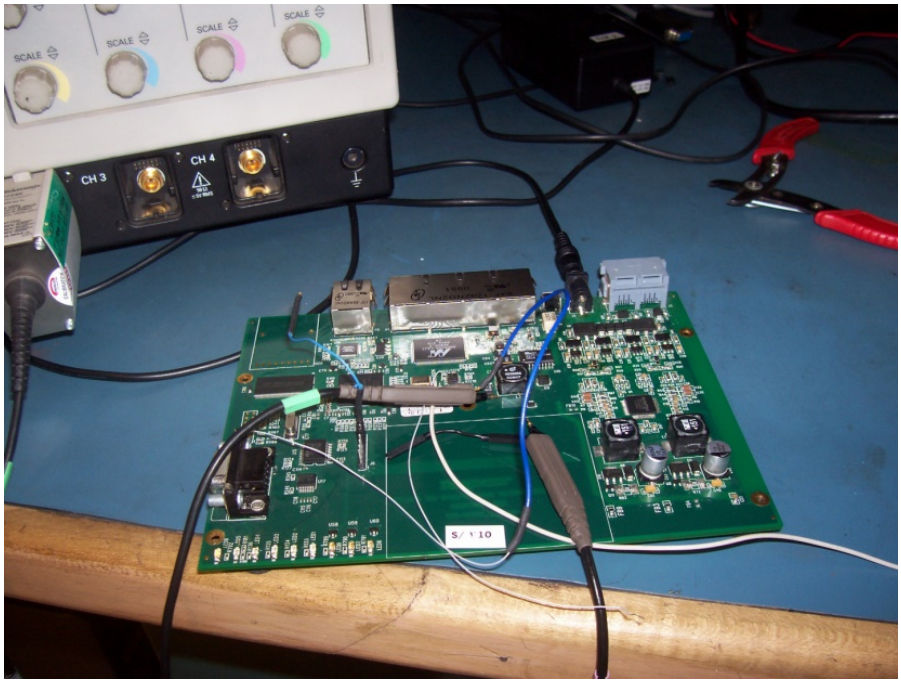


(b)

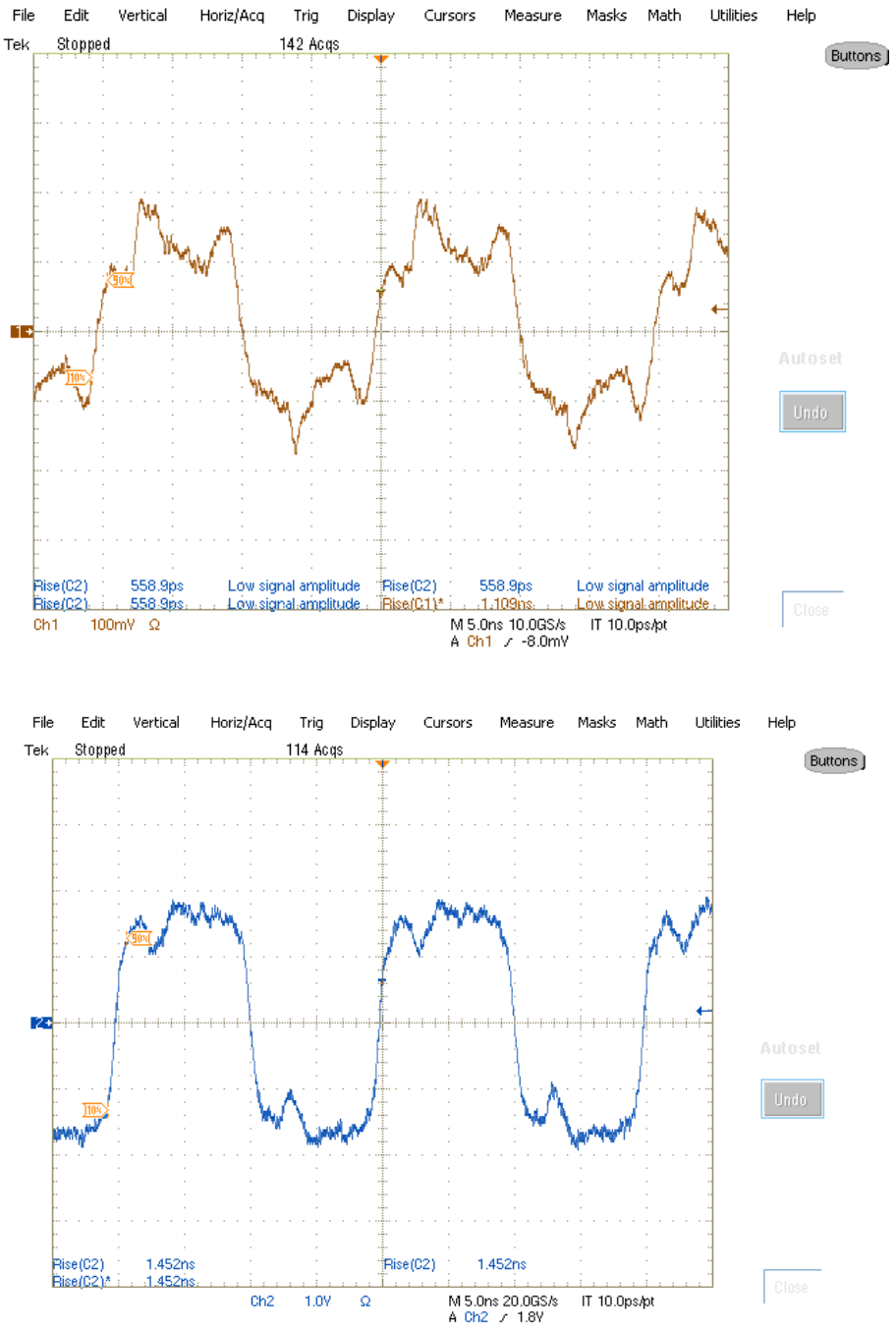
Figure 4.16(a): PCB layout which shows the slot crossing, 4.16(b) track width increased during slot crossing from 5 mils to 8 mils.

Figure 4.17(a) and (b) show the actual experimental setup on real PCB which is used for measurement and their results, respectively. Dual probes logic analyzer is used during

measurement the result. The brown color wave shape, showing the result for unbalanced line when tracks cross the split gap, is distorted due to discontinuity of impedance in transmission line and increase of undershoot, overshoot amplitude [47]. The blue color wave shape, showing result for balanced transmission line, achieved by increased track width during slot crossing. Blue color wave has lesser overshoots, undershoots amplitude and looks better.



(a)



(b)

Figure 4.17(a): Shows the experimental setup of real PCB which is used for measurement. 4.17(b), shows the measurement result, brown colour wave shape for unbalanced line and blue colour wave shape for balanced line.

4.9 Summary

When signal cross-over occurs between two different split planes, significant signal degradation happens on the received output signal due to change of impedance when signal crosses the split planes. The impedance control method is found to be very effective in minimizing the degradation of the received output signal by reducing the overshoot, undershoot, and ringing of the signal. The capacitance per unit length of the conductor decreases and impedance of the transmission line increases while crossing the split gap as demonstrated by equations 4.10 and 4.11 in the present study. When a high-speed signal on PCB crosses the split planes, the return-current path and the radiation of the signal increases due to an increase in the return loop inductance. To control the characteristic impedance of the conductor during split planes crossing, track width is increased in this study. Based on the simulation result, stitching capacitors can be placed along the traces, when they are crossing split planes, to help route return currents to mitigate signal integrity degradations on the high-speed propagating signal. The return and insertion loss in impedance control board are improved by a factor of 5 dB and .2dB, respectively, during split-plane crossing. Simulation results also show that track impedance matches the constant impedance transmission line while crossing the split gap thereby reducing the reflection of the signal.

In brief, the proposed methods solve two major SI problems. First, balancing the impedances of the traces from the transmitter to the receivers, including in areas where the traces are crossing the split plane, is facilitated. Secondly, it resolves the return current-path problem, which is a major cause of signal degradation.

CHAPTER 5

MODELING OF POWER PLANES FOR IMPROVING EMC

5.0 Introduction

All EMC problems begin and end with electronic circuitry. PCB itself injects switching noise on the board, which decreases the EMC performance of electronic equipment, especially sensitive equipment requiring high precision, such as medical instruments. EMC of any instrument is the ability of a product to coexist in its intended electromagnetic environment without causing or suffering functional degradation or damage.

EMC problems at the PCB level are always massive and complicated, which is more so in the case of medical instruments that are very sensitive to any noise, which changes the output of the instrument. A sudden change in the amount of current drawn by an active component on a PCB can cause a transient voltage on the power bus, which can be large enough to interfere with the normal operation of other components on the board. High-speed digital Integrated Circuits operate in frequency bands where passive components cannot be considered as ideal, and to the contrary, contain parasitic elements. The impedances being dependent on the frequency, the emission levels generated by voltage and current drops may not be compliant to the different EMC standards making it impossible to predict the compliance of a system. However, it is possible to reduce the risk by implementing rules and design techniques in most applications.

The signal integrity (SI) problems occur at the PCB level due to signal frequency increase in the PCB. Undesired electromagnetic emissions (EM) represent one of the most critical issues to be accounted for in electronic system design. The PCB sizes are getting smaller and smaller while the signal speed is increasing, which results in severe EMC problems. EM fields radiated by high speed signal traces can cause both narrow and broadband interference with nearby electronic equipment.

EMI is a major problem in modern electronic circuits, including and especially medical instrument that contain analog circuitry affected adversely by high frequency signals because of electrostatic discharge, power line disturbances, and ground plane bouncing. In order to reduce

the interference in any electronic system, either remove the source of the interference or protect the circuit being affected [62]. Although, the circuit may be working at the board level, it may be radiating noise to other parts of the circuit, causing problems at the system level. Emissions from any digital circuit are normally of higher frequency, which are coming from the harmonics produced by the high-frequency signals in PCB. The fast switching current flows in loops, which act as small antennas in the PCB, radiate magnetic fields known as differential-mode radiation.

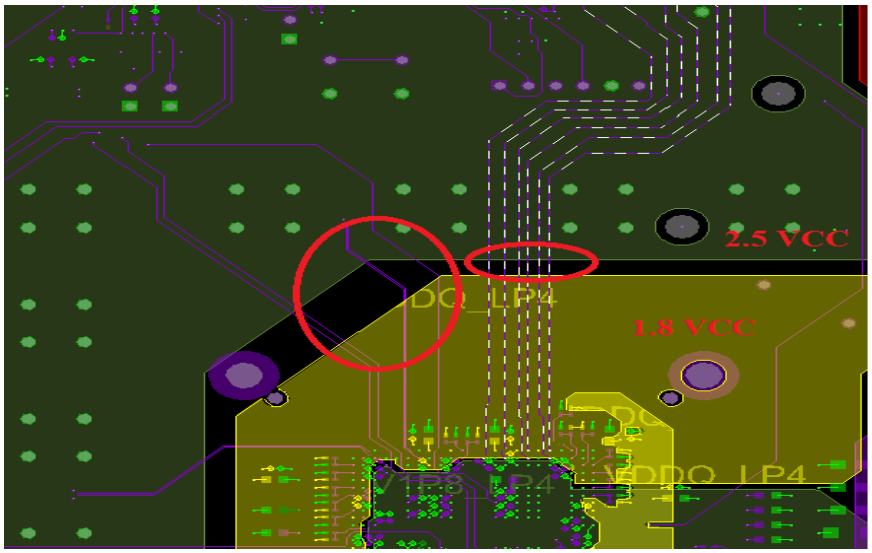


Figure 5.1: Discontinuities in the current return path when high speed traces crossing the split plane.

5.1 EMC

A major EMC problem occurs when there are discontinuities in the current return path as shown as figure 5.1. Some high speed traces are crossing the split plane, creating a discontinuity in the path on the PCB. These discontinuities cause the return current to flow in larger loops, which increases the radiation from the board, as well as, increases the crosstalk between adjacent traces and causes waveform distortion. EMC is grouped into two categories: internal and external [63].

3. Internal Category: The internal category is the result of signal degradation along a transmission path, including parasitic coupling between circuits in addition to field coupling between internal subassemblies, such as a power supply to a disk drive. Stated more specifically, the problems are of signal losses and reflections along the path, along with crosstalk between adjacent signal traces.

4. External Category: External problems are divided into emissions and immunity as shown in figure 5.2. Emissions derive primarily from harmonics of clocks or other periodic signals. Remedies concentrate on containing the periodic signal to as small an area as possible, blocking parasitic coupling paths to the outside world.

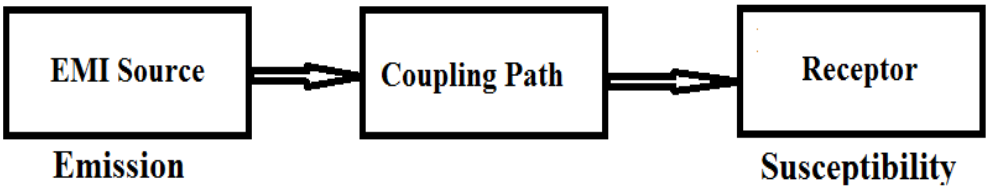


Figure 5.2 Cause of EMC on PCB: emission and susceptibility.

The “Source” – near / far field…high magnetic field or electric field

The “Path” – radiated or conducted

The “Receiver” – intentional or unintentional

Designing electronic products to meet EMC requirements is becoming more and more challenging. Faster clock speeds and lower operating voltages are leading to enhanced emissions via apertures and seams, from heat sinks as well as an increase in the susceptibility of products [64]. In addition, the trend towards integrating multiple wireless capabilities into products makes it necessary to also deal with the electromagnetic interference (EMI) effects of intentional radiators. These, and other, ever-increasing challenges are testing the limits of conventional EMC design methods [65]. The rules of thumb, best-practice techniques and experience that are commonly used during the design process often fail to work at higher frequencies. The result, in many cases, is that the design fails when tested. This leads to additional time and resources being spent on redesign and retesting [66]. The cost of a comparable design change typically increases by several orders of magnitude as the design moves through the development stages from concept to detailed and to validation. So, expensive, late-stage fixes are often the only option available when EMC problems are not discovered until the prototype phase. The need to change the design and re-test the product may also cause the product to be delivered late, which can reduce the revenues generated by the product over its lifecycle.

Traditionally, EMC problems have been found only near the end of the design cycle, after a prototype is built and can be taken to an EMC laboratory for measurements. The drawback to this approach is that: if problems are found, it's so late in the design cycle that fixes are very expensive. Clearly, if EMC problems could be identified and fixed before layout, significant savings would result. Finding problems early also avoids another aspect of the traditional approach to EMC: "band-aiding" a product by adding shielding and other expensive "kludges" rather than solving radiation problems at their source.

In this chapter, better EMC is achieved by using plane layers as an inbuilt capacitor in a multilayer PCB of medical devices. Boards with embedded capacitance utilize the natural capacitance between the powers and return planes to provide power-bus decoupling. By minimizing the spacing between the two solid planes and filling this space with a material that has high relative permittivity, the interplane capacitance can be greatly enhanced. Consequently, it is possible to eliminate most or all of the decoupling capacitors mounted on the surface of the board, freeing up valuable surface routing area, and improving product reliability.

5.2 Type of Radiation in Multilayer PCB

The traces on a PCB form unintended antennas that can generate electromagnetic radiation and cause EMC problems as shown in figure 5.3. Radiation is generated when currents flow in the trace antennas; the more and longer the current flows, the greater the risk of excess radiation being produced [67]. There are basically two ways to reduce the radiation generated by a net: diminish the effectiveness of the antenna that the trace forms, or reduce the current that flows in the antenna.

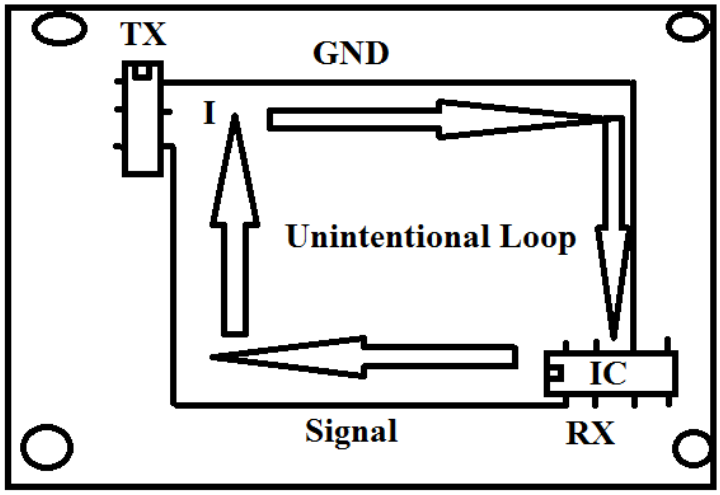


Figure 5.3 Electromagnetic radiation due to loop antenna on the PCB.

Radiation Type on PCB:

1. Differential mode radiation: Direct radiation from high speed signal traces.
2. Current driven radiation: The size of the real board is finite, a portion of the magnetic field due to a signal current wraps around the board and there is an effective voltage drop across the return plane. This voltage drop, can induce common-mode currents that drive various EMI antennas on the board. These EMI antennas could be cables, heat sinks or other metallic structures [68].
3. Voltage driven radiation: Any metallic structures that are at a different potential than other metallic structures may carry common mode currents and, in turn, create radiated emissions. At this time, the voltage driven radiation algorithm only estimates the radiated fields due to the high-frequency voltages induced on heatsinks in a shielding enclosure [69].
4. Radiation by I/O coupling algorithm: High frequency signals can couple to input/output (I/O) nets that carry the coupled energy away from the board. The common-mode currents induced on the cables attached to I/O nets can result in significant radiated emissions. Figure 5.4 shows emission mechanism of a signal net coupling noise to an I/O net, which then carries the noise off the board. If the signal net and the I/O net are separated by conducting planes, the coupling between the nets is not significant. There are two primary high-frequency trace-to-trace coupling mechanisms, capacitive and inductive coupling. Capacitive and inductive coupling are due to the electric and

magnetic fields, respectively. The noise voltages induced by both capacitive and inductive coupling are calculated for each I/O net [70]. But, only the maximum value is stored as the noise voltage used to estimate emissions. The total noise voltage driving an I/O net is calculated as the sum of the induced noise voltages on each segment of the I/O net.

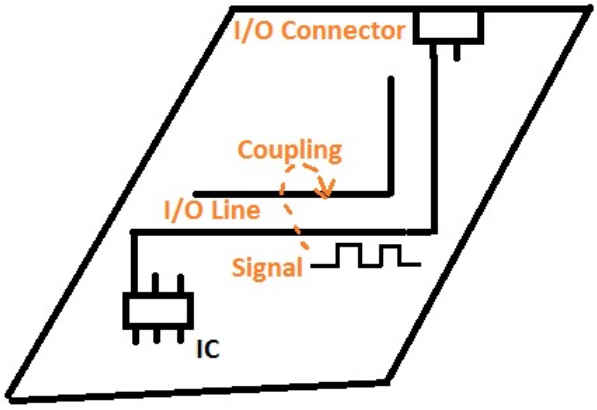


Figure 5.4: Signal net coupling noise to an I/O net.

5.3 Differential-mode Versus Common-mode Radiation

Differential-mode radiation from a PCB is caused by current flow in the unintended antennas formed by a board's traces as shows in figure 5.5. Traces that suffer from signal-integrity problems (e.g., ringing or long settling times) harbor excess currents and, therefore, generate excess radiation. Correcting these integrity problems can reduce a trace's radiated emissions at critical frequencies by as much as 20dB. Differential-mode radiation is generated when two equal- currents flow in opposite directions in close proximity to each other [71]. PCBs with ground/power planes, the current in a trace has exactly this configuration: as the current flows down the trace, an "image" current immediately above or below the trace returns to the driving source.

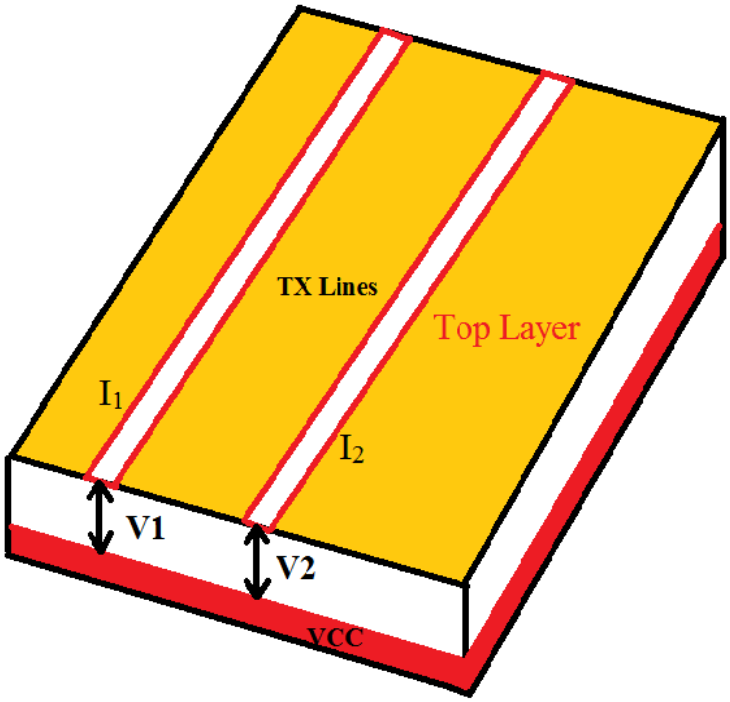


Figure 5.5: Differential and common mode radiation for high speed TX lines on multilayer PCB.

Even though the oppositely directed currents tend to cancel each other's radiation, the cancellation is not perfect because of the non-zero spatial and temporal (time) separation between them.

$$V_1 = Z_{11}\, I_1 + Z_{12}\, I_2 \qquad (5.1)$$

$$V_2 = Z_{21}\, I_1 + Z_{22}\, I_2 \qquad (5.2)$$

Both TX lines are symmetrical structure,

$$Z_{11} = Z_{22}$$

Odd mode, a negative current, $-I_1$ flow in second TX line

$$V_{odd} = \frac{1}{2}(V1 - V2)$$

$$= (Z_{11}-Z_{12})\, I_1$$

$$\frac{Vodd}{I1} = Z_{11}- Z_{12} = Z_{odd} \qquad (5.3)$$

Even mode, both TX lines flow same current, I_1

$$V_{even} = \frac{1}{2}(V1 + V2)$$

$$= (Z_{11}+Z_{12})\, I_1$$

$$\frac{Veven}{I1} = Z_{11} + Z_{12} = Z_{even} \qquad (5.4)$$

Differential mode impedance:

$$V_{diff} = 2\ Z_{odd}$$

Common mode impedance:

$$V_{comm} = \frac{Zeven}{2}$$

Common-mode radiation is generated when a current flows without a nearby current to oppose it [72]. Under these circumstances, the radiation generated can be much larger than typical differential-mode radiation. In real digital systems, common-mode currents tend to result from system-level conditions; *e.g.*, poorly designed cables (without adequate ground returns) or compromised/missing ground planes (one classic way of "compromising" a ground plane is to cut it and allow signals to pass over the cut.) Double-sided PCBs (boards with no ground planes) produce inherently non-differential radiation, because no pathways are provided for tight differential-mode return currents.

5.4 Far-Field versus Near-Field Radiation

The radiation generated by a PCB trace is complex. Near the trace, the electric field includes a radial (outward-directed) component; further away, the E-field's radial component diminishes [73]. EMC labs typically take measurements designed to measure far-field radiation: the sensing antenna is located 3, 10 or 30 meters away from the PCB under test, so that (except for at the lowest frequencies), only far-field radiation is sampled.

In figure 5.6 the near E-field of high speed interconnect on the PCB is shown. The maximum E-field near the high frequency traces is 1.189 dB V/m.

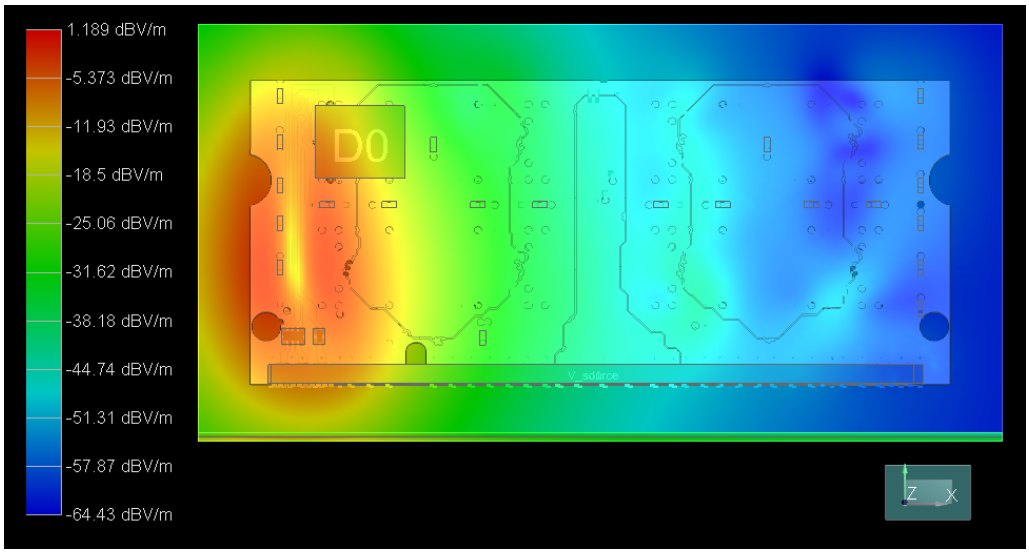


Figure 5.6: Simulation result of E-field of high speed interconnect on the PCB.

5.5 Radiation from Periodic Versus Random Signals

The data content of a digital signal greatly affects the way in which it radiates. Periodic signals (like clocks or regularly repeating control signals like RAS or CAS) have their energy "bunched" into tight peaks with large amplitudes. Random signals (like a data line) have their energy spread broadly and tend to have no peaks. Therefore, except in unusual cases, it is the periodic signals on a PCB that cause radiated-emissions failures.

5.6 Government EMC Regulations

Ultimately, designers are forced to be concerned about EMC and a radiated emission is that governmental bodies throughout the world require that electronic products not generate excessive amounts of radiation. EMC standards vary from country to country. The most important sets of regulations are FCC (applicable in the United States), CISPR (throughout European Community) and VCCI (Japan). Other, similar regulations apply in other markets. If a product generates radiation in excess of one of these standards, it may not be allowed for sale in the target market.

Within each standard, distinctions are made between two classes of products: "Class A" for industrial products, and "Class B" for commercial (or consumer) products. The standards are more-stringent for commercial products. Two most unavoidable types of board radiation: the

differential-mode radiation that comes from signal traces traveling over ground and power planes, and the radiation that is generated by component packages.

5.7 Power Plane Modeling

Multilayer PCBs have a power and ground plane distributed network to enhance the overall performance of system operation. The plane layers provide a low impedance path. A low impedance path allows the minimum amount of voltage drop across the power supply of components. If an imbalance exists within the power distribution network, the common mode RF energy is developed [74]. The physical relationships of plane layers separated by a dielectric core create a large capacitor as shown in figure 5.7. Depending on the thickness of the core material and the dielectric constant in layer stack up, various values of interplane capacitances are created. By taking advantage of the interplane capacitance between the power and the ground planes of a PCB, EMC of the system is improved.

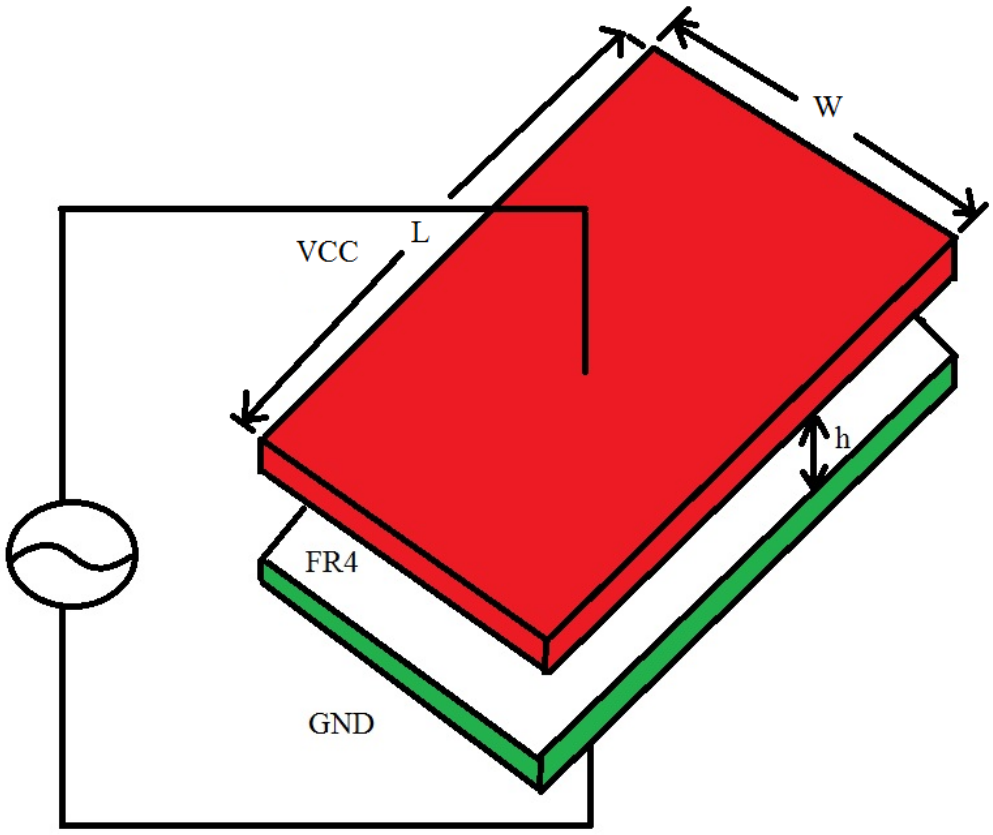
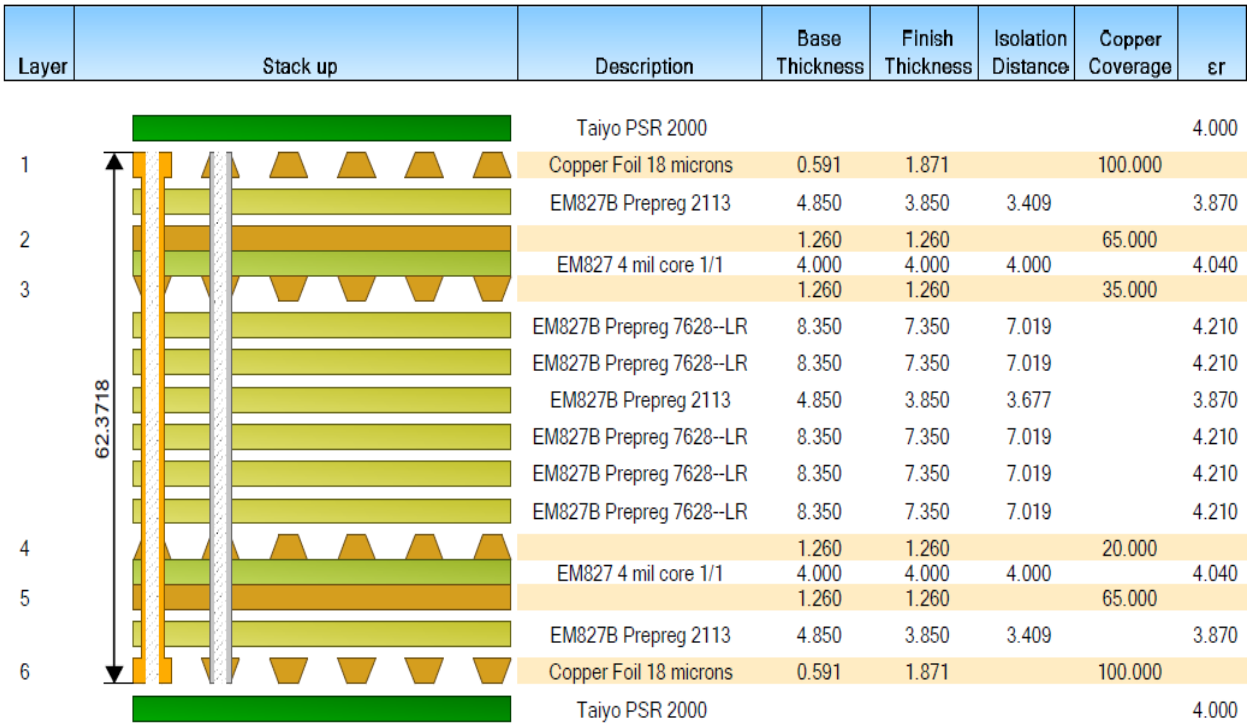


Figure 5.7: Parallel plate capacitance on the PCB

The increase in interplane capacitance is achieved either by reducing the layer spacing or by increasing the dielectric constant of the PCB material. The value of PCB capacitance is estimated by$C = \frac{\varepsilon A}{h}$, where ε is the dielectric constant, h is the spacing of the planes and A the effective area of the planes. Dielectric thickness is a critical parameter. Multilayer PCBs have multiple sets of plane layers. The complete layer stack up of a 6 layer PCB with dielectric thickness is indicated in figure 5.8.



Layer	Stack up	Description	Base Thickness	Finish Thickness	Isolation Distance	Copper Coverage	εr
		Taiyo PSR 2000					4.000
1		Copper Foil 18 microns	0.591	1.871		100.000	
		EM827B Prepreg 2113	4.850	3.850	3.409		3.870
2			1.260	1.260		65.000	
		EM827 4 mil core 1/1	4.000	4.000	4.000		4.040
3			1.260	1.260		35.000	
		EM827B Prepreg 7628--LR	8.350	7.350	7.019		4.210
		EM827B Prepreg 7628--LR	8.350	7.350	7.019		4.210
		EM827B Prepreg 2113	4.850	3.850	3.677		3.870
		EM827B Prepreg 7628--LR	8.350	7.350	7.019		4.210
		EM827B Prepreg 7628--LR	8.350	7.350	7.019		4.210
		EM827B Prepreg 7628--LR	8.350	7.350	7.019		4.210
4			1.260	1.260		20.000	
		EM827 4 mil core 1/1	4.000	4.000	4.000		4.040
5			1.260	1.260		65.000	
		EM827B Prepreg 2113	4.850	3.850	3.409		3.870
6		Copper Foil 18 microns	0.591	1.871		100.000	
		Taiyo PSR 2000					4.000

Figure 5.8: 6 layer PCB stackup.

5.8 Power-Bus Input Impedance

Power bus in an embedded capacitance board is designed to have low impedance at high frequencies may be a few ohms or less, the active components look like relatively high impedance sources due to their connection inductance. Therefore, the power-bus voltage at one location due to the current drawn by a component at another location is approximately proportional to the transfer impedance between these two locations. At frequencies where the board is electrically small, the power-bus transfer impedance is equal to the power-bus input impedance. At higher frequencies, the transfer impedance depends on the location of the source

and measurement ports. However, input impedance measurements over a broad frequency range still provide a good indication of the relative ability of the power bus to minimize noise.

5.9 Target Impedance of Plane

The characteristic impedance of the plane layer is calculated by using the equation, $Z_0 = \frac{1}{2\pi f C}$. The characteristic impedance depends upon the interplane capacitance between the ground and the power layers. The interplane capacitance also depends upon the core thickness between the power plane layers. Figure 5.9 shows that the impedance of the power plane layer decreases with the increase in the signal frequency at different dielectric thickness values, i.e. 5 mil, 10 mil, and 50 mil. In a normal 4 layer stack up, plane impedance is higher than the proposed layer stack up PCB.

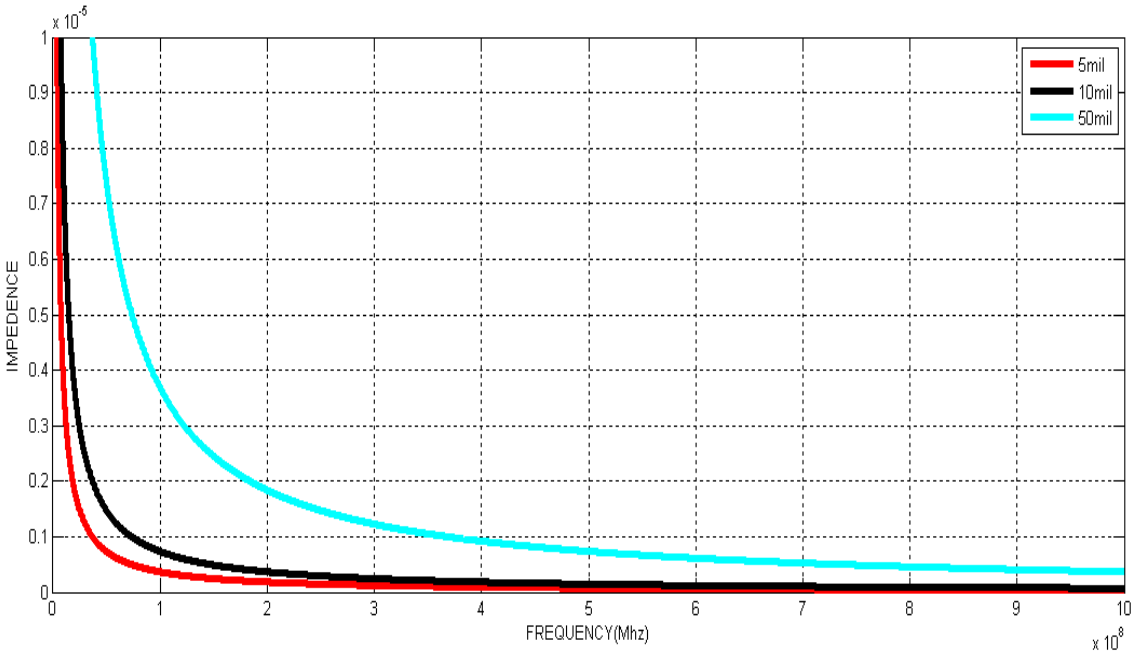


Figure 5.9: Impedance of power plane layer change with frequency.

Power distribution network (PDN) has a capacitive behavior at low frequencies and shows inductive behavior as we move towards the higher frequency range. However, this inductive trend is punctuated with a number of discrete resonances and anti-resonances. As far as a driver on-chip is concerned, the PDN must appear to be an ideal AC ground between its power and

ground terminals. Therefore, the inductance of the PDN must be reduced to enable easy flow of charge to the required active circuits to mitigate the noise. The target impedance of the PDN is decided based on the core voltage and average current drawn by the processor. Based on the equations for voltage drop across the power supply impedance, it is possible to define a maximum allowed ripple. In practice, the maximum allowed ripple is assumed to be 5% of the power supply. Voltage, Vdd.

$$Z_{target} = \frac{Vdd\ X\ 5\ \%}{Id\ X\ 50\%}$$

The current term in the denominator is ½ the switching current in a clock cycle, which is assumed to be the current in each clock edge. Decreasing supply voltages coupled with increasing power requirements tends to place stringent requirements on the target impedance of the digital part.

5.10 Description of the Test Vehicle

Two different 4 layer stack up boards, the conventional FR-4 and embedded capacitance boards respectively, have been analyzed for SI, and EMC performance. The active circuit on each board is the same clock circuits, which are the clock circuits with the frequency 100 MHz and 188 MHz respectively. Figure 5.10 shows a conventional FR4 board, 4 layer stack up, 5 inch x 4 inch PCB with 64 mil board thickness which is used in most of the medical products.

	Subclass Name	Type	Material	Thickness (MIL)	Dielectric Constant	Loss Tangent
1		SURFACE	AIR		1	0
2	TOP	CONDUCTOR	COPPER	0.5	4.5	0
3		DIELECTRIC	FR-4	4	4.5	0.035
4	GND	PLANE	COPPER	2	4.5	0.035
5		DIELECTRIC	FR-4	47	4.5	0.035
6	PWR	PLANE	COPPER	2	4.5	0.035
7		DIELECTRIC	FR-4	4	4.5	0.035
8	BOTTOM	CONDUCTOR	COPPER	0.5	4.5	0
9		SURFACE	AIR		1	0

Figure 5.10: Conventional 4 layer stack up with 63 mil board finishing.

Core layer thickness between inner plane layer 2 and 3 is 47 mil. In conventional FR4 board, plane coupling is very weak due to thick dielectric core layer between the plane layers. Effectively, the plane capacitance value is very small between the plane layers. Figure 5.11 shows the proposed embedded capacitance board, the inter layer capacitance is increased by changing the PCB thickness of 62 mil to 30 mil. The dielectric core thickness, 2 mils, is also decreased between the plane layers. Figure 5.12 and figure 5.13 shown the test board layout and 3D view of the test board respectively.

	Subclass Name	Type	Material	Thickness (MIL)	Dielectric Constant
1		SURFACE	AIR		1
2	TOP	CONDUCTOR	COPPER	1	4.5
3		DIELECTRIC	FR-4	10	4.5
4	GND	PLANE	COPPER	2	4.5
5		DIELECTRIC	FR-4	2	4.5
6	PWR	PLANE	COPPER	2	4.5
7		DIELECTRIC	FR-4	10	4.5
8	BOTTOM	CONDUCTOR	COPPER	1	4.5
9		SURFACE	AIR		1

Figure 5.11 Proposed 4 layer stack up with 30 mil finishing board.

Adjacent pairs of ground and power plane layers in a PCB's layer stack up provide an intrinsic, distributed capacitance that still behaves like a capacitor up to GHz range.

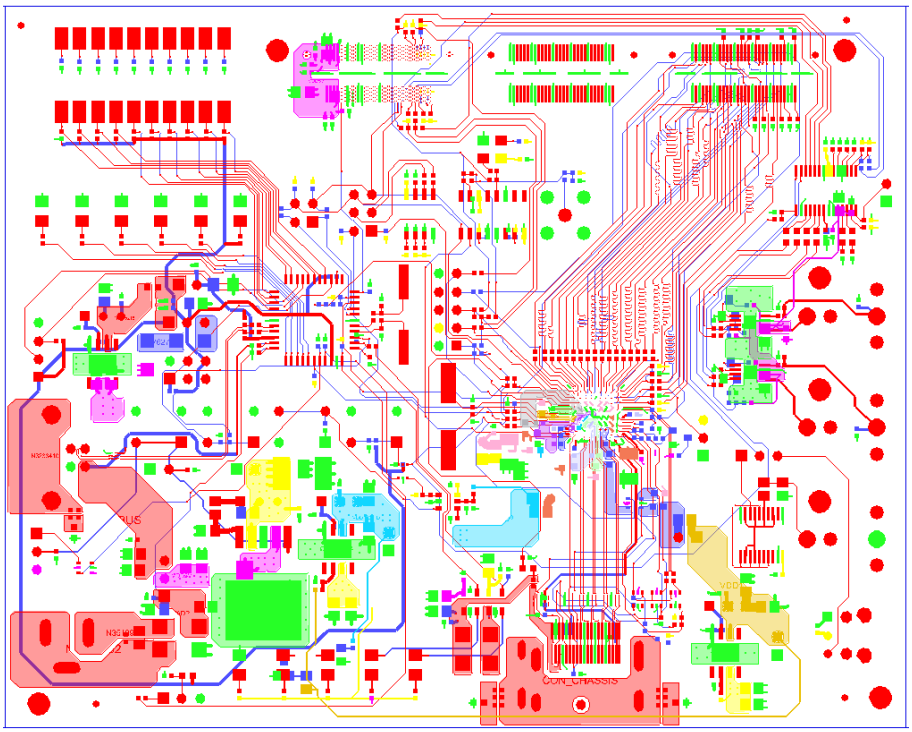


Figure 5.12: Layout of test board.

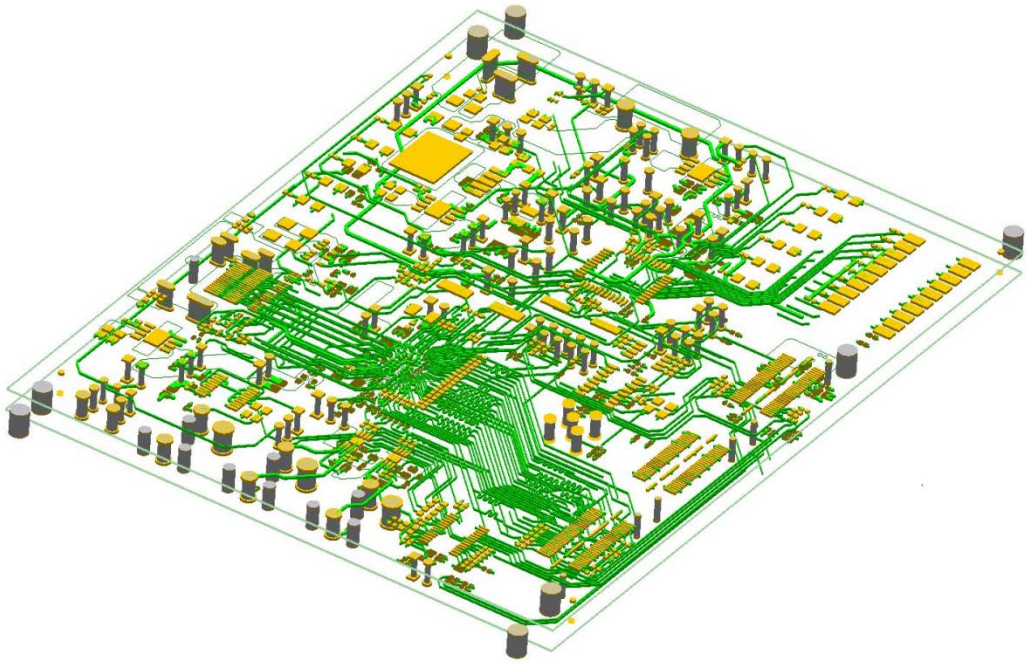


Figure 5.13: 3D views of the test board.

5.11 Simulation of the Embedded Capacitance and the Conventional Board

5.11.1 Comparison of the Impedance of the Embedded Capacitance and the conventional boards

The impedance comparing curves of the embedded capacitance and the conventional boards are shown in figure 5.14. The red curve represents embedded capacitor board and purple curve conventional FR4 board. The impedance of the embedded capacitors board is less than that of the conventional board within 100 MHz ~ 2 GHz. The impedance difference is very obvious when the frequency is higher than 1GHz. In addition, the inhibition of the board-level resonance by the embedded capacitors is obviously better than that of the conventional capacitors from the impedance curves.

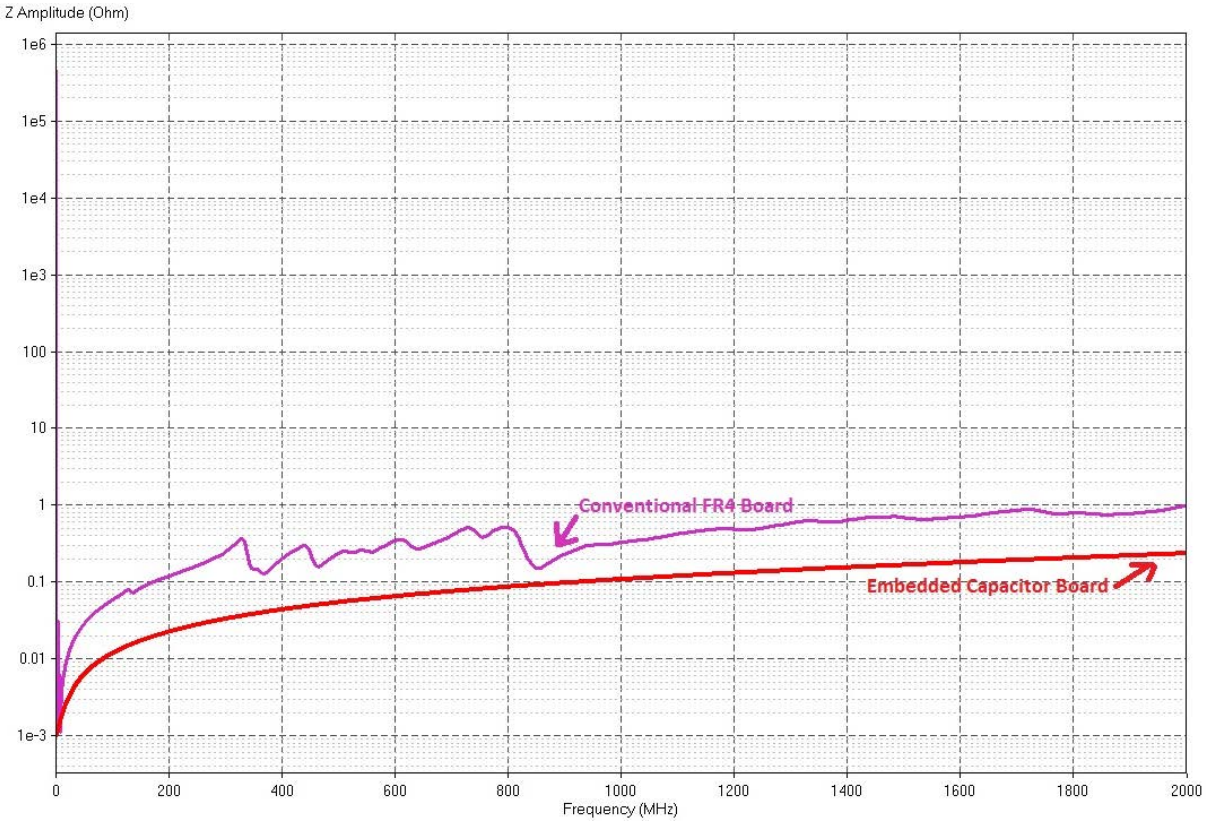


Figure 5.14: Comparison of impedance curves between the embedded capacitors and the conventional board.

5.11.2Comparison of the Power Noise simulation of the Embedded Capacitance and the conventional boards

Comparison of the power ripple noise testing results is shown in figure 5.15(a) and 5.15(b). It is visually clear that the power ripple noise of the conventional board is 183.65 mV peak to peak while that of the proposed structure board is only 28.24 mV. The power ripple noise of the conventional FR-4 board is much higher than that of the proposed structure board. This trend is consistent with the impedance simulation results.

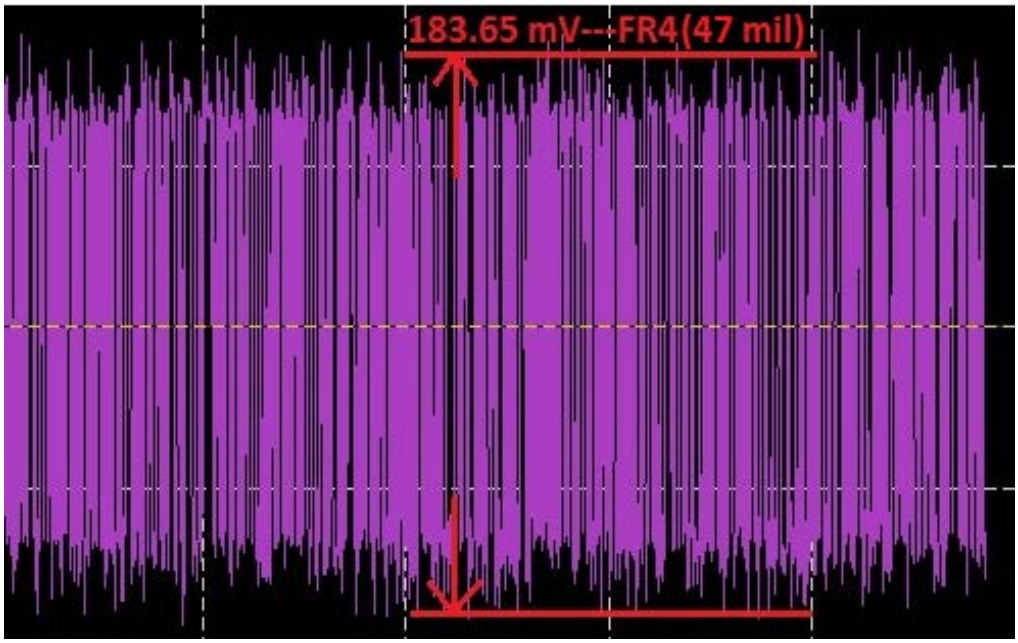


Figure 5.15(a): The power ripple noise in the conventional board.

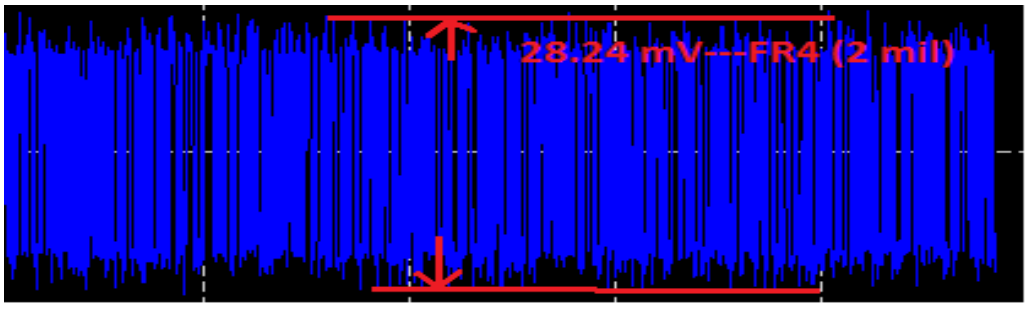


Figure 5.15(b): The power ripple noise in the proposed structure board.

5.11.3 Comparison of the Radiation Emission of the Embedded Capacitance and the conventional boards

EMC simulation of the embedded capacitance and the conventional boards within 100 MHz ~ 2 GHz was analyzed at the same frequency noise excitation. The results of the 3m, field radiated emission are shown in figure 5.16(a) and 5.17(b).

Figure 5.16(a) and 5.16(b) shows the radiation and electric and magnetic field pattern of the conventional board respectively. Figure 5.17(a) and 5.17(b) shows the radiation and electric and magnetic field pattern of the proposed 4 layer stack up boards. In figure 5.16(a) harmonic at 500 MHz, 750 MHz, and 1 GHz frequency is above 50 dB. When the dielectric thickness between power and ground plane is 47 mil, the interplane capacitance is small across plane layers. This layer stack up is less effective for EMC products. Figure 5.17(a) shows that when dielectric core thickness is 3 mil between the plane layers, the harmonic is reduced at the rate of 15 dB to 25 dB. Plane capacitor is directly proportional to the dielectric core thickness between power plane layers. These figures show that the result of the embedded capacitance board is obviously better than that of the conventional FR-4 board within 100MHz ~ 2GHz.

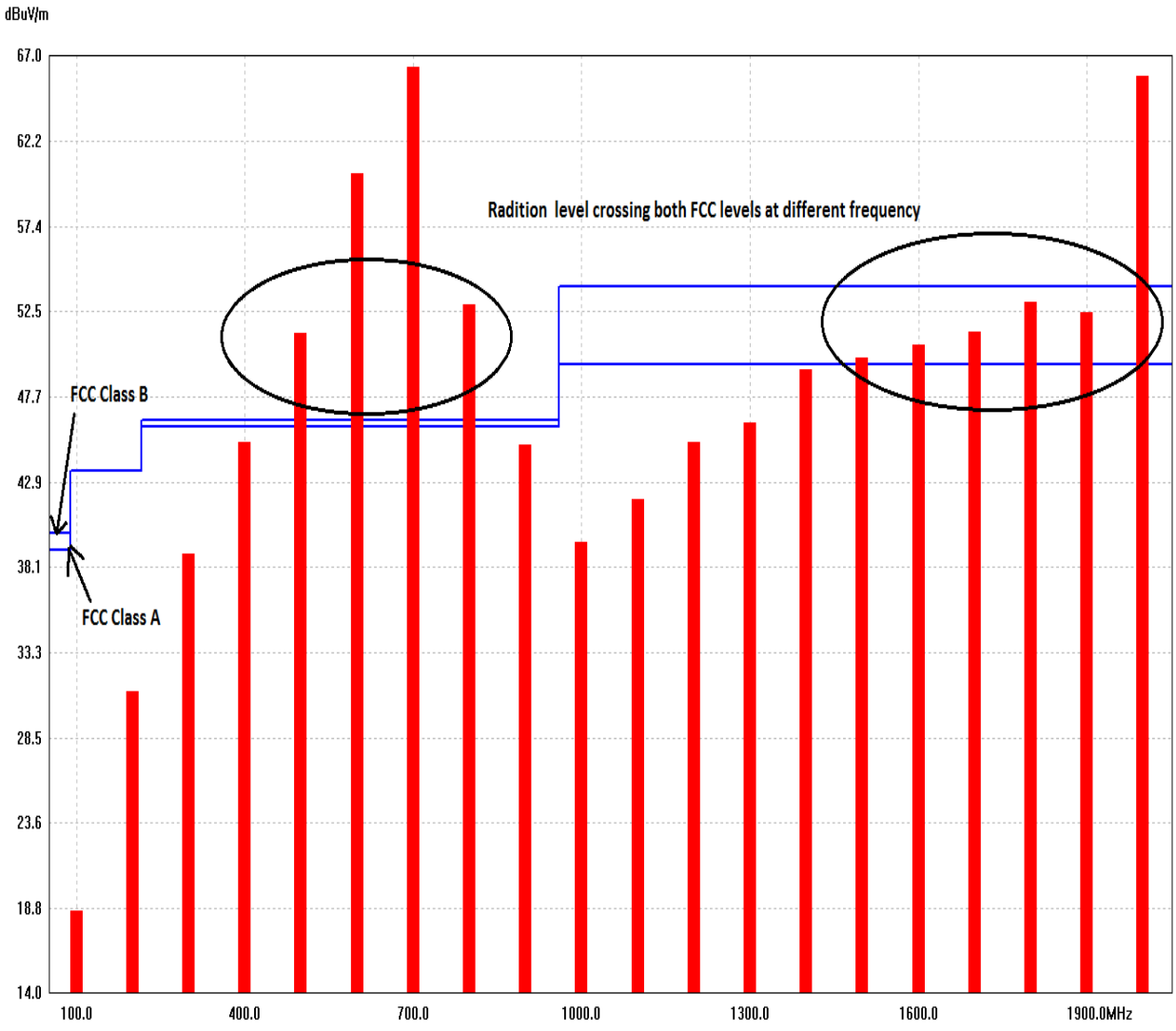


Figure 5.16(a): Emission pattern simulaction result for conventional 4 layer PCB.

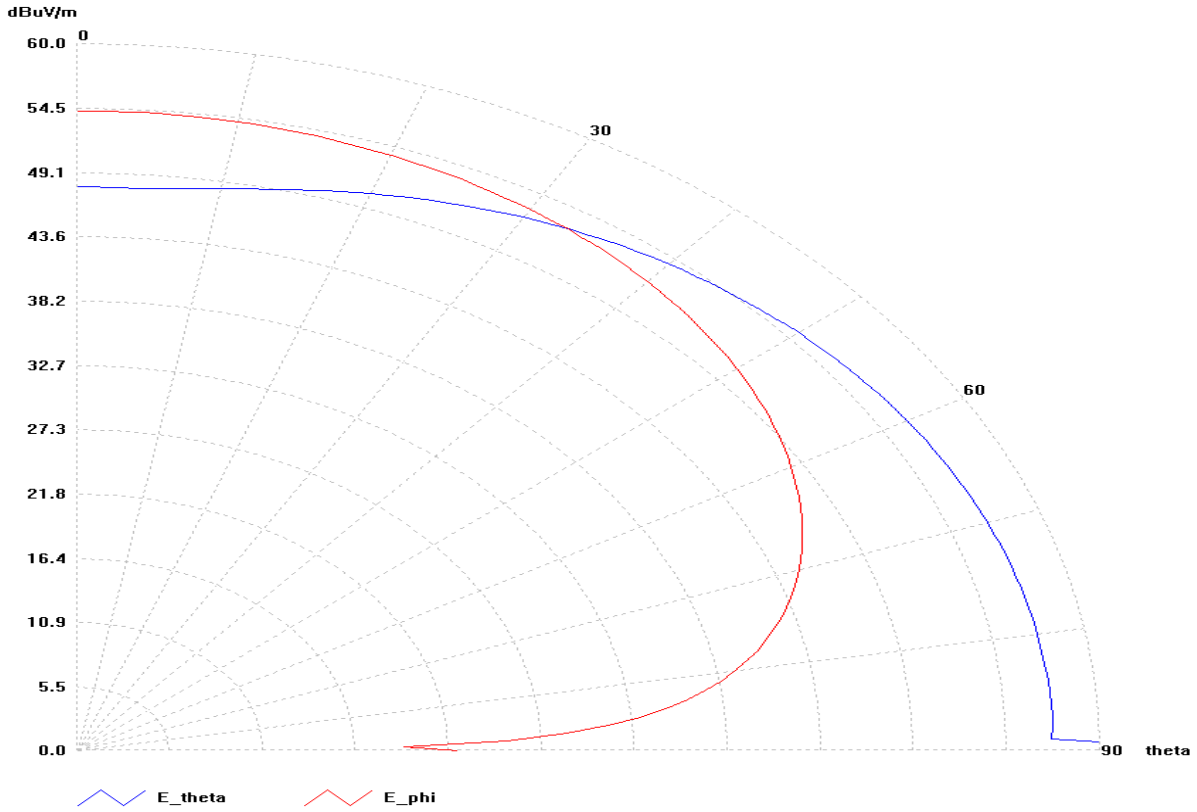


Figure 5.16(b): Electic and magnitc field pattern for conventional 4 layer PCB.

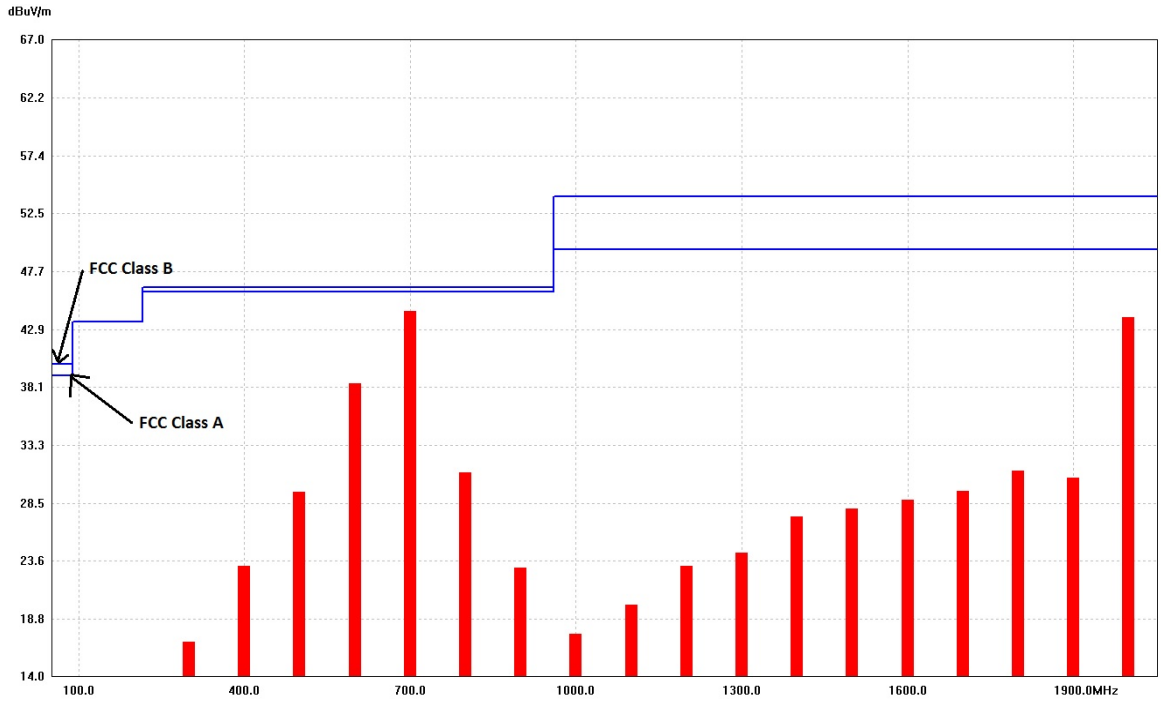


Figure 5.17(a): Emission pattern simulaction result for proposed 4layer PCB

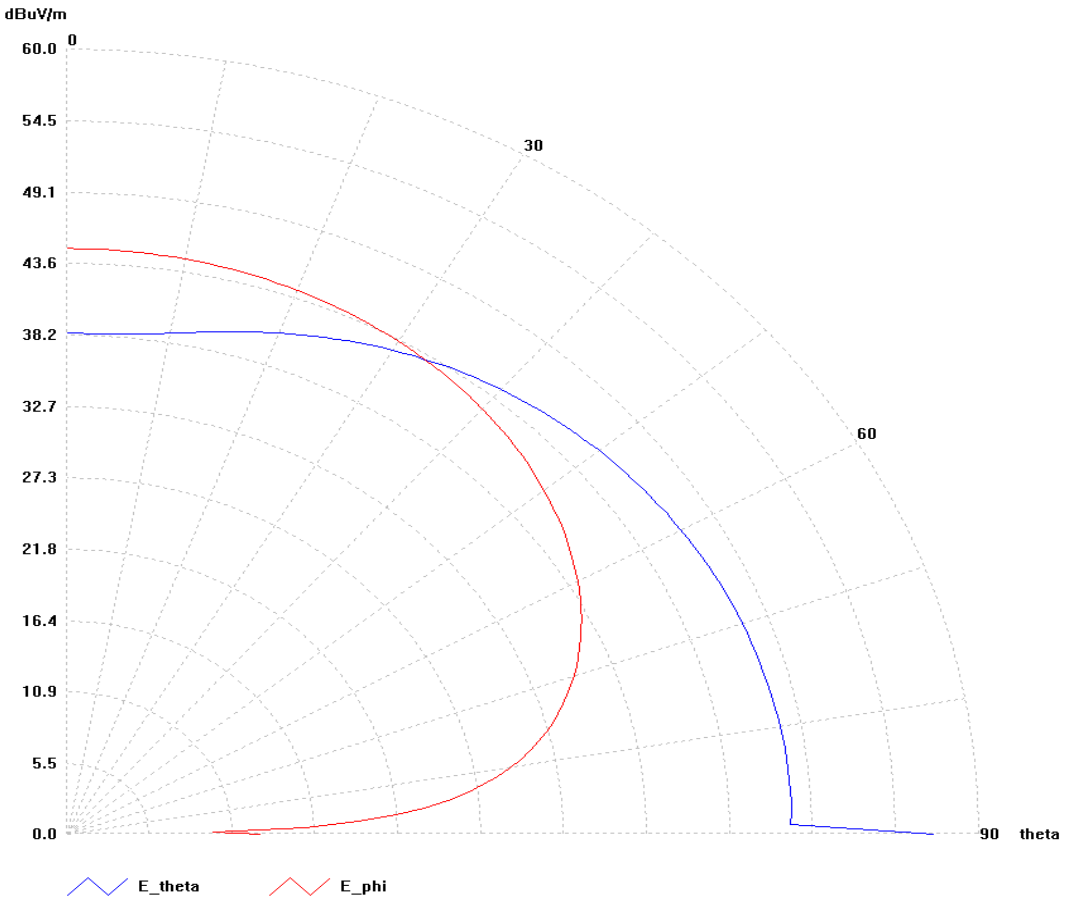


Figure 5.17(b): Electic and magnitc field pattern for proposed 4 layer PCB.

EMC of the system is further improved by using two sets of power and ground planes with different dielectric spacing between the planes layers; resulting in multiple inbuilt capacitors on the PCB.

EMC is further improved by using the proposed 6 layer stackup board. Figure 5.18, shows the proposed 6-layer stackup and figure 5.19 (a) shows the traditional pattern of 6 layer stackup board where less harmonic is generated; reduced by 18 dB to 28 dB at different frequencies. Figure 5.19(b) shows the electric and magnetic field patterns. The improvement in EMC by using the proposed 4 and 6 layer stack up boards, which radiates less emission as compared to the conventional 4 layer stackup board, is shown in table 5.1. The proposed 6 layer stackup PCB is very effective in reducing the emission level to give better results as compared to other two layer stackup boards.

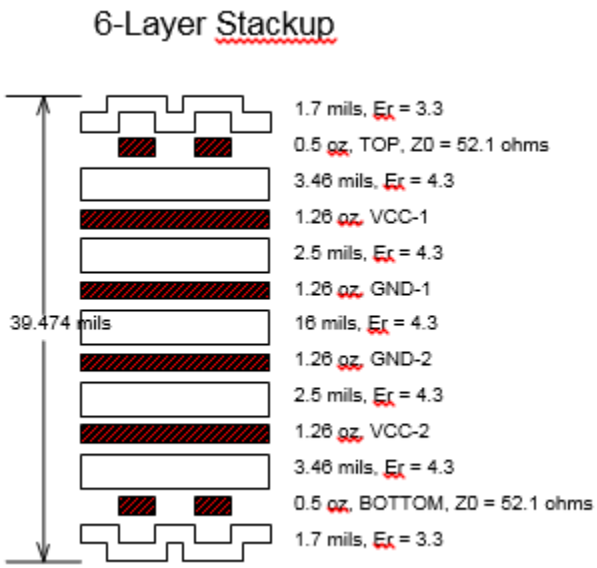


Figure 5.18: Proposed 6 layer structure board.

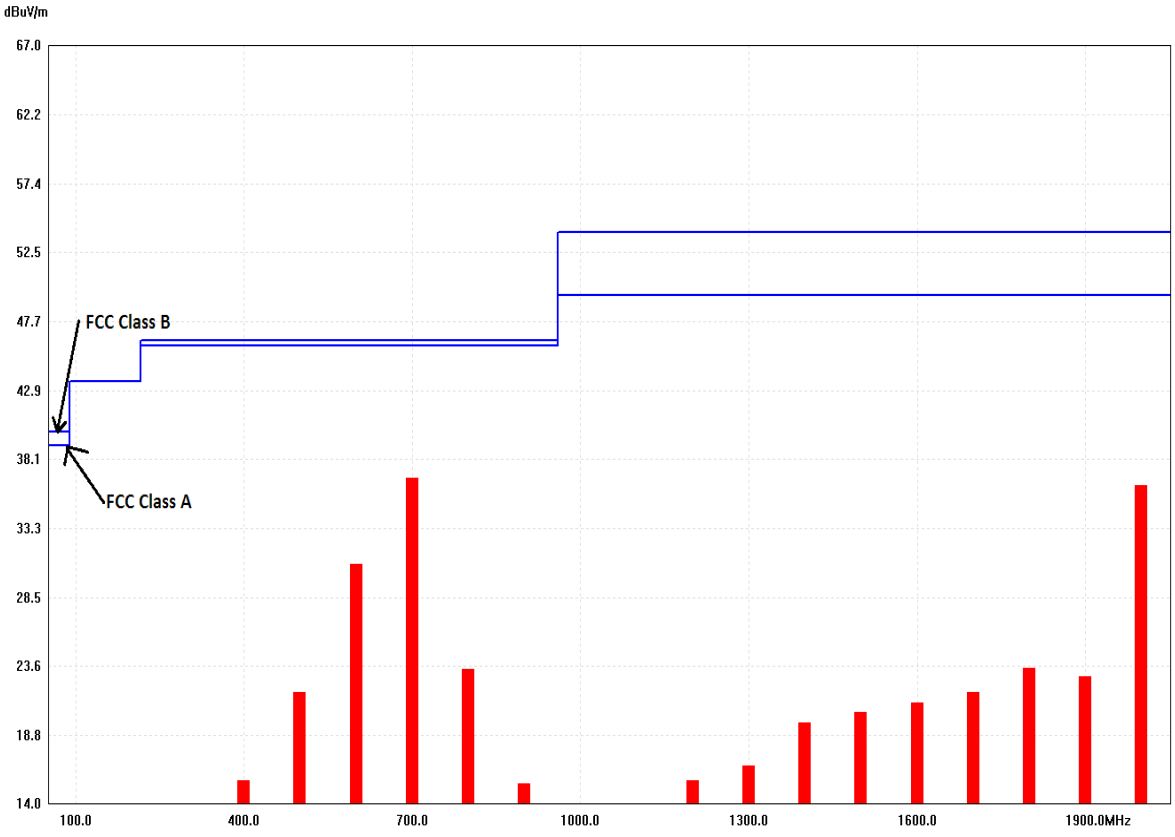


Figure 5.19(a): Radition pattern simulaction result for proposed 6 layer board.

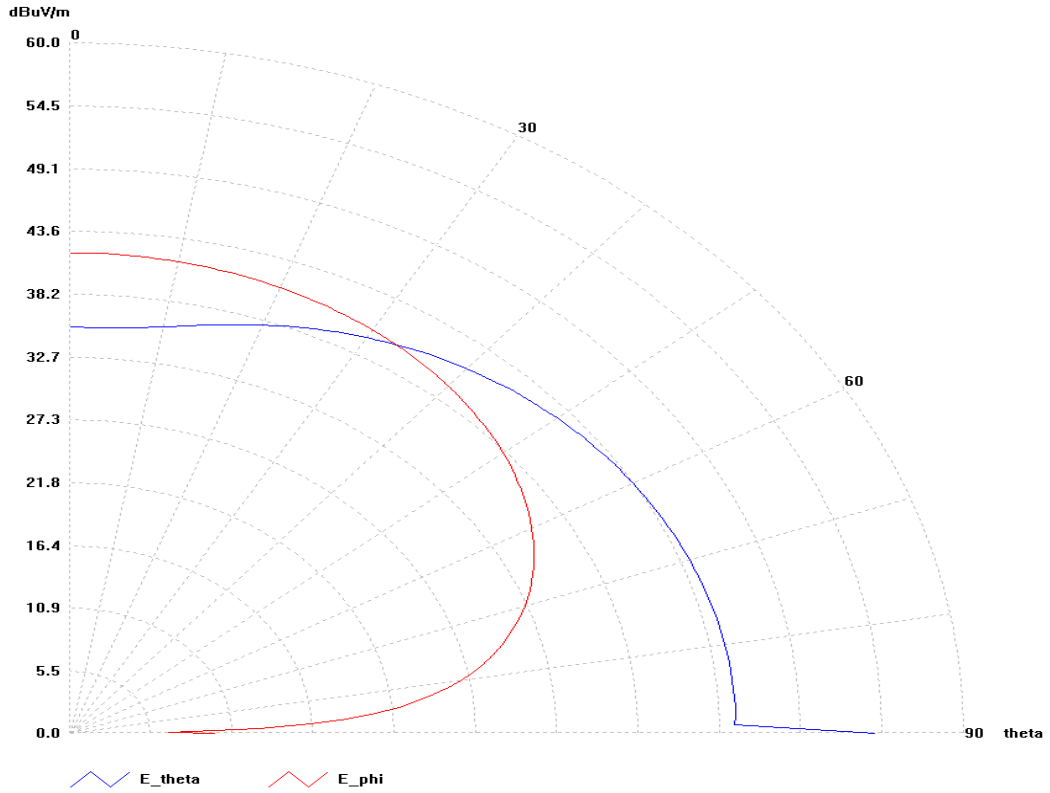


Figure 5.19(b): Electic and magnitc field pattern for proposed 6 layer board.

Table 5.1 Comparison of the emission level at different frequencies for conventional 4 layer, proposed 4 and 6 layer boards.

S.No.	Frequency (MHz)	Emission (μV/m)		
		Conventional 4 layer	Proposed 4layer	Proposed 6 layer
1	130.863	1.404971	0.47302	0.125017
2	131.478	4.569807	1.538881	0.406706
3	132.094	60.591801	20.407991	5.393551
4	132.710	72.415909	24.3944	6.447174
5	265.112	12.179284	5.593587	0.869591
6	331.621	3.002558	0.496251	0.214614
7	395.667	4.732378	2.207284	0.61995
8	396.283	9.12237	5.855924	1.195979
9	397.515	165.14473	67.2668	21.680374
10	399.362	10.185191	1.258397	1.339113
11	531.148	14.076144	4.862829	0.798772
12	664.166	101.266724	3.40705	3.342648
13	927.123	7.970347	9.606318	2.097764
14	930.202	20.774591	11.363628	2.48249

5.12Measurement Results

Figure 5.20(a) and 5.20(b) shows the measurement setup for the conventional as well as the proposed boards and figure 5.21 compares the oscilloscope waveform for both the boards when a noise source is put at a distance of less than 1 meter from the boards. The signal waveshape at receiver end is degrading due to noise source to change the shape of the signal in the PCB. The current waveshape is also affected by radio system to reduce the EMC of the system. This system is less sustainable if EMI source is close to the system. On the other hand, the signal waveshape is less affected in the proposed board. The EMC performance of the system is thus improved.

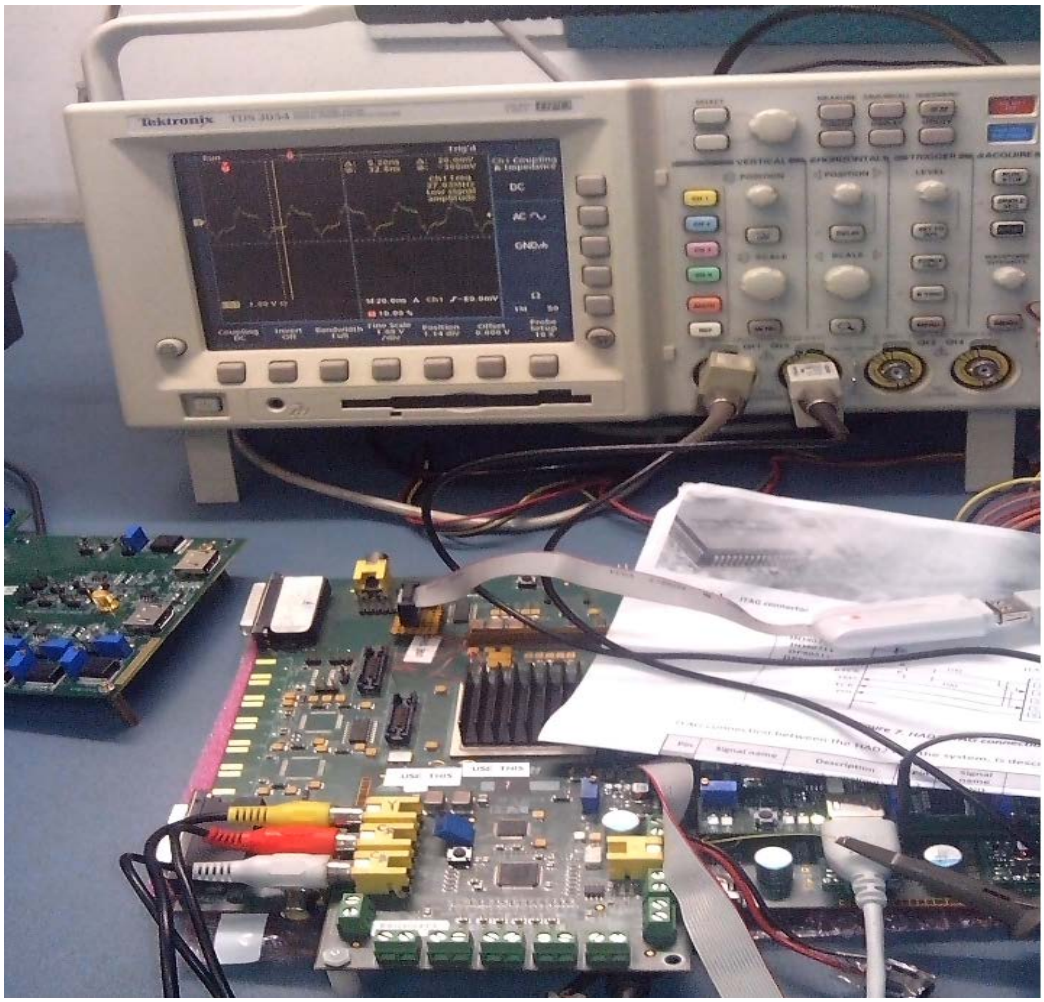


Figure 5.20(a): Meaurement setup for conventional board.

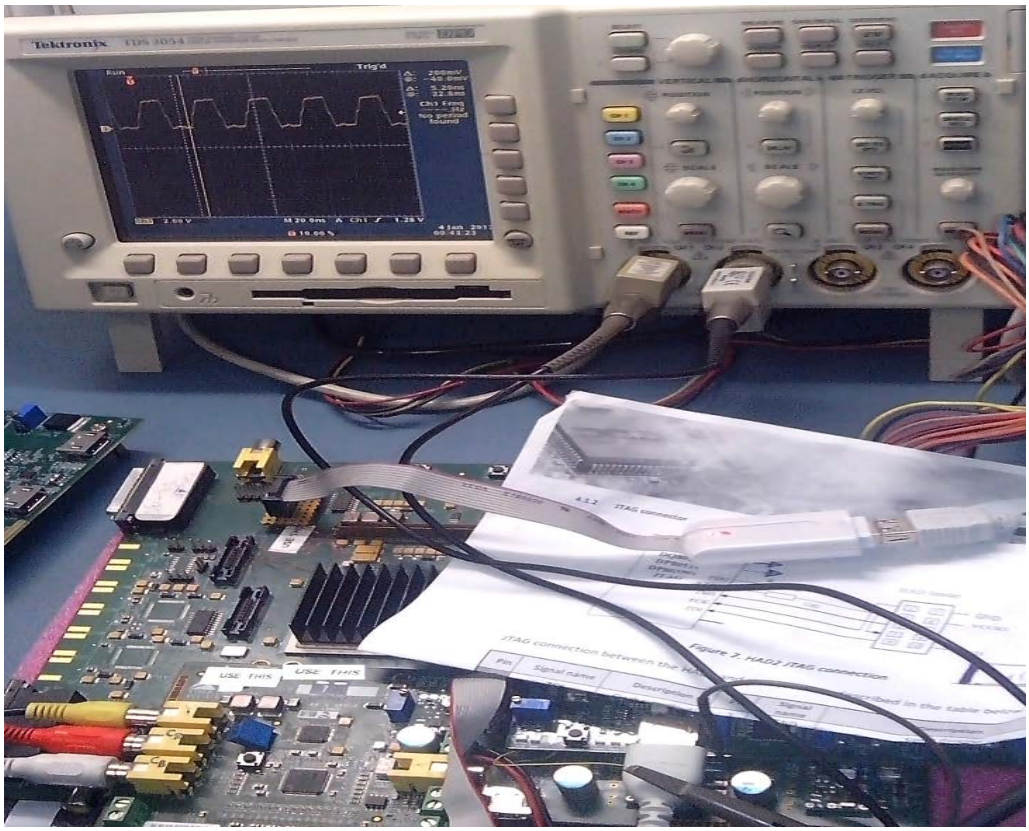


Figure 5.20(b): Meaurement setup for proposed board.

(Proposed board) (Conventional board)

Figure 5.21: Comparison of the 50 MHz clock wave for the embedded capacitance and the conventional board.

Results show that the signal qualities, including ringing, noise margin, and duty cycle of the embedded capacitance material board are slightly better than those of the conventional board. The root cause of the differences in signal qualities mentioned above is that the inhibition of power noise by the embedded capacitance board is better than that of the conventional board.

5.13 Summary

Development of a quality medical product design for better EMC takes advantage of the interplane capacitance in the PCB. The high speed signals on the boards are characterized by low voltages, steep signal edge, and jitter. They could be affected by the noise of the board-level of the power distribution system is very important to ensure the high-speed signal qualities. Therefore, achieving lower noise at the board-level power distribution system is very important to ensure the high speed signal qualities. As suggested in this study, the interplane capacitors could reduce the noise of the board-level power distribution system and improve the signal integrity of the high-speed signals. Even when the frequency is higher than 1GHz, the interplane capacitor is effective in reducing noise. So the stability and the reliability of the products could be greatly improved for EMC. Figures 5.17(a) shows that when using thin (2 mil) core between plane layers, the harmonic is reduced to an extent of 15dB to 25dB; and, using two sets of power plane layers reduces the harmonics further by 5dB to 28dB at different frequencies as shown in Figure 5.19(a).

At higher frequencies, the interplane capacitance is more effective due to the inductance of the trace, which limits the amount of charge supply for a very short time. By minimizing the board resonances using decoupling capacitors and proper power and ground-plane designs, the radiated emissions that cause EMI in PCB is reduced. Table 5.1 shows that EMC of any medical system can be further improved by using two sets of power and ground plane layers in a multilayer PCB.

CHAPTER 6

REDUCING SSN ON MULTI-GIGABIT LINKS USING INTER PLANE COUPLING

6.0 Introduction

In high-speed PCBs, such as high-speed biomedical systems, a major challenge is simultaneous switching noise (SSN) that increases switching current resulting in high-frequency noise. The SSN has already become a major bottleneck in high speed digital designs and the thousands of interconnect in future designs, augurs a complex modeling of the SSN for analysis.

Performance of high-speed biomedical systems, which often contain continuously switching signal at a very high data rate of up to 5Gbps in multilayer printed circuit boards, is affected adversely by simultaneous switching noise caused by parasitic inductance in the power supply distribution network [73]. The de-coupling capacitors, which are traditionally used to reduce or mitigate SSN, are ineffective at high data rates. In addition, the SSN is typically very difficult to quantify because it depends heavily on the physical geometry of the system.

The SSN is described by the equation

$$V_{SSN}=N\,L_{eff}\,\frac{dI}{dt}$$

where V_{SSN} is simultaneous switching noise, N *is* number of drivers switching, L_{eff} is equivalent inductance in which current must pass and I is current per driver. When a large number of signals switch at the same time, the power supply must deliver enough current to satisfy the sudden demand. Since the current must pass through an inductance (L_{eff}), a noise of V_{SSN} is introduced into the power supply. SSN occurs at both the chip level and the board level. At the chip level, the power supply is not perfect. Any sudden demand for current must be supplied by the board-level power though the inductive chip package and lead frame. On the board level, sudden current demands must be supplied through inductive connectors. Significant simultaneous switching noise (SSN) coupling occurs through the signal via transition when the signal via suffers return current interruption caused by reference plane exchange. The coupled SSN decreases noise and timing margins of digital and analog circuits, resulting in reduction of achievable jitter performance, bit error ratio (BER), and system reliability. The output results of the medical instrument may be changed or the instrument may give wrong results.

In this chapter, an integrated plane coupling method is introduced that creates a high value capacitance between the planes to effectively minimize simultaneous switching noise coupling. To prove the efficacy of the system, the effect of simultaneous switching noise coupling with traces and vias is investigated and a solution proposed for a high-speed printed circuit board in medical systems [74]. A test board is then built and analyzed, followed by a comparison of measured and simulated results. Both measured and simulated results indicate the effectiveness of the proposed method in minimizing simultaneous switching noise coupling in high-speed biomedical systems.

6.1 High Speed Interface Test Board

The PCB is the core of all electronic devices, including medical instrument. In all PCBs, power and signal integrity are major challenges that must be attended to while designing biomedical systems. A decrease in power supply voltage increases simultaneous switching of high-speed interfaces; thereby, increasing switching current (di/dt) and leading to a significant increase in power supply noise [75]. The noise margin can be significantly decreased by routing high speed traces on the PCB through via-decoupling simultaneous switching noise generated in power planes to interconnecting traces in high density printed circuit board. In spite of the progress in the industry towards faster edge rates, lower voltage levels and higher integrations; simultaneous switching noise is still a concern worth of attention while designing high-speed digital circuit systems. Non-ideal signal paths produce inductance that, along with the mutual inductive coupling of power supply distribution networks, causes simultaneous switching noise [76]. Simultaneous switching noise, in turn, contributes observable signal and power integrity problems and electromagnetic interference leading to resonance modes between power and ground planes as in parallel plane mode [77]. Figure 6.1 shows the high speed interface, i.e. HDMI and DDR3, structure board.

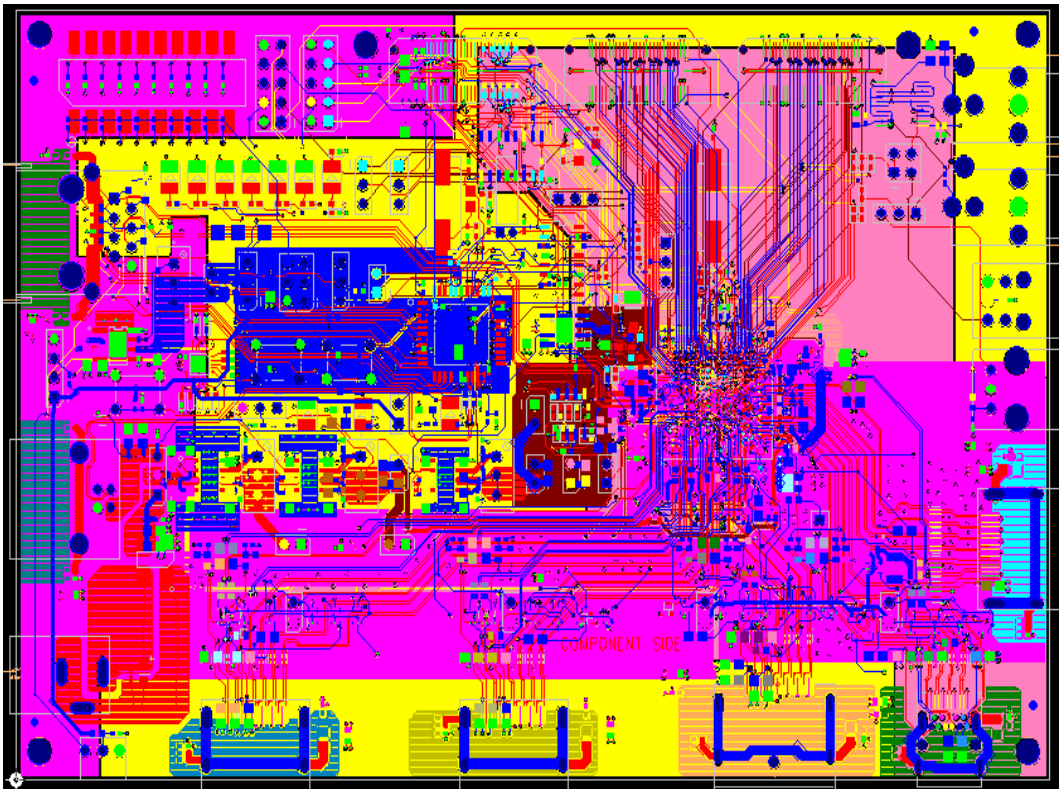


Figure 6.1: High speed interface structure board, i.e. HDMI and DDR3

The high speed interface board contains planes, which are used to supply power to the chips. Here, a plane-pair, which consists of two planes, power and ground, separated by an insulator, behaves as a cavity resonator at high frequencies. When circuits such as output drivers switch, they deposit a time varying charge on the power and ground planes which result in a displacement current source in the cavity. This current source excites radial electromagnetic waves in the cavity that reflect from the edges of the planes, causing multiple resonances in the cavity. Depending on the impedance profile of the cavity, which can contain multiple resonances, planes can bounce causing voltage fluctuations on the power supply rails of the chip.

6.2 Present Techniques for Minimize SSN Effect

The popular present technique that uses decoupling capacitors to minimize simultaneous switching noise to increase reliability and quality of medical systems, has some limitations and the other technique that uses a split ring resonator technique is rarely used because it is difficult to implement in real designs [78]. The proposed technique is not difficult to implement and easily overcomes the problems posed by the decoupling capacitor technique. In the decoupling

capacitor technique, discrete de-coupling capacitors of different values are mounted on the board. Adding decoupling capacitors has various disadvantages; routing area is blocked in high density boards because de-coupling capacitors are placed close to the power pins of integrated circuit devices. Loop inductance is increased because of the long stubs between power and ground of the de-coupling capacitors of different values that cannot be placed directly on the integrated circuit pins. Resulting increase in production cost because of the large number of de-coupling capacitors with different values mounted on the board [79].

In the proposed technique, an integrated plane coupling method is used to minimize simultaneous switching noise in industries, such as medical applications, requiring high precision and fast speed and employing high-speed, multilayer PCB designs used in high-definition multimedia interface 1.2, with transfer data up to 2.133 Gbps, and double data rate 3 chips, with transfer data at the rate of 4.95 Gbps.

The inbuilt inter-plane coupling of the proposed method is implemented by changing the thickness of the dielectric material and planes of a PCB to produce the required capacitance to eliminate simultaneous switching noise introduced by via coupling. The uniqueness of the proposed method is in creating multiple plane capacitances by using more than one set of plane layers, thereby, providing cost effectiveness and a higher efficiency in comparison to the decoupling technique.

6.3 Simultaneous Switching Noise Coupling Mechanism

Similar to all high-speed interfaces, medical system microprocessors use multi-layer PCB for packaging and power distribution. A multi-layer PCB has many metal layers separated by dielectric substrates. The power distribution network is usually distributed in many power plane layers. The intermediate layers consist of the power planes, which provide supply voltage and the ground planes that act as references. The drivers are connected to the layers using interconnect tracks and vias. This is illustrated in figure 6.2, where the power distribution network is spread across many power planes; V_{dd} being the supply voltage and V_{ss} being the reference voltage.

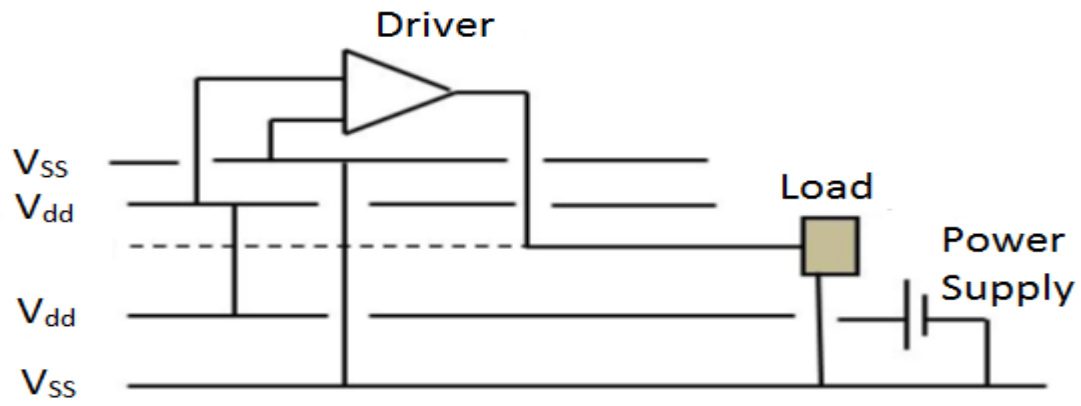


Figure 6.2: Schematic representation of the nature of switching noise in a multilayer printed circuit board through vias and traces.

Similar to the voltage surge in the power supply distribution network inside an integrated circuit die caused by simultaneous switching of millions of internal gates, multilayer PCB experiences a surge resulting in simultaneous switching noise when simultaneous switching happens in routed traces due to high speed data rate in the nets [80]. The severity of simultaneous switching noise is increased in modern high-speed circuits because of the increase of data speed foraying into the GHz range.

The surge is traditionally attributed to the inductive nature of board parasitic that introduces an effective inductance, L_{eff}, due to high-speed data signals. L_{eff} is given by the following equation:

$$L_{eff} = \frac{\emptyset}{i} \qquad (6.1)$$

In equation (1), i is a time varying current flowing through a closed path, thereby, generating a magnetic flux. Using Faraday's law, the induced noise voltage is given by the equation:

$$V_i = \frac{d\emptyset}{dt} \qquad (6.2)$$

The induced noise voltage between power and reference ground layer can be expressed as:

$$V_i = L_{eff}\frac{d\emptyset}{dt} \qquad (6.3)$$

The noise voltage in equation (6.3) is a glitch or voltage fluctuation that can be seen as a displacement of the ground level from zero to a non-zero value because it corresponds to an effective change of the supply voltage level. The voltage fluctuation, caused by the switching

state of a gate, increases manifold when generated by the simultaneous switching of hundreds or more gates and drivers. With the increase in the number of switching devices, the transient current consumed by the switching gates would increase.

6.4 Simultaneous Switching Noise Coupling Mechanism through Via

In a multi-layer board, a ground plane as well as a power plane can be used as the reference for signal trace, *e.g.*, interconnects of data lines in double data rate 3 with multi-bit in-memory module can take the different layers on the module. The signal nets can be routed either as stripline or microstrip; when a transmission line changes layer through via there is a change in reference plane. Simultaneous switching noise generated by current consumption of driver chips is coupled to signal through two coupling mechanisms; references changing via and interconnect coupling. Figure 6.3 shows the simultaneous switching noise coupling mechanism through the reference changing via in a typical 6-layer standard board. Reference changing vias must be used to transit between power or ground planes that require multiple layers for effective routing of many signals in a limited space. The reference changing vias, become the structures causing the simultaneous switching noise coupling to signal. When driver chips consume a number of instant currents, the simultaneous switching noise generated near the reference changing via has a relation with power/ground cavity impedance near via, which is frequency-dependent. Higher the power/ground cavity impedance (Z), higher the simultaneous switching noise voltage (V_{ssn}). Also, via $V_1$and via V_2, the simultaneous switching noise voltage coupled to each port of the signal line, are proportional to input impedances of the two transmission lines.

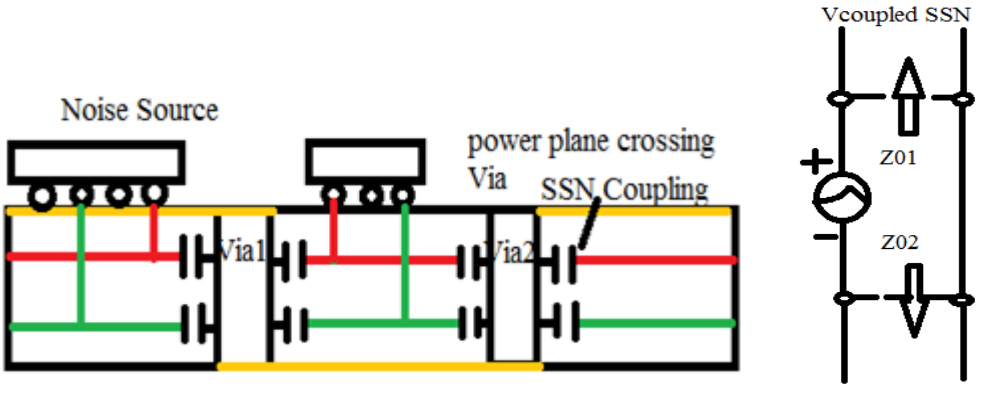


Figure 6.3: (a) Schematic model for sources of noise and coupling in power planes (b) Equivalent circuit model to describe the SSN coupling at the signal via transition.

The generated SSN could be transmitted to noise-sensitive circuits such as I/O interface interconnects and ground return current paths as well as through signal traces and vias. Among the SSN coupling paths at signal interconnections, the signal via is the most significant noise coupling structure, especially when the signal path is exchanging its reference planes. Figure 6.4 illustrates the coupling mechanism between the SSN and a signal via with reference plane exchange through a power/ground plane pair in a PCB.

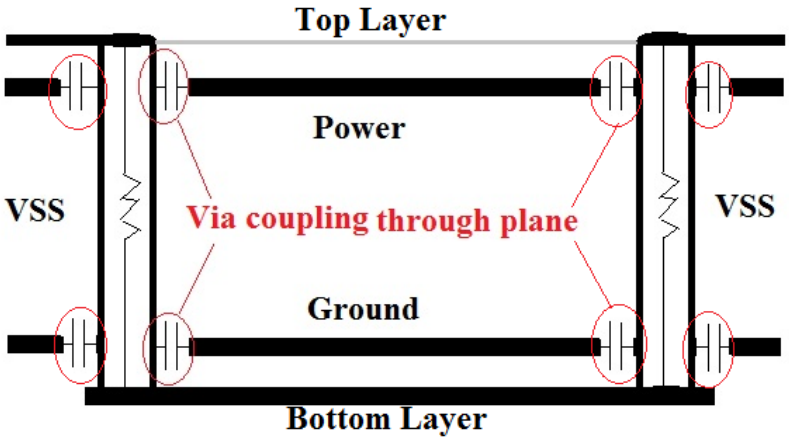


Figure 6.4: SSN coupling to signal by signal via exchange reference.

The signal via is the heavily utilized interconnection structure in high-density PCBs and enables complicated routing between the many active and passive devices mounted on or embedded inside the multilayer structure. To minimize radiated emission from such signal traces as microstrip lines, strip lines are used and the signal via is necessary to make a transition from the microstrip line to the strip line. Unless the two reference planes are tied together using an electrically shorted circuit with minimal inductance, the signal interconnect encounters a very large signal reflection and the SSN noise coupling caused by the disrupted return current path at the reference plane transition. When one of the reference planes is a power plane and the other reference plane is a ground plane, it is not possible to connect them with a low-inductance via. The signal reflection and the noise coupling are maximal at resonance frequencies of the power/ground planes.

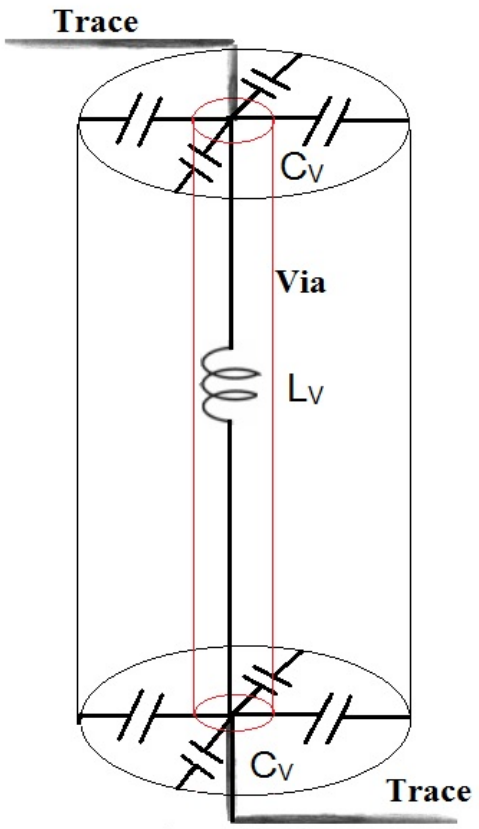


Figure 6.5: Via coupling model

The via coupling model is shown in figure 6.5 for the 6 layer stack up board. The electrical model of the metallic via column is expressed as an inductor, while the capacitive coupling between via and adjacent reference a plane is modeled by coupling capacitors surrounding the metallic via the column. The signal via is coupled equally to both power plane (layer 5) and ground plane (layer 2) of the plane pair in a balanced manner. Via neck effect is added to the model by adding an inductor. This effect is induced by the absence of the reference plane under the signal trace at the via clearance.

When simultaneous switching noise is generated near the reference change via of a plane pair, the time-varying simultaneous switching noise voltage is built up between the power plane and the ground plane. Thus, simultaneous switching noise is developed across the two planes at the via position. The amplitude and the phase of noise at via location are dependent on the resonance mode number and the location of via. The simultaneous switching noise becomes a voltage

source between the two reference planes at via location, resulting in the injection of electromagnetic waves into via location as expressed in equations (6.4) and (6.5):

$$V_{ssn,01} = \frac{Zin1}{Zin1+Zin2}. V_{ssn} \quad (6.4)$$

$$V_{ssn,02} = \frac{Zin2}{Zin1+Zin2}. V_{ssn} \quad (6.5)$$

In equations (6.4) and (6.5), Zin1 and Zin2, represent the characteristic impedances of the two transmission lines. As indicated, the coupled SSN voltage is related to the characteristic impedances of the two transmission lines, Z01and Z02. The coupled SSN can then be calculated using the above equations with the given characteristic line impedances. Because Z01and Z02 are the same, half of is coupled to the signal line through via transition.

6.5 Simultaneous Switching Noise Coupling Mechanism through Trace

As the supply voltage is scaled down and the power dissipation goes higher, the switching current makes a significant power supply noise with the increased clock frequency. The simultaneous switching noise (SSN) generated in power system is more strongly coupled to interconnecting lines, as the layout density of digital circuit increases. Many signal traces are routed, including via transitions, and some power/ground is partitioned to several island planes, as shown in Figure 6.6. In these complex designs, the switching noise on power/ground planes is strongly coupled to signal traces. However, at the same time, the increasing speed of signal requires a more tight noise margin and strict signal integrity. Thus, the coupling of power/ground noise to signal traces gives rise to troublesome problems for signal quality and timing, and ultimately degrades the high speed performance.

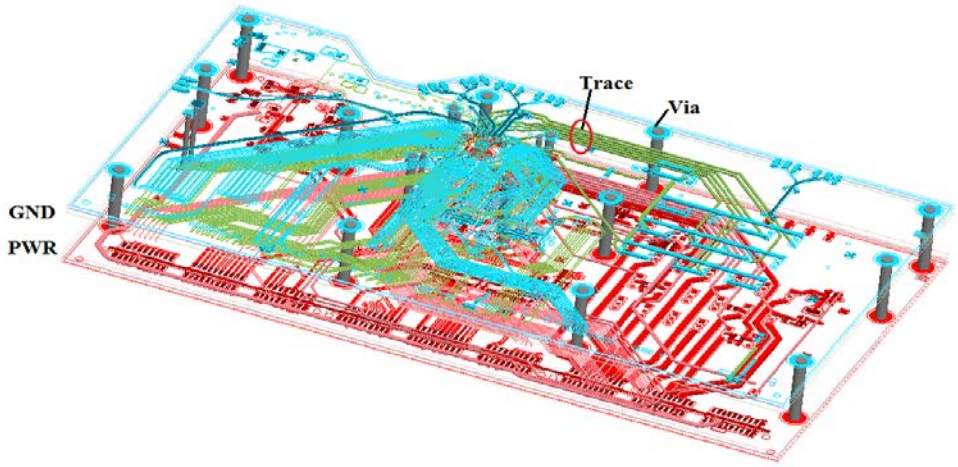


Figure 6.6: 3D model of the multilayer board for trace coupling

When a signal trace is routed between power/ground plane pair, it is directly influenced by the electromagnetic field generated by the fluctuating voltage (SSN) that appears between the planes as shown in figure 6.7.

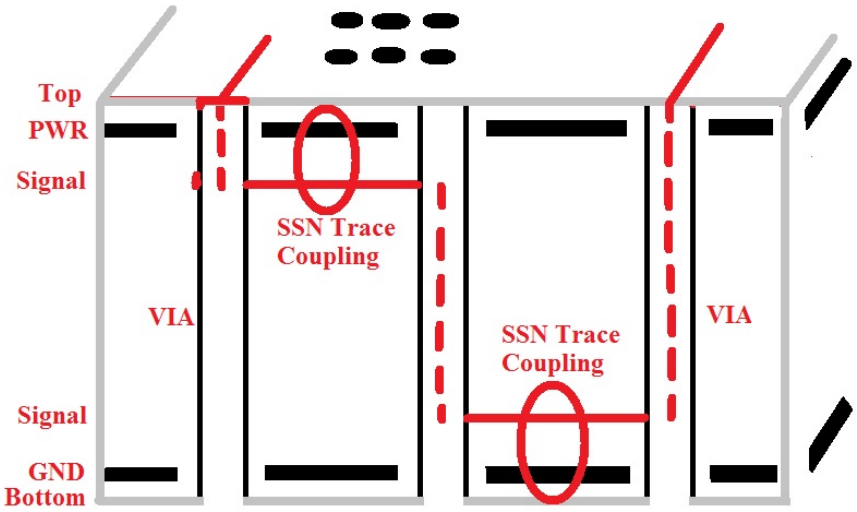


Figure 6.7: SSN coupling through signal trace by strip line

The SSN field between the plane pair and the field generated by the signal propagating along the trace co-exist. Total electromagnetic field (E, H) is the sum of the field generated by SSN (E_n, H_n) and the field propagating along the signal trace (E_i, H_i) [7]. The voltage and current on signal trace is calculated by the following equation,

$$V_{total} = \int \boldsymbol{E} \cdot d\boldsymbol{l} \;=\; \int \boldsymbol{Ei} \cdot d\boldsymbol{l} + \int \boldsymbol{En} \cdot d\boldsymbol{l} = v + V \qquad (6.6)$$

$$I_{total} = \oint_C \mathbf{H} \cdot d\mathbf{l} \;= \oint_C \mathbf{Hi} \cdot d\mathbf{l} + \oint_C \mathbf{Hn} \cdot d\mathbf{l} = i + I \qquad (6.7)$$

where, V, I represent the voltage and the current from the SSN field, v, i represent those from the propagating wave along a signal trace, and , it represent the total voltage and current. The total voltage and current (V_{total}, I_{total}) observed on a signal trace are equal to the sum of the V, I originated from SSN field, and v, i originated from the wave propagating along the signal trace.

6.6 Signal Traces between a Noisy Planes

When a high speed signal is routed between the noisy planes, the plane noise is easily coupled with the signal nets as shown in the figure 6.8. A noise voltage is induced into the signal trace

due to SSN coupling, the line equation of the signal trace with impressed voltage and current has been derived as an equation:

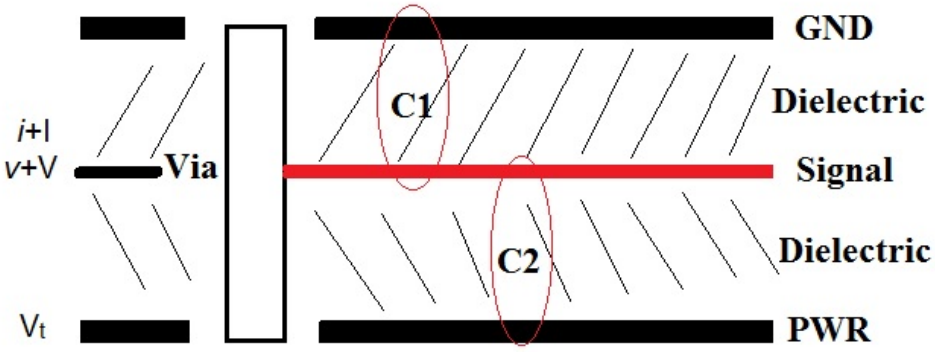


Figure 6.8 Transmission line between a noisy plane pair

$$-\frac{\partial i}{\partial x} = C_1\frac{\partial(V+v)}{\partial t} - C2\frac{\partial Vn}{\partial t} - C2\frac{\partial(V+v)}{\partial t} \quad (6.8)$$

$$-\frac{\partial v}{\partial x} = L\frac{\partial(i+I)}{\partial t} \quad (6.9)$$

where, v and I represent the voltage and current produced by the wave propagating along the signal trace. V_{ssn} the SSN voltage between the power plane layers and V, I represent the voltage and current impressed on the signal trace by SSN. C1 capacitor is created between the signal and ground layer and C2 capacitor is created between the signal and power layer. C1 and C2 are inversely proportional to the distance between the signal and plane layers. Coupling SSN noise depends upon the parameters of the signal trace, i.e., L, C1, and C2.

The noise coupling impedance can be used for the time domain analysis. If a periodical switching current source I(t)is given in time domain, its frequency spectrum I(f)can be calculated by Fourier transform. The frequency spectrum of coupled noise voltage is a product the of I(f) and the coupling impedance,

$$V_{couple}(f) = I(f) \times Z_{couple} \quad (6.10)$$

The noise voltage is superposed on signal voltage which results in jitter and, even, logic fault in data lines.

6.7 Inter Plane Coupling Mechanism

There is a limitation on the efficacy of discrete decoupling capacitors, traditionally used to counter simultaneous switching noise, because of interconnect impedance of capacitors mounted on a PCB. This limitation of discrete capacitance can be overcome by using embedded inter-plane capacitance, which is present naturally because of the inherent property of two conductive planes separated by a dielectric substrate. For effective utilization of inter-plane capacitance for a PCB, the dielectric constant of the board can be increased or layer spacing of the board can be reduced, thereby, shrinking the thickness of the printed circuit board.

The inter-plane capacitance of a PCB is given by $C = \frac{\varepsilon A}{S}$, where ε is the dielectric constant, S is the spacing of the planes, and at the effective area of the planes. Figure 6.9 shows a lumped-element model for the power distribution impedance on a board with closely spaced power and ground planes. The impedance between the planes in power distribution network is directly proportional to the voltage induced by the current drawn from the power bus; lower the impedance, lower the voltage induced by the current. The lumped element model described is valid at those frequencies, where the plane can be modeled with a single capacitor. This is possible at frequencies at which plane inductance is small. The lumped model can be used to calculate the power bus impedance at frequencies well below the first board resonance.

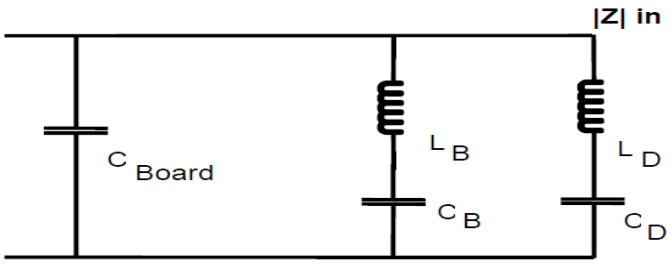


Figure 6.9: Lumped element model of power bus

At low frequencies, the impedance of the power bus can be expressed as,

$$Z_{bus} = \frac{1}{jw(C1+C2+\cdots.Cn)} \qquad (6.9)$$

At higher frequencies, some of the decoupling capacitors begin to behave like inductors. The inductance of these capacitors forms a resonant circuit with the inter-plane capacitance and the capacitors that do not yet behave like inductors. At resonant frequencies, the impedance of the

power bus is very high and the board starts ringing. If the impedance of the power plane layer and the signal frequency at different dielectric thickness values are plotted, as shown in figure 6.10, it can be observed that at a given thickness, the impedance is inversely proportional to the frequency.

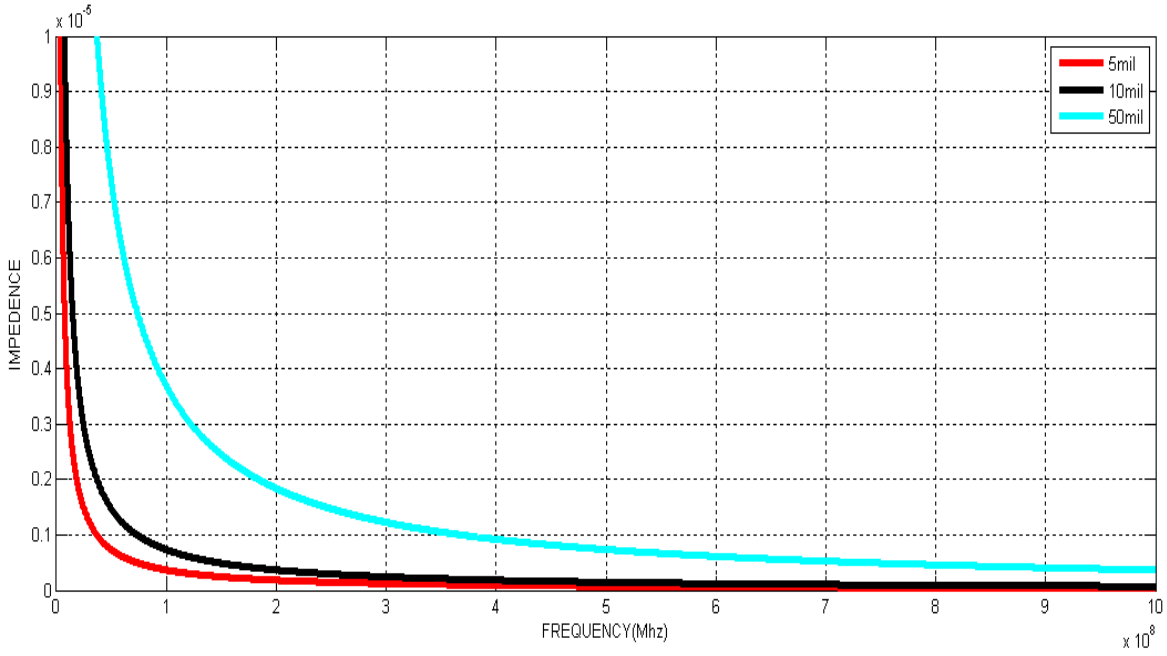


Figure 6.10: Impedance of power plane layer with different thickness of dielectric material.

Normal 6-layer stack-up PCB plane impedance is higher than integrated capacitance layer stack-up PCB. Although, all capacitors on the board help in decoupling of the power bus, the decoupling is more effective for large values of a capacitor. Therefore, it is important to achieve high capacitance to ensure sufficient loss, especially at resonant frequencies, where impedance of a power bus is very high leading to the ringing of the board.

6.8 Test Vehicle Description

The present study used a 6 x 4 inch high speed interface board with double data rate 3 and high-definition multimedia interface. The double data rate 3 interface introduces simultaneous switching noise in the power distribution network because of the high rate of 2.133 Gbps in all 64 high-speed data lines that, are switching simultaneously at a high speed. Eye pattern and jitter of data lines are changed due to simultaneous switching noise in the output of the system. The

high-definition multimedia interfaces 1.2, which are also present in the same board and are transmitting data serially up to 4.95 Gbps, contribute to the increase of the simultaneous switching noise level in power supply distribution network of the board.

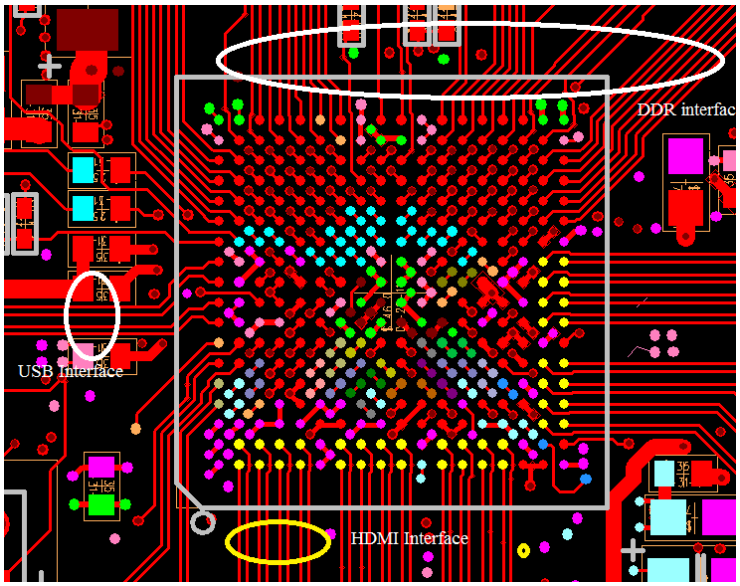


Figure 6.11: 6 layer proposed method board and shows high speed interface.

In the present study, two boards following two different techniques to minimize the effect of simultaneous switching noise were made;, one for the standard method employing de-coupling capacitors; and another for the proposed method employing an integrated power plane capacitor.

The standard board has 6-layers with two sets of power plane layers, layers 2 and 3 and layers 4 and 5, with 1.6 mm board thickness and 50 mil dielectric thickness between each of the two sets of plane layers as shown in figure 6.11.

Figure 6.12: SSN noise in 6 layer structure board.

The SSN noise is generated when high speed data lines are simultaneously switching at high data rate as shown in figure 6.12. Channel 2 represents high speed data lines and channel 4 represents SSN noise introduced at the PDN voltage, VDD. The peak to peak noise voltage is 232mV during data lines transition.

Figure 6.13 shows the improvement in the 3D results when proposed 6 layer stack up board is used and figure 6.14 for the reference board result. Simulation result shows that the proposed board result is better than the reference structure board.

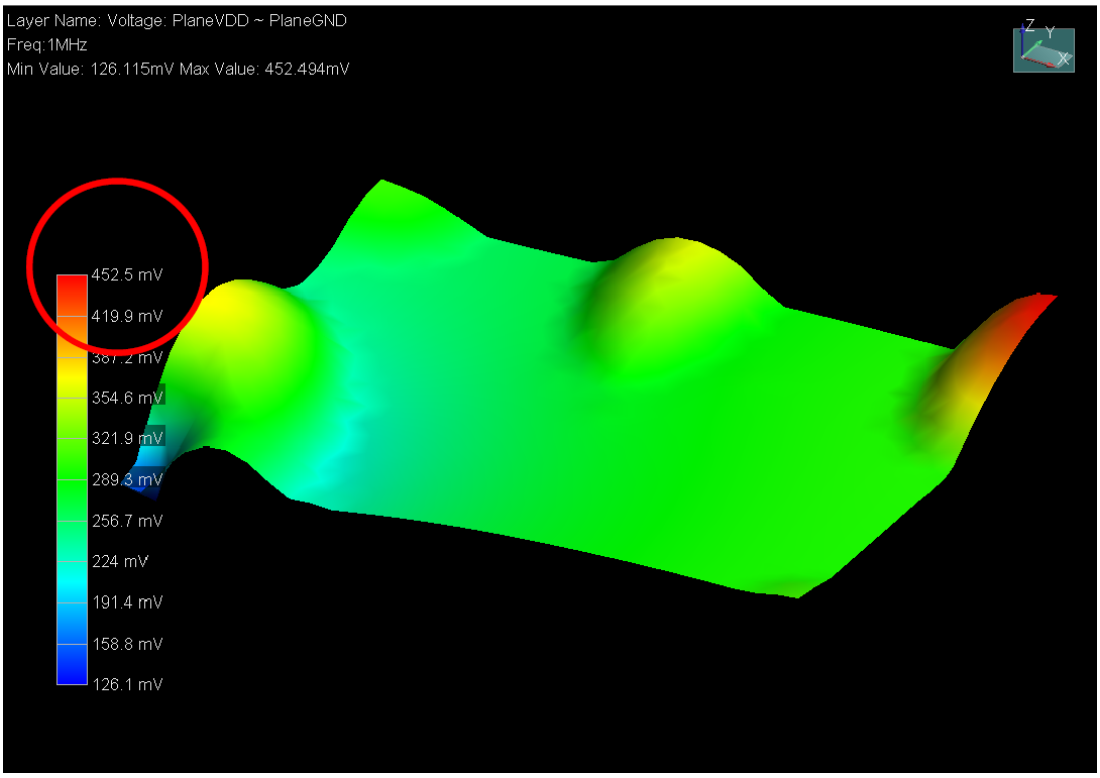


Figure 6.13: 3D simulation results for proposed board

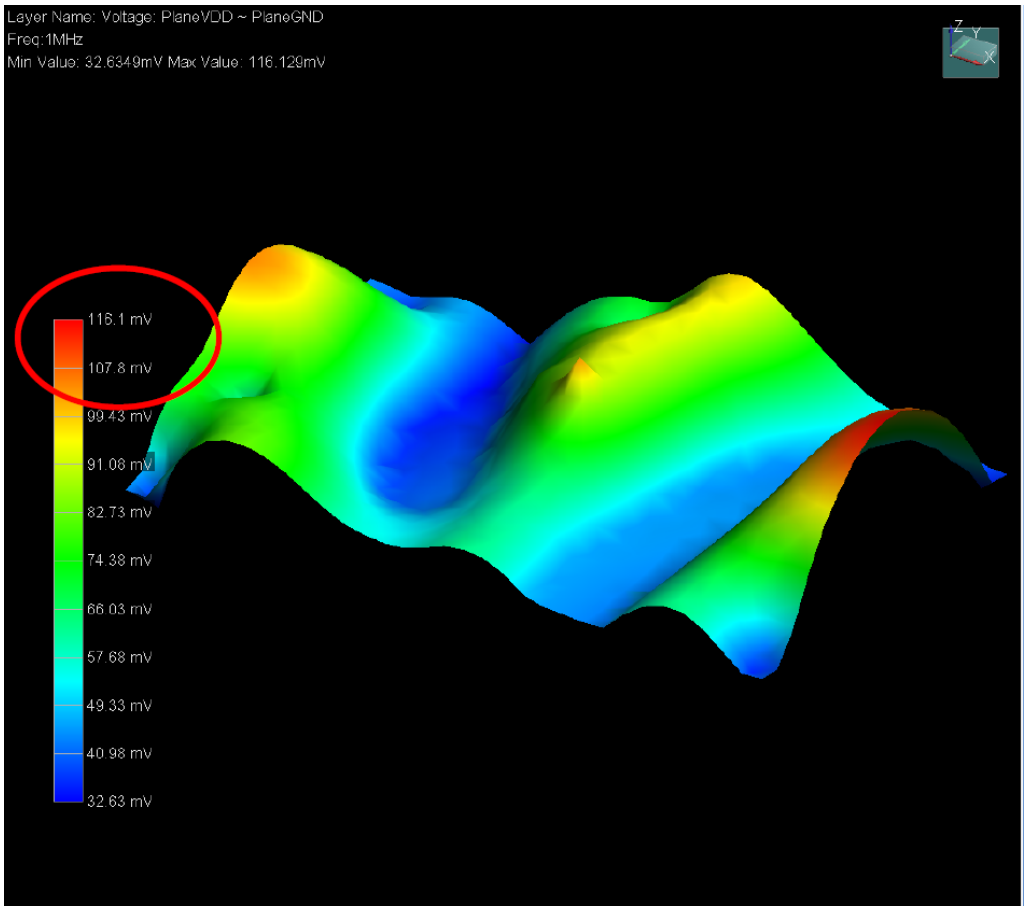


Figure 6.14: 3D simulation results for reference board

The proposed board is an integrated capacitor 6-layer board, which also has two sets of power plane layers with 1 mm board thickness and 1 mil dielectric thickness between the two sets of plane layers for each pair. The resulting improvement in the coupling between the power plane layers provides a low impedance path between the power source and the power pin of the semiconductor components, which in turn allows a minimum amount of voltage drop across the power supply of components. Common mode RF energy is developed if an imbalance exists within the power distribution network. The board, however, might require extra precaution during assembly because of the reduced thickness.

Compared to the minimum inter-plane capacitance of the standard 6-layer board, with 1.6 mm thickness, due to 50 mil dielectric thickness between the plane layers; multiple sets of high value inter-plane capacitances are generated in the proposed 6-layer board due to the decreased dielectric thickness of 1 mil between the plane layers. Multiple inter-plane capacitances of the

proposed board also increases the total plane capacitances by multiple times, making it an effective solution for high speed medical systems.

In the current study, the two boards are evaluated using the following methodology; comparison is made of the measured results of the two boards for the power supply distribution network resonance and anti-resonance frequencies, simultaneous switching noise, and impedance; this is followed by a comparison of the measured and simulated results; and finally, a comparison is made of the signal eye quality of both the boards.

6.9 Resonance and Anti-resonance Frequencies for PDN

In the evaluation methodology, the power supply distribution network resonance and anti-resonance frequencies are determined; for example, by simulating the frequency domain self-impedance profile of the power supply distribution network interconnects and associated capacitances over a wide frequency range. The anti-resonance frequency is of interest because, generally, the largest magnitude of voltage noise is a result of toggling signals near one of the anti-resonance frequencies. Also, the parasitic capacitances attached to the power supply change the power supply distribution network system resonant frequencies. The resonance frequency induced by simultaneous switching noise caused by via inductance and decoupling capacitance is given as follows.

$$f_r = \frac{1}{2\pi\sqrt{L_{eff}C}} \qquad (6.10)$$

where f_r is the resonance frequency, L_{eff} is the inductance, and C is the capacitance. The power supply distribution network is changed due to changes in the inductance of the power supply.

The impedances and cross-coupling of signal interconnects affect the resonant frequencies of the system by affecting the current demand of the signaling circuits. The superposition of pre-existing noise waveforms with new noise waveforms caused by signal current demands of the system results in simultaneous switching noise , which is not a major problem at low speed, because the induced noise settle quickly and there is very little superposition of the voltage noise waveforms. Simultaneous switching noise is high for signals operating near the system resonant frequencies because the voltage noise waveforms do not settle quickly resulting in the rapid superimposition of signals. Figure 6.15 shows that the resonance frequency is changed at

different values of capacitors. High speed data lines are simultaneously switching at the rate of 2.133 Gbps.

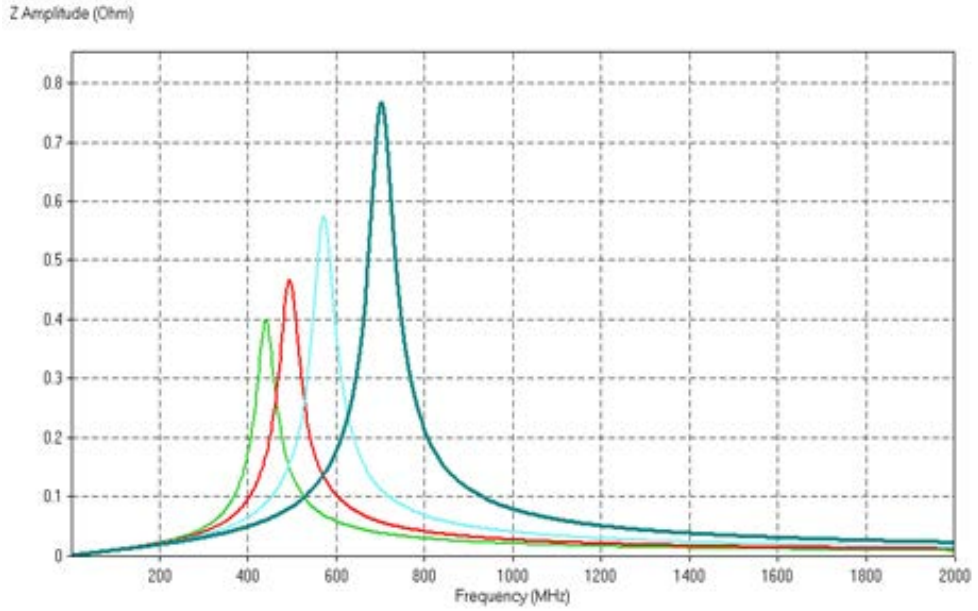


Figure 6.15: Resonance frequency is changed at different values of capacitance.

As shown in the figure 6.15, the resonance frequency for a 10 nF capacitor is 700 MHz and the resonance frequency for a 100 nFcapacitor is 580 MHz, both the resonance frequencies being very close to the 1066 MHz operating frequency of the system. In practice, because of the intrinsic effective series-inductance and effective series-resistance, the decoupling capacitance does not behave like a pure capacitance at high frequencies. Instead, at frequencies above the resonance frequency decoupling capacitors appear inductive and are not affective, thereby increasing the affect of simultaneous switching noise on signal quality.

6.10 Power Ripple and Plane Impedance Variation

In the proposed method, it is very effective for resonance frequency because of the increase in the integrated capacitance between the plane layers due to the decreased dielectric thickness between the two power plane layers. In addition, the power distribution is improved and noise immunity is provided by the integrated capacitors. The integrated plane capacitance is also more effective in managing impedance, which shoots up in case of decoupling capacitors, of the system at the resonance frequency. The decoupling capacitor board results in a LC tank circuit, which produces the maximum impedance at resonance frequency, resulting in parallel resonance.

The effective series resistance and inductance can be further brought down by inserting banks of small parallel decoupling capacitors in the substrate. Figure 6.16 shows the power ripple when only decap is placed on the board and figure 6.17 shows the power ripple when the proposed structure is used. In figure 6.16, the peak voltage, 80 mV, is the inductive overshoot. The voltage noise rings out as a damped sinusoid at the power supply distribution network resonant frequency. The peak-to-peak voltage noise is 230 mV, which is 17% of the 1.35 V nominal voltage rail. In figure 6.17, the peak value is 20 mV; overshoot and the peak to peak voltage, 71 mV, reduces when integrated decoupling capacitors is introduced between the power plane.

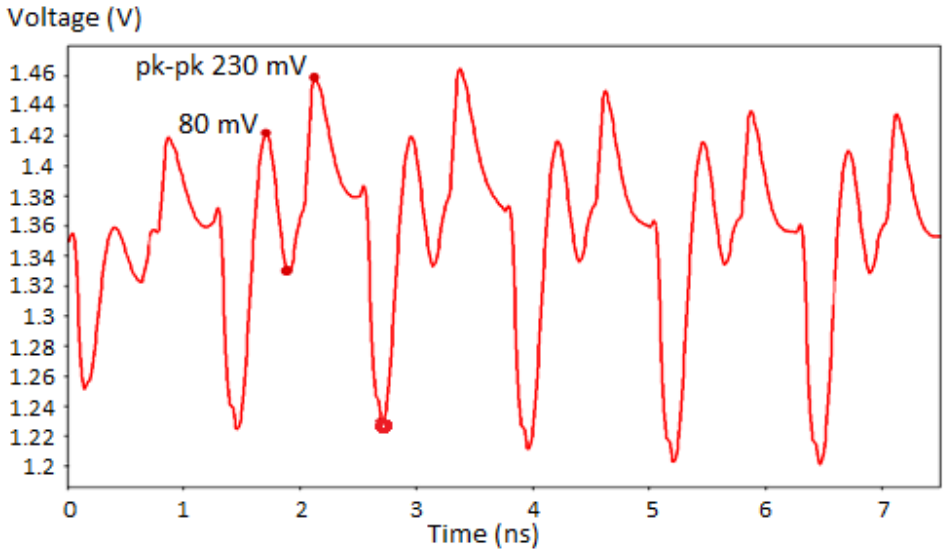


Figure 6.16: Power ripple plot for standard board.

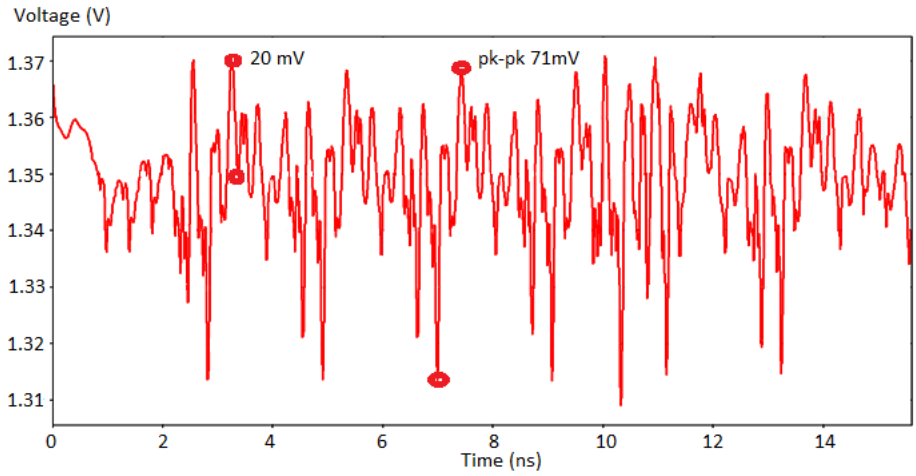


Figure 6.17: Power ripples plot for the proposed board structure.

The simultaneous switching noise has an inverse relationship with Z_0 because of which transmission lines with high characteristic impedance and smaller di/dt require less current to charge resulting in lower simultaneous switching noise; whereas, a transmission line with low Z_0 is capacitive and requires a larger current, resulting in larger simultaneous switching noise resulting in delay of signal line due to delay in signal rise time. Also, large simultaneous switching noise results related to the Z_0 of the transmission line.The characteristic impedance of the plane layer is calculated by the equation, $Z_0 = \frac{1}{2\pi f C}$.

Figure 6.18 shows that the impedance of the power plane layer decreases with the increase in the signal frequency at two different dielectric thickness values, that is, 1 mil and 50 mil. The red shape represents a standard board and the blue shape the proposed structure board.

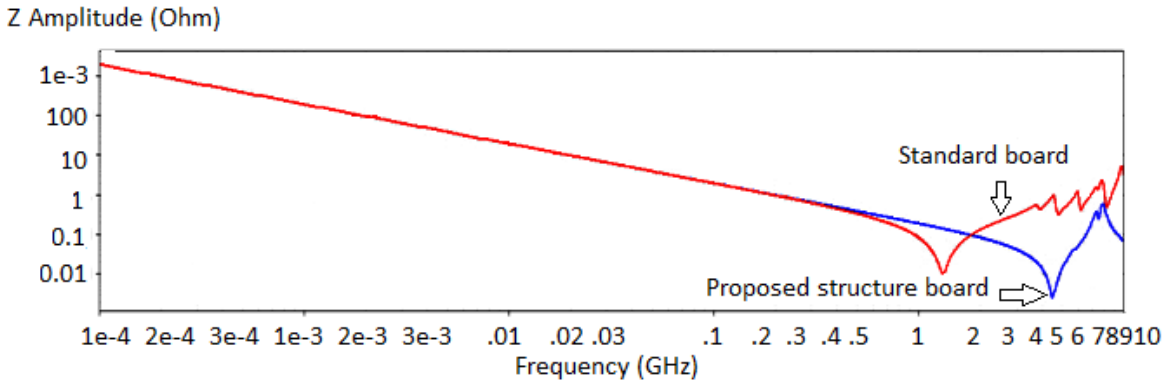


Figure 6.18: Power plane impedance variation comparisons for both structure boards with respect to frequency.

6.11 Impact of Signal Insertion Loss on Timing Margin

The efficacy of the proposed board compared to the existing technique is apparent at high switching rate where simultaneous switching noise affects the signal quality leading to false triggering and wrong results for the system. Figure 6.19 shows that for a standard 6-layer board with de-coupling capacitors mounted on the board, the return loss is about -10 dB at 2 GHz due to less coupling between power plane layers and more simultaneous switching noise introduced in the board. On the other hand, Figure 6.20 shows that by using the proposed integrated structure board, the return loss is -15 dB at 2 GHz. The smaller value of return loss signifies a higher transmission and lesser reflection of signal. The proposed method improves return loss by 5dB, which is a very significant value, especially for any high speed medical system. An increase

in the operating frequency increases reflection loss, which can create serious timing error problem in medical systems. Power ripple, 230 mV peak to peak at 2 GHz, is also high.

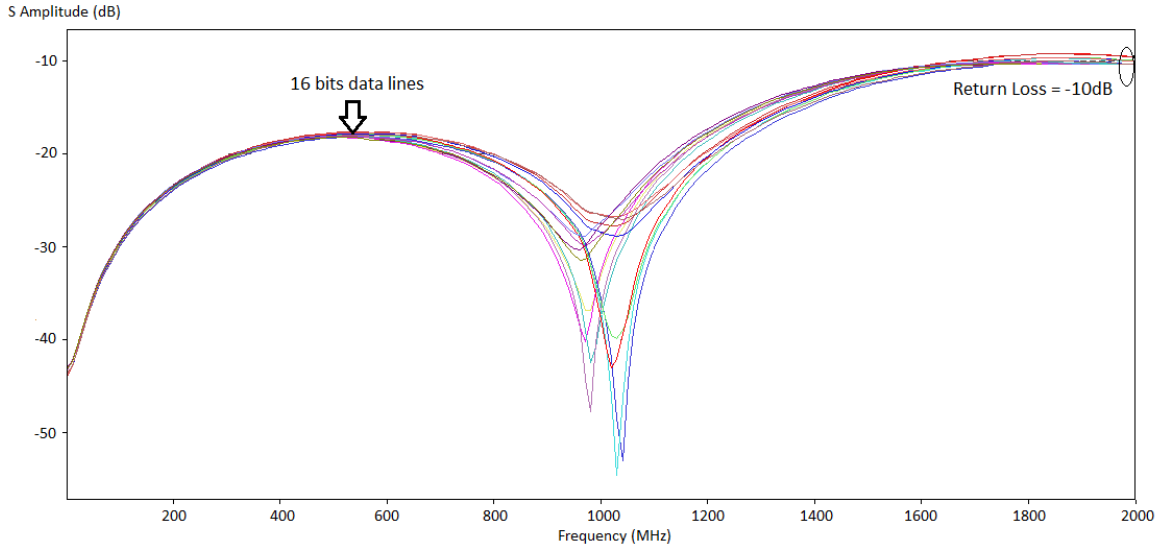


Figure 6.19: Return loss of 16 bit data lines, for standard 6-layer board, -10 dB at 2 Gbps.

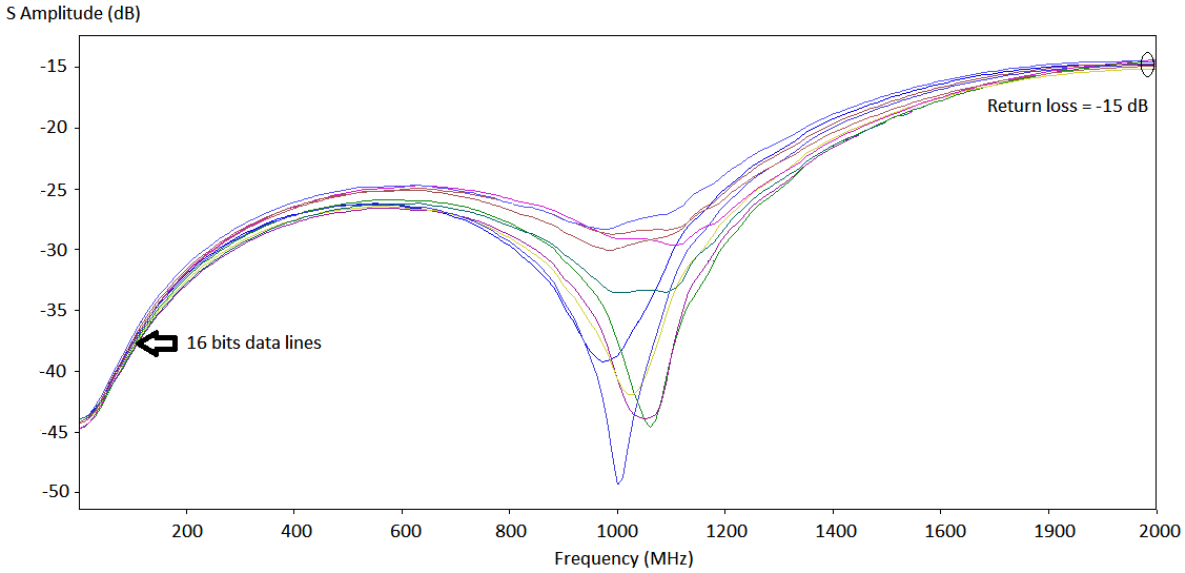


Figure 6.20: Return loss of 16 bit data lines, for proposed structure board, -15 dB at 2 Gbps.

Figure 6.21 and Figure 6.22 show the insertion loss of 16 bit data lines, are represented by multiple colored curves, -0.8 dB, for a standard board which in the proposed structure is -0.6 dB at 2 Gbps. Insertion loss is improved by 0.2dB in the proposed method.

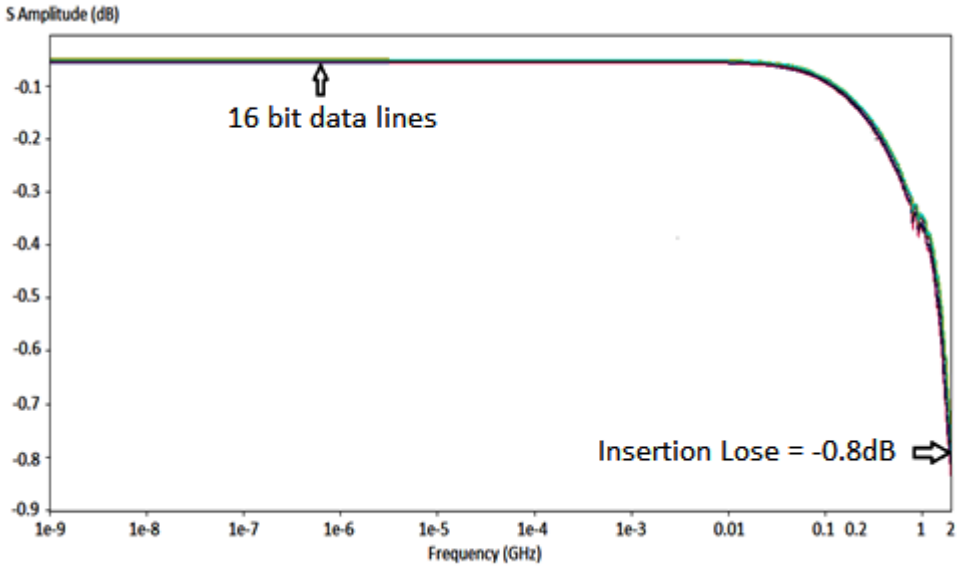


Figure 6.21: Insertion loss of 16 bit data lines, for standard 6-layer board, -0.8 dB at 2 Gbps.

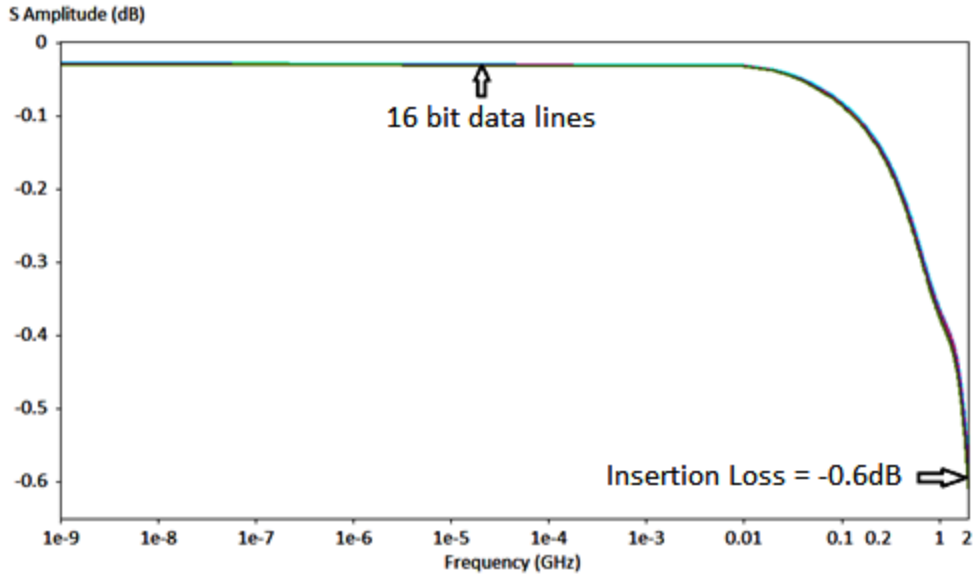


Figure 6.22: Insertion loss of 16 bit data lines, for proposed structure board, -0.6dB at 2 Gbps.

6.12 Test Structures and Simulation Results

Two test structures, 6-layered standard and proposed boards, were manufactured as shown in Fig. 6.23(a). The standard board had multiple via transitions and used thick core between plane layers. Capacitor pads were provided at each via transition so as to reduce PDN impedance if capacitors are placed directly on the power pins of the devices**.** The proposed structure board also

had multiple via transitions and used thin core between planes layers. Figure 6.23(b) shows the real measurement result for both the boards. In real measurement, two high speed interfaces were active, double data rate 3 and high-definition multimedia interface. The simultaneous switching noise was introduced in the board through via and signal interconnect coupling. It was determined from the measurement results, in the proposed board signal quality was good with minimal ringing and without any overshoot or undershoot. The standard board produced ringing, overshoot, and undershoot problems. In addition, the signal wave shape on the standard board was degraded.

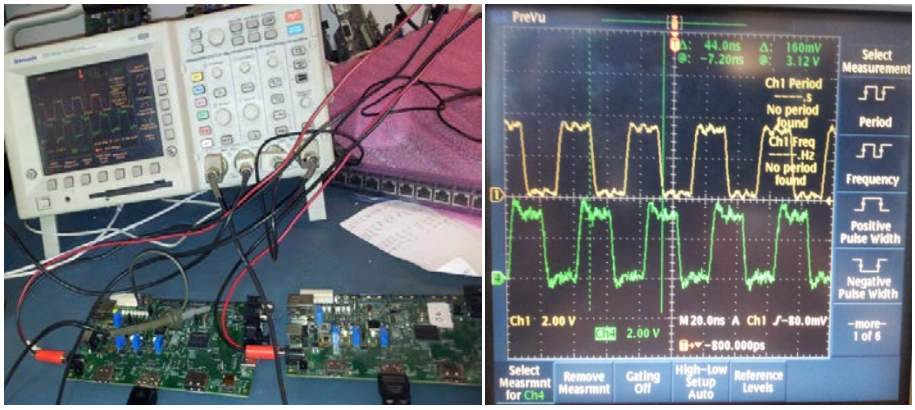


Figure 6.23(a): Real Meaurement setup for standard and proposed boards (b) compare the waveshape.

S-parameters of the proposed structure and standard board were simulated using the System SI tool. These S-parameter were used in the test bench setup in the System SI tool. The eye patterns which are used to discuss the signal quality in high-speed circuits at the output side were simulated by using random 16-bit pattern in System SI. The input data signal was 2.133 Gbps. The simulated signal eye patterns for integrated capacitor and conventional structure are shown in Figure 6.24 and Figure 6.25.

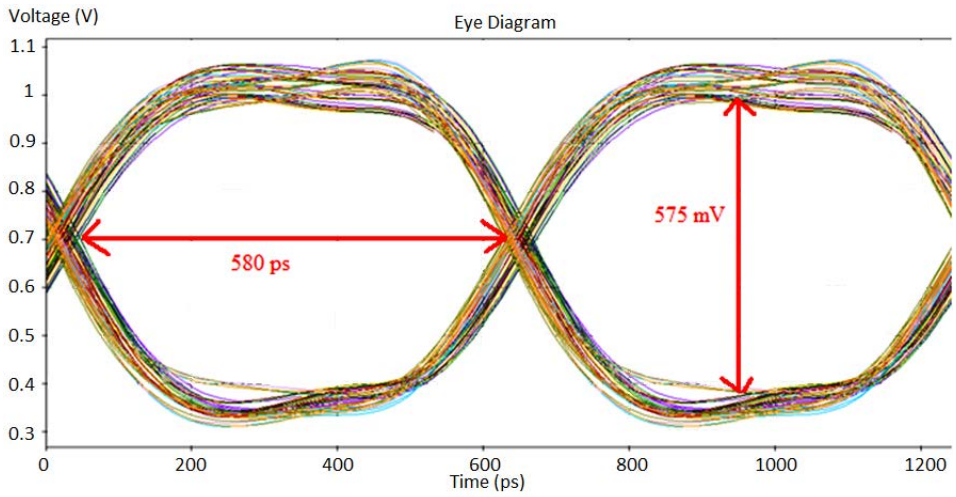


Figure 6.24: The simulation results of eye pattern of 16-bit data lines for the proposed structure board at data rate 2.133 Gbps.

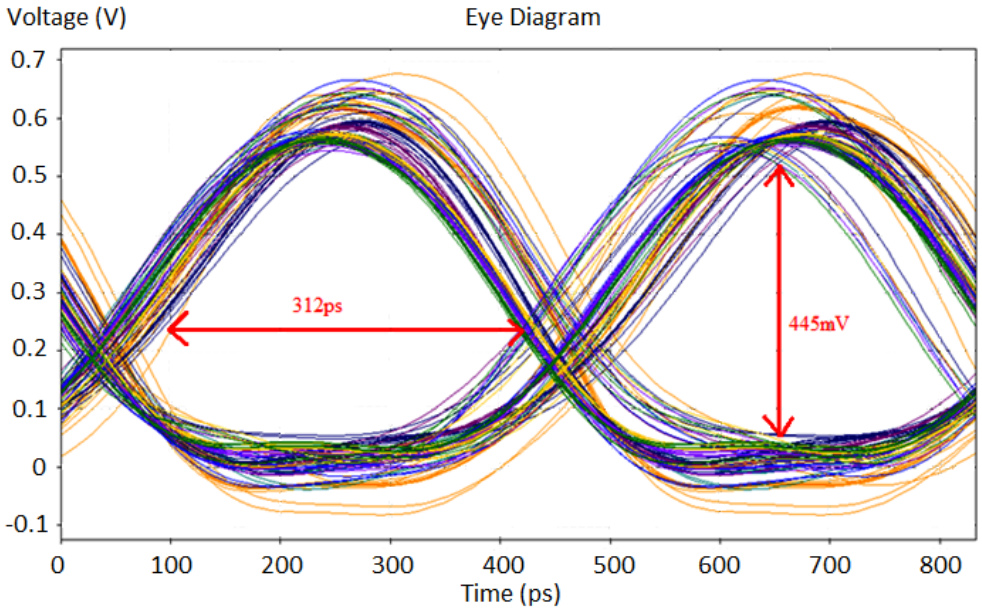


Figure 6.25: The simulation result of eye pattern of 16-bit data lines for the standard six layer board at data rate 2.133 Gbps.

It was observed that for the reference board, the maximum eye open was 445 mV and the maximum eye width was 312 ps. In the proposed method, the maximum eye open was 575 mV and the maximum eye width was 580 ps. The eye pattern of the proposed method was much better than the reference board. Figure 6.26 and Figure 6.27 shows measured eye pattern results for both the structures. Real measurement and simulation eye pattern results are similar to each

other. The eye pattern height and width are improved in the proposed method compared to the reference board. The jitter, which increased in the standard board, improved in the proposed board.

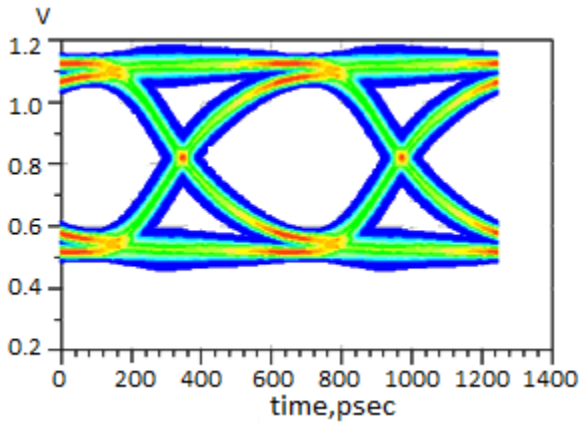


Figure 6.26: The measured results of eye pattern of 16-bit data lines for the proposed structure with small jitter, and more eye opening at data rate 2.133 Gbps.

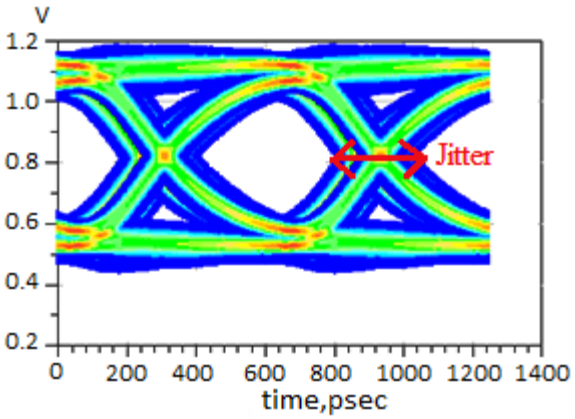


Figure 6.27: The measured results of eye pattern of 16-bit data lines for the reference board with high jitter and less eye opening at data rate 2.133 Gbps.

6.13 Summary

This thesis proposes that power supply distribution network noise caused by simultaneous switching noise at PCB level can be controlled effectively by integrated capacitors between the power planes at data speed 2.133 Gbps. The simulated result of the proposed structure board also shows that the S- parameter of the transmission line are further improved by 5dB and the insertion loss is improved by 0.2dB at the operating frequency. In addition, the SI performance such as overshoot, undershoot and eye opening of signals of the proposed structure is better than the conventional structure board. The proposed method also enables minimizing the simultaneous switching noise effect, which is verified by comparing the simulated results and measured parameters such as noise and eye diagram of the high-speed signals. The decoupling capacitors, integrated into the dielectric substrate can provide high capacitance at low cost and is very effective in reducing the simultaneous switching noise effect on the signal eye quality tests.

CHAPTER 7

CONCLUSIONS AND FUTURE WORK

7.0 Conclusions

This research work is focused on a novel method for improving the EMC for medical instrumentation. On the design side, four methods were developed and simulation results were compared with measurement results. These four novels methods can also be used for other high-speed applications such as aircraft, military, telecommunication, automotive, mobile/ smart phones, IOT and so on. The research work used both measurement and simulation techniques to correlate the results. Conclusions of this research work can be summarized as below.

1. In chapter 3, a routing method is proposed which is based on rotating the angle of transmission line on PCB to minimize the fiber weave effect on intra-pair skew in high-speed differential signaling. The research points to methods that identify and characterize skew to ensure a robust design. The fiber weave effect must be comprehended and properly accounted for in future high speed bus designs by using a routing angle of 10^0 for traces on PCB (only for high speed signals). Table 3.5 shows when the fiber weave effect requires special accommodations to alleviate its effects and when it can be ignored.

2. In chapter 4, impedance control method is proposed to minimize the split plane effect during the crossing of split planes by high speed signals. The proposed impedance control method minimizes the degradation of the received output signal of the transmission line and improves return loss up to 5dB and insertion loss up to 0.2dB while crossing the split gap. The method also reduces overshoot and undershoot at the receiver side as shown in Figure 4.17(a) and 4.17(b). Return-current path induced loop inductance, which increases the radiation of the signal, can be controlled by increasing the track width. The proposed method along with mounting de-caps between split planes on PCB is very effective to minimize split plane effect during the crossing of split planes by the signals. Simulation results confirm that track impedance matches during the crossing of split gap with rest of the constant impedance transmission line and reduces the reflection of signals.

3. In chapter 5, another method is proposed to improve the EMC by using interplane capacitance in the PCB. The interplane capacitors reduce the noise of the board-level power distribution system and improve the signal integrity of the high-speed signals, even for frequencies higher than 1GHz. Results show harmonic reduction rate of 15 dB to 25 dB for thin (2 mil) core between plane layers. In comparison, harmonic reduction rate of 5 dB to 28 dB at different frequencies can be achieved using two sets of power plane layers. By minimizing the board resonances using decoupling capacitors and a proper power and ground plane design reduce radiated emissions that cause EMI in PCB. The results in table 5.1 show that EMC of any medical system is further improved by using two sets of power and ground plane layers in a multilayer PCB.

4. In chapter 6, finally, the research proposes using integrated capacitors between the power planes at data speed 2.133 Gbps to control simultaneous switching noise at printed circuit board level. As confirmed by simulated results, the S- parameter of the transmission line is further improved by 5 dB and the insertion loss is improved by 0.2 dB at the operating frequency. The proposed method has an advantage over the conventional structure in SI performance in addition to cost benefits and reduction of simultaneous switching noise effect on the signal eye quality.

7.1 Recommendations for Future Work

The following research work may be pursued further:

1. Power Integrity is also a major cause of failure of any circuit. Signal integrity (SI) analysis allows visibility of how signals are going to behave as they traverse PCB traces, vias, connectors, passive components, etc. In high-speed digital circuit, supplying a clear power to the integrated circuit and managing the coupling of power noise which can cause fluctuations or disturbances in the power distribution system have become the bottleneck of high-speed digital circuit designs. So it is expected to be a challenging problem for the power integrity (PI) design due to the wider bandwidth of the noise. Keeping the power distribution network (PDN) impedance very low in a wide frequency range and reducing simultaneous switching noise (SSN) are priority for any power integrity (PI) design. This research work can be further enhanced to investigate both in

time and frequency domains the power integrity with the help of full-wave finite-element simulations.

2. Further PCB domain today has literally evolved to rigid flex PCB. The use of rigid flex PCB is increasing in medical products. Therefore, there is lot of scope of research to investigate the signal integrity issues in rigid board.
3. This research can be augmented to investigate the shielding technique on PCB. Shielding forms a conductive barrier enveloping an electrical circuit to provide isolation and prevent the EMI from “leaking” out. Once the PCB design has been optimized for minimal emissions, the next stage of the design process is to shield critical sections of the board to prevent emissions, or prevent emissions from other portions of the system from affecting sensitive circuits. Research can be done to find the effective shielding techniques to select or complete shielding on PCB.

7.2 Papers Published

1. The following publications are a result of this work:

7.2.1 Journal Publications

1. Singh Surender; Agarwal Ravinder and Singh V. R.; Using Impedance Control Method to Achieve Signal Integrity in Biomedical Equipment. Instrumentation Science & Technology (Taylor & Francis). 2012, 40 (6), 476–489.

2. Singh Surender; Agarwal Ravinder and Singh V. R.; Simultaneous Switching Noise Enabler in High Speed Biomedical System by Integrated Plane Coupling. Instrumentation Science & Technology (Taylor & Francis). 2015, 43 (5), 497–510.
3. Singh Surender; Agarwal Ravinder and Singh V. R.; Modeling of Power Planes for Improving EMC in High Speed Medical System. International Journal of Engineering Research & Technology. 2015, 4 (2), 628–632.
4. Singh Surender; Agarwal Ravinder and Singh V. R.; Analysis and verification of fiber weave effect on jitter for high speed interconnect in high speed medical system. International Journal of Engineering Research & Technology (Taylor & Francis). 2016(Communicated).

7.2.2 Conference Publications

5. Singh Surender; Agarwal Ravinder and Singh V. R.; An Investigation on the Resistive and Dielectric Losses In High Speed Bio Medical PCBs. National Conference on Latest Trends in Neural Networks and Digital Signal Processing, 26th March, 2010, GCET, Greater Noida
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